SILICON-TUNGSTEN SAMPLING ELECTROMAGNETIC CALORIMETER FOR THE TEV ELECTRON-POSITRON LINEAR COLLIDER

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A high granularity 3D calorimeter providing a detailed picture of the shower, adequate for efficient pattern recognition and needed energy resolution is mandatory for exploiting the discovery potential of the planned e^+e^- linear collider. For the electromagnetic calorimeter, the CALICE collaboration proposes a highly granular tungsten-silicon sampling calorimeter. The silicon device is made of PIN diode matrices with readout pads of 1x1 cm^2. Such a calorimeter suits perfectly the energy flow measurements and enables a detailed event reconstruction. Prototype in construction is described and first measurements with source or cosmic is presented. Schedule of the next years R&D is also given.

1. Introduction

At the future e+e− linear collider, the detector must be able to perform very efficient particle Flow reconstruction. One of the ways to perform it consists in instrumenting calorimeters with a high degree of tracking capabilities, which enable a reliable track-shower association and energy identification. To optimize the track-shower association, both the electromagnetic (ECAL) and hadronic (HCAL) calorimeter must be put inside the coil, like it is shown in figure 1, avoiding any blind region in the middle of the shower development. Therefore, the available space for both calorimeters is given by the internal radius of the coil and a compact ECAL is mandatory to have enough interaction length for the HCAL. In addition, it has been shown that a "tracking calorimeter" could be the right choice to optimize the performance of the pattern recognition, since it produces a 3D view of the shower development inside the calorimeter. Such a calorimeter must have a large segmentation with small readout pad size and a good shower to shower separation, i.e. a small Molière radius but also a small hadronic shower spatial dispersion. Basic construction units of the electromagnetic calorimeter are modules, mechanical stiffness of which is ensured by a carbon fiber skeleton, minimizing the dead region.

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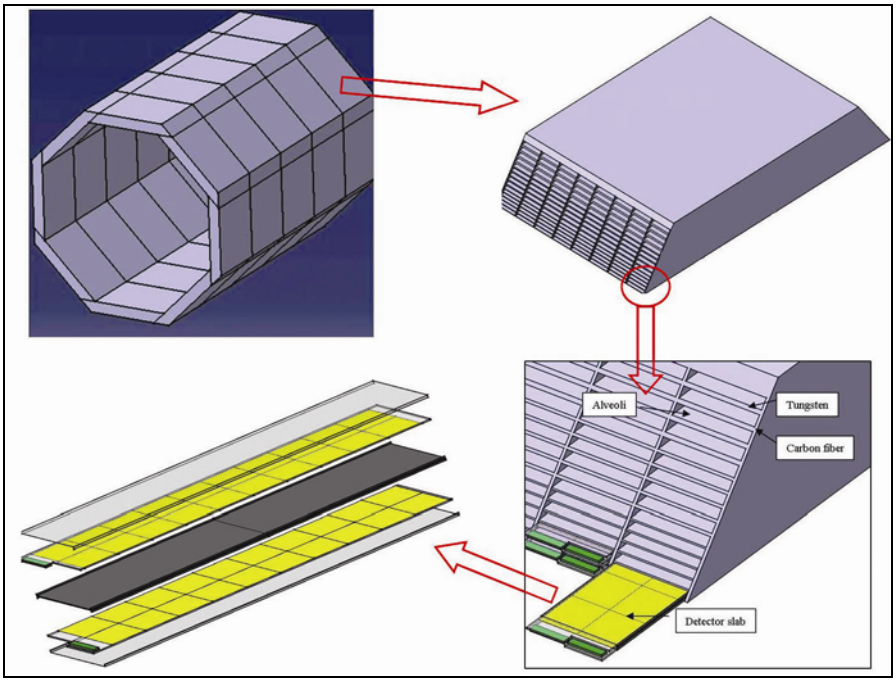

Figure 1: Cross section of the barrel part of the detection system (top left) and basic construction elements of the electromagnetic calorimeter, with at the end (bottom left) the basic detector element, called detector slab.

2. Electromagnetic calorimeter concept

All these considerations led to choose high density and Z number material for the radiator going naturally for the tungsten, which has a Molière radius r_M of 9mm and a radiation length (X_0) of 3.5 mm. For the active part of the device, silicon PIN diodes seem perfect but their cost. The individual e.m. energy resolution needed and the future cost evolution will drive the area of silicon and therefore the number of layers. Many studies have been done with 40 layers, as given in the TESLA TDR [1], while a prototype under construction will have only 30 layers. The pad size comes from a compromise between the density of extraction lines of the readout, the electronics cost together with a pad size not much larger than the Molière radius. For the studies as well as for the device in construction, a pad size of $1x1cm^2$ has been adopted.

The basic detection units are detector slabs (Fig. 2) which consist in a stiffening H-structure from carbon fiber material embedding a tungsten sheet and overlaid

by silicon pad sensors. The entire slab is shielded by an aluminum envelope and is slit into the module.

As it is shown in fig.2, for the final project, one of the possible geometrical designs locate the VFE chip inside the detector. That will be possible only if the power dissipation is not too high, if the duty cycle could reduce it efficiently and/or a cooling system could be designed for such a thin device, and if a 500 GeV e.m. shower crossing the VFE chip would not disturb it too strongly. All these points are part of the CALICE R&D program. Insuring the behavior of the ECAL prototype in the test beam, for the prototype, the VFE chip are located outside, on the external part of the PCB.

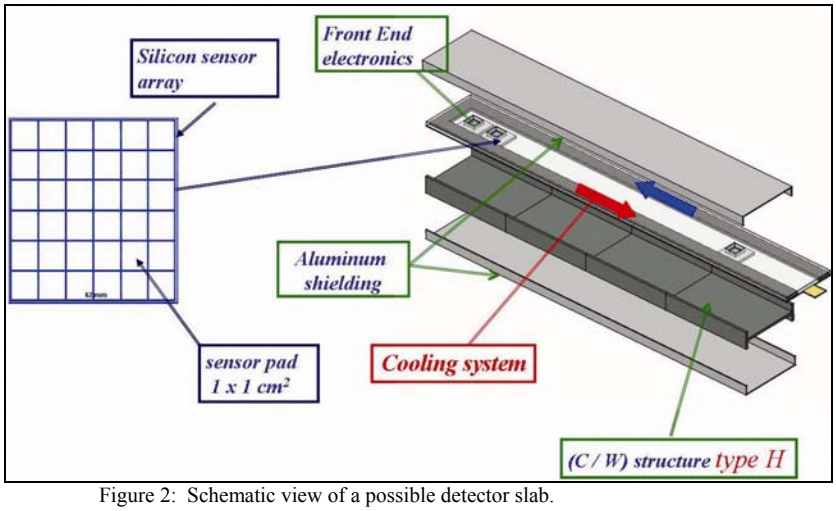

Figure 2: Schematic view of a possible detector slab.

3. Current status of the project

The CALICE project has been proposed to the DESY "Physics Review Committee" which approved it as PRC 02-01. The agenda of the project concerns also the construction of a prototype, with test beam at the end of 2004 with low energy electron, and high energy hadrons and electrons in the year 2005-2006. The test with hadrons beam is foreseen to be done together with the different HCAL options of CALICE. Today, the options are namely the analogical HCAL based on scintillator tile with stainless steel for radiator, and the so-called digital HCAL, where the readout of the active device works in binary mode, i.e. yes/no (1bit). In this later case, the number of pads hits is, following the GEANT4 simulation, linear with the incoming hadron energy. Similar behaviour is foreseen with the ECAL, but with a strong saturation effect for energies higher than about 1 to 2 GeV.

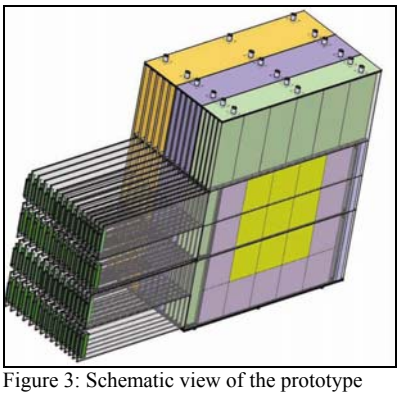

Figure 3: Schematic view of the prototype

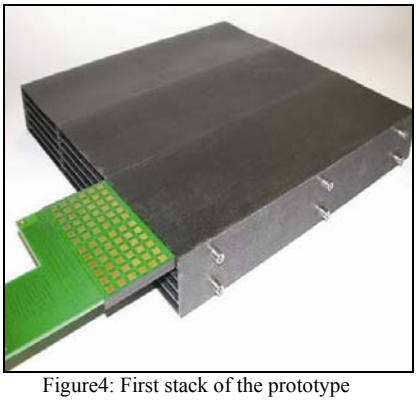

Figure4: First stack of the prototype

4. First results with simulation

4.1 General description

The ECAL prototype mimics the final project with tungsten wrapped in carbon fiber, with 30 layers and a pad size of 1x1cm^2 but the very front end (VFE) electronics is located outside the device, on the same PCB on which the silicon wafers are glued. The schematic view of the prototype is shown on fig. 3, with different color for the three stacks, each one with different tungsten thickness. This choice ensures a good resolution at low energy, due to the tin tungsten in the first stack, and a good containment of the e.m. shower due to a tungsten thickness 3 times larger in the third stack. The overall thickness is about 20 cm or 24X0. The structure is realized by carbon fiber wrapping half of the tungsten sheet, leaving free space between each tungsten sheet, called alveoli. In these free spaces, detector slabs are slit. The LLR group has already produced the first stack structure as it is shown in Fig.4. The detector slab consists of 2 active readout layers and one tungsten sheet. The active layer is made of PCB 14 layers (2.1mm) and 500 microns high resistivity silicon wafers. The PCB has been designed at LAL and the production will be made in Korea under the control of KNU.
The wafers have been processed in Russia at MSU and a production will soon begin in Prague under control of IOP-ASCR and Charles University.

4.2 The active device

The wafers are cut in matrices of 62x62 mm with 36 pads, while the space reserved for the guard ring is about 1mm. It must be noted that there is only one set of guard ring per matrix. The first batch of the production, made in Russia, managed by the MSU group, is of very high quality, with a typical leakage current less than few nA/pad for all the pads, but for few per cent of the production,

where 1 or 2 pads among the 36 of a matrix goes up to 20 nA/pad. The matrix will work in overdepleted mode around 250V. The connection to the PCB is realized by conductive glue for each pad, with an AC coupling mode of for the readout. For the final project, it is considered to use amorphous silicon deposited directly on the pad, to make the resistance and capacitance. It is the object of an R&D program inside the CALICE-ECAL groups. For the prototype, the AC coupling is realized using discrete components put directly on the PCB, before the amplification in the VFE chip.

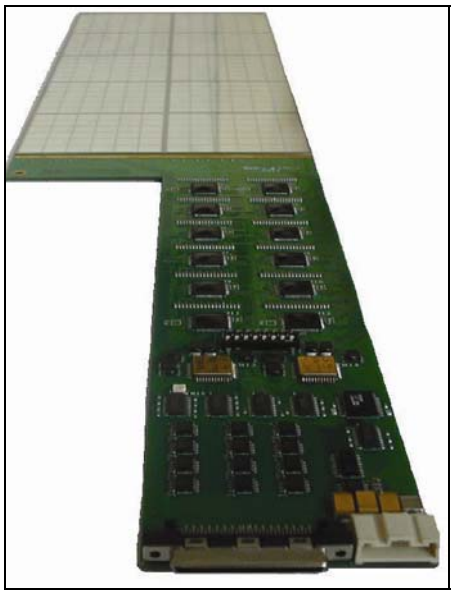

Figure 5: PCB equipped with silicon matrices and VFE chip

4.3 The very front end electronics

The PIN diodes are read by a VFE chip developed by the LAL-Orsay group. It consists in a preamplifier with two gains, a shaper and a multiplexer. This chip treats 18 channels, with low noise, high dynamical range. The results are a linearity of 0.2%, a signal uniformity better than 2% and less than 0.2% of cross talk. All of these are measured value over the 600 MIPS of dynamical range. The PCB with the silicon matrix and the VFE on the side is shown on fig. 5. The schematic view of the VFE is presented in fig. 7.

4.4 Assembling and testing

One of the important advantages of the silicium is the response stability with time and temperature. In order to check it, the detector will be calibrated with cosmic muons using a test bench developed at the LLR, before going on real test beam in

DESY at the end of 2004. A dedicated DAQ system has been developed, working on a single PCB, and based on National Instrument PCI board with 32 differential input channels, able to read a single detector slab. The calibration at the m.i.p. level will also be used to intercalibrate the different channels, since the wafer thickness is known only with a tolerance of ±3%, as given by the wafers producers.
Such a variation of thickness could be one of the major components of the constant term of the calorimeter. Taking into account this effect, could improve drastically the energy resolution. Using strontium source, this DAQ has been used to produce the first measurement on a full chain of detection, namely:

Silicon diodes – Conductive glue – PCB – VFE – DAQ

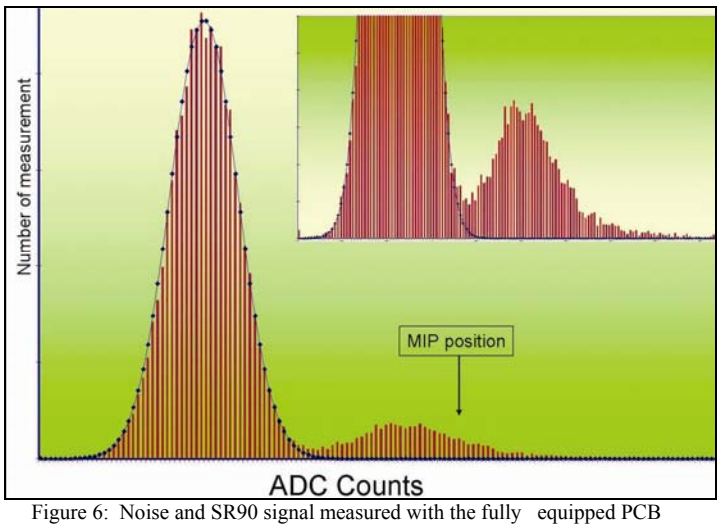

Figure 6: Noise and SR90 signal measured with the fully equipped PCB

This measurement is shown in fig. 6. It shows a total noise at the level of ¼ of a m.i.p. and a m.i.p. signal about at the expected place of 40 000 e-. For the test of the detector slab assembly, and together with the wafer intercalibration, a cosmic test bench has been developed. Four functions are implemented, Scintillators-PM, Trigger, Command generator, and Acquisition. The detection system is made of 2 planes of scintillators read by PM. The trigger is then defined as usual by time coincidence between 2 PM's from two different planes. The generated trigger is put in a NIM format, ready to be used by any DAQ. For the individual detector slab DAQ, it has been decided to use a commercial board from *National Instrum*ent, with

- 32 multiplexed differential channels
- a sampling rate at 1.25 Mb/s per channel
- a dynamical range of 12 bits and an interface PCI 32 bits.

Such a board allows to process individual detector slab in stand alone, for the test and calibration.

The signal generator card is built using a XILINX CPLD, with master clock from the DAQ board, but with possible connexion to an internal clock. The signal transmission is in LVDS, through a TTL translator. Slow control and calibration for each detector slab run under USB. The calibration can be performed in two modes, one in USB, with readout and validation goes through the USB port and one with external validation. The injected value could be done from the ADC output on the DAQ board, or from a totally external node, with the TTL translator.

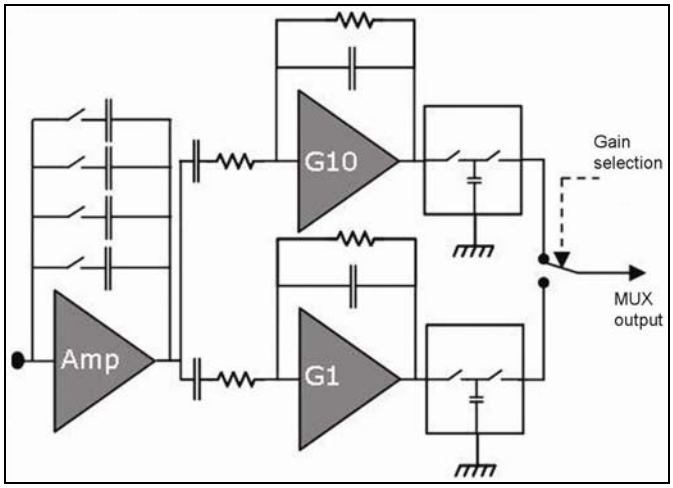

Figure 7: Schematic view of the VFE chip , version 3, for the ECAL prototype

4.5 The DAQ for the prototype

The readout of the full prototype, where there are about 10,000 channels, will be done with a custom designed VME readout board. This has been developed by the UK groups and is based on the CMS tracker readout. The timing, multiplexing and calibration control signals for the VFE board are sent in LVDS by the readout board, with the actual VFE channel outputs being returned as a differential analogue signal. The multiplexed outputs are digitised on the readout card using a 16-bit, 500 kHz ADC, which should allow complete readout from the VFE within 100 μs. The resulting ADC data are buffered on board in an 8 MByte memory, allowing up to 2000 events to be stored before VME access is needed. This should allow an event rate above 1 kHz during a spill with the aim being to achieve an average of more than 100Hz over a run. Two prototype readout boards are under test and the full system of six boards is scheduled for fabrication in summer 2004.

5. First simulation and test

A simulation of the prototype, based on GEANT4, has been developed, using a framework and interface program called MOKKA [3]. First results and tests have been performed, like the dynamical range for electrons up to 50 GeV when starting to about half a m.i.p., the importance of the dead zone between wafers if consecutive layers are not staggered, the first set of physics variables to test, such as lateral dispersion, longitudinal profile, energy resolution, etc..
A new simulation version, with a very precise description of the mechanics and readout
is under development at LLR for the ECAL, at DESY for the tile HCAL and at ANL and NIU for the digital HCAL. It will be release in the first months of 2004.

6. Schedule of the test

At the end of the year 2003, the status of the ECAL prototype is the following:

- Good quality silicon matrices are in production and test at MSU and IOP-Prague. About half of the needed wafers are already produced.
- All the needed tungsten sheets have been produced. The carbon fiber-tungsten structures are in fabrication. The needed tools for assembling is ready at LLR.
- The 14 layer PCB which support the wafers, designed in LAL are now in production in Korea at KNU.
- VFE electronics is under production, after design and test at LAL, LLR
- ADC-DAQ boards will be tested in spring before production in summer 2004 under the control of the involved UK laboratories.
- Preparation for testing with cosmic muons at LLR is in progress for a general test of the prototype.

The first test beam is planned at DESY in the fall of 2004.

7. Conclusion

The CALICE collaboration is preparing actively the ECAL prototype for the test beam foreseen in 2004-2006. A matrix of silicon PIN diodes has been read through conductive glued on a dedicated 14 layers PCB are amplified by VFE custom chip and read by test DAQ. The signal collection is good and the overall ENC is at the level of ¼ of mip. The assembly at LLR-Ecole polytechnique will start in spring 2004 and a cosmic test bench will be used to intercalibrate and test the mounting for individual detector slab. The general DAQ is under development in UK laboratories and the needed VME boards will be produced in summer 2004. A first test beam period is planed for fall 2004 at DESY with low energy electron. The general test beam period is foreseen in 2005-2006, with the two HCAL options of the CALICE collaboration.

Appendix

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