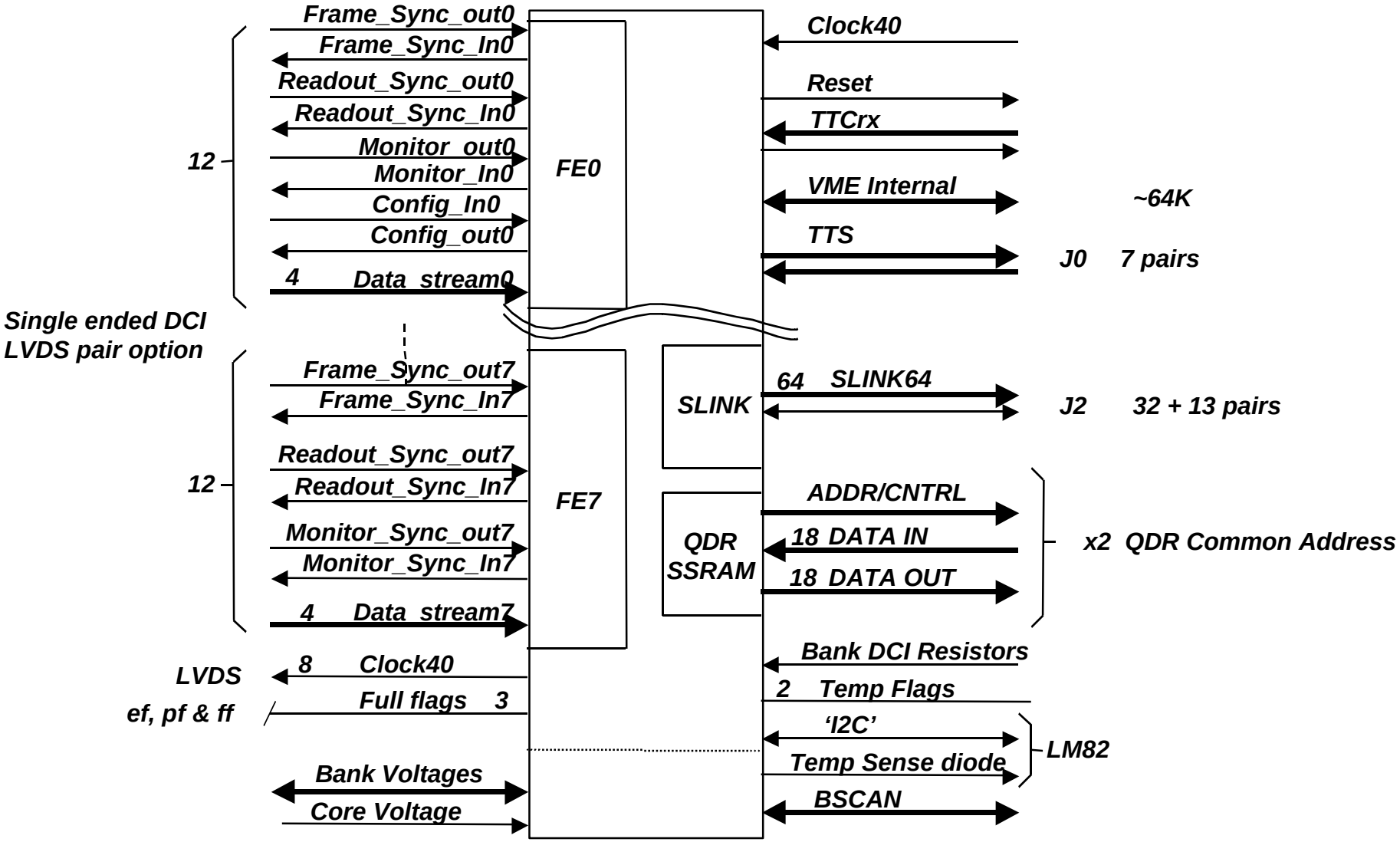
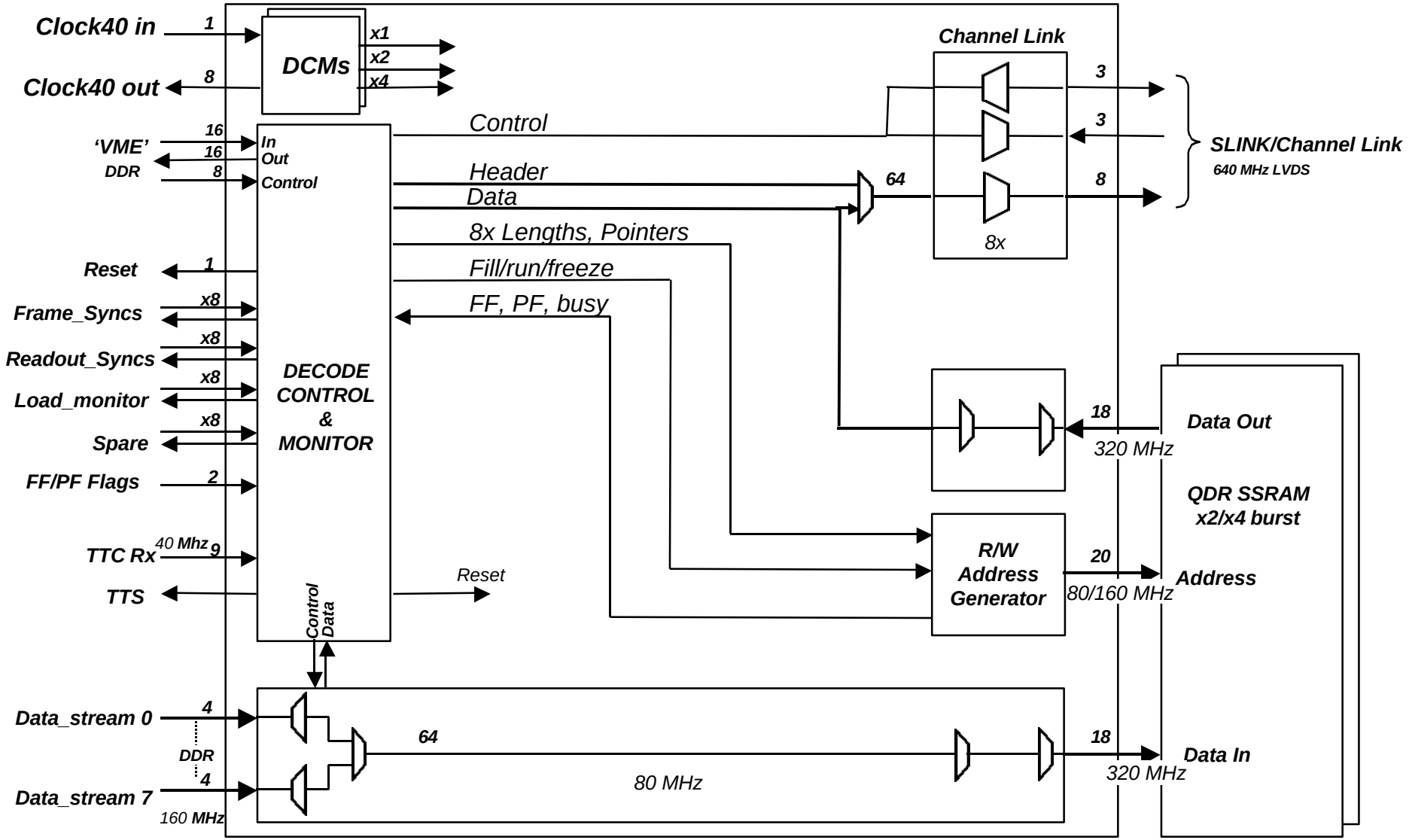
CMS Tracker FED
Back End FPGA

CLRC

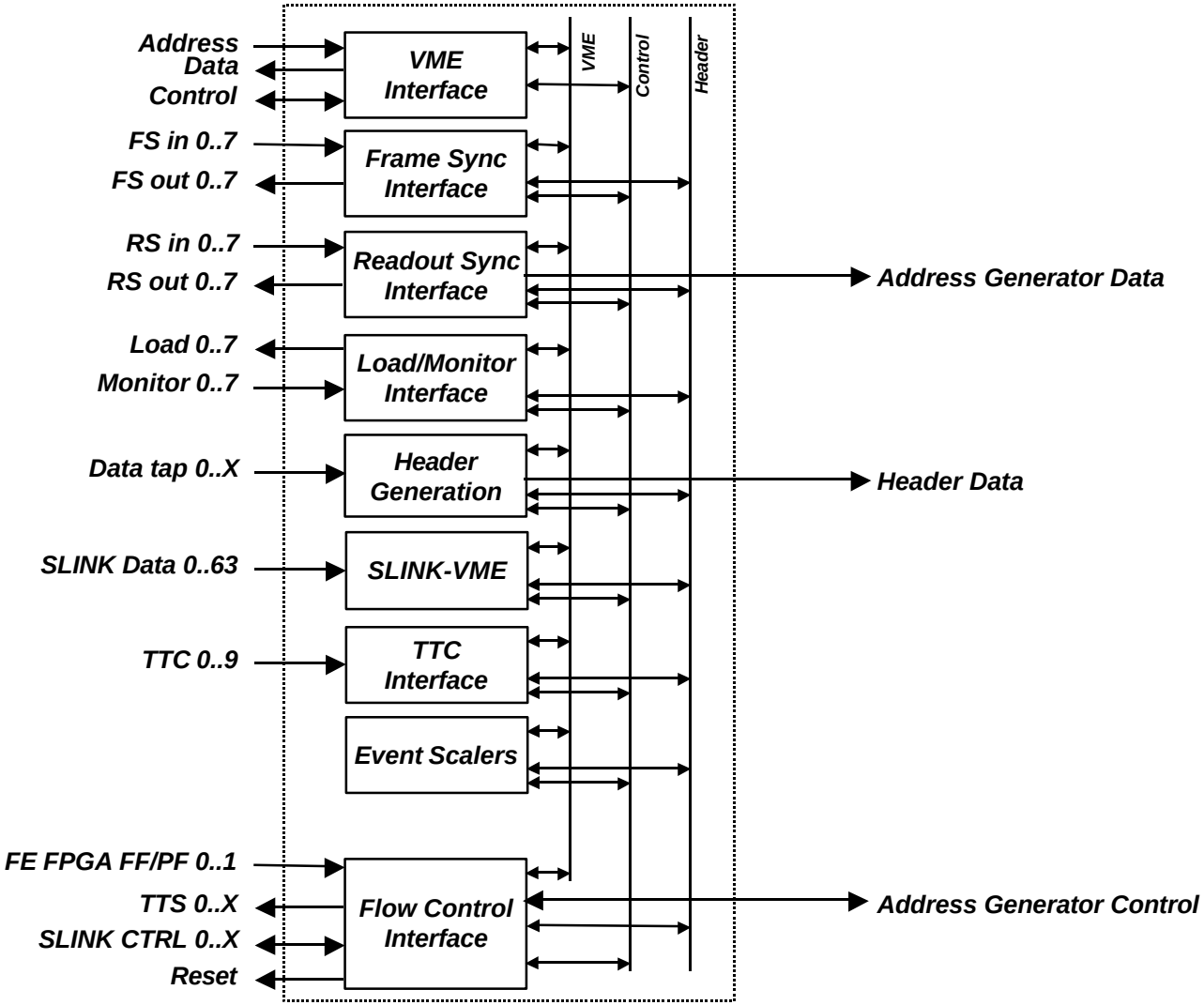


CMS Tracker FED
Back End FPGA

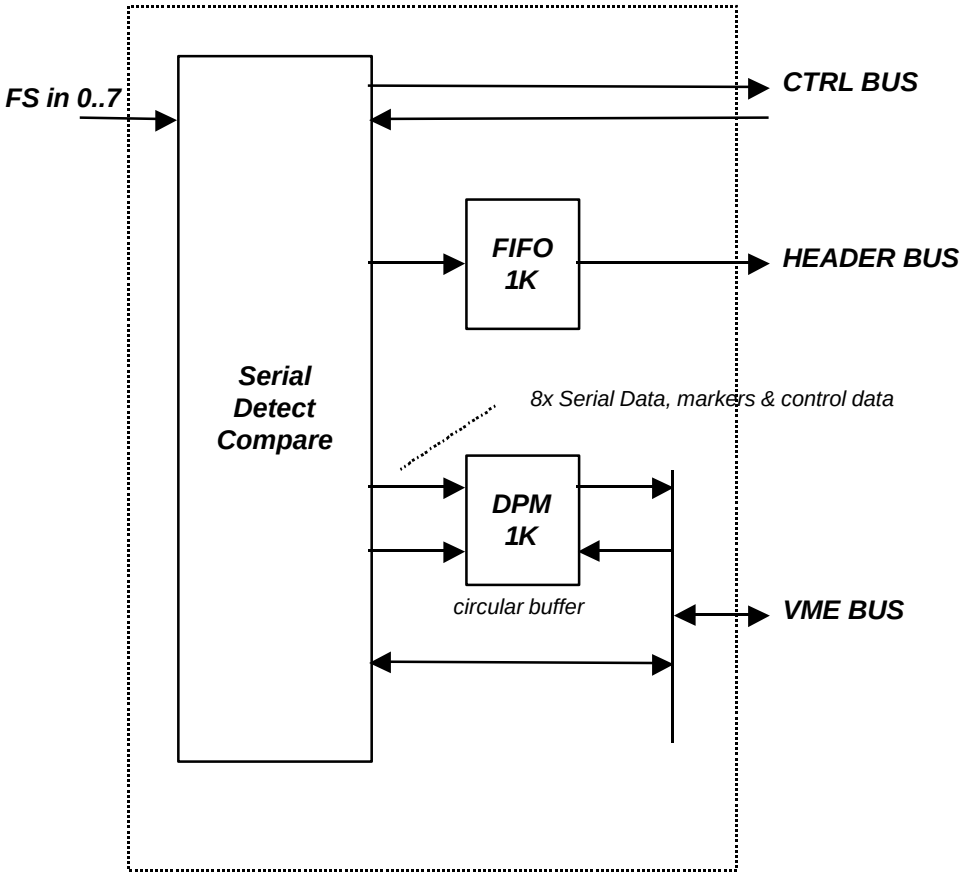
CLRC



Back End Control Block



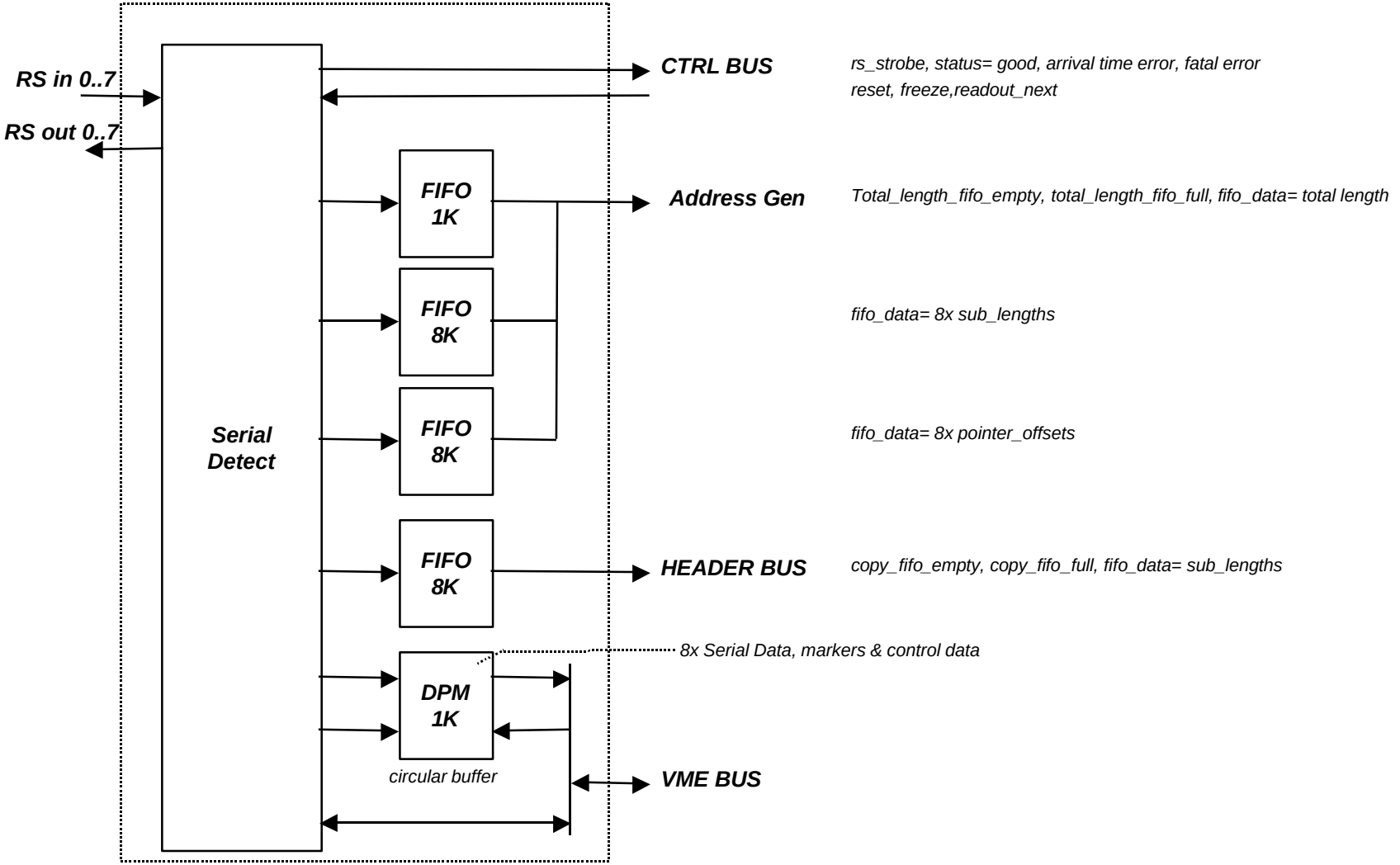
Frame Sync



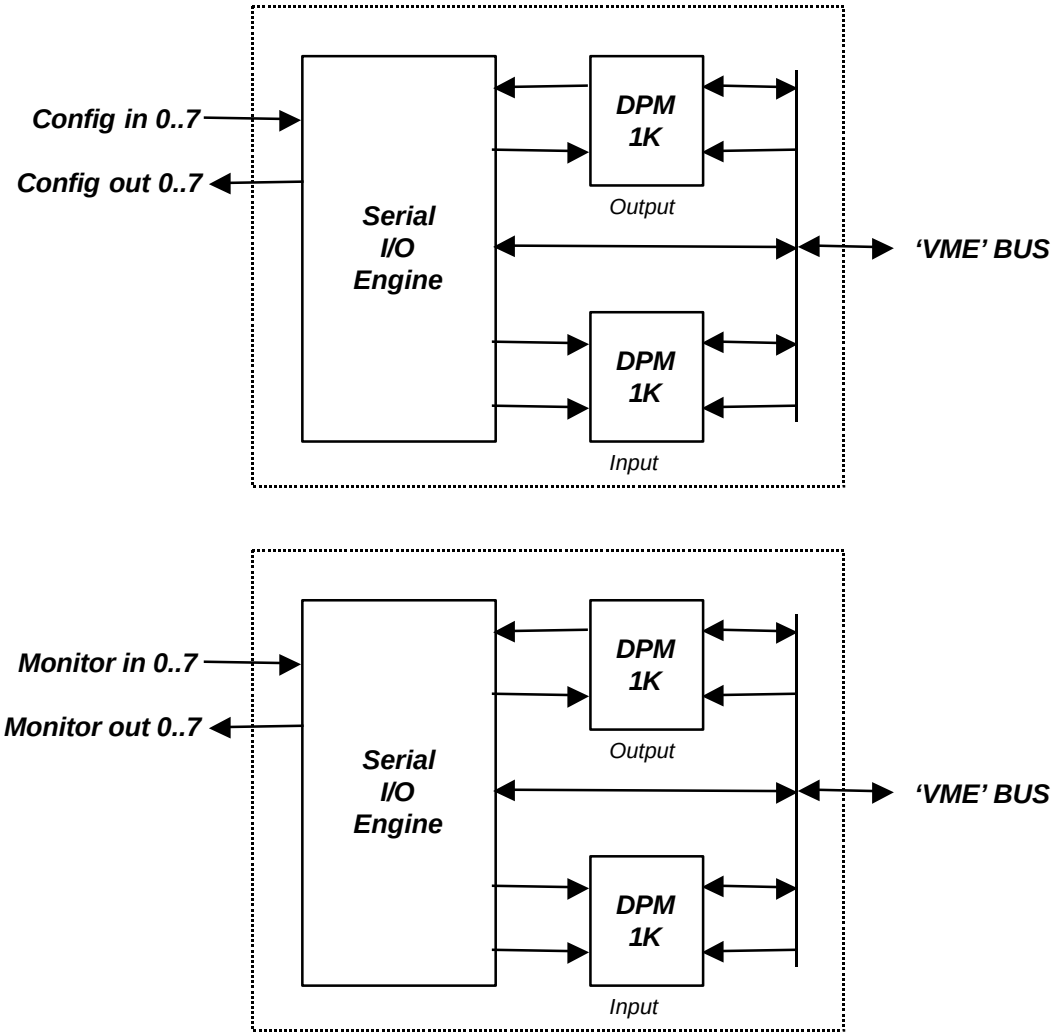
fs_strobe, status= good, some header errors, arrival time error, fatal error reset, freeze

fs_fifo_empty, fs_fifo_full, fifo_data=median header+status

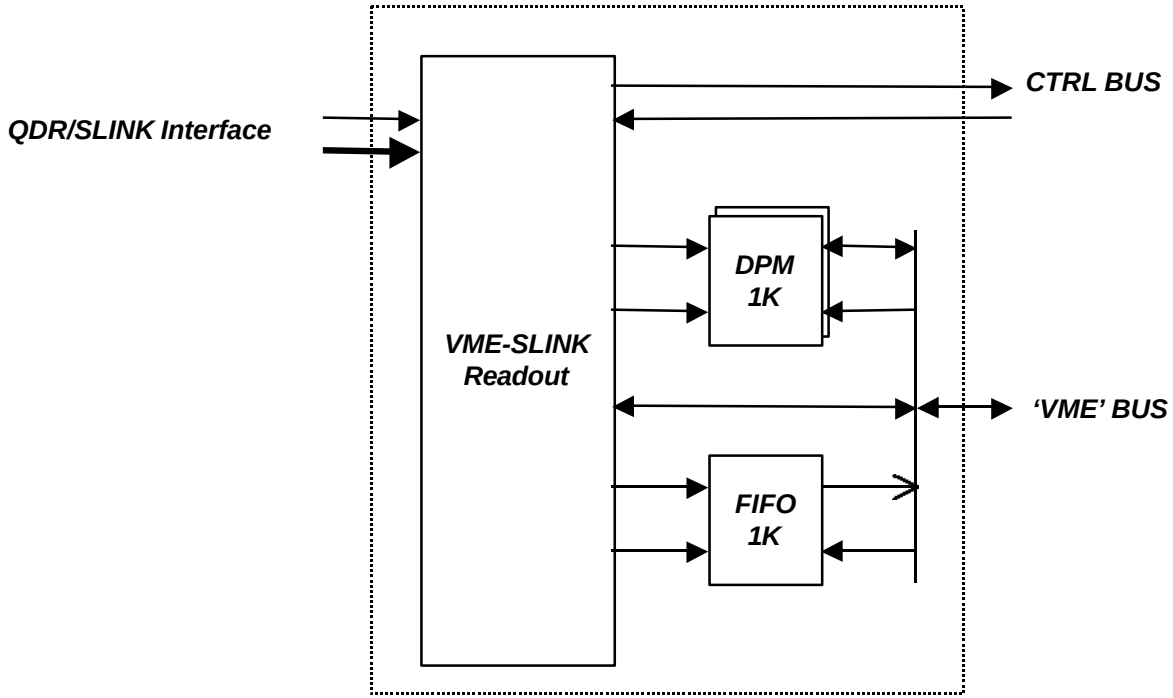
Readout Sync



Load/Monitor

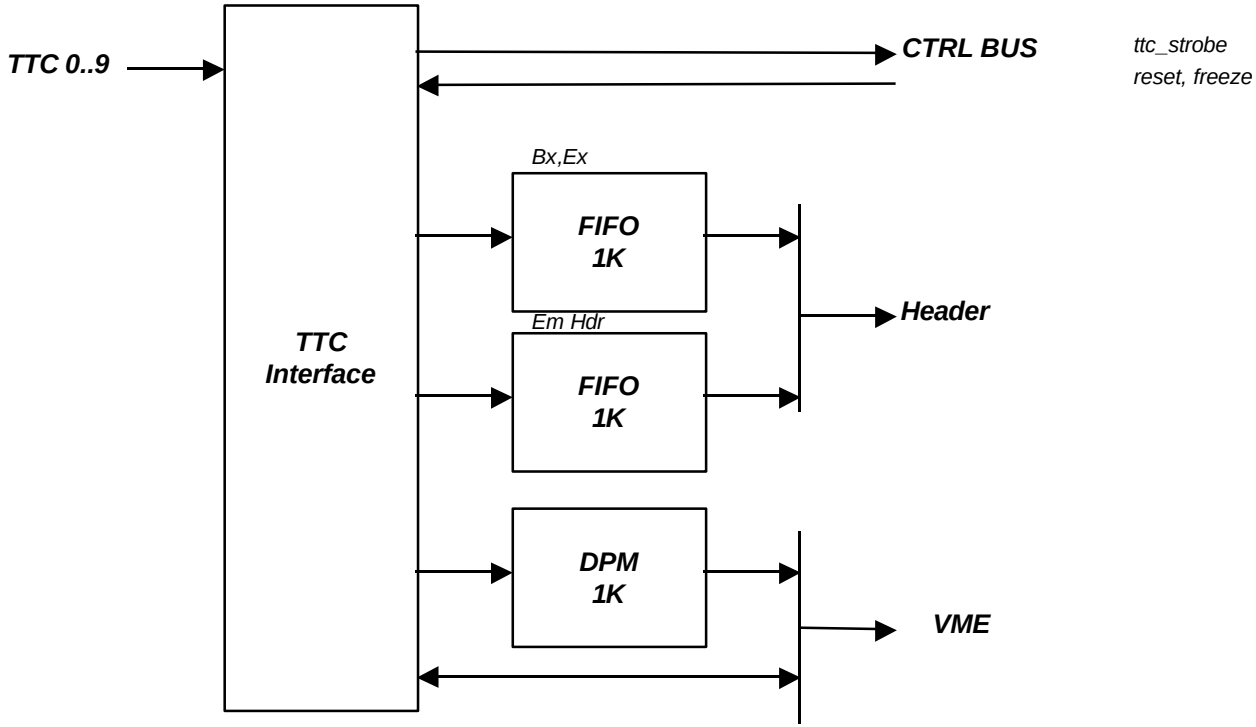


SLINK-VME



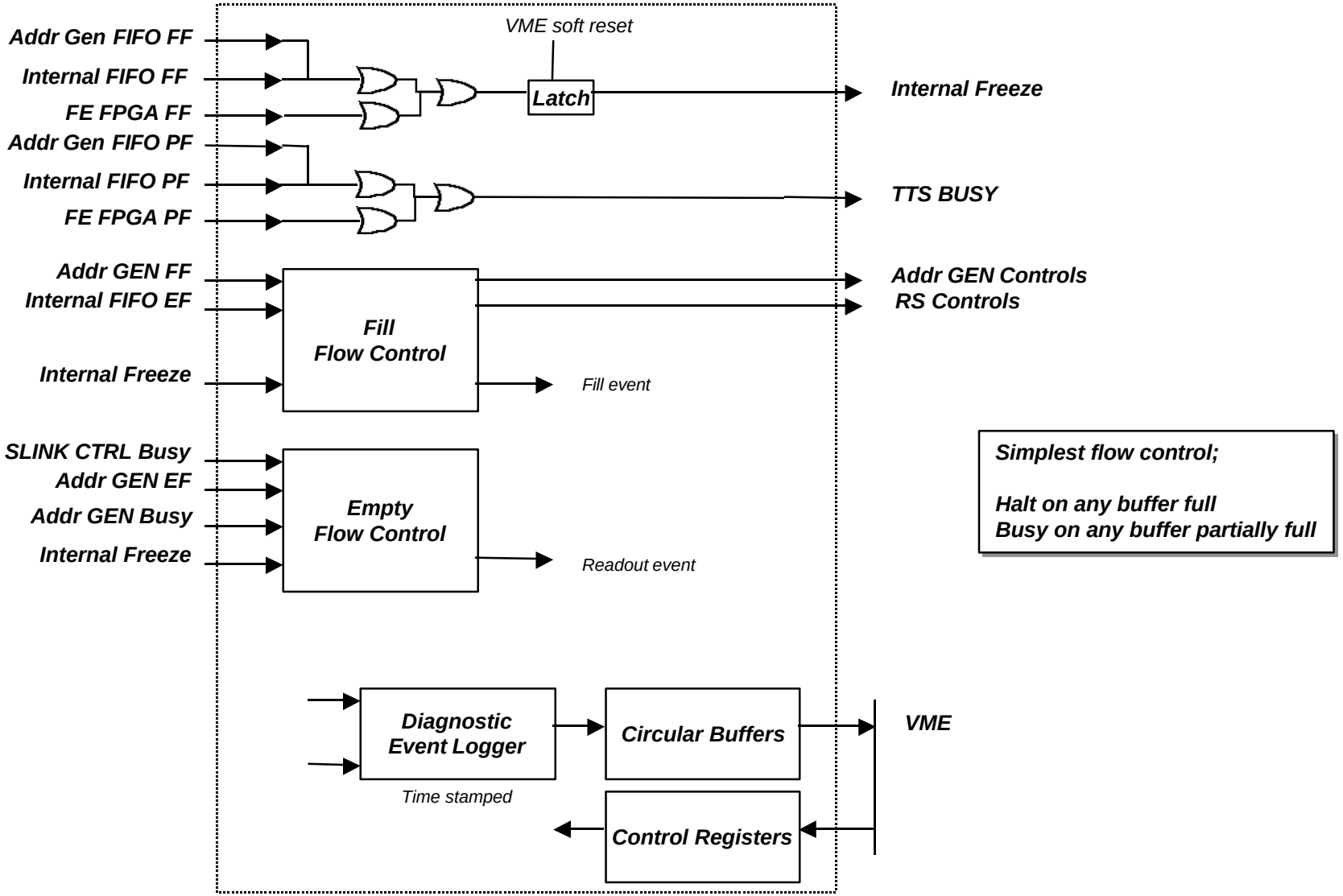
QDR Event Data moved in blocks into DPM
Burst transfer over VME
Wait on software handshake before continuing
Double buffered

TTC Interface



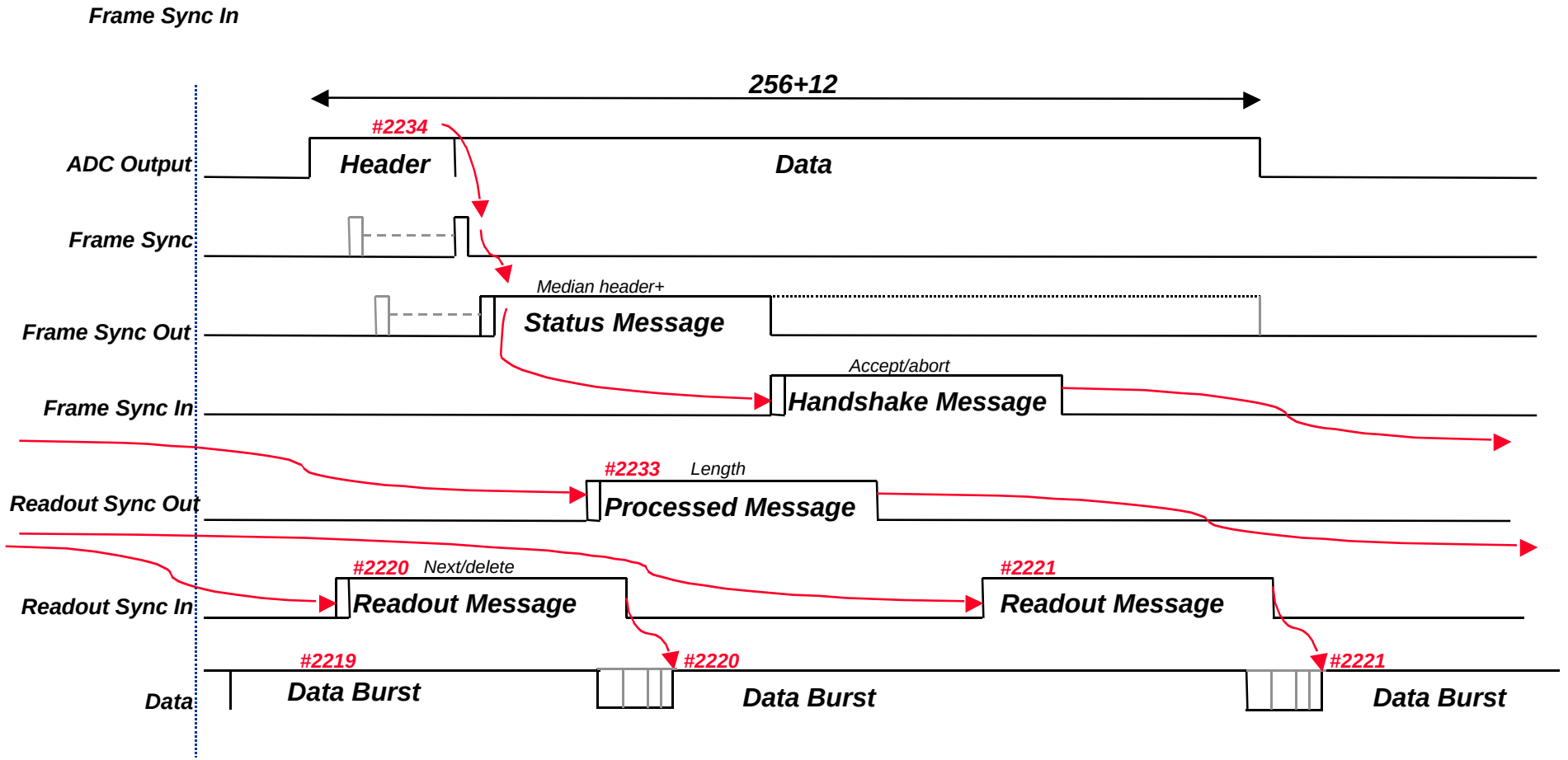
Flow Control core

CLRC



CMS Tracker FED
System Timing

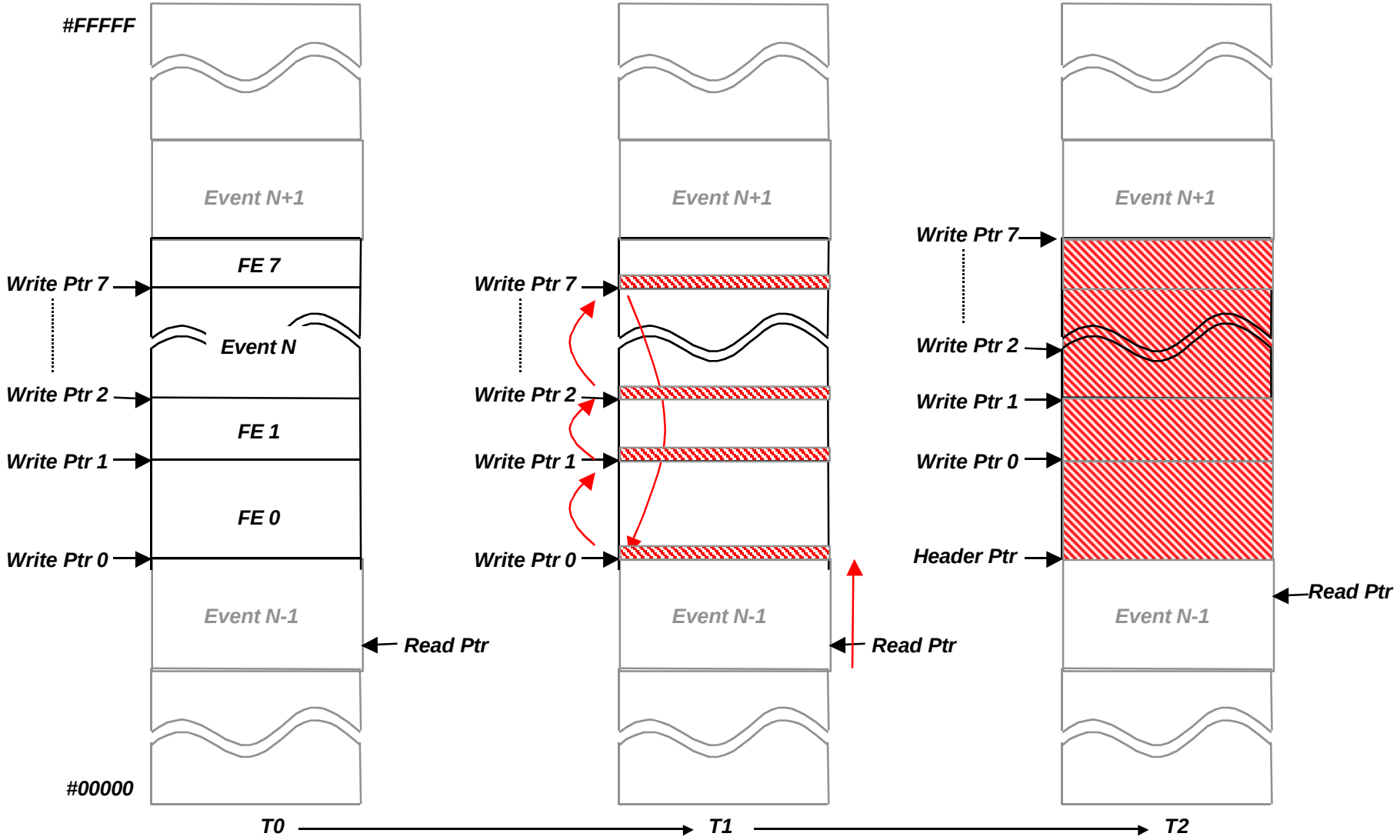
CLRC



NB Frame Sync In - Abort/Accept not used, auto accepts. Readout Sync In - delete not used.

CMS Tracker FED
Back End FPGA

CLRC



CMS Tracker FED - Back End FPGA
Floorplan

CLRC

Die

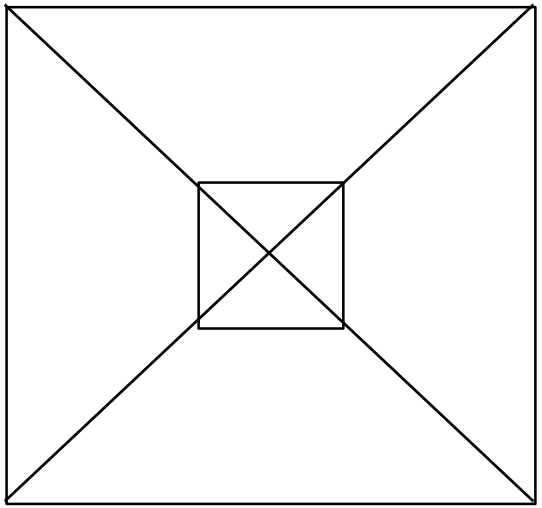
Package

VME

FE_FPGA_Inputs

SLINK

QDR



Same frame 456 & 676 ?

Clocks

XC2V1000FG456 - 324 I/O
XC2V1500FG676 - 396 I/O
XC2V2000FG676 - 456 I/O
XC2V3000FG676 - 484 I/O