HCAL Readout Boards - User Manual

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FEB

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Preliminary

1. Introduction

The HCAL (hadronic calorimeter, [1]) readout boards form the interface between the Tile HCAL particle sensors and the VME based data acquisition (DAQ CRC boards, [2]). Two types of boards will be installed in the final setup: The HCAL Analog Board (HAB) and the HCAL Base Board HBAB (Fig. 1). The HABs contain one front-end ASIC [3] for the readout of 18 silicon photomultipliers (SiPMs) and additional control and calibration electronics. Each HBAB carries in the full assembled configuration 6 HABs, by which 108 detector channels can be read out. Two versions of HBABs will be used for each HCAL layer, corresponding to the ECAL setup 'left-populated and right-populated'. This manual describes the communication of the HBABs with the data acquisition. Connector pin definitions and setup of HBAB and HAB are shown in a more detailed way in Appendix A-C. The schematics of the boards can be found in [4]. Please notice the **safety** information in Section 7 (up to +100V DC bias voltage on the boards).

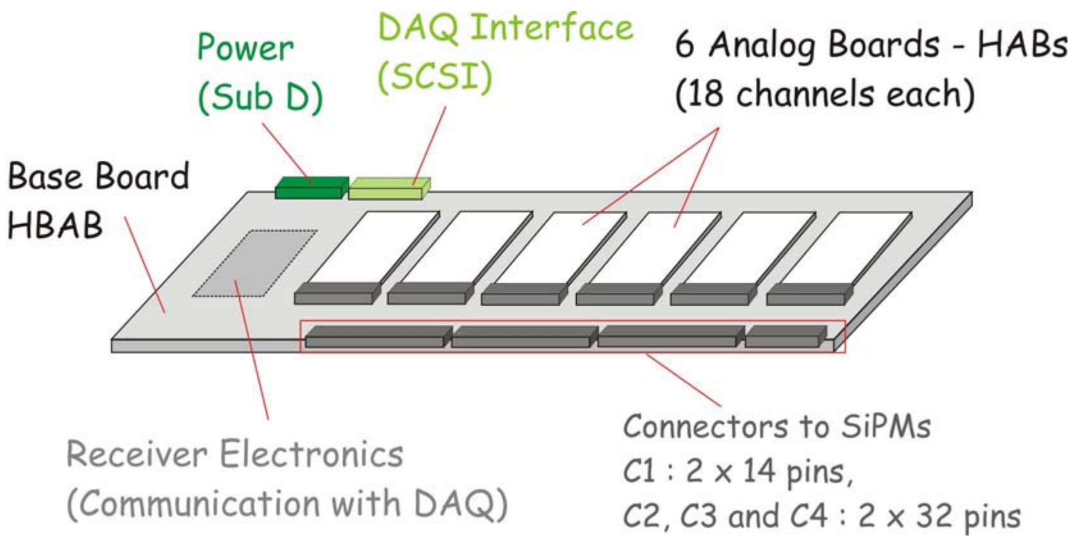


Fig. 1 : The left-populated HCAL Base Board (HBAB) assembled with 6 HCAL Analog Boards (HAB). Each HBAB forms the interface to 108 detector channels via the connectors C1 to C4.

2. Interface to the Data Acquisition (DAQ)

The complete communication of the HBAB with the DAQ is accomplished via the board's SCSI connector. The respective pin and signal definition is shown in Table A1 for the left and right populated versions. The setting of operating parameters (e.g. ASIC gain-, DAC-, filter-settings) is realized by a shift register (SR) on each HAB (c.f. Fig. C2). The SRs of all HABs are connected in series, that means the SR output of HAB n is connected to the SR input of HAB (n+1). The SR output of the last HAB is provided back to the DAQ for a verification of the loading procedure. The SR length is 160 bits (stages) per installed HAB, so 960 bits in total for each HBAB. Additionally to these 960 bits, a logical '1' is sent as first bit of this sequence for verification purposes. The SRs of left- and right-populated boards are programmed separately. The communication of the HBABs with the data acquisition is shown in Fig. 2.

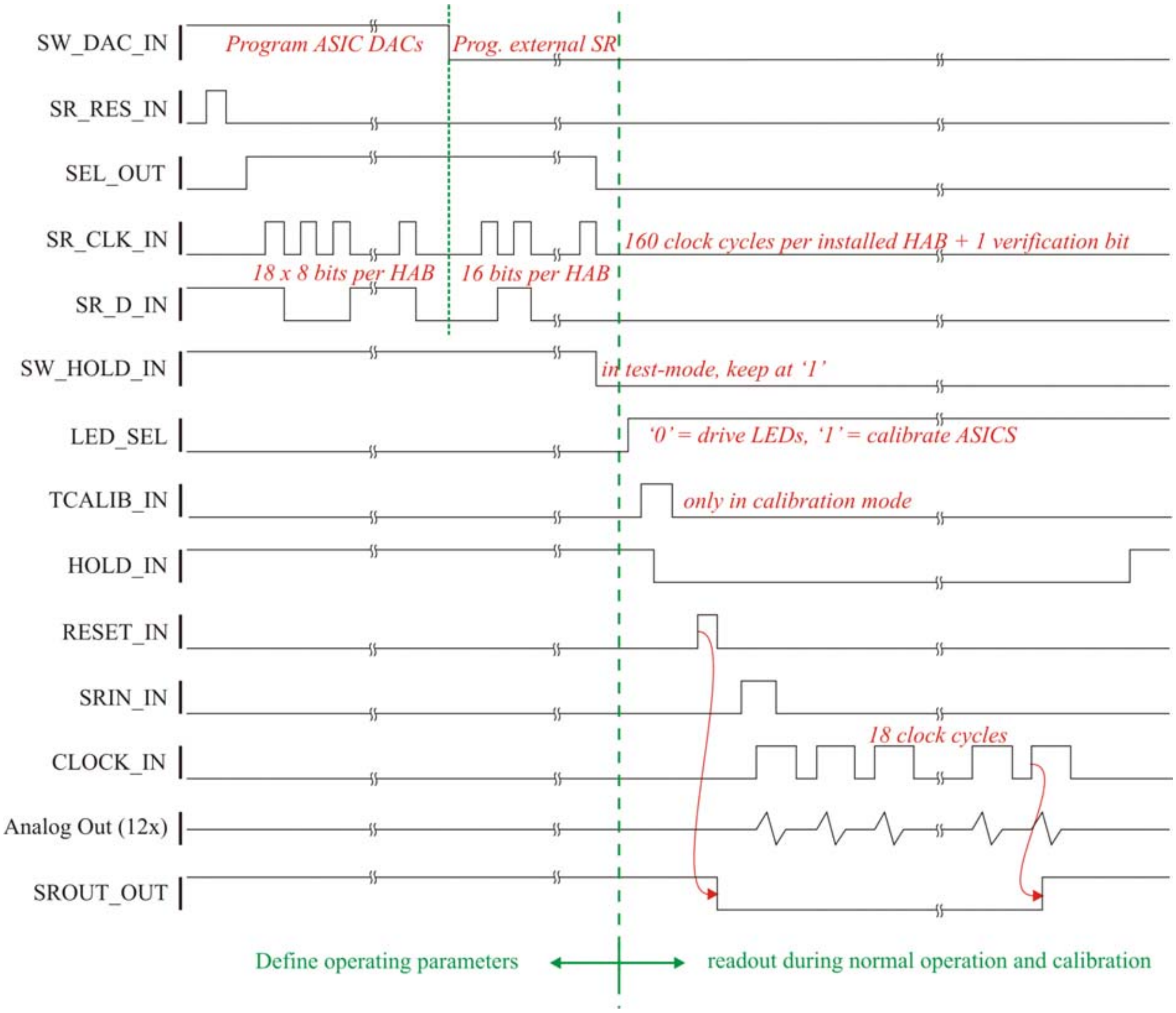


Fig. 2 : Communication of the HBABs with the data acquisition when defining the operating parameters (left), and during normal operation (right).

In the new version of the HAB, the parameter SR is divided into two parts that have to be programmed one after the other (cf. left part of Fig. 2). At first, the ASIC internal DACs have to be programmed. During this first step, the SW_DAC_IN has to be set to '1' in order to connect the ASIC's DAC SR to the CRC boards. Afterwards the ASIC external SR has to be programmed by switching the SW_DAC_IN to '0' and sending the 16 configuration bits per HAB. In both cases, the SRs of all HABs on a base board HBAB are connected in series. By this, the SR length is 864 bits (18x8 bits times 6 HABs) when SW_DAC_IN is '1' and 96 bits (16 bits times 6 HABs) when SW_DAC_IN is '0'. When the SW_DAC_IN is switched from '1' to '0', the SR_CLK_IN must be stable at '0' (cf. Fig. 2, dotted green line).
In the following, the user can switch between physics and calibration mode by reloading the external SR, while the DAC settings remain in their initial state (SW_DAC_IN always '0').

A calibration of the complete readout chain can be realized by an analog DC voltage (VCALIB) and a trigger signal (TCALIB, rising edge). The voltage VCALIB is always present at the CMB input, as soon as it is defined and enabled by the CRC board. The ASIC is not connected to VCALIB without a respective TCALIB trigger.

Except for the analog outputs of the HBABs and the VCALIB signal (both differential signals), all signals are transferred in LVDS logic between HBABs and data acquisition (CRC module), as described in [2].

3. Power and Temperature Monitor Interface

Four different power supply voltages have to be supplied to the HBAB,
VP6 (+6V), VM6 (-6V), HV (+100V max.) and GND via a 9pin Sub D male plug. The respective pin definition can be found in Table A2. Each cable should have a cross section of 1mm² (except for HV).

On pin 6 (HBAB left version) and pin 7 (HBAB right version), the current output of a temperature sensor LM35DM, which is placed close to the ASIC of HAB no. D (cf. Fig. B2), is provided. These outputs should be terminated with 500 Ohm to the local ground close to the temperature analyzing electronics. With 500 Ohm termination the gain is about 25mV/°C.

4. HCAL Testboard

The HCAL testboard is designed to carry a single HCAL Analog Board HAB (18 analog input channels). The testboard configuration corresponds to version 'left-populated' of the HBAB, while only one output will be used (Analog Out 1(+, -)). Except for the LED control, the same communication protocol with the DAQ as for the Base Board HBAB is used. The parameter shift register has a length of 160 bits. On the testboard, the signals VCALIB and TCALIB are provided to the ASIC and the LED board at the same time, while the LED section can be disabled by a manual jumper.
Additionally, the testboard offers ac-coupled, 50 Ohm test-inputs to each analog input of the ASIC for charge injection measurements. If the charge injection inputs are used, the respective jumpers on the testboards have to be closed (cf. Section 6.3).
Do not use the charge injection inputs when the HV bias voltage is applied to the testboard. With applied HV bias voltage, the charge injection jumpers must be removed and the charge injection cables disconnected.

5. Board Tests

All boards will be tested for broken traces and short circuits in the unassembled state by the board's manufacturer. The ASICS will be assembled in a full tested state. A functionality test of all assembled HAB boards will be done with the HAB modules plugged into a HCAL Testboard and controlled by the CRC data acquisition [2]. This test should include :

- Measuring of the power dissipation for +6V and -6V (testboard + HAB, for a specific set of switches).
- Loading of the parameter shift register.
- Measuring of noise and pedestal level for a specific set of the switches.
- Send a calibration pulse to the ASIC and do a complete readout of the 18 channels in calibration or physics mode.
- HV bias voltage test (without SiPM, only to check the electrical strength). See Section 7!

For a small number of HABs the following system characteristics should be measured with the testboard :

- Variations of the dynamic range and linearity for one ASIC (charge injection, one set of switches).
- Channel-to-channel crosstalk (charge injection into one channel).
- Dependence of gain, dynamic range, linearity and noise on temperature.

The Base Boards (HBAB) will be tested with a full set of tested Analog Boards (HAB). In this setup, the whole readout chain can be tested. Additionally, all tests from above can be repeated at least for a small number of boards, except for the charge injection tests.

6. Jumper Settings and Hardware Switches

For the exact locations of the jumpers see the schematics of the boards in [4]. The jumper type ‘solder’ refers to a resistor that has to be removed or placed in order to change the switch’s position. The jumper type ‘clip’ can be removed or set manually.

6.1 HCAL Analog Board HAB

Switch	Jumper Type	Default setting	How to switch
sw_cp1	solder	‘0’	place R107 to set to ‘1’, remove to set to ‘0’
sw_cp2	solder	‘0’	place R105 to set to ‘1’, remove to set to ‘0’
sw_cp3	solder	‘0’	place R104 to set to ‘1’, remove to set to ‘0’
sw_capa_dac	solder	‘0’	place R60 to set to ‘1’, remove to set to ‘0’

6.2 HCAL Base Board HBAB

Switch	Jumper Type	Name	Action
Temp. Monitor (1)	solder	JMP23 to temp(1)	HBAB left populated, Temp. Monitor on HAB A
Temp. Monitor (1)	solder	JMP23 to temp(2)	HBAB left populated, Temp. Monitor on HAB D
Temp. Monitor (2)	solder	JMP22 to temp(1)	HBAB right populated, Temp. Monitor on HAB A
Temp. Monitor (2)	solder	JMP22 to temp(2)	HBAB right populated, Temp. Monitor on HAB D

Switch	Jumper Type	Default setting	How to switch
Type0	solder	‘1’	remove R58 to set to ‘0’, place to set to ‘1’
Type1	solder	‘1’	remove R59 to set to ‘0’, place to set to ‘1’
Type2	solder	‘1’	remove R55 to set to ‘0’, place to set to ‘1’
Type3	solder	‘1’	remove R54 to set to ‘0’, place to set to ‘1’

If an HBAB is used without one or more Analog Boards HABs, the respective signal chains for the parameter shift register and the SROUT outputs must be bypassed. For this purpose, the following jumpers on the HBAB must be closed. If an open HAB position on the HBAB is equipped again, the respective jumpers must be opened again.
Notice : The length of the parameter shift register depends on the number of installed HABs.
The HAB positions A-F in the following table can be found in Fig. B2.

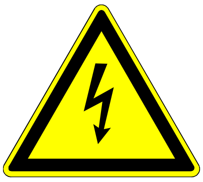
HBAB operation without Analog Board :	Close the Jumpers (clip type)
HAB A	JMP7 (SROUT), JMP8 (SR_D = SR_Q)
HAB B	JMP9, JMP10
HAB C	JMP11, JMP12
HAB D	JMP13, JMP14
HAB E	JMP15, JMP16
HAB F	JMP17, JMP18

6.3 HCAL Testboard

Switch	Jumper Type	Default setting	How to switch
JMP20: Enable TTL Buffer	clip	closed	disable test-output SRIN and LED trigger TCALIB by removing this jumper
JMP2 - JMP19: charge inject.	clip	open	close these jumpers only for charge injection tests
JMP1	clip	open	connects between Lemo connector J1 and analog ASIC input in0 (SiPM1)

7. Safety

All three boards described in this manual, the HCAL Analog Board HAB, the HCAL Base board HBAB (versions left- and right-populated) and the HCAL Testboard, contain a **high bias voltage (+100V DC max.)** on board connectors and open traces. Do not connect a higher voltage than 100V DC to any of the boards. All boards of this manual are not foreseen to be operated as stand-alone electronics, but are part of a system, for which the local safety rules must be fulfilled. Normally, this can be achieved by an exclusive operation in a closed, grounded metal case.



For an operation of all boards described in this manual at DESY Hamburg, the safety rules of [5] must be fulfilled.

At any other location than DESY, the local safety rules must be fulfilled and the local safety-responsible person is in charge.

References

[1] CALICE Home Page : CAlorimeter for the LInear Collider with Electrons
http://polywww.in2p3.fr/flc/calice.html

[2] Internal Note : "CALICE ECAL Readout Electronics: VFE PCB Interface Specification", June 2004

[3] S. Blin, J. Fleury, C. de la Taille, G. Martin, L. Raux , "H-CAL SiPM ASIC Status", CALICE meeting 7.12.2004, Hamburg

[4] CALICE scintillator HCAL electronics web page :
https://www.desy.de/~sefkow/HCALelectronics.html

[5] Unfallverhütungsvorschrift "Elektrische Anlagen und Betriebsmittel", GUV-V A2, Landesunfallkasse Hamburg, letzte Fassung : Oktober 1999, http://www.luk-hamburg.de

Appendix A – Pin Definition of HBAB's SCSI- and SUB D Connectors

HBAB SCSI Connector			Signal Description
Pin No	left populated	right populated	(only differences to ECAL setup)
35, 1	Analog Out 1 (+, -)		
36, 2		Analog Out 7 (+, -)	
37, 3			
38, 4	Analog Out 2 (+, -)		
39, 5		Analog Out 8 (+, -)	
40, 6	HOLD_IN (+,-)	HOLD_IN (+,-)	
41, 7	VCALIB (+, -)	VCALIB (+, -)	
42, 8	SRIN_IN (+, -)	SRIN_IN (+, -)	
43, 9	RESET_IN (+, -)	RESET_IN (+, -)	
44, 10	SR_RES_IN (+, -)	SR_RES_IN (+, -)	'1' = Reset of Parameter Shift Register
45, 11	SR_D_IN (+, -)	SR_D_IN (+, -)	Data Input of Parameter Shift Reg.
46, 12	SEL_OUT (+, -)	SEL_OUT (+, -)	To DAQ : '0' = SROUT, '1' = SR_Q/SR_DAC
47, 13	CLOCK_IN (+, -)	CLOCK_IN (+, -)	
48, 14	Analog Out 3 (+, -)		
49, 15		Analog Out 9 (+, -)	
50, 16	SR_CLK_IN (+, -)	SR_CLK_IN (+, -)	Load Clock of Parameter Shift Reg.
51, 17	SW_HOLD_IN (+, -)	SW_HOLD_IN (+, -)	'0' = Send HOLD, '1' = Send logical '1' to HAB
52, 18	SW_DAC_IN (+, -)	SW_DAC_IN (+, -)	'1' : Connect ASIC DAC after Programming
53, 19			
54, 20	Analog Out 4 (+, -)		
55, 21		Analog Out 10 (+, -)	
56, 22	SROUT_OUT (+, -)	SROUT_OUT (+, -)	Output to DAQ : SROUT or SR_Q
57, 23	ADDRESS (+, -)	ADDRESS (+, -)	Drives an LED, only for test. **NOT on testboard**
58, 24	LED_SEL (+, -)	LED_SEL (+, -)	'0' = Drive LEDs, '1' = Calibrate ASICs (TCALIB)
59, 25	TCALIB_IN (+, -)		
60, 26		TCALIB2_IN (+, -)	
61, 27	TYPE0 (+, -)	TYPE0 (+, -)	
62, 28	TYPE1 (+, -)	TYPE1 (+, -)	
63, 29	TYPE2 (+, -)	TYPE2 (+, -)	
64, 30	Analog Out 5 (+, -)		
65, 31		Analog Out 11 (+, -)	
66, 32	TYPE3 (+, -)	TYPE3 (+, -)	
67, 33	Analog Out 6 (+, -)		
68, 34		Analog Out 12 (+, -)	

Table A1 : Pin Definition of the SCSI Connector
(Interface to CRC Data Acquisition Board)

Power Connector : 9pin Sub D male plug	
Pin No	Signal / Power
1	HV (+100V DC max)
2	GND
3	VM6 (-6V)
4	GND
5	VP6 (+6V)
6	Temperature 1, Current Out
7	Temperature 2, Current Out
8	GND
9	VP6 (+6V)

Table A2 : Pin Definition of the 9-pin male Sub D Connector (Interface to the Power Supplies)

Appendix B : HCAL Base Board HBAB

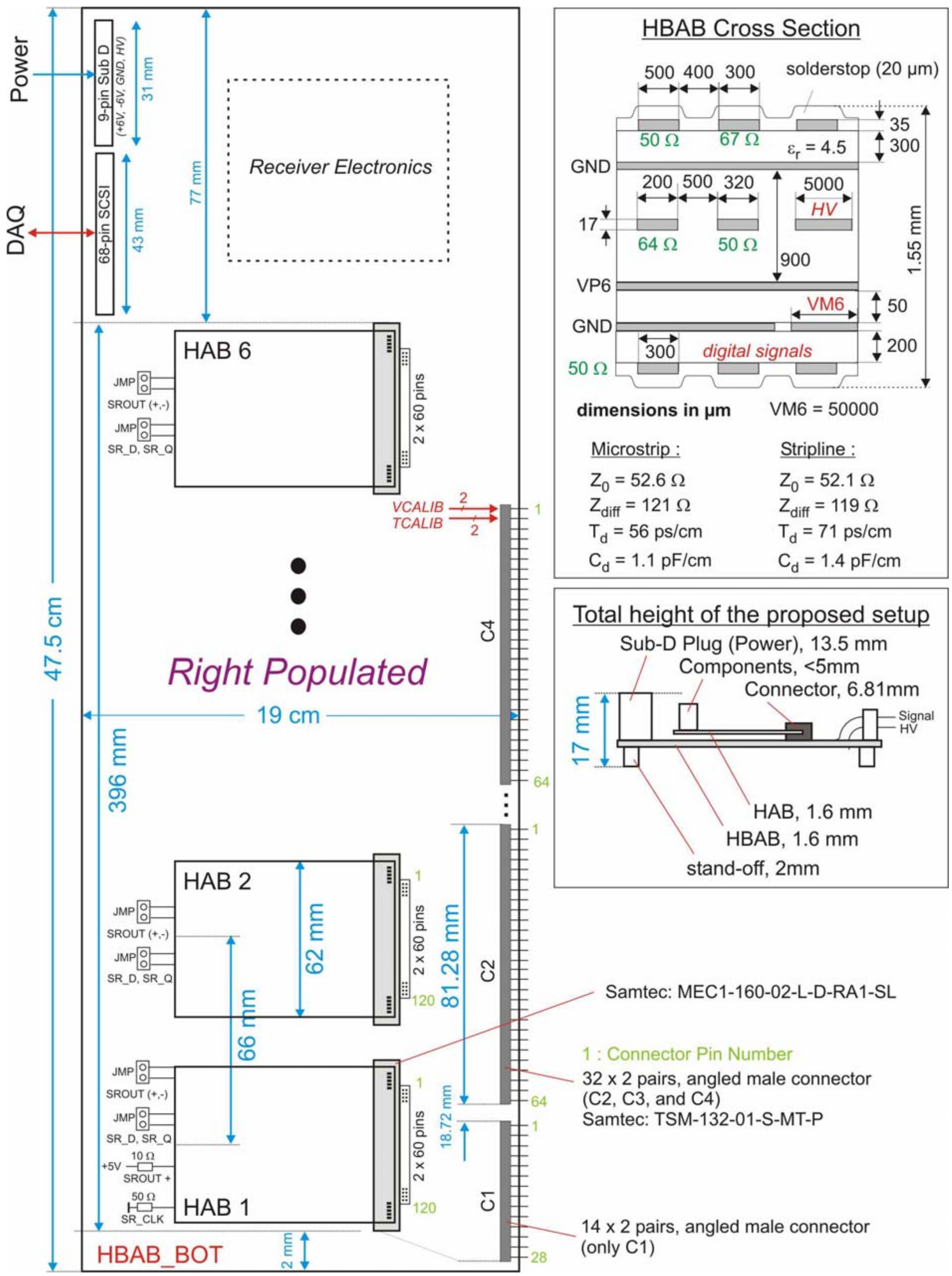


Fig. B1 : Structure and Dimensions of the HCAL Base Board HBAB

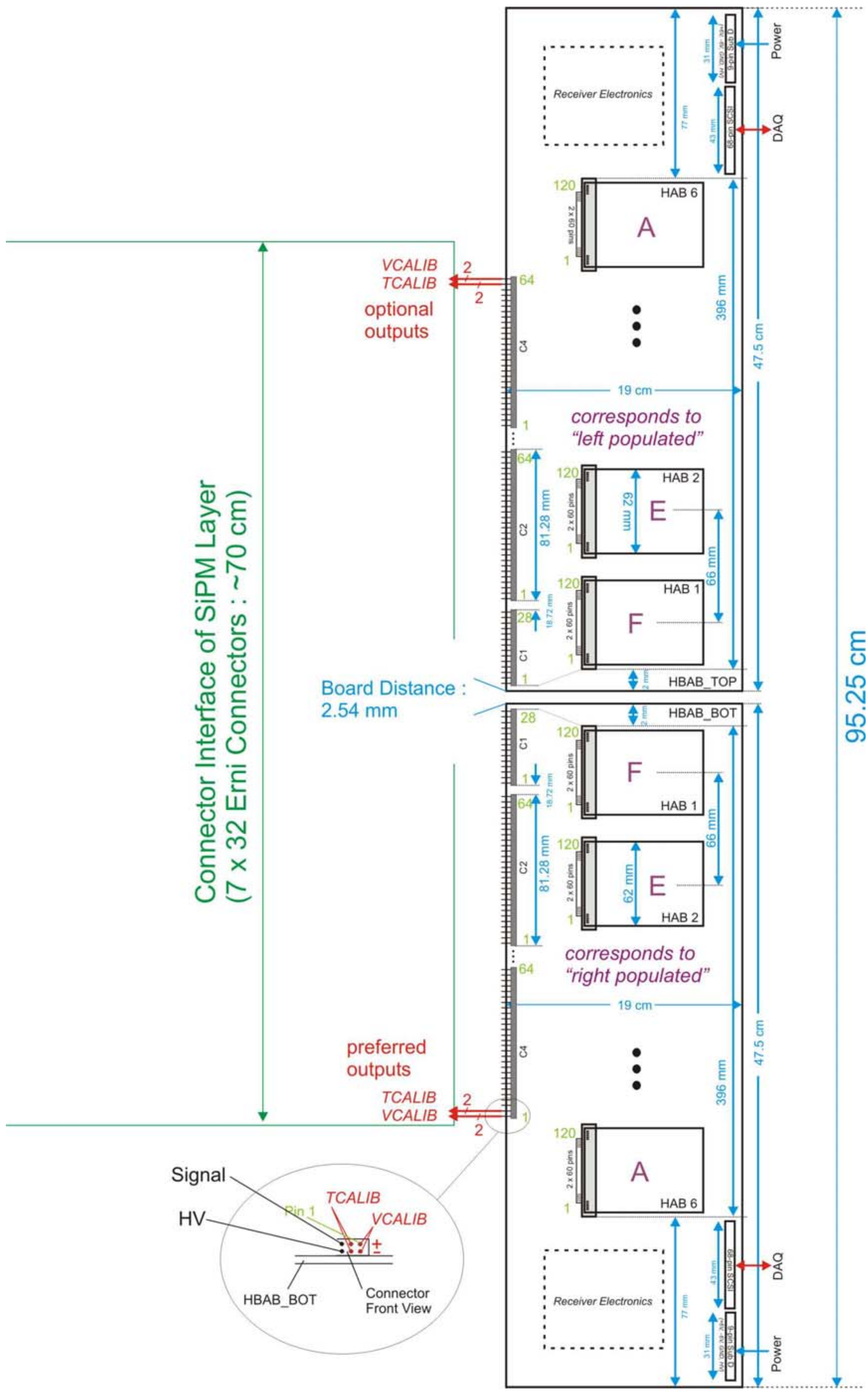
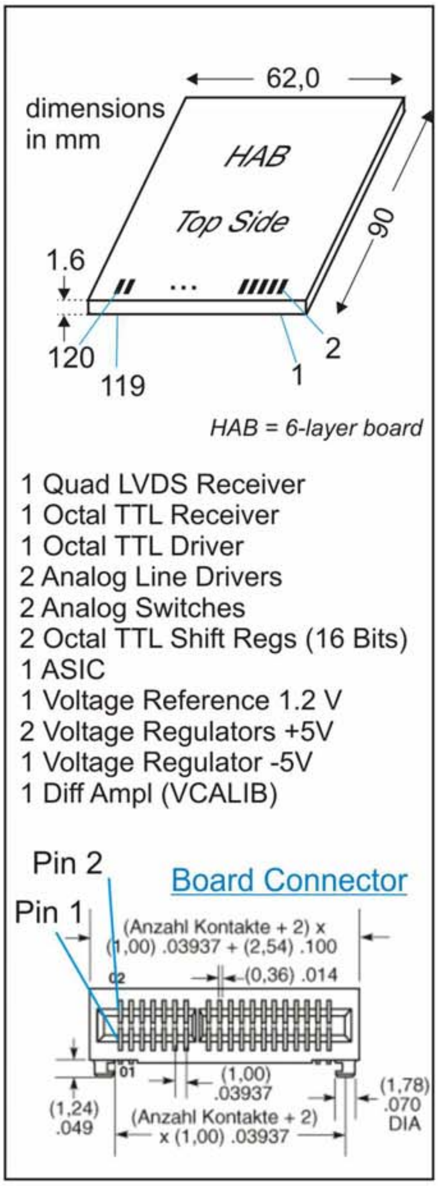


Fig. B2 : Setup of two HBABs at The SiPM Interface

Appendix C : HCAL Analog Board HAB

Output1+	2	1	HOLD1- (LVDS1)
Output1-	4	3	HOLD1+
GND	6	5	CLOCK1+ (LVDS2)
SRIN- (LVDS 3)	8	7	CLOCK1-
SRIN+	10	9	GND
TCALIB1+ (LVDS 4)	12	11	RESET (TTL In1)
TCALIB1-	14	13	GND
GND	16	15	SR_RES (TTL In2)
VCALIB+ (analog)	18	17	SR_D (TTL In3)
VCALIB-	20	19	SR_Q (TTL Out1)
GND	22	21	SR_CLK (TTL In 4, 50Ω)
GND	24	23	VP6 (+6V)
GND	26	25	SW_DAC (TTL In5)
VP6 (+6V)	28	27	SW_HOLD (TTL In6)
VP6 (+6V)	30	29	VM6 (-6V)
polar.	32	31	polar.
VP6 (+6V)	34	33	SROUT_IN (Wired AND)
VM6 (-6V)	36	35	SROUT_OUT (Wired AND)
VM6 (-6V)	38	37	
	40	39	TEMP+
HV_IN (+80V)	42	41	
HV_IN (+80V)	44	43	
	46	45	HV18
SiPM18	48	47	
	50	49	HV17
SiPM17	52	51	
	54	53	HV16
SiPM16	56	55	
	58	57	HV15
SiPM15	60	59	
	62	61	
polar.	64	63	polar.
	66	65	HV14
SiPM14	68	67	
	70	69	HV13
SiPM13	72	71	
	74	73	HV12
SiPM12	76	75	
	78	77	HV11
SiPM11	80	79	
	82	81	HV10
SiPM10	84	83	
	86	85	HV9
SiPM9	88	87	
	90	89	HV8
SiPM8	92	91	
	94	93	HV7
SiPM7	96	95	
	98	97	HV6
SiPM6	100	99	
	102	101	HV5
SiPM5	104	103	
	106	105	HV4
SiPM4	108	107	
	110	109	HV3
SiPM3	112	111	
	114	113	HV2
SiPM2	116	115	
	118	117	HV1
SiPM1	120	119	

Achtung neue Pindefinition (14.12.04)
Caution : New Pin Definition (14.12.04)



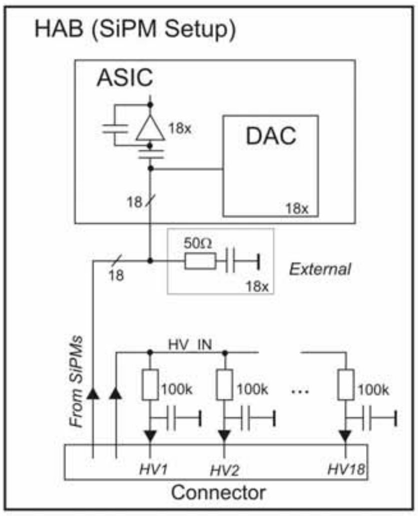


Fig. C1 : Pin Definition of the HAB (left) and setup details (right)

Step 1 : SW_DAC=1 : Load ASIC DAC Shift Register,
18 x 8 bits per HAB, 864 bits per HBAB (6 HABs)

Step 2 : SW_DAC=0 : Load external Shift Register,
16 bits per HAB, 96 bits per HBAB (6 HABs)

External Shift Register

1. sw_cr0 (Pin 35)
2. sw_cr1 (Pin 36)
3. sw_cr2 (Pin 37)
4. sw_cr3 (Pin 38)
5. sw_g (Pin 41)
6. sw_buf (Pin 48)
7. sw_cf0 (Pin 57)
8. sw_cf1 (Pin 58)
9. sw_cf2 (Pin 59)
10. sw_cf3 (Pin 60)
11. sw_cp0 (Pin 64)
12. sw_RC6_spe2 (Pin 65)
13. sw2_RC6 (Pin 66)
14. sw_RC6_spe1 (Pin 67)
15. sw_Rc6_spe0 (Pin 71)
16. sw_RC6 (Pin 75)

Bit 1 enters the HAB first !!
Numbers in brackets are
ASIC pin numbers.

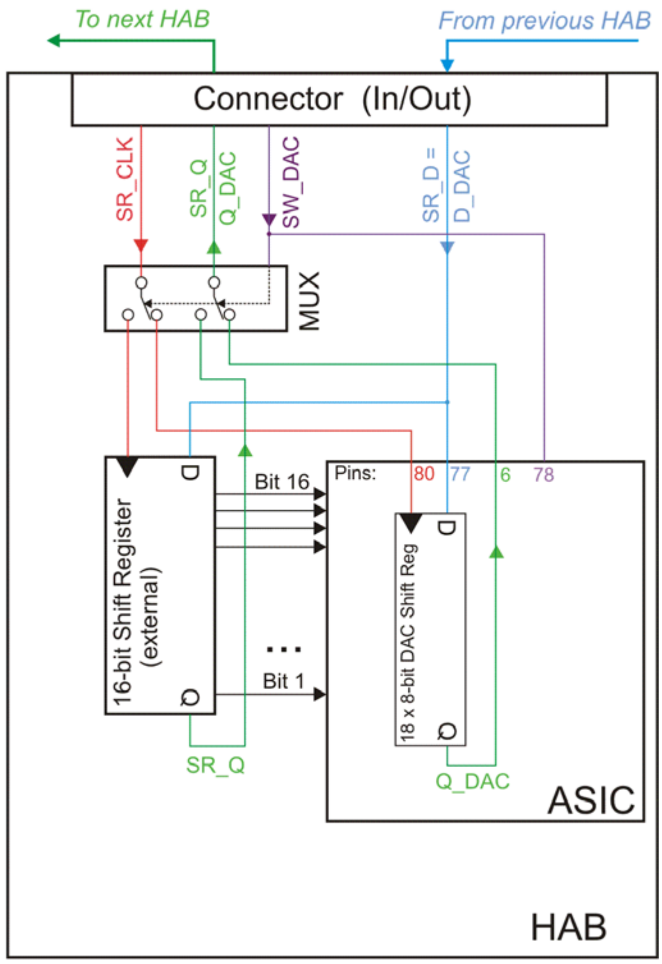


Fig. C2 : Implementation of the Parameter Shift Register on the HAB