HARDROC ASIC

User Guide

DRAFT,March 19, 2007

I. Presentation :

The HaRDROC (Hadronic RPC ReadOut Chip) ASIC has been designed for the readout of the "Digital" Hadronic CALorimeter (DHCAL) that will be used in the International Linear Collider. .

1. DHCAL forseen detectors:

A **new generation of high precision detectors** is developed to be used in a very near future for the detector on the ILC lepton collider.
Such detectors are already under investigation all over the world. This takes place in the frame of the preparation for the International Linear Collider (ILC). The main aspect of the investigated detectors is their ability to allow the application of the so-called particle flow algorithms which consist of following the particle in each part of the whole detector and not only in the tracker as it used to be. Being able to follow a particle in the different sub-detectors will allow to chose the particle energy measurement in the sub-detector which provides the best energy resolution for the traced particle. This implies to conceive electromagnetic and hadronic calorimeters in a new manner. They should indeed provide not only very precise energy measurement but also strong tracking capacity.

To realise a hadronic calorimeter with tracking capacity, 3 options are currently under study:

- A hadronic calorimeter with a sensitive part based on plastic scintillating tiles associated to **SiPM** and using the same analogue electronics readout proposed for the electromagnetic calorimeter. The size of the plastic tiles are however large (3x3 cm^2). A specific ASIC (SPIROC) is under design for the readout of such a detector
- A more granular detector concept using Glass Resistive Plate Chambers (GRPC) with pads of 1X1 cm^2 size. It will be made of planes of stainless steel making the absorber part of the calorimeter. Each stainless steel plane will be followed by a plane of an active medium. As active medium, two kinds of chambers are under investigation: the **Glass Resistive Plate Chamber (GRPC)** and **the MICROMEGAS chamber (µMEGAS).**

HARDROC has been designed for the readout of GRPC or µMEGAS.

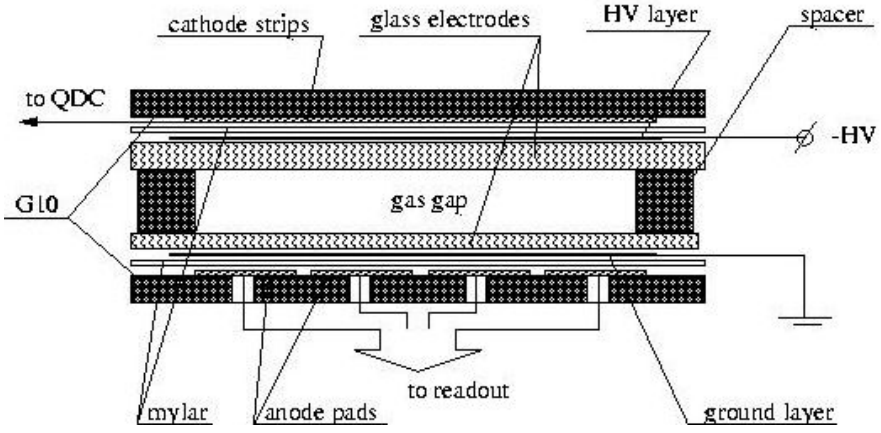


Figure 1: RPC design

II. HARDROC specifications:

An hadronic calorimeters of **very fine granularity** needs appropriate electronics readout. The number of **electronics channels (4 10^5 /m^3)** is a new feature of hadronic calorimeter domain.

The **electronics readout system** is based on a semi-digital readout with two thresholds (2 bits readout). This is a compromise between the analogue solution of the German-Russian solution (SiPM) and the binary one proposed by the Americans. This compromise allows both good tracking and good energy measurement.

The new electronics readout is **intended to be embedded in the detector**. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to **10 µWatt per channel** using the power pulsing scheme, possible thanks to the ILC bunch pattern: 1 ms of acquisition data for 199 ms of dead time.

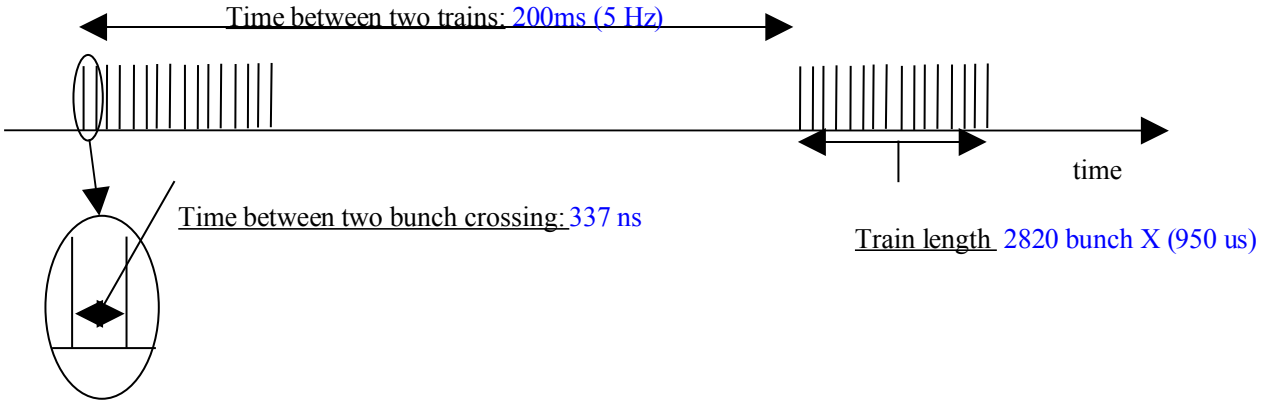


Figure 2: ILC bunch pattern

A prototype made of 40 planes of 70X70 cm2 interleaved with absorber planes of stainless steel 1 cm thick will require 64X64X40 electronics channels. Because of the very high number of electronic channels, it is essential to limit the amount of the transmitted data and hence the recorded ones without losing information. To achieve this aim, the acquisition system will make use of zero suppression techniques and data concentrators for each detector plane. The data of each plane will then be transferred to computing unit through a USB device.

As the detector used is still not defined (RPC or GEM), the analog front-end of the HARDROC chip has to deal with several dynamic ranges and shaping. It services 64 inputs and provides a single serial data output.

HARDROC1 has been designed using the AMS SiGe 0.35 m technology (Fig. 3). The package used is CQFP240. The area of the chip is 16mm2. It has been submitted in Sept 2006 and received in December 2006.

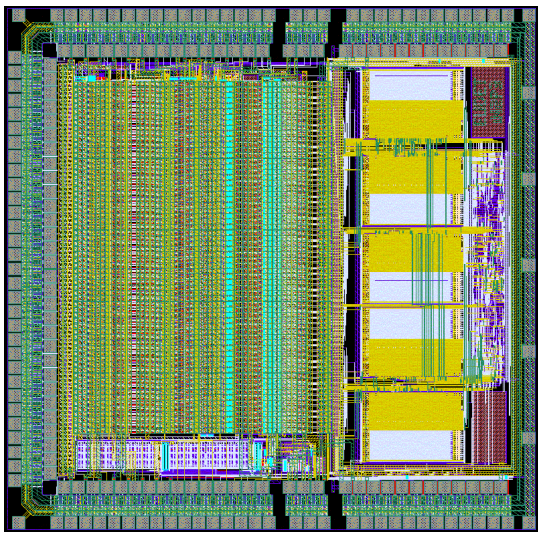


Figure 3: Layout of HARDROC1

Fig. 4 represents the bloc diagram of HARDROC1 with its main features. The chip has 64 "super common base" inputs, 1 serial output and a multiplexed charge output.

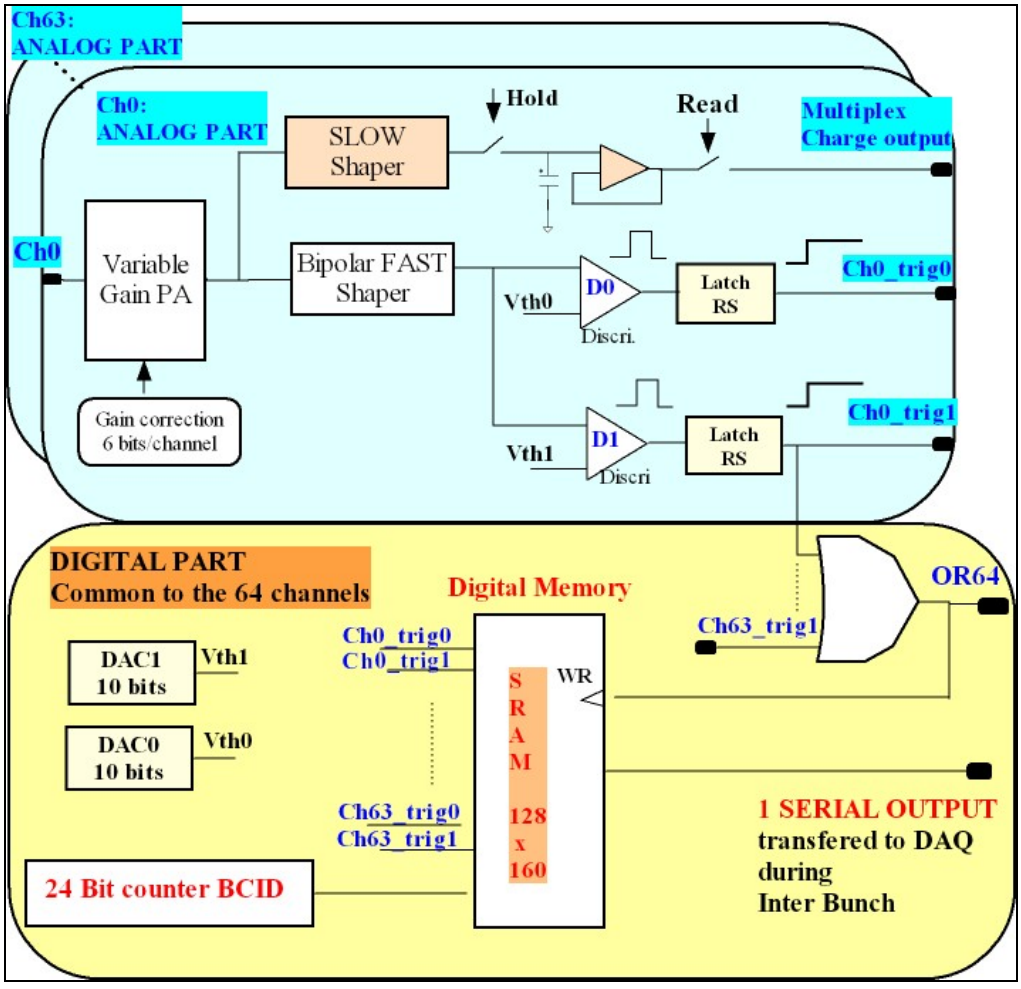


Figure 4: Simplified schematics of HARDROC1

Each channel is made of a variable gain preamplifier with low input tunable impedance (50-100 Ω), a low offset and a low bias current (20 µA) in order to minimize the cross talk. This variable gain allows adapting the gain depending on the detector choice, up to a factor 4 to an

accuracy of 6% with 6 bits. This gain tuning is also convenient to switch off a noisy channel. The amplified current feeds then two paths:

- A slow shaper path which consists in a $CRRC^2$ shaper and a Sample and Hold Widlar differential buffer. This S&H block stores the charge in a 2pF capacitor and delivers a multiplexed charge measurement with a 5 MHz readout speed.
- A fast (15ns) shaper path made of a CRRC bipolar shaper followed by 2 discriminators the thresholds of which are set by 2 internal 10 bit DACs.
- Each trigger output is latched to hold the state of the response until the end of the clock cycle. The trigger1 outputs (corresponding to Vth1 <Vth0) are OR wired to generate an internal trigger used to start the memorization of the 128 trigger outputs as well as the Bunch Crossing Identification delivered by a 24 bit counter. Indeed, to reconstruct hits in the DAQ, the chip must provide an event ID for each hit. It's also possible to capture event data using an external trigger provided from outside the chip.
- All the biases are programmed through the Slow Control
- The chip is power pulsed to decrease the power consumption. 10µV/channel is targeted with a 1% beam duty cycle

III. HARDROC analog part :

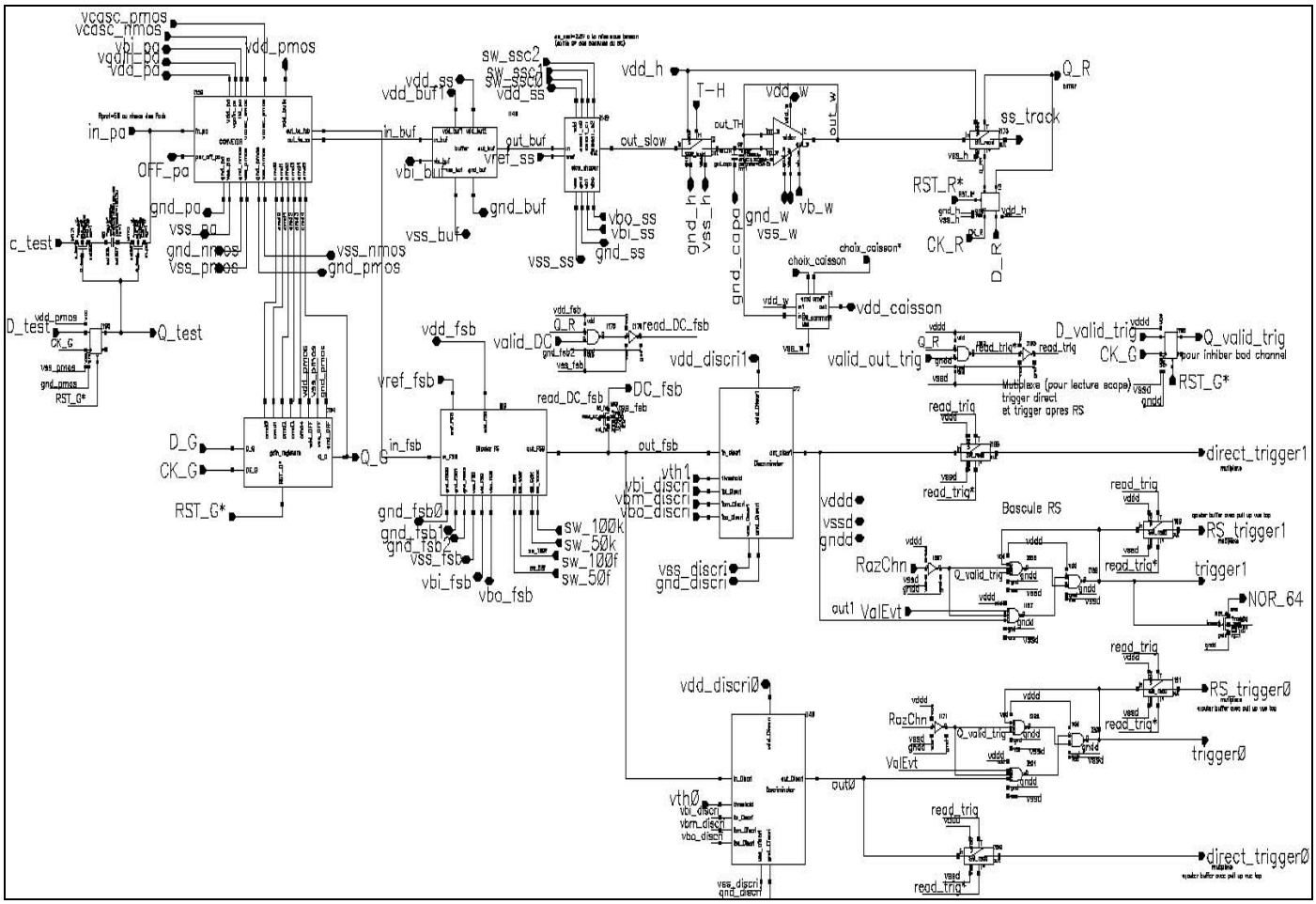
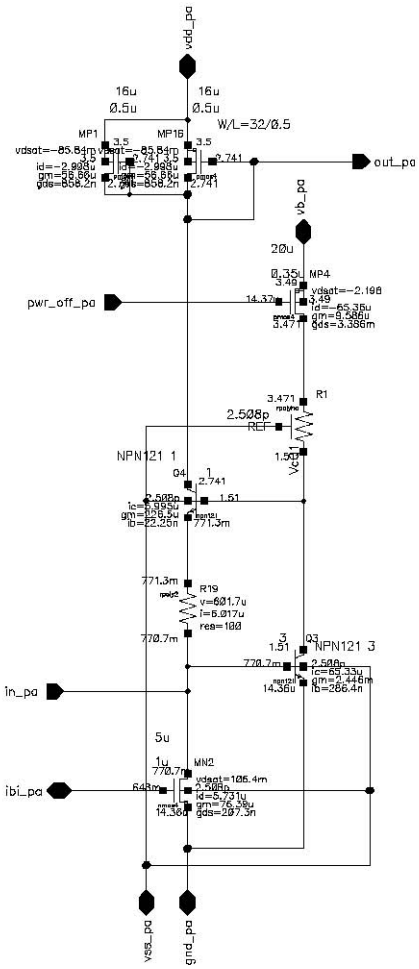


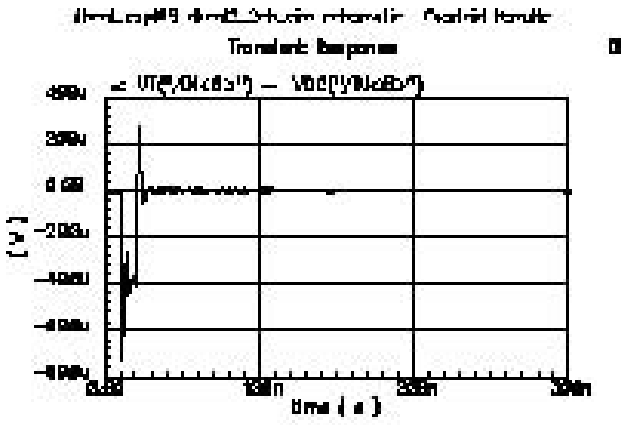
Figure 5: ONE CHANNEL (analog part)

1- Input Preamp: Super Common Base configuration

The input impedance of the SBC is given by: Zin= $1/gm_1gm_2Rc$ which is a low value resulting in small currents in the mirrors and thereby reducing the crosstalk.

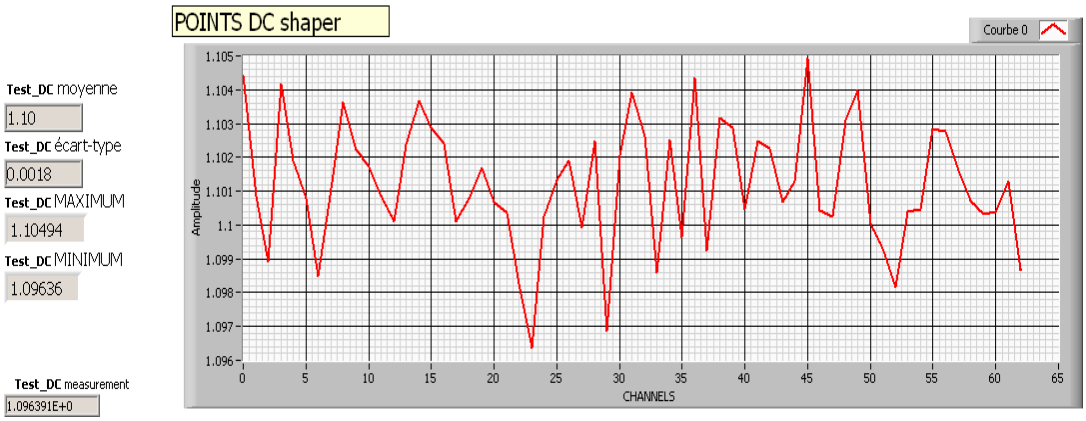
The current source is made with a 39k resistor the noise of which is $\sqrt{\frac{4kT}{R}}$ $0.65\,pA/\sqrt{Hz}$. A real current source would exhibit a noise of $2qI=2*1.6.10^{-19}.20.10^{-6}$ = 2.5 pA/√Hz, which is not acceptable.

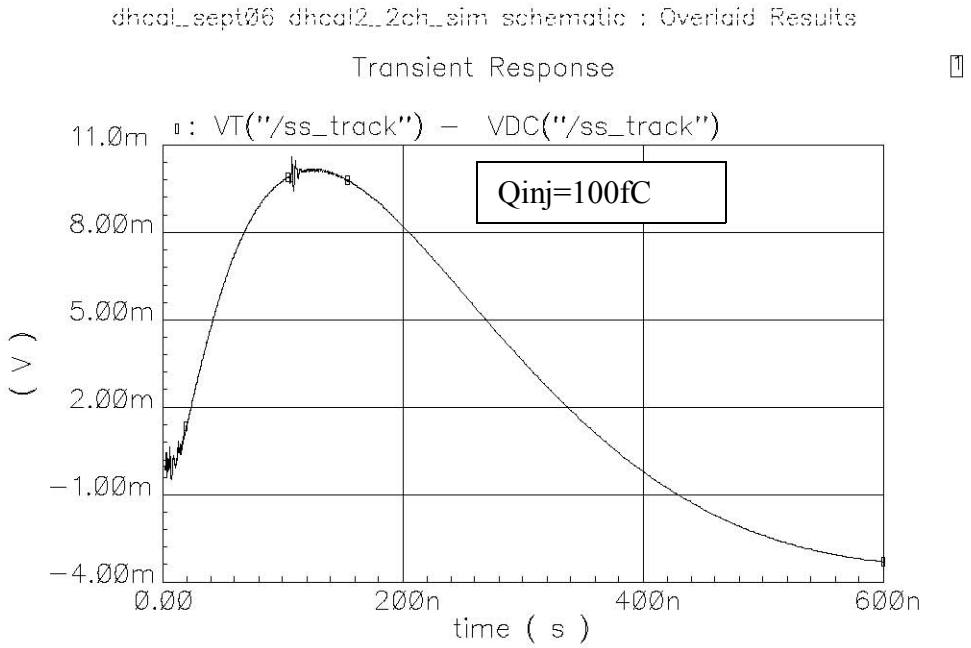


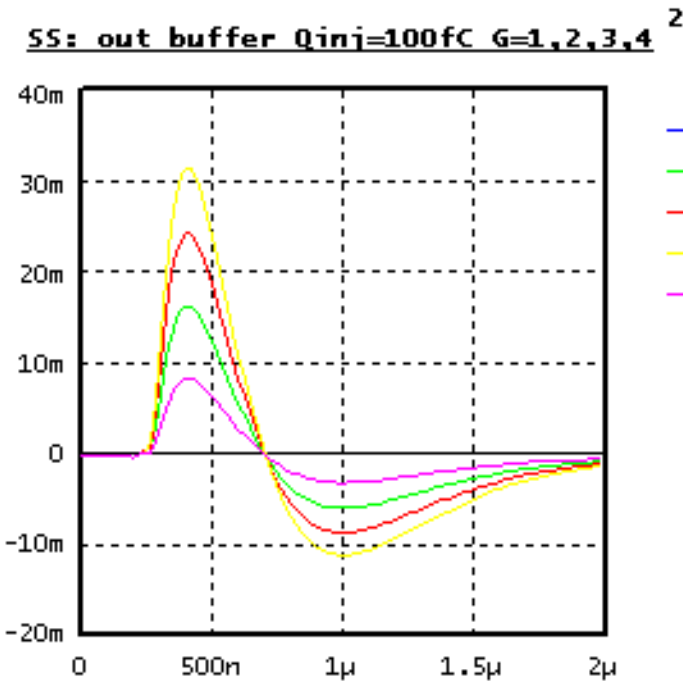


2- Slow channel

DC uniformity of the 64 channels: <>=1.10V σ=1.8mV

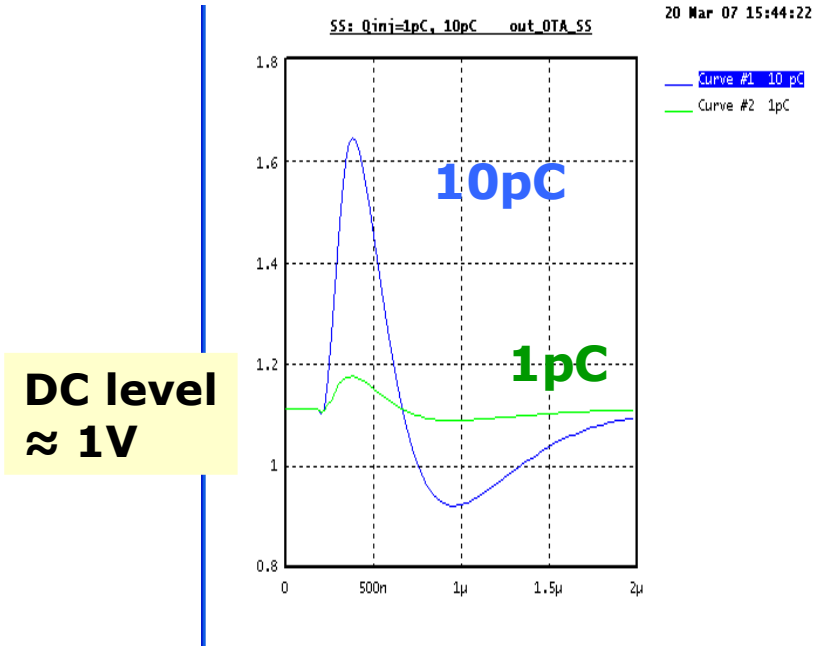




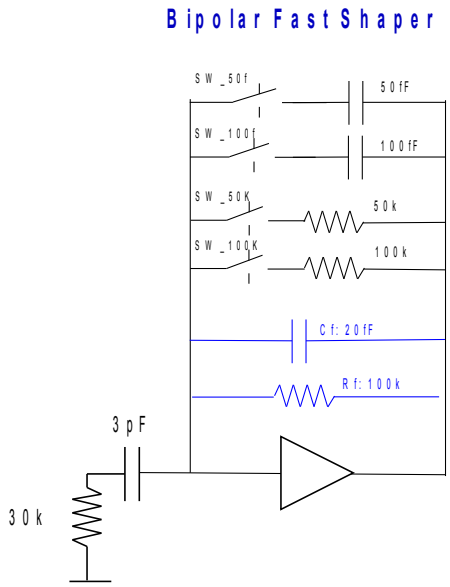


Qinj=100 fC (1V attenuated by 40dB in 10pF) :

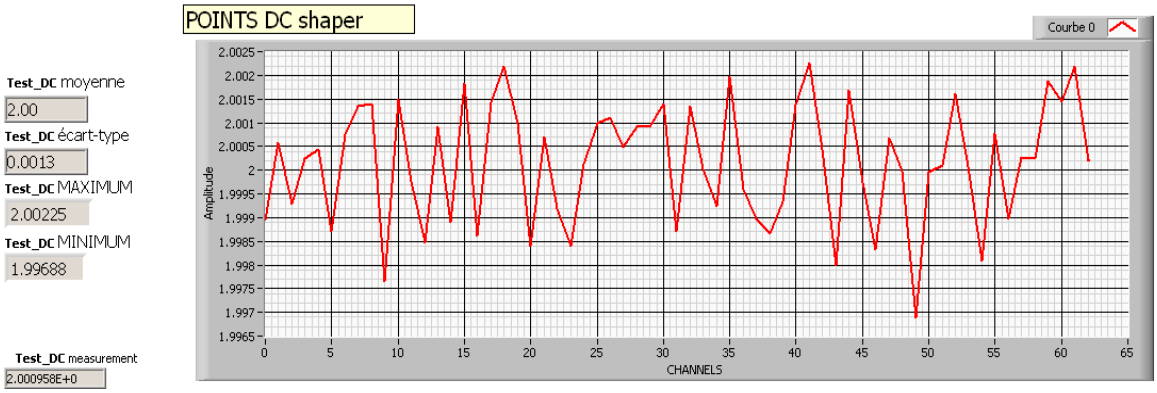
Gain PA= 1	18.47 mV	tp=144 ns
G=2	16.51 mV	148 ns
G=3	24.44 mV	146ns
G=4	31.66mV	145ns

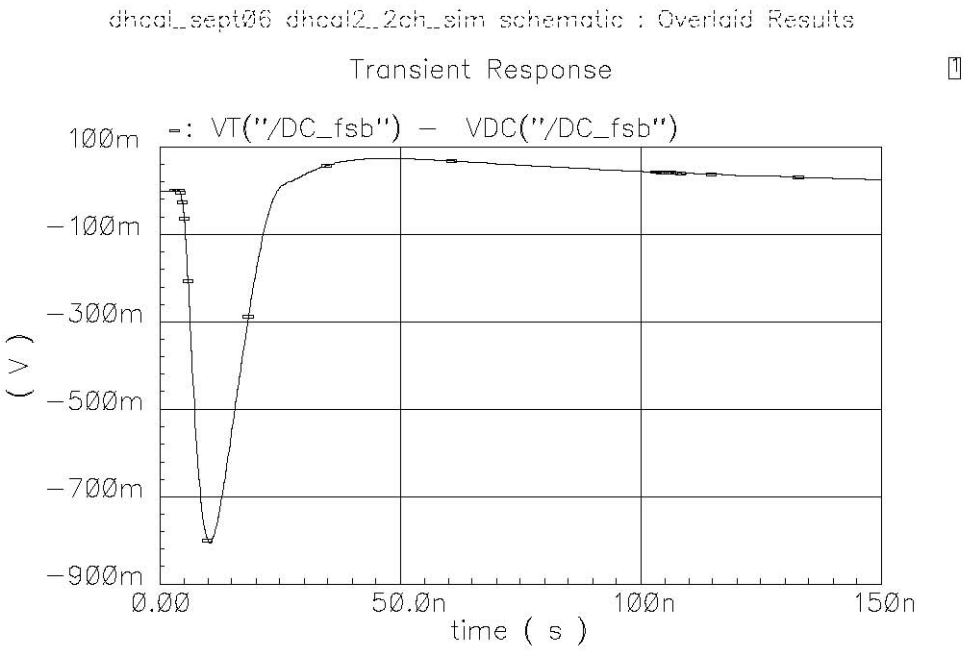


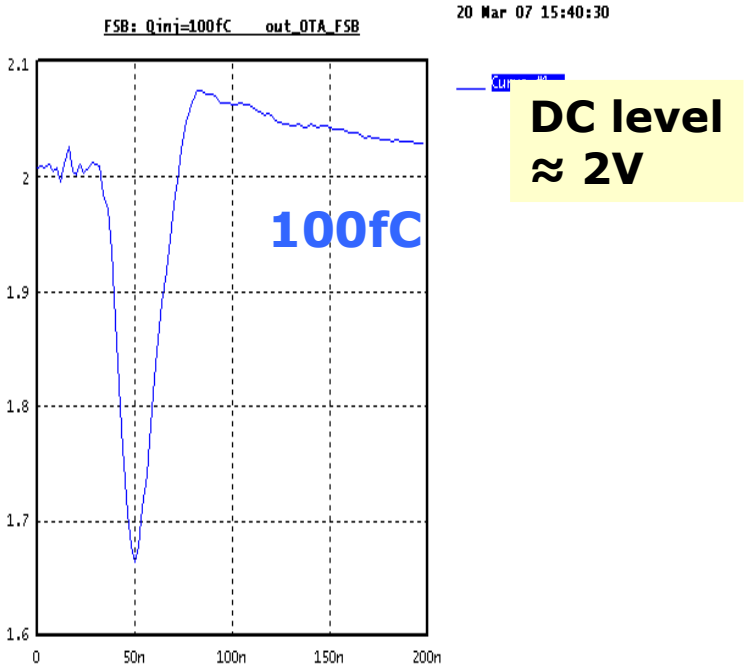
3- Bipolar Fast shaper



DC uniformity of the 64 channels: <>=2.00V σ=1.3mV







- **100fC => 350mV, tp=15ns, ie 3.5mV/fC**

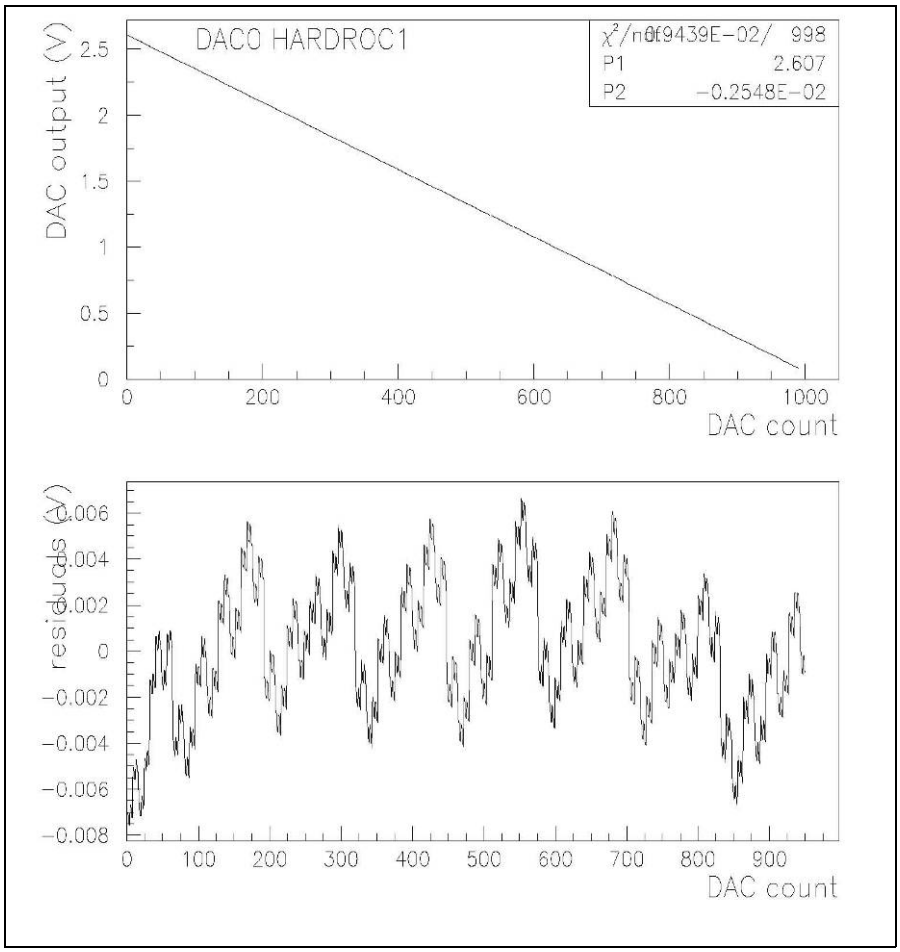
4- DAC

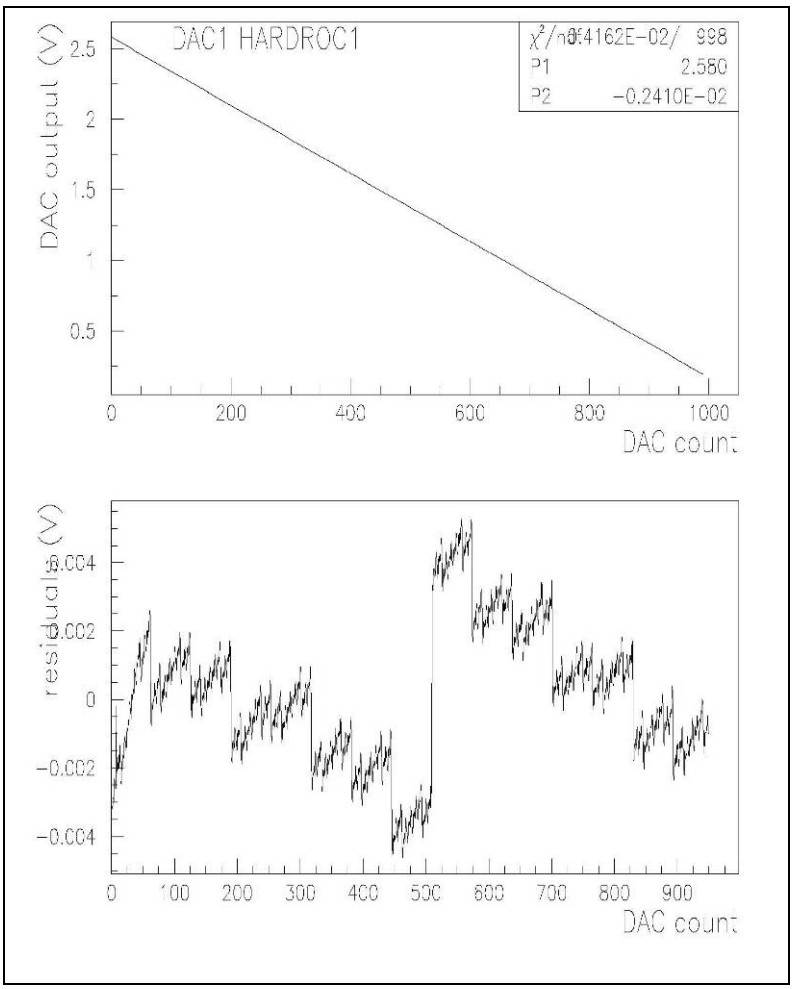
2 integrated DACs to deliver Threshold voltages

Residuals within ±5 mV / 2.6V dynamic range.

INL= 0.2% (2LSB)

2.5 mV/UDAC





5- Discriminator

III. HARDROC digital part :

1- ANALOG-DIGITAL Interface

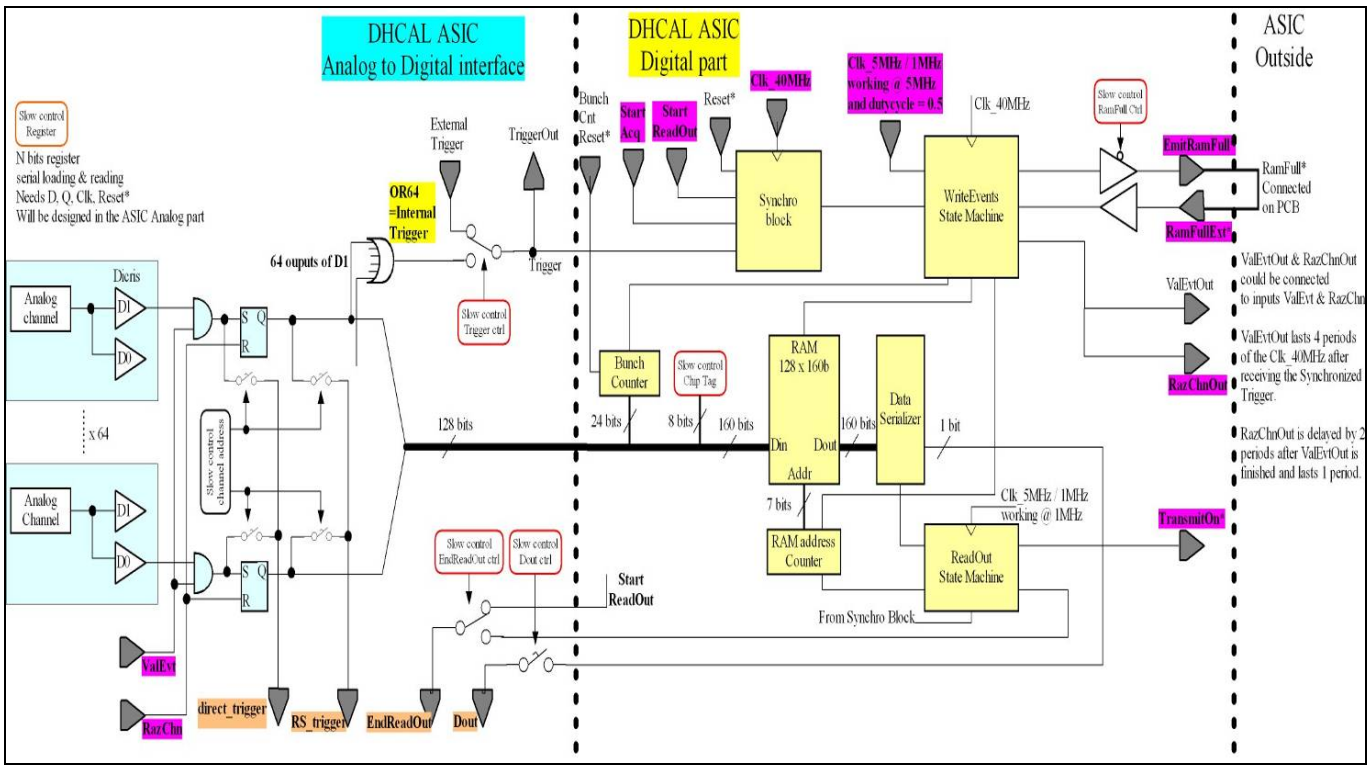


Figure 6: Interface between analog and digital part

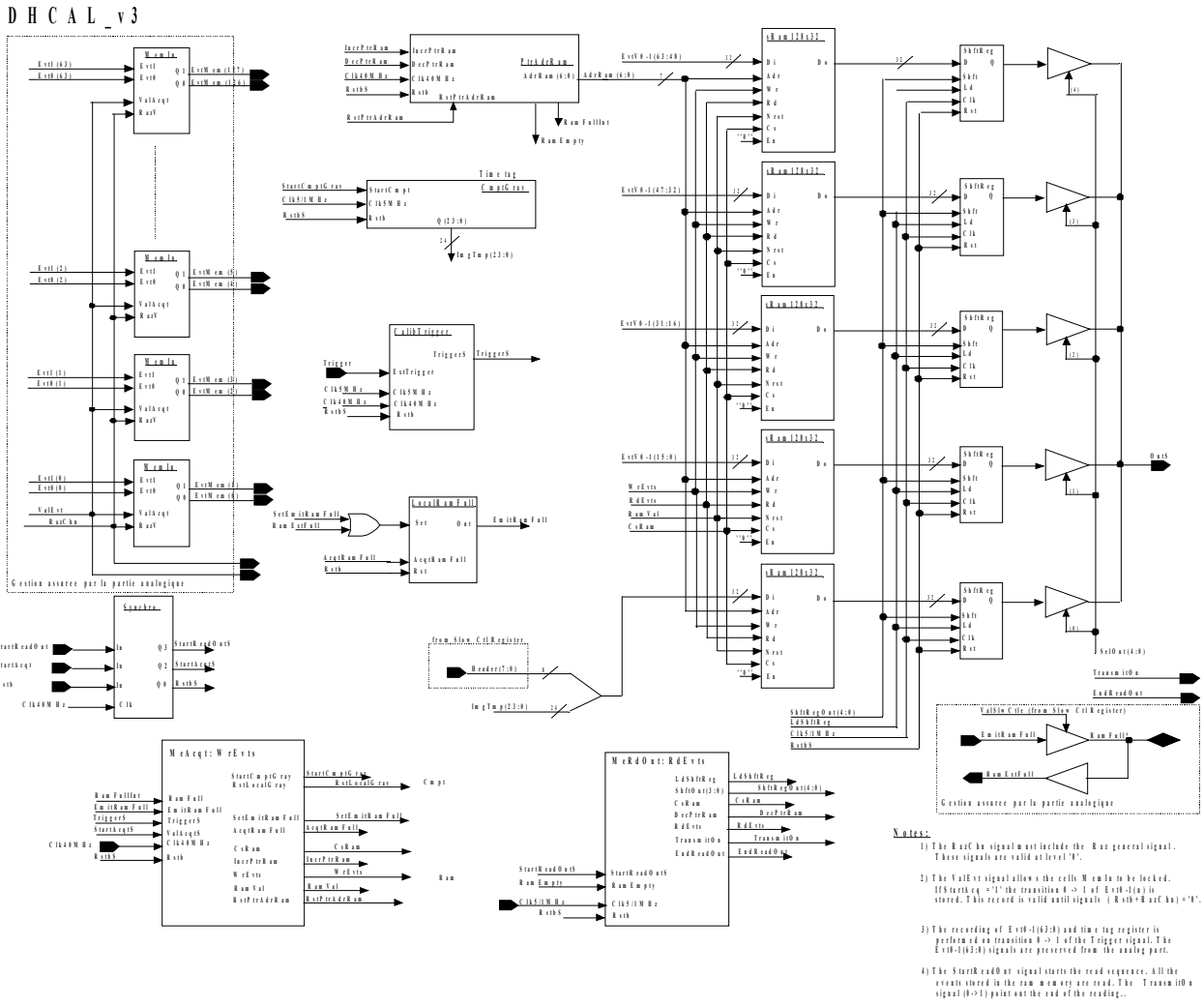
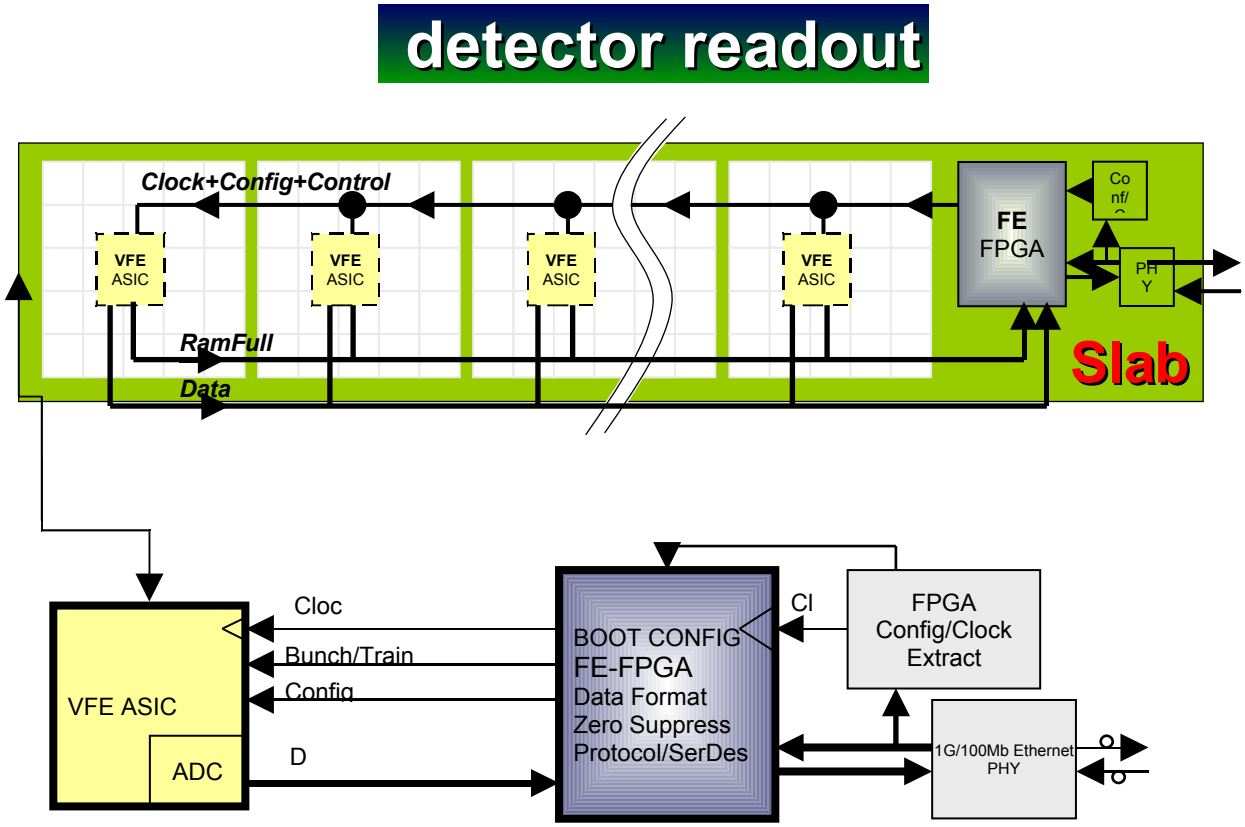
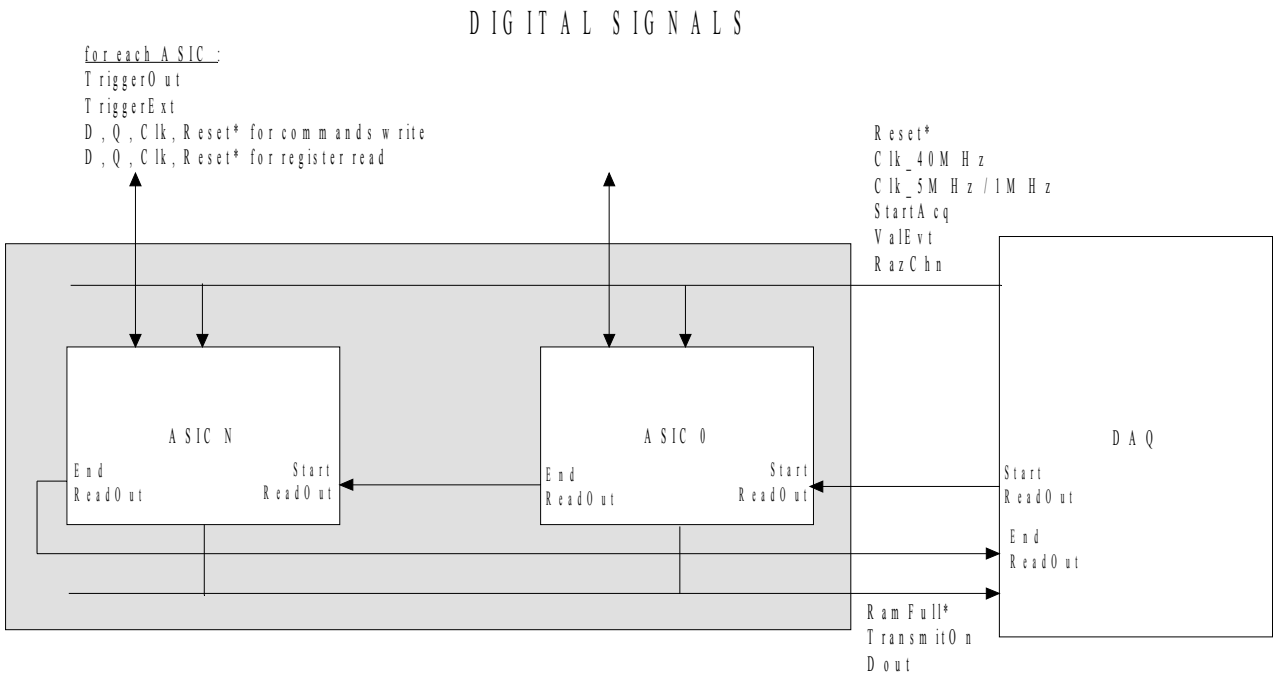


Figure 7: Digital part

1. Digital Front-end description :



There will be 16 64 ch ASICs/SLAB. To minimize the number of lines on the PCB, the ASICs are daisy chained.

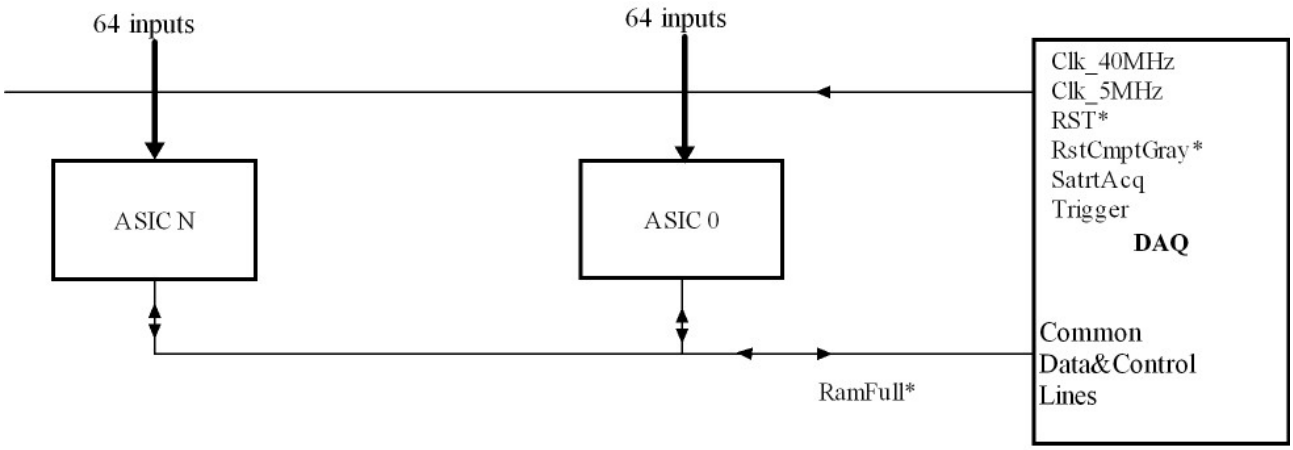


The following table lists the signals that will be routed on the PCB.

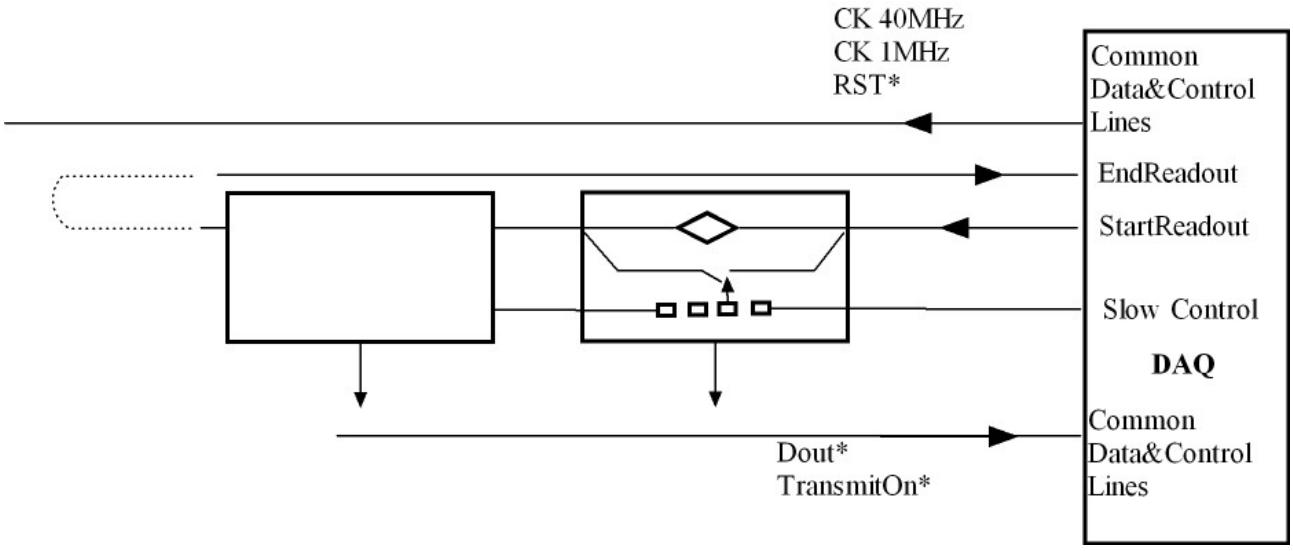
Signal name	INPUT/OUPUT	Valid on	Common	Adaptation	Single/Diff
Reset*	INPUT	LOW	YES	YES	SINGLE
Clk_5MHz / 1MHz	INPUT	RISING	YES	YES	DIFF
Clk_40MHz	INPUT	RISING	YES	YES	DIFF
StartAcq	INPUT	HIGH	YES	YES	SINGLE
ValEvt	INPUT	HIGH	YES	YES	DIFF
RazChn	INPUT	HIGH	YES	YES	DIFF
StartReadOut	INPUT	HIGH	NO	NO	SINGLE
EndReadOut	OUTPUT	HIGH	NO	NO	SINGLE
TransmitOn	OUTPUT	HIGH	YES	YES	SINGLE
Dout	OUTPUT	-	YES	YES	SINGLE
RamFull*	BIDIR	LOW	YES	YES	SINGLE
TriggerExt	INPUT	RISING	NO	NO	SINGLE
TriggerOut	OUTPUT	RISING	NO	NO	SINGLE

The DAQ provides the 40 MHz clock which is necessary for the state machin of the ASIC memory. The slow clock (5 or 1MHz) is used for the acquisition and the readout mode.
TransmitOn, RamFull* and Dout are open collector signals.

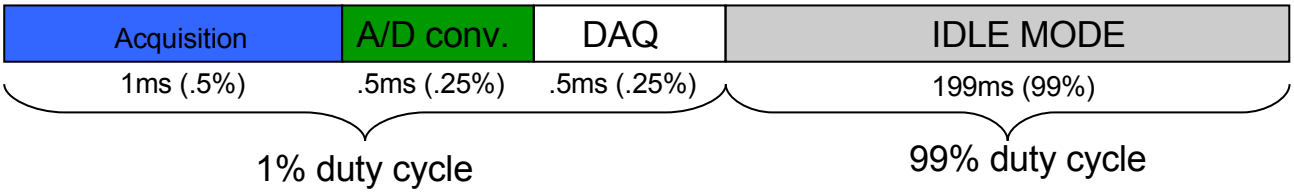
Acquisition mode:
The StartAcq signal initiates the acquisition; The ValEvt signal (LVDS) is a validation window necessary to enable the latch of the triggers. Up to 128 events are stored in the memory. The acquisition is stopped when the RamFull signal is sent by one of the ASICs.



Readout mode:
The readout is made using a token ring mechanism initiated by the DAQ with the possibility to bypass a chip by slow control.
One data line is activated by each chip sequentially.



Timing:



IV. PINOUT :

pin number	pin name	connect to	DC voltage	DC current	Bias
1	in<2>	detector	0.8V		
29	in<30>	detector			
30	in<31>	detector			
31	**gnd_pa**	**gnda**			
32	in<32>	detector			
60	in<60>	detector			
61	in<61>	detector			
62	**vssi**				
63	in<62>	detector			
64	in<63>	detector			
65	**gnd_pa**	**gnda**			
66	**vdd_pad**		3,5V		
67	**vdd_pa**	**vdda**	3.5V		connected to 231
68	ctest				
69	**gnd_nmos**				
70	vcasc_pmos		1V		divider 1K,2.5K
71	**vssa**				
72	vcasc_nmos		1,5V		divider 1.5K,2K
73	**vdd_buf1**				
74	**gnd_buf**	**gnda**			
75	**vdd_pmos**				
76	ibi_otadac		0.8V	178uA	100K to gnd_bg
77	**vdd_dac**				
78	ibo_otadac		0.6V	28uA	1K to gnd_bg
79	**gnd_dac**				
80	***Q_R***				LVTTL ASIC input
81	***hold***				LVTTL ASIC input
82	vcasc_dac		1V		divider (10K,25K)
83	***D_R***				LVTTL ASIC input
84	iref_dac	**External 68K to gnd**			150K to v_bg
85	***CK_R***				LVTTL ASIC input
86	vref_otadac		2V		(200K,50K) to v_bg
87	***rst_R****				LVTTL ASIC input
88	**vdd_bg**				
89	**pwr_on_dac**				**Slow Control**
90	ibi_otabg		2.6V	25uA	100K to gnd_bg
91	**gnd_bg**				
92	ibo_otabg		2,5V	2.5mA	1K to gnd_bg
93	**vssa**				
94	vth0				
95	**vdd_d0**				

96	**gnd_d**				
97	**vdd_d1**				
98	vth1				
99	**vssm**				
100	**vssd**				
101	**gndd**				
102	**vddd2**				
103	**vddd**				
104	ib_rec		0.8V	106uA	25K to vddd
105	***pwr_on_d***				LVTTL ASIC input
106	***Val_Evt***				LVDS ASIC input (from DAQ)
107	***Val_Evt****				
108	***out_RazChn_int***				LVTTL ASIC output
109	***rst****				LVTTL ASIC input
110	***Raz_Chn***				LVDS ASIC input
111	***Raz_Chn****				
112	***CK_40M***				LVDS output (from DAQ)
113	***CK_40M****				
114	***CK_5M***				LVDS output (1/8 de 40M)
115	***CK_5M****				
116	***out_trig_int***				LVTTL ASIC output (NOR64 or ext)
117	***trigger_ext***				LVTTL ASIC input
118	***End_ReadOut***				LVTTL ASIC output
119	***Start_ReadOut***				LVTTL ASIC input
120	NC1				
121	***Start_Acq***				LVTTL ASIC input
122	**vddd2**				
123	***rst_counter****				LVTTL ASIC input
124	NC				
125	**vssd**				
126	NC				
127	**vssd**				
128	NC				
129	**vssd**	**gndd**			
130	NC				
131…	NC				
…148	NC				
149	**vssd**				
150	NC				
151	**vssd**				
152…	NC				
…174	NC				
175	**vssd**				
176	NC				
177	**vssd**				

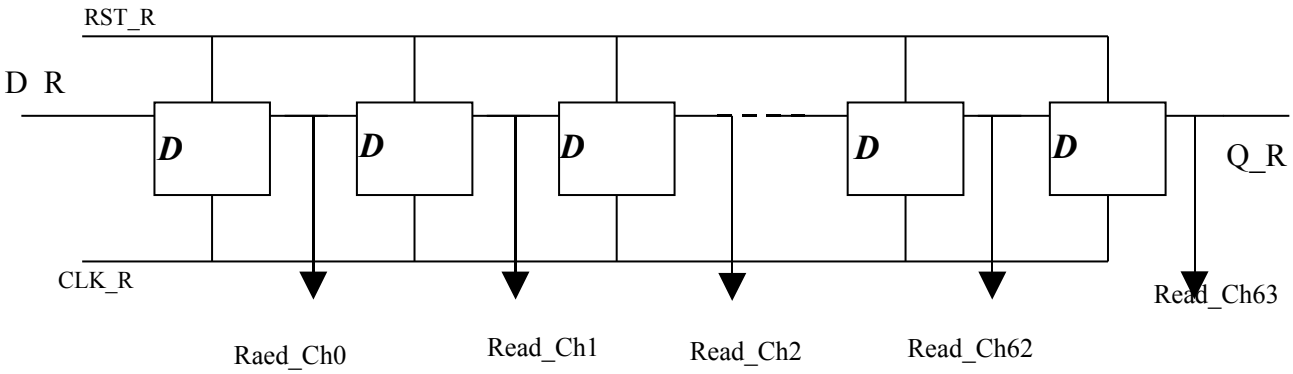
178	NC				
179	**vddd2**				
180	NC				
181	**rtn**	**rtn**			DC=0 ou 0,5V
182	***RamFull_ext***				LVTTL ASIC input
183	***RamFull****				OC ASIC output : LVTTL (testboard)
184	RamFull_007				Test point (Not Connected to DAQ)
185	***Dout****				OC ASIC output : LVTTL (testboard)
186	Dout_007				Test point (NC to DAQ)
187	***TransmitOn****				OC ASIC output : LVTTL (testboard)
188	TransmitOn_007				Test point (NC to DAQ)
189	***rst_SC****				LVTTL ASIC input
190	***Q_SC***				LVTTL ASIC input
191	***D_SC***				LVTTL ASIC input
192	***out_RS_trig1***				LVTTL ASIC output (to DAQ)
193	***CK_SC***				LVTTL ASIC input
194	***out_RS_trig0***				LVTTL ASIC output (to DAQ)
195	***pwr_on_ss***				LVTTL ASIC input
196	out_trig1				LVTTL ASIC output (Lemo)
197	***pwr_on_a***				LVTTL ASIC input
198	out_trig0				LVTTL ASIC output (Lemo)
199	**vddd**				
200	**vddd2**				
201	**gndd**				
202	**vssd**				
203	**vdd_d2**	**guard ring for discriminators**			
204	ibi_d		0.8V	27uA	100K to vdda
205	ibm_d		2.5V	25uA	100K to gnd
206	ibo_d				100K to gnd
207	**gnd_d**				
208	**vssm**				
209	**vssa**				
210	v_bg		2,5V		
211	**gnd_fsb1**				
212	out_fsb	**R115=1K instead of 10K**			**To decrease Slew Rate**
213	vref_fsb	**External 2.7K**	2V		2.7K external in / /(2.2K,300) to v_bg
214	ibo_fsb		2.3V	22uA	100k to gnd
215	**vdd_fsb**				
216	ibi_fsb		2.4V	41uA	60K to gnd
217	**gnd_fsb0**				
218	out_Q	**R115=1K instead of 10K**			**To decrease Slew Rate**
219	**vdd_w**				
220	ib_otaq	**External 2K to gnd**	1V	450uA	5592 to vdd
221	**gnd_w**				
222	**gnd_capa**				

223	EN_otaq				
224	ib_w		0.8V	11uA	25K to vdd
225	**gnd_ss**				
226	ibo_ss		0.8V	11uA	25k to vdd
227	**vdd_ss**				
228	ibi_ss		0.8V	11uA	25K to vdd
229	vref_ss		1,1V		(11K,14K) to v_bg
230	ib_buf				50K to vdd
231	**gnd_nmos**				
232	vgain_pa		3.5V		300//300 to vdd
233	**vdd_pa**				
234	ib_pa		0.7V	6uA	500K to vdd
235	**vssa**				
236	**vssi**				
237	**gnd_pa**				
238	in<0>	detector			
239	in<1>	detector			
240	**vssi**				

V. READ and SLOW CONTROL REGISTERS:

2 shift registers are integrated:
- One Read register to select (multiplex) one channel among the 64.

RST*:
0 => Reset all the registers *D to 0* → *empty the shift register* → *disable the output*



- One slow control register to load serially the 571 slow controls parameters:

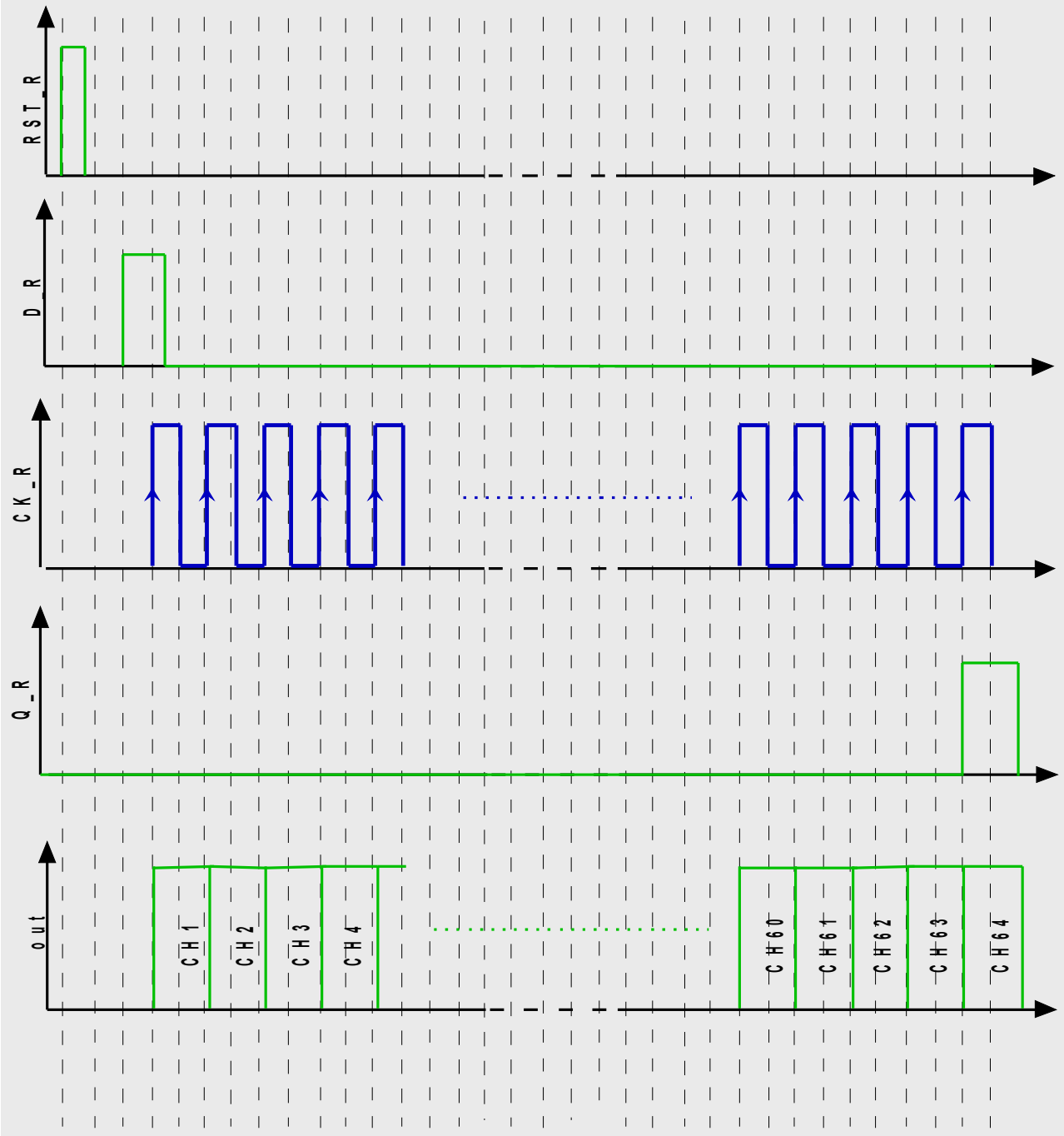
CELL	BIT#	BIT NAME
Dig_bias	**1**	**EN_RamFull**
	2	**EN_Dout**
	3	**EN_TransmitOn**
	4	**EN_out_discri**

	5	**Header 0**
	6	**Header 1**
	7	**Header 2**
	8	**Header 3**
	9	**Header 4**
	10	**Header 5**
	11	**Header 6**
	12	**Header 7**
	13	**bypass_chip**
	14	**EN_out_trig_int**
	15	**EN_trig_int**
	16	**EN_trig_ext**
	17	**EN_out_raz_int**
	18	**EN_raz_int**
	19	**EN_raz_ext**
	20	**Not used**
One_Channel0	**21**	**Valid_trig channel 0**
One_Channel1	**22**	**Valid_trig channel 1**
	…	**…**
One_Channel63	**84**	**Valid_trig channel 63**
dual_dac_10bits	**85**	**B0 0**
	86	**B0 1**
	…	**…**
	94	**B0 9**
	95	**B1 0**
	96	**B1 1**
	…	**…**
	104	**B1 9**
	105	**ON_otadac**
	106	**ON_dac**
	107	**ON_otabg**
One_Channel0	**108**	**Ctest ch 0**
One_Channel1	**109**	**Ctest ch 1**

	…	…
One_Channel63	171	Ctest ch 63

One_Channel0	**172**	**Preamp gain cmd0 ch 0**
	173	**Preamp gain cmd1 ch 0**
	174	**Preamp gain cmd2 ch 0**
	175	**Preamp gain cmd3 ch 0**
	176	**Preamp gain cmd4 ch 0**
	177	**Preamp gain cmd5 ch 0**
One_Channel1	**178**	**Preamp gain cmd0 ch 1**
	179	**Preamp gain cmd1 ch 1**
	…	…
	183	**Preamp gain cmd5 ch 1**
One_Channel2	**184**	**Preamp gain cmd0 ch 2**
	185	**Preamp gain cmd1 ch 2**
	…	…
	189	**Preamp gain cmd5 ch 2**
	…	…
One_Channel63	**550**	**Preamp gain cmd0 ch63**
	551	**Preamp gain cmd0 ch63**
	…	…
	555	**Preamp gain cmd0 ch63**
CELL	**BIT#**	**BIT NAME**
Bias	**556**	**ON_pa**
	557	**ON_buf**
	558	**ON_ss**
	559	**ON_w**
	560	**ON_otaq**
	561	**ON_fsb**
	562	**ON_discri**
	563	**Valid_DC**
	564	**Sw_50f**

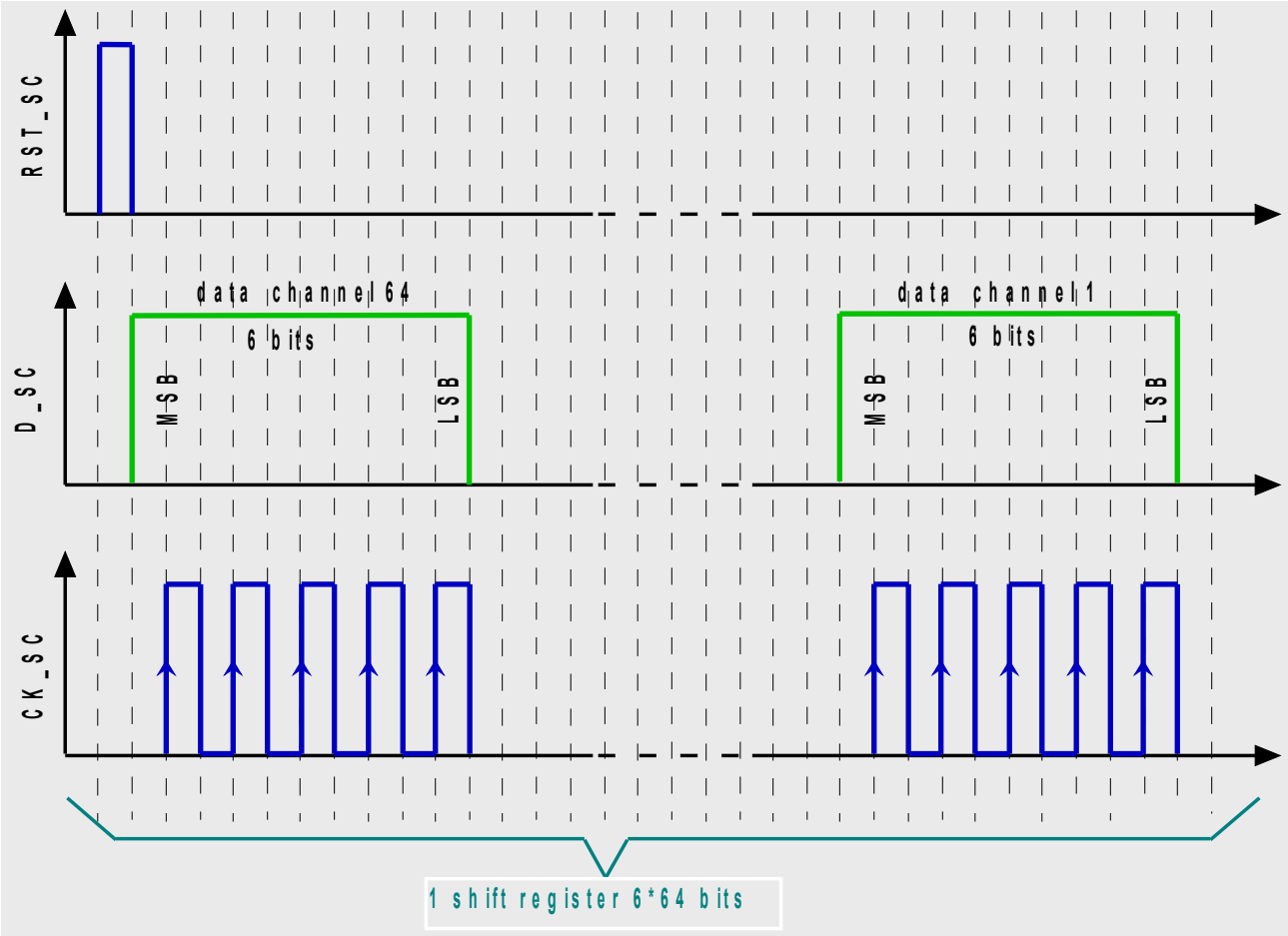
	565	Sw_100f
	566	Sw_100k
	567	Sw_50k
	568	Choix_caisson
	569	Sw_ssc2
	570	Sw_ssc1
	571	Sw_ssc0



SC register :

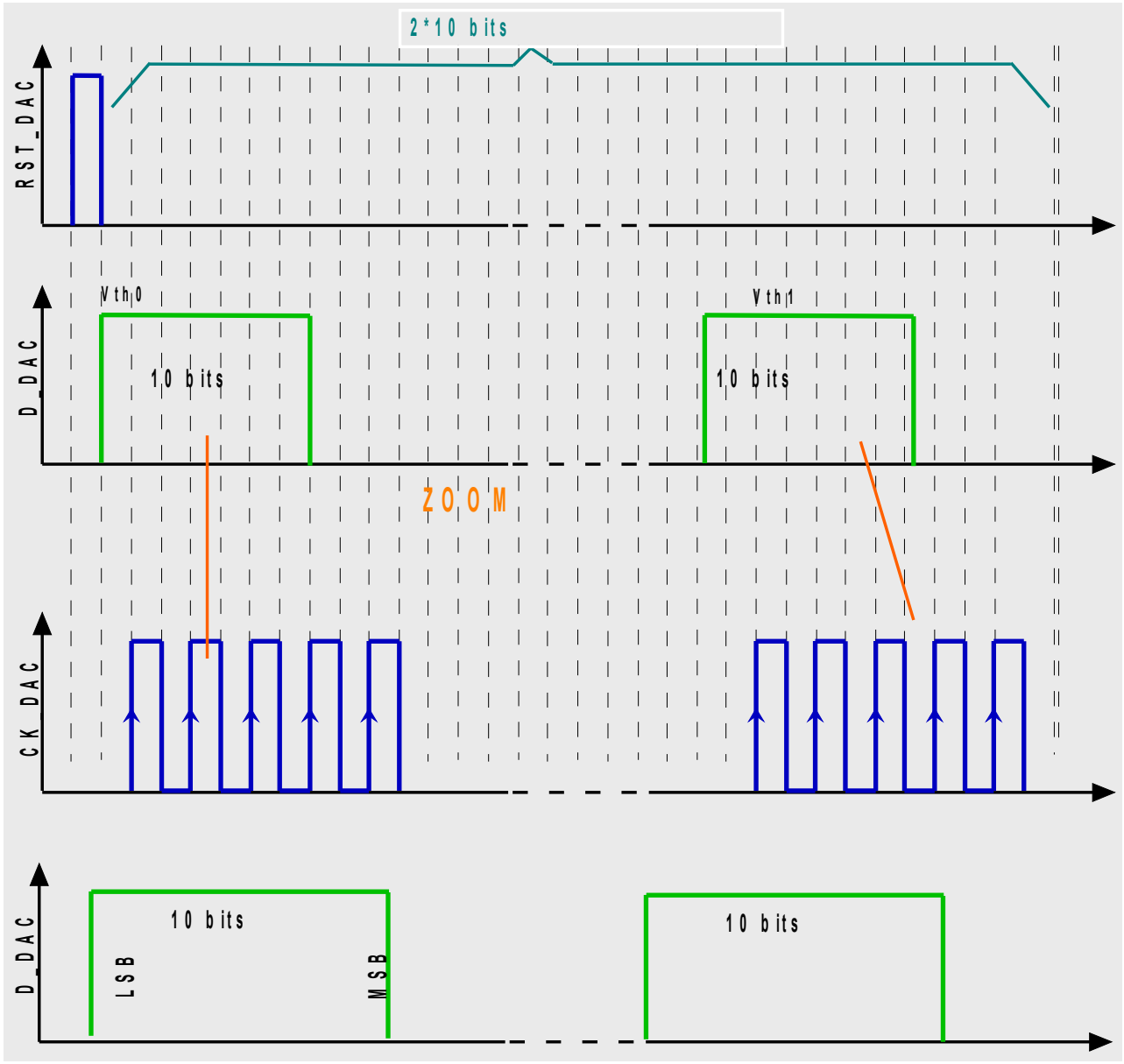
Gain value serial loading

Reset gain register: RST_SC*
D_SC, Q_SC, CK_SC
6 bits * 64 channels



DAC value serial loading

D_DAC, Q_DAC, CK_DAC
2 DACs, 10 bits per DAC


2*10 bits
RST_DAC
D_DAC
Vth0
10 bits
Vth1
10 bits
ZOOM
CK_DAC
D_DAC
10 bits
LSB
MSB
10 bits