110000

MODEL 1176
16 CHANNEL VME TDC

PRELIMINARY

CAUTION

Cooling

It is imperative that the Model 1176 TDC be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50° C.

Installation

Crate power should be turned off during insertion or removal of modules in accordance with the VME specification.

Specifications

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

Electrostatic Sensitivity

While measures have been taken to protect the MTD132A ASIC from electrostatic damage, it is still imperative to follow anti-static procedures when handling this CMOS device. Removal of the MTD132A from its socket may void the warranty.

Cautions

The user should eliminate any possible ground loops between the VME system and any other sytems, such as CAMAC crates.

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1. General Information

1.1. Purpose

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model 1176 Time-to-Digital Converter. In addition, it describes the converter's theory of operation and presents information regarding its function and application.

1.2. Unpacking and Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

1.3. Warranty

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

1.4. Product Assistance

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030, or your local field service office.

1.5. Maintenance Agreements

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering

improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

1.6. Documentation Discrepancies

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products.. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

1.7. Software Licensing Agreement

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

1.8. Service Procedure

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

1176 MULTIHIT TIME-TO-DIGITAL CONVERTER

- 1 nsec LSB
- 16-Bit Range, 65 μsec Full Scale
- Common START or STOP
- Multihit Capability, 16 Measurements (Hits)/Channel
- 20 nsec Double Edge Resolution
- Leading and/or Trailing Edge, Allows Pulse Width Measurements
- Chip Level Zero Suppression
- Prompt Trigger Outputs
- Multi-Event Buffer: 32 Events
- 16 Channels

TDCs FOR HIGH RATE ENVIRONMENTS

The 16-channel, VME Model 1176 Multihit Time-to-Digital Converter (TDC) has been designed for high rate environments. The module features a 16-bit dynamic range and 1 nsec LSB, 750 psec R.M.S. The double edge resolution is below 20 nsec. The module is ideal for time measurements of drift chambers, time projection chambers or other detectors requiring time interval measurements with high accuracy.

The Model 1176 can be operated in either a COMMON STOP or COMMON START mode. At the end of the acquisition period, the time elapsed between each hit and the COMMON STOP or START along with the address of the associated channel is made available for readout. Readout is via standard VME, and the data is automatically zero suppressed. A trigger port with prompt outputs is also provided.

FUNCTIONAL DESCRIPTION

The Model 1176 is based on the MTD132A, an application specific integrated circuit, which is an 8-channel, 16-bit dynamic range TDC circuit with 1 nsec least count. Arrival times can be recorded for either the rising, falling or both edges.

The COMMON input located on the front panel accepts standard ECL signals and has jumper connected, 110 W terminating resistors. By removing these jumpers the common signal can be daisy chained to several 1176 modules, as long as the last terminating resistors are left connected. This scheme eliminates the extra propagation delays caused by embedded repeaters and leaves only the very slight delays due to the cables (approximately 50 psec/cm).

Buffering time depends on the number of hits recorded. VME readout may start after buffering ends. The 1176 supports block transfer for faster readout.

An on-board tester delivers hits to all channels for functional verification. The number of hits and pulse width are programmable. A test cycle is initiated by writing to CSR0.

Prompt hit information is presented to an ECL auxiliary port for inclusion in first level trigger decisions. These prompt signals are compatible with the LeCroy ECLine series of logic units.

The Model 1176 is similar to the Model 2277 CAMAC TDC and the Model 1876 FASTBUS TDC. The 1176 serves as an ideal testbed for chamber developments. It supports 32 full size event buffers.

OTHER APPLICATIONS

By capturing both the leading and trailing edge time information, the 1176 can be used in a "time-over-threshold" technique to simultaneously determine the time and total charge collected (or, in some cases the time and peak value) for a given detector element using only one channel of TDC electronics. This technique avoids many of the traditional problems encountered with other methods, such as amplitude saturation, at a greatly reduced cost.

SPECIFICATIONS

VME CONTROL

VME Device Type: A24/D32/D16/D8 (EO) Slave.
Base Address: Front-panel switch selectable, A16-A23.
Address Modifier Codes: AM = 39, 3B, 3D, 3F.
DTACK: On valid address and no internal error.

GENERAL

Channels: 16, differential ECL inputs. Impedance 112 Ω. Unused inputs/outputs are allowed to float.
Common Start/Stop: Front panel ECL 2-pin connectors; 110 Ω jumpered terminating resistors.
Multi-Event Buffer: 32 events (the last hit in an event is marked by Bit 23 = 0).
Range: 16 bits.
Full Scale: 65.536 µsec.
Sensitivity: 1 nsec least count.
Double Edge Resolution: Can measure two dissimilar edges separated by as little as 20 nsec. Edges of the same polarity must be no closer than 40 nsec. This implies a double pulse resolution of 40 nsec.
Long Term Stability: 10 ppm/year.
Integral Non-Linearity: 10 ppm.
Differential Non-Linearity: ±0.2 LSB maximum.
Channel-to-Channel Pedestal: < ±1 nsec.
RMS Noise: 750 psec.
Digital Clear: 100 nsec.
Fast Clear Window (FCW): Starts at end of Time Range (Common Start) or at Common Stop. Can be programmed via CSR between 1 µsec and 128 µsec. During this period, the user can apply a FAST CLEAR to discard the event just captured.
Multiple Event Buffer: The digital data memory is logically organized as a FIFO, large enough to store the results of up to 32 events. A 5-bit event counter allows the user to keep track of how many events the readout is trailing the triggers.
Internal Tester: Even channels and/or odd channels may be tested. The tester generates square ware pulses (50% duty cycle). The pulse trains can have 1, 2, 4 or 8 cycles with half periods of 125, 250, 500, or 2000 nsec.
Buffering: 1.25 µsec + 125 nsec per hit.
Readout: VME readout can begin after Buffering in Progress is false and can continue at full VME speed.
Data Format: 16 bits data, 1 bit edge polarity, 4 bits channel address, 1 validity, 1 end of event.
Packaging: Single-width VME module in conformance with VME Specification (ANS/IEEE-1014). Height, 6 U.

FRONT PANEL LEDS

MODE: Bicolor LED indicates COMMON START/STOP.

ADDRESS: Yellow LED indicates VME address to module.

HIT: Green LED indicates whether any channel received a hit.

COMMON: Red LED indicates whether a COMMON START/STOP was received.

DIFFERENTIAL ECL SIGNALS

IN: Hit Inputs; 16 channels.

TRIG OUT: Fast Trigger Outputs; 8 outputs - pairwise OR'd channels.

BSY: Busy Output; indicates front end disabled due to buffering, acquisition disabled or module is full.

TIM: Timeout Input; determines Common Start acquisition window when enabled.

TST: Test Input; provides test pulses to the odd or even numbered channels, as programmed.

CLR: Clear Input; resets module - aborts conversion.

CM: Common Start/Stop Input; 2 bridged connectors.

ALLOCATION OF ADDRESS SPACE

0x0000 to 0x03FF:	Event 0
0x0400 to 0x07FF:	Event 1
.	
.	
.	
0x7C00 to 0x7FFF:	Event 31
0x8001 to 0x8003:	CSR
0x8000:	Acquisition Event Pointer

DATA WORD FORMAT

BIT(S)	FUNCTION	PATTERN	VALUE
0-15	DATA	0X0000-OXFFFF	
16	HIT PHASE	0	FALLING EDGE
		1	RISING EDGE
17-20	CHANNEL	0000	CHANNEL 0
		0001	CHANNEL 1
		0010	CHANNEL 2
		0011	CHANNEL 3
		0100	CHANNEL 4
		0101	CHANNEL 5
		0110	CHANNEL 6
		0111	CHANNEL 7
		1000	CHANNEL 8
		1001	CHANNEL 9
		1010	CHANNEL 10
		1011	CHANNEL 11
		1100	CHANNEL 12
		1101	CHANNEL 13
		1110	CHANNEL 14
		1111	CHANNEL 15
21	DATA VALID	0	GOOD DATA
		1	CORRUPT DATA
22	UNUSED		
23	LAST WORD	0	LAST WORD IN EVENT
		1	NOT LAST WORD IN EVENT

CONTROL REGISTER BIT CONFIGURATIONS

	BIT(S)	CONTROL FUNCTION	PATTERN	VALUE
CSR Byte 1	23	MODULE CLEAR	0	NO CLEAR
			1	CLEAR
	22-21	RESERVED		
	20	ACQUISITION	0	ENABLE
			1	DISABLE
	19	AUX FAST CLEAR	0	DISABLE
			1	ENABLE
	18, 17, 16	FAST CLEAR WINDOW	000	1 µsec
			001	2 µsec
			010	4 µsec
			011	8 µsec
			100	16 µsec
			101	32 µsec
			110	64 µsec
			111	128 µsec
CSR Byte 2	15	MODE	0	COMMON STOP
			1	COMMON START
	14	TRIGGER OUT MODE	0	LATCH
			1	PULSE
	13	HIT LEADING EDGE RECORDING	0	ENABLE
			1	DISABLE
	12	HIT TRAILING EDGE RECORDING	0	ENABLE
			1	DISABLE
	11	AUX COMMON	0	DISABLE
			1	ENABLE
	10, 9, 8	COMMON START TIMEOUT	000	500 nsec
			001	1 µsec
			010	2 µsec
			011	4 µsec
			100	8 µsec
			101	16 µsec
			110	32 µsec
			111	FP Controlled (< 64 µsec)
CSR Byte 3	7, 6	TESTER HIT DURATION	00	125 nsec
			01	250 nsec
			10	1000 nsec
			11	2000 nsec
	5, 4	TESTER HIT BURST	00	1 hit
			01	2 hits
			10	4 hits
			11	8 hits
	3	TEST ODD CHANNELS	0	DISABLE
			1	ENABLE
	2	TEST EVEN CHANNELS	0	DISABLE
			1	ENABLE
	1	RESERVED		
	0	INTERNAL TEST	0	CONFIGURATION MODE
			1	INTERNAL TESTER MODE

2. Product Description

2.1. Introduction

The LeCroy Model 1176 provides 16 channels of either Common Start or Common Stop multihit. multievent Time-to-Digital Conversion designed for elementary particle or nuclear physics experiments. All input time signals to be measured, "hits", are received via differential ECL (dECL) front panel inputs. Each channel exhibits 1.0 nsec LSB and can store up to 16 hits per event within a 65.536 μsec range. The time measurement is performed using the MTD132A, a full custom ASIC developed by LeCroy Corporation.

2.2. Product Description

The 1176 can be programmed to operate in either Common Start or Common Stop mode. When operating in Common Start mode, a hit window is required. This window of up to one full scale may be controlled via the front panel or by programming three bits in the control status register (CSR).

The 1176 has 16 channels of front panel hit inputs and a common input. All inputs are differential ECL (dECL) and are terminated by a balanced 110 ohm impedance matching network. Each channel can record up to 16 hits per event. Rising and falling edge detection is programmed globally in CSR. The double edge resolution is 20 nsec (double pulse resolution is 40 nsec). If more than 16 hits arrive at a given channel. the last 16 are retained. A 32 event deep buffer allows efficient VME data readout.

Trigger outputs are provided at the front panel in dECL. For trigger purpose only, the input pulses are pairwise ORed (0&1, 2&3, etc.).

The 1176 may be tested using either an internal tester or a front panel dECL TEST input. The internal tester can be programmed and activated via CSR. It generates hit and common pulse sequences with programmable duration and length (the internal tester generates the hits and the common in the right order based on the mode the 1176 is in). The test pulses may be applied to odd and/or even channels. The front panel TEST input is fanned out to all channels and allows testing with external signals, in which case an external common hit is required as well.

2.3. Specifications

- Standard VME 6U by 160mm single width.
- A24/D32/D16/D8(EO) VME module.
- Responds to the following address modifier (AM) codes: 39, 3B, 3D, and 3F.
- High speed VME block transfer rate; 10 Megabytes per second.
- Power: 3.5A at +5 volts, 0.1A at +12 volts.
- Please refer to the Model 1176 technical data sheet effective at the time of purchase for a complete summary of all relevant specifications.

2.4. Front Panel

The LeCroy Module 1176 TDC front panel provides the user with connectors for system integration and LEDs to assist system debugging. Cables necessary for proper installation can be purchased from LeCroy. See Section 3 for more information regarding cabling. Below is a drawing of the front panel of the 1176 TDC.

Figure 2-1 Front Panel

2.4.1. Displays

Five LEDs on the front panel of the 1176 indicate the status of operations and functionality. The LEDs are described in the order as they appear on the front panel - top to bottom:

- **MODE:** This bi-color LED indicates the mode in which the 1176 is operating: green = common start, red = common stop.
- **ADDR**: Flashes yellow each time the 1176 is addressed in VME.
- **COM**: Flashes red each time a common hit (start or stop) is received.
- **HIT**: Flashes green each time a hit on any channel is received.
- **PWR**: Indicates in green all power supplies are functioning.

2.4.2. Inputs and Outputs

Below the LEDs is the 34 pin hit inputs header, marked IN. The channels are arranged sequentially from channel 0 at the top to channel 15. The bottom pin pair is ground. The hit inputs are dECL, polarity is indicated.

The next header is marked TRIG OUT. It provides hit information for trigger purposes. It contains 8 dECL outputs, each represent two channels ORed together. The first channel of the pair is marked (0 for ch0 and ch1).

The control header contains 6 signals as described below:

- **BSY**: Busy output. This dECL output indicates the 1176 can't accept hits. this occurs either during MTD readout or when the multievent buffer is full.
- **TIM**: Timeout input. A dECL input used to receive an external common start timeout. The rising edge of this input, when selected, ends acquisition in common start mode.
- **TST**: Test input. A dECL input distribute hits to all odd and/or even channels, useful for testing the 1176 with reduced amount of cables. A common hit is still required with this input.
- **CLR**: Clear input. A dECL input used to fast clear events and abort acquisition or MTD readout. CSR and data from previous events is not affected.
- **CM**: Common input. A dECL input for the common hit. The time measurement is from the rising edge. Two inputs shorted together are provided for easy daisy chaining modules.

2.4.3. Address

At the bottom of the front panel are two hexadecimal rotary switches. These are used to set the module's unique VME address. (bits A16-A23).

2.5. VME Address Map

The 1176 TDC has a VME A24:D32:D16:D08(EO) slave interface and supports misaligned transfers. All memory addresses and CSR may be read and written into via VME. Block transfer cycles of up to 256 bytes are supported. In VME, each address refers to a specific byte. The following lists show the byte addressing to which the Model 1176 responds.

This example shows how if channel 0 for a single event has 16 hits could be readout.

0x0000	Reads Zero	D31-D24
0x0001	Channel 0 Event 0 Hit 0	D23-D16
0x0002	Channel 0 Event 0 Hit 0	D15-D8
0x0003	Channel 0 Event 0 Hit 0	D7-D0
0x0004	Reads Zero	D31-D24
0x0005	Channel 0 Event 0 Hit 1	D23-D16
0x0006	Channel 0 Event 0 Hit 1	D15-D8
0x0007	Channel 0 Event 0 Hit 1	D7-D0
.		
.		
.		
0x003C	Reads Zero	D31-D24
0x003D	Channel 0 Event 0 Hit F	D23-D16
0x003E	Channel 0 Event 0 Hit F	D15-D8
0x003F	Channel 0 Event 0 Hit F	D7-D0

From here on, we will use D32 terminology and refer to the address of the upper byte in a 32 bit word. In D32 operation, you normally address the upper byte and the lower bytes becomes included in the 32 bit word read or written. For D16, two reads or writes are performed to the appropriate upper byte and the appropriate lower byte comes along.

Address Structure	
A16-A23	Base Address (front panel switches)
A15	CSR
A1-A14	Data Space
A0	Undefined in VME

Address	Description
0x0000	Event 0
0x0400	Event 1
0x0800	Event 2
0x0c00	Event 3
.	
.	
.	
0x7400	Event 29
0x7800	Event 30
0x7c00	Event 31
0x8000	CSR
0x8004-0xffff	Invalid Addresses

2.6. Control and Status Register (CSR)

The 1176 TDC has a 32 bit Control Status Register (CSR) which contains the programmable status bits controlling the TDC's operation. CSR is divided into 4 fields as follows:

Bits	Field	Address (hex)
24-31	Event Counter	8000
16-23	Fast Clear	8001
08-15	Acquisition	8002
00-07	Tester	8003

The default value of CSR at power-up or sysreset is 0. Below is a description of the functions of CSR bits:

Event Counter Field:

31-30	Reserved
29	Event Buffer Full Flag
28-24	Event Counter, bit 28 is the MSB and bit 24 is the LSB

Fast Clear Field:

23	Clear (write only, reads 0).
22-21	Reserved
20	Disable Acquisition
19	Enable AUX Fast Clear
18-16	Fast Clear Window

Acquisition Field:

15	Acquisition Mode
14	Trigger Mode
13	Hit Rising Edge Registration
12	Hit Falling Edge Registration
11	Enable AUX Common Hit
10-8	Common Start Acquisition Timeout

Tester Field:

7-6	Tester Hit Duration
5-4	Tester Hit Burst
3	Enable Odd Channels Test
2	Enable Even Channels Test
1	Reserved
0	Execute Test Cycle (write only, reads 0).

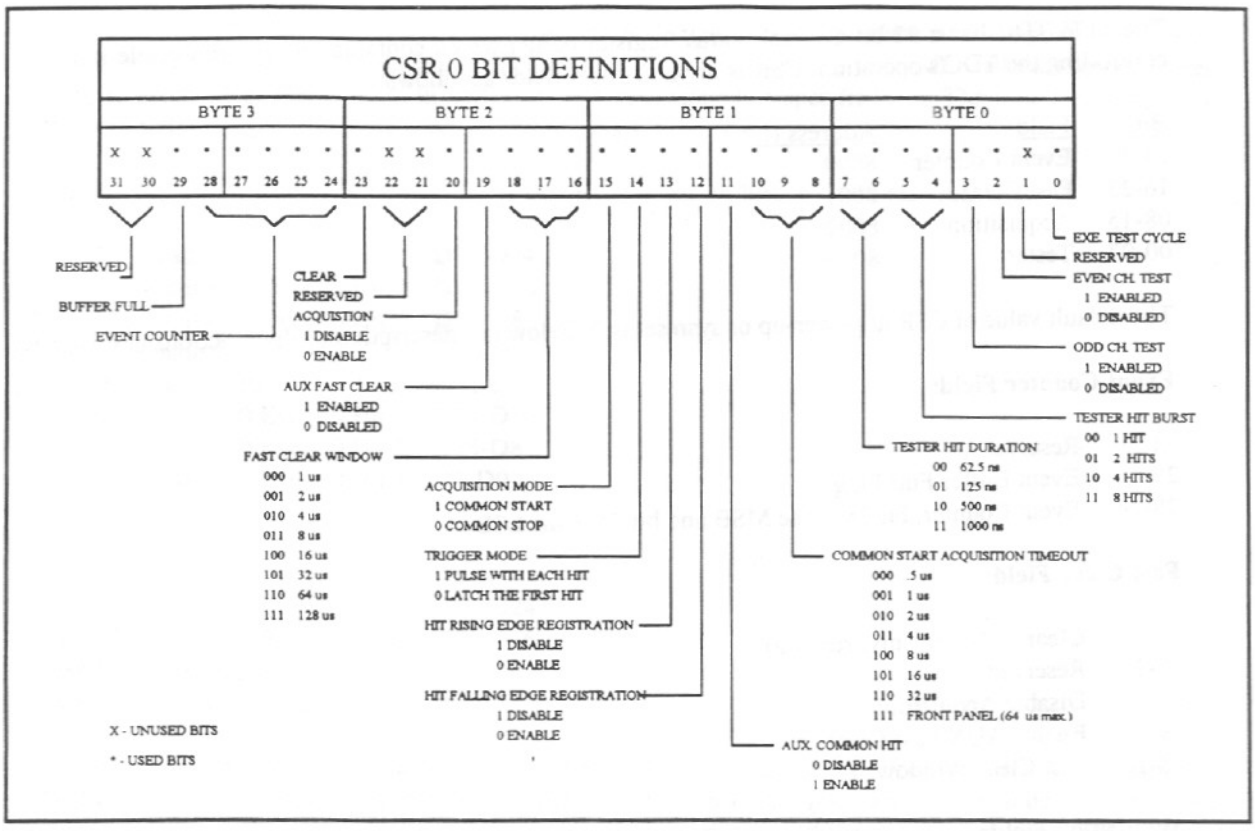

Figure 2-2 1176 CSR Bit Definition

2.7. Data Word Format

The 1176 data is read out as a 24 bit word. Bits 15-0 are the time data, bit 16 is the hit phase (denoting rising or falling edge by 1 or 0 respectively), bits 20-17 are the channel number, bits 22-21 are always 0, and bit 23 (=0) indicates the last word in the event. VME data byte 0 (bits 31-24) is unused and will read back always 0. In the case of an empty event, the word read will have bit 23 (last word) as 0 and bit 21 (valid) as 1.

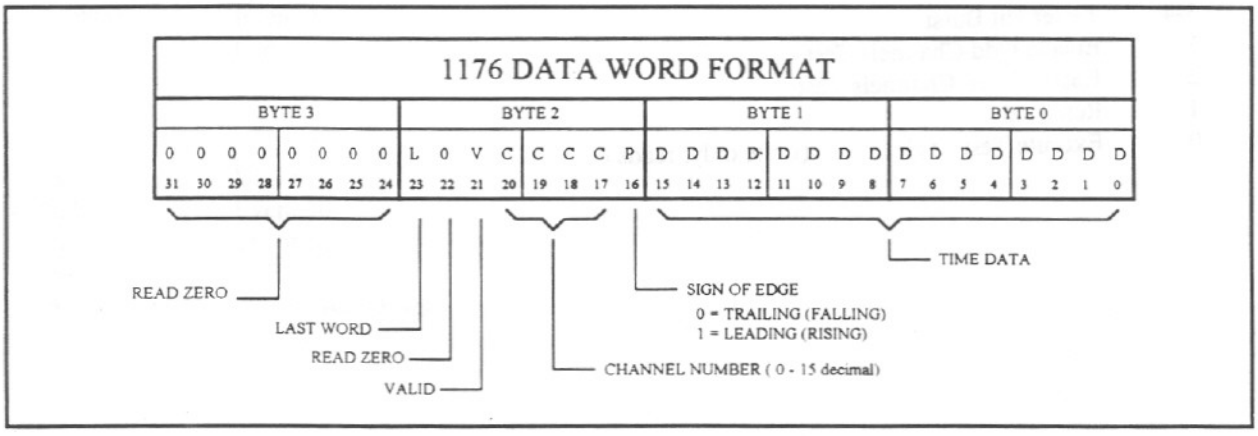

Figure 2-3 1176 Data Word Format

3. Installation

3.1. General Installation

The LeCroy Model 1176 TDC is intended for use within a standard VME crate. The following voltage sources must be properly connected to the backplane : +5 V, +12 V, and -12 V.

Before inserting the Model 1176 TDC into the VME crate, the VME base address must be set. The two address switches at the bottom of the front panel select the base address by specifying address bits <23:16> in hex. The upper switch (labeled 4-7) selects address bits <23:20>. A zero means no bits selected and F means all bits selected. The lower switch (labeled 0-3) selects address bits <19:16>. For example, if a base address of 0x250000 were desired, set the upper switch to 2 and the lower switch to 5.

3.2. Cables

The optimal method of cabling is use of coax cables as signal cables. They generally result in lower noise pick-up and less crosstalk. However, the use of twisted-pair cables generally results in lower cabling costs and typical higher density, thus the 1176 was designed to accept 34 connector ribbon cable. If using twisted-pairs, care should be taken to install high quality, shielded cables to minimize the effects of noise and crosstalk. Many of such cables can be purchased from LeCroy Corporation. In particular, there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The model numbers of such cables are as follows:

- **STC-DC /34/L** - flat multiwire cable for short interconnections.
- **LTC-DC /34-L** or **DC2 /34-L** - twisted-pair multiwire cable for long interconnection.
- **STP-DC /02-L** - single twisted-pair cable, 3 ft maximum length.

NOTE that L is the length in feet that must be specified by the user.

All inputs are differential ECL and terminated by 112 ohms. The terminations are SIP components and may be easily replaced to accommodate other characteristic impedances.

4. Operating Instructions

4.1. General Operation

The operation of the 1176 can be divided into four unique phases. The first phase includes all the setup necessary before the 1176 TDC can successfully be used. This includes installation of the module and programming the control register (CSR). The module will not latch hits until the control registers have been programmed. Once all the setup is complete, the module is in acquisition mode and ready to accept hits. The module remains in acquisition mode until either a Common Start Timeout or a Common Stop occurs, depending on the acquisition mode programmed. Following acquisition mode, the module buffers the data into a multiple event data buffer. During this stage the module asserts a Busy and no acquisition or VME readout may occur. If no fast clear is asserted during the user programmable Fast Clear Window (FCW), the data is saved and the module returns to Acquisition. VME readout of any event may be performed at any time the module does not assert Busy. The 1176 TDC saves data from events until the multi-event buffer is full, in which case acquisition is disabled until either a reset is issued or the data is readout.

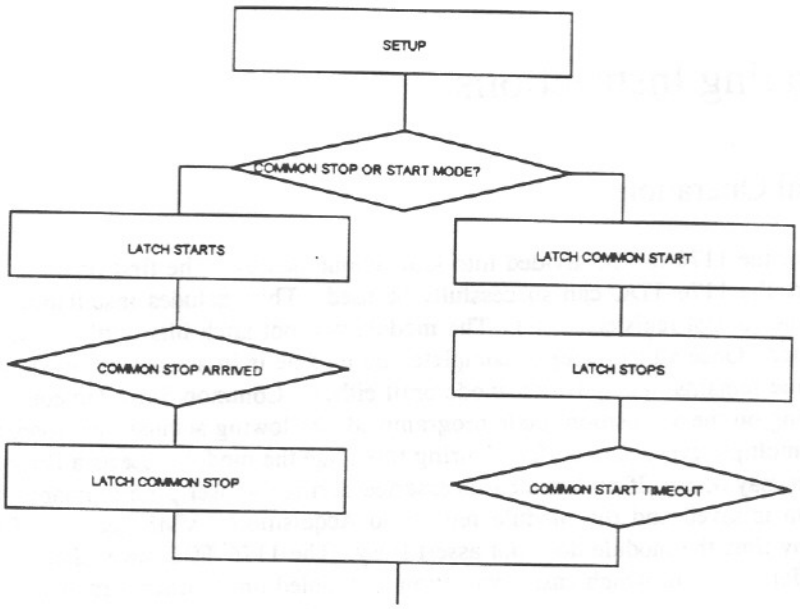

Figure 4-1 1176 General Operational Flowchart

4.2. Common Start vs. Common Stop Modes

The LeCroy Model 1176 TDC was designed to operate in both Common Start and Common Stop modes. Sensitivity for the individual channel input pulses can be programmed in CSR register either hits rising edges, falling edges or both. In either mode, channels can store up to 16 hits arrival times. The common hit is always measured from the rising edge.

When in Common Stop Mode, the individual hit pulses must precede the common stop. The hits are received via the front panel inputs marked IN, and the common is received via either of the front panel inputs marked COM or via the backplane if enabled. Time is measured from the enabled hits edges to the rising edge of the common. In either mode the last 16 hits are saved with earlier hits discarded. Only one (the first) common hit is accepted per event.

Figure 4-2 demonstrates proper timing of the signals in Common Stop mode where 16 hits have been provided via the hit input and a stop pulse has been provided via the common input. After a power-on causing a Power On Reset (POR) pulse to the module, the 1176 is in Acquisition and ready to accept hits provided CSR has been properly programmed. If both hit edges were enabled, all 16 hits shown in the figure would be latched. the leading edge of the Common ends acquisition and disable the acceptance of further hits. The common must be at least 20 nsec wide and the trailing edge must arrive before readout can occur. The front end is disabled from accepting inputs while BUSY is asserted.

When operating in Common Start Mode, a full scale timeout is required. The hit window determined the period during which the module will latch hits. The hit window begins at the arrival of a common start and end with the timeout pulse. The common start timeout is programmable in CSR or may be provided via the front panel input marked TIM. The module times out after 64 usec by default. Hits arriving after timeout are discarded.

Figure 4-3 demonstrates proper timing of the signals in Common Start Mode where a start pulse has been provided via the COM input and 16 hits have been provided via the IN inputs. As in Common Stop Mode, the 1176 enters acquisition immediately after POR provided CSR is properly programmed. The 1176 will latch all edges arriving between the leading edge of the common hit and the timeout pulse. In either mode there must be at leasts 20 nsec between selected edges to be properly latched. (double edge resolution)

Note that the scale at the bottom of the figure is in nsec.

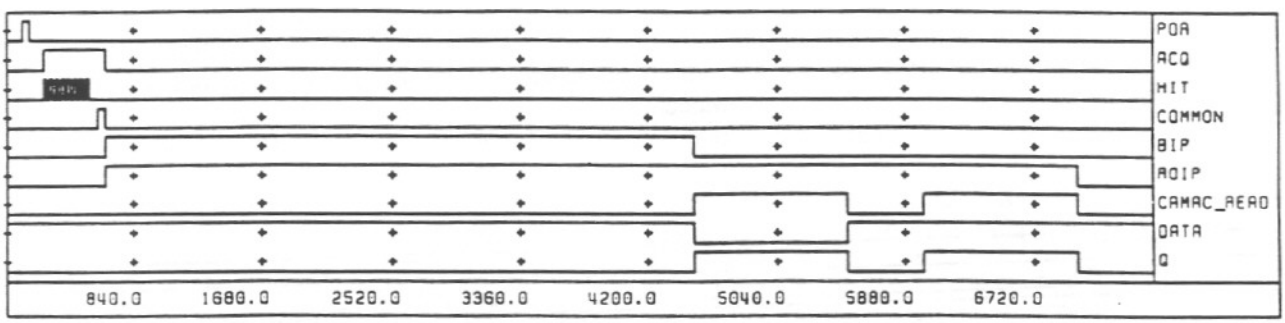

Figure 4-2 An example of proper signal timing for operation in Common Stop Mode

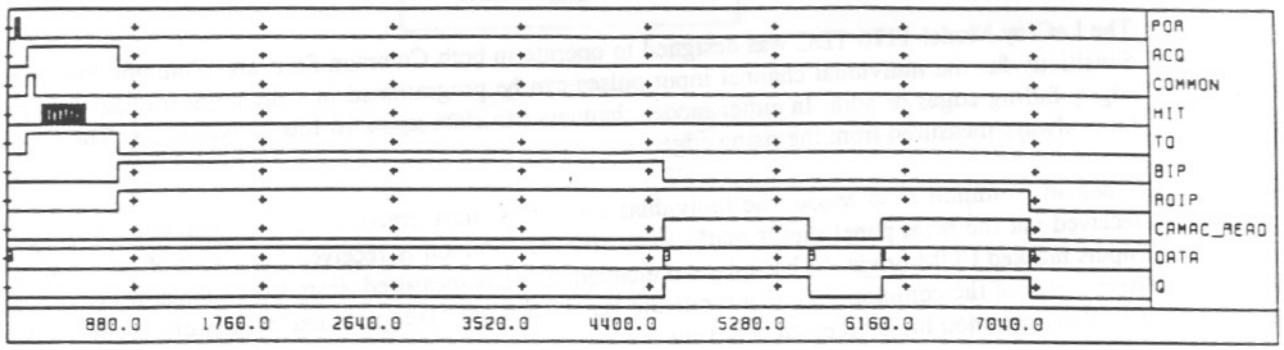

Figure 4-3 An example of proper signal timing for operation in Common Start Mode

4.3. Pulse vs. Latch Mode

Eight dECL front panel trigger outputs marked TRIG OUT are available to the user for external trigger logic. Neighboring channels are pairwised ORed (0&1, 2&3, etc.) to produce a true trigger out when either of the channels receives a hit. The trigger outputs can be programmed to operate in either a Pulsed or a Latched Mode by programming bit 14 in CSR. (see section 2.7) When in Latch Mode, the trigger outputs are cleared by either a fast clear, VME reset or the completion of the MTD132 data buffering. In Pulse Mode the trigger outputs remain active 20 nsec after a hit.

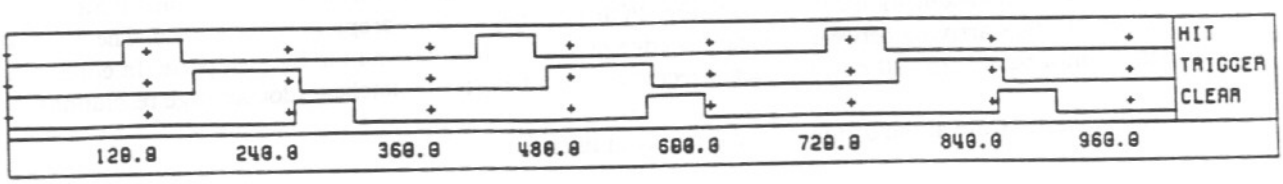

Figure 4-4 Example of timing relationship between hits and the trigger outputs when operating in Latch Mode

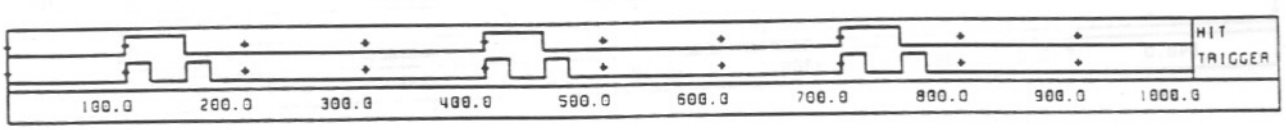

Figure 4-5 Example of timing relationship between hits and the trigger outputs when operating in Pulse Mode

4.4. Front Panel Control Signal Inputs

All front panel control signals are dECL and are terminated by 112 Ω as shown. The terminations are SIP components and may be easily replaced to accomodate other characteristic impedances.

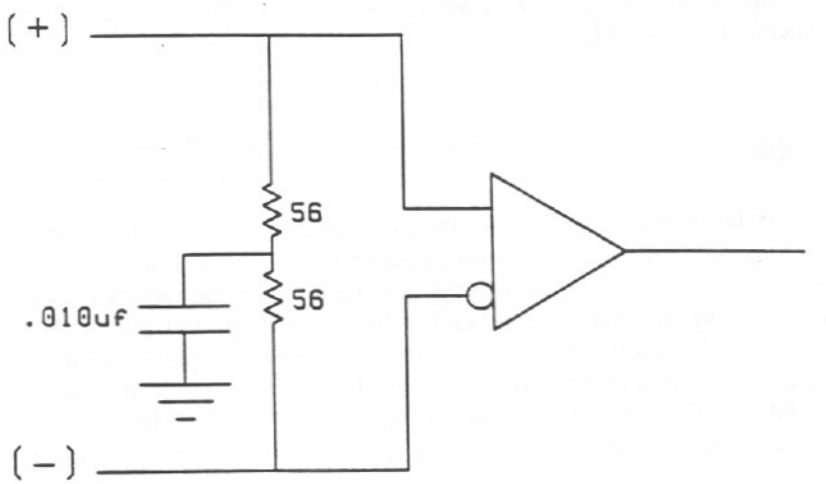

Figure 4-6 ECL Terminations

4.5. Readout

The user may read out data from any event providing the 1176 TDC is not buffering data at the same time. The current event number can be obtained by reading the value of the event counter at address 8000. Each event has a dedicated memory address range of 256 words (16 hits times 16 channels). The memory is 4 bytes wide, of which 3 bytes contain the data word and the fourth is all zeroes. The first address of the selected event to be read out is loaded on the VME address bus (bits 14 - 10) with bit 9 - 0 starting at 0 for the address of the first hit data and then incremented, based on the mode of VME readout, (D32 at one word per read cycle, D16 at one word per two read cycle or D08 at one word per three read cycles, providing byte 0 is not read out), until all data of this event is read out. This is determined by testing bit 23 of each data word. The FIRST data word in a given event which contains a 0 at bit 23 is the LAST word of the event. In case no hits occurred at a given event, the first word to be read out will have bit 23 equals 0 AND bit 21 - INVALID - will be TRUE. In all events with valid hits bit 21 is always 0.

NOTE: Readout of a given event MUST end with the first data word which has bit 23 = 0. Old data from previous events may be still stored in memory and be confused with the new data if bit 23 is not tested for all data words.

When the readout of a given event is completed, the next event is accessed by incrementing the event address (bits 14 -10) while zeroing the hit address (bits 9 - 0). The readout typically continues until all events are read in which case the event address is one less than the event counter. Once readout is completed, the event counter should be cleared by writing a 0 into address 8000. The next event to be acquired will be number 0. Failure to zero the event counter will eventually result in a FULL signal as all 32 events are buffered. The 1176 TDC will then disable further acquisition until the event counter is not full. The FULL flag bit 29 of CSR (read only).

40	8002	Common Stop, En Rise, Fall
ff	8003	Test Cycle: 8 Pulses, 1000ns to odd and even channels.

This will create an full event with 16 hits on all 16 channels, a total of 256 32-bit words. The event counter should be set to 0 (write 00 to 8000) as soon as buffering is complete (BUSY is false). The data can be read in either D08, D16 or D32 mode. Each data word takes 4 bytes, of which byte 0 (31-24) is always zero. The whole event will take 1kb. Please refer to section 2.7 - Data Word Format for data interpretation. Note that the last word in the event is marked (bit 23 = 0).

To test the module in Common Start mode, repeat step 4 with c7 written to address 8002. Other test patterns can be generated. see section 2.6 - CSR.

4.9. Testing the 1176 Using The Test Input

1. Install the module in the crate as explained in the Installation section.

2. Power up the crate.

3. Issue a Master Reset to the module using SYSRESET or writing a one to CSR bit 23 (data 80 address 8001).

4. Initiate CSR using D08 mode with the following data:

Data	Address	Action
00	8000	Reset Event Counter
00	8001	Set FCW 1us, enable ACQ
40	8002	Common Stop, En Rise, Fall
0c	8003	En odd and even channels.

5. Provide an external common stop pulse by connecting a twisted pair cable from an external generator to the front panel input marked COM. Provide external hits by connecting a twisted pair cable from an external generator to the front panel input marked TST. Make certain that the hits (into TST) reach the TDC before the COM.

6. Wait for the buffering to complete (BSY false). The event counter should be then set to 0 (write 00 to 8000). The data can be read in either D08, D16 or D32 mode. Each data word takes 4 bytes, of which byte 0 (31-24) is always zero. Please refer to section 2.7 - Data Word Format for data interpretation. Note that the last word in the event is marked (bit 23 = 0).

To test the module in Common Start mode, repeat step 4 with C7 written to address 8002. Make certain that the COM reaches the TDC before the hits (into TST). Other configurations are possible. See section 2.6 - CSR.

4.10. Example Code

```
/*
 inttest.c
 1176 internal tester function.
 version 1.0
*/
#include <stdio.h>
#include <inttest.h>
#include <graph.h>
#include <key_def.h>
#include <rsdutil.h>
#include <color.h>
#include <vmelib.h>

void test_pulse(unsigned long base_address)
{
 unsigned long address, priority[256], hit_phase[256];
 unsigned long data_valid[256], channel[256];
 unsigned long data[256], rawdata[256];
 unsigned long csr0_address, event, mtd[256];
 unsigned long csr0_word, rd_event, event_num;

 unsigned int i, newi, event_word, int_csr0;
 unsigned int temp;

 char scratch[80];

 /* Send a reset to the vme bus. */
 /* This is necessary if the 1176 is plugged in with power on. */
 vme_reset();

 /* Write to CSR0, trigger the internal tester. */
 csr0_address = base_address + 0x8000;

 /* Enter the number of events to test. */
 do {
   grintf(7, 20, YELLOW, BLACK, "Enter number of events (1 to 32):  ");
   scanf("%d", &event_word);
 }while( (event_word < 1) || (event_word > 32) );
 /* Clear screen text. */
 grintf(7, 20, YELLOW, BLACK, "                                    ");

 /* Enter a control word for csr0. */
 do {
   grintf(7, 20, YELLOW, BLACK, "Enter a control word for CSR0 (000000 to FFFFFF):  ");
   scanf("%x", &csr0_word);
 }while( (csr0_word < 0x000000) || (csr0_word > 0xffffff) );
 /* Clear screen text. */
 grintf(7, 20, YELLOW, BLACK, "                                              ");

 /* Cause conversions to take place using internal tester. */
```

```
do {
  int_csr0 = (unsigned int)(csr0_word & 0xffff);
  wr_vme((csr0_address + 2), (int_csr0 + 1));
  event = (rd32_vme(csr0_address) & 0x3f000000) >> 24;
  event_word--;
}while(event_word != 0);

/* Reset the 1176 to prepare for readout. */
/*vme_reset();*/

/* READOUT LOOP. */
/* Get the event count and test for buffer full. */
event = (rd32_vme(csr0_address) & 0x3f000000) >> 24;
if ( event == 0x20) {
  grintf(4, 20, YELLOW, BLACK, "BUFFER is FULL");
}
event_num = event;
rd_event = 0;
/* Read out data. */
do {
  event_num = event_num - 1;
  for (i = 0; i < 256; i++) {
    address = base_address + (event_num << 10) + (i << 2);
    rawdata[i] = rd32_vme(address) & 0x00ffffff;
    /* Format the data bits. */
    data[i] = rawdata[i] & 0x0000ffff;
    hit_phase[i] = (rawdata[i] & 0x00010000) >> 16;
    channel[i] = (rawdata[i] & 0x000e0000) >> 17;
    mtd[i] = (rawdata[i] & 0x00100000) >> 20;
    data_valid[i] = (rawdata[i] & 0x00200000) >> 21;
    priority[i] = (rawdata[i] & 0x00800000) >> 23;

    /* Print out data on screen. */
    grintf(5, 20, YELLOW, BLACK, "EVENT PRIORITY VALID MTD  CH PHASE DATA");
/*  temp = (unsigned int) rd_event;*/
    _settextcolor(CYAN);
    _settextposition( (6 + i), 20);
    sprintf(scratch, "%4lX %4lX    %4lX %4lX %4lX%4lX   %4lX", event_num, priority[i],
                        data_valid[i], mtd[i], channel[i], hit_phase[i], data[i]);
    _outtext(scratch);
    newi = i + 1;
    if (priority[i] == 0) {
/*                  printf("STOP");*/
    break;
    }
  }
  /* Hit the enter key to display the next events results. */
 do {
    grintf(22, 30, YELLOW, BLACK, "HIT ENTER FOR NEXT EVENT");
 while(getkey() != ENTER);
 /* Increment the read event counter. */
 rd_event++;
}while(rd_event != event);
/* Wait for key hit to exit routine. */
do {
```

```
    grintf(23, 30, RED, BLACK, "Hit ESC to EXIT.");
  }while(getkey() != ESC_KEY);

  /* clear screen before exiting function */
  _clearscreen(_GCLEARSCREEN);  /* Clear the output screen    */

}/* End main. */
```

5. Theory of Operation

At the heart of the LeCroy Model 1176 TDC is the MTD132. The MTD132 is an eight channel Time to Digital Converter (TDC) implemented as a full custom ASIC. It combines a synchronous counter and a asynchronous interpolation system with eight parallel channels. Each channel is capable of recording the arrival of sixteen pulse edges with sixteen bit dynamic range. Both Common Start and Common Stop operations are supported. On-chip sparse data readout is implemented, with all possible ambiguities resolved.

5.1. Gray Code Counter Coarse Time Measurement

A sixteen bit gray code counter provides the backbone of the time measurement system. This counter is executed using a bitwise pipelined and interleaved divide by two technique. Two-way interleaving permits the count frequency to be double that of the counter clock frequency. The counter output is buffered and distributed to the eight channel memories and to the common register. The fourteen LSB of this counter in conjunction with the analog delay section form the time measurement. The remaining MSB's are used for stale data detection.

The counter includes a reset capability. The MTD132A has a reset input which is used to clear the counter and data memories, etc. The counter is zeroed during a clear. In general, the clear input is used only on power on, and to destroy the data from the hit memories and the trigger latches.

5.2. Asynchronous Delay Line Time Interpolation

To increase the resolution of the TDC beyond that provided by the counter, an asynchronous delay line interpolator is incorporated. This consists of three tapped delays. The input to the first tap is fed by one of the counter clock phases. Each delay tap consists of a current controlled starved inverter followed by a conventional inverter. The current starved inverters allow some of control over tap delay.

Following the delay line tap outputs are buffers identical to those used by the counter. The state of the delay line is stored along with that of the coarse counter for each hit.

5.3. Common Input Latch

The buffered counter and delay line outputs are transmitted to both the channel memories and to a "common hit" register. This is used to record a Common Start or Common Stop value. The meaning is relevant only to the operation of the output data processor, not to operation during data collection.

5.4. Rising and Falling Edge Detection

The MTD132A allows the selective recording of rising (leading), falling (trailing) or both edges on channel inputs. These modes are selected using two CMOS input pins. These inputs are not latched and must be maintained at the selected values during chip operation. The leading/trailing edge nature of the time measurement is recorded on hit arrival and presented during read-out.

5.5. Test Input

A mechanism for stimulating channels for test and calibration purposes is included. During the acquisition period, a pulse on the TEST input can register all the odd and/or even channels based on the programming of the status register. The edge(s) recorded depends on the state of the edge selection inputs. The channels essentially OR their test and hit inputs. No distinction is made between test and hit inputs during read-out.

5.6. Data Processor

During read-out of the MTD132A, the data from the common latch and the individual channel memories are converted to binary and subtracted from each other. This produces the time difference between the individual channel input pulses and the common pulse. The direction of the subtraction is determined by the mode of operation - Common Start or Common Stop. All this data processing is done in a pipelined fashion to expedite data read-out.

5.7. Read Only Memory Channel Number Encoding

A means of identifying which channel each data word is read from is necessary, because channels may be skipped entirely, and a variable number of words read out from each channel. A small read only memory is used inside the MTD132A to produce a one of eight to three bit binary encoding of channel number. As a chip is activated for read-out, the ROM word associated with the channel is activated, and the resulting encoded position is transmitted off chip by a set of three tri-state output pads. In addition, it is necessary to identify which chip is active when many chips share a data bus. A Chip Active flag becomes valid when a chip is reading out. The Chip Active flags are encoded externally for chip identification

5.8. Sparse Data Priority Readout System

The MTD132A has a sparse priority read-out system. Only potentially valid words are read out of a given MTD132A. Empty words, empty channels and even empty chips are skipped over transparently. This system of priority search is extended to multi-chip systems, such as is the case with the 1176, by the propagation of a priority search flag between chips. Two pins, Priority In and Priority Out receive and transmit the signals.

A chip level look-ahead is used to speed up the search function. The Priority Input does not go directly into the first channel's search string. Rather, the input to the first channel is always set as though no previous channel assumes priority. The search proceeds in each chip in parallel - the first channel with priority in each chip is found. The Priority Out flag is just the OR of the chip Priority In flag and the priority out of the last channel. The Priority In flag is used to inhibit read-out in chips which do not have priority. In this way, a large speed improvement is obtained in systems that daisy chain many chips.

5.9. Wire-OR'ed Trigger Outputs

Each pair of channels in the MTD132A maintains an SR flip flop that is set when a hit or test input arrives. The edge at which this occurs is determined by the state of the leading and trailing edge selection. These four OR'ed values are transmitted off chip by modified CMOS output buffers. A mode control pin determines the function of the trigger outputs making them latching or transparent. When high, the trigger outputs are transparent, pulsing low briefly each time a selected edge arrives on the appropriate channel hit input. When low, the trigger outputs are latched. The trigger flip-flops are cleared during a chip reset. Once off-chip the trigger outputs are buffered and provided at the front panel outputs.

5.10. Readout Data Processor

Data from channels are combined with the common hit latch externally to identify which chip is being read out. The middle delay line tap data becomes the second least significant bit, and an XOR of the first and third tap data becomes the least significant bit. The fourteen course counter bits become bits 2 to 15 (of 0 to 15).