System Requirements Specification

Cosmic Calibration Test Bench

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Summary

1 APPLICATION FIELDS 7

1.1 DOCUMENT IDENTIFICATION 7
1.2 SYSTEM PRESENTATION 7
1.3 DOCUMENT OVERVIEW 7

2 REFERENCES 9

3 SYSTEM REQUIREMENTS 10

3.1 COSMIC CALIBRATION TEST BENCH OVERVIEW 10
3.2 SYSTEM INTERFACES REQUIREMENTS 12
3.2.1 Interface 1: user actions on bench computer 12
3.2.2 Interface 2: VFE-PCB interaction with acquisition sub-system 12
3.2.3 Interface 3: Scintillators planes and hodoscope sub-system 14
3.2.4 Interface 4: Acquisition sub-system and hodoscope sub-system 14
3.2.5 Interface 5: Acquisition sub-system and bench computer 15
3.2.6 Interface 6: Hodoscope sub-system and bench computer 15
3.3 SYSTEM CAPABILITIES REQUIREMENTS 15
3.3.1 Functionality 1: Manage scintillators power supply 16
3.3.2 Functionality 2: Monitor particle track 16
3.3.3 Functionality 3: Manage the trigger 16
3.3.4 Functionality 4: Timing for device under test 16
3.3.5 Functionality 5: Acquire data from device under test 17
3.3.6 Functionality 6: Store acquired data 17
3.3.7 Functionality 7: Calibration 17
3.4 SYSTEM TIMING REQUIREMENTS 17

4 GLOSSARY 18

5 ANNEXE A: USB I/O 24 MODULE 19

5.1 PRESENTATION 19
5.2 FEATURES 19
5.3 SERIAL NUMBERS 19

6 ANNEXE B: USB INTERFACE FOR VFE CALIBRATION CONTROL 20

7 ANNEXE C: USB INTERFACE FOR HODOSCOPE SUB-SYSTEM CONTROL 21

List of figures

Figure 1. Cosmic Calibration Test Bench Overview. 10
Figure 2. Detailed overview of the Cosmic Calibration Test Bench system architecture. 11
Figure 3. Timing sequence for VFE-PCB..... 13
Figure 4. Disposition of scintillator planes for particle track monitoring. 14
Figure 5. View of USB I/O 24 Module. 19

List of arrays

Array 1. Details for requirement abbreviations. 8
Array 2. USB I/O 24 Module Interface for Calibration sub-system. 20
Array 3. USB I/O 24 Module Interface for Hodoscope sub-system. 21
Array 4. Pin configuration to read part of particle track position. 21

1 APPLICATION FIELDS

1.1 Document Identification

This **S**ystem **R**equirements **S**pecification (SRS) concerned the Cosmic Calibration Test Bench developed for the FLC – CALICE experiment. It describes the entire (hardware and software) architecture of the system identified by the reference: BENCH1002.

1.2 System Presentation

The main purpose of this test bench is to provide an environment to debug, characterize, calibrate and validate a particle detector. The device under test may have the capability to detect the cosmic particles.

The Cosmic Calibration Test Bench have the following capabilities:

- monitoring the cosmic particle tracking,
- generate the timing for the device under test (particle detector),
- generate the timing (trigger) for data acquisition,
- read and store the cosmic particle detection impact on device under test,
- calibrate the device under test.

The first application for this Cosmic Calibration Test Bench is the FLC – CALICE VFE-PCB test, characterization, validation and calibration. This test bench should be as generic as possible in hardware or software components.

For future applications, the Cosmic Calibration Test Bench may evolve with new hardware and software capabilities, especially with the device under test interface.

1.3 Document Overview

This document describes the requirements to satisfy for the Cosmic Calibration Test Bench. It defines:

- the capabilities of the system,
- the interface between the system and his environment,
- the timing constraints,
- the conception constraints.

This document is used as a reference document for hardware and software conception of the system. All requirements can be marked with the following styles:

⇒ SRS_HWI_REQ_n.m **Title** **[parent]**

or:

⇒ SRS_SWI_REQ_n.m **Title** **[parent]**

or:

⇒ SRS_INT_REQ_n.m **Title** **[parent]**

All abbreviations used for requirement are detailed in the following array (Array 1).

Fields	Description
SRS	**S**ystem **R**equirements **S**pecification.
HWI	**H**ard**W**are **I**tem.
SWI	**S**oft**W**are **I**tem.
INT	Interface between two items.
REQ	Requirement description abbreviation.
n	ID of the requirement on the capability or interface.
m	(optional) ID of the sub-requirement of the requirement **n**.
Title	(optional) To remind the requirement object.
[parent]	(optional) The parent requirement description abbreviation for sub-requirements only.

Array 1. ***Details for requirement abbreviations.***

The description of the requirement is marked with a double line on the top and on the left of the description text like this:

Requirement description …

2 REFERENCES

We describe in this paragraph all documents we used to write this system specification.

Document [1]: "Cosmic Bench – System Architecture"
Presentation done in March 2003, small summary of the architecture we will use for Cosmic Calibration Test Bench.
Authors: Franck Gastaldi (LLR), Simon Chollet (LLR).
Reference: LLR1002-PPT-System Architecture-1.0.
Revision: March 2003.

Document [2]: "VFE-PCB Test Bench – Level 0 – Proposal"
Presentation of the Cosmic Calibration Test Bench.
Authors: Franck Gastaldi (LLR), Simon Chollet (LLR).
Reference: LLR1002-PPT-VFE_PCB Test Bench-1.0.
Revision: March 2003.

Document [3]: "FLC_PHY2 – Front end chip datasheet"
Datasheet for the VFE-PCB ship: FLC_PHY2.
Authors: Julien Fleury (LAL).
Reference: –.
Revision: May 2003.

Document [4]: "FLC_PHY2 – Calibration Interface"
Interface for calibration of the FLC_PHY2 ship.
Authors: Julien Fleury (LAL).
Reference: –.
Revision: May 2003.

3 SYSTEM REQUIREMENTS

Before enumerating all requirements for this system, we will describe an overview of the Cosmic Calibration Test Bench with its sub-systems.

3.1 Cosmic Calibration Test Bench Overview

The following figure (Figure 1) presents all main items used to develop the Cosmic Calibration Test Bench.

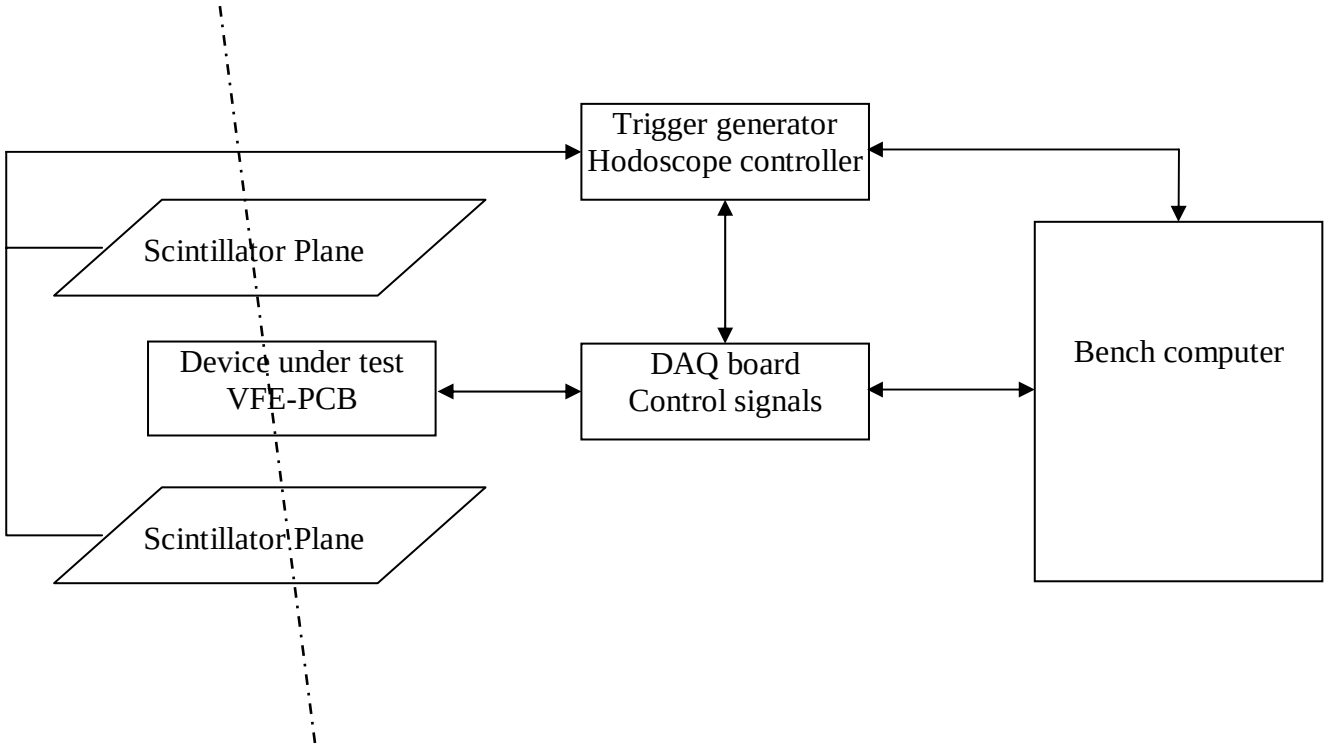

Figure 1. Cosmic Calibration Test Bench Overview.

For the FLC-CALICE experiment, the device under test is the VFE-PCB done by the LAL. This device is constituted of **6** silicium wafers and **12** FLC_PHY2 ships.

There are two scintillators planes to detect and monitoring the particle track. Each scintillators plane has **32** photomultipliers: **16** for X direction, **16** for Y direction. The position (X, Y) of the particle track is calculated with all scintillators planes: a couple of (X, Y) coordinates: (X_1, Y_1) and (X_2, Y_2).

The “Trigger generator / Hodoscope controller” sub-system permits to generate trigger for acquisition, supplies the scintillators planes, but also gives the position of the particle track to the bench computer.

The “DAQ board / Control signals” sub-system permits to read data from the VFE-PCB and generate the correct timing for the FLC_PHY2 ship.

At last, the bench computer permits to control the complete system. It gives user some facilities to control the test bench with some simplified **G**raphic **U**ser **I**nterface (GUI).

For more details on the system and its sub-systems, we have the following figure (Figure 2):

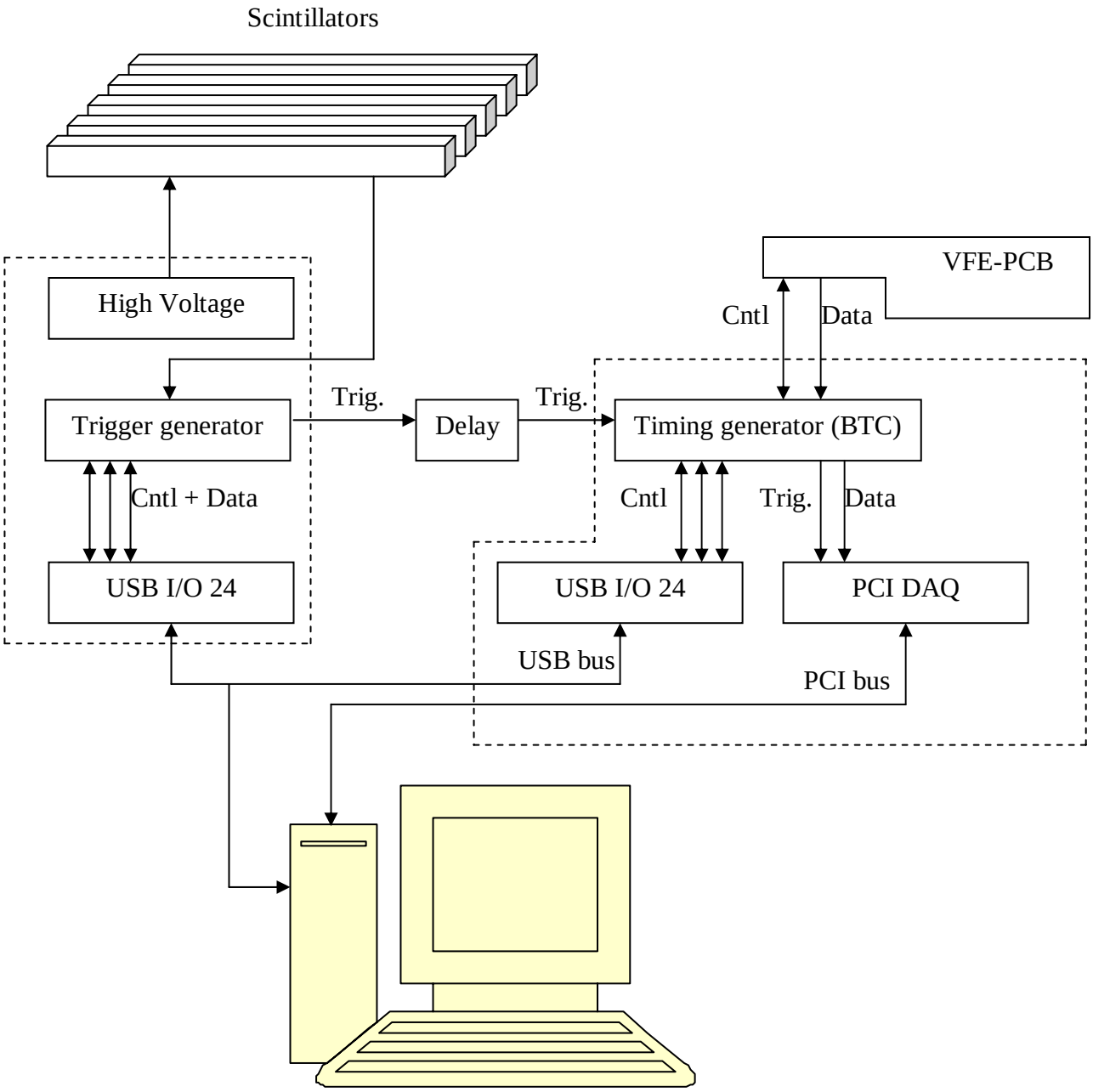

Figure 2. Detailed overview of the Cosmic Calibration Test Bench system architecture.

3.2 System Interfaces Requirements

In this paragraph, we will enumerate all internal and external interfaces for the complete system.
The previous figure (Figure 2) shows all interfaces for the system, we give the list:

- interface between the user and the bench computer,
- interface between the VFE-PCB and acquisition sub-system,
- interface between the scintillator planes and the “Trigger generator / Hodoscope controller” sub-system,
- interface between the acquisition sub-system and the “Trigger generator / Hodoscope controller” sub-system,
- interface between the “Trigger generator / Hodoscope controller” sub-system and the bench computer,
- interface between the acquisition sub-system and the bench computer.

3.2.1 Interface 1: user actions on bench computer

⇒ SRS_INT_USER_BENCH_1 User actions

The Graphical User Interface (GUI) should control each sub-system individually. Moreover, the GUI should be as easy to use as possible: the user doesn't have to know the test or calibration sequence, or the different communication between each sub-system.

To simplify the GUI, for example, we can propose to develop one dialog box per sub-system.

3.2.2 Interface 2: VFE-PCB interaction with acquisition sub-system

⇒ SRS_INT_VFE_ACQ_1 VFE-PCB Control

Each FLC_PHY2 ship on VFE-PCB has 5 LVDS control inputs:
- ***SR_Hold.***
- ***SR_Reset.***
- ***SR_Inpu.t***
- ***SR_Clock.***
- ***Switch_LED.***

Each FLC_PHY2 ship on VFE-PCB has 5 LVDS control outputs:
- ***SR_Output.***
- ***Type0 … Type3.***

The sequence of these control signals is given in the following diagram:

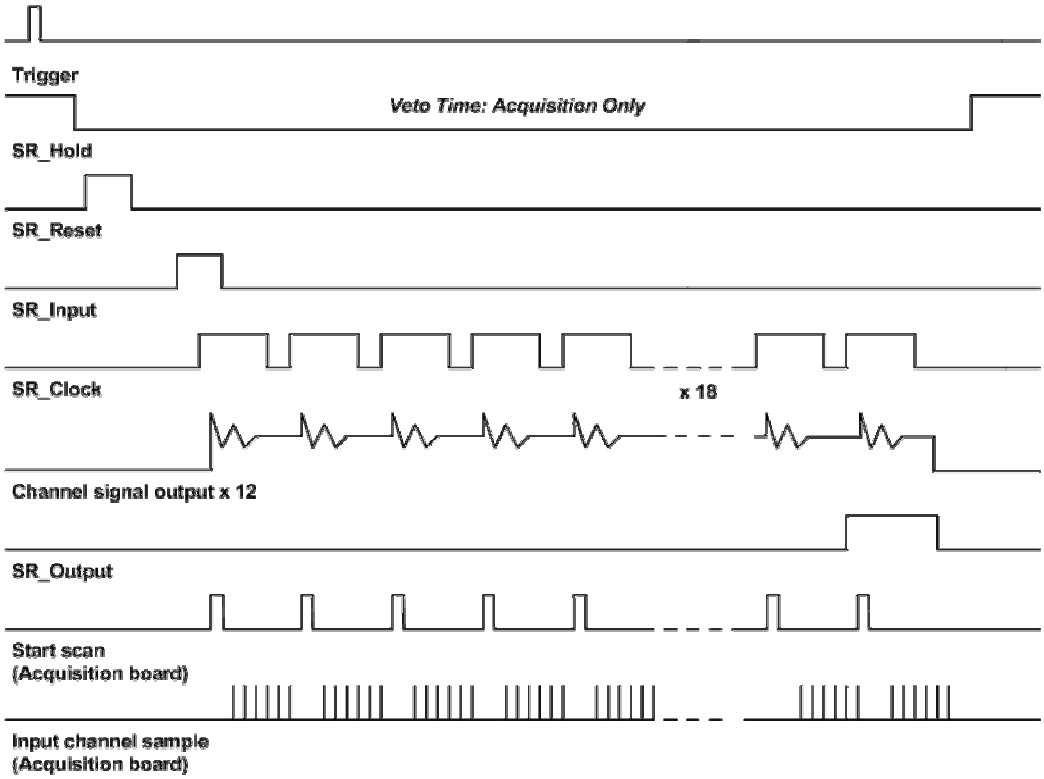

Figure 3. Timing sequence for VFE-PCB.

In this diagram, the "Trigger" signal is given by the "Trigger generator / Hodoscope controller" sub-system.

The "Switch_LED" signal permits to switch on / off a LED on the VFE-PCB in order to check if the communication between the VFE-PCB and other sub-system is operational.
The "Type0...3" signals give the address information for the position of the VFE-PCB in the final detector prototype.

⇒ SRS_INT_VFE_ACQ_2 VFE-PCB Data

The VFE-PCB has 1 data output:
- Differential analog output.
There are 12 chips on one VFE-PCB, the acquisition sub-system has to read these 12 differential analog outputs.

The acquisition sub-system should have a precision of 10 bits and dynamic range of 14 bits.

⇒ SRS_INT_VFE_ACQ_3 VFE-PCB Calibration

The VFE-PCB has 9 calibration inputs:
- 6 LVDS Enable Channels.
- 2 LVDS Select Channels.
- Differential calibration voltage.

The calibration voltage should have a precision of 12 bits.

The sequence of these control signals may be defined later.

3.2.3 Interface 3: Scintillators planes and hodoscope sub-system

⇒ SRS_INT_SCIN_HODO_1 **Scintillators power supply**

The scintillators planes must be powered by the hodoscope sub-system.
Each scintillators should have its own power supply and adjustment.

Power adjustments may be done manually or automatically, this functionality should be integrated later.

⇒ SRS_INT_SCIN_HODO_2 **Scintillators X, Y particle track position**

The scintillators planes have 32 (16 x 2) scintillators for X position, and 32 (16 x 2) for Y direction.
The position of a particle track is given by reading 64 (32 + 32) digital channels.

In the future Cosmic Calibration Test Bench, there are **4** scintillators planes, the disposition of the planes is shown in the following figure:

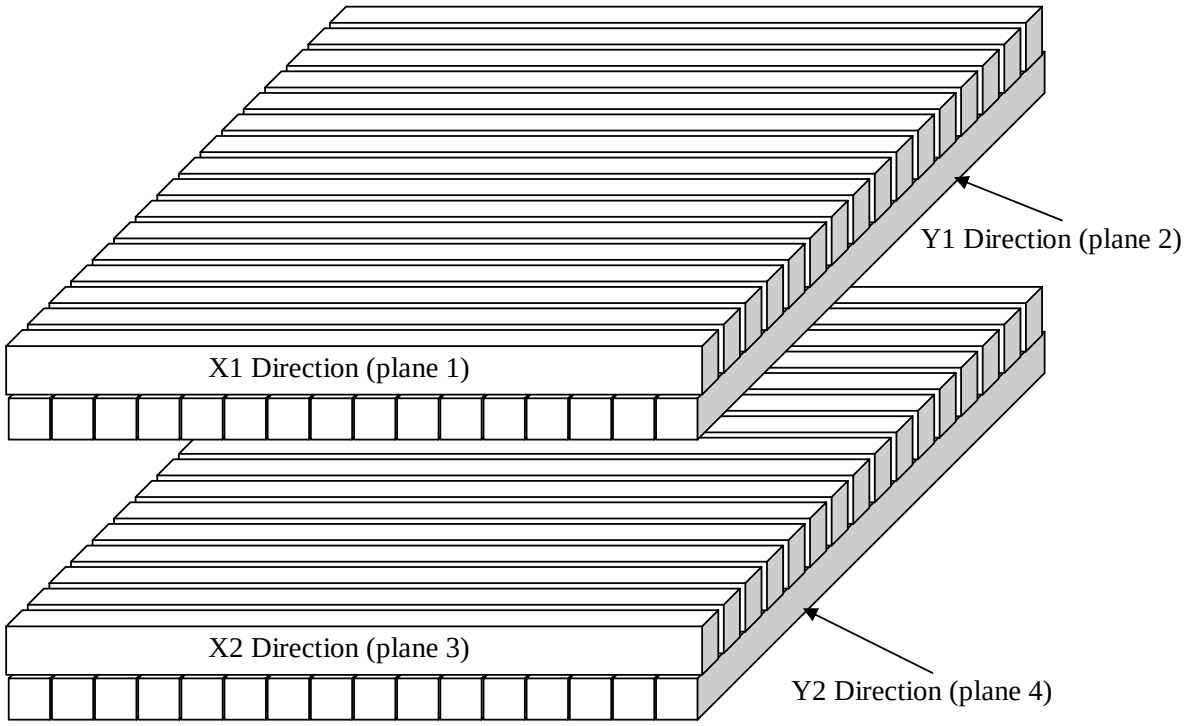

Figure 4. Disposition of scintillator planes for particle track monitoring.

3.2.4 Interface 4: Acquisition sub-system and hodoscope sub-system

⇒ SRS_INT_ACQ_HODO_1 **Acquisition trigger generation**

When a cosmic particle hit some VFE-PCB wafers, the hodoscope sub-system must generate a trigger signal with a delay adjustable with 10 ns precision.

Typically, the adjustment of the delay should be from **100 ns** to **300 ns**. This delay permits to set the moment when the maximum of charge is been read on the device under test.

3.2.5 Interface 5: Acquisition sub-system and bench computer

⇒ SRS_INT_ACQ_CPU_1 **Acquisition data transfer**

The number of data to read for one VFE-PCB is 216 (12 ship x 18 channels) in 1 ms maximum. The data transfer between the acquisition sub-system and the bench computer must be greater than 216 000 samples per second.

The data transfer rate must be greater than 520 Ko/s.
To assure this transfer rate, we can choose, for example, the **PCI bus**.

⇒ SRS_INT_ACQ_CPU_2 **Acquisition command control**

All commands for VFE-PCB can be considerate as "Slow control" in comparison of data transfer rate.

To get or send VFE-PCB control commands, we can choose, for example, the **USB bus**.

3.2.6 Interface 6: Hodoscope sub-system and bench computer

⇒ SRS_INT_HODO_CPU_1 **Particle track monitoring**

The hodoscope sub-system has to store the particle track with 64 digital data.
These 64 digital data must be transferred to the computer bench when a cosmic particle has hit the VFE-PCB.

⇒ SRS_INT_HODO_CPU_2 **Control hodoscope**

The hodoscope sub-system must be initialized each time it stores a particle track position before next hit.
The hodoscope sub-system must warn the computer when a particle hit the VFE-PCB.
The supply power system can communicate with external by Ethernet, RS232 or GPIB bus.

To get data or send commands to the hodoscope sub-system, we can choose, for example, the **USB bus**.

3.3 System Capabilities Requirements

In this paragraph, we will describe all functionalities that the Cosmic Calibration Test Bench should have.
The proposed functionalities for the Cosmic Calibration Test Bench are listed below:

- manage power supply on each scintillator,
- monitor the particle track,
- manage the acquisition trigger,
- control the device under test timing,
- read the device under test outputs,
- store data from device under test,
- run a calibration for the device under test.

3.3.1 Functionality 1: Manage scintillators power supply

⇒ SRS_HWI_HODO_POWER_1 **Power for each scintillator**

The hodoscope power system must have one voltage channel for each scintillator.

⇒ SRS_SWI_HODO_POWER_1 **Supervise each scintillators power supply**

The supply power system can set each analog offset particle detection for each scintillator.

In a first time, this functionality will be done manually.

3.3.2 Functionality 2: Monitor particle track

⇒ SRS_HWI_HODO_TRACK_1 **Read each scintillator data**

The hodoscope sub-system must read all the 64 digital inputs from scintillator planes before generate the trigger.

⇒ SRS_HWI_HODO_TRACK_2 **Store the position of particle track**

The hodoscope sub-system must store the particle track position before warn the computer that a cosmic particle has hit the VFE-PCB.

3.3.3 Functionality 3: Manage the trigger

⇒ SRS_HWI_HODO_TRIG_1 **Generate a trigger**

The hodoscope sub-system must generate a trigger signal only if a particle hits the VFE-PCB.

⇒ SRS_HWI_HODO_TRIG_2 **Control delay for acquisition trigger**

The hodoscope sub-system must generate a trigger signal with a delay of 200 ns after the particle detection.
The adjustment of this delay must have a precision adjustable from 100 ns to 300 ns with a step of 10 ns.

3.3.4 Functionality 4: Timing for device under test

⇒ SRS_HWI_BTC_TIME_1 **Generate timing for device under test**

The Bench Timing Control (BTC) has to control the timing sequence of the device under test.
This timing sequence for VFE-PCB configuration is shown in the Figure 3.

3.3.5 Functionality 5: Acquire data from device under test

⇒ SRS_HWI_DATA_ACQ_1 **Acquisition sub-system**

The acquisition sub-system must implement functionality for reading 216 data on 12 channels from VFE-PCB in a time less than 1 ms.

⇒ SRS_HWI_DATA_ACQ_2 **Start acquisition on trigger**

The acquisition of all 18 data sets must start on the apparition of a particle hit, i.e. a trigger generated by the hodoscope sub-system.

⇒ SRS_SWI_DATA_ACQ_1 **Acquired data transfer**

The transfer of data should be done by a DMA access to guarantee the better data transfer rate.

3.3.6 Functionality 6: Store acquired data

⇒ SRS_SWI_STORE_ACQ_1 **Store acquired data**

The transferred data must be recorded in a file.
In this file, the following information may appear:
- ***Header: date, VFE-PCB information.***
- ***Data: ID of scintillator hit: (X_1, Y_1) and (X_2, Y_2), data from VFE-PCB.***
- ***Marker for end of file.***

In order to simplify the access of the recorded file by other applications, we can choose, for example, an text format (ASCII, ANSI or UNICODE).

3.3.7 Functionality 7: Calibration

⇒ SRS_SWI_CALIB_DEV_1 **Generate calibration commands**

The Cosmic Calibration Test Bench software must have a procedure to manage the calibration procedure of device under test.
The calibration voltage must have a precision greater than 12 bits.

3.4 System Timing Requirements

In this paragraph, we will detail all timing constraints on the Cosmic Calibration Test Bench.
The density of a cosmic particle is approximately **1** per **second** per **cm²**.

The data rate that we have to manage is very slow: we choose to have an acquisition that is able to read 10 data each second (frequency = **10 Hz**).

4 GLOSSARY

BTC: **B**ench **T**iming **C**ontrol.
FLC: **F**uture **L**inear **C**ollider.
GUI: **G**raphic **U**ser **I**nterface.
LAL: **L**aboratoire de l'**A**ccélérateur **L**inéaire.
LLR: **L**aboratoire **L**eprince-**R**inguet.
HWI: **H**ard**W**are **I**tem.
SRS: **S**ystem **R**equirements **S**pecification.
SWI: **S**oft**W**are **I**tem.
TBD: **T**o **B**e **D**efined.
VFE: **V**ery **F**ront-end **E**lectronic.

5 ANNEXE A: USB I/O 24 MODULE

5.1 Presentation

The USBIO24 is a low-cost integrated module for the input and/or output of digital signals from a computer system by connection to the USB port.
The module features 24 x 5V level signal lines individually programmable as input or output. As the module connects to the USB port, multiple modules can be connected to a single PC by the use of a USB hub. Each module features a serial number and the PC can identify each module uniquely allowing for multiple modules to be connected for a single application.
The outputs of the module are able to source or sink up to 30mA per I/O to allow for direct connection to a variety of devices.

The USB I/O 24 Module is shown in the following picture:

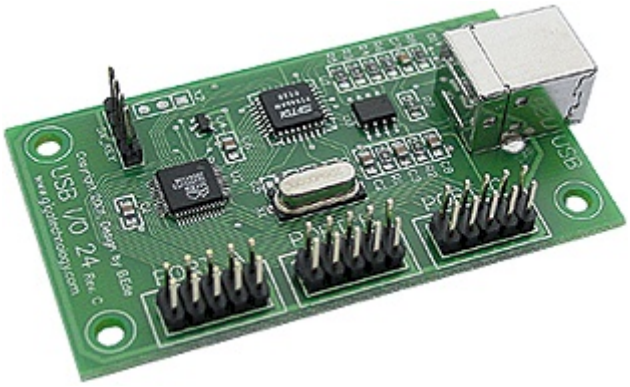

Figure 5. View of USB I/O 24 Module.

5.2 Features

The USB I/O 24 Module has the following features:

- 24 independently programmable Input / Output Pins Grouped into 3 ports,
- single module High-Speed Digital Input / Output solution,
- up to 128 modules can be connected to a single PC,
- easy to connect by 0.1” pitch headers to suit standard IDC connectors,
- integrated Type-B USB Connector,
- on-board unique serial number in EEPROM and custom programmable FLASH microcontroller,
- both USB Enumeration information and Microcontroller can be re-programmed to suit customer needs,
- module powered by the USB from the PC.

5.3 Serial Numbers

For the hodoscope sub-system, we choose: "*LLR_HODO_10*" string. For the BTC sub-system, we choose: "*LLR_BTC_10*" string.

6 ANNEXE B: USB INTERFACE FOR VFE CALIBRATION CONTROL

The VFE calibration sub-system control pins and corresponding bits are given in the following array:

Port	Bit	Pin	Direction	Control signal
Port A	-	10	-	Ground.
	0	9	Output	Internal T2.
	1	8	Output	Internal T1.
	2	7	Output	Channel Select 6.
	3	6	Output	Channel Select 3.
	4	5	Output	Channel Select 5.
	5	4	Output	Channel Select 2.
	6	3	Output	Channel Select 4.
	7	2	Output	Channel Select 1.
	-	1	-	5 volts from computer (NC).
Port B	-	10	-	Ground.
	0	9	Output	USB Reset.
	1	8	Input	Type 3.
	2	7	Output	External T2.
	3	6	Input	Type 2.
	4	5	Output	External T1.
	5	4	Input	Type 1.
	6	3	Output	VFE-PCB LED control (0 = OFF, 1 = ON).
	7	2	Input	Type 0.
	-	1	-	5 volts from computer (NC).
Port C	-	10	-	Ground.
	0	9	Input	NC.
	1	8	Output	Gain Switch (1 or 10).
	2	7	Input	NC.
	3	6	Input	NC.
	4	5	Input	NC.
	5	4	Input	NC.
	6	3	Input	NC.
	7	2	Input	NC.
	-	1	-	5 volts from computer (NC).

Array 2. ***USB I/O 24 Module Interface for Calibration sub-system.***

Legend:
NC : Not connected.

7 ANNEXE C: USB INTERFACE FOR HODOSCOPE SUB-SYSTEM CONTROL

The hodoscope sub-system control pins and corresponding bits are given in the following array:

Port	Bit	Pin	Direction	Control signal
Port A	-	10	-	Ground.
	0	9	Input	Bit 8 for particle track position.
	1	8	Input	Bit 9 for particle track position.
	2	7	Input	Bit 10 for particle track position.
	3	6	Input	Bit 11 for particle track position.
	4	5	Input	Bit 12 for particle track position.
	5	4	Input	Bit 13 for particle track position.
	6	3	Input	Bit 14 for particle track position.
	7	2	Input	Bit 15 for particle track position.
	-	1	-	5 volts from computer.
Port B	-	10	-	Ground.
	0	9	Input	Bit 0 for particle track position.
	1	8	Input	Bit 1 for particle track position.
	2	7	Input	Bit 2 for particle track position.
	3	6	Input	Bit 3 for particle track position.
	4	5	Input	Bit 4 for particle track position.
	5	4	Input	Bit 5 for particle track position.
	6	3	Input	Bit 6 for particle track position.
	7	2	Input	Bit 7 for particle track position.
	-	1	-	5 volts from computer.
Port C	-	10	-	Ground.
	0	9	Output	Reset hodoscope.
	1	8	Output	Select particle track position 0.
	2	7	Output	Select particle track position 1.
	3	6	Input	Event OK.
	4	5	Input	NC.
	5	4	Input	NC.
	6	3	Input	NC.
	7	2	Input	NC.
	-	1	-	5 volts from computer.

Array 3. ***USB I/O 24 Module Interface for Hodoscope sub-system.***

Legend:
NC : Not connected.

The following array (Array 4) shows the configuration of bits to select the correct track position.

Bit 1 (Port C - pin 2)	Bit 2 (Port C - pin 3)	Data	Plane, coordinate
0	0	0 .. 15	Plane 1 – X1
0	1	16 .. 31	Plane 2 – Y1
1	0	32 .. 47	Plane 3 – X2
1	1	48 .. 63	Plane 4 – Y2

Array 4. ***Pin configuration to read part of particle track position.***