CALICE ECAL Readout Electronics: Slave FPGA

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1 Block diagram

An overview of the slave FPGA is shown in Fig. 1 and it is estimated to need around 102 I/O pins. The FPGA is clocked using the 12.5MHz board clock and loaded from an SROM on power up.

Configuration data to control the functions of the FPGA are loaded from the master FPGA via a read-write configuration bus. These are used by all sections of the board and include timing settings, DAC levels, etc. Most of the configuration data values are stored until needed during a trigger sequence. The exceptions are related to the DAC. This needs to be set before any trigger is received. It is only used in calibration or self-test mode. In calibration mode, set within the configuration data, the DAC is set and the (constant) voltage is sent to the VFE-PCB's on the "Calibration signal level" line. In test mode, the DAC is looped back into the ADC directly within the readout board. The switch to use the DAC, rather than VFE-PCB "Channel signal output" as the ADC input is also in the configuration data and is set using the LPBK line from the "ADC data & control" block. The sequence to set the DAC is generated in the "DAC data & control" block using serial transmission of the 16-bit value. This is done on any of the following occurances:

- The DAC value in the configuration data is altered, if either of the calibration mode or test mode are selected.
- The calibration mode in the configuration data is set on or off; in the latter case, the DAC is set to zero.
- The test mode in the configuration data is set on or off; in the latter case, the DAC is set to zero.

2 ADC timing

A trigger (from any source) initiates the signal sequence to drive the VFE-PCB, read the channel data and digitise them. The time between all signals except one set is not critical and can be set to multiples of the 12.5MHz clock period, i.e. 80ns. However, the time between the trigger (or the calibration strobes (CALSTRB) if in calibration mode) and the sample-and-hold (SHLD) going to the VFE-PCB's must be timed to within at most 10ns. Hence, the slave FPGA will subdivide the 12.5MHz clock internally by a factor of eight to get a 100MHz clock and time this

Figure 1: Overview of the slave FPGA

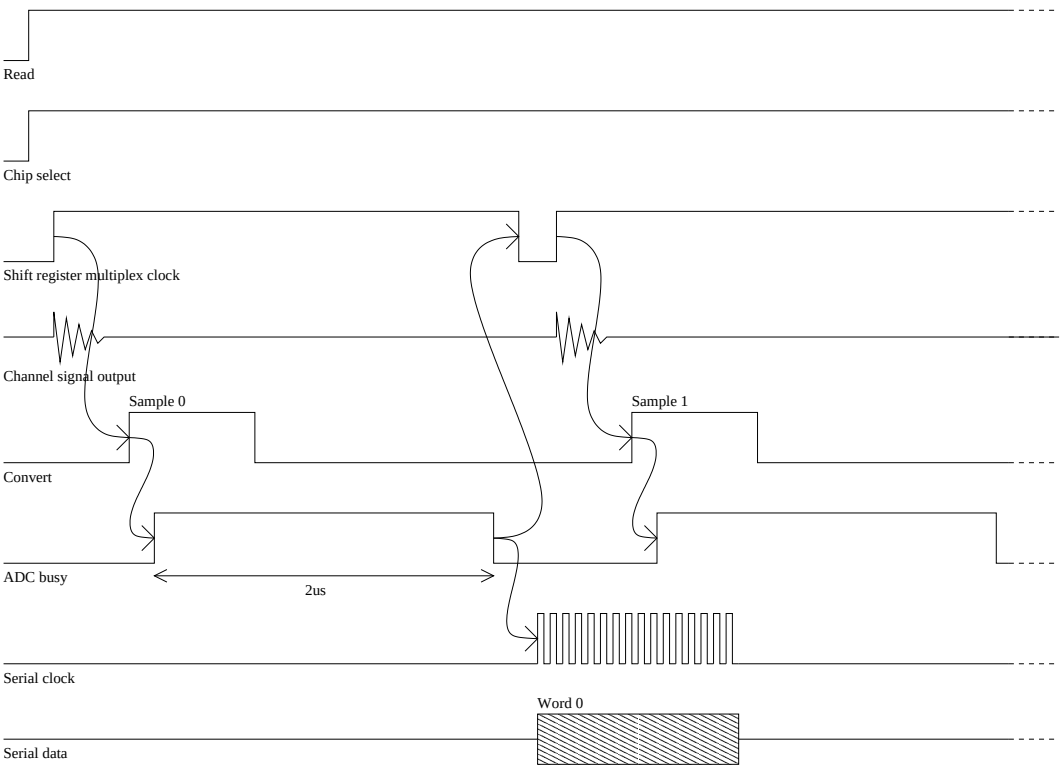

Figure 2: ADC timing sequence for the slave FPGA

critical interval from that. All time settings will be configurable from the configuration data block.

The timing of the signals driving the readout sequence is shown in Fig. 2. Not shown are the calibration strobe and some shift register control signals from the "VFE multiplex control" block which are sent straight to the connector.

The shift register multiplex clock (SRMCLK) puts each channel in sequence onto the analogue output line. After some settling time, the convert (CNVST) signal to the ADC is sent and the ADC then asserts busy for around 2μs. Following this, the next multiplex clock can be sent while the data from the previous convert can be read out in parallel. This is done serially, clocking out (SCLK) the data using the 12.5MHz board clock onto the serial data output (SDOUT) line. The total time per multiplex clock will be around 2.5μs, so the time for 18 channels to be digitised will take in total around 50μs. This is short compared with the allowed time per event at 1kHz of 1ms.