CALICE ECAL Readout Electronics: Slave-To-Master Event Data Path

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1 Transmitted data

The event data from the slave to the master FPGA's are sent during the readout sequence following a trigger. The data path proposed is a point-to-point link with eight lines per slave.

The data consist of 18 words of 16-bit data for each ADC. The two shift register output bits from the VFE-PCB's are also detected by the slave FPGA. The times of arrival of the rising edge of these two signals will be stored in the slave and sent following the ADC data as two extra words.

2 Timing

The timing of the signals is shown in Fig. 1. The 12.5 MHz board clock is common to both the slave and master FPGA and is slow enough that edge and jitter effects can be ignored. The data are set on the rising edge of the clock by the slave and detected on the falling edge in the master.

The ADC data are sent straight through the slave FPGA, with only potentially some time alignment to the board clock being necessary. The data from the six ADC's controlled by each slave FPGA are sent in parallel, MSB first.

The time for each channel on the multiplex line is around 2.5μs, limited by the ADC clocking speed. The time taken to send 16 bits of data on the 12.5MHz clock is only 1.3μs, so there needs to be gaps in the data being sent. A "write enable" line controls when the master needs to accept the data.

The extra shift register output words are not shown here, but would appear as an extra 19th sequence, with two of the six lines containing the bit edge times and the other four lines carrying no information.

The rising edge of a "link active" line indicates to the master that the previously stored data should be discarded and new data overwritten into its internal memory. This allows multiple triggers without readout. The master must be ready to accept the data at any time.

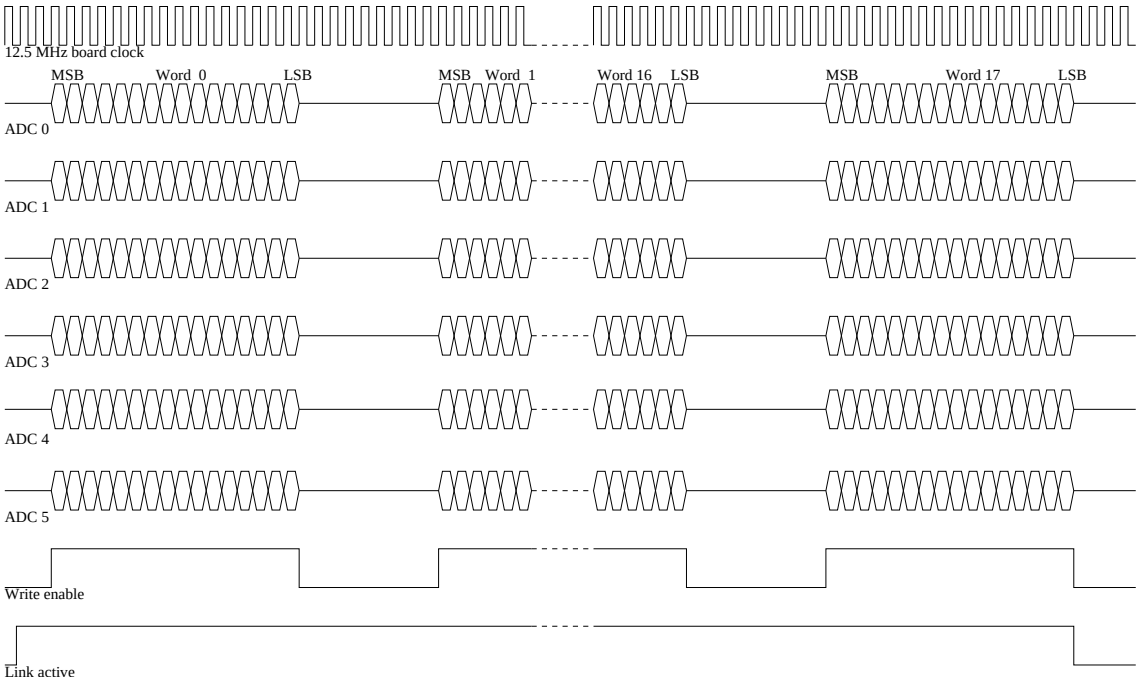

Figure 1: Timing diagram for the slave-to-master event data path