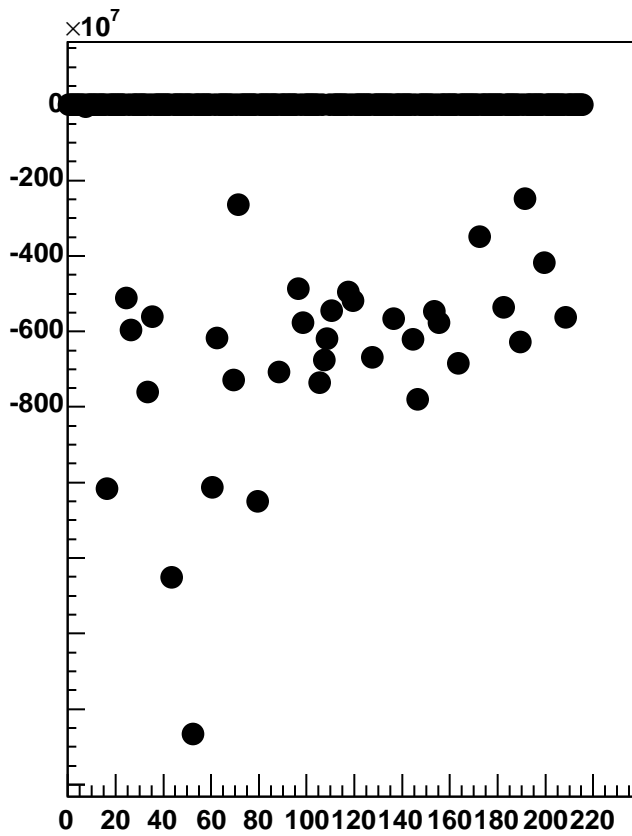
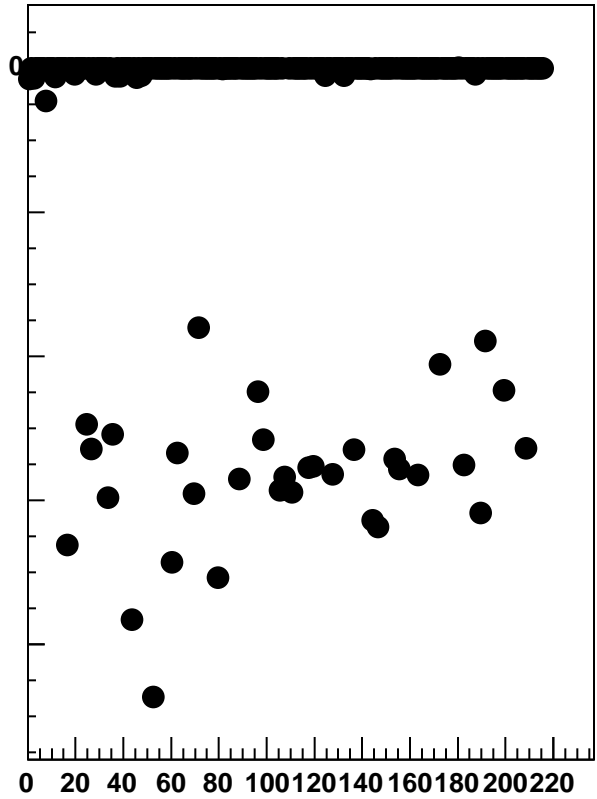


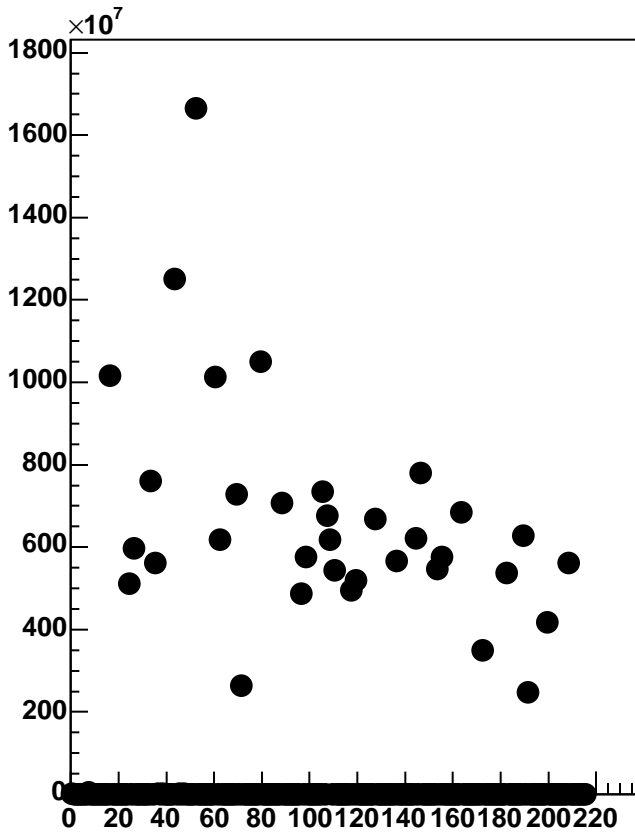
Channel Enabled, DAC=1600, Fit Baseline vs 18\*Chip+Chan



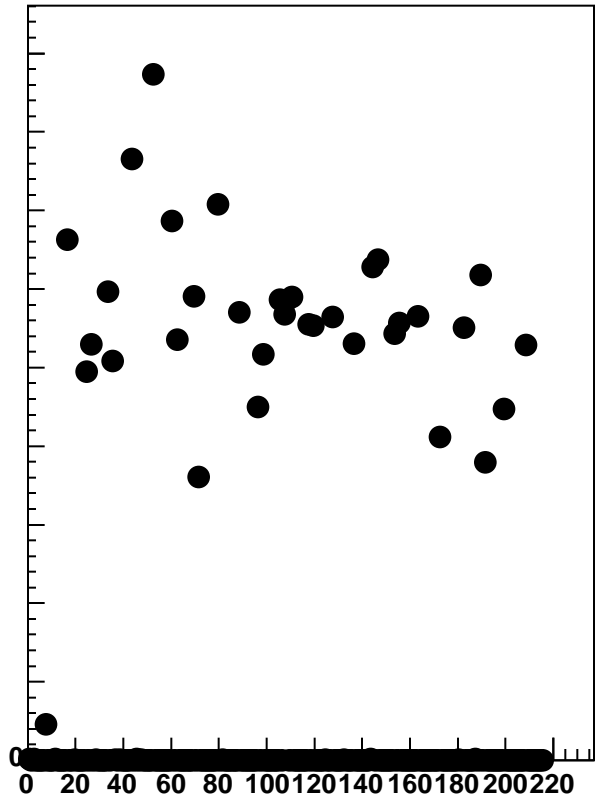
Channel Enabled, DAC=1600, Fit Start Time vs 18\*Chip+Chan



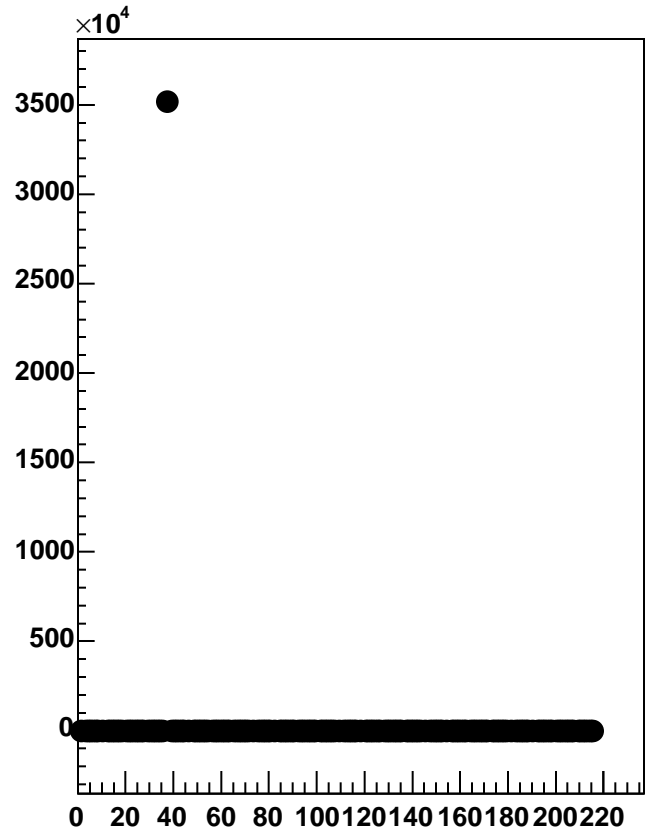
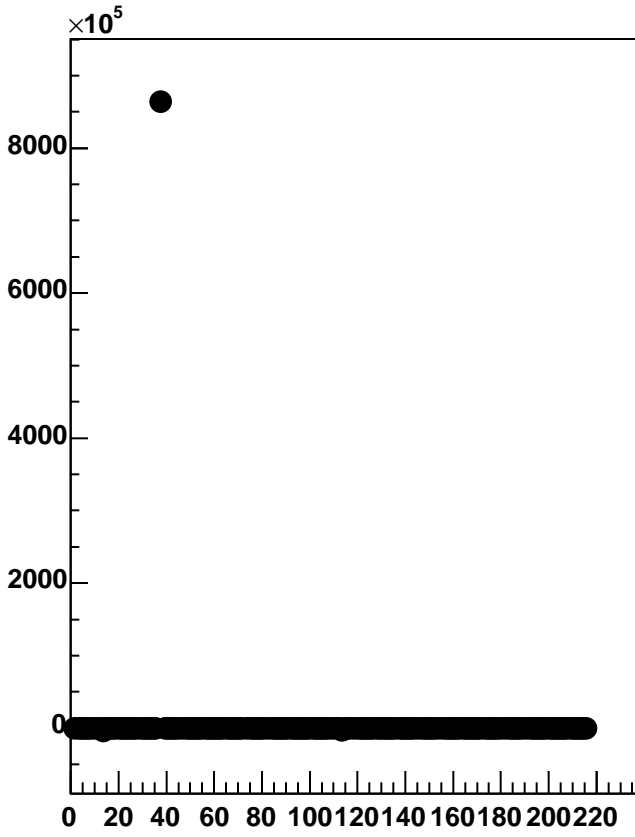
Channel Enabled, DAC=1600, Fit Normalisation vs 18\*Chip+Chan



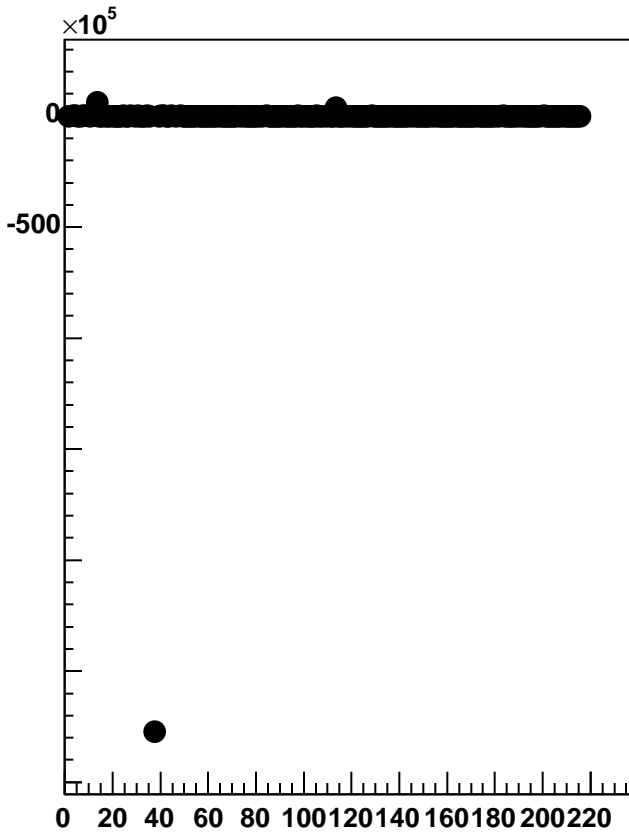
Channel Enabled, DAC=1600, Fit Error vs 18\*Chip+Chan



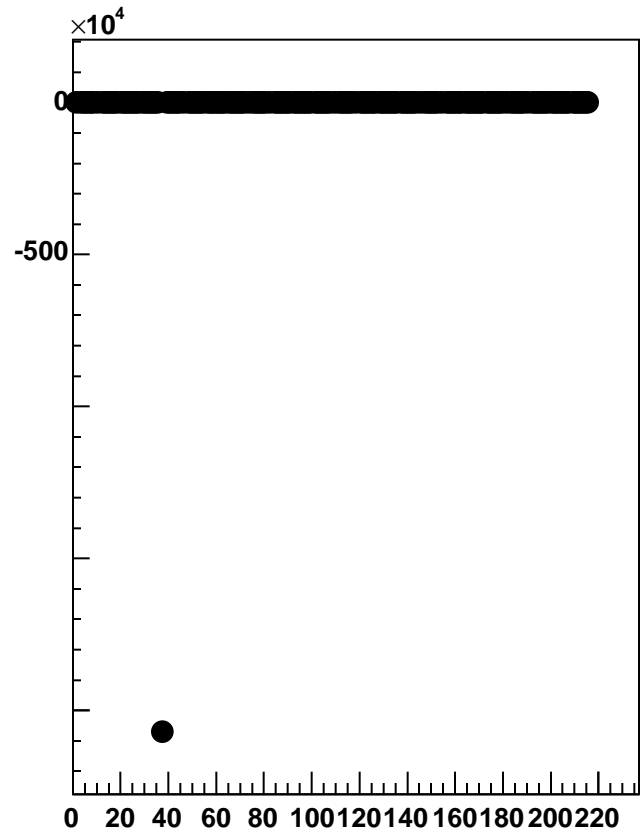
Disabled 0, DAC=1600, Fit Baseline vs 18\*Chip+Chan



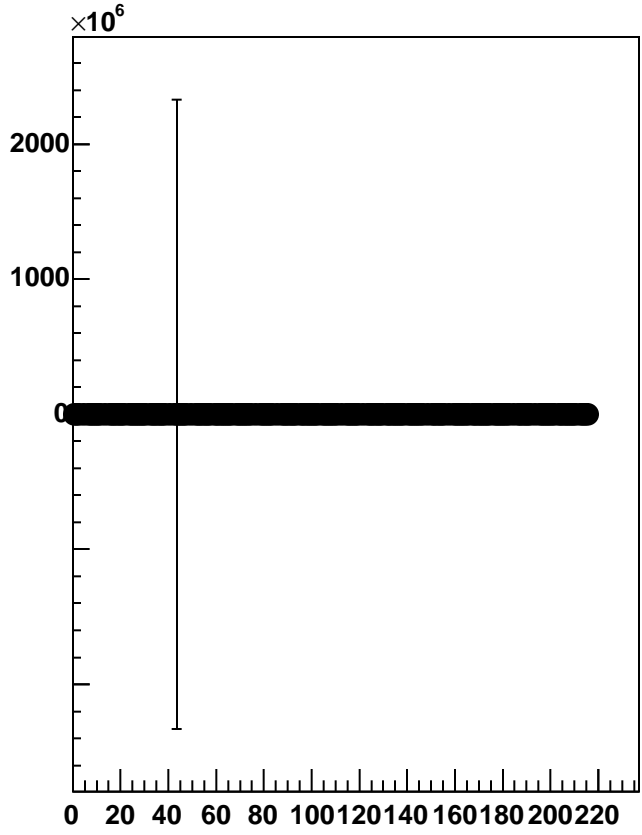
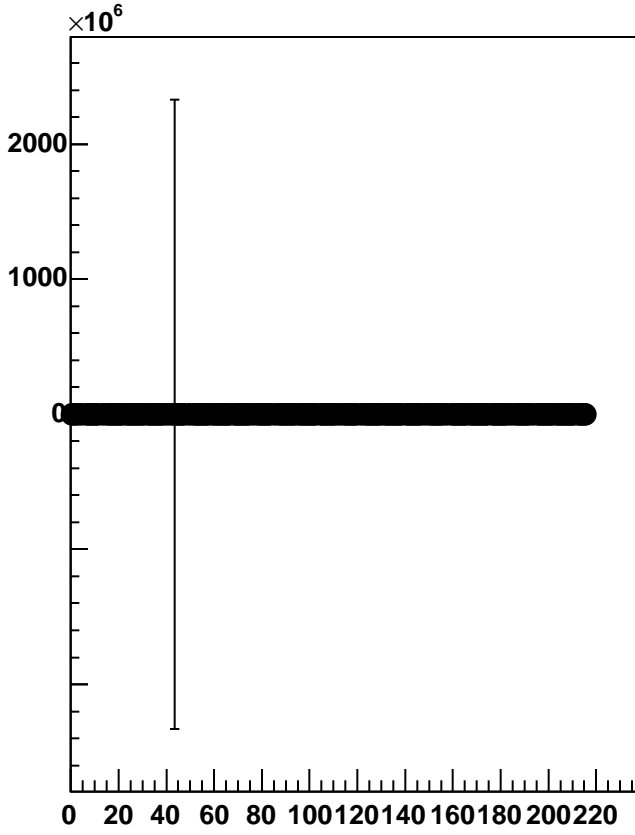
Disabled 0, DAC=1600, Fit Normalisation vs 18\*Chip+Chan



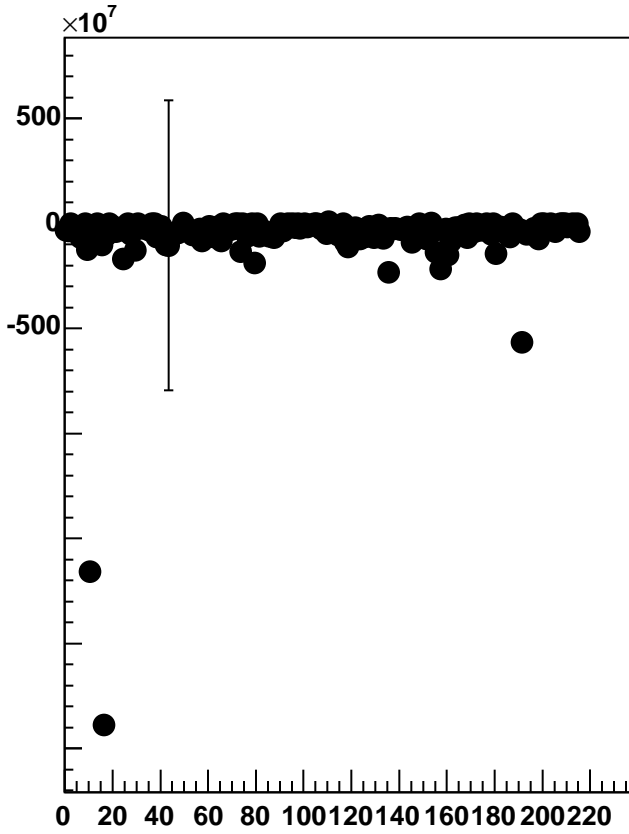
Disabled 0, DAC=1600, Fit Shaping Time vs 18\*Chip+Chan



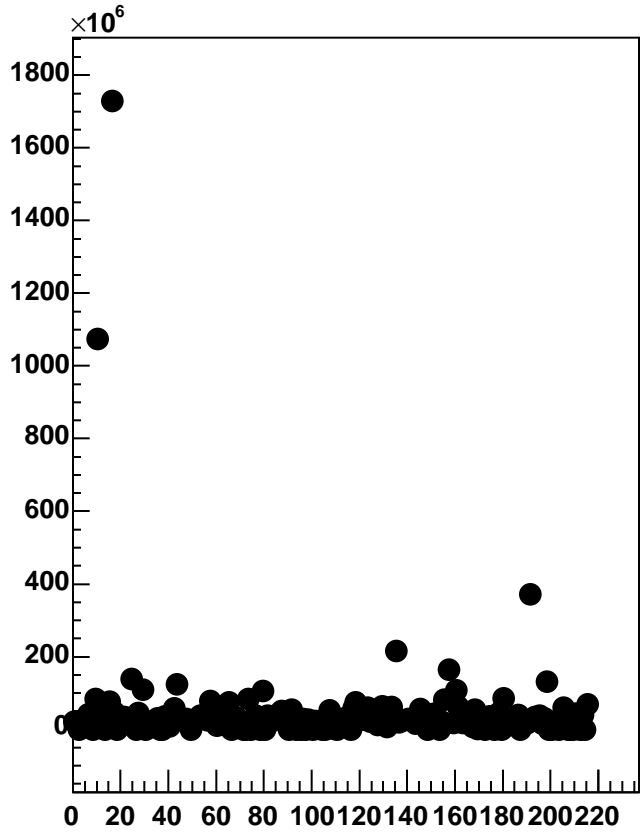
Disabled 1, DAC=1600, Fit Baseline vs 18\*Chip+Chan



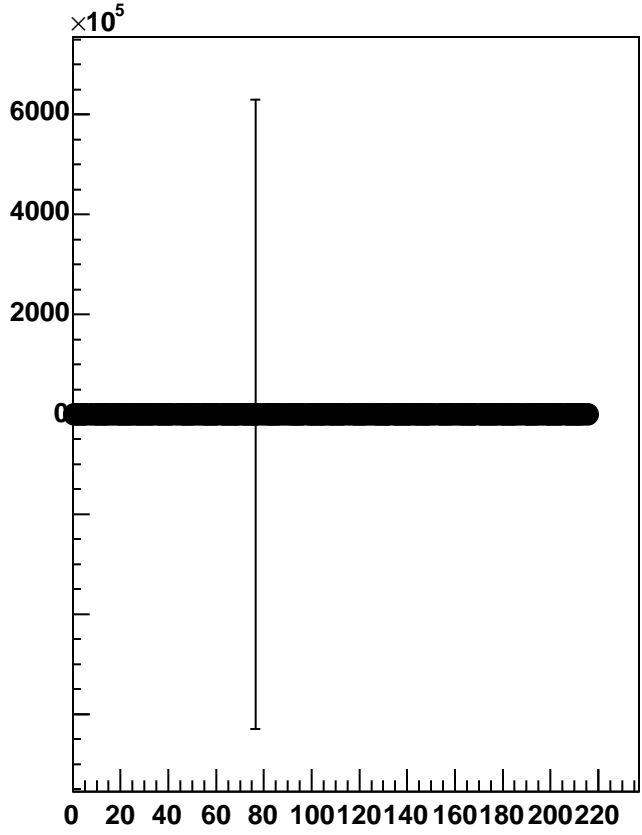
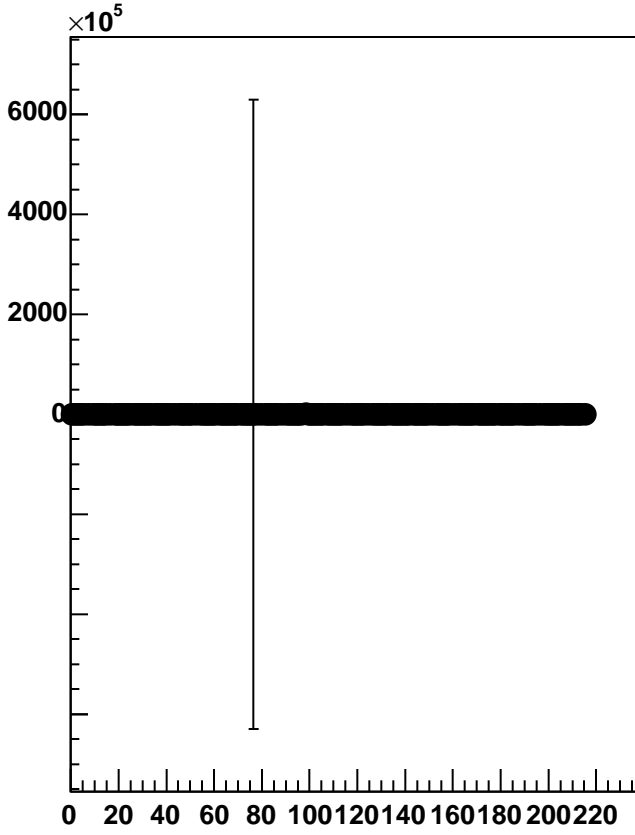
Disabled 1, DAC=1600, Fit Normalisation vs 18\*Chip+Chan



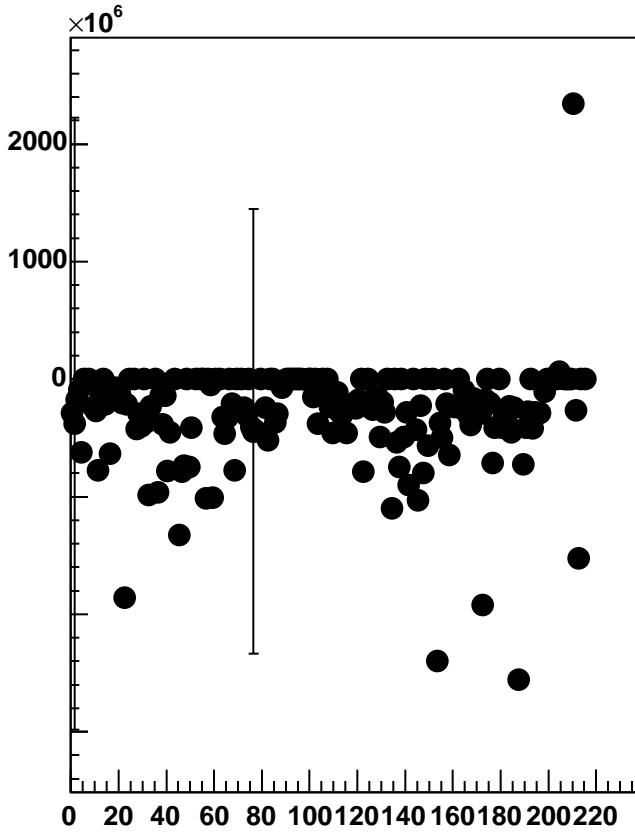
Disabled 1, DAC=1600, Fit Shaping Time vs 18\*Chip+Chan



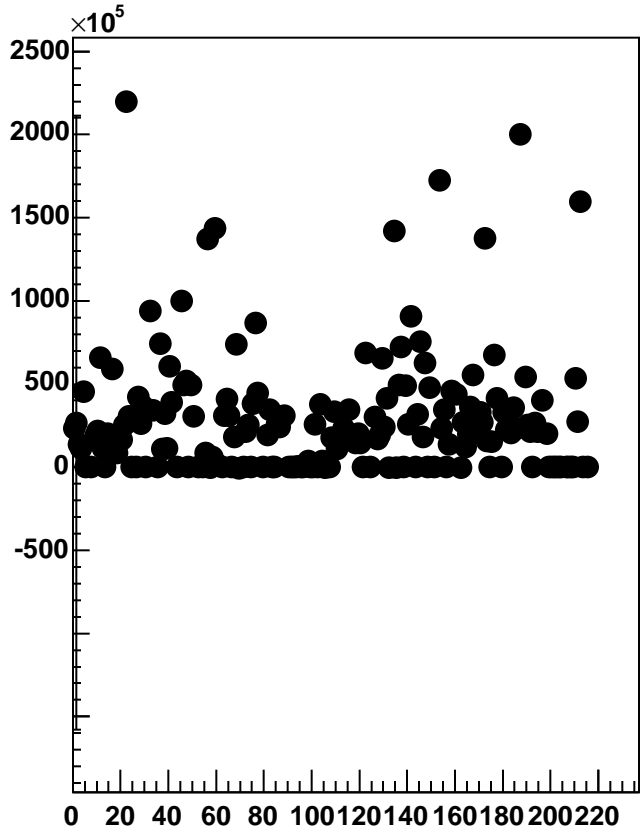
Disabled 2, DAC=1600, Fit Baseline vs 18\*Chip+Chan



Disabled 2, DAC=1600, Fit Normalisation vs 18\*Chip+Chan

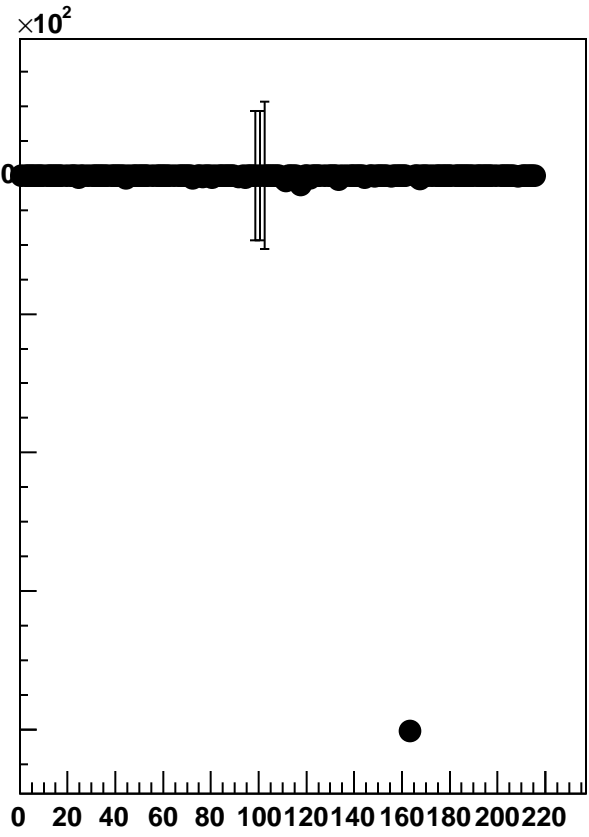
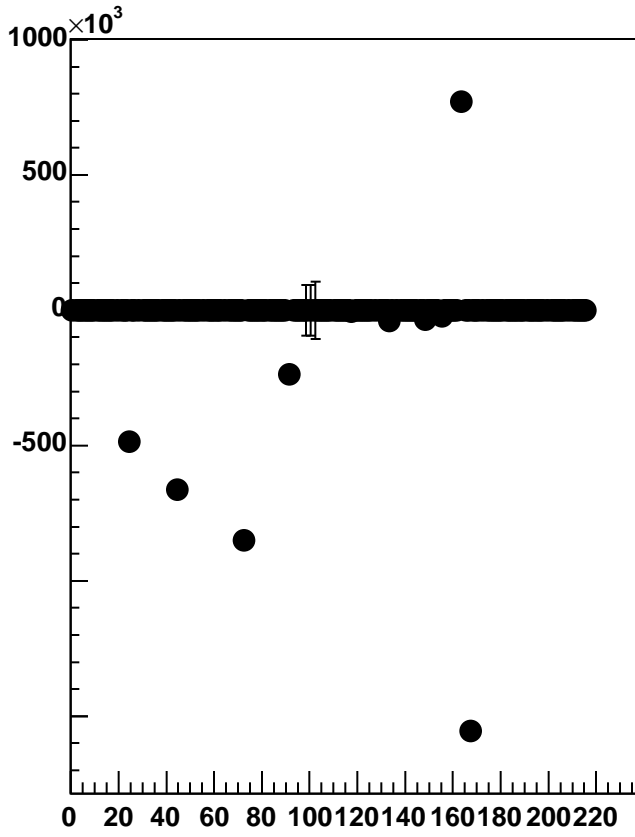


Disabled 2, DAC=1600, Fit Shaping Time vs 18\*Chip+Chan

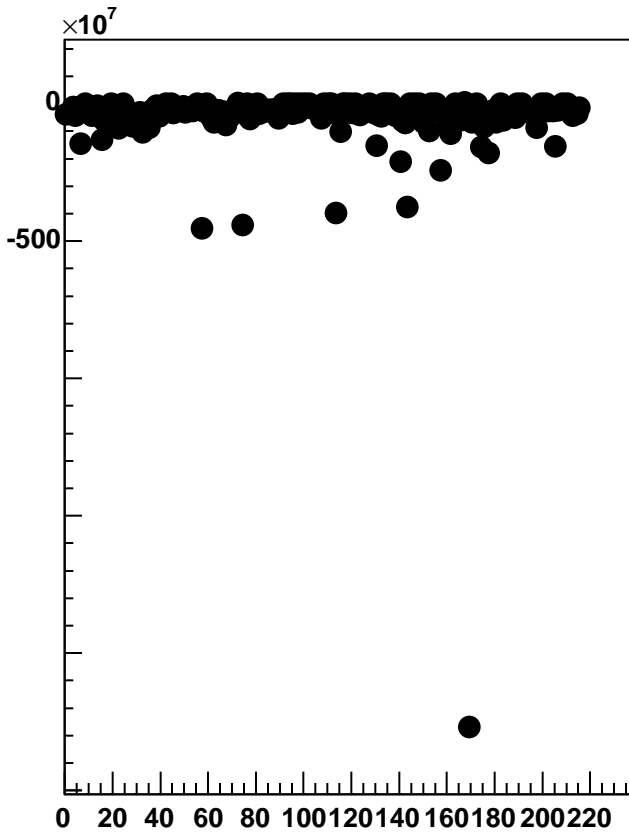




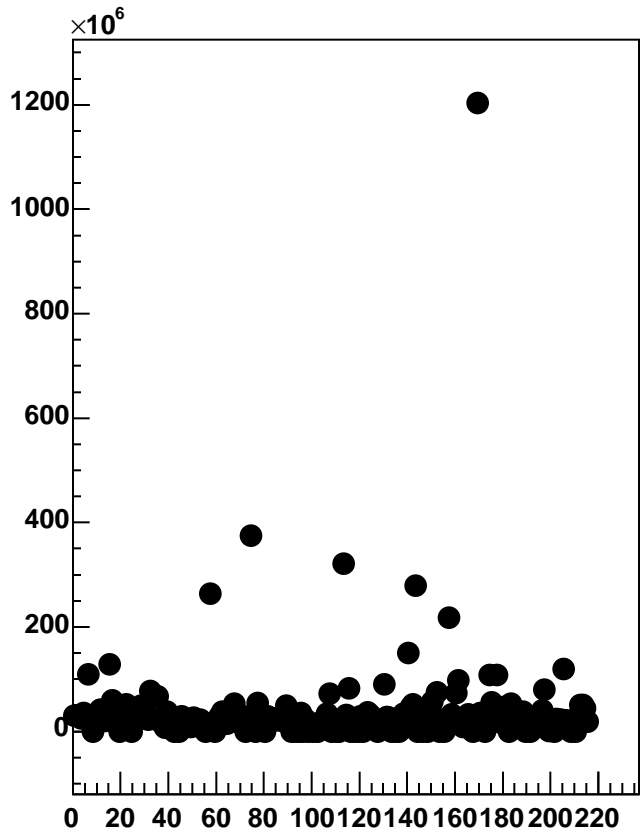
Disabled 3, DAC=1600, Fit Baseline vs 18°Chip+Chan



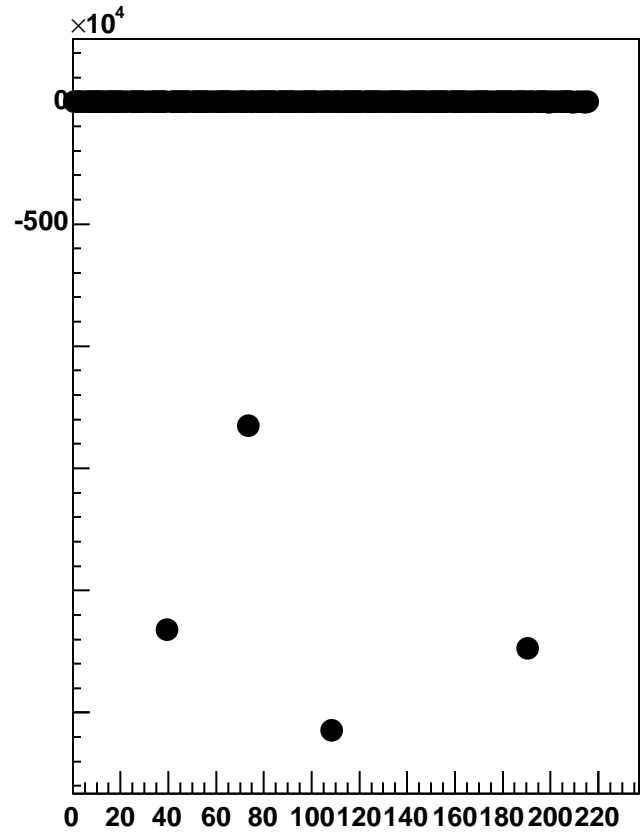
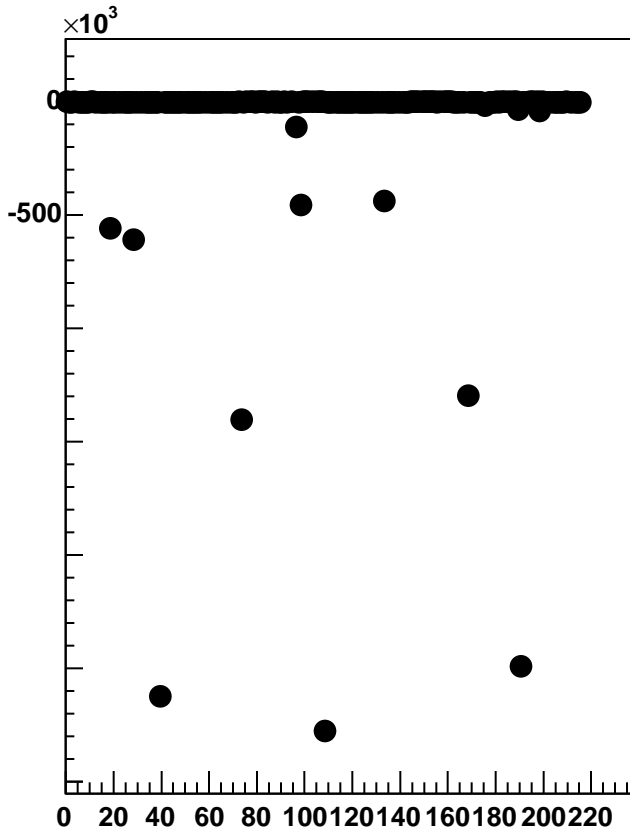
Disabled 3, DAC=1600, Fit Normalisation vs 18°Chip+Chan



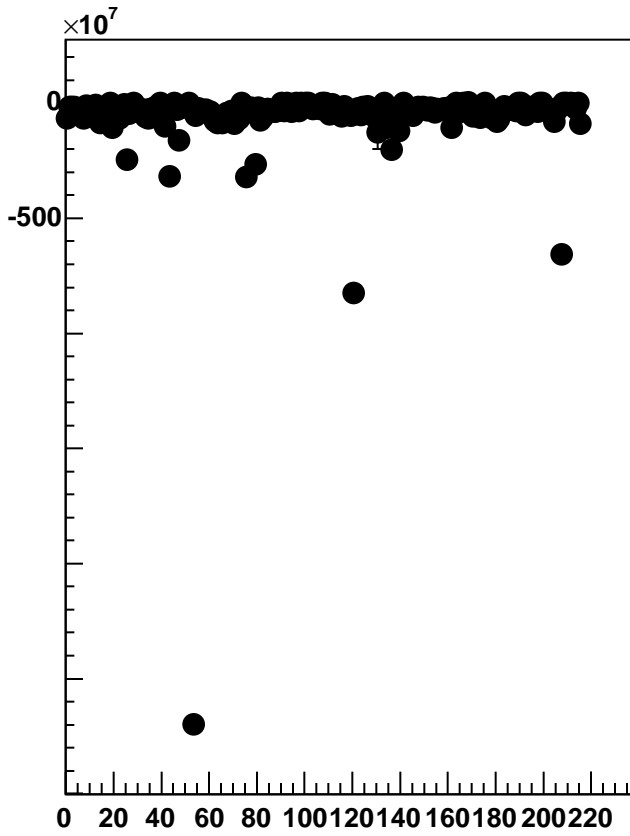
Disabled 3, DAC=1600, Fit Shaping Time vs 18°Chip+Chan



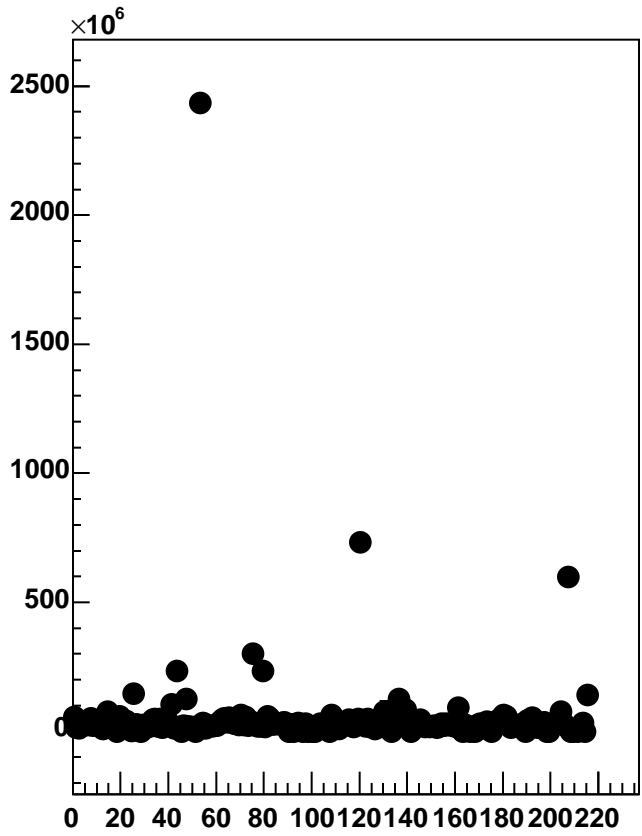
Disabled 4, DAC=1600, Fit Baseline vs 18°Chip+Chan



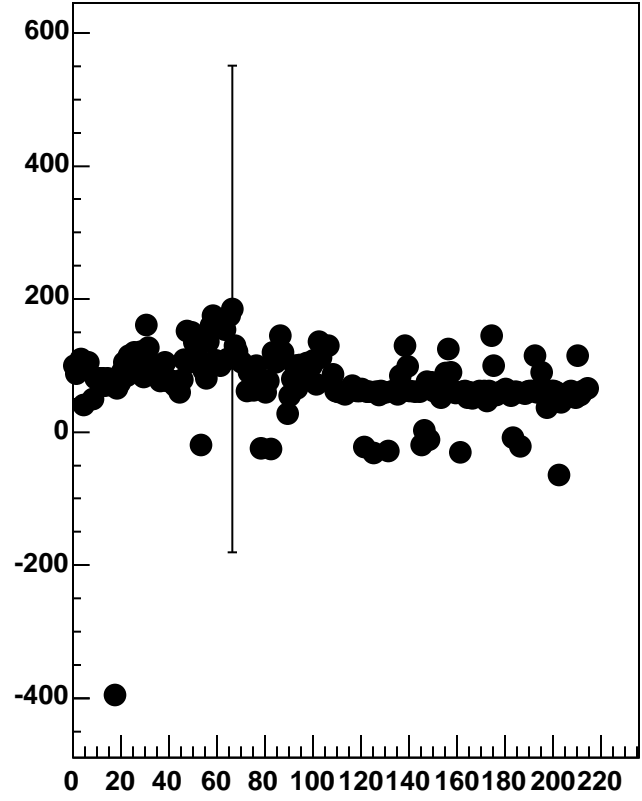
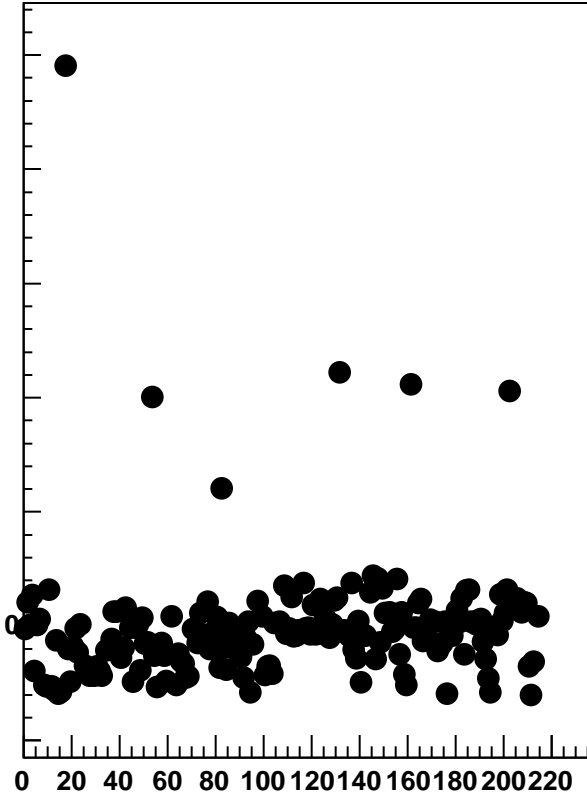
Disabled 4, DAC=1600, Fit Normalisation vs 18°Chip+Chan



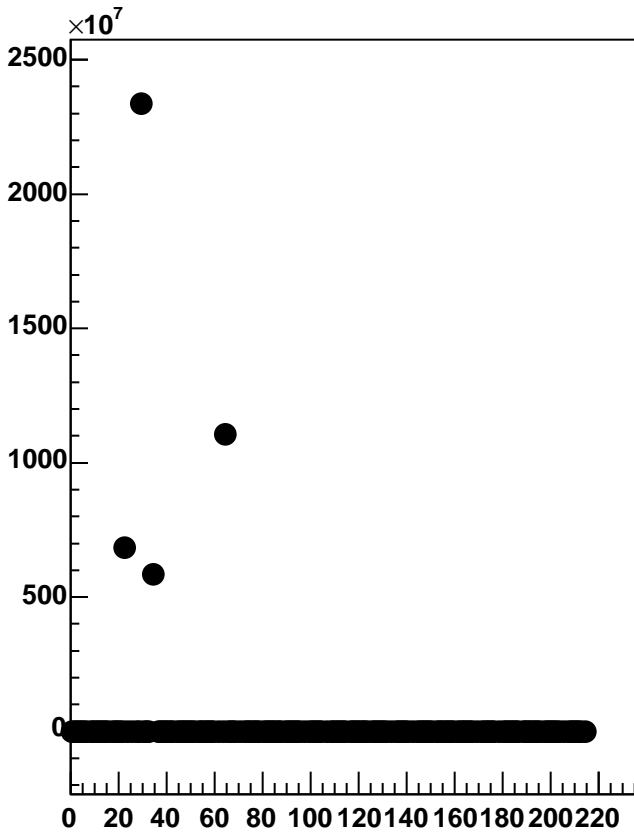
Disabled 4, DAC=1600, Fit Shaping Time vs 18°Chip+Chan



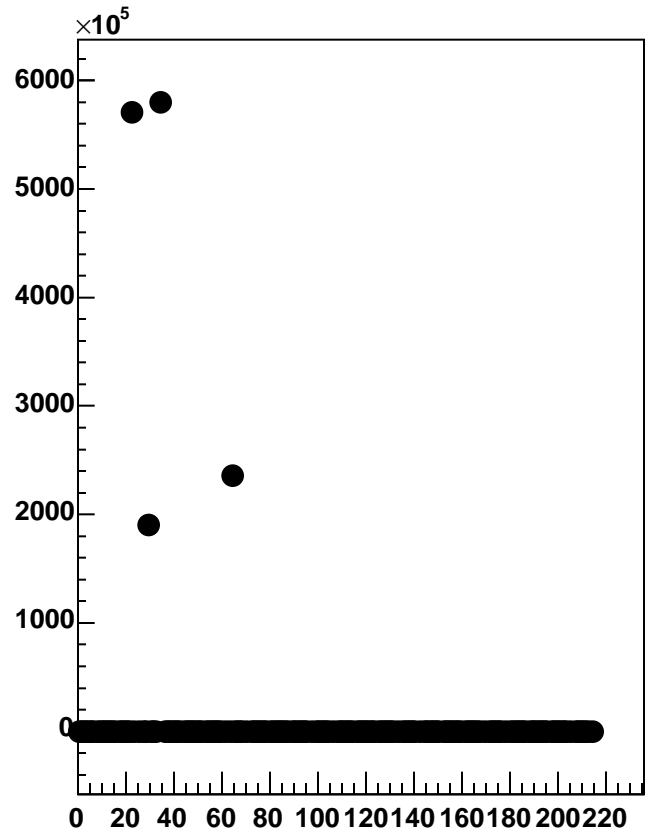
Disabled 5, DAC=1600, Fit Baseline vs 18°Chip+Chan



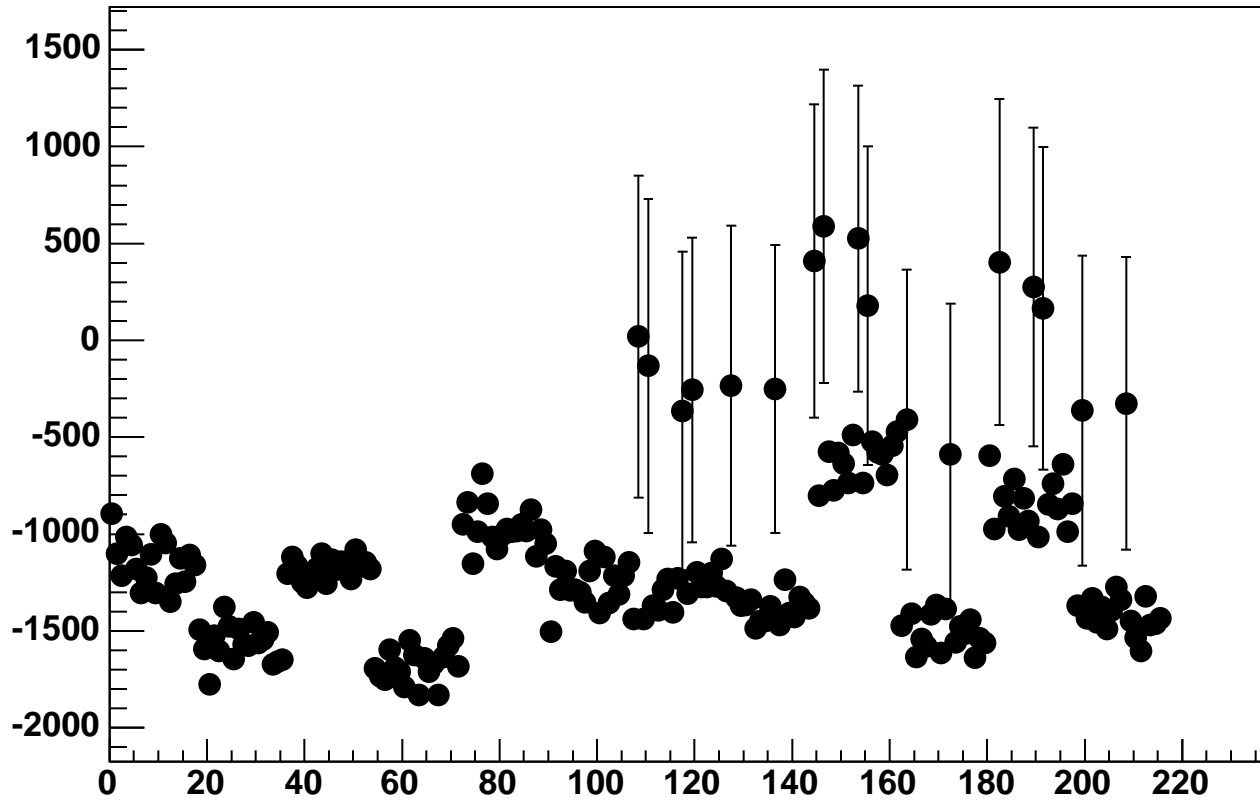
Disabled 5, DAC=1600, Fit Normalisation vs 18°Chip+Chan



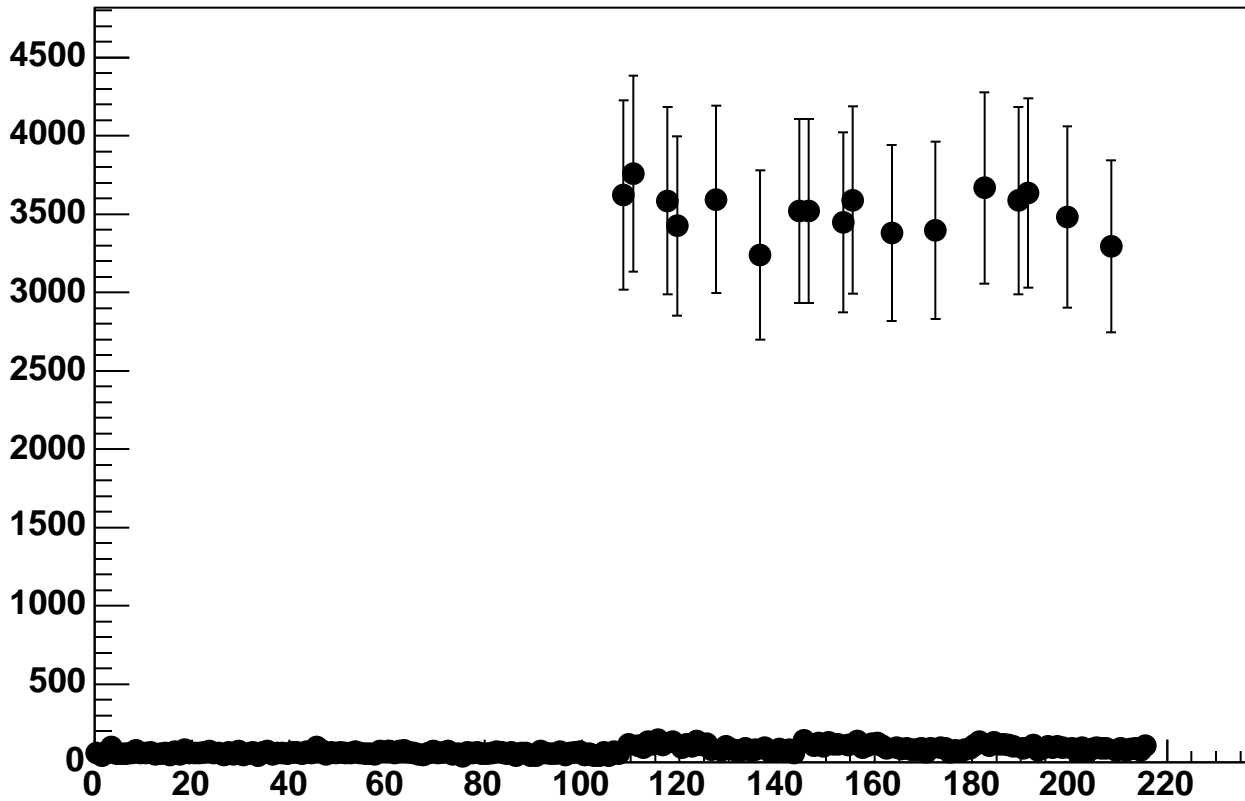
Disabled 5, DAC=1600, Fit Shaping Time vs 18°Chip+Chan



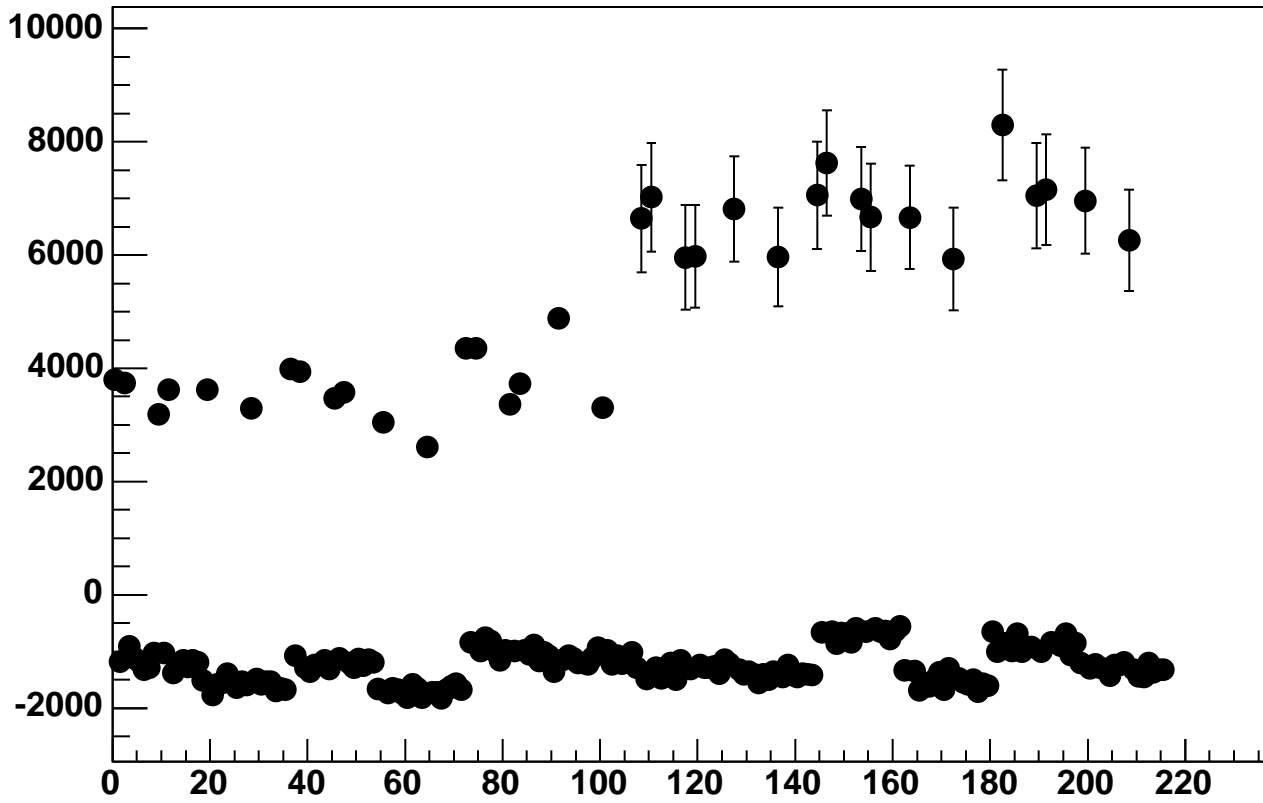
Enable 0, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan



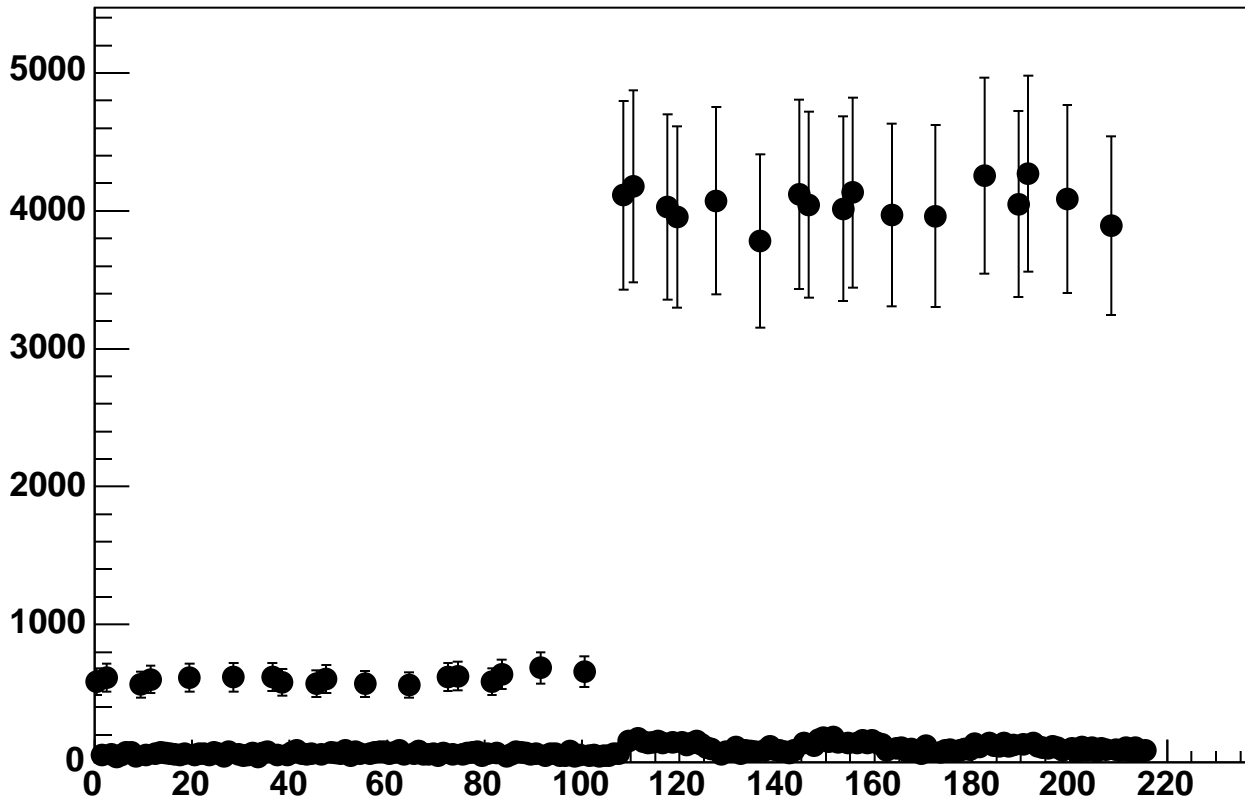
Enable 0, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan



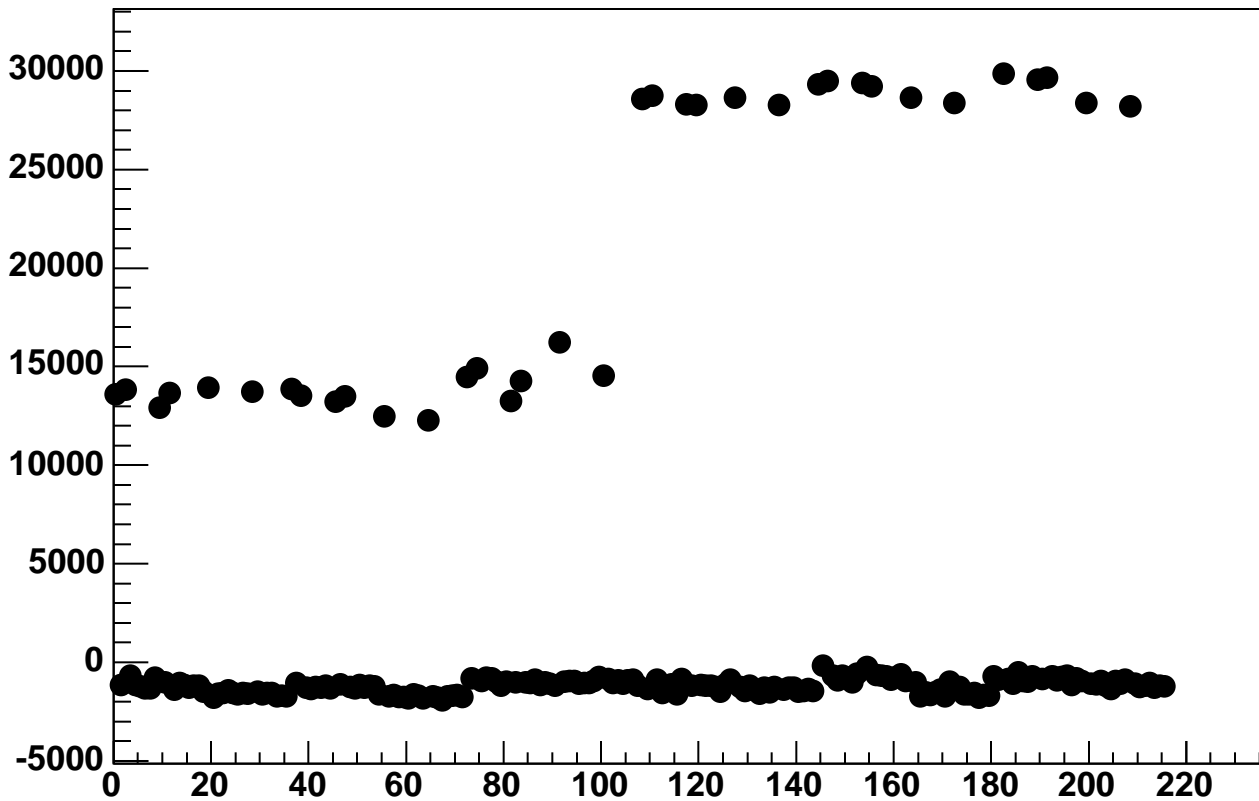
Enable 0, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



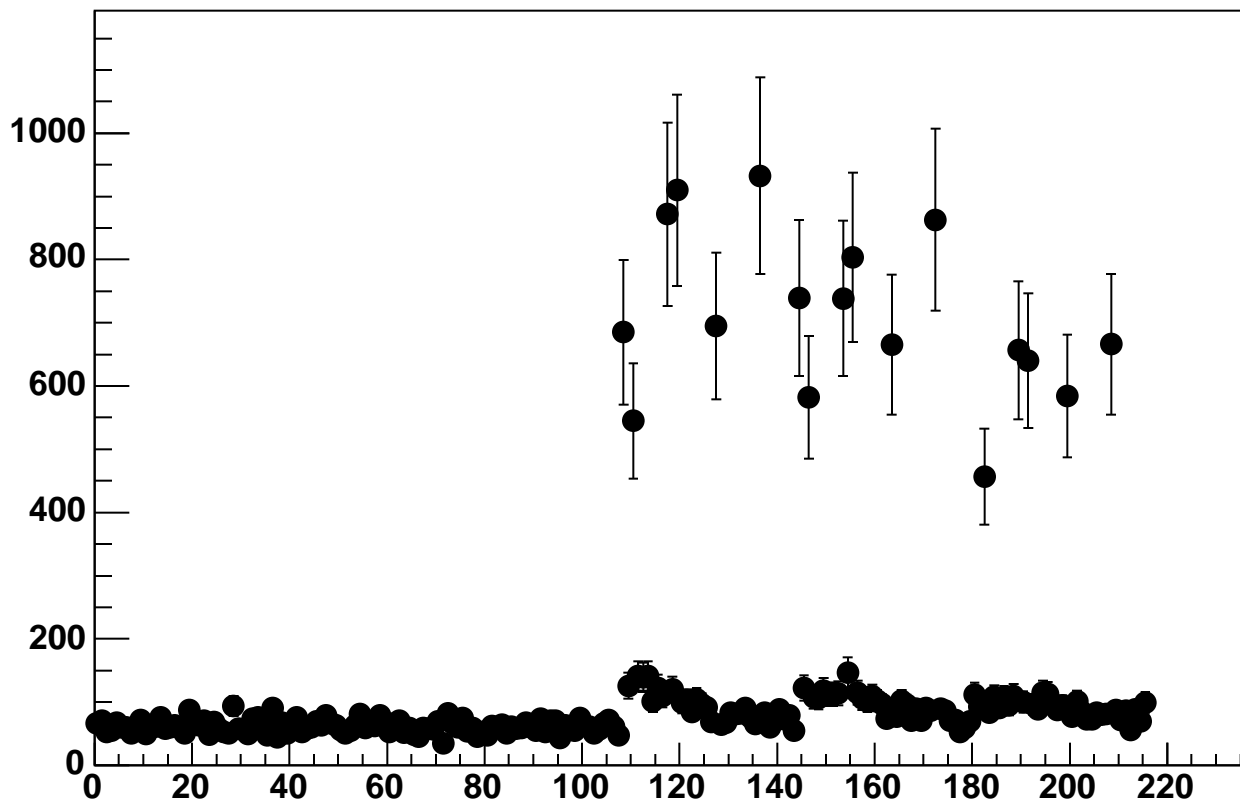
Enable 0, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



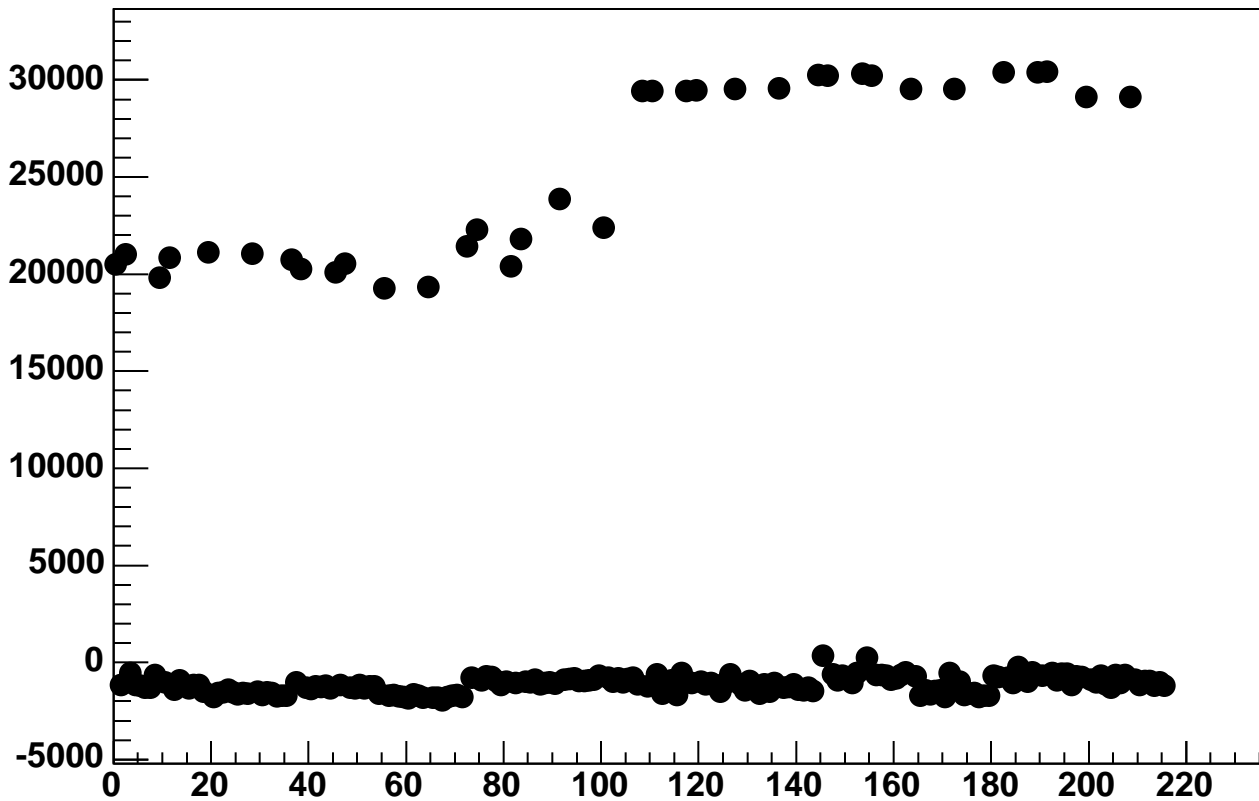
Enable 0, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan



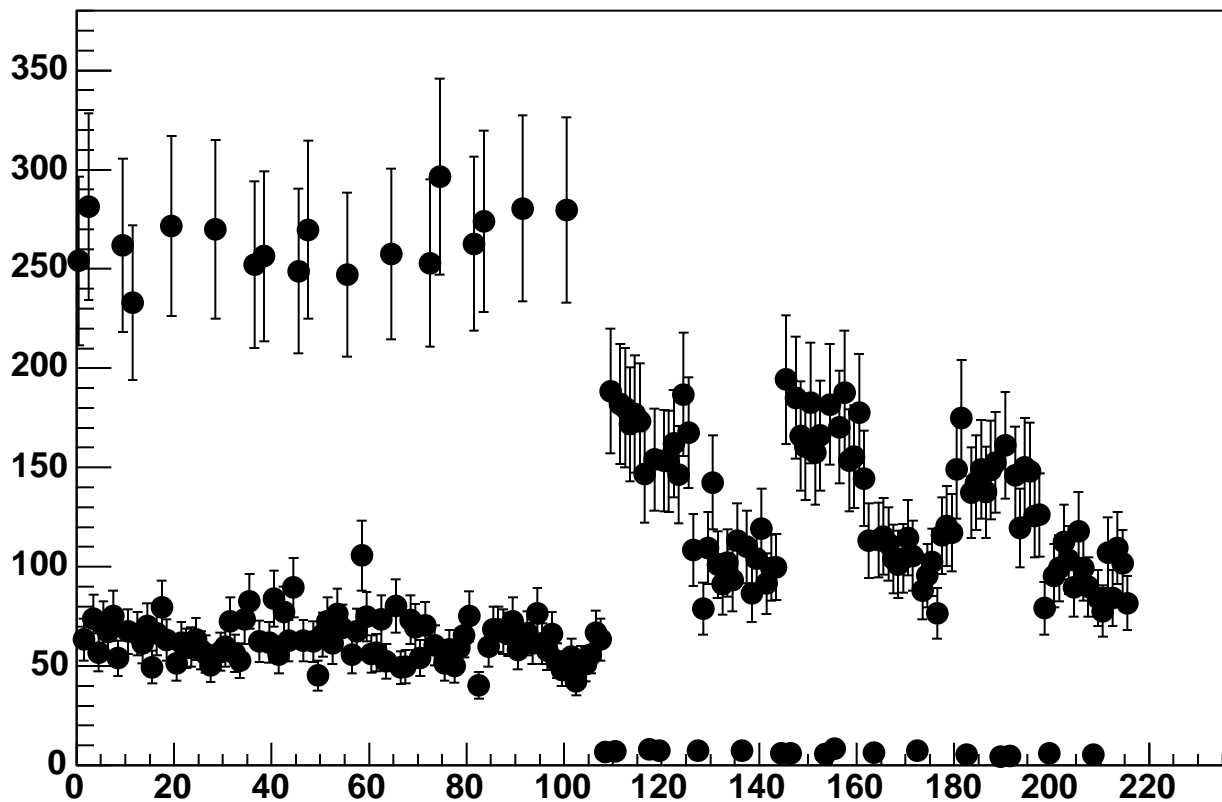
Enable 0, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan



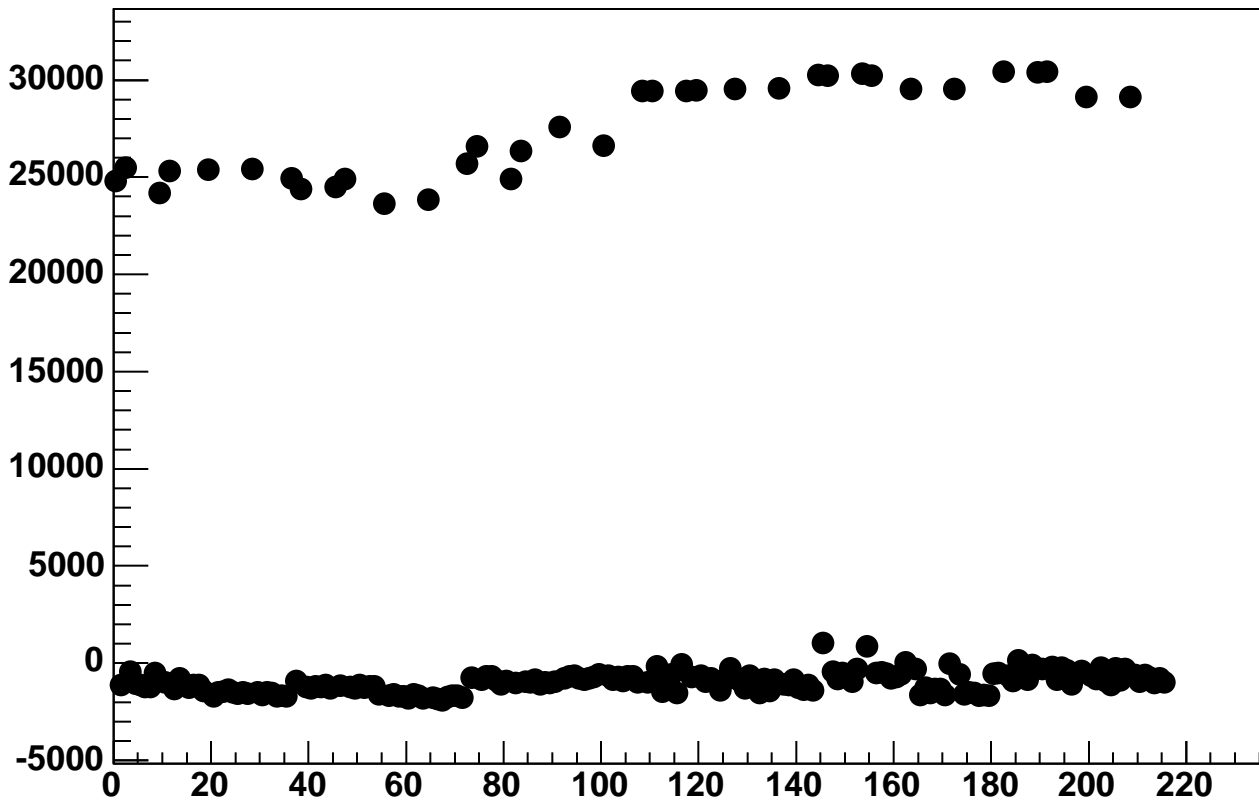
Enable 0, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



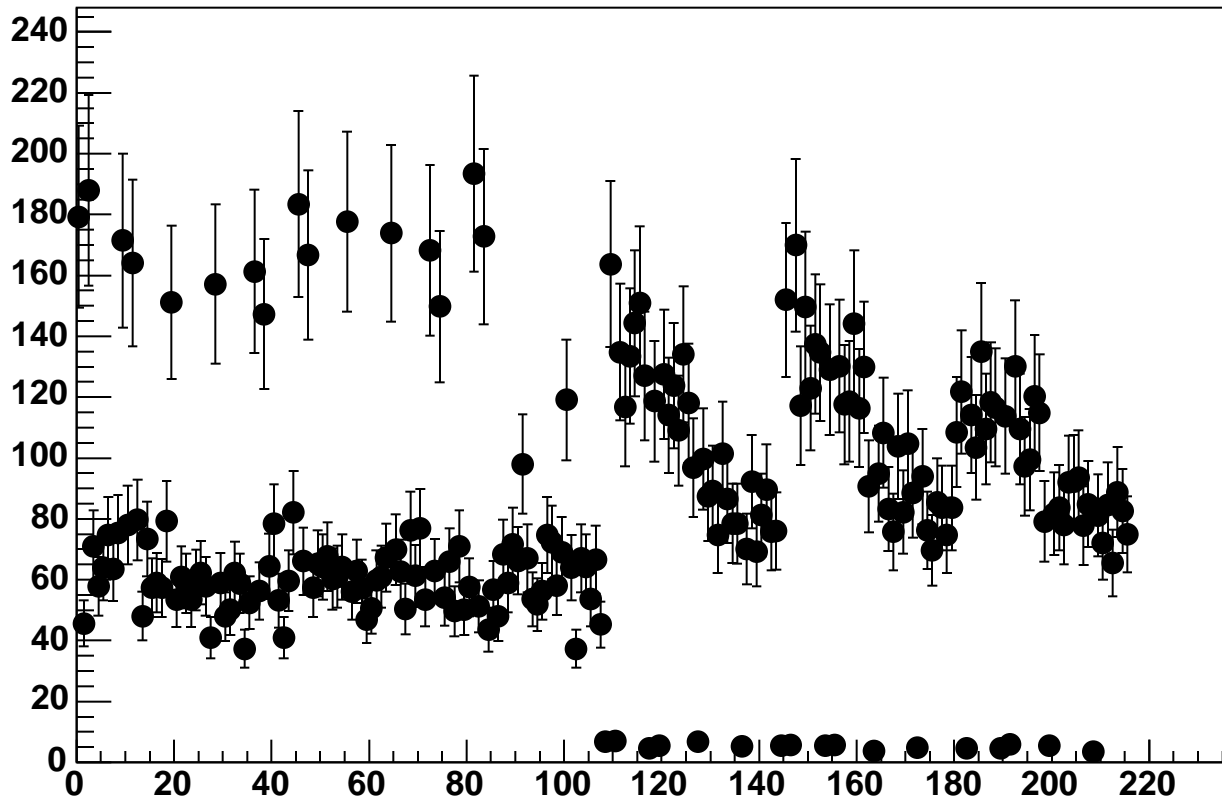
Enable 0, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan

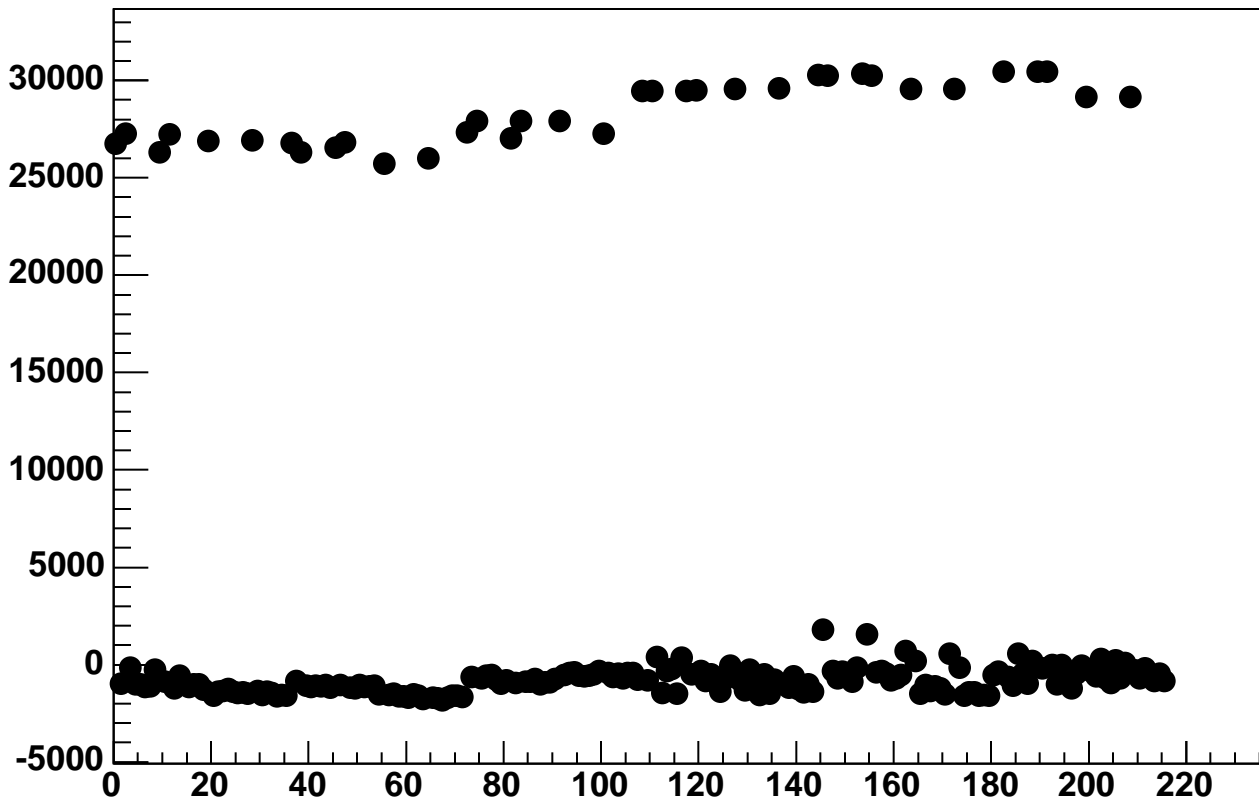


Enable 0, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan

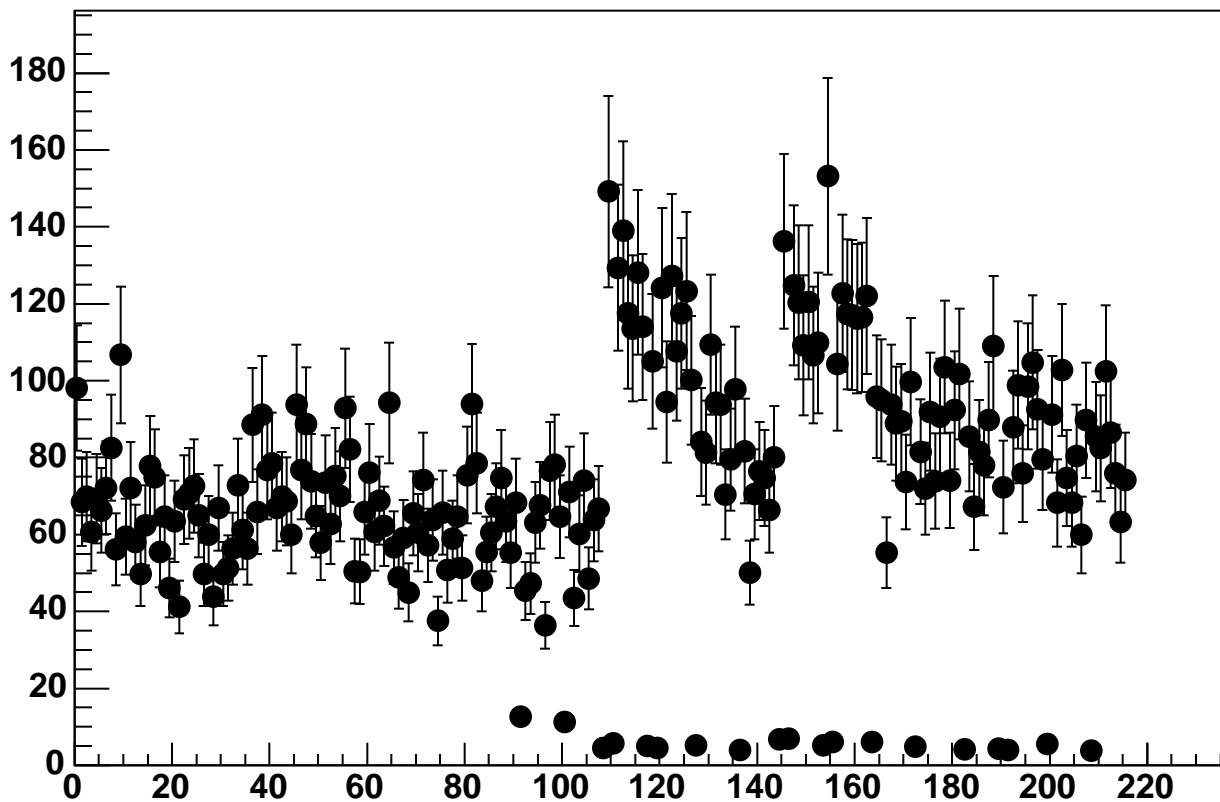




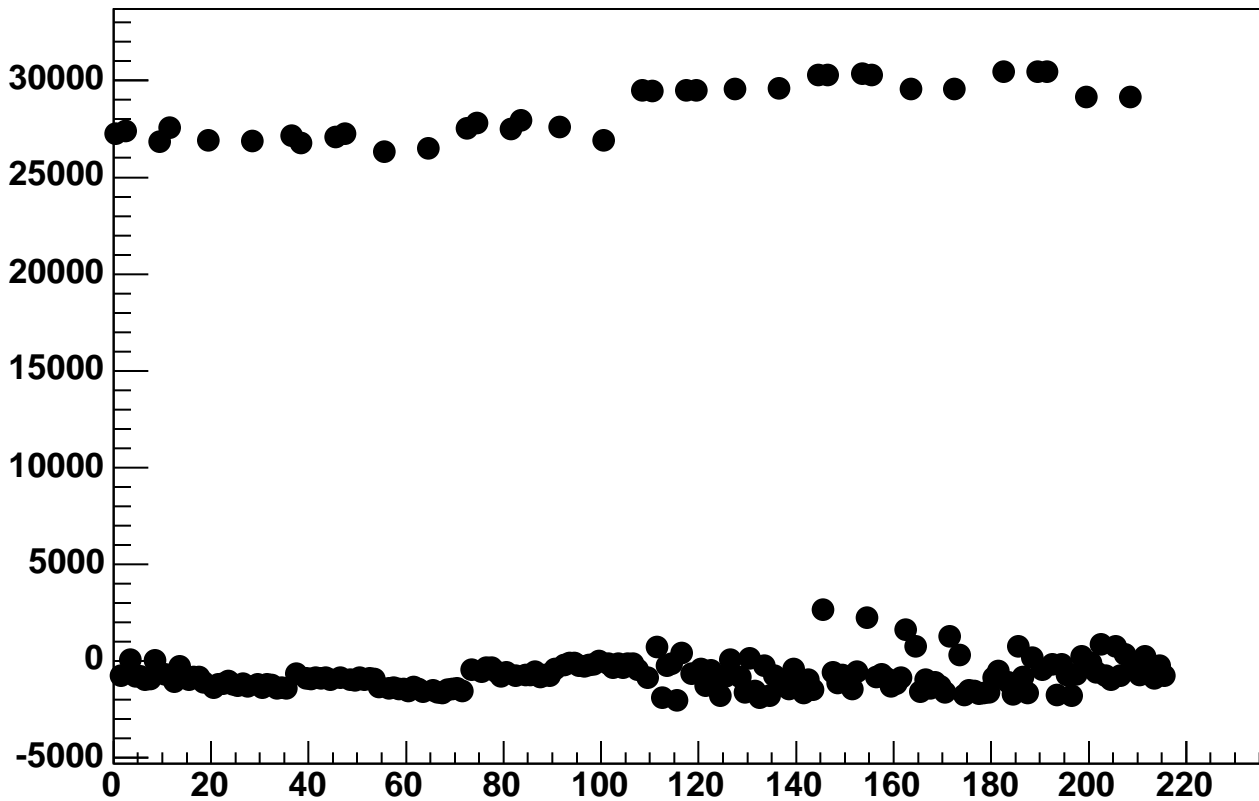
Enable 0, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



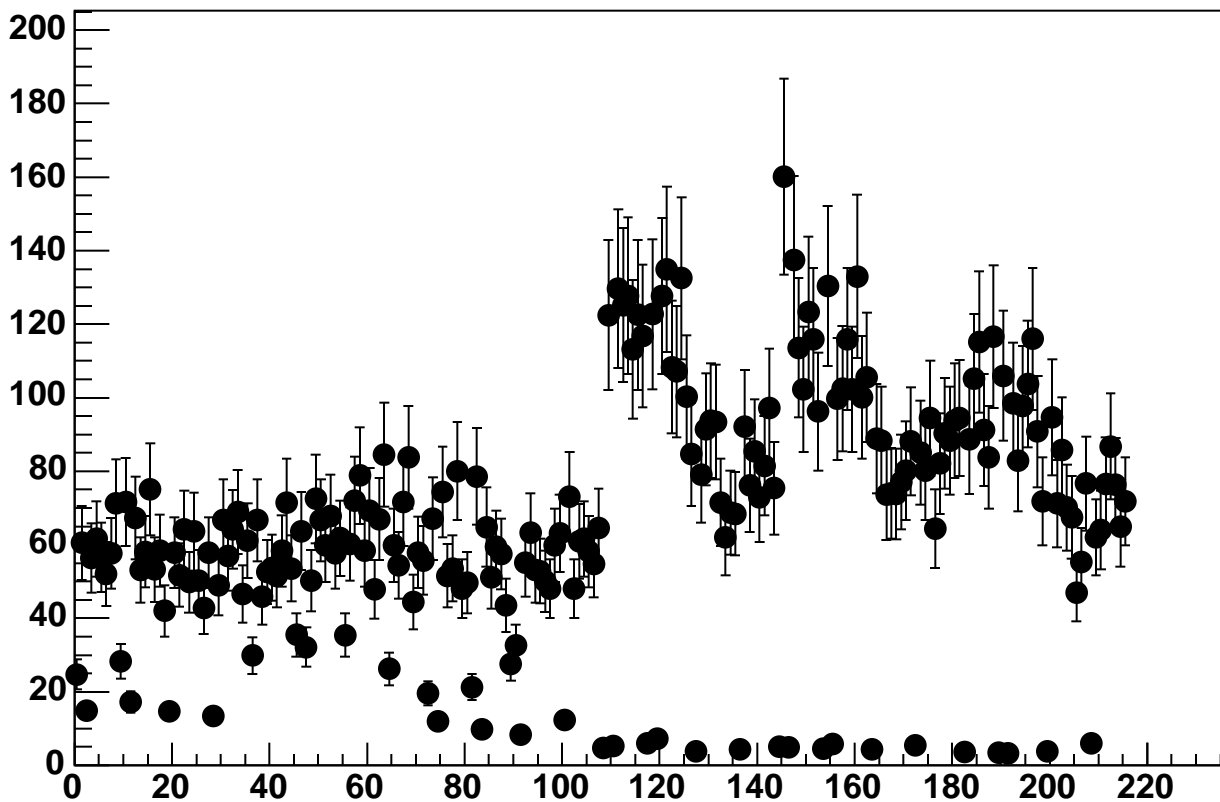
Enable 0, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



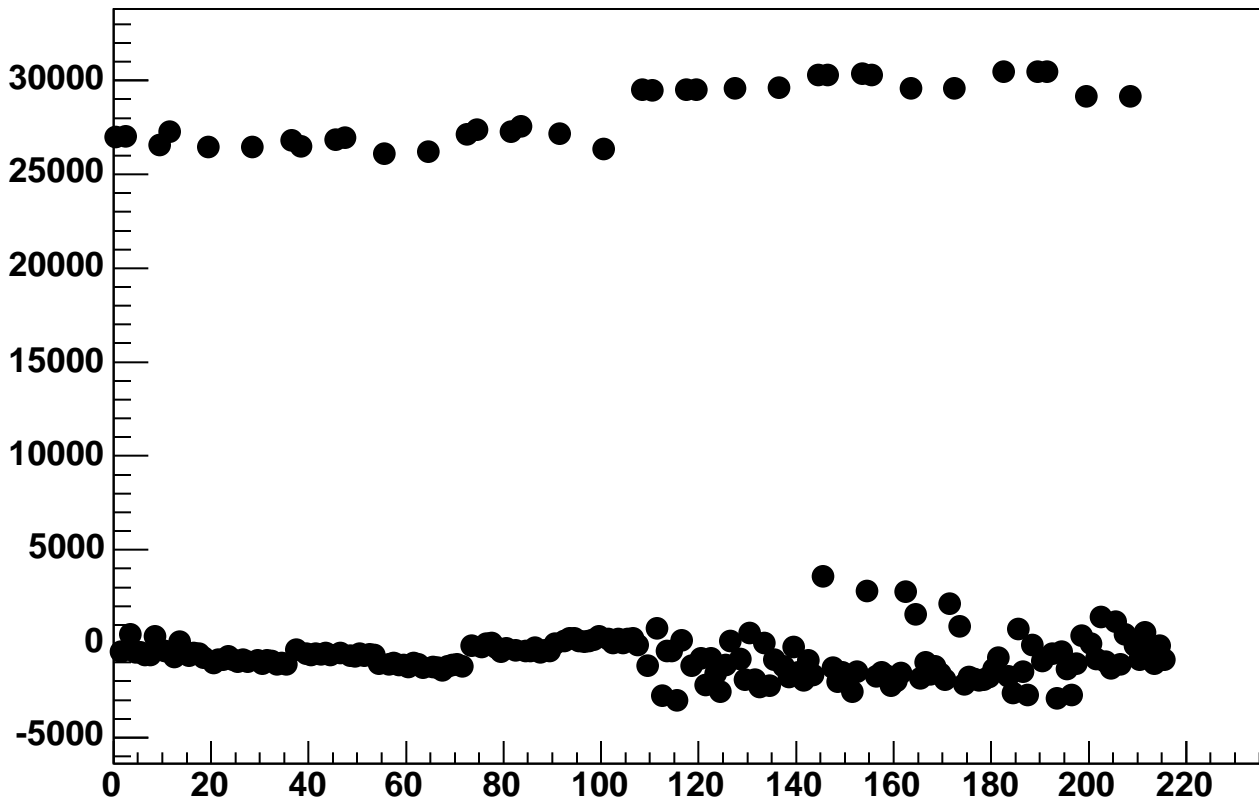
Enable 0, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan



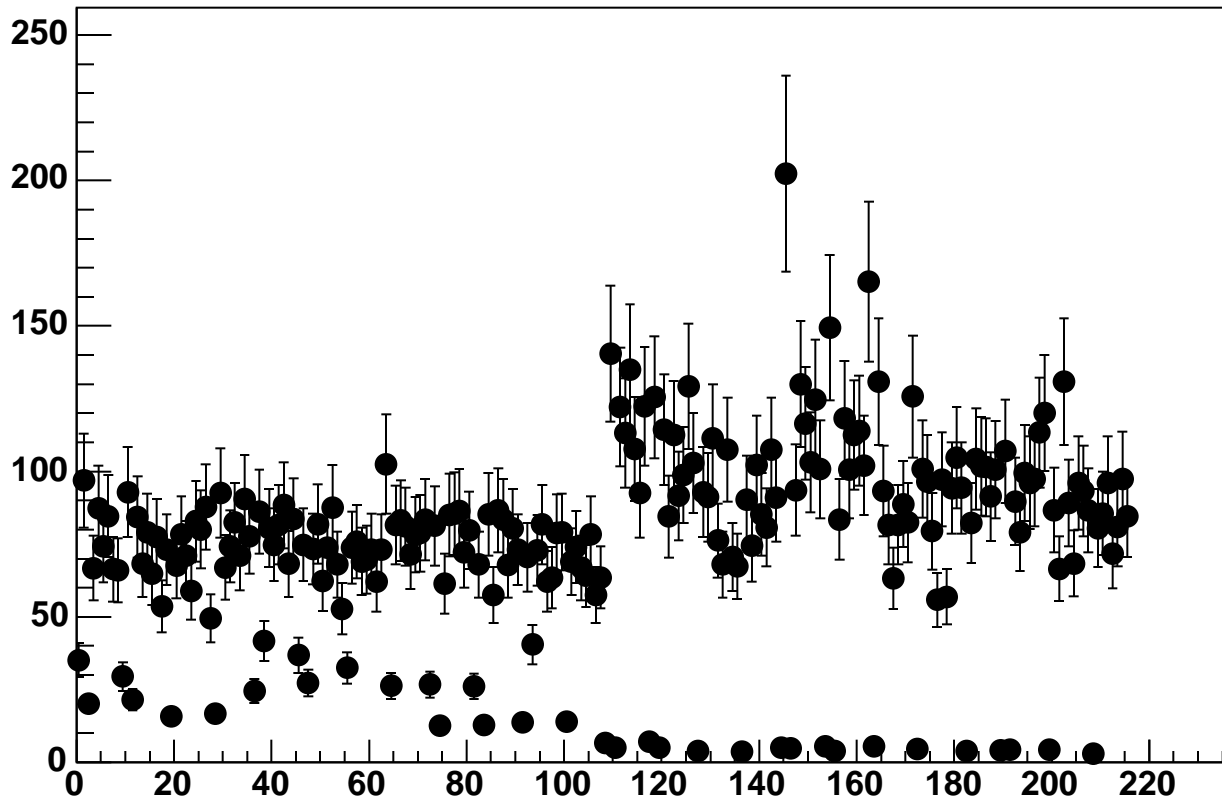
Enable 0, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan



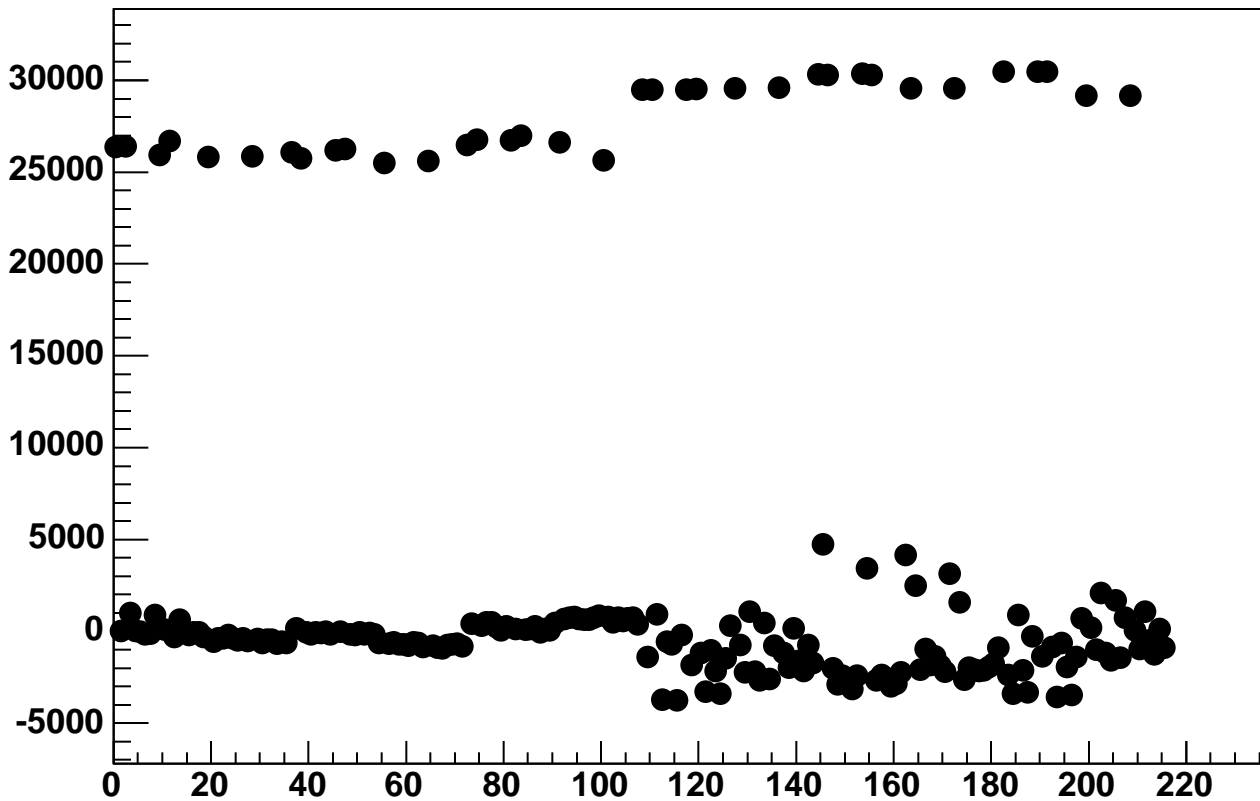
Enable 0, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



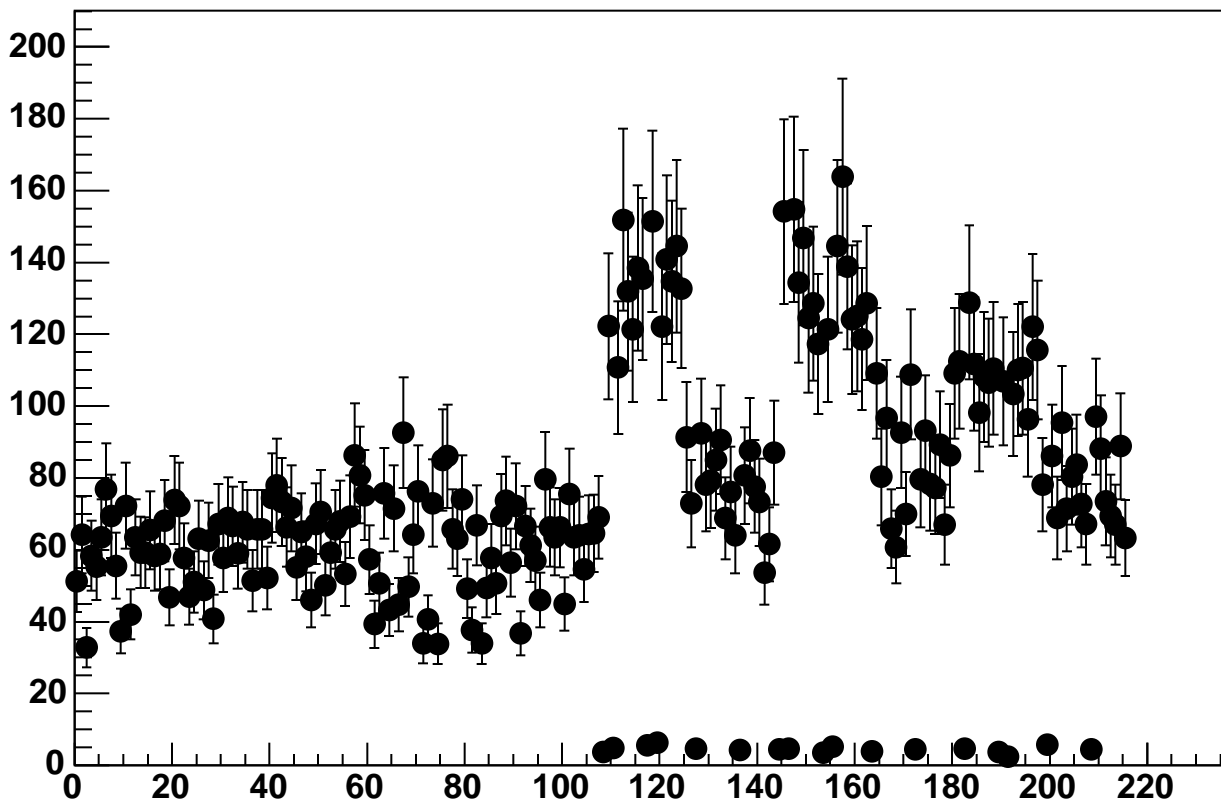
Enable 0, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



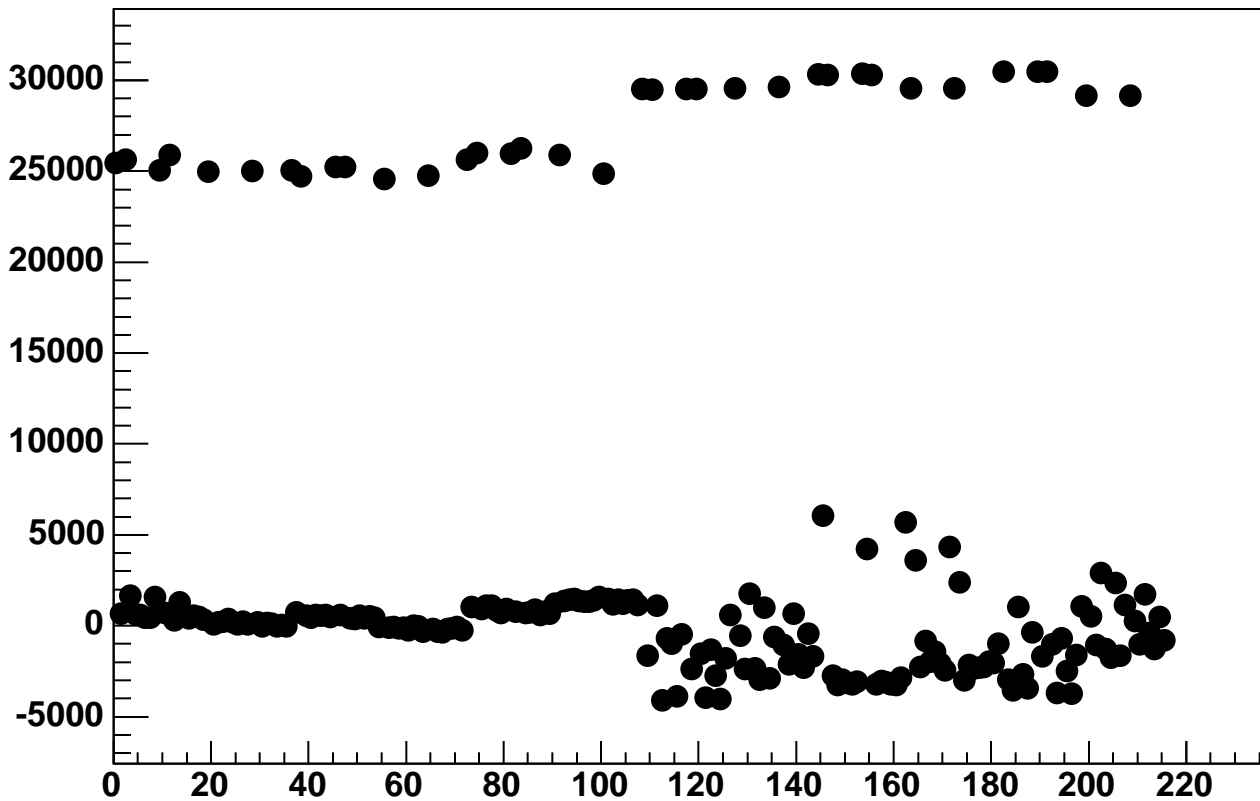
Enable 0, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan



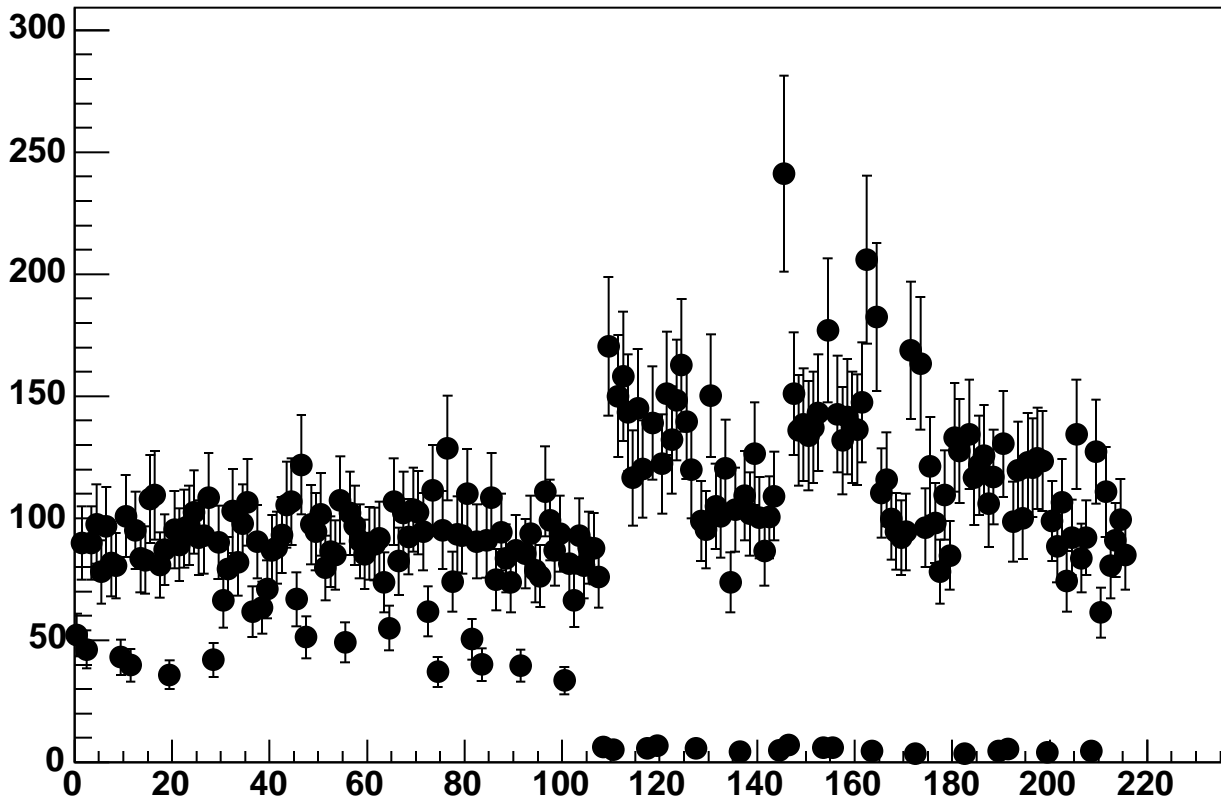
Enable 0, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan



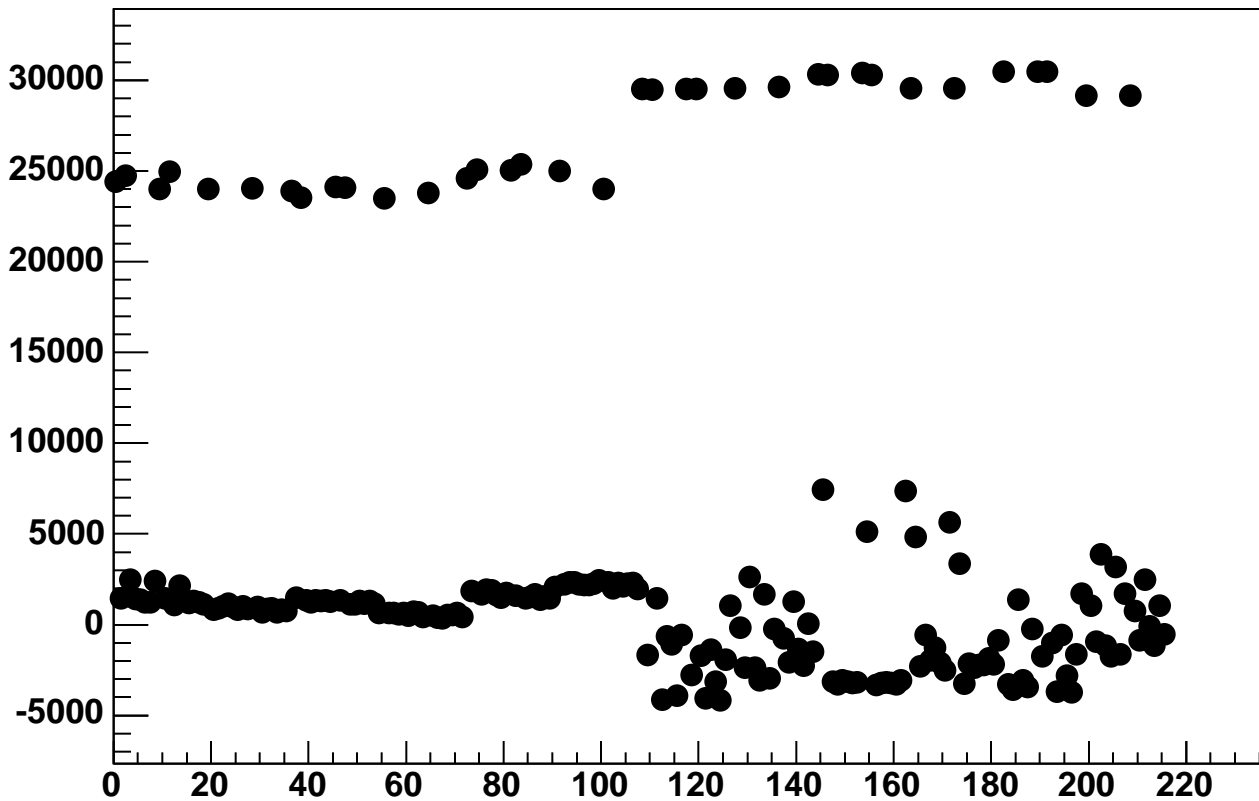
Enable 0, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



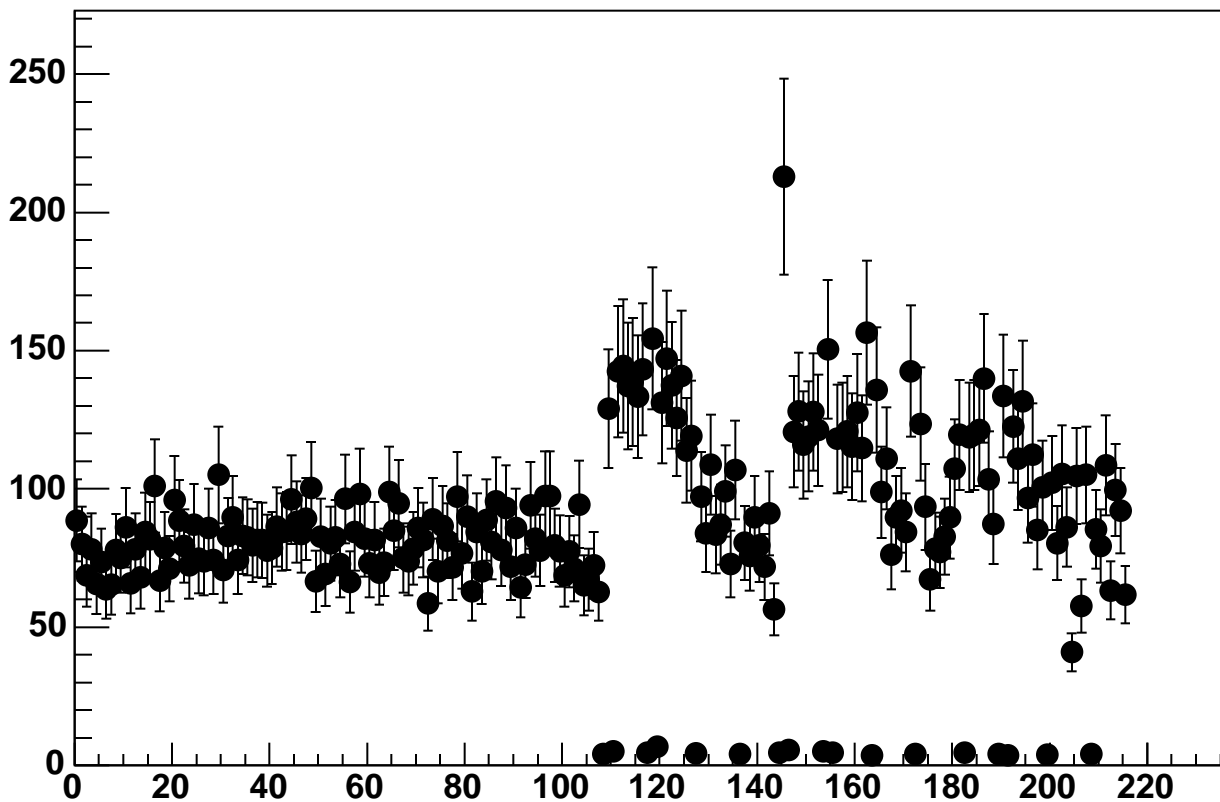
Enable 0, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



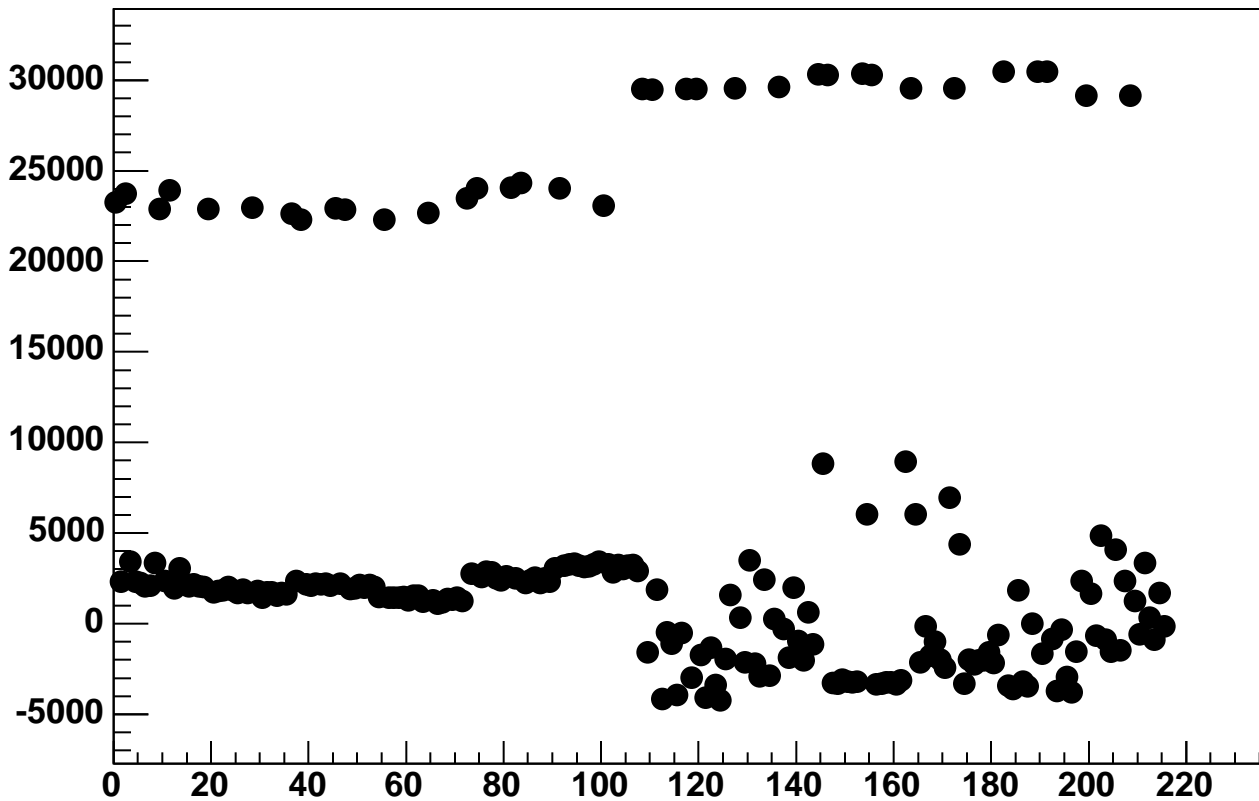
Enable 0, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan



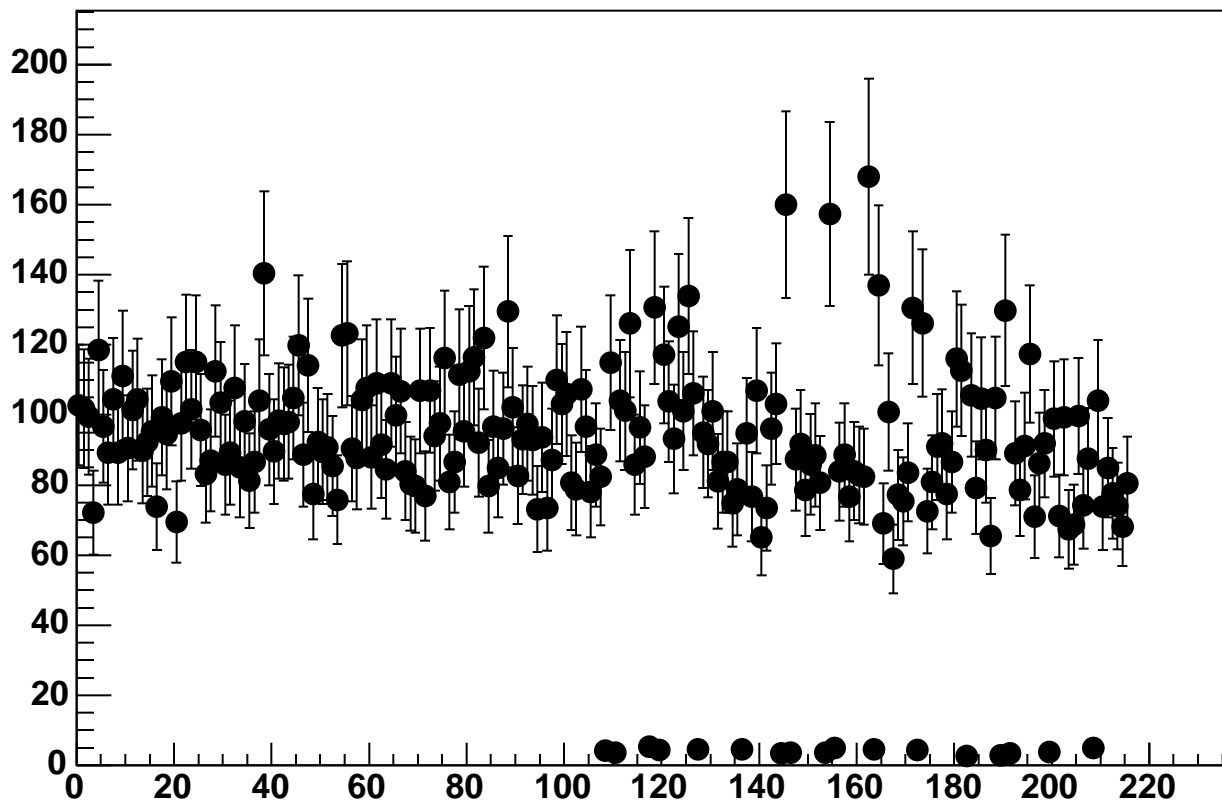
Enable 0, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan



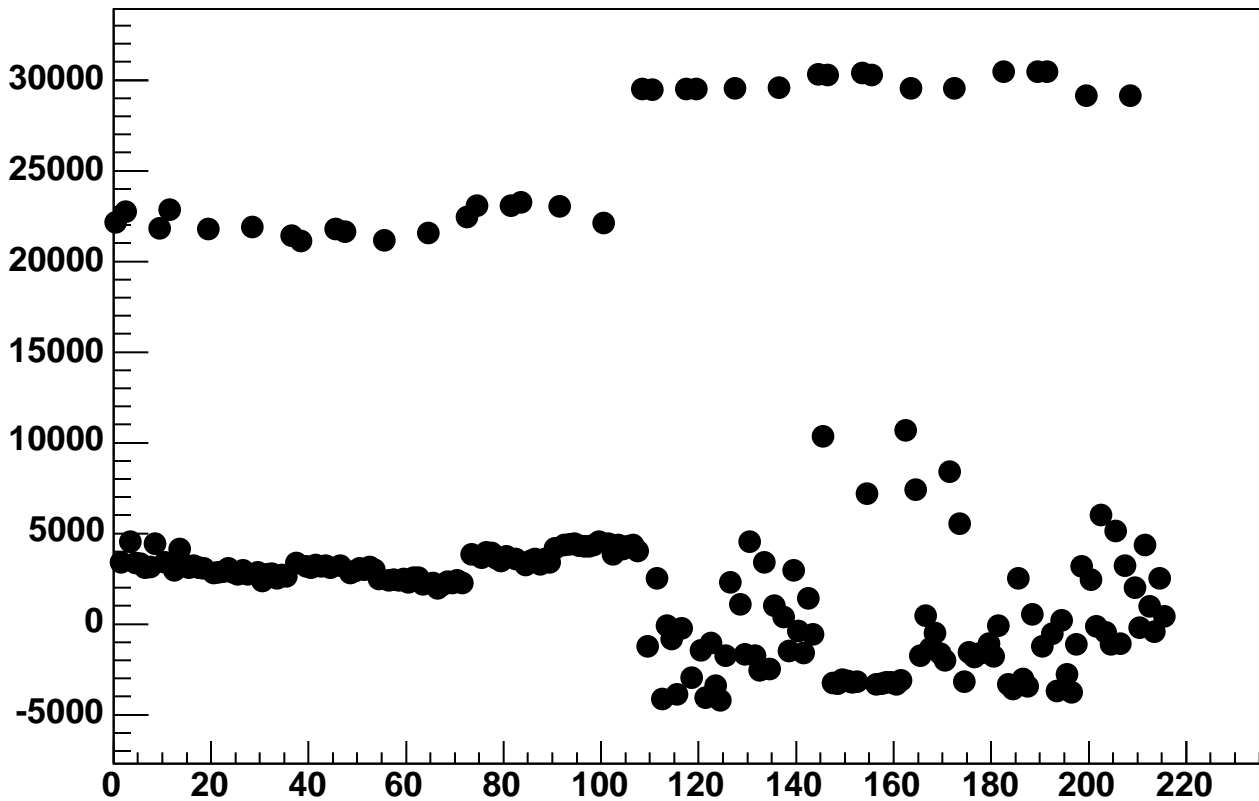
Enable 0, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



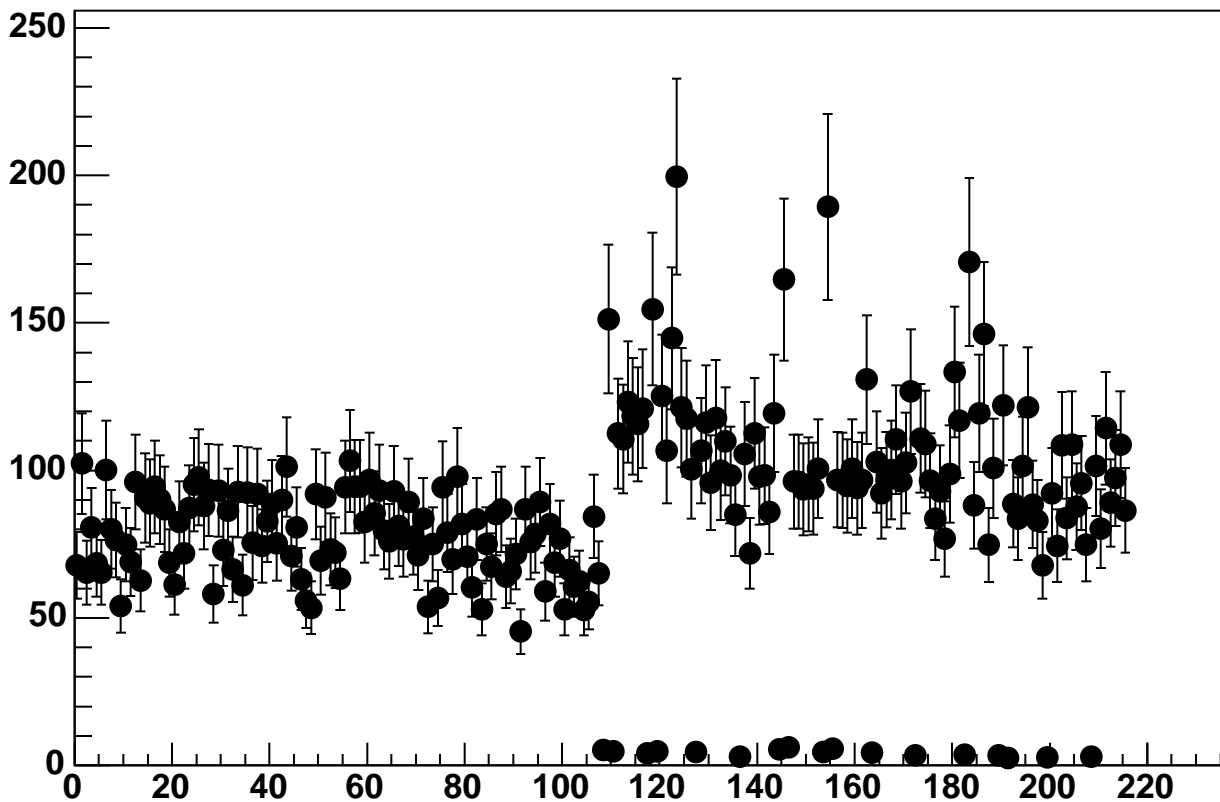
Enable 0, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan

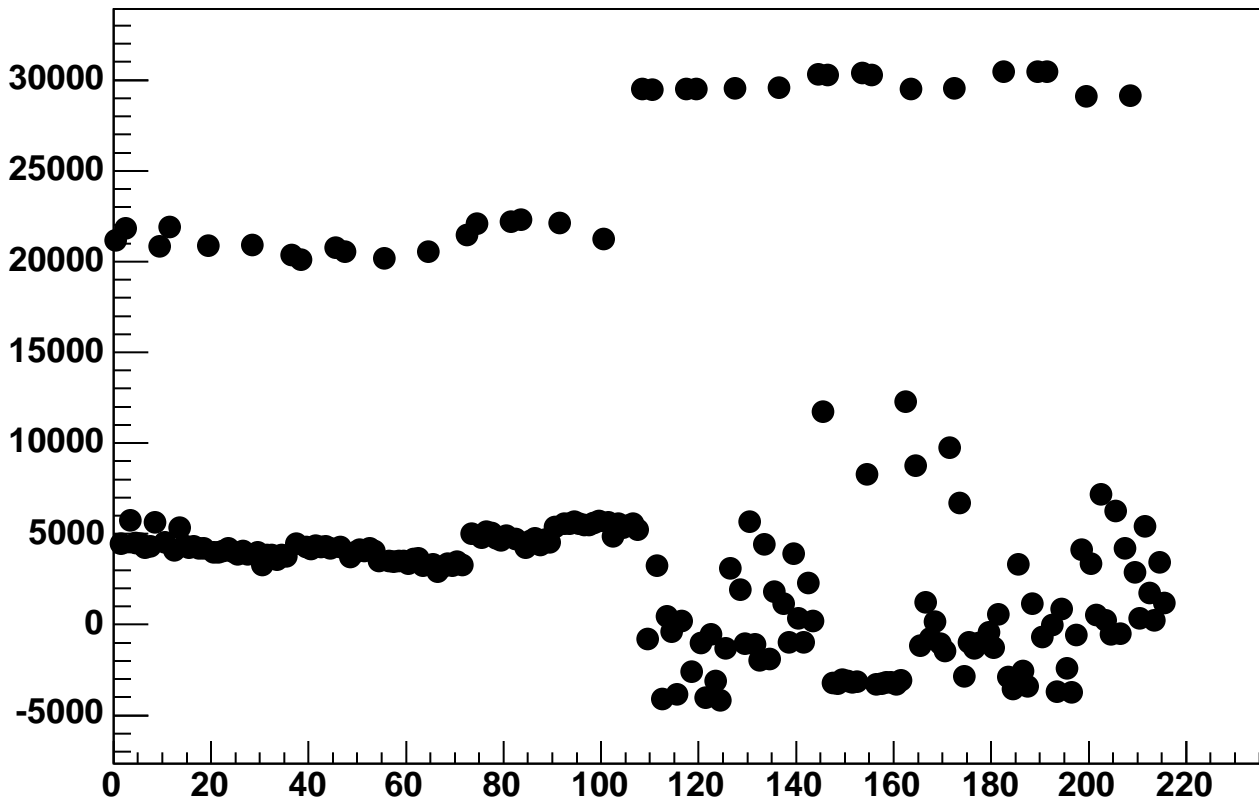


Enable 0, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan

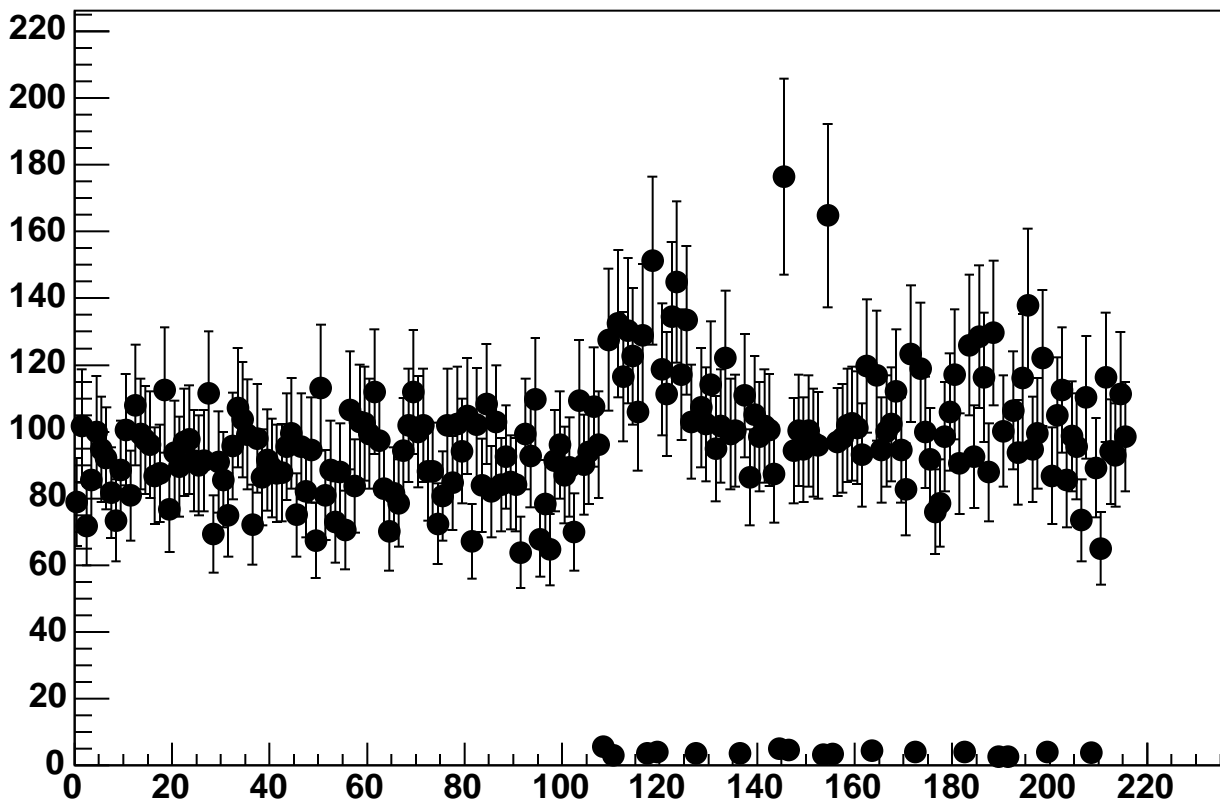




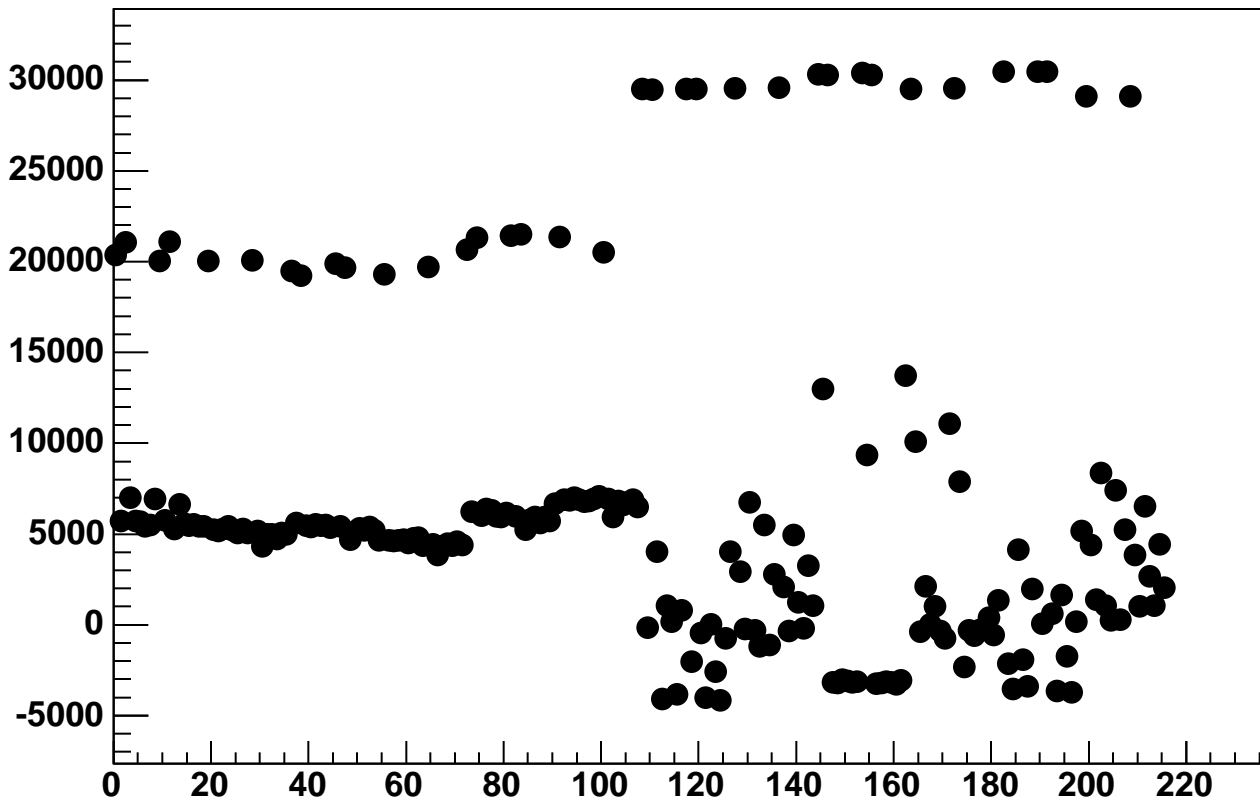
Enable 0, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



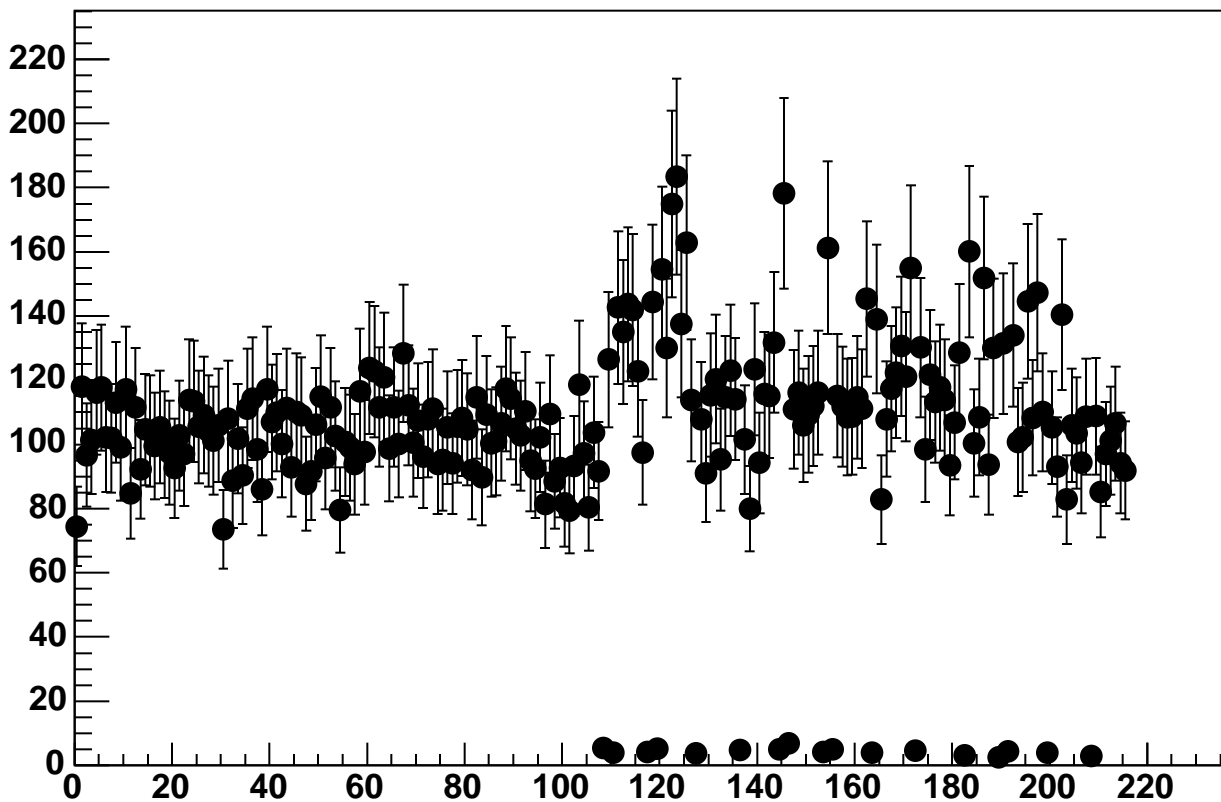
Enable 0, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



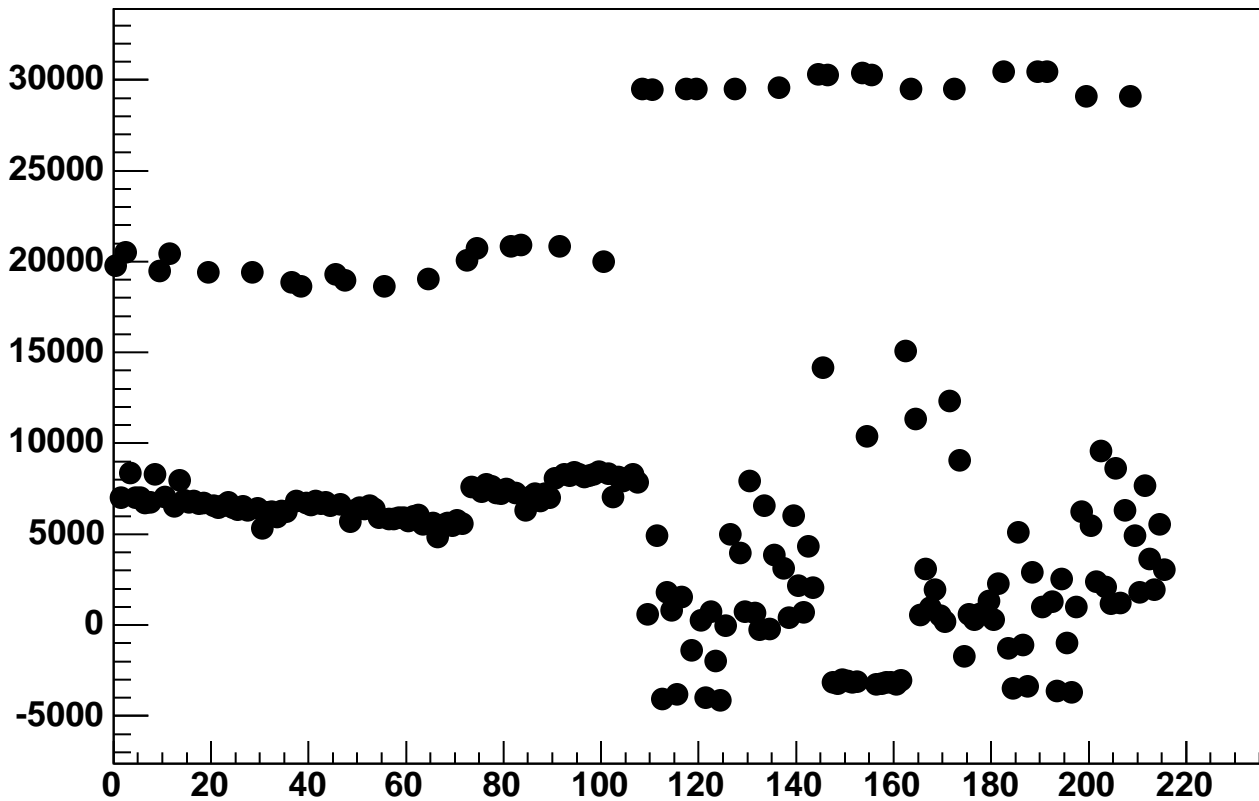
Enable 0, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan



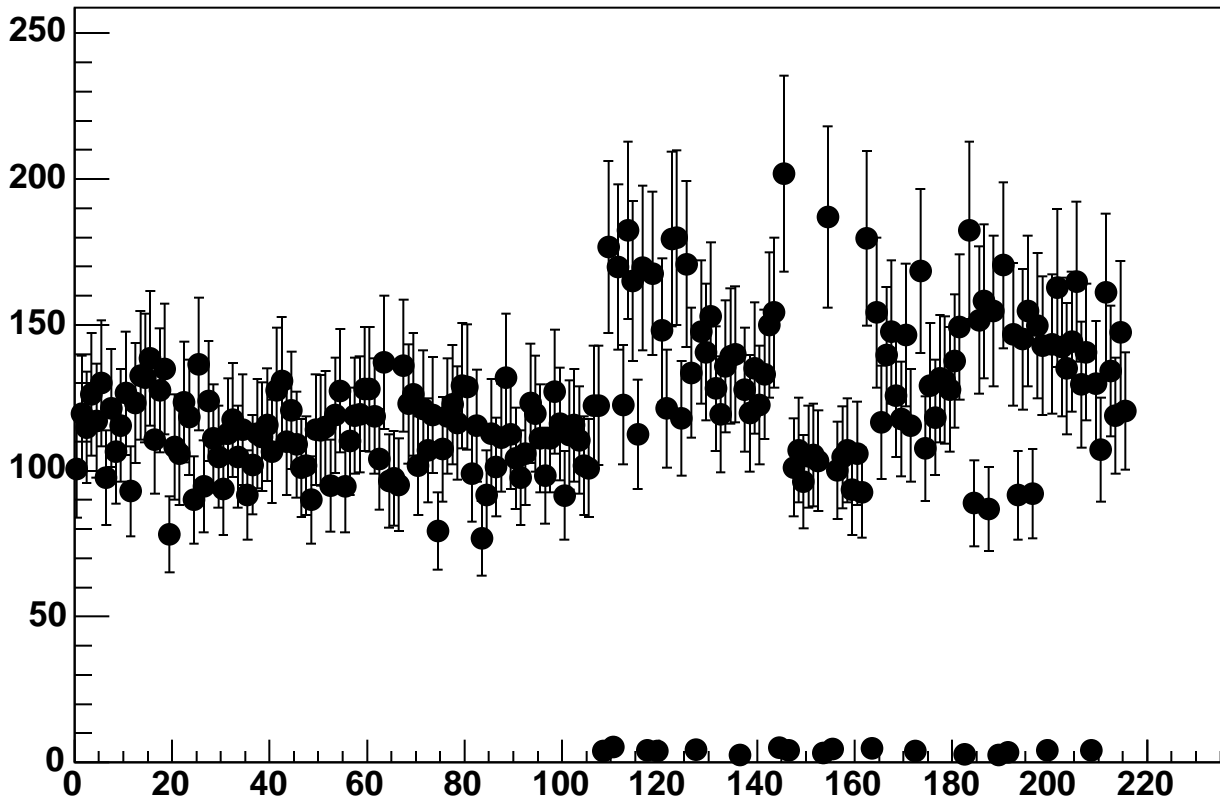
Enable 0, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan



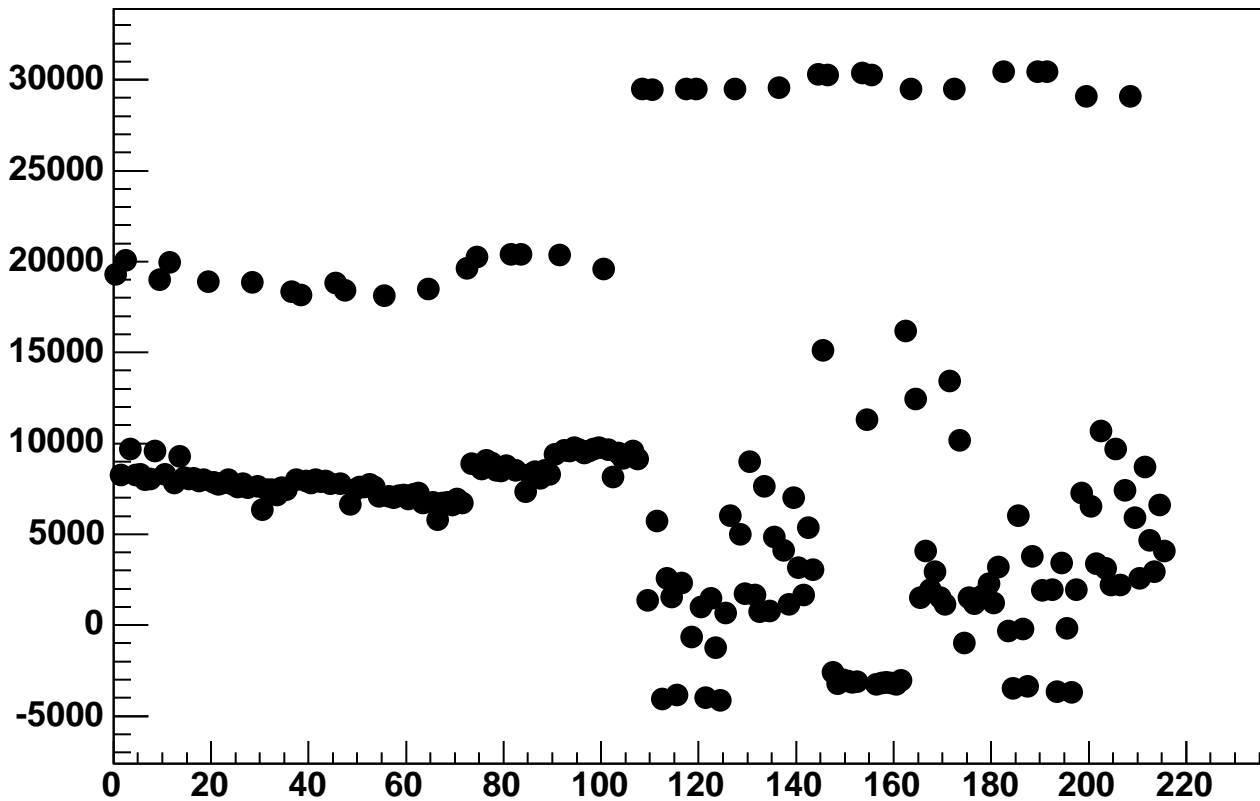
Enable 0, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



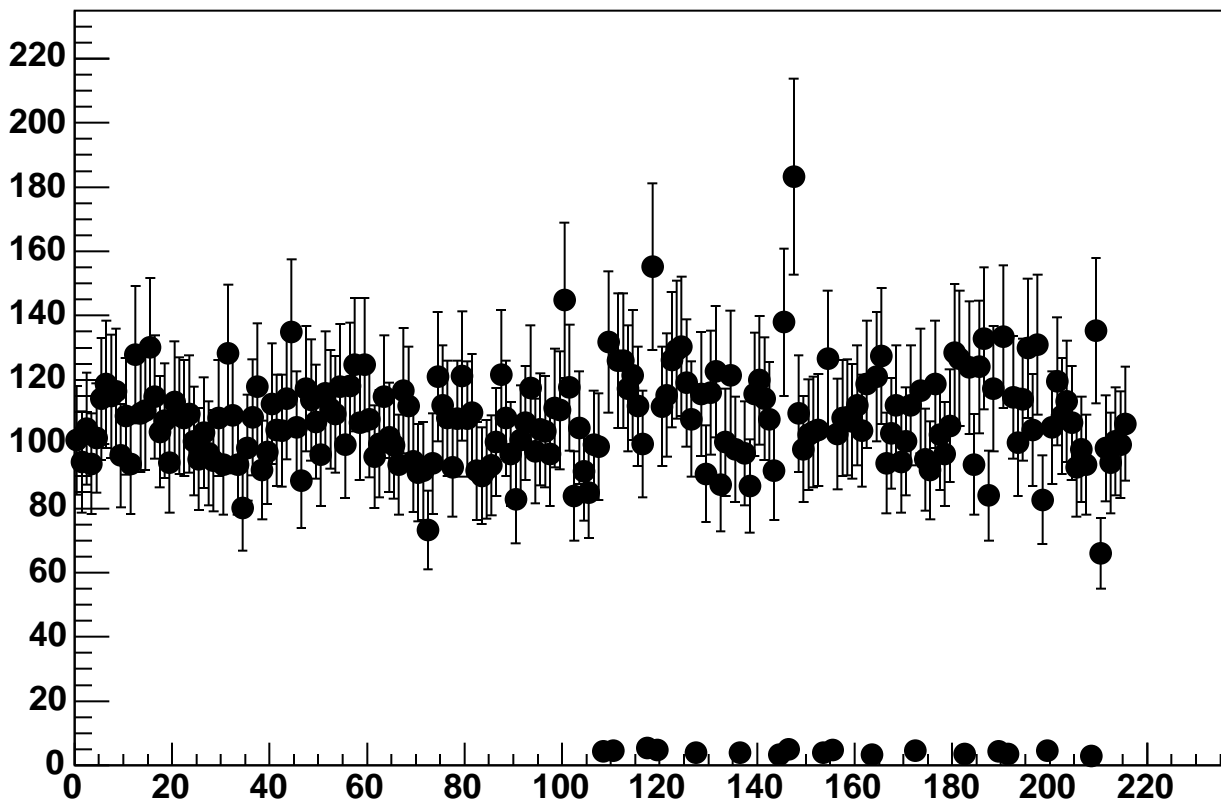
Enable 0, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



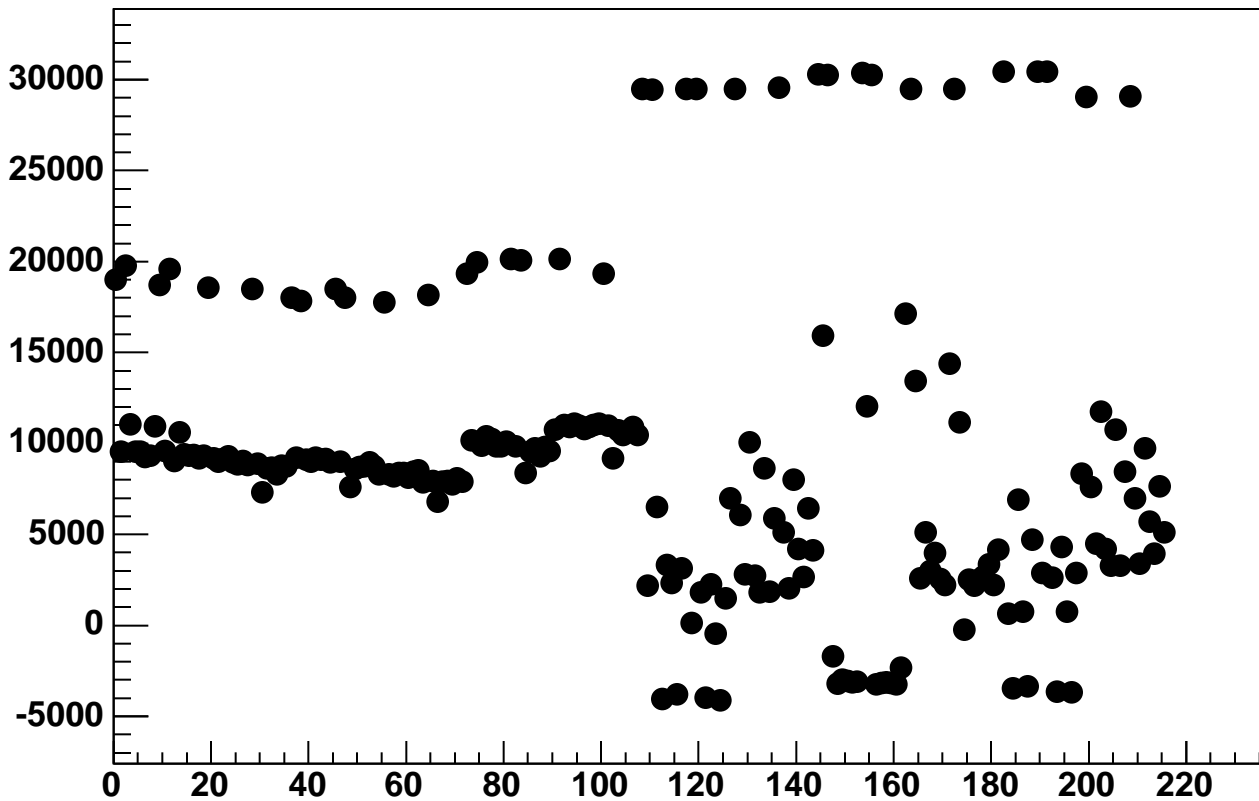
Enable 0, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan



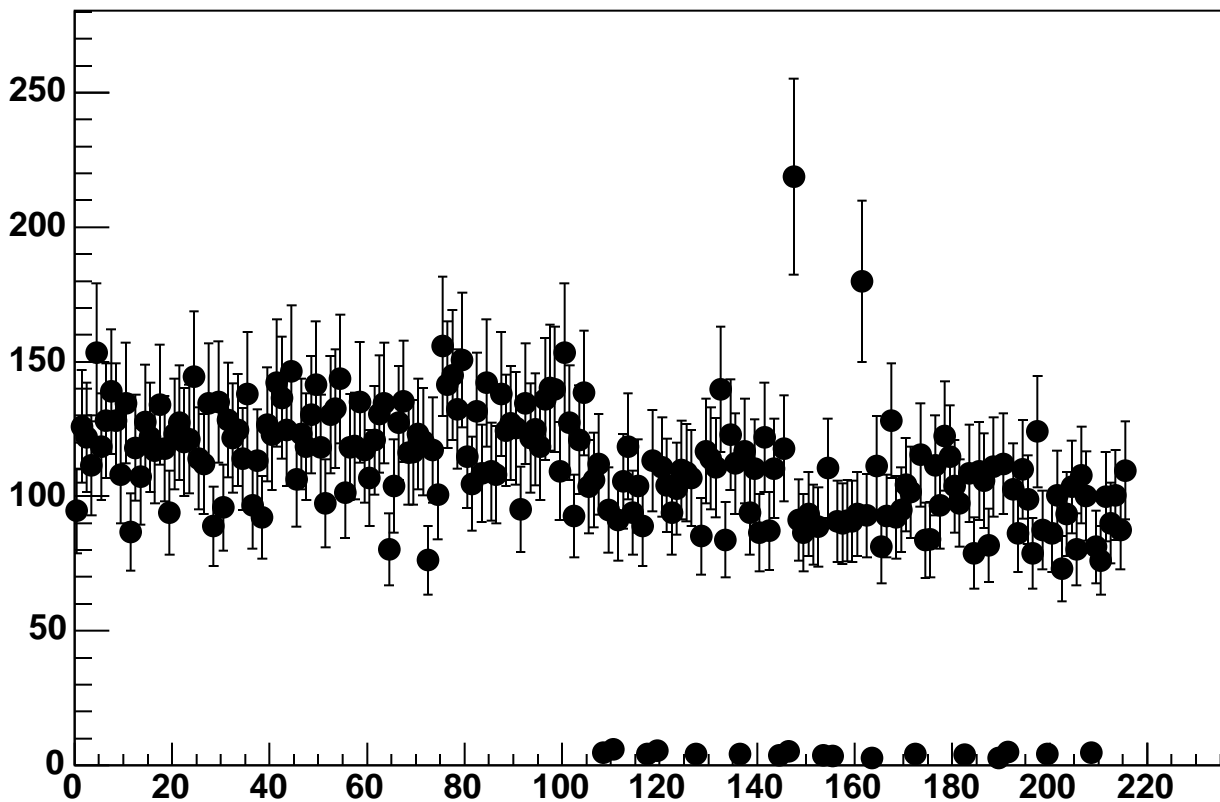
Enable 0, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan



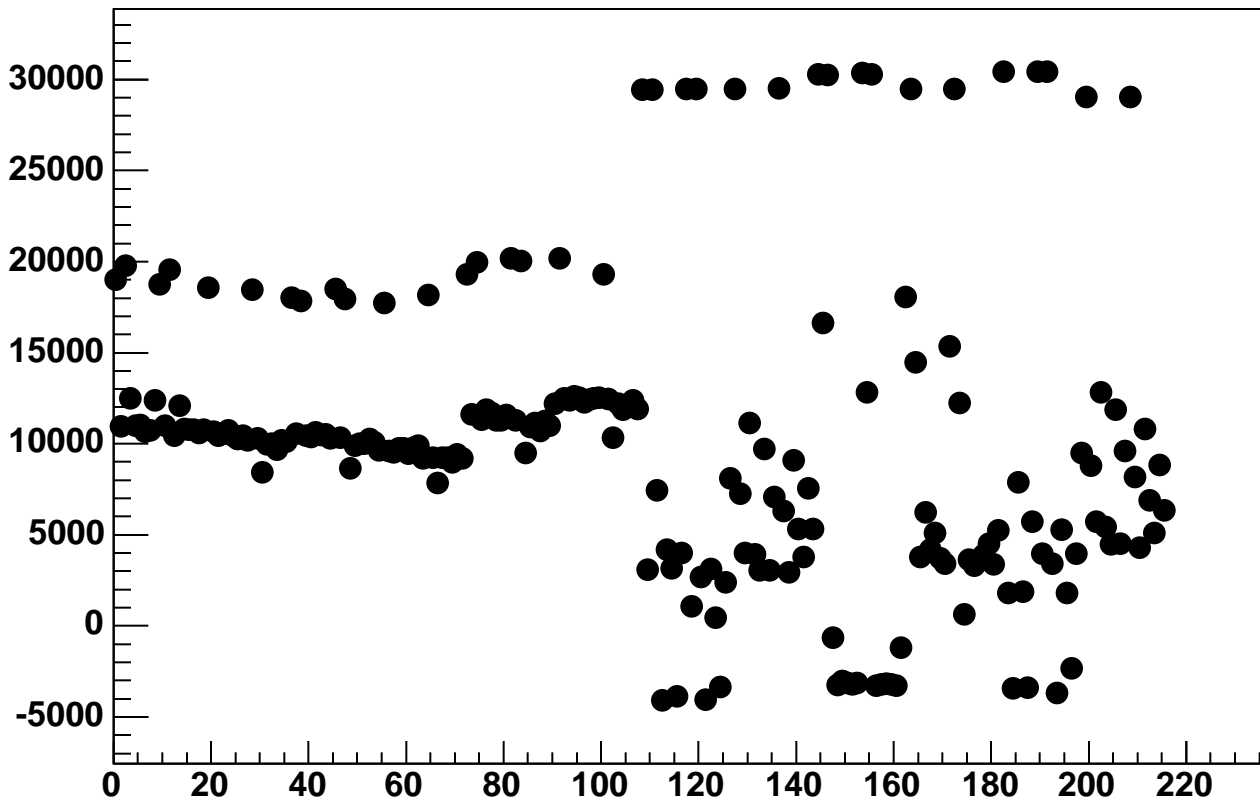
Enable 0, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



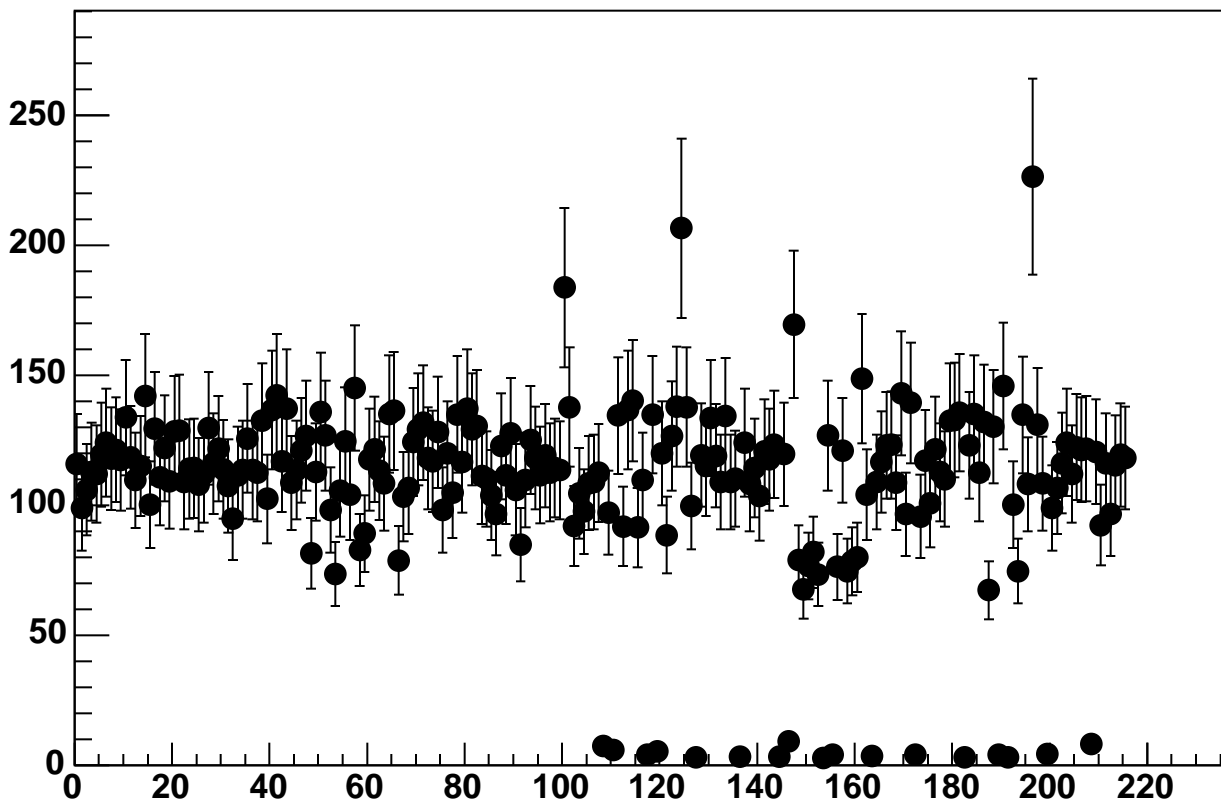
Enable 0, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



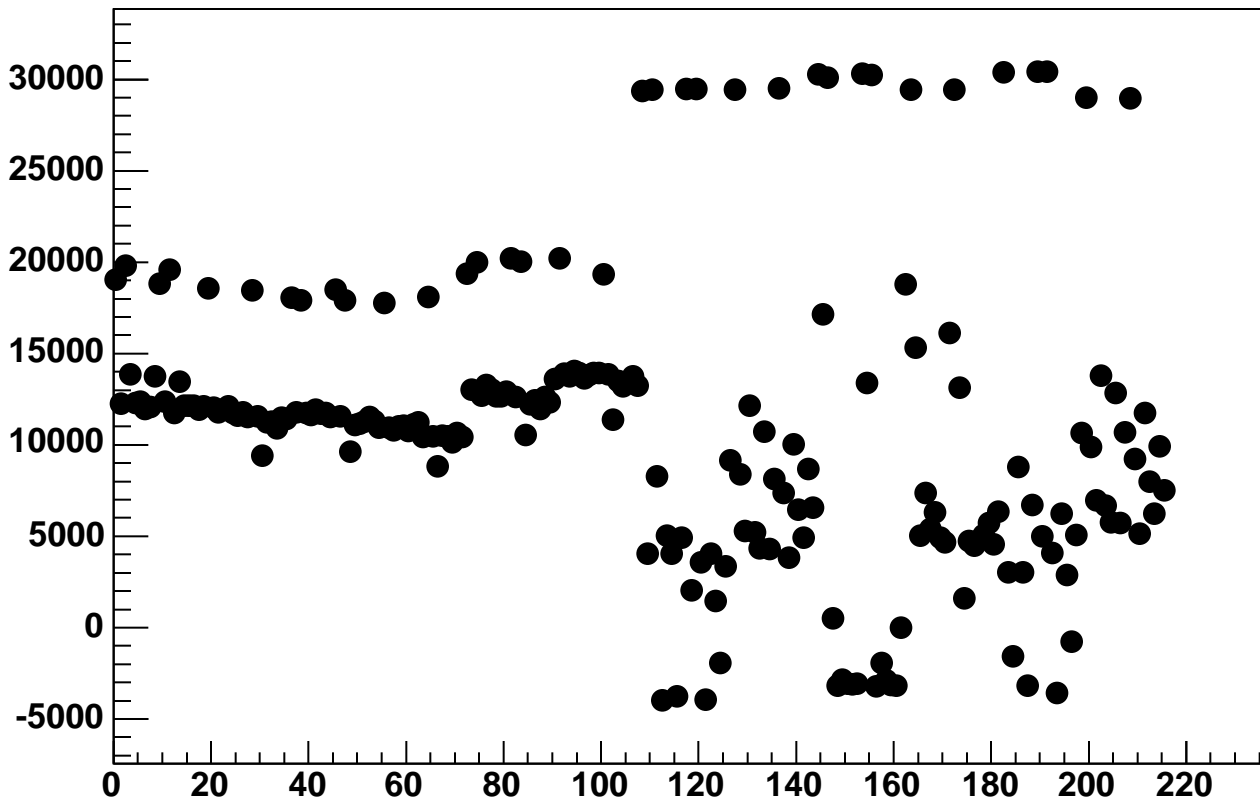
Enable 0, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan



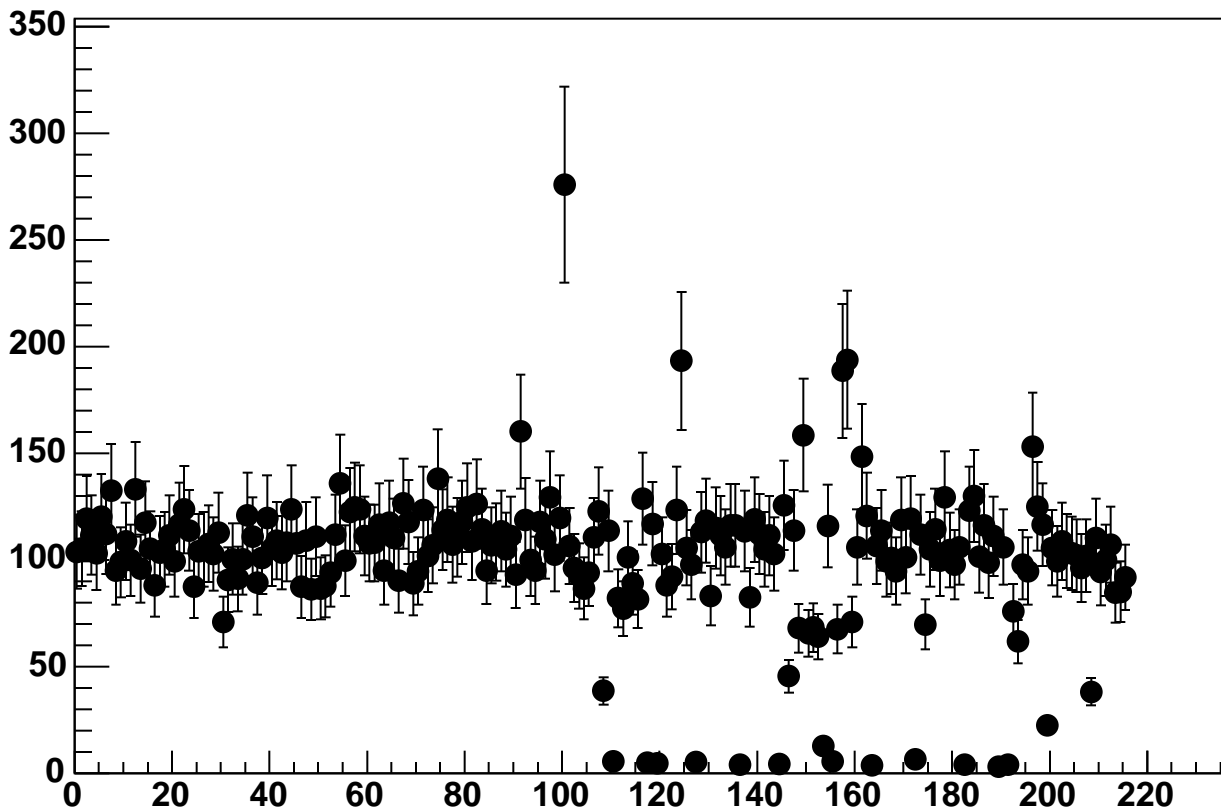
Enable 0, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan



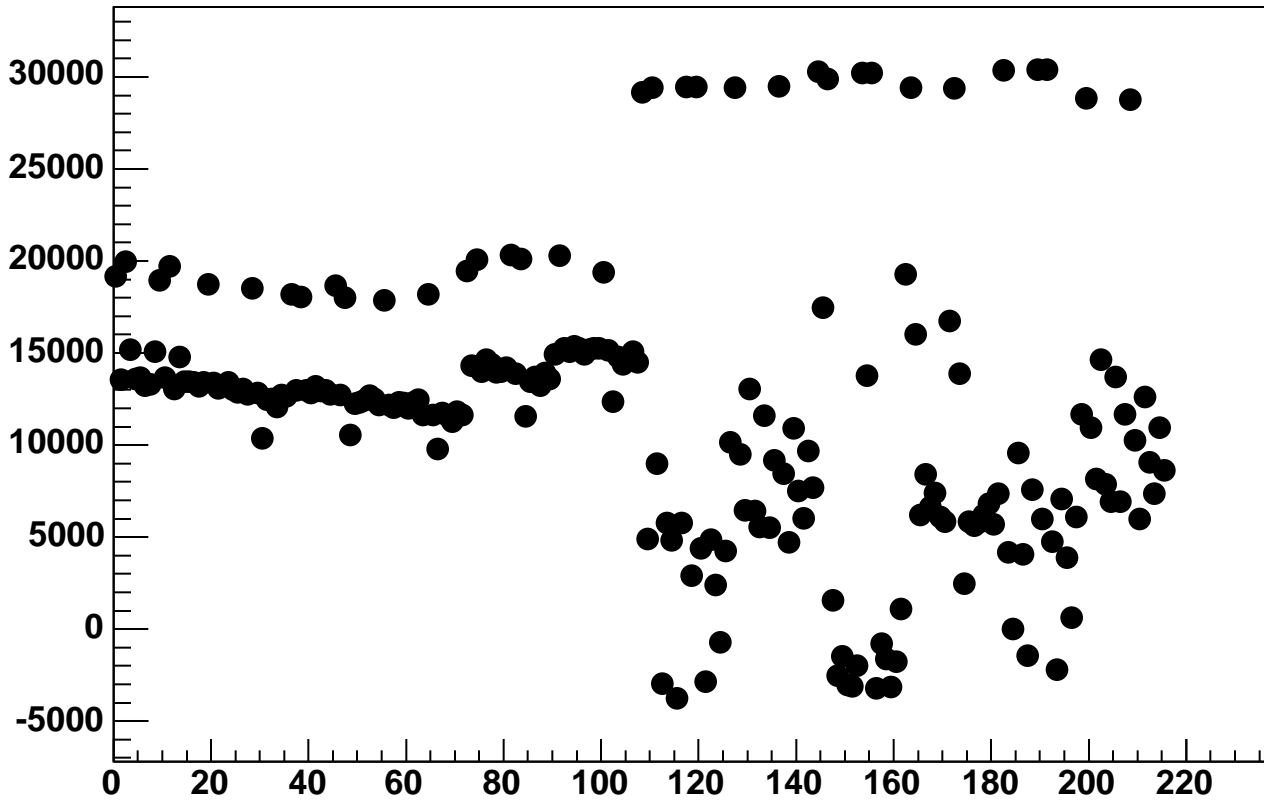
Enable 0, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



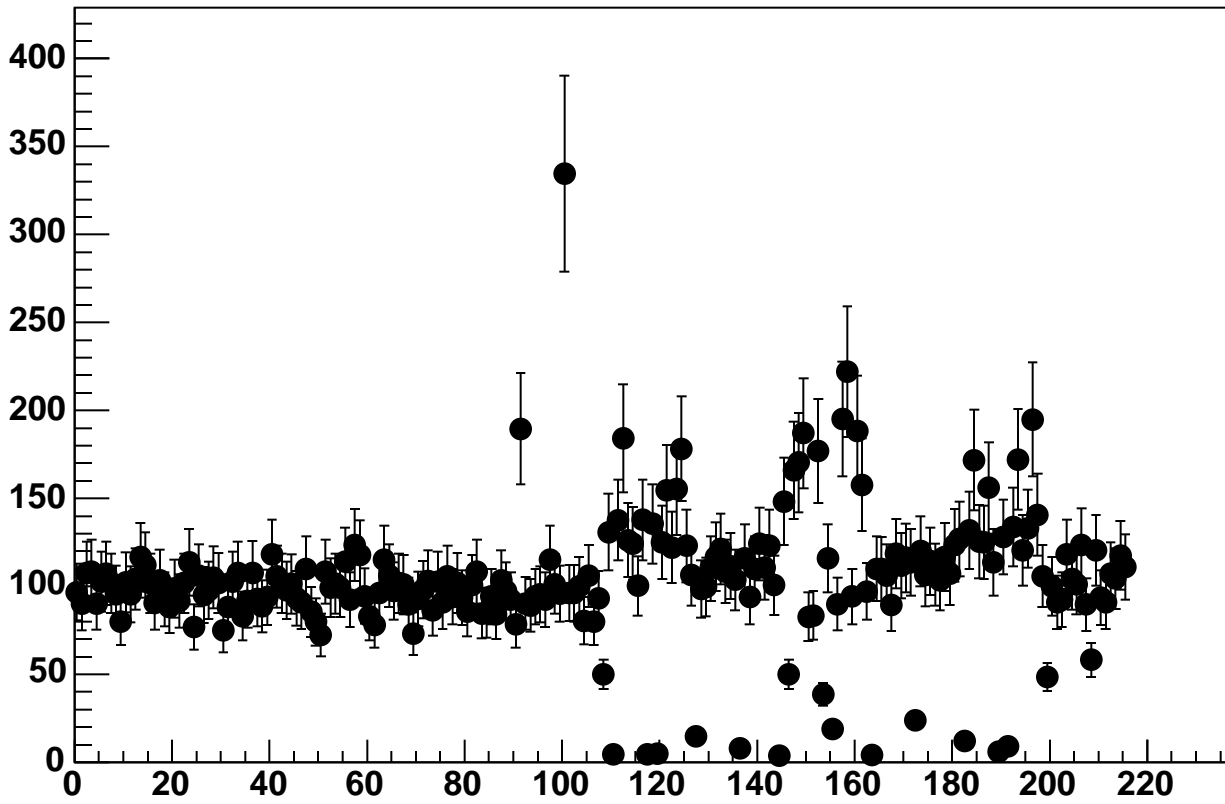
Enable 0, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan

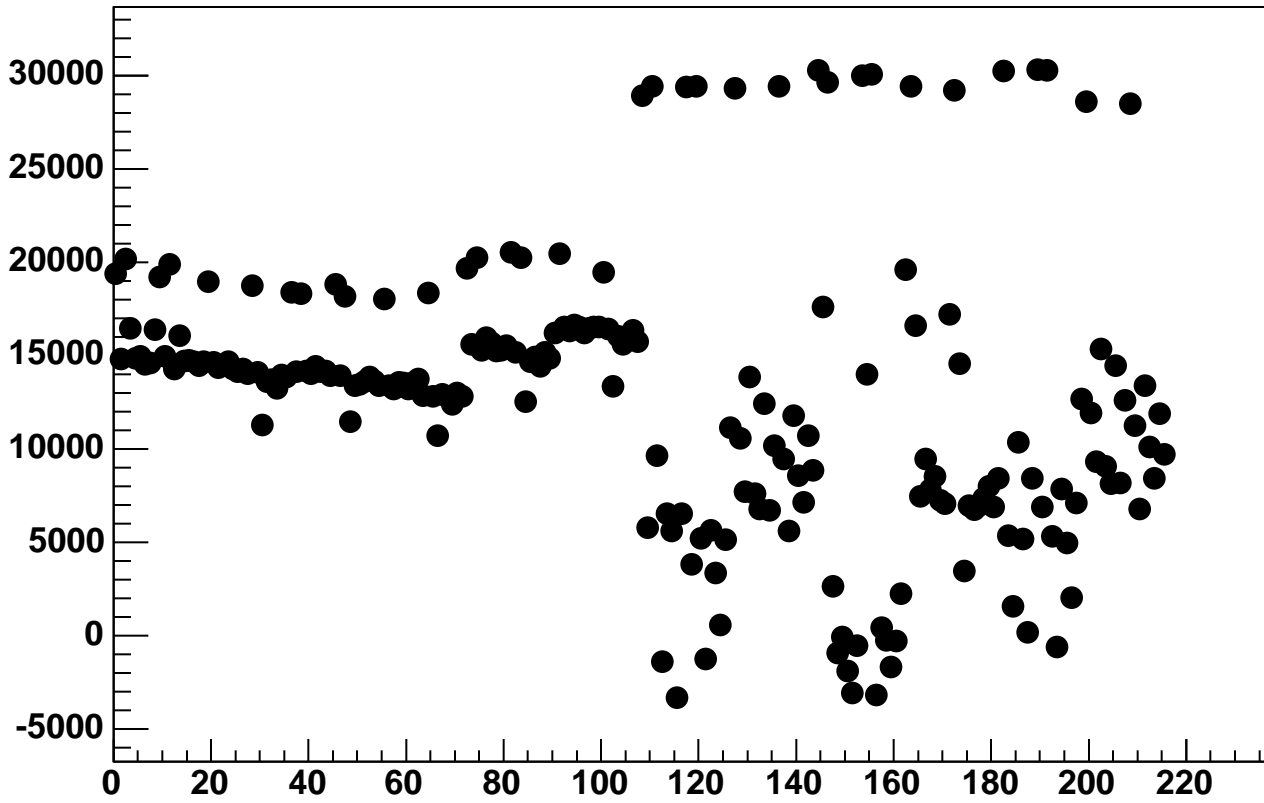


Enable 0, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan

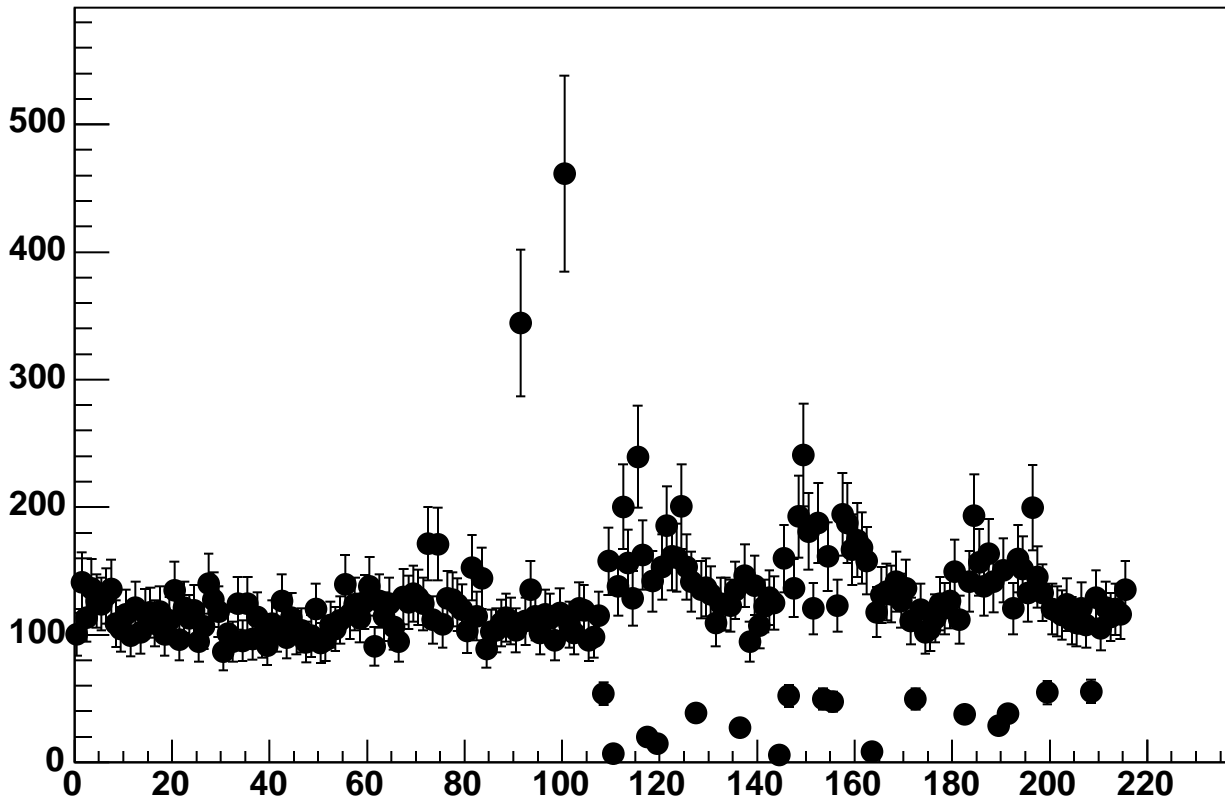




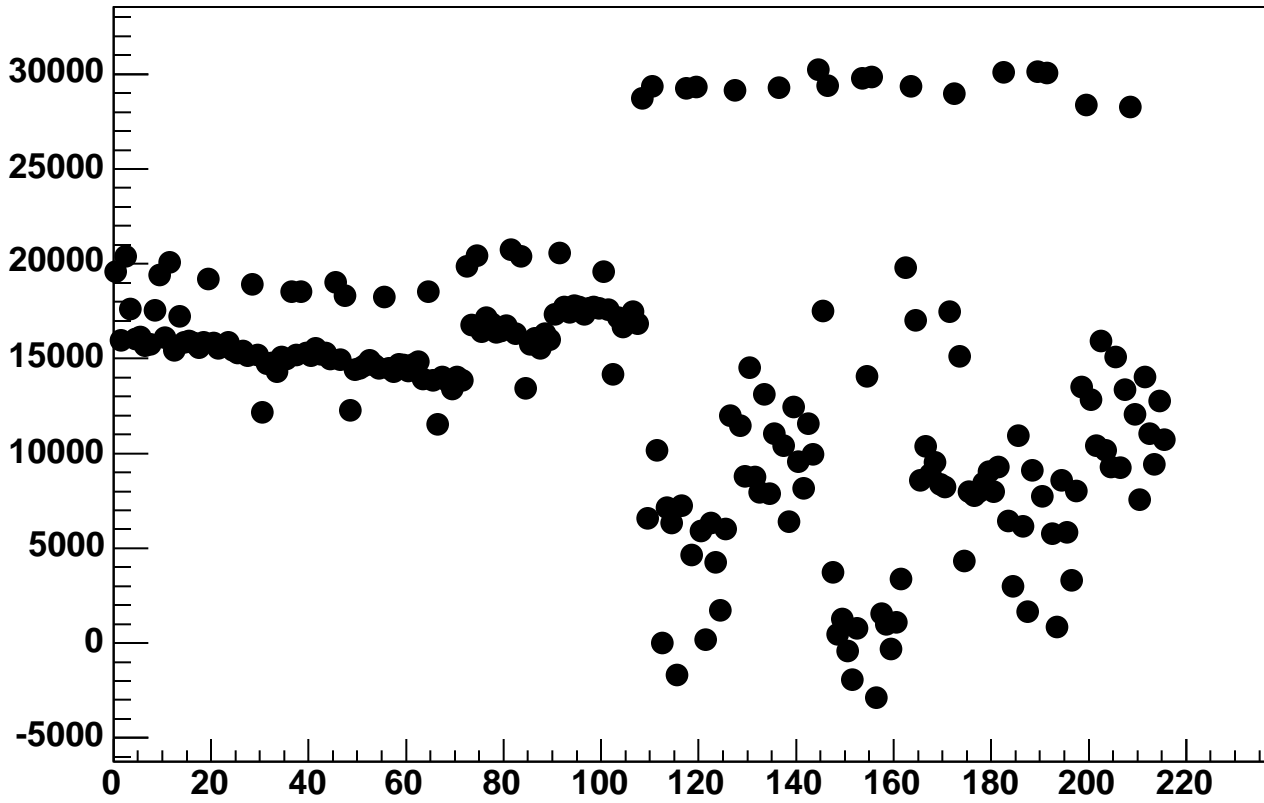
Enable 0, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



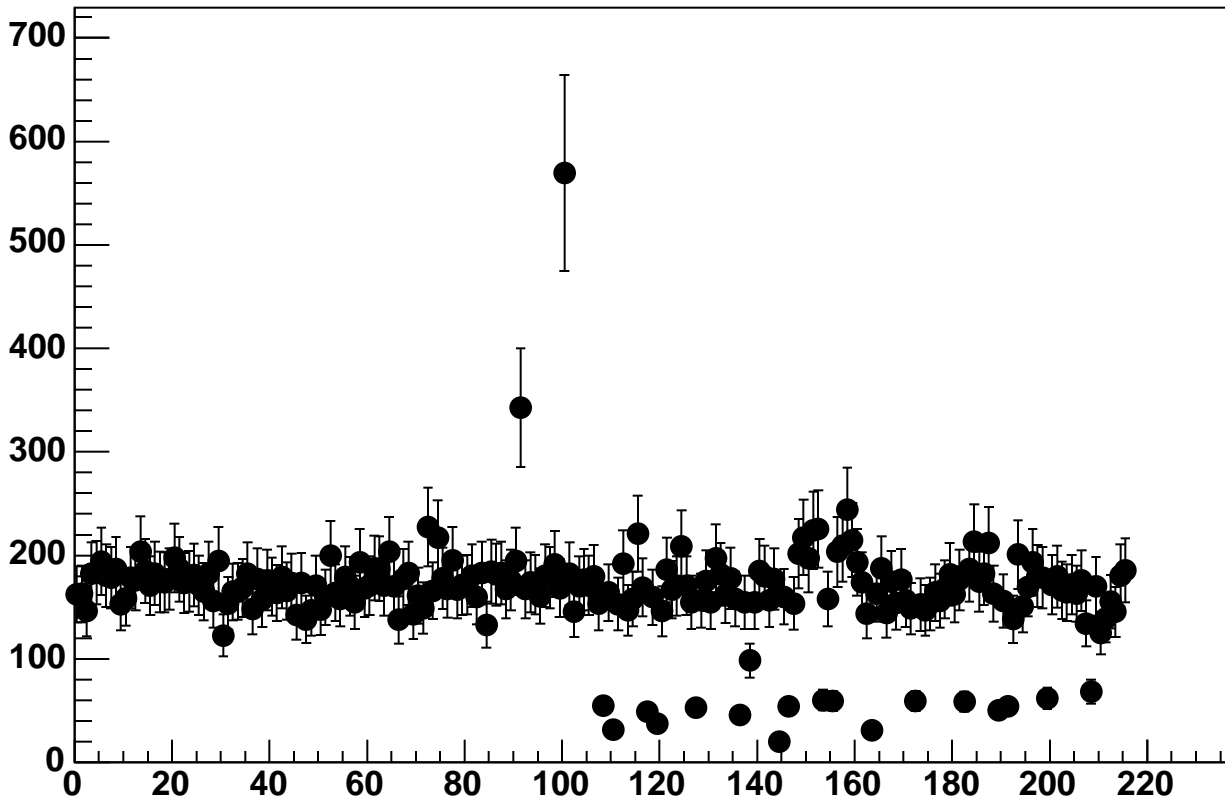
Enable 0, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



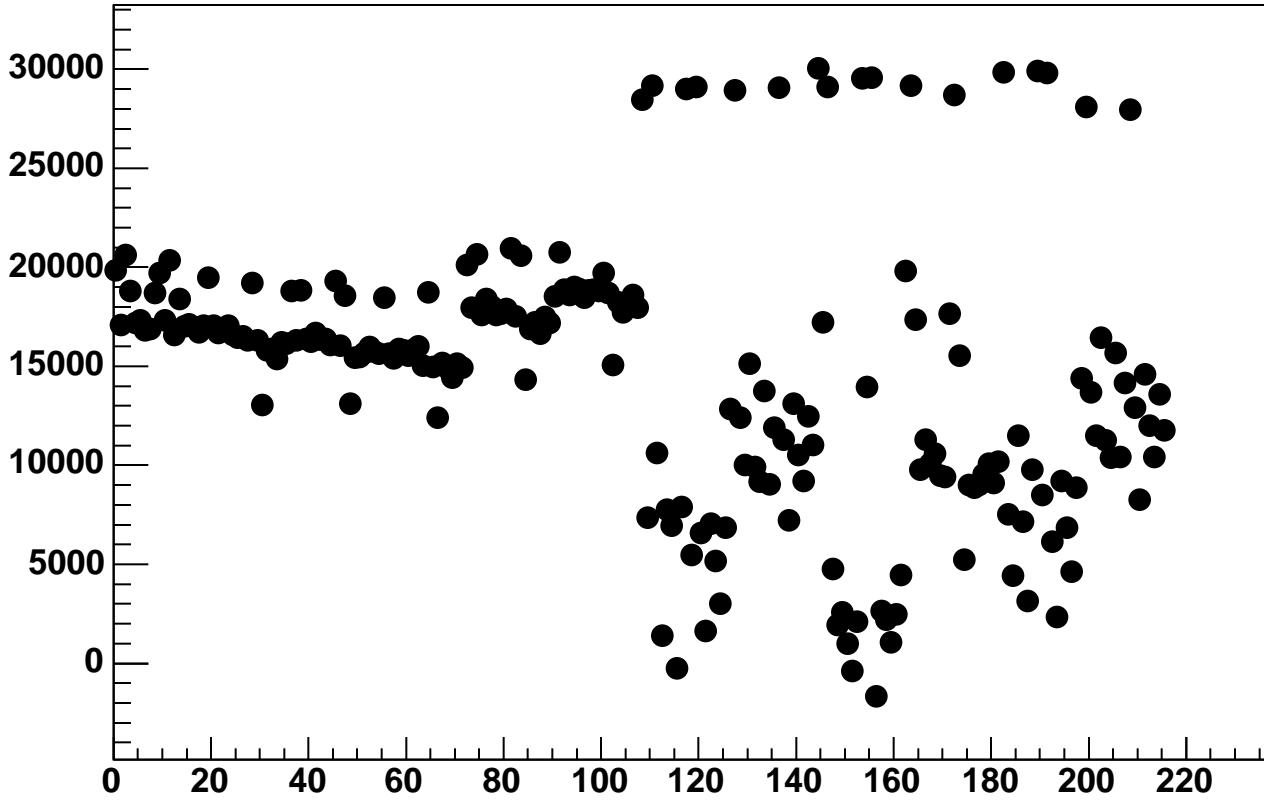
Enable 0, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan



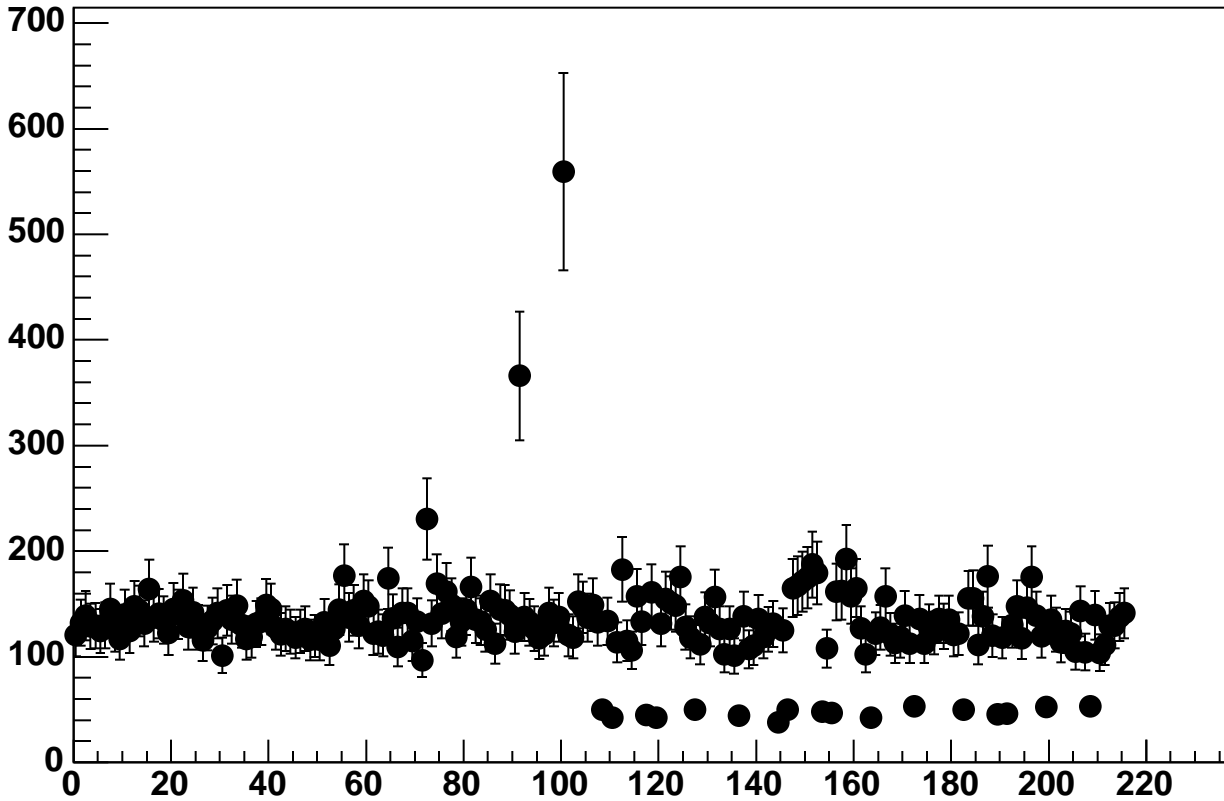
Enable 0, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan



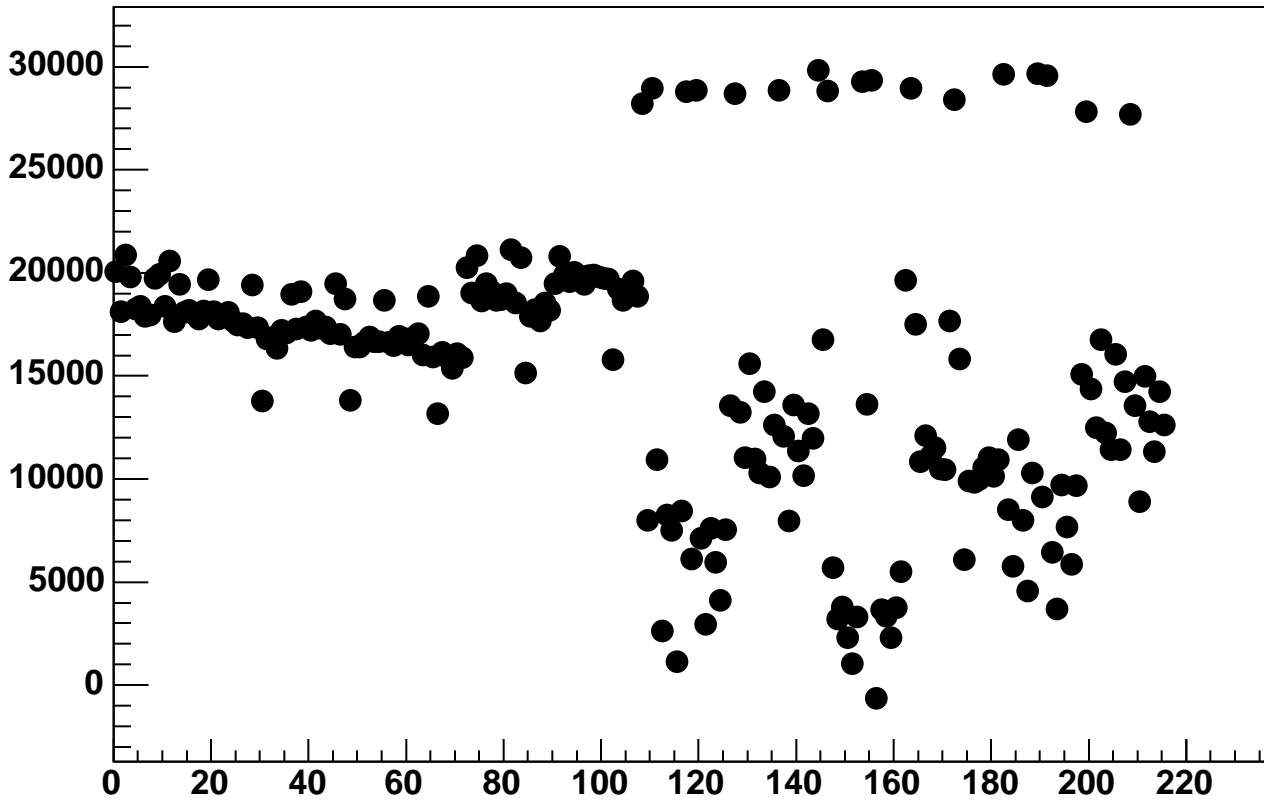
Enable 0, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



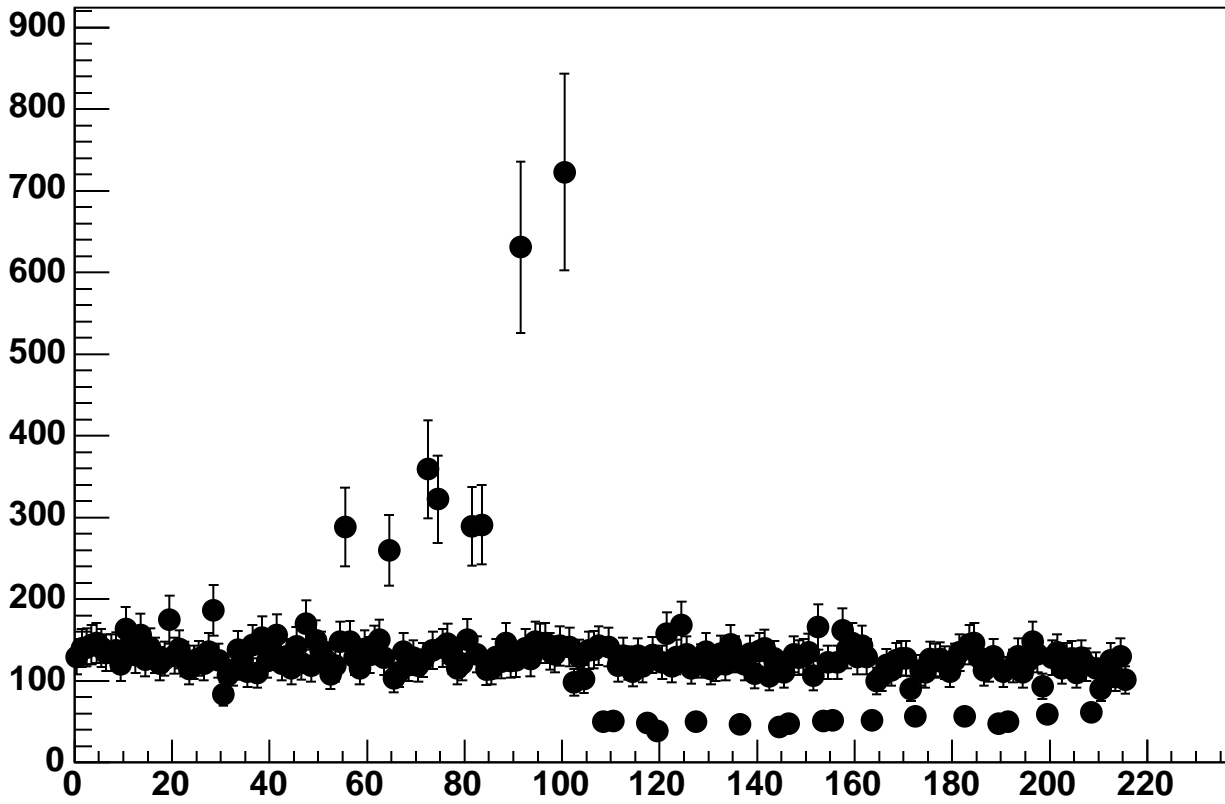
Enable 0, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



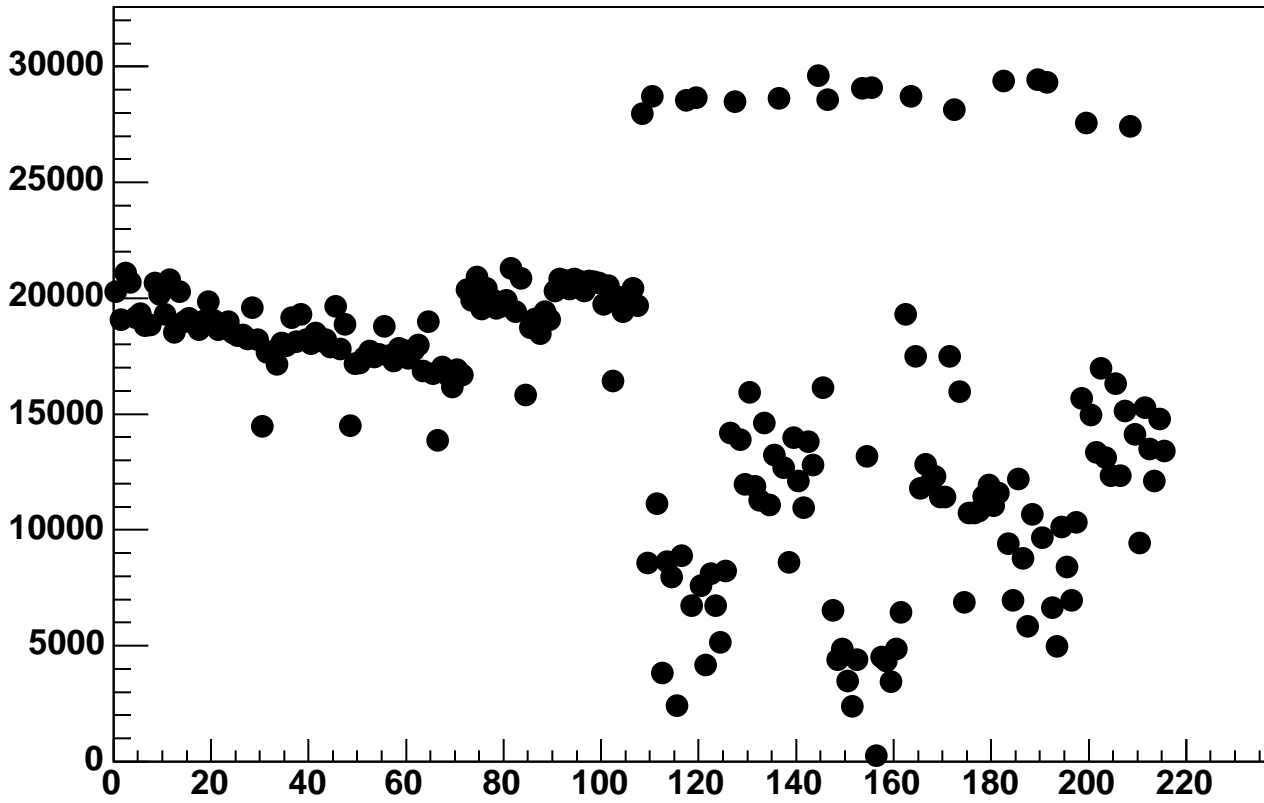
Enable 0, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan



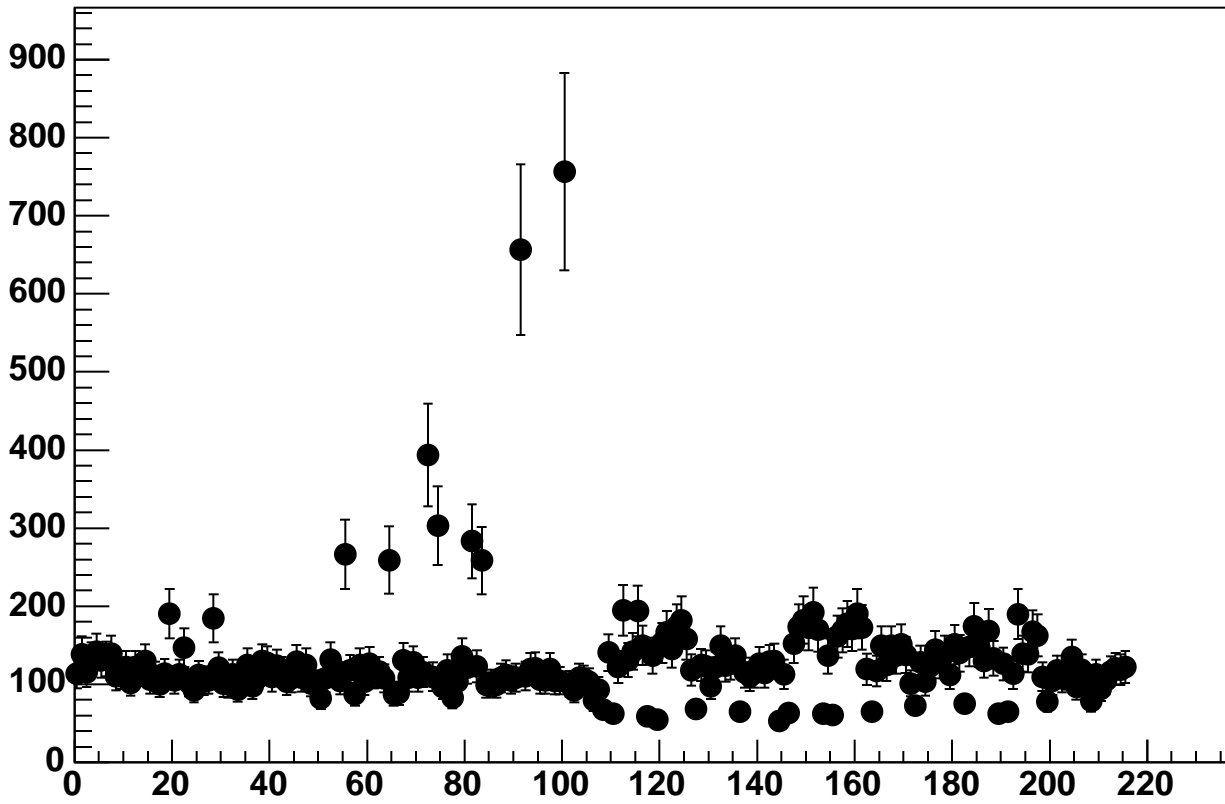
Enable 0, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan



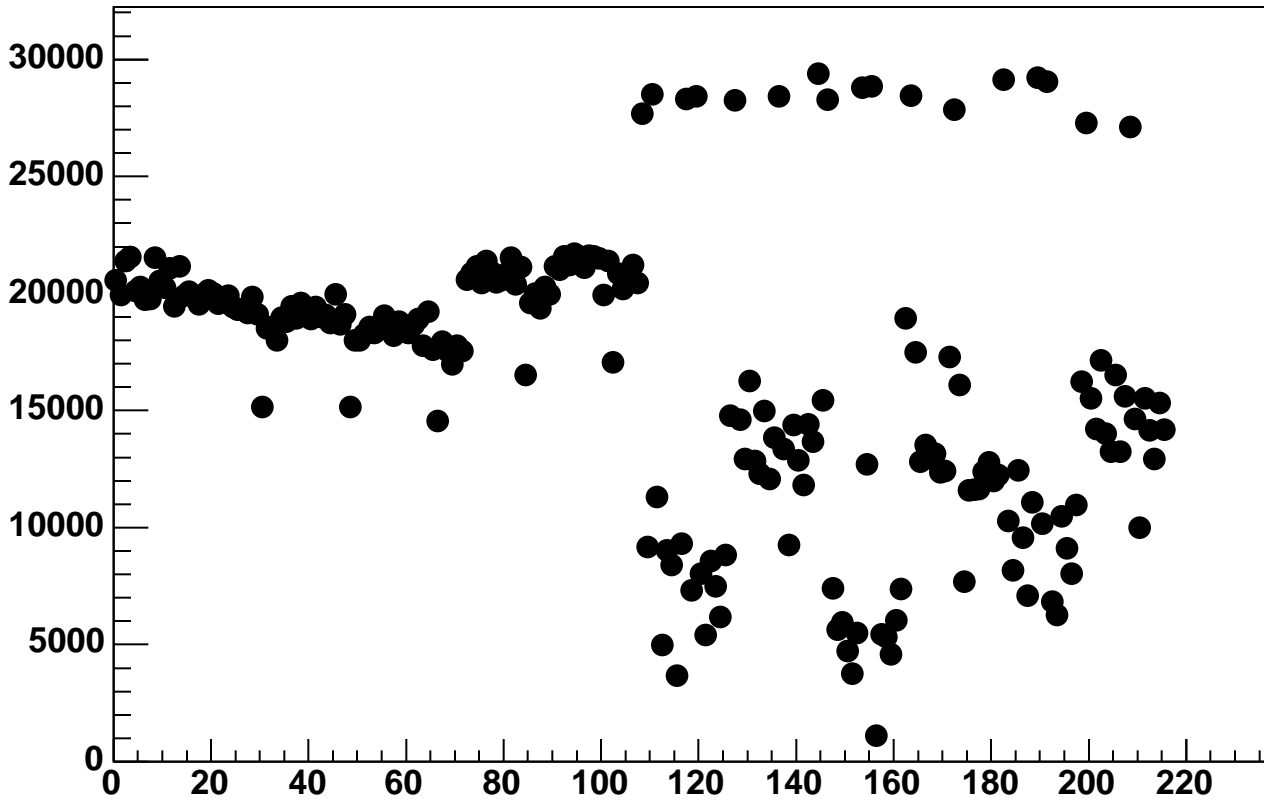
Enable 0, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



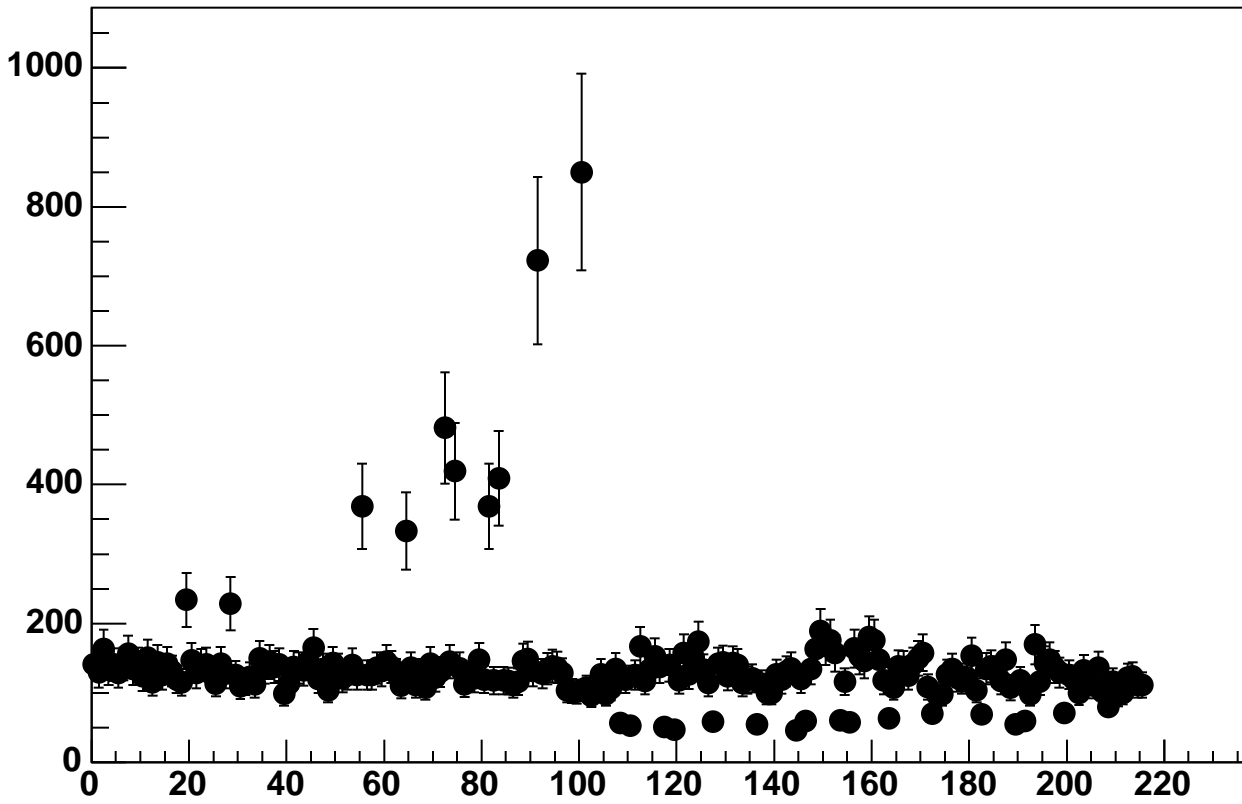
Enable 0, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



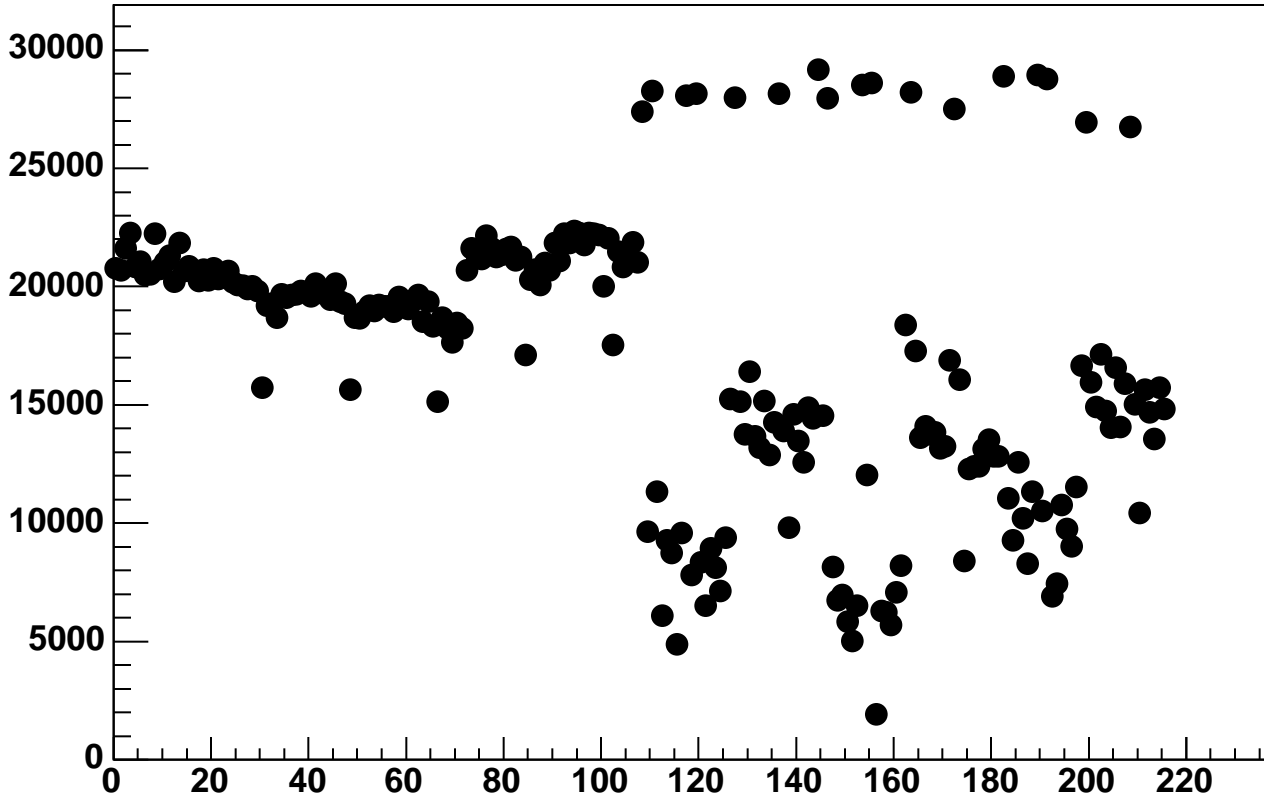
Enable 0, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan



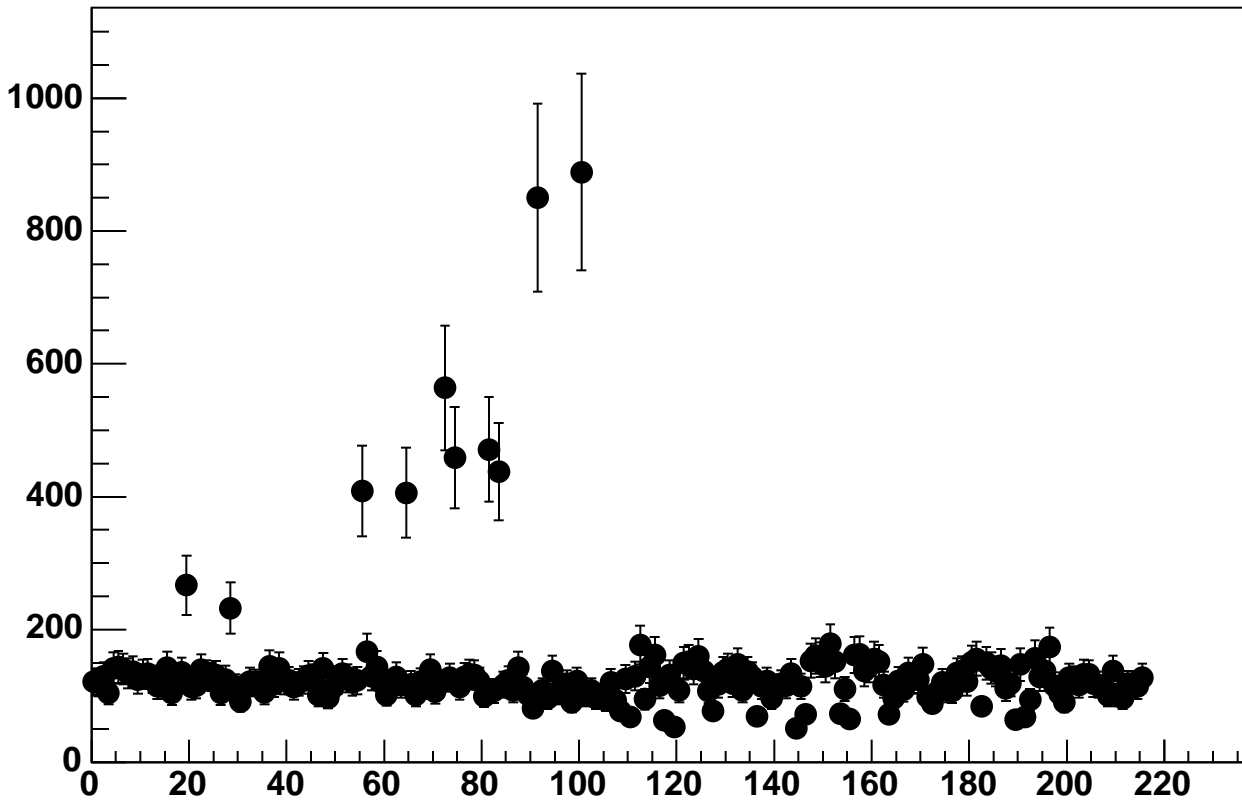
Enable 0, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan



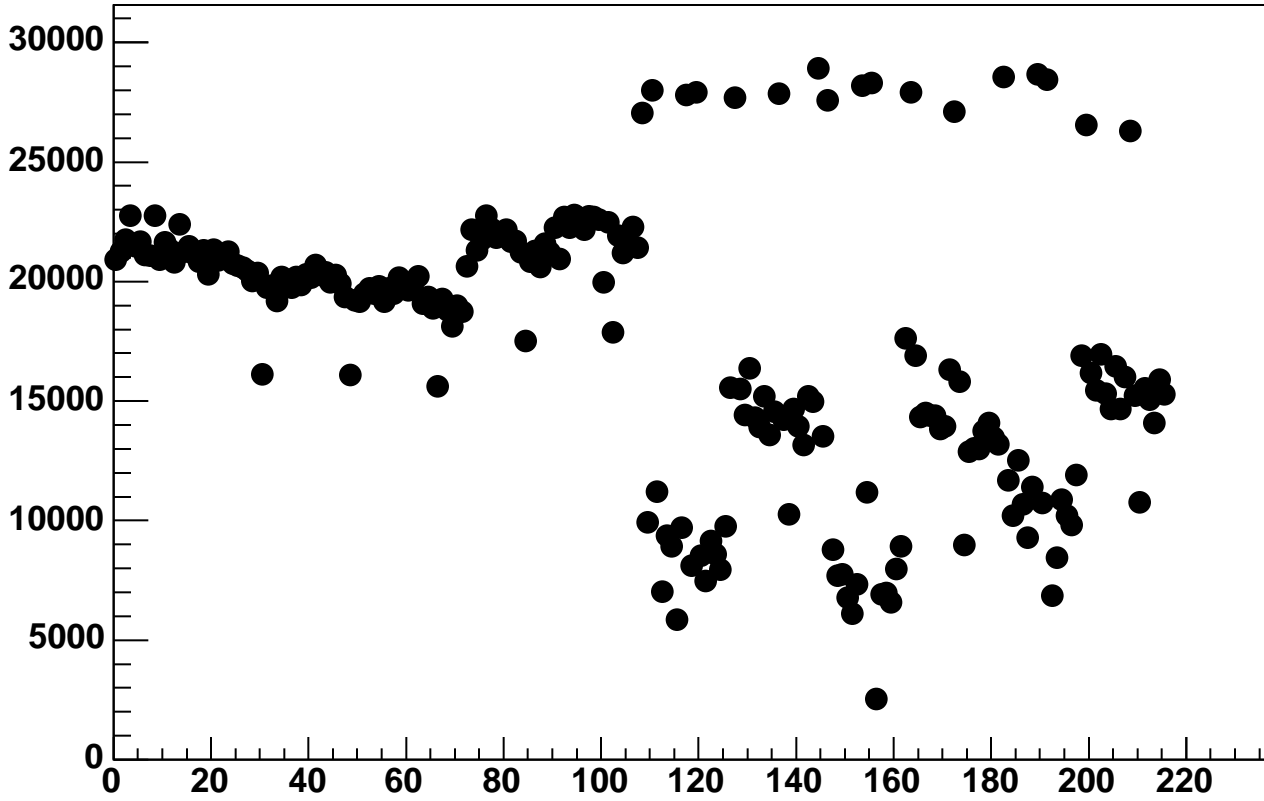
Enable 0, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



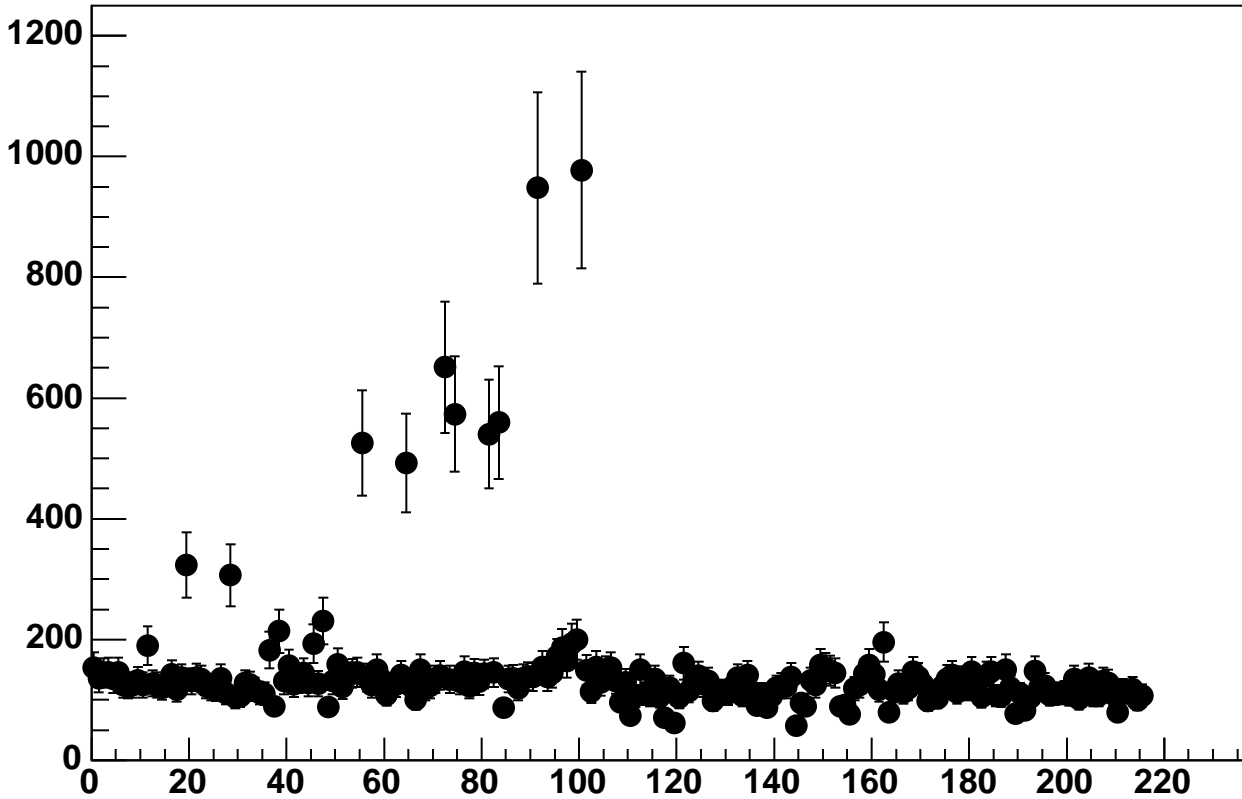
Enable 0, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan

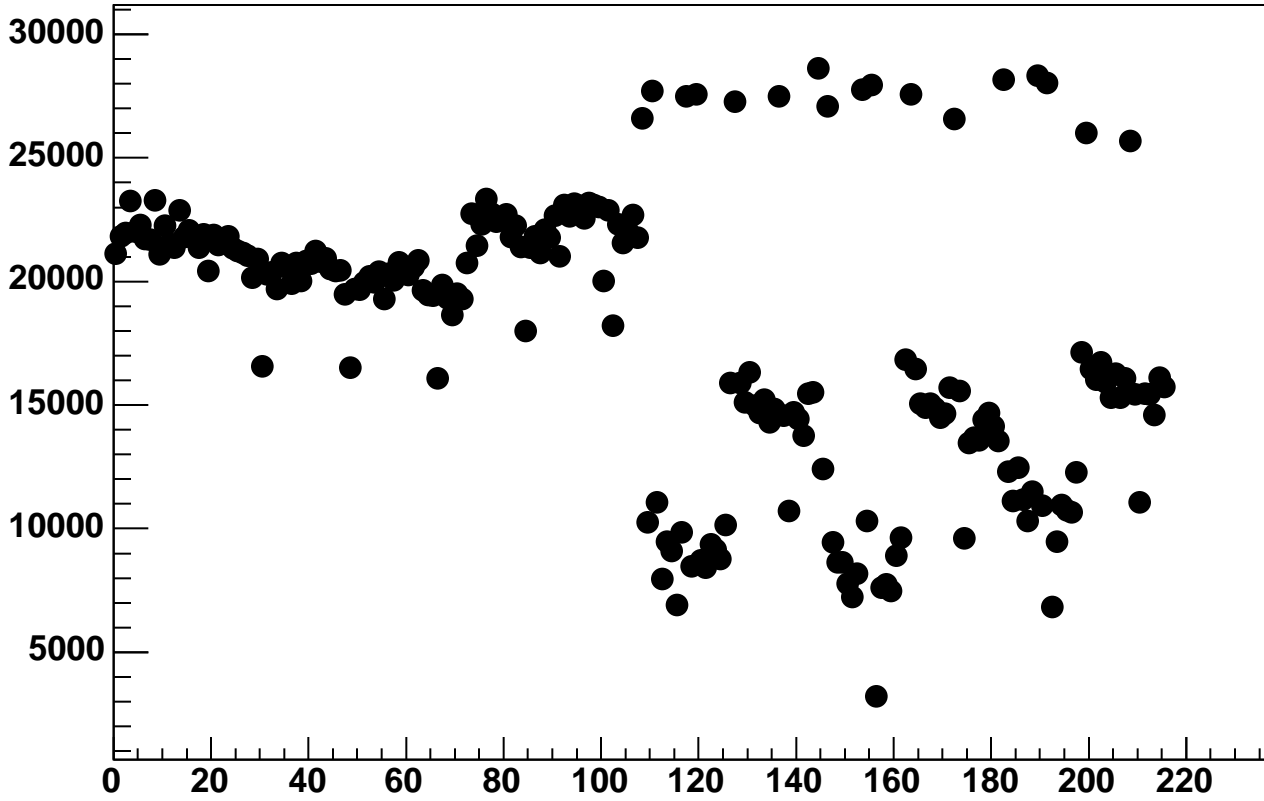


Enable 0, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan

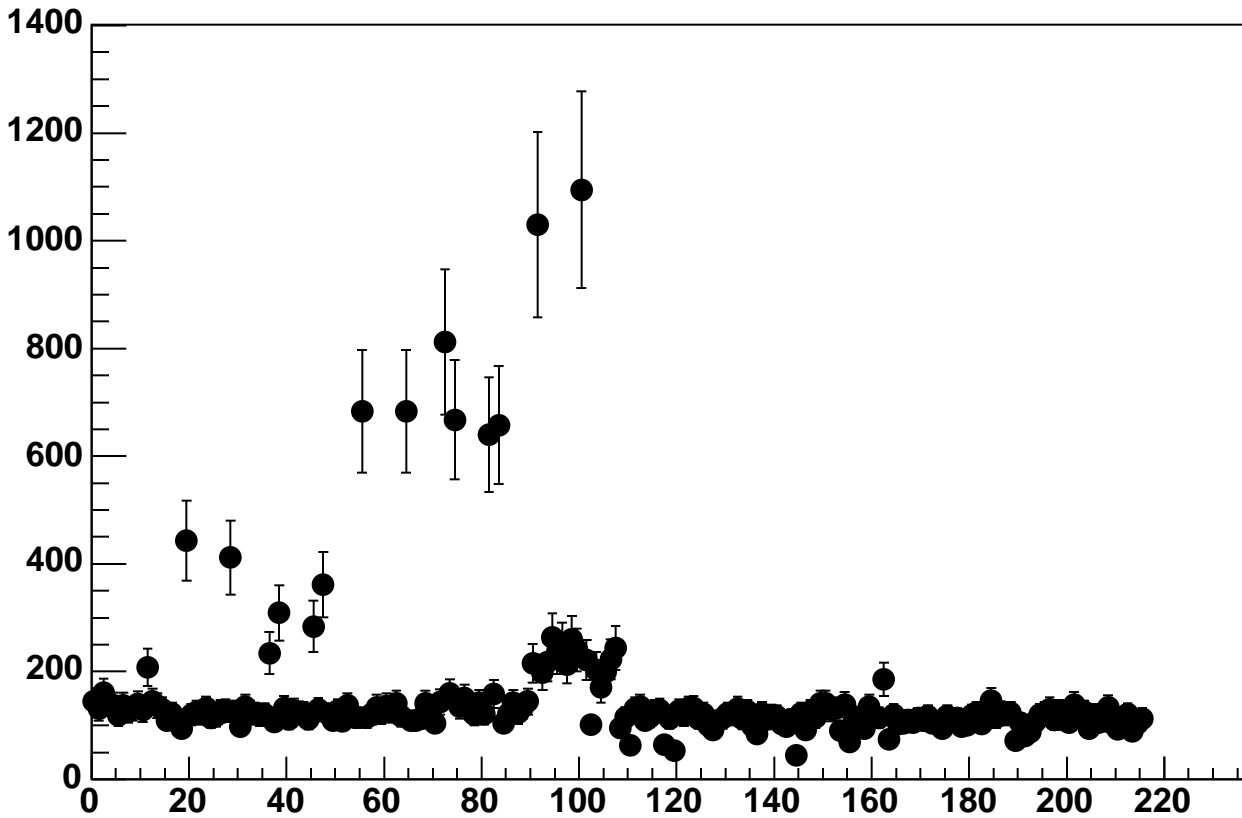




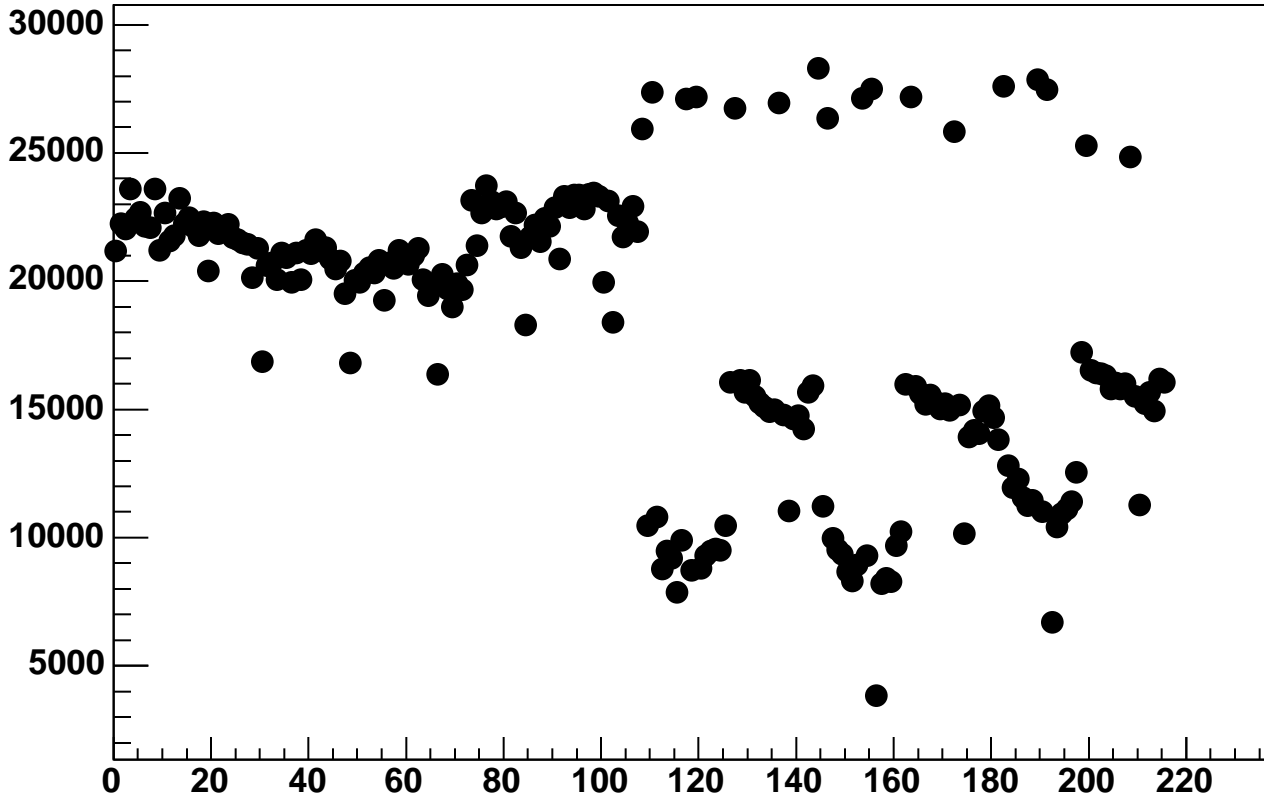
Enable 0, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



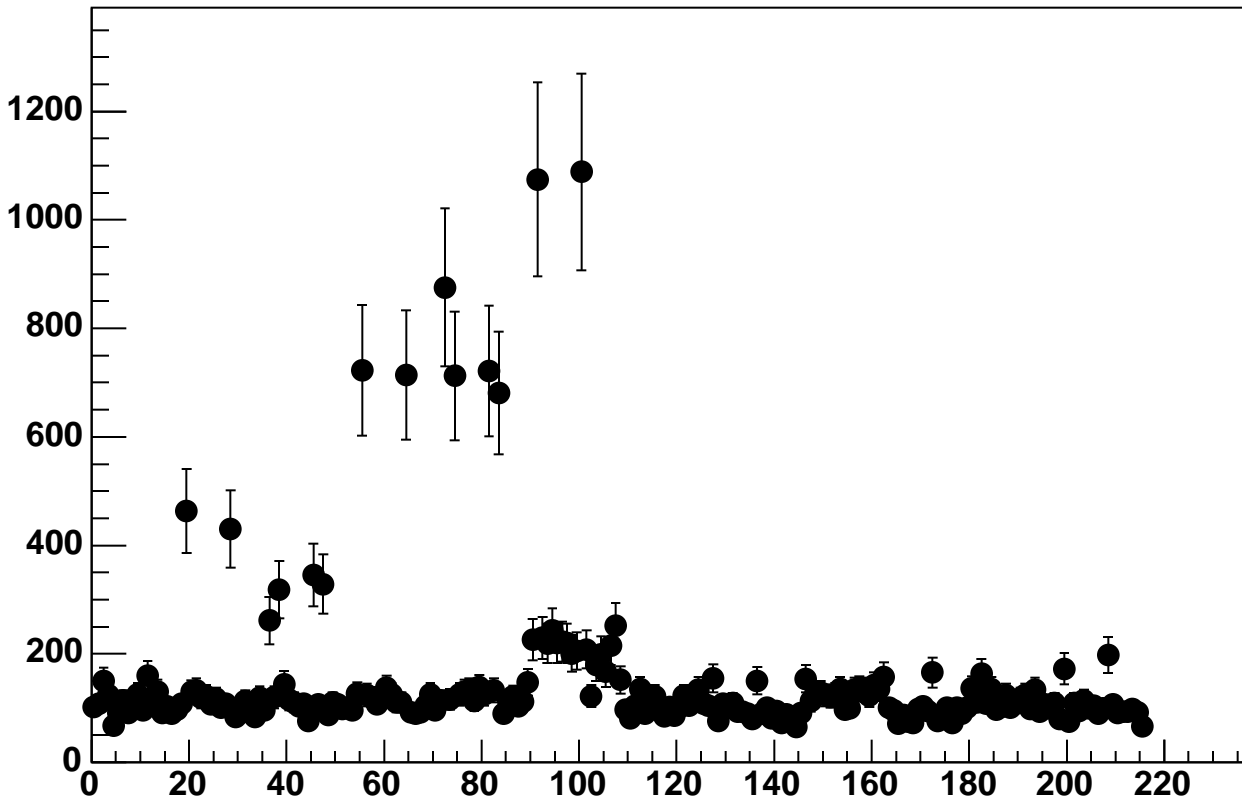
Enable 0, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



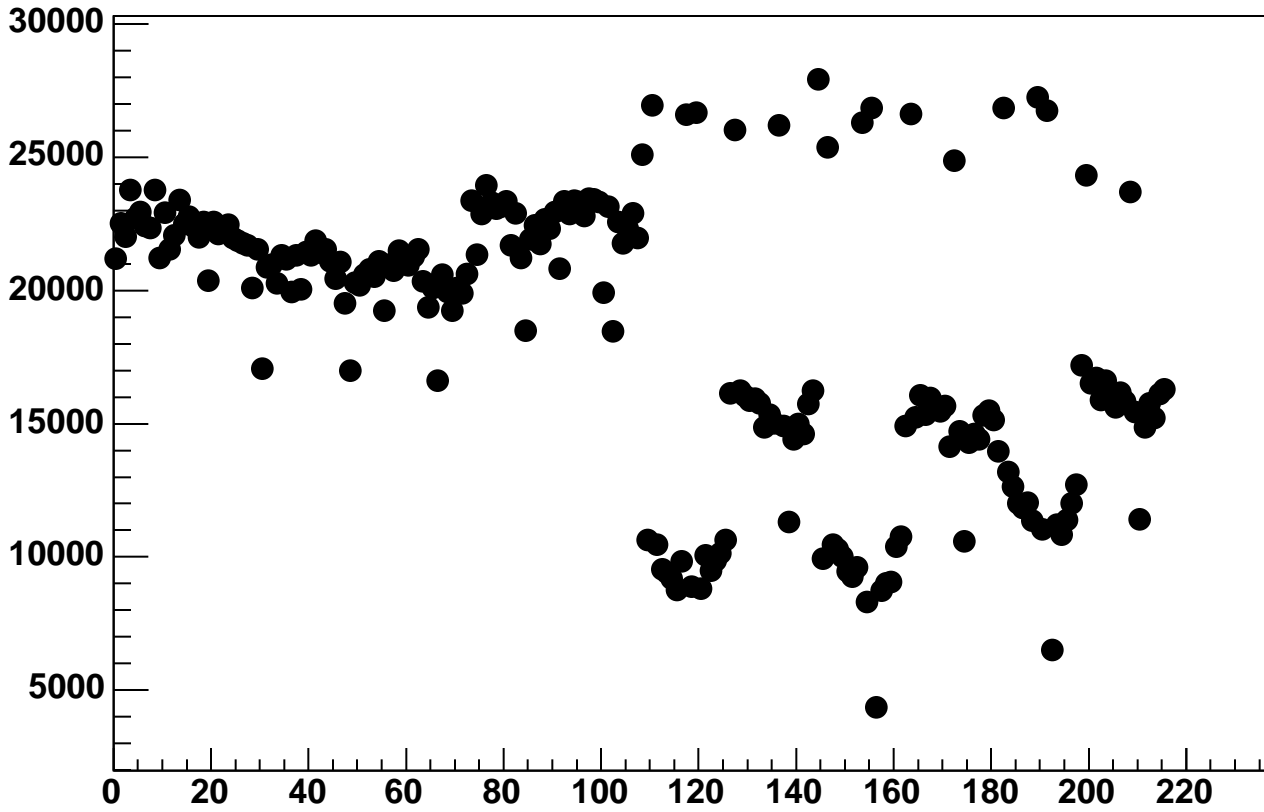
Enable 0, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan



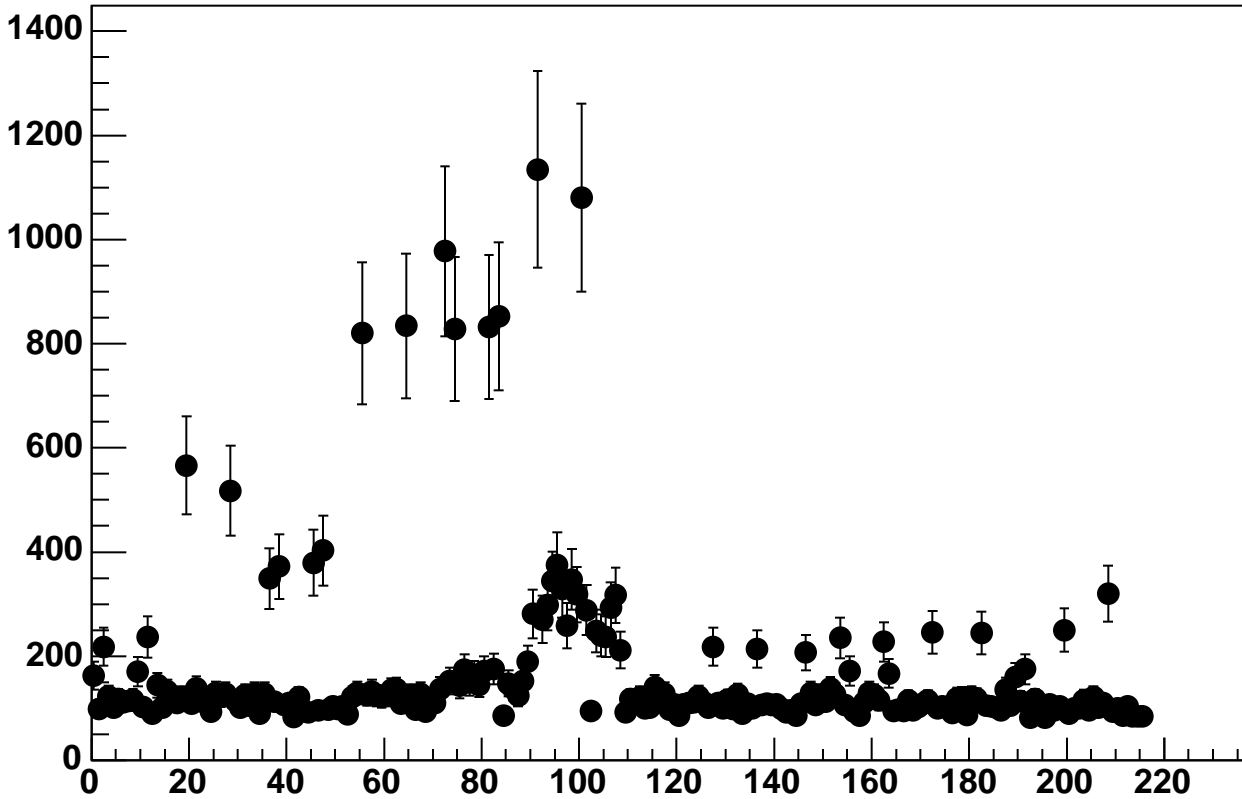
Enable 0, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan



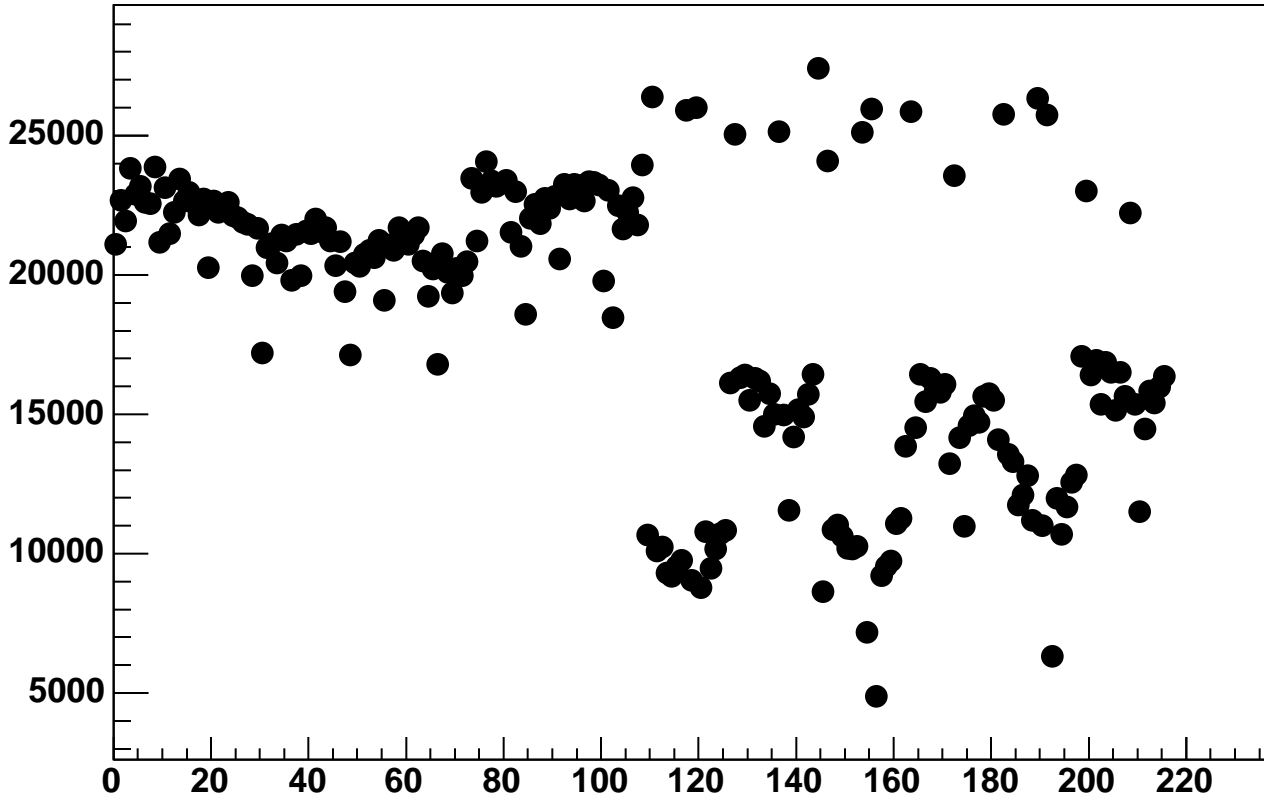
Enable 0, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



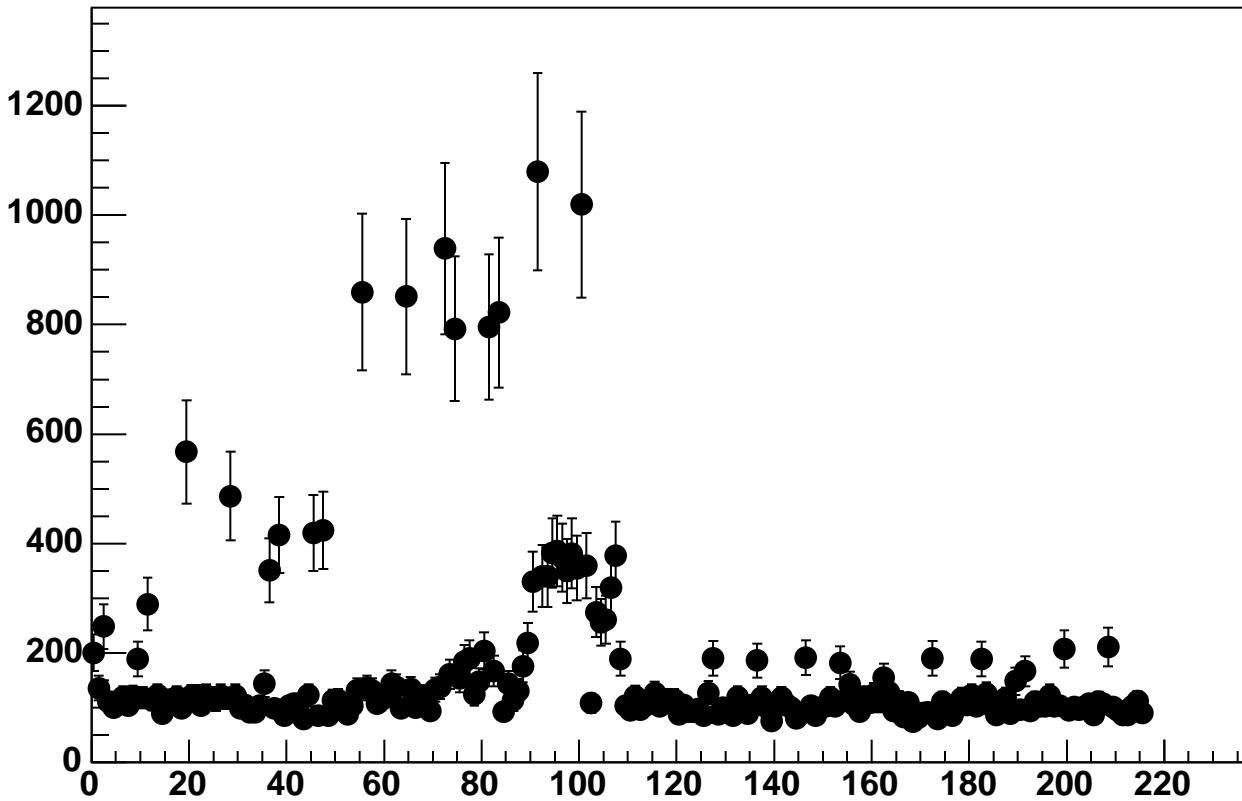
Enable 0, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



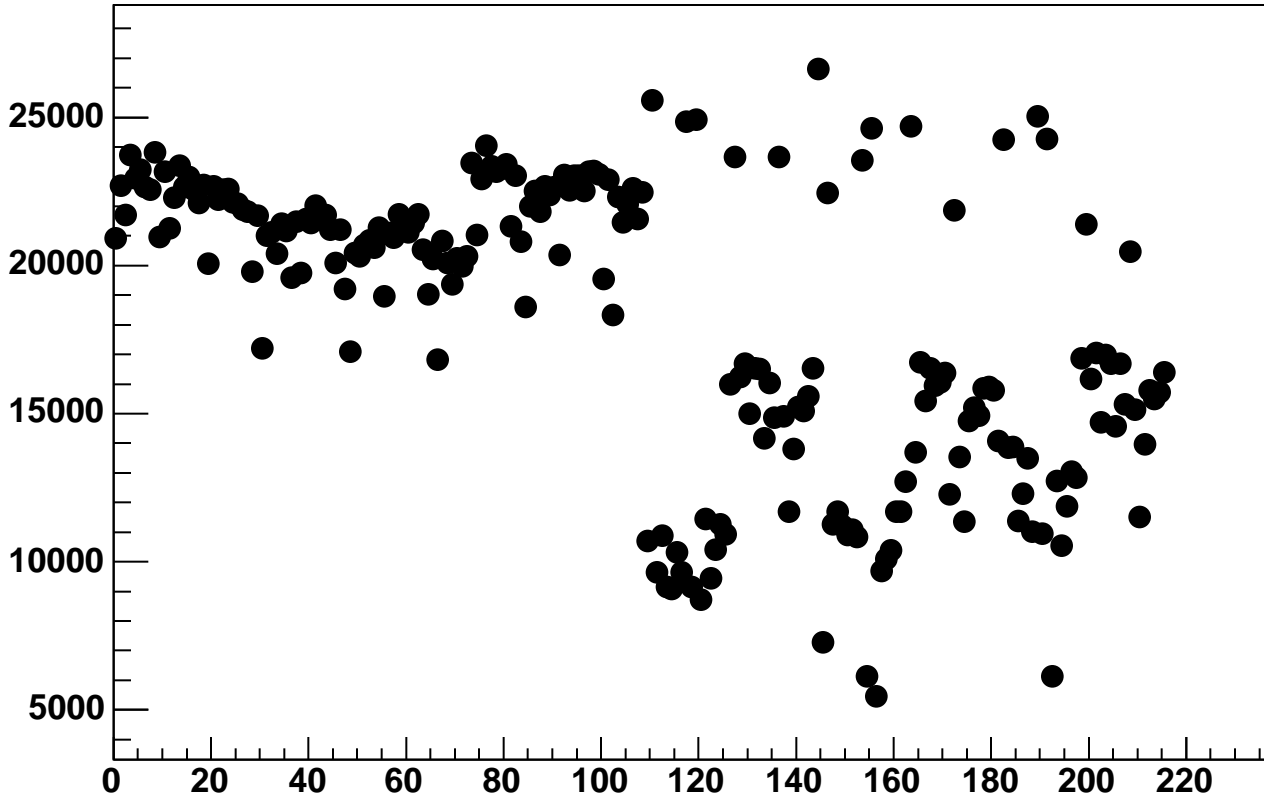
Enable 0, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan



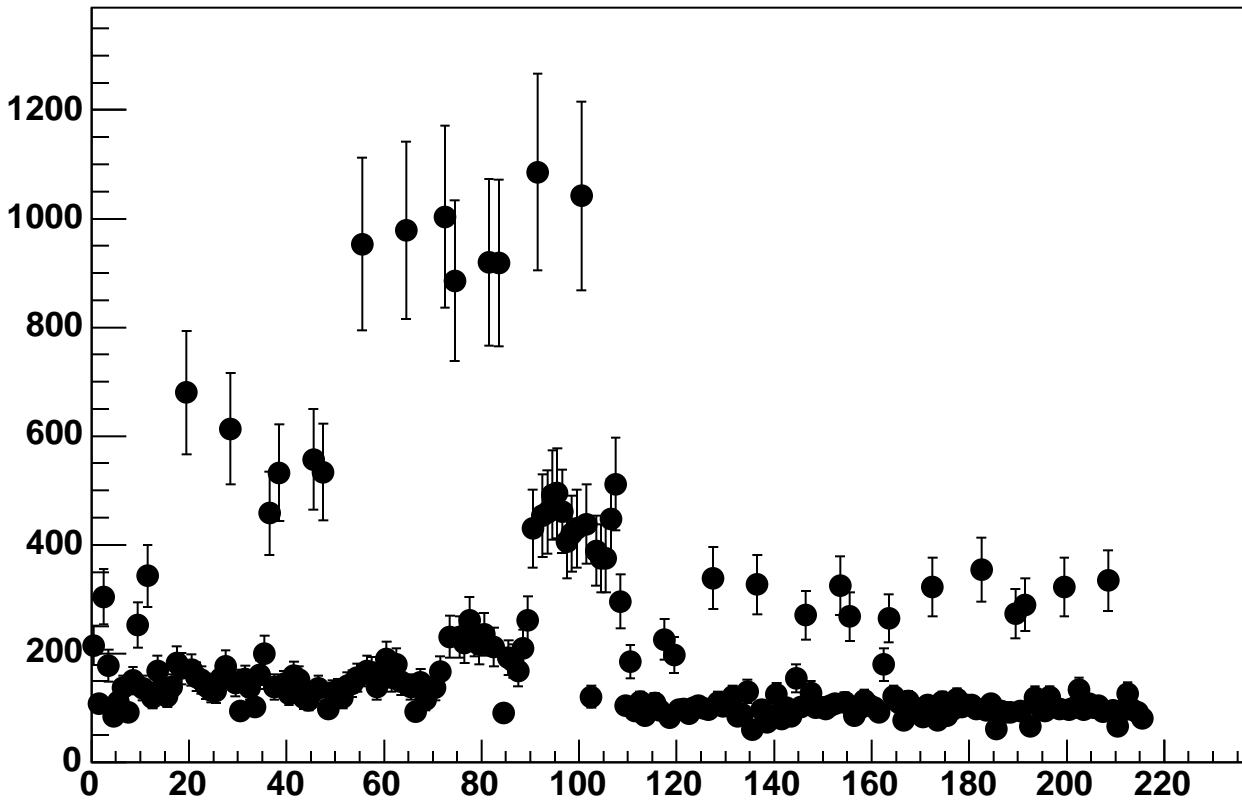
Enable 0, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan



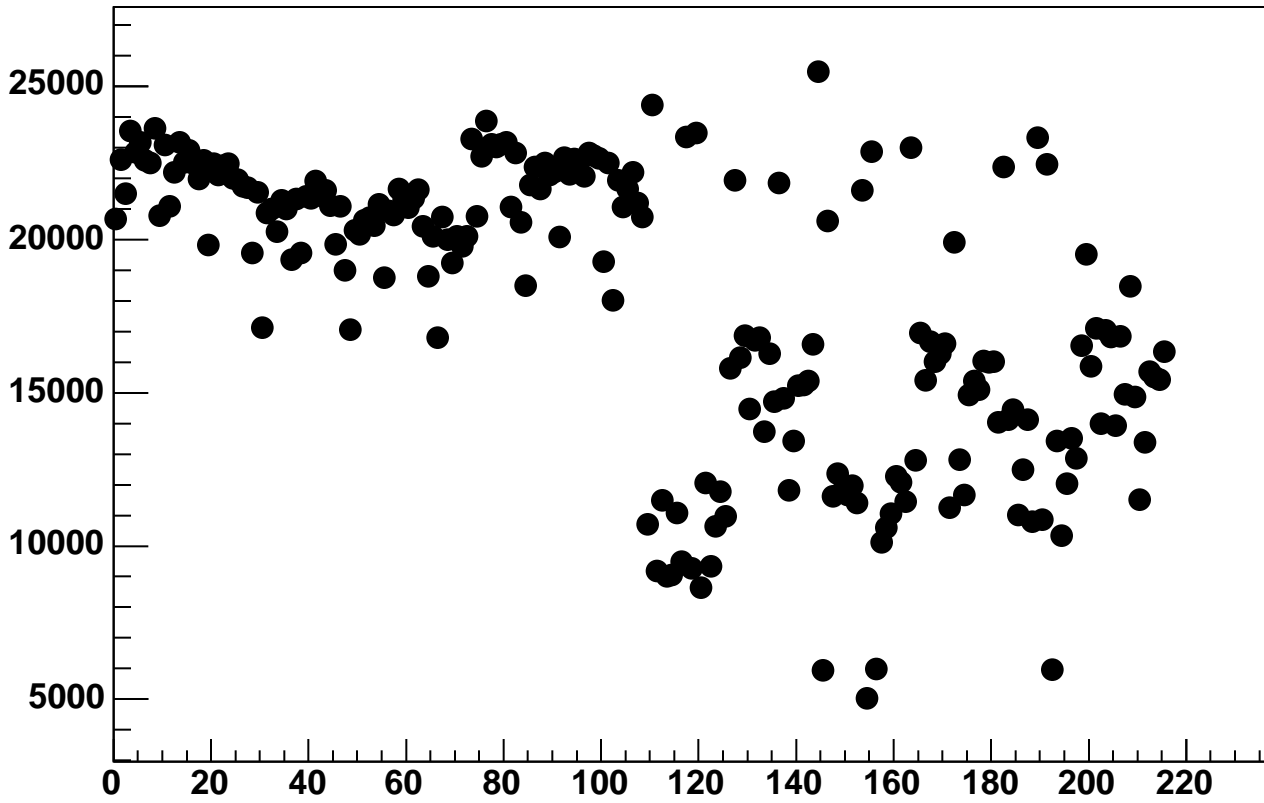
Enable 0, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



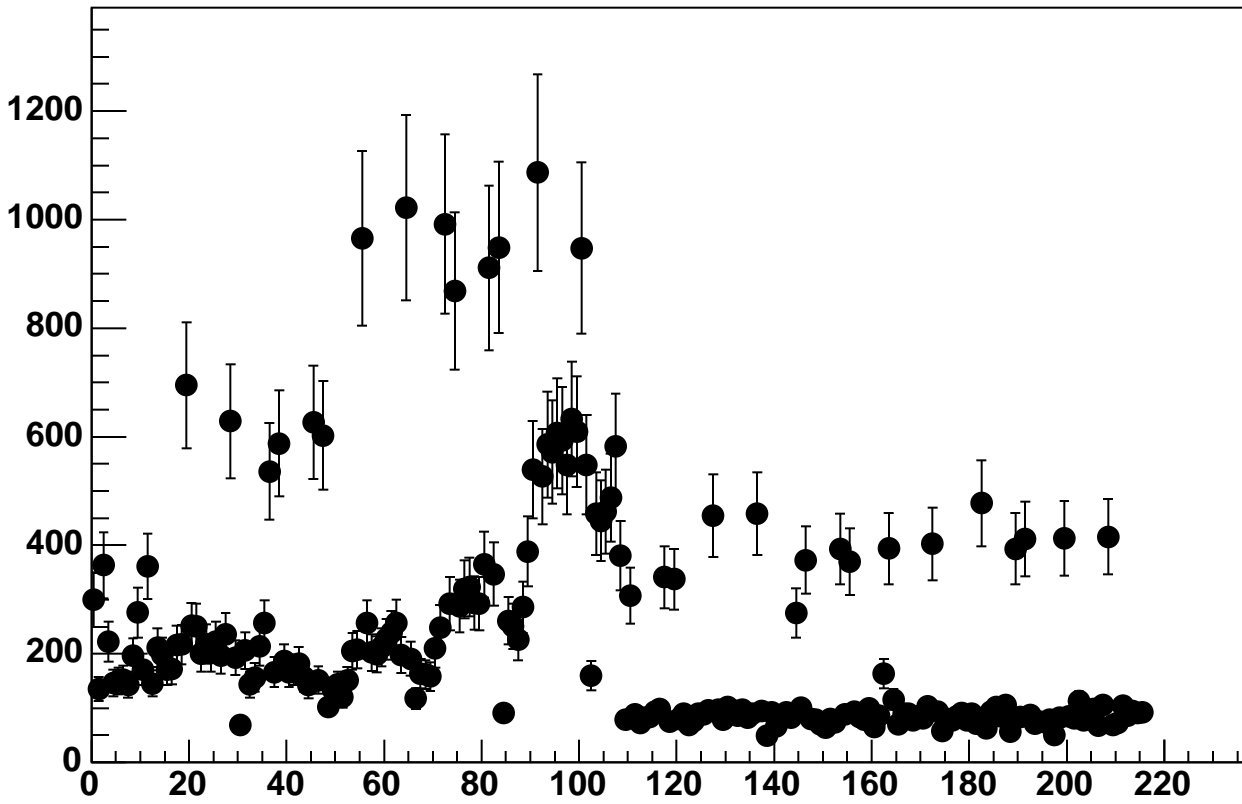
Enable 0, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



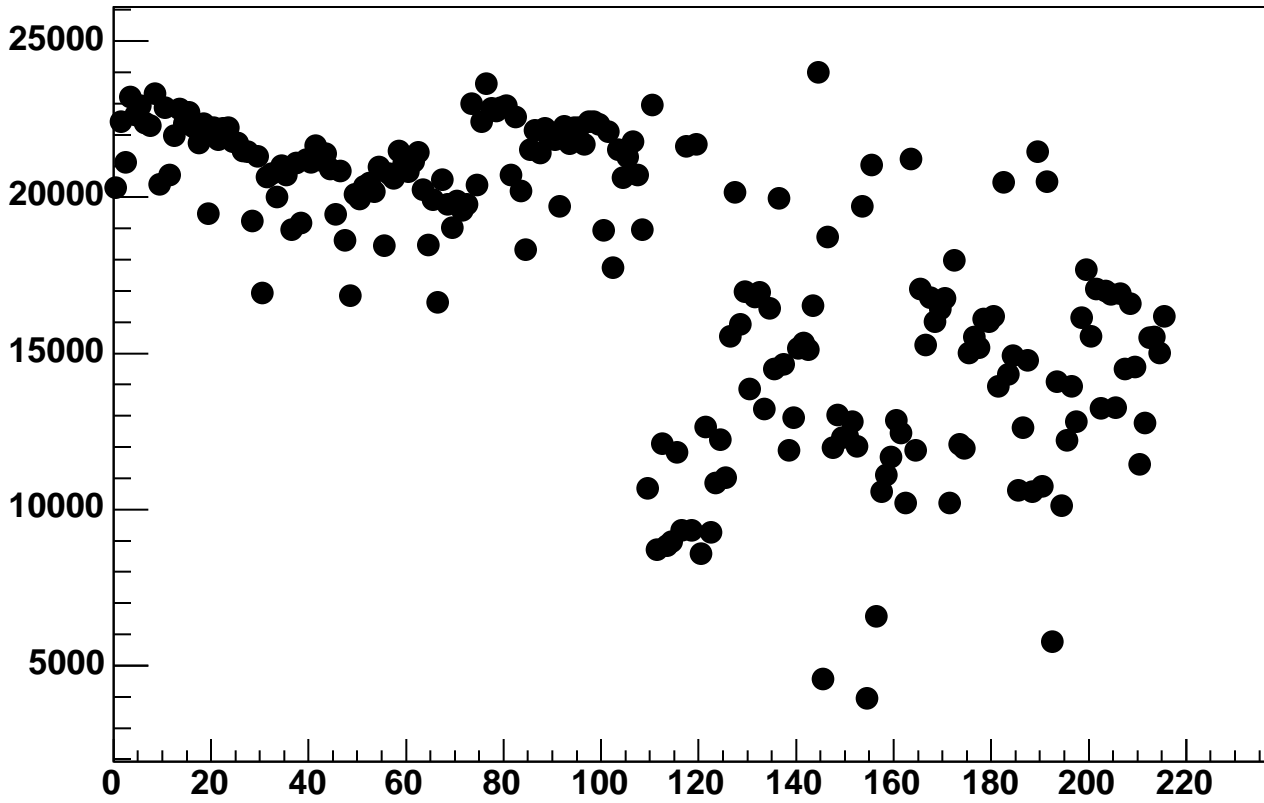
Enable 0, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan



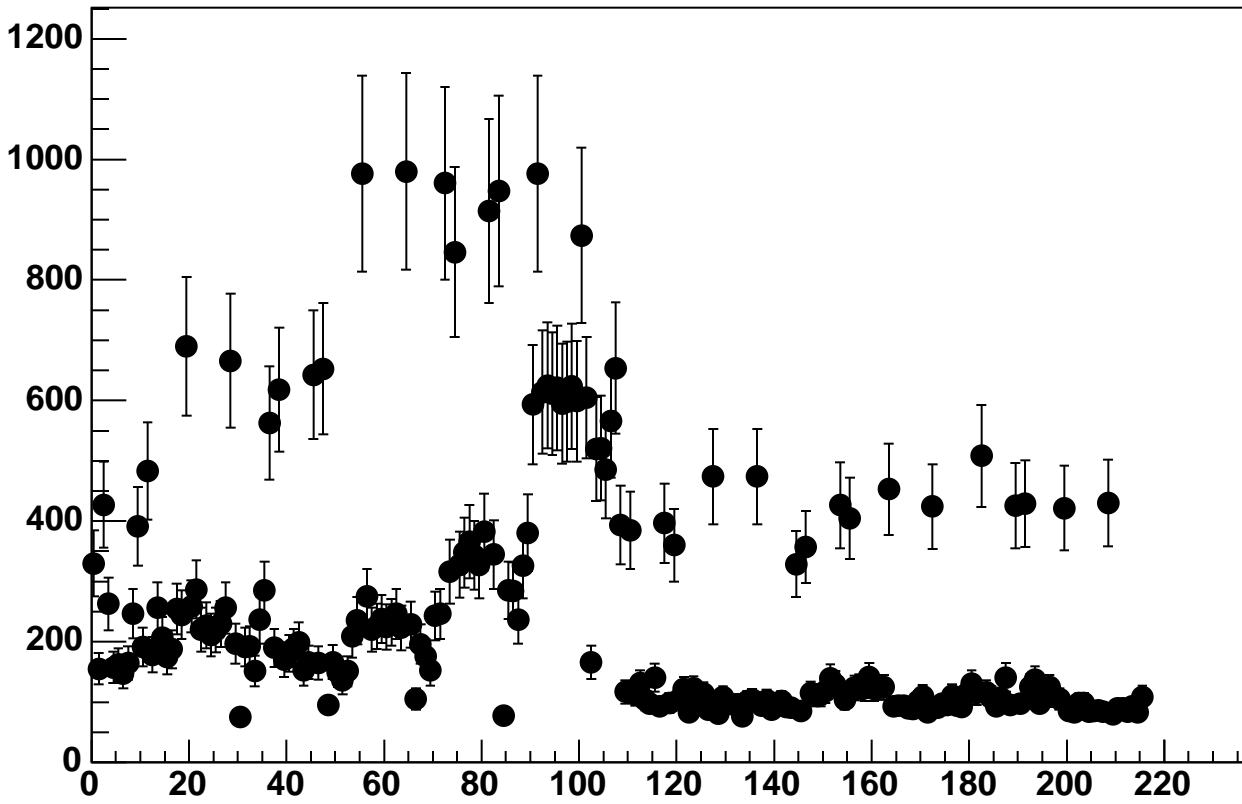
Enable 0, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan



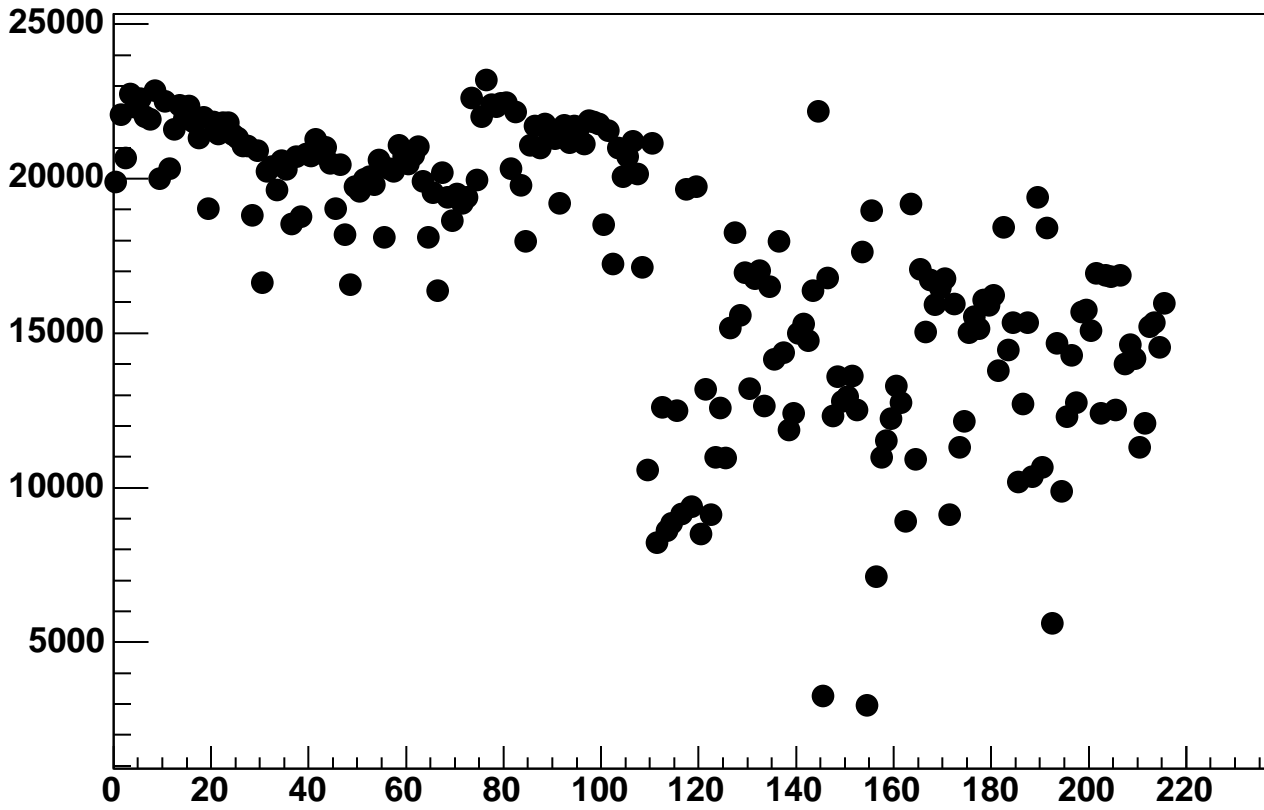
Enable 0, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



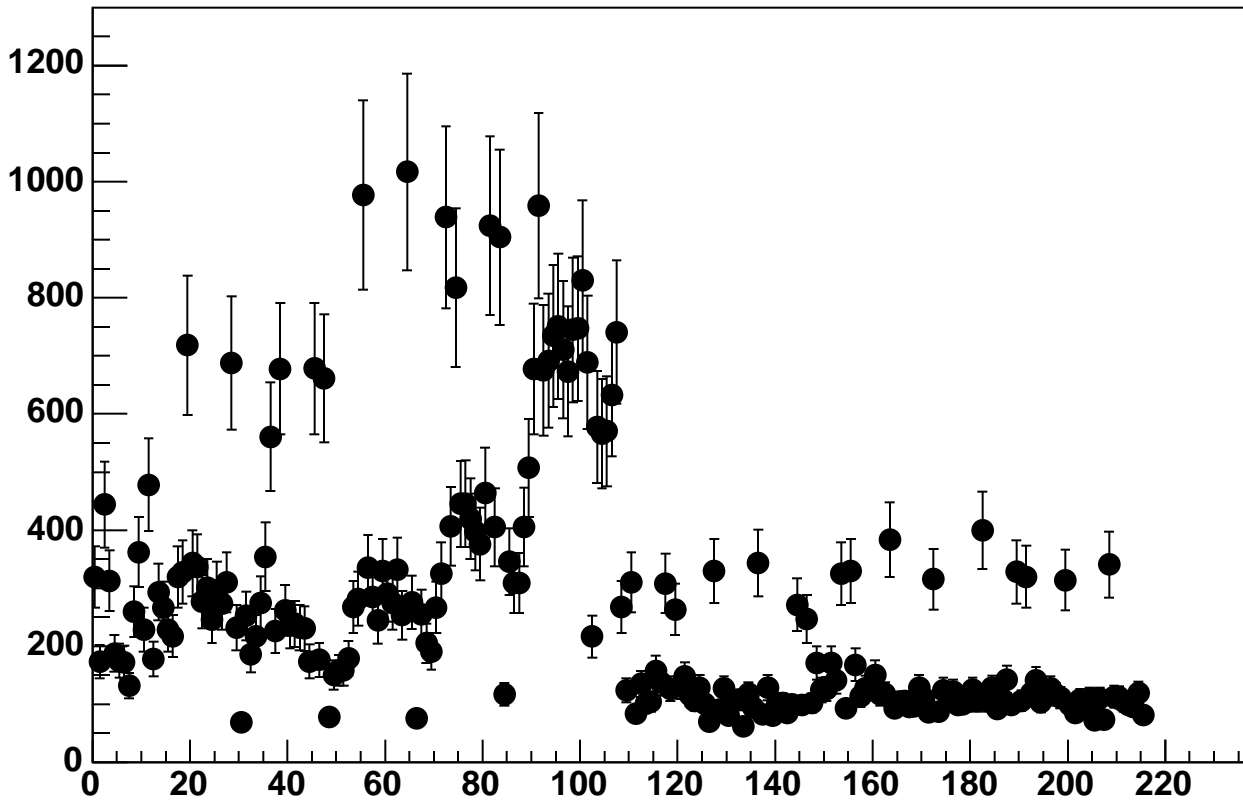
Enable 0, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan

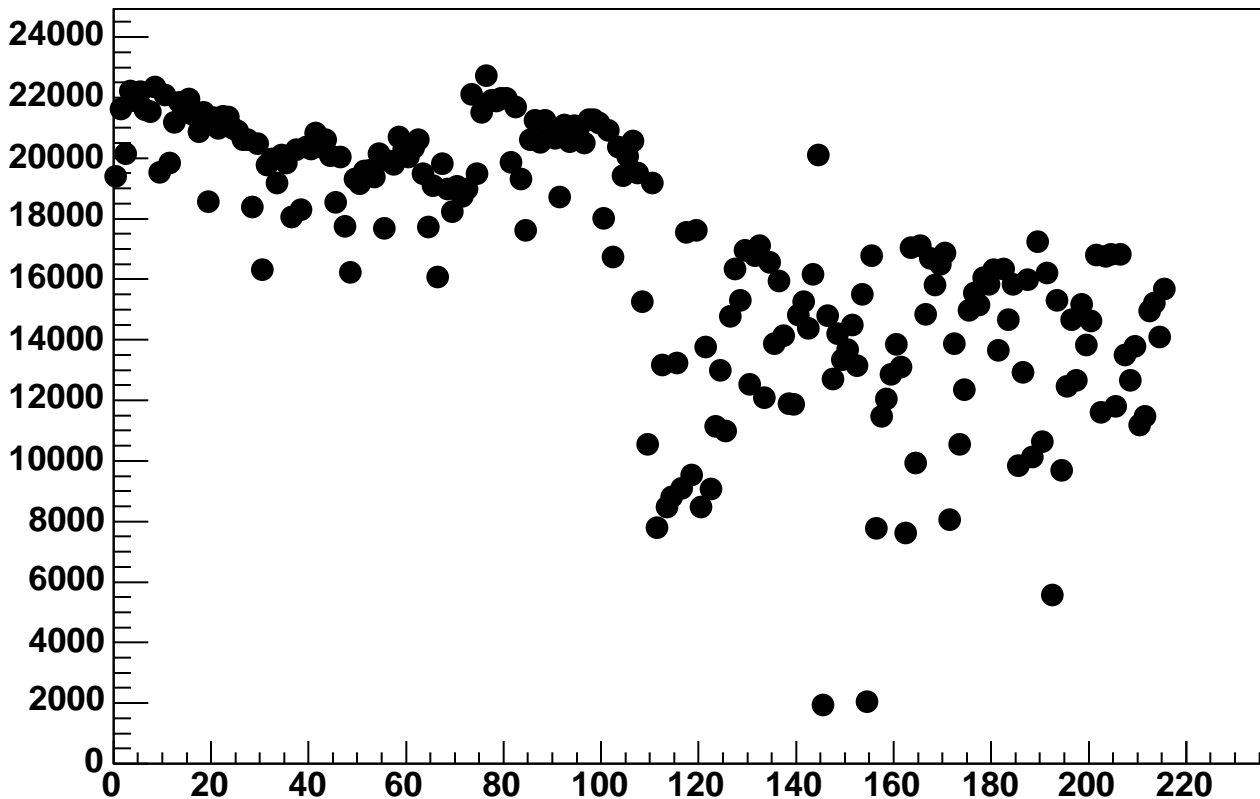


Enable 0, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan

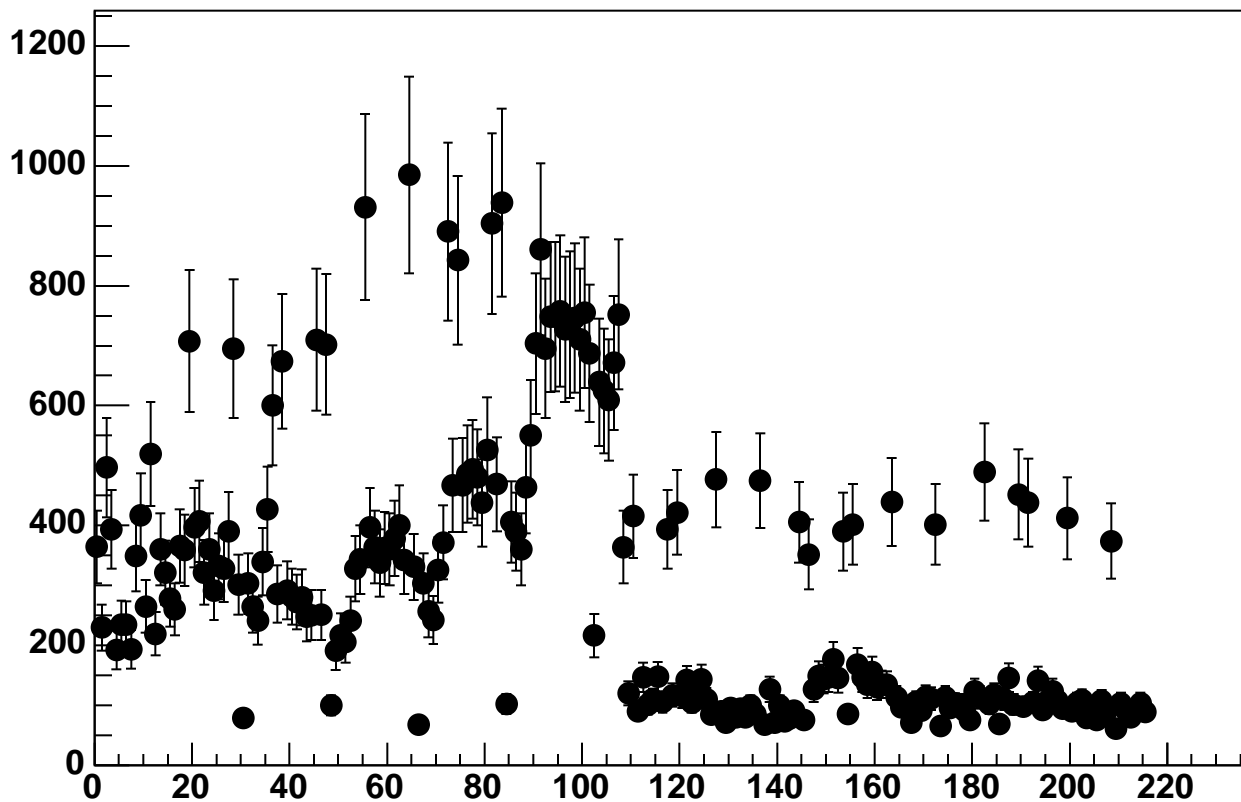




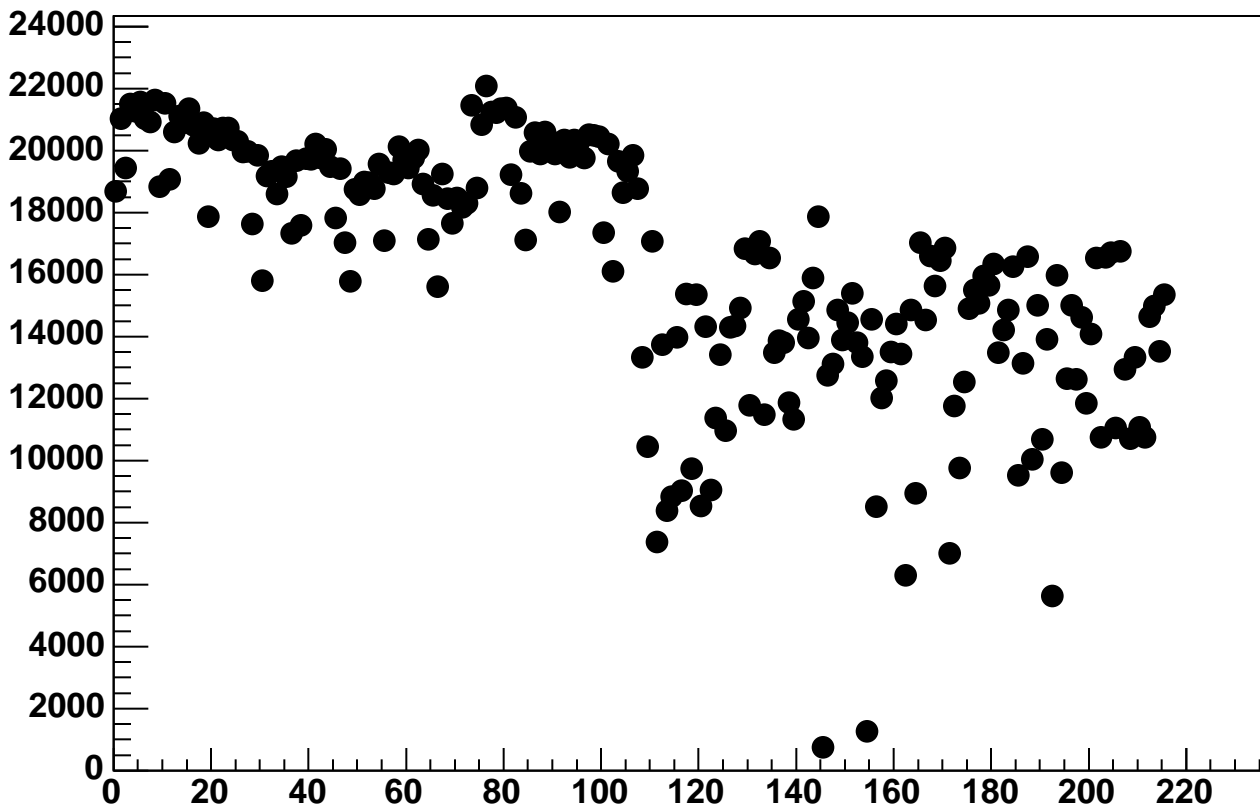
Enable 0, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



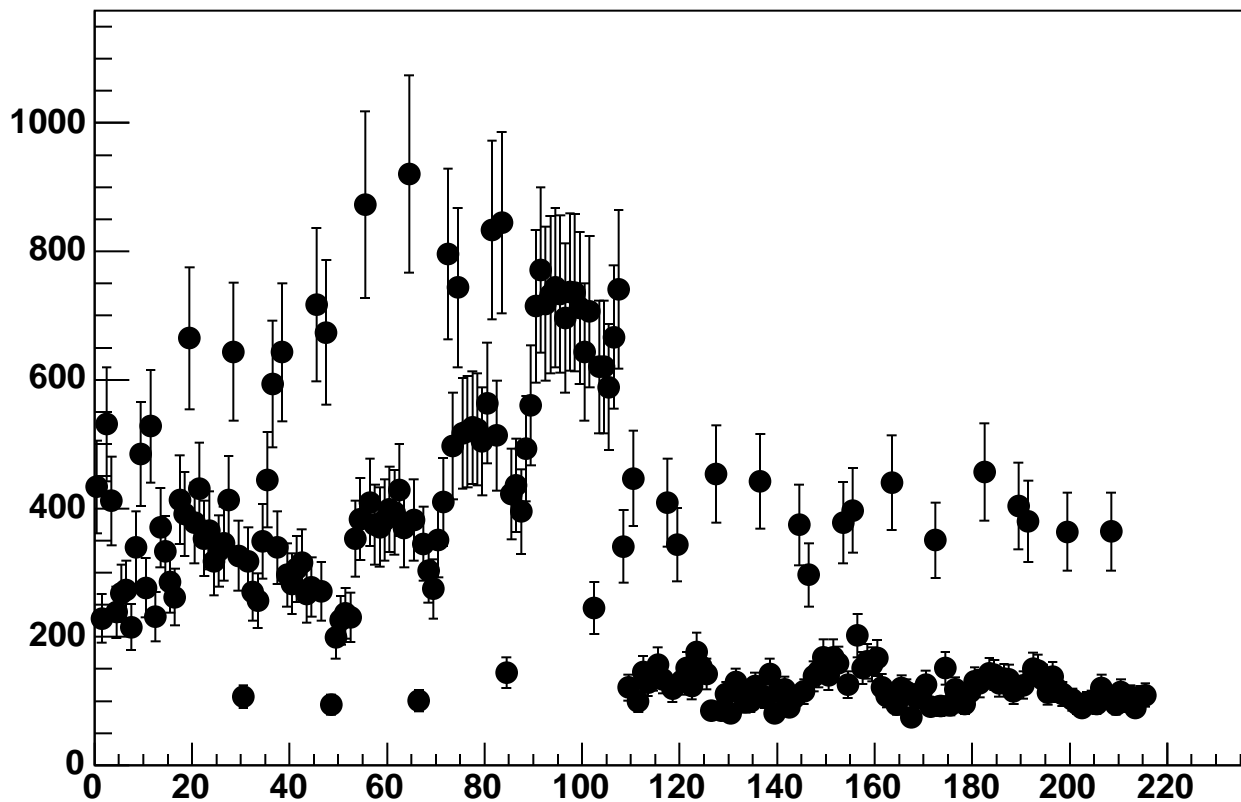
Enable 0, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



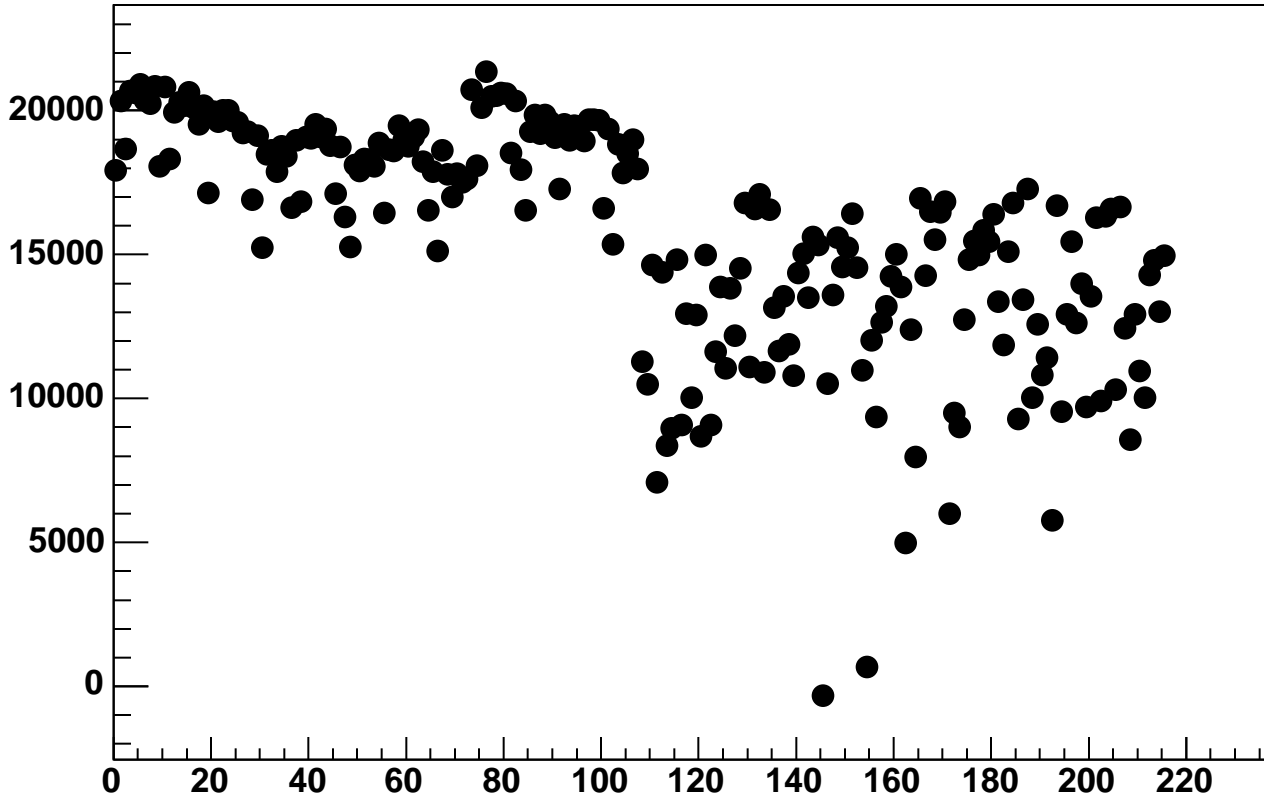
Enable 0, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan



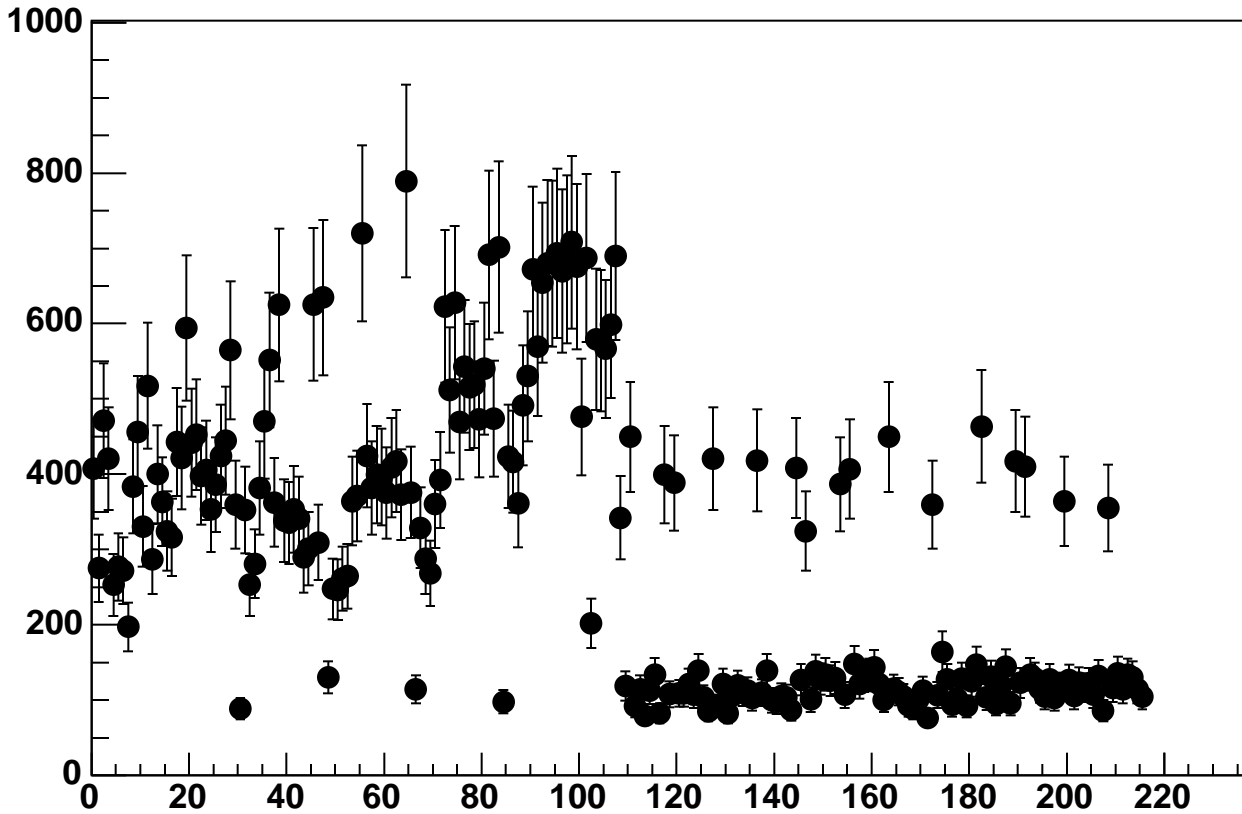
Enable 0, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan



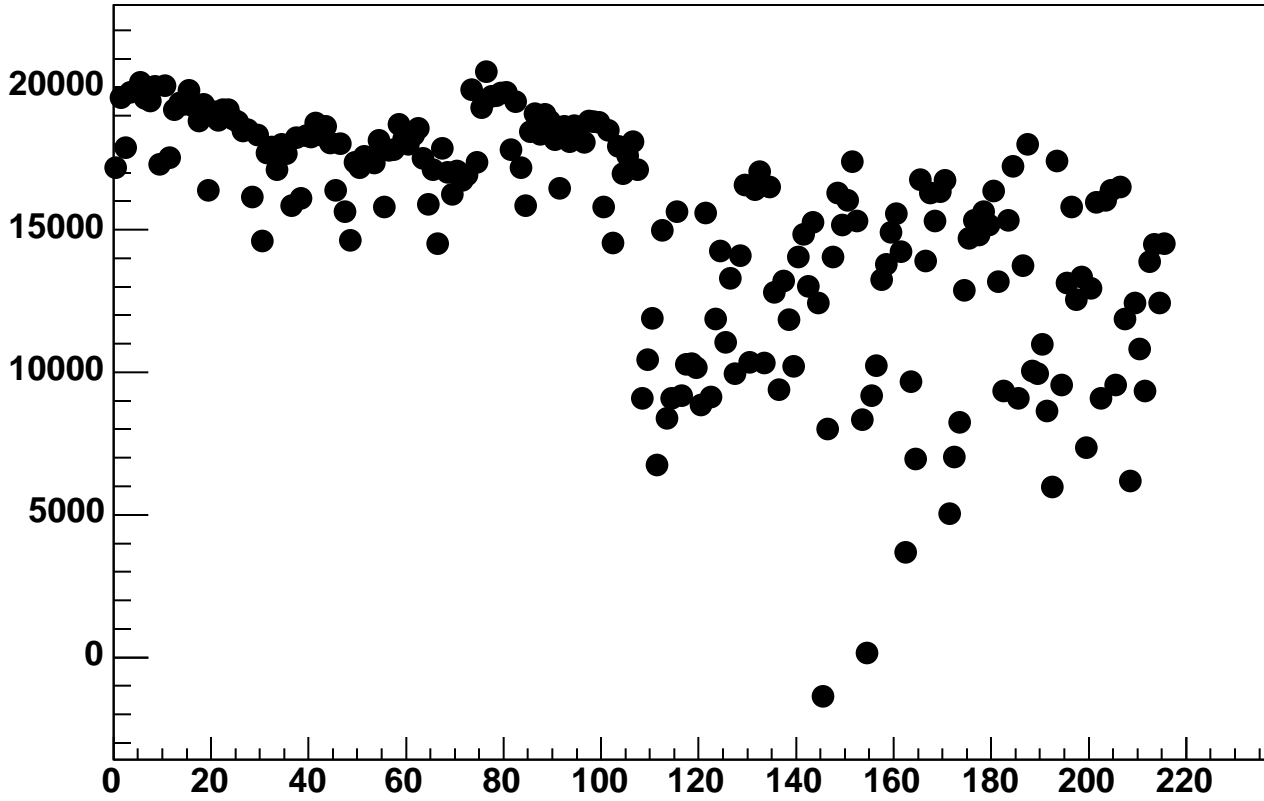
Enable 0, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



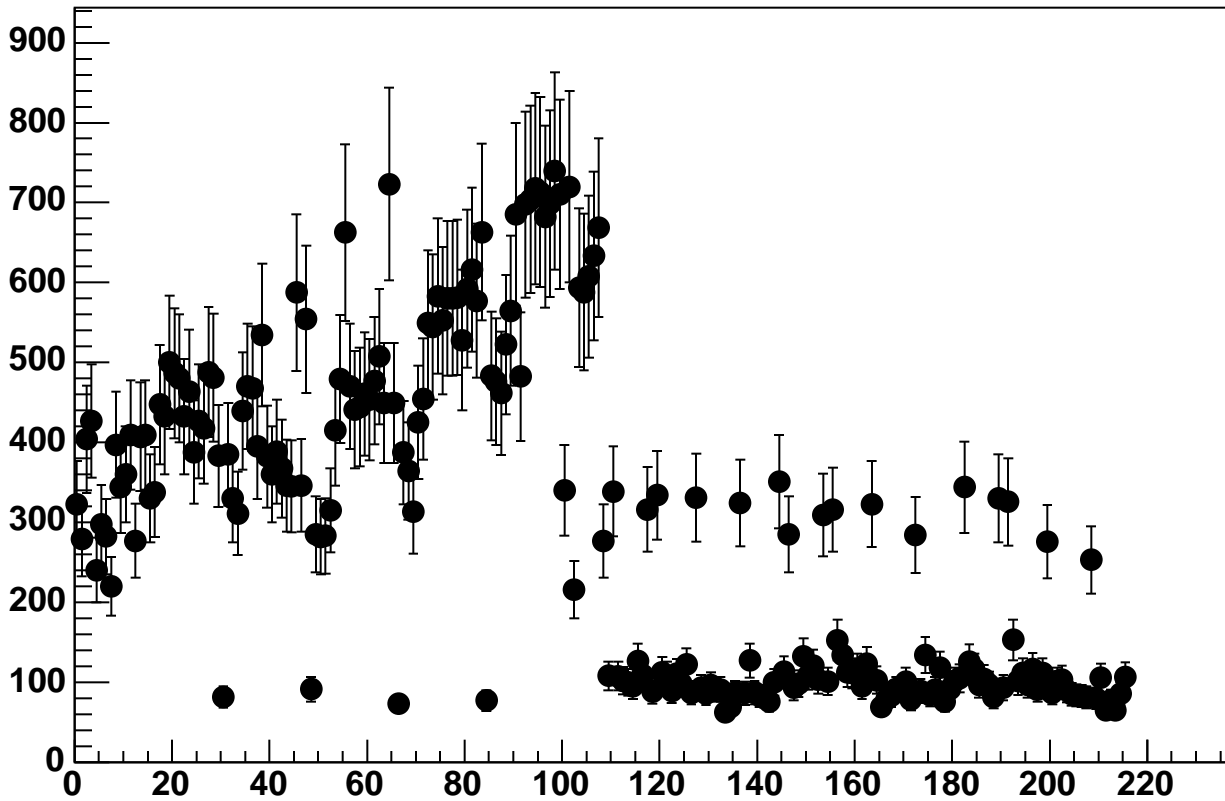
Enable 0, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



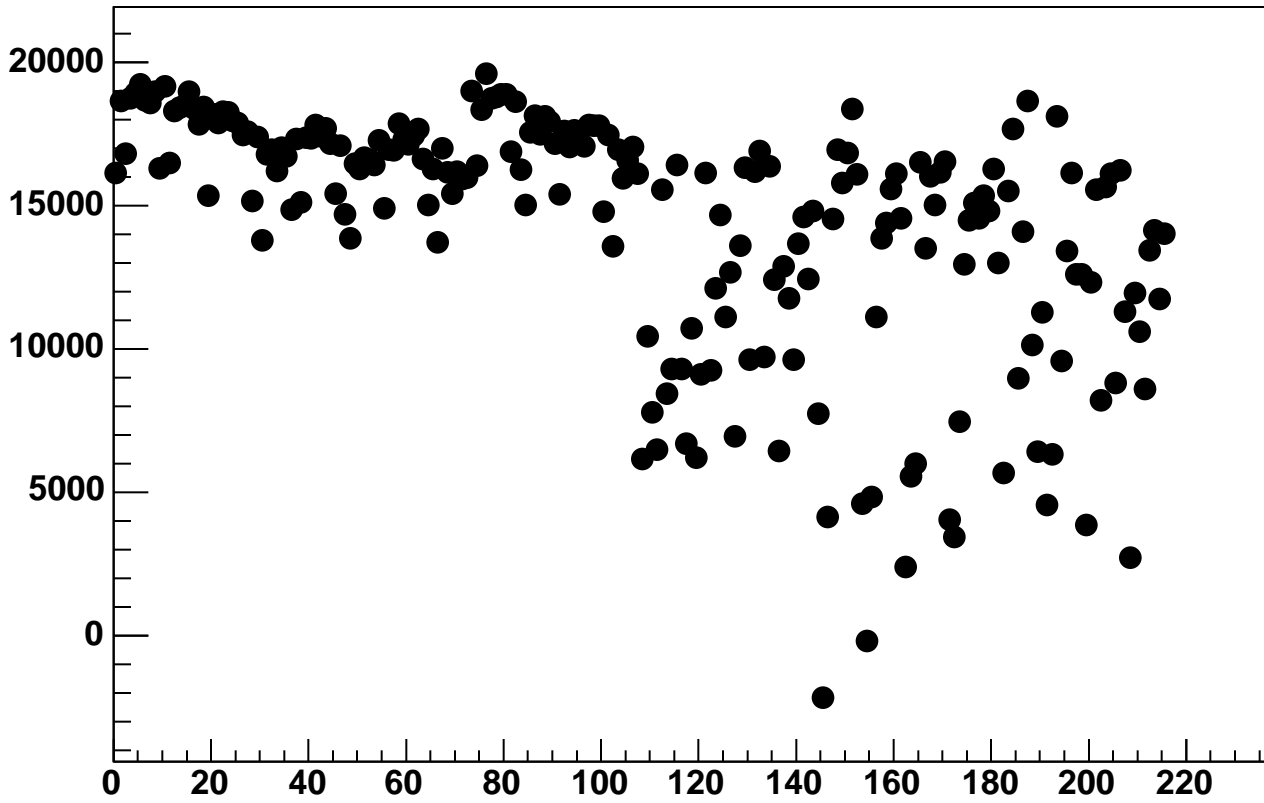
Enable 0, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan



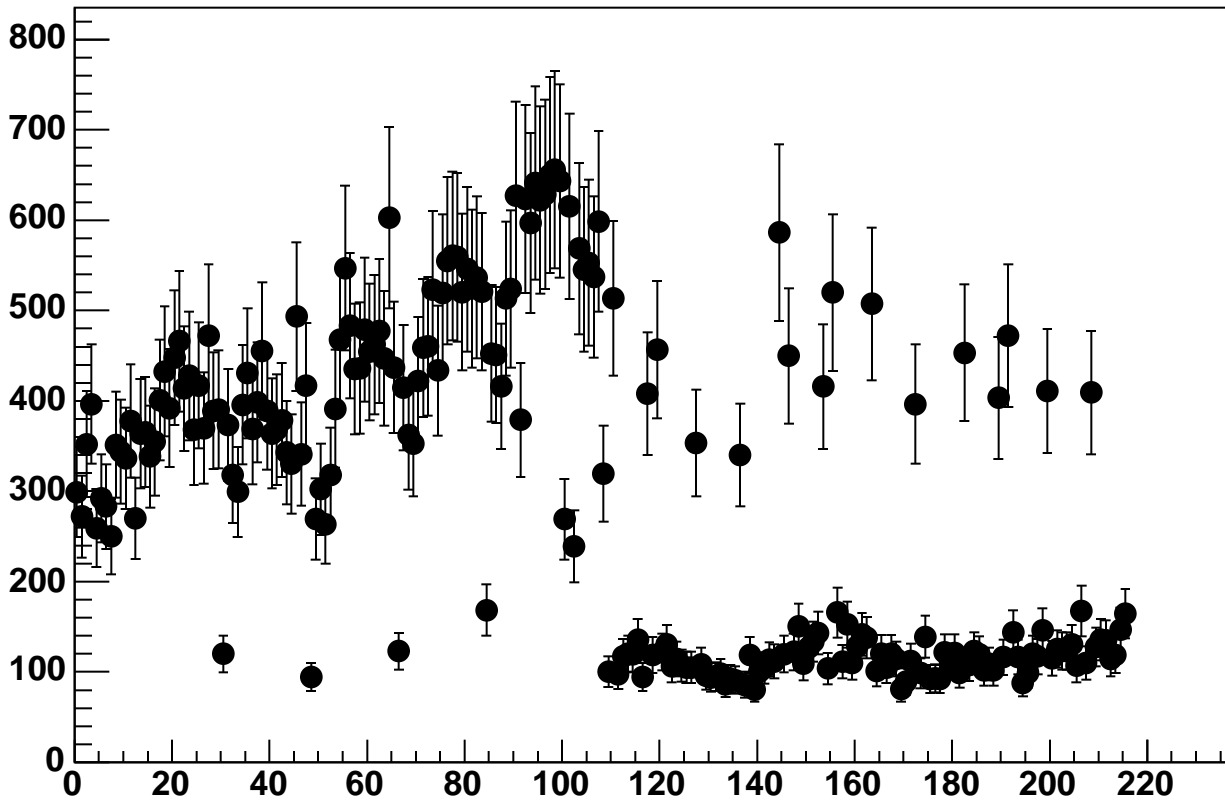
Enable 0, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan



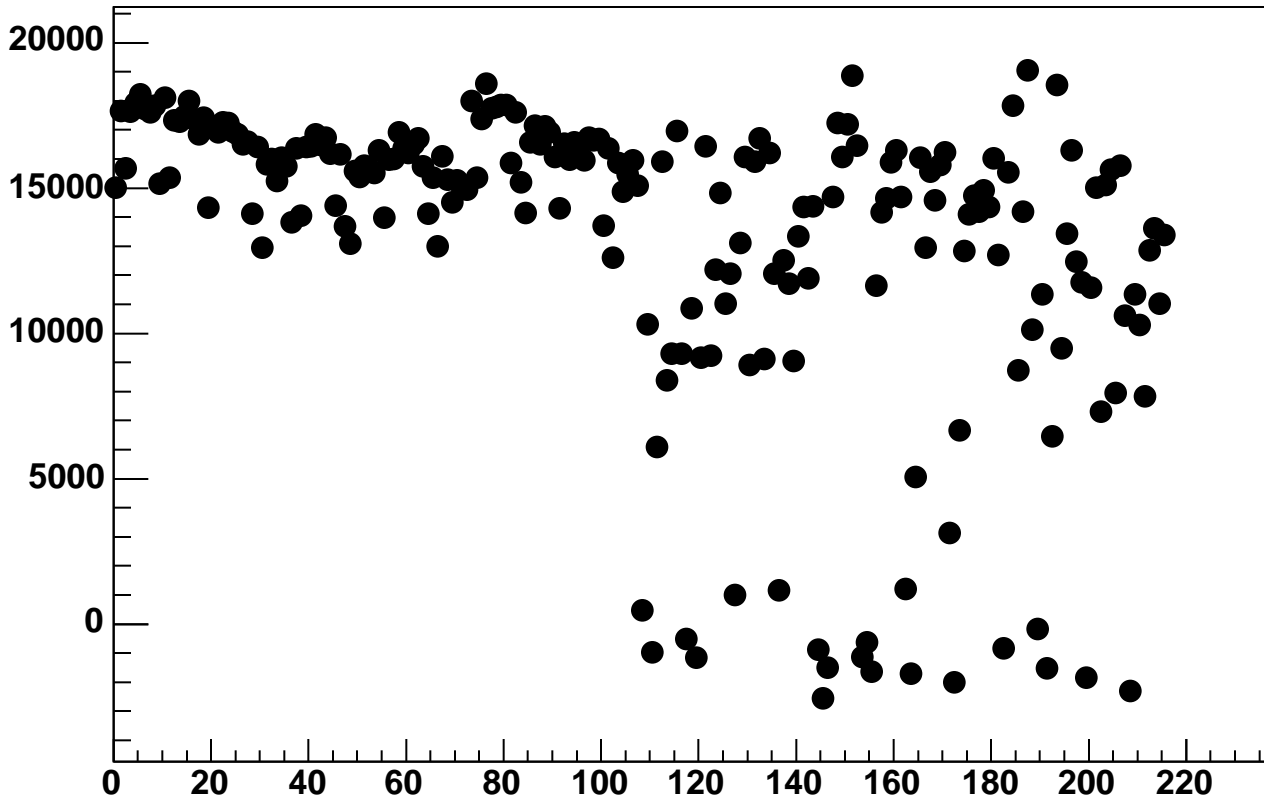
Enable 0, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



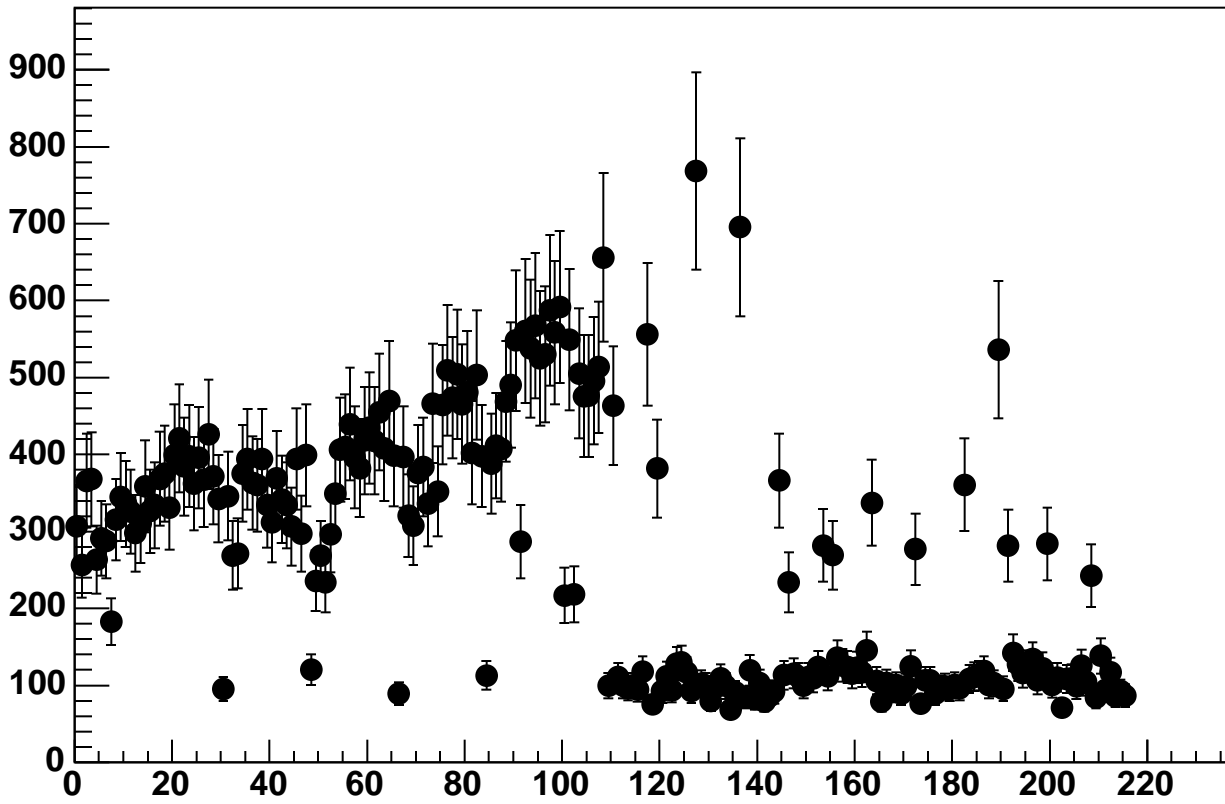
Enable 0, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



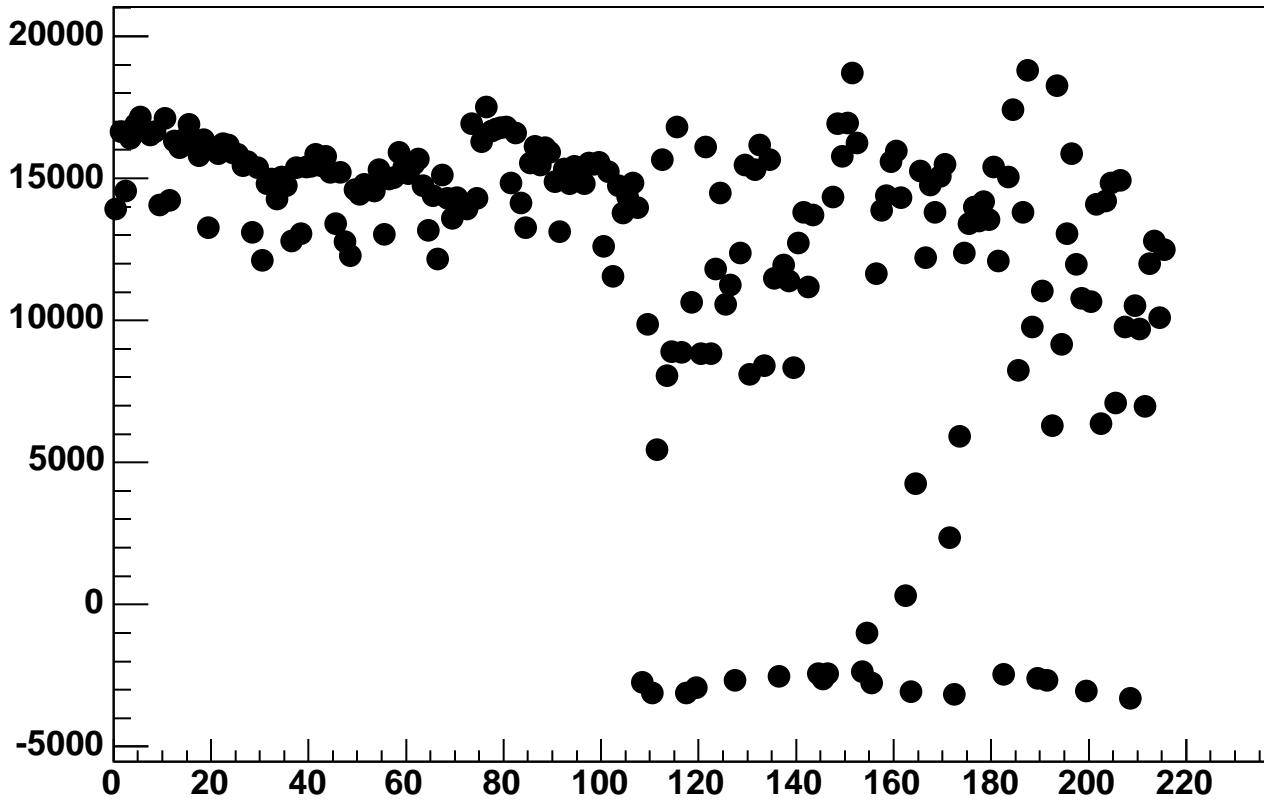
Enable 0, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan



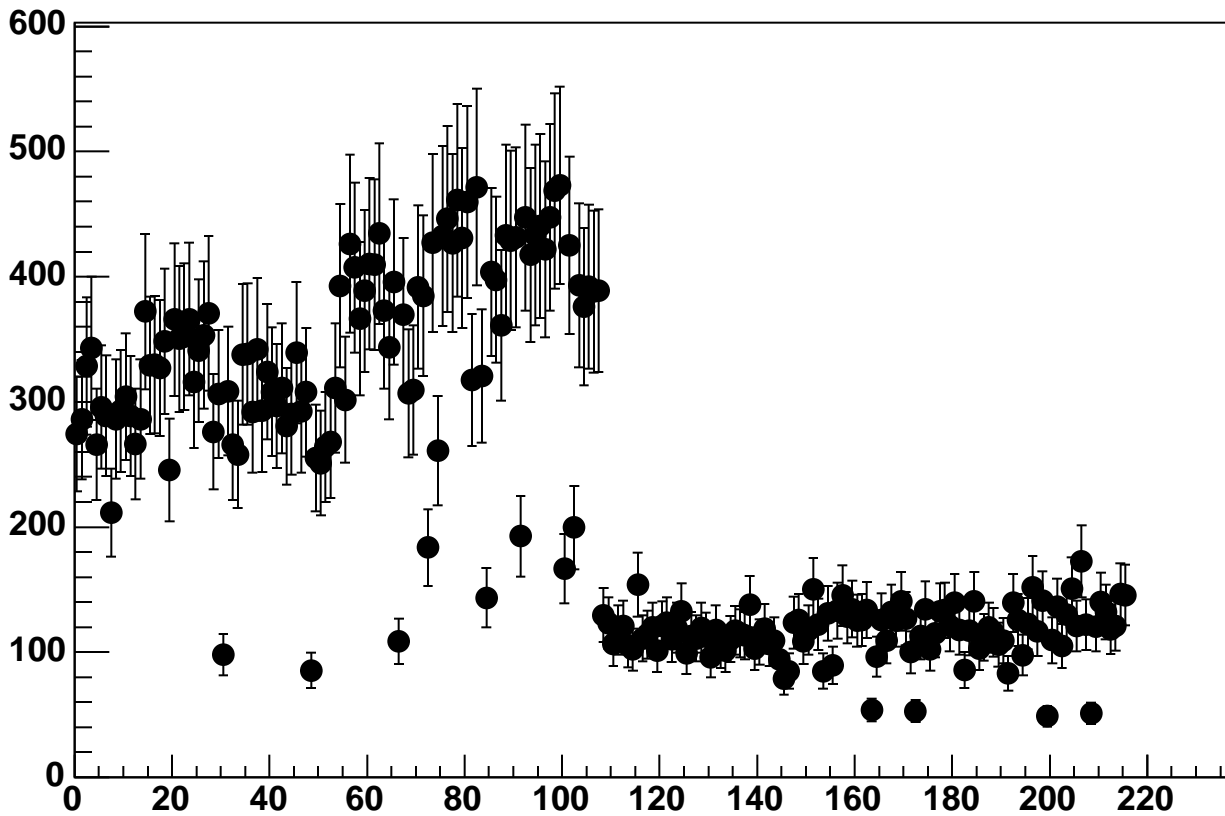
Enable 0, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan



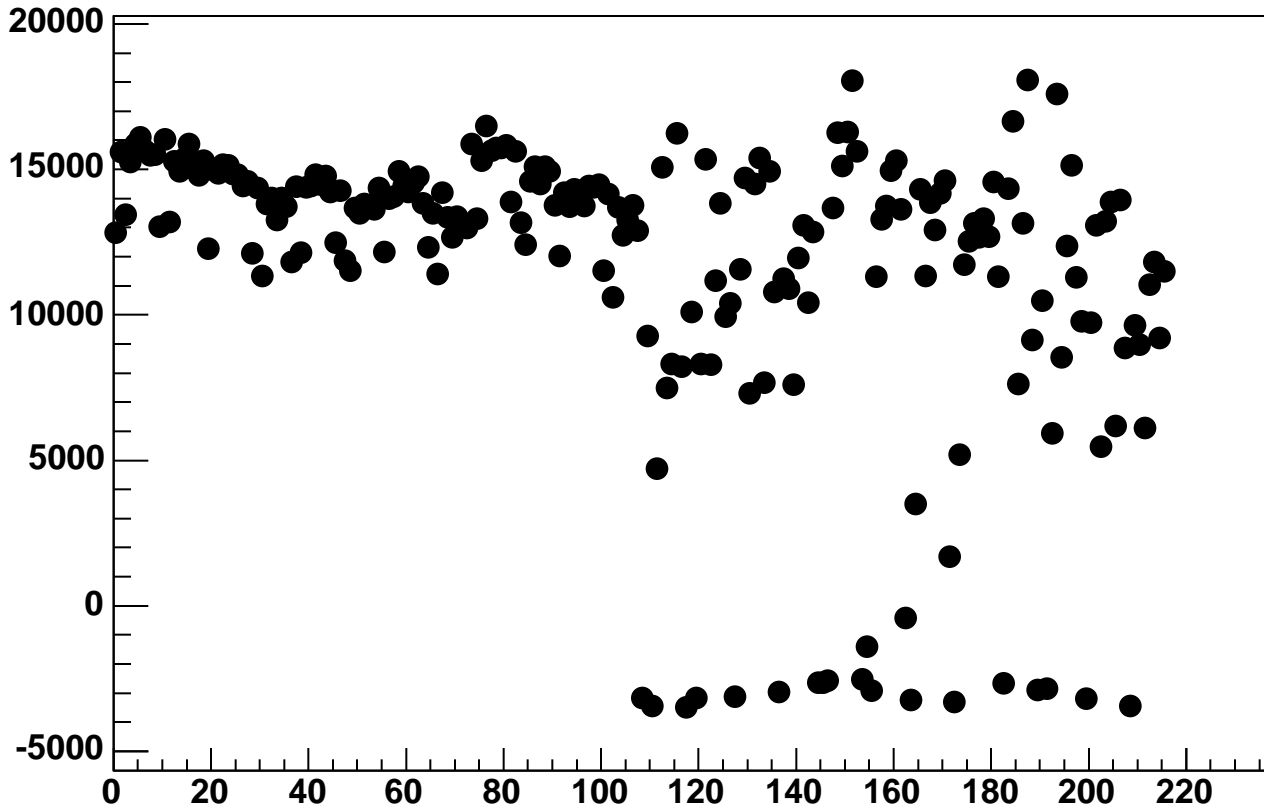
Enable 0, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



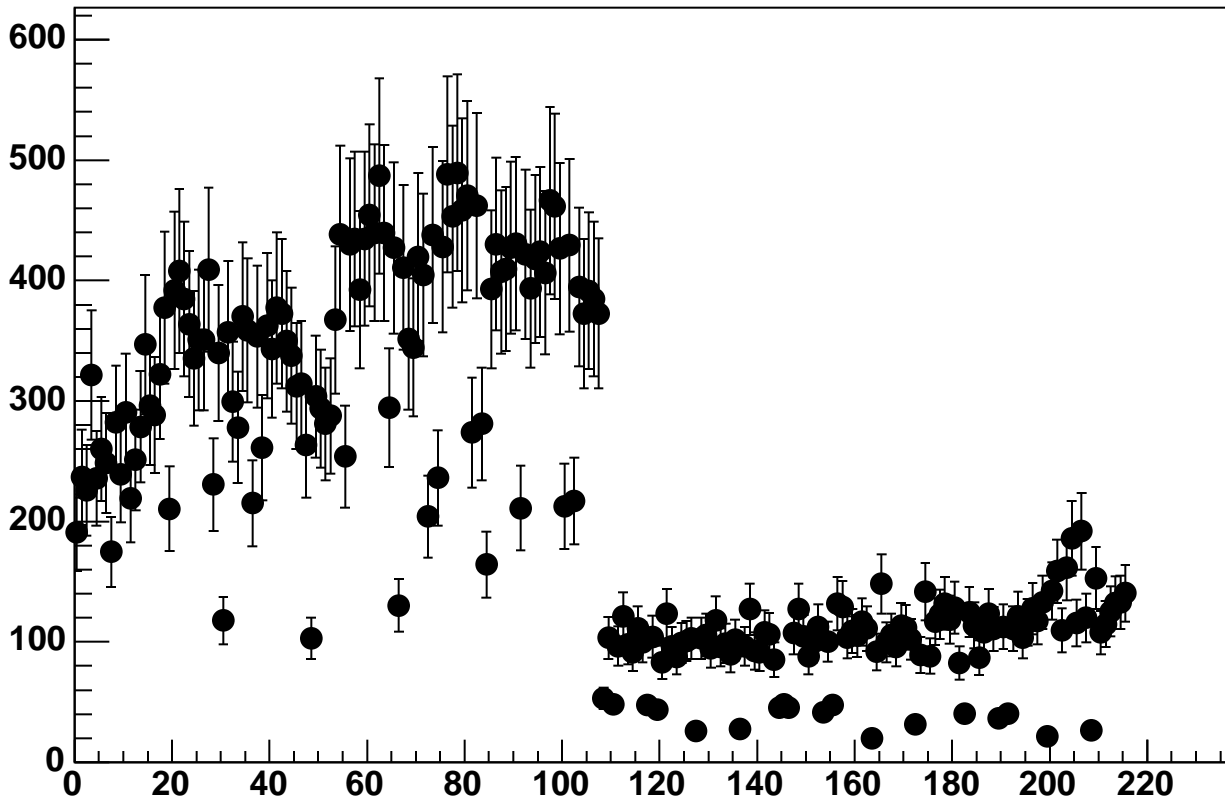
Enable 0, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



Enable 0, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan

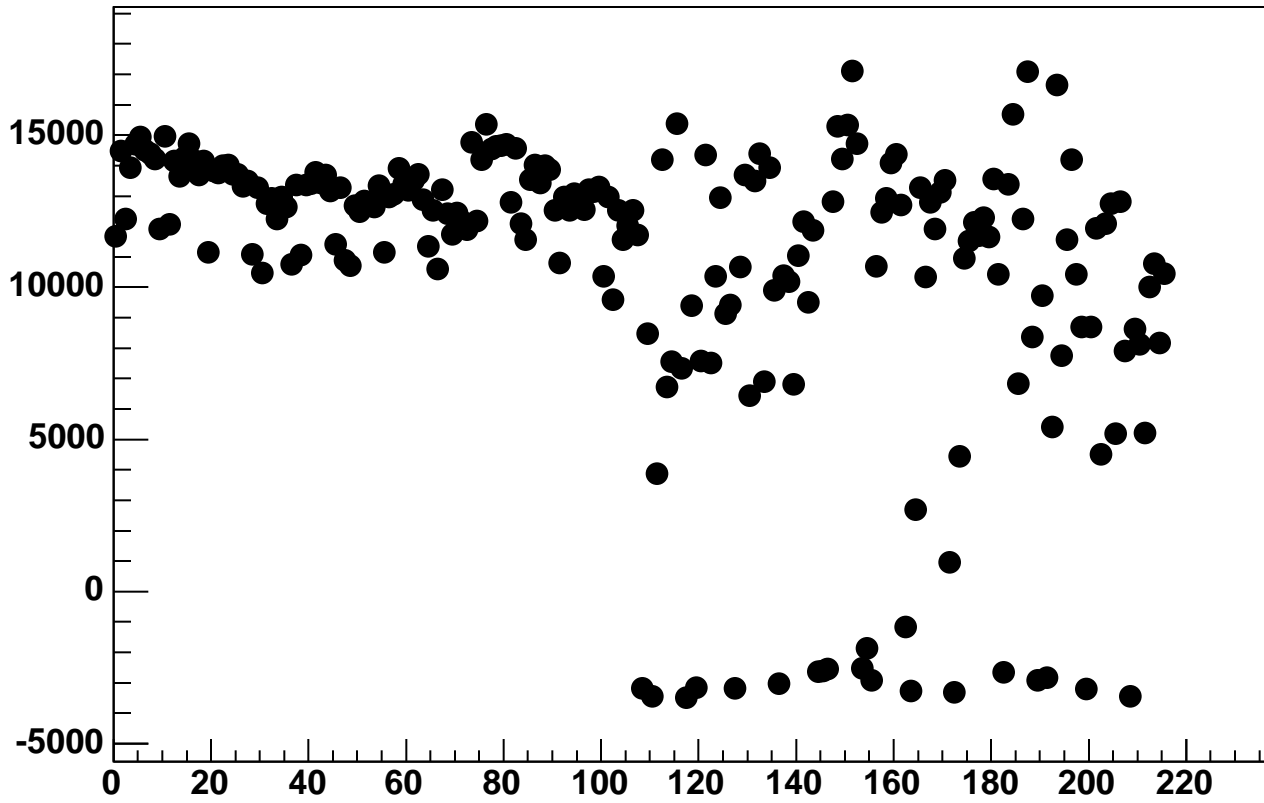


Enable 0, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan

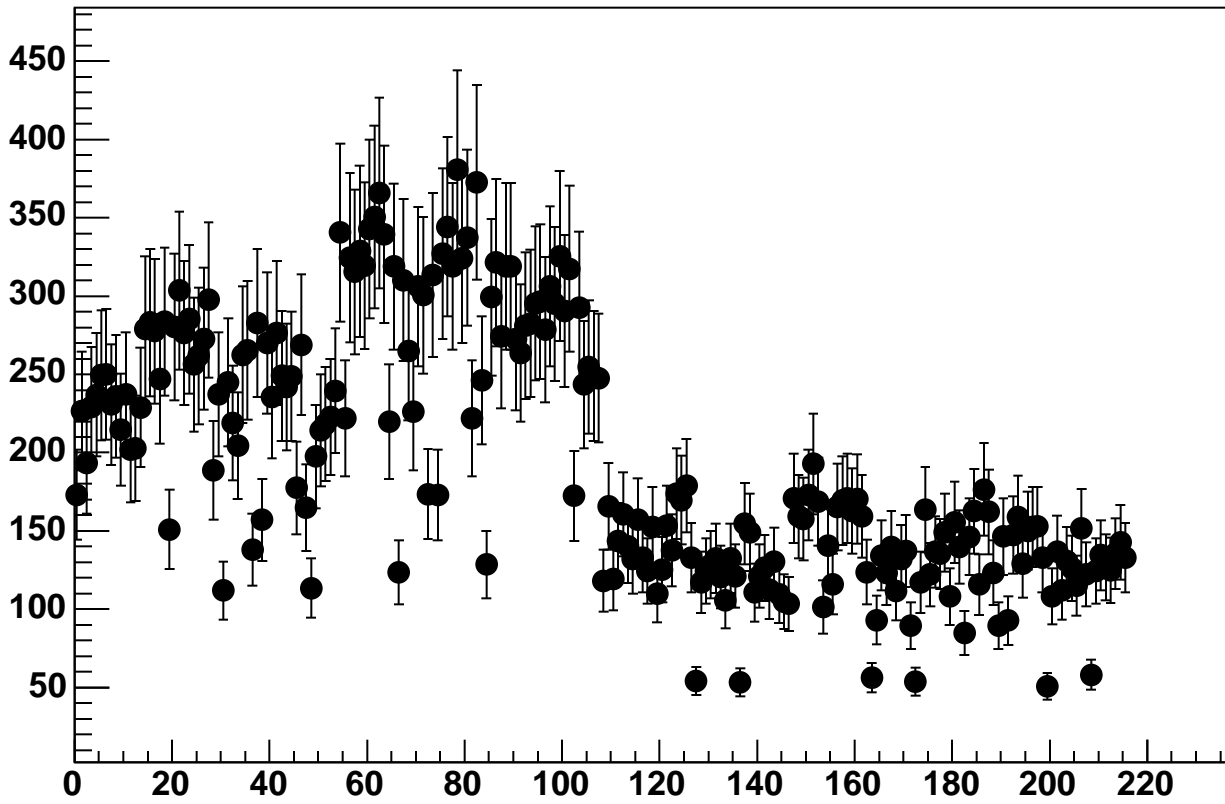




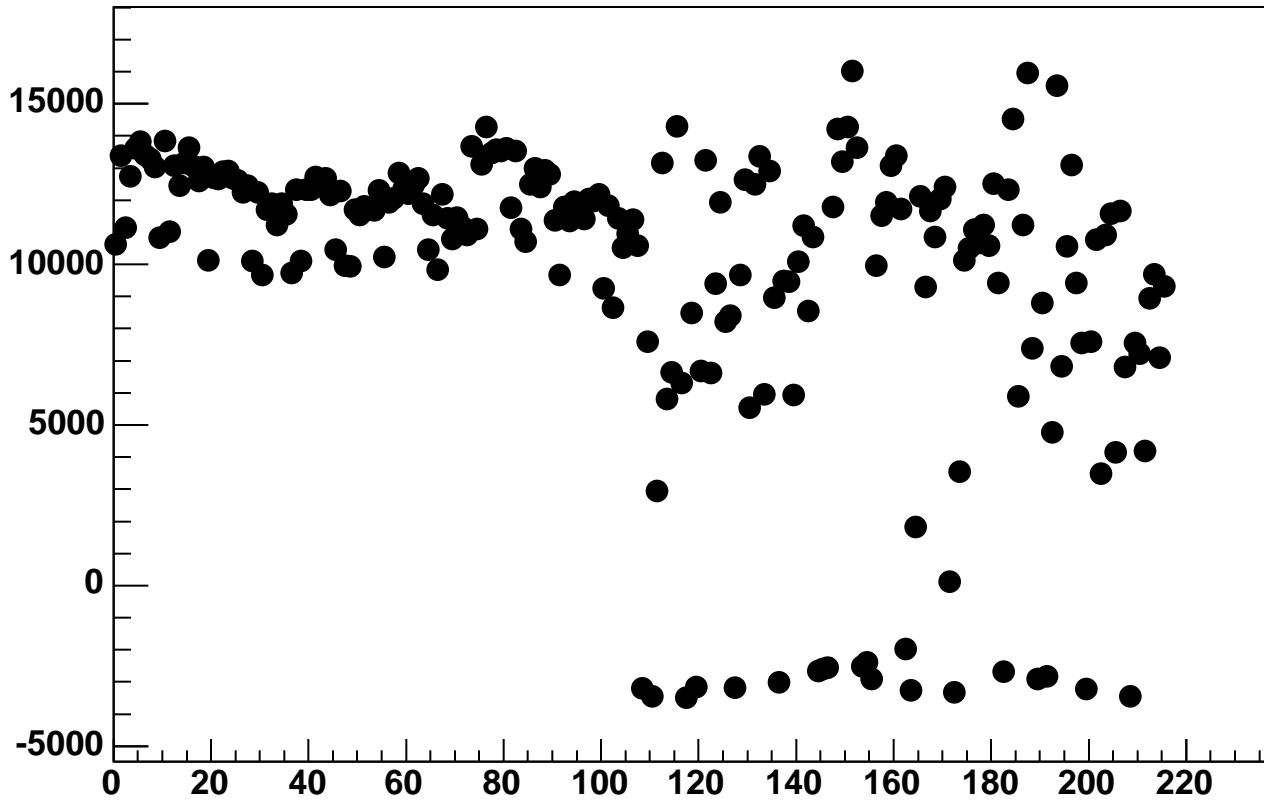
Enable 0, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



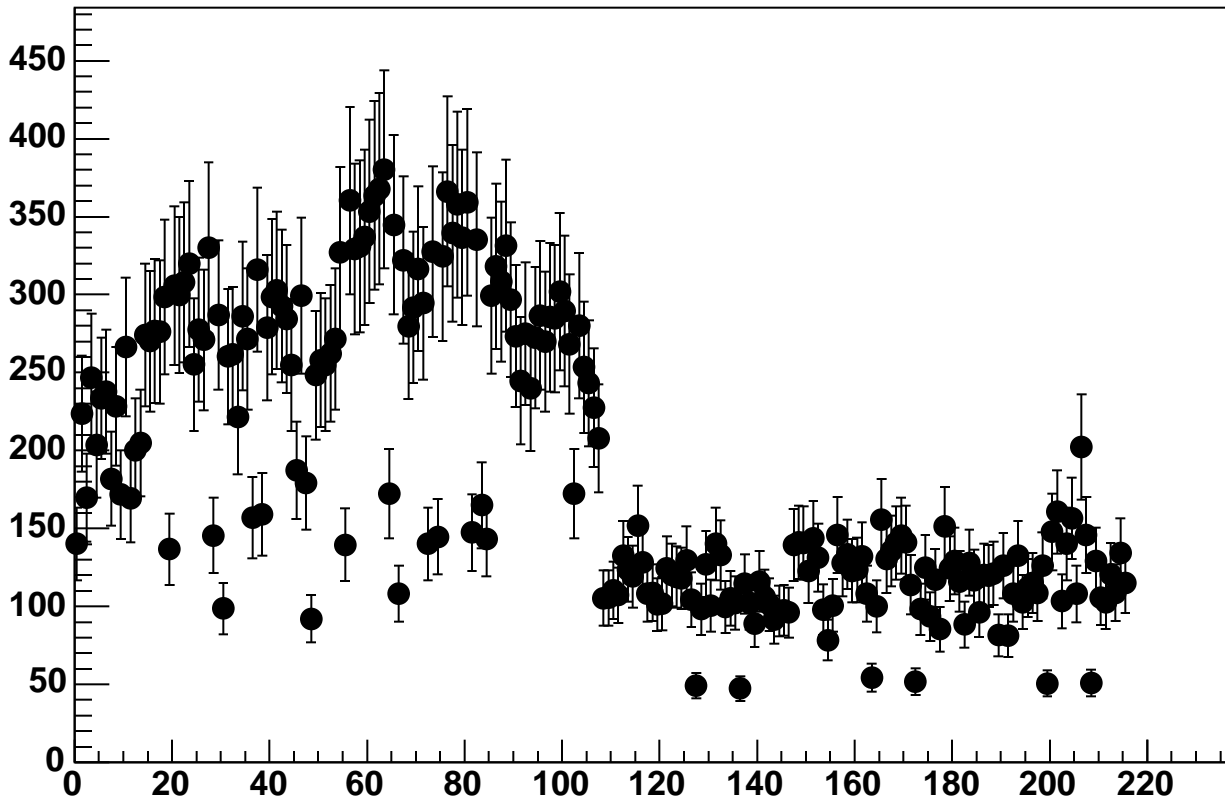
Enable 0, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



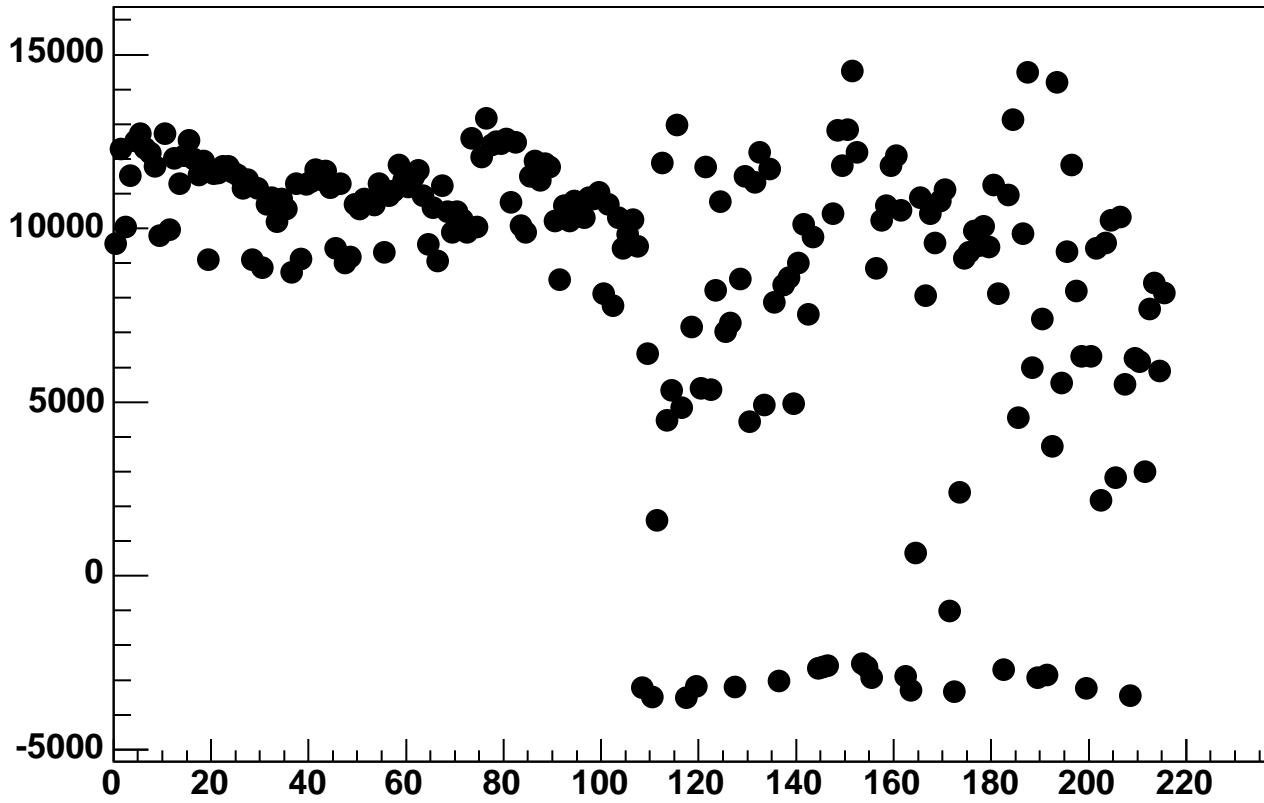
Enable 0, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan



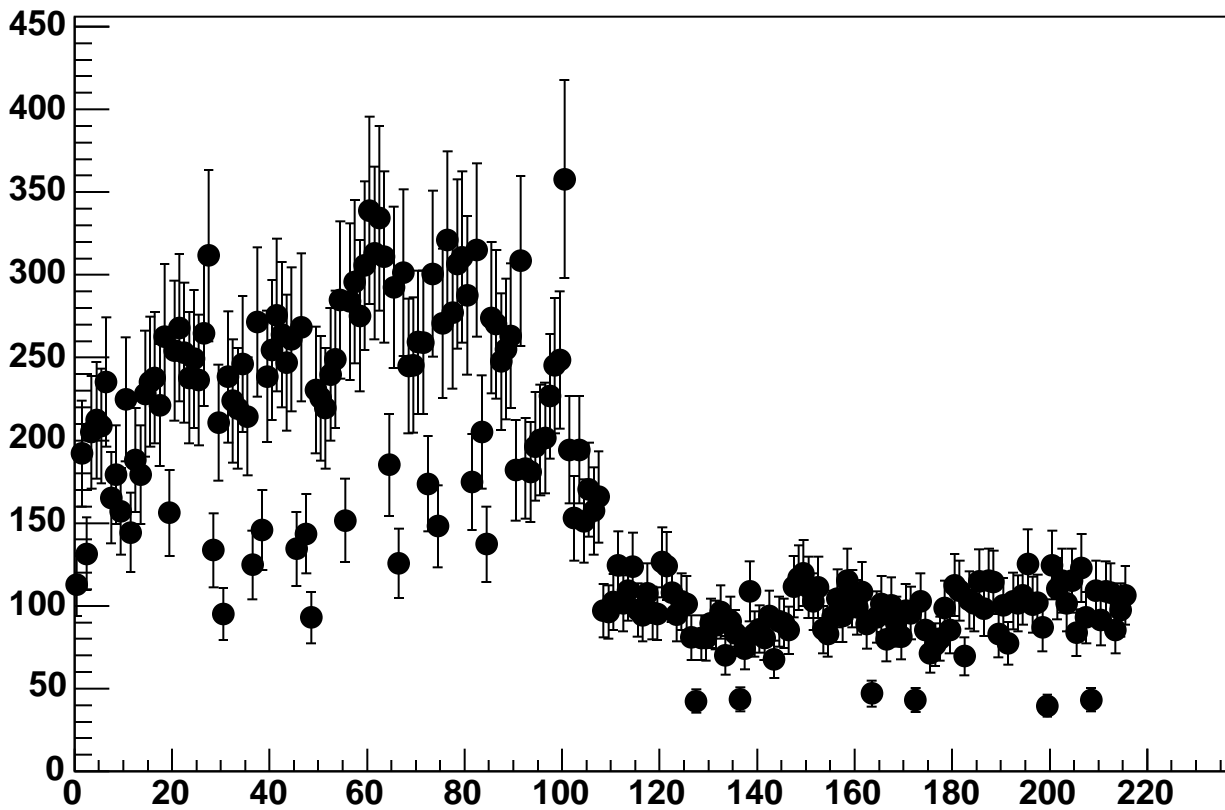
Enable 0, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan



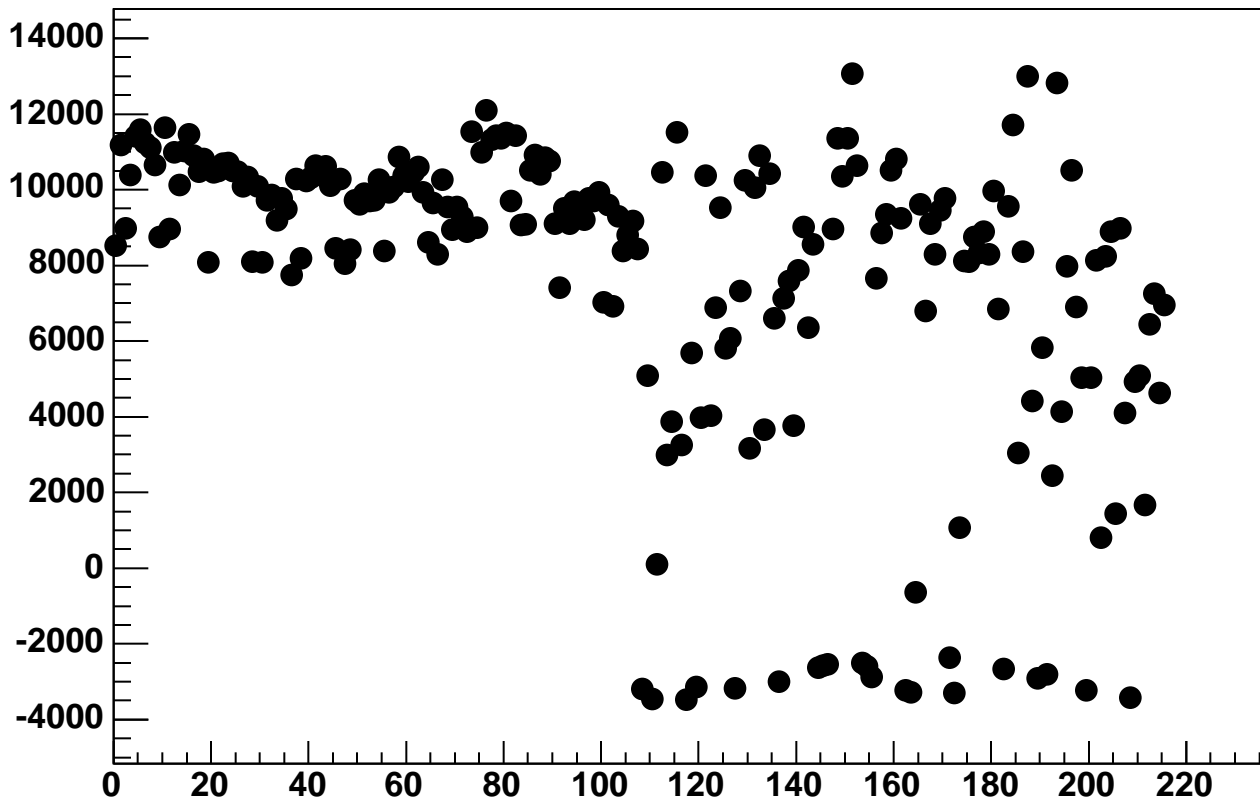
Enable 0, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



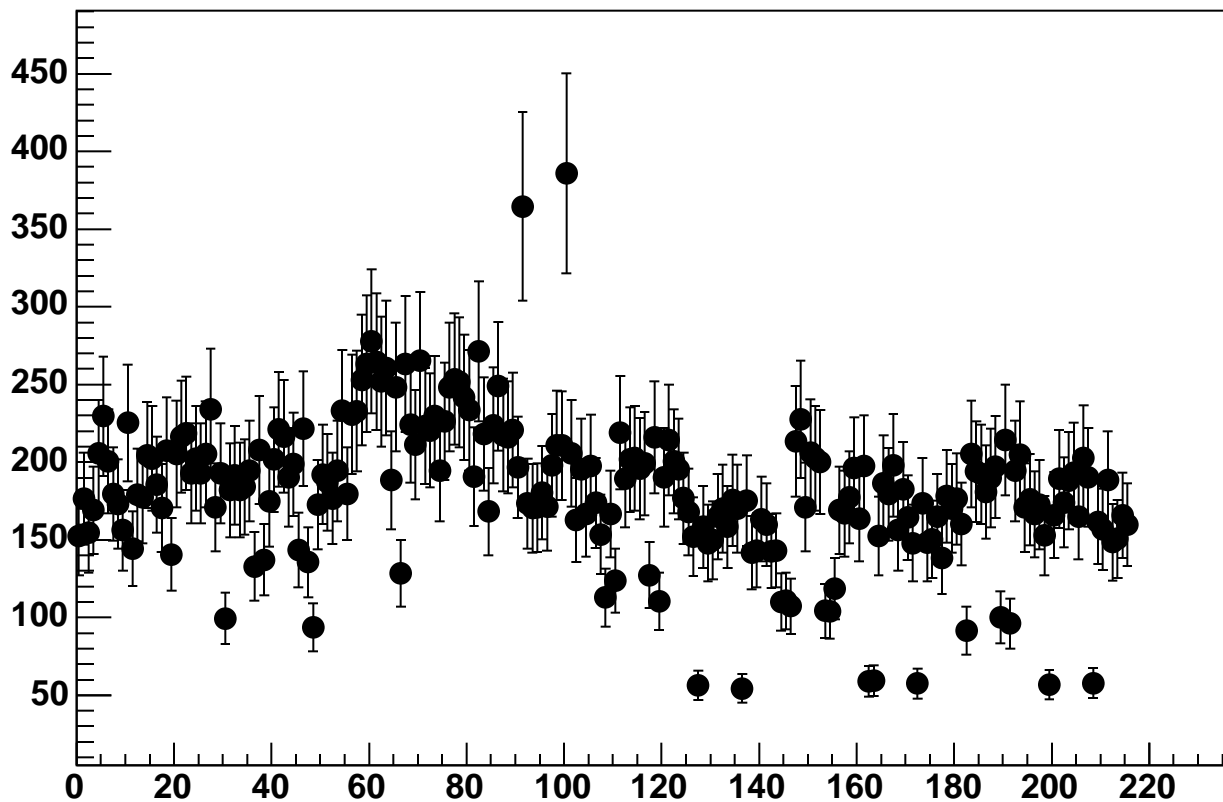
Enable 0, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



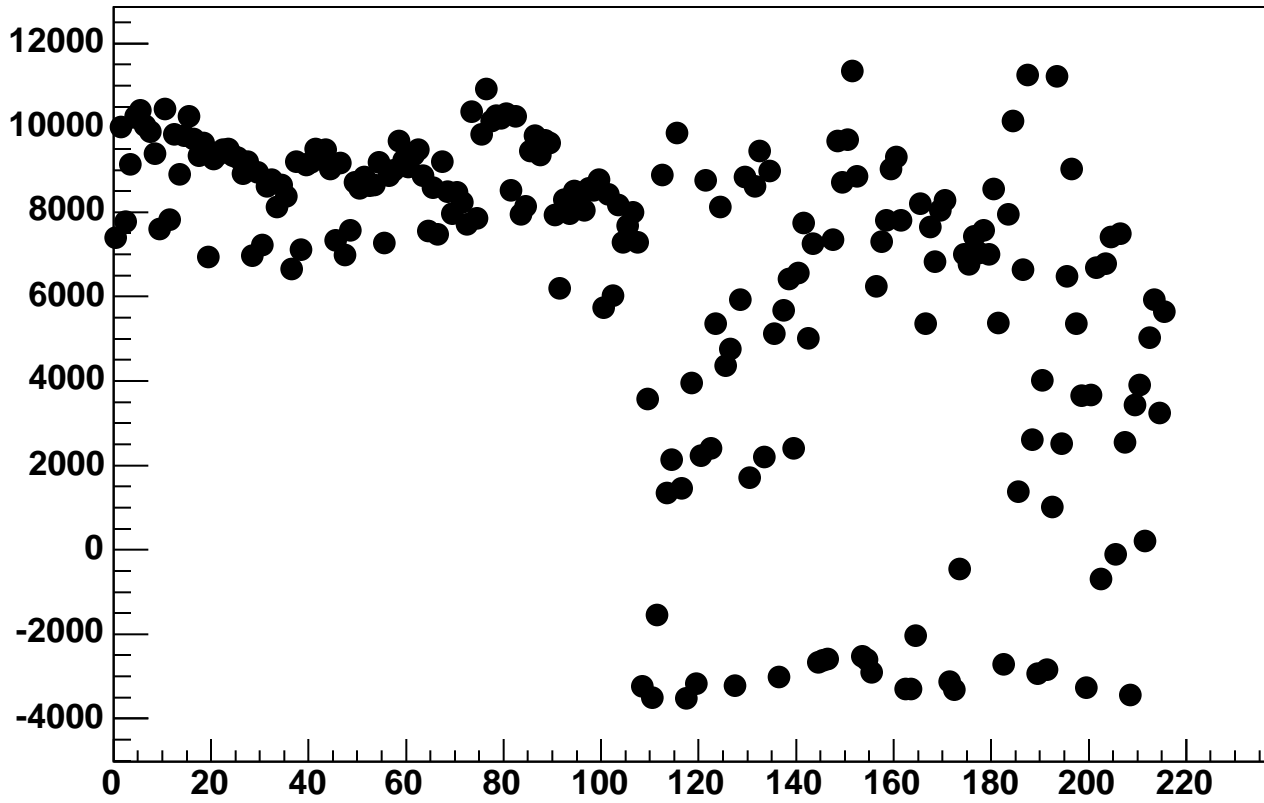
Enable 0, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan



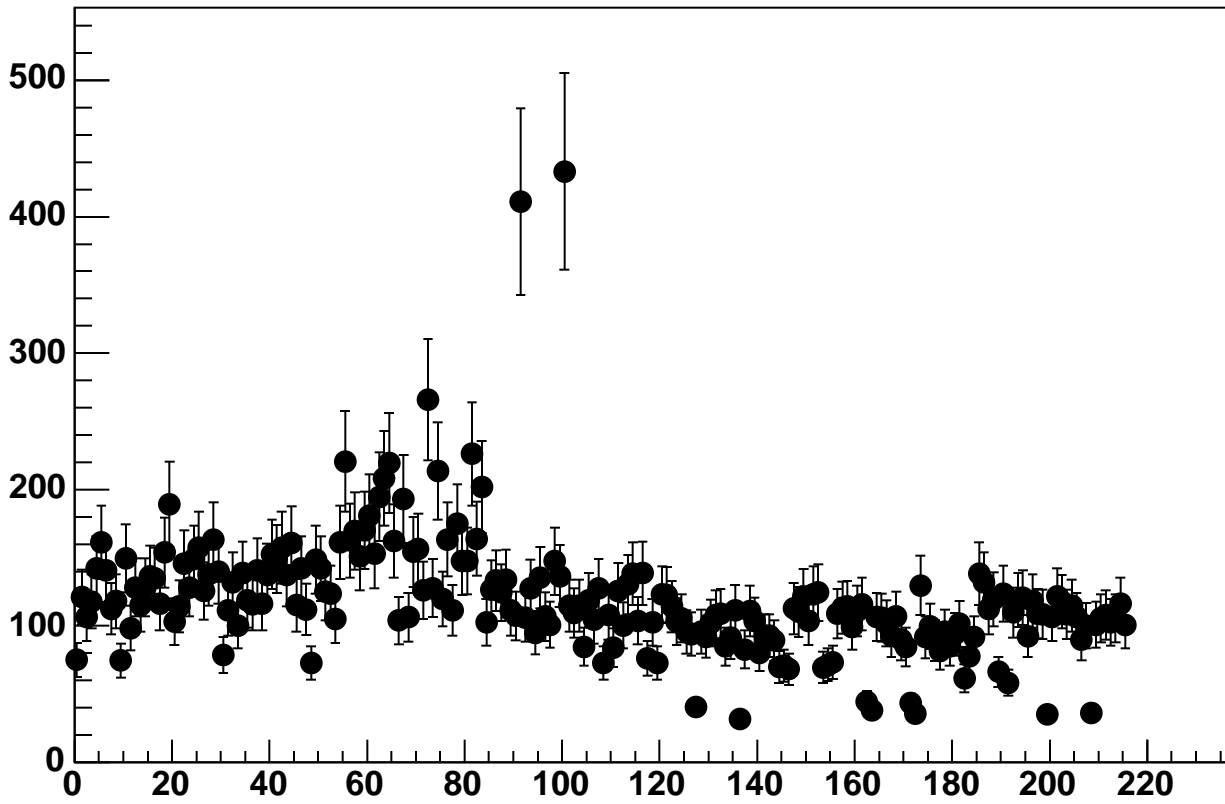
Enable 0, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan



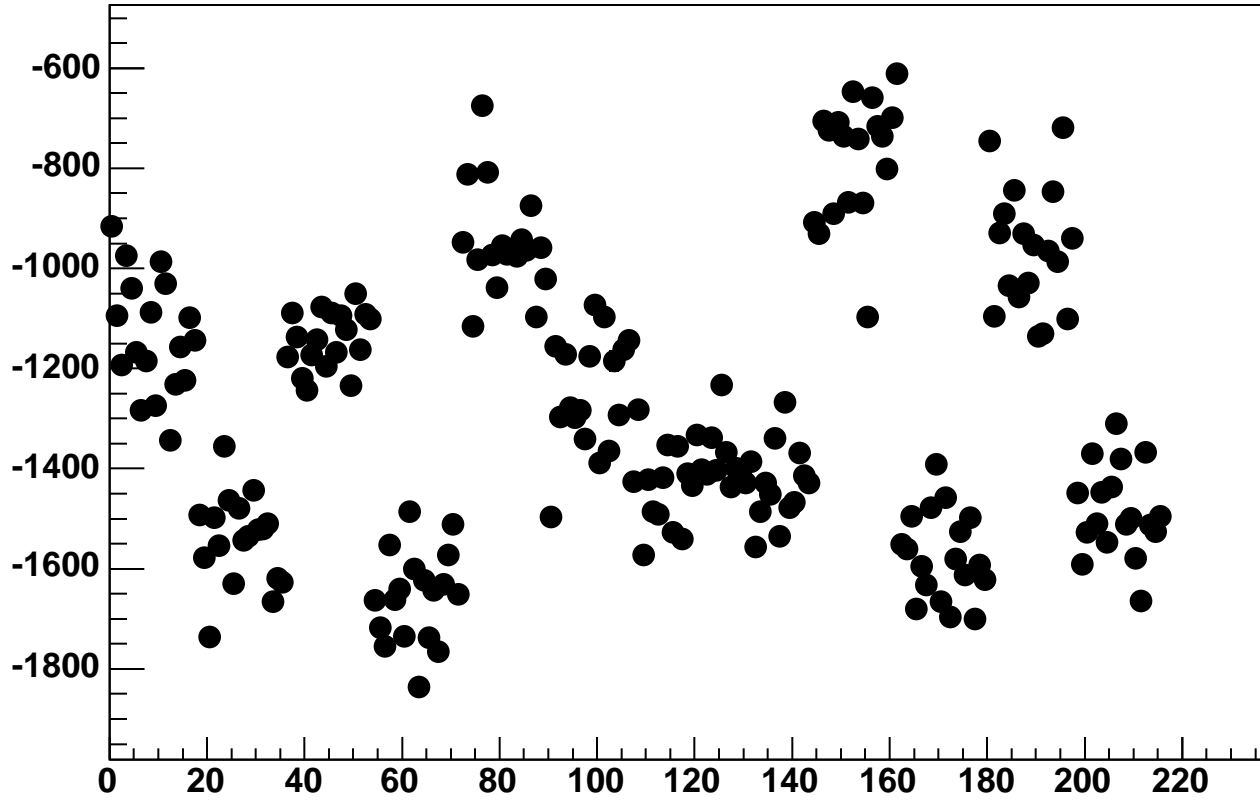
Enable 0, DAC=1600, Hold=245, ADC Mean vs 18\*Chip+Chan



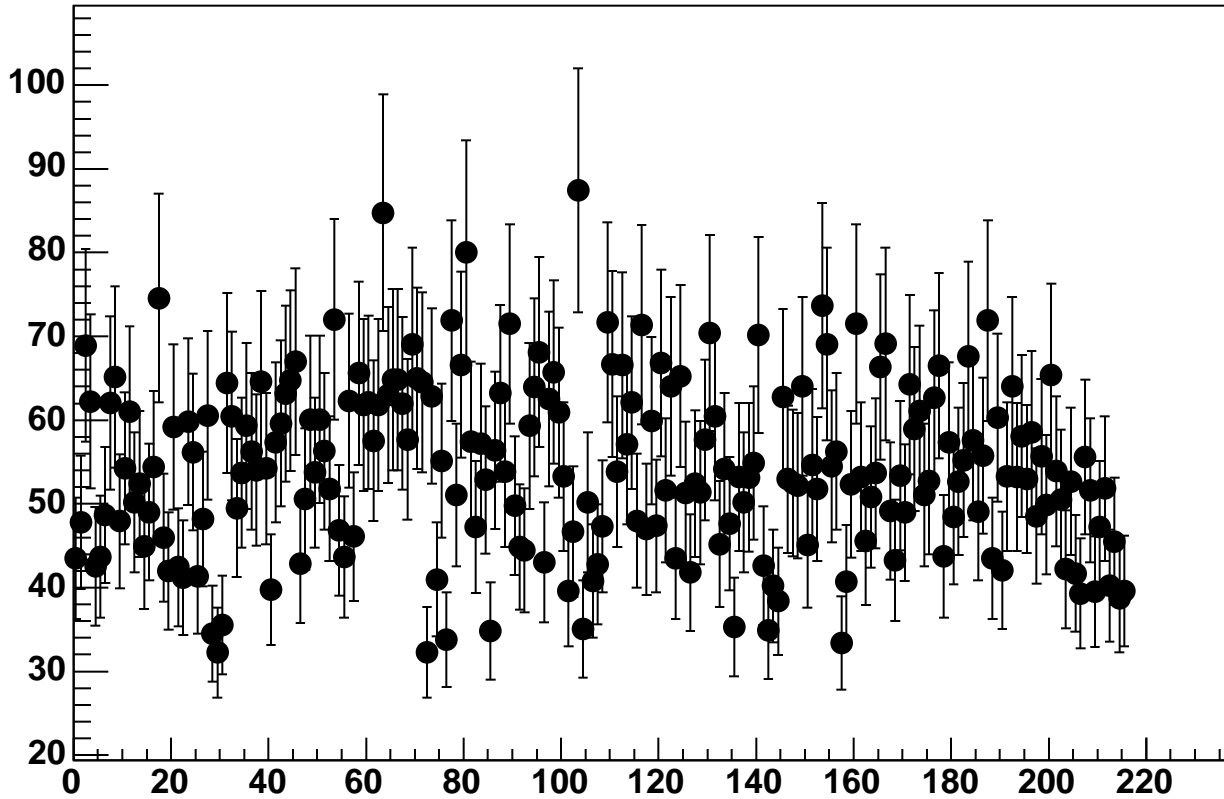
Enable 0, DAC=1600, Hold=245, ADC Noise vs 18\*Chip+Chan



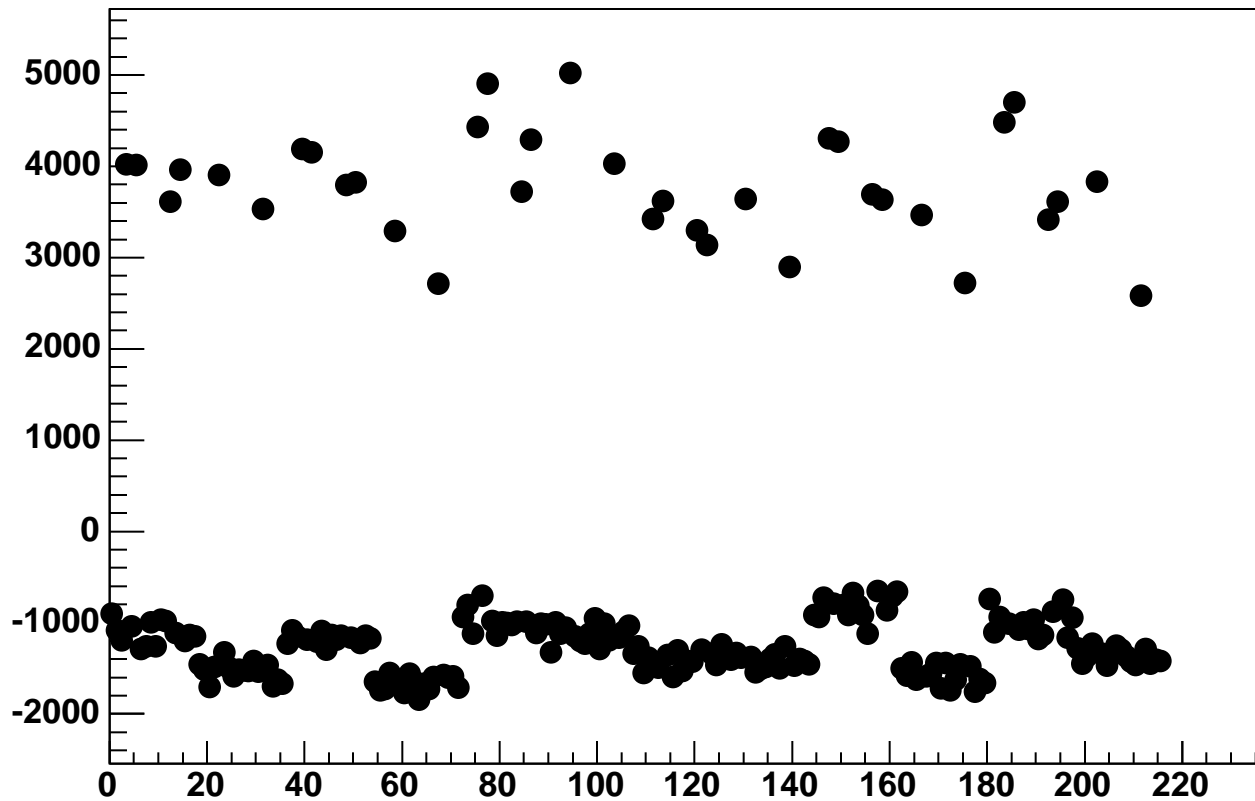
Enable 1, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan



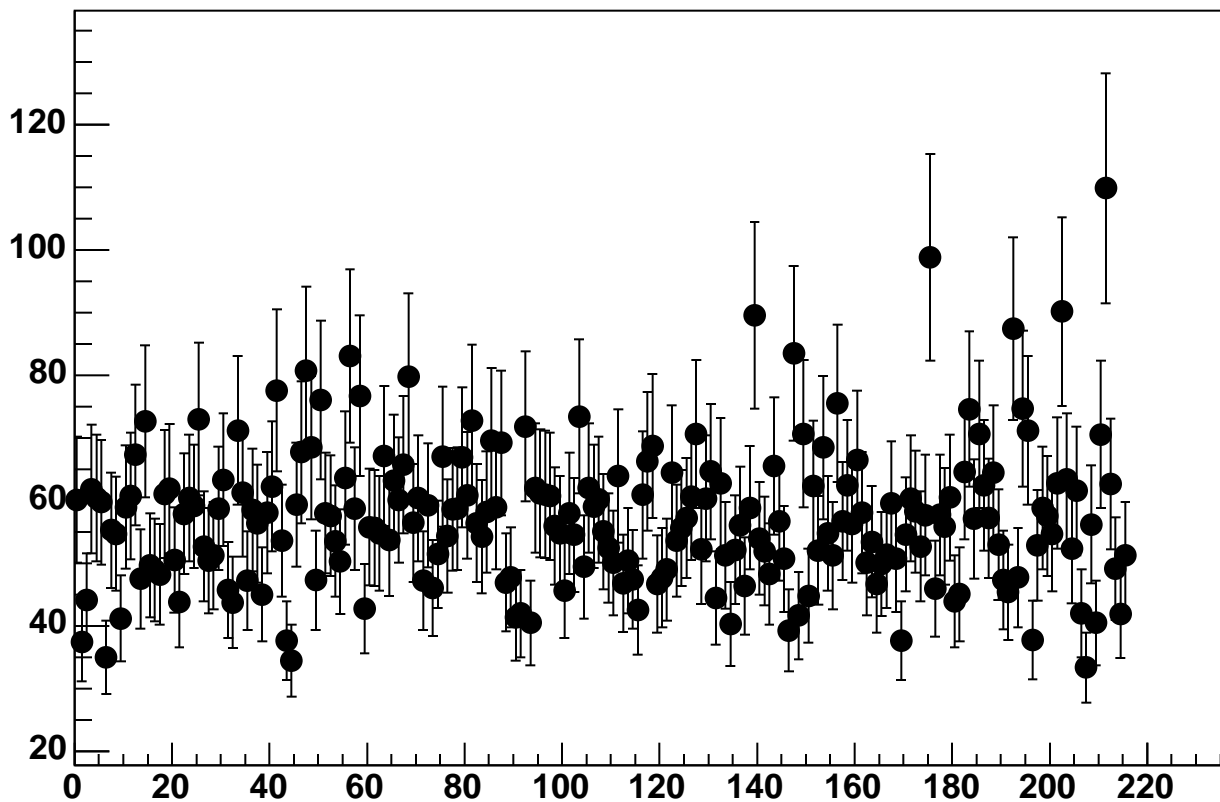
Enable 1, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan



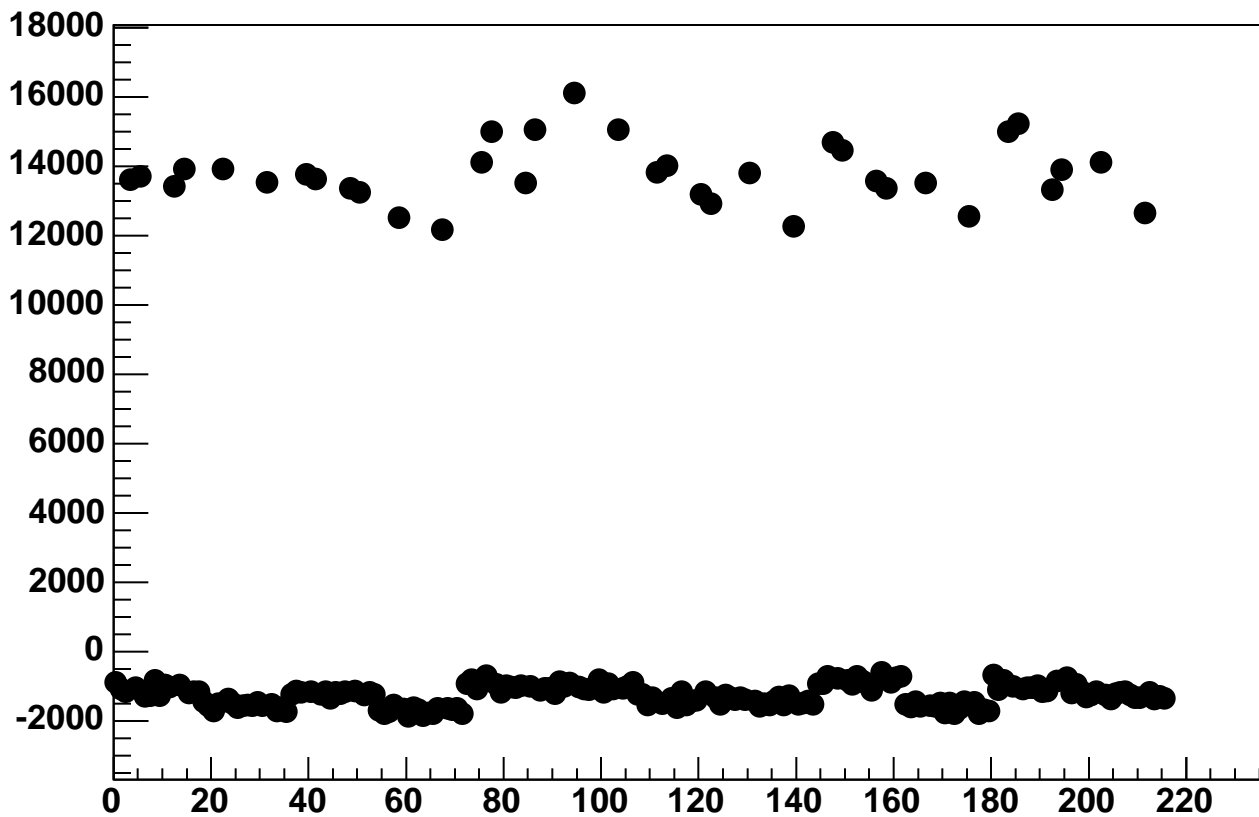
Enable 1, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



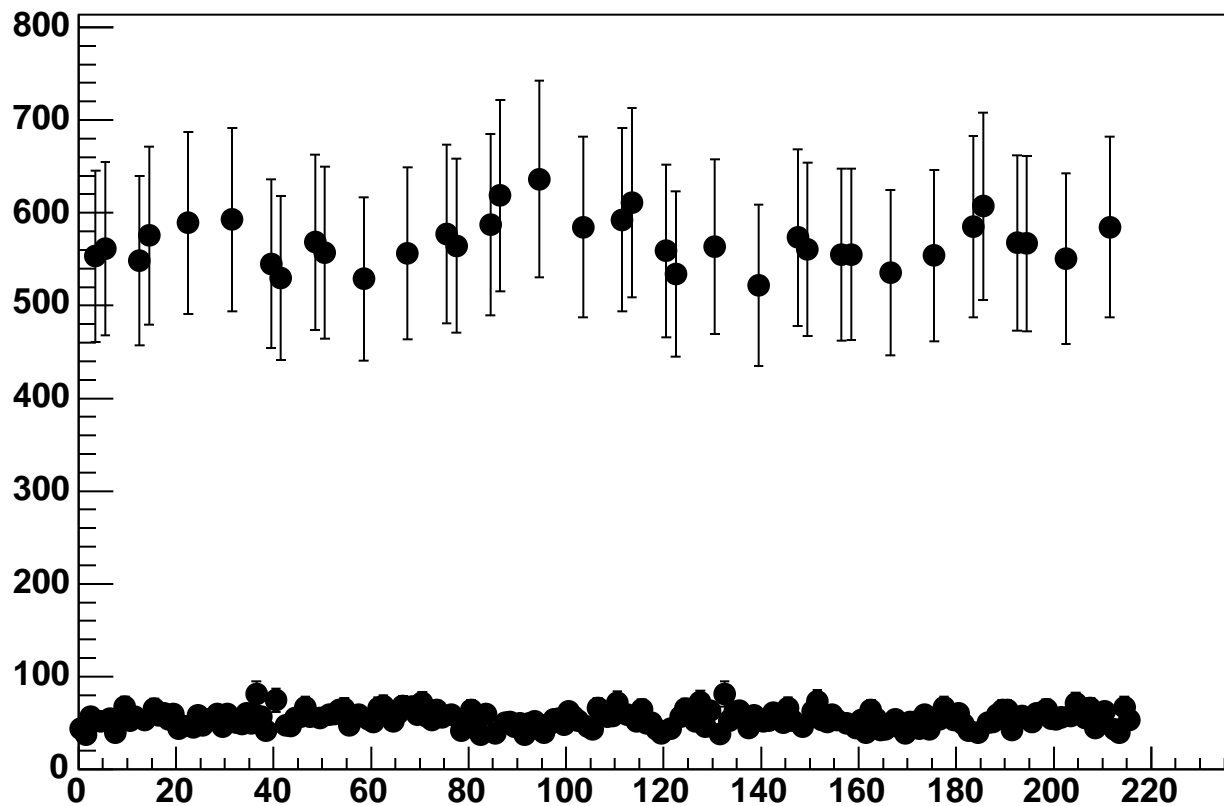
Enable 1, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan

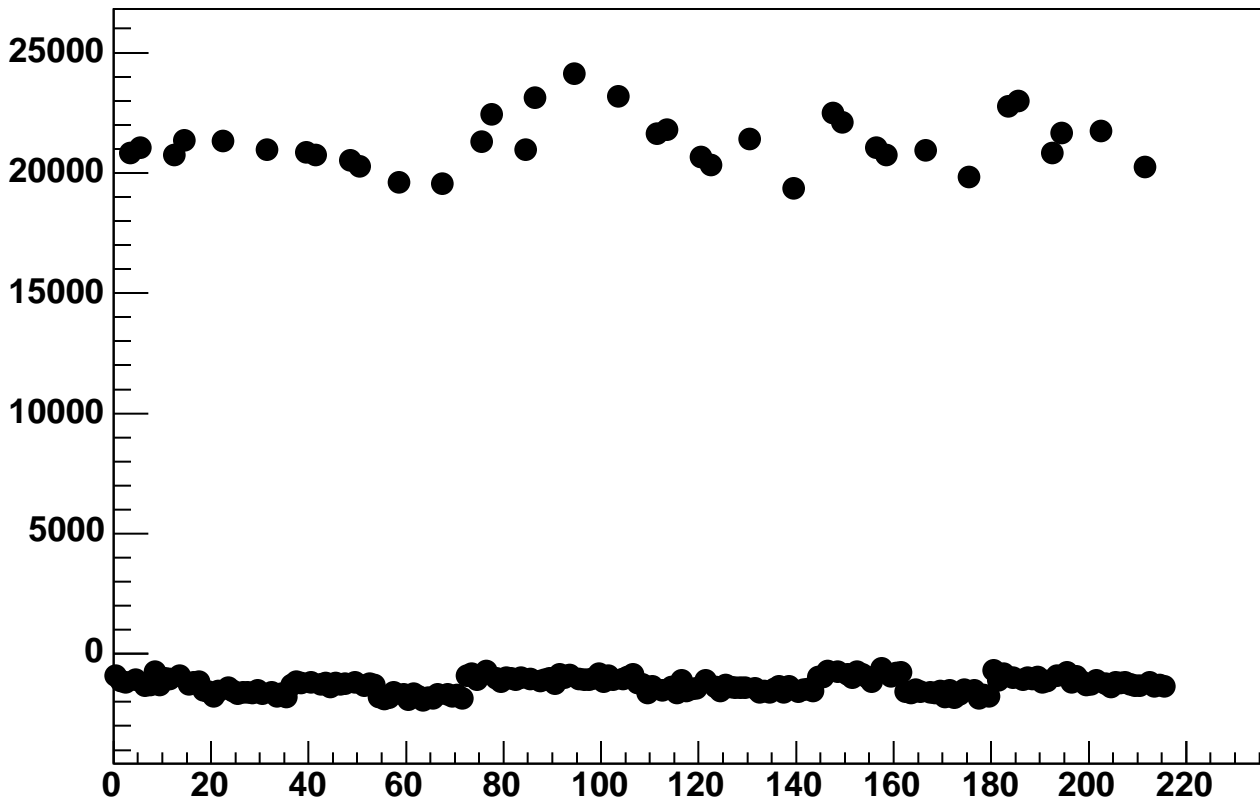


Enable 1, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan

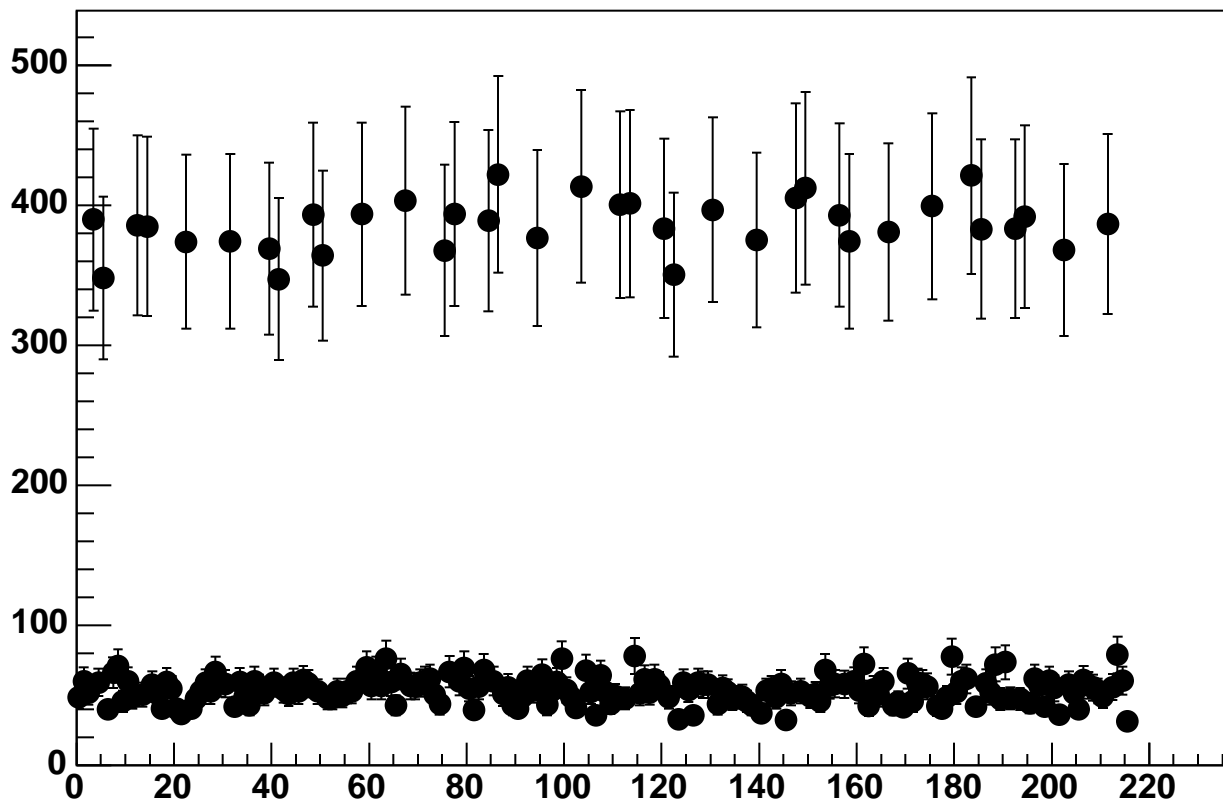




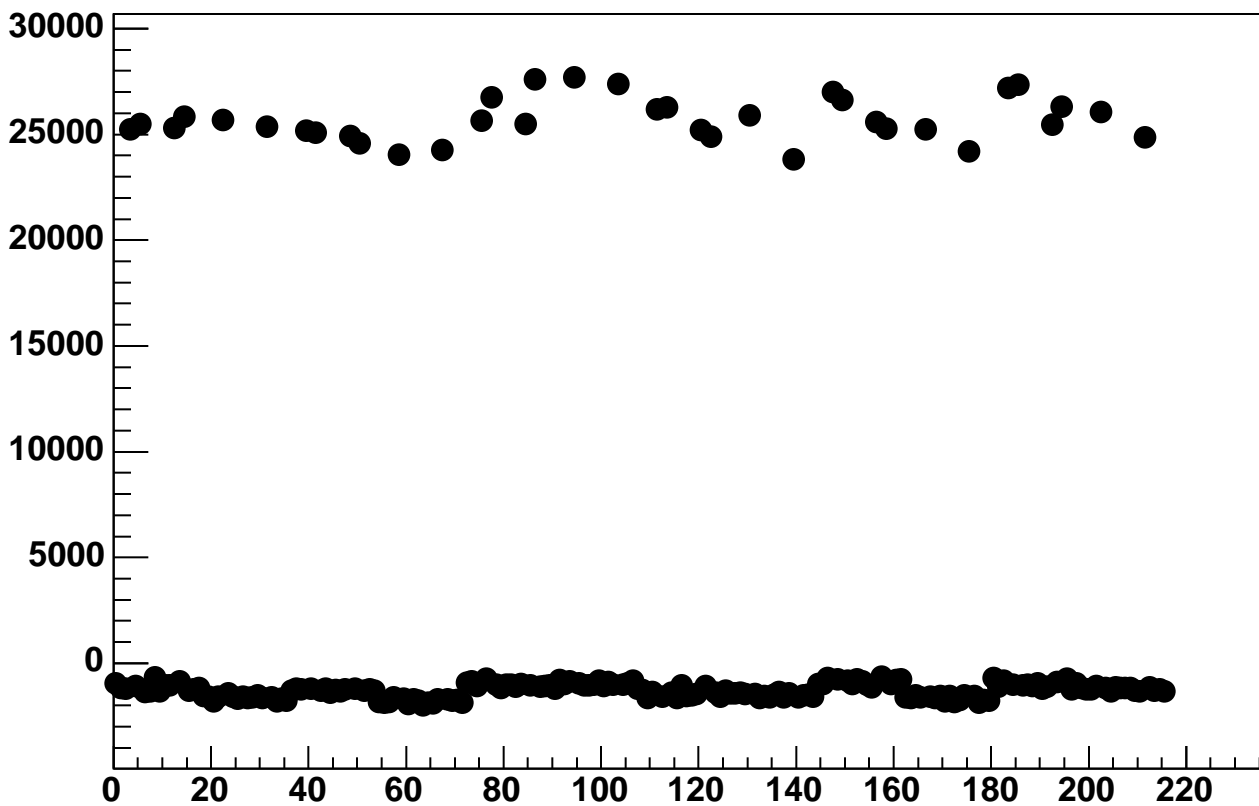
Enable 1, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



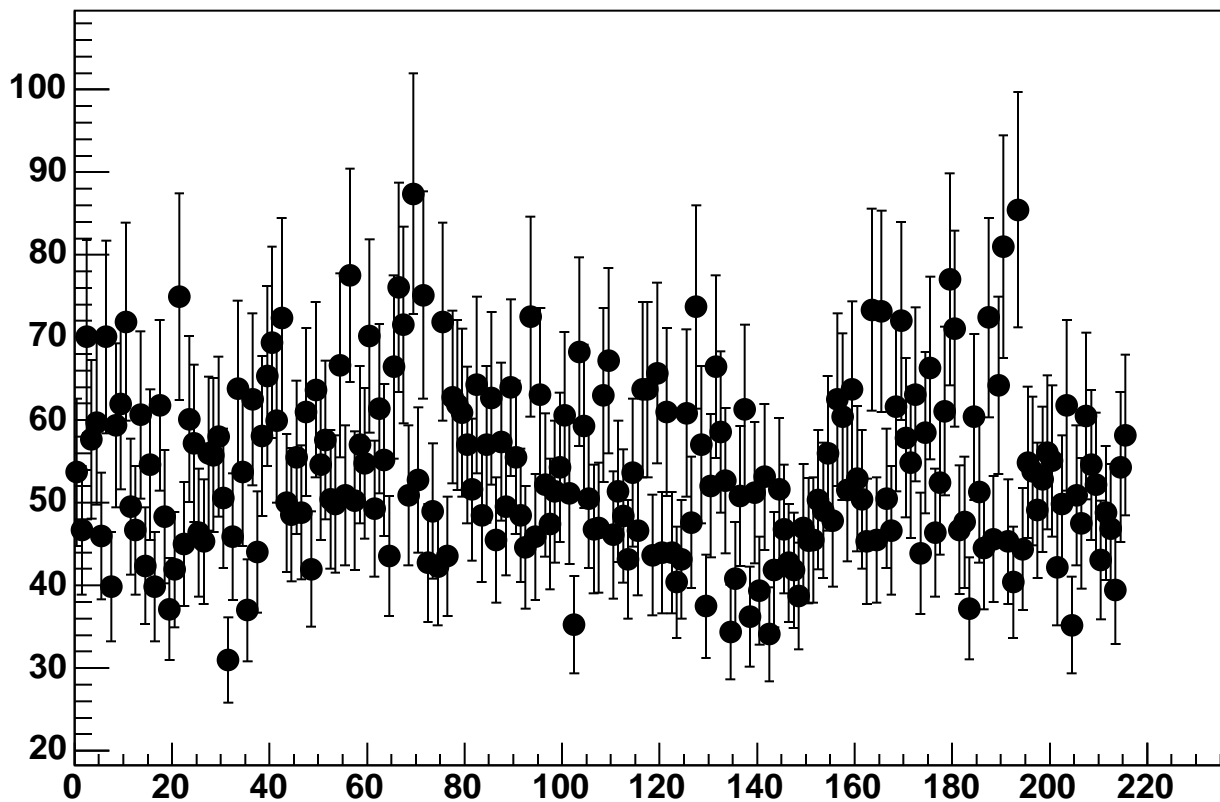
Enable 1, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



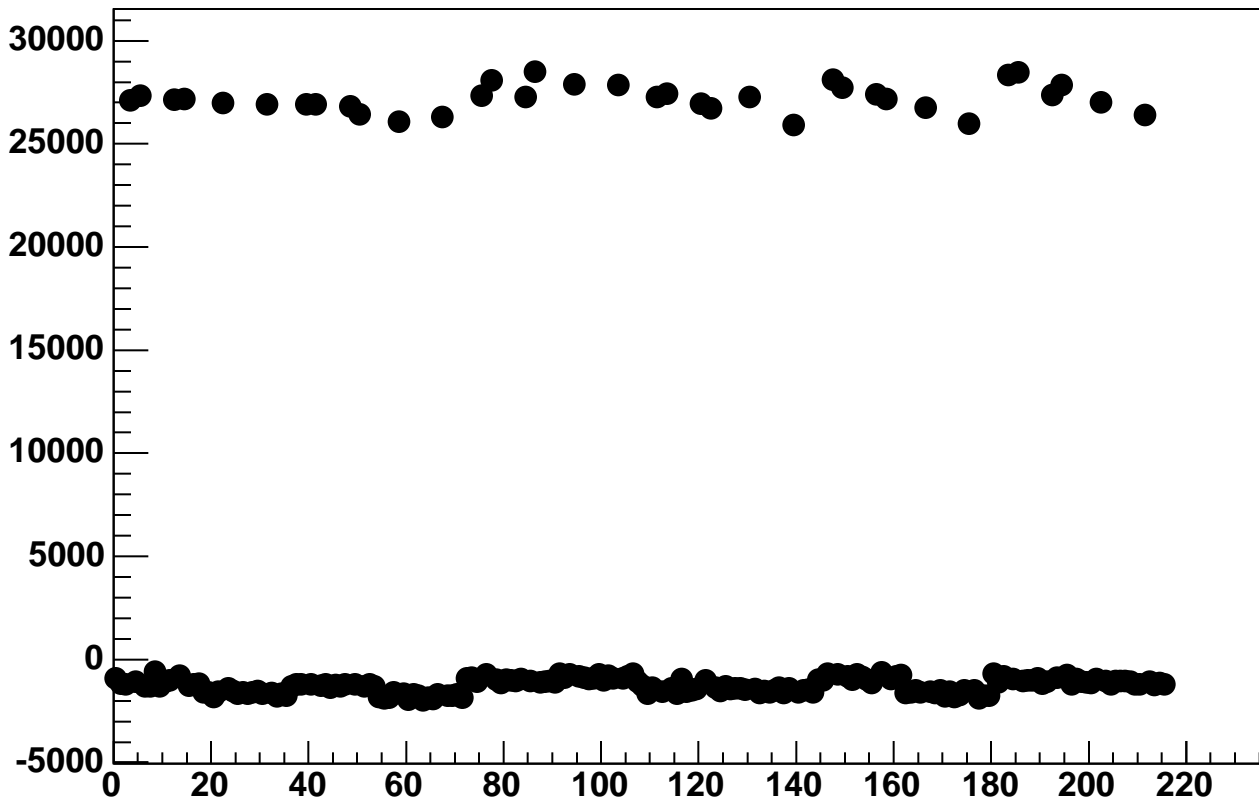
Enable 1, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan



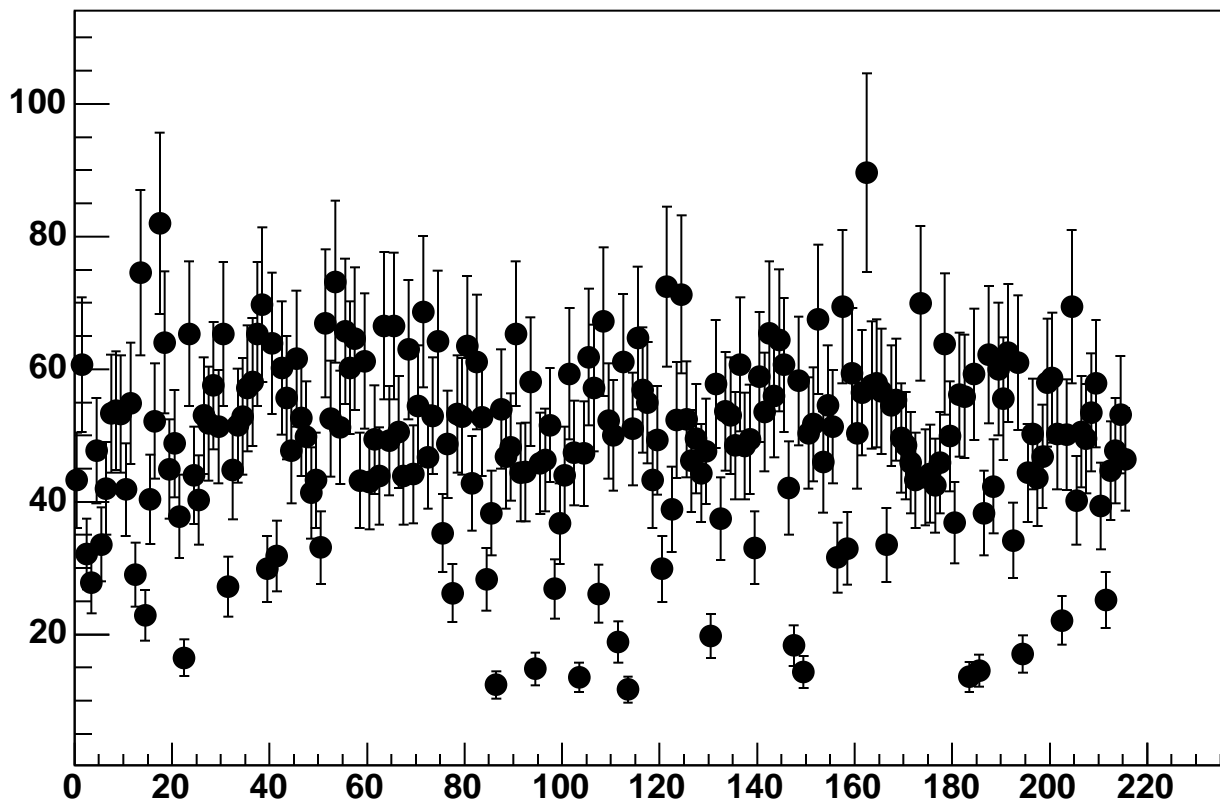
Enable 1, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan



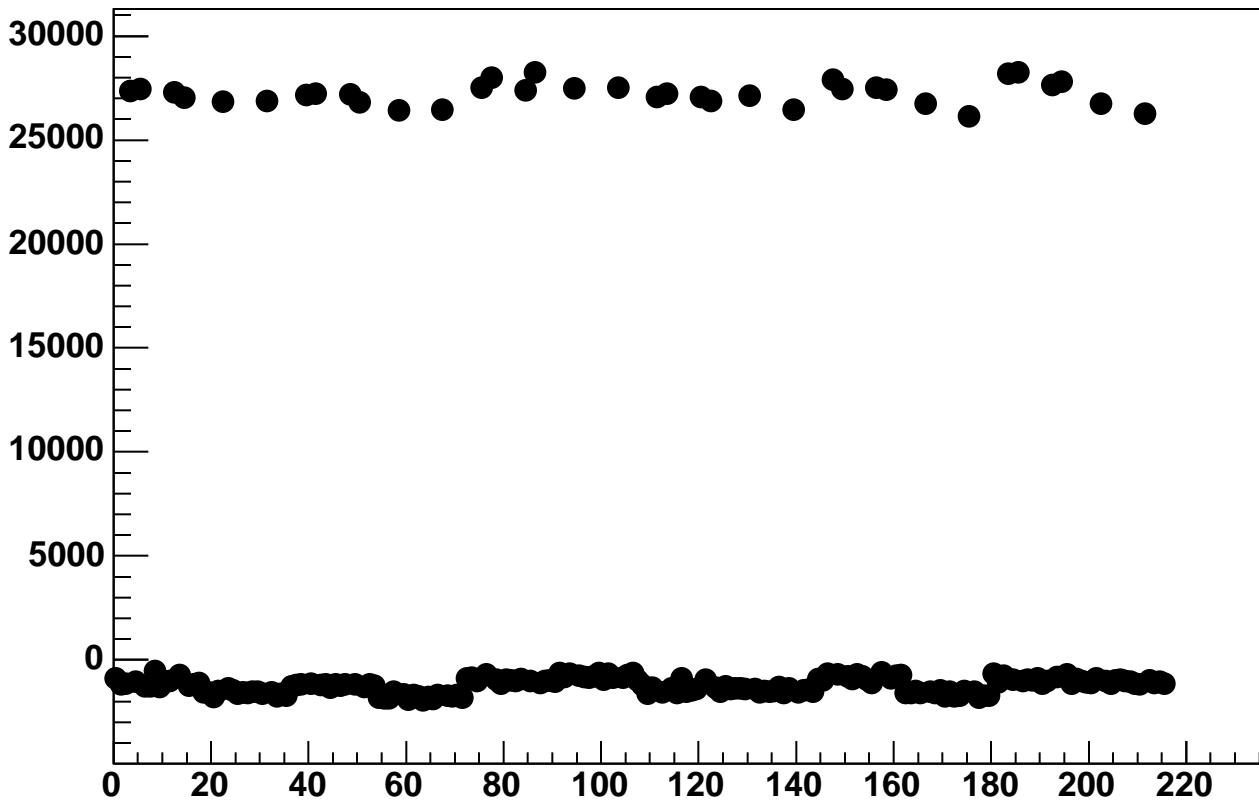
Enable 1, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



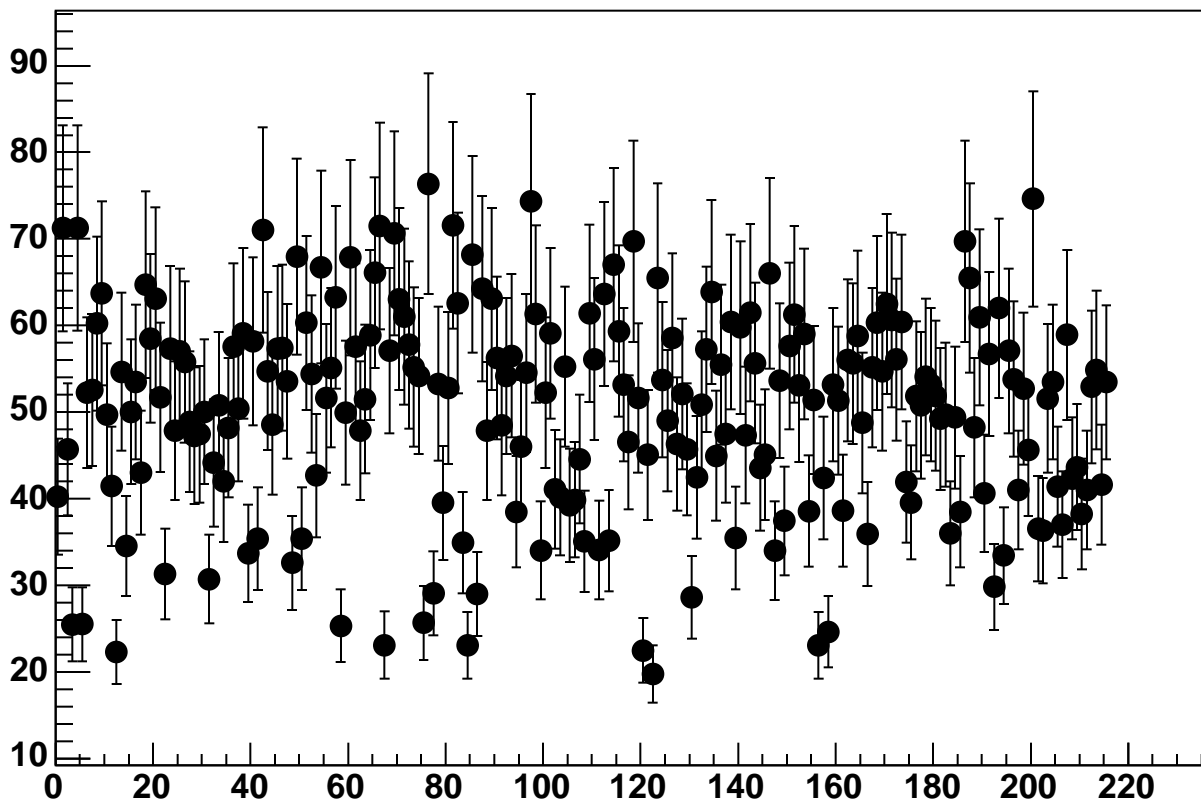
Enable 1, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



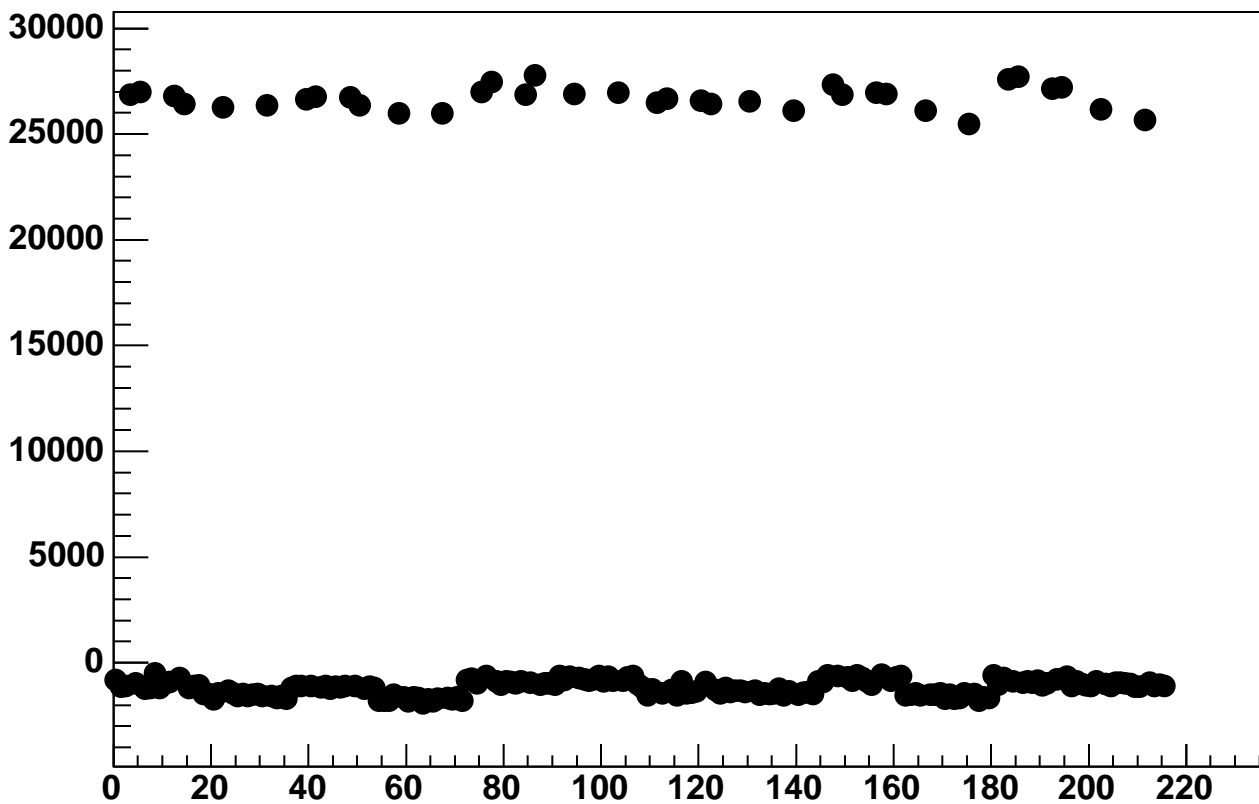
Enable 1, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan



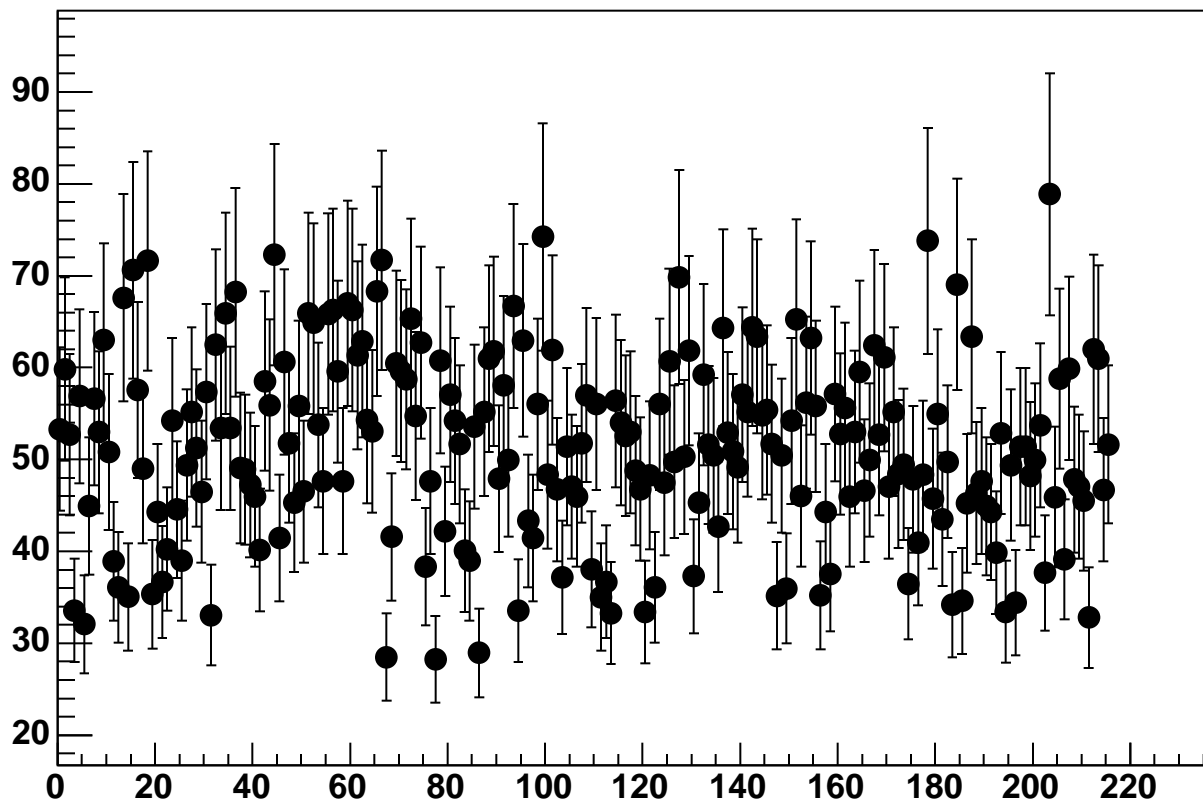
Enable 1, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan



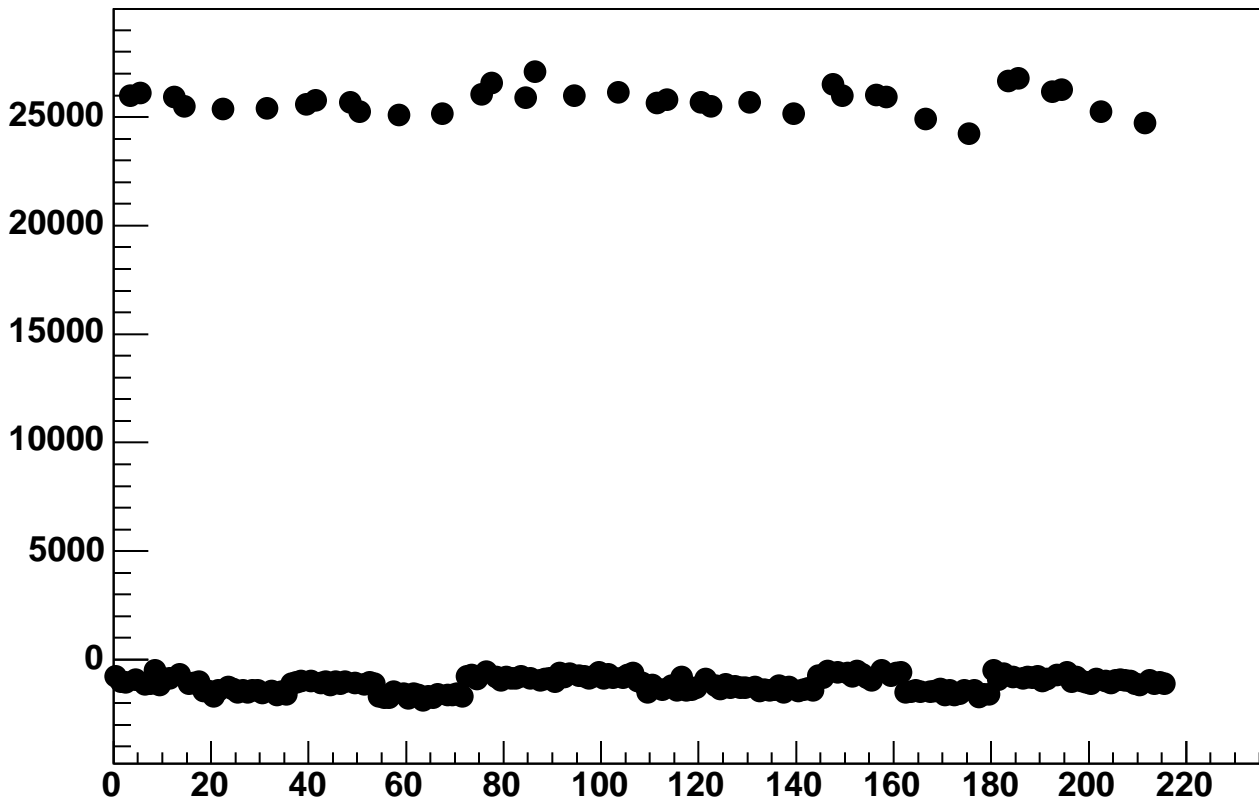
Enable 1, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



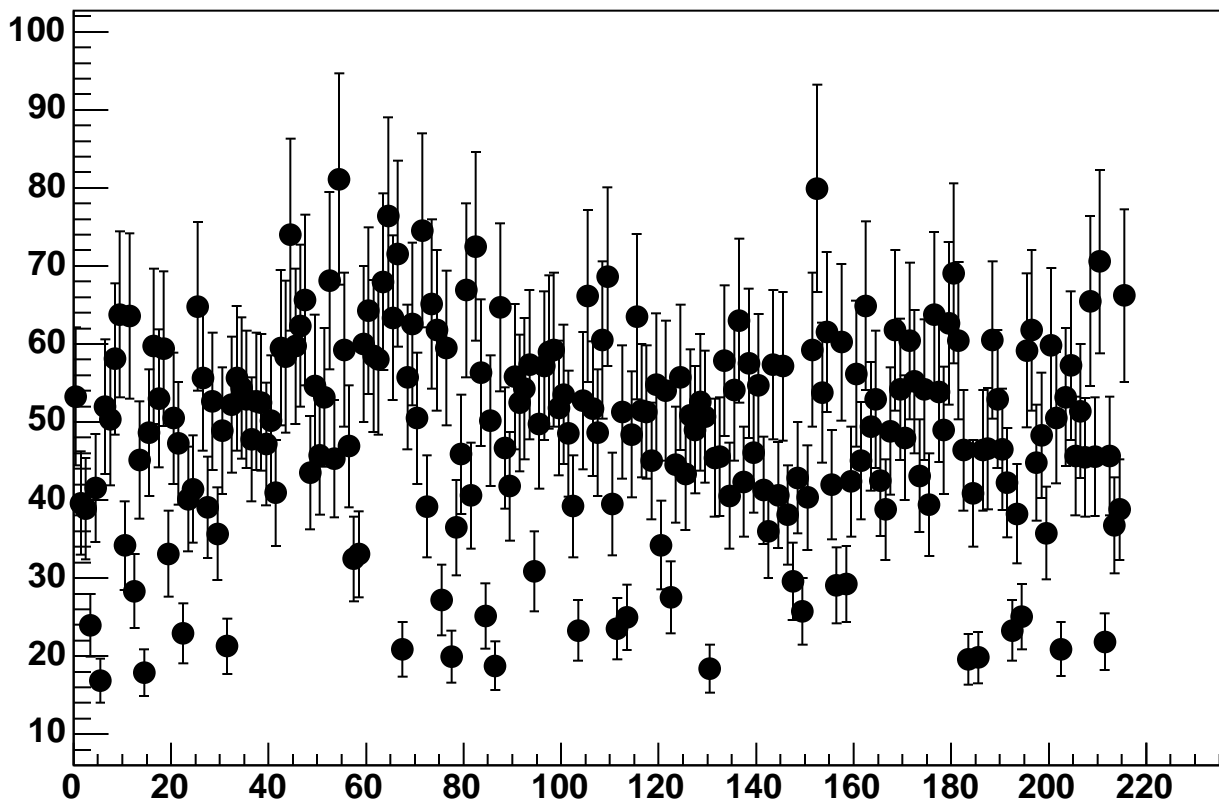
Enable 1, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



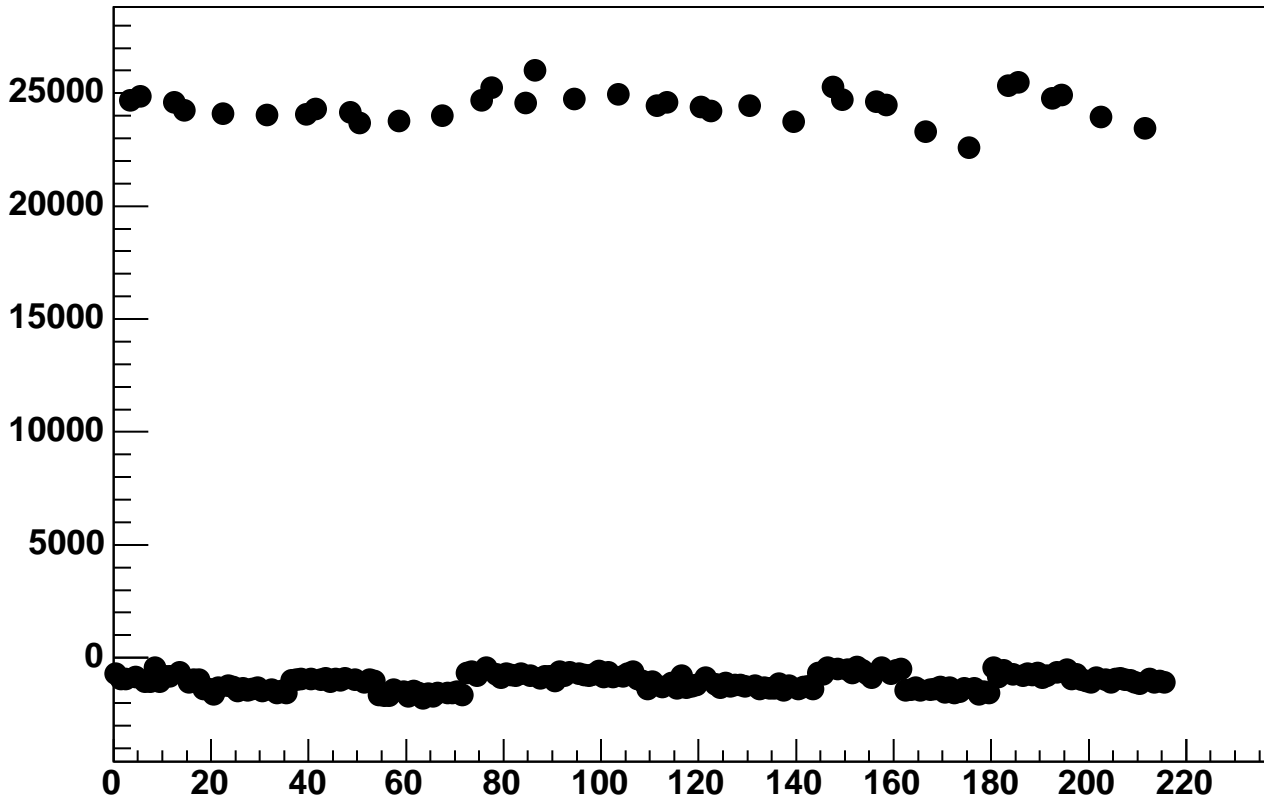
Enable 1, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan



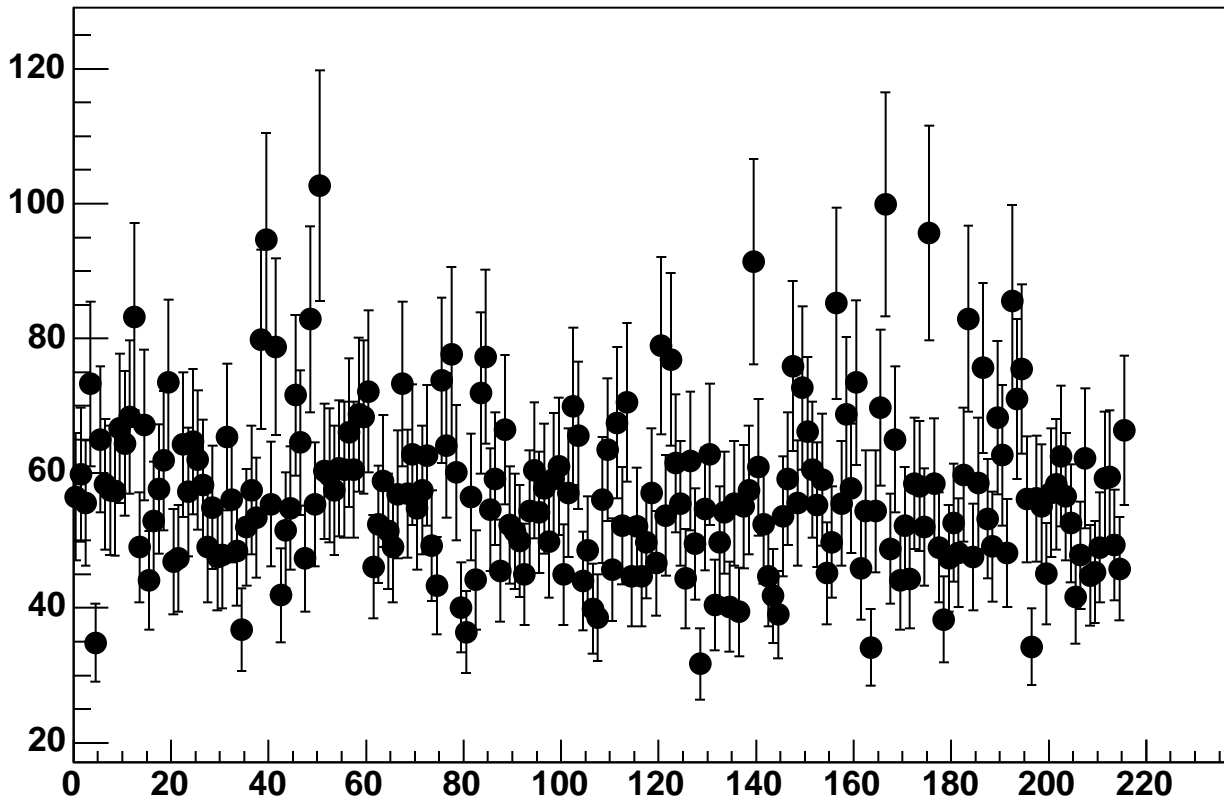
Enable 1, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan



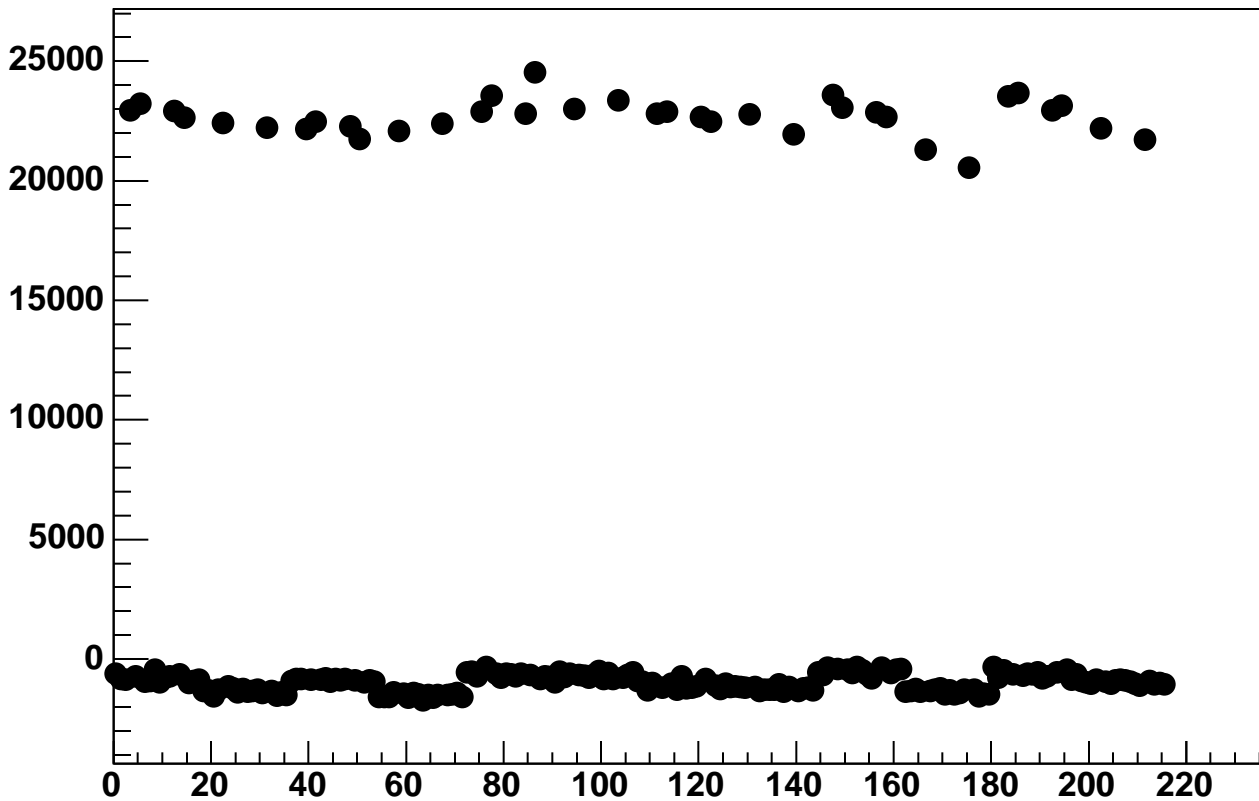
Enable 1, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



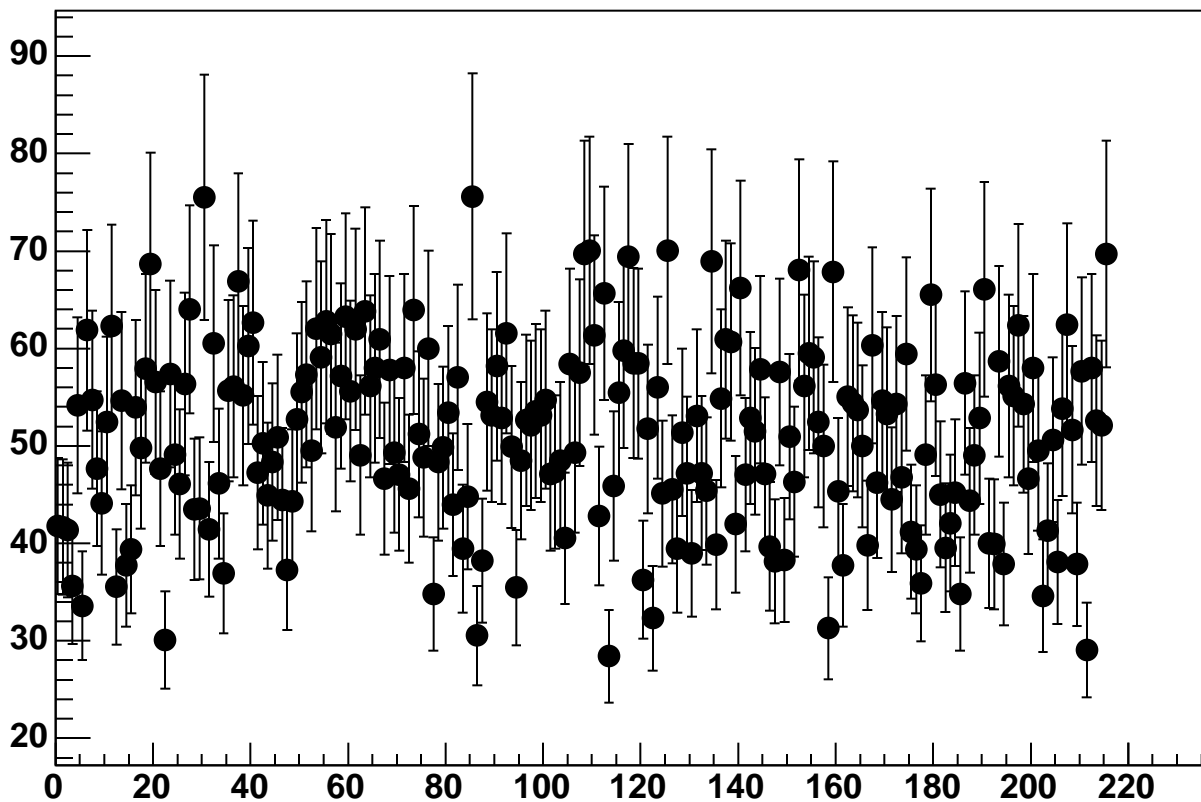
Enable 1, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan

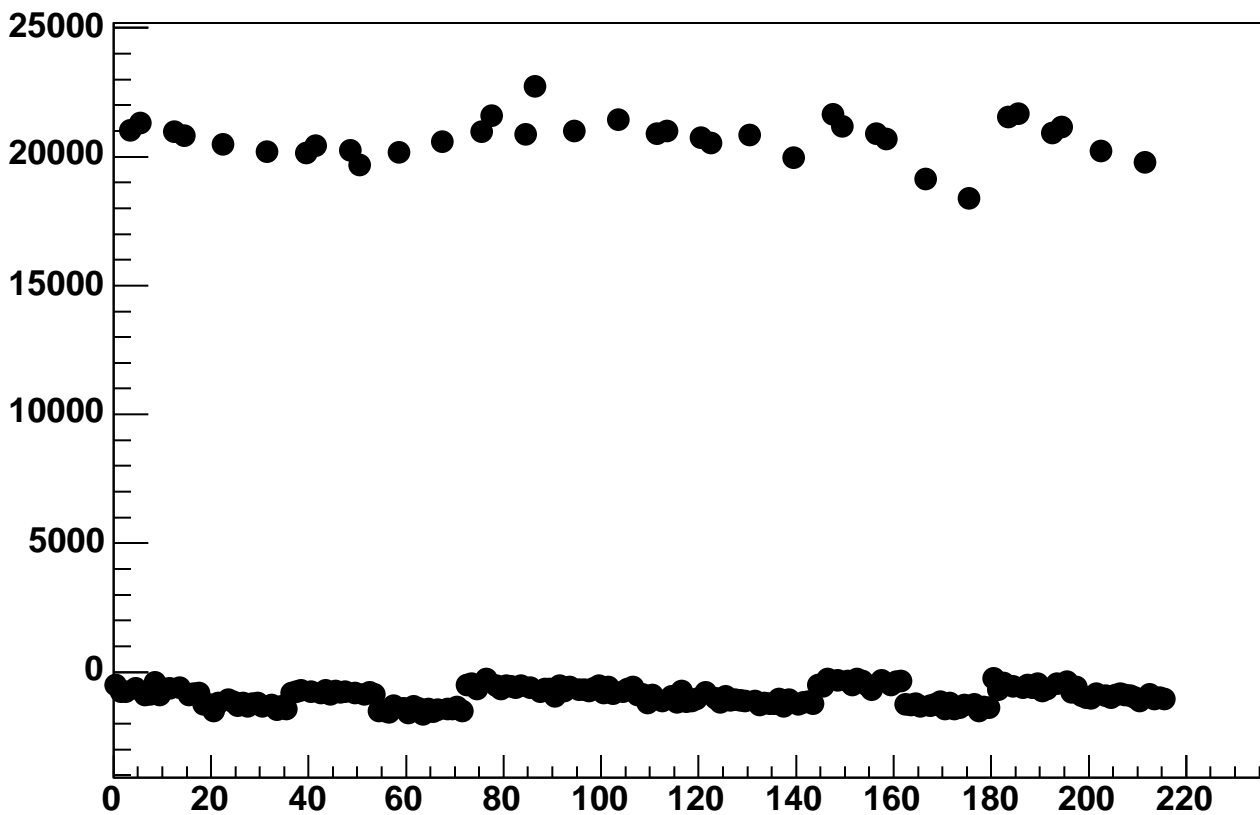


Enable 1, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan

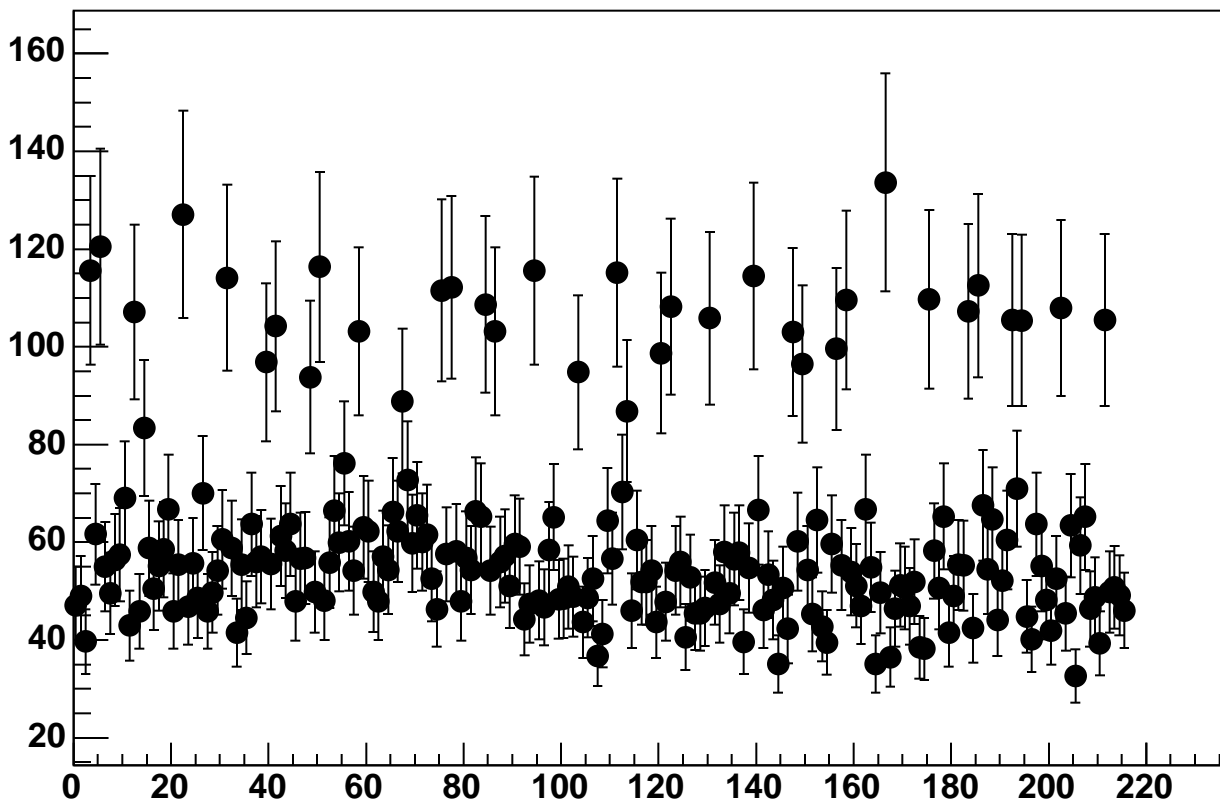




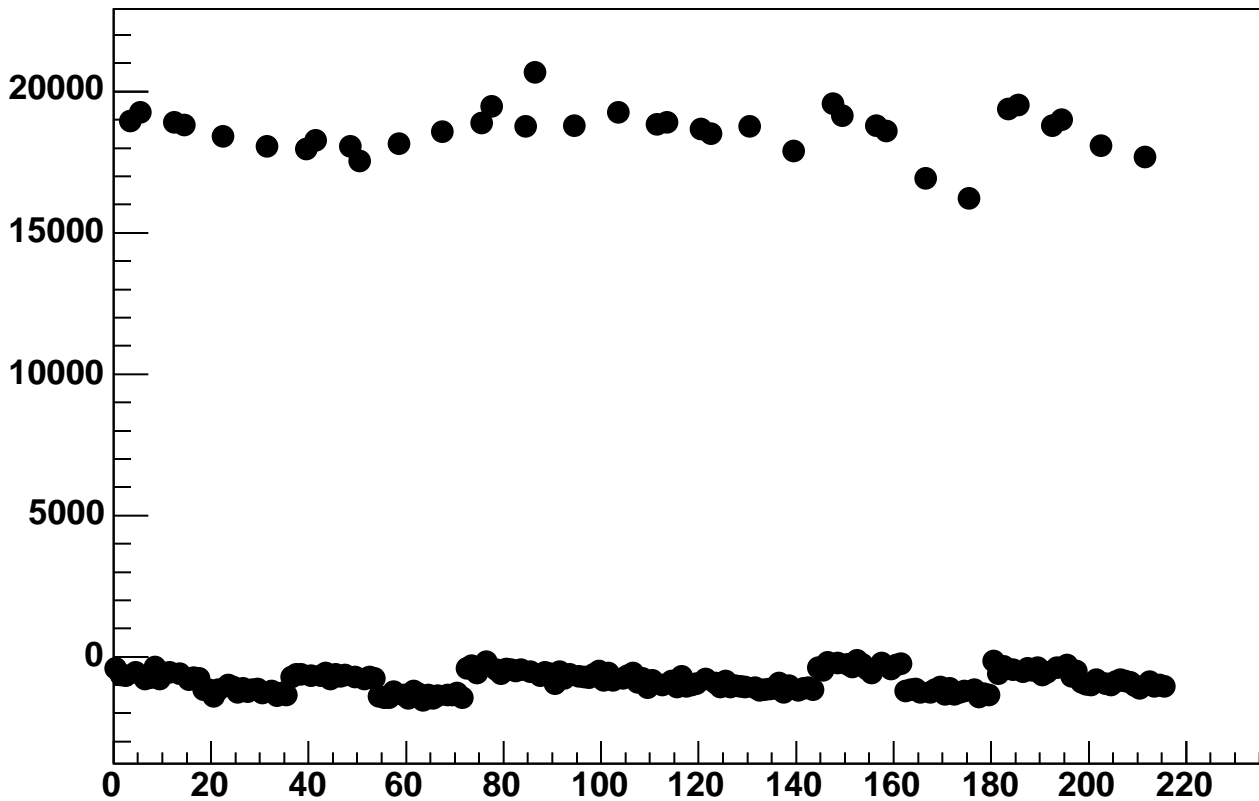
Enable 1, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



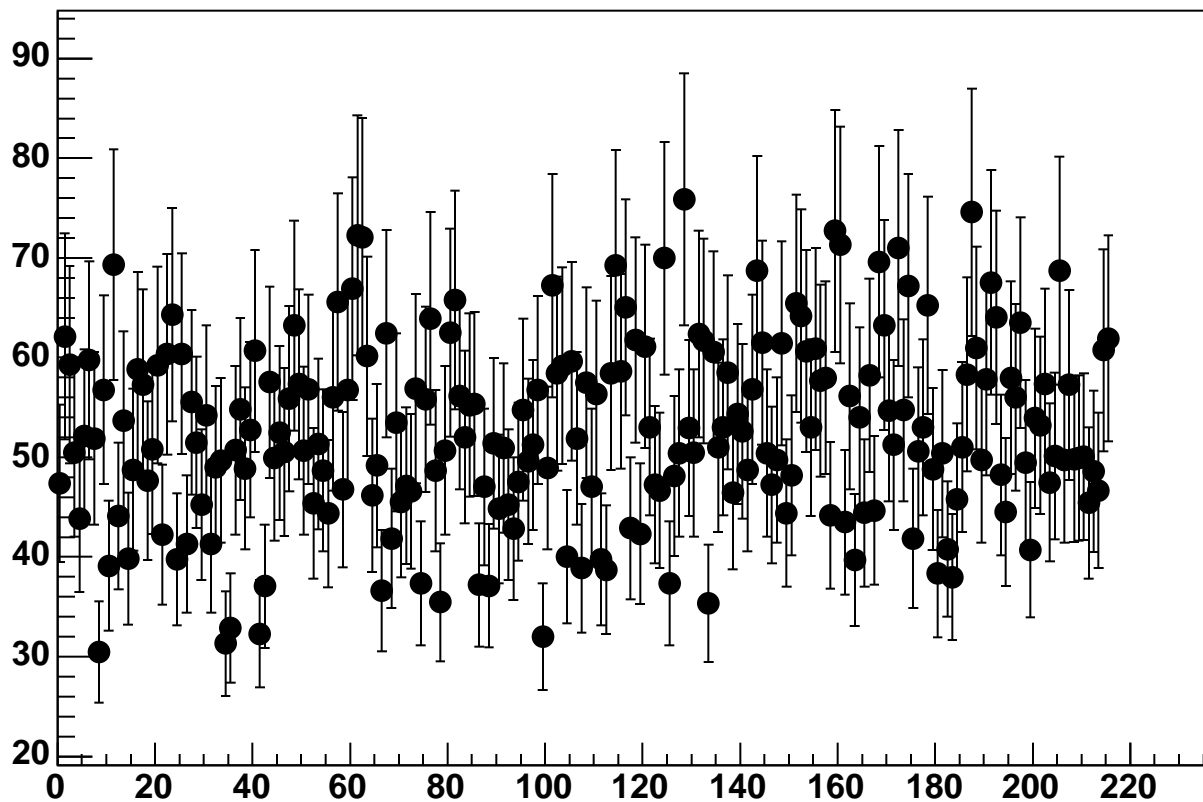
Enable 1, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



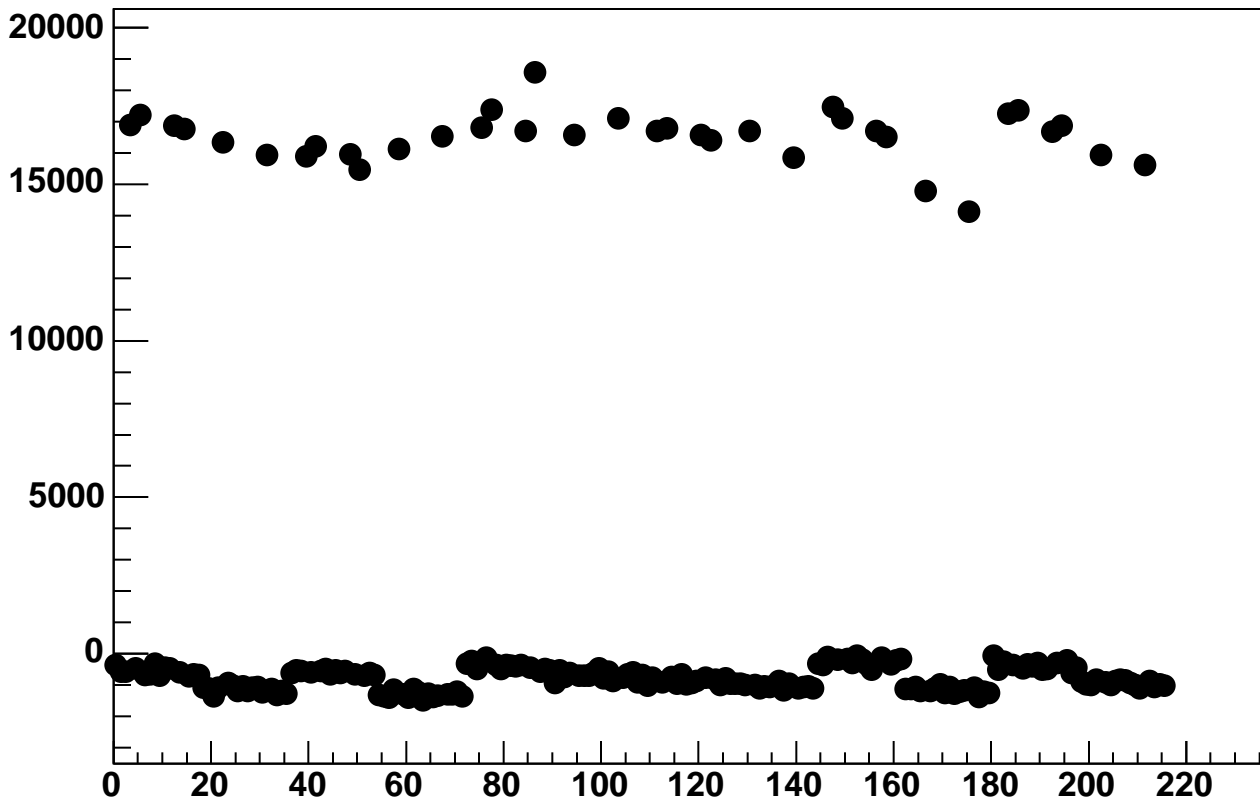
Enable 1, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan



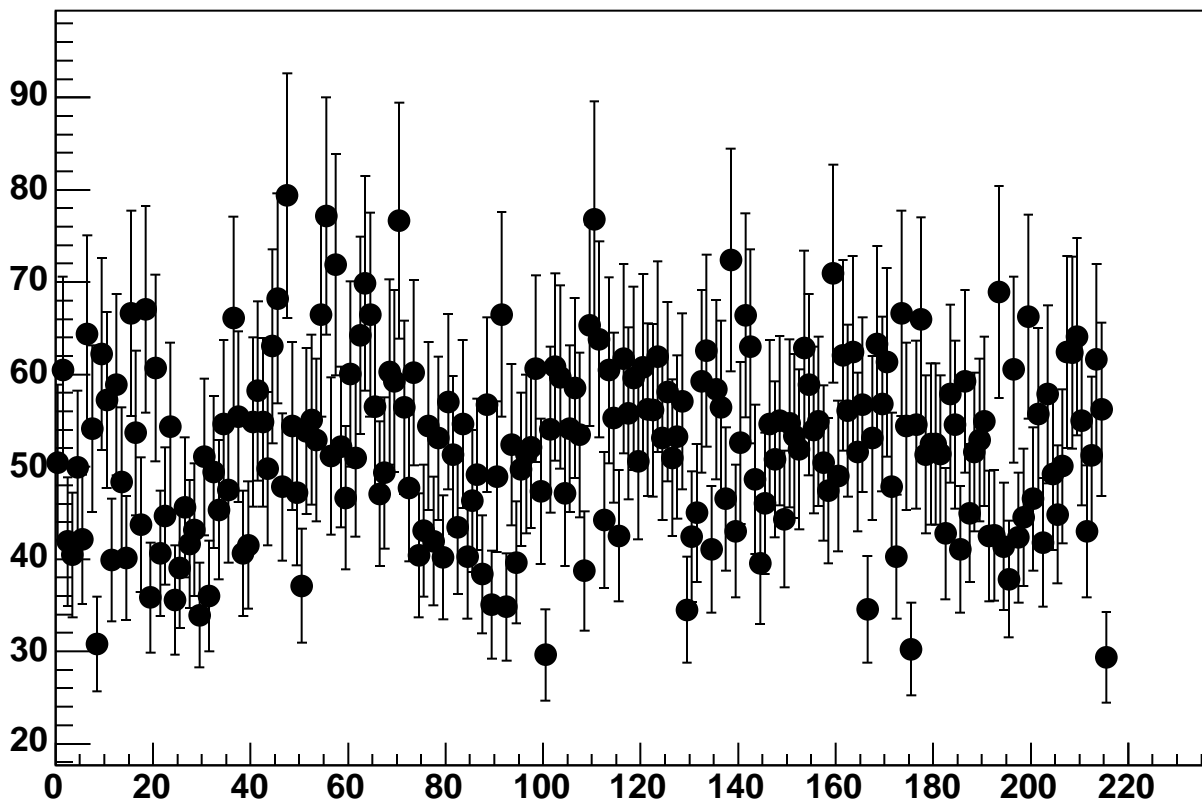
Enable 1, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan



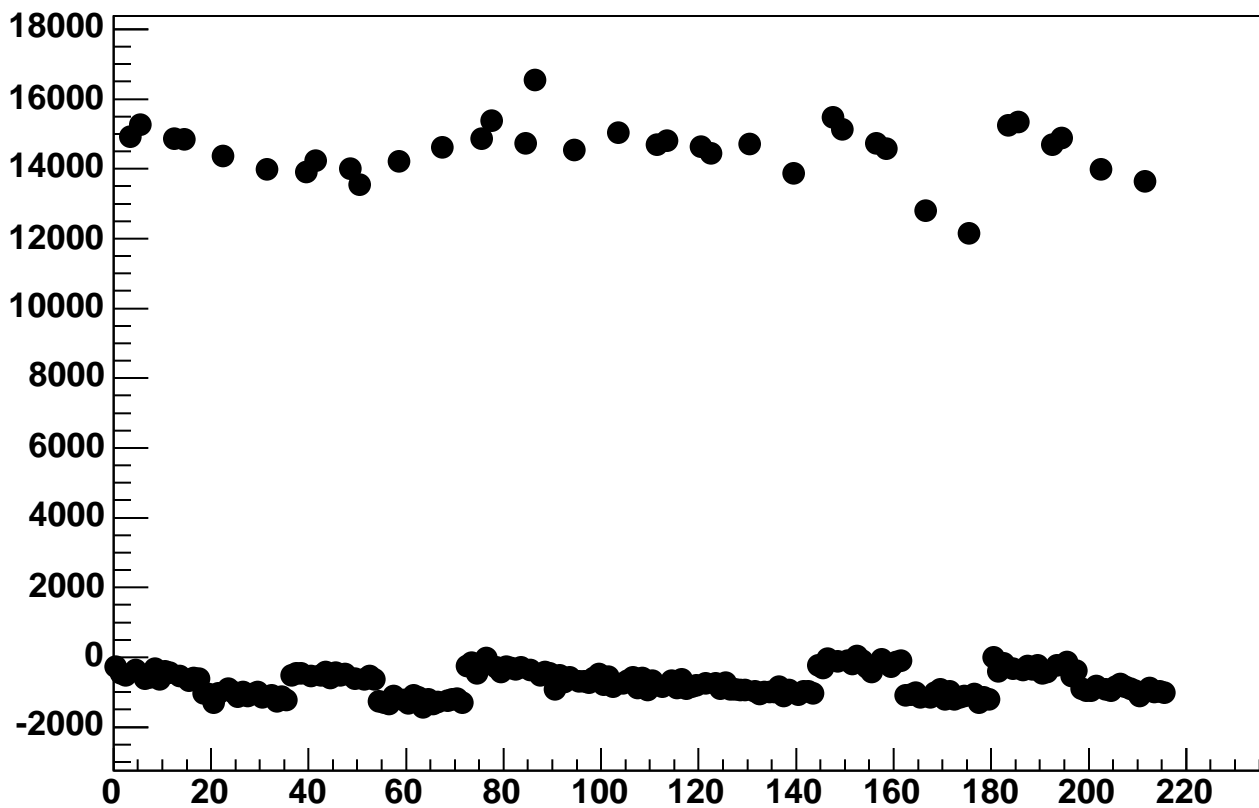
Enable 1, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



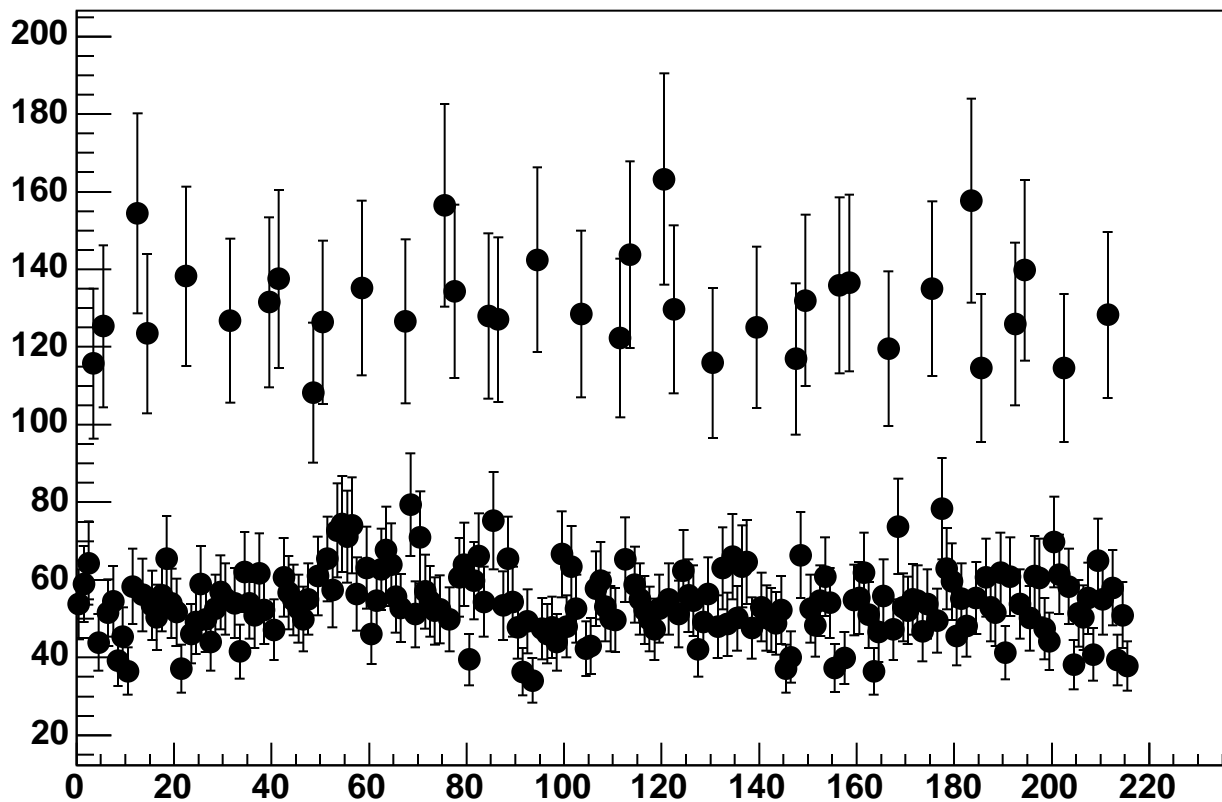
Enable 1, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



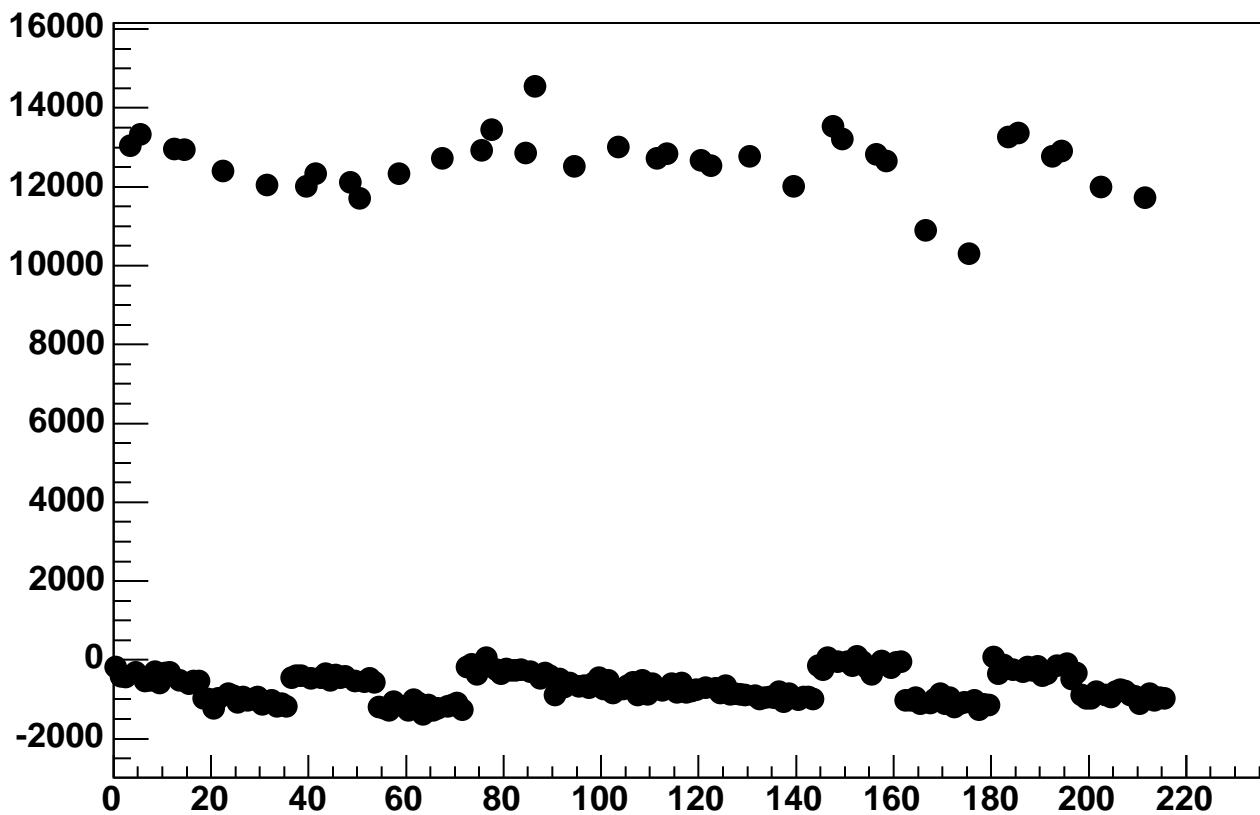
Enable 1, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan



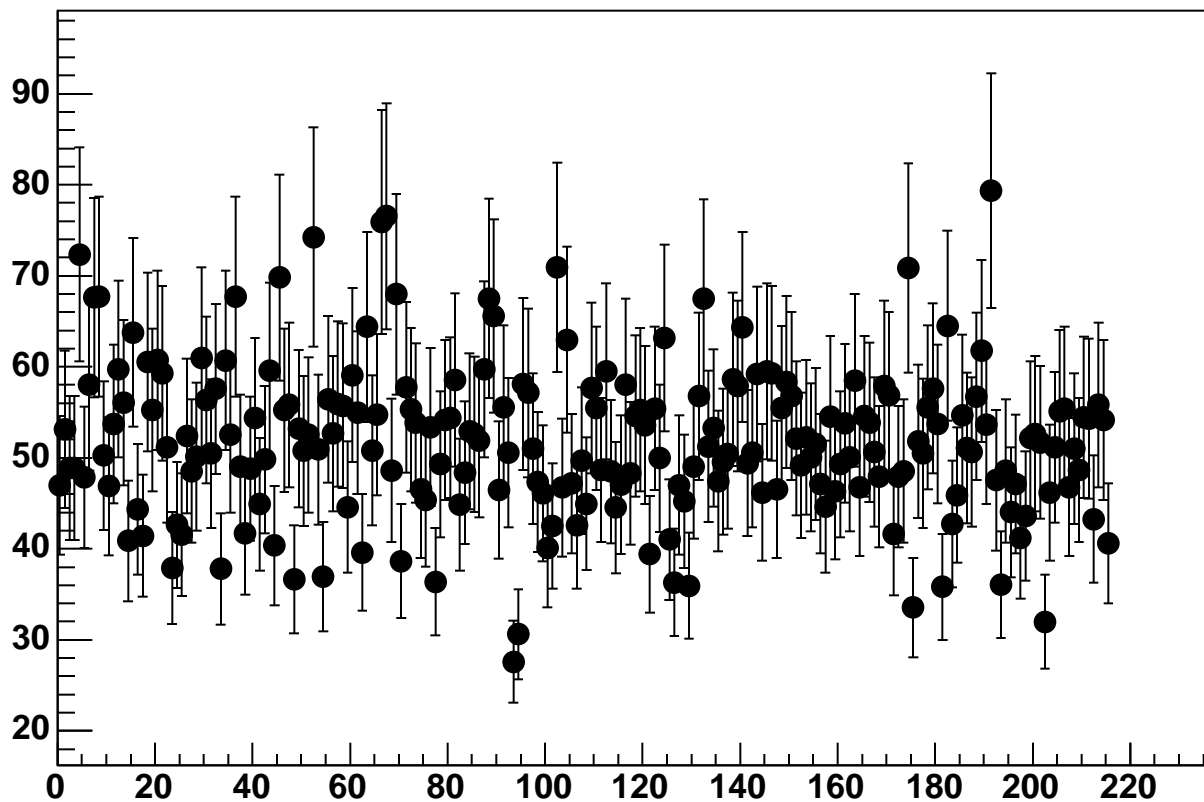
Enable 1, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan



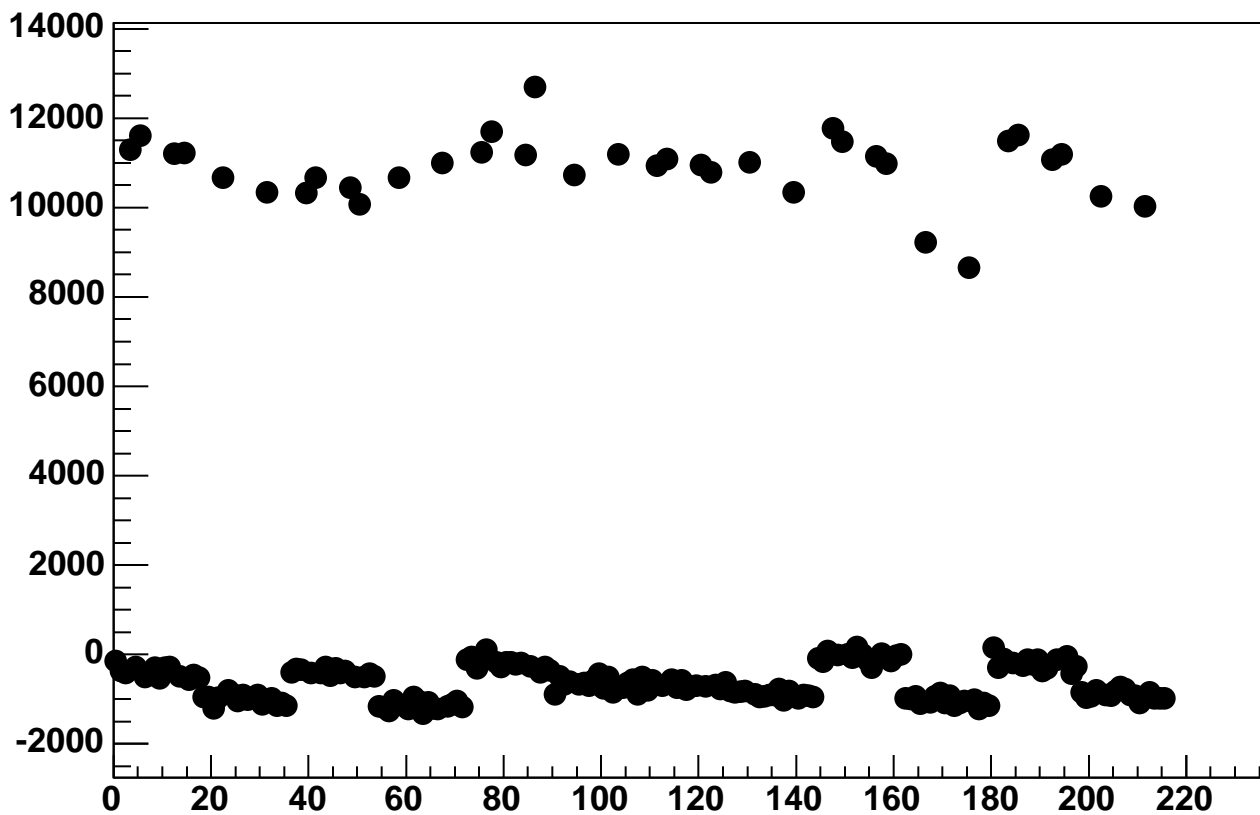
Enable 1, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



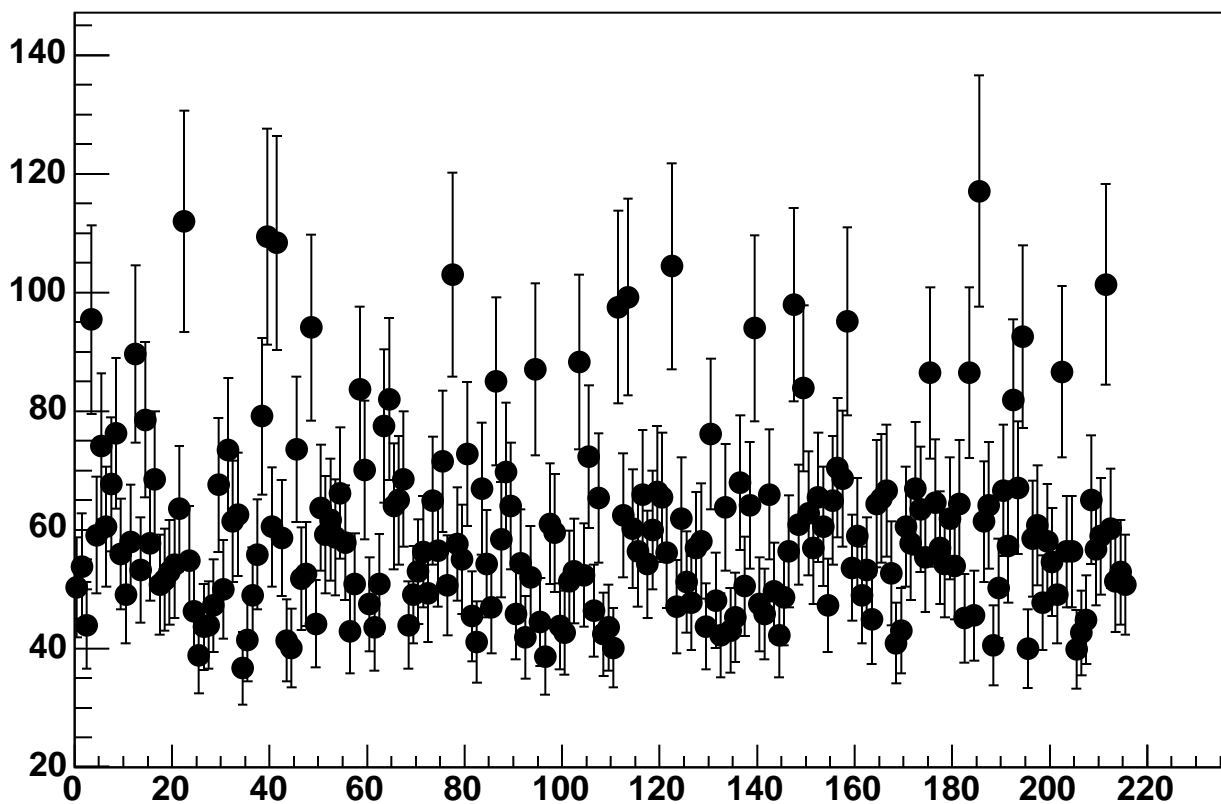
Enable 1, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



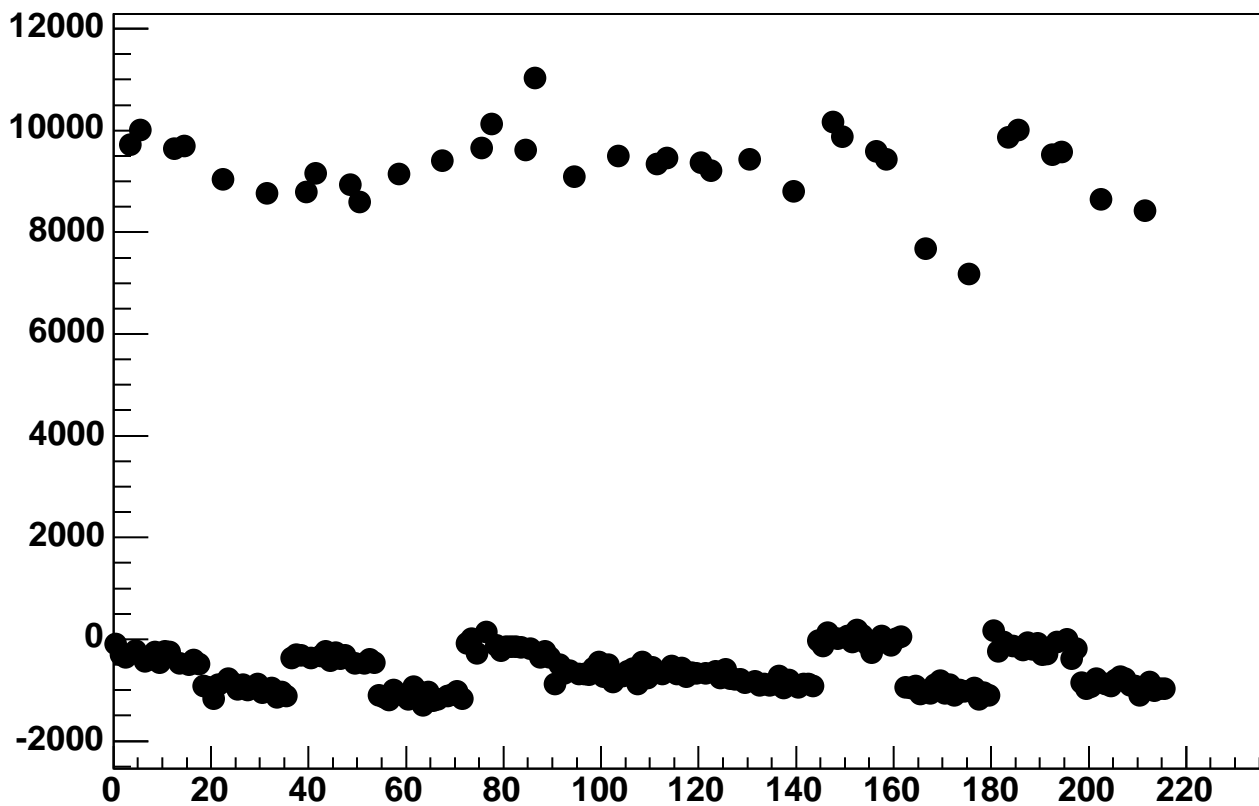
Enable 1, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan



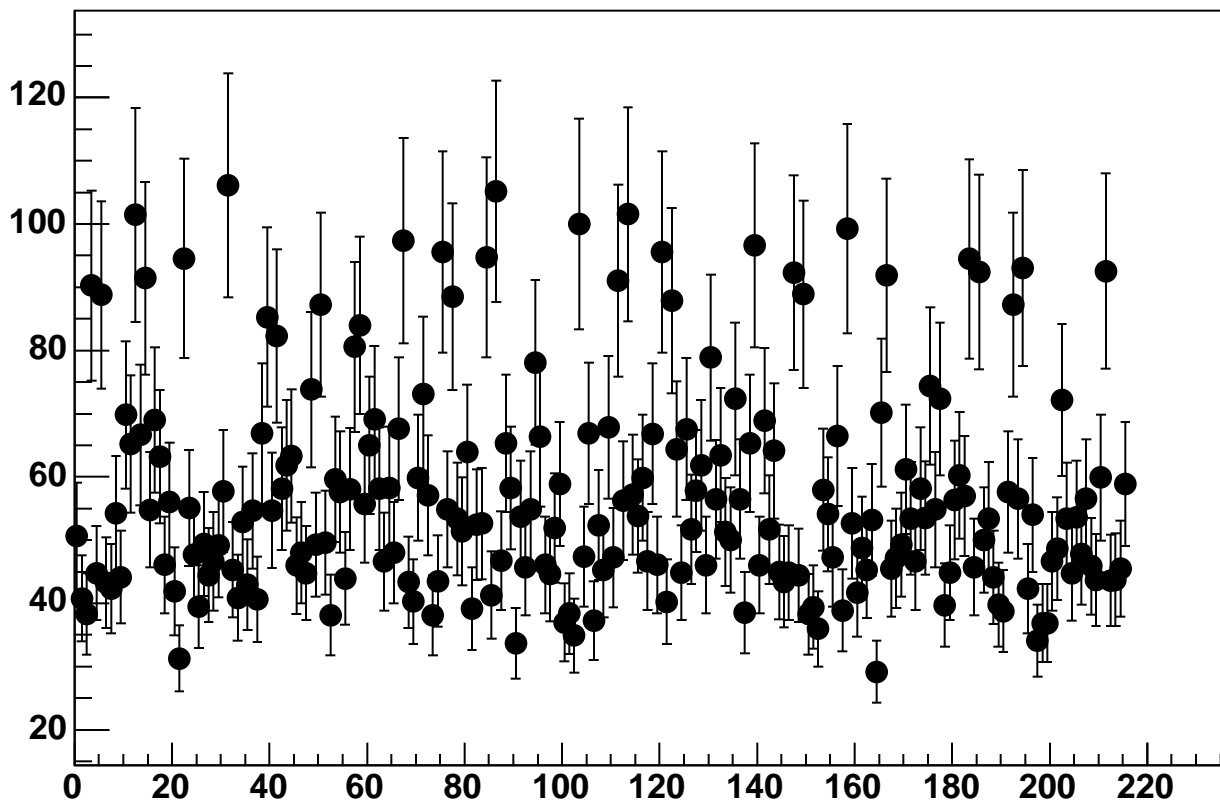
Enable 1, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan



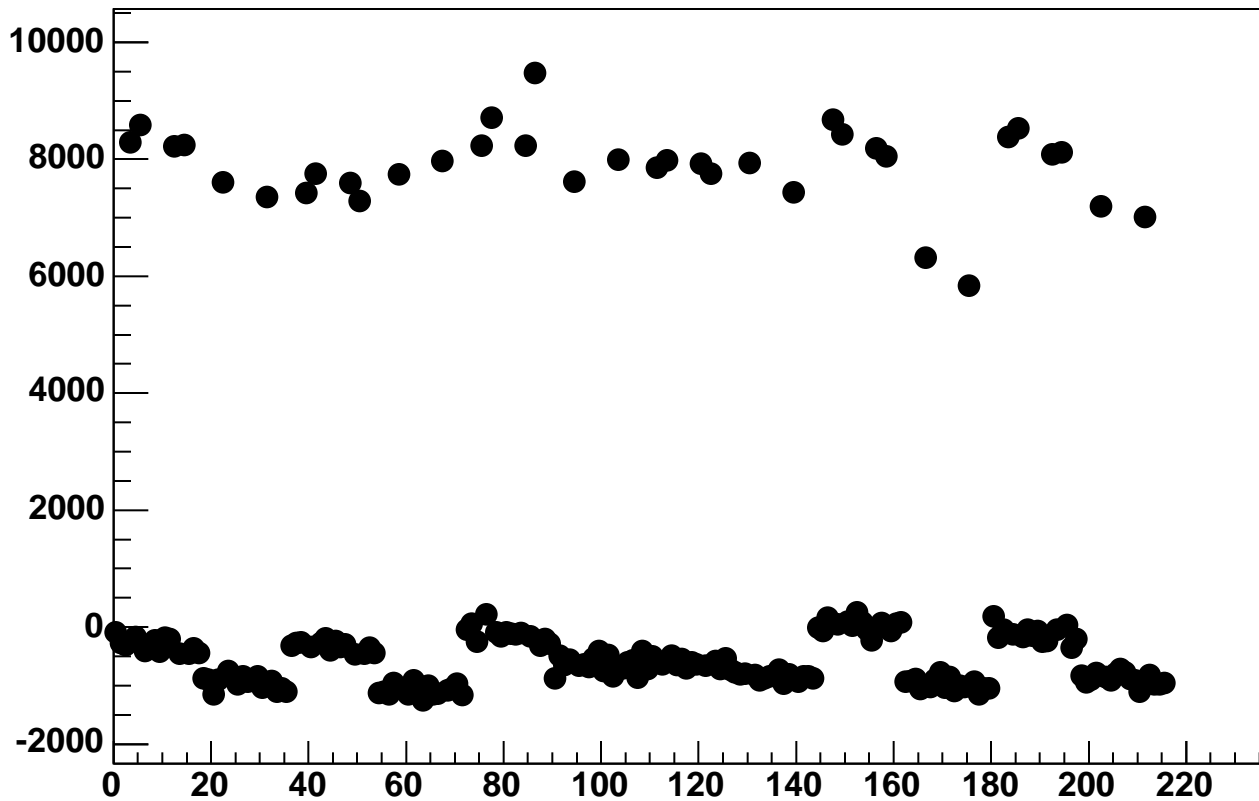
Enable 1, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



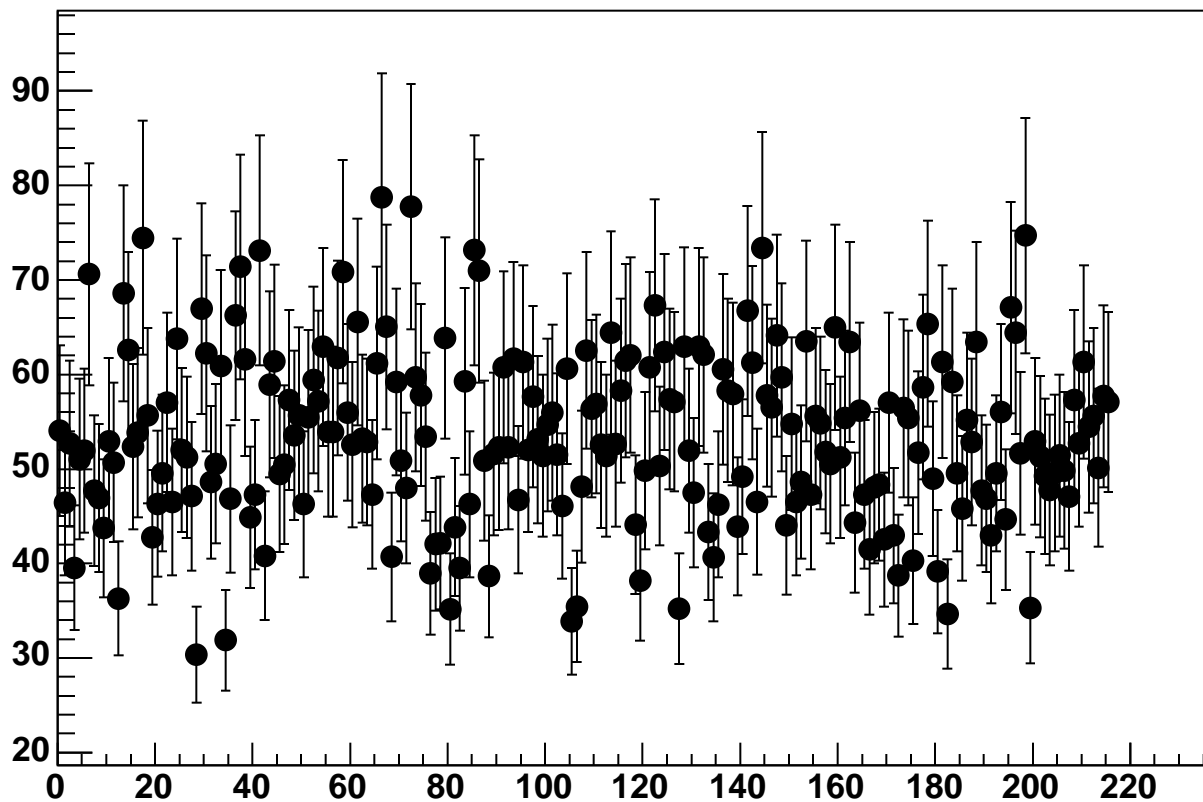
Enable 1, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan

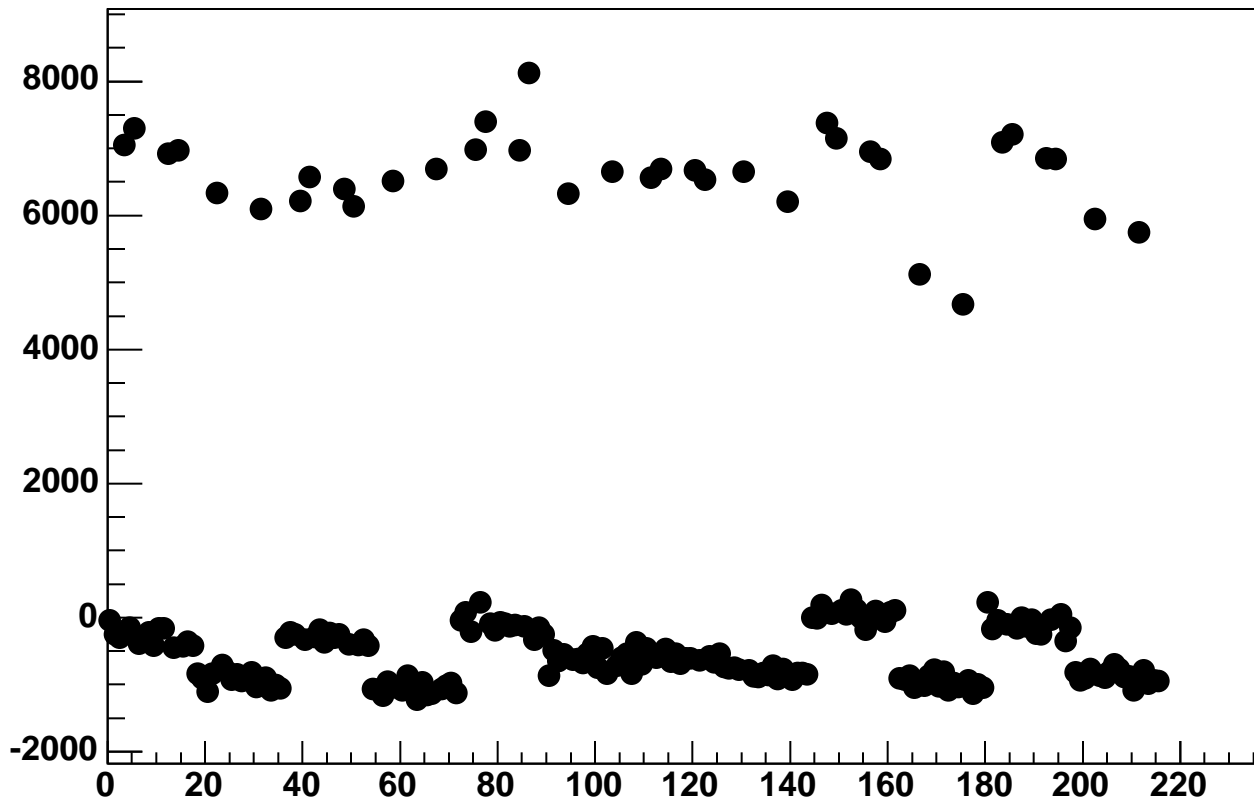


Enable 1, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan

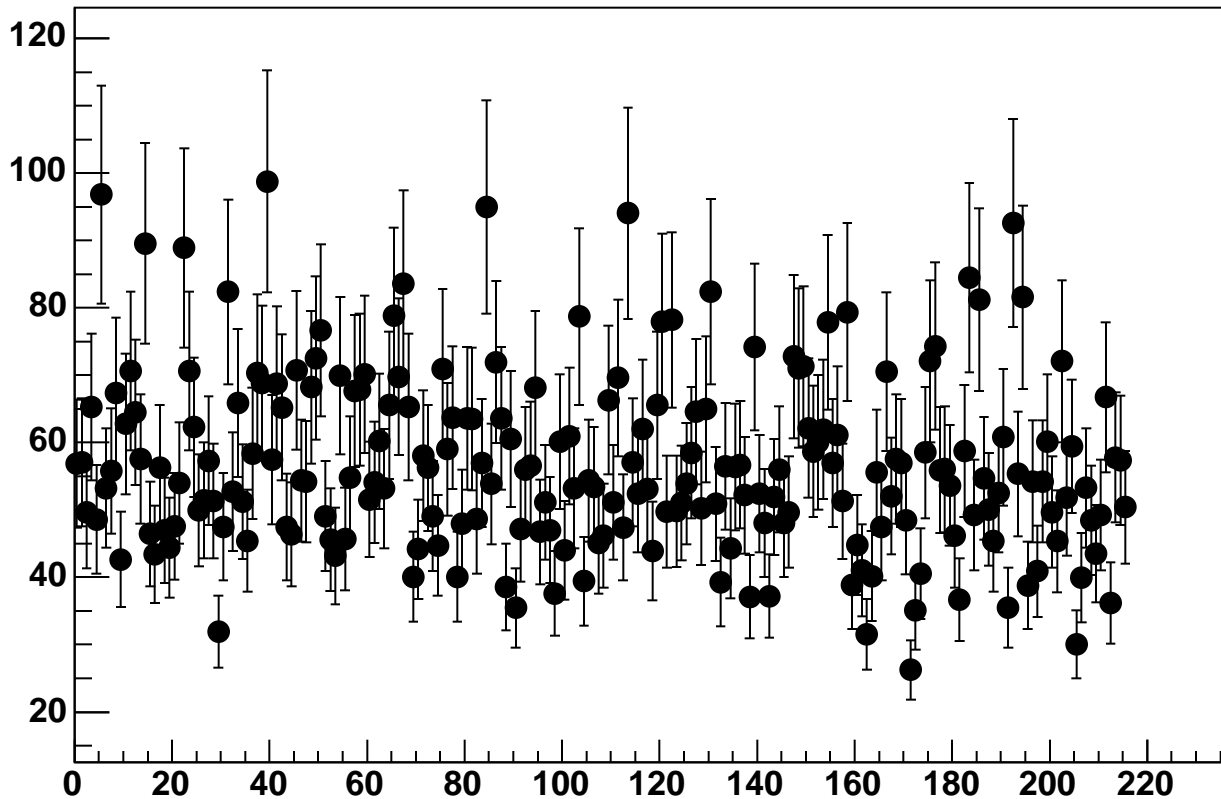




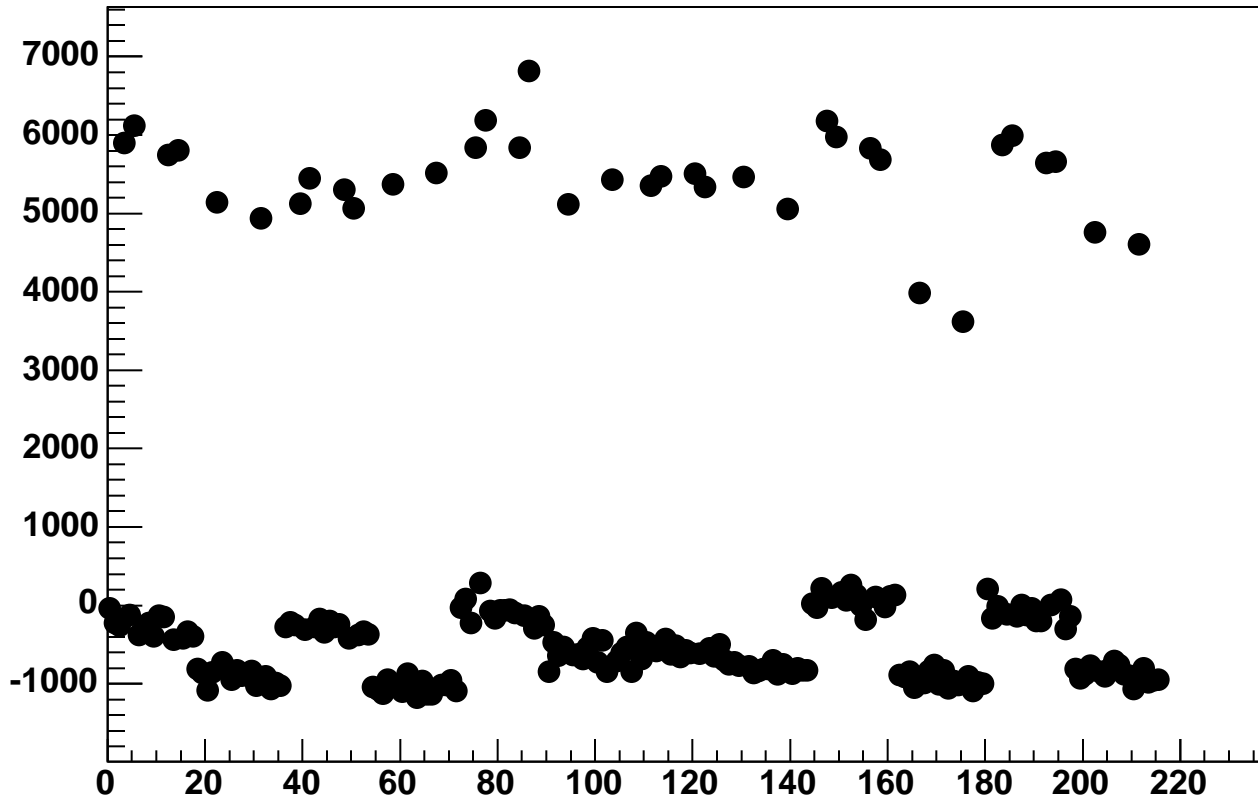
Enable 1, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



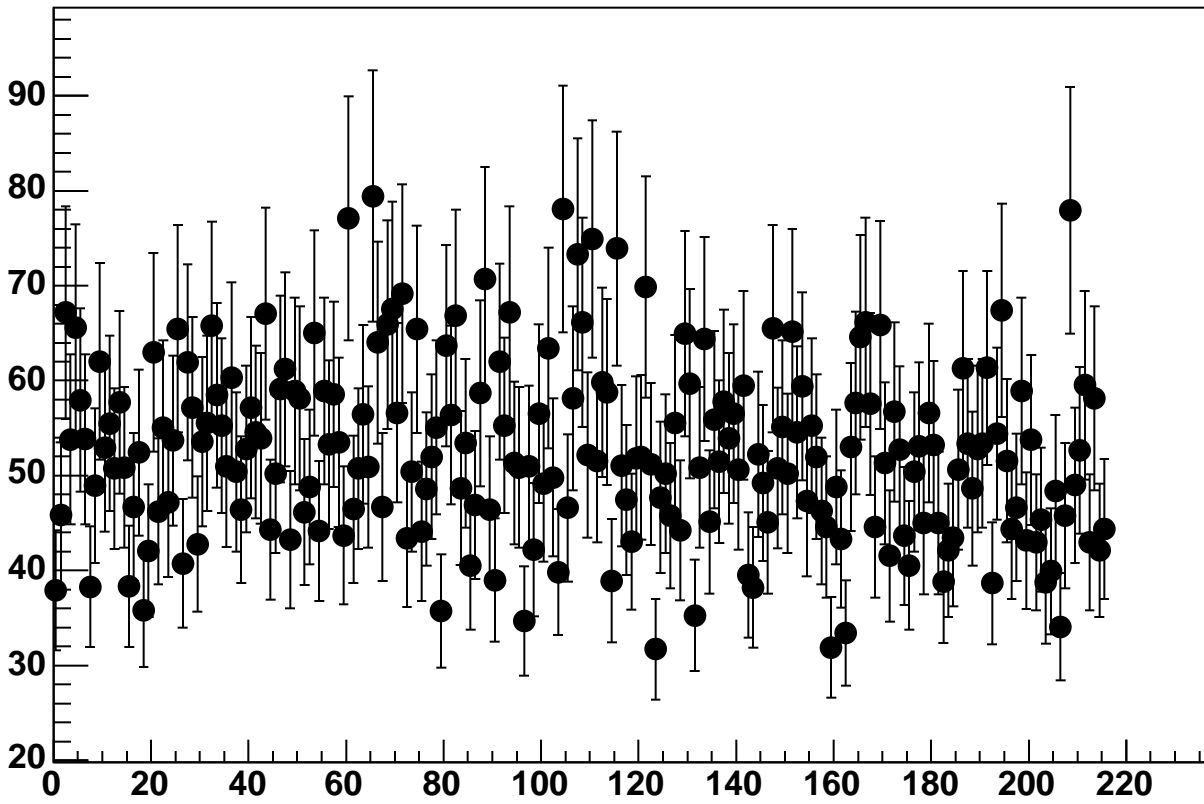
Enable 1, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



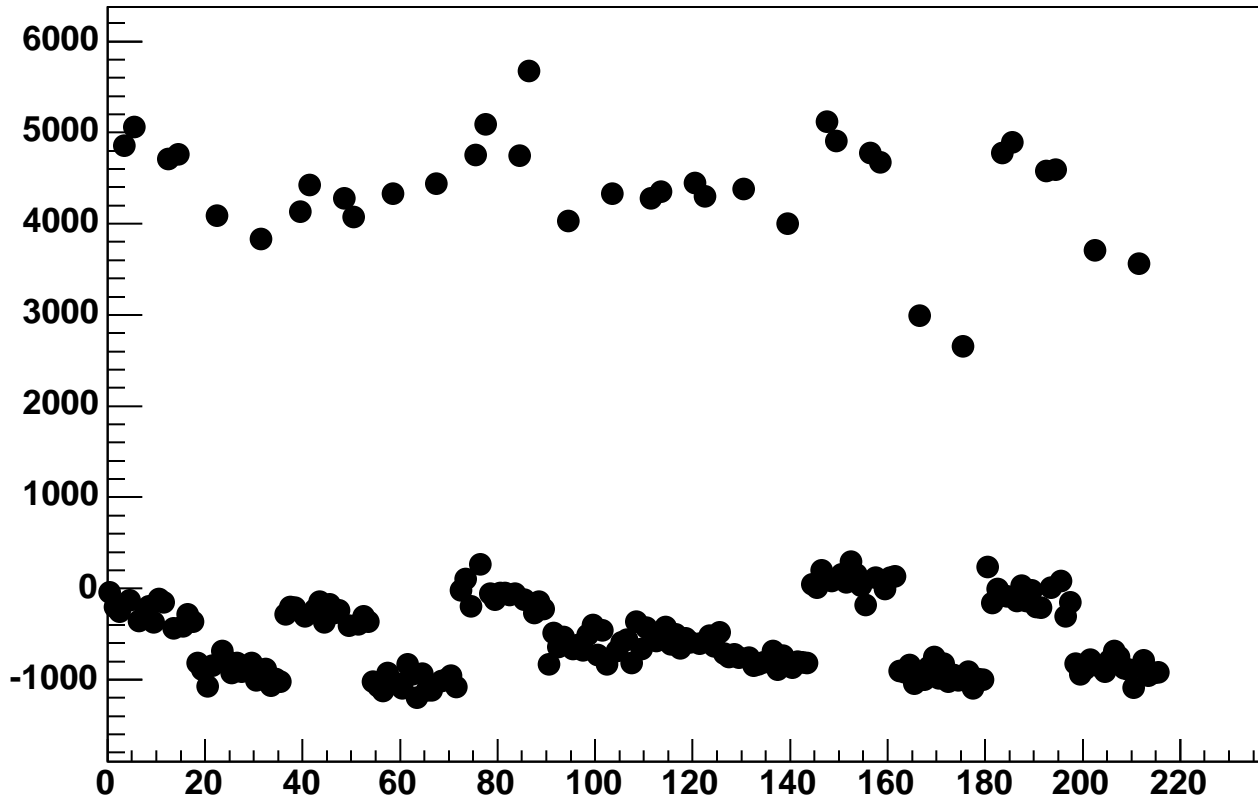
Enable 1, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan



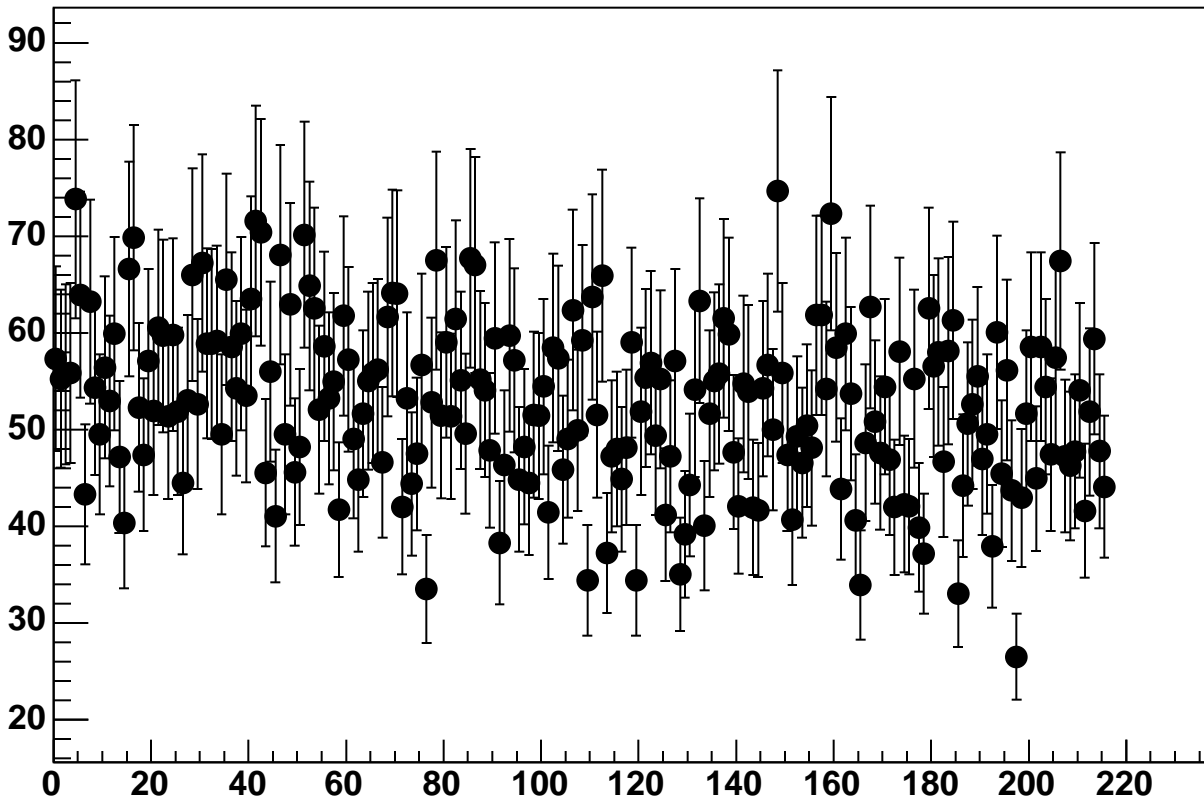
Enable 1, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan



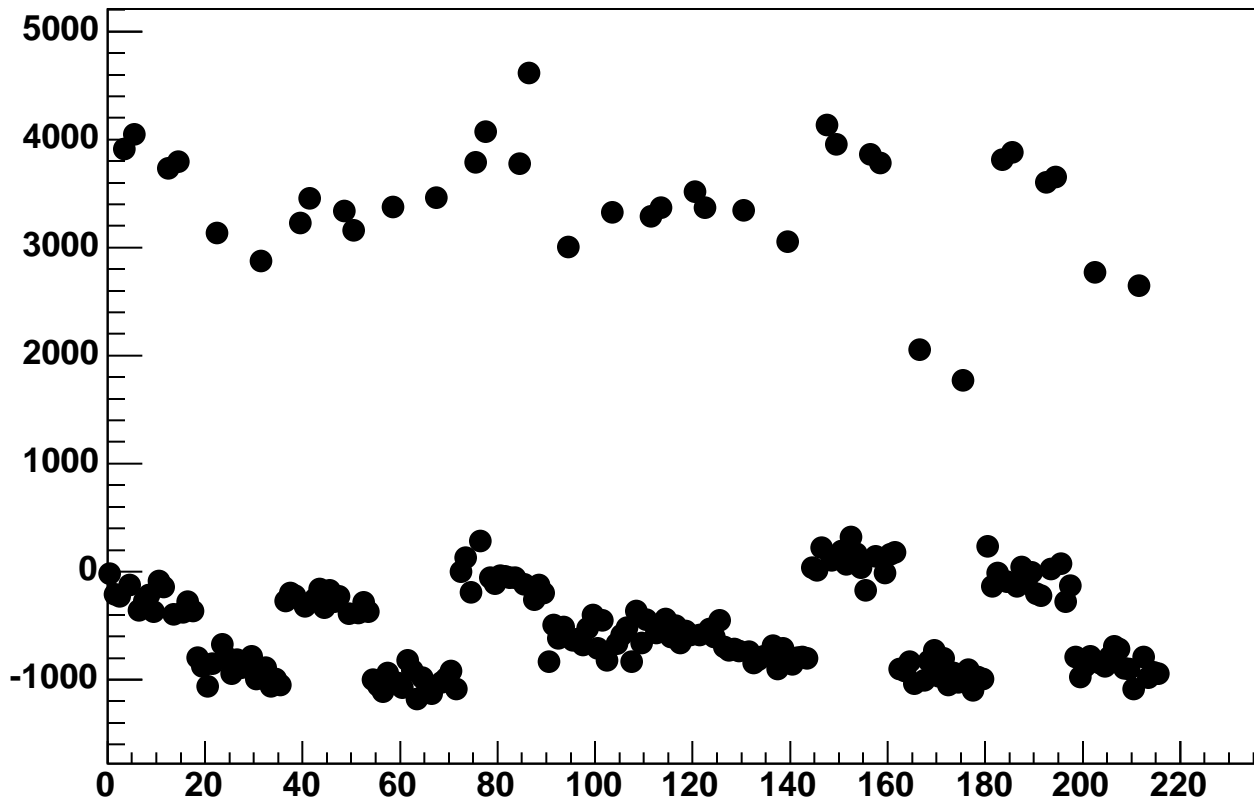
Enable 1, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



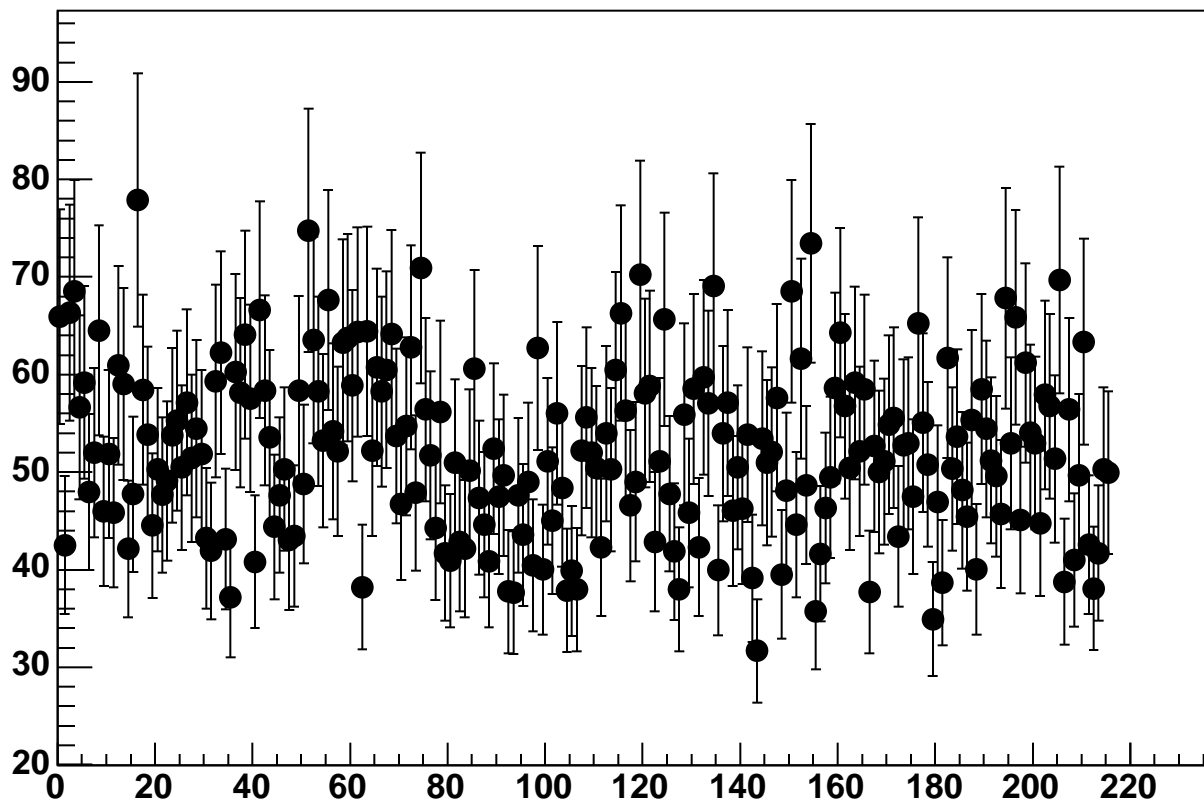
Enable 1, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



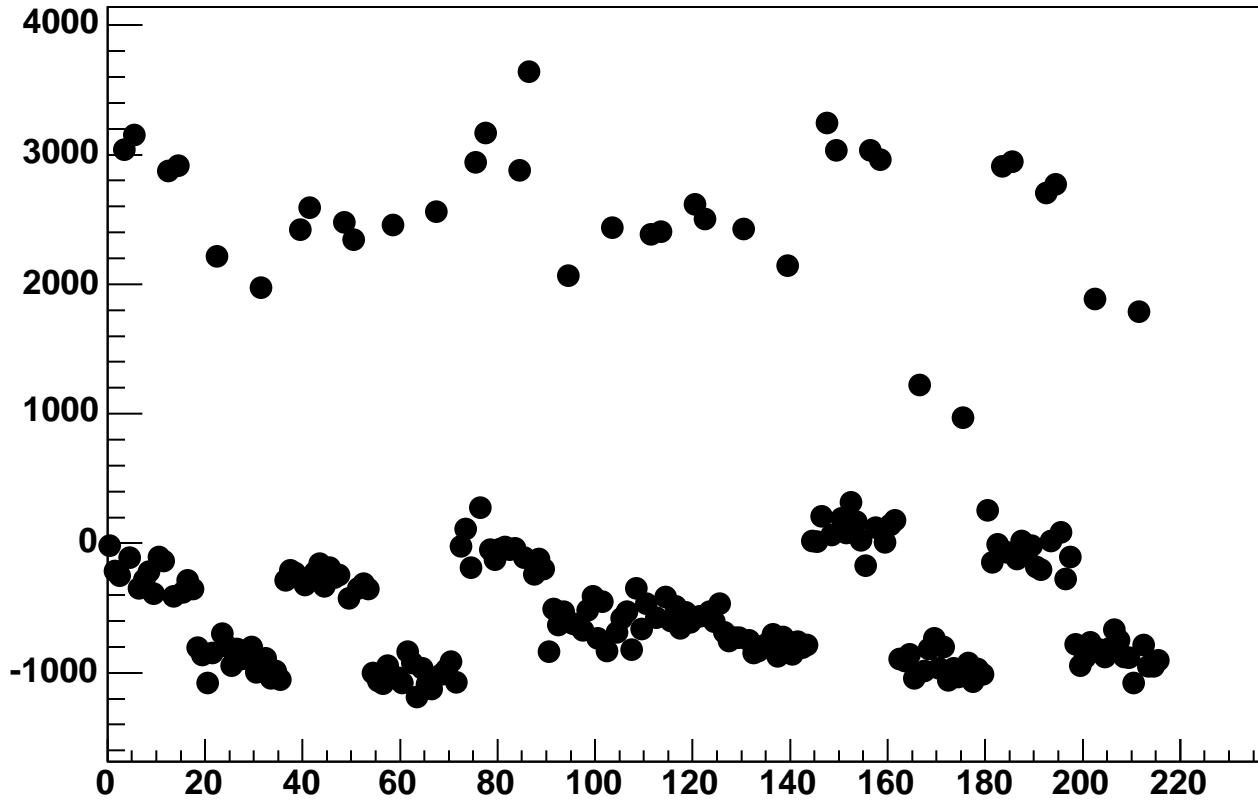
Enable 1, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan



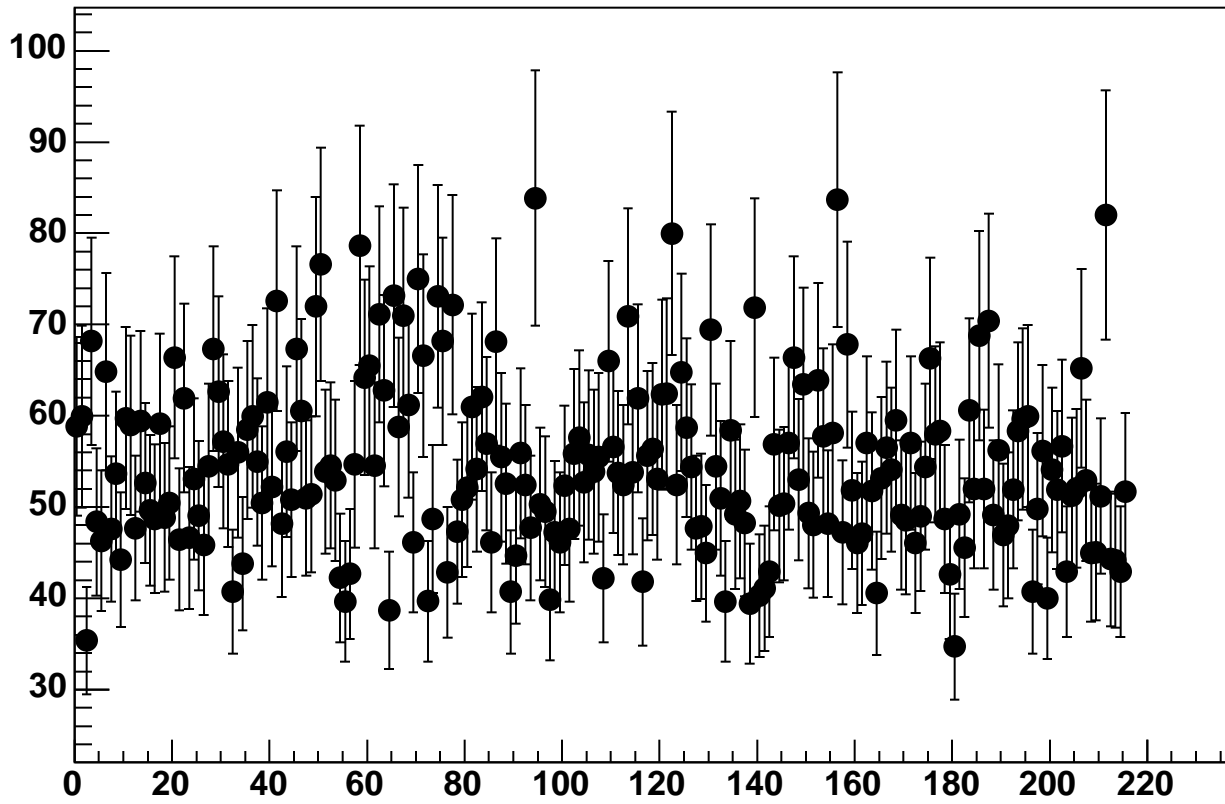
Enable 1, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan



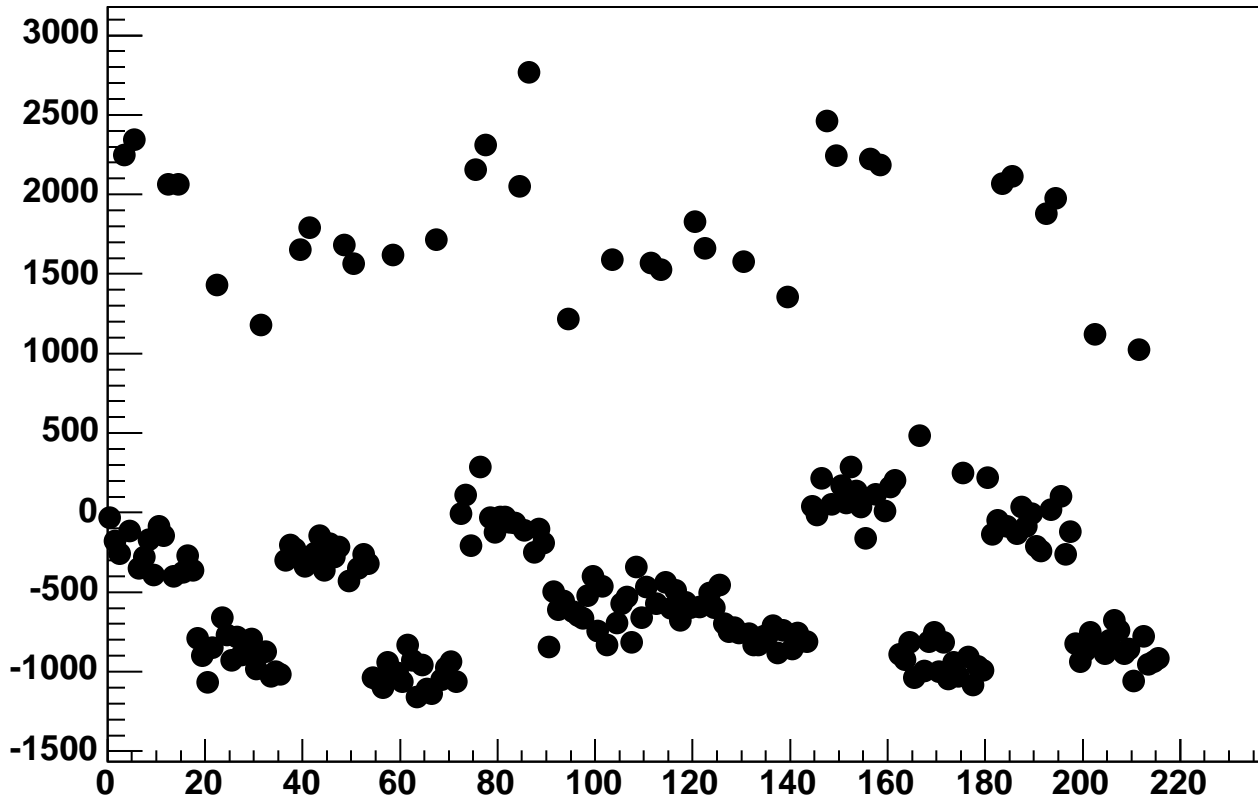
Enable 1, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



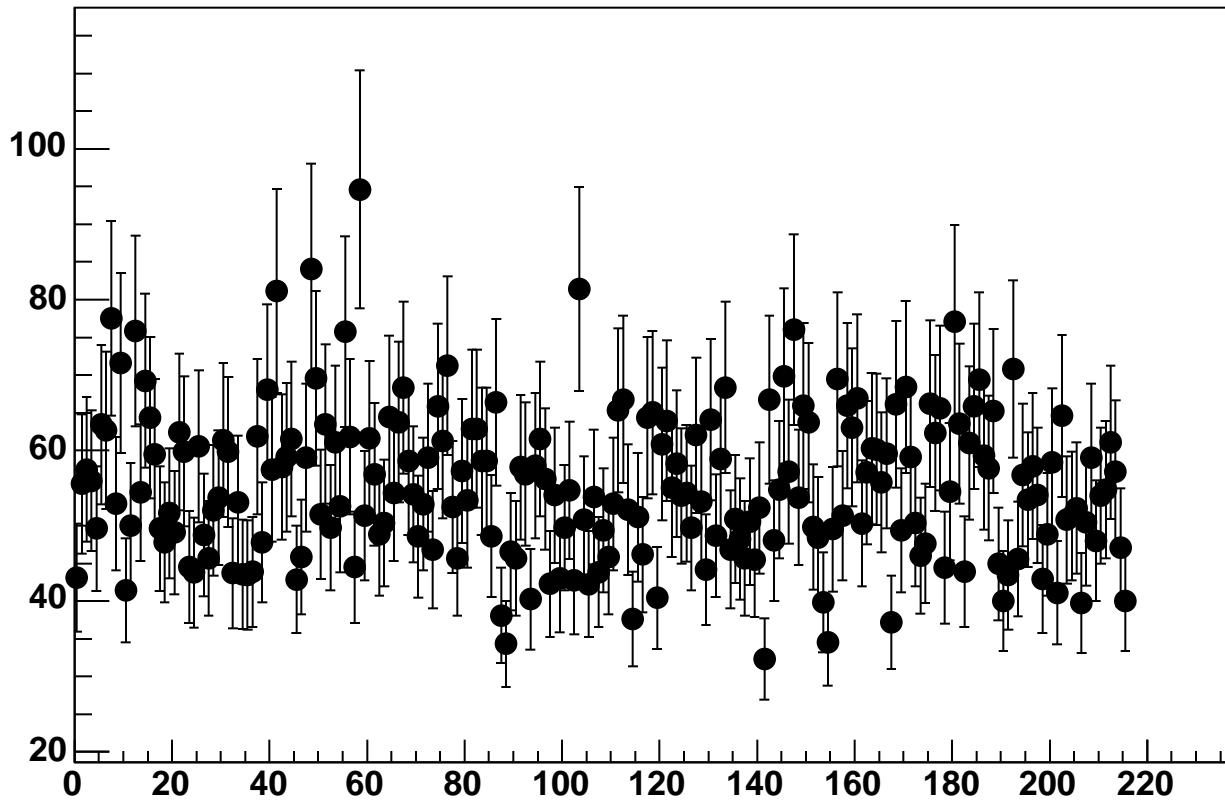
Enable 1, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



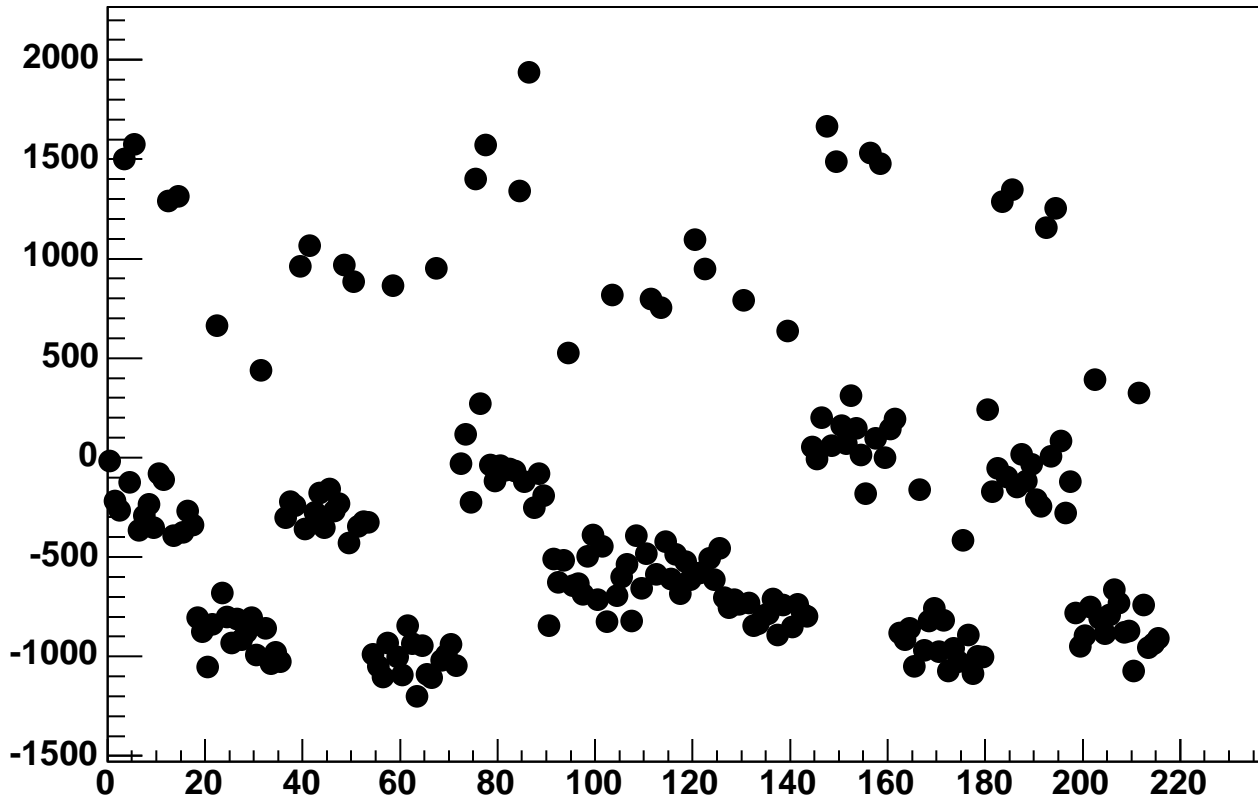
Enable 1, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan



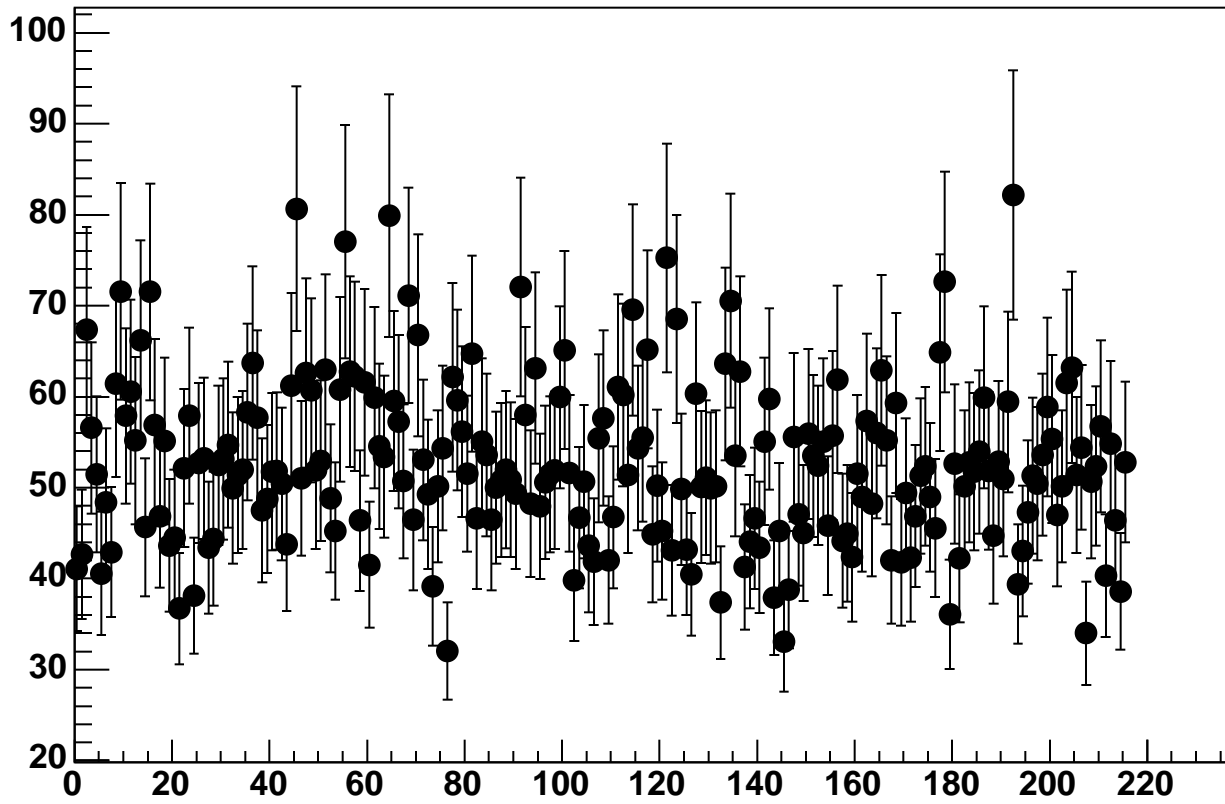
Enable 1, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan



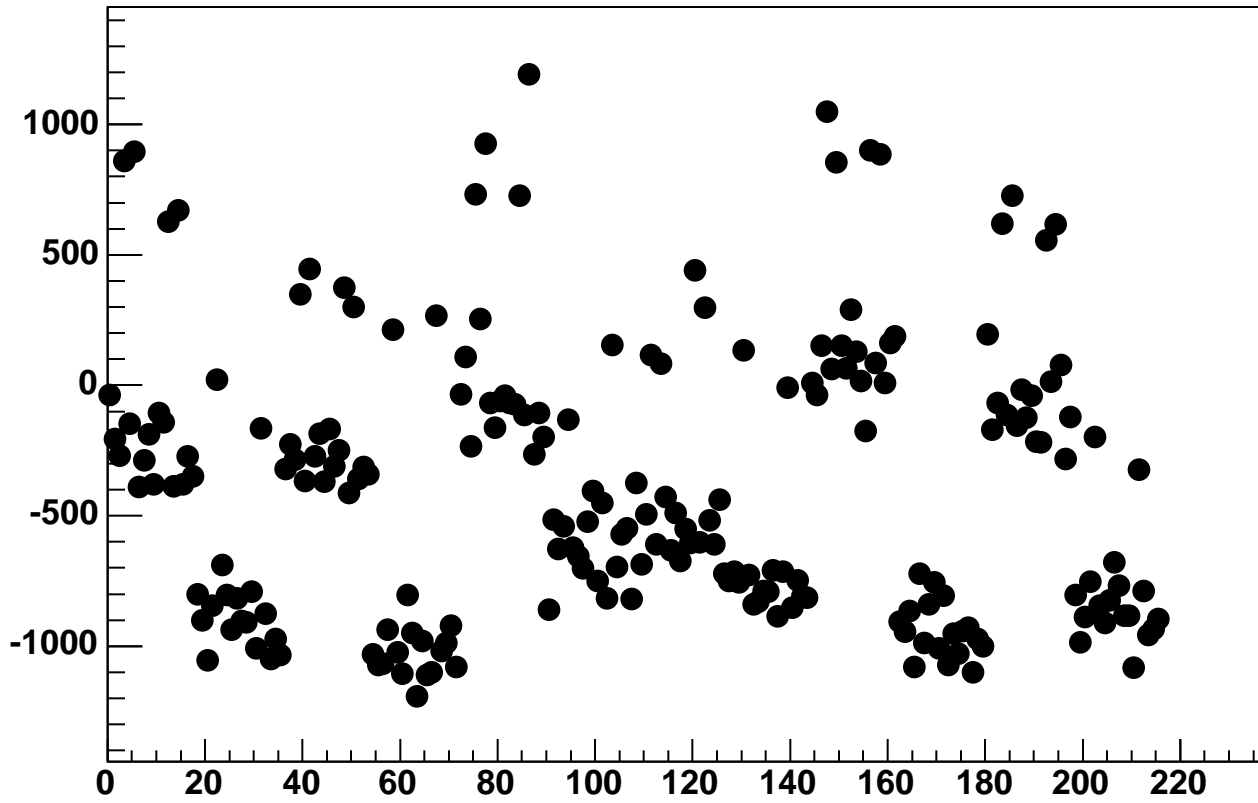
Enable 1, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



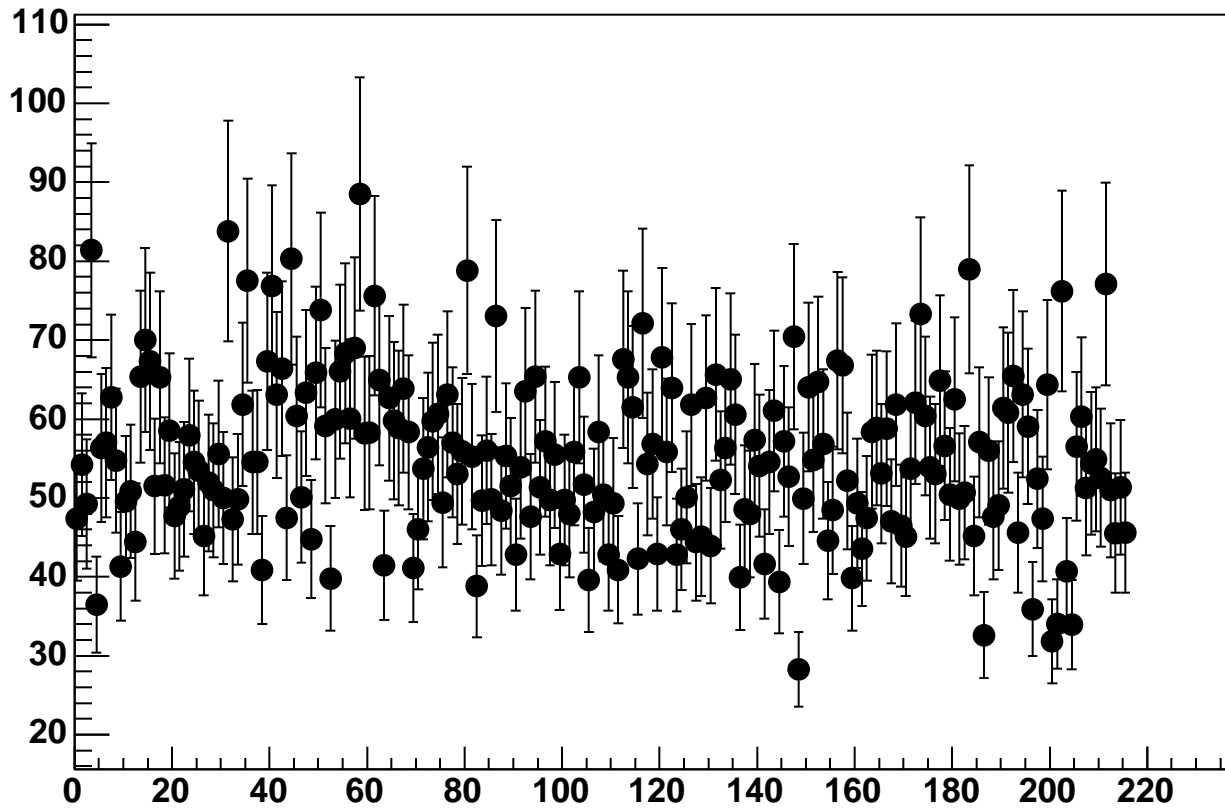
Enable 1, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan

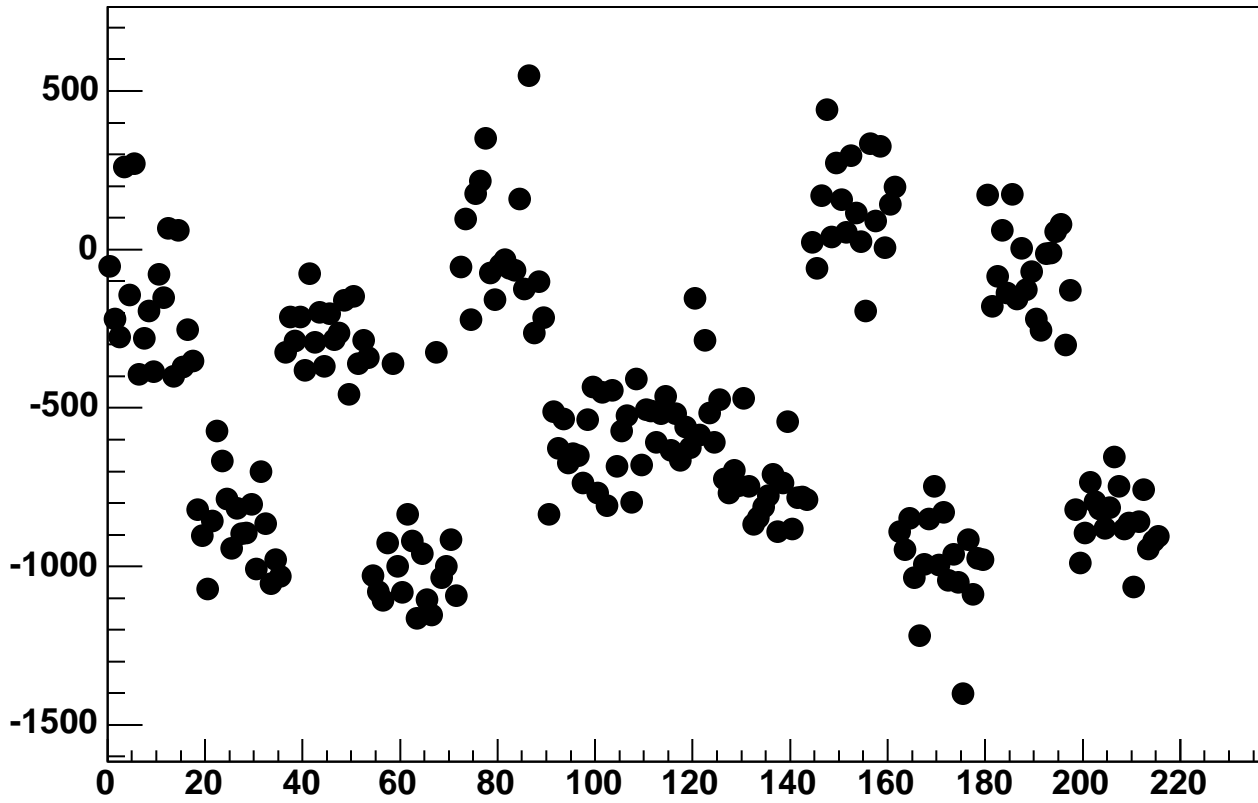


Enable 1, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan

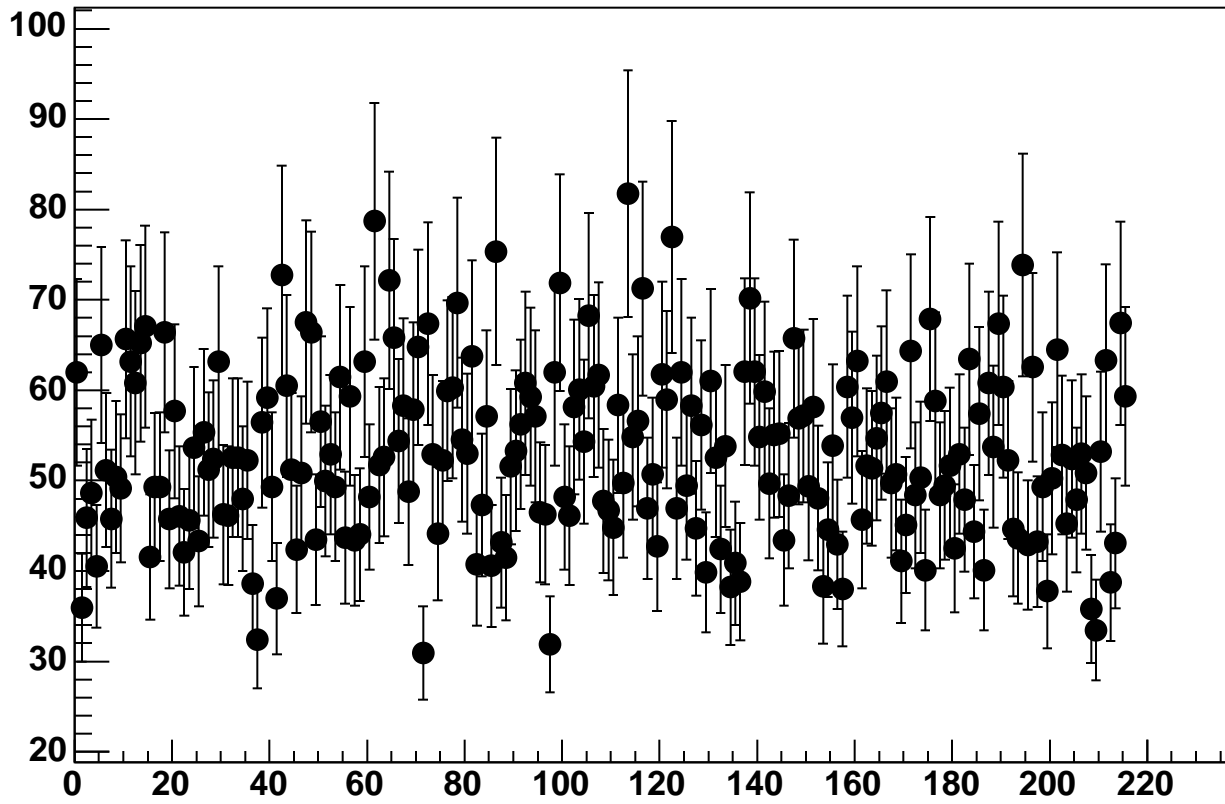




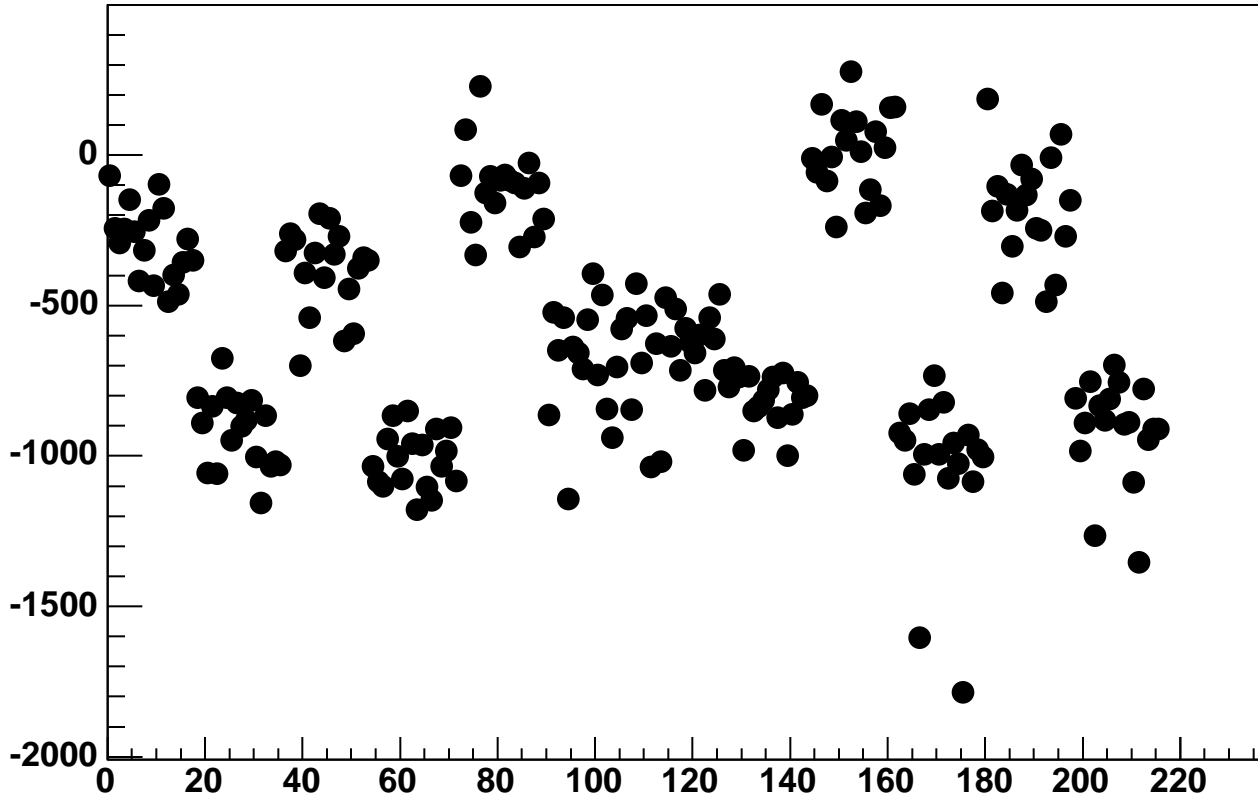
Enable 1, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



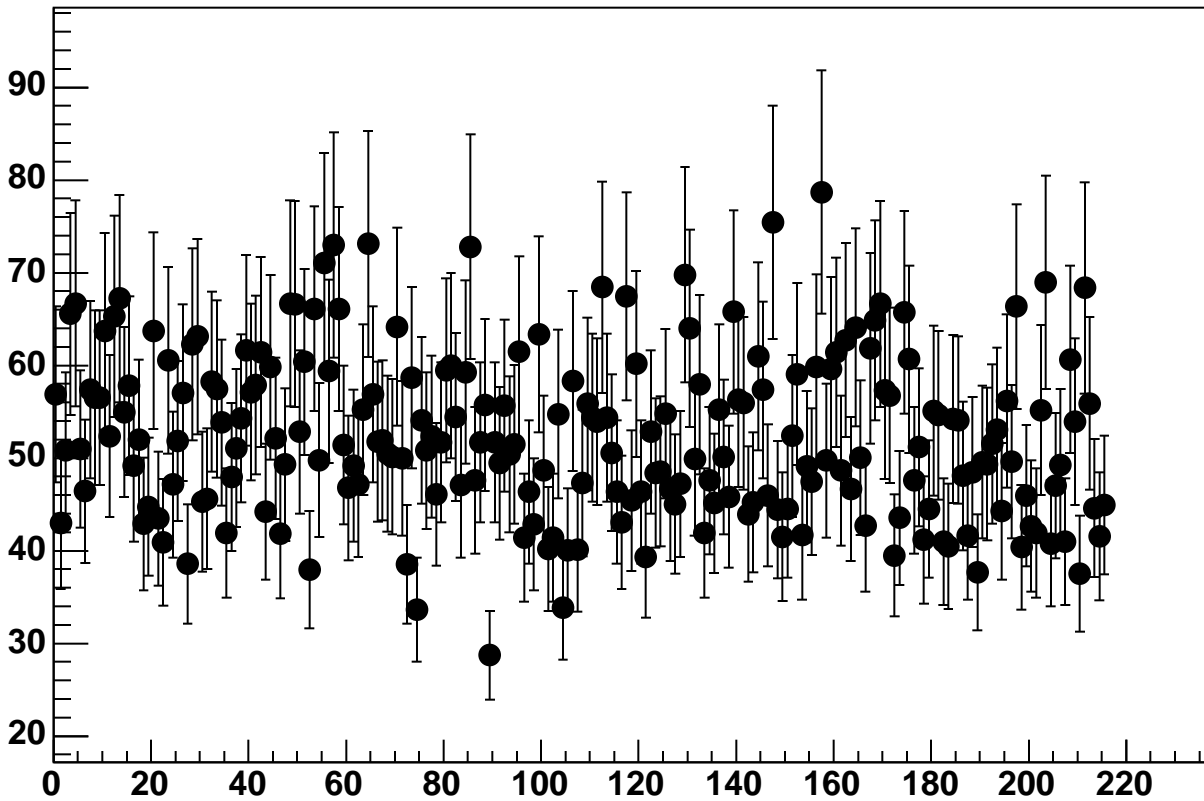
Enable 1, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



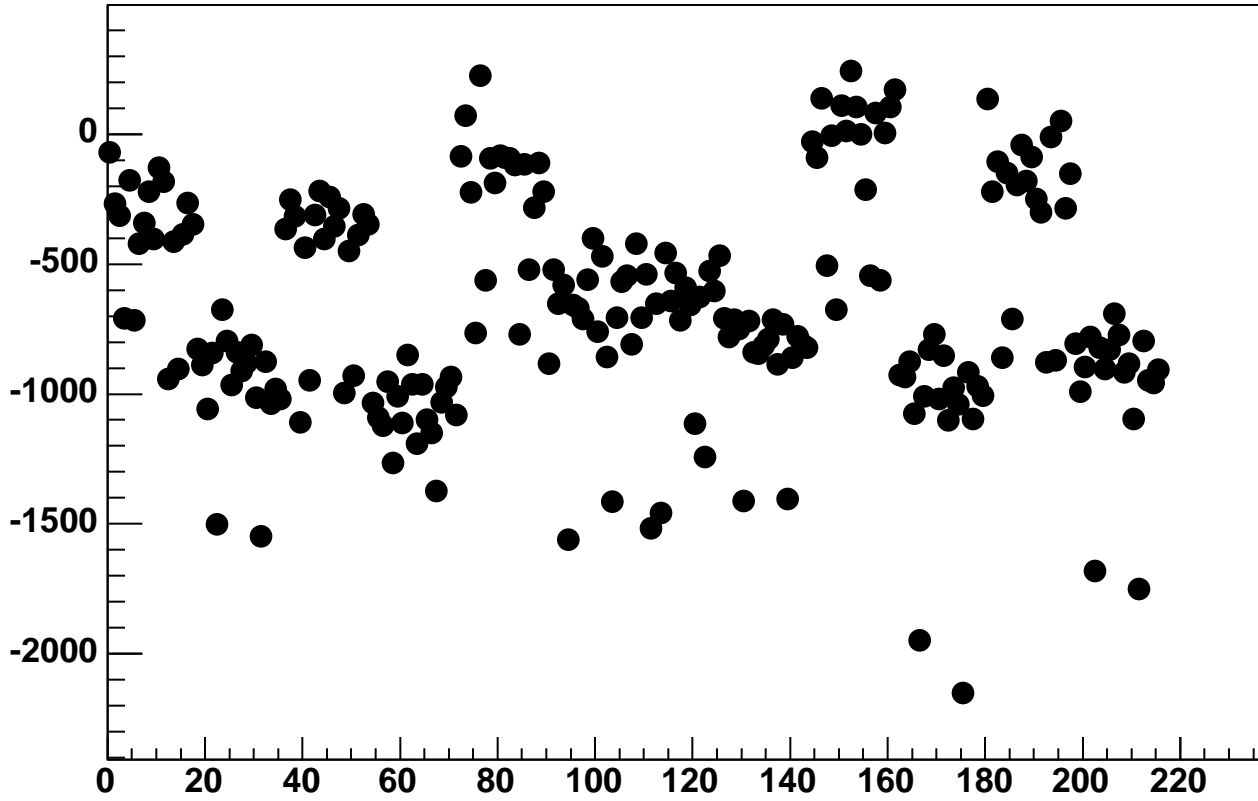
Enable 1, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan



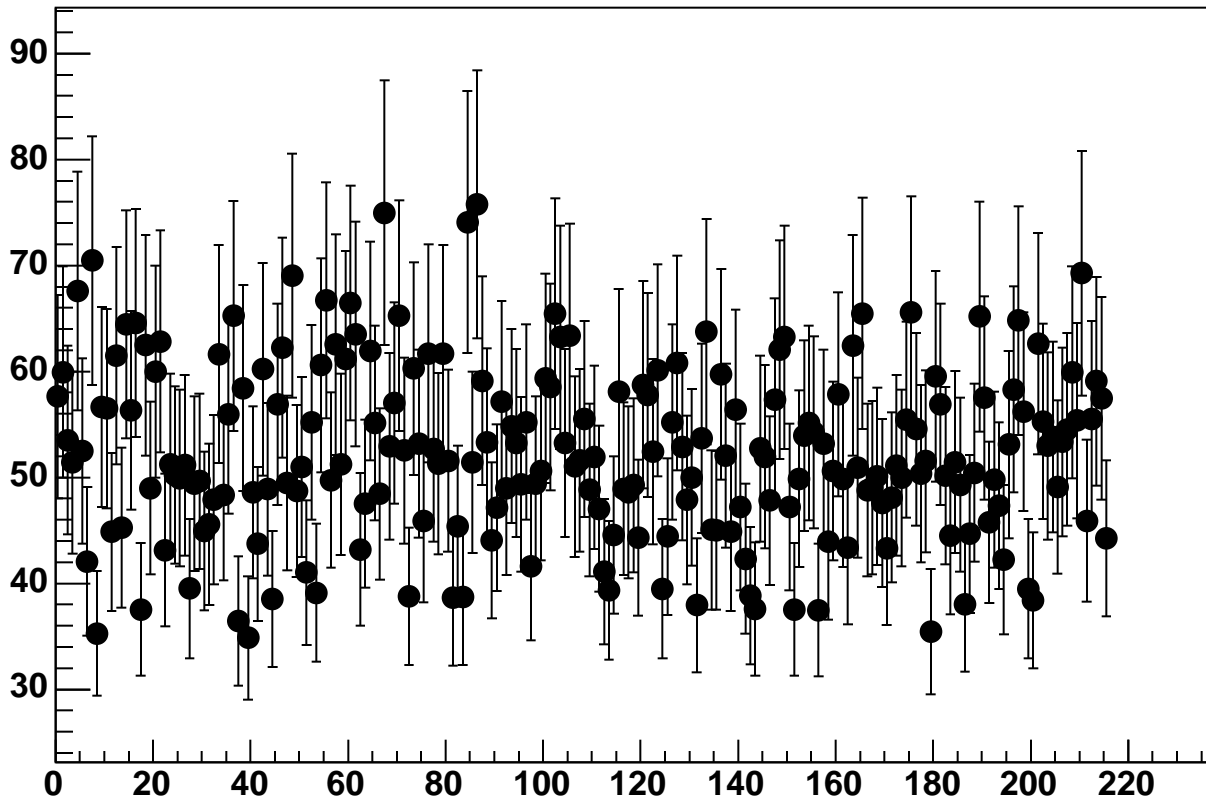
Enable 1, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan



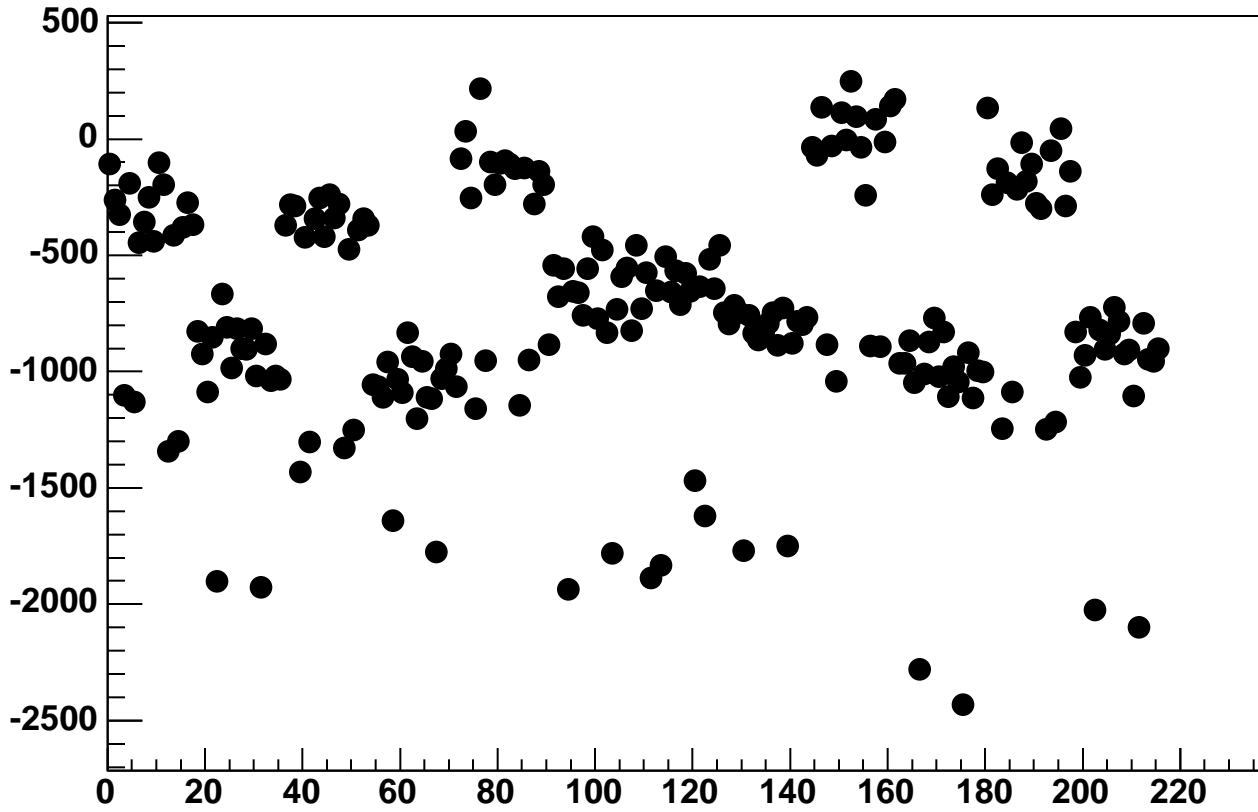
Enable 1, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



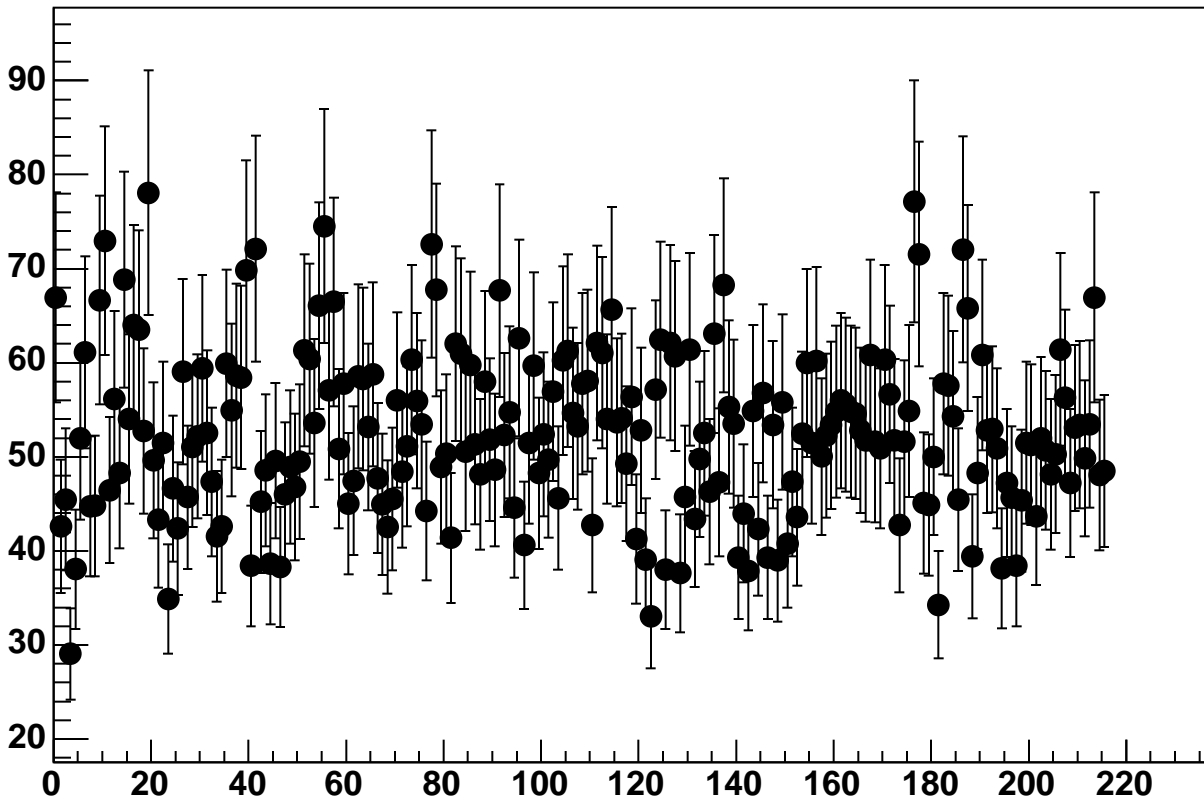
Enable 1, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



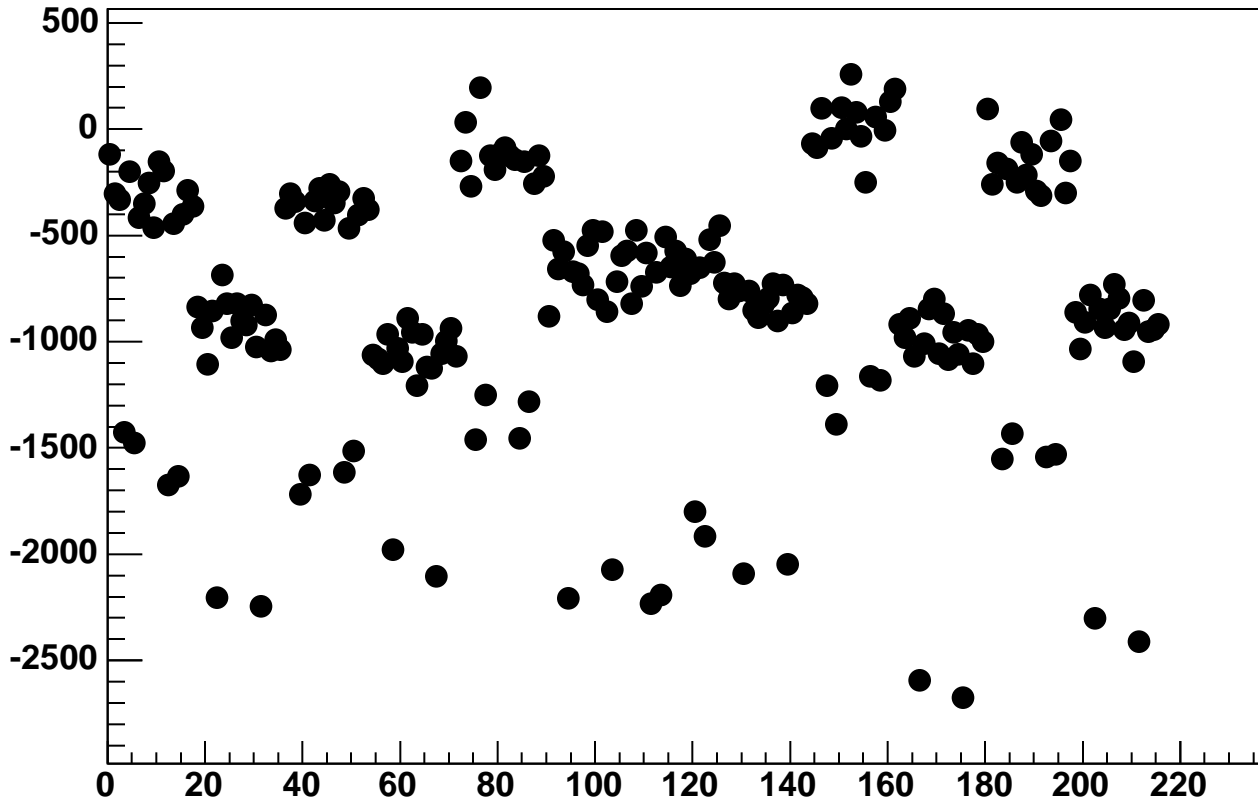
Enable 1, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan



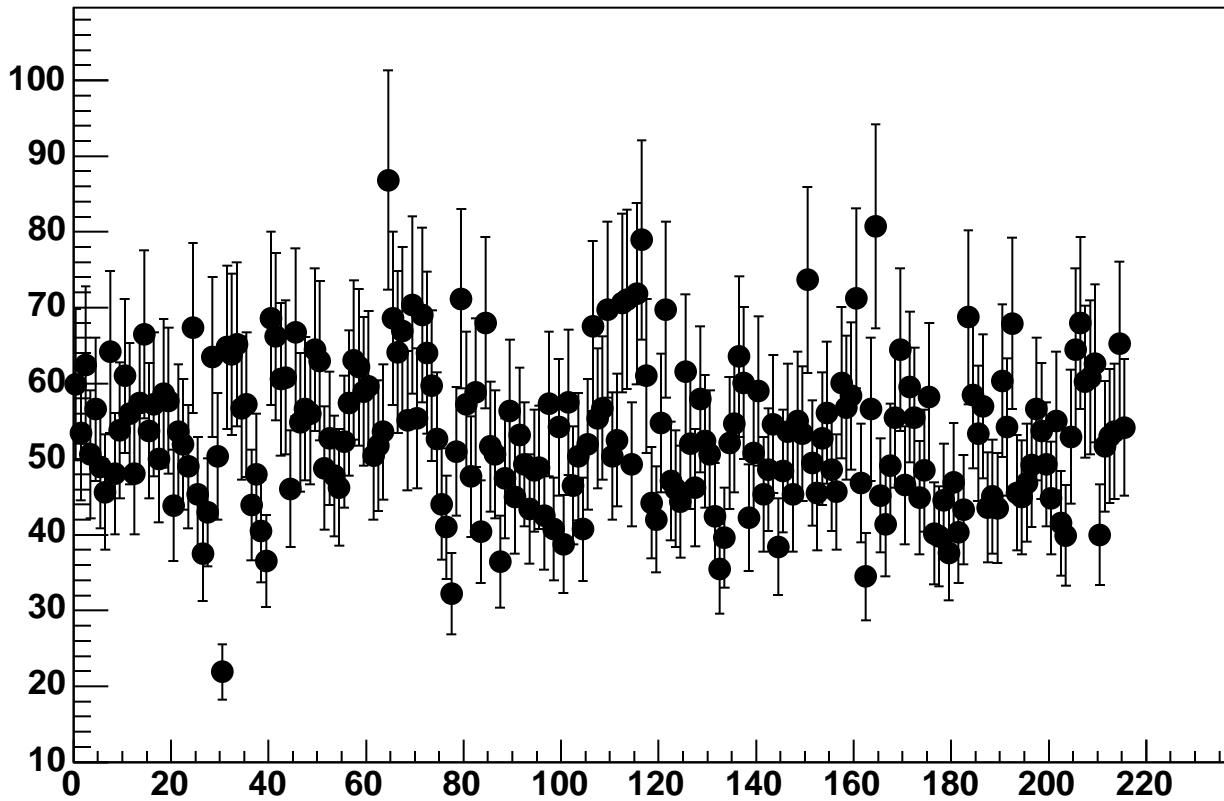
Enable 1, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan



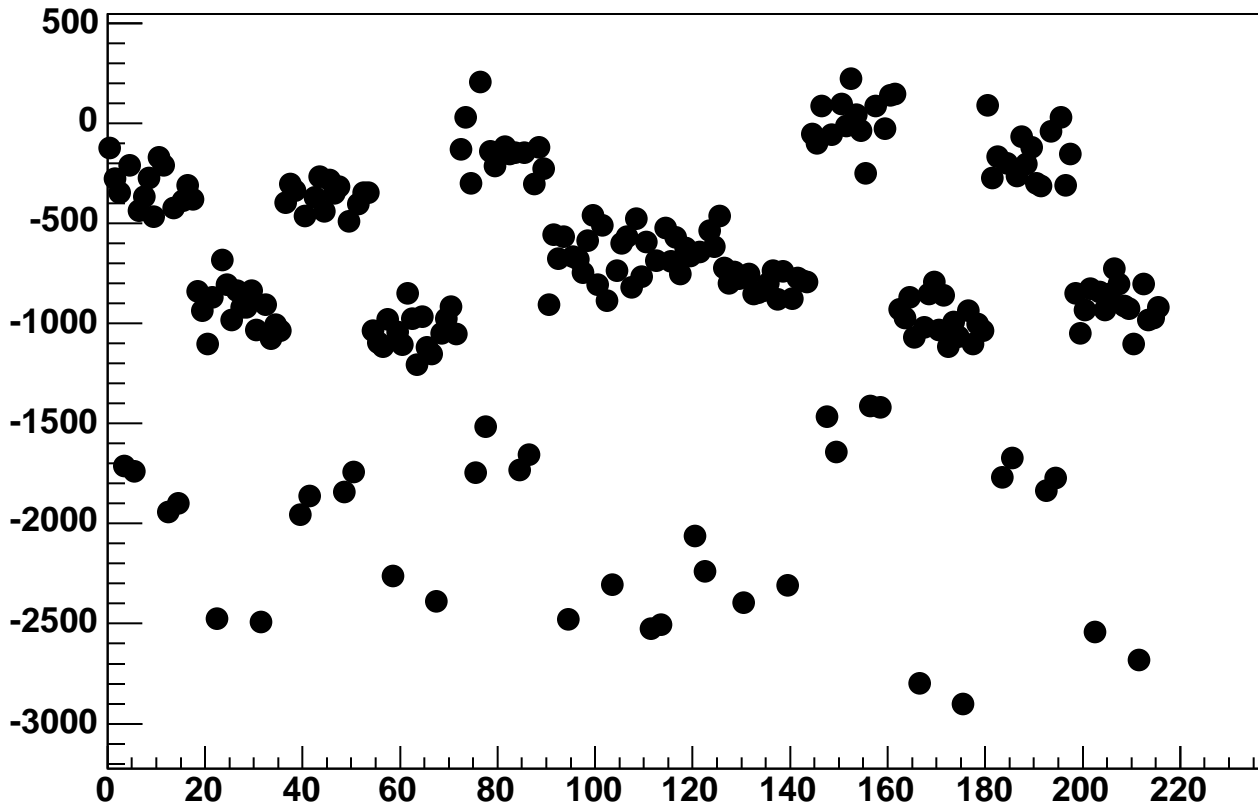
Enable 1, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



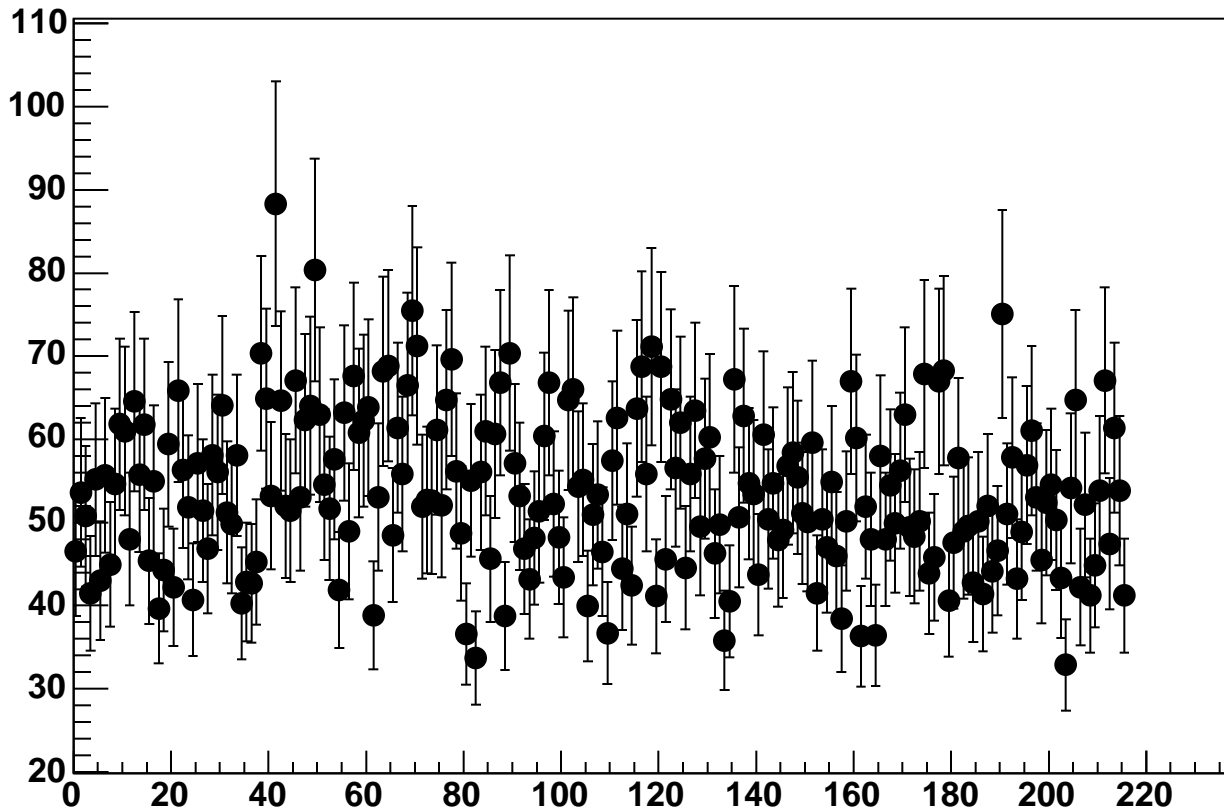
Enable 1, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



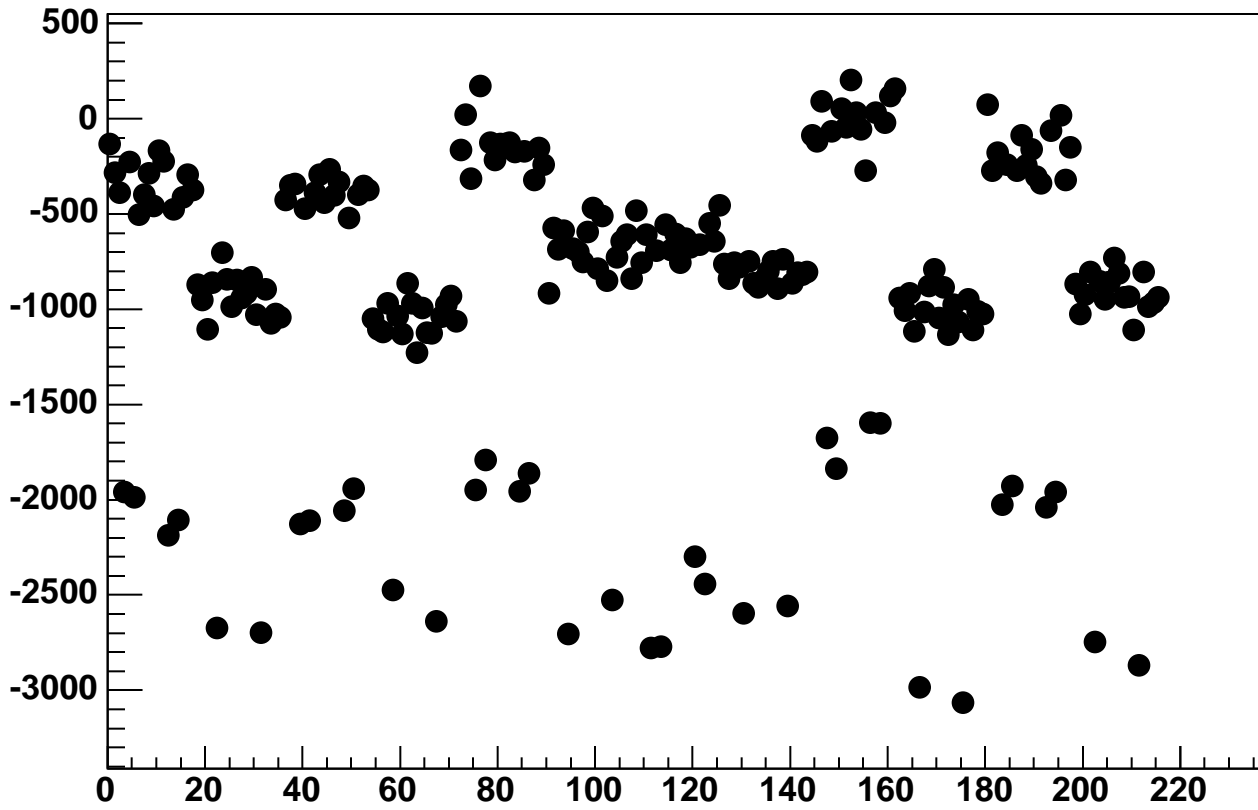
Enable 1, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan



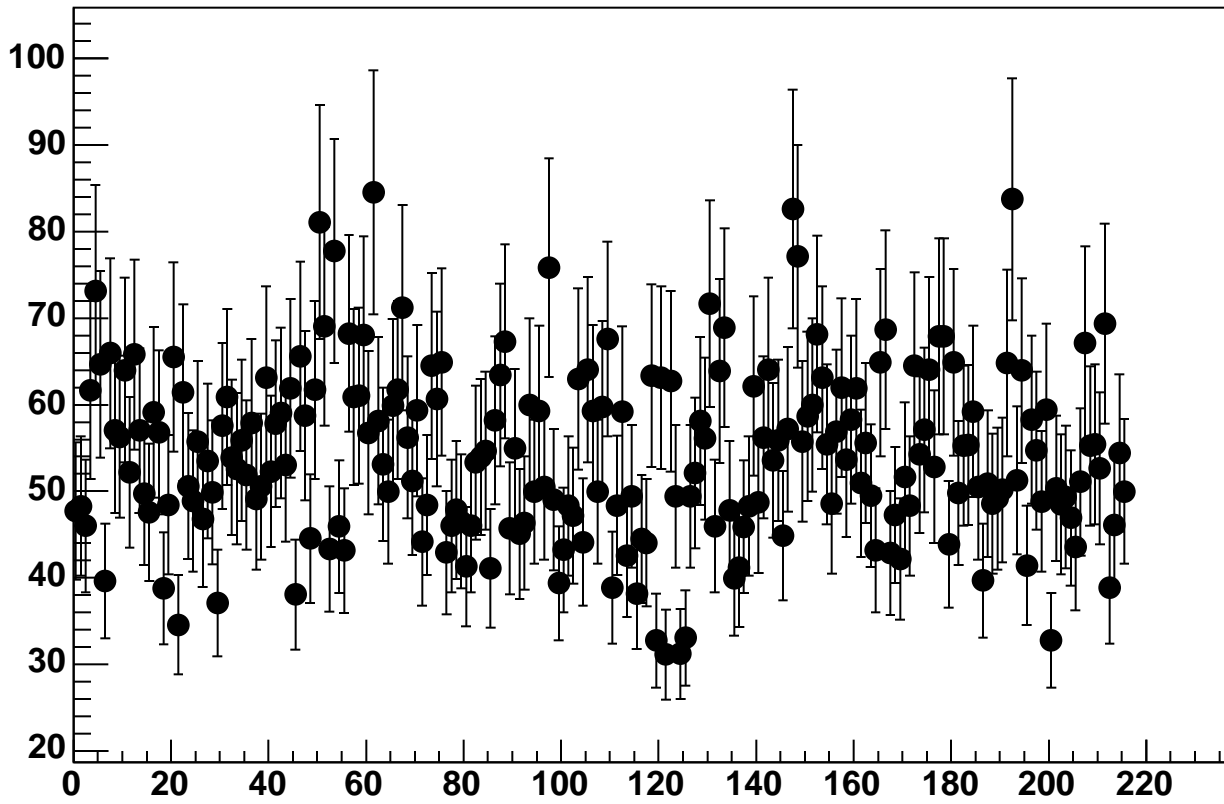
Enable 1, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan



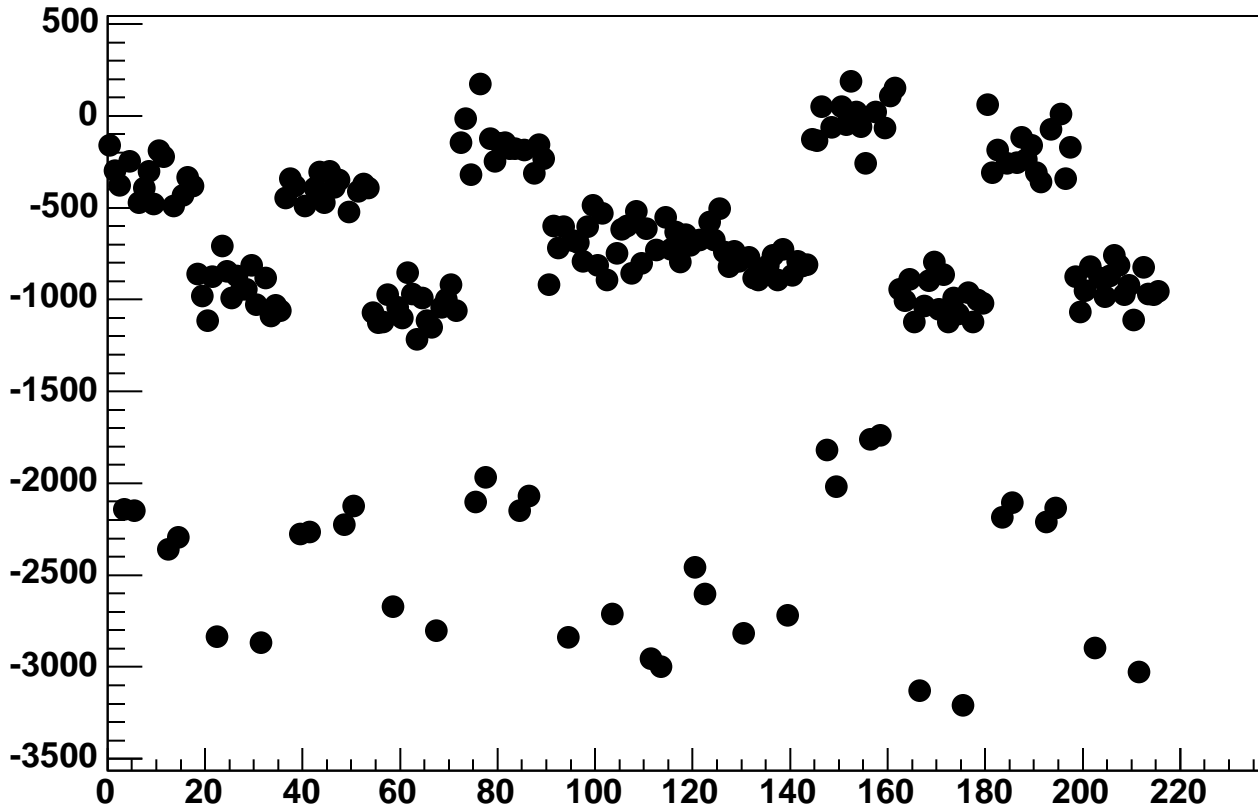
Enable 1, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



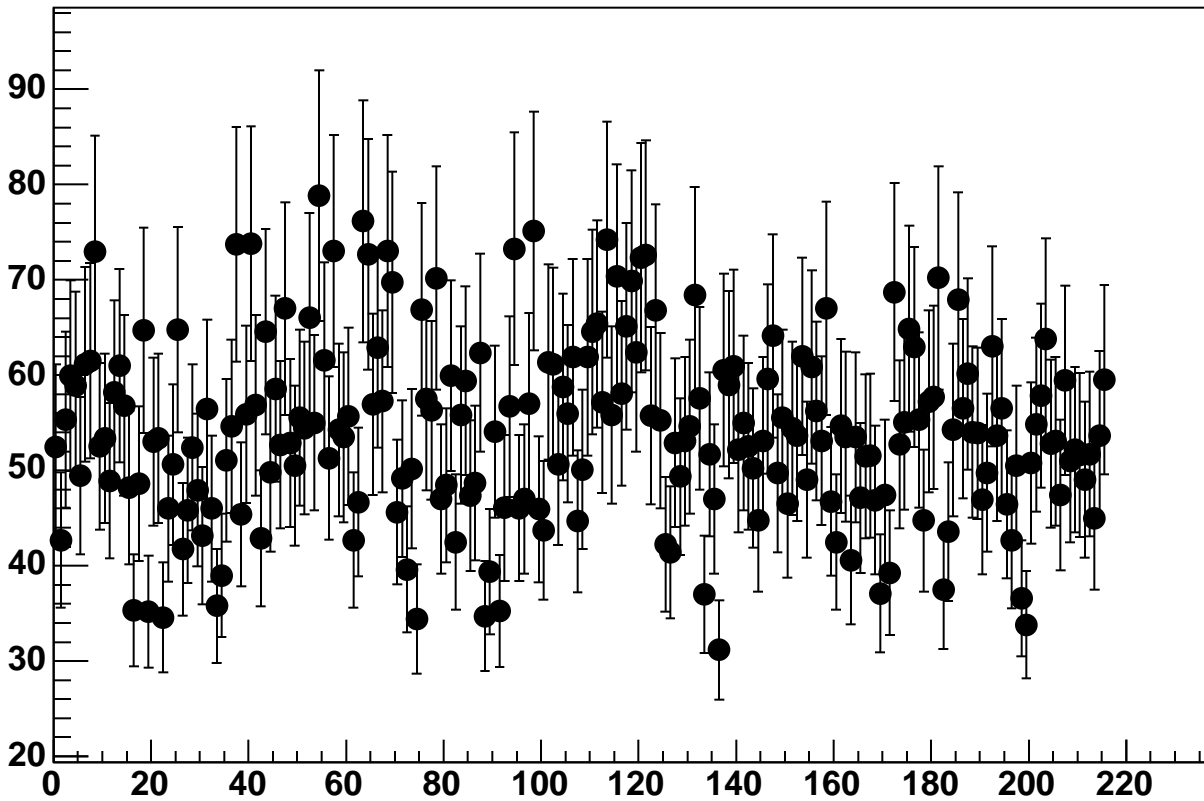
Enable 1, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan

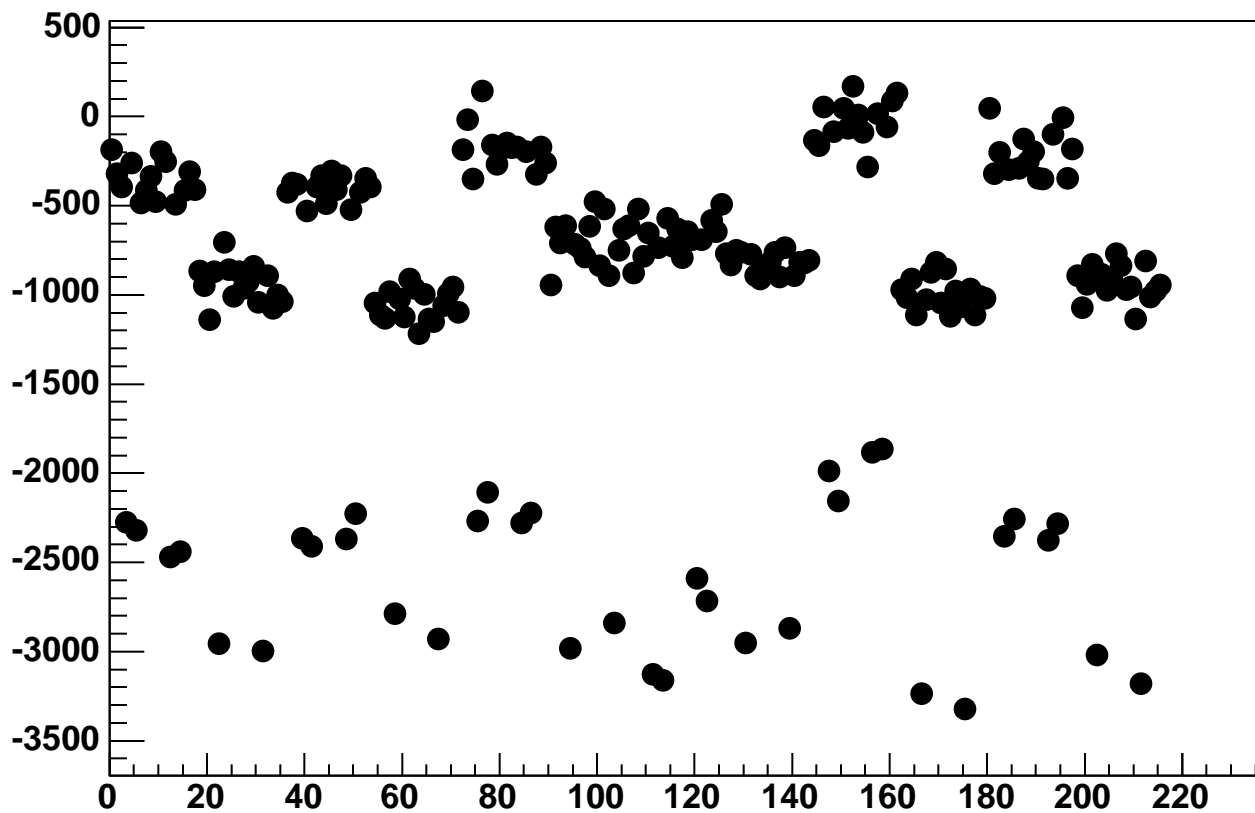


Enable 1, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan

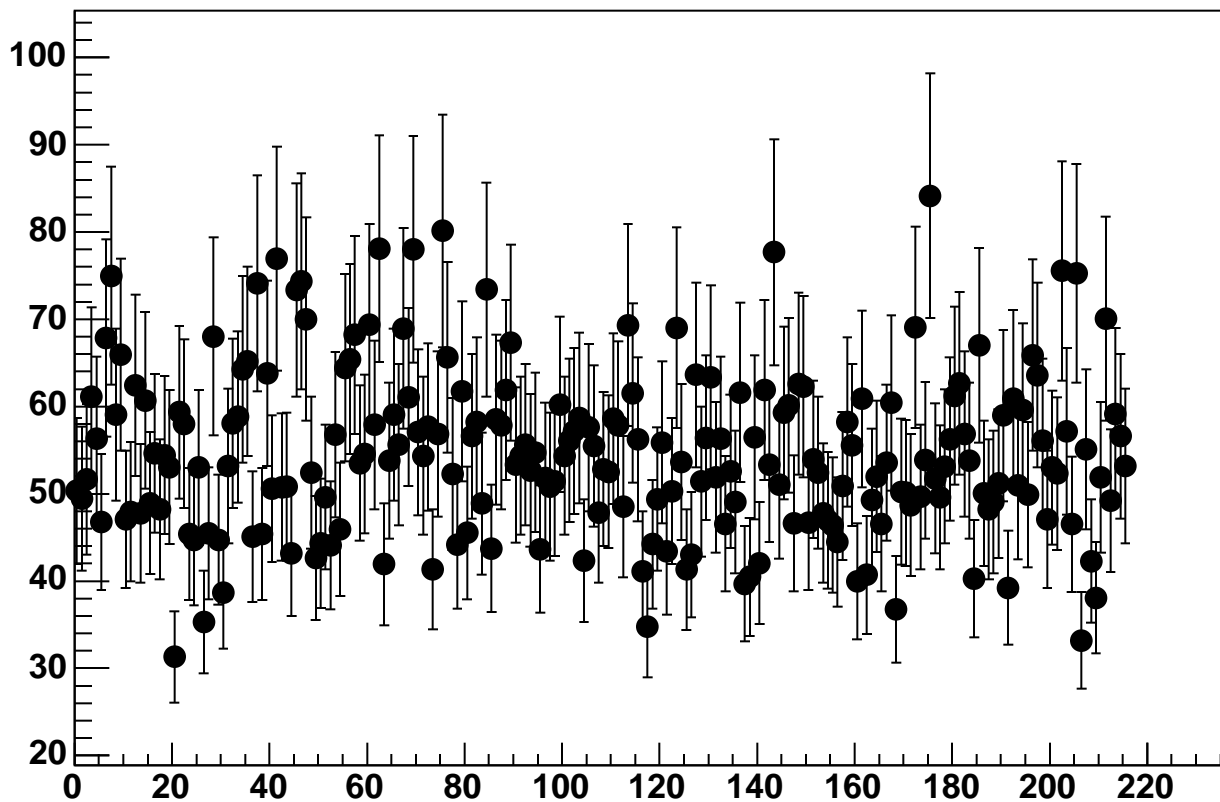




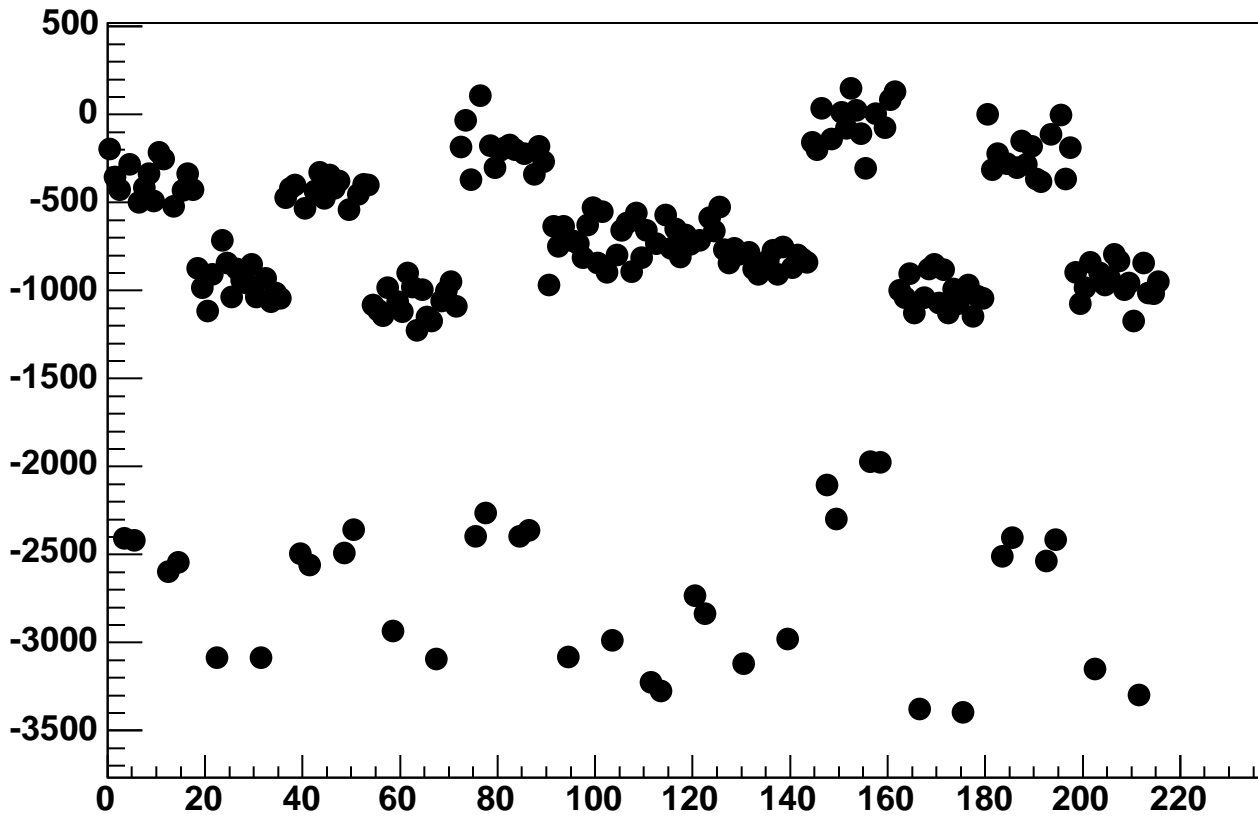
Enable 1, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



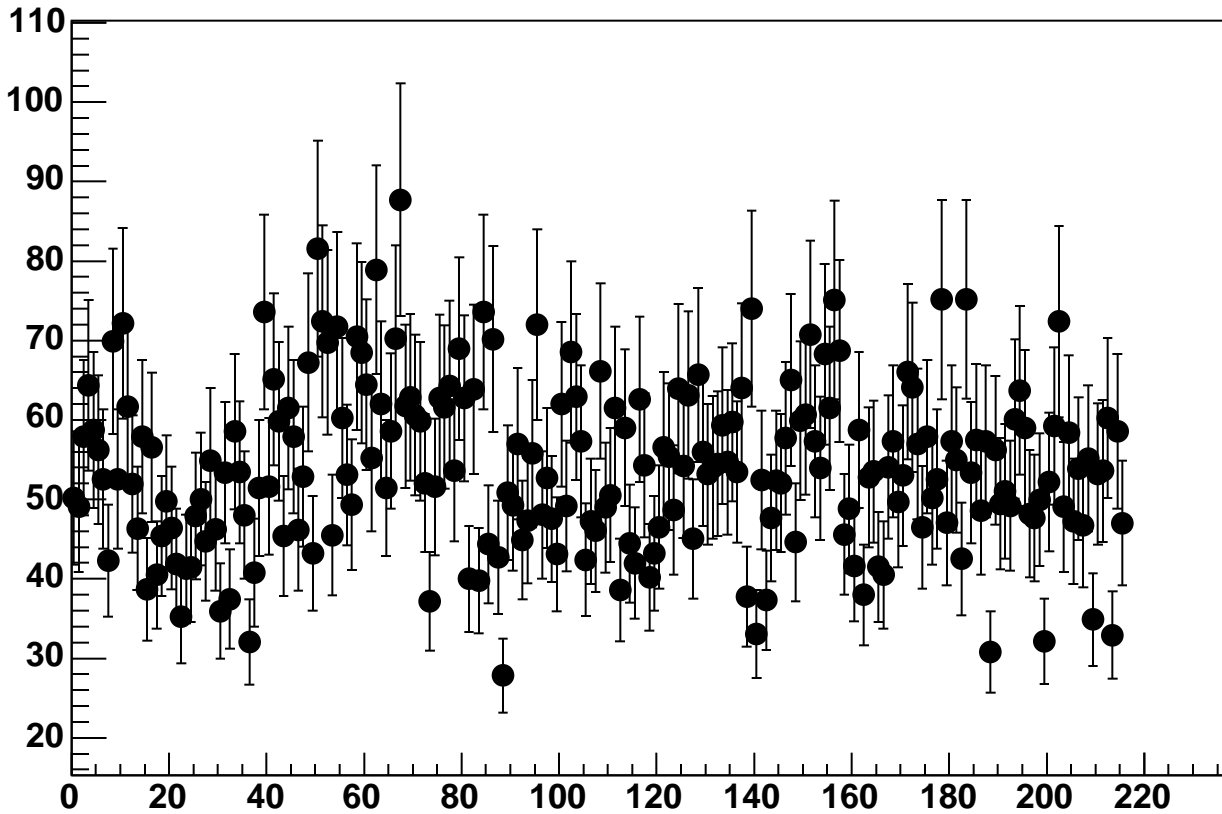
Enable 1, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



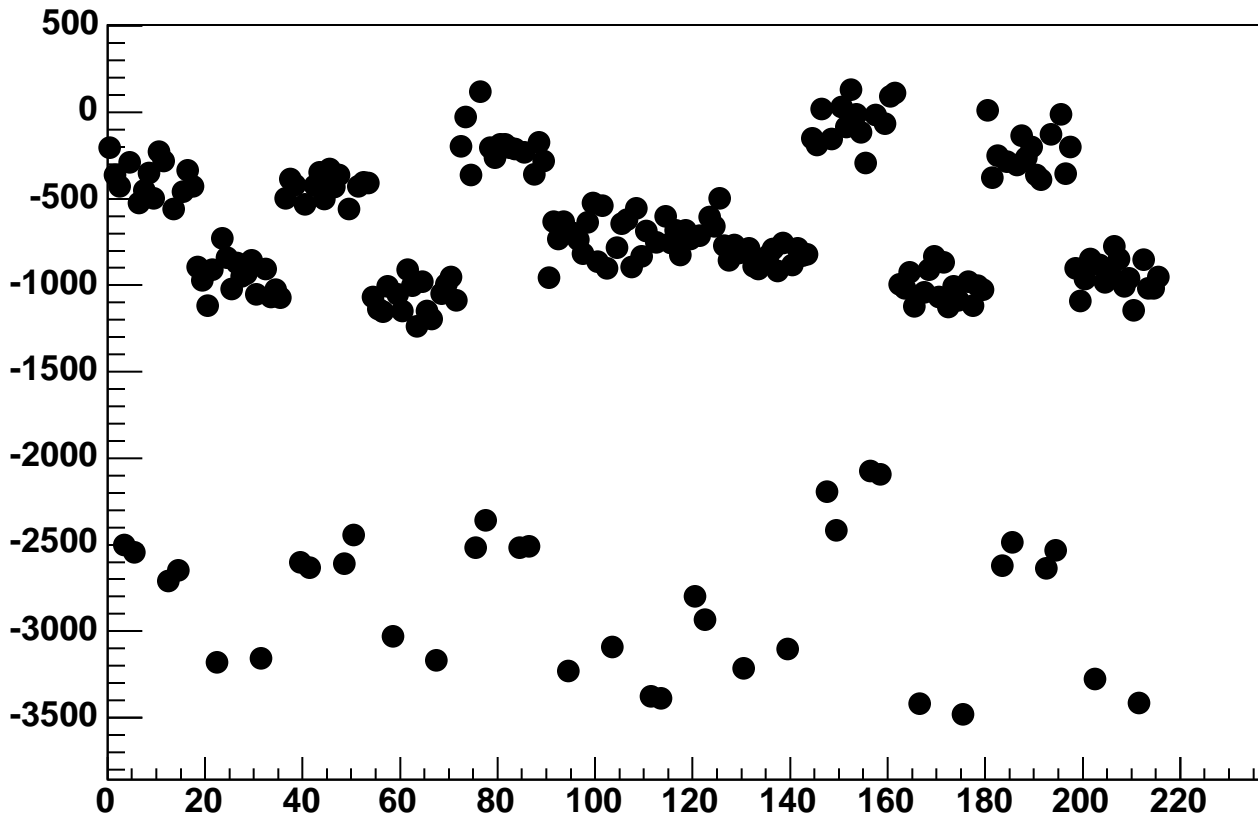
Enable 1, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan



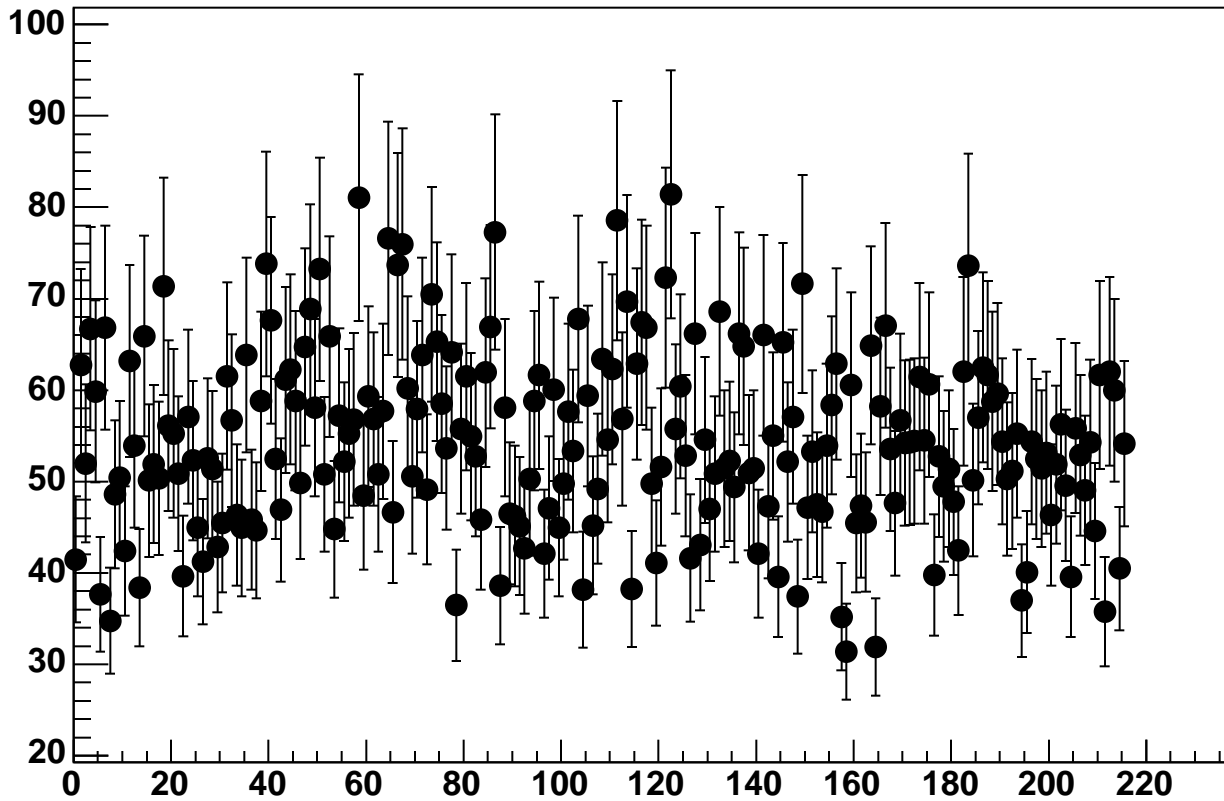
Enable 1, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan



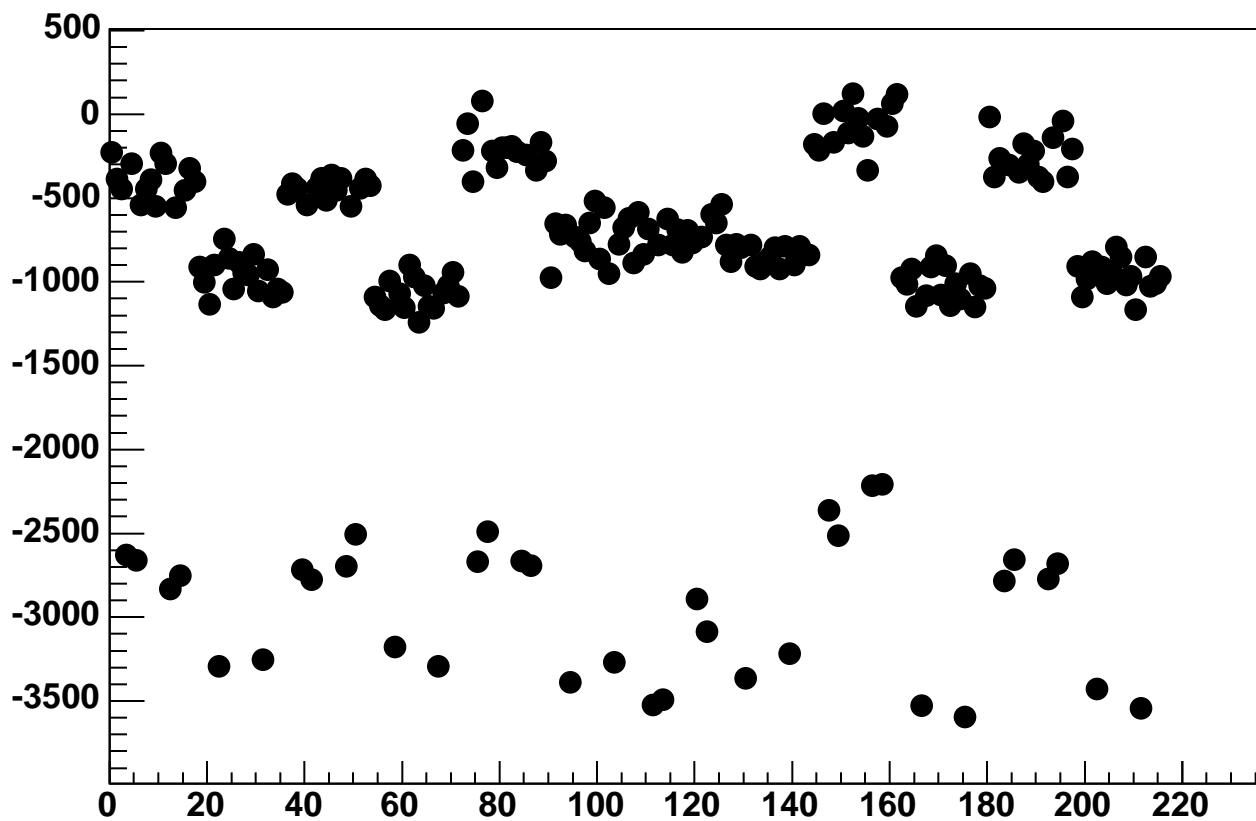
Enable 1, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



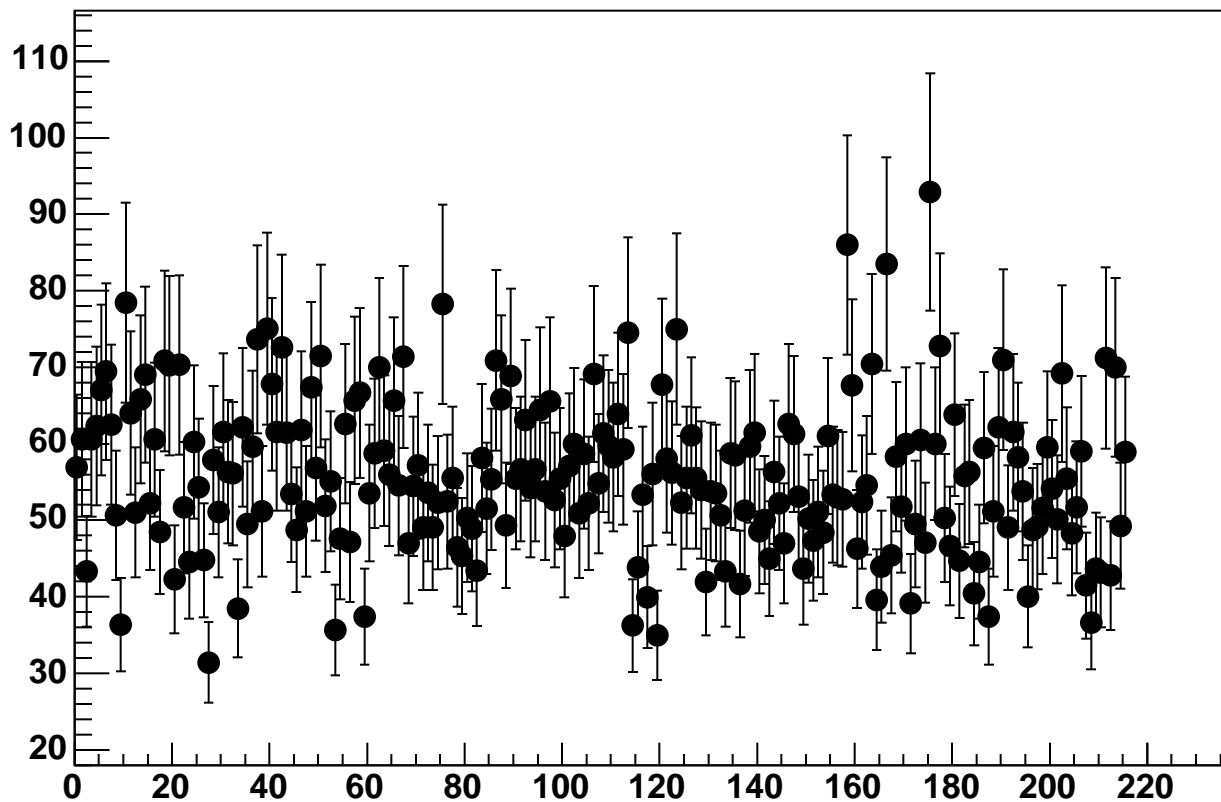
Enable 1, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



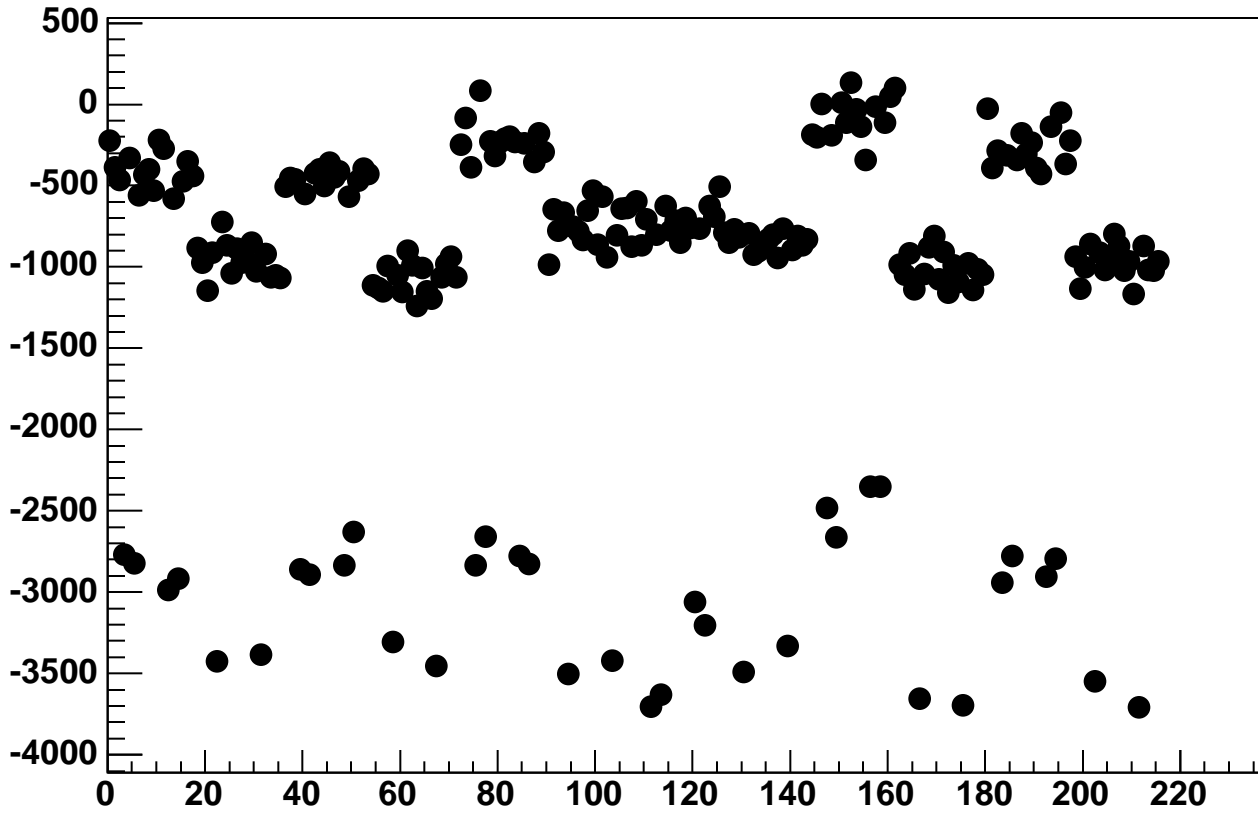
Enable 1, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan



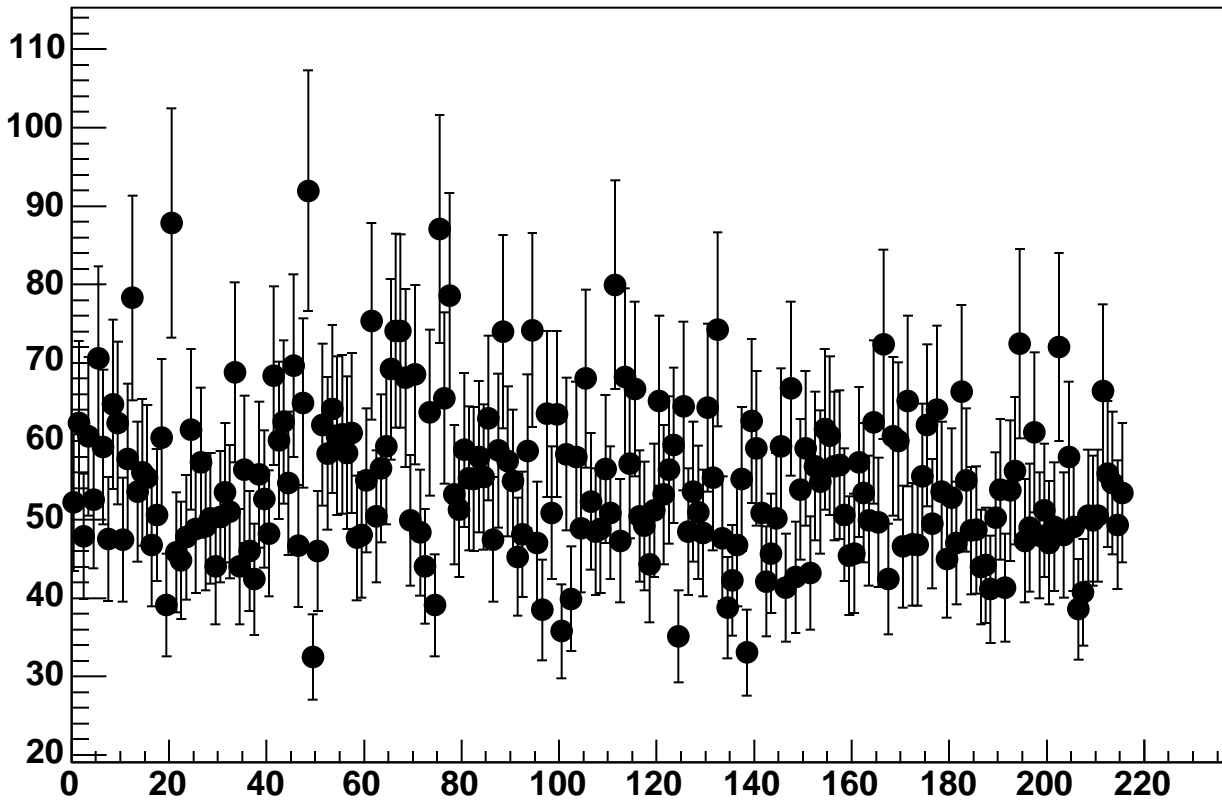
Enable 1, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan



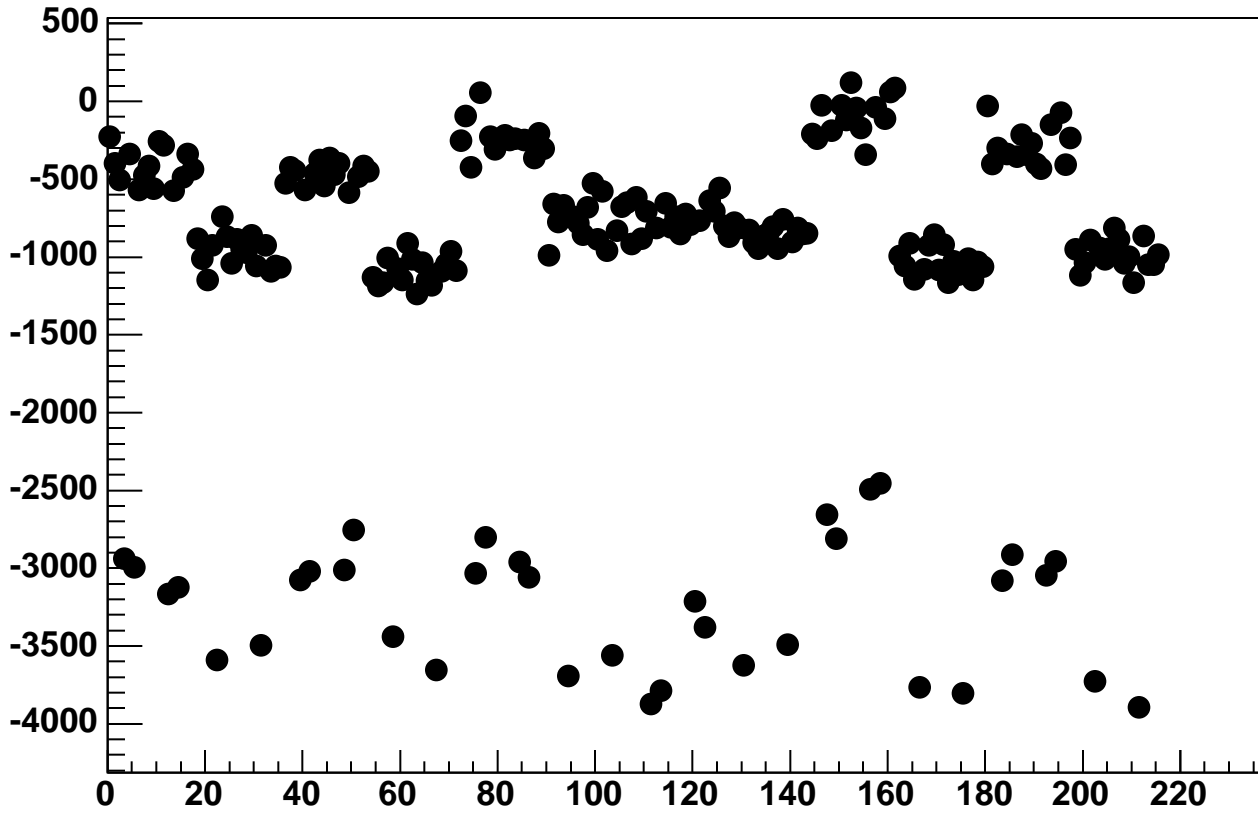
Enable 1, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



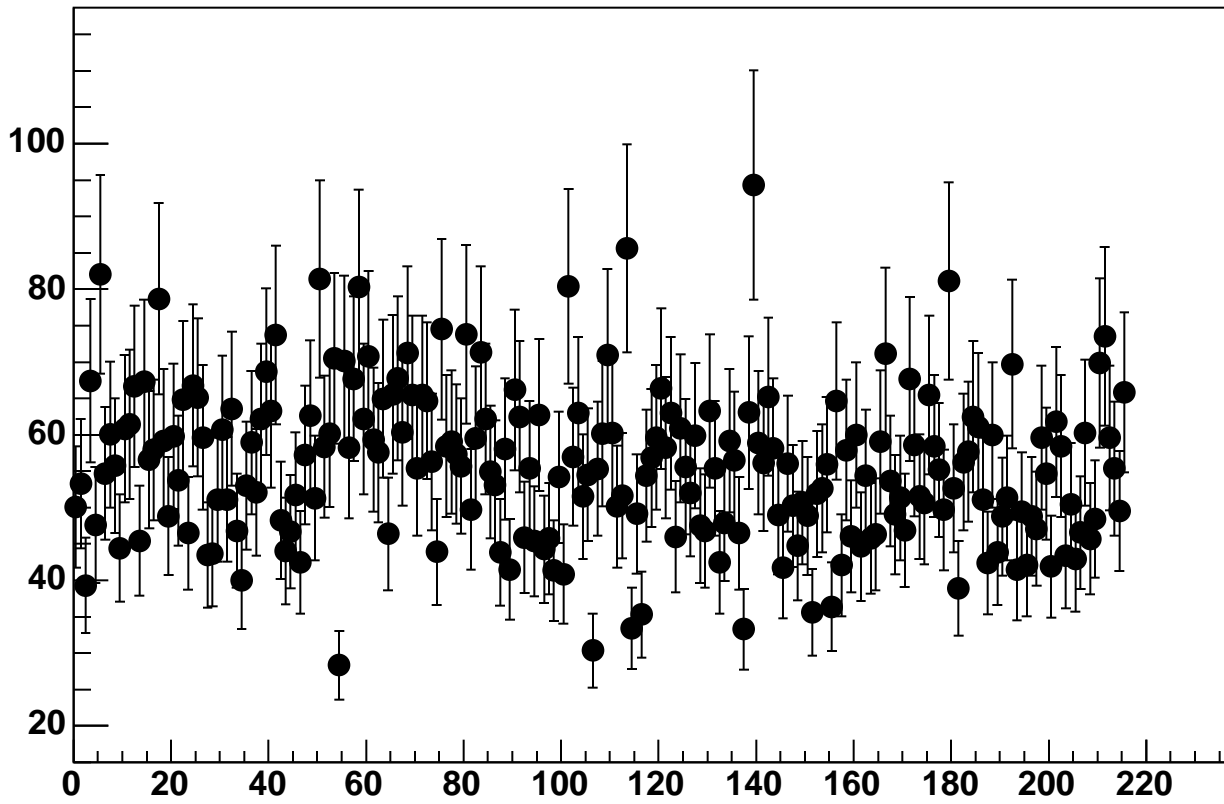
Enable 1, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



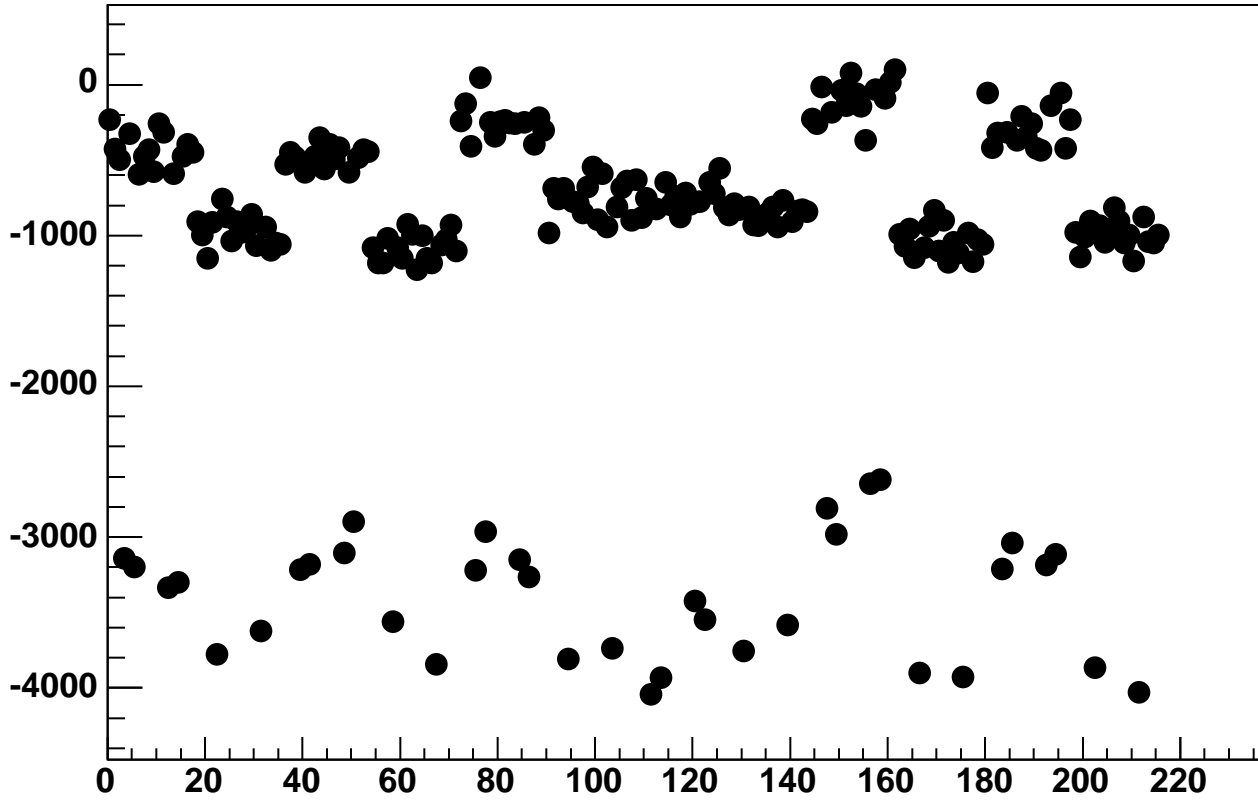
Enable 1, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan



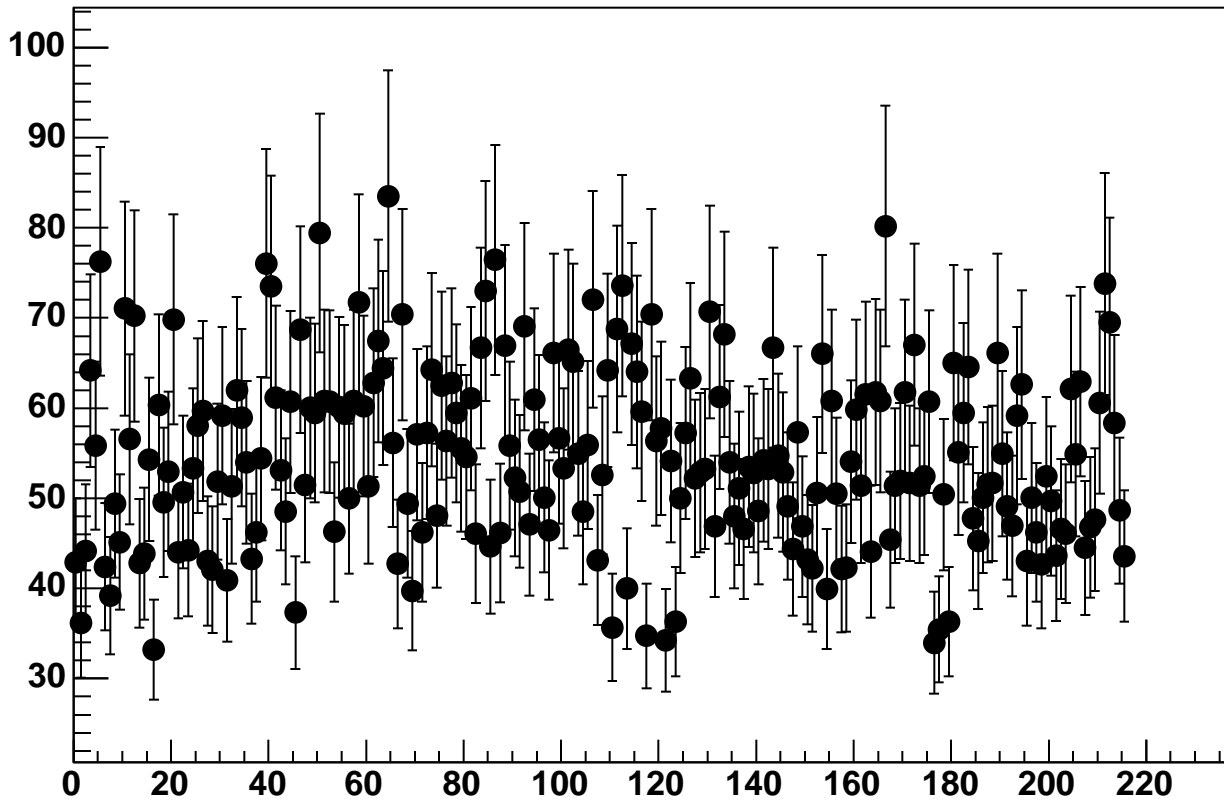
Enable 1, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan



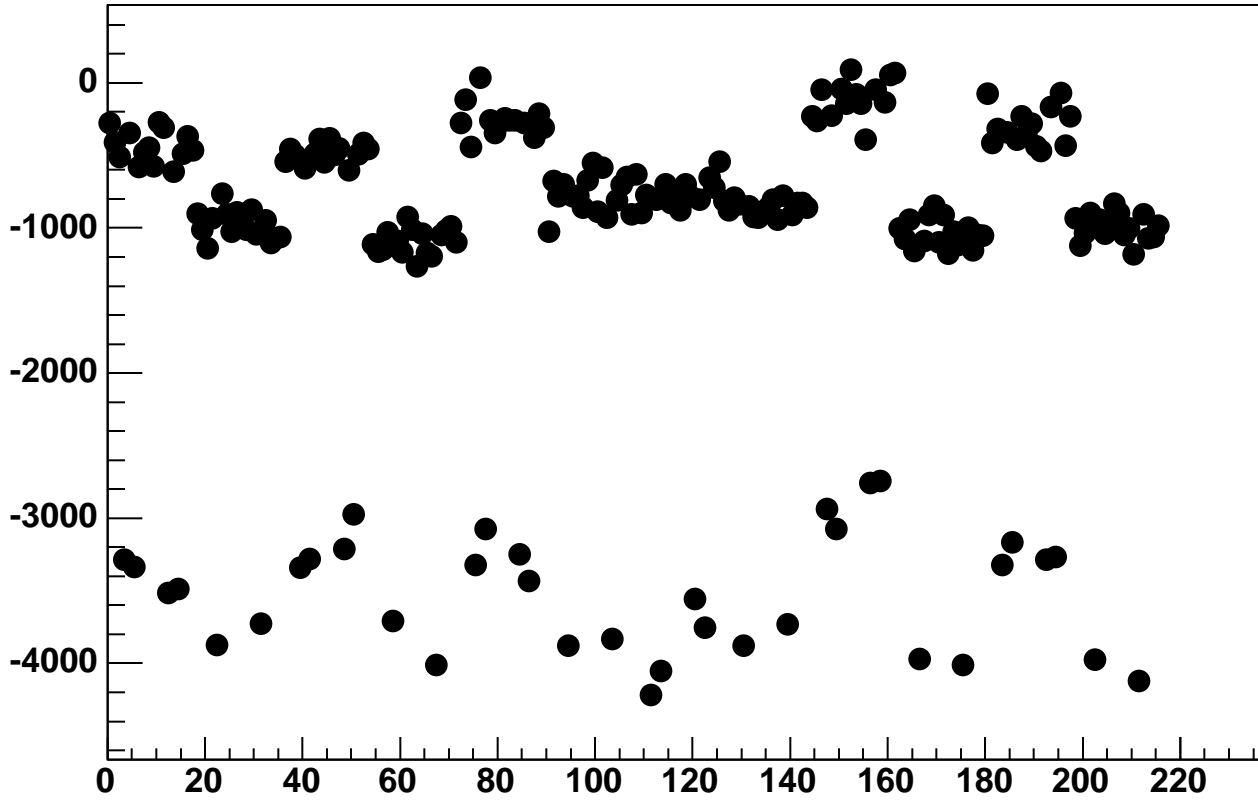
Enable 1, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



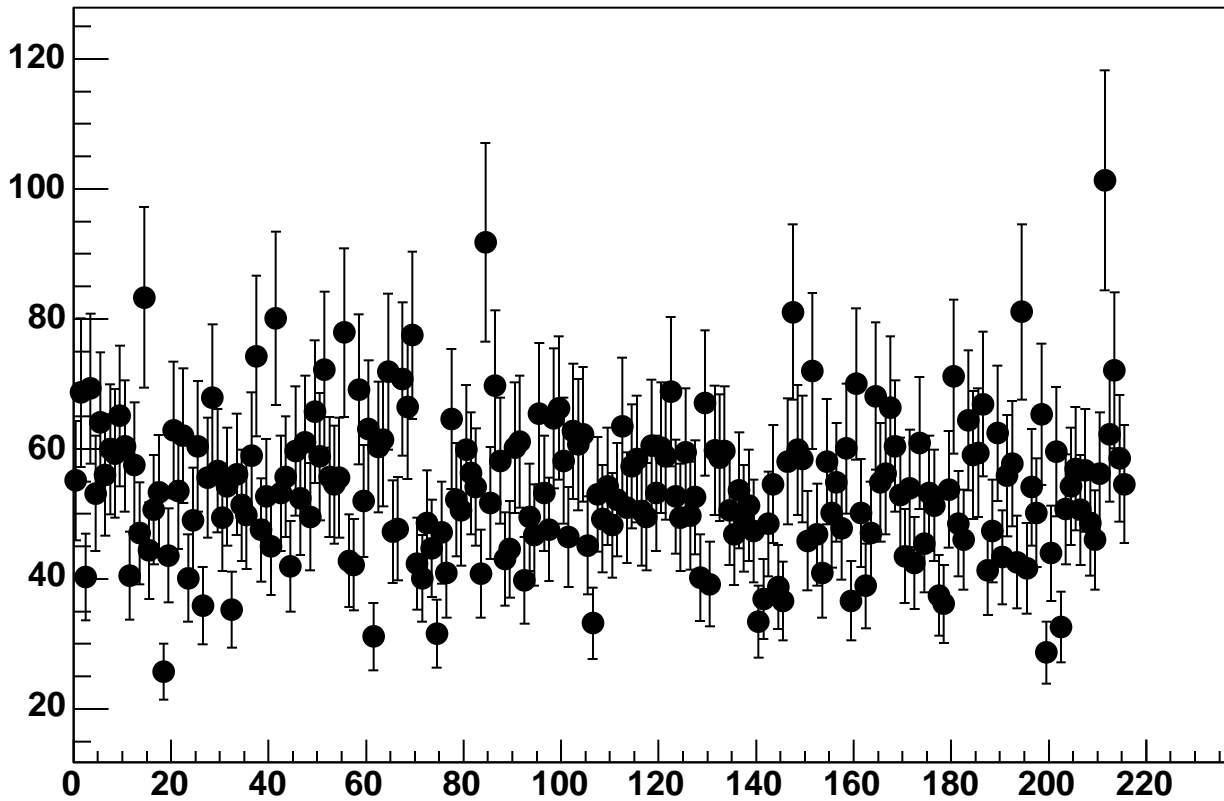
Enable 1, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



Enable 1, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan

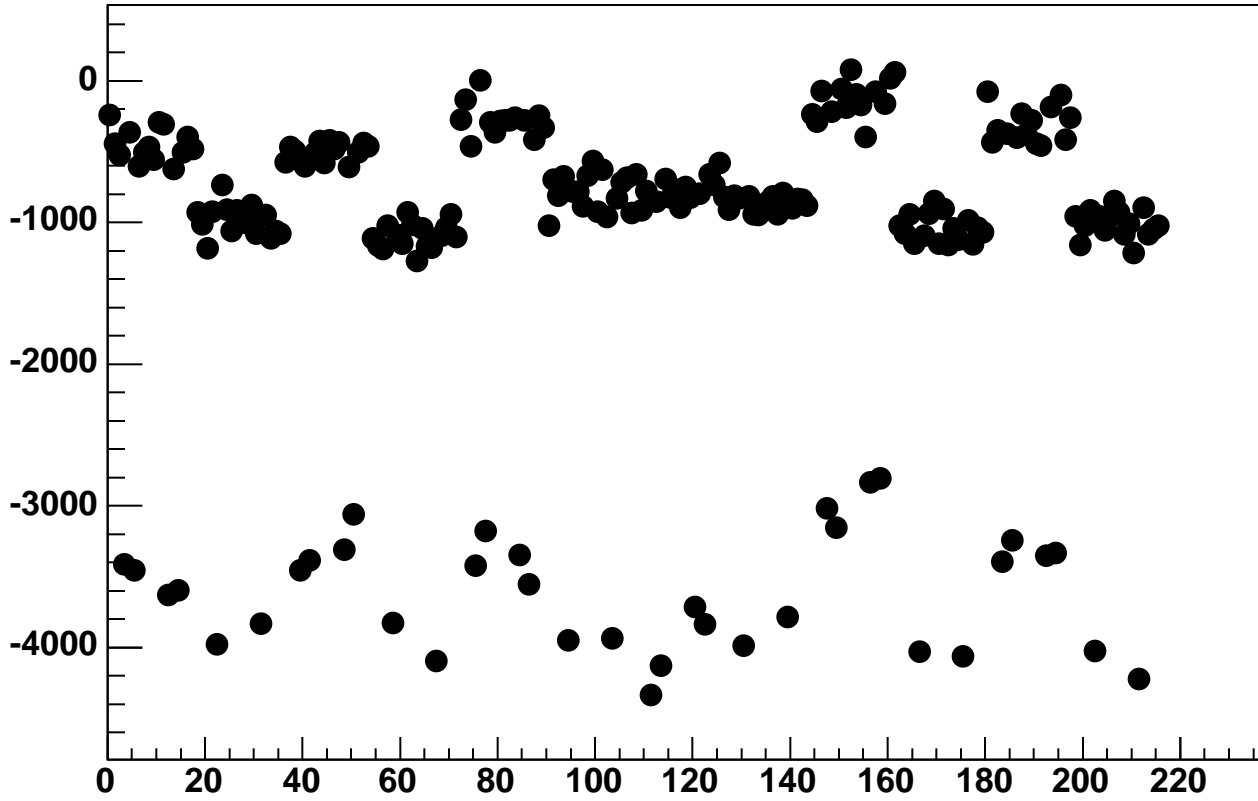


Enable 1, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan

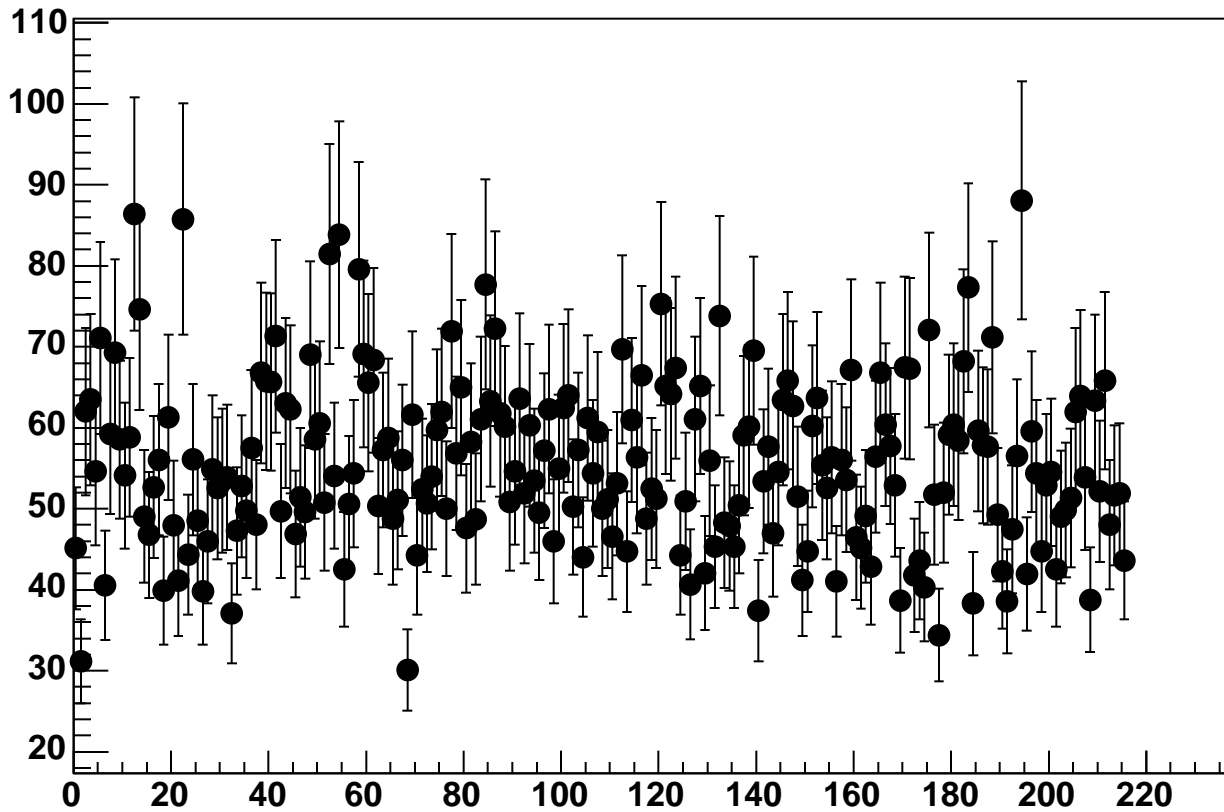




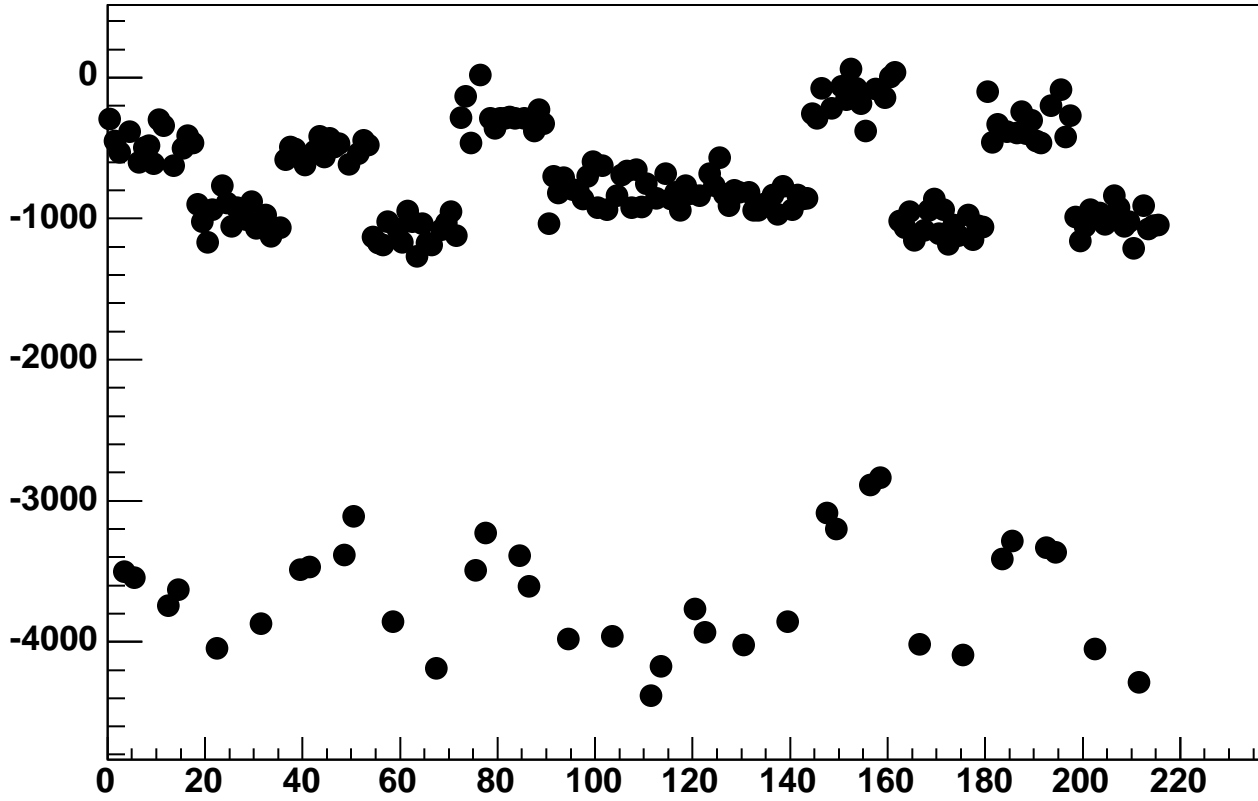
Enable 1, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



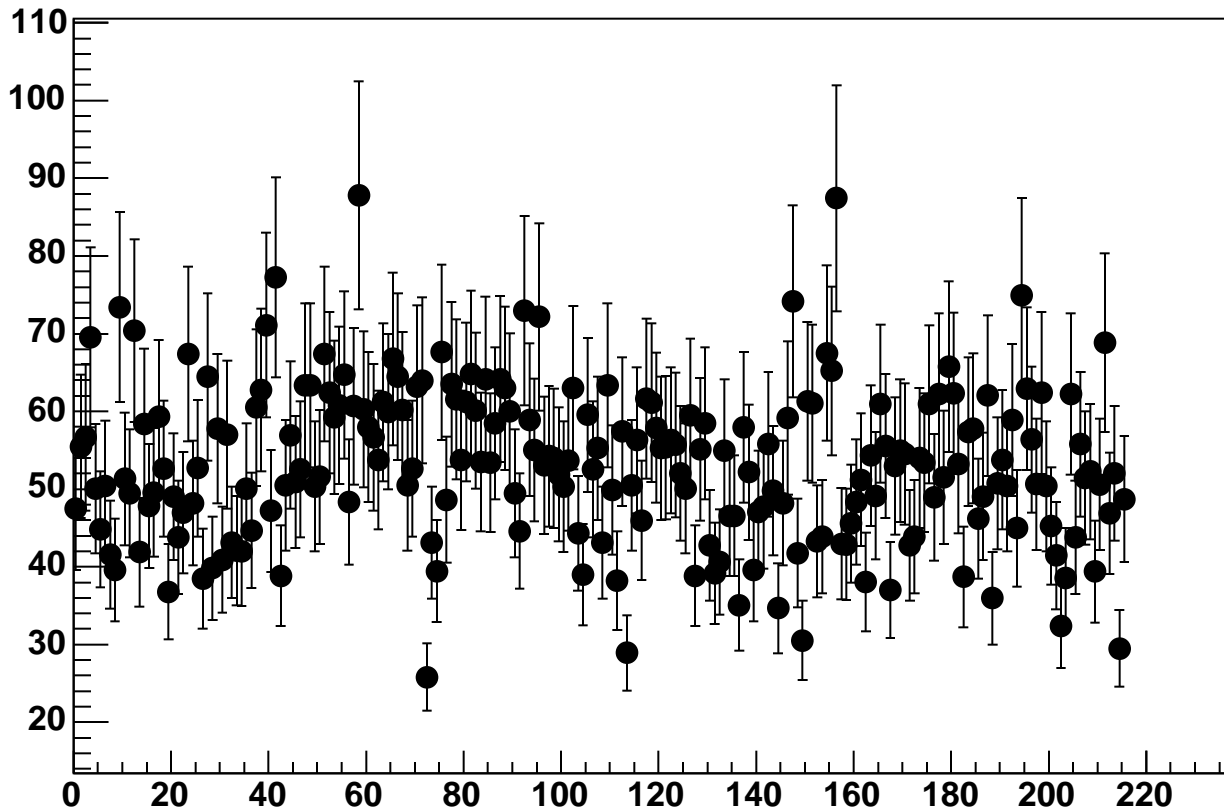
Enable 1, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



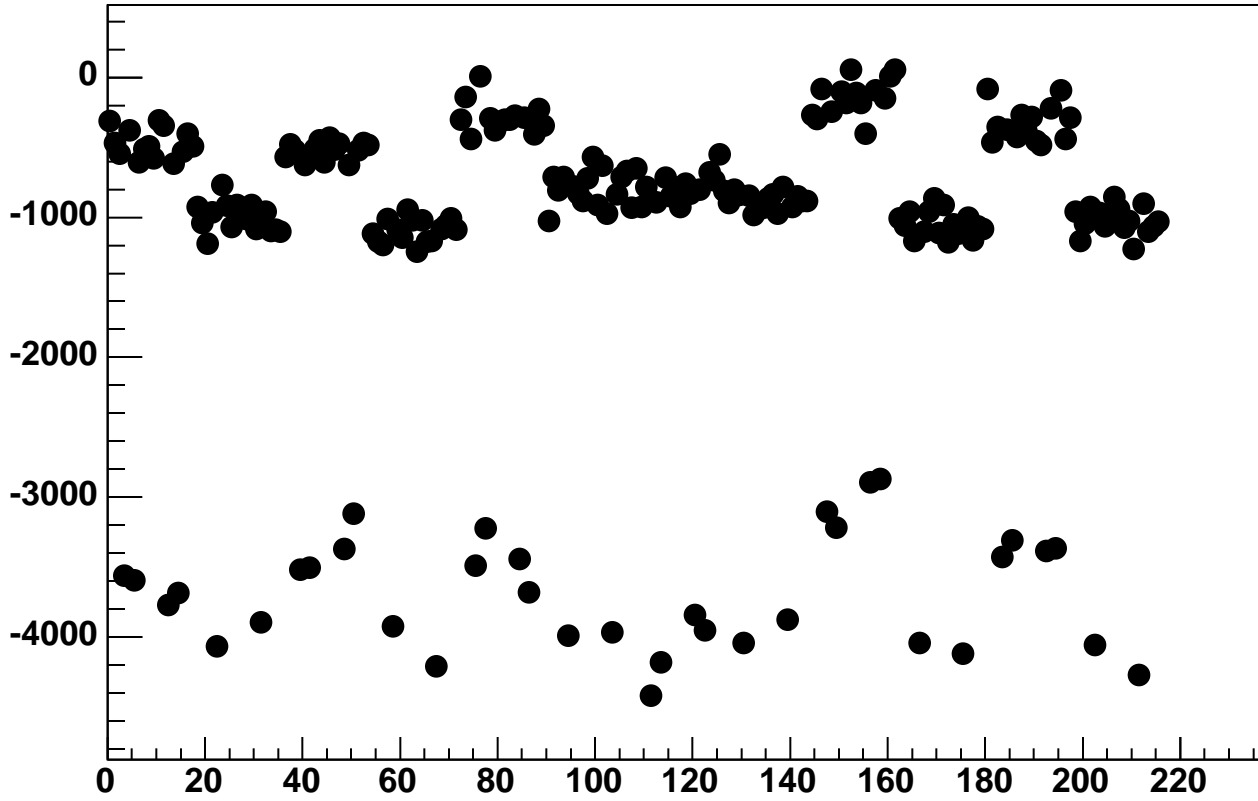
Enable 1, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan



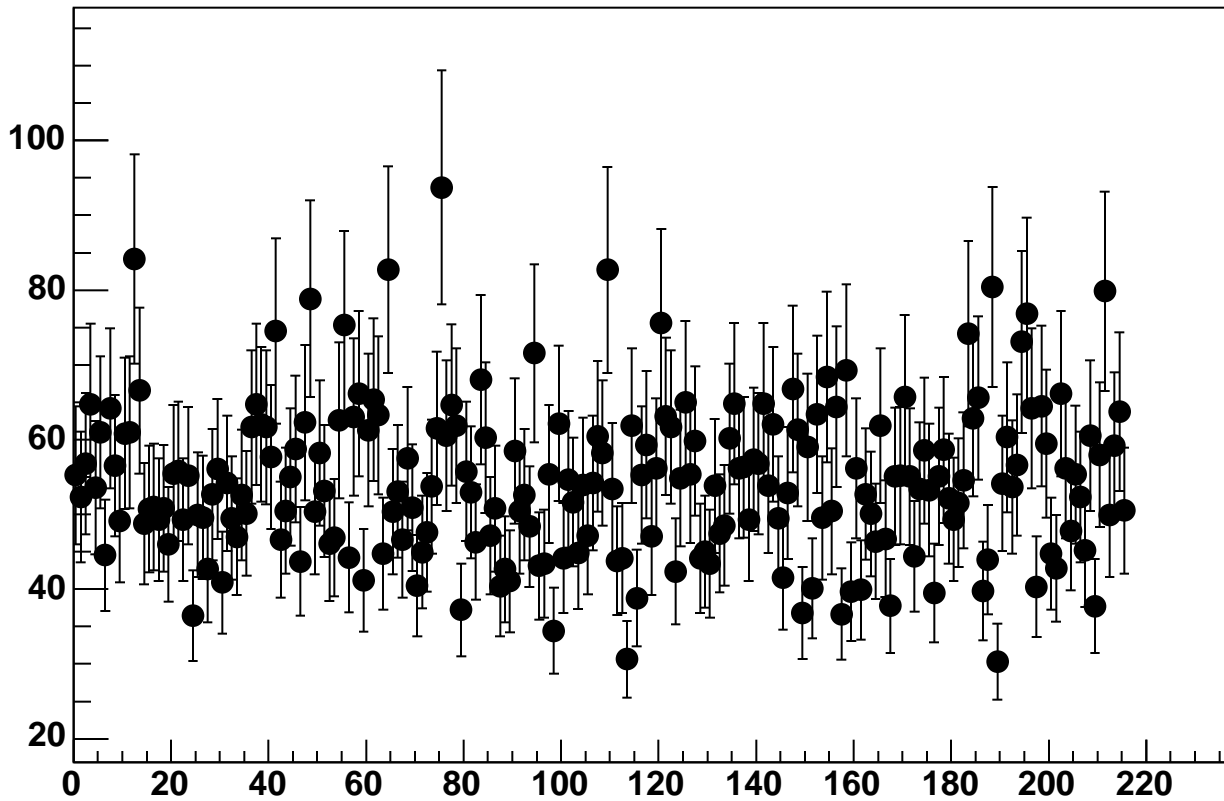
Enable 1, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan



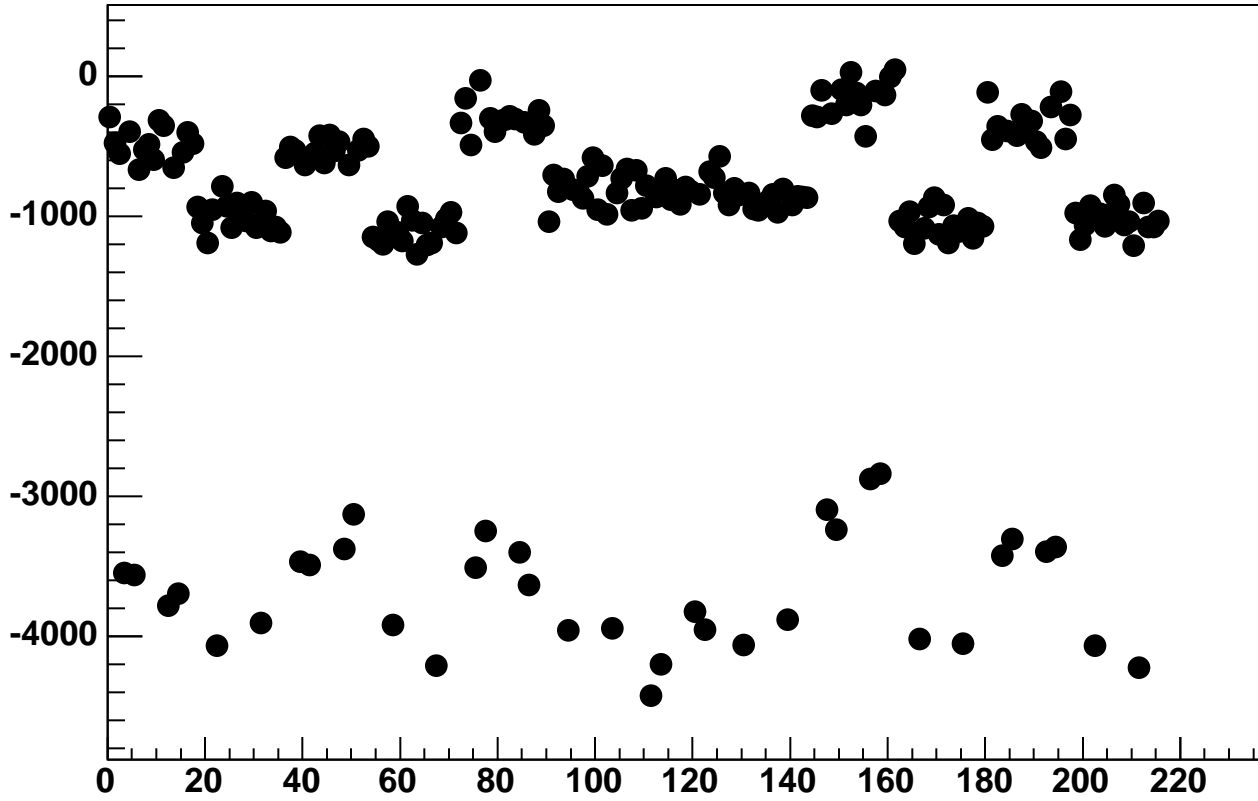
Enable 1, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



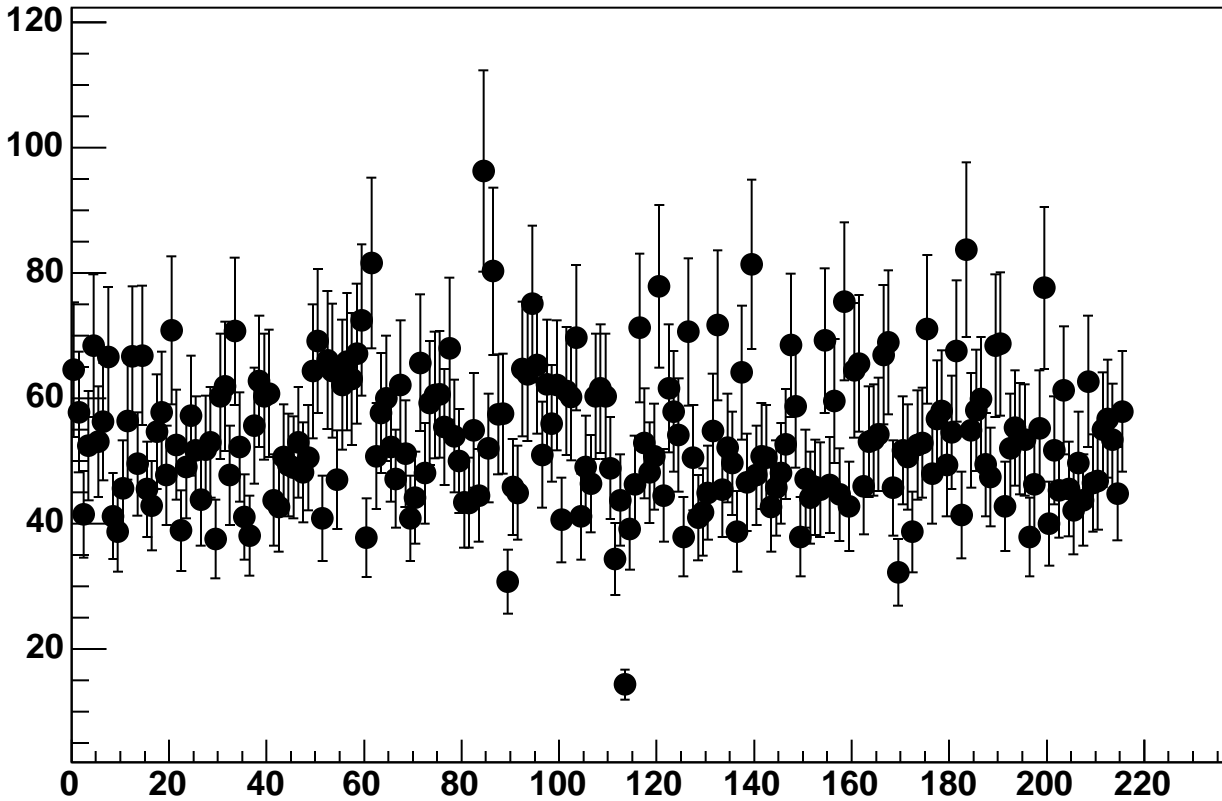
Enable 1, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



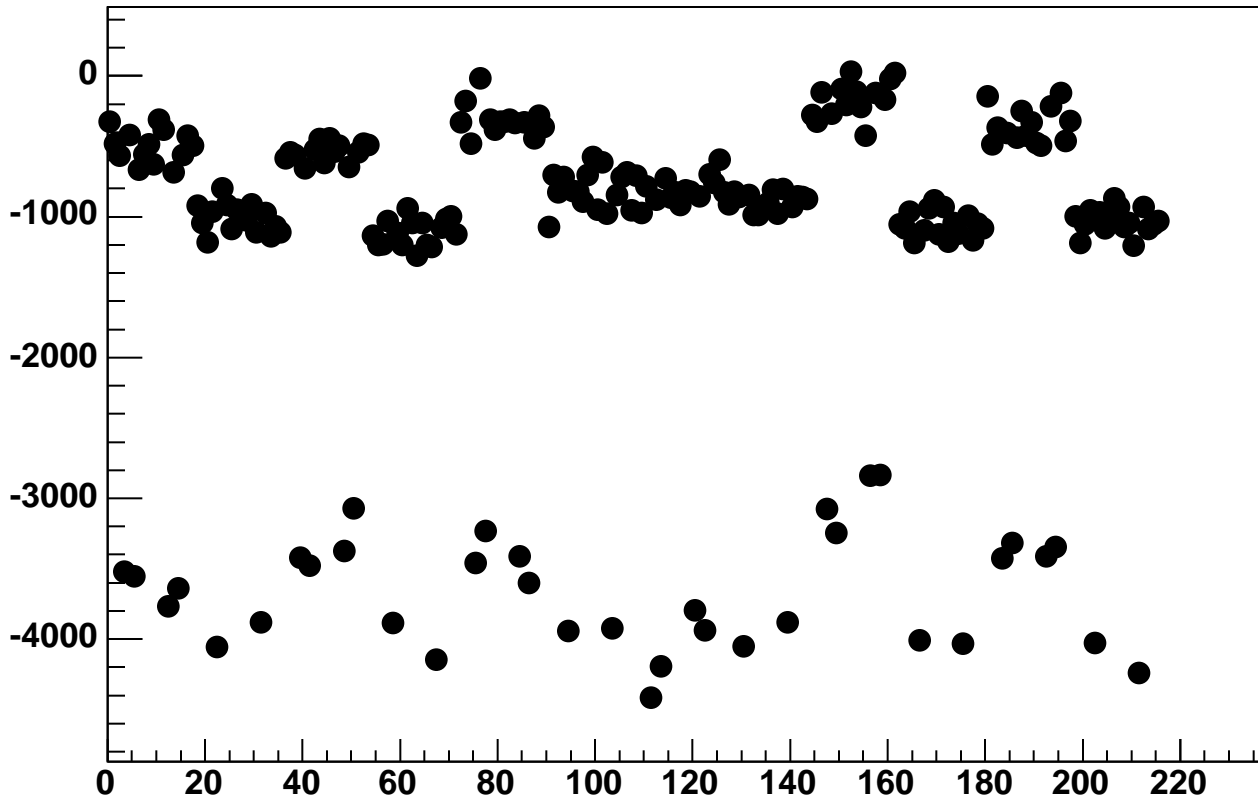
Enable 1, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan



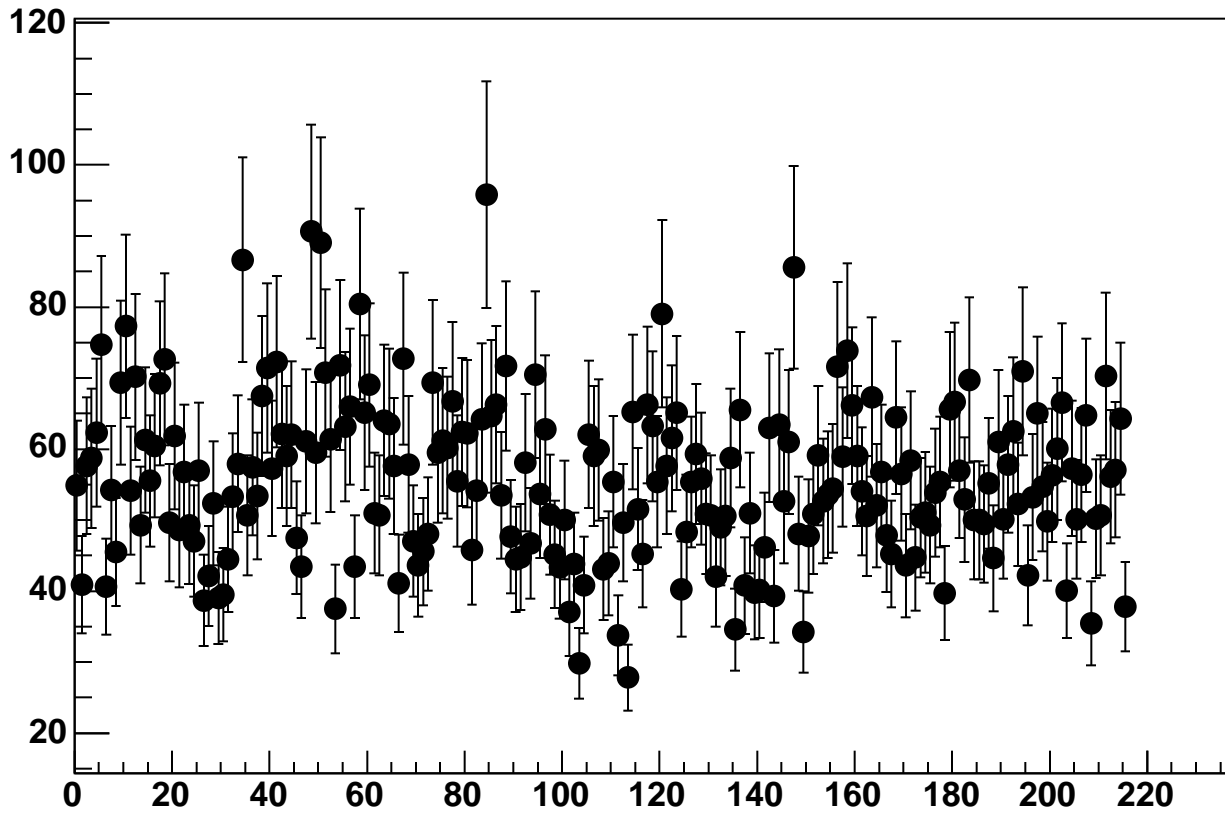
Enable 1, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan



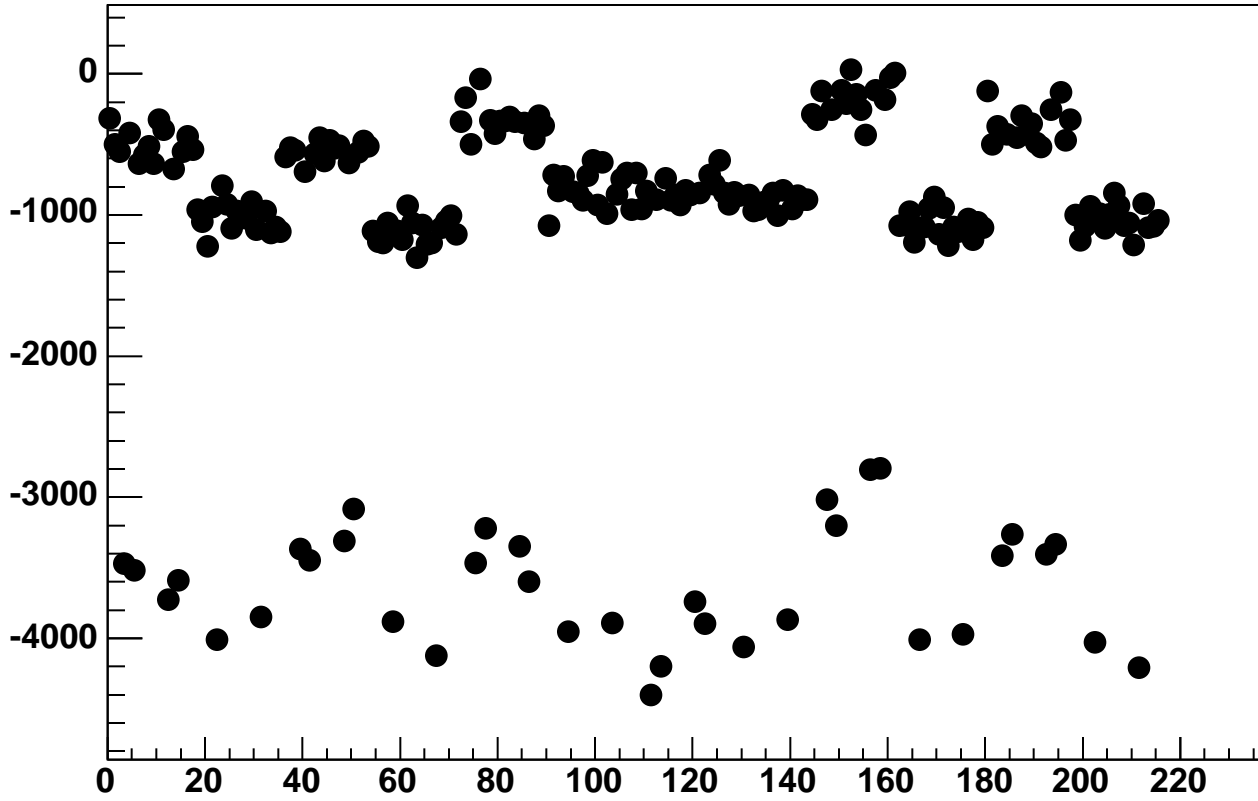
Enable 1, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



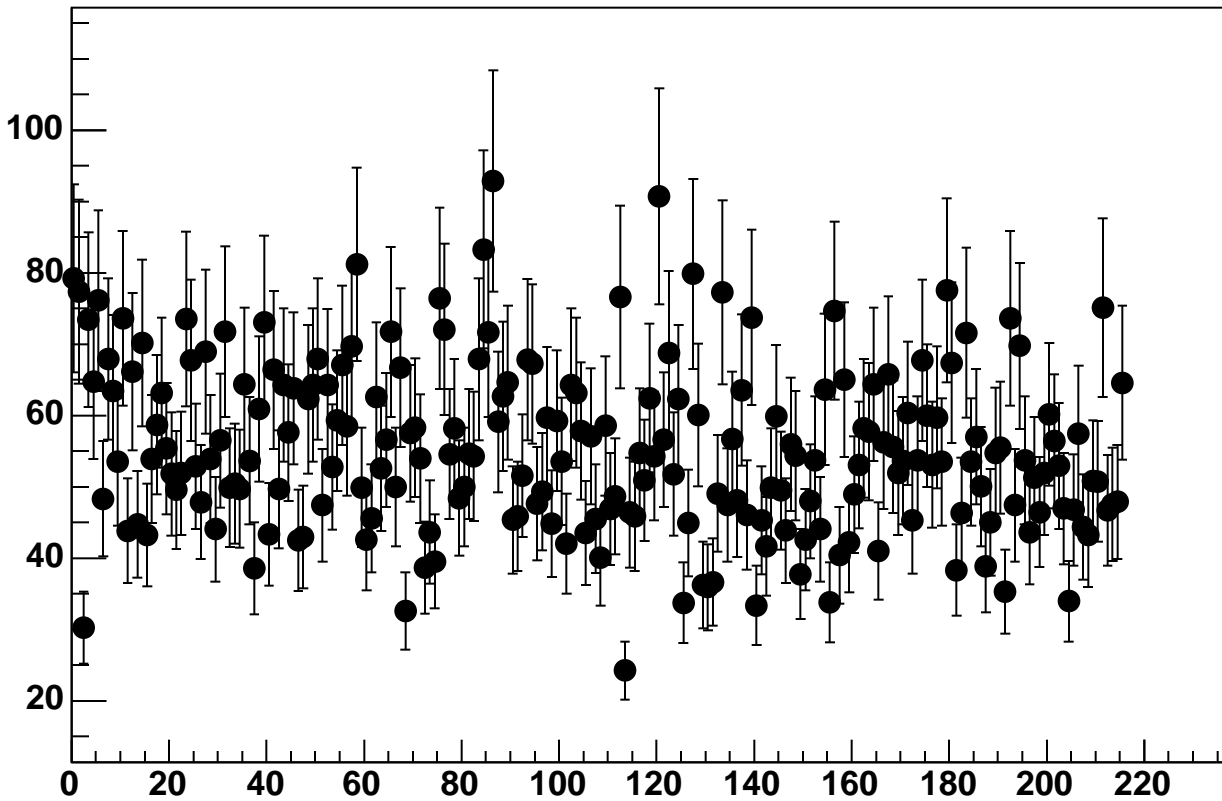
Enable 1, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



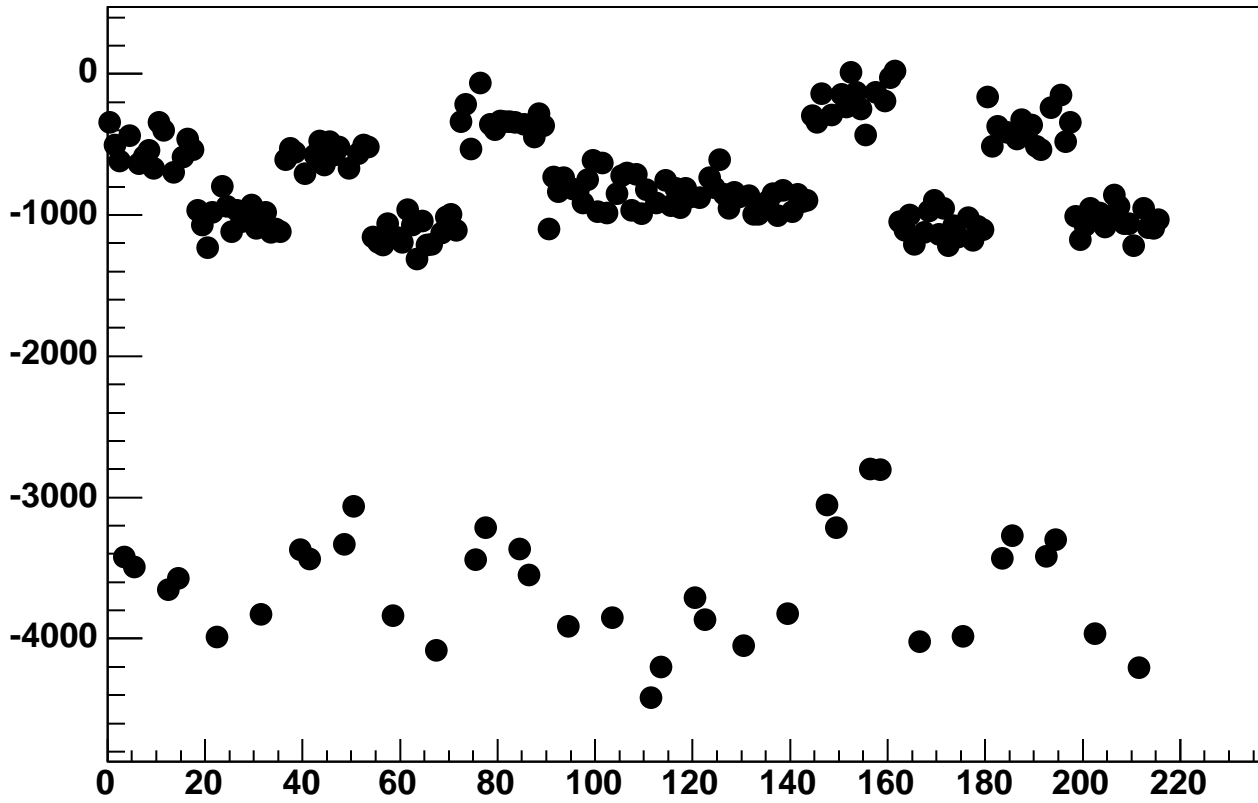
Enable 1, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan



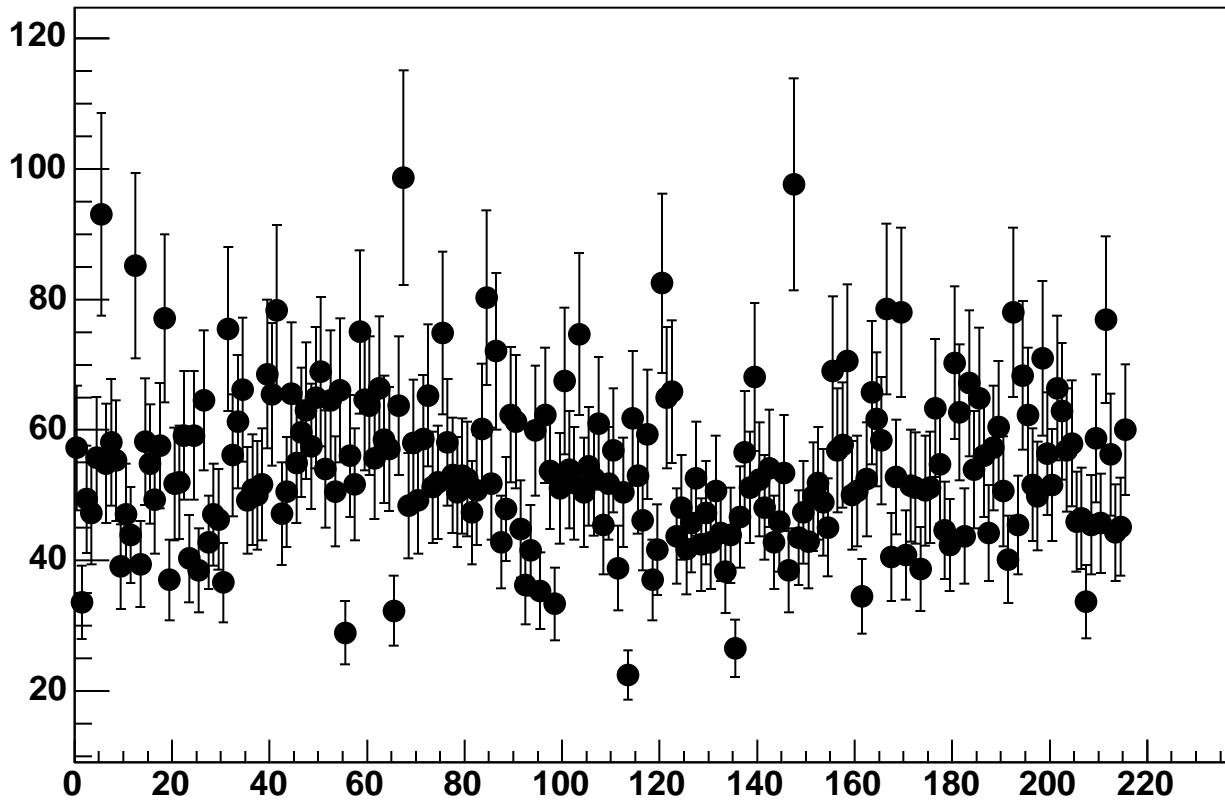
Enable 1, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan



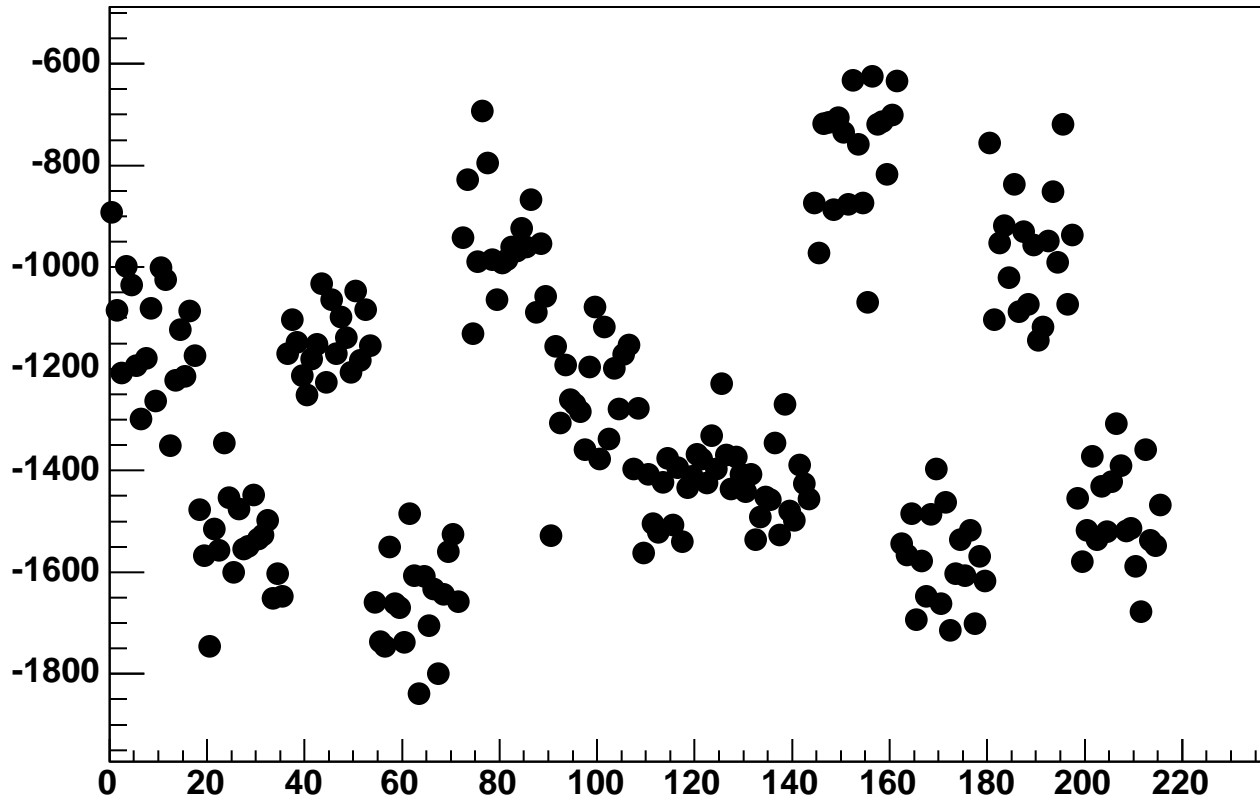
Enable 1, DAC=1600, Hold=245, ADC Mean vs 18\*Chip+Chan



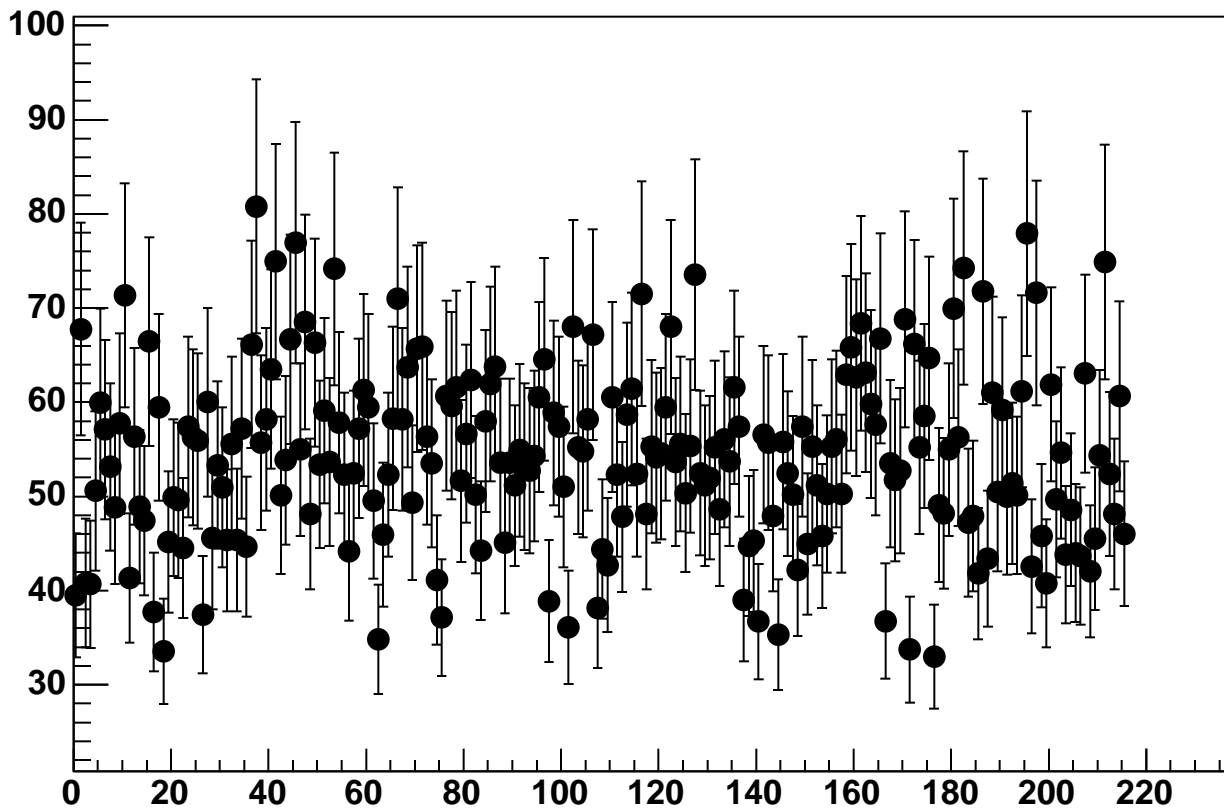
Enable 1, DAC=1600, Hold=245, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan

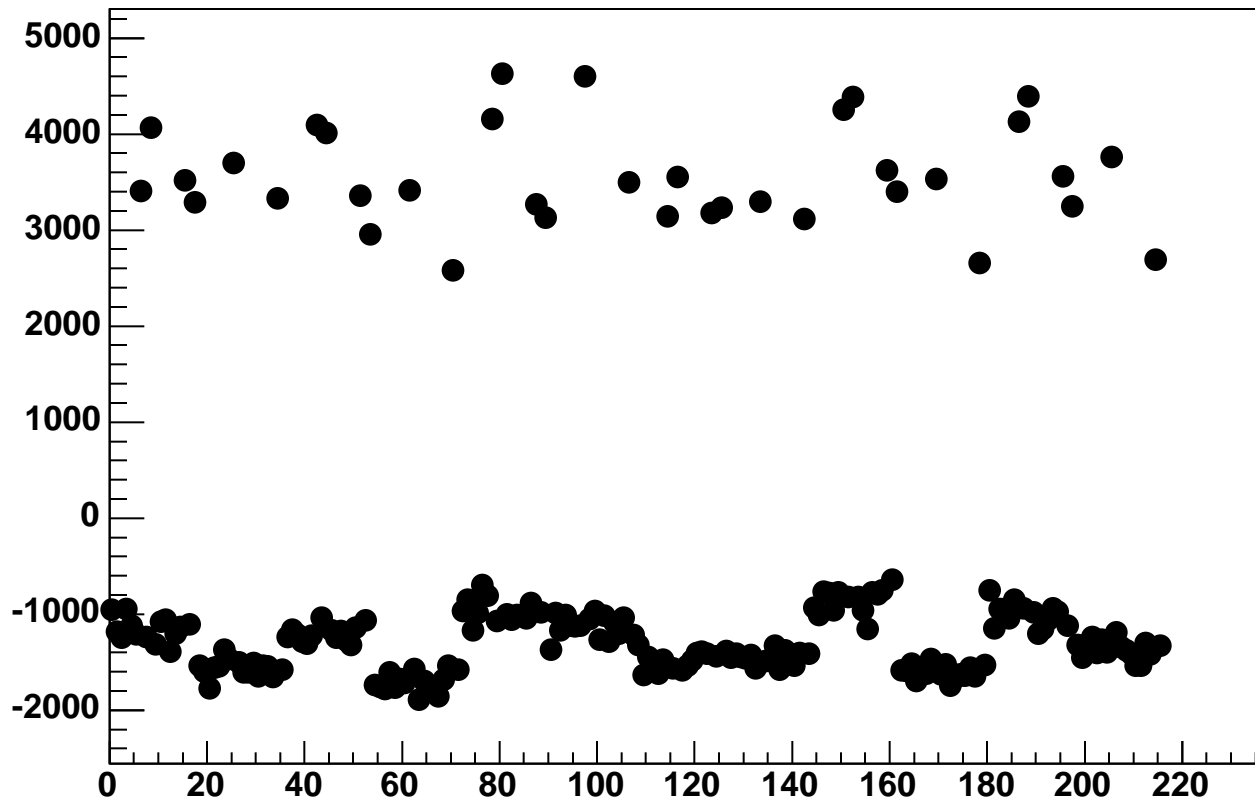


Enable 2, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan

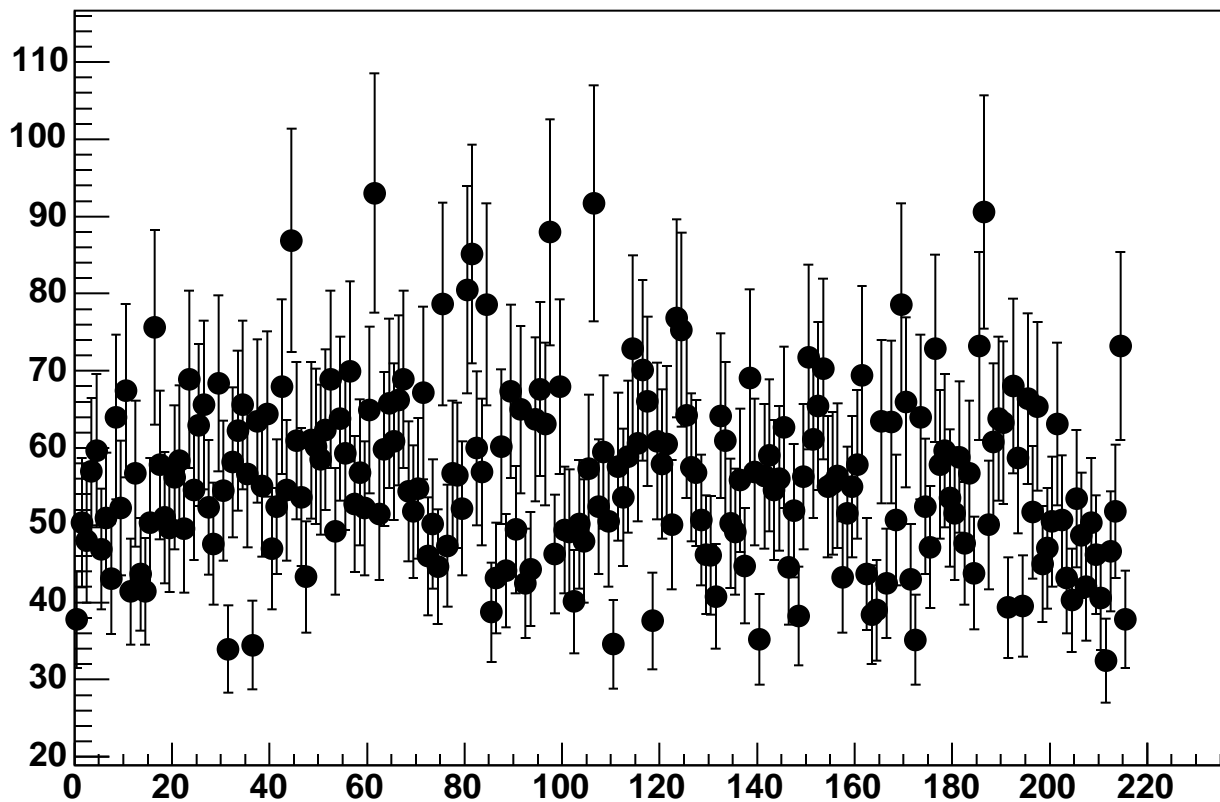




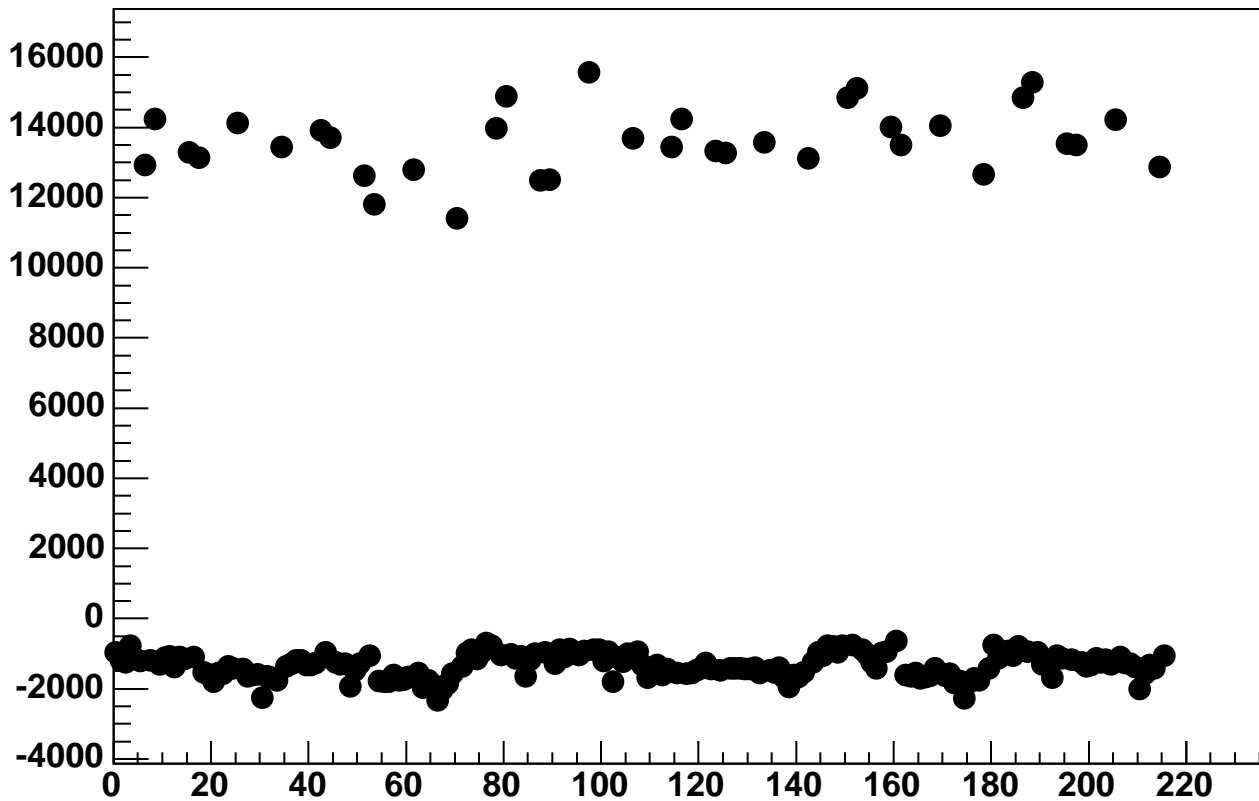
Enable 2, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



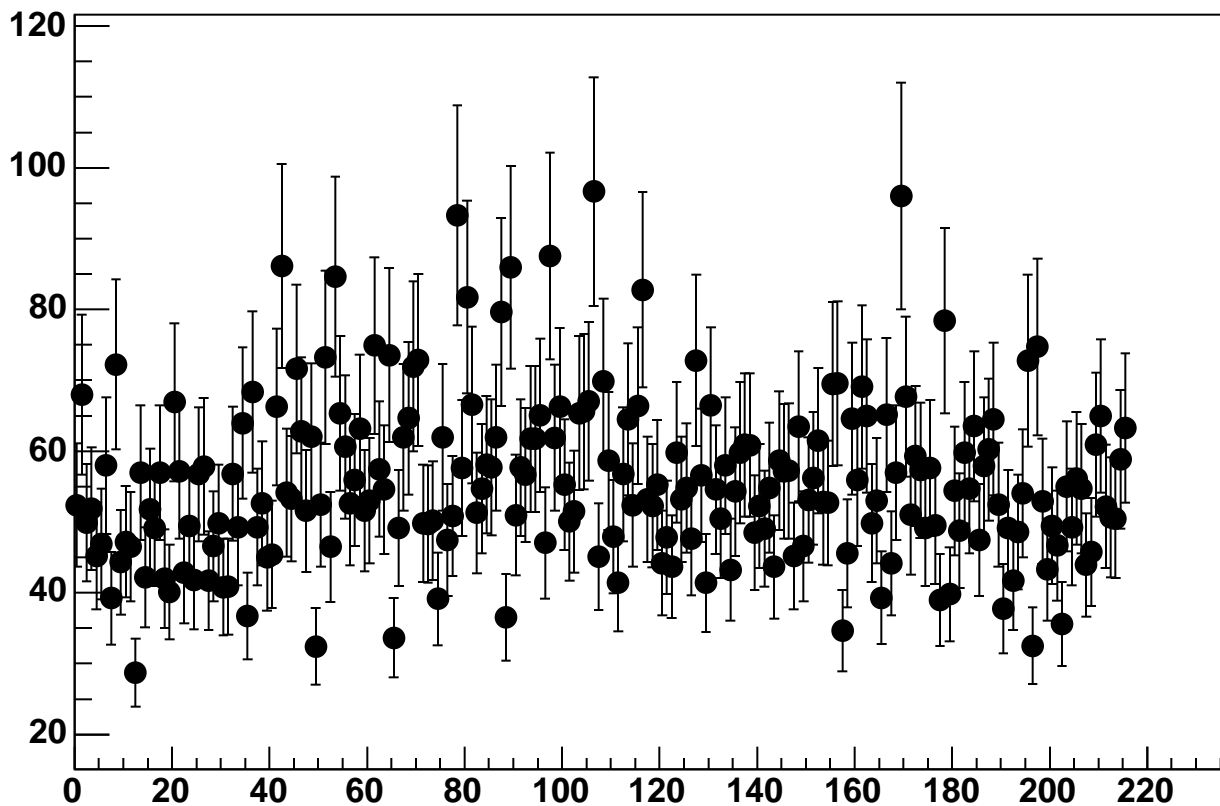
Enable 2, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



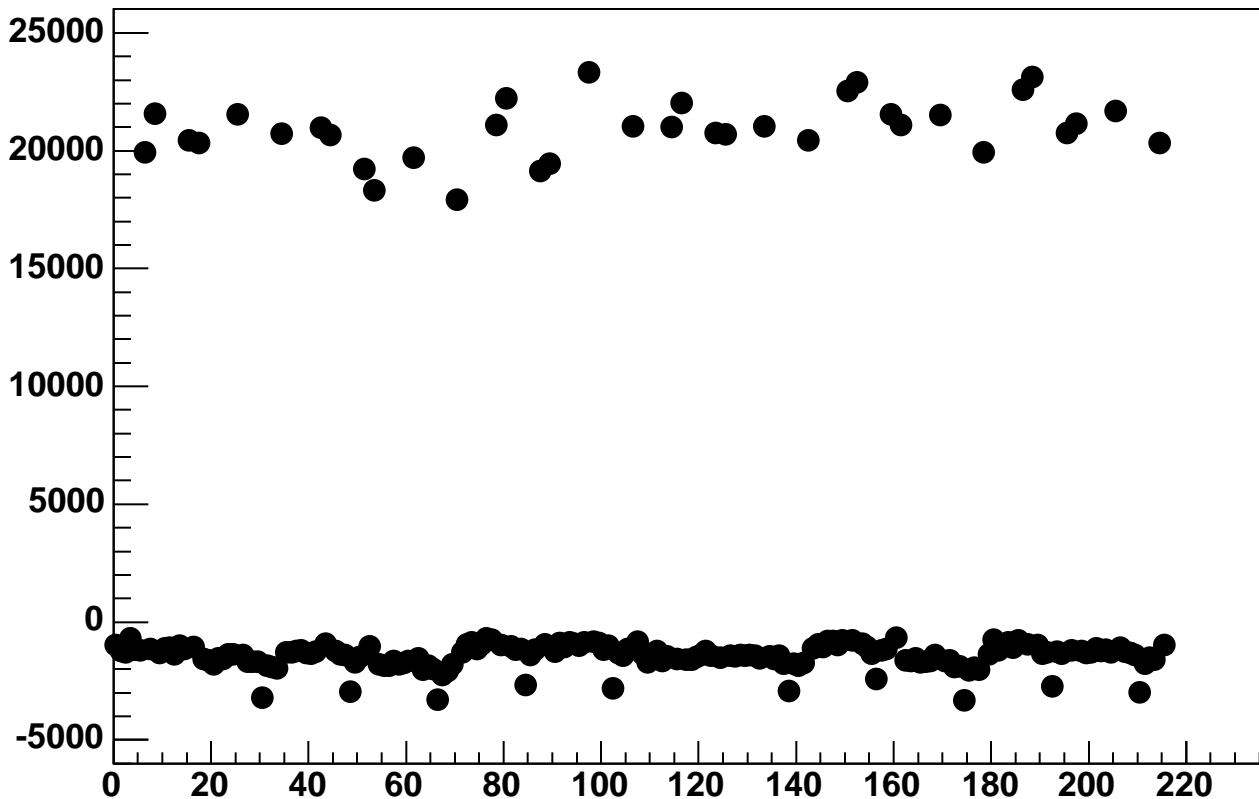
Enable 2, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan



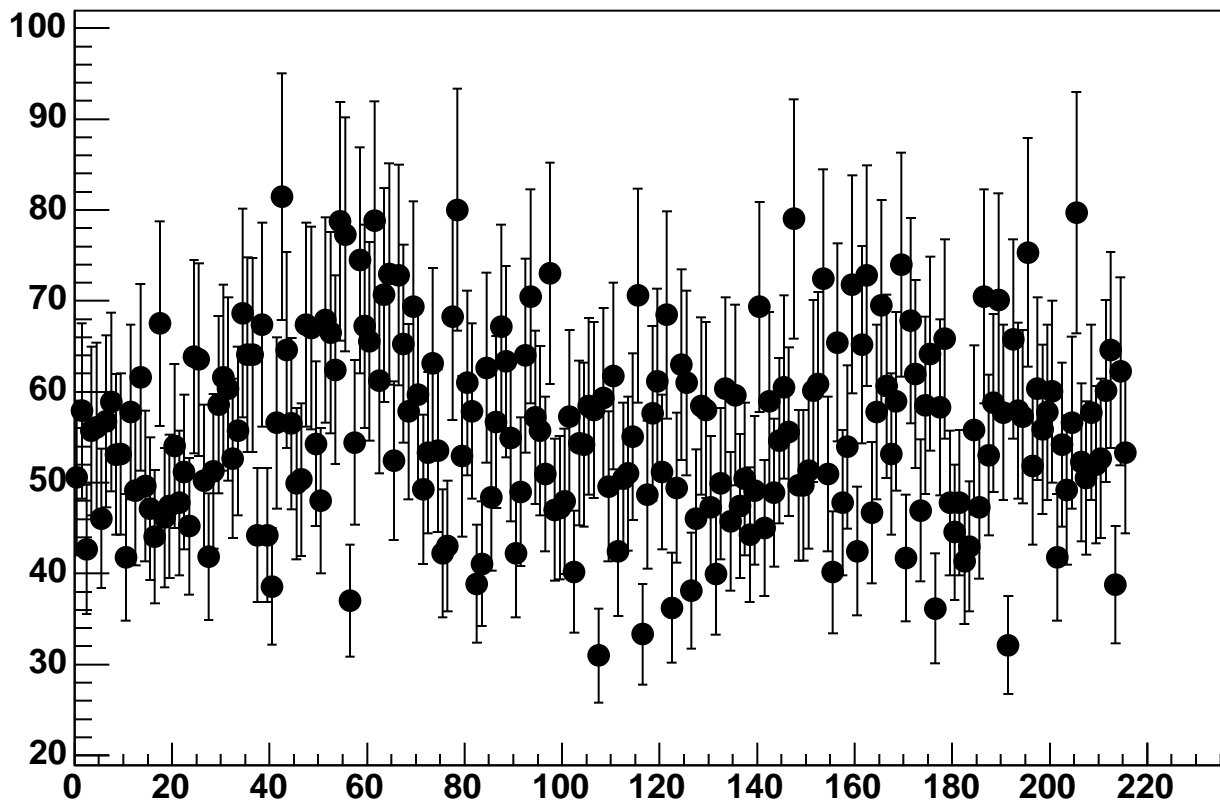
Enable 2, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan



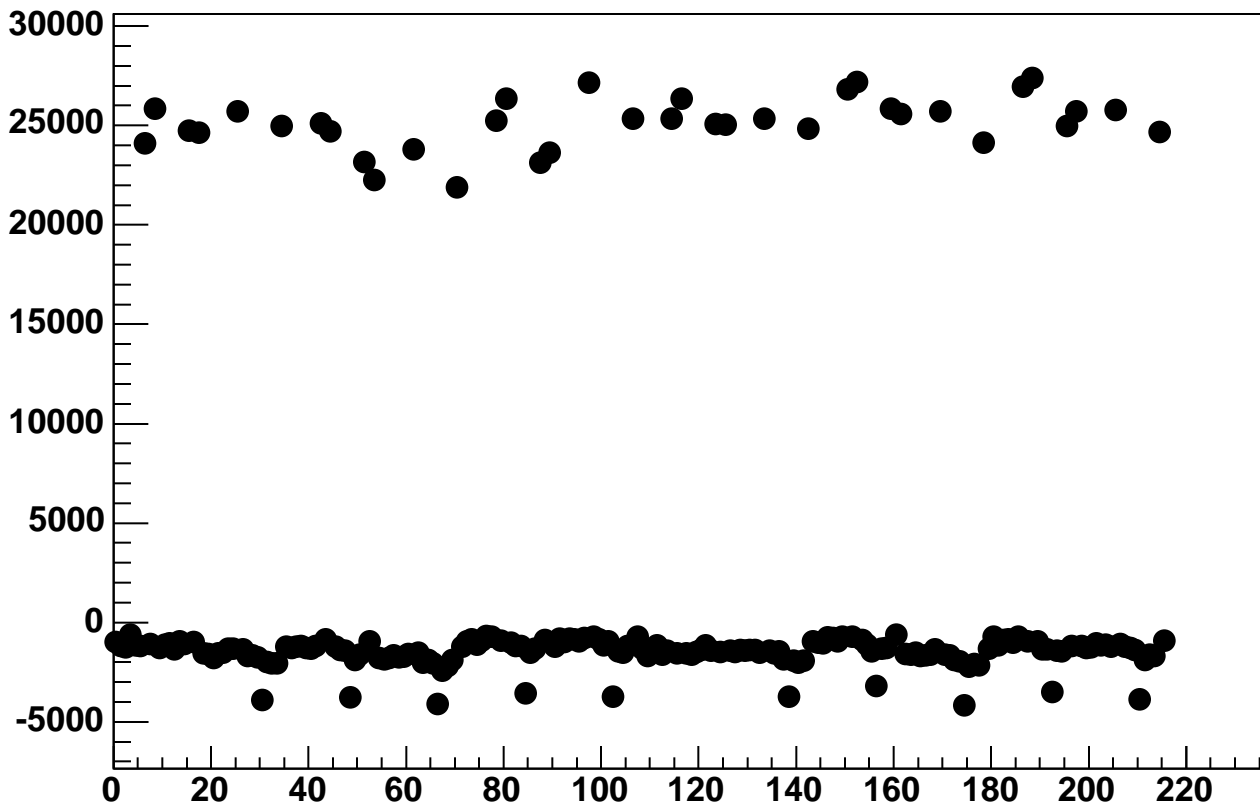
Enable 2, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



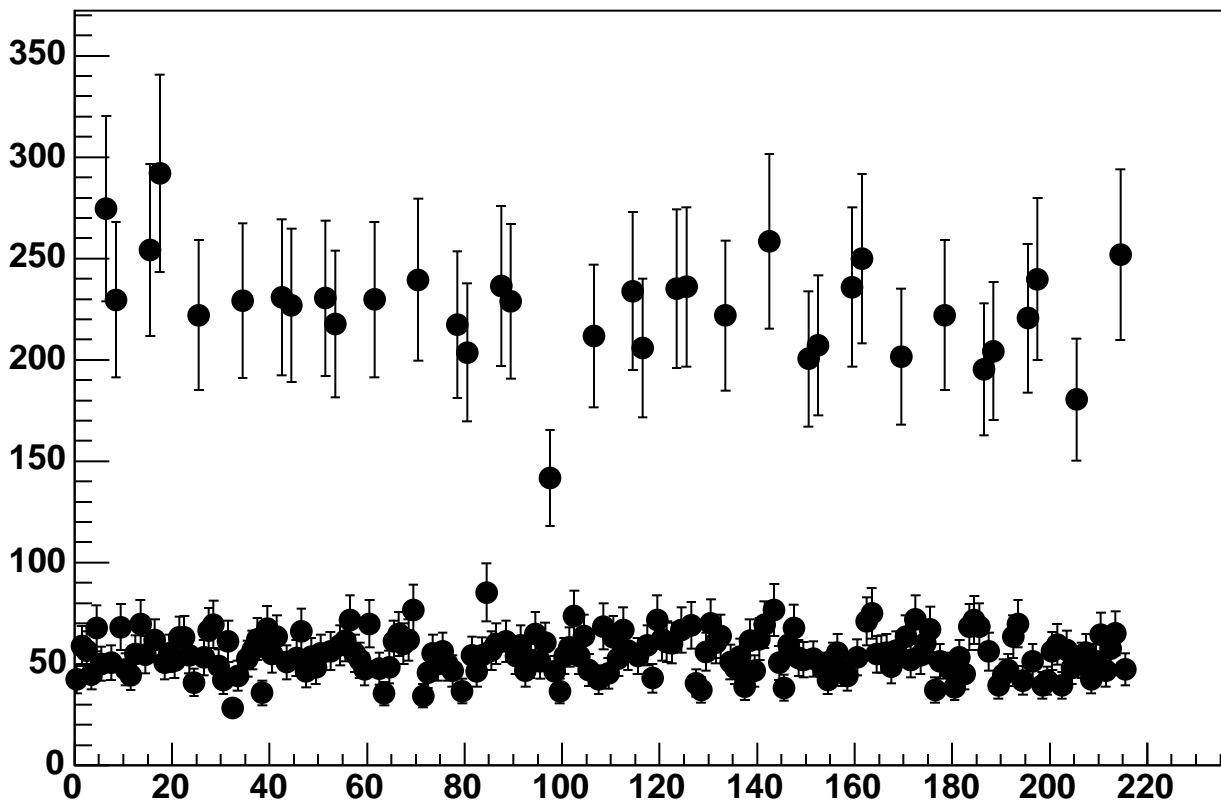
Enable 2, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



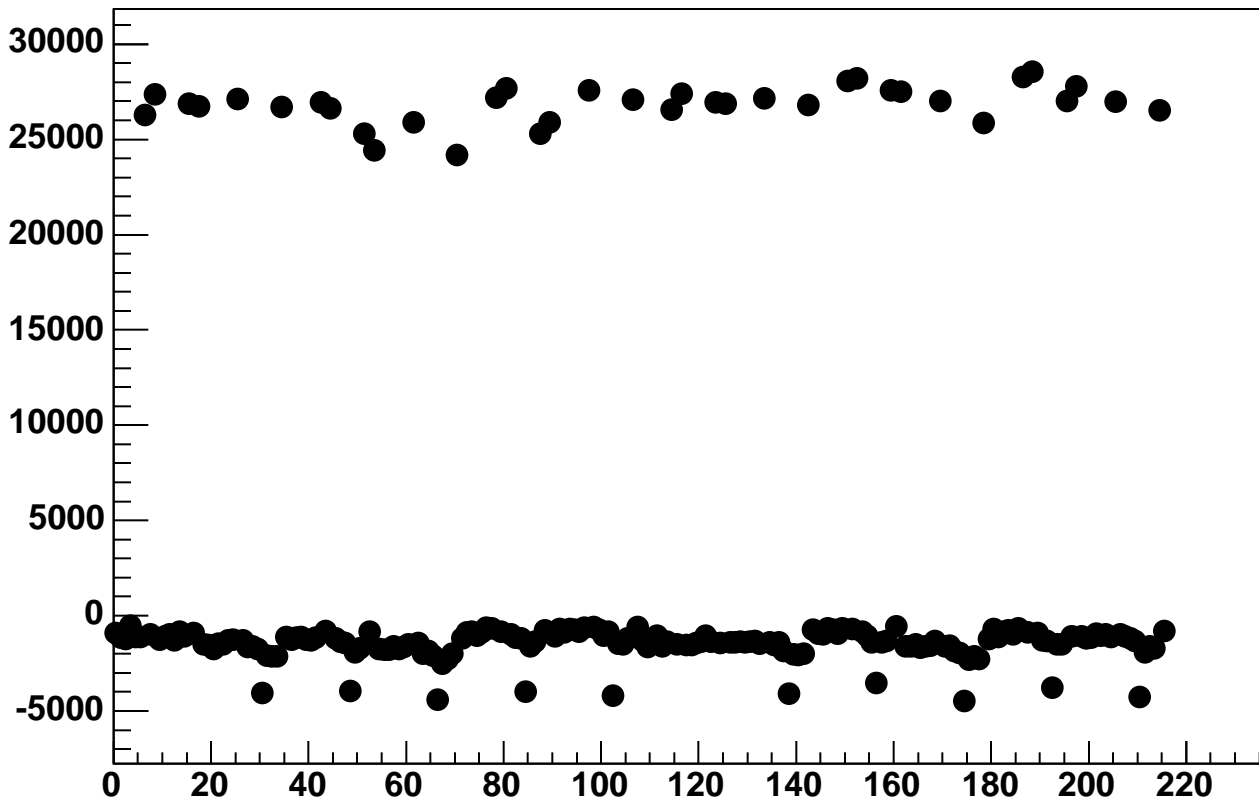
Enable 2, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan



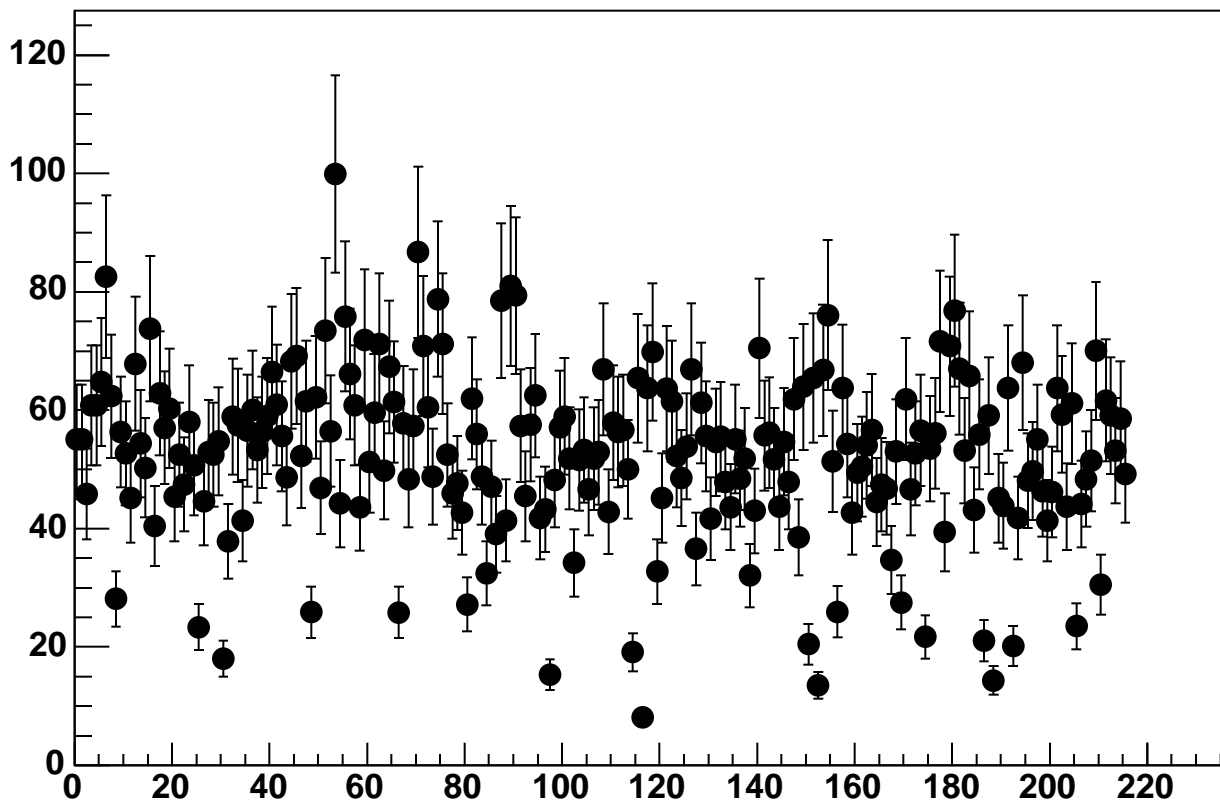
Enable 2, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan



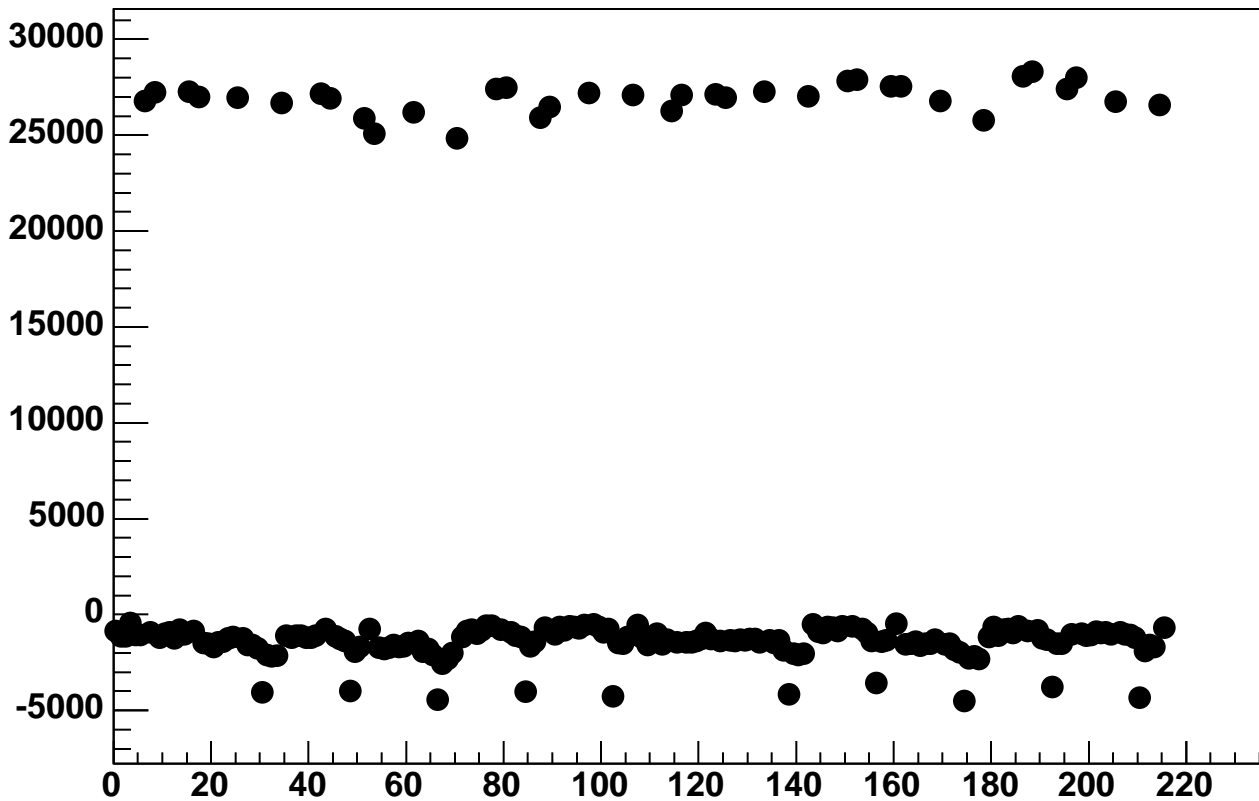
Enable 2, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



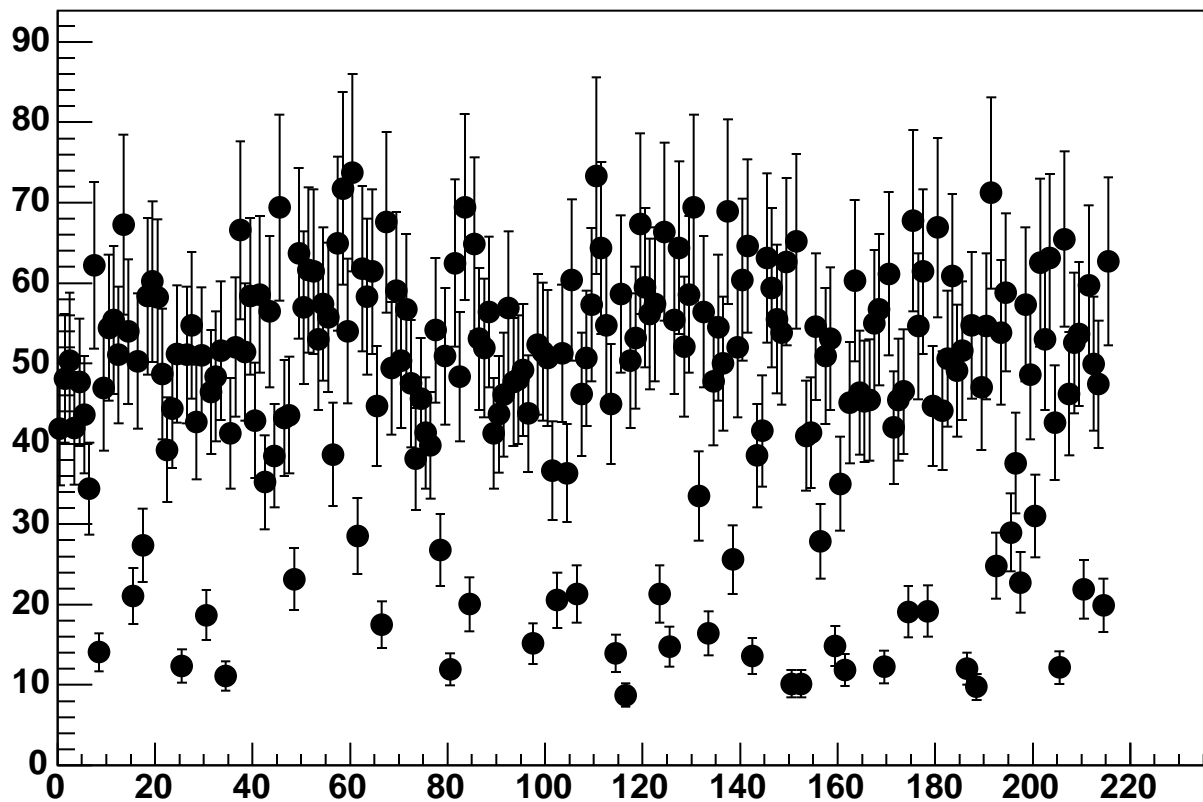
Enable 2, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



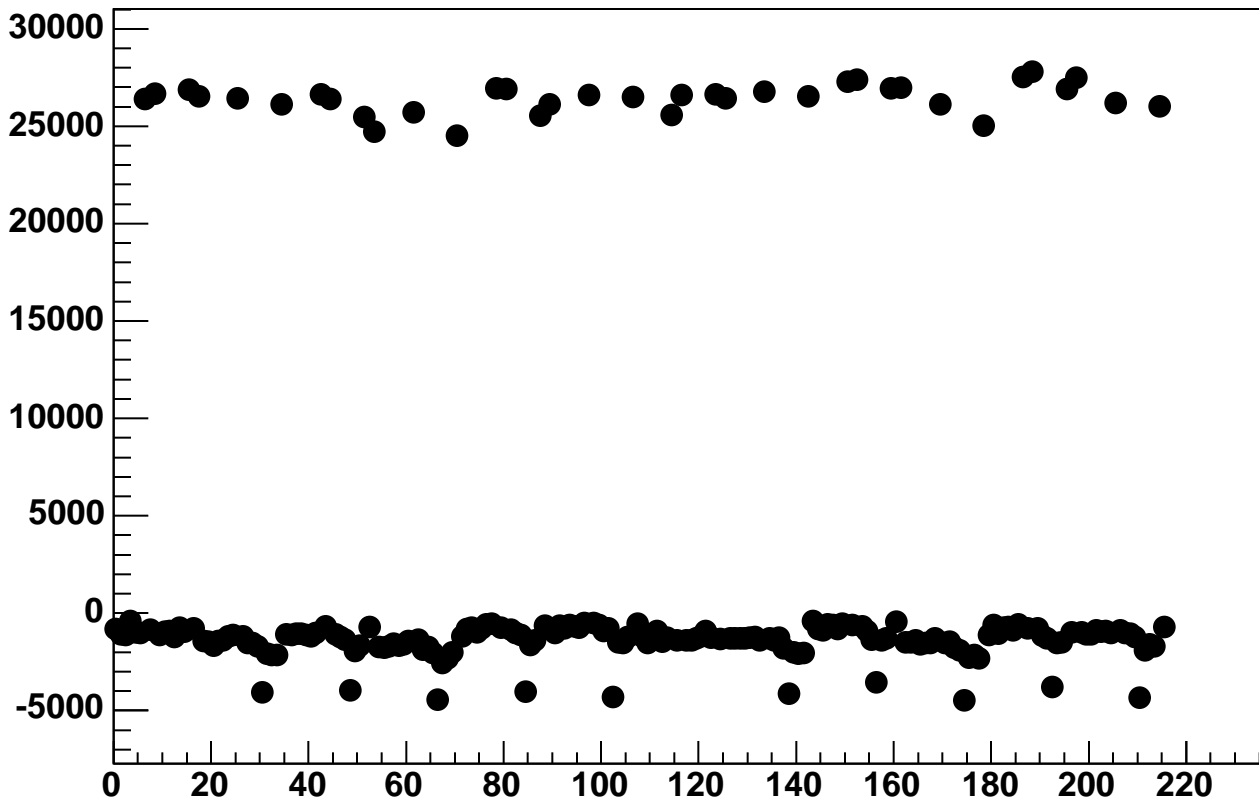
Enable 2, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan



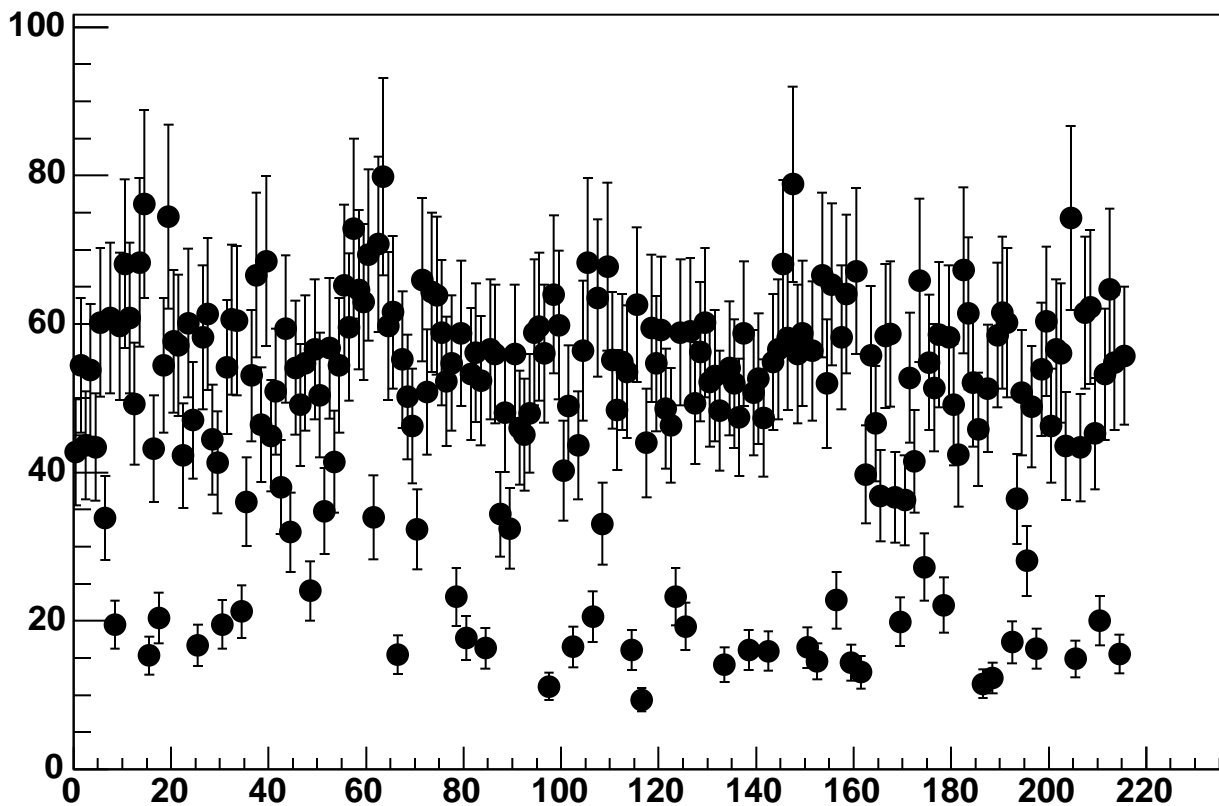
Enable 2, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan



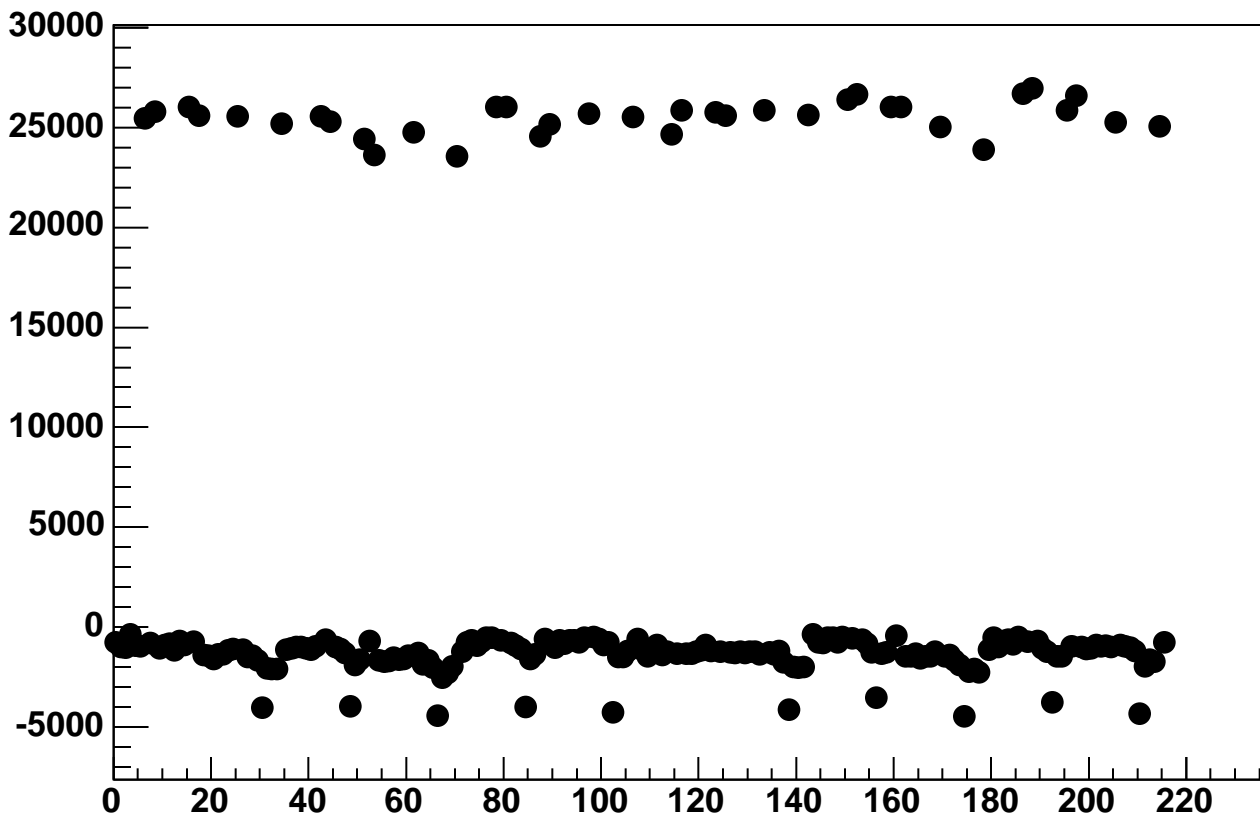
Enable 2, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



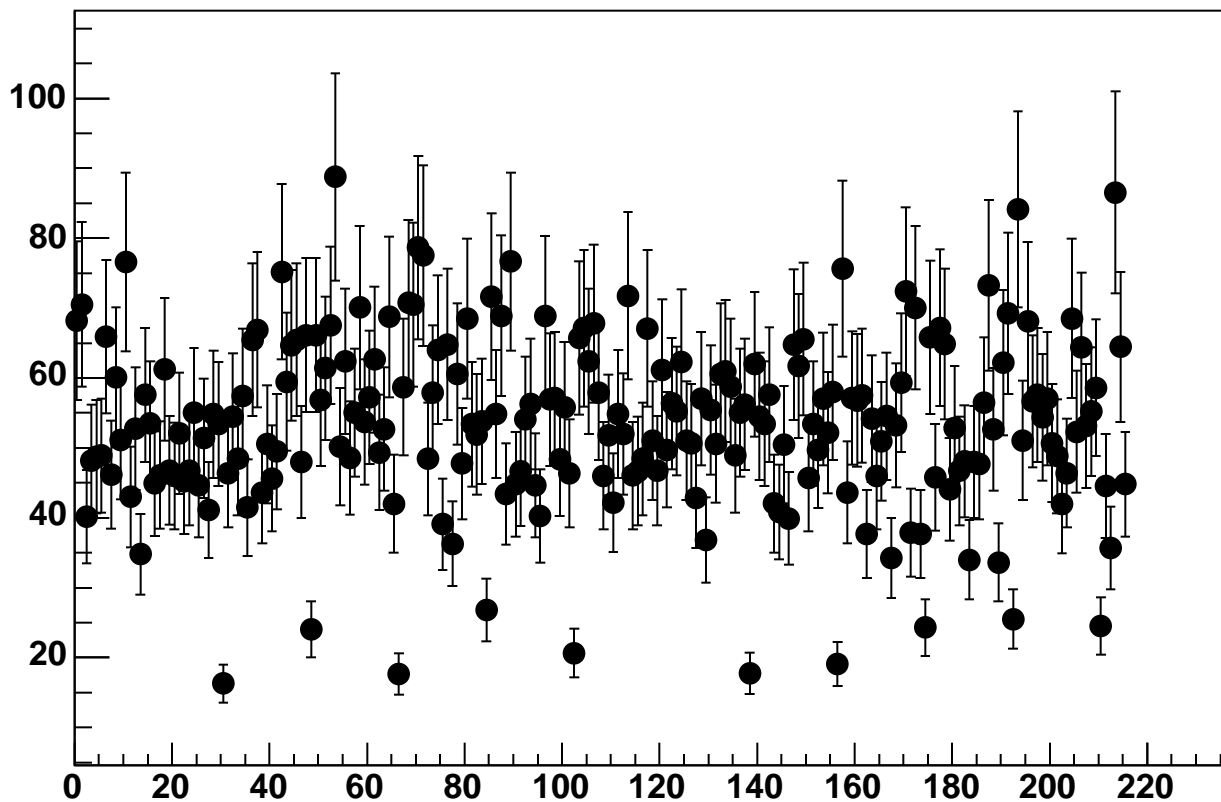
Enable 2, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan

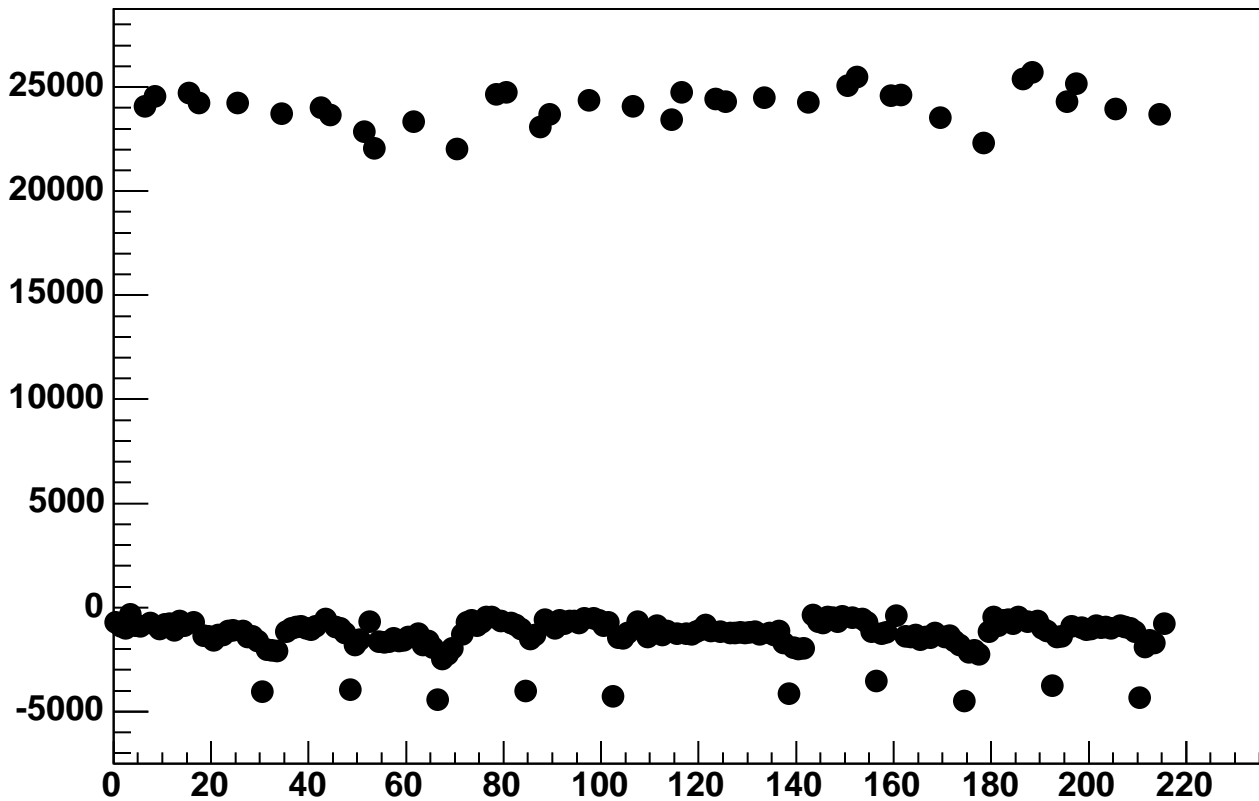


Enable 2, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan

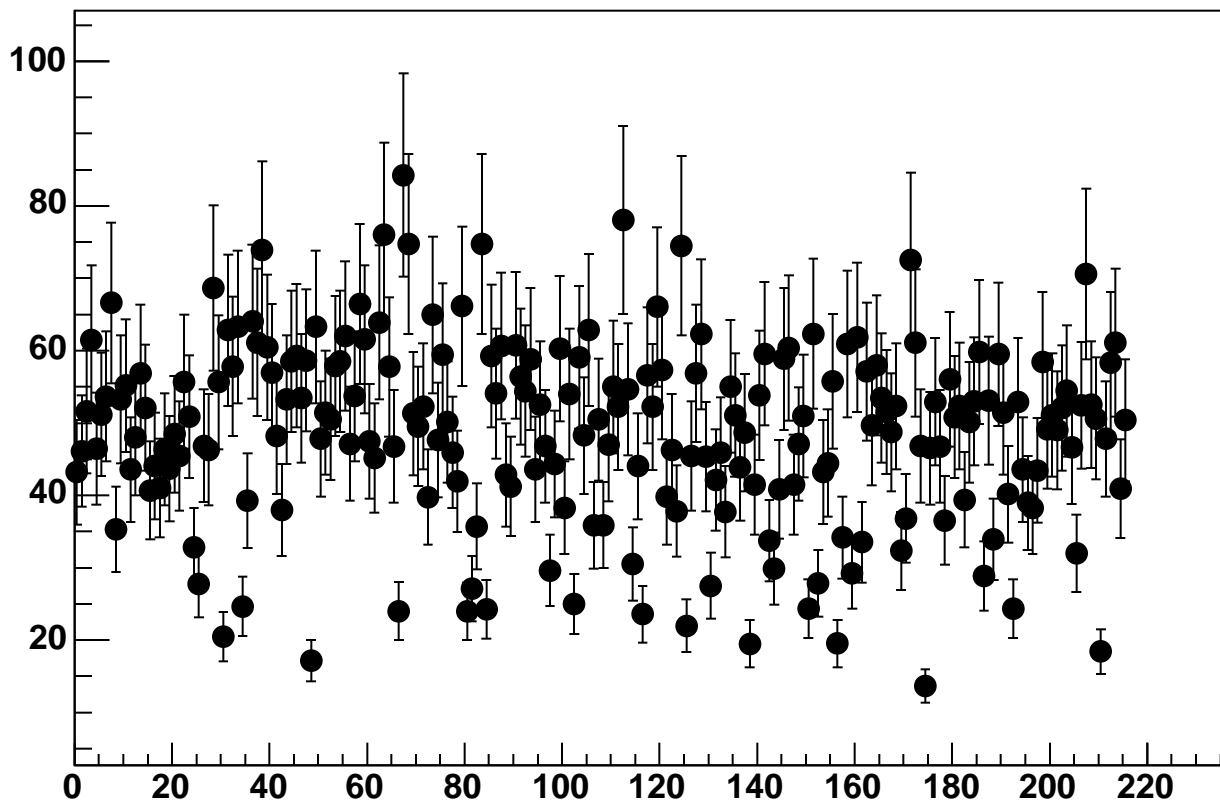




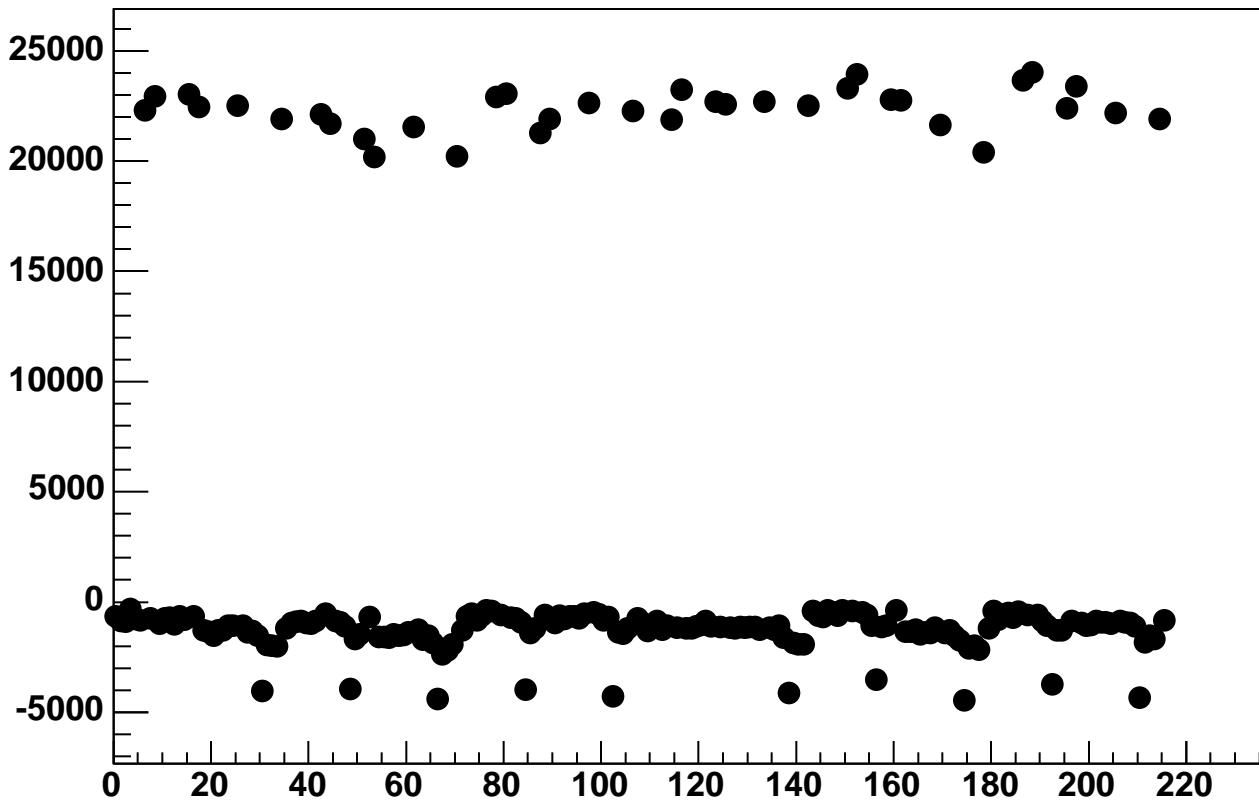
Enable 2, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



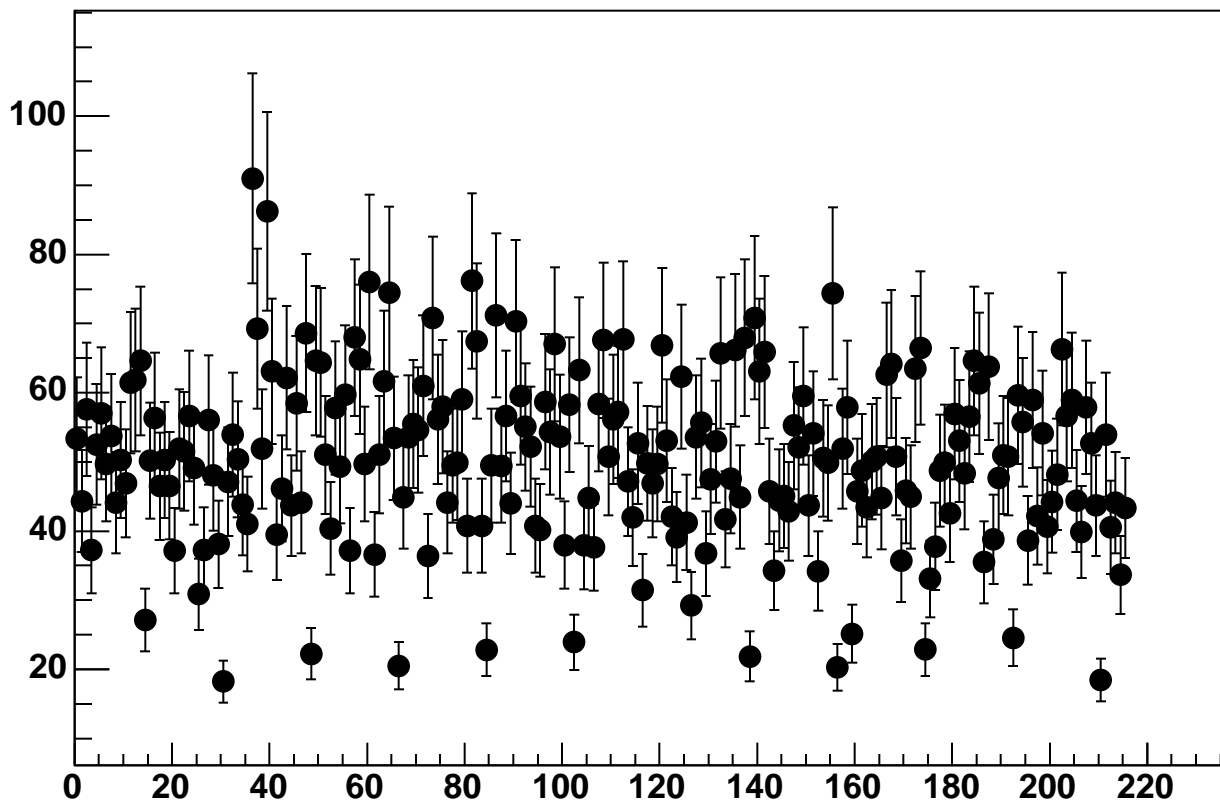
Enable 2, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



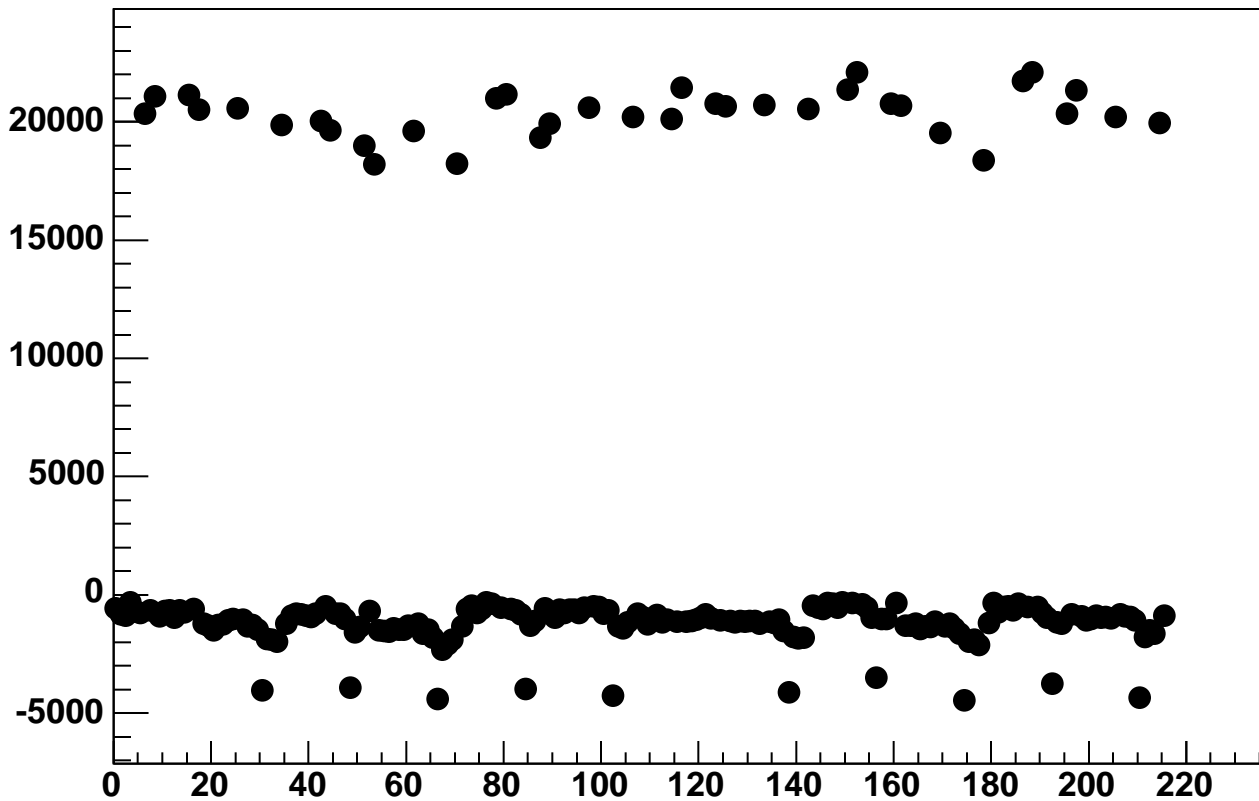
Enable 2, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan



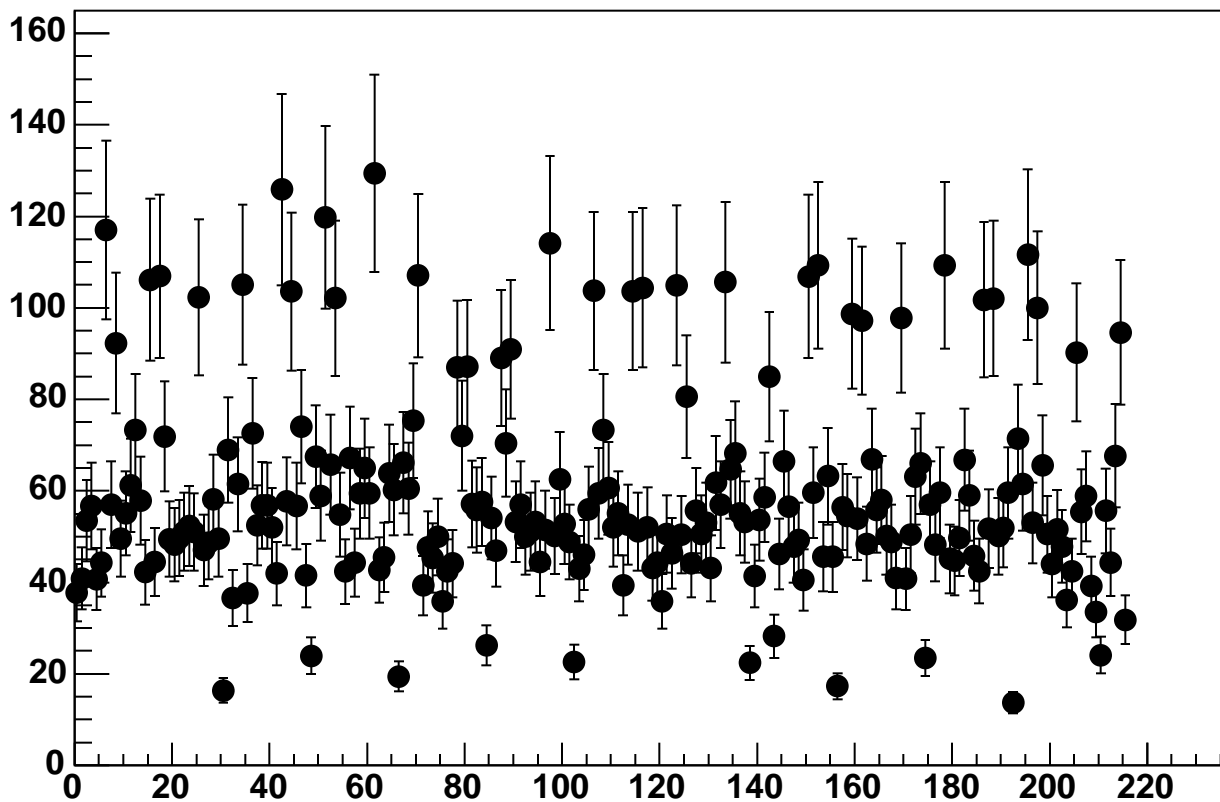
Enable 2, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan



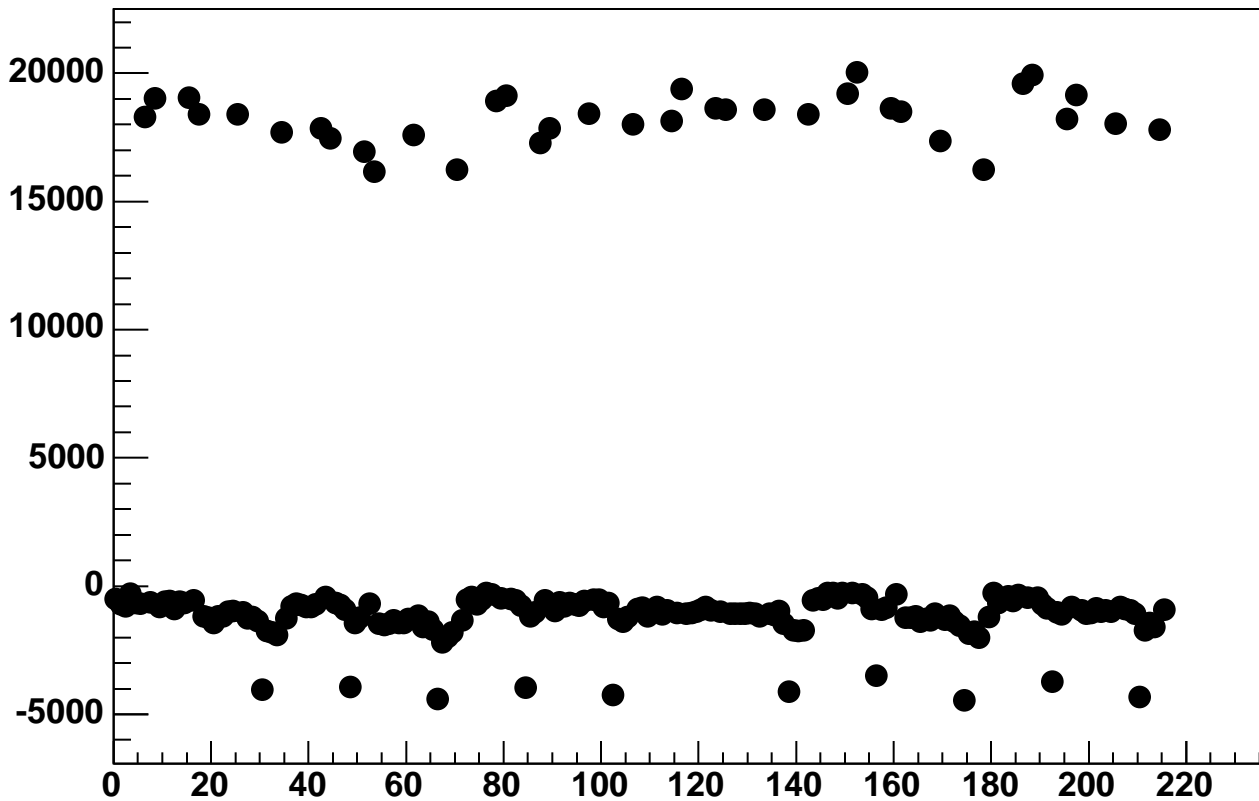
Enable 2, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



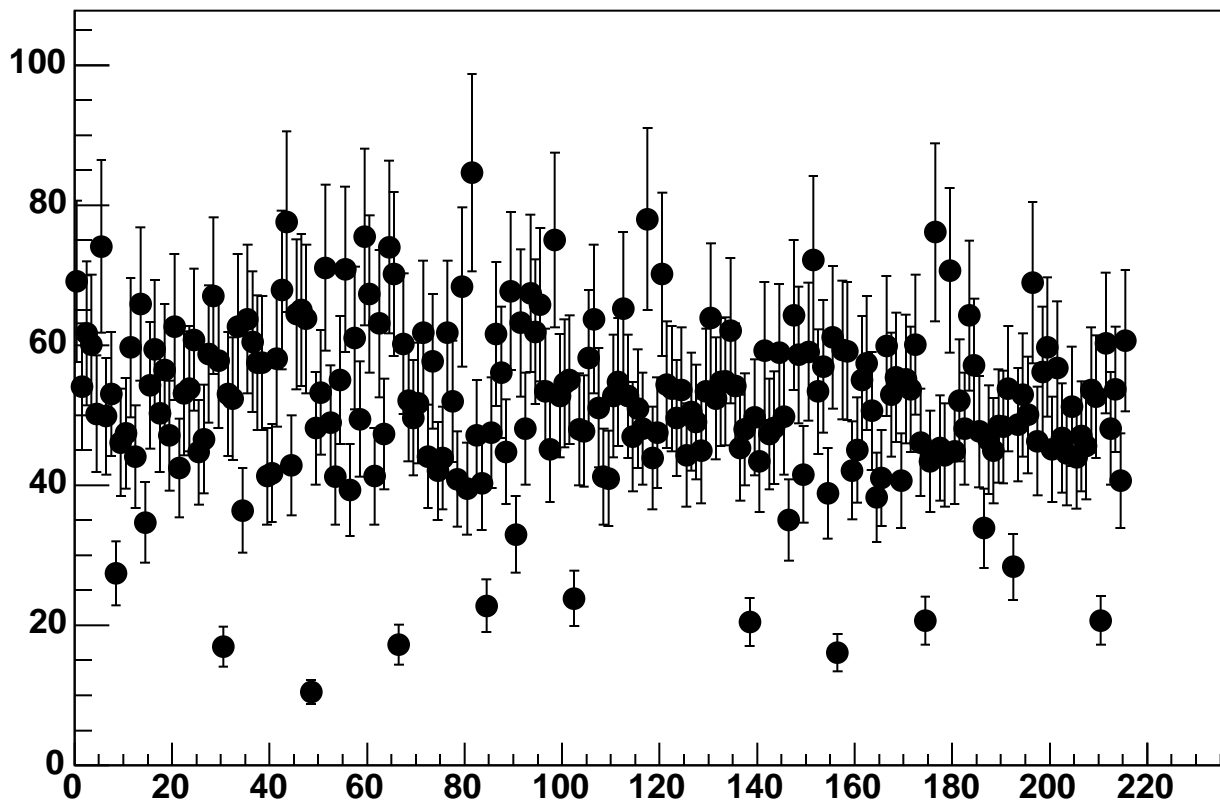
Enable 2, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



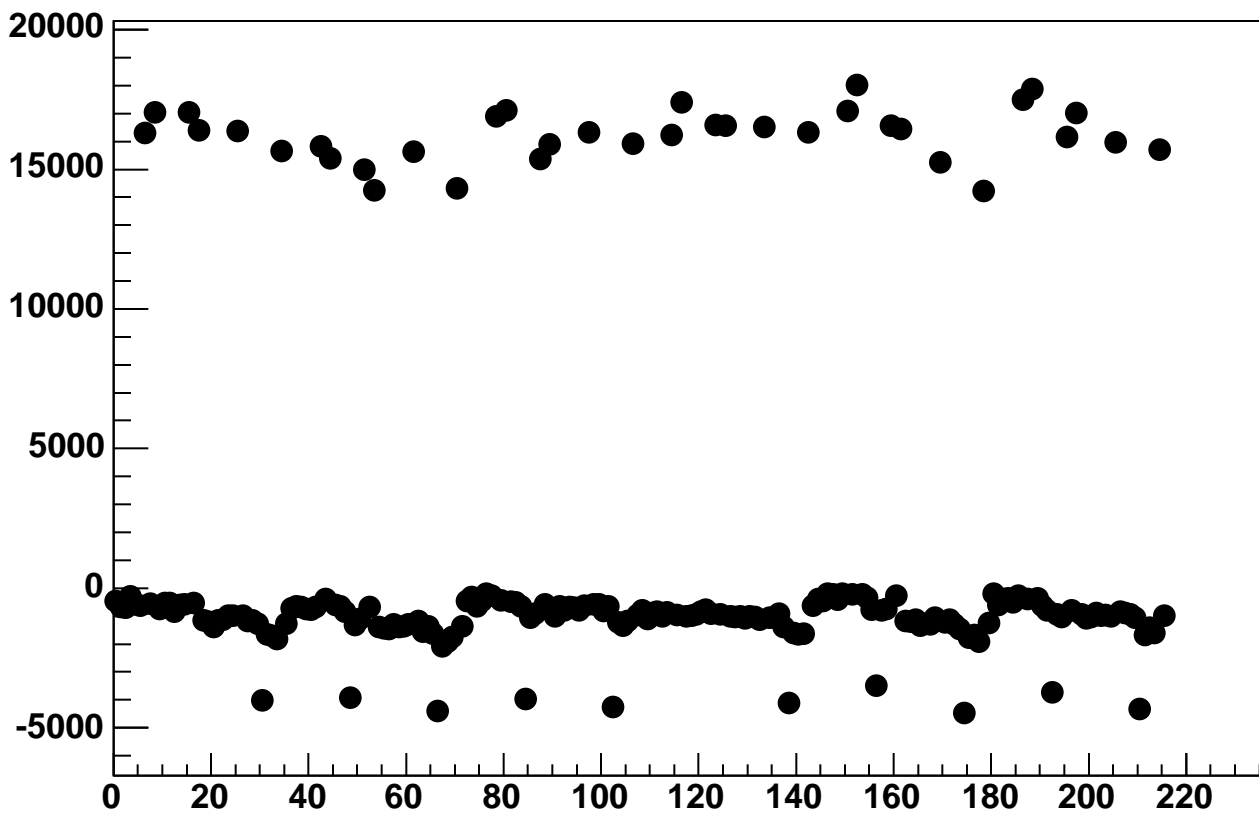
Enable 2, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan



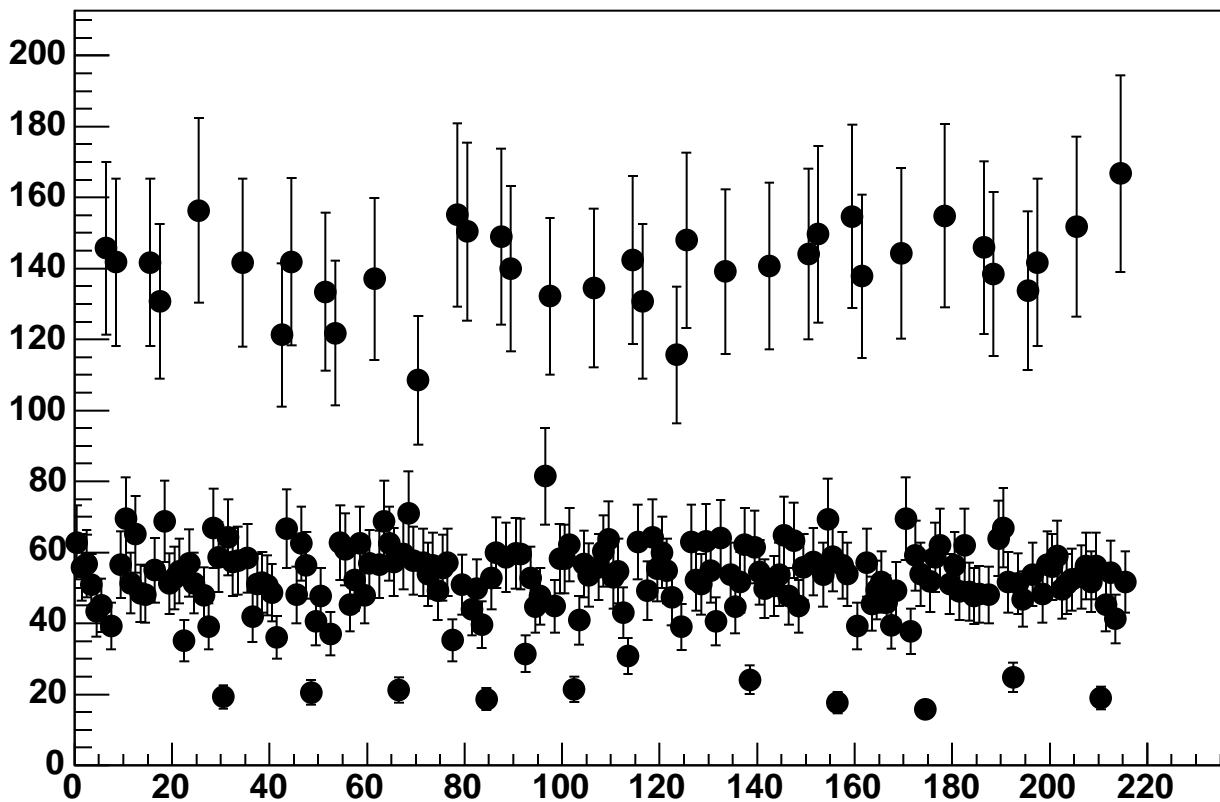
Enable 2, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan



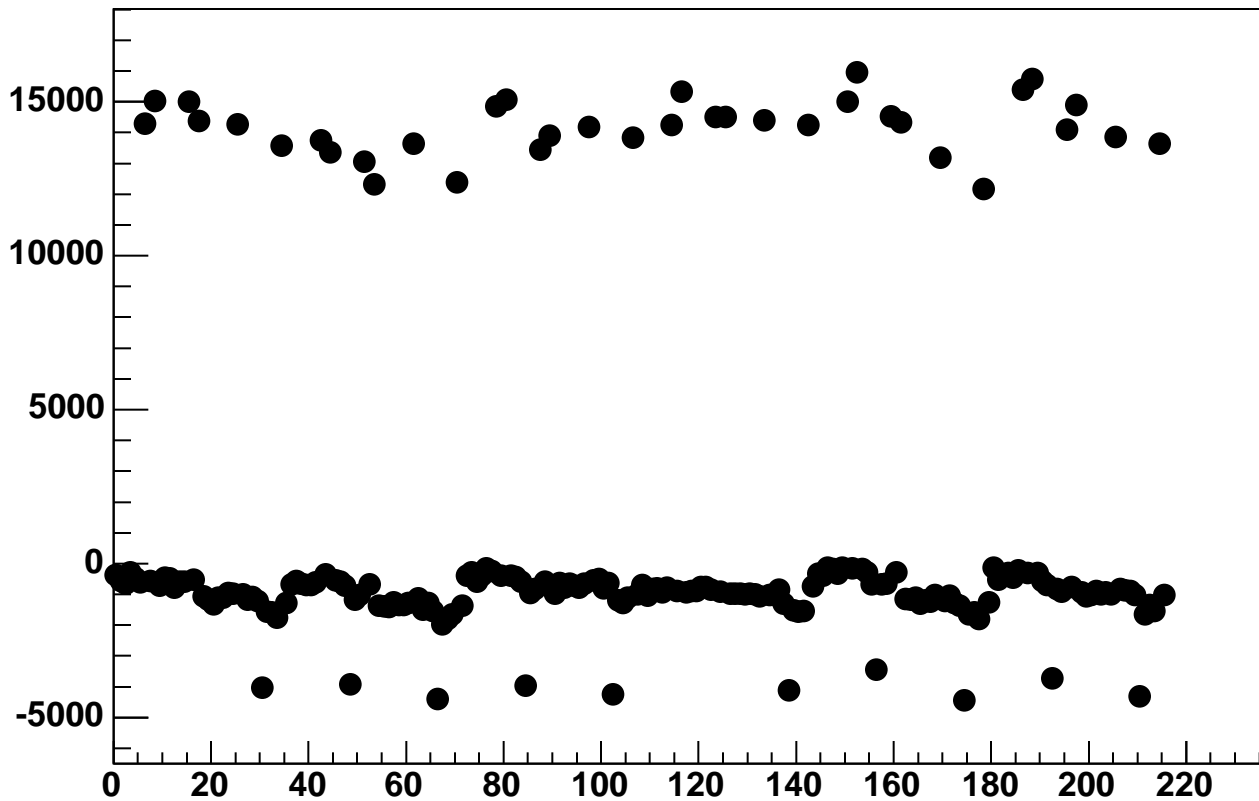
Enable 2, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



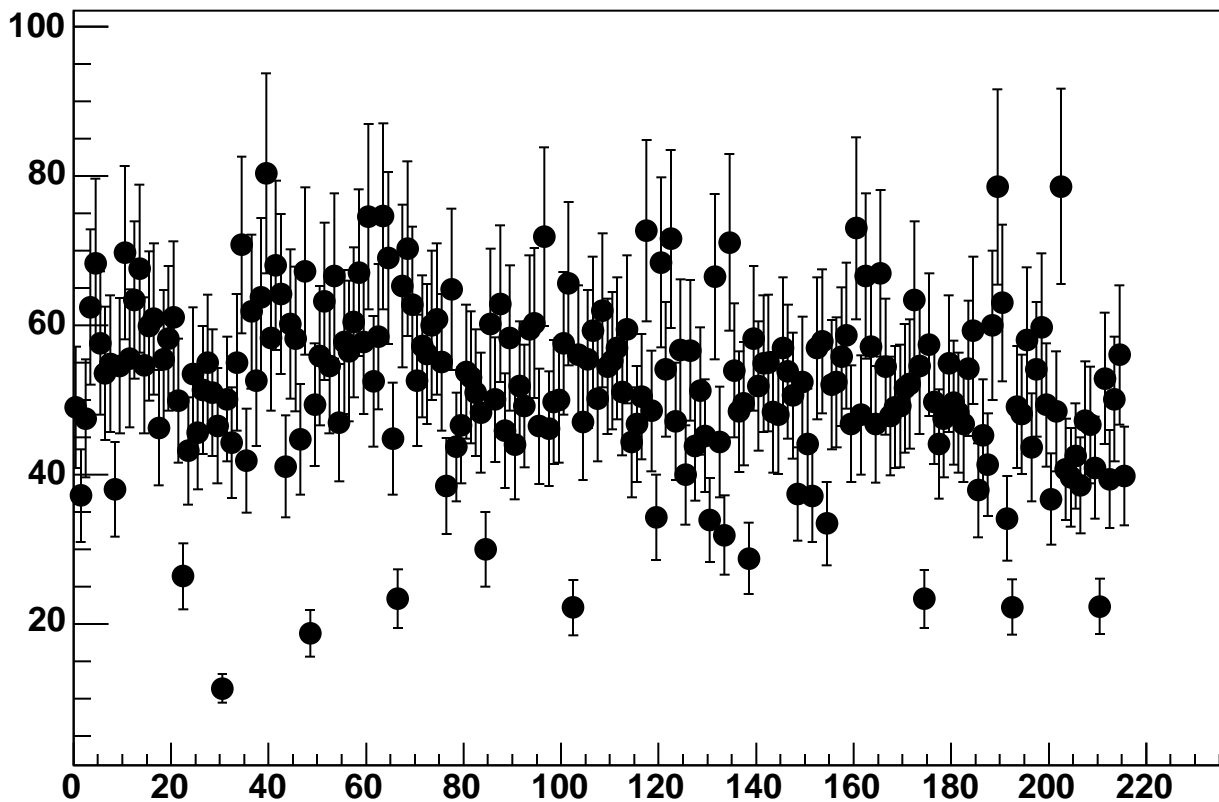
Enable 2, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



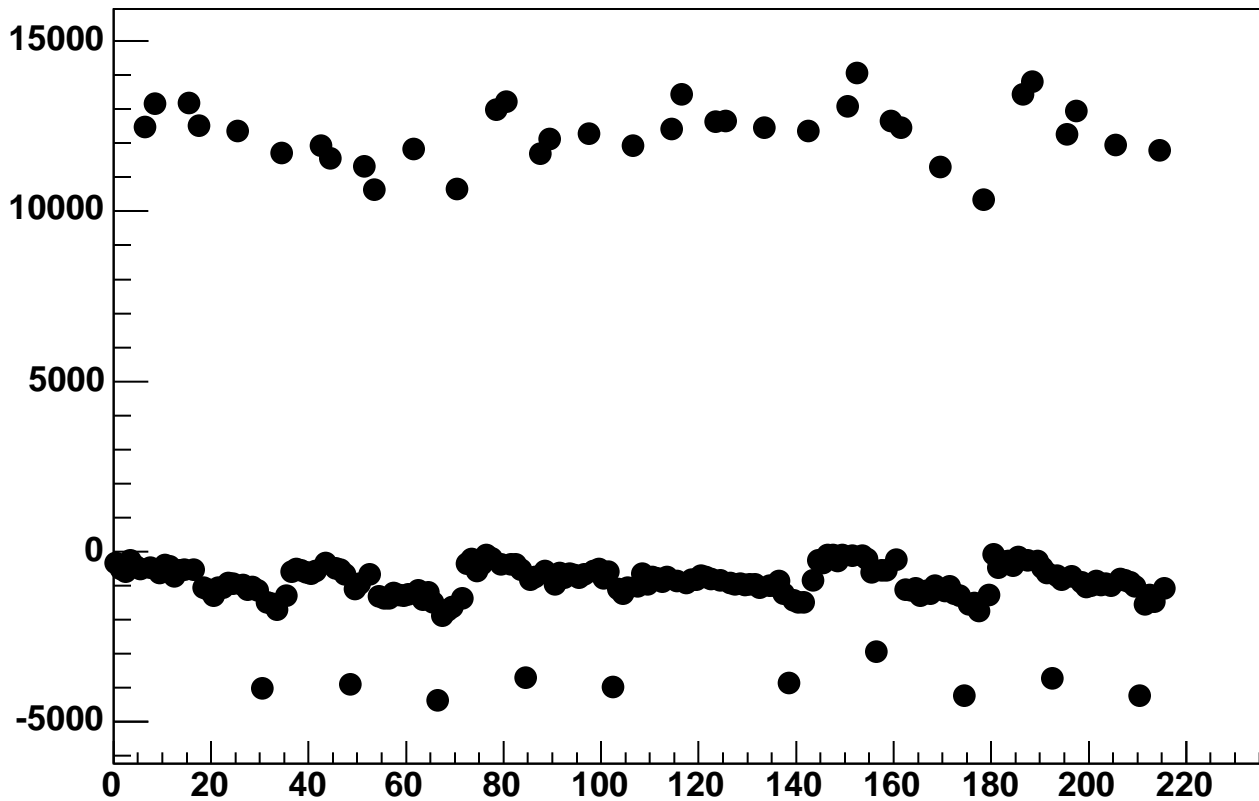
Enable 2, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan



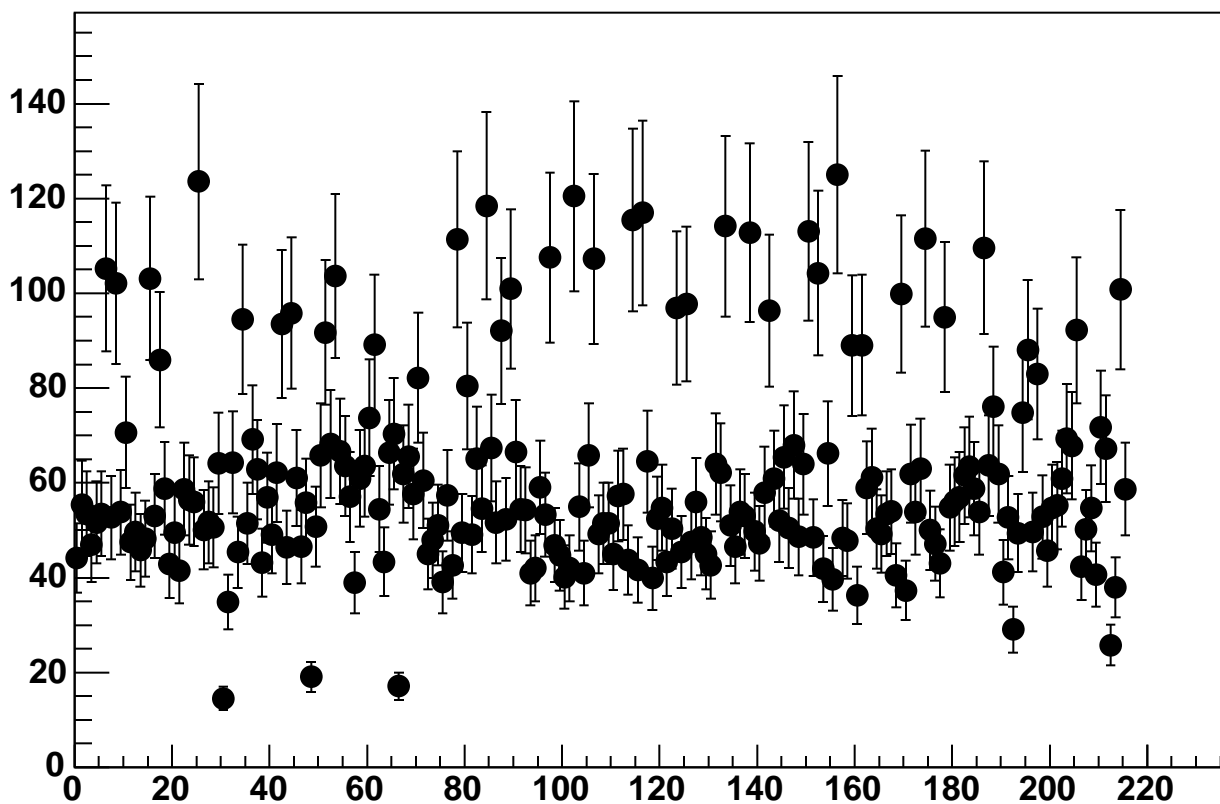
Enable 2, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan



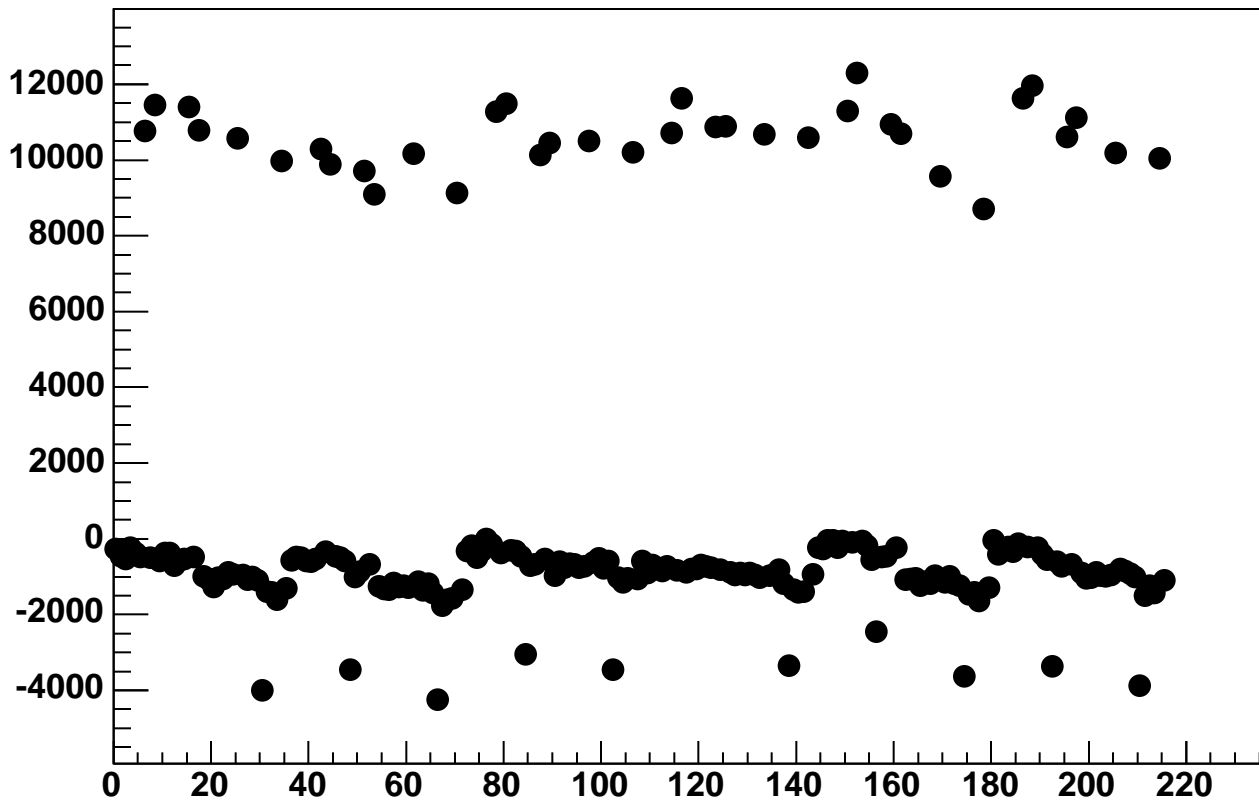
Enable 2, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



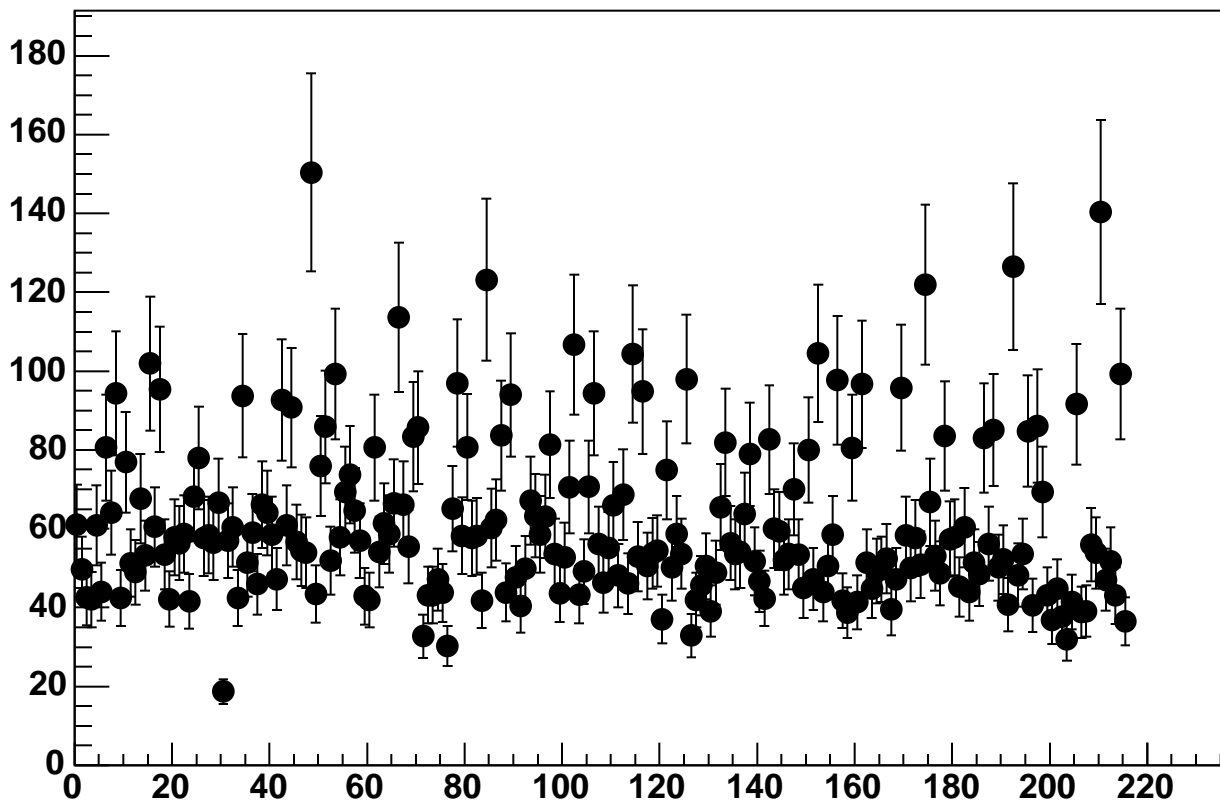
Enable 2, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan

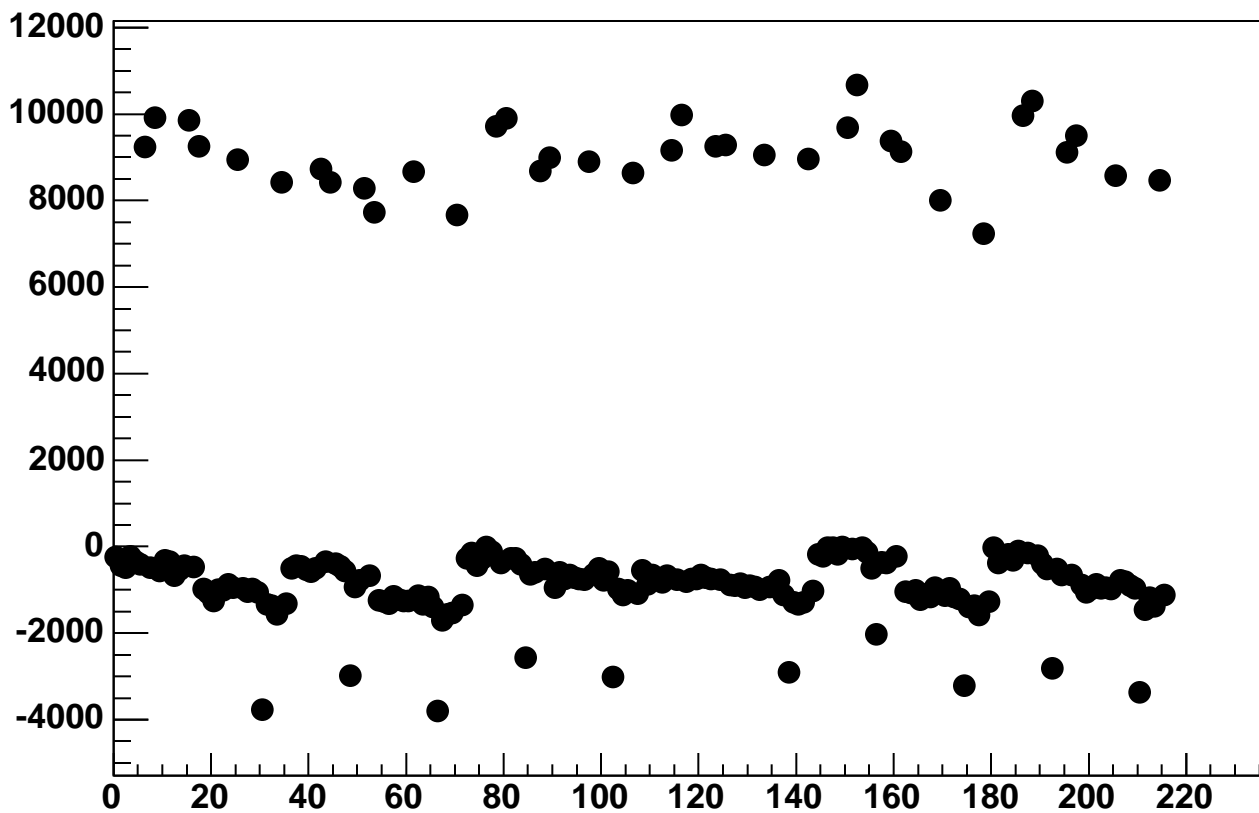


Enable 2, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan

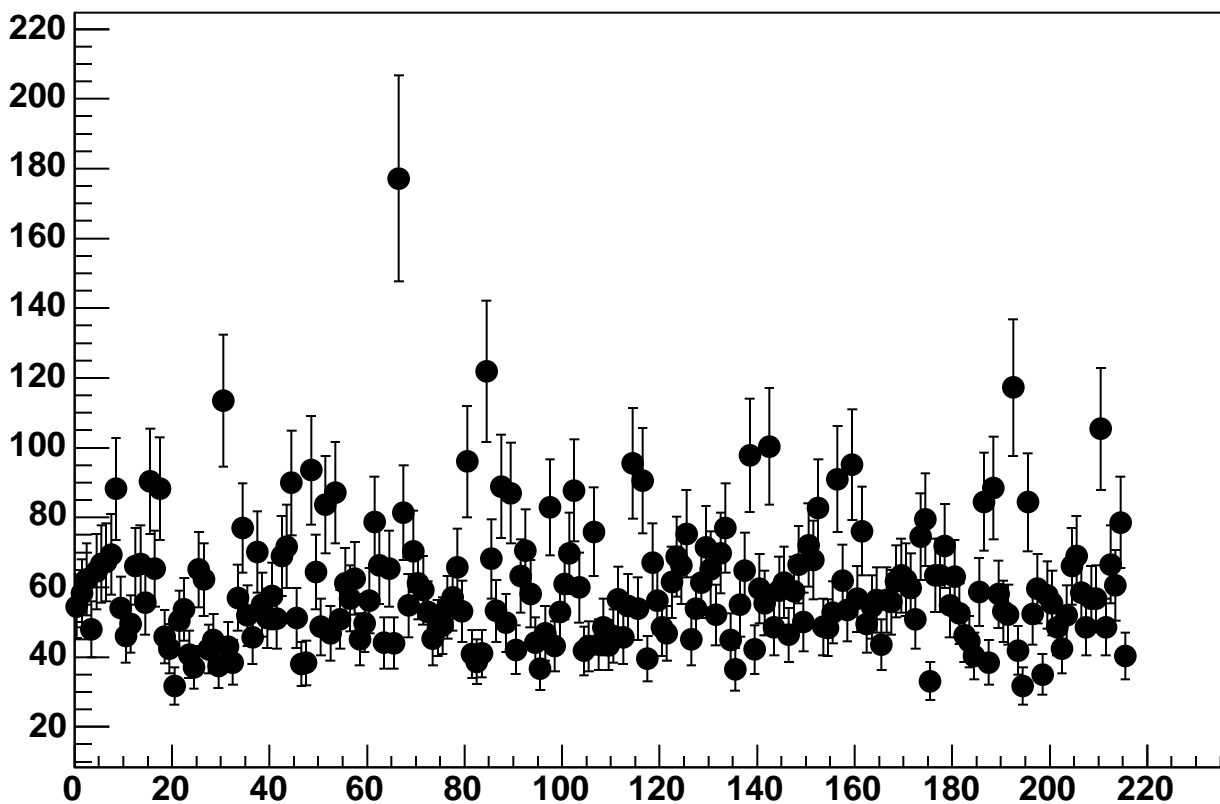




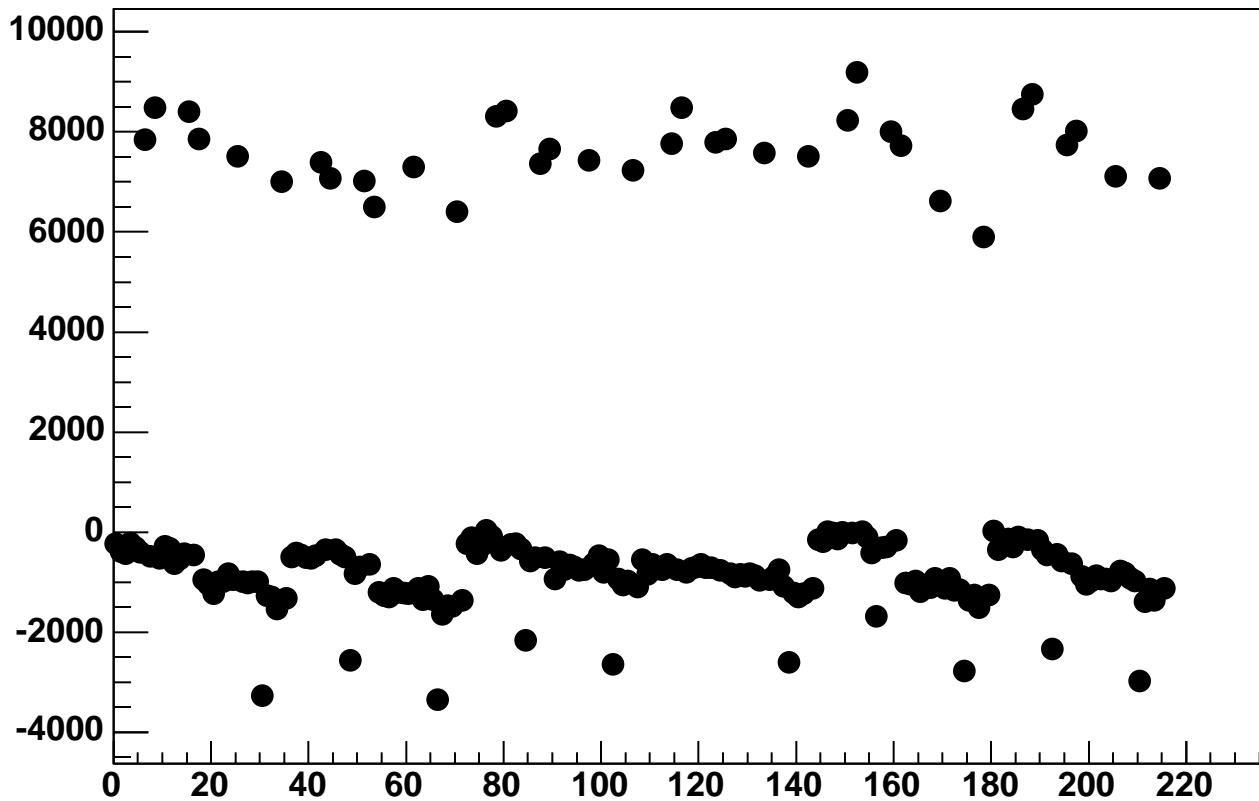
Enable 2, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



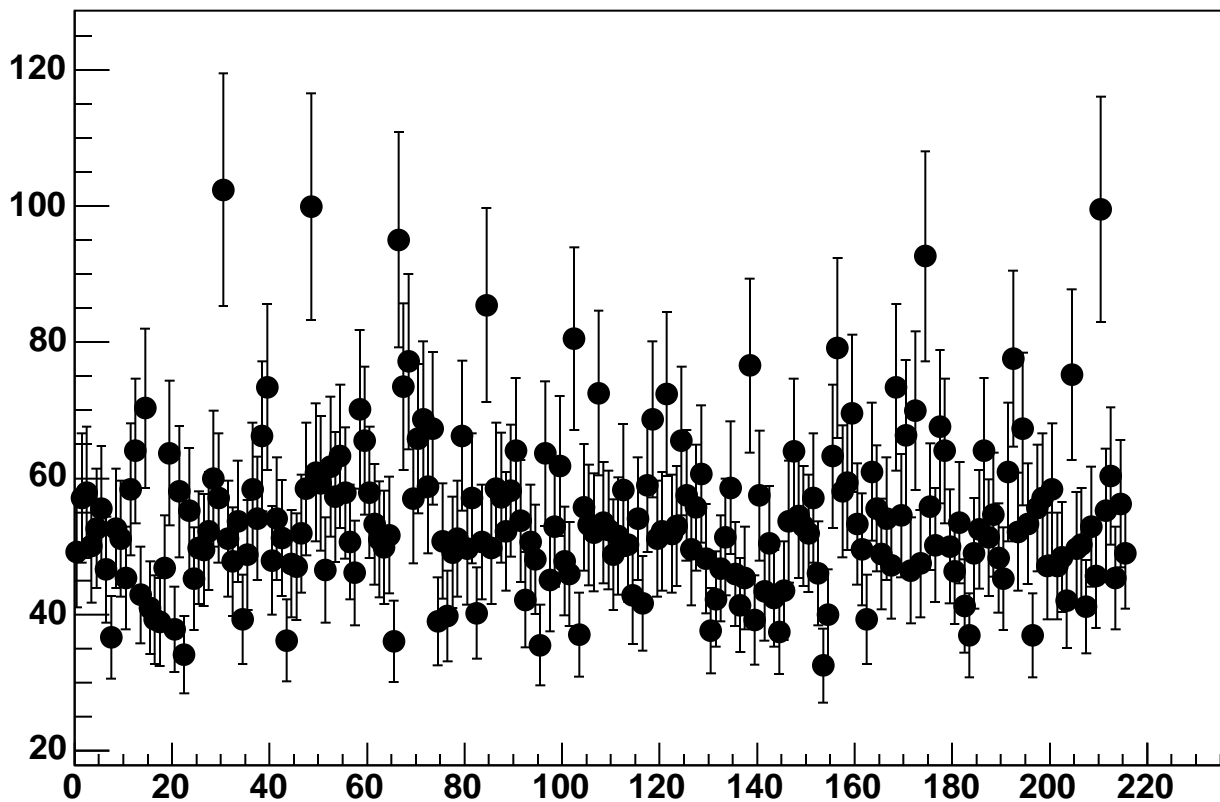
Enable 2, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



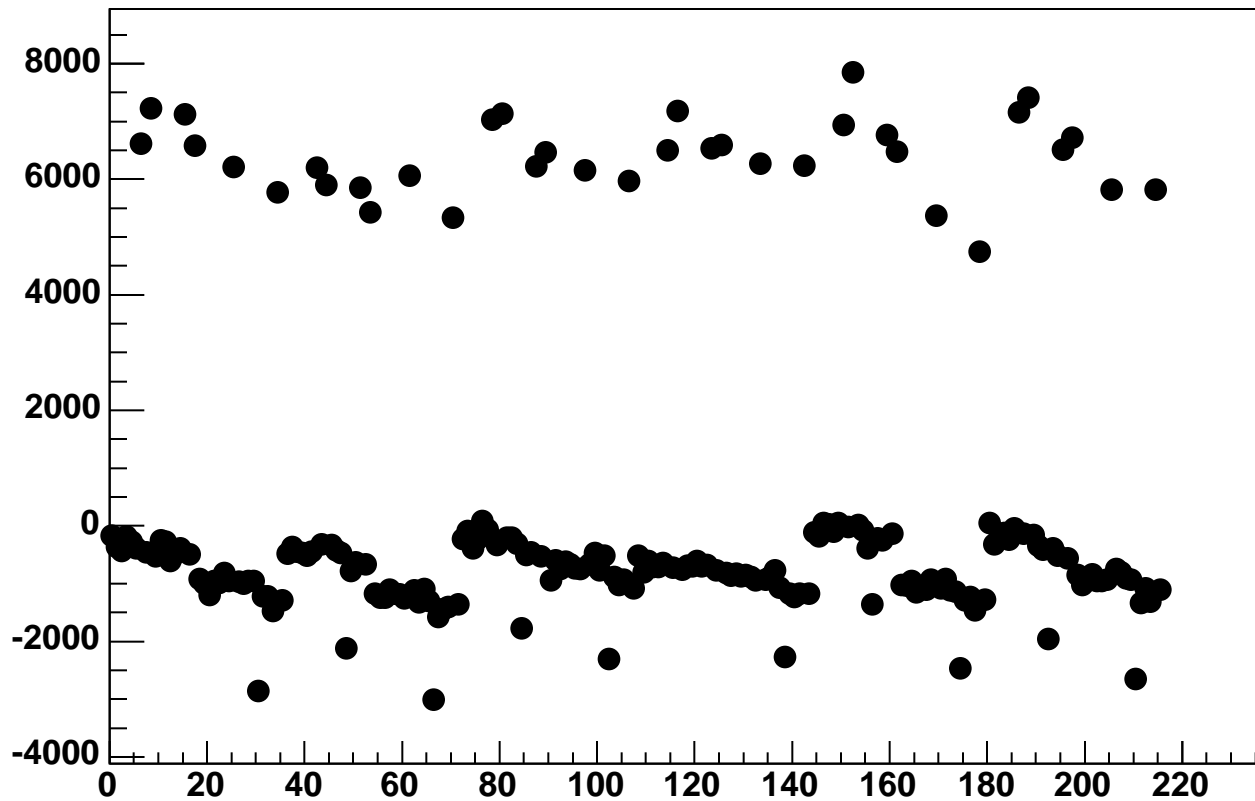
Enable 2, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan



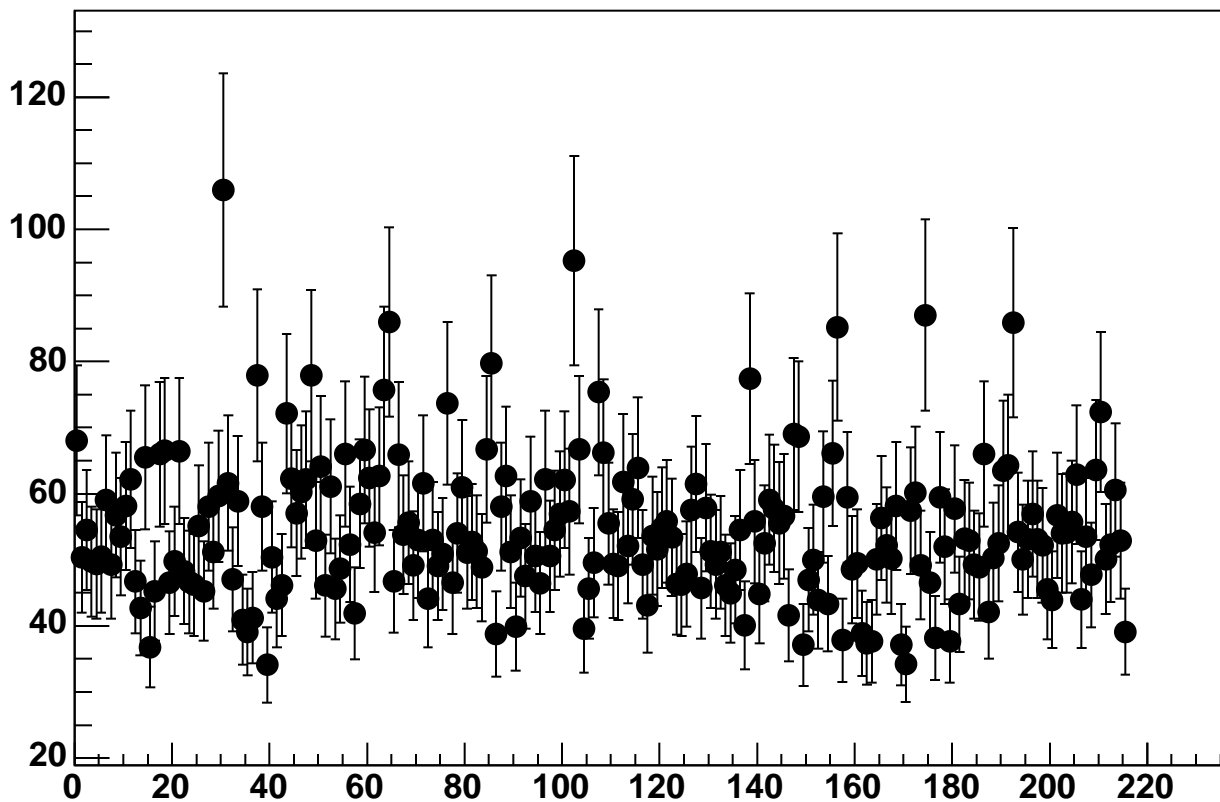
Enable 2, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan



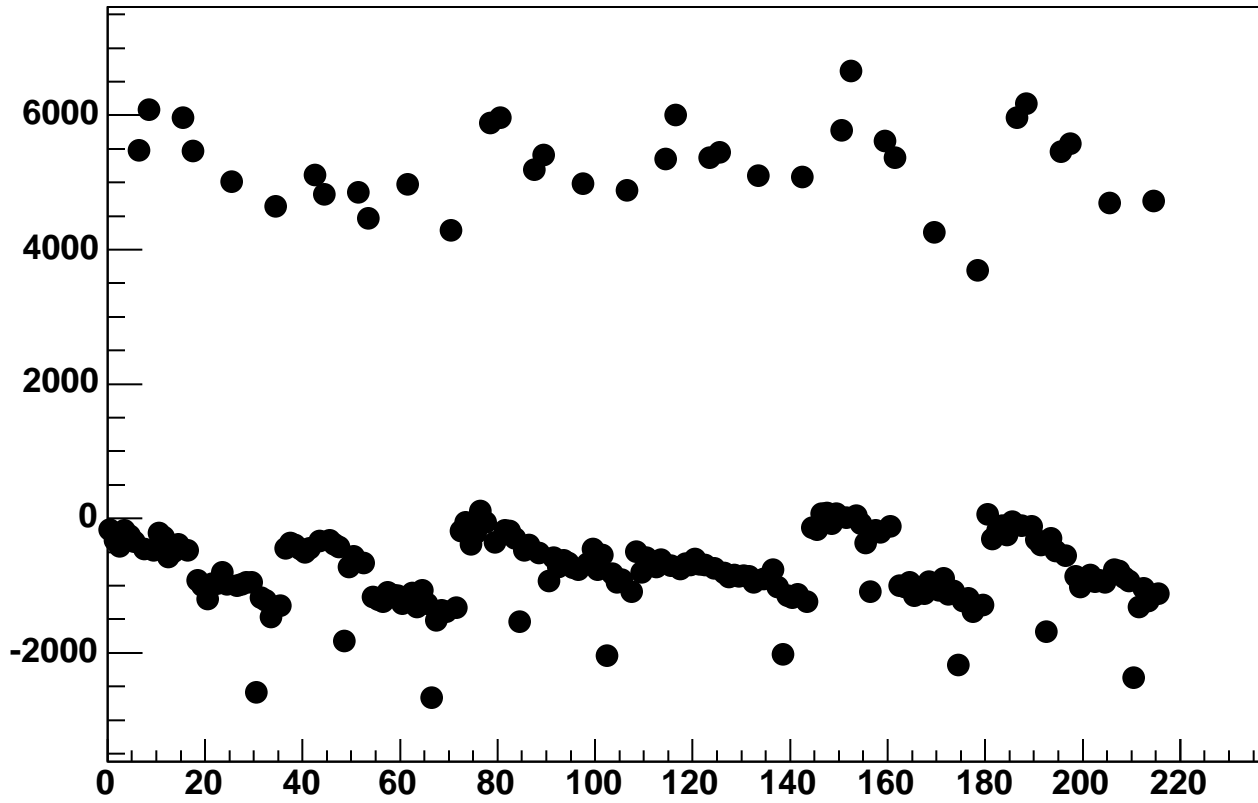
Enable 2, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



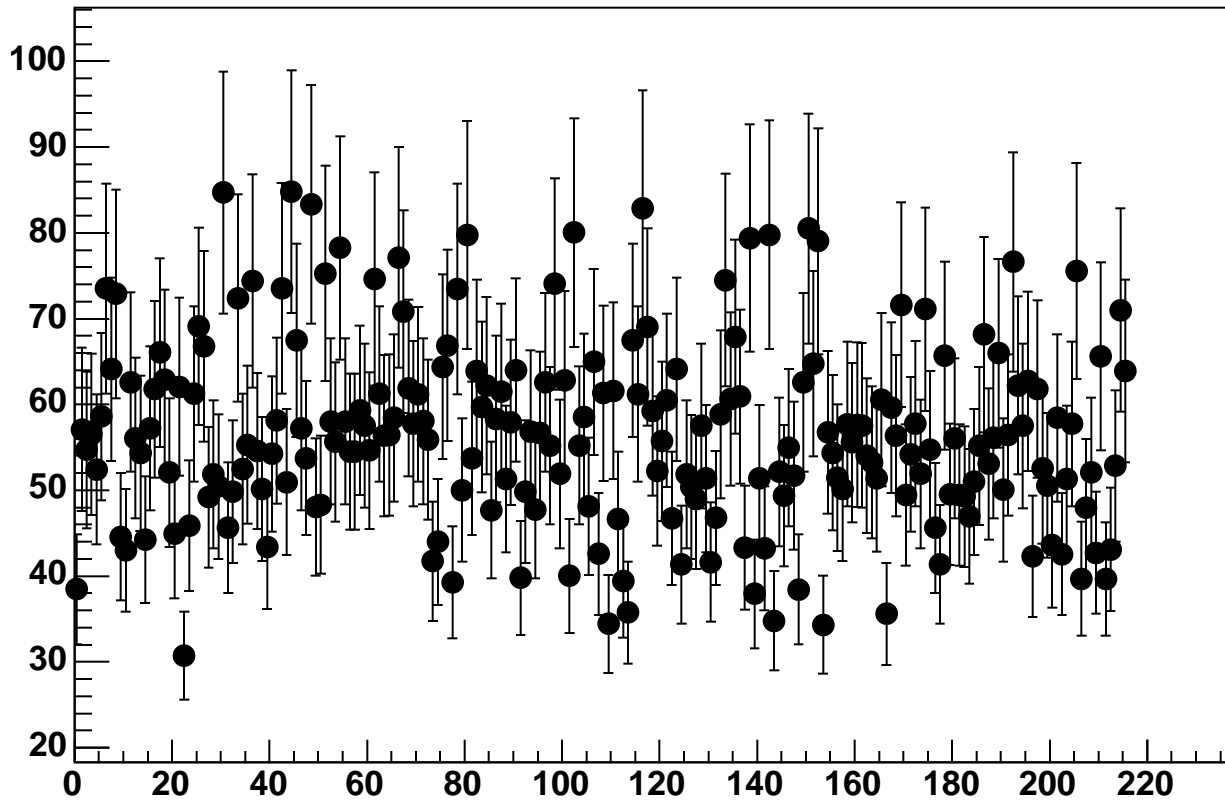
Enable 2, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



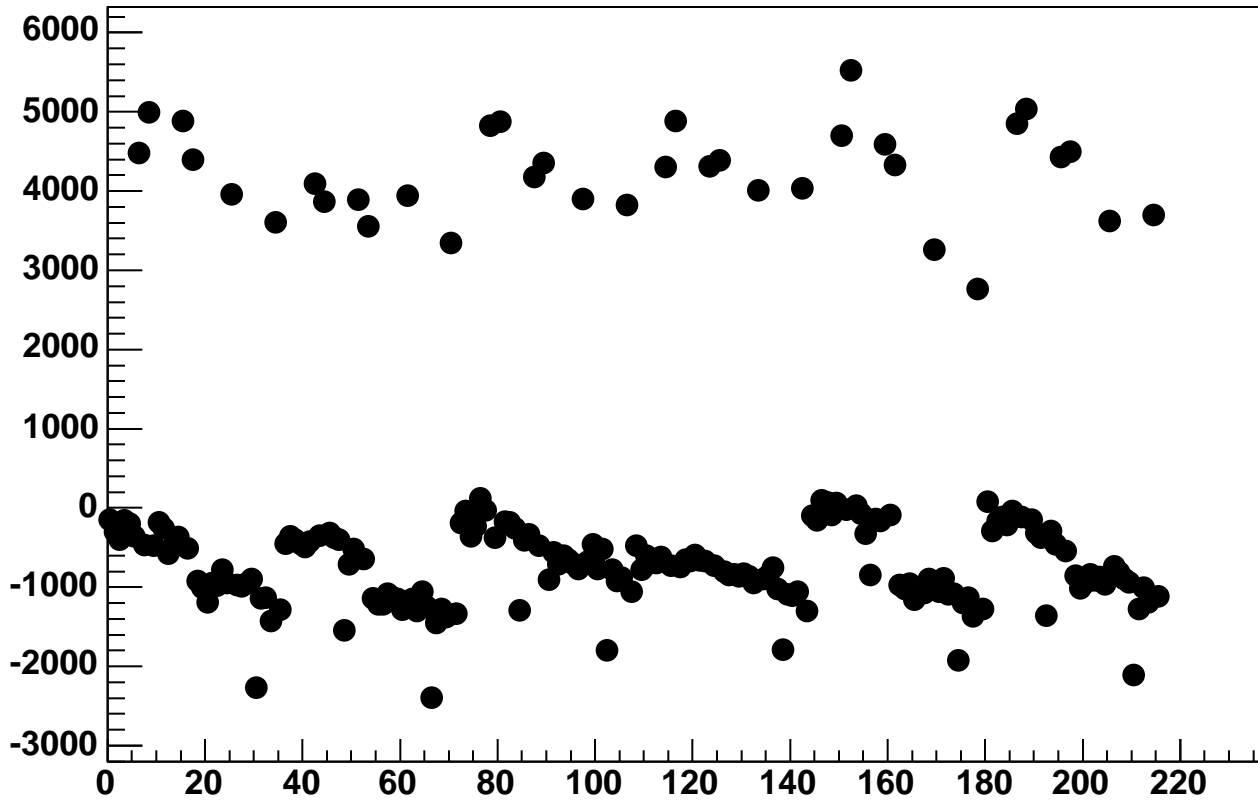
Enable 2, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan



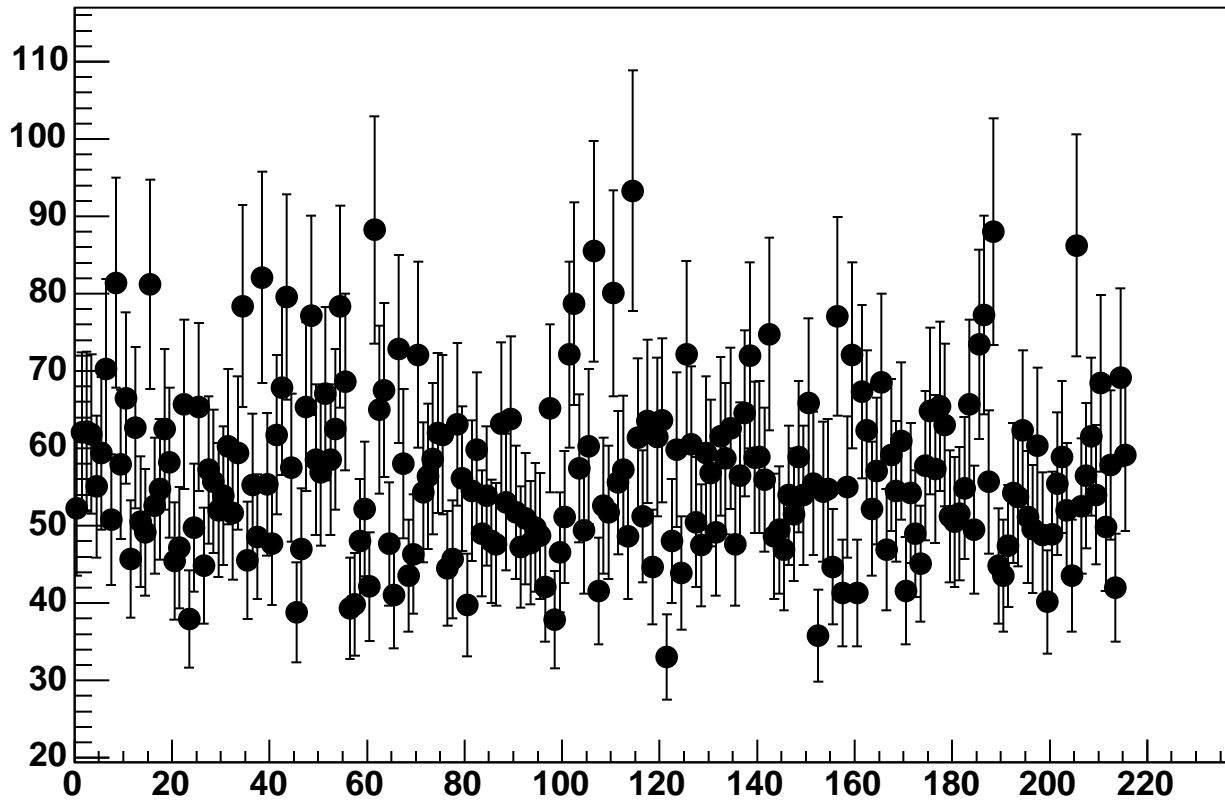
Enable 2, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan



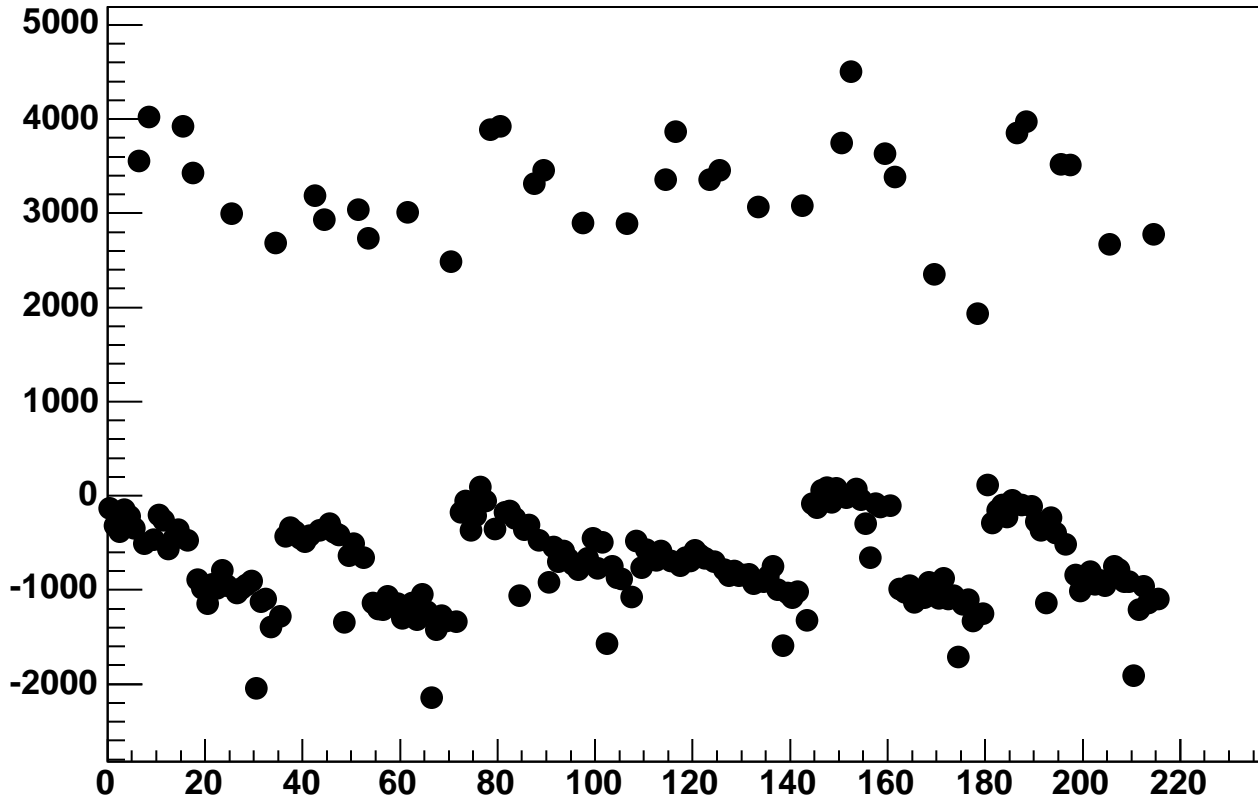
Enable 2, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



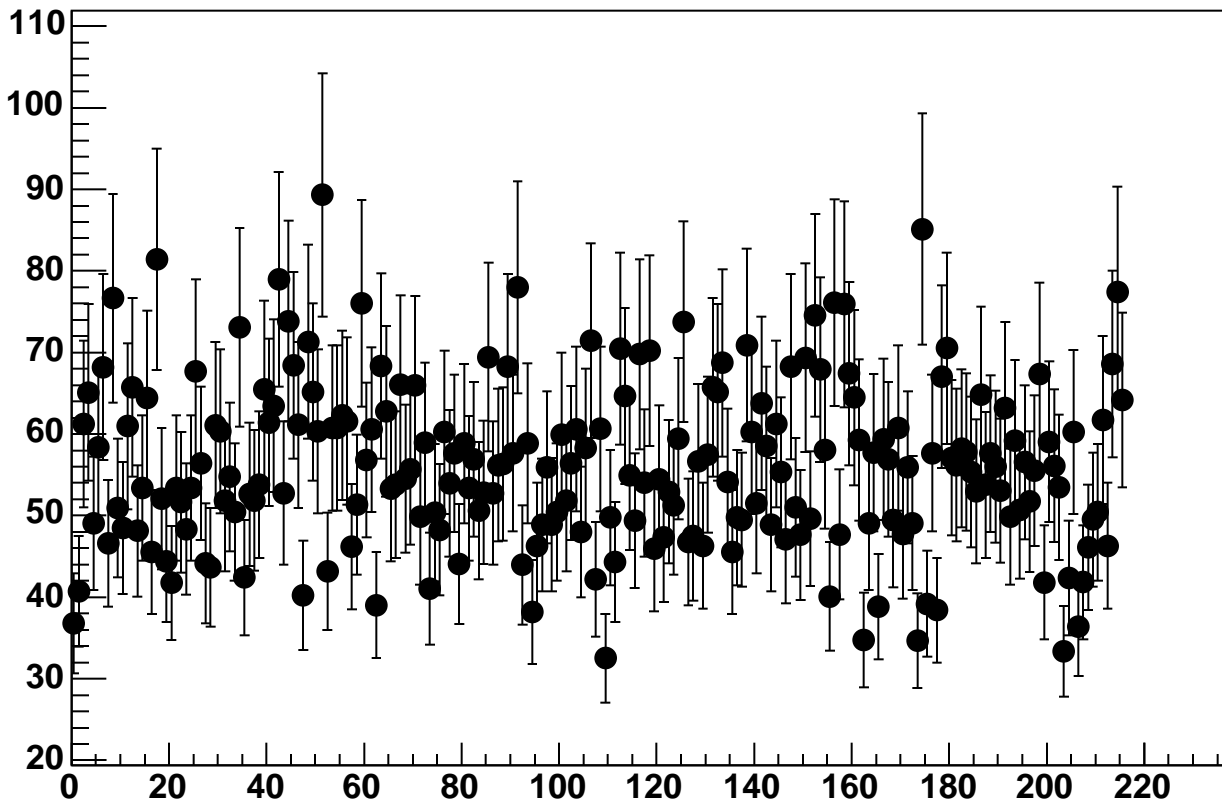
Enable 2, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



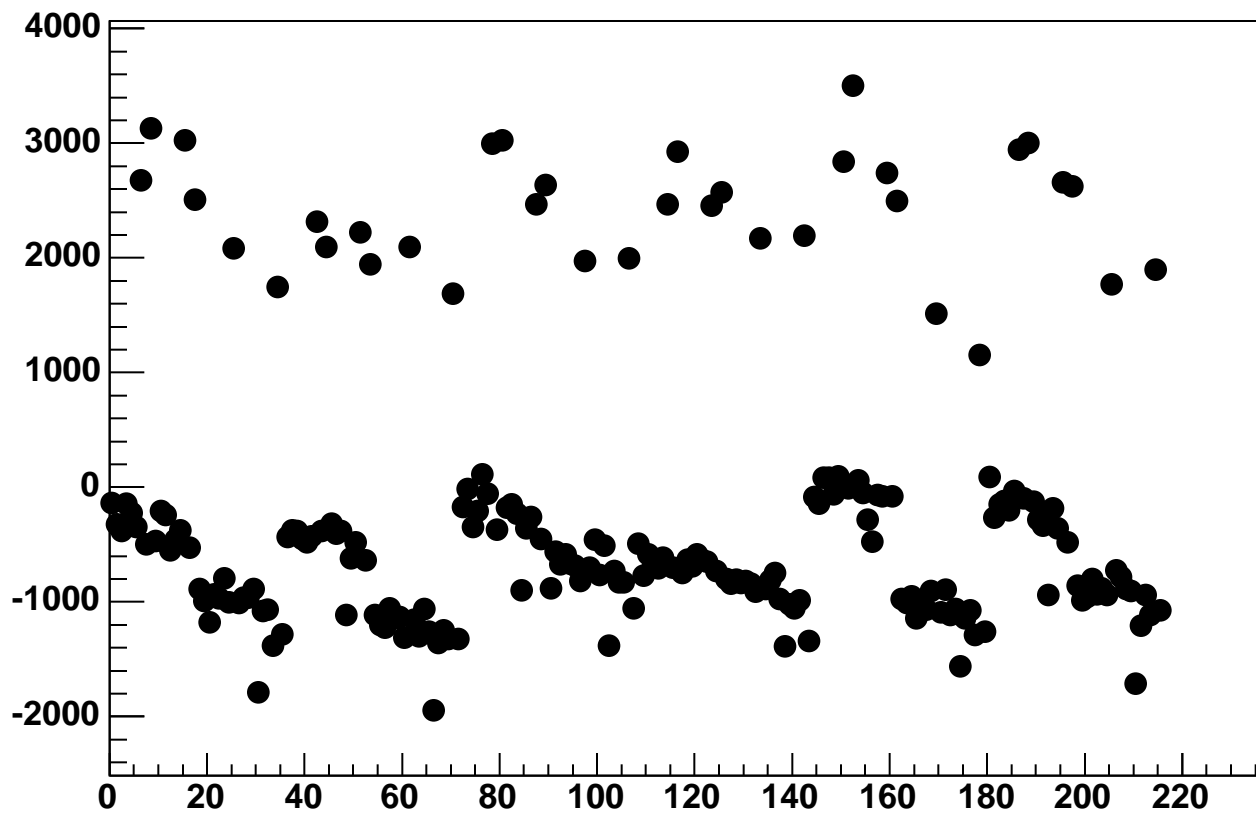
Enable 2, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan



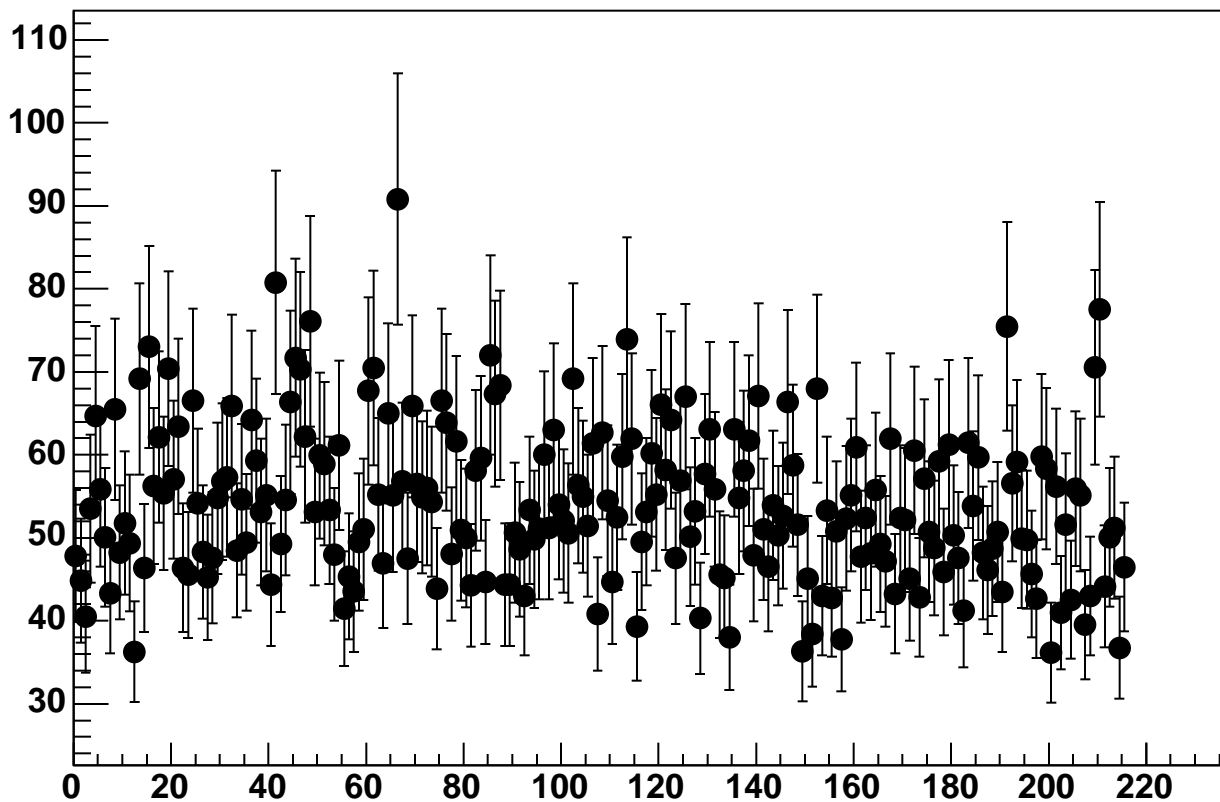
Enable 2, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan



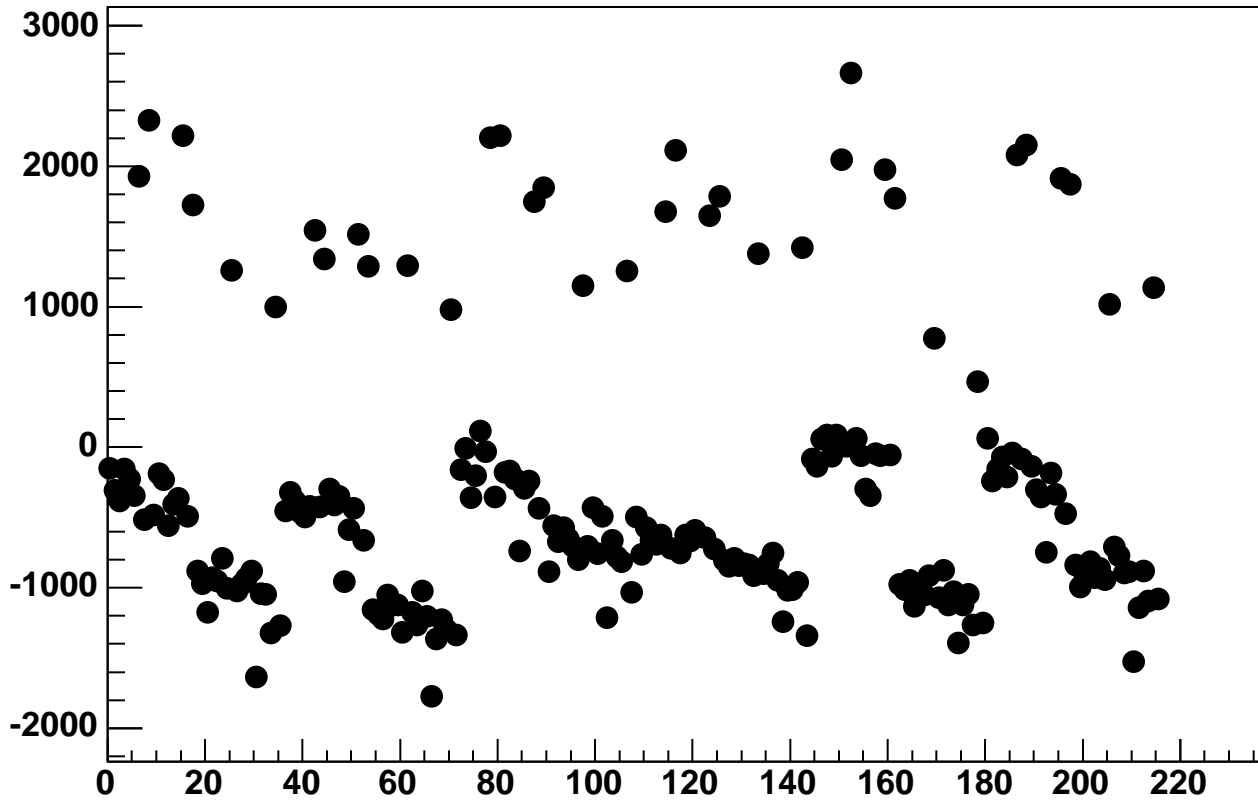
Enable 2, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



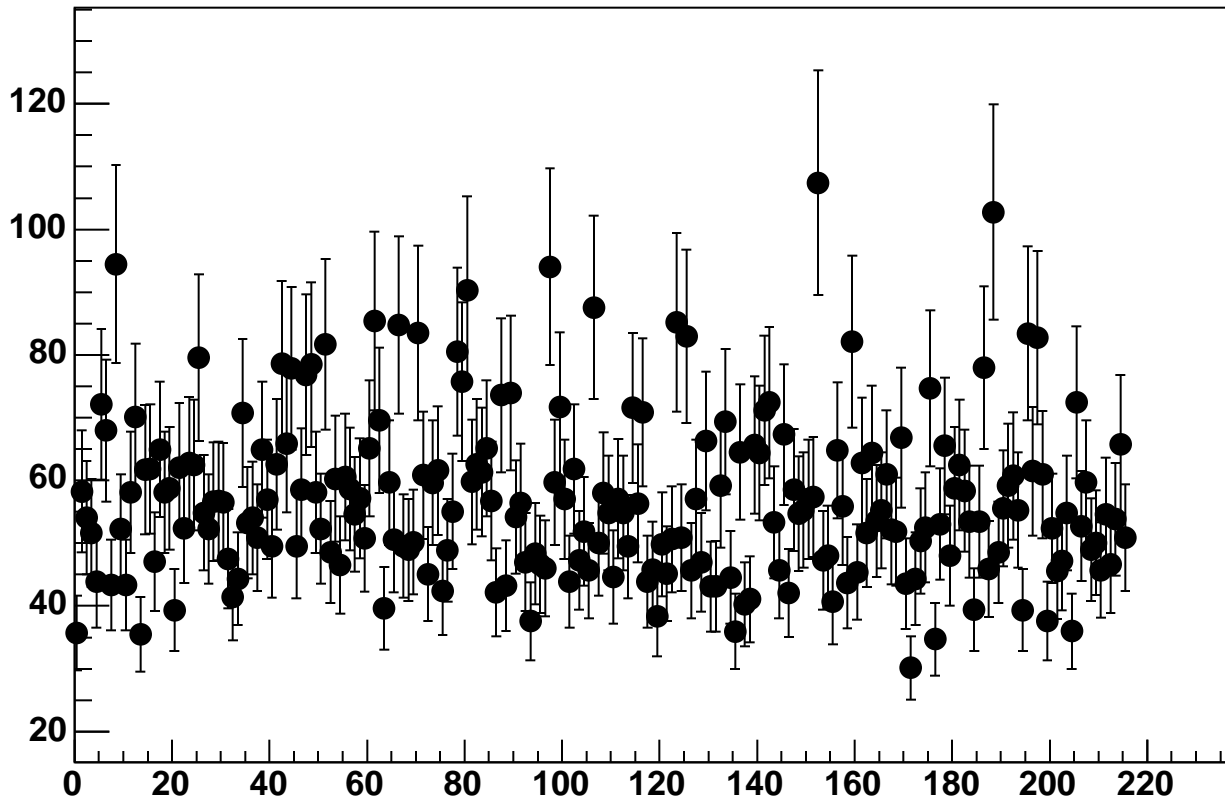
Enable 2, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan

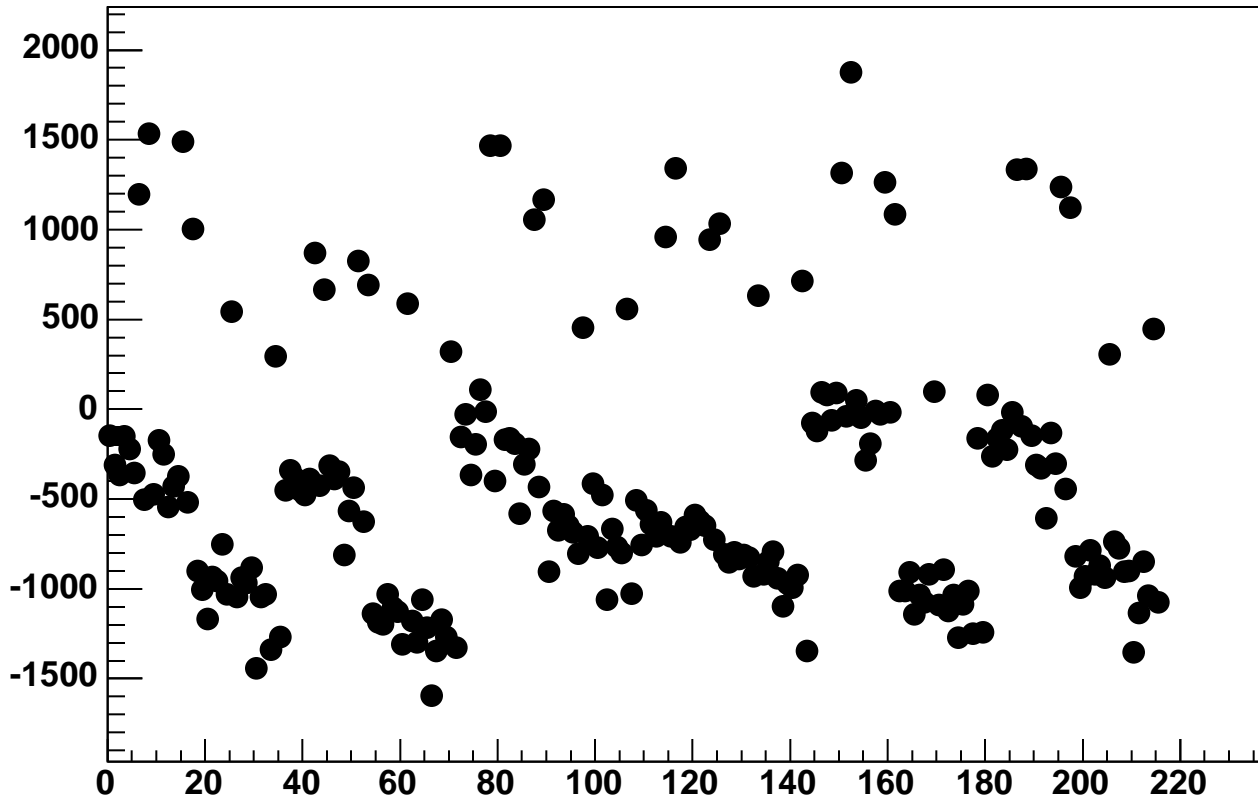


Enable 2, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan

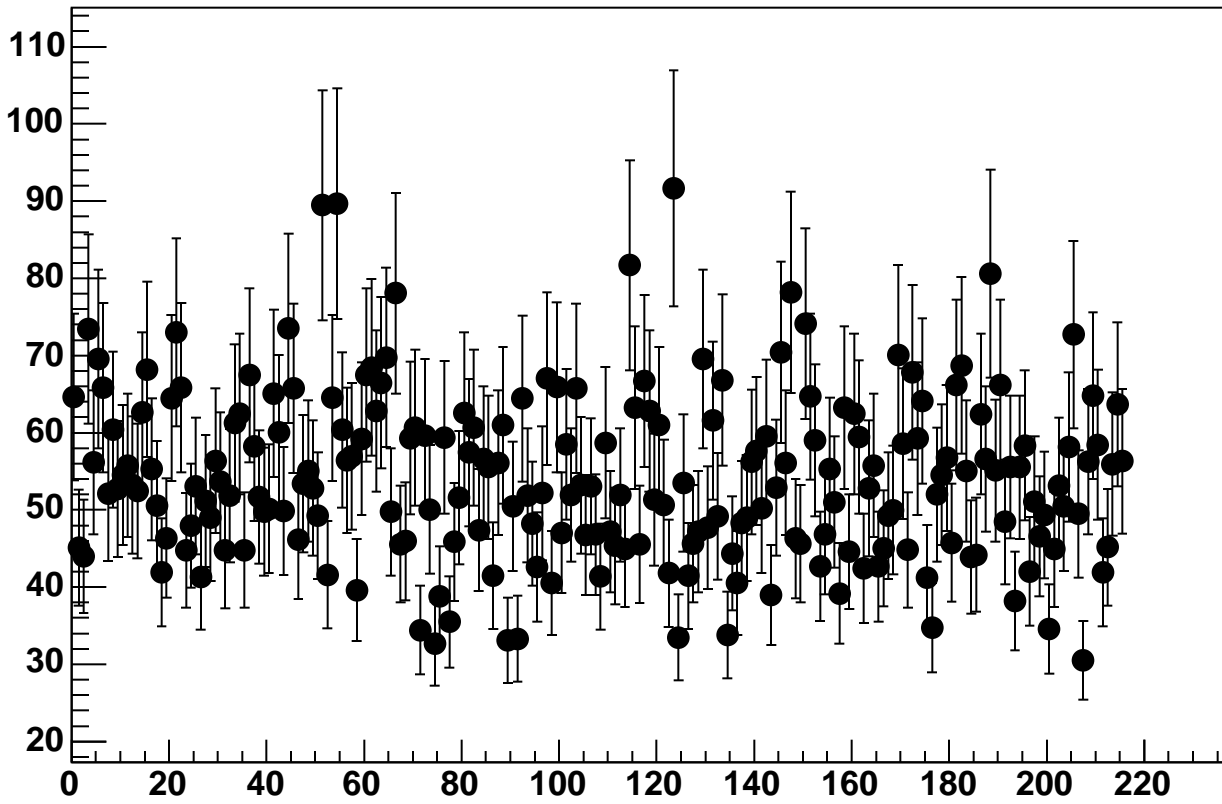




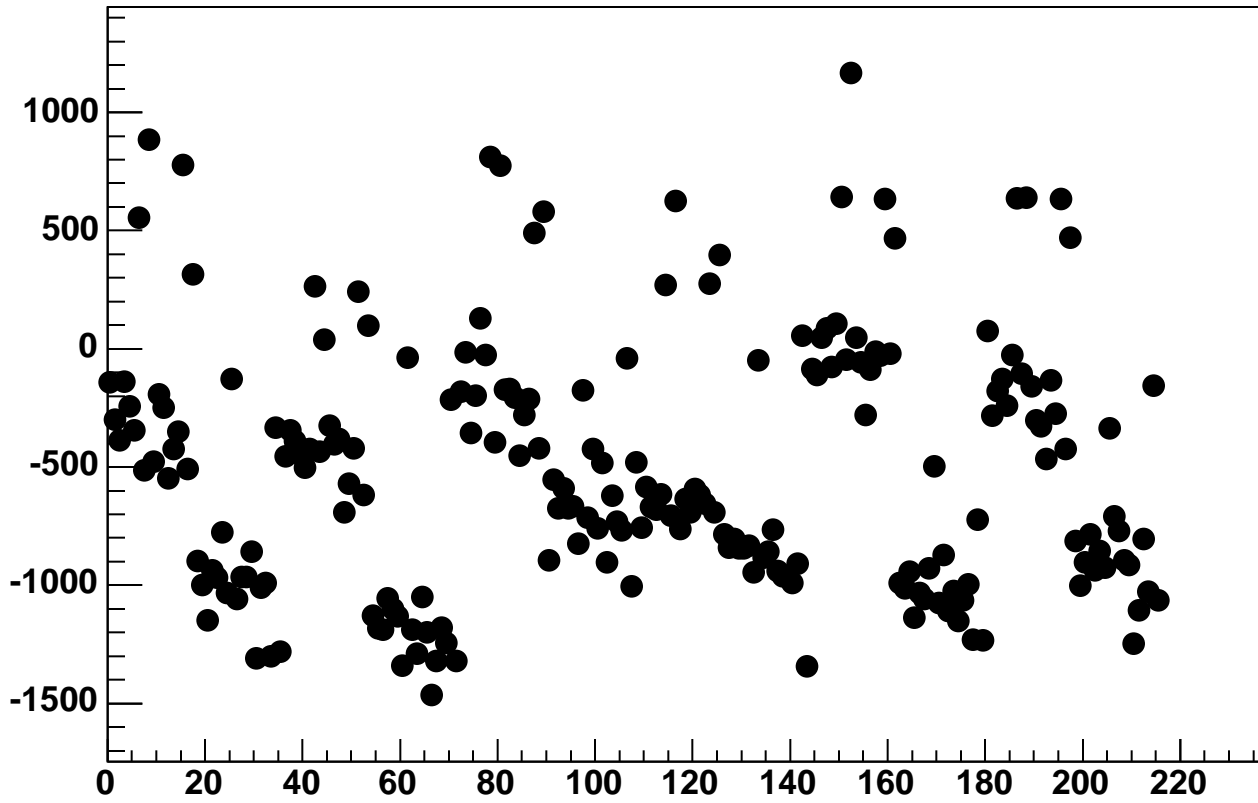
Enable 2, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



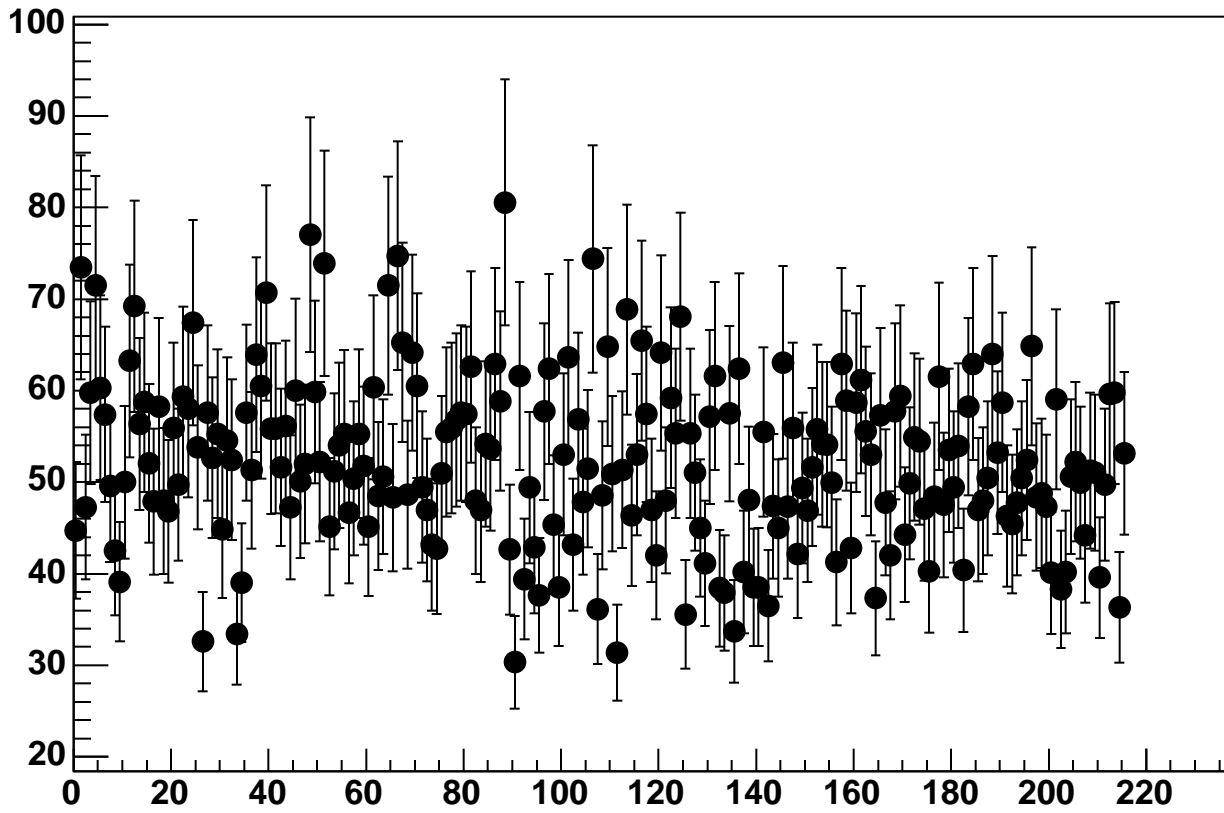
Enable 2, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



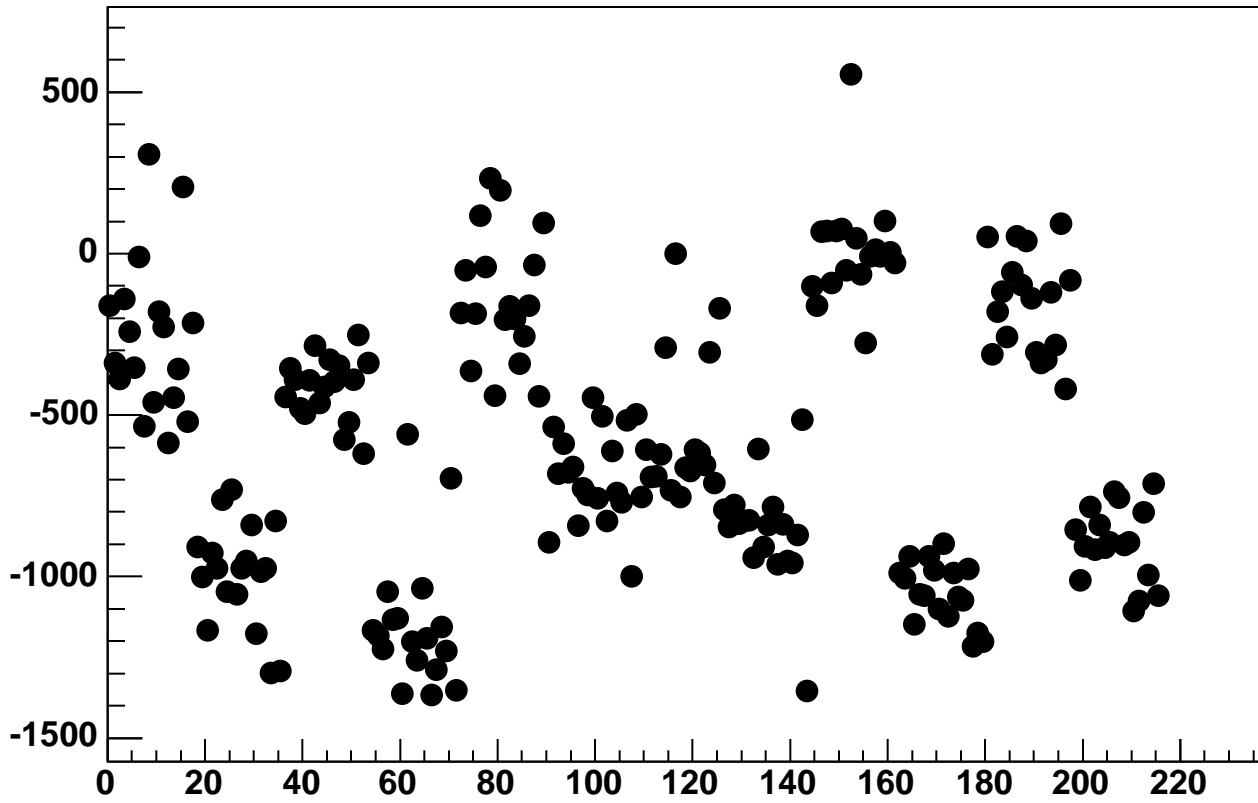
Enable 2, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan



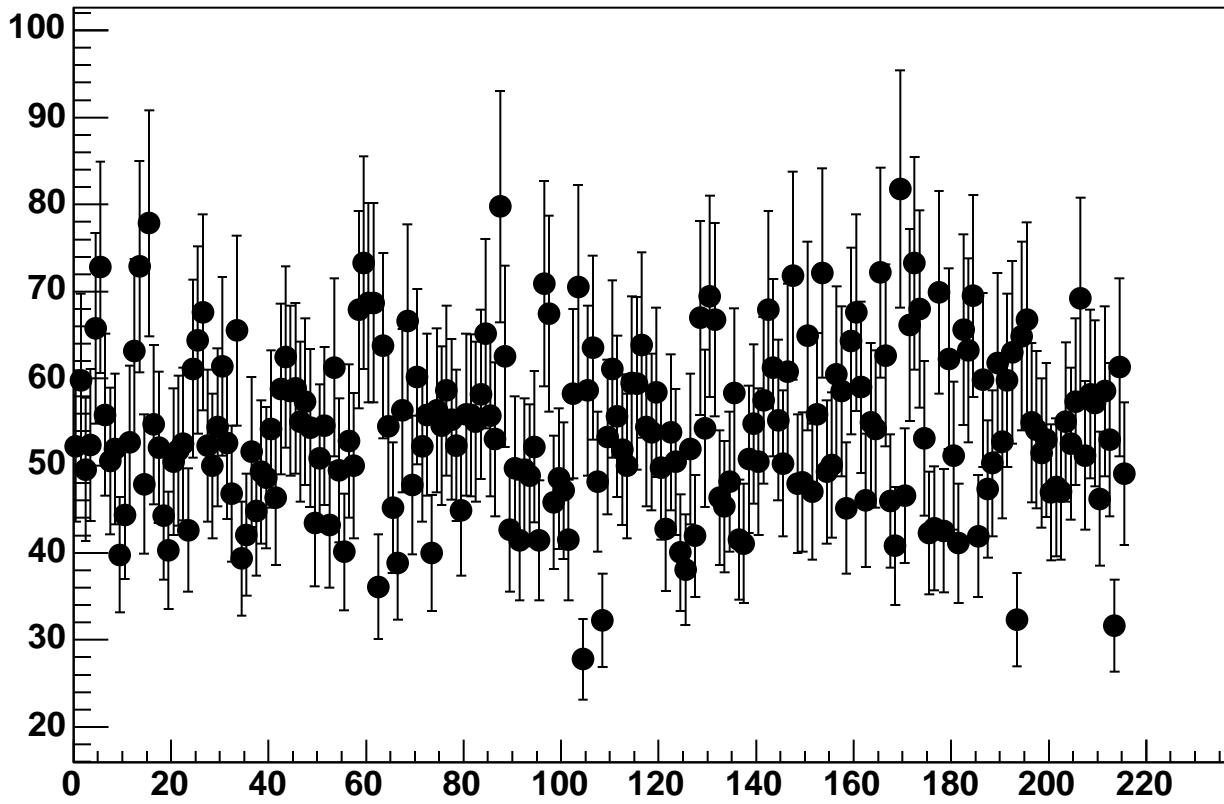
Enable 2, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan



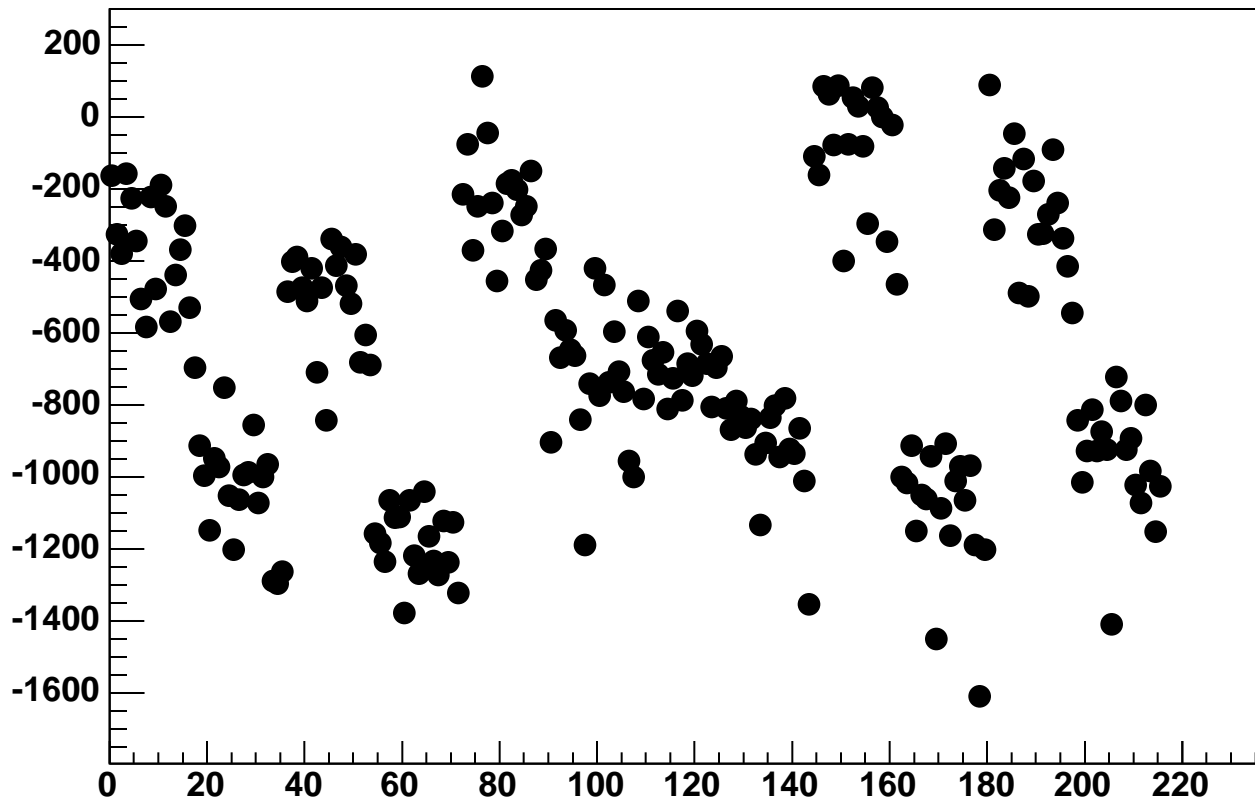
Enable 2, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



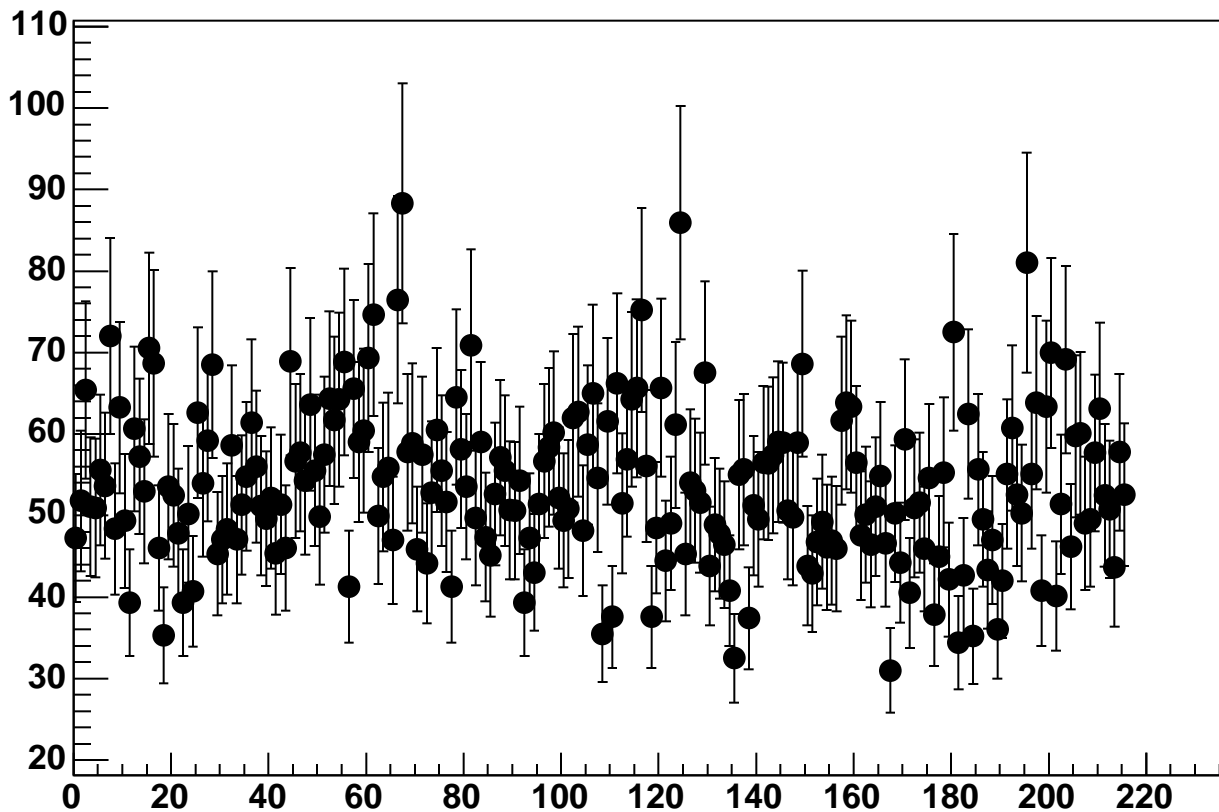
Enable 2, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



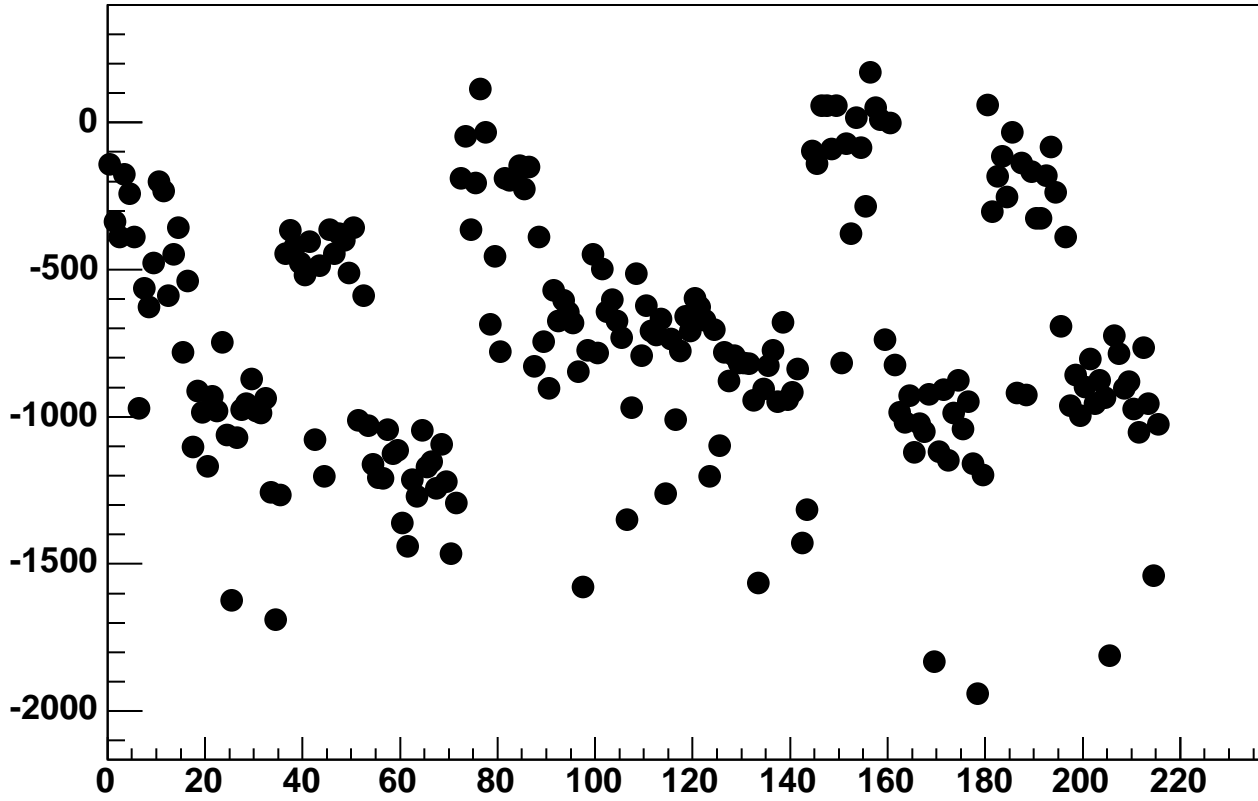
Enable 2, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan



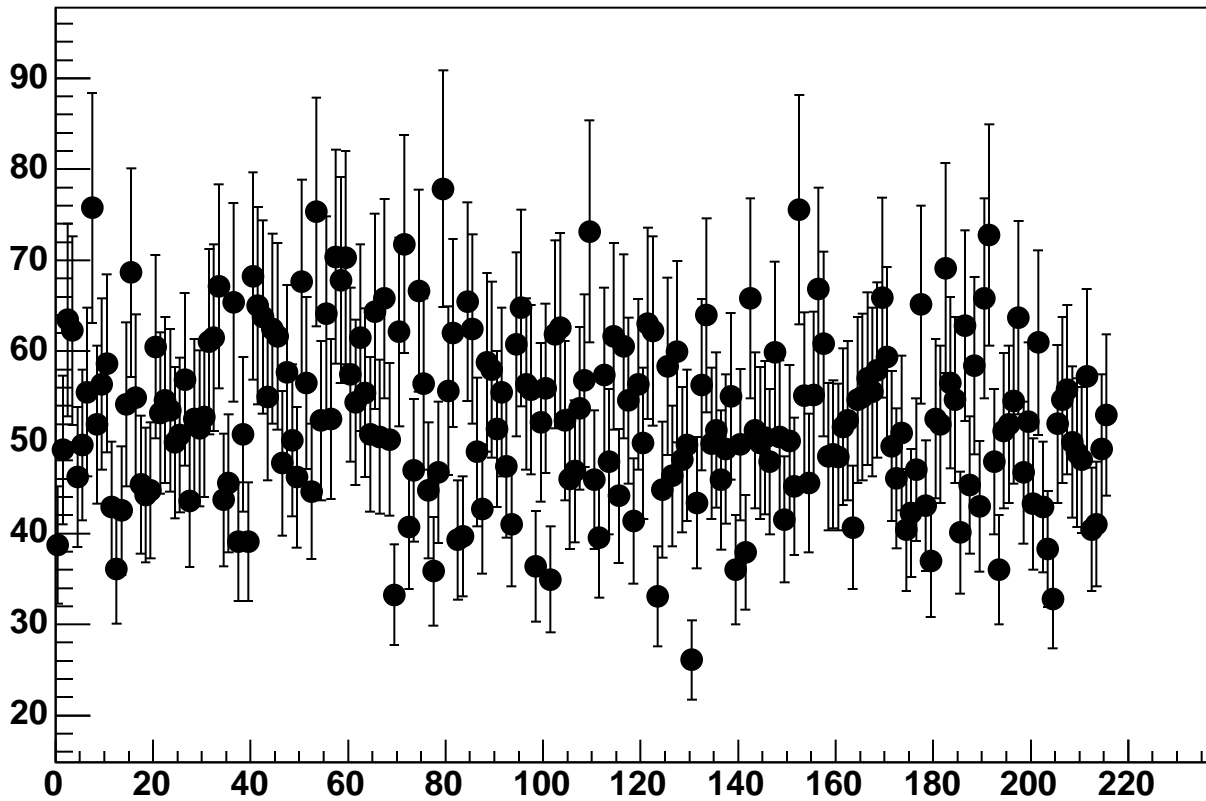
Enable 2, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan



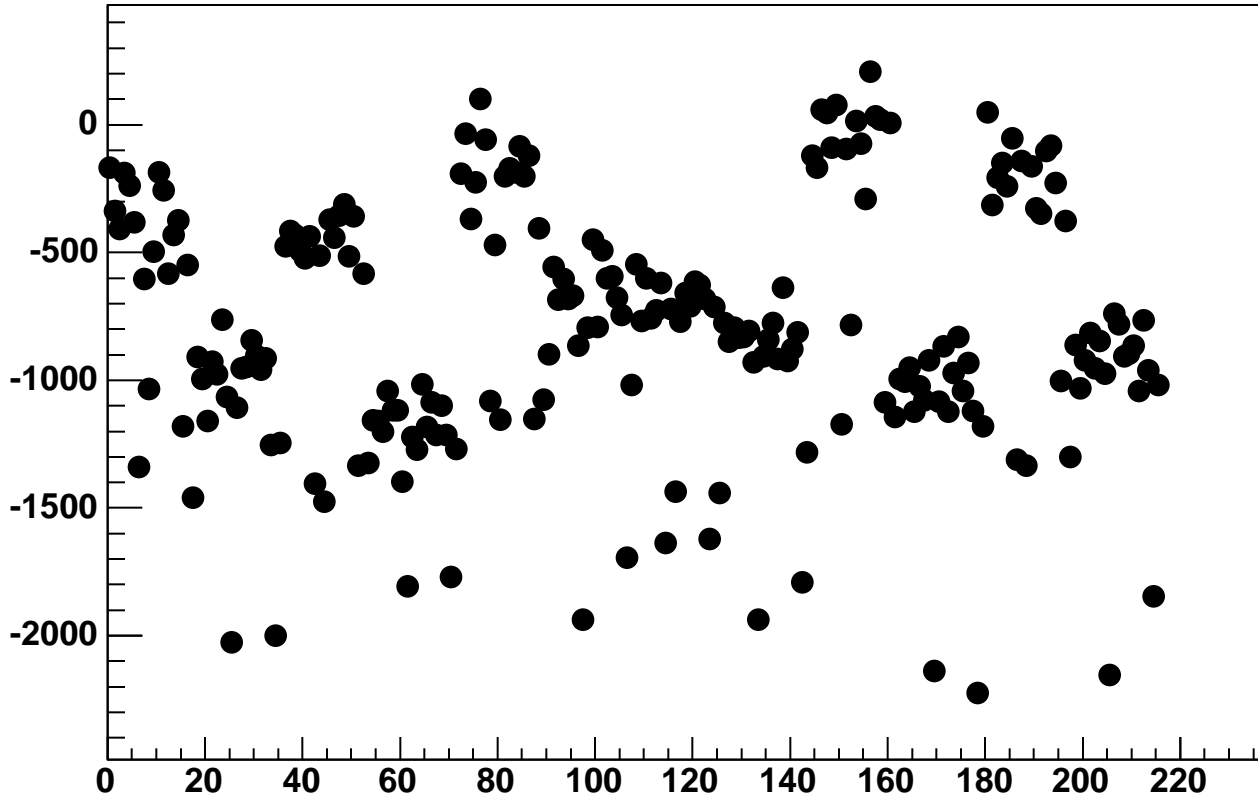
Enable 2, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



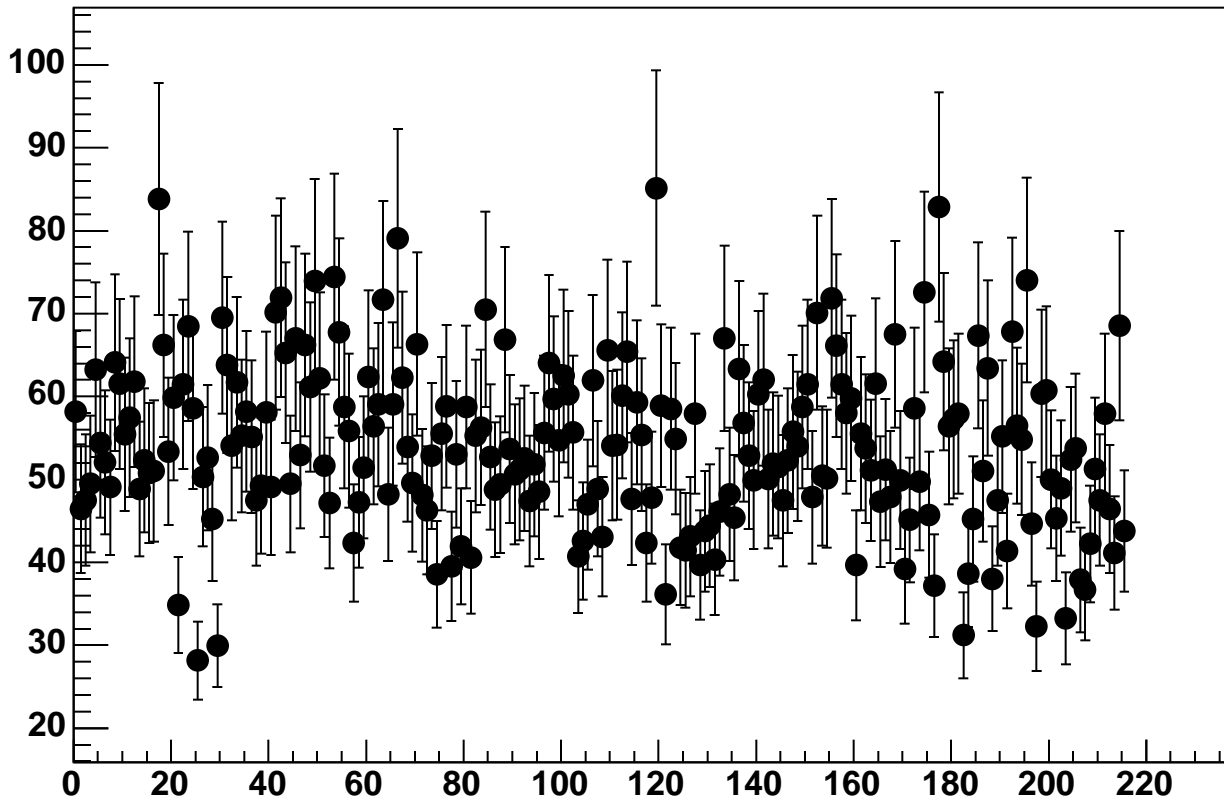
Enable 2, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



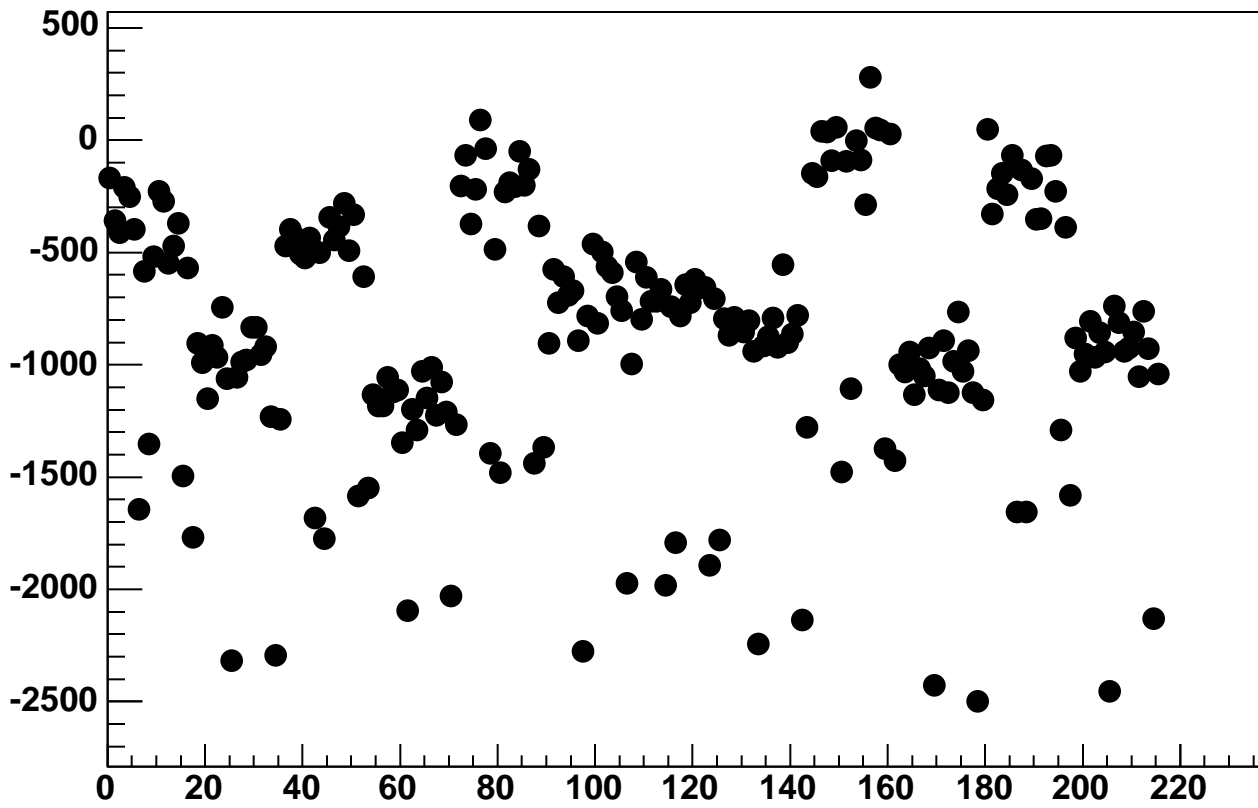
Enable 2, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan



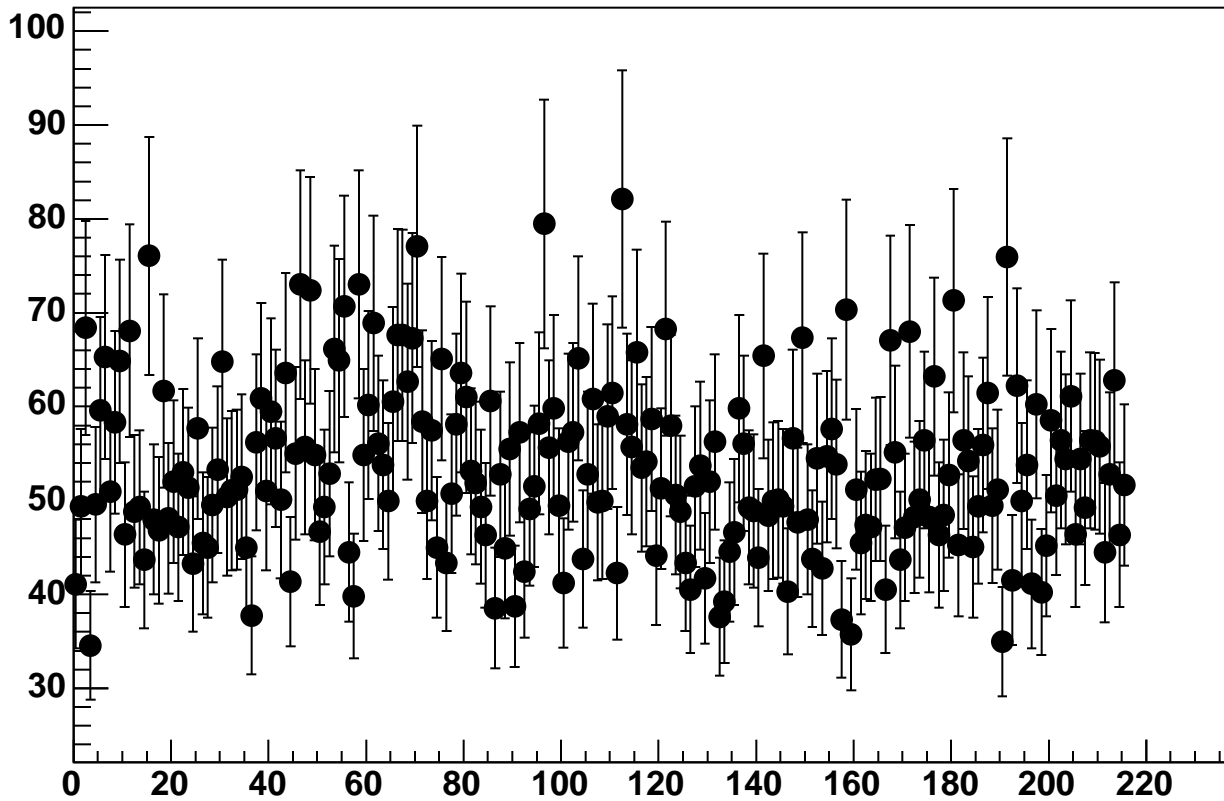
Enable 2, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan



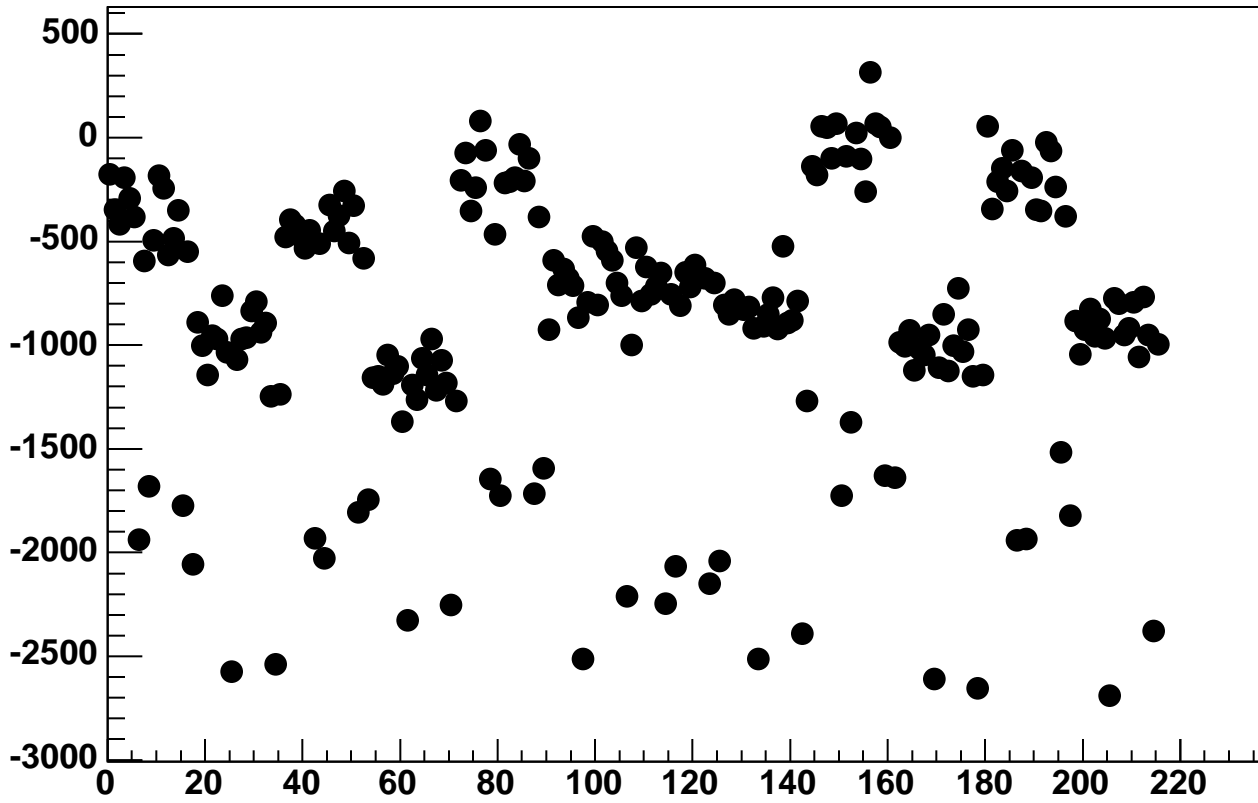
Enable 2, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



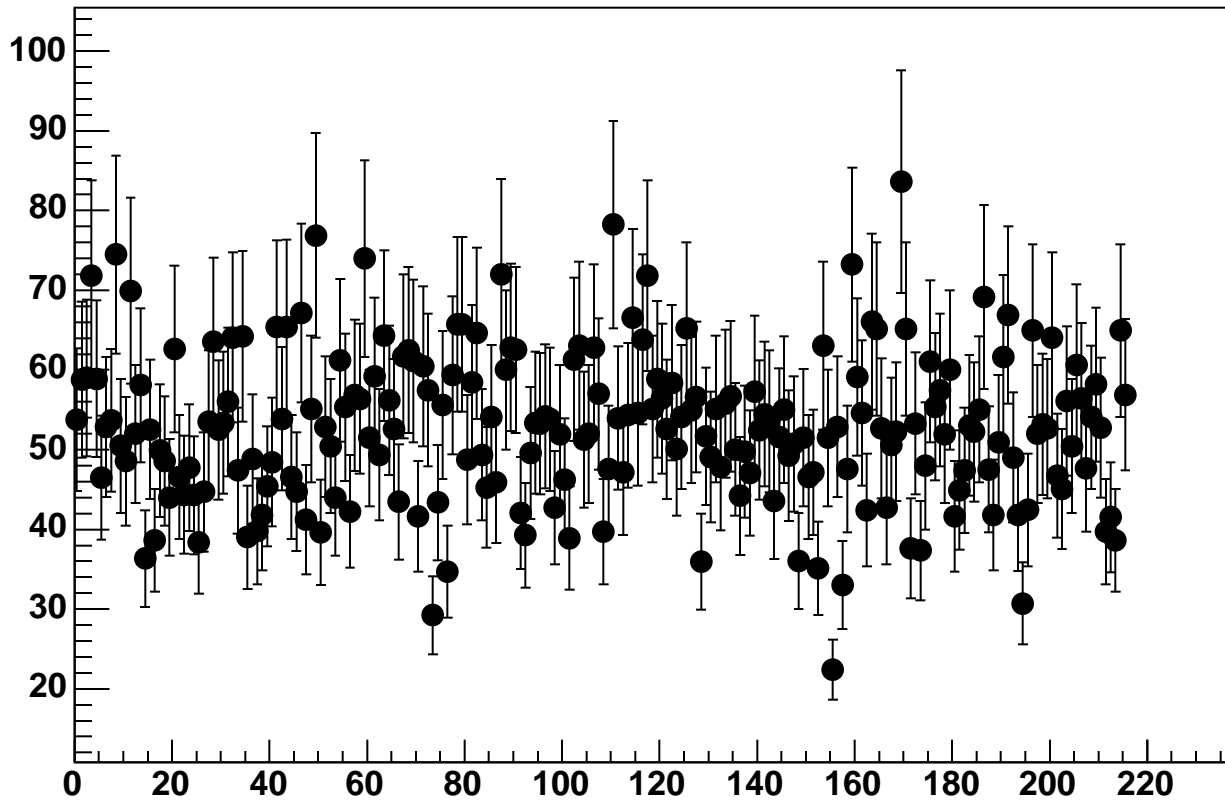
Enable 2, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan

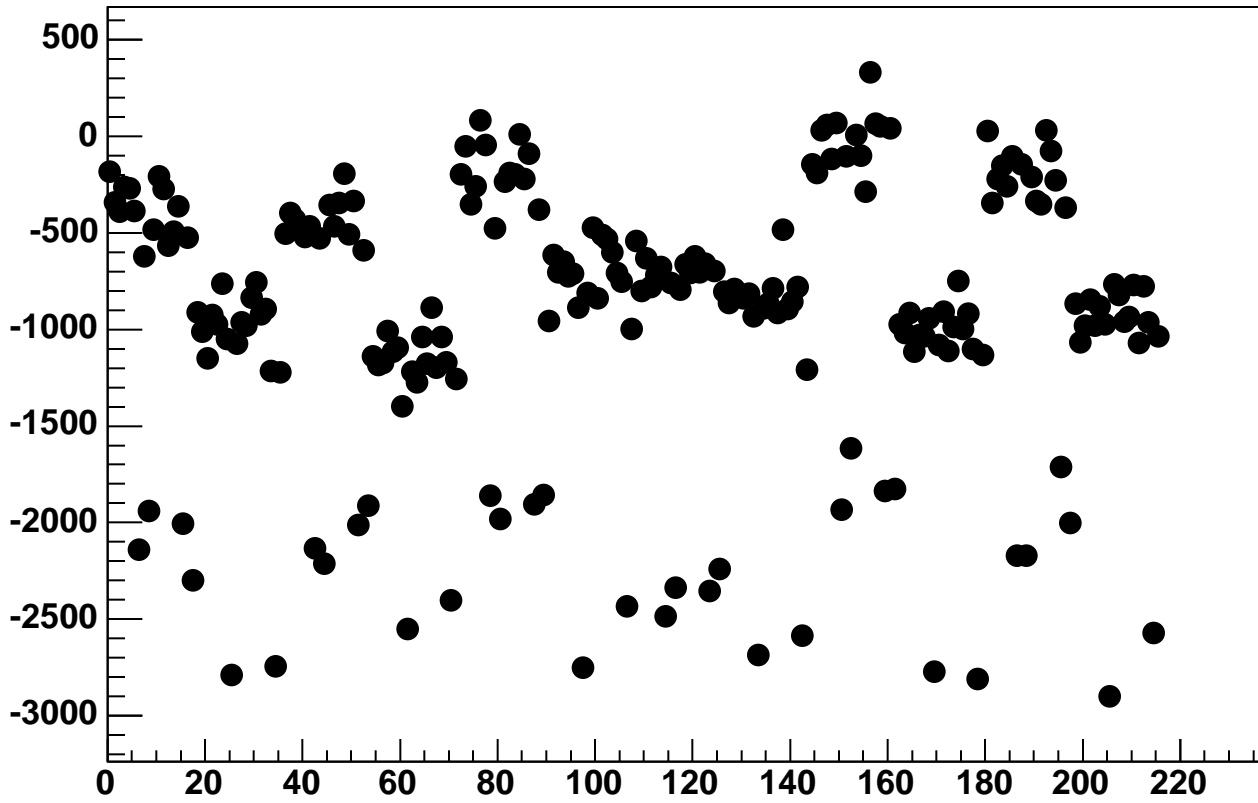


Enable 2, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan

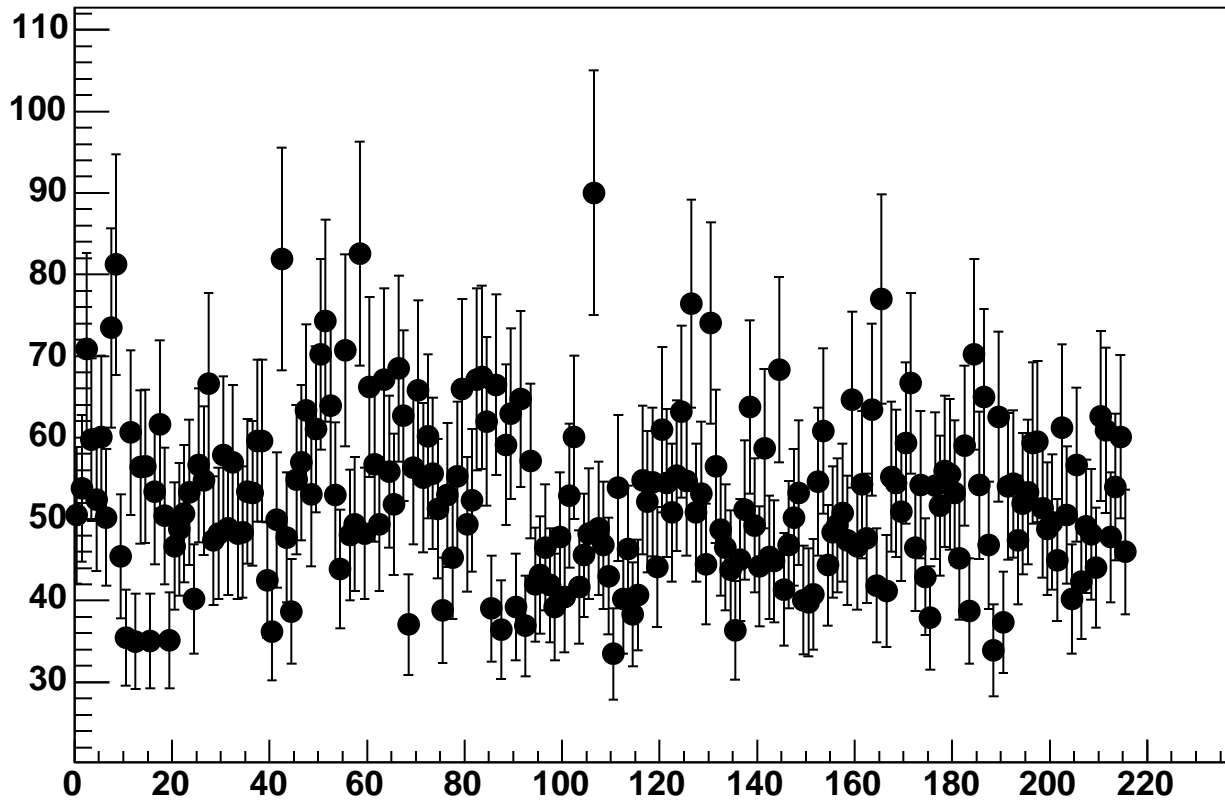




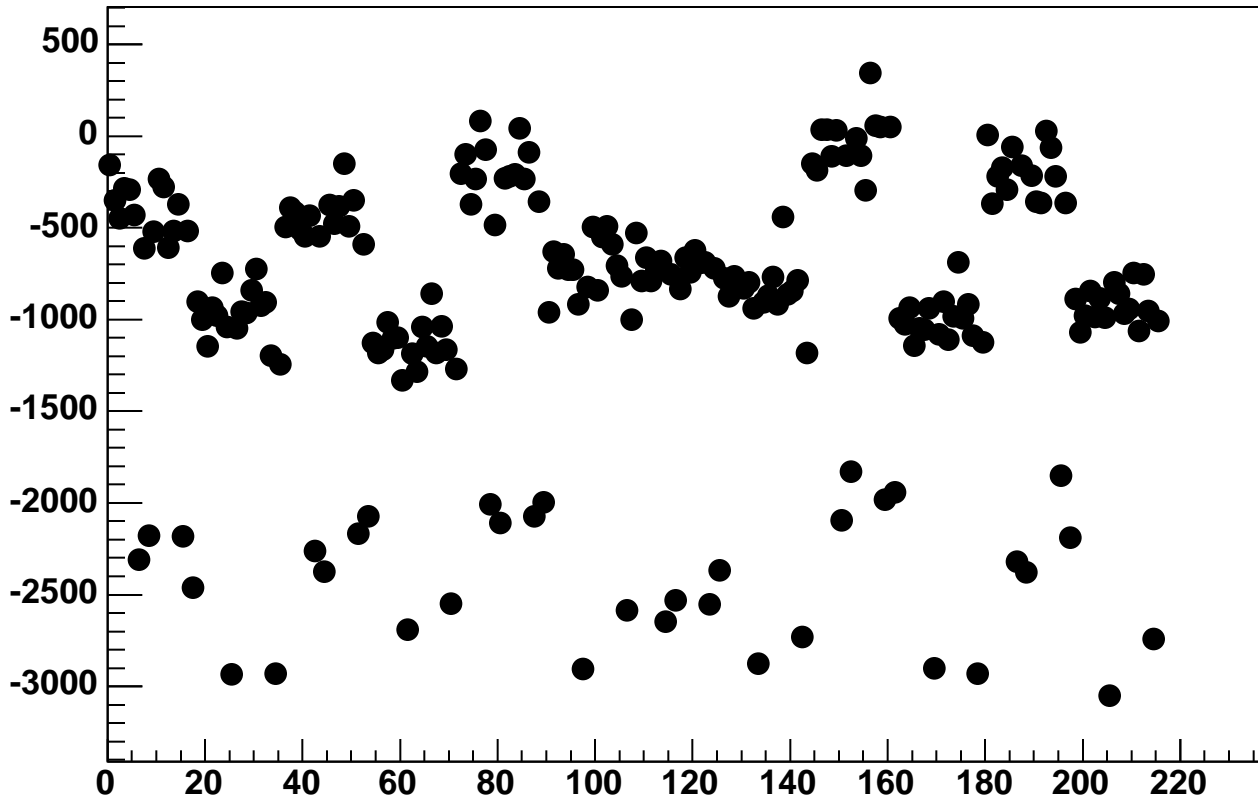
Enable 2, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



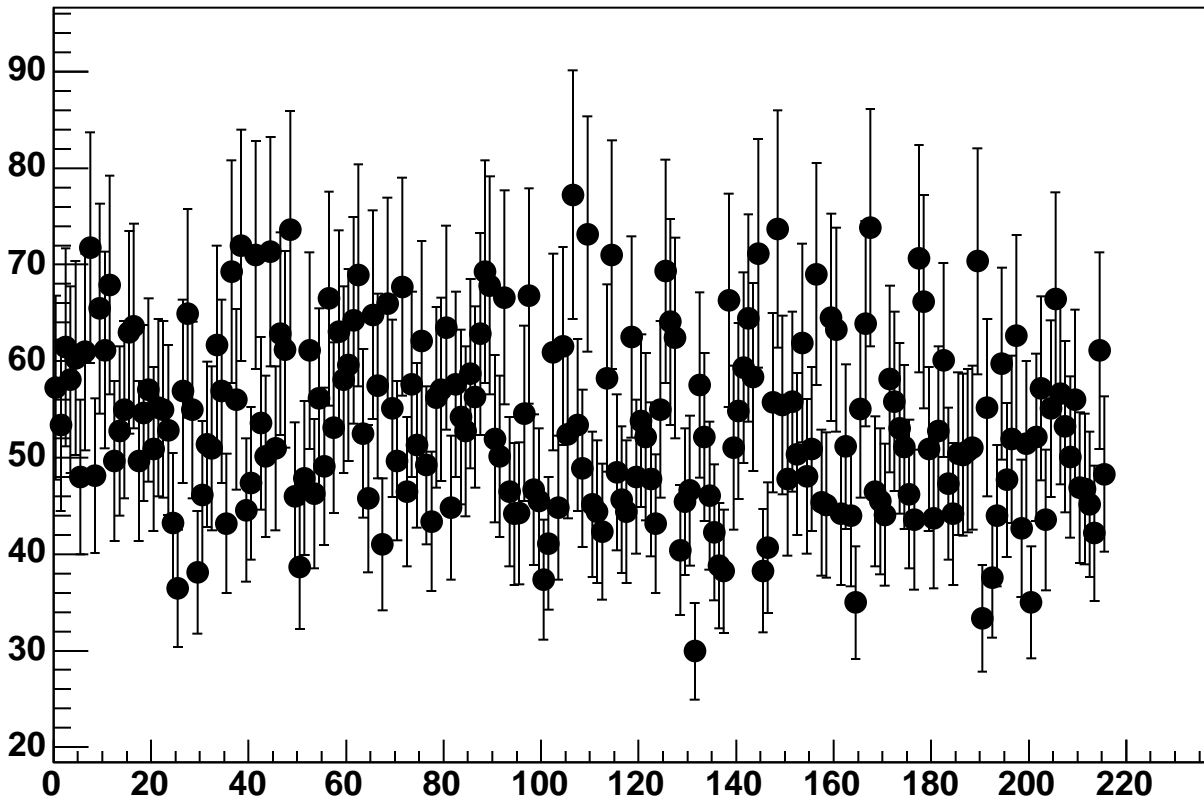
Enable 2, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



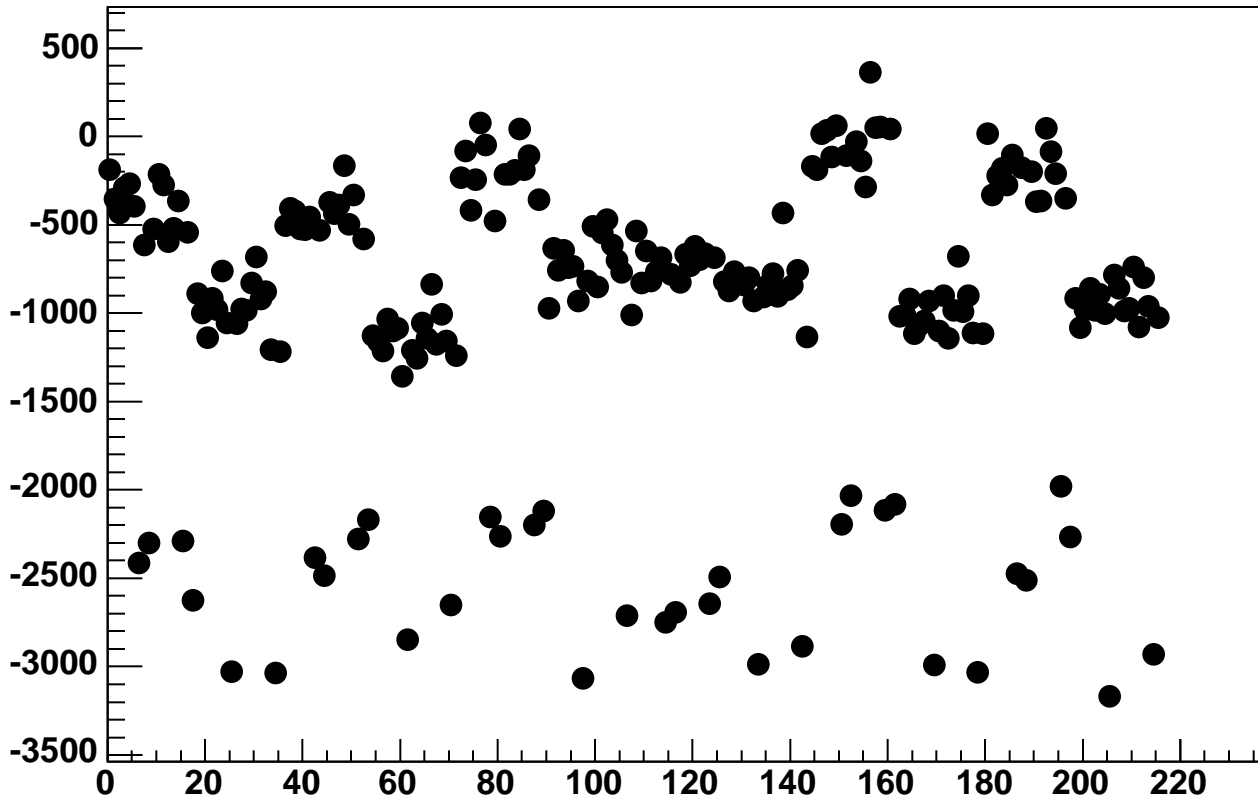
Enable 2, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan



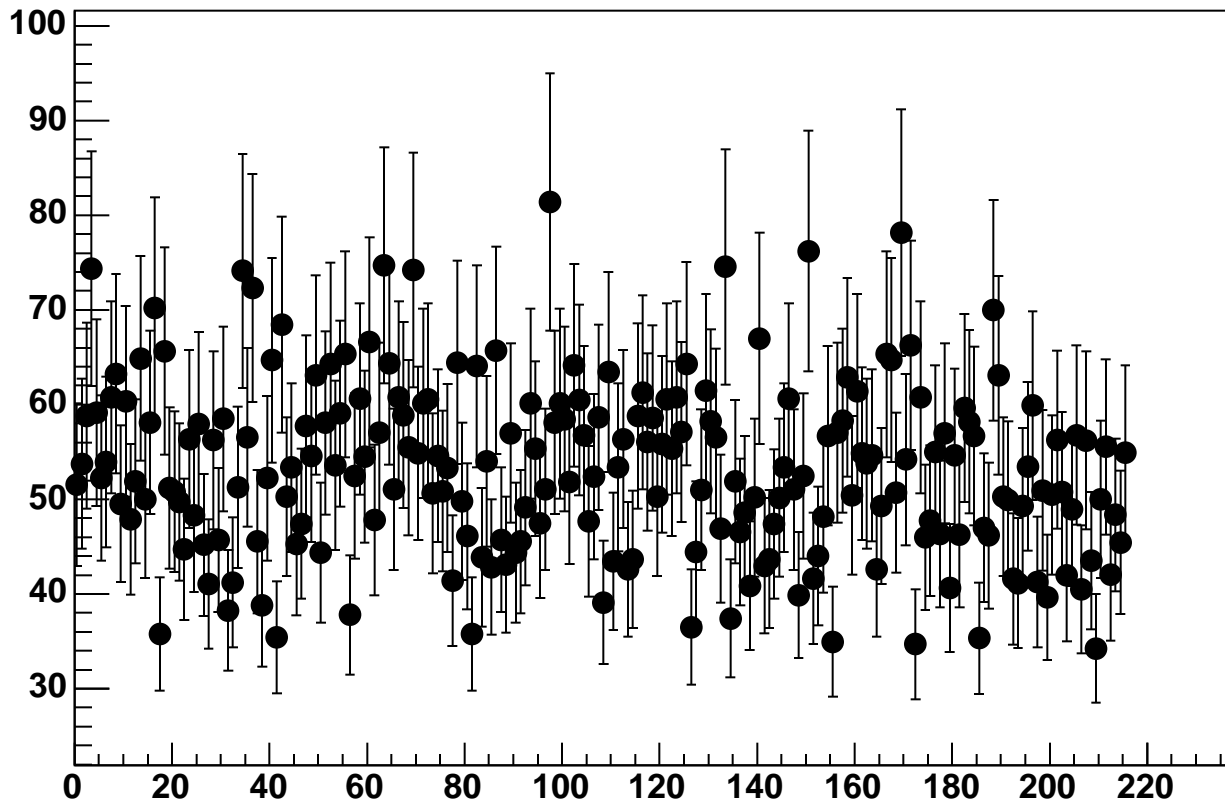
Enable 2, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan



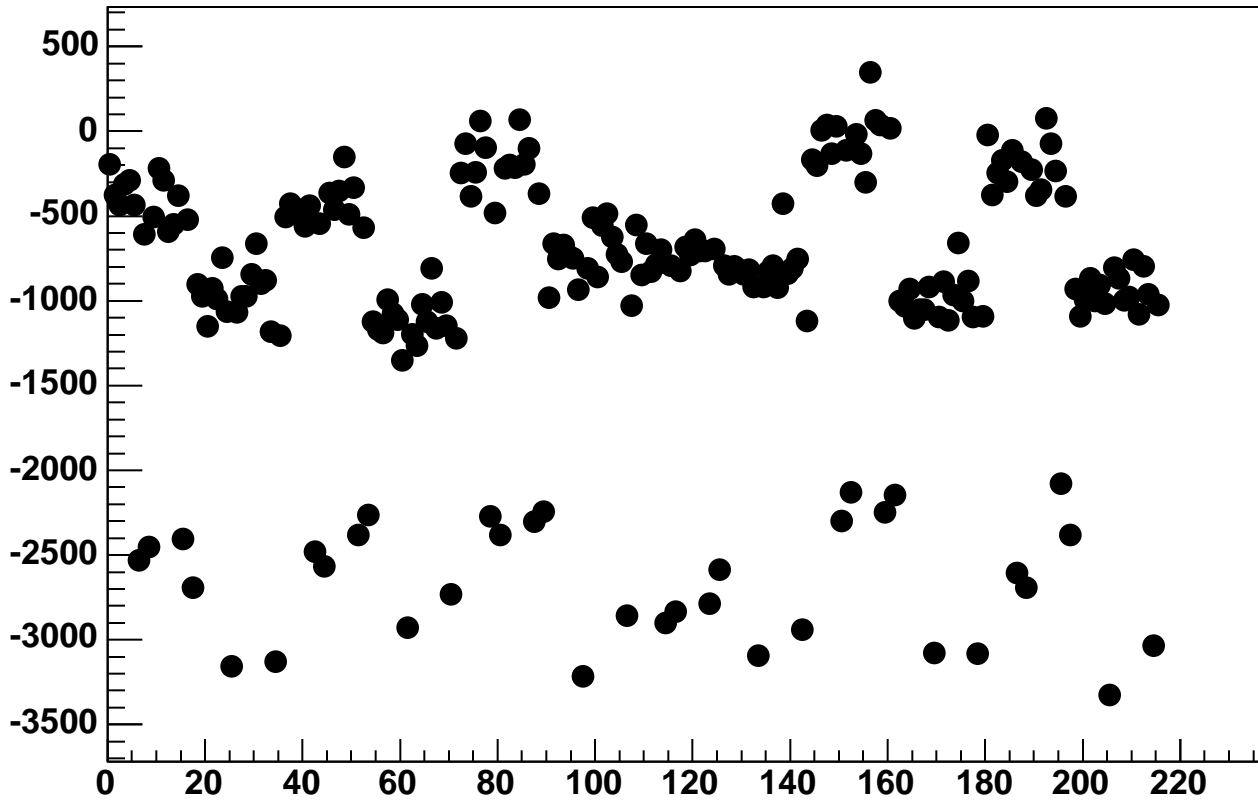
Enable 2, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



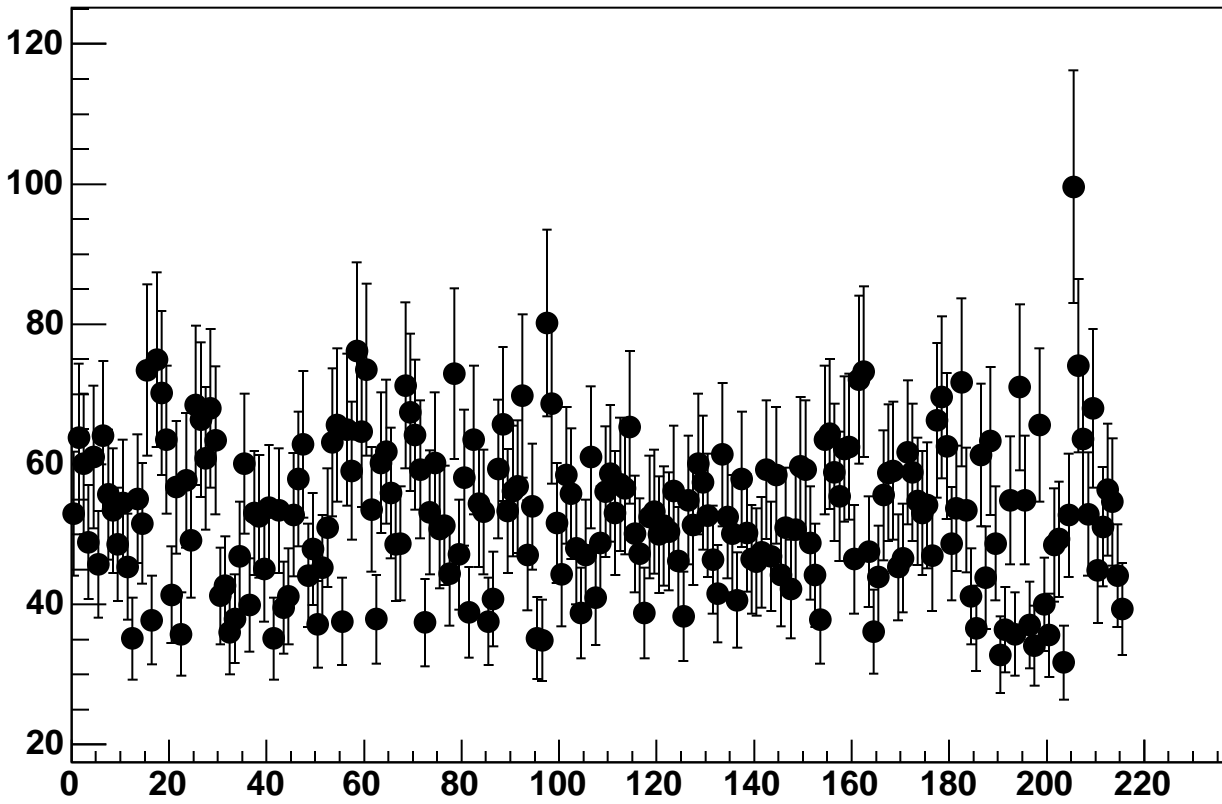
Enable 2, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



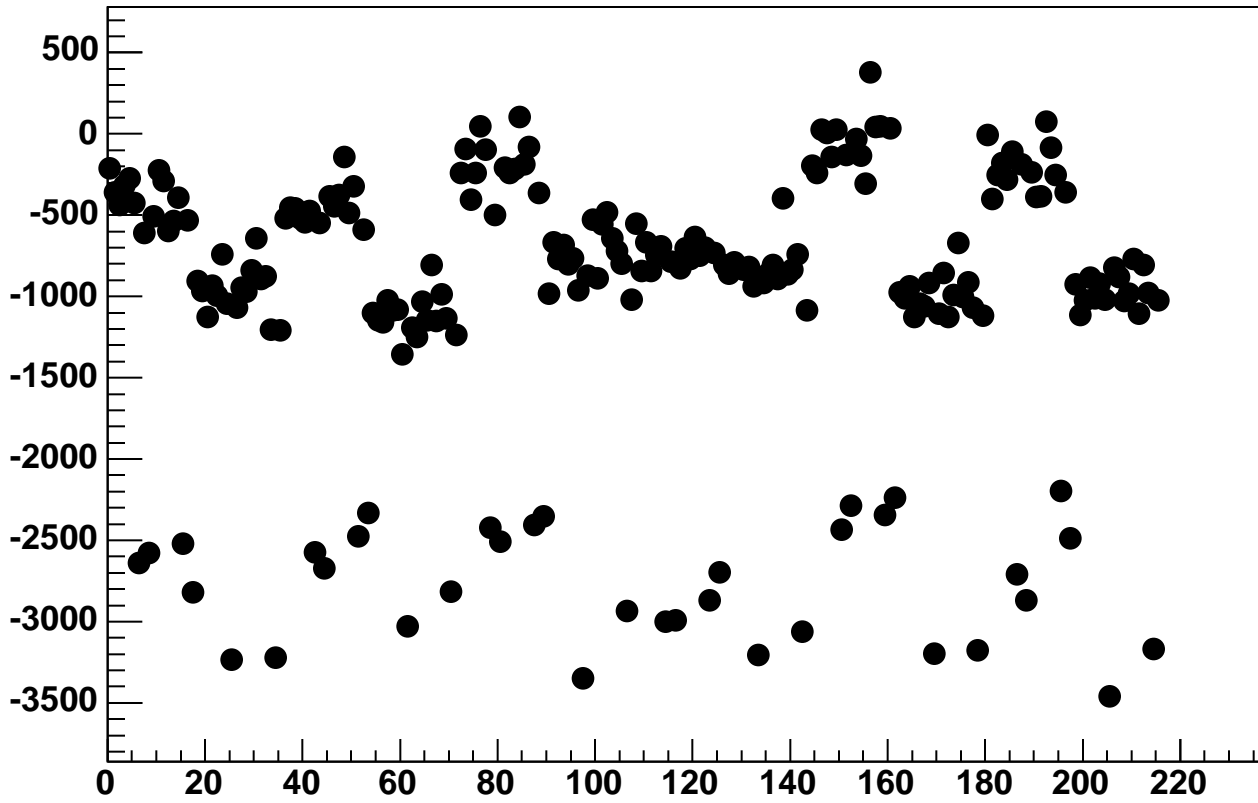
Enable 2, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan



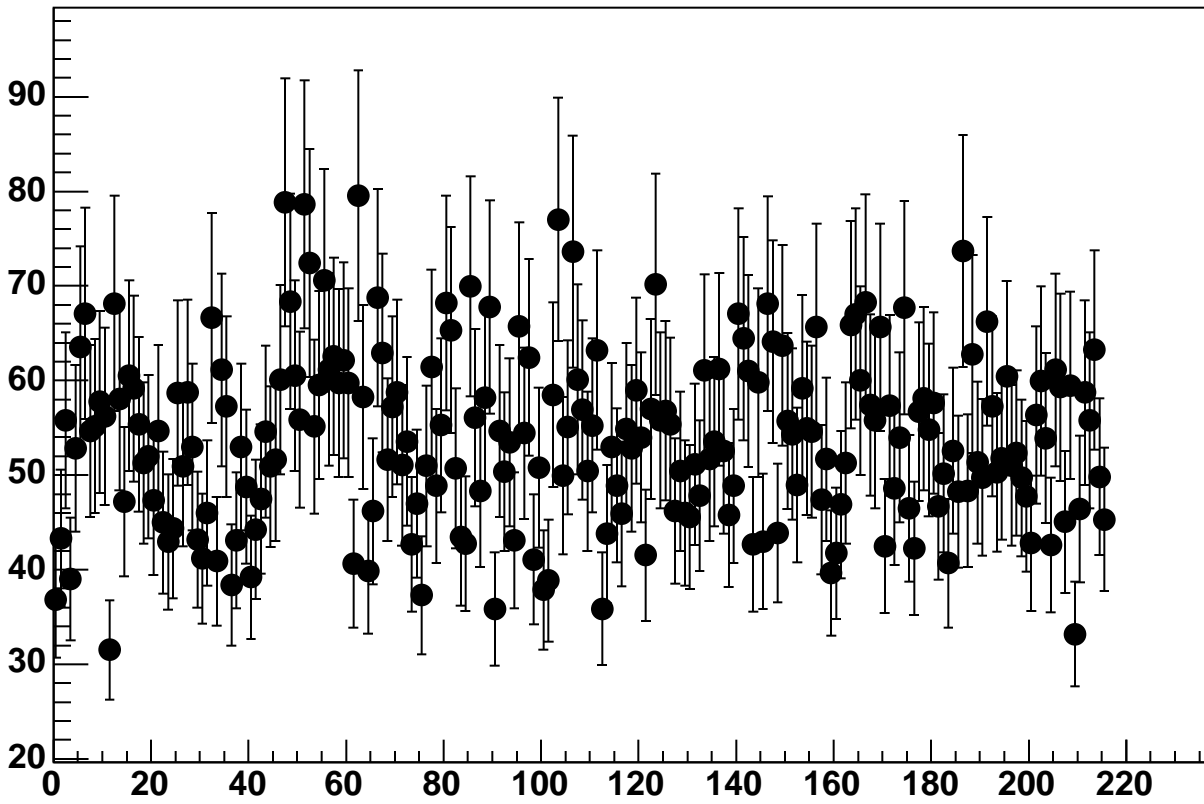
Enable 2, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan



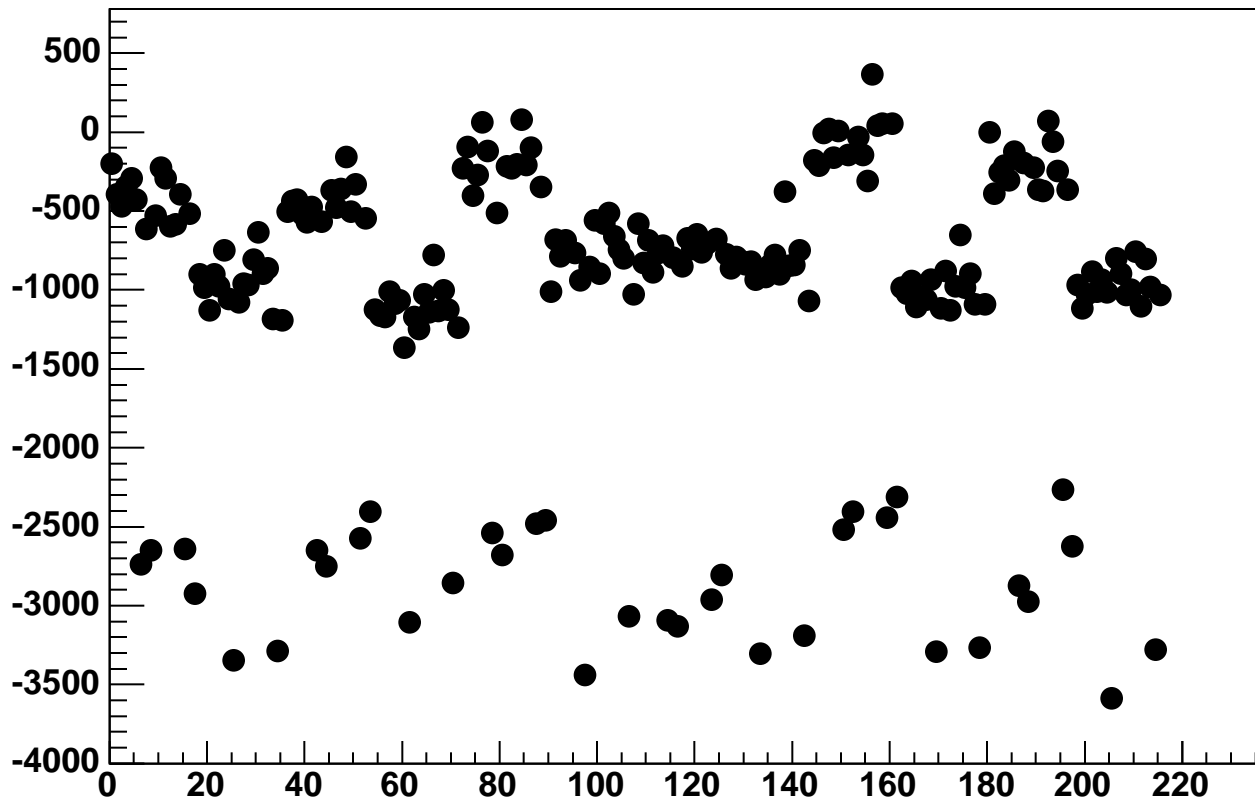
Enable 2, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



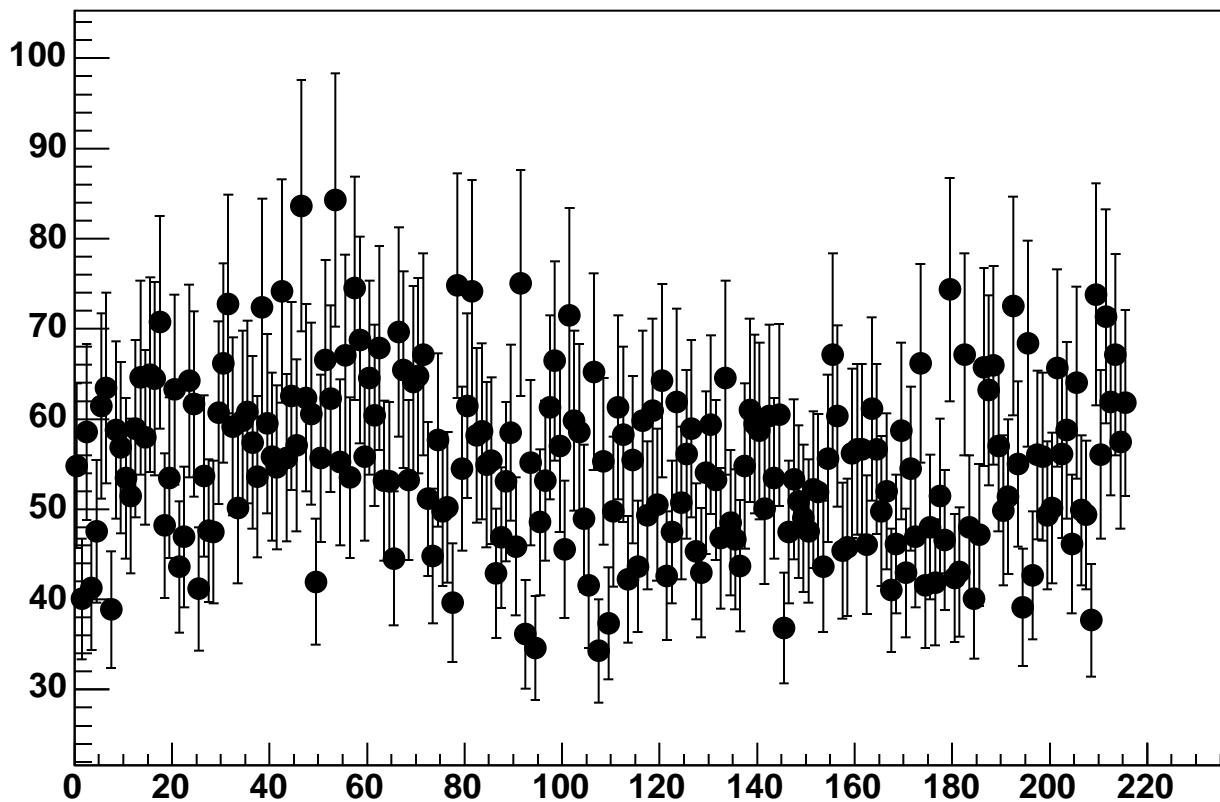
Enable 2, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



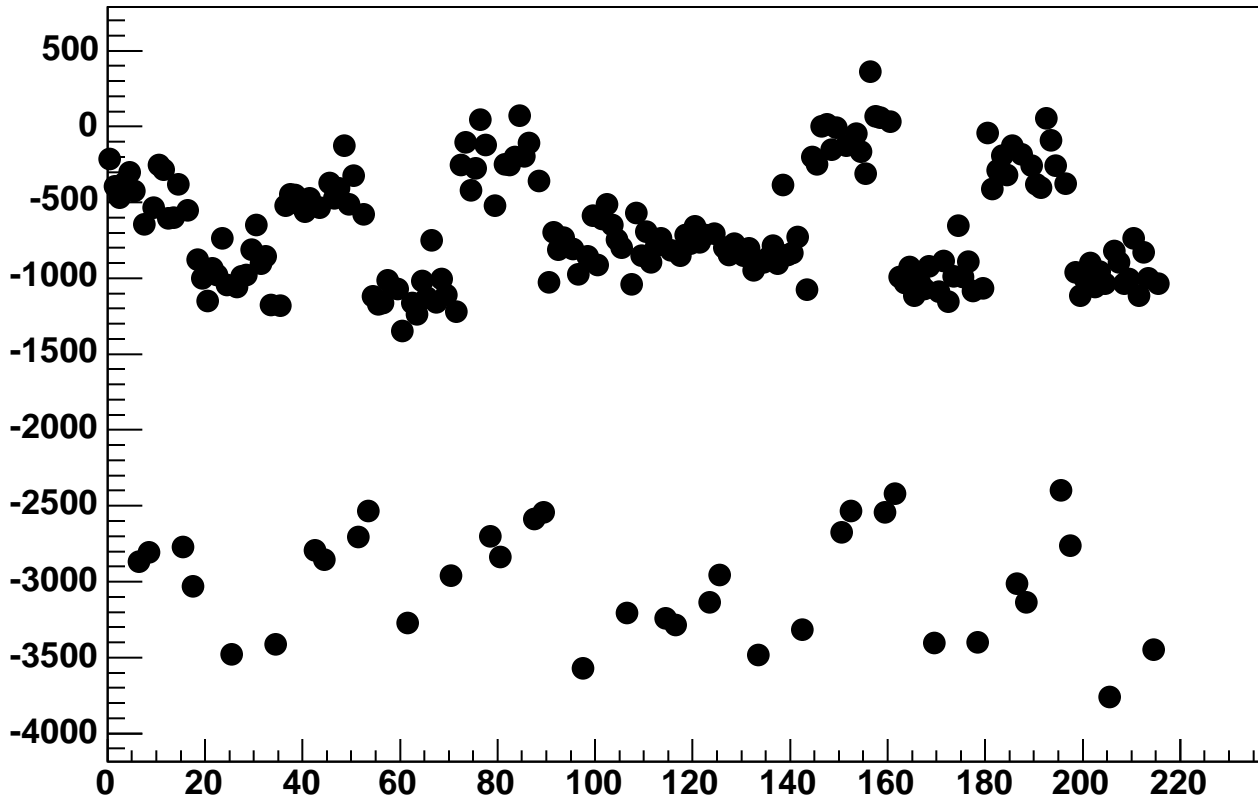
Enable 2, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan



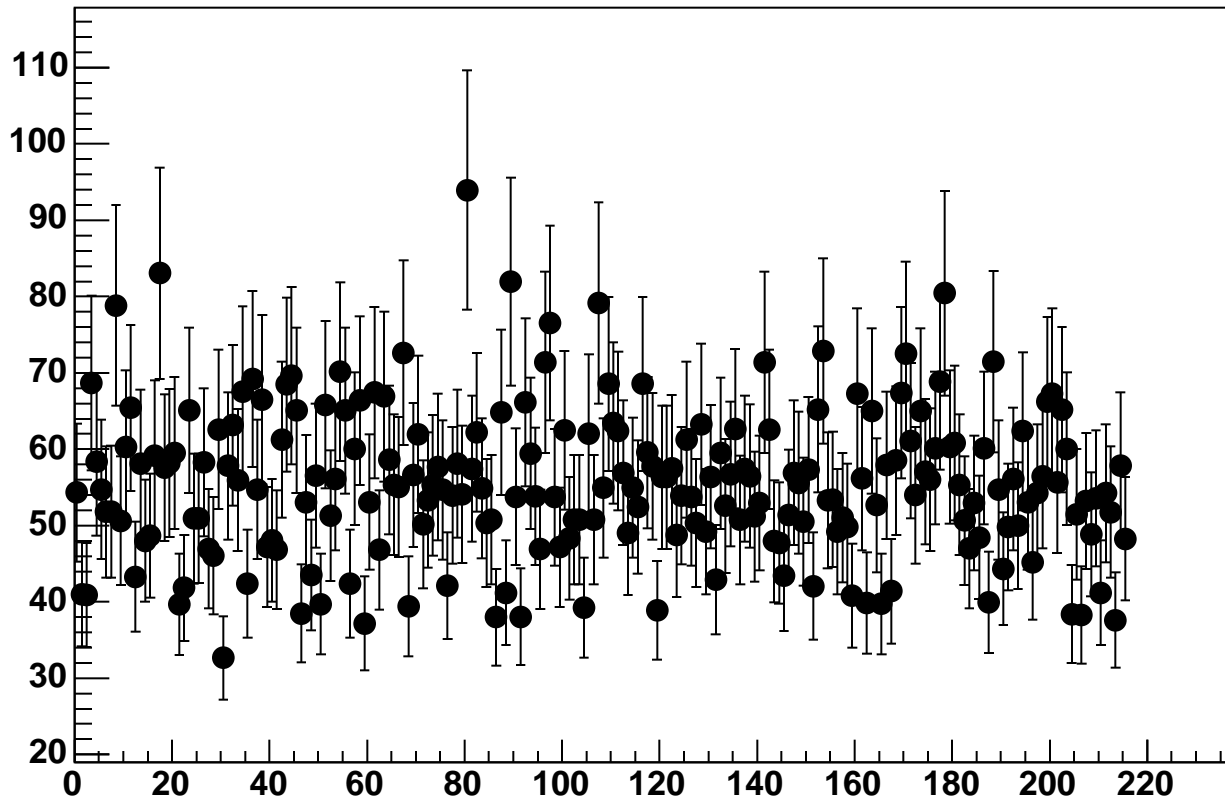
Enable 2, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan



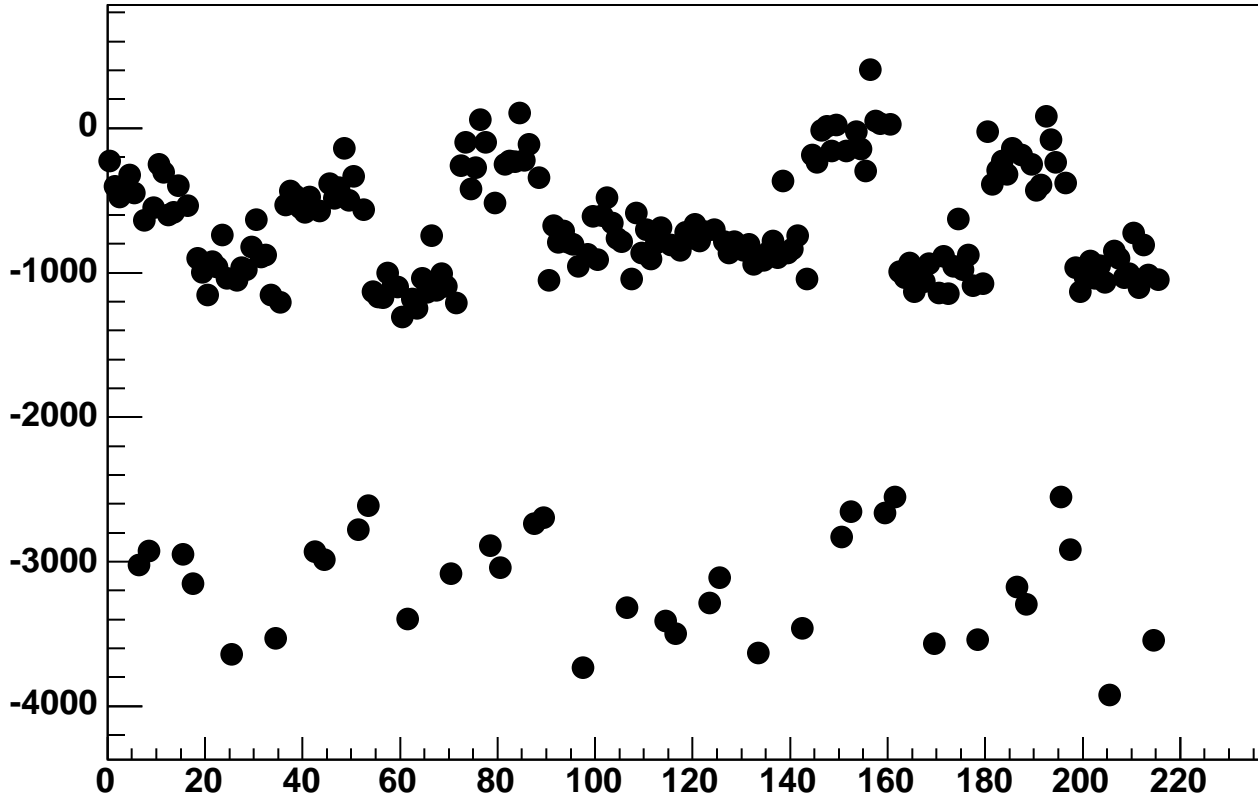
Enable 2, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



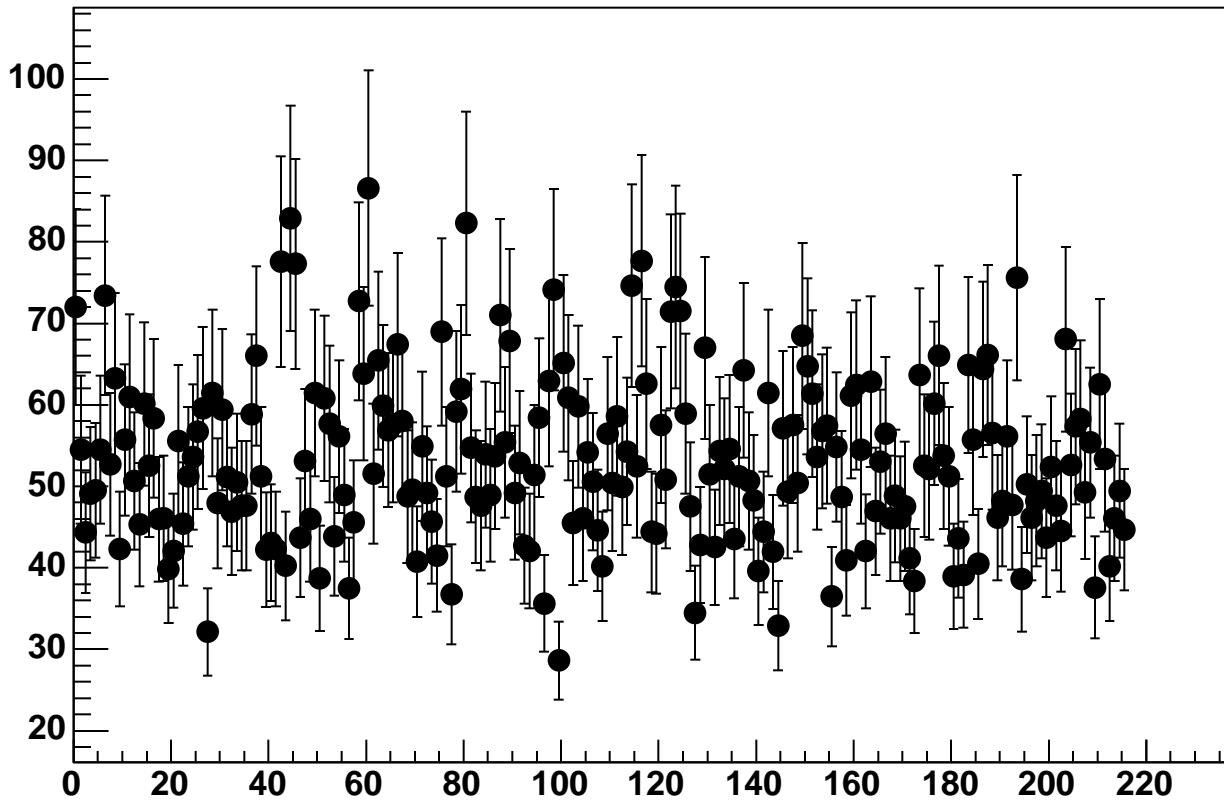
Enable 2, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan

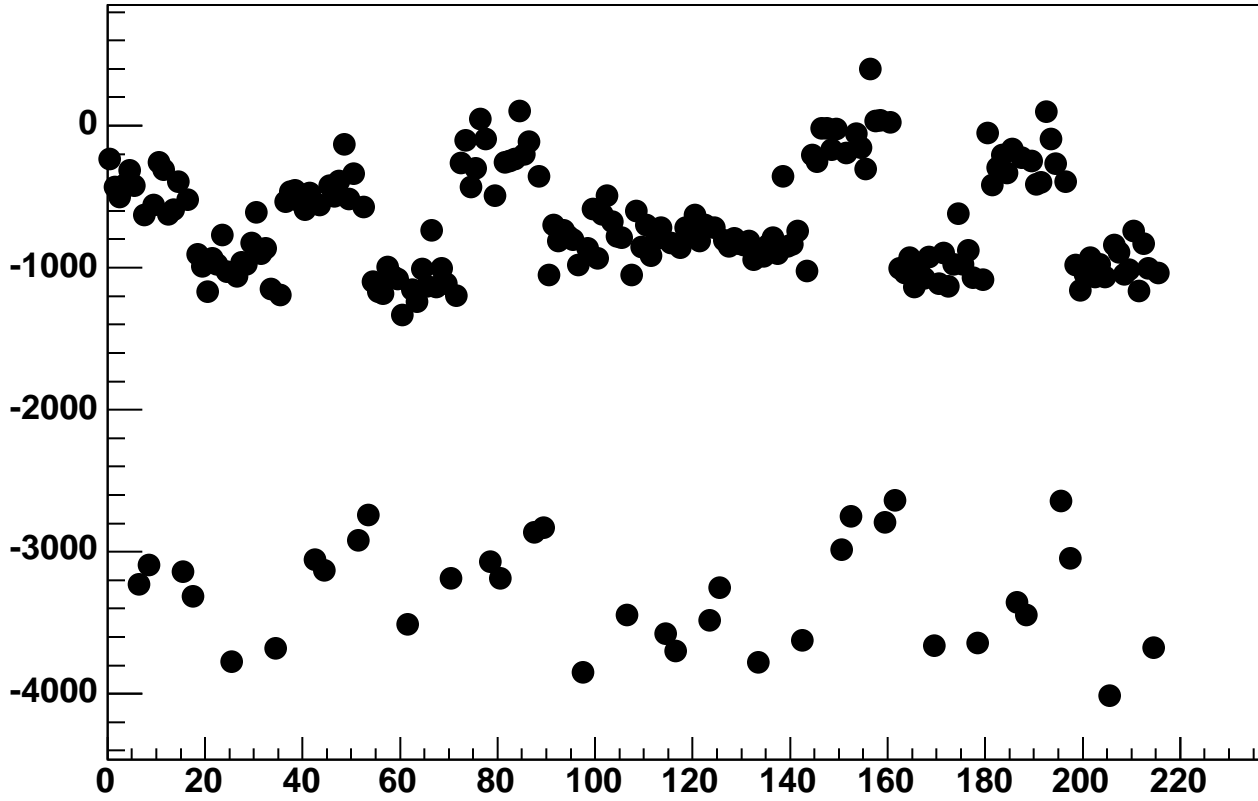


Enable 2, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan

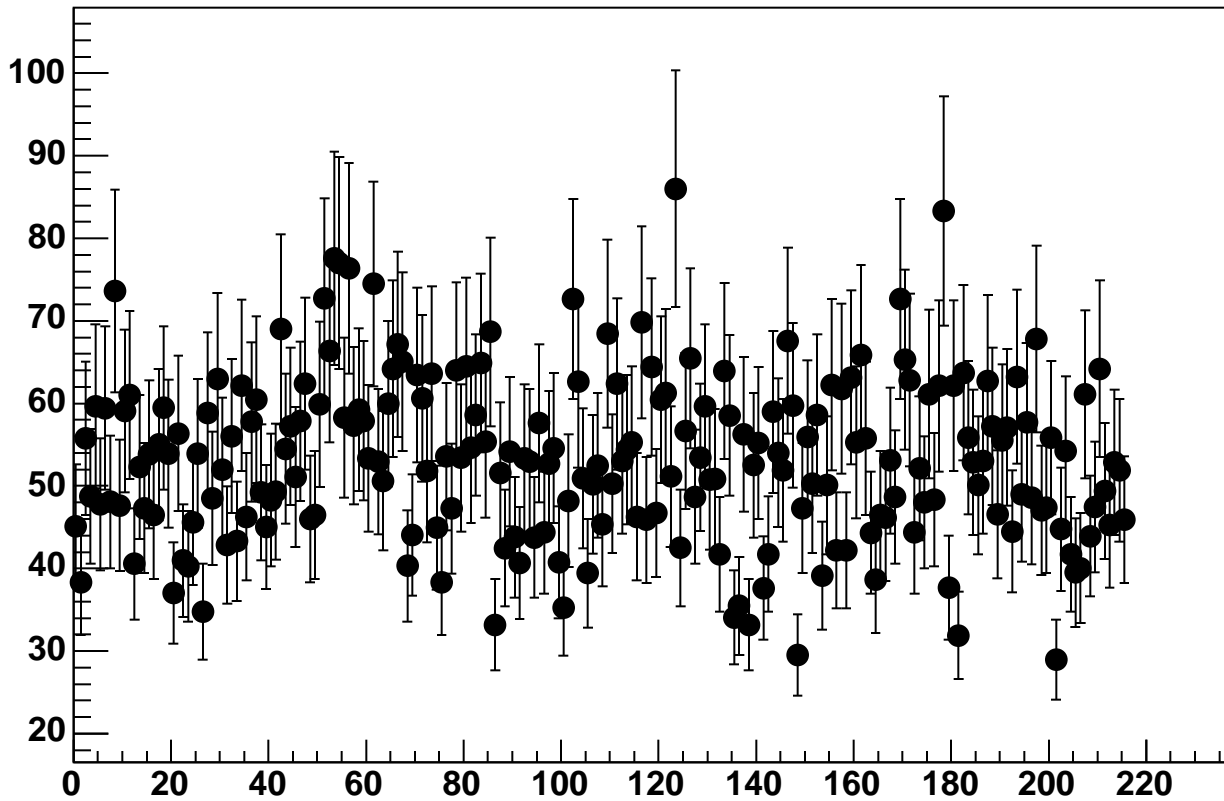




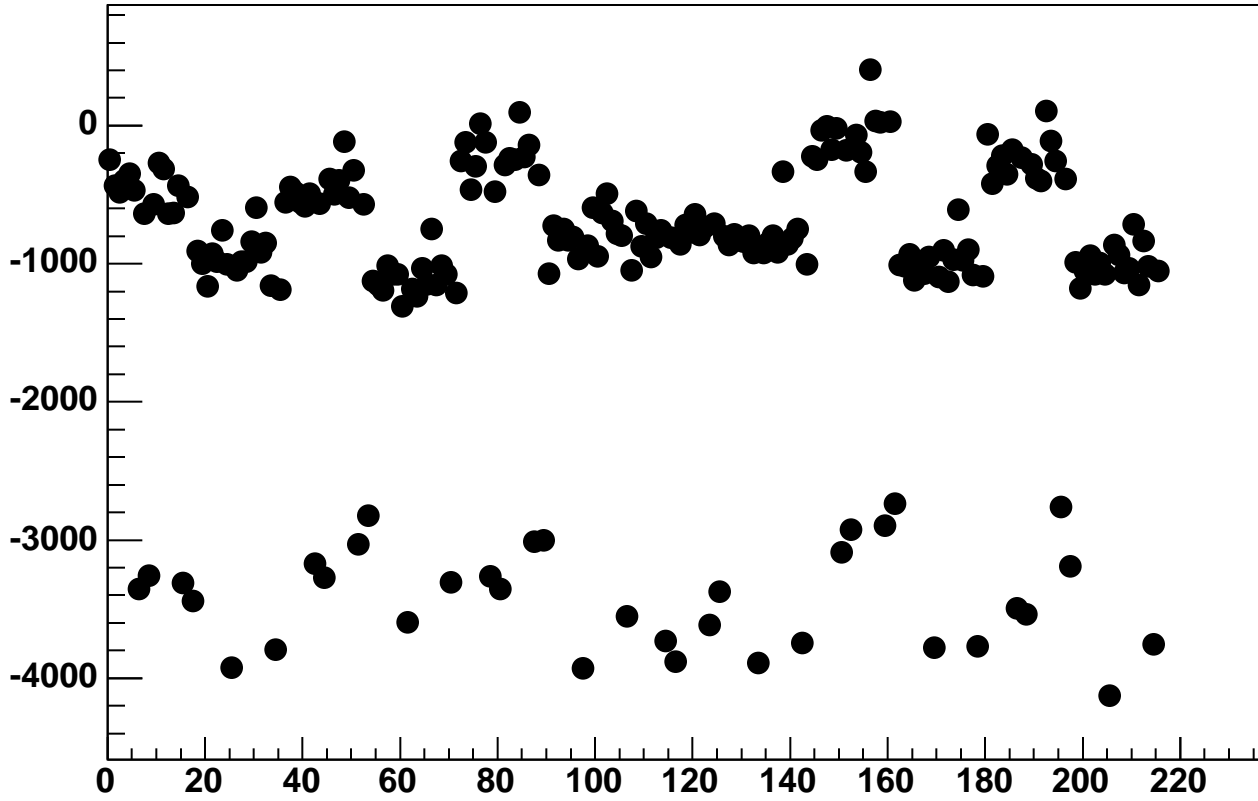
Enable 2, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



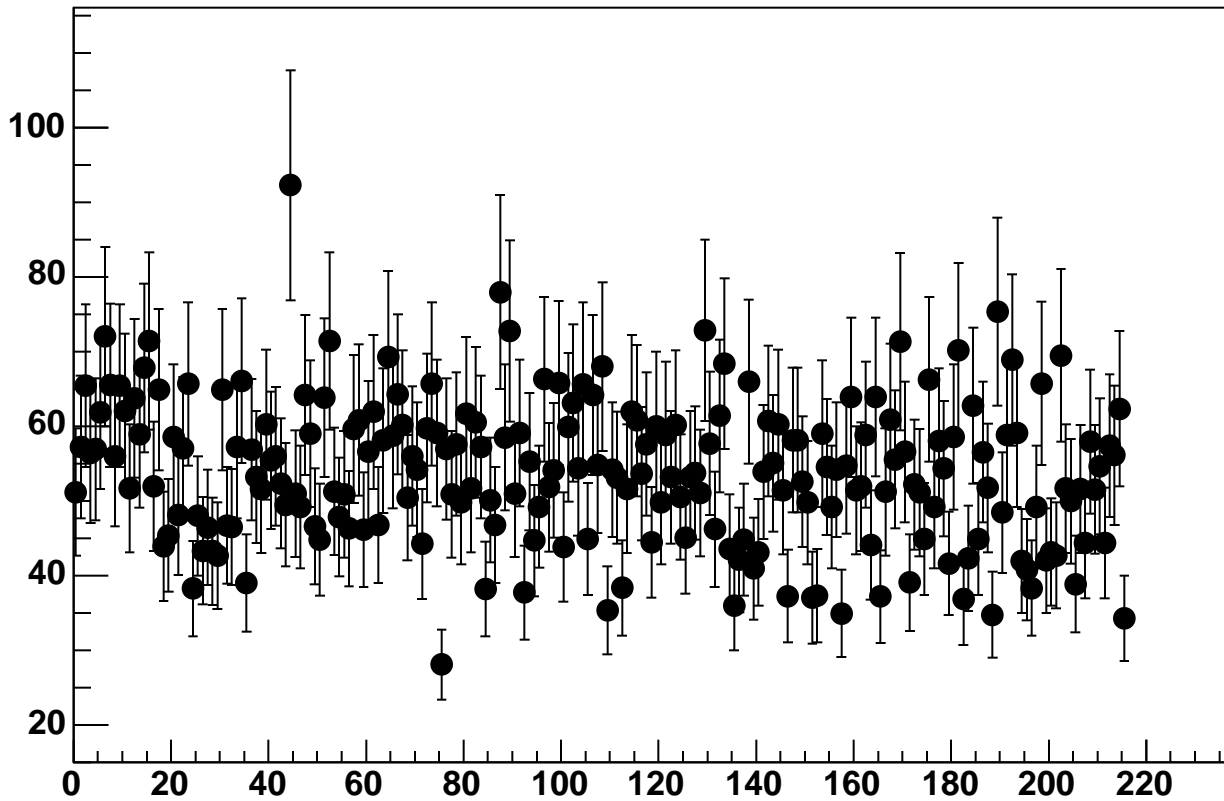
Enable 2, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



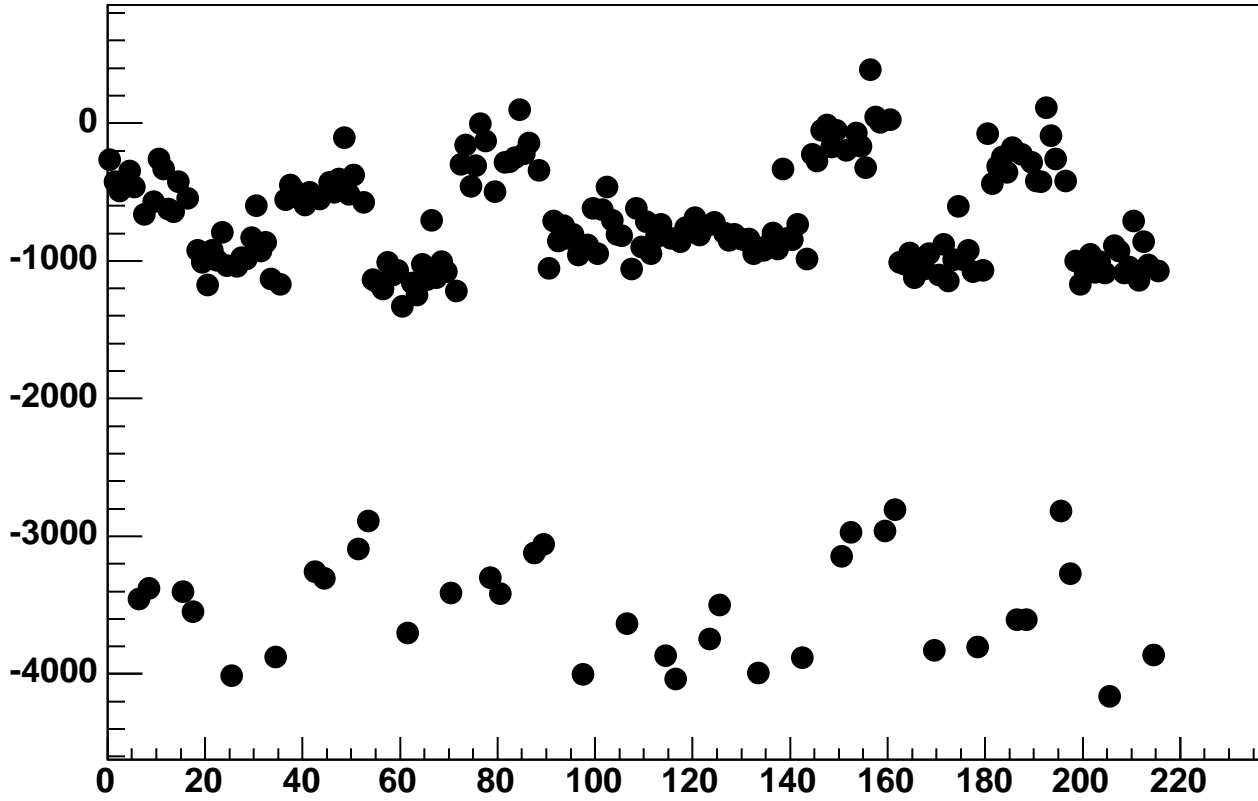
Enable 2, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan



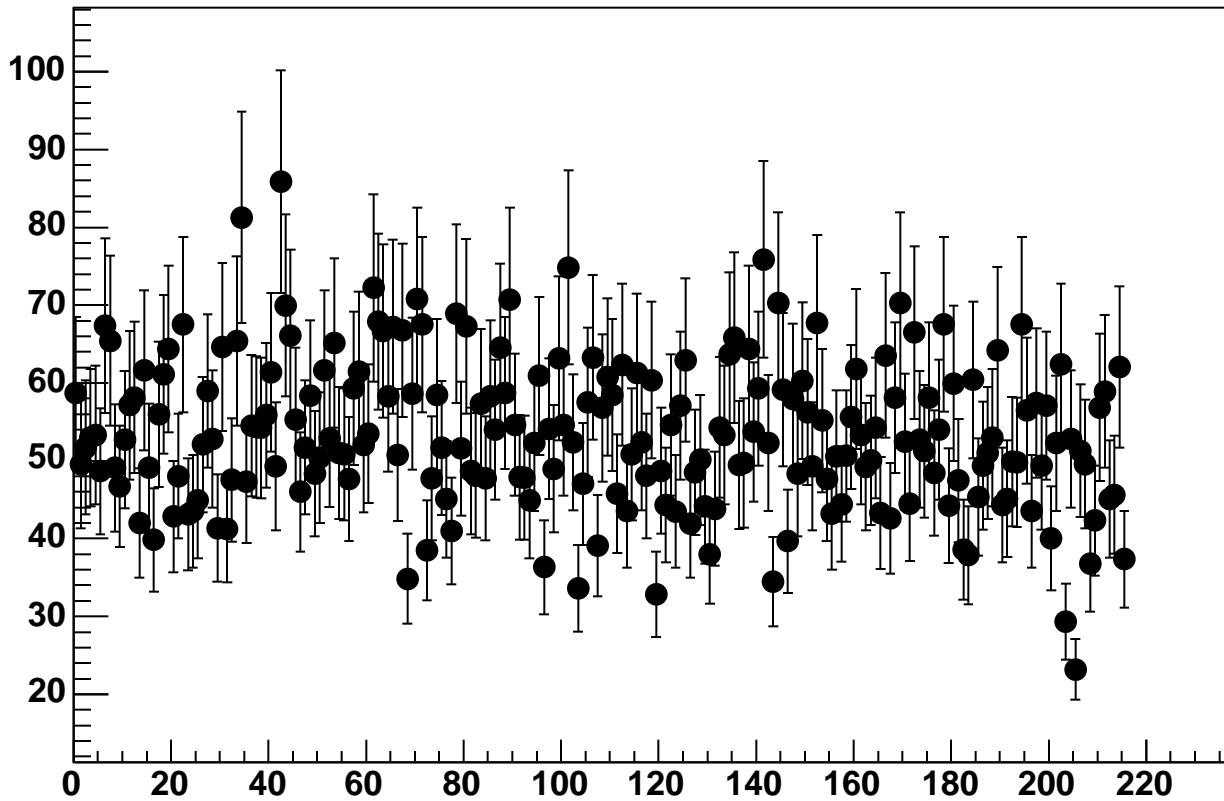
Enable 2, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan



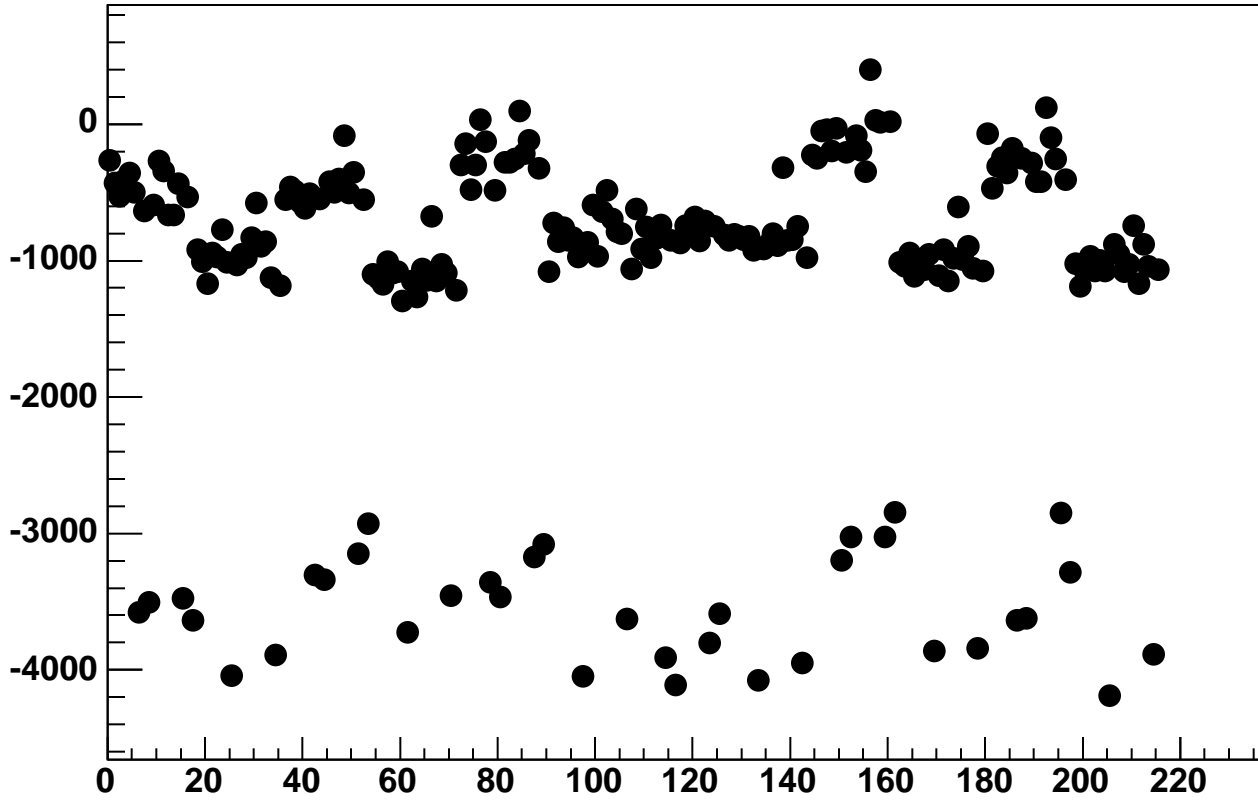
Enable 2, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



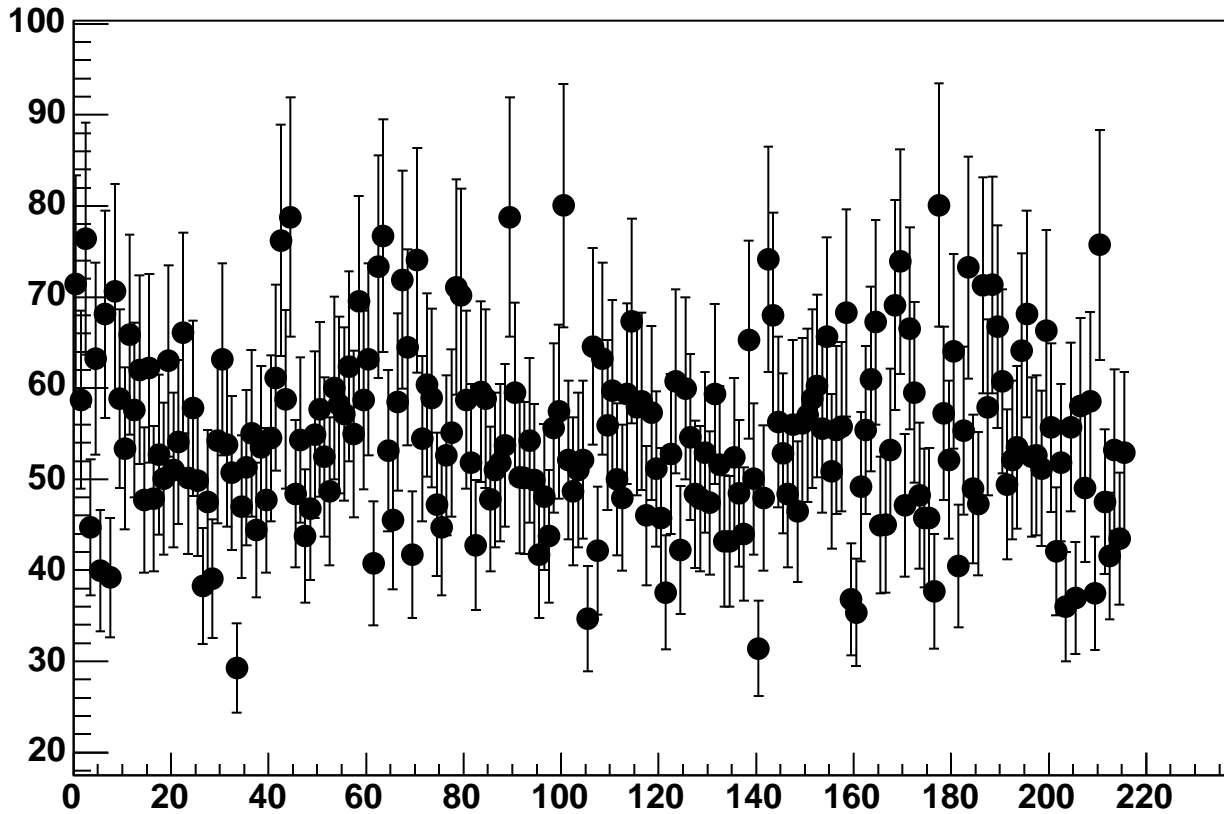
Enable 2, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



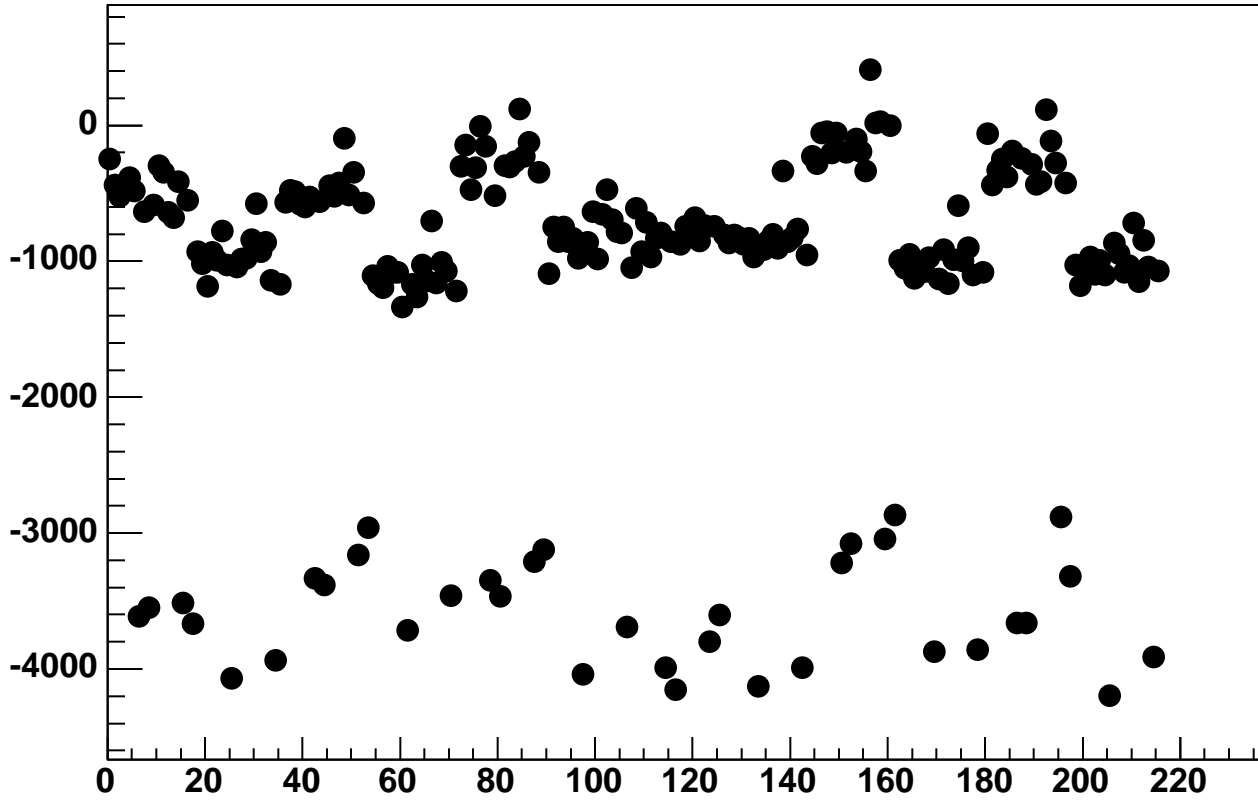
Enable 2, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan



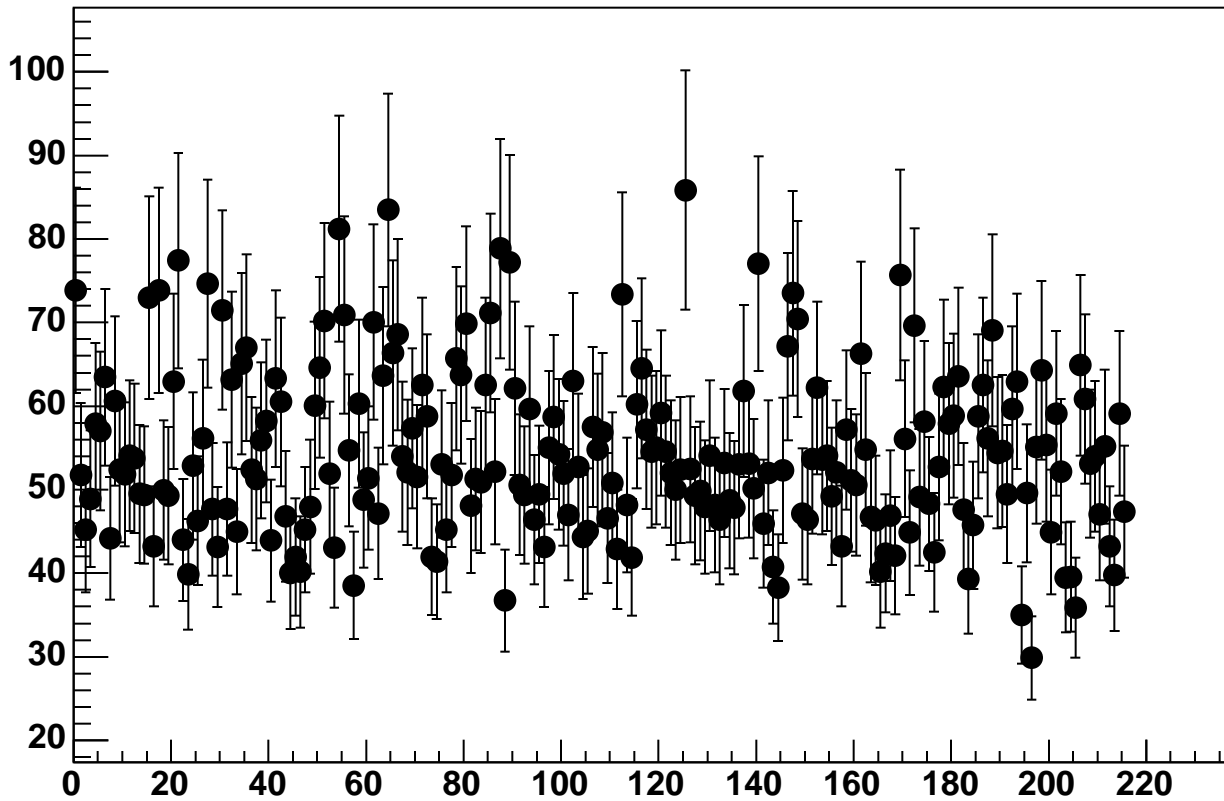
Enable 2, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan



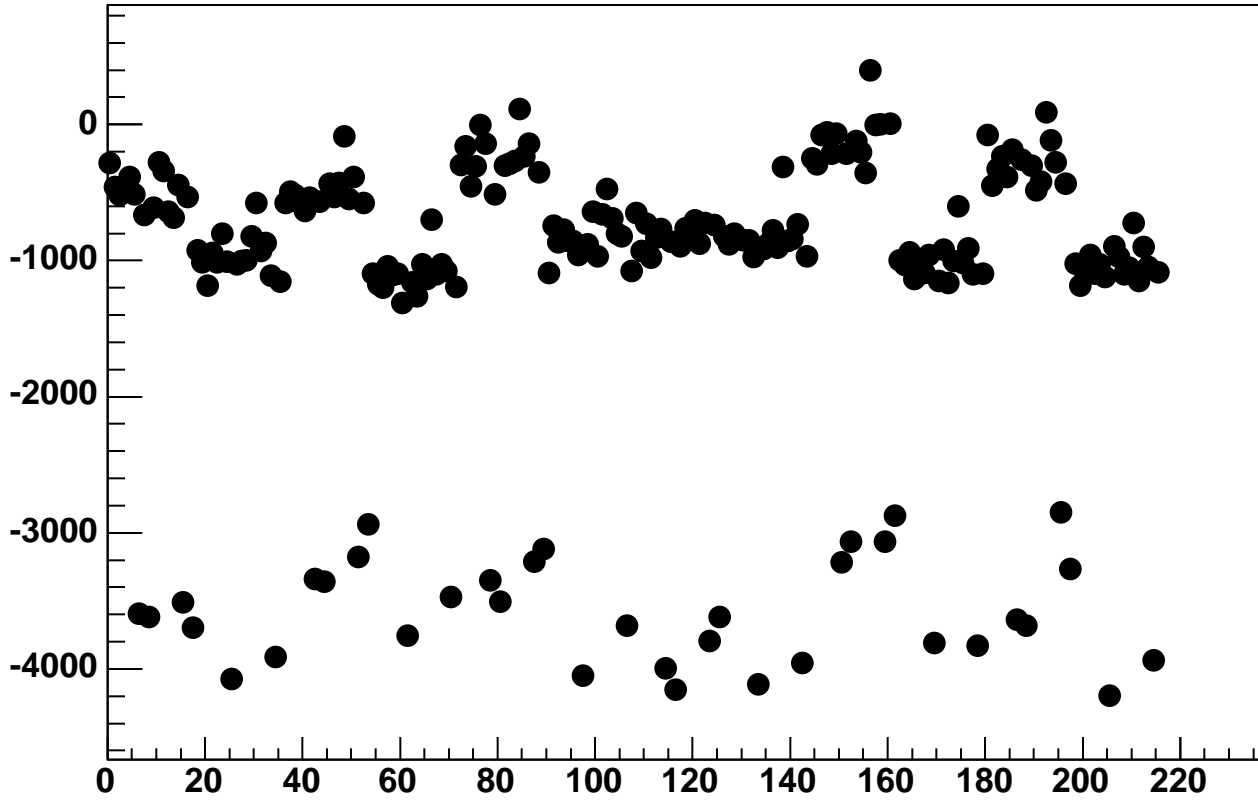
Enable 2, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



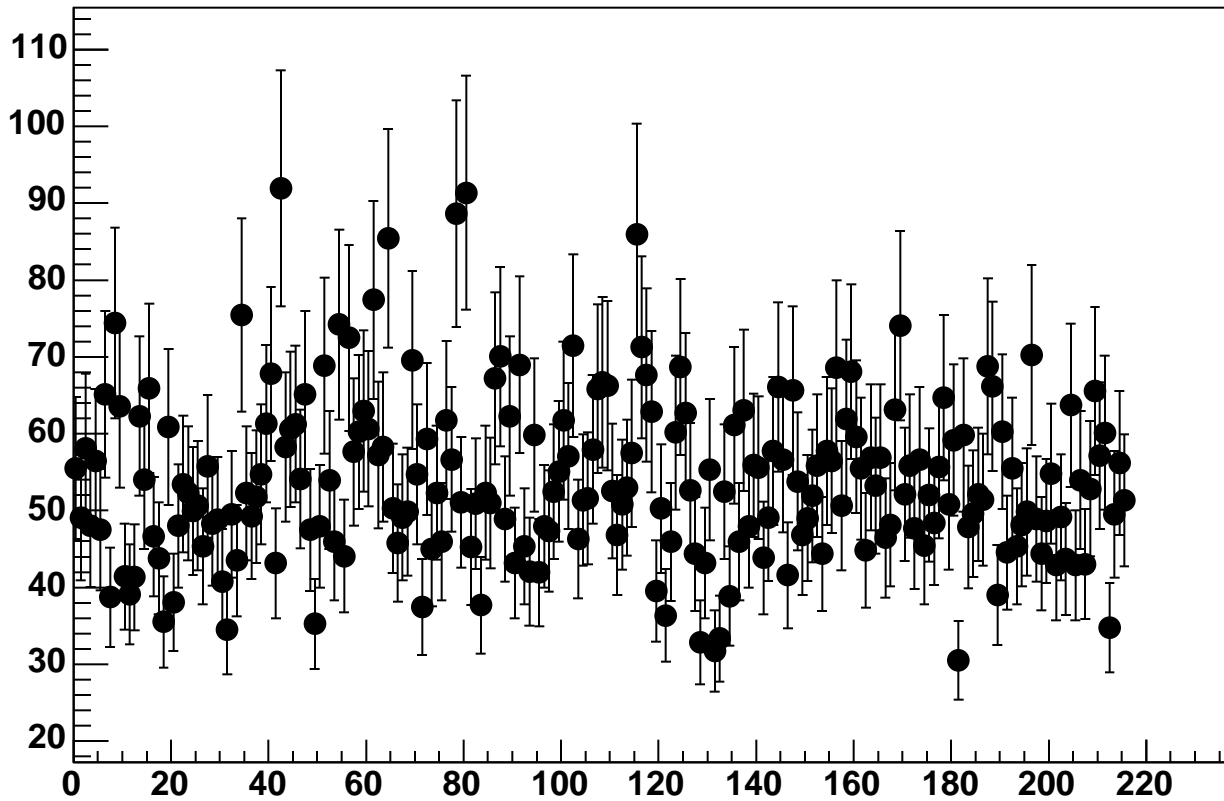
Enable 2, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



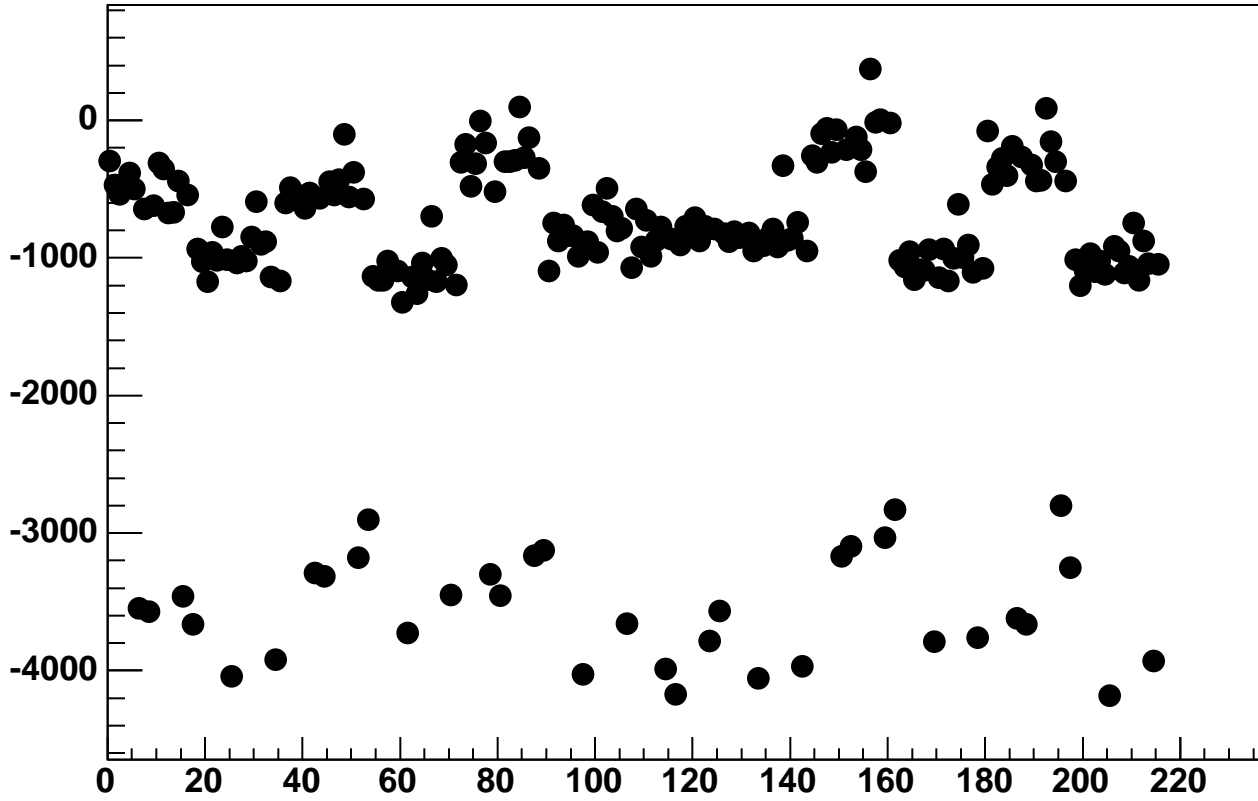
Enable 2, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan



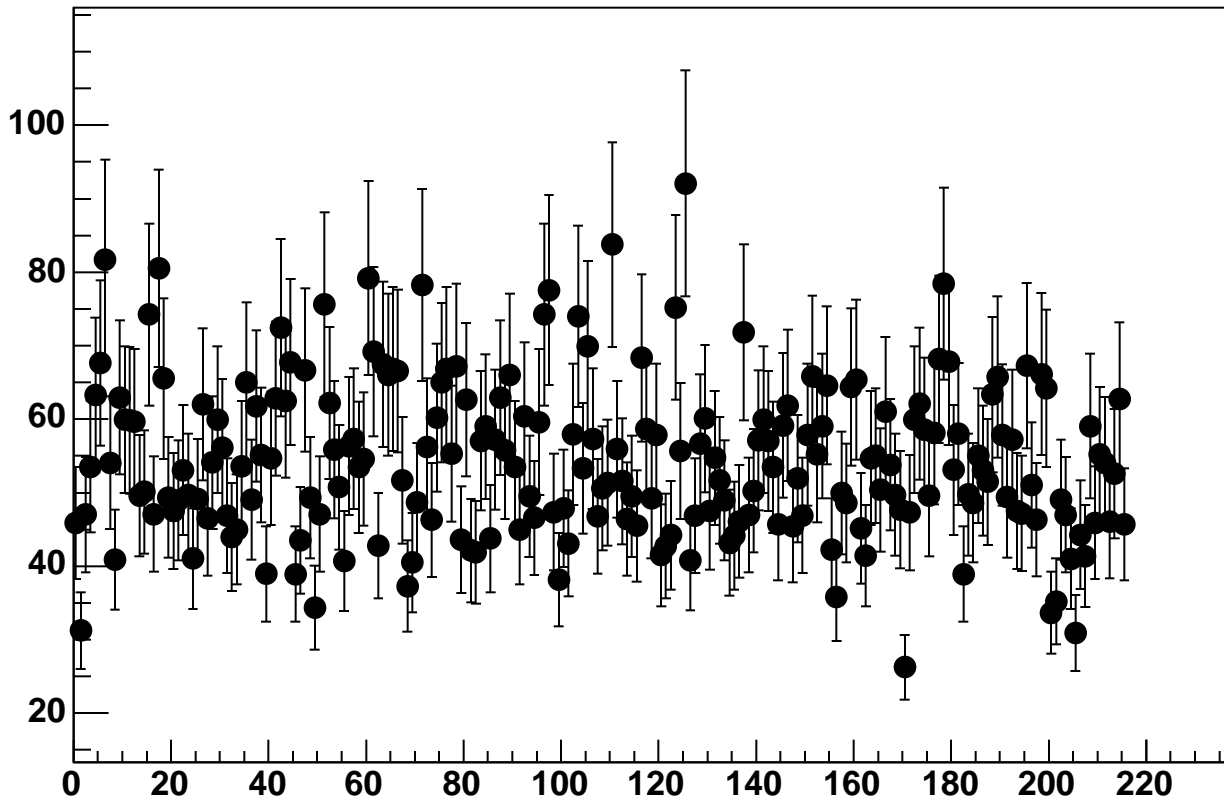
Enable 2, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan



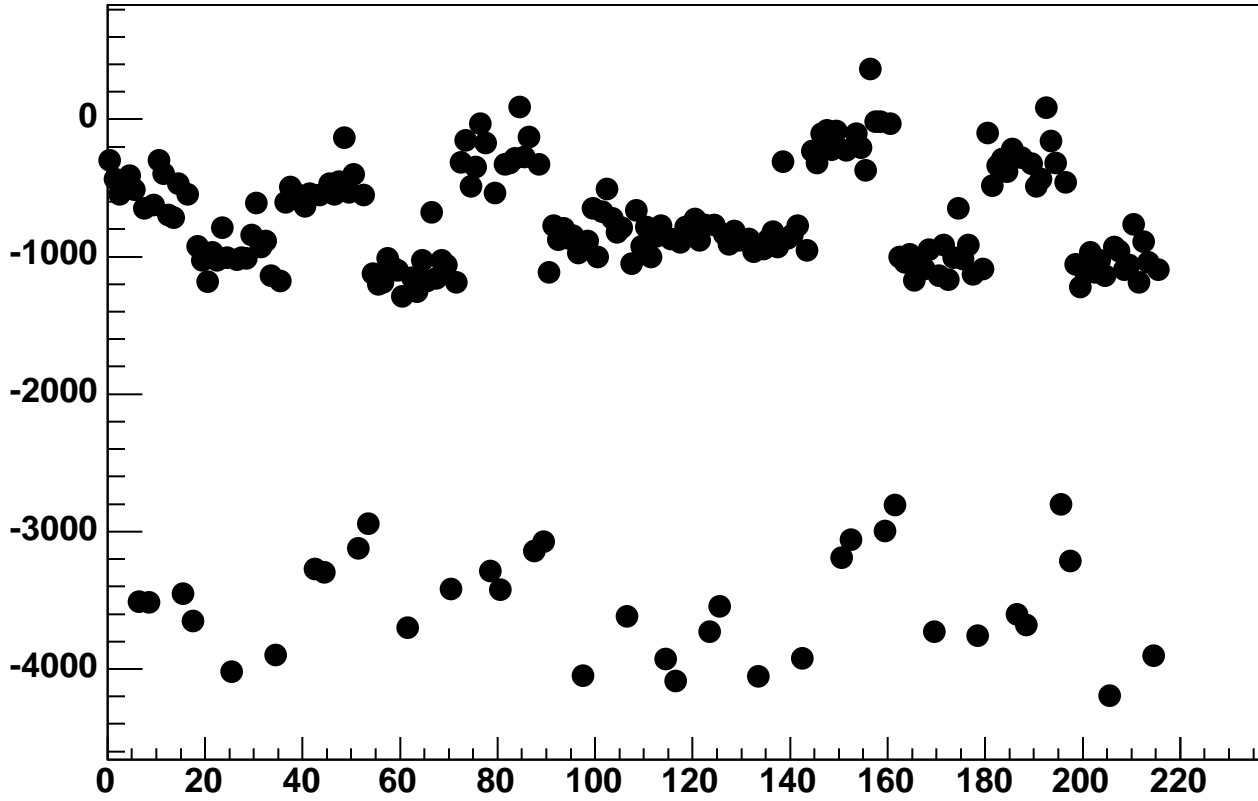
Enable 2, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



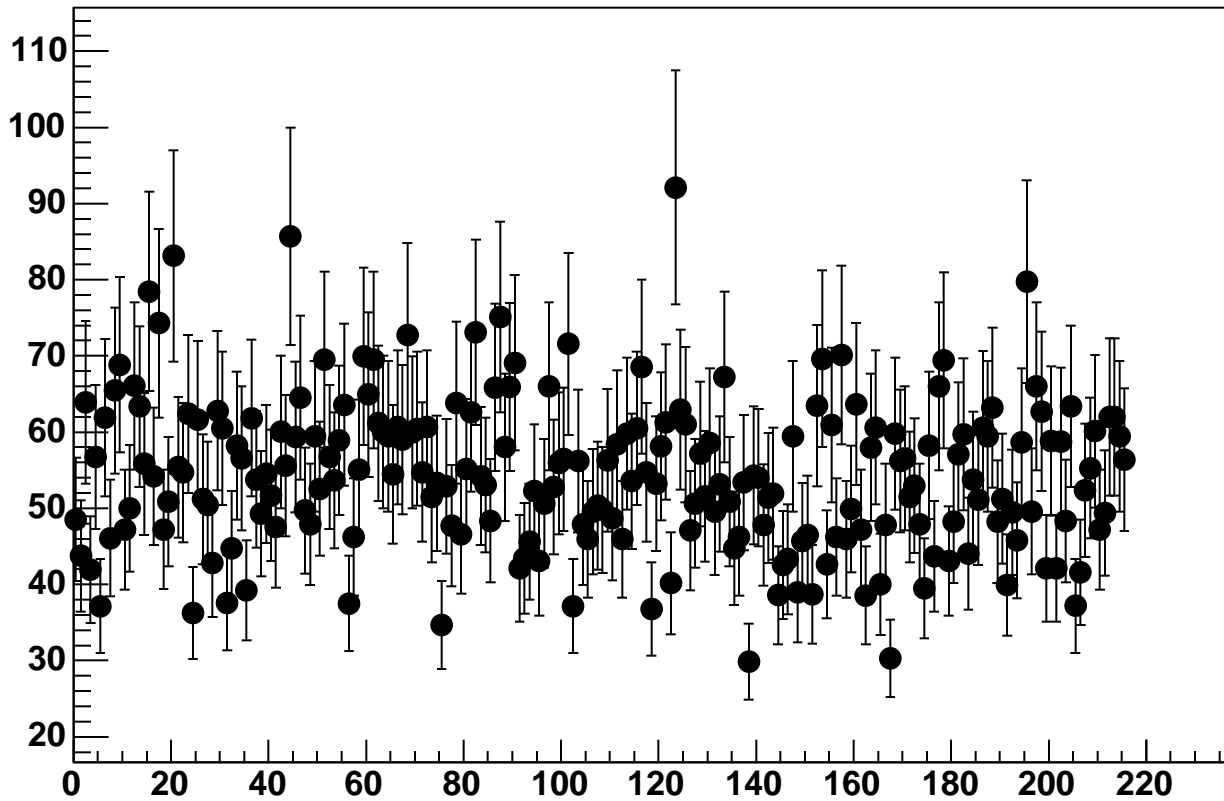
Enable 2, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



Enable 2, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan

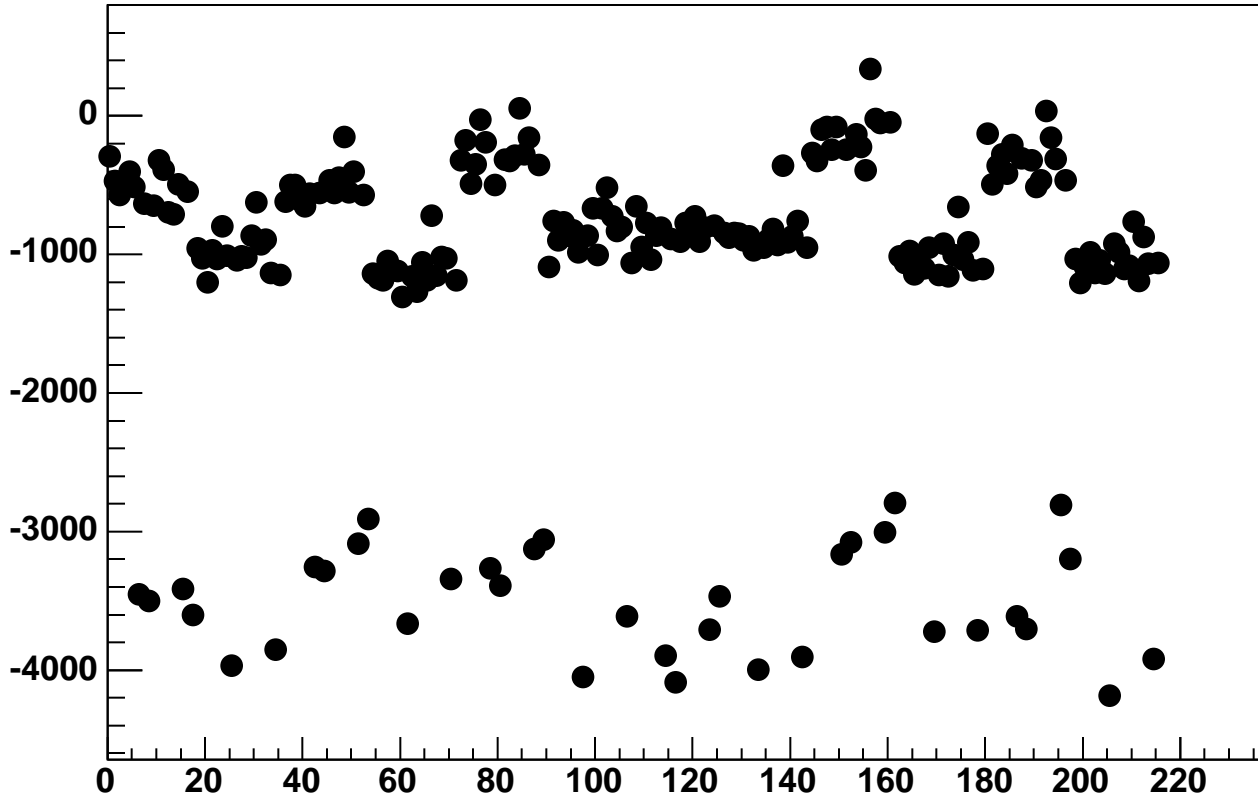


Enable 2, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan

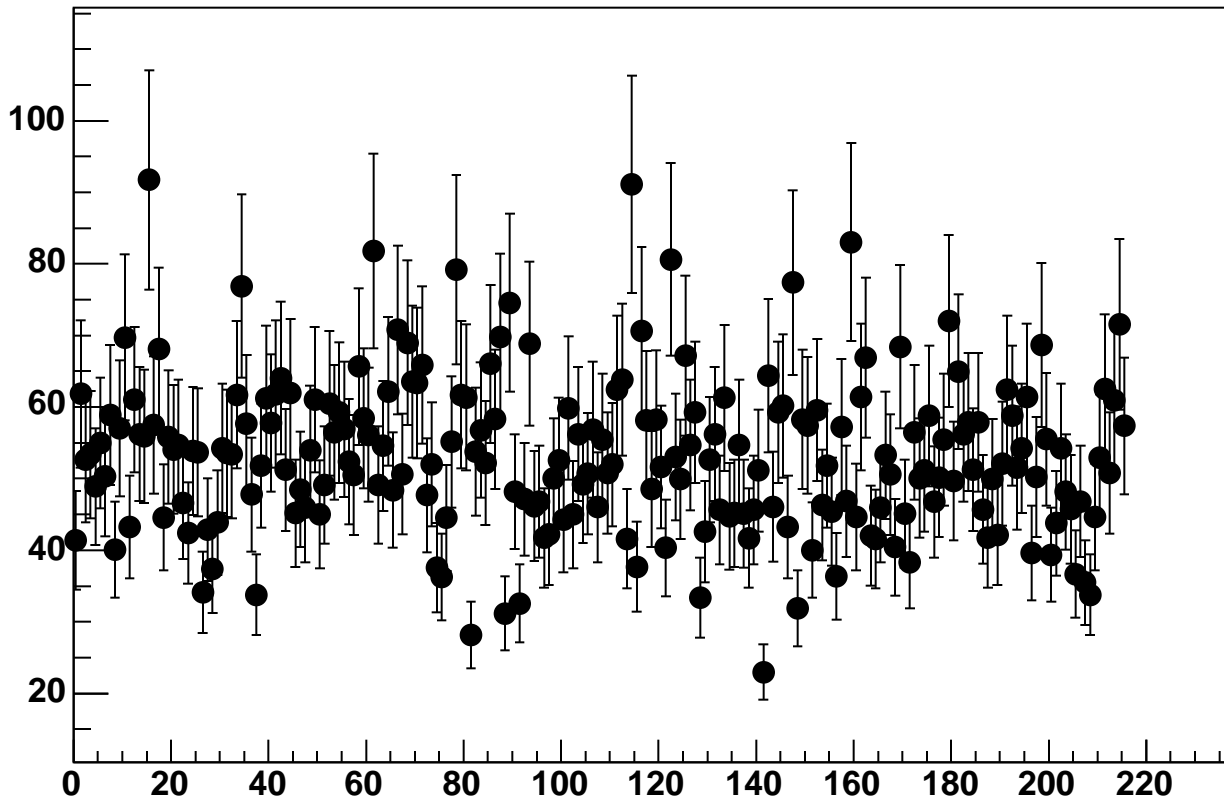




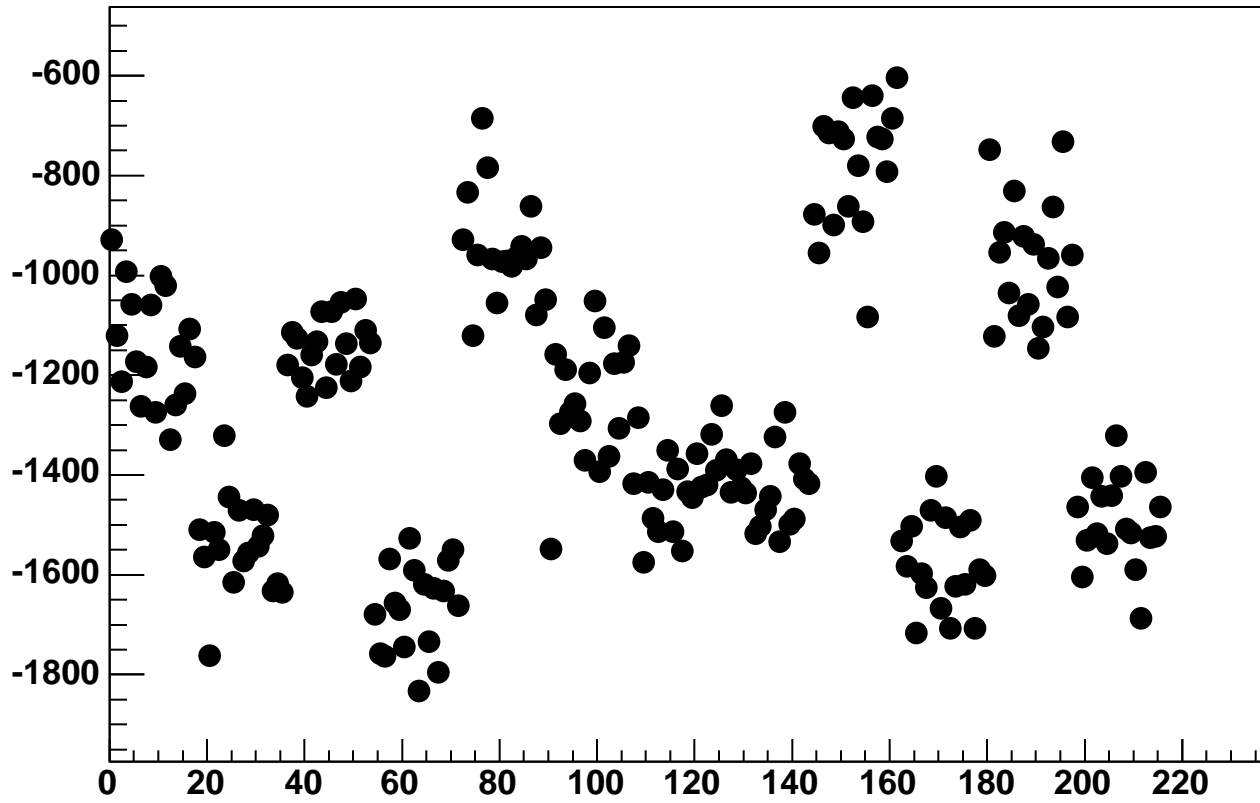
Enable 2, DAC=1600, Hold=245, ADC Mean vs 18\*Chip+Chan



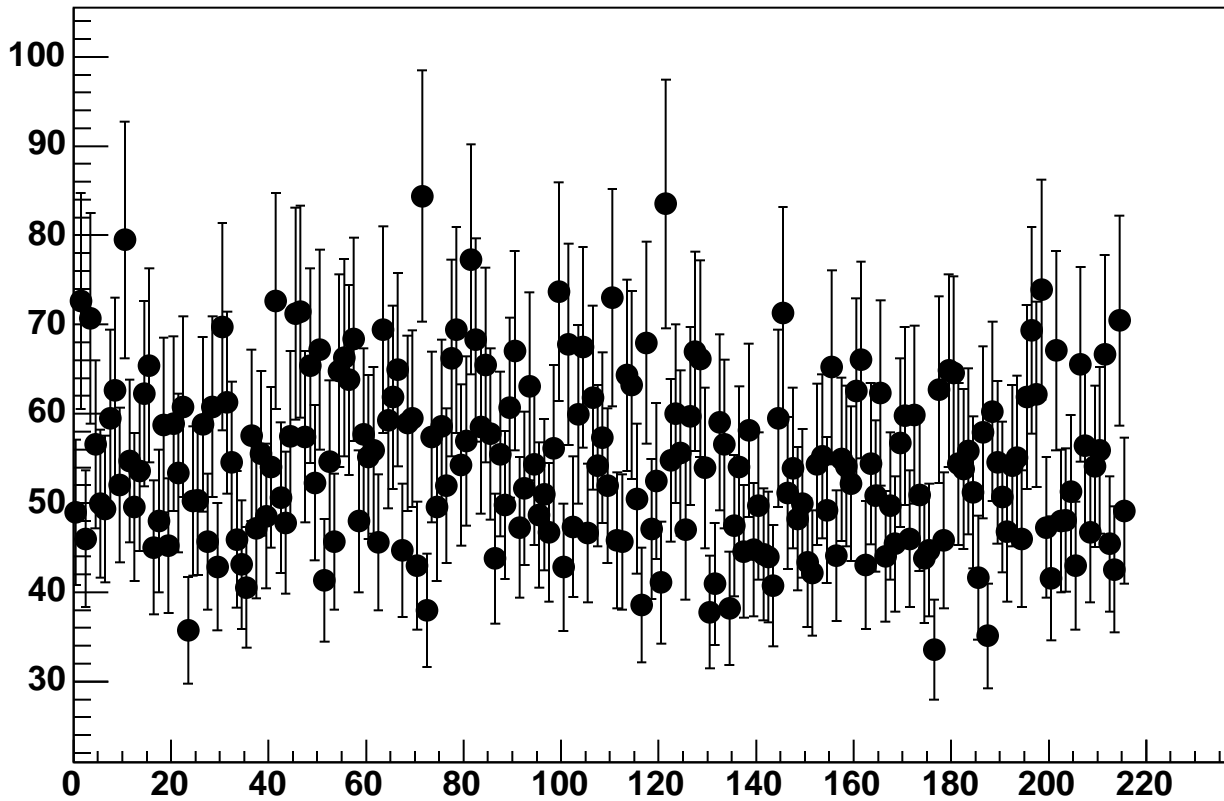
Enable 2, DAC=1600, Hold=245, ADC Noise vs 18\*Chip+Chan



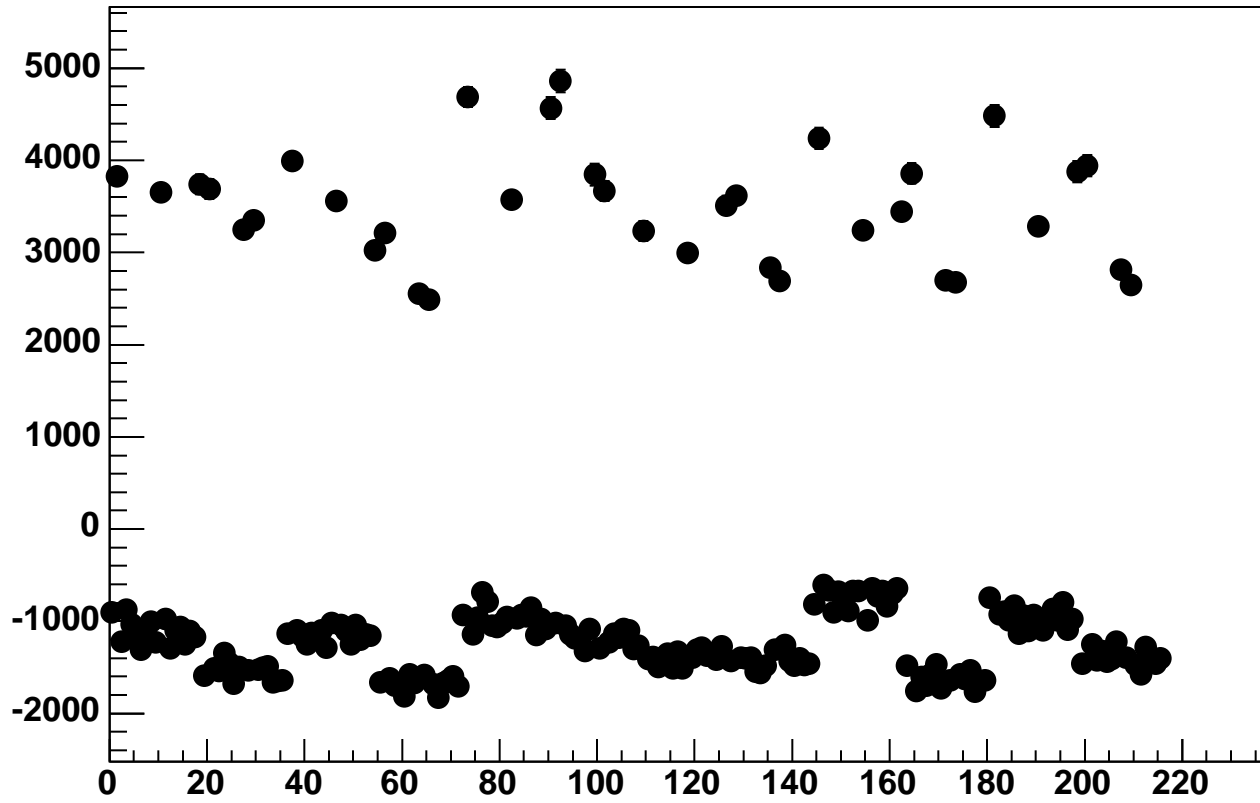
Enable 3, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan



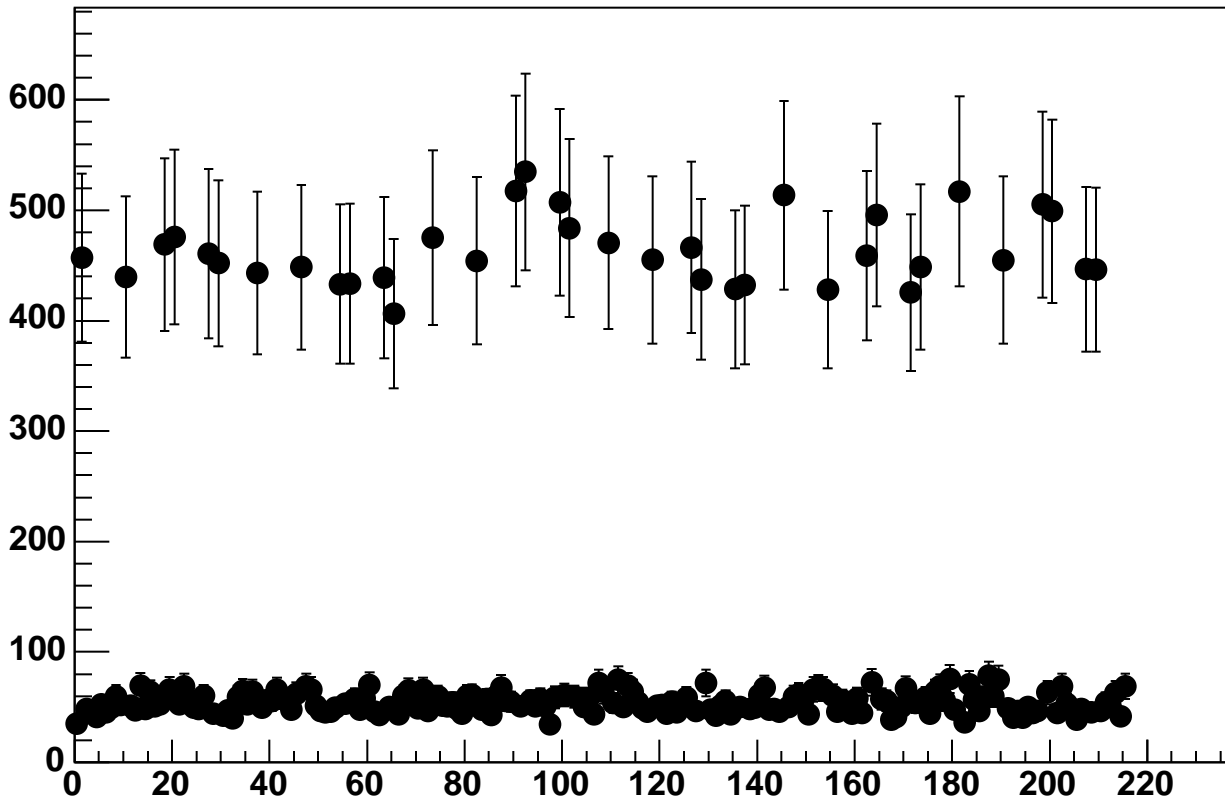
Enable 3, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan



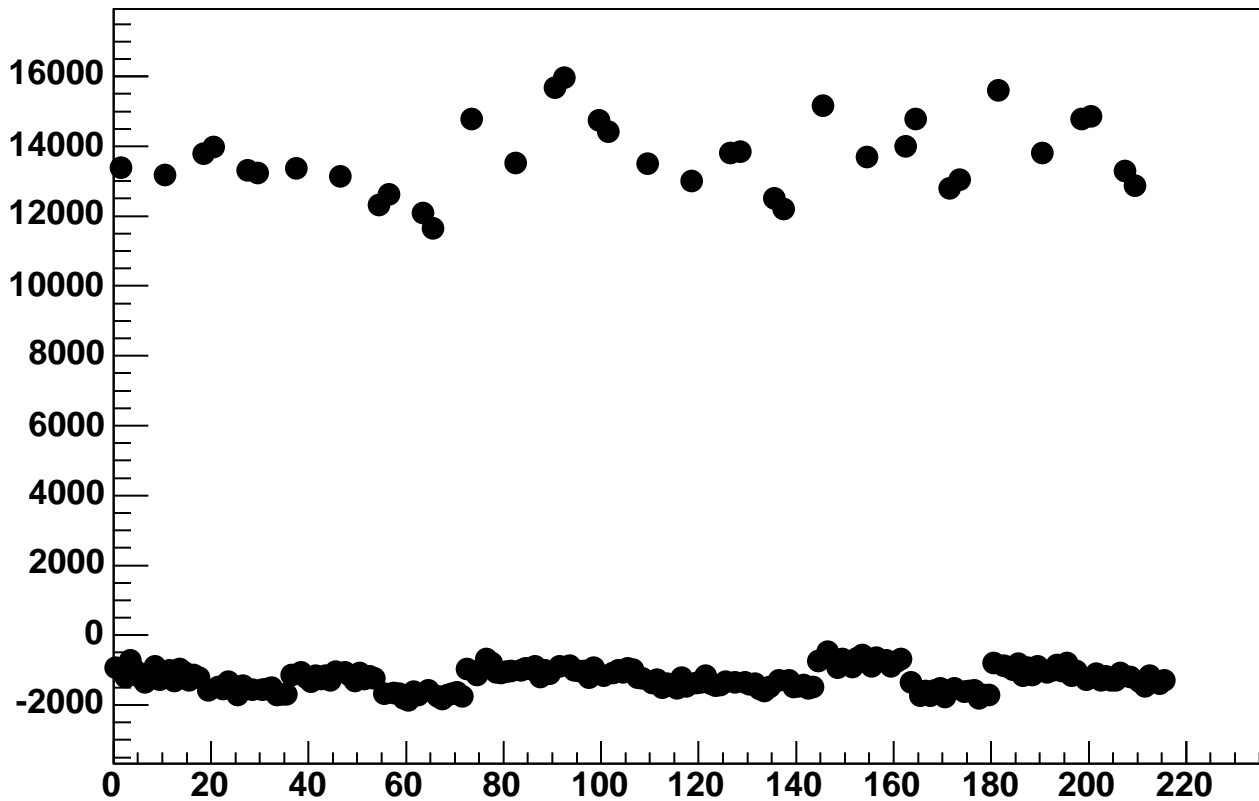
Enable 3, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



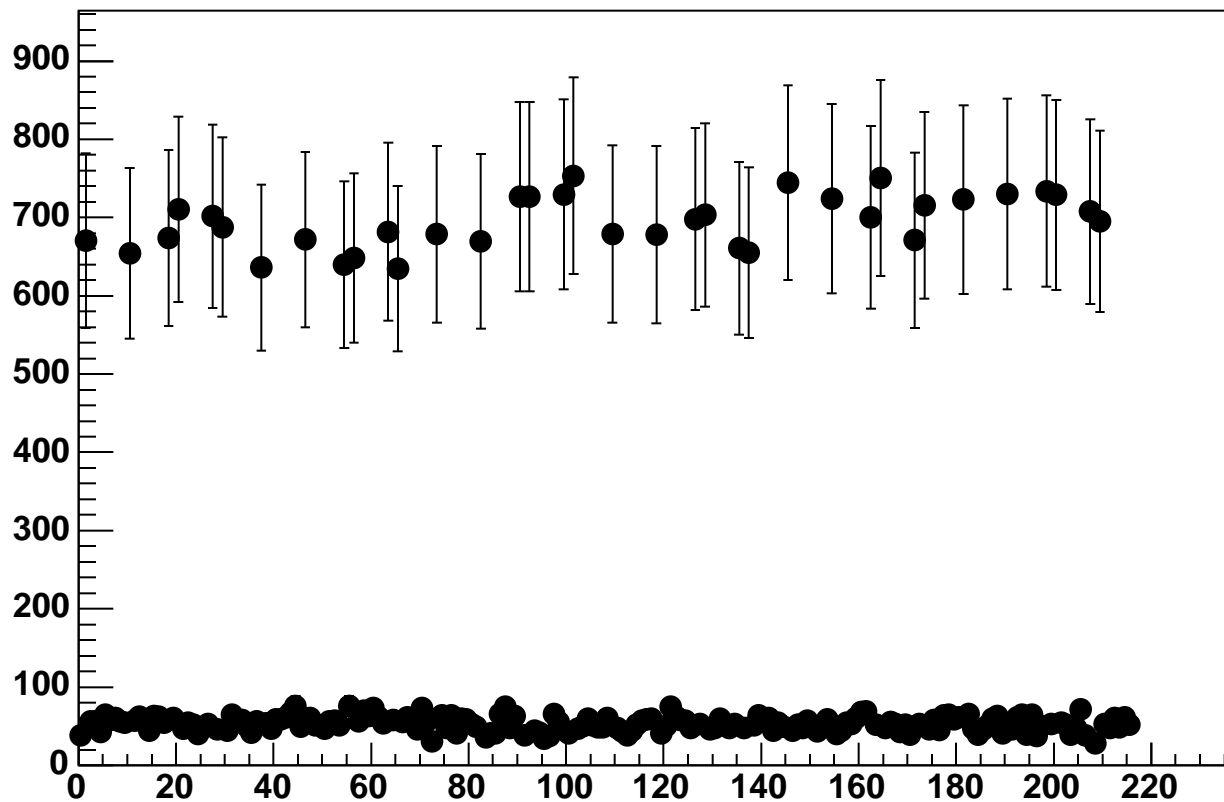
Enable 3, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



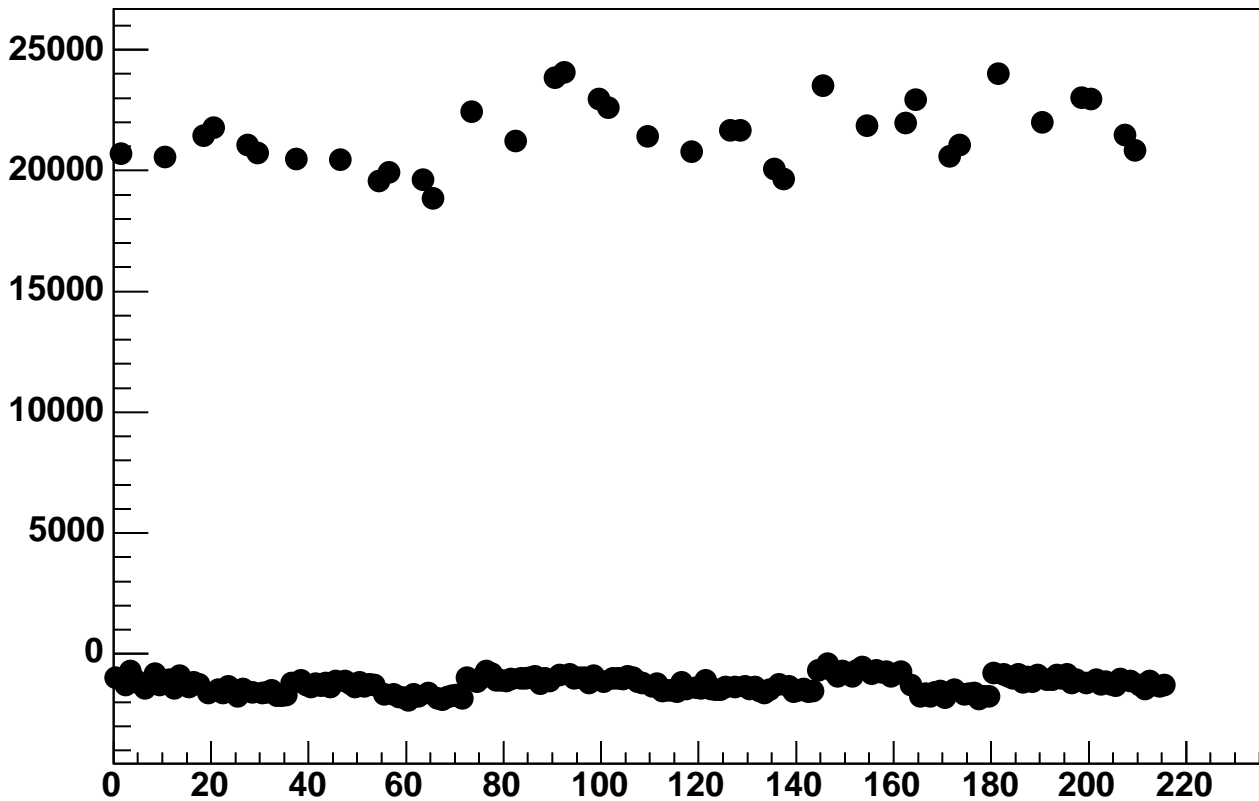
Enable 3, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan



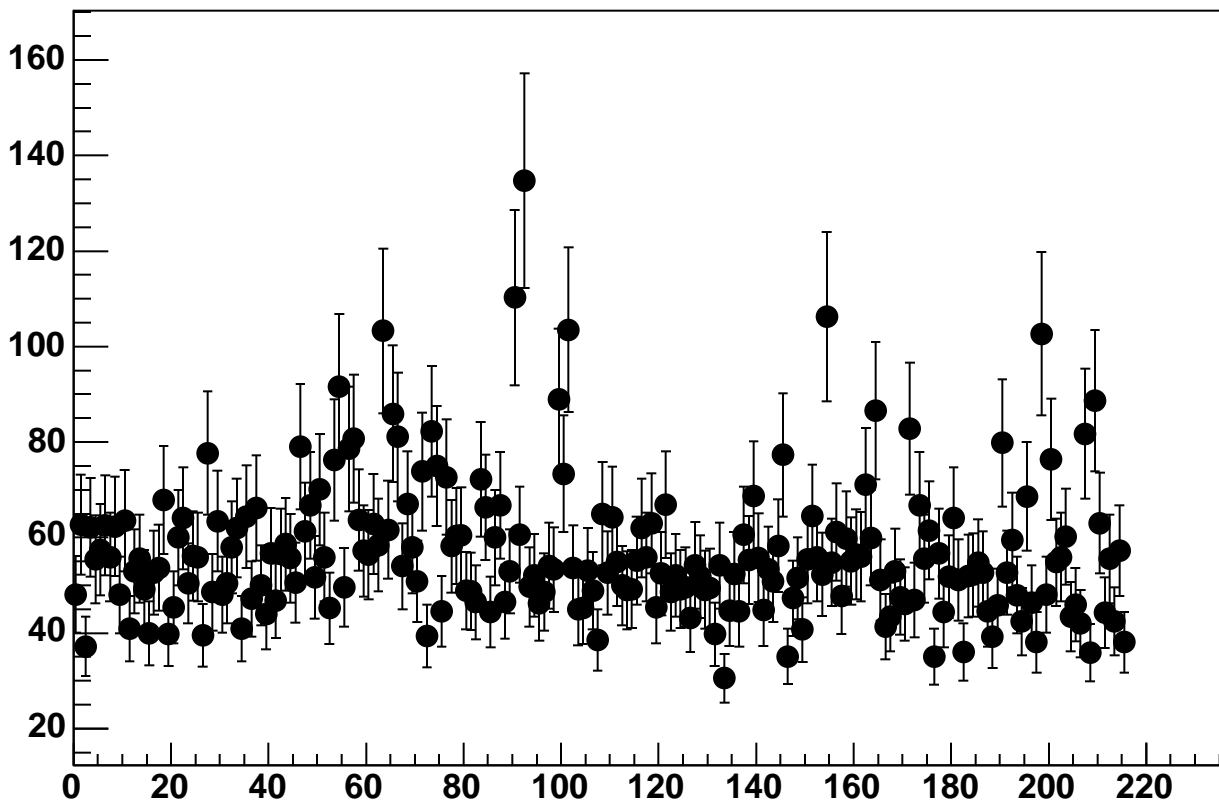
Enable 3, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan



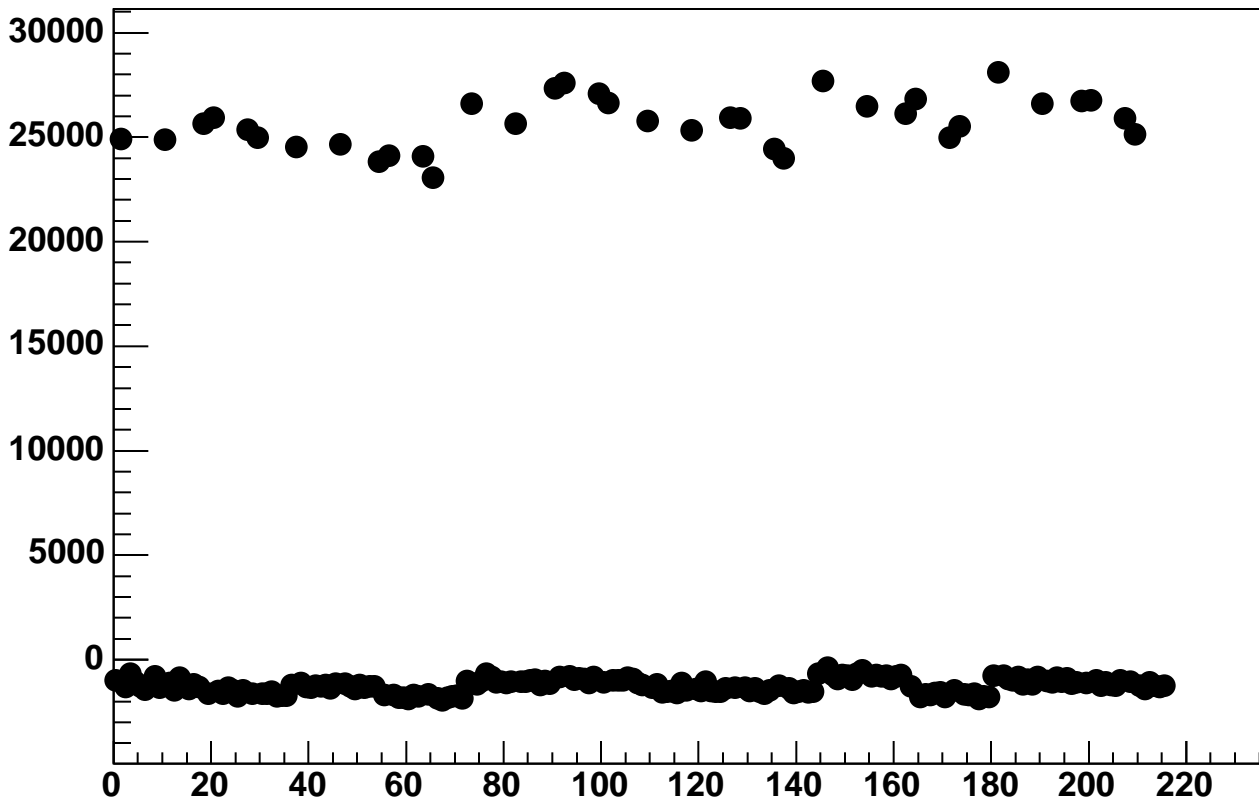
Enable 3, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



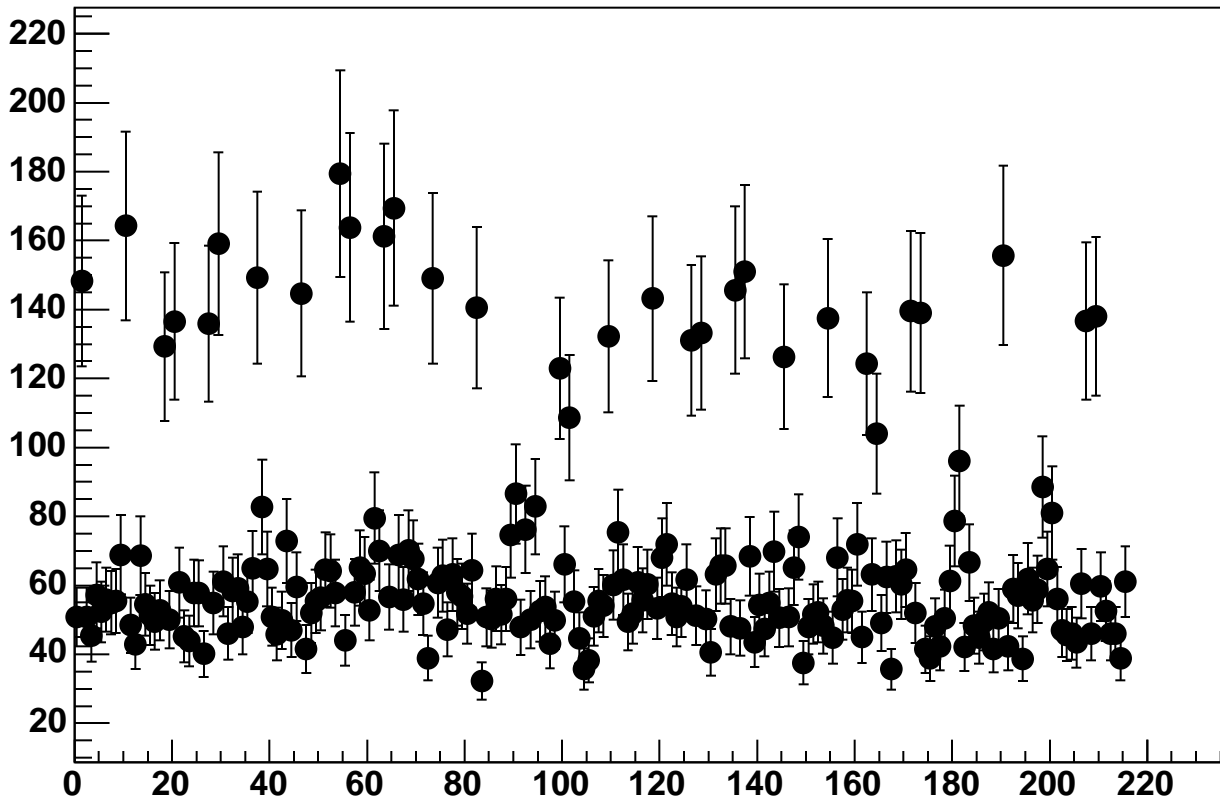
Enable 3, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



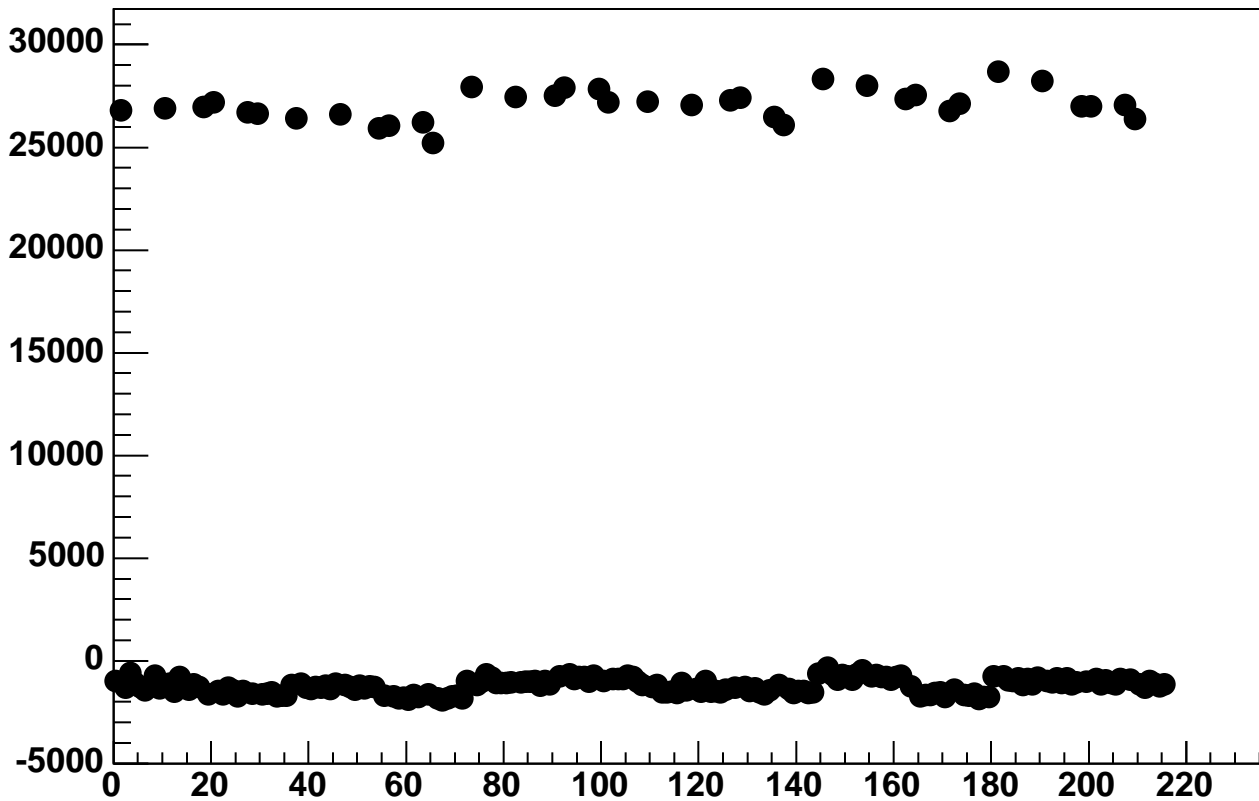
Enable 3, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan



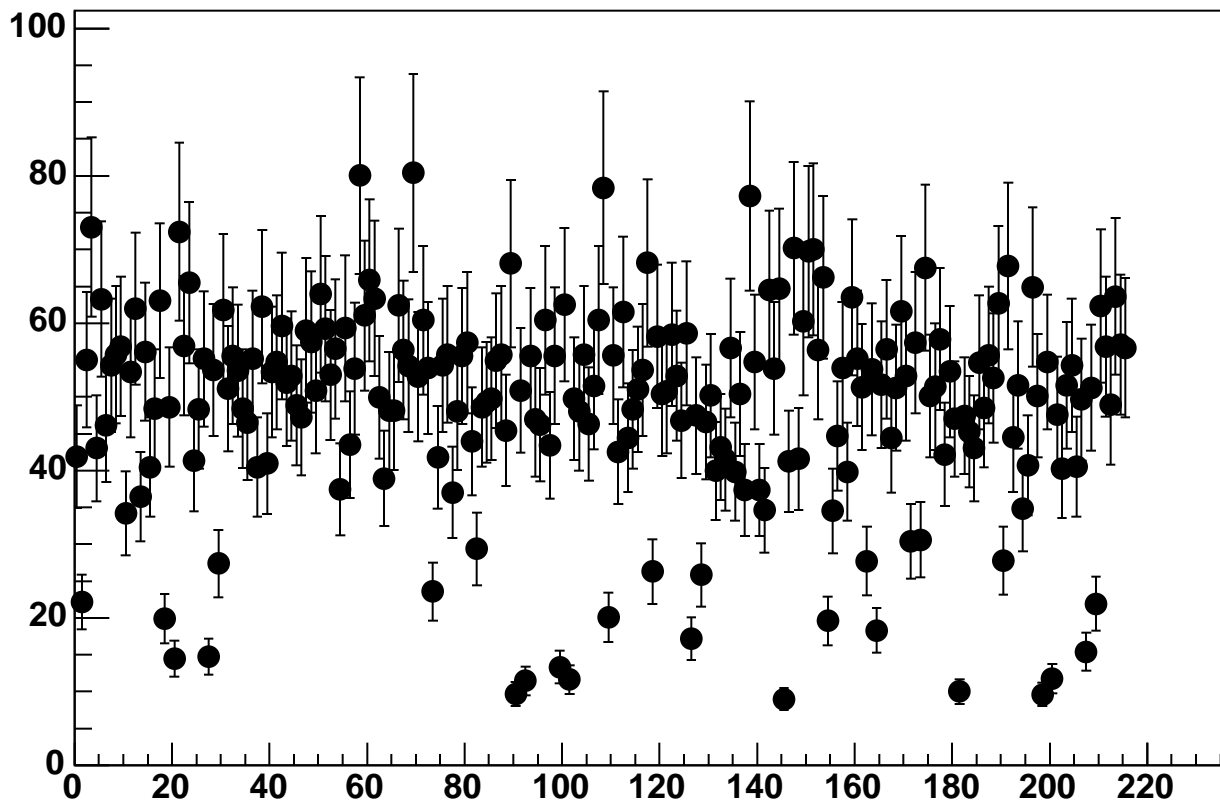
Enable 3, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan



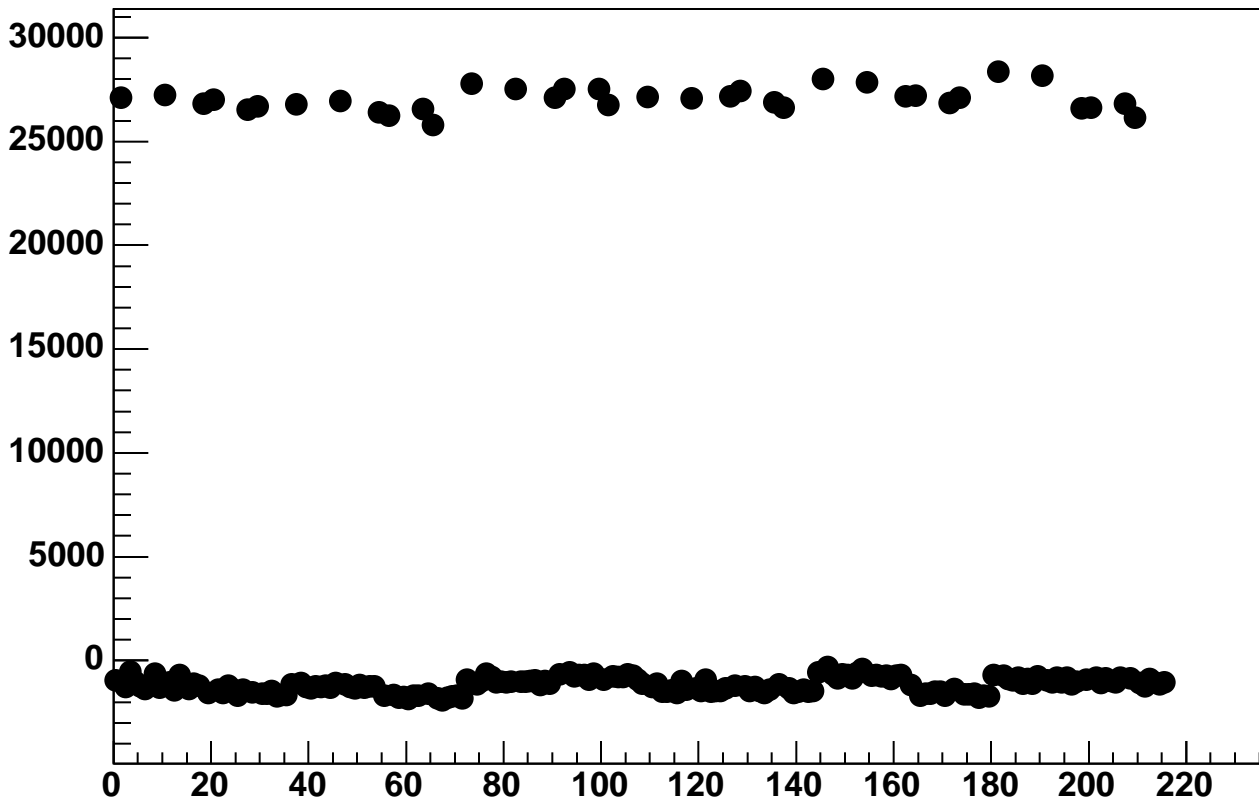
Enable 3, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



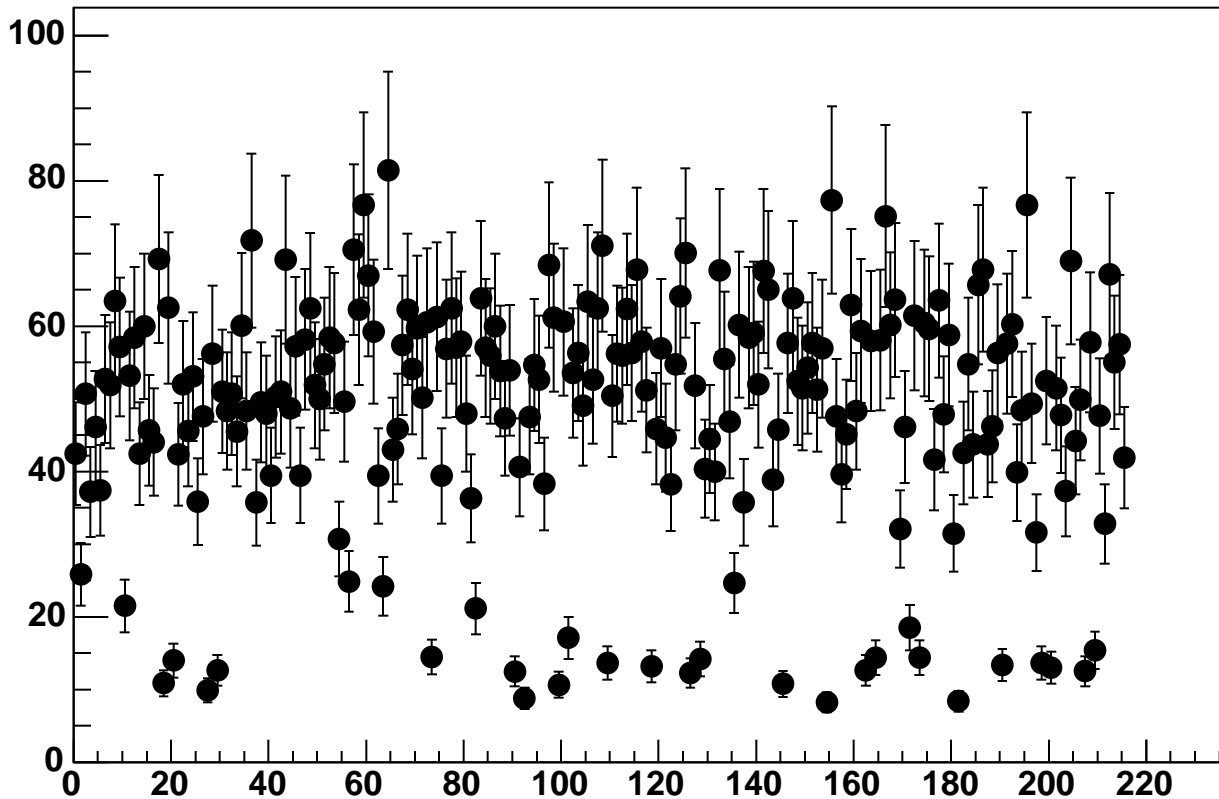
Enable 3, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan

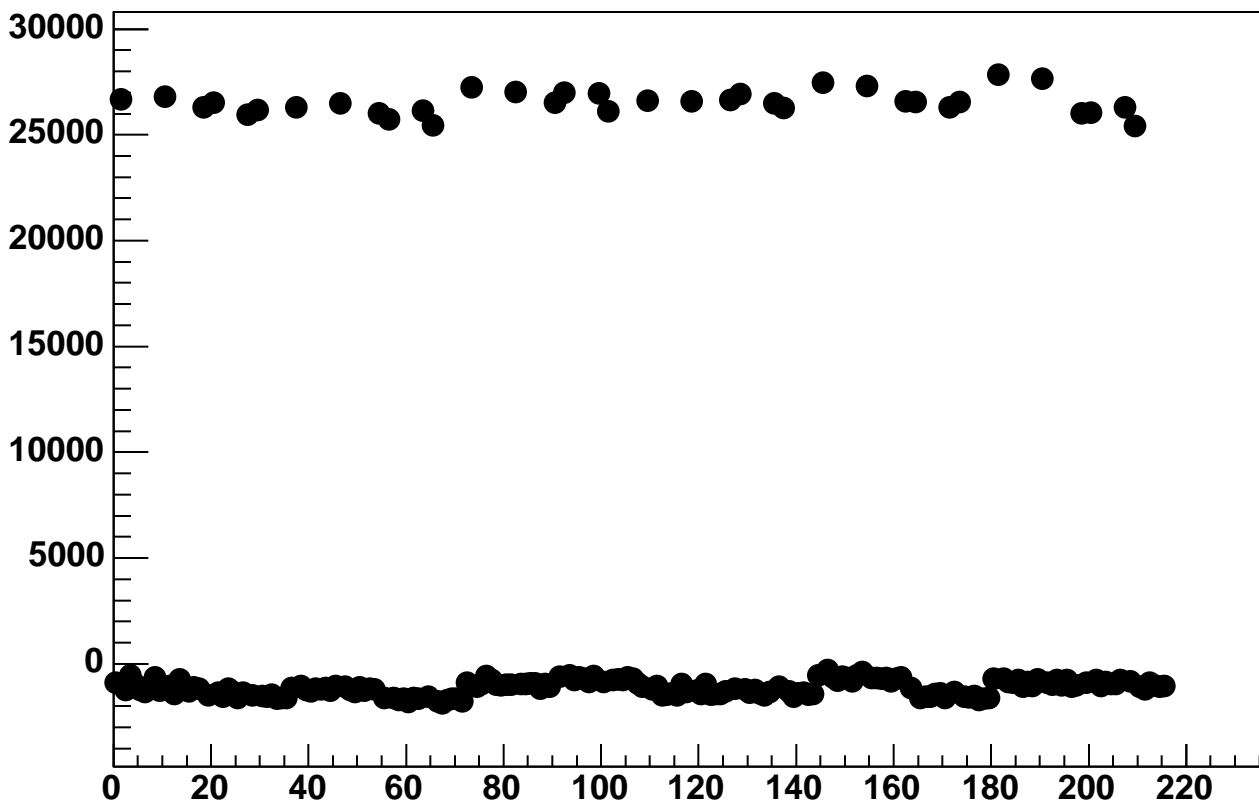


Enable 3, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan

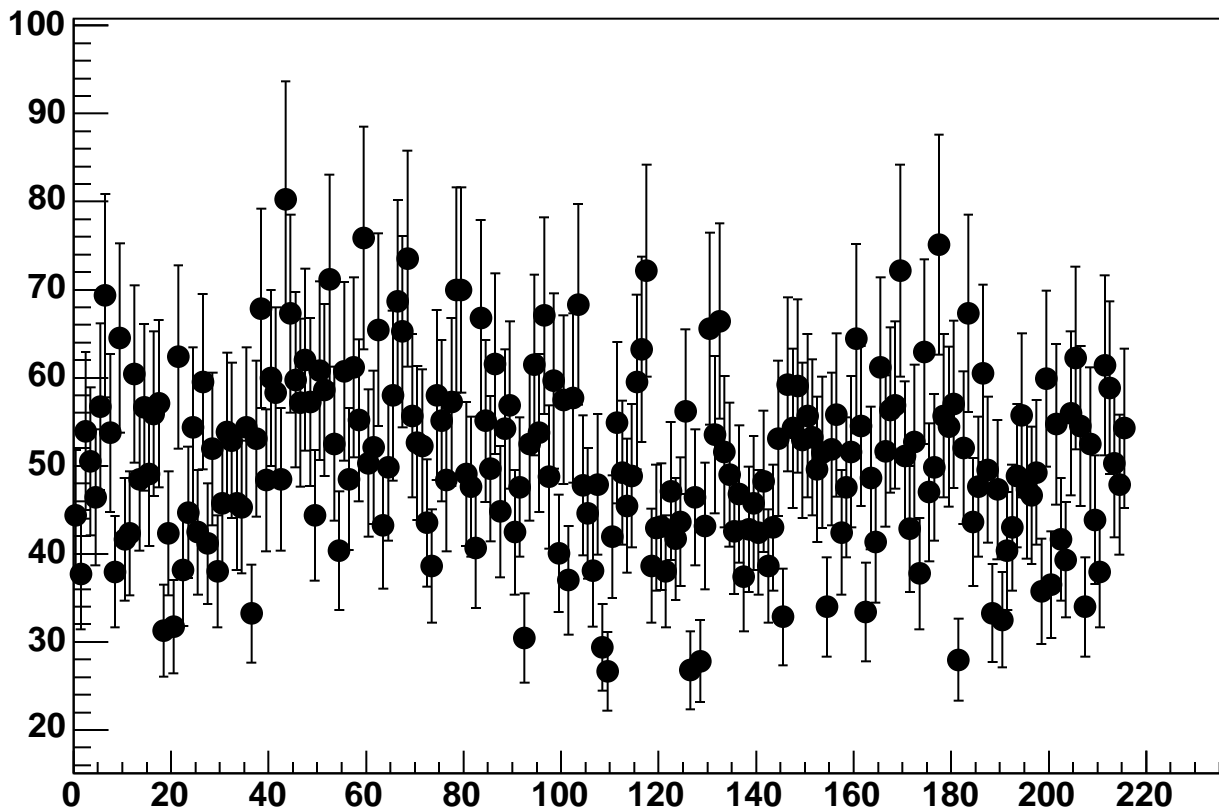




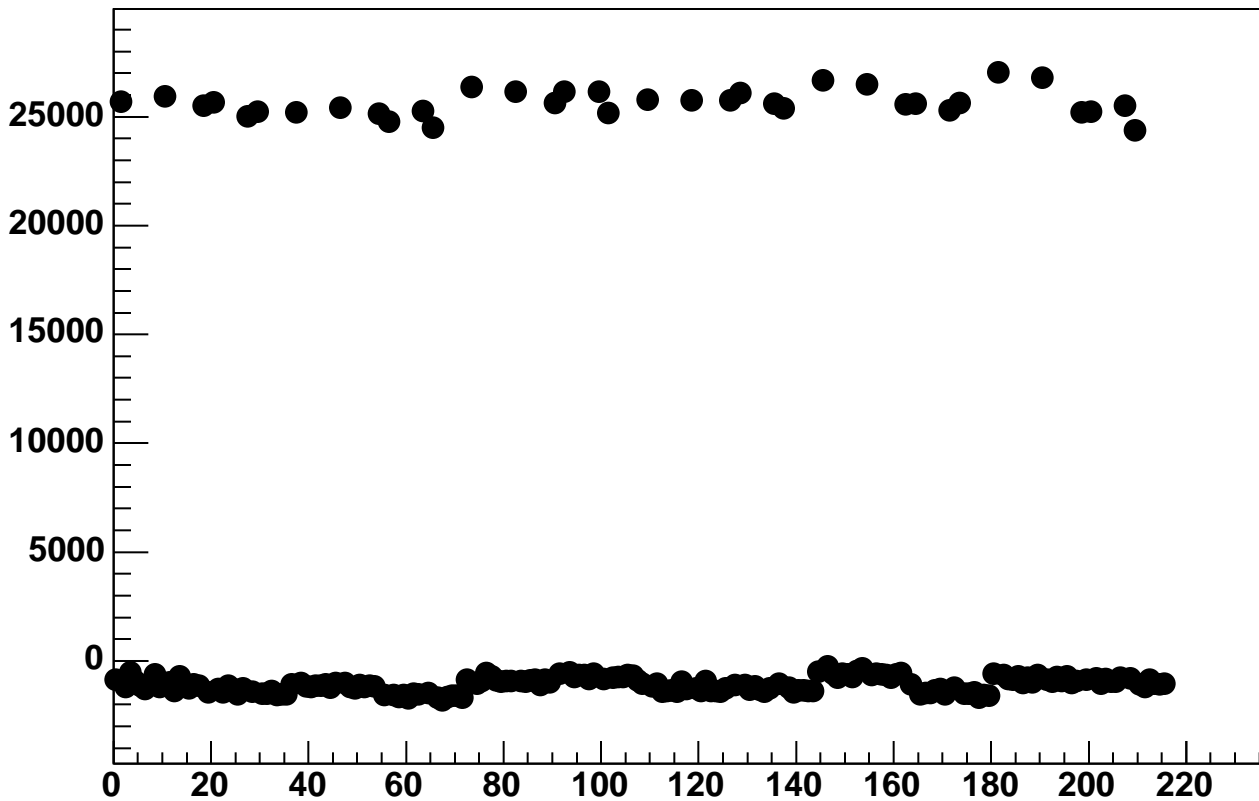
Enable 3, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



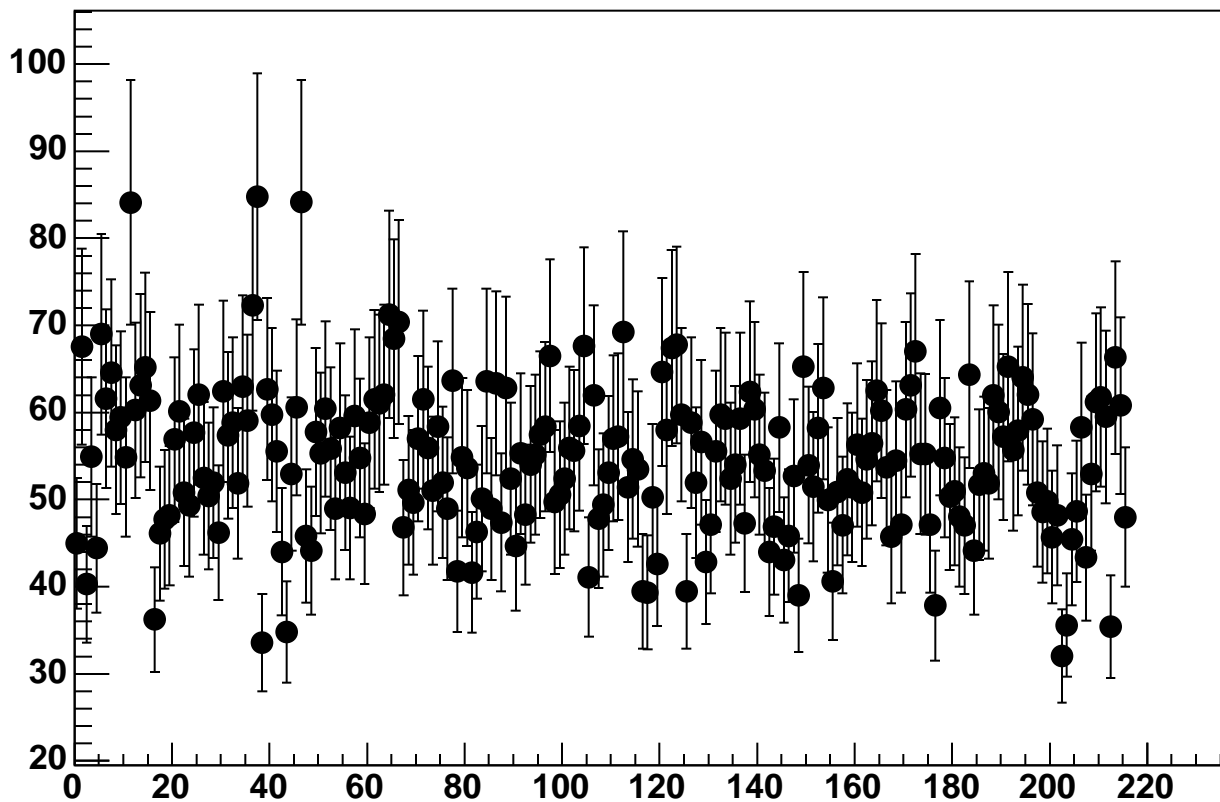
Enable 3, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



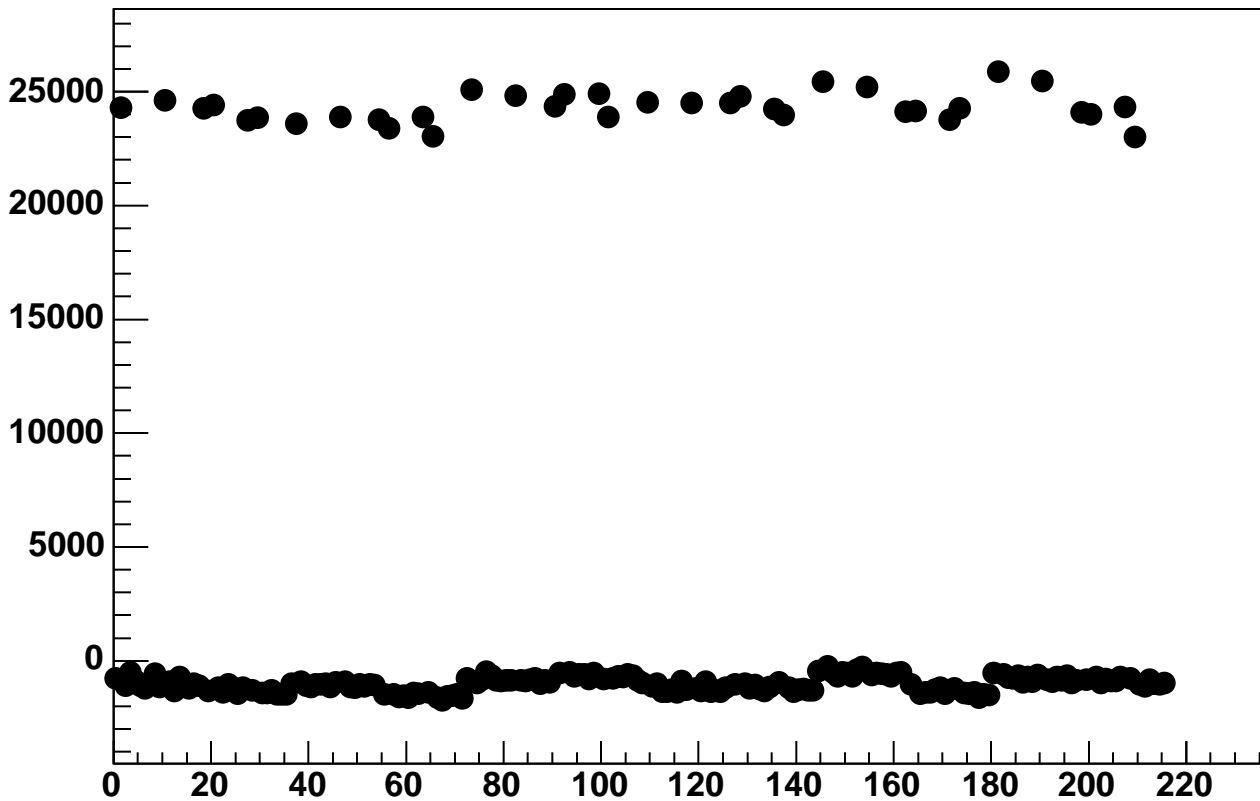
Enable 3, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan



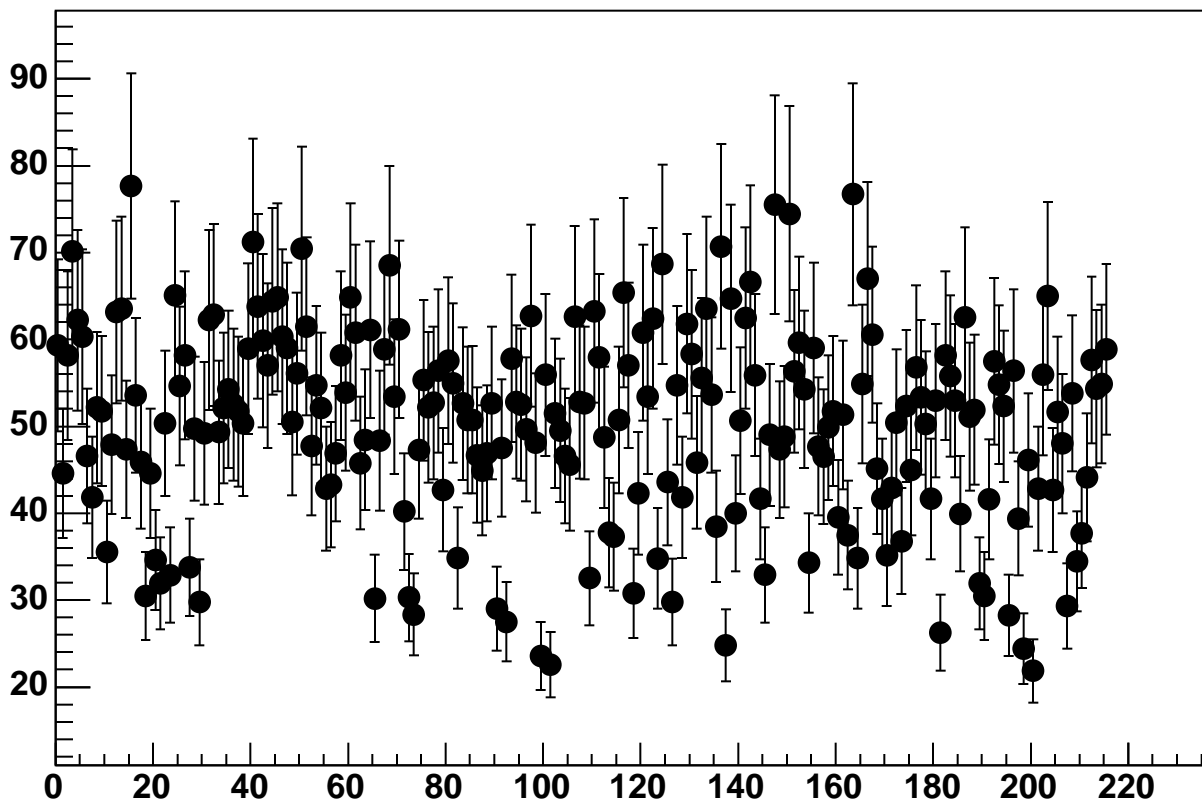
Enable 3, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan



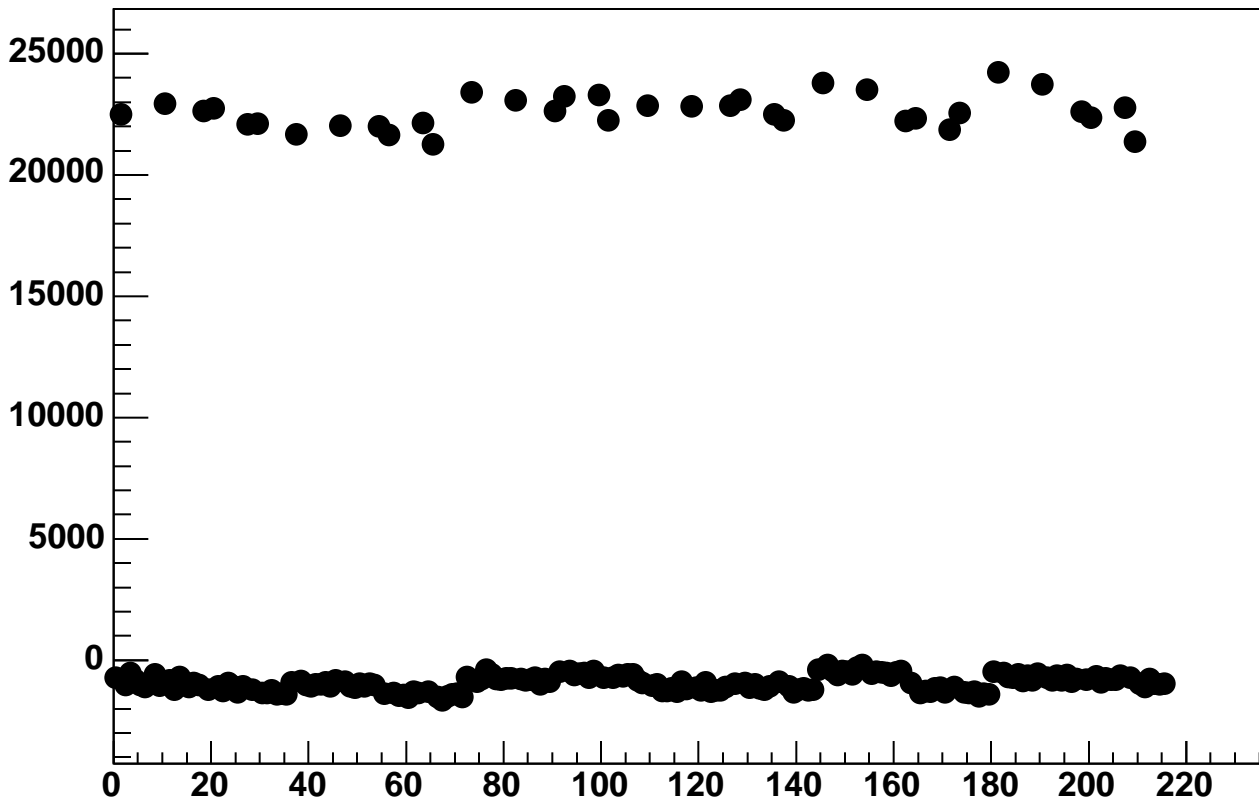
Enable 3, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



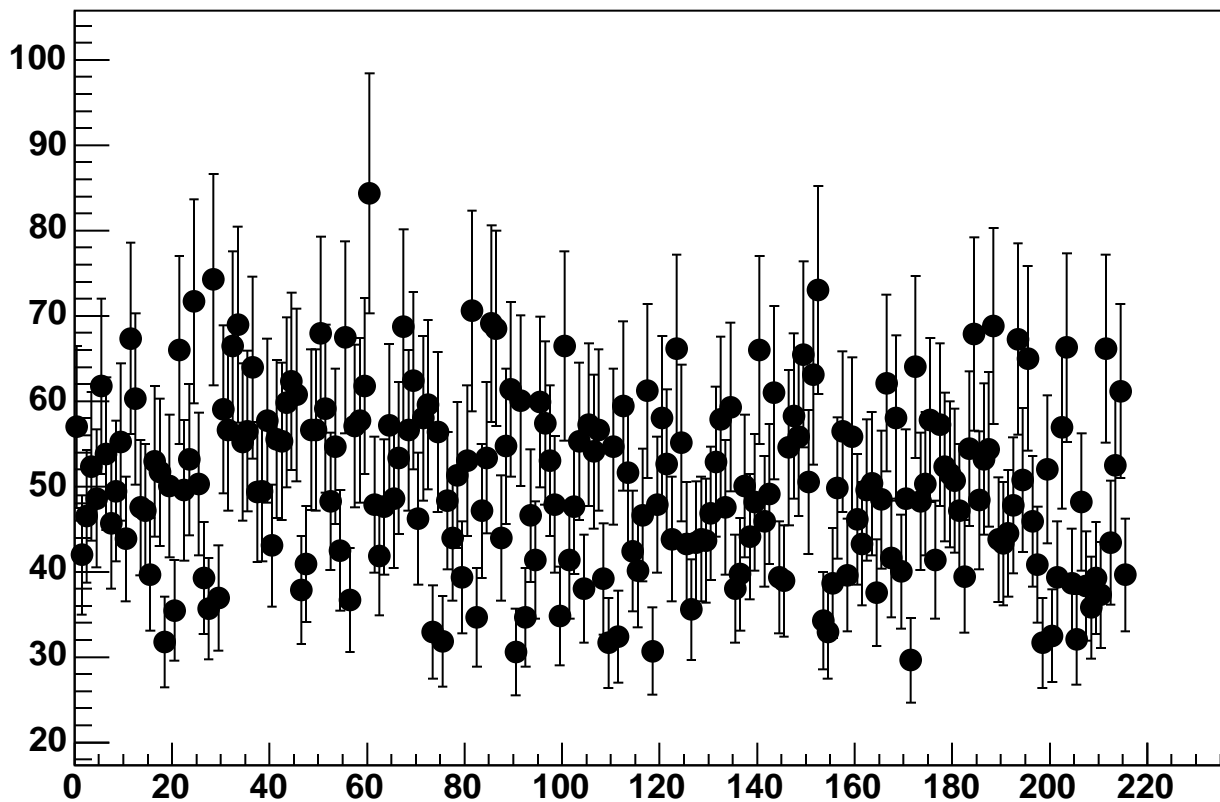
Enable 3, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



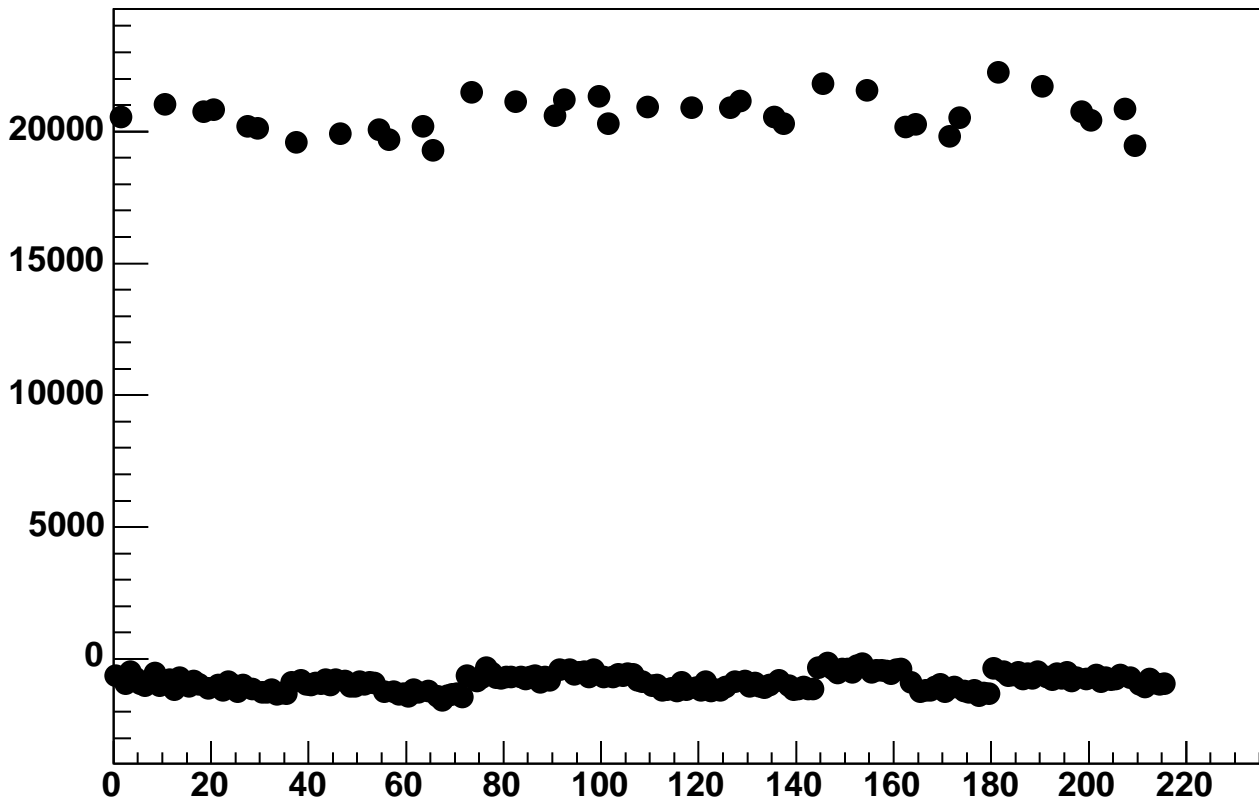
Enable 3, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan



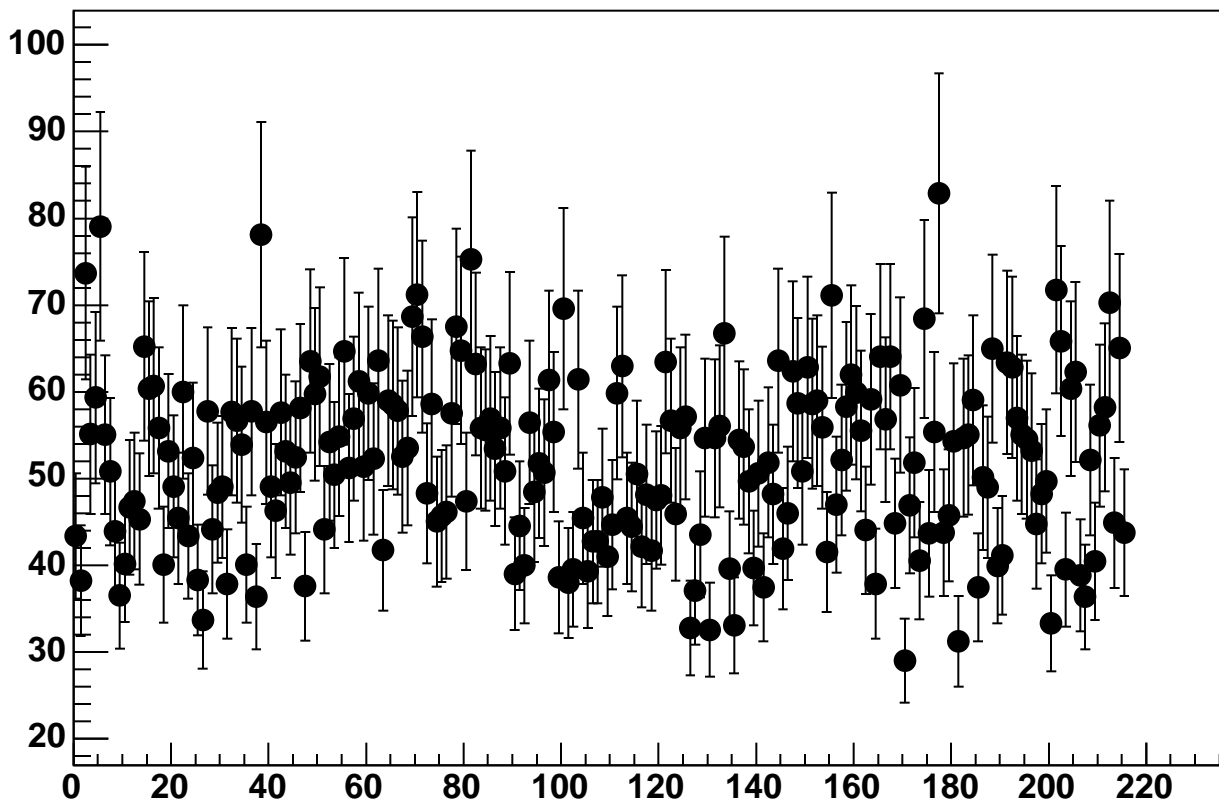
Enable 3, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan



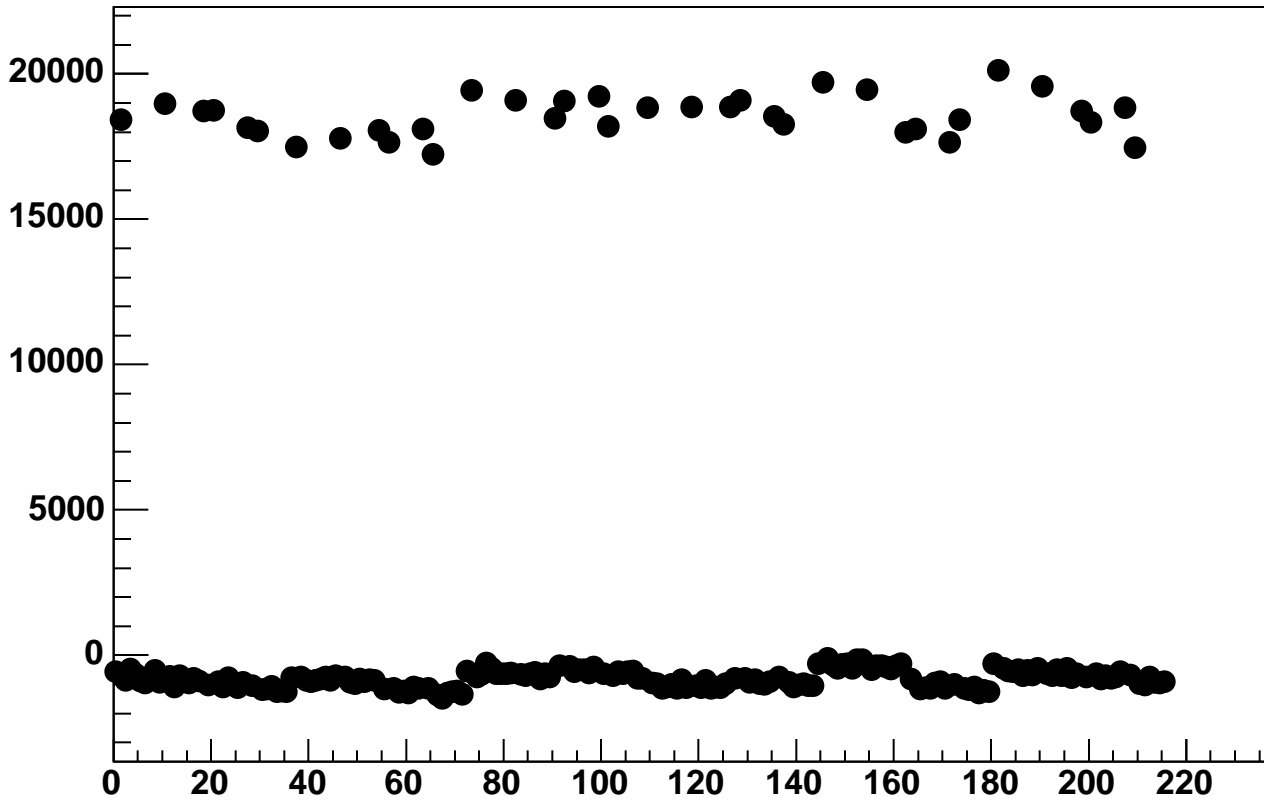
Enable 3, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



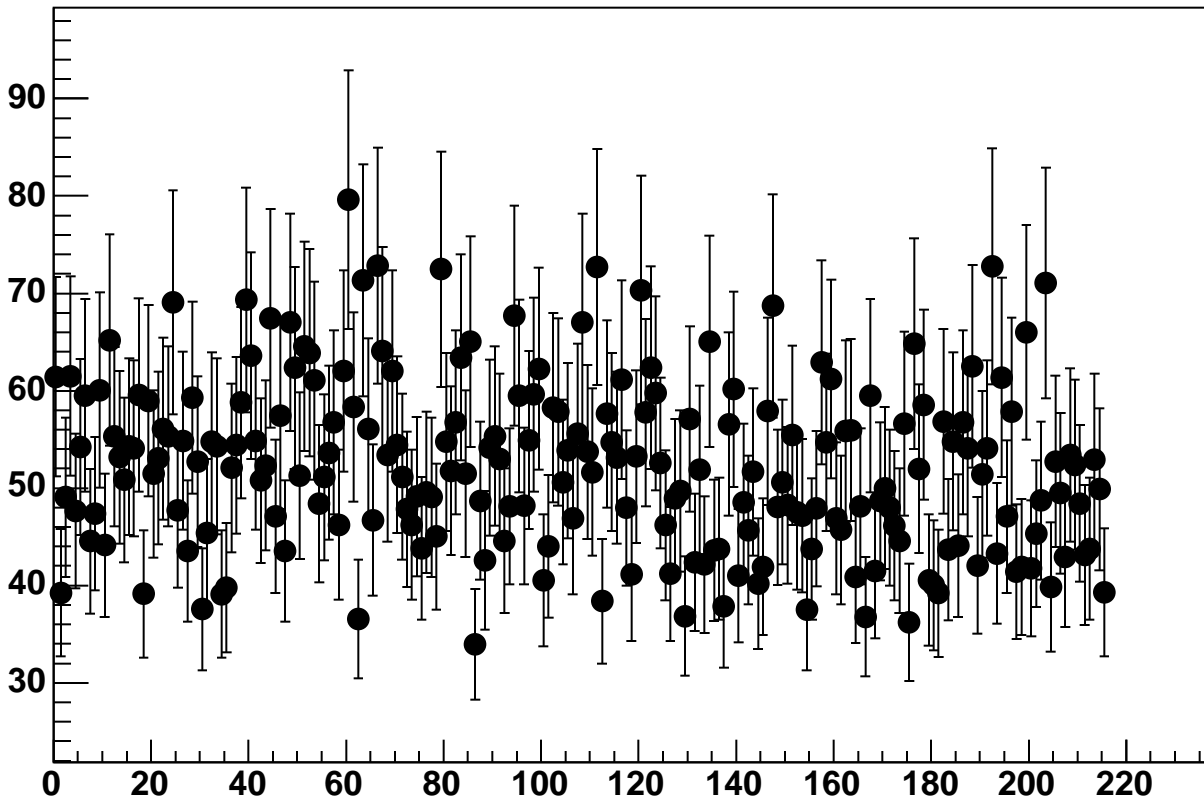
Enable 3, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



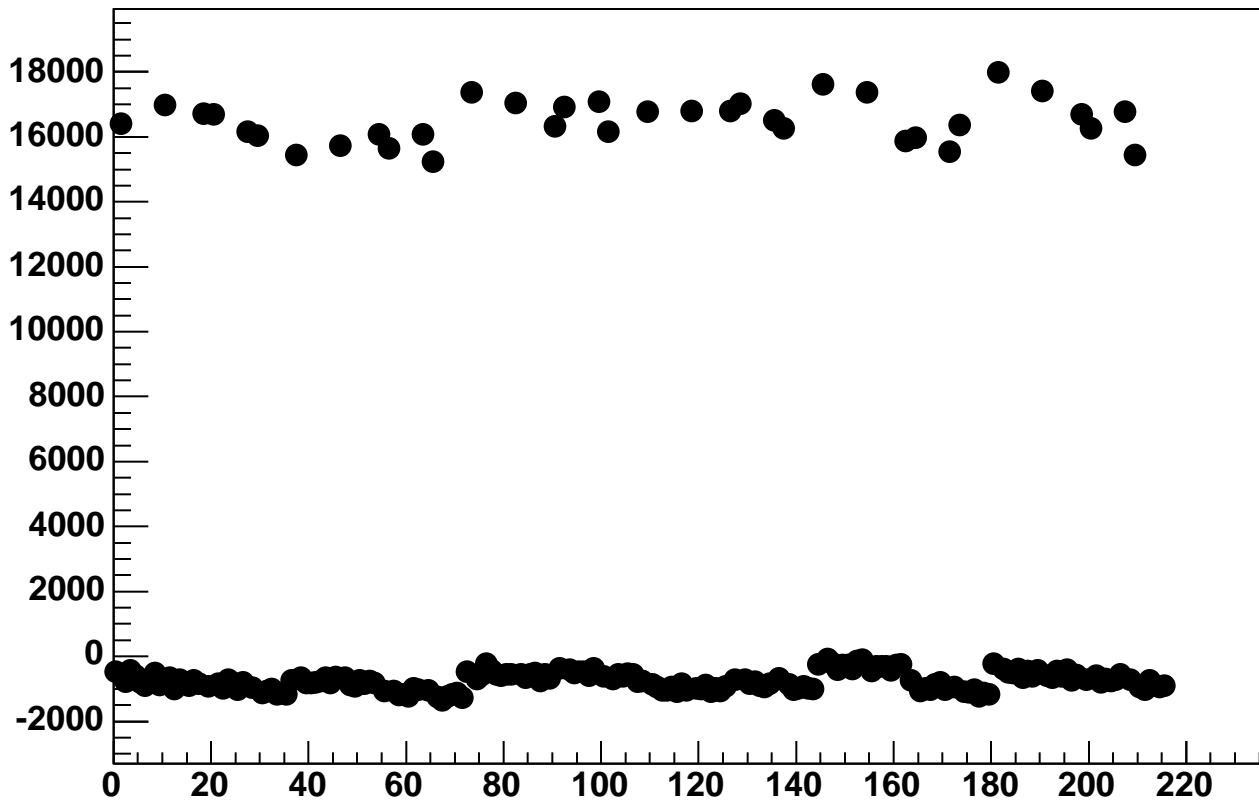
Enable 3, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan



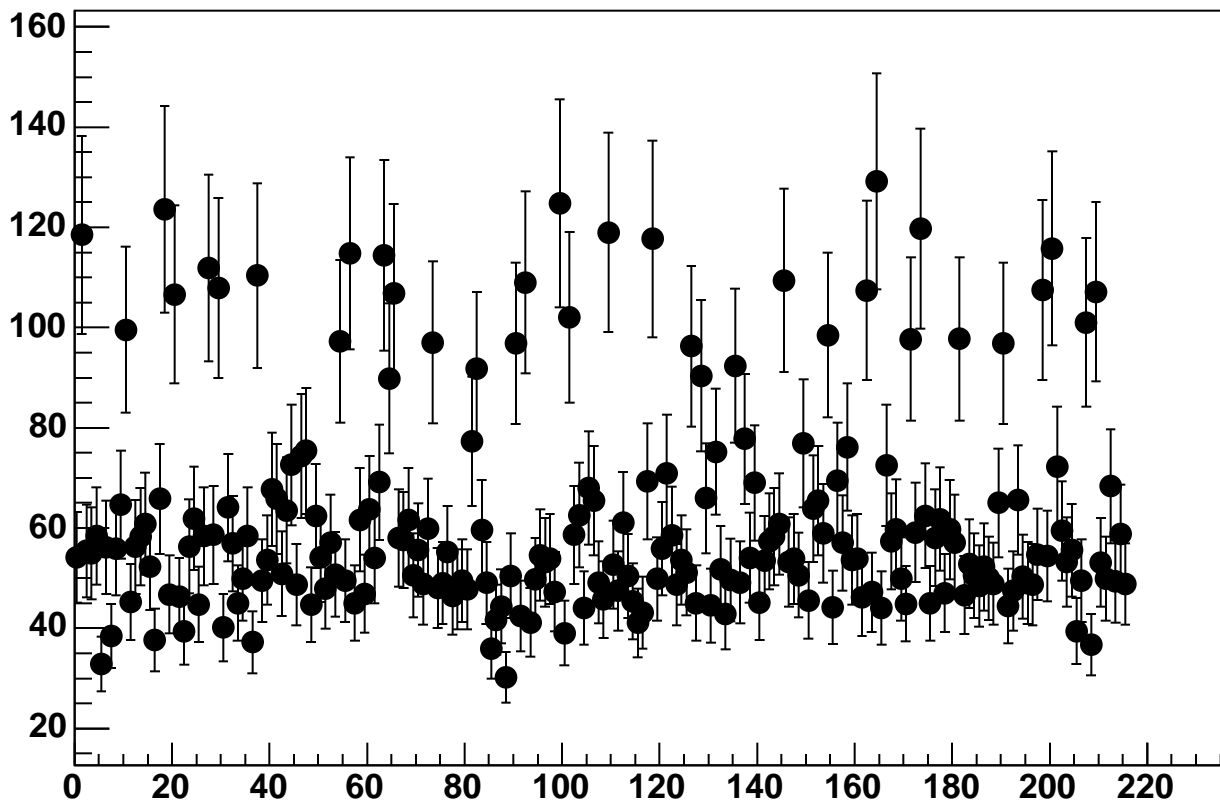
Enable 3, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan



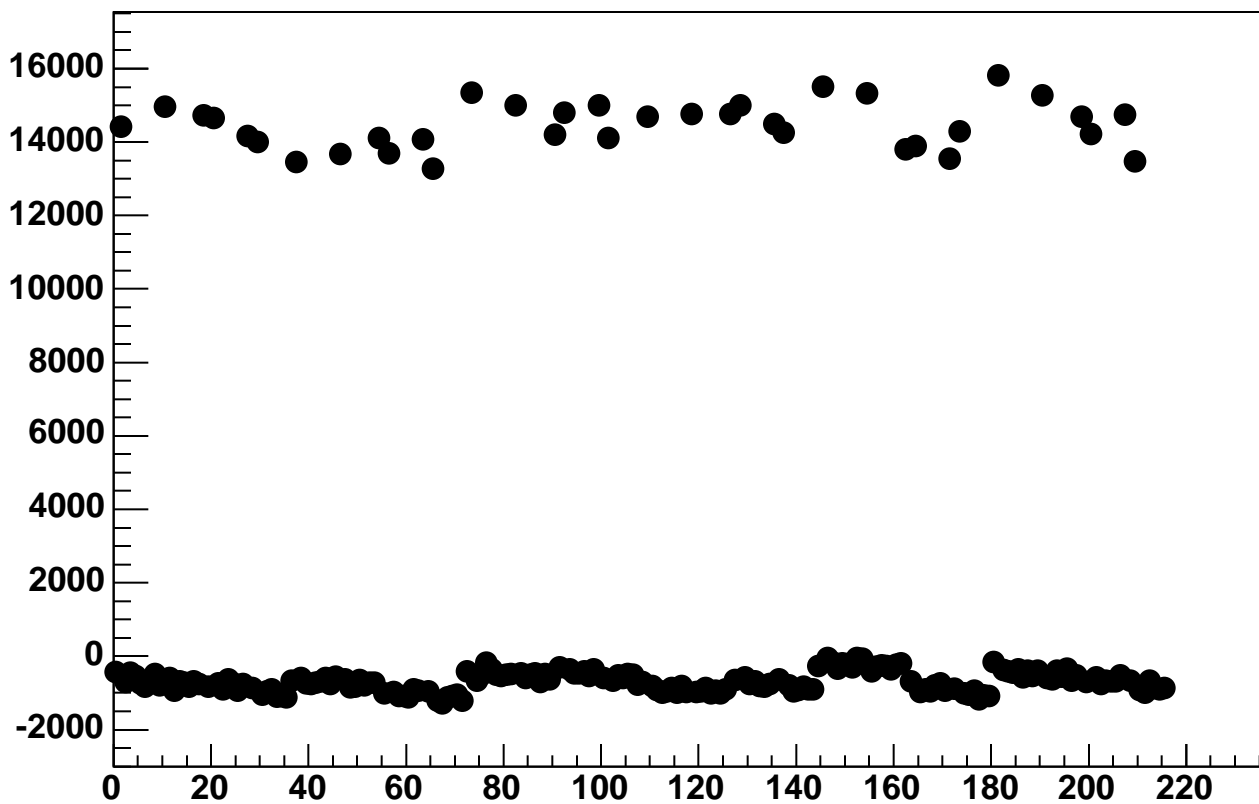
Enable 3, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



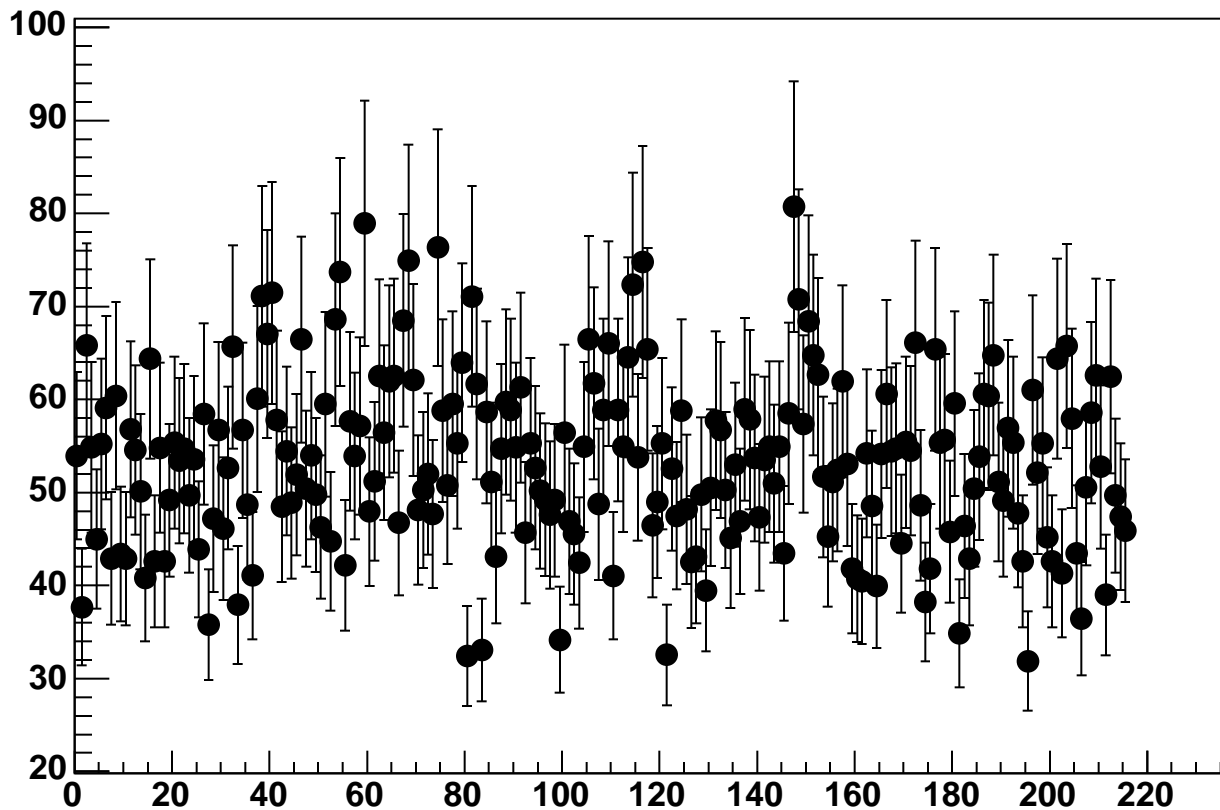
Enable 3, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan

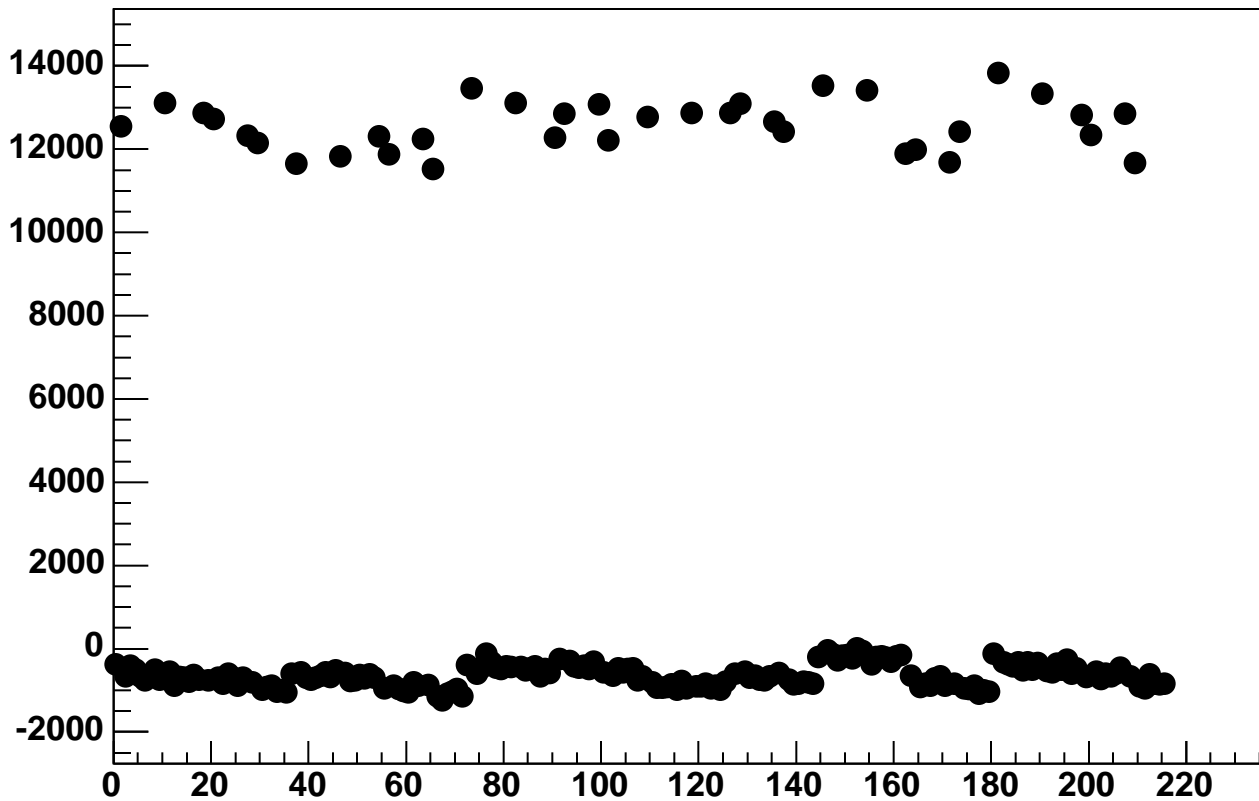


Enable 3, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan

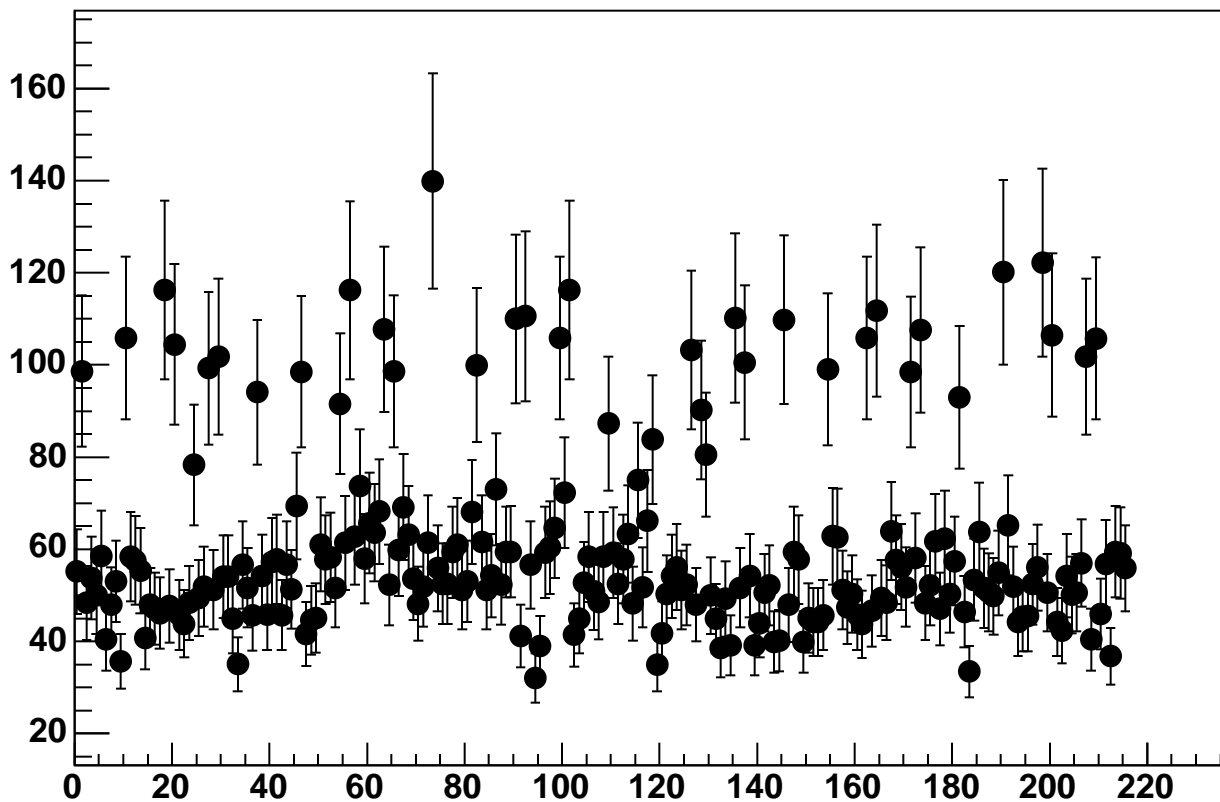




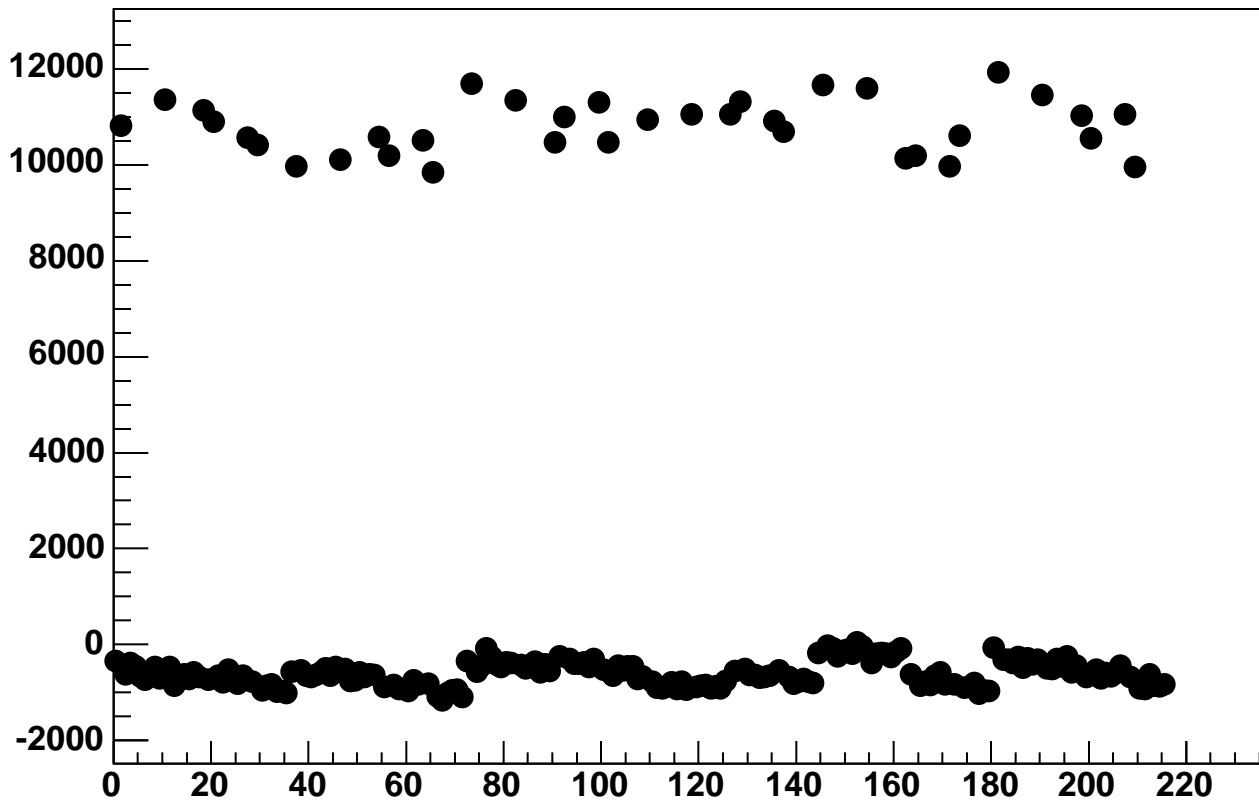
Enable 3, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



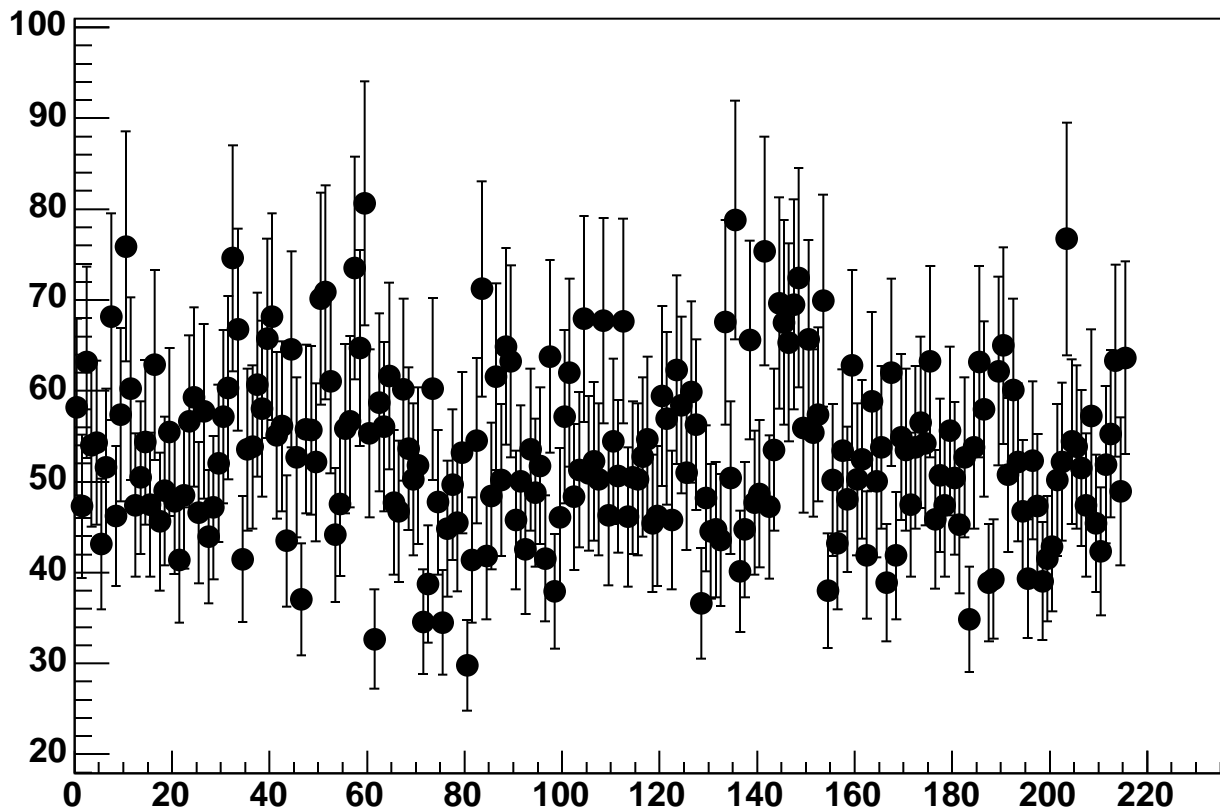
Enable 3, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



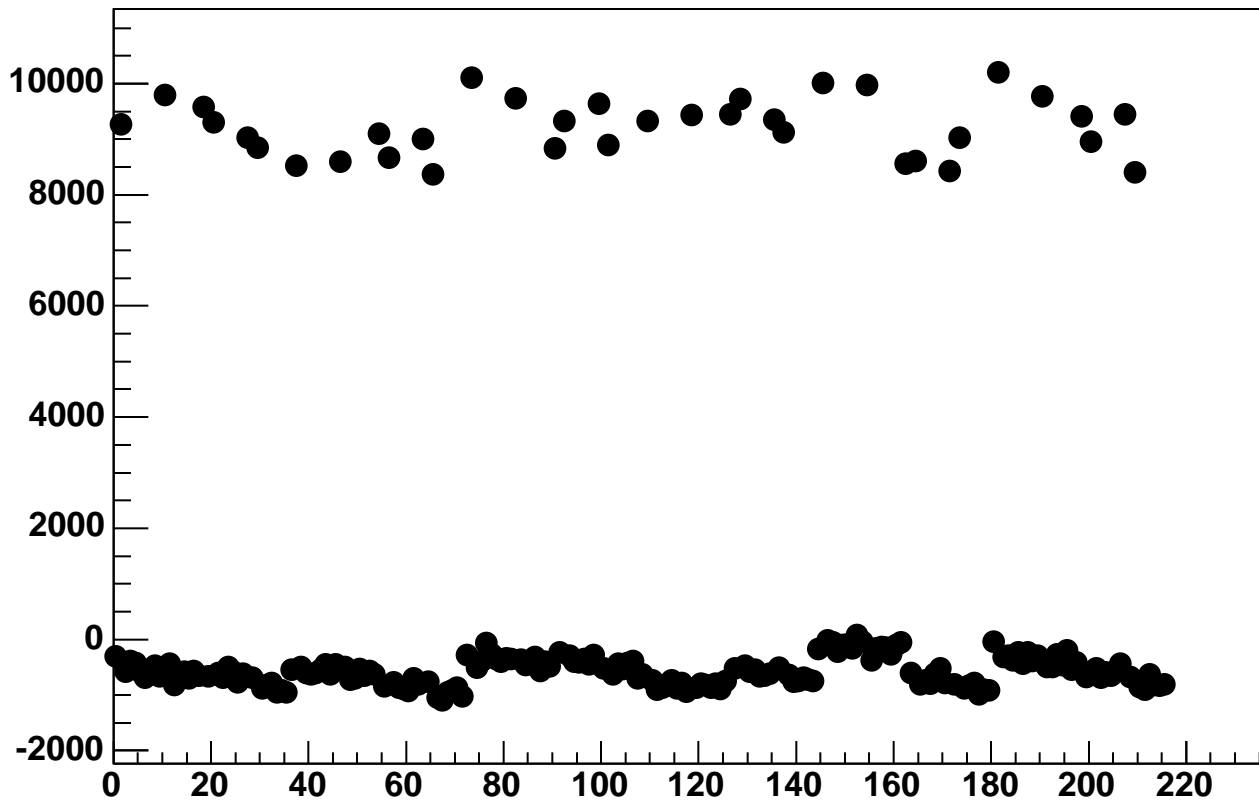
Enable 3, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan



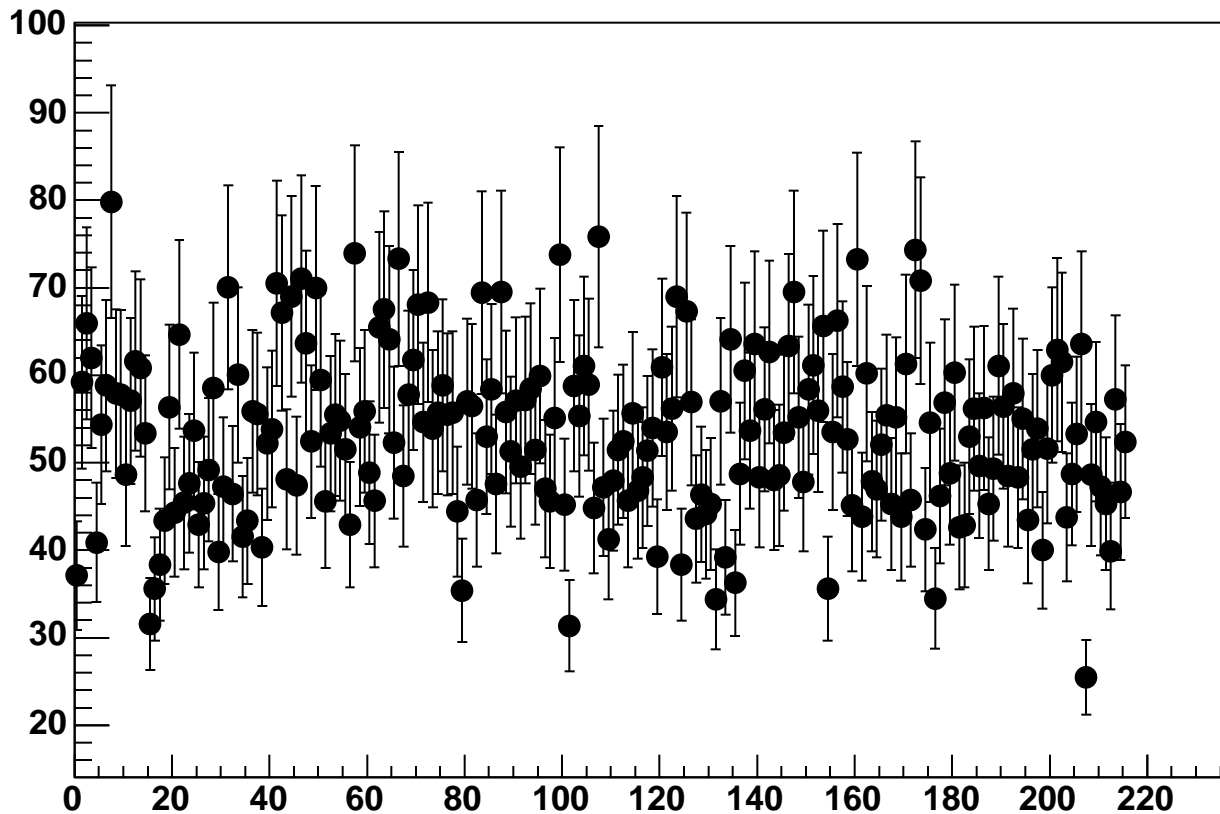
Enable 3, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan



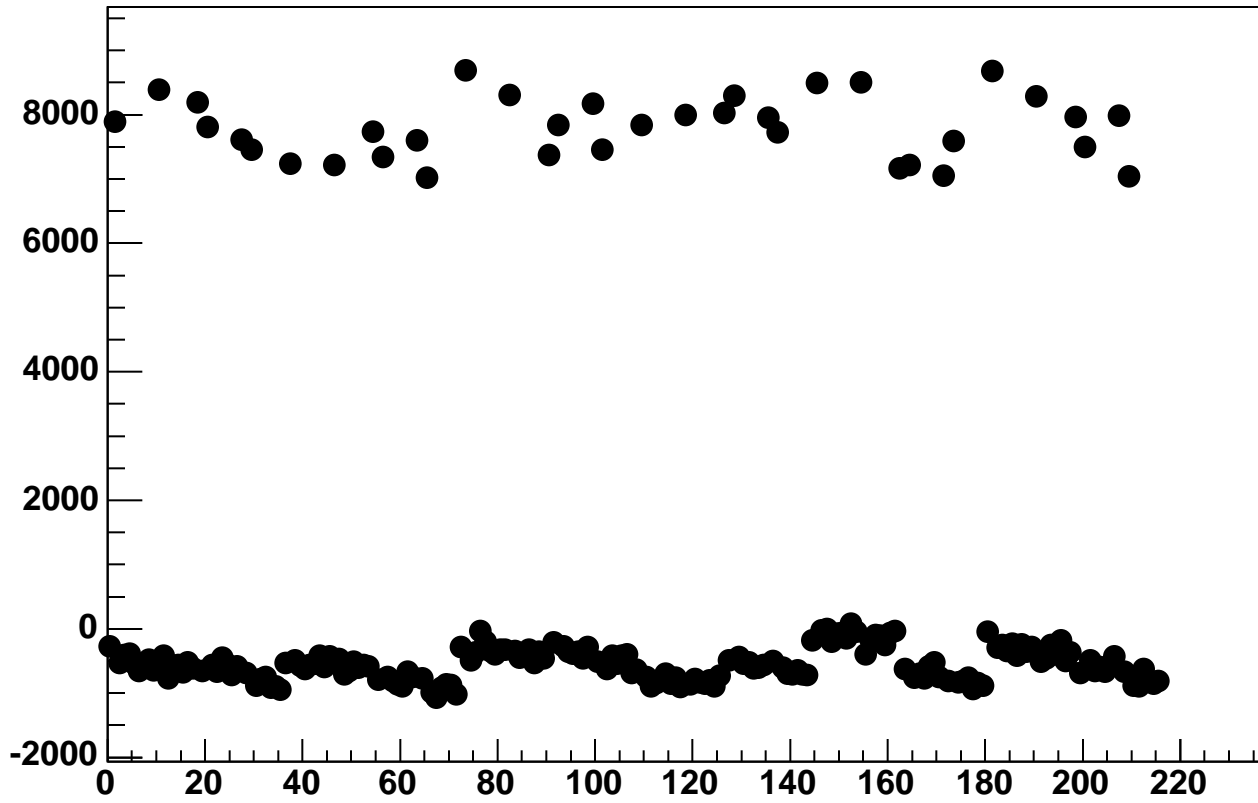
Enable 3, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



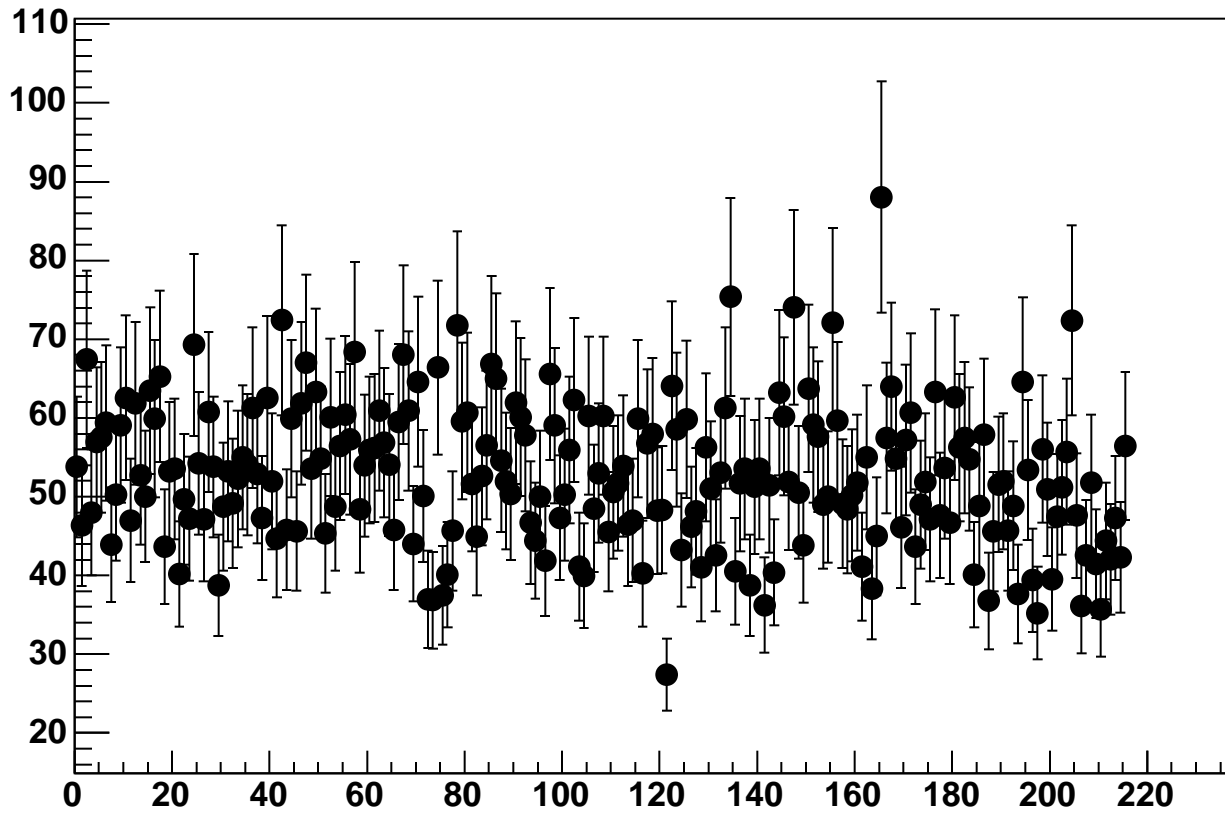
Enable 3, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



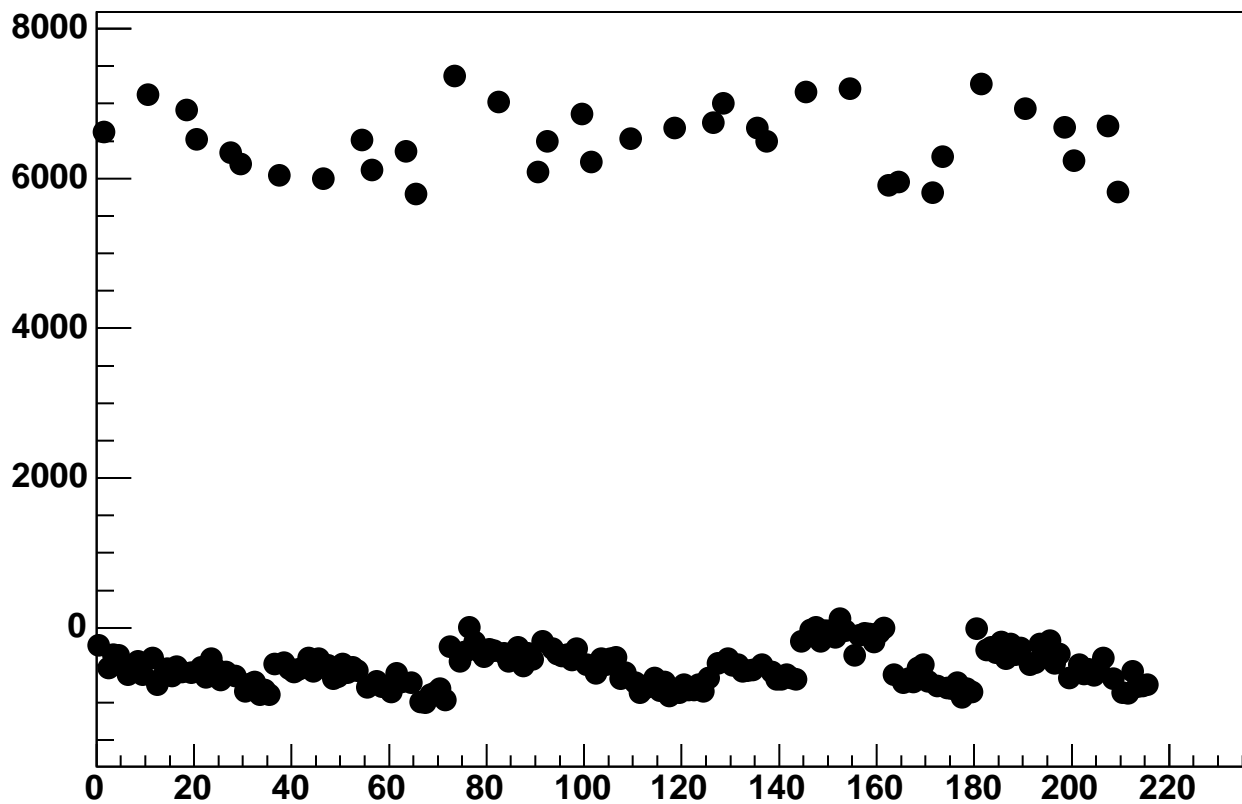
Enable 3, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan



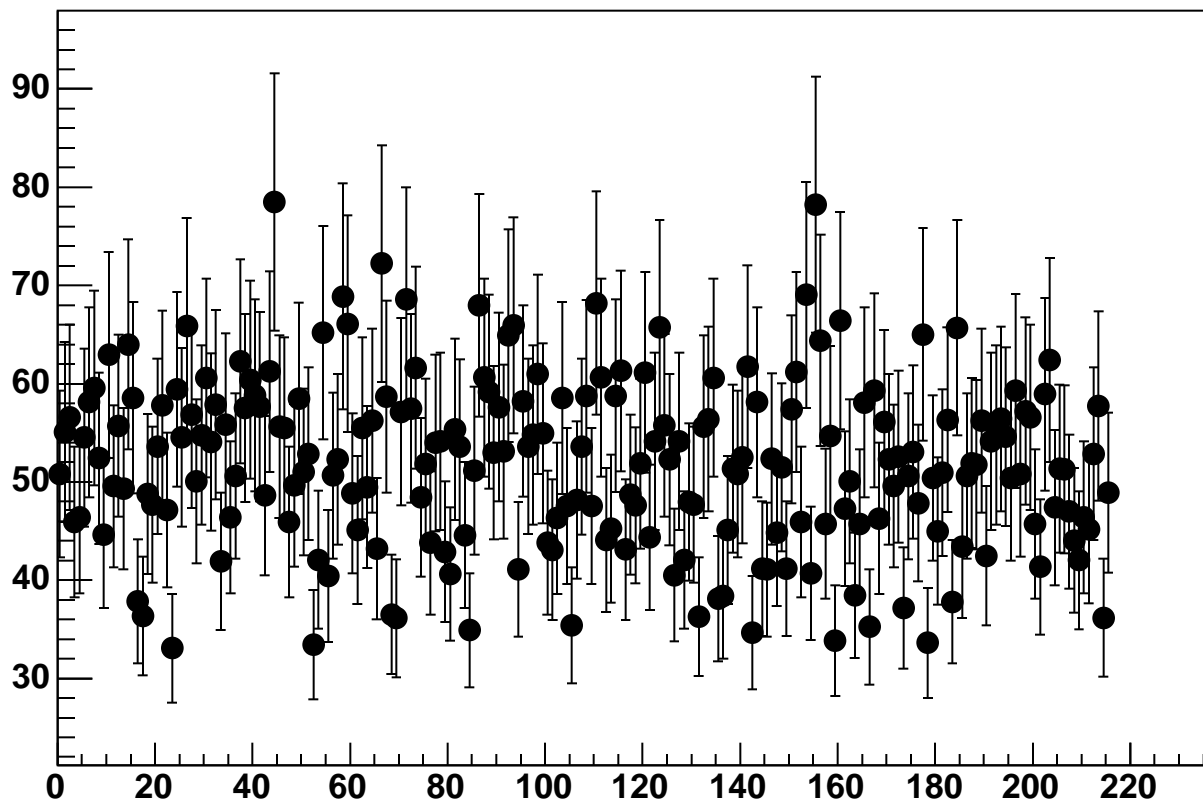
Enable 3, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan



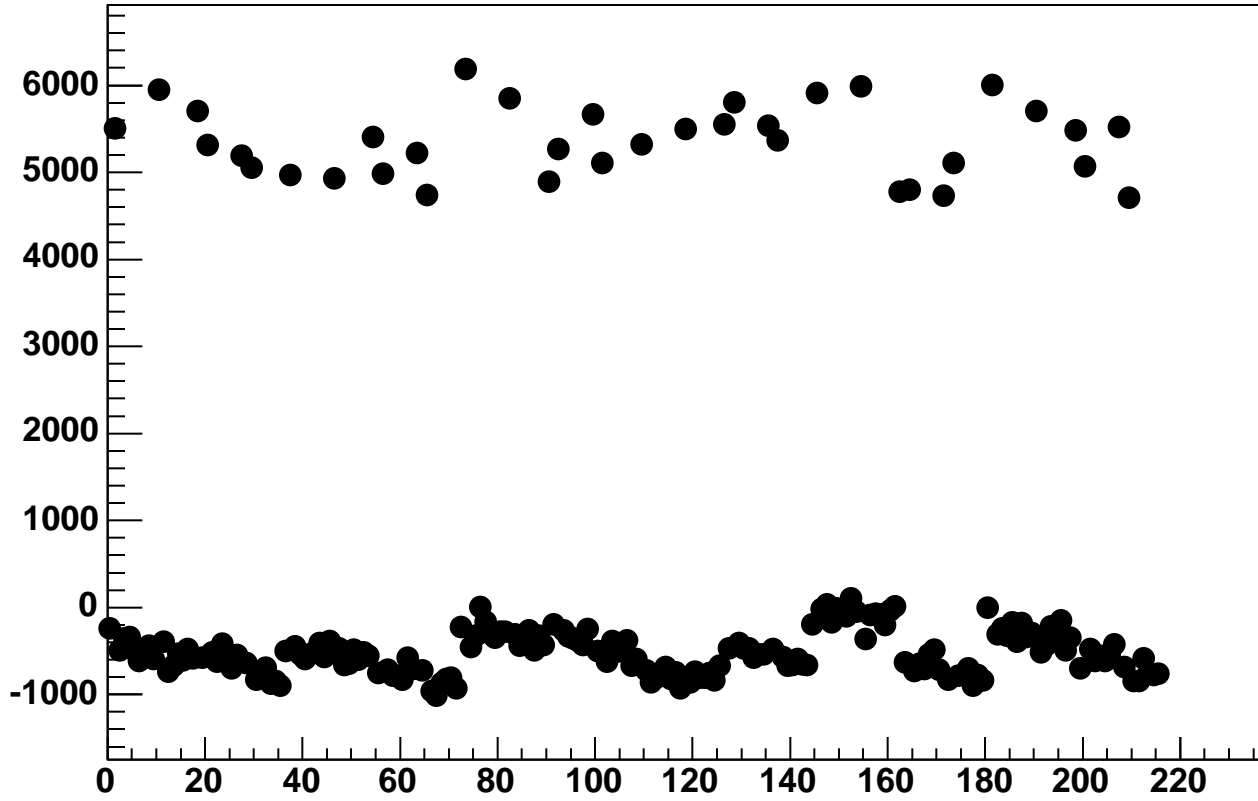
Enable 3, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



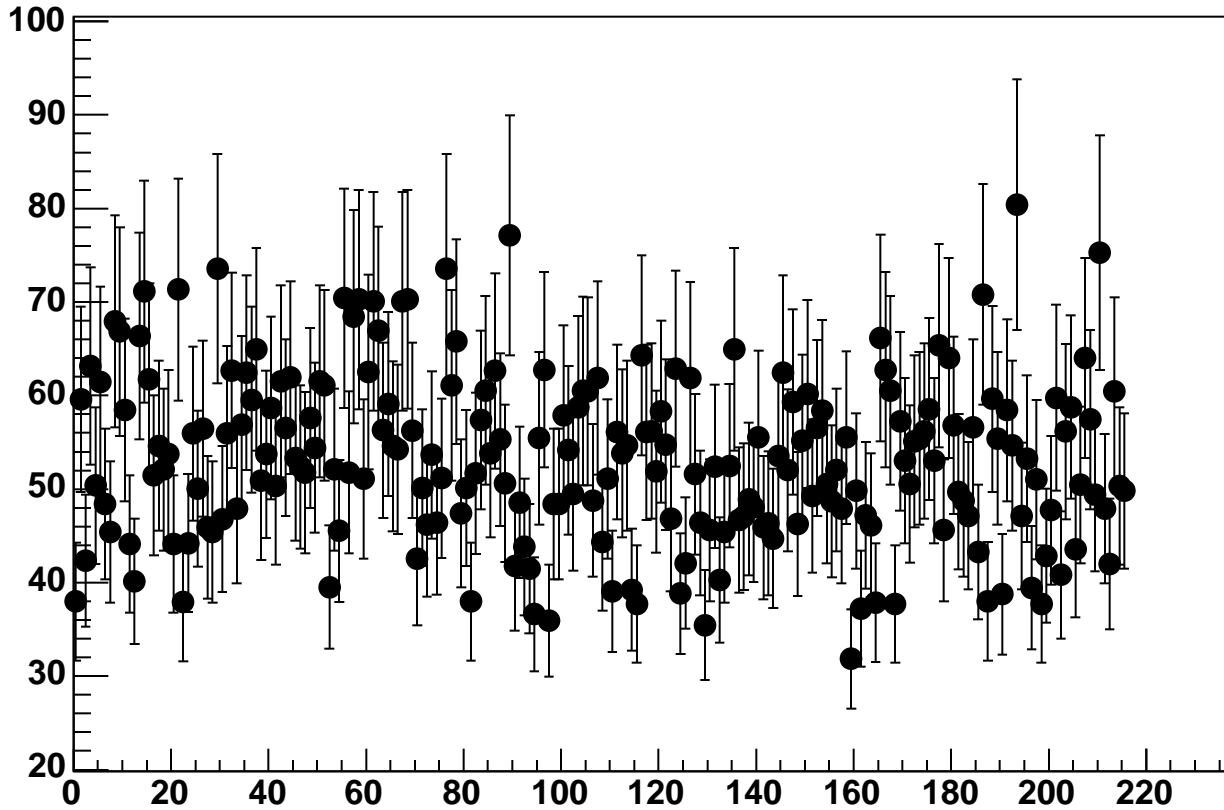
Enable 3, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



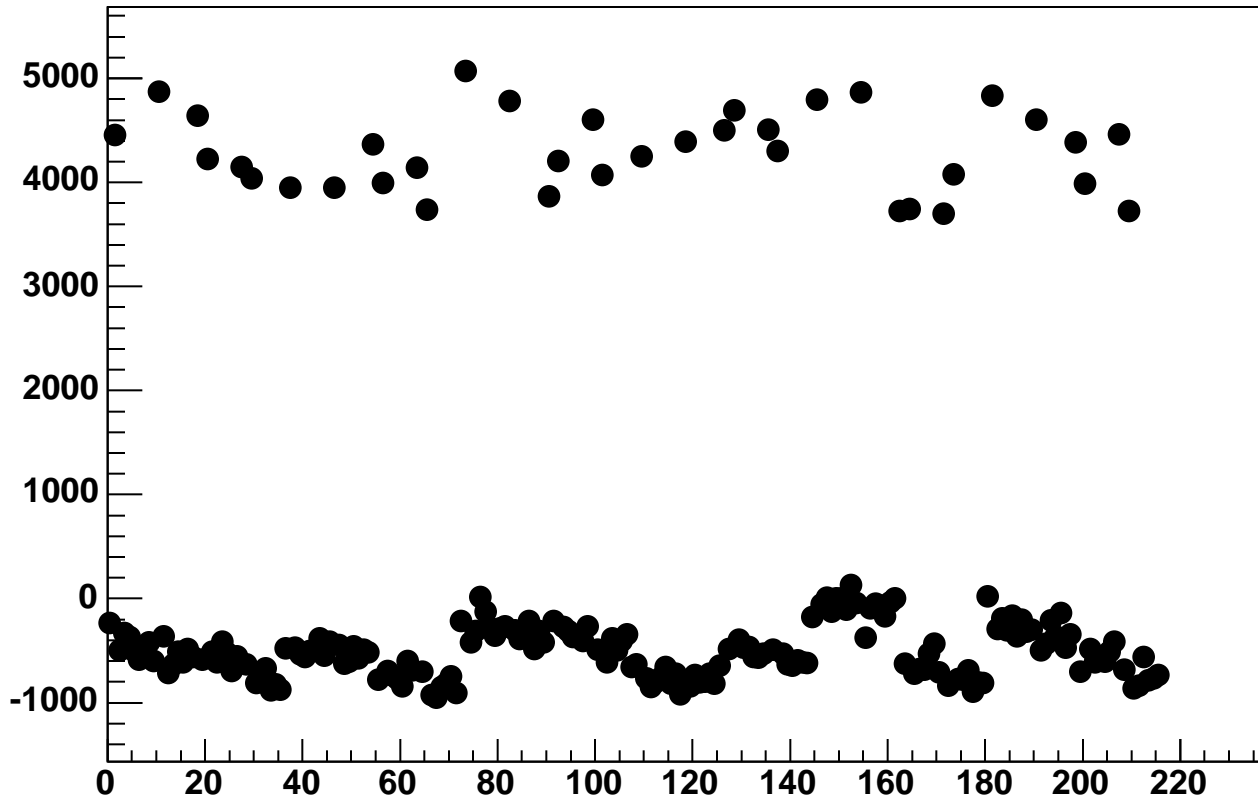
Enable 3, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan



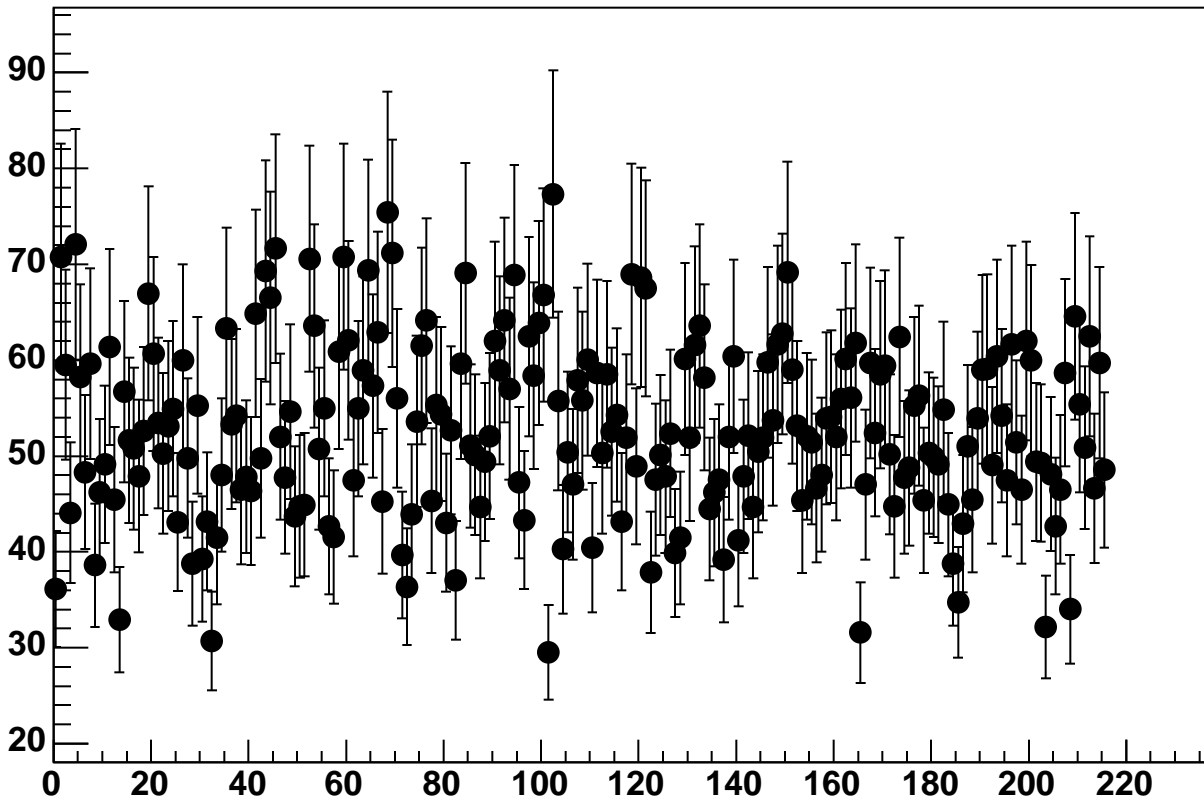
Enable 3, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan



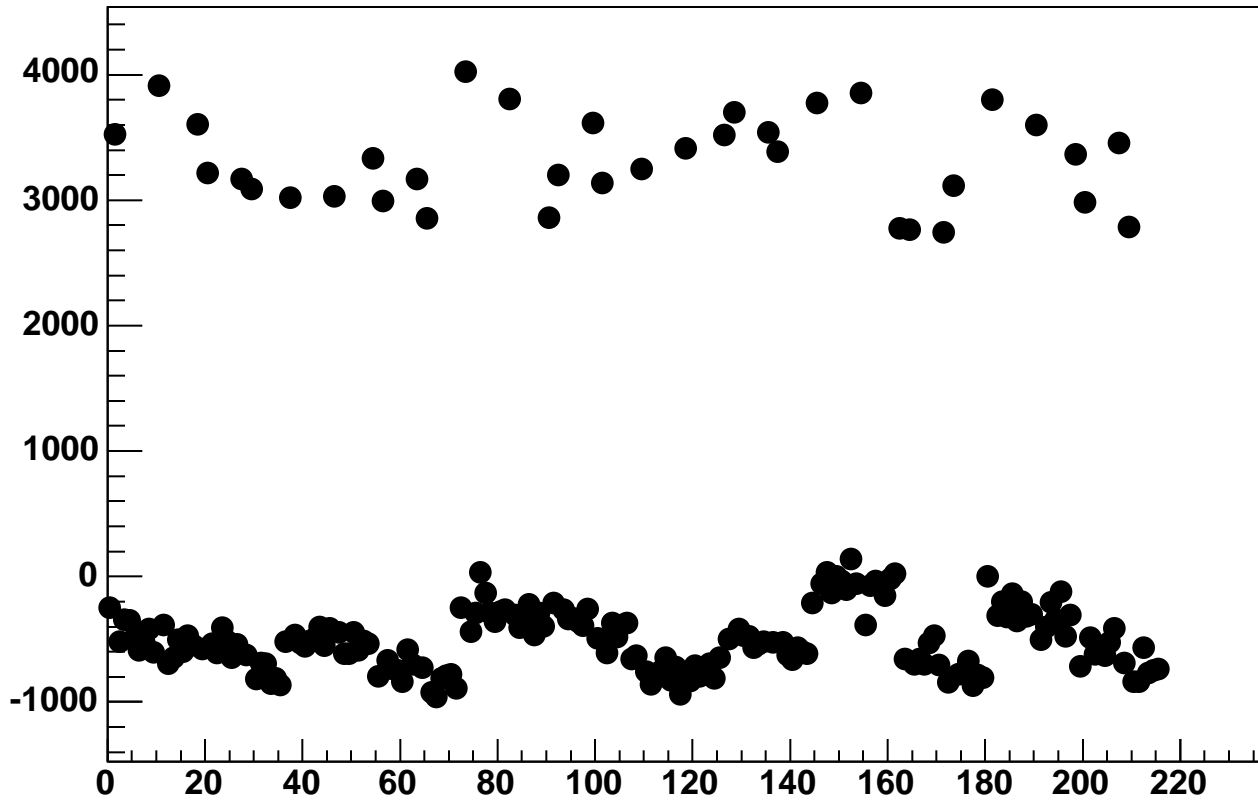
Enable 3, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



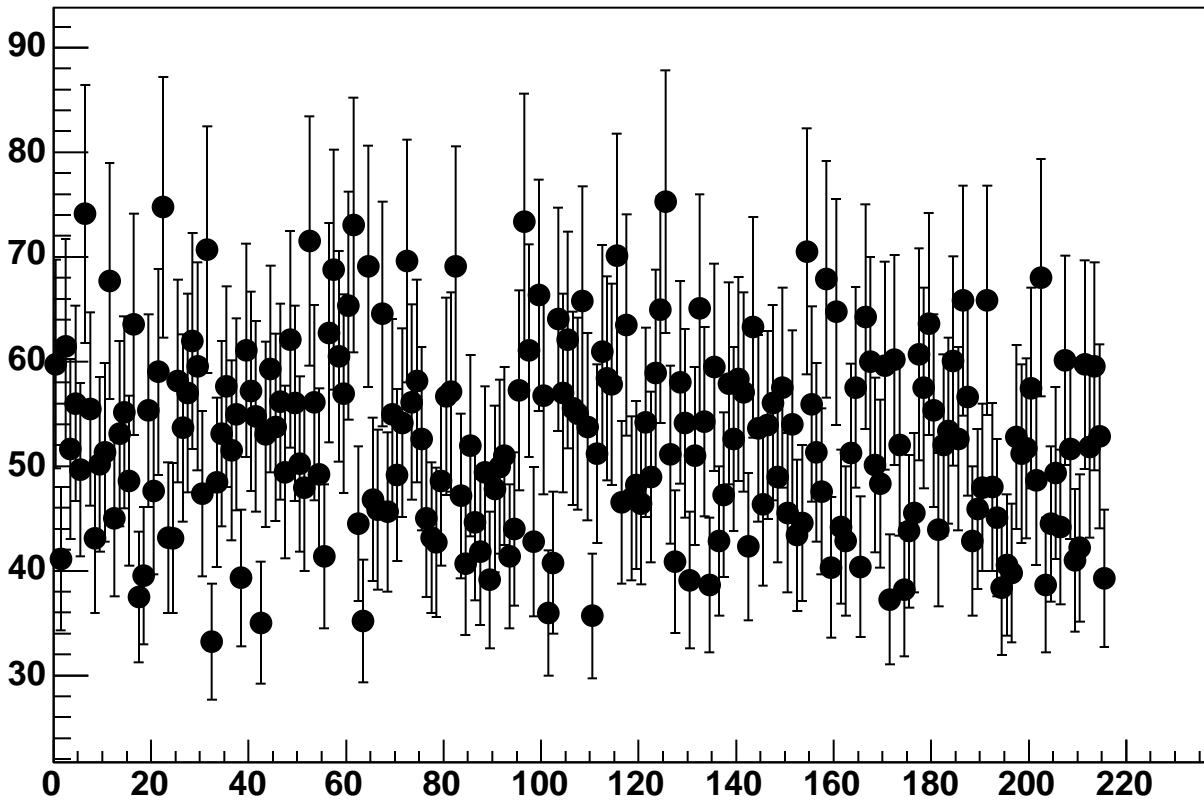
Enable 3, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan

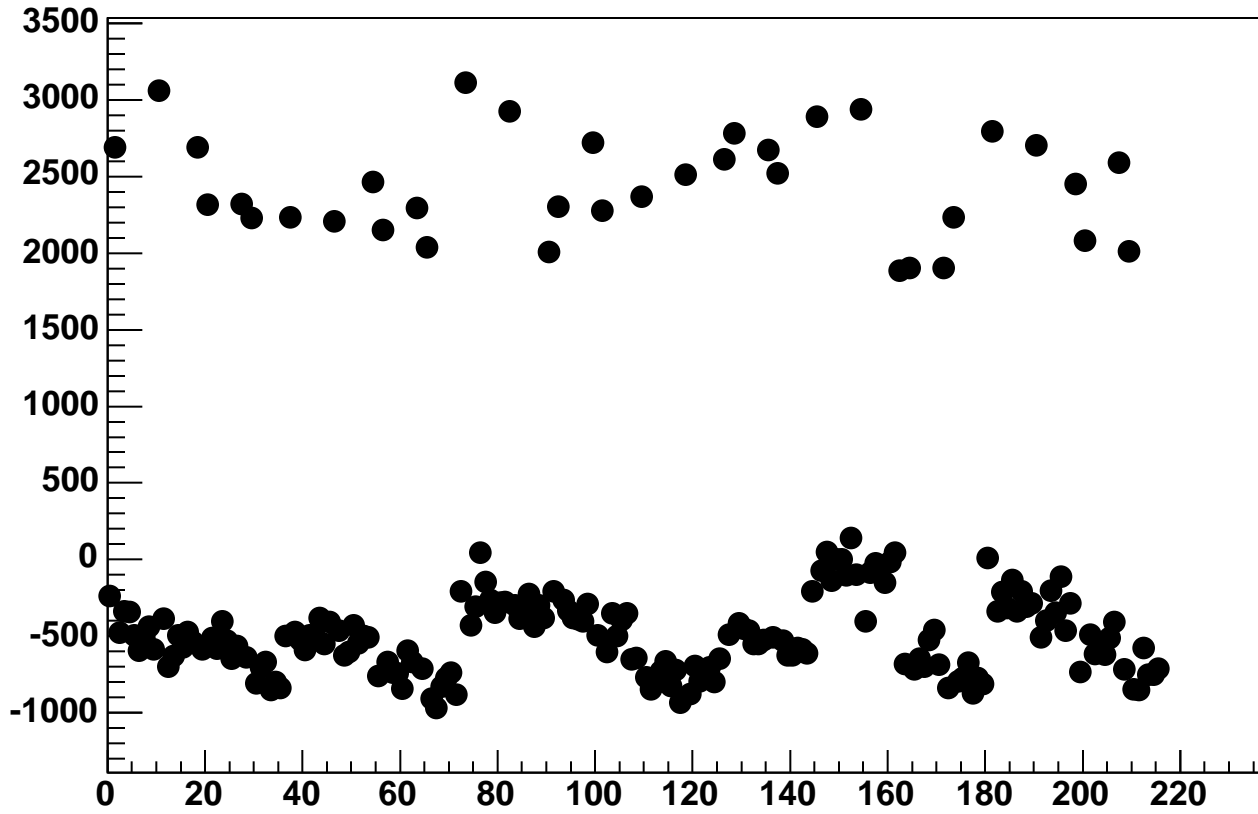


Enable 3, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan

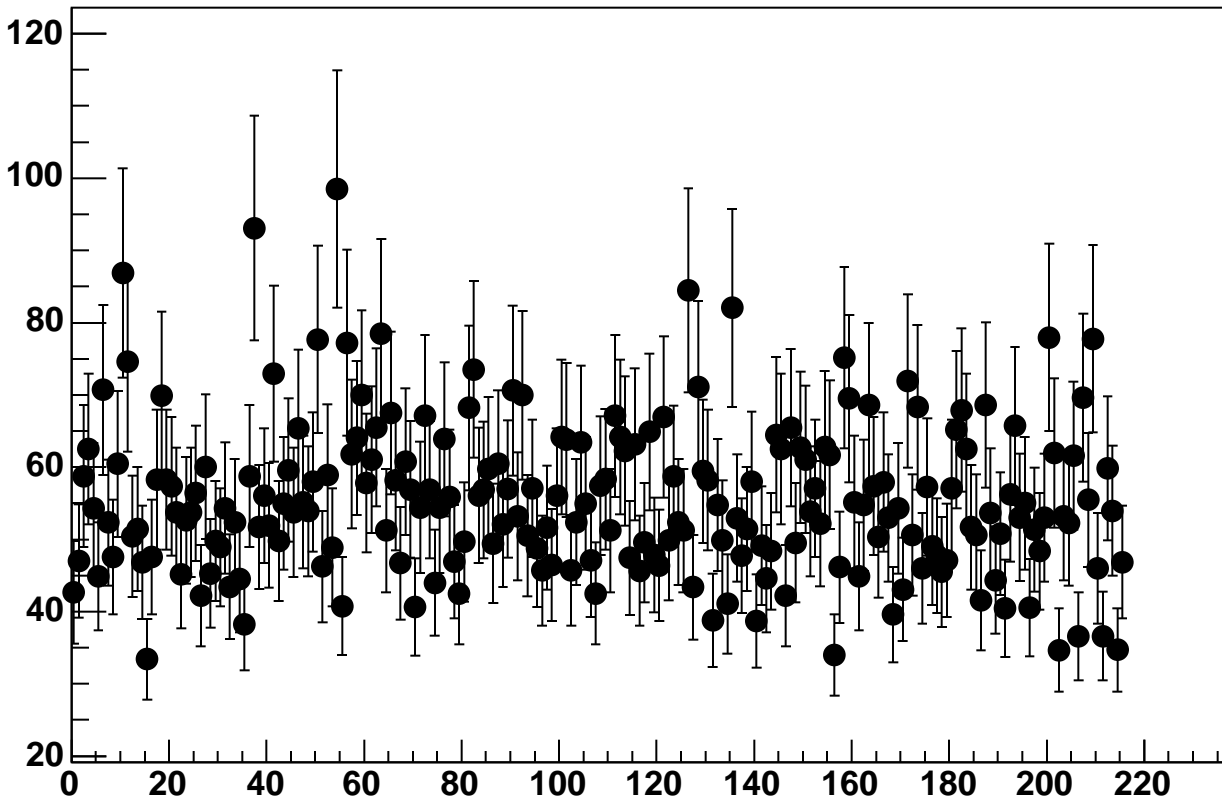




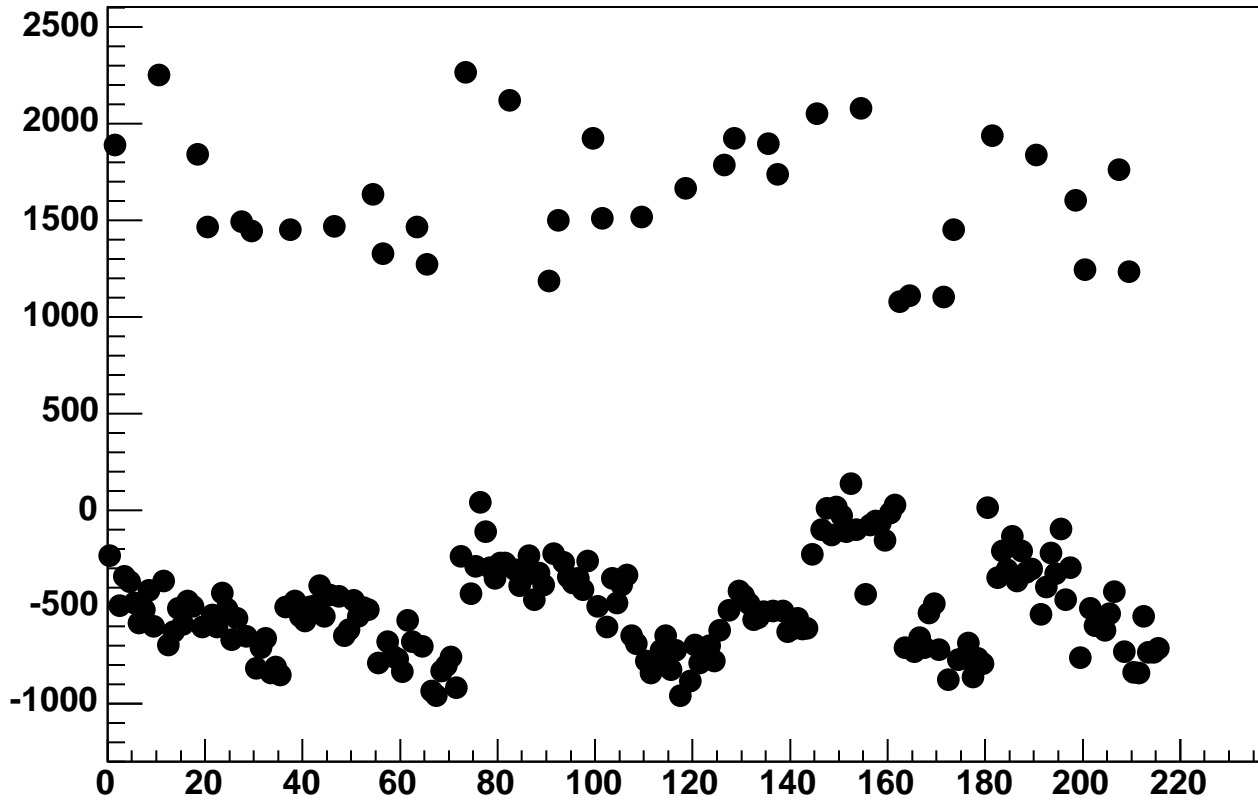
Enable 3, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



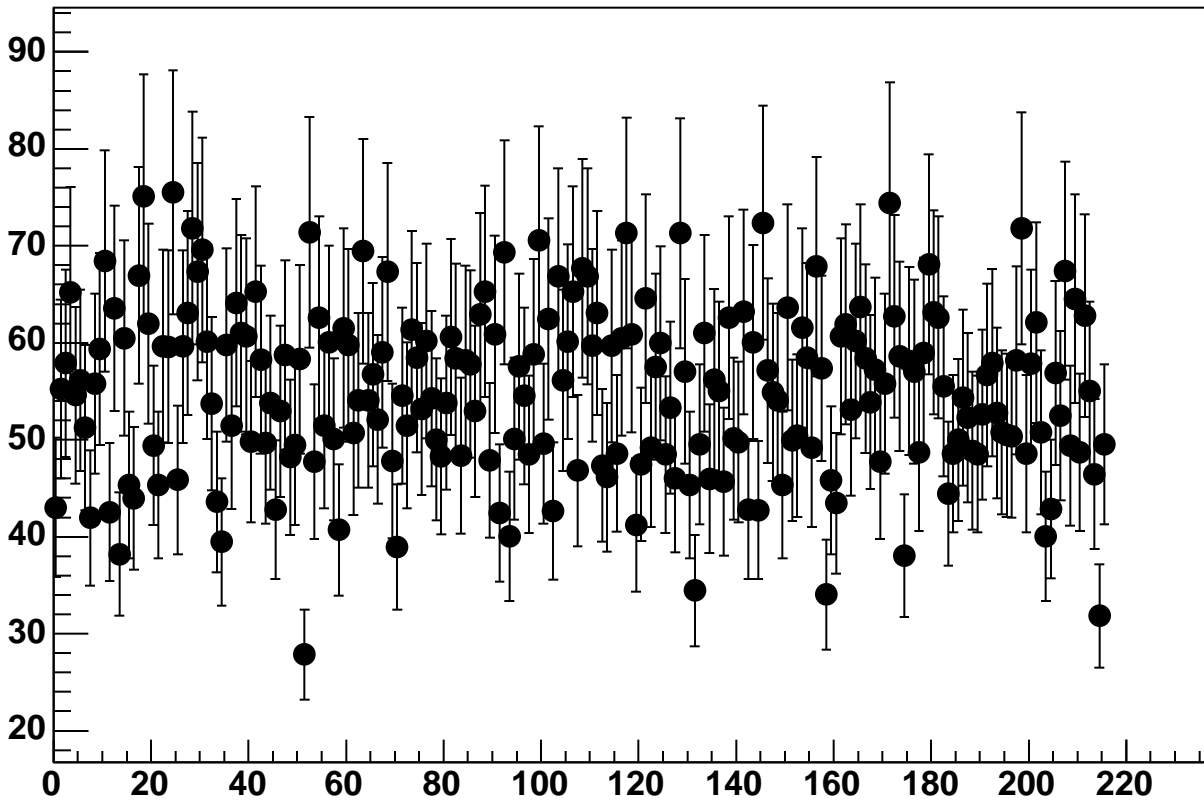
Enable 3, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



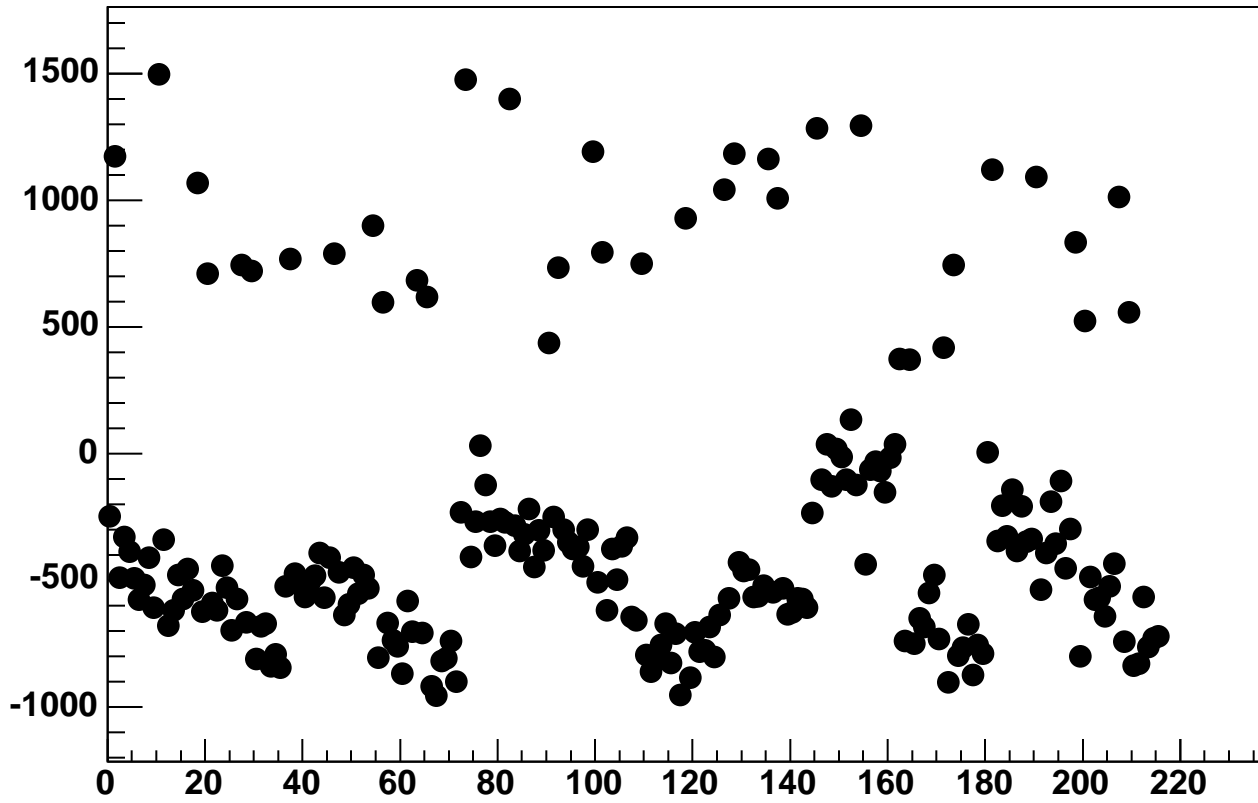
Enable 3, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan



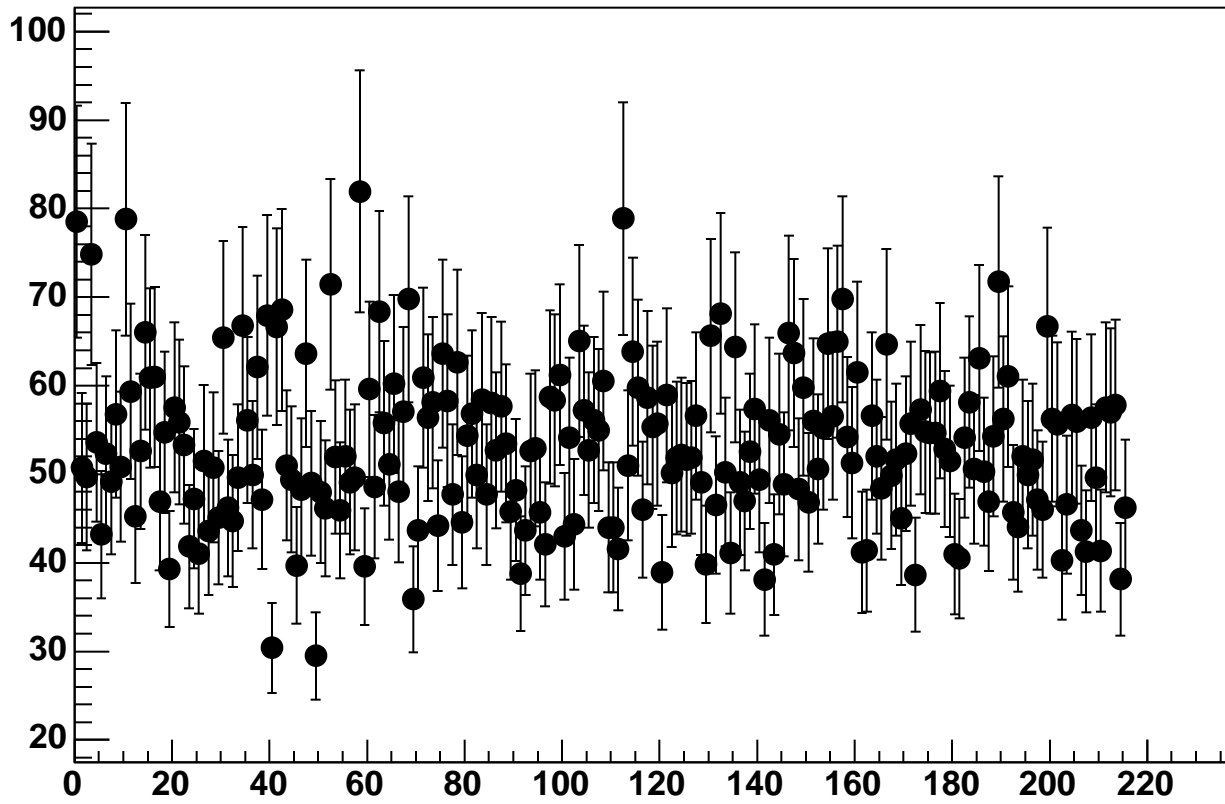
Enable 3, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan



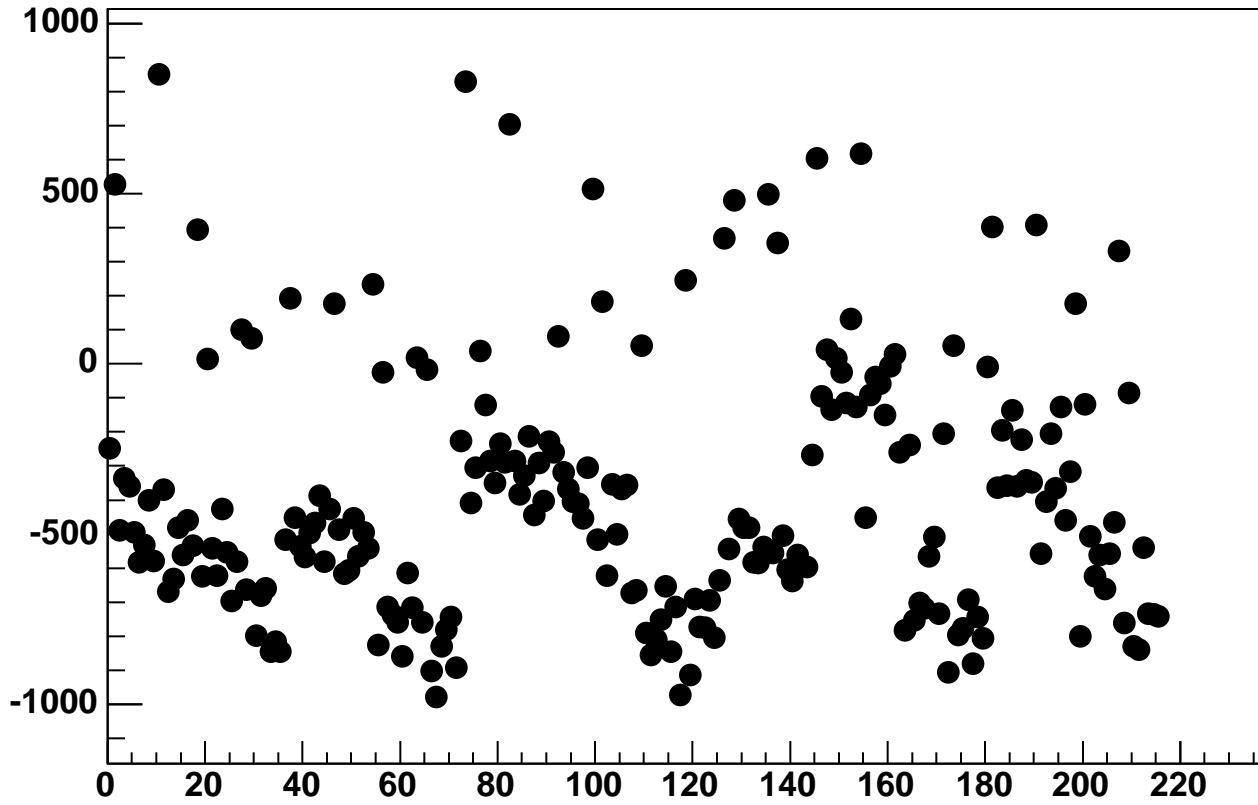
Enable 3, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



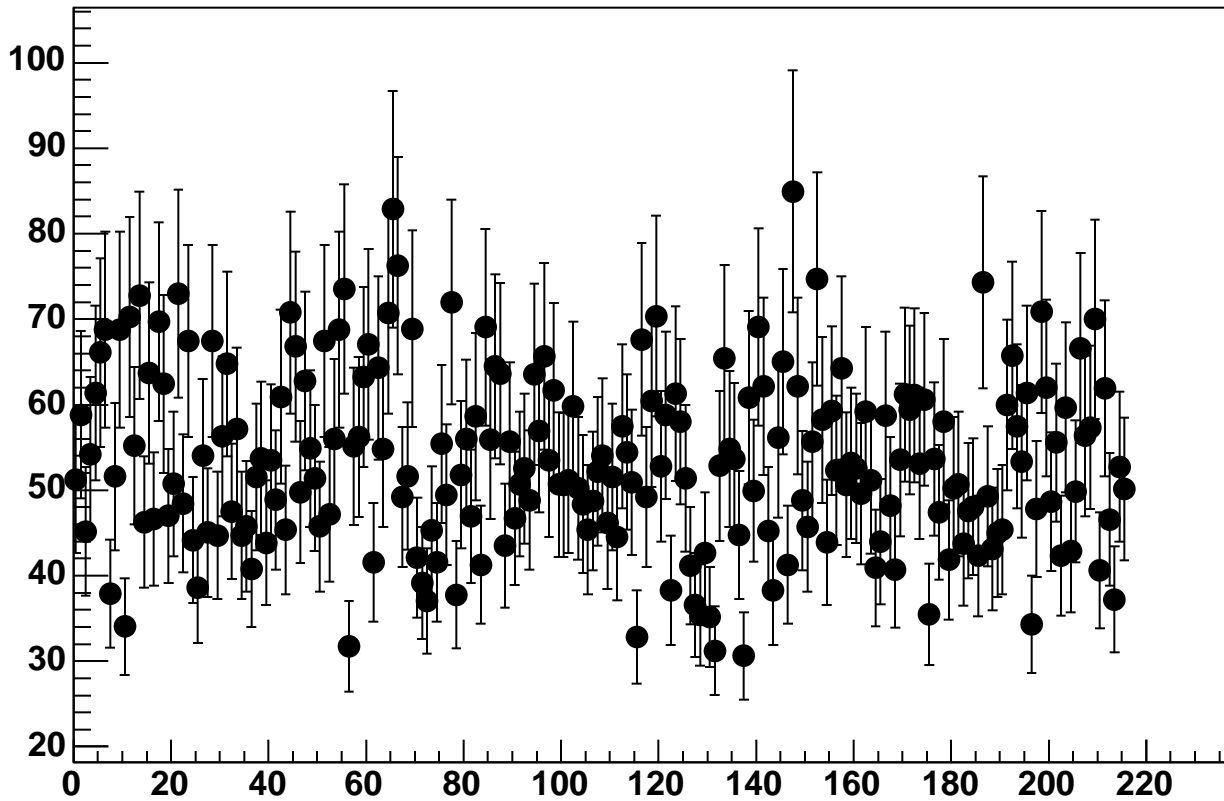
Enable 3, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



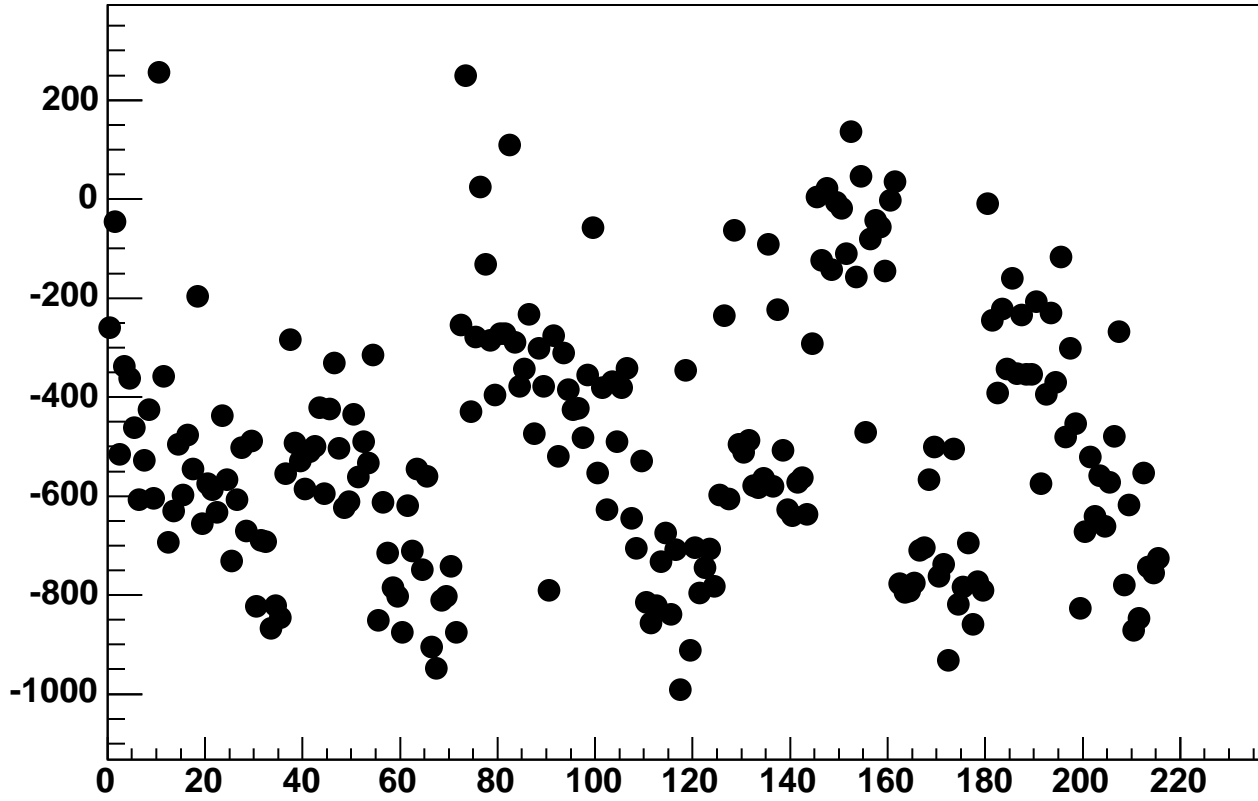
Enable 3, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan



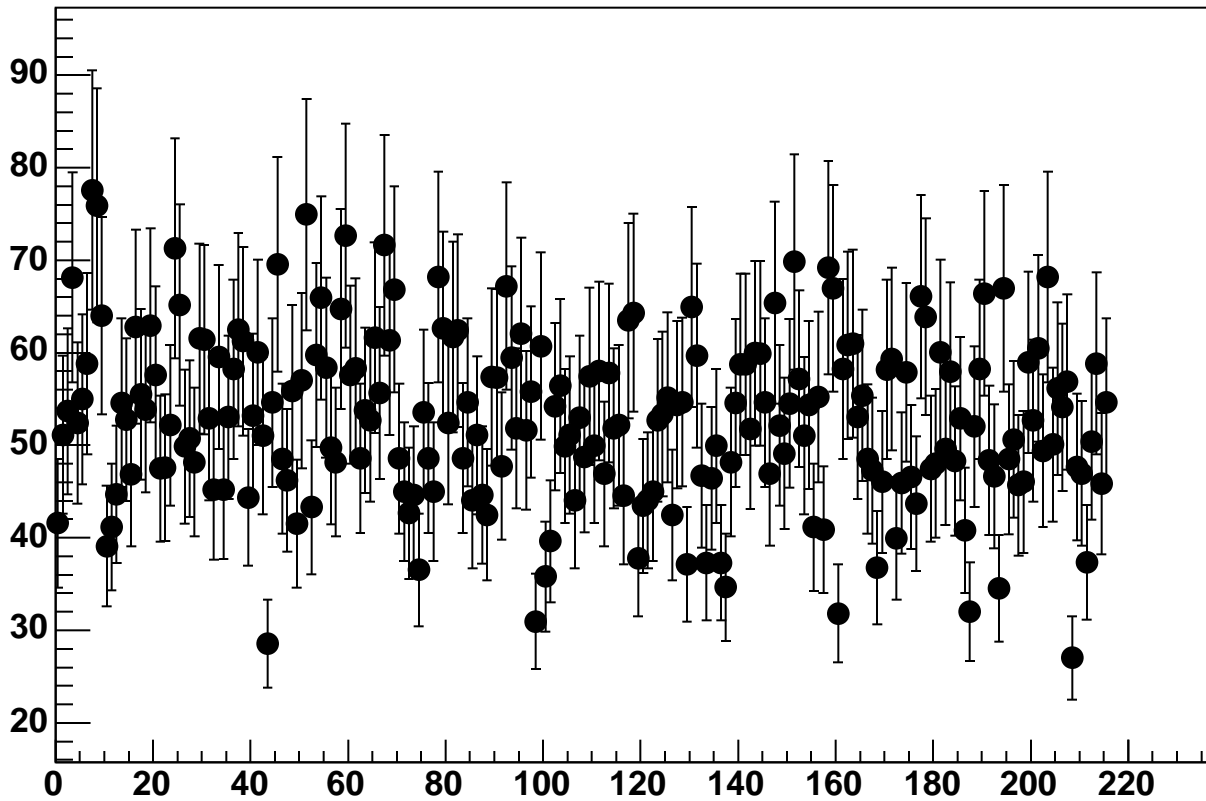
Enable 3, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan



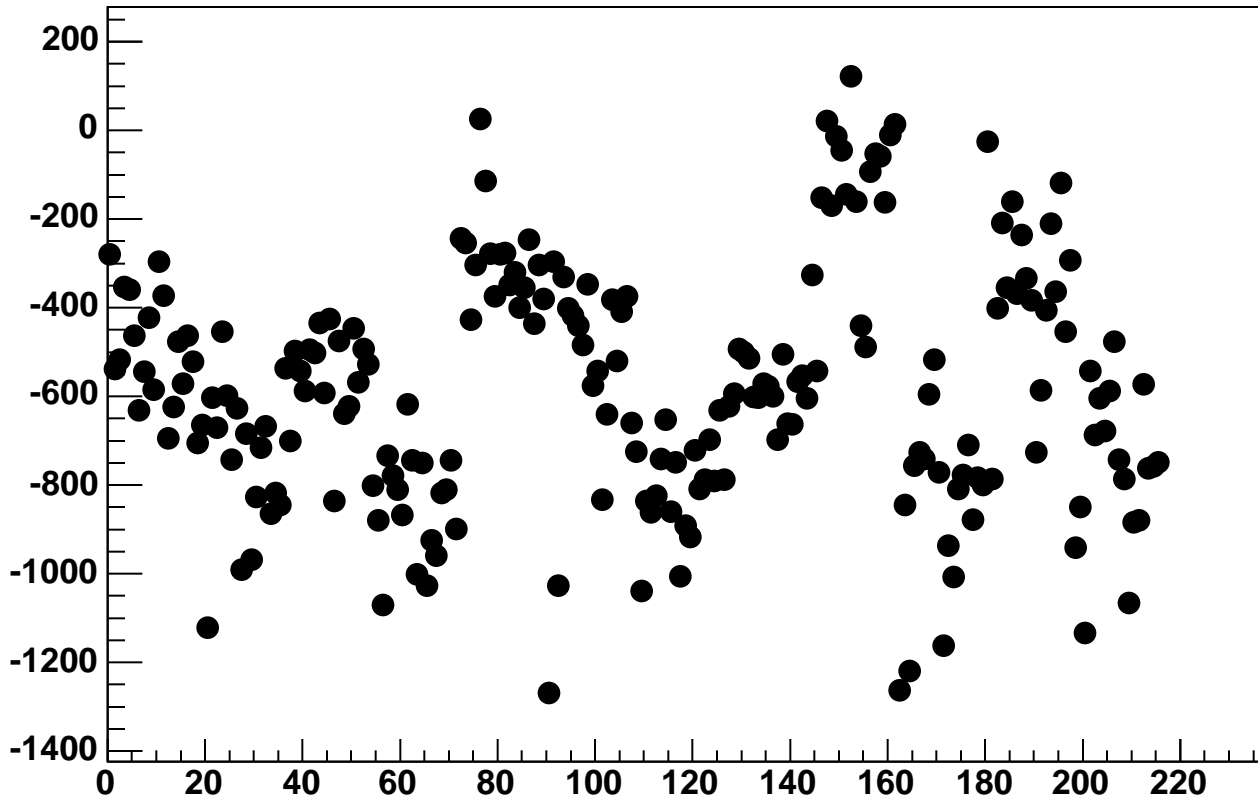
Enable 3, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



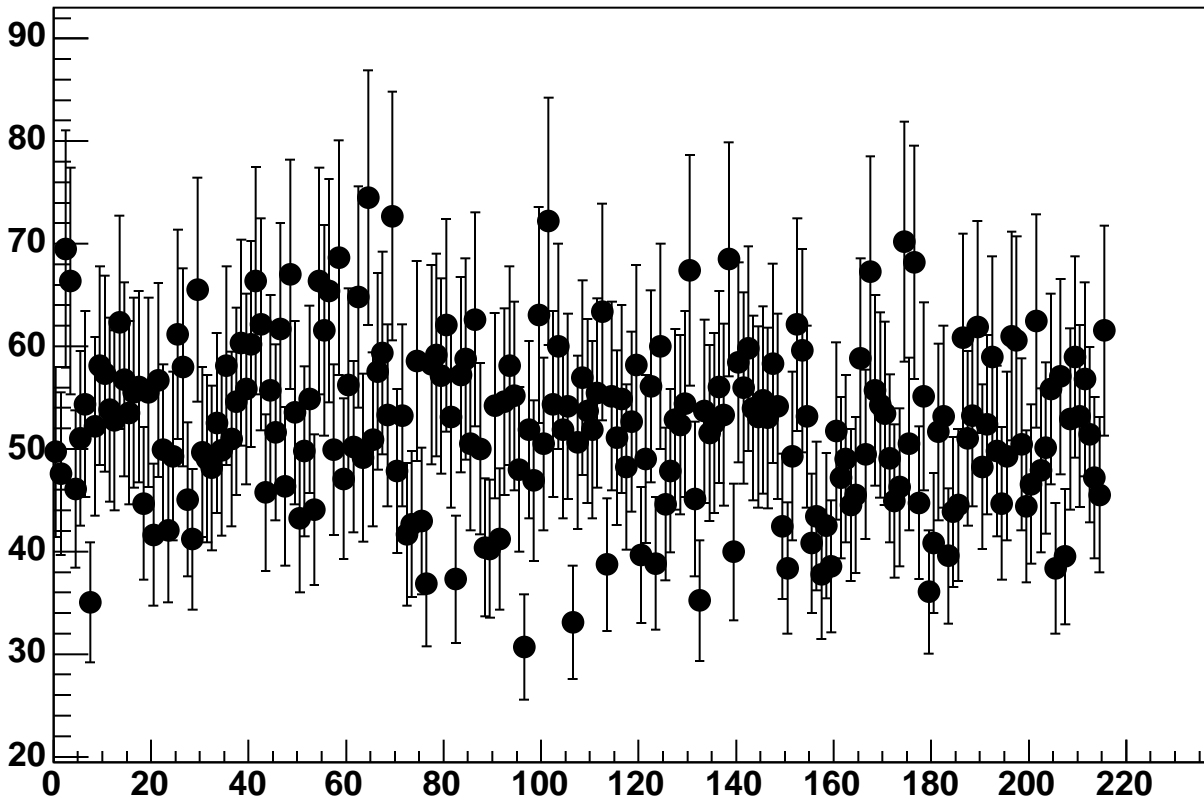
Enable 3, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



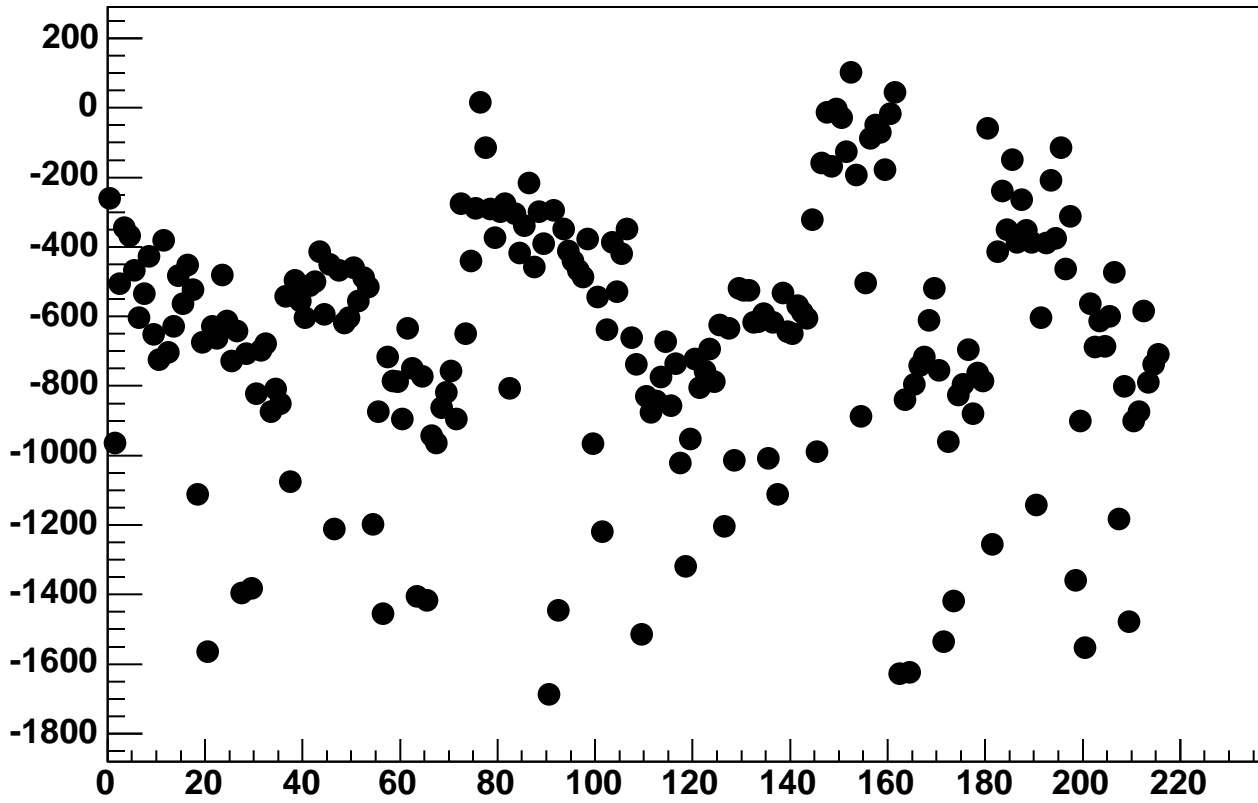
Enable 3, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan



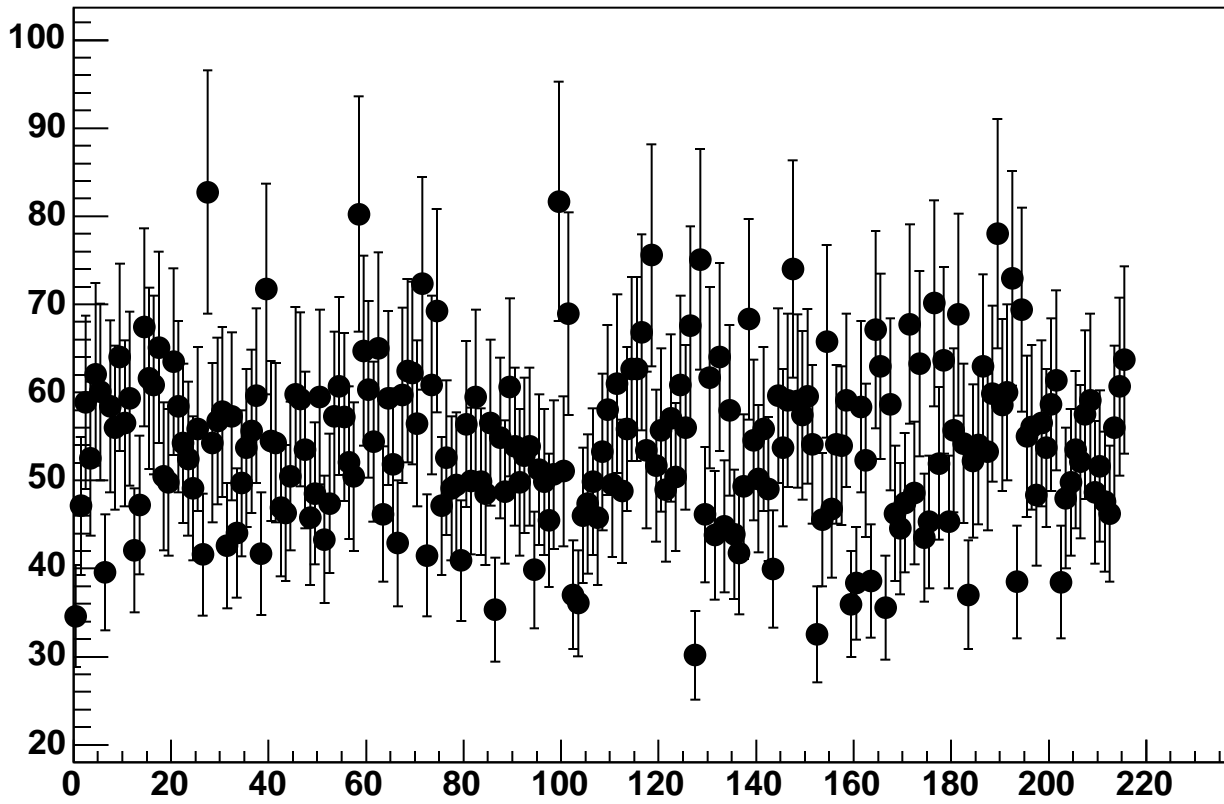
Enable 3, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan



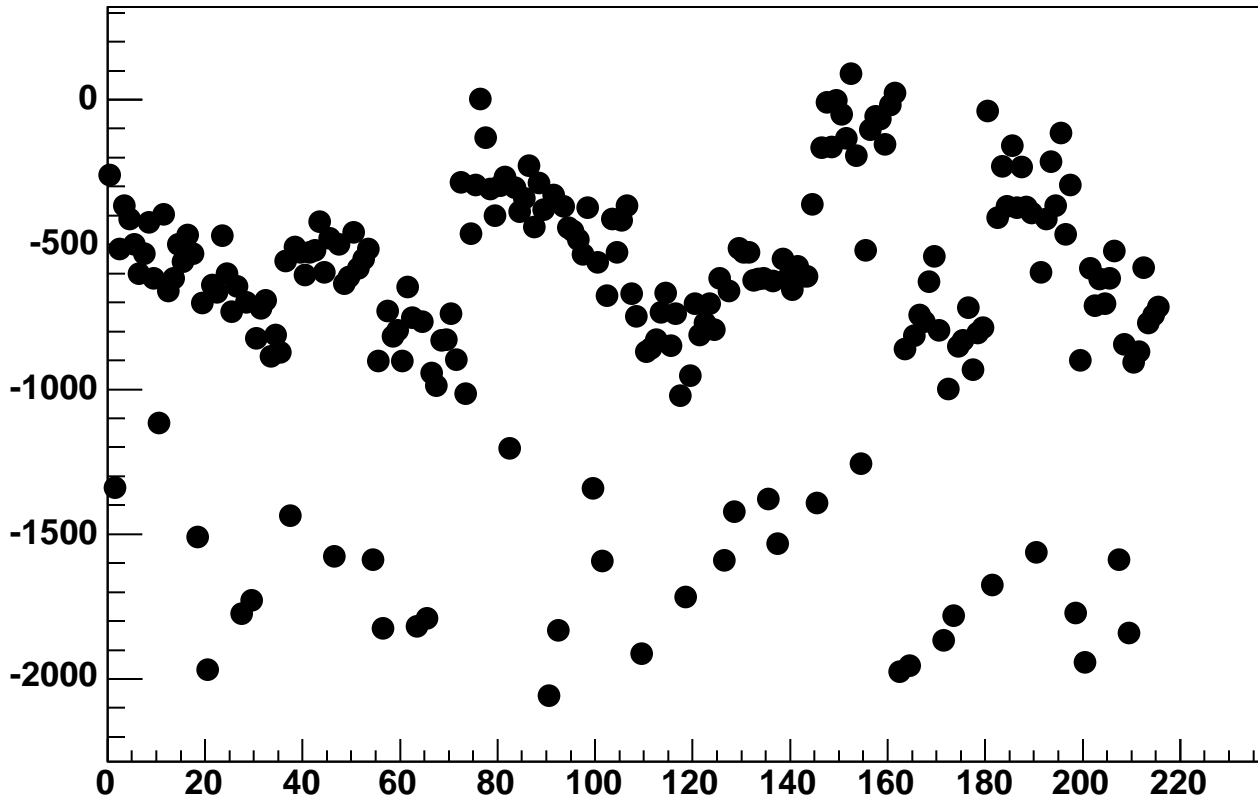
Enable 3, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



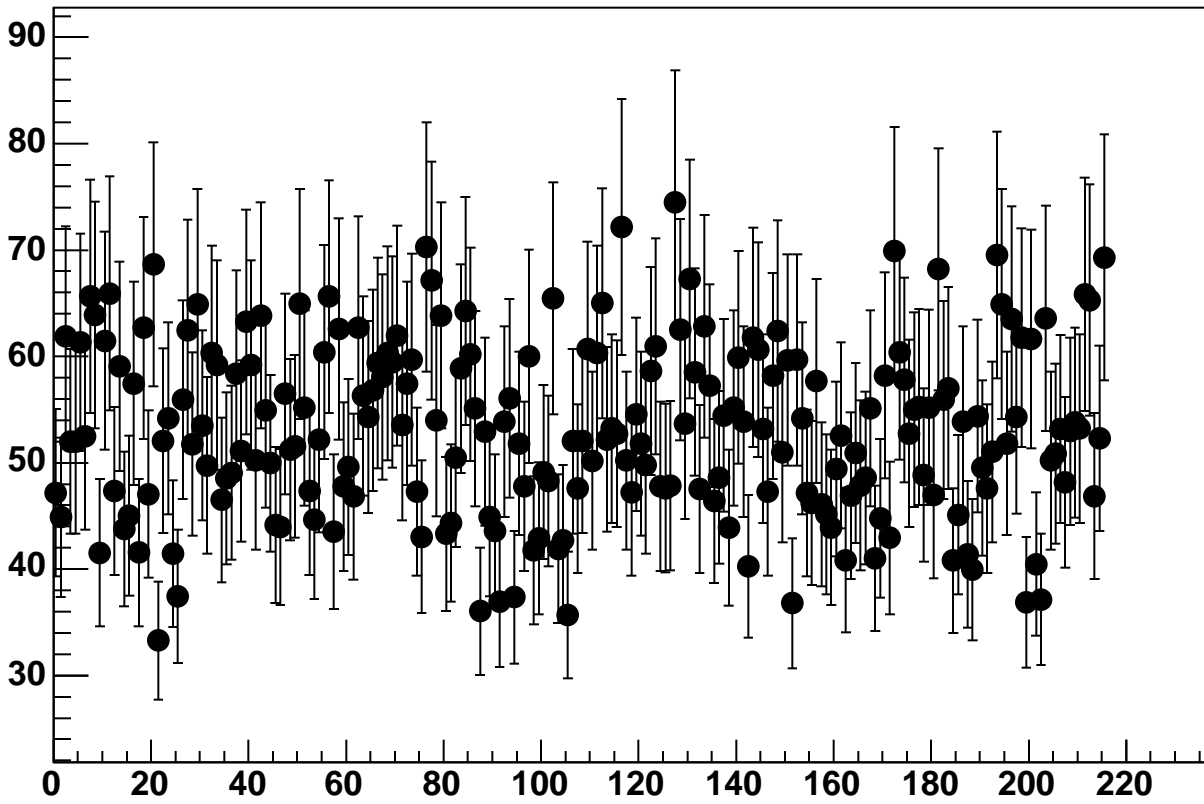
Enable 3, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan

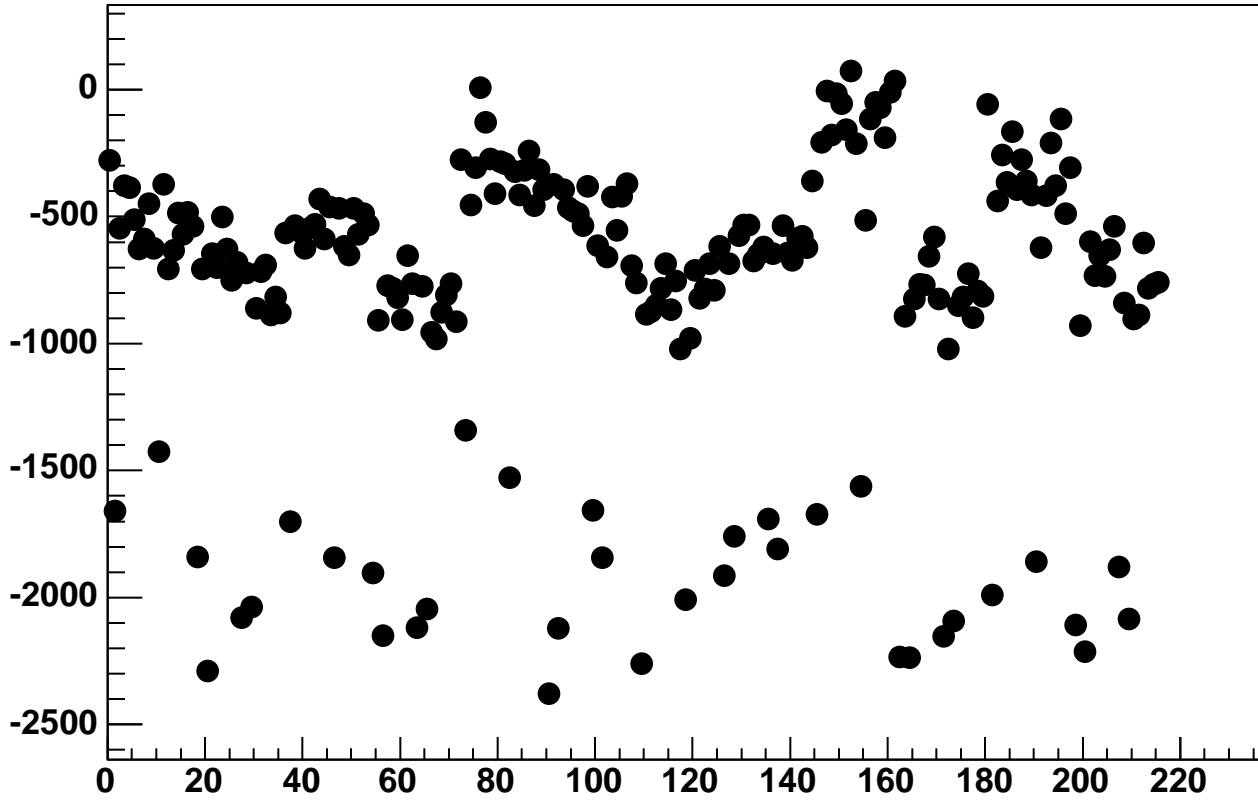


Enable 3, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan

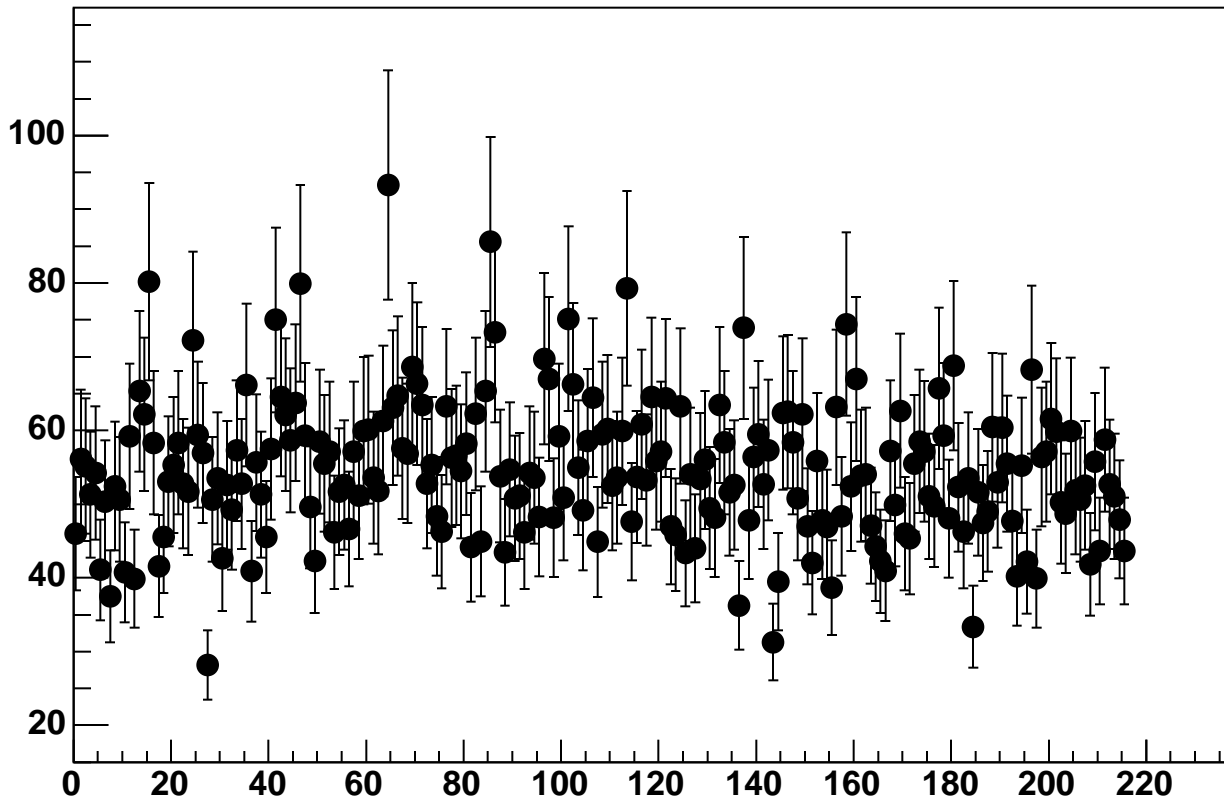




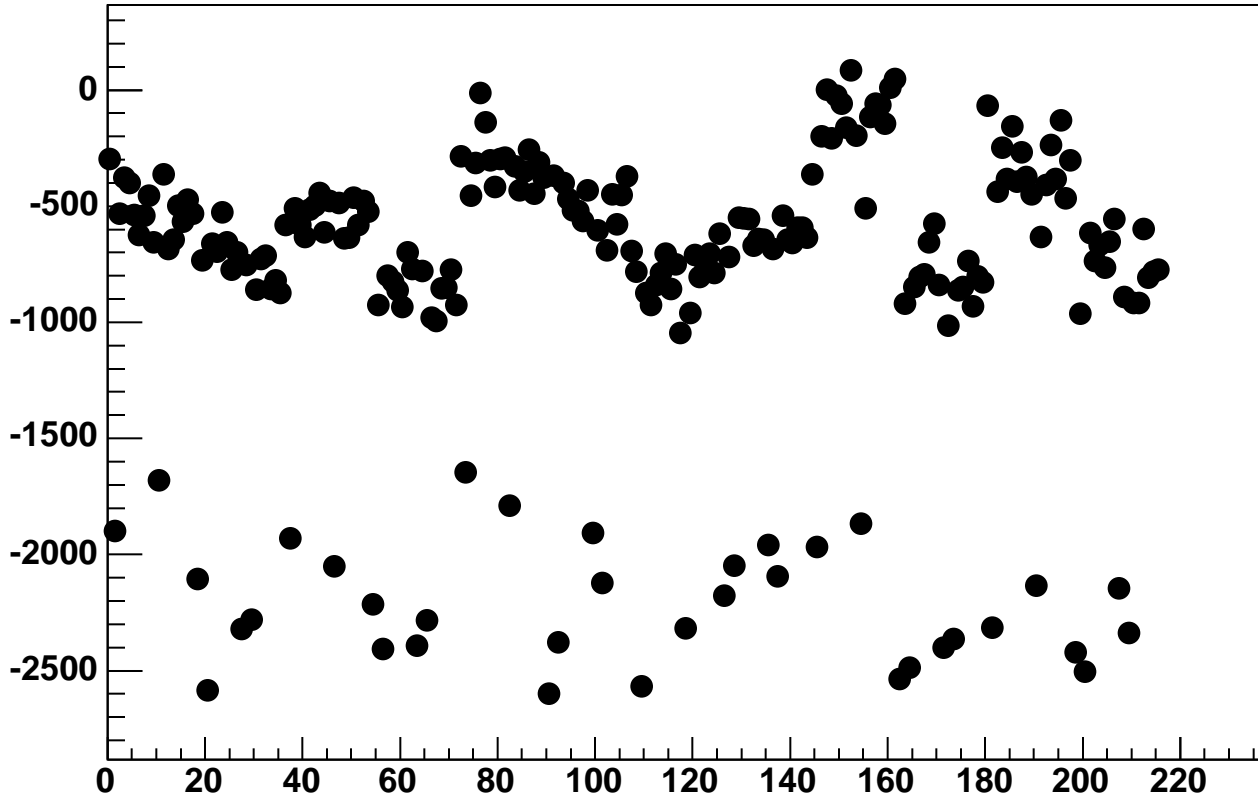
Enable 3, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



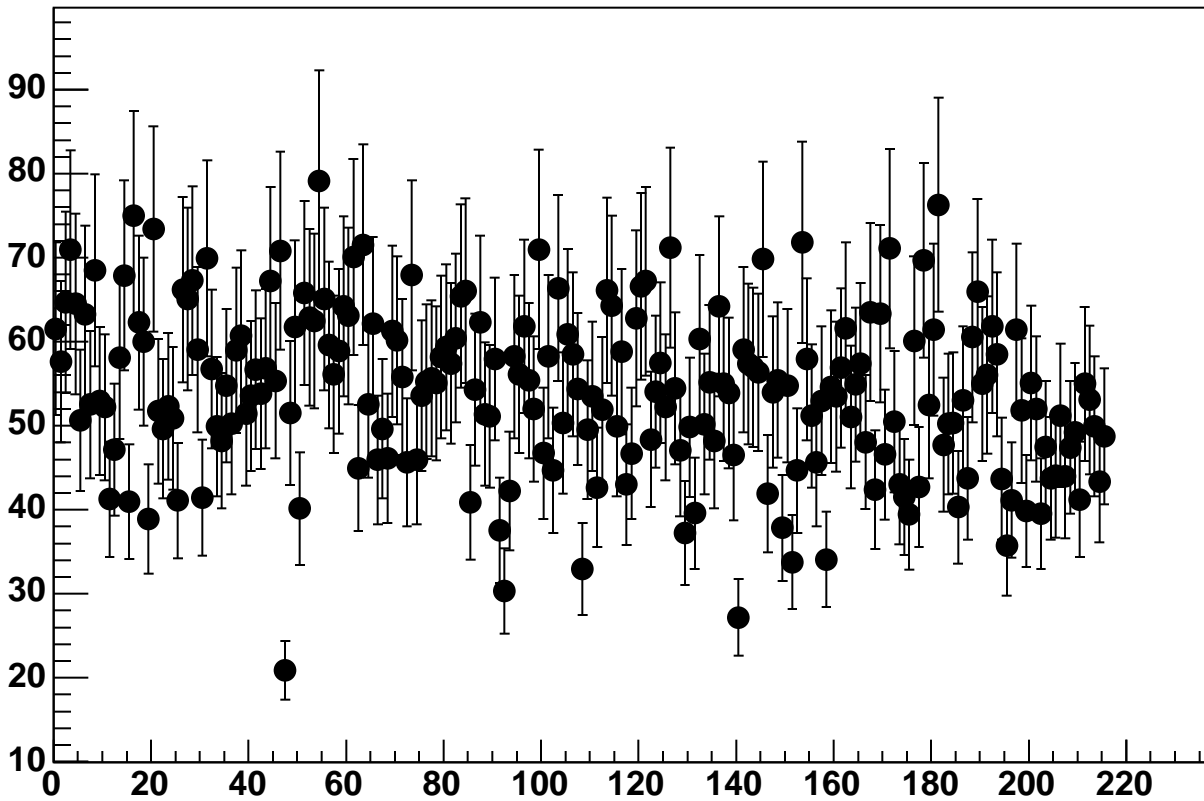
Enable 3, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



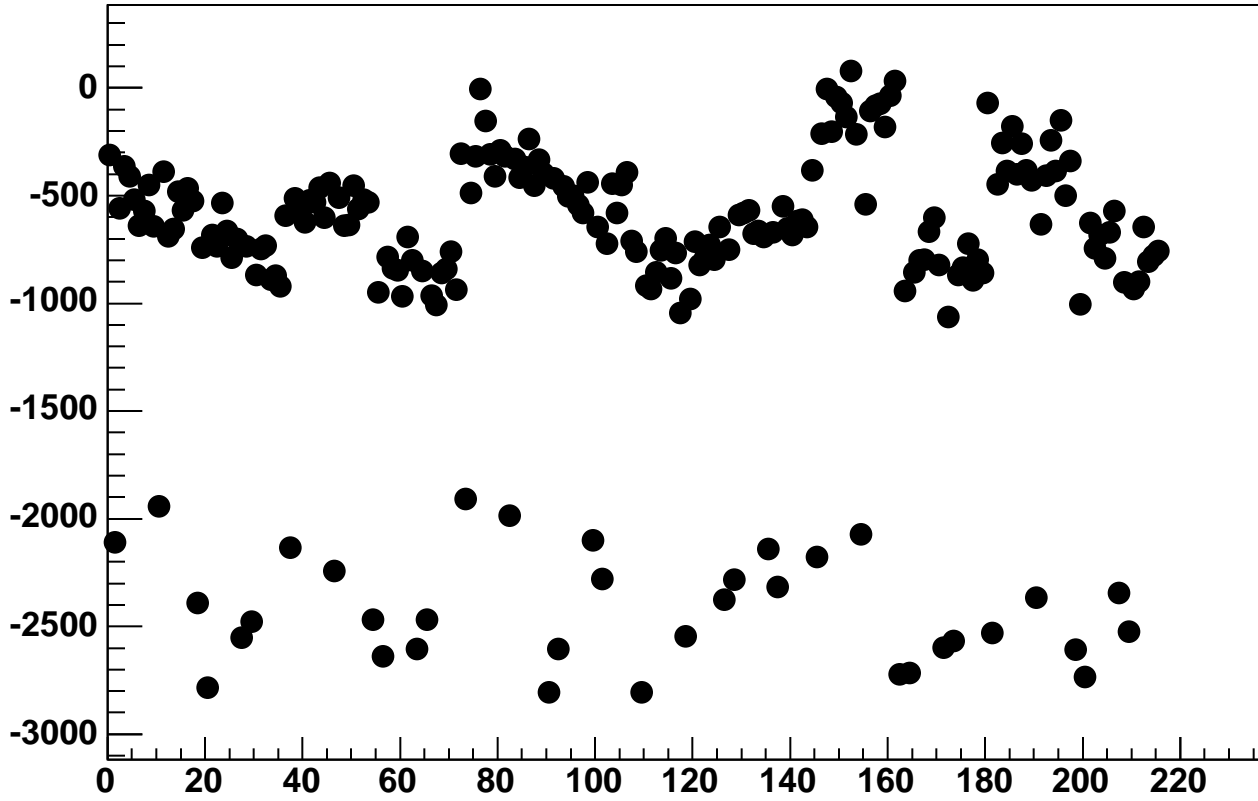
Enable 3, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan



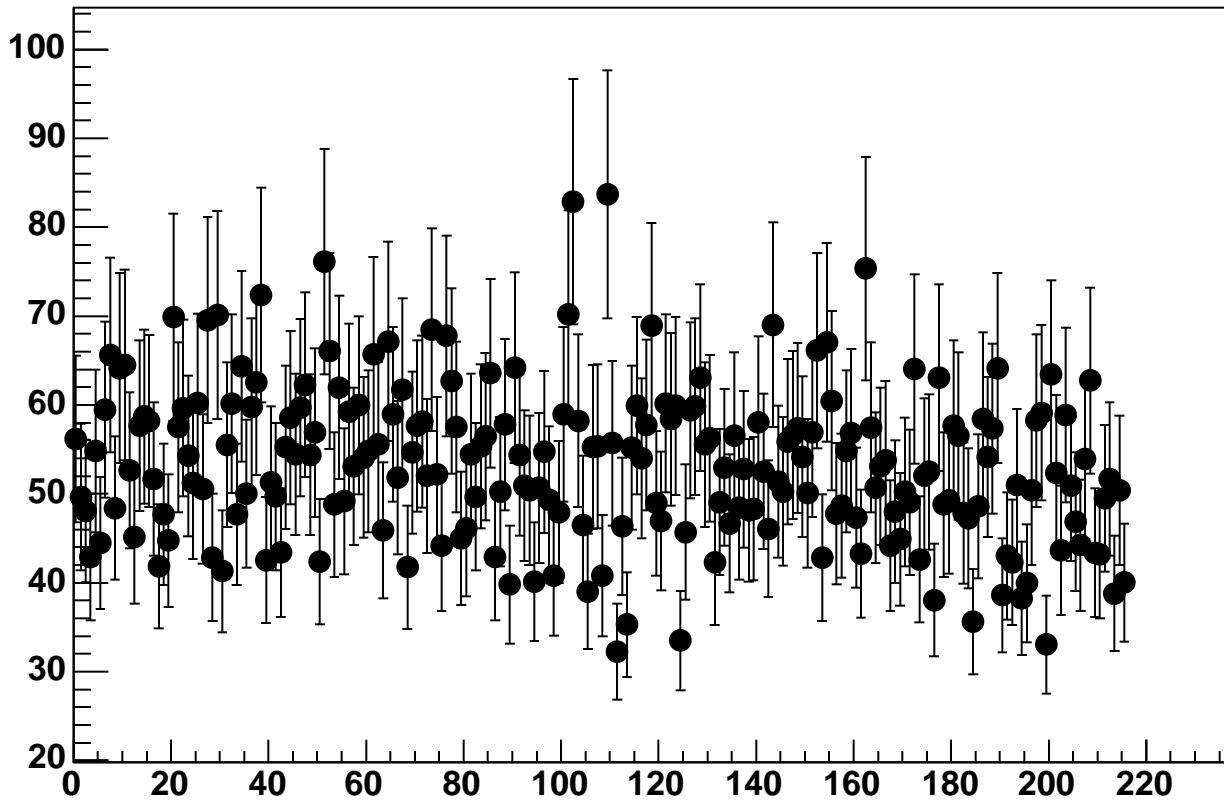
Enable 3, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan



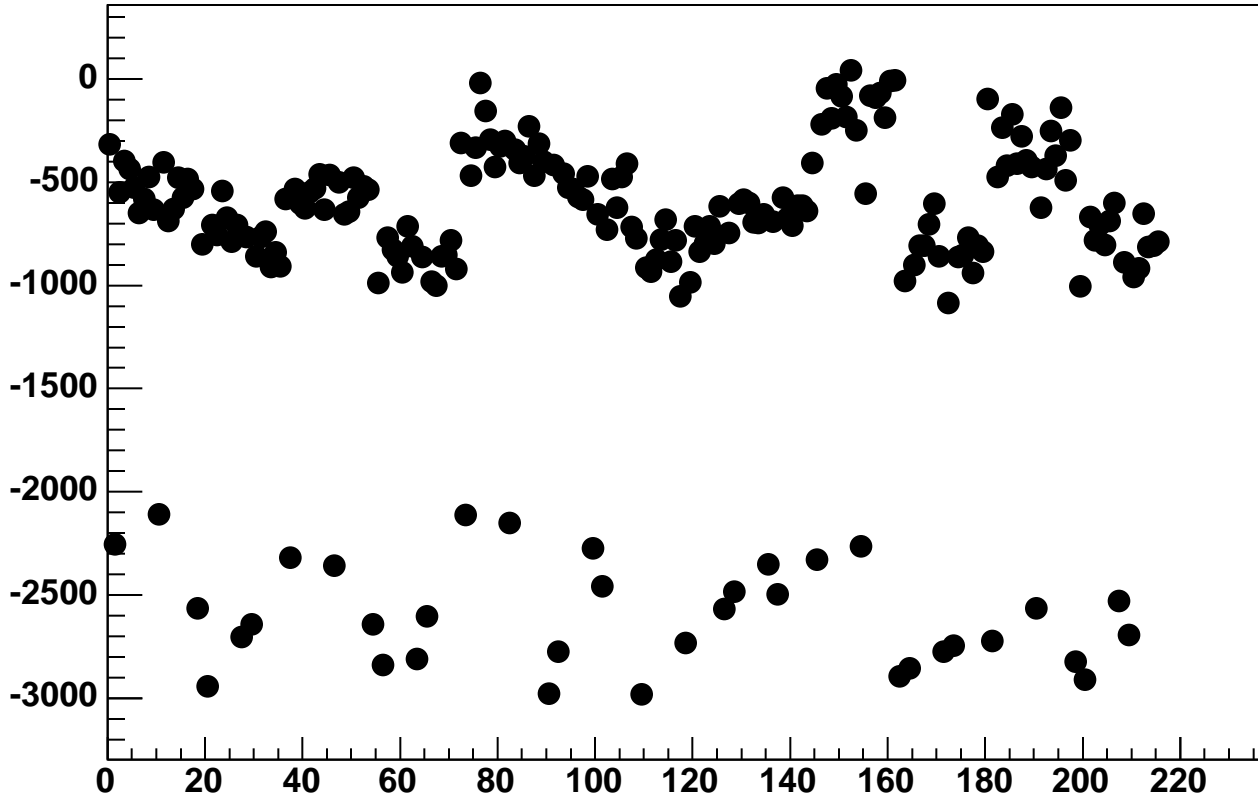
Enable 3, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



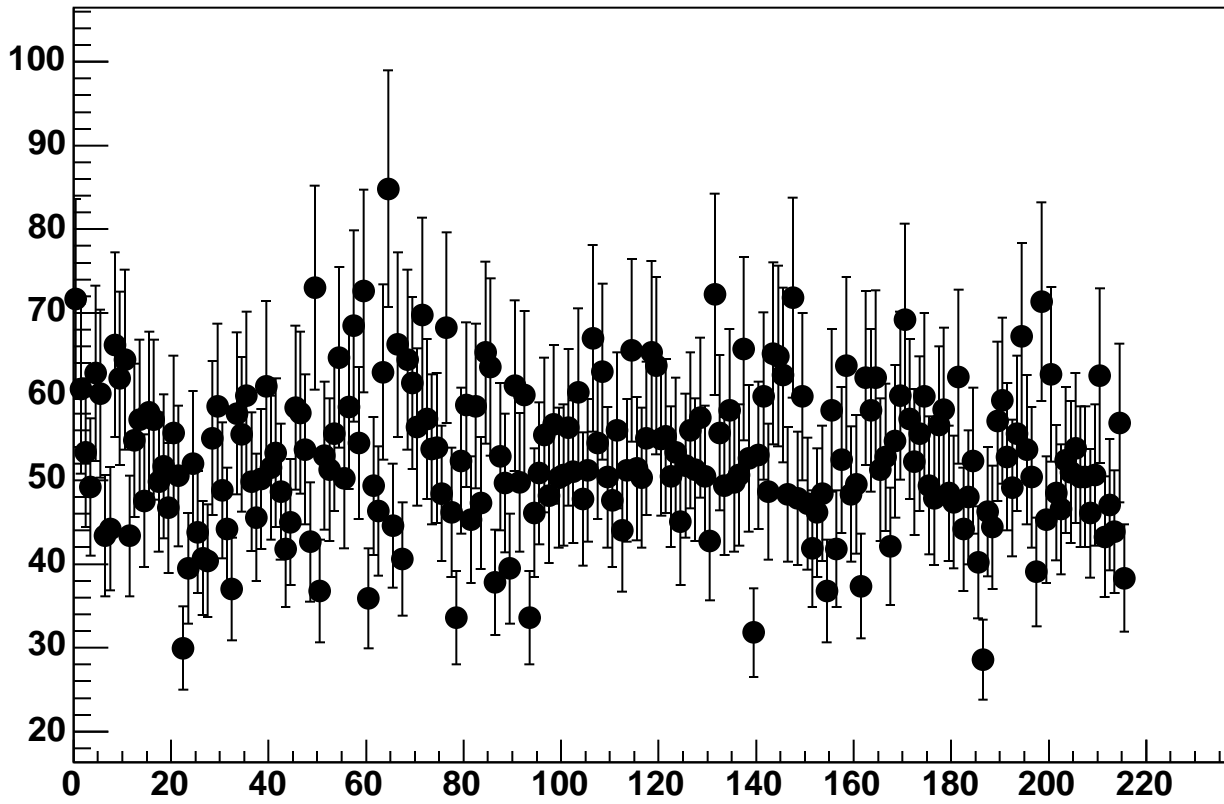
Enable 3, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



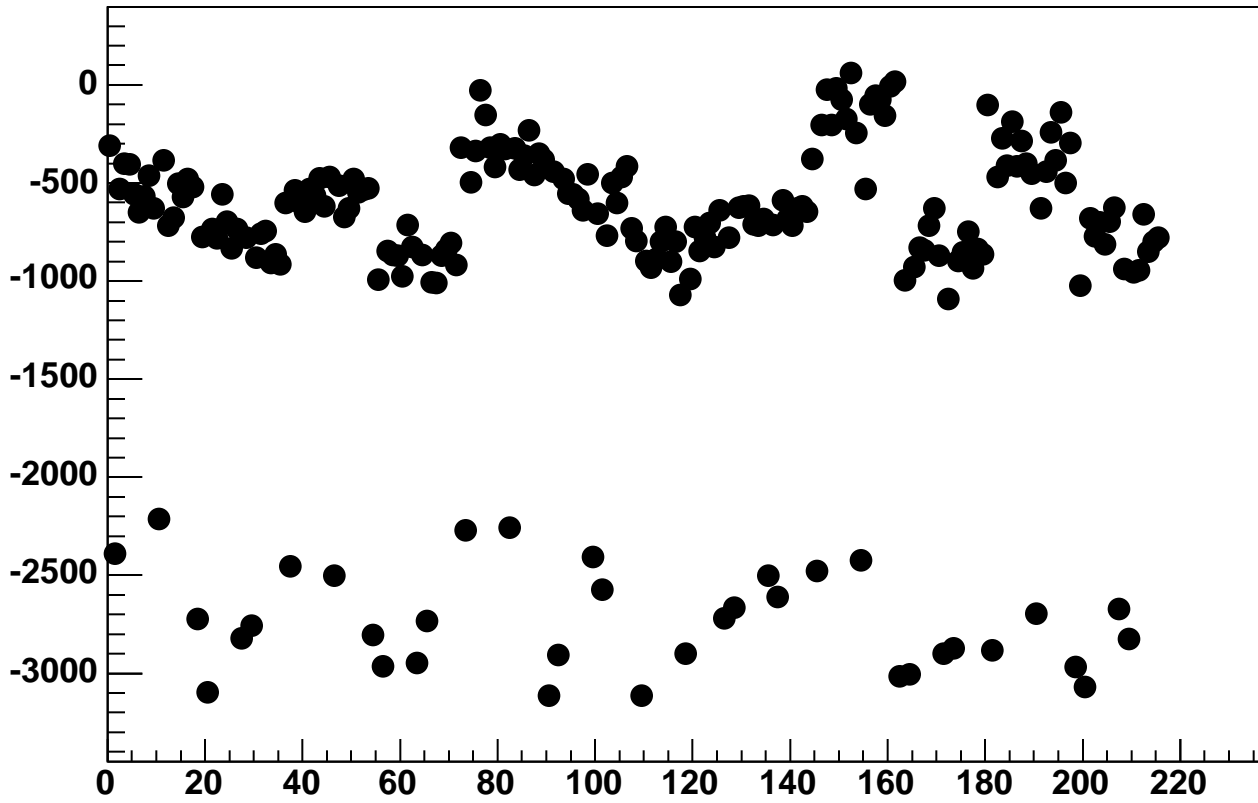
Enable 3, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan



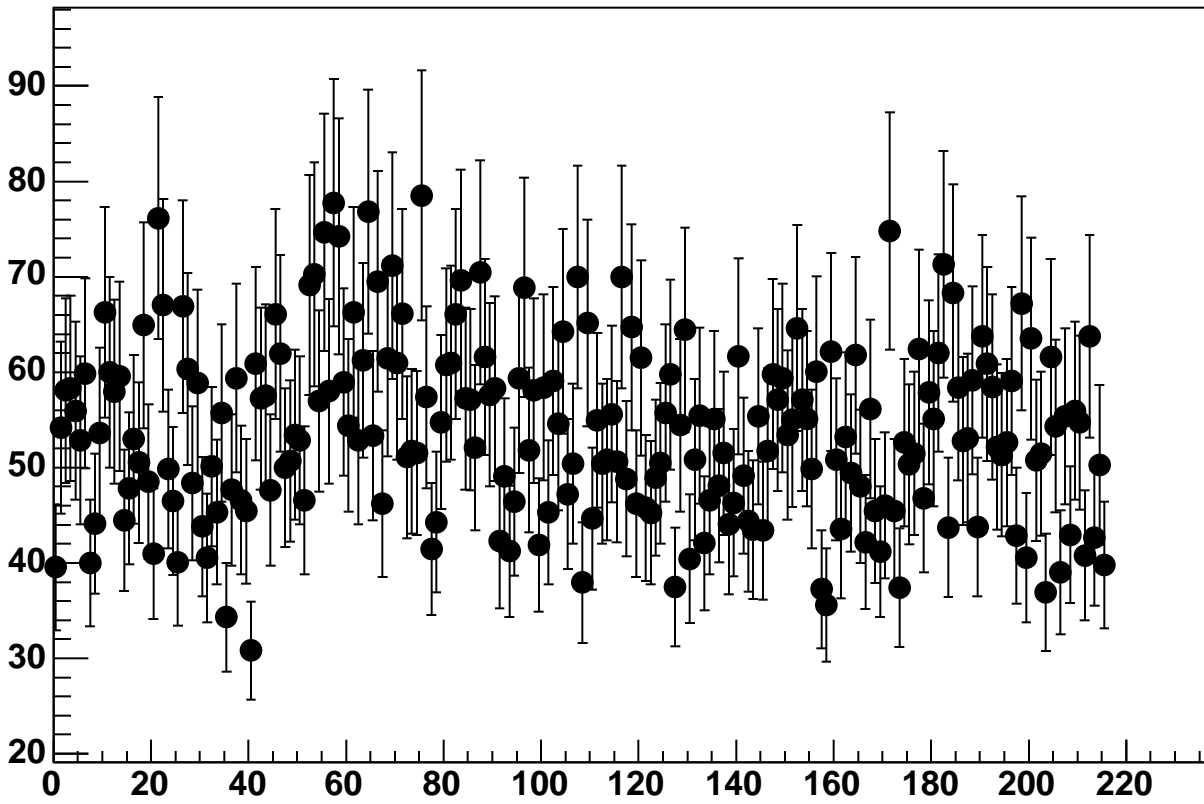
Enable 3, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan



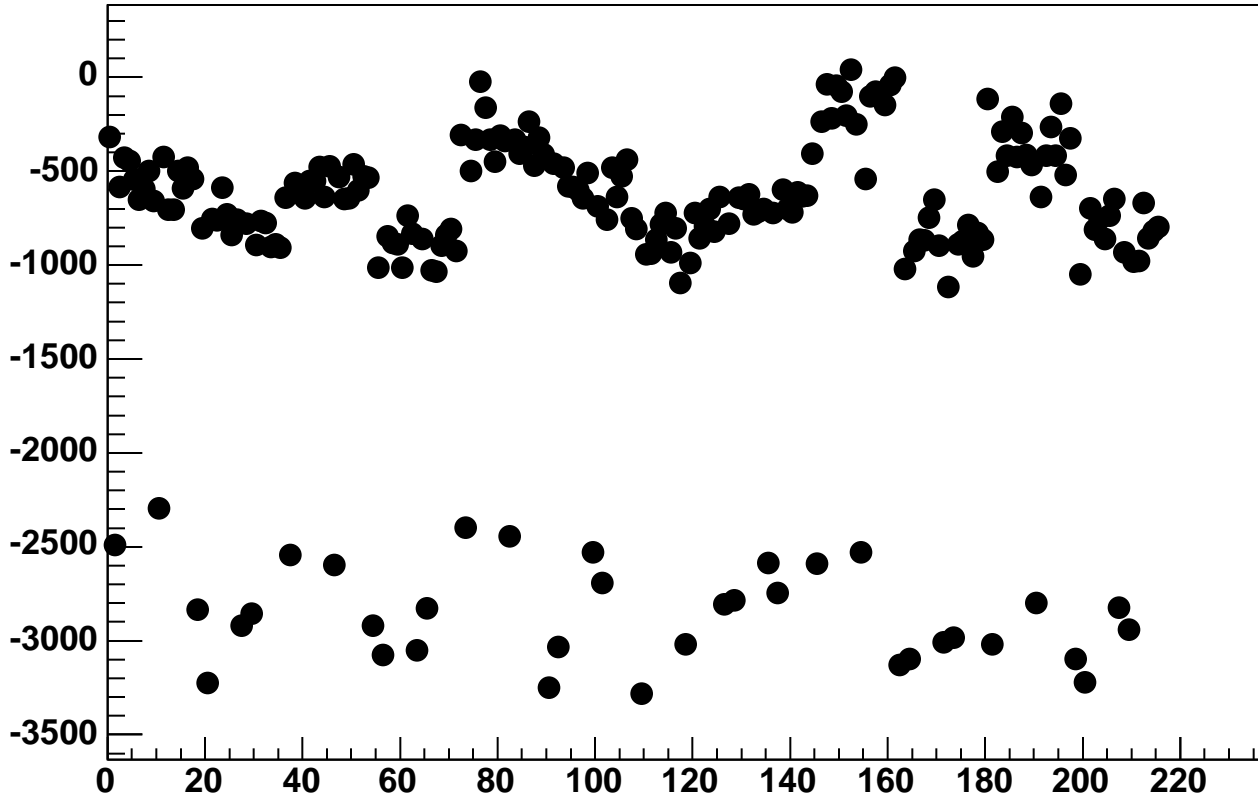
Enable 3, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



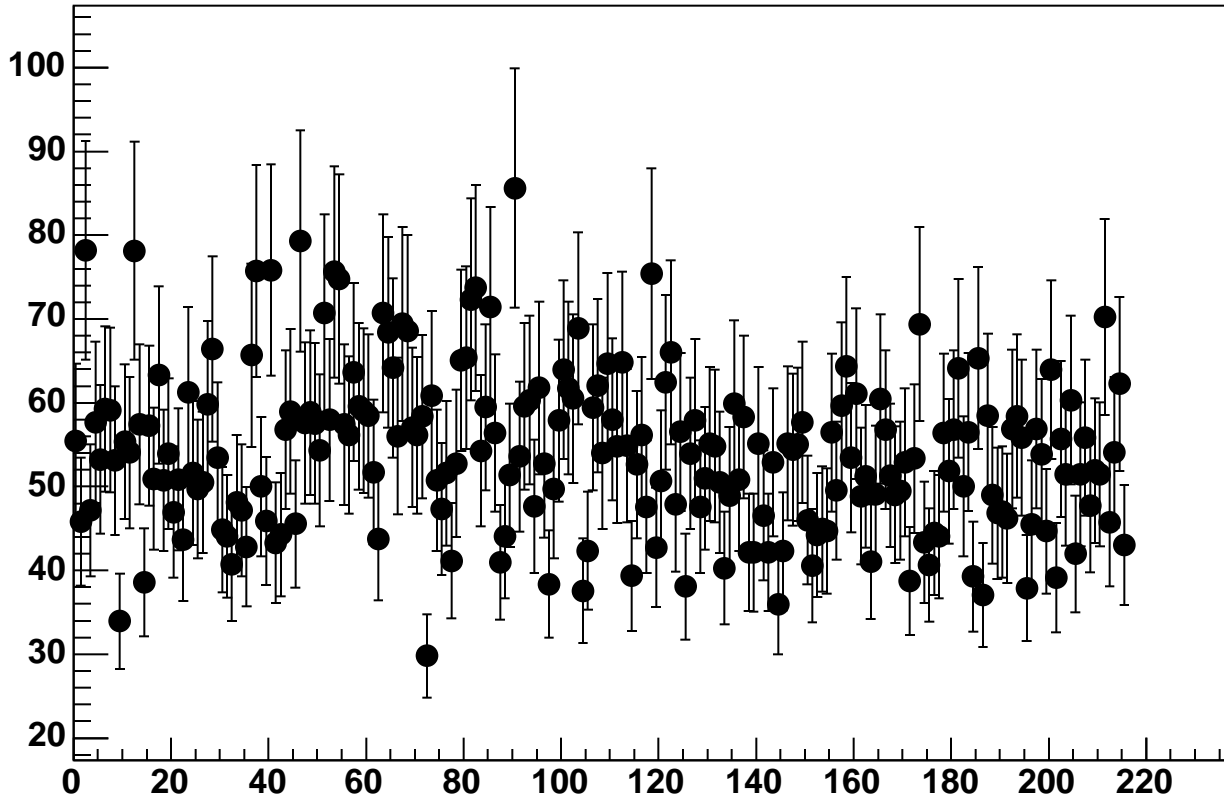
Enable 3, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



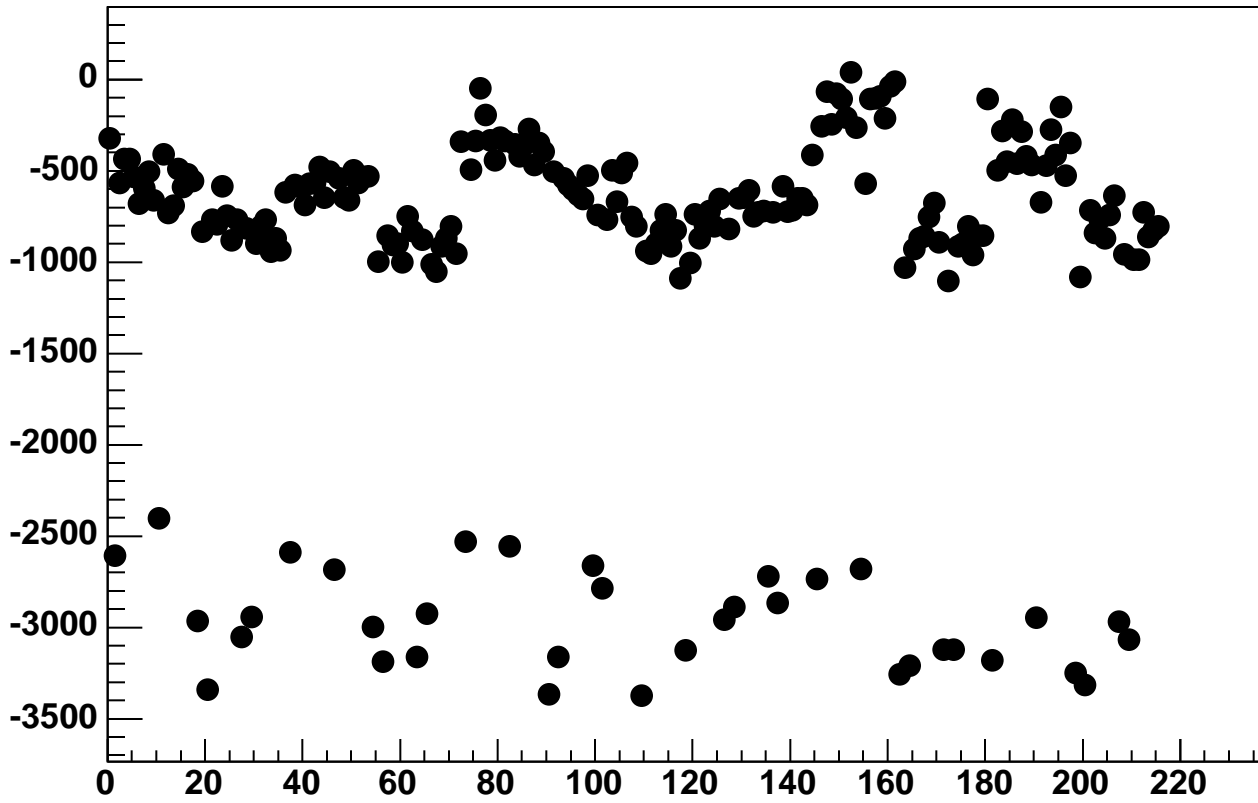
Enable 3, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan



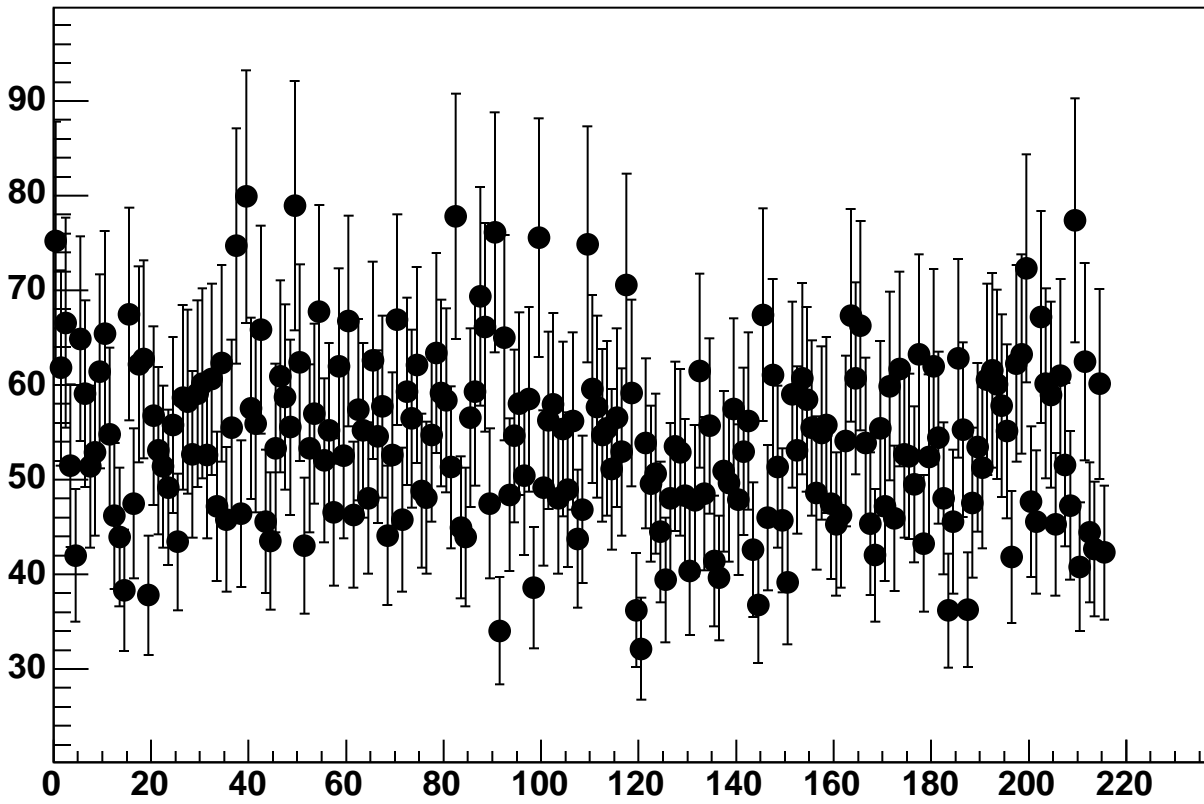
Enable 3, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan



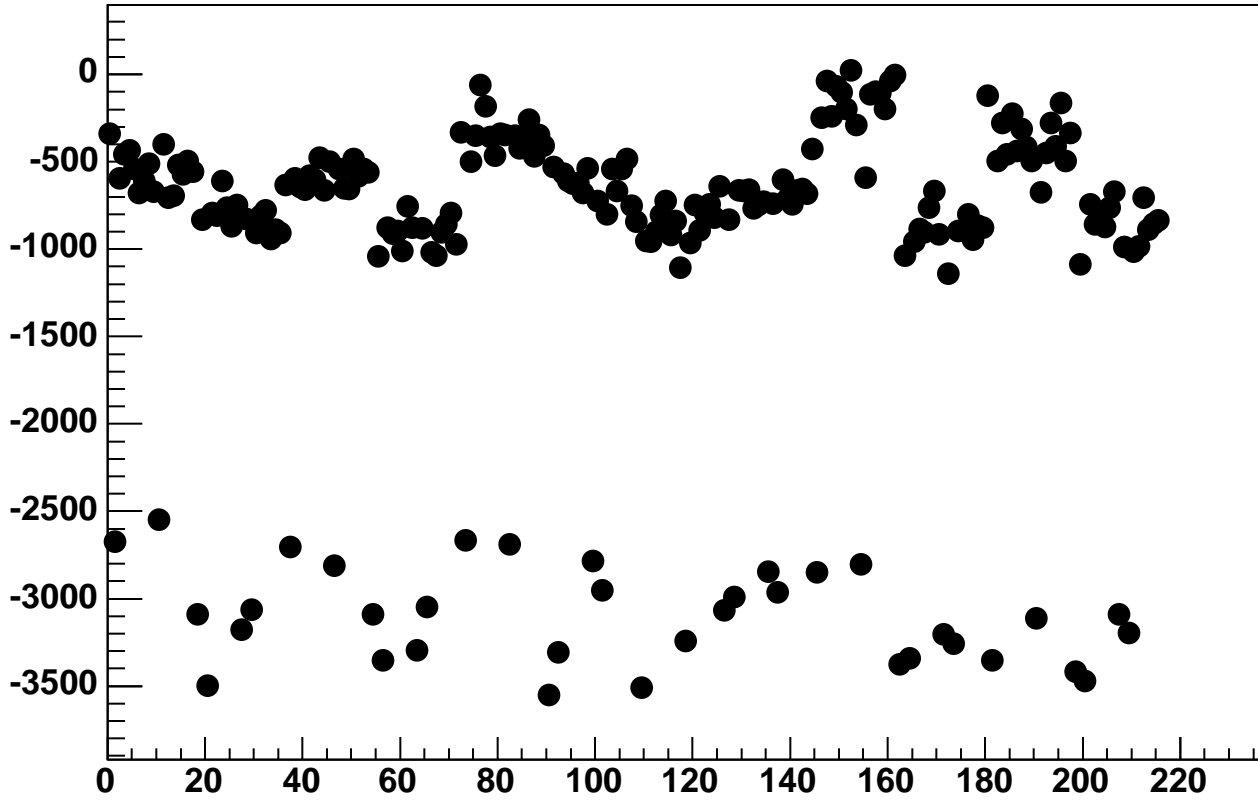
Enable 3, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



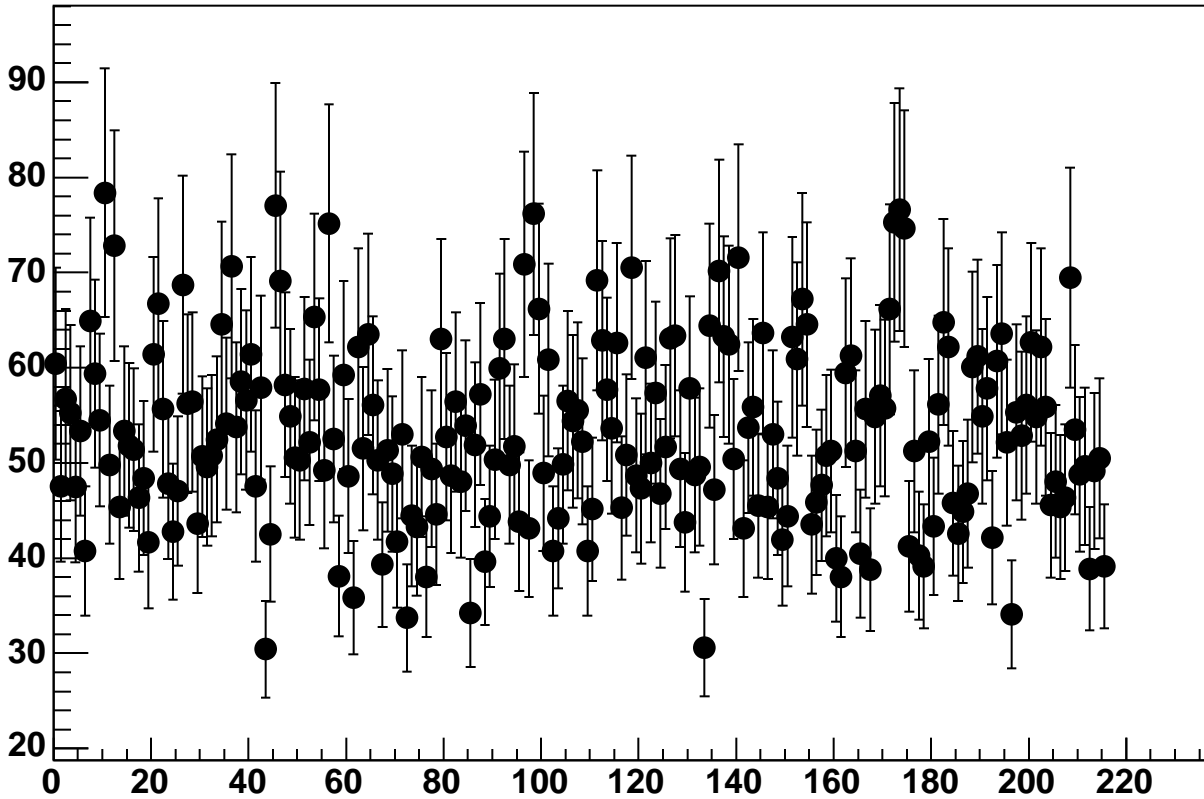
Enable 3, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan

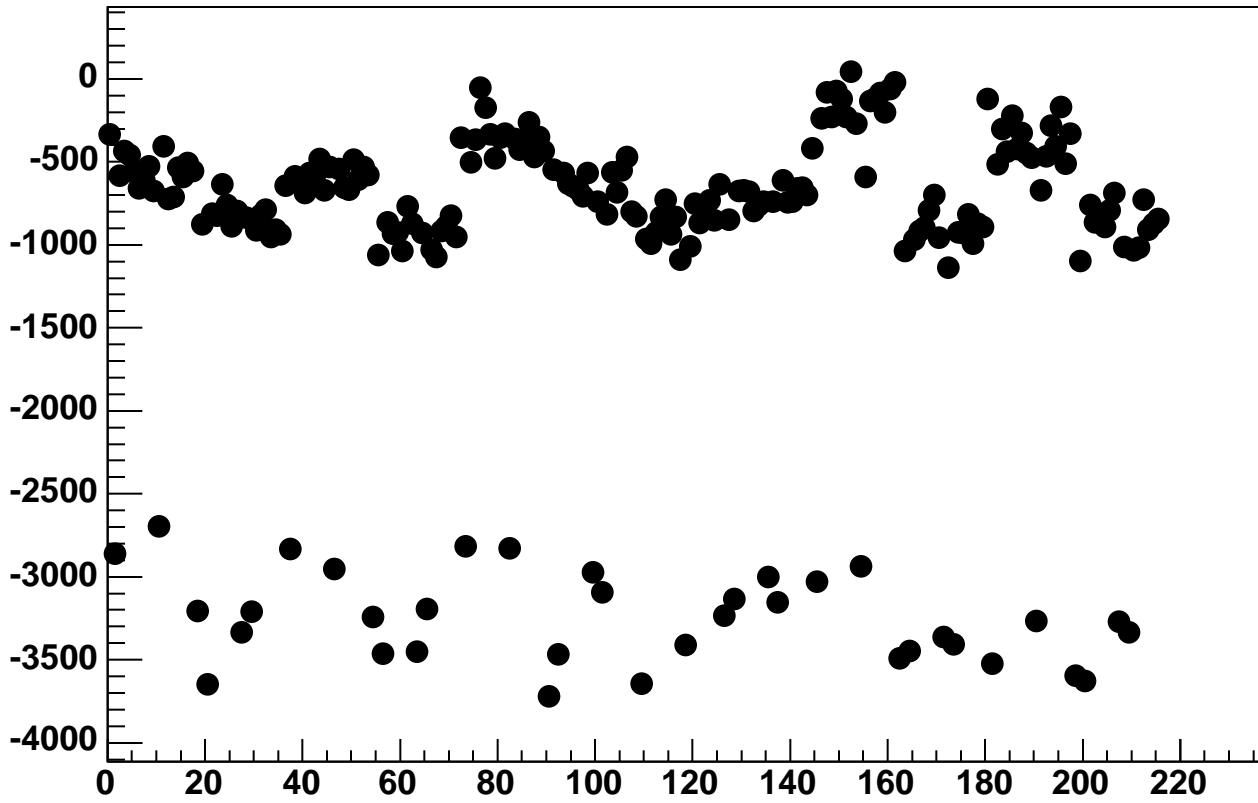


Enable 3, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan

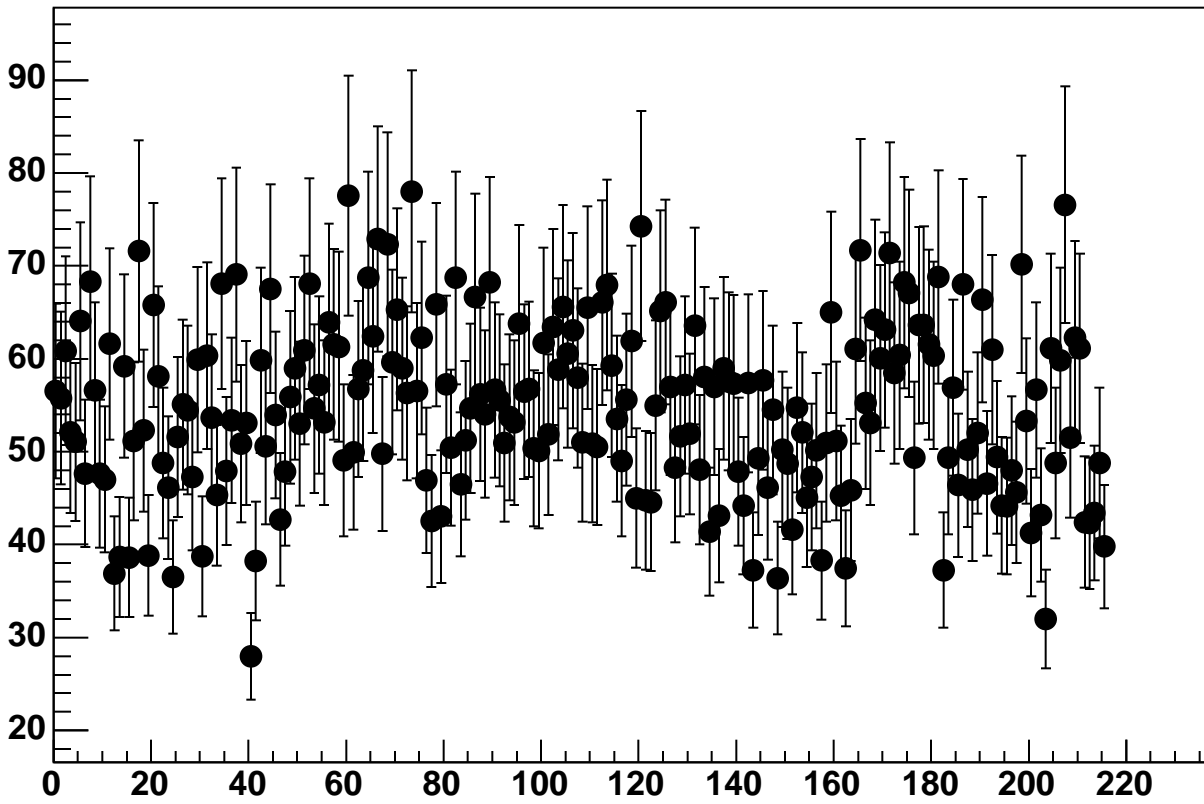




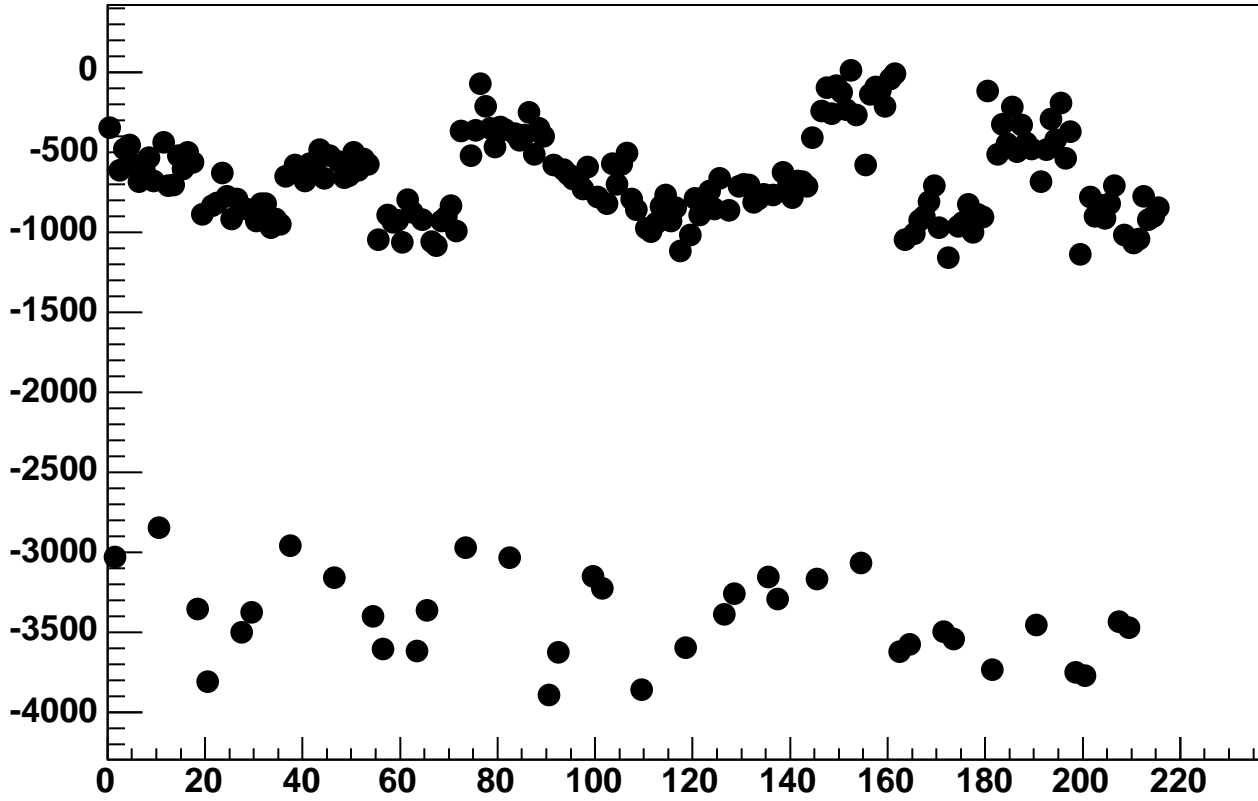
Enable 3, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



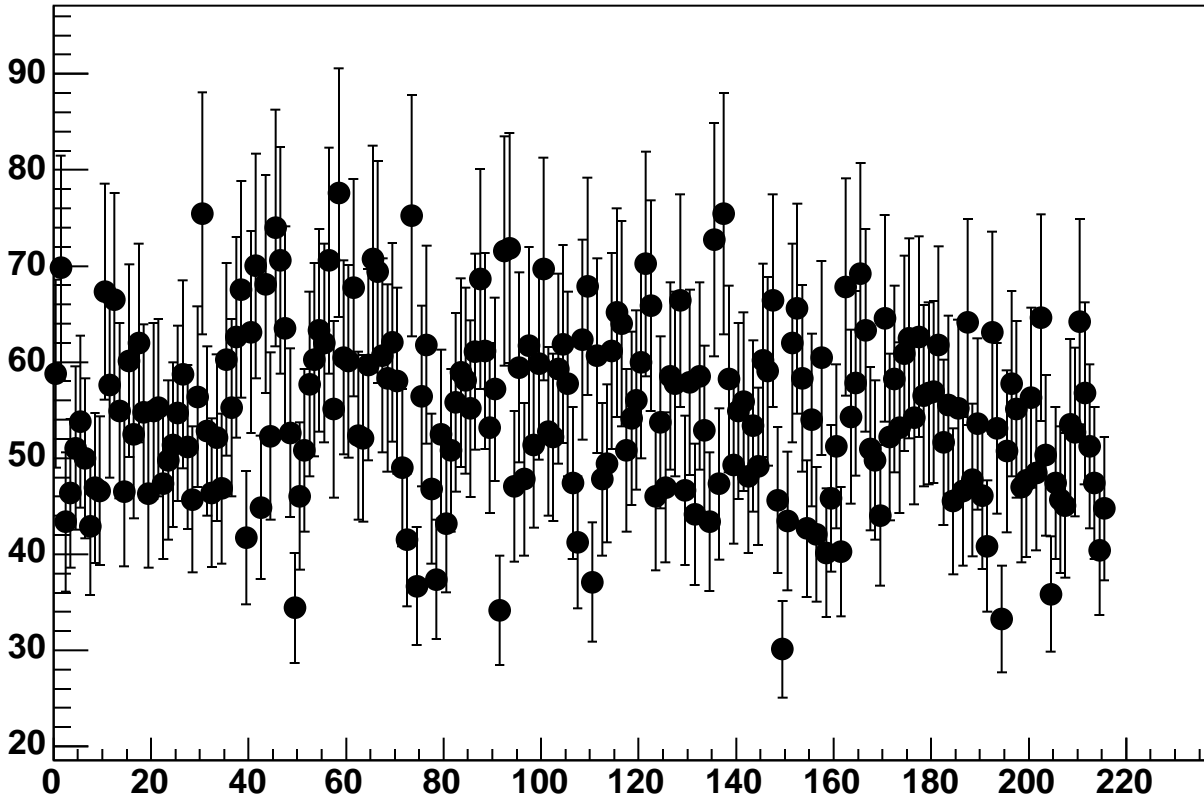
Enable 3, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



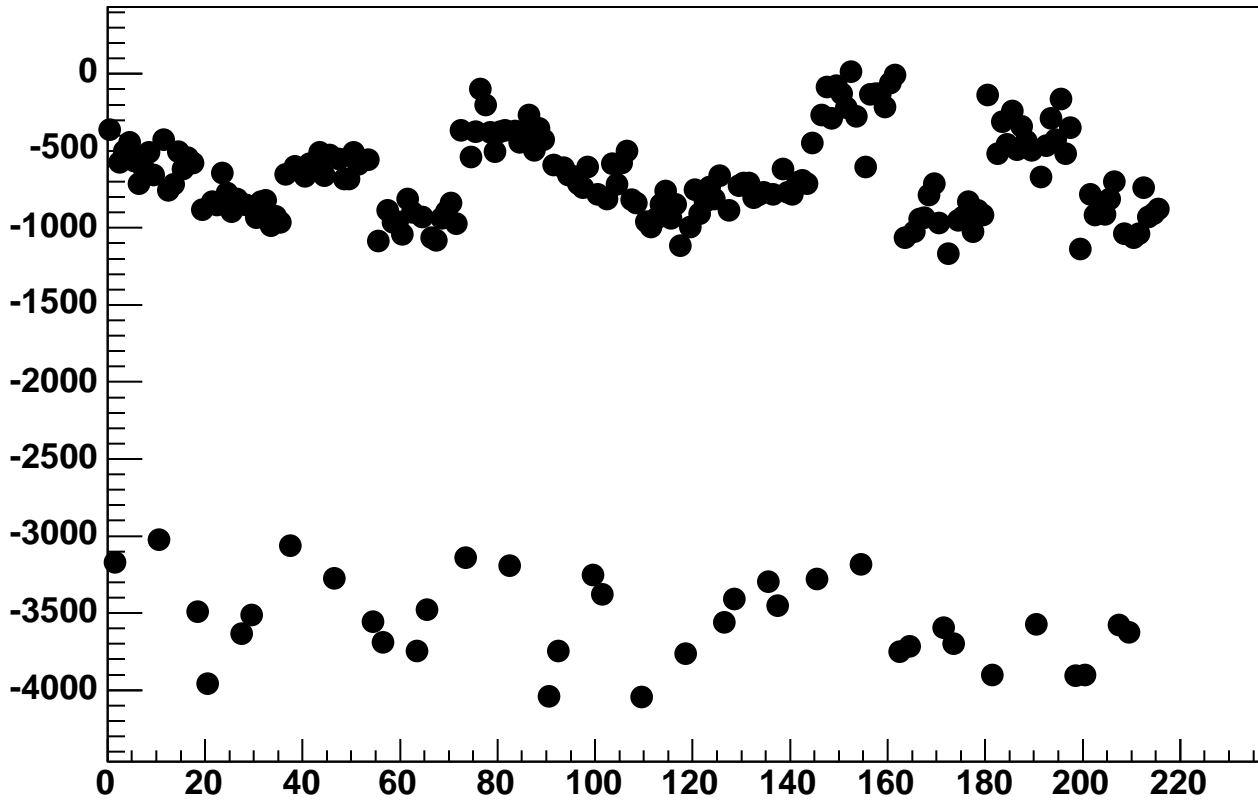
Enable 3, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan



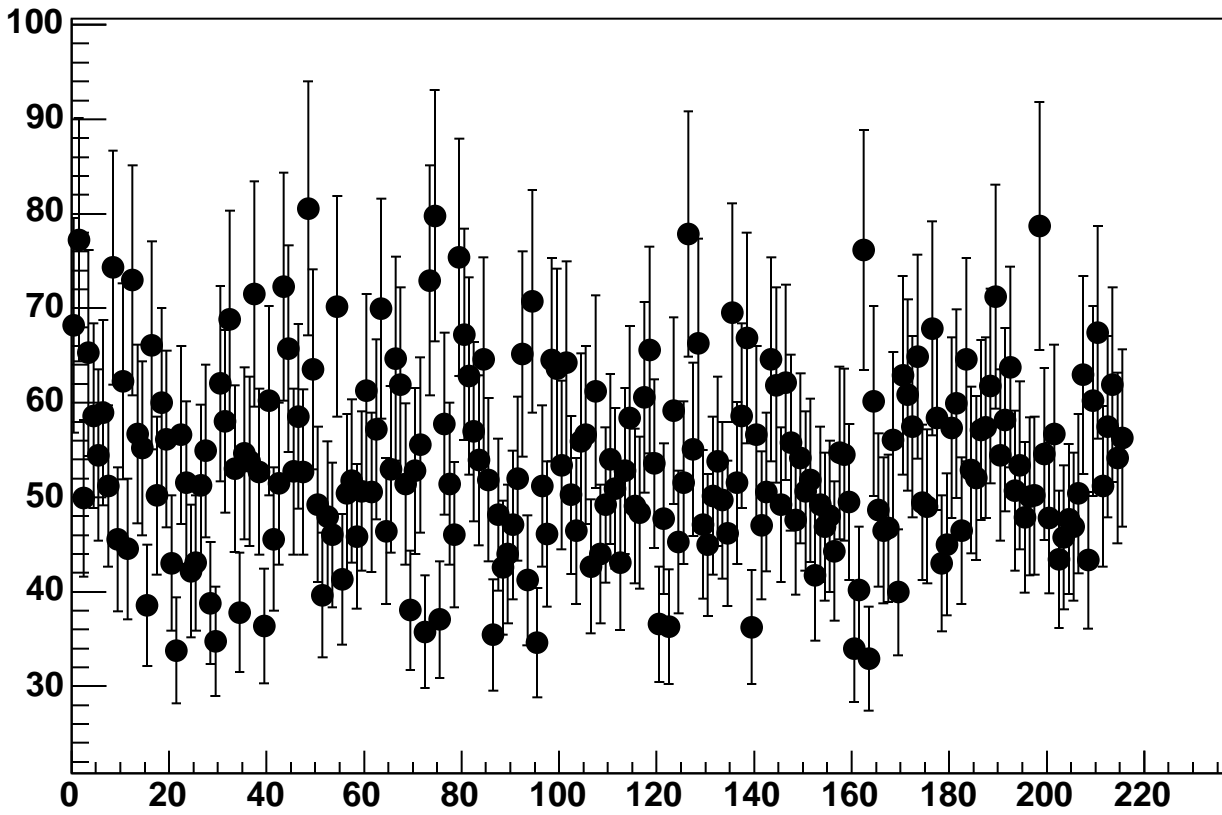
Enable 3, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan



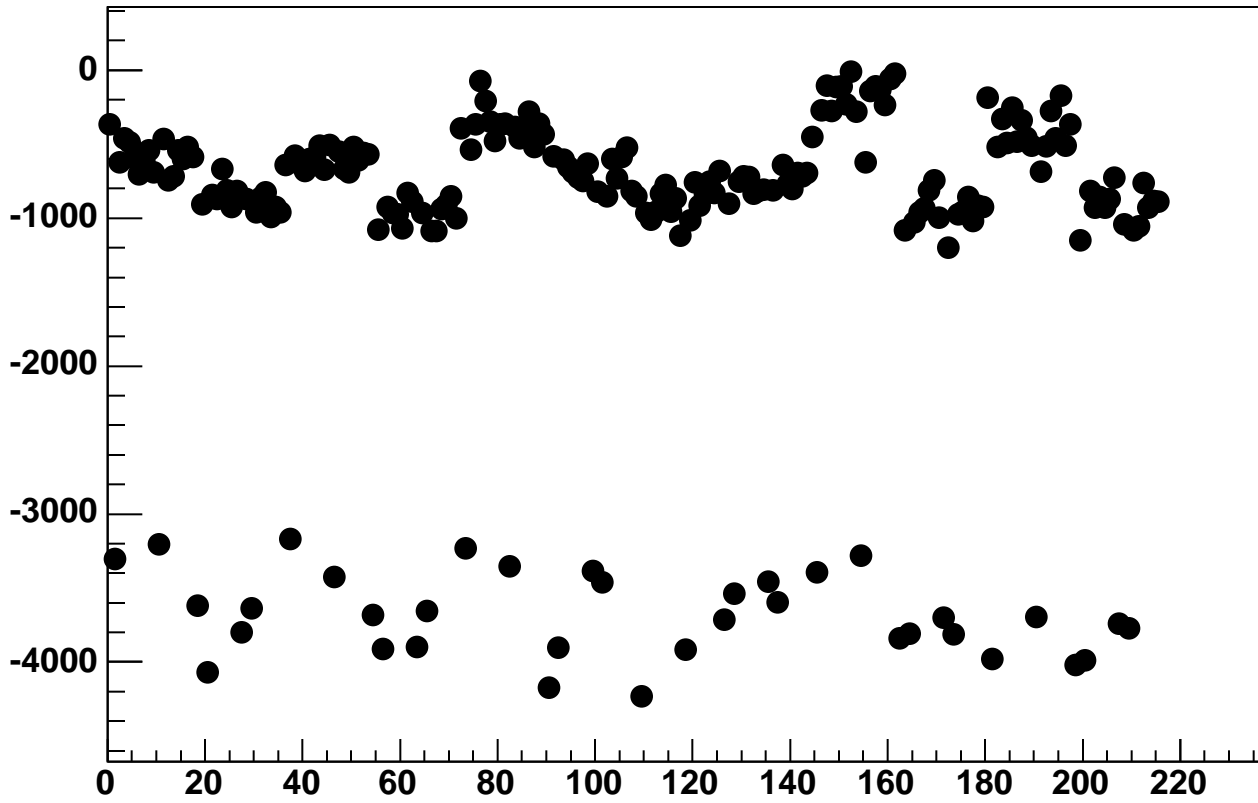
Enable 3, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



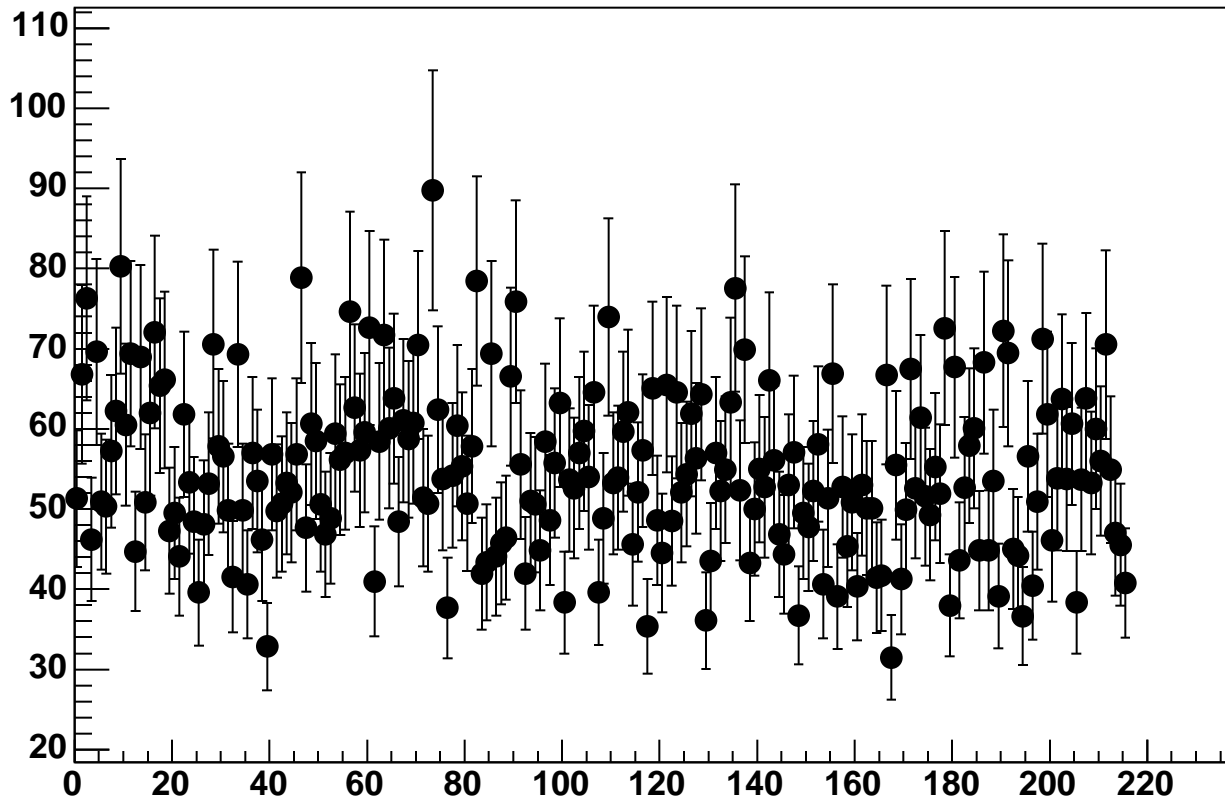
Enable 3, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



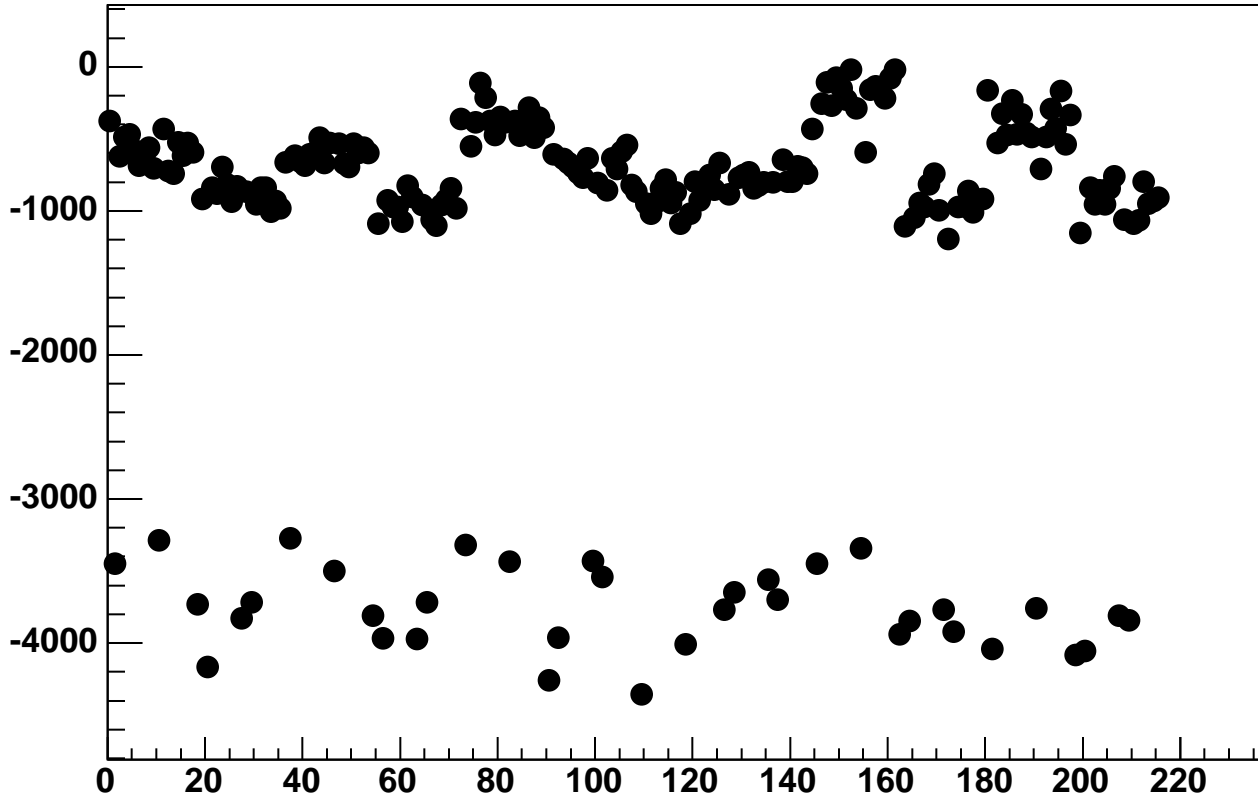
Enable 3, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan



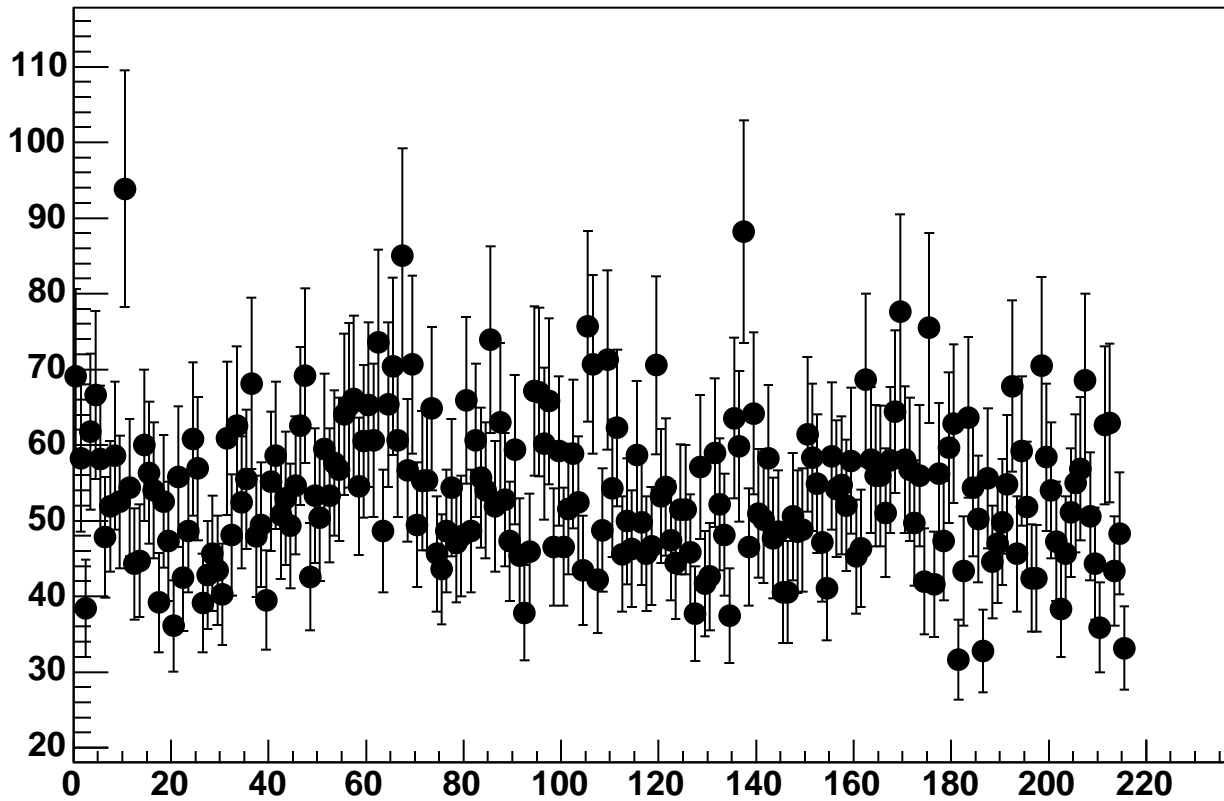
Enable 3, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan



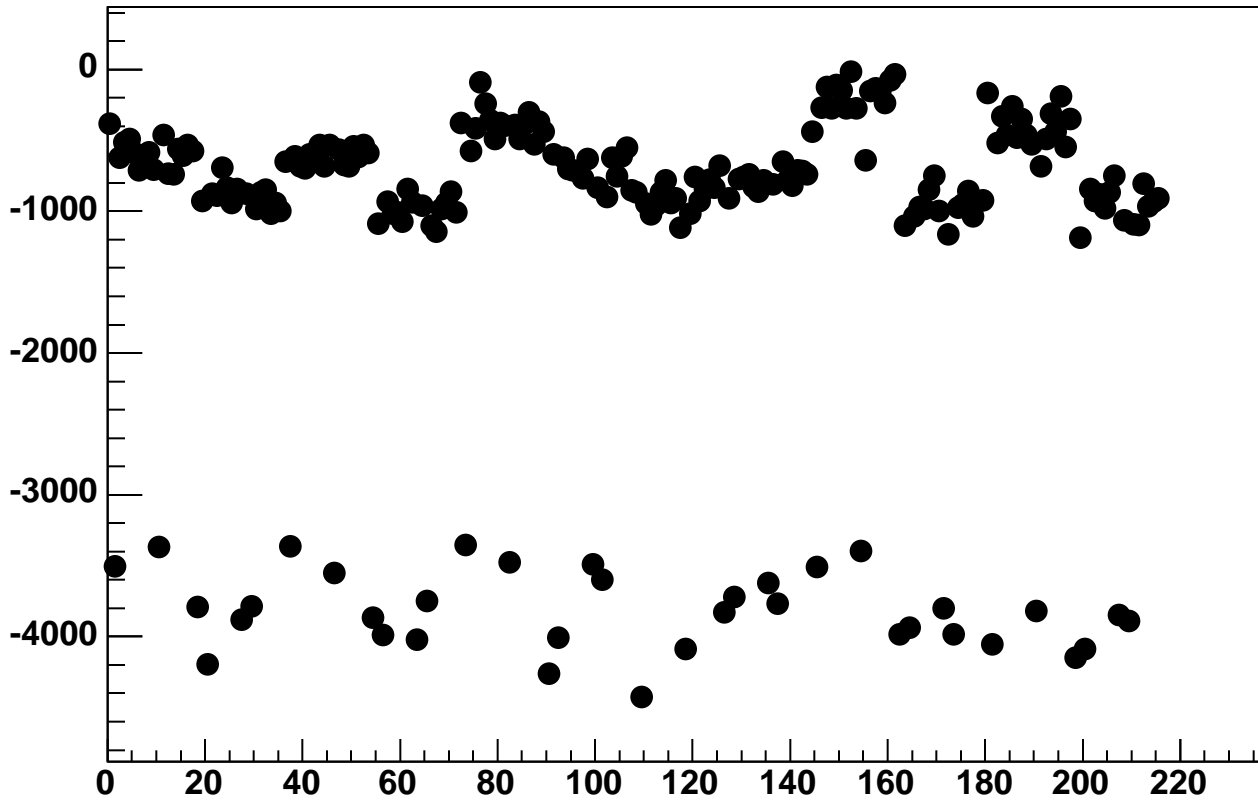
Enable 3, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



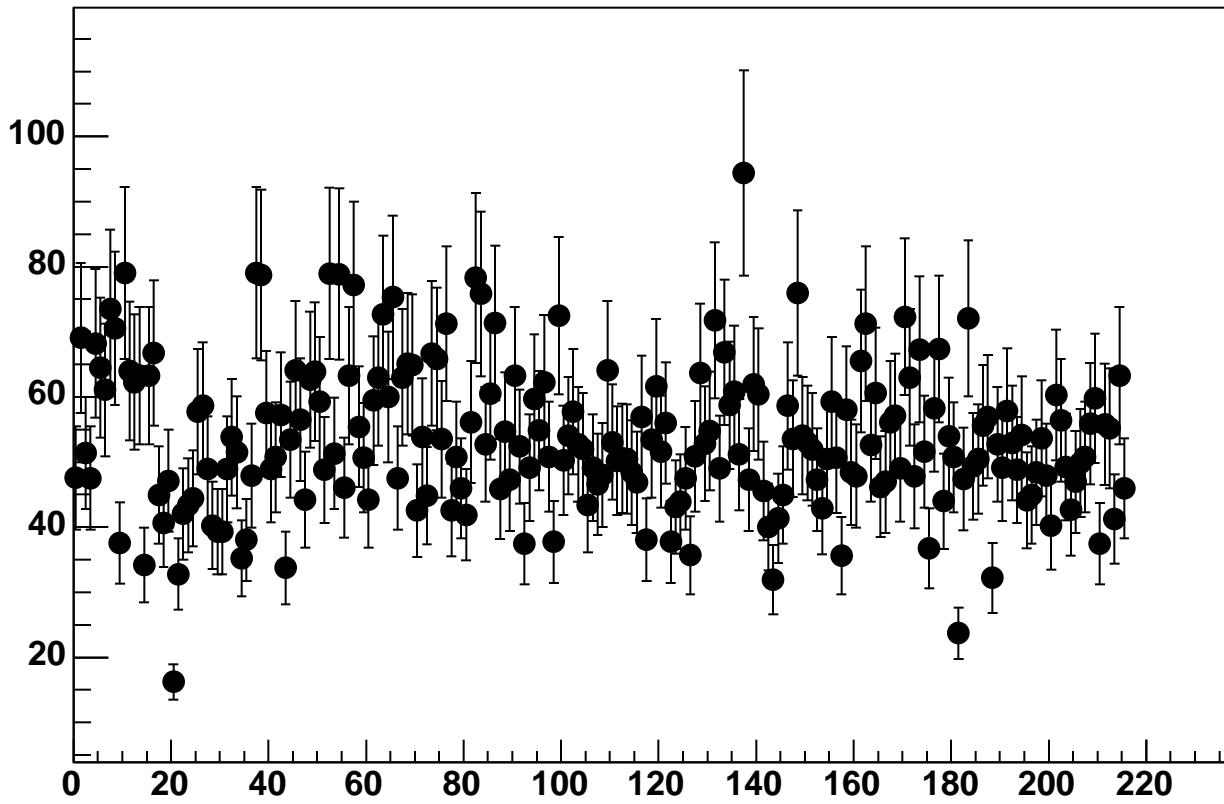
Enable 3, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



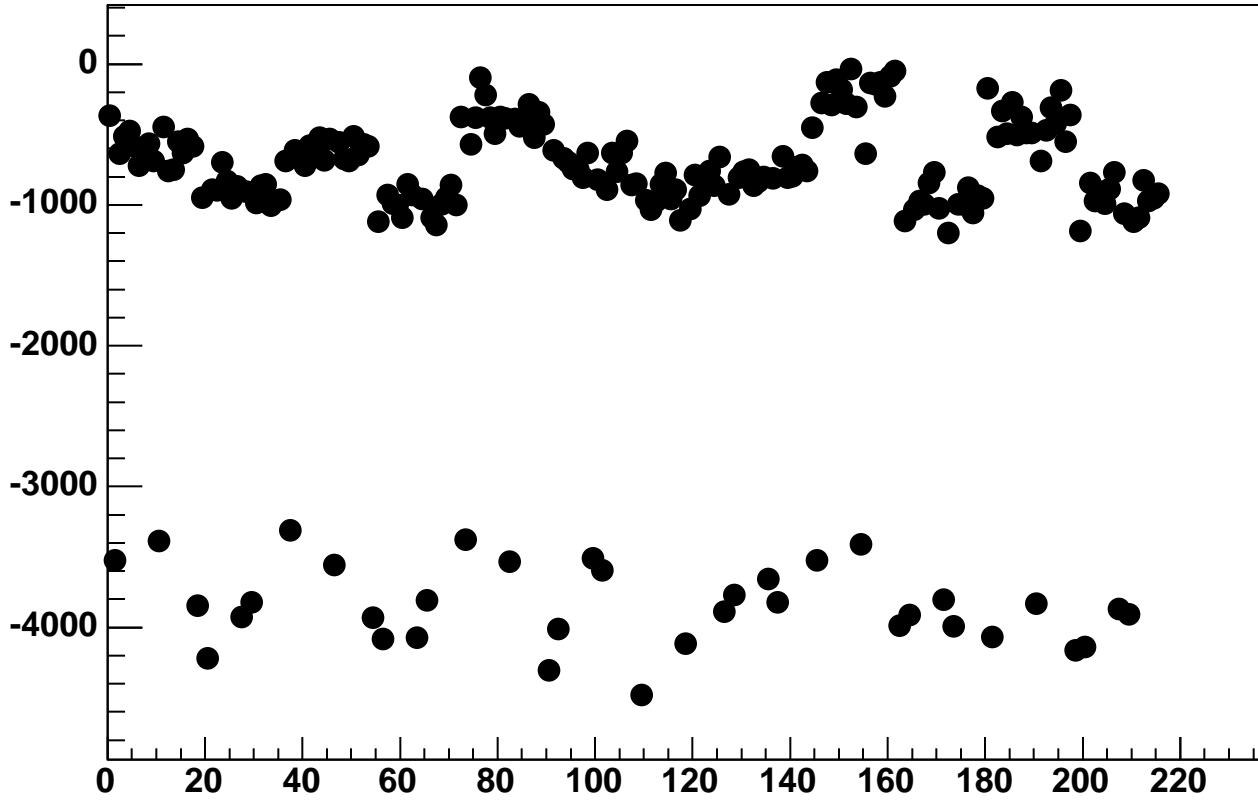
Enable 3, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan



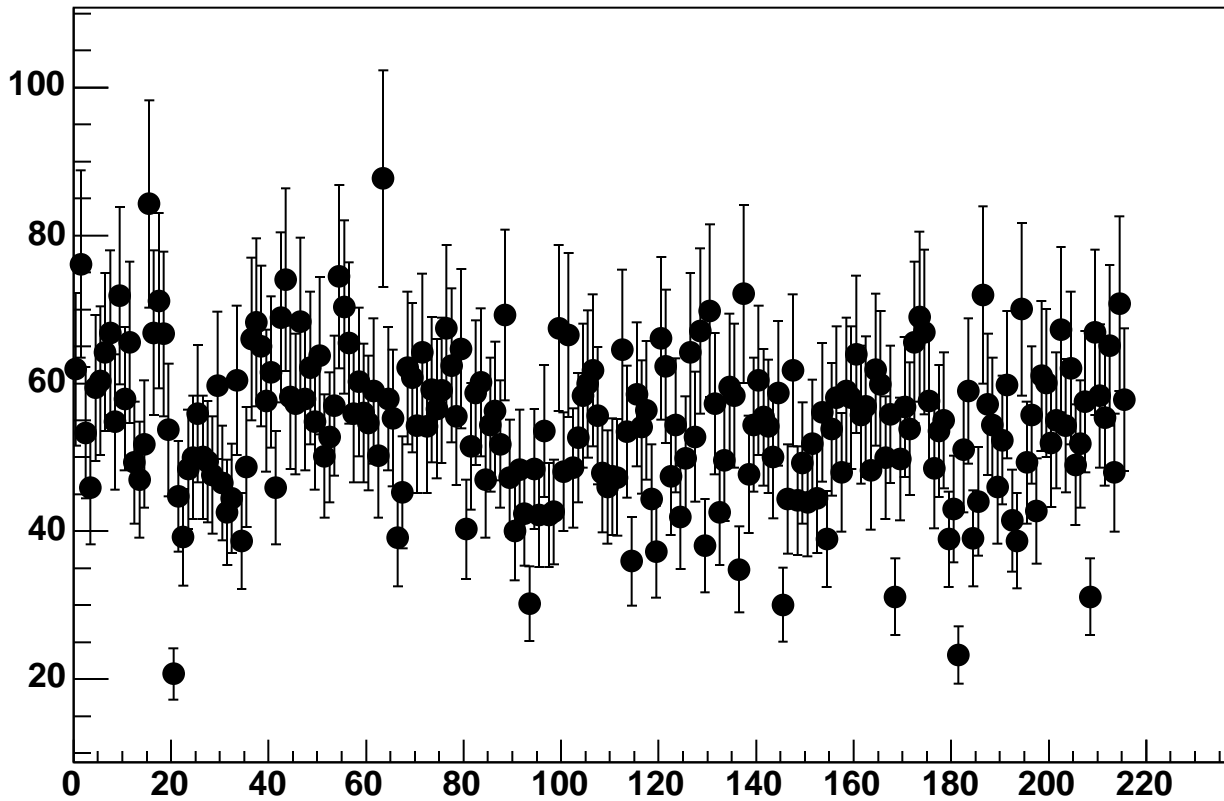
Enable 3, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan



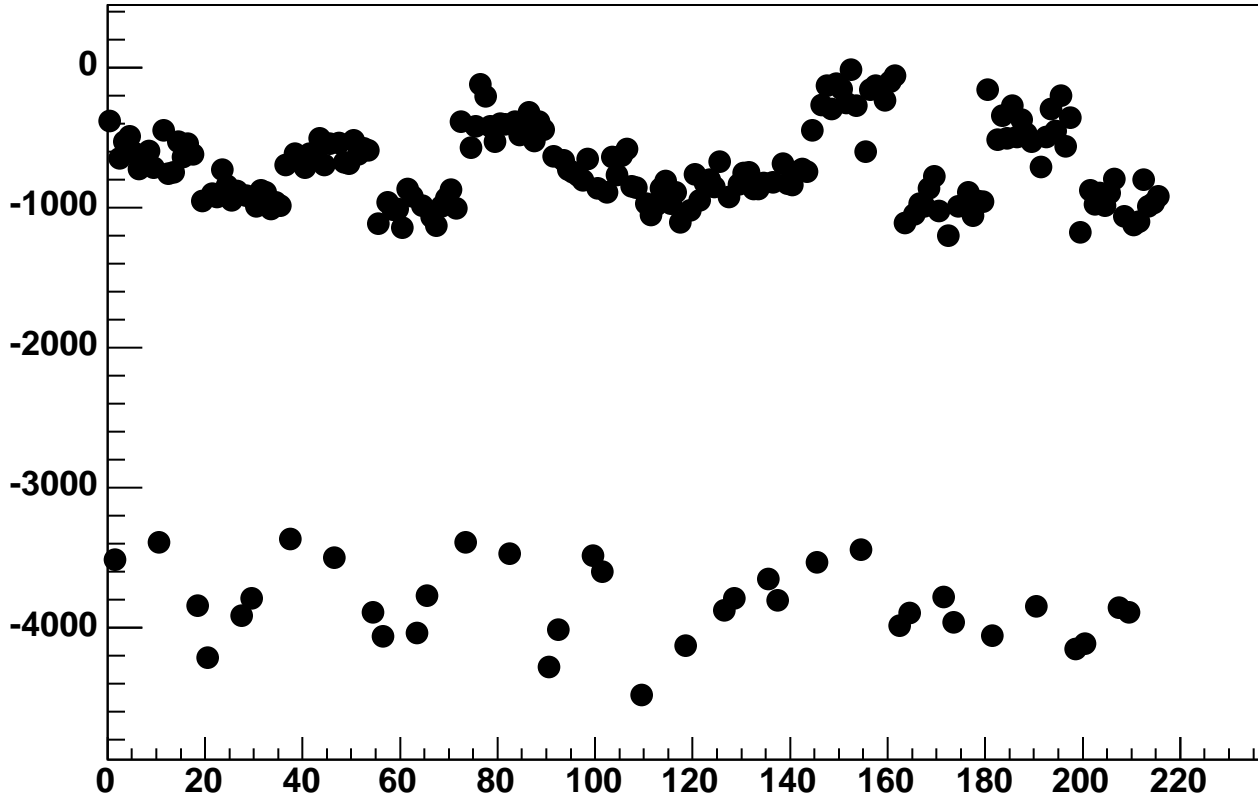
Enable 3, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



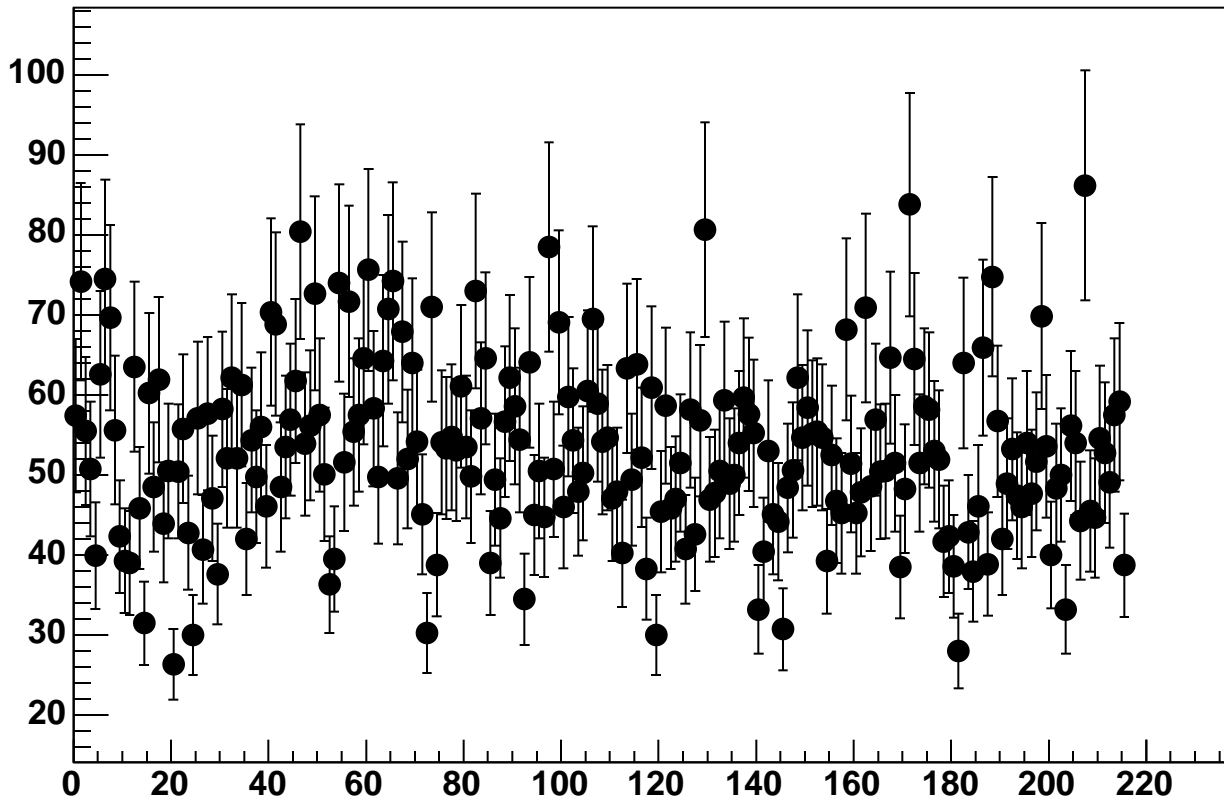
Enable 3, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



Enable 3, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan

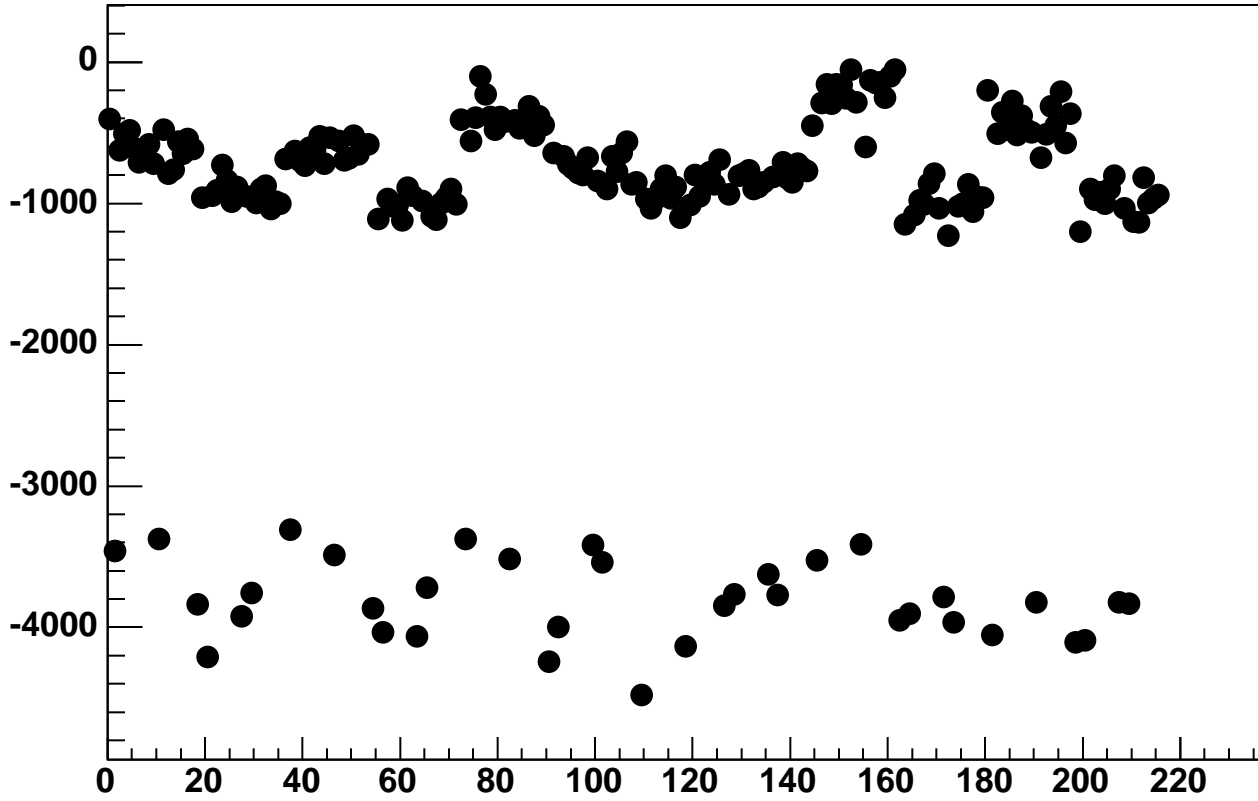


Enable 3, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan

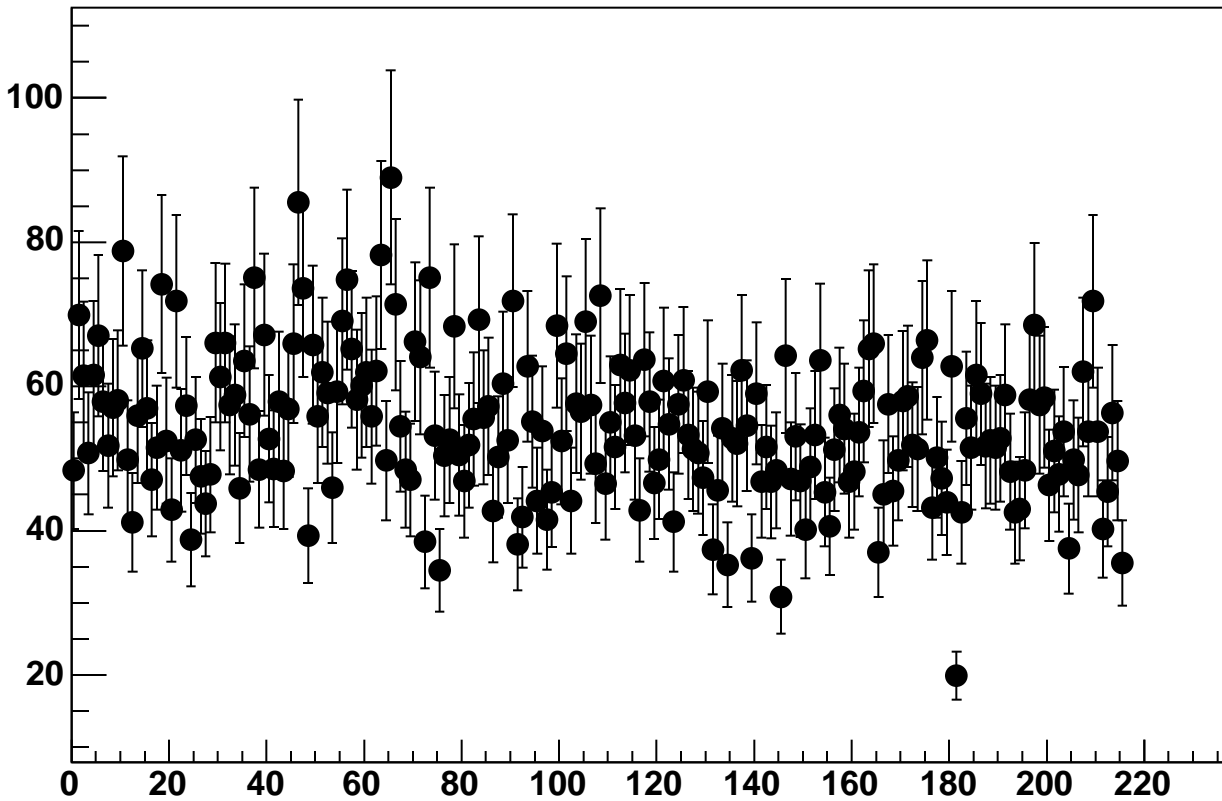




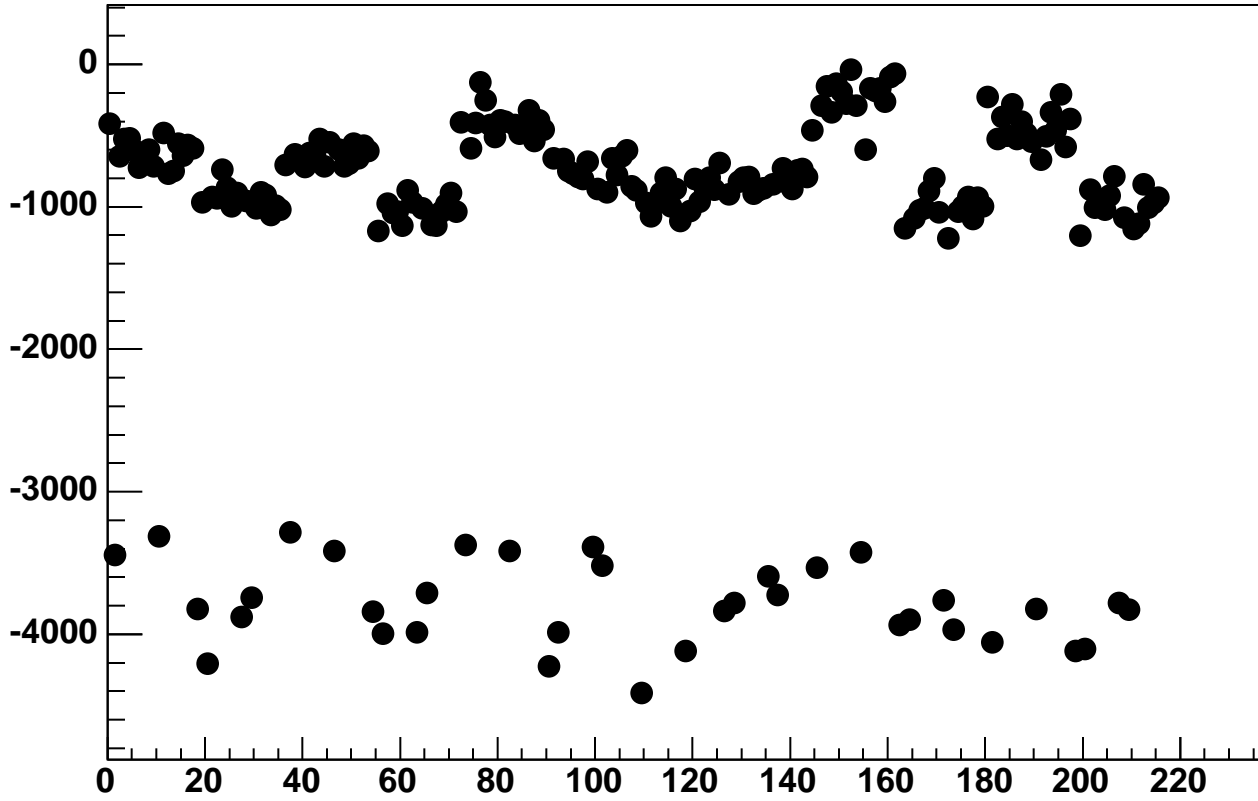
Enable 3, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



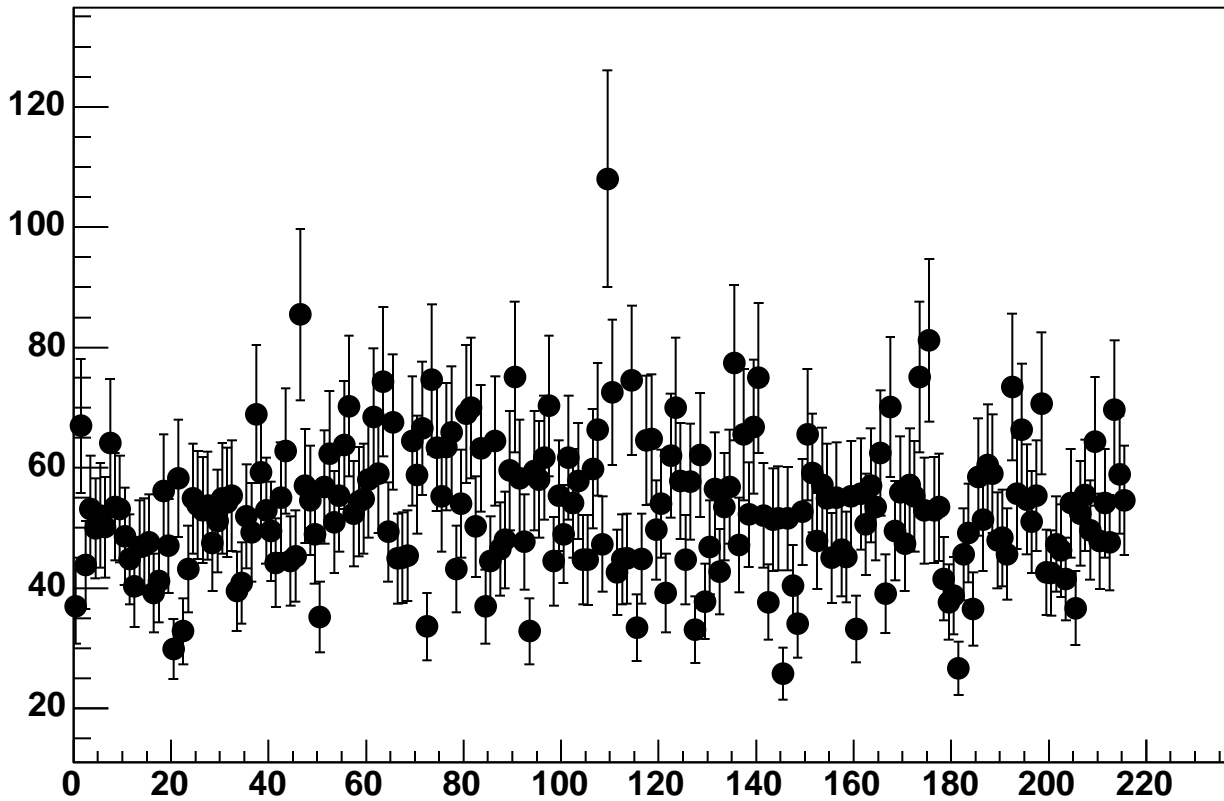
Enable 3, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



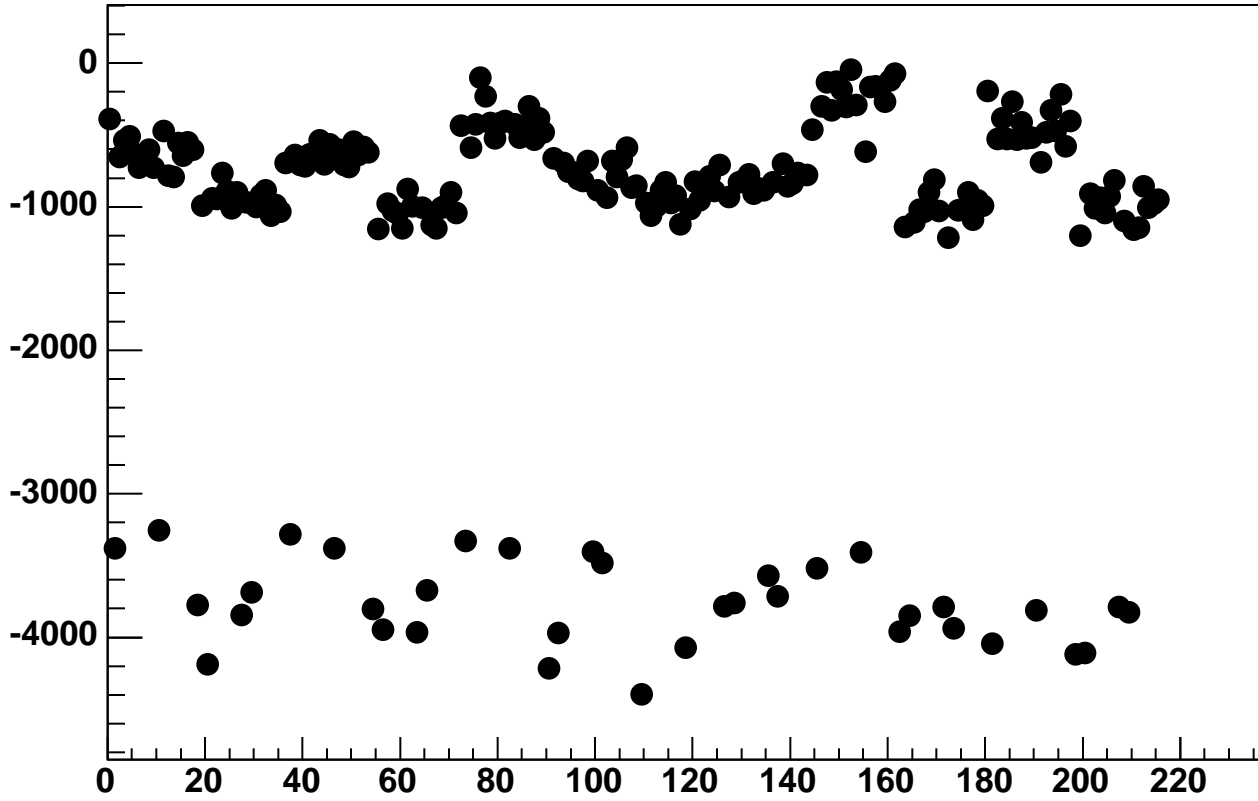
Enable 3, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan



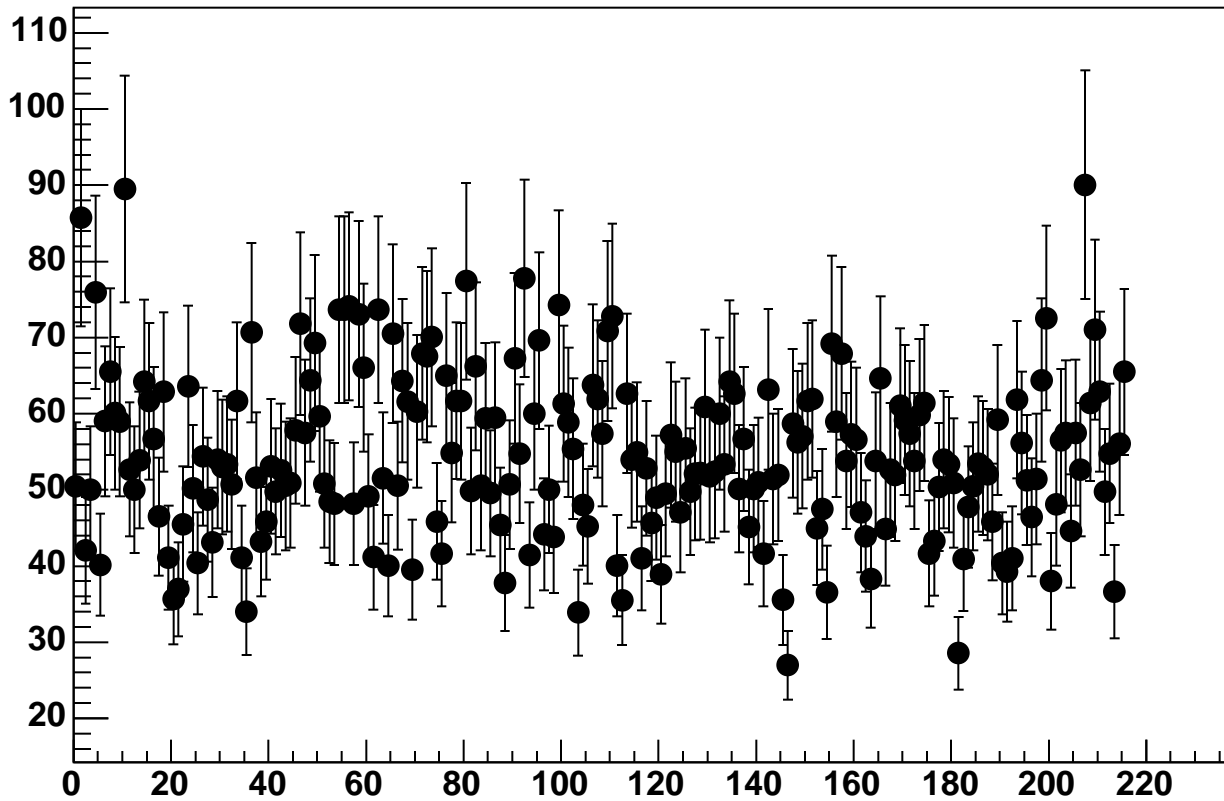
Enable 3, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan



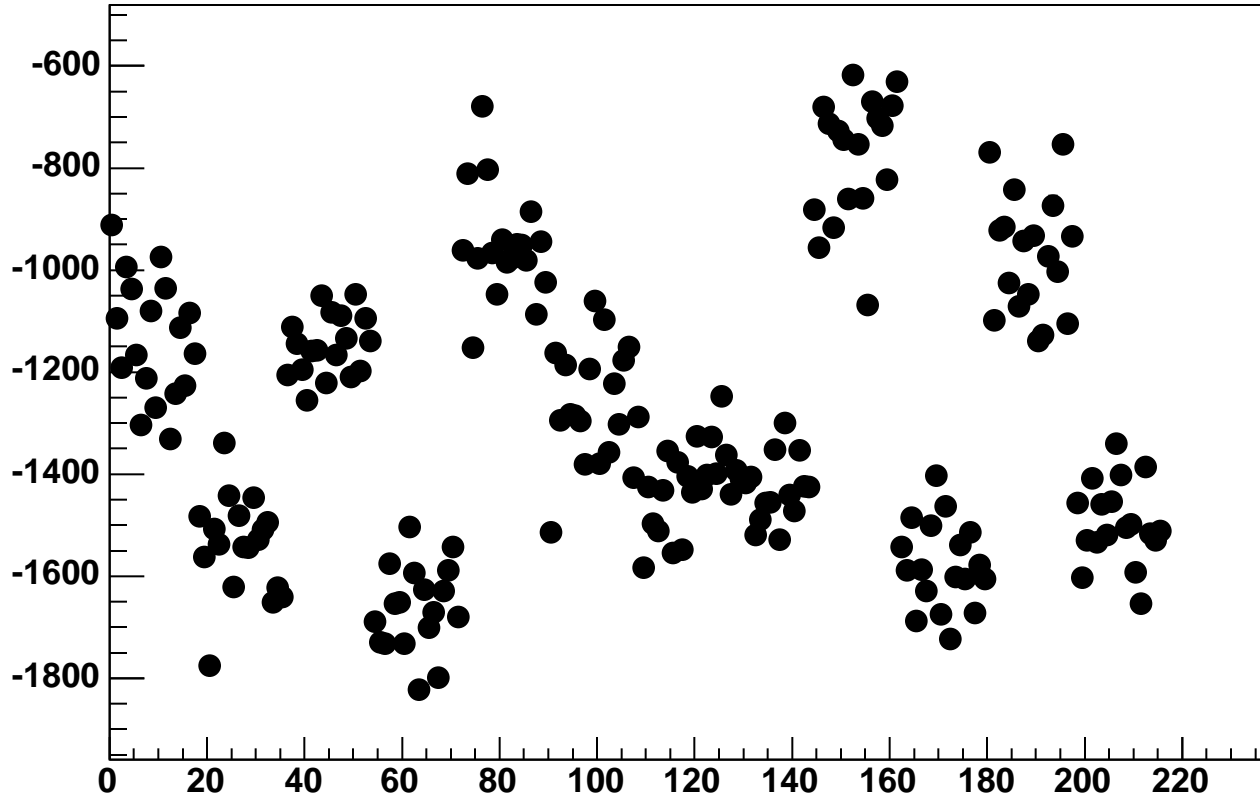
Enable 3, DAC=1600, Hold=245, ADC Mean vs 18\*Chip+Chan



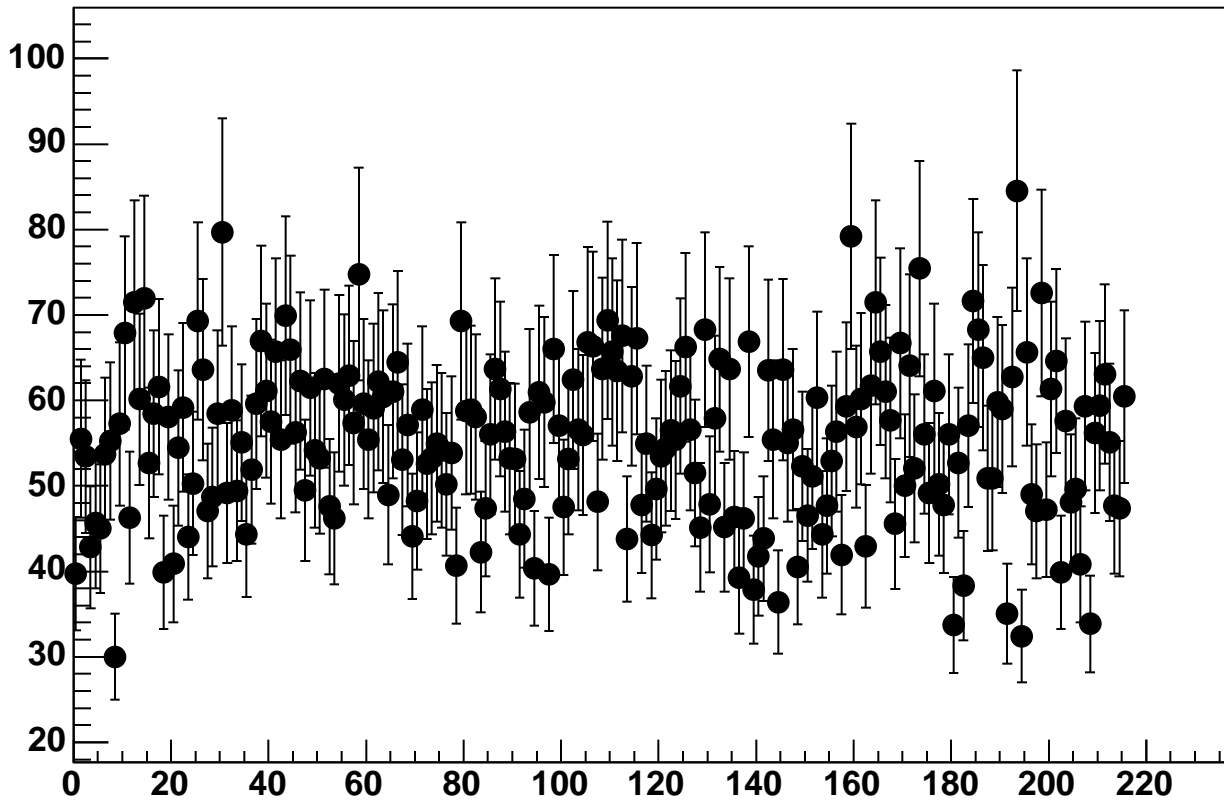
Enable 3, DAC=1600, Hold=245, ADC Noise vs 18\*Chip+Chan



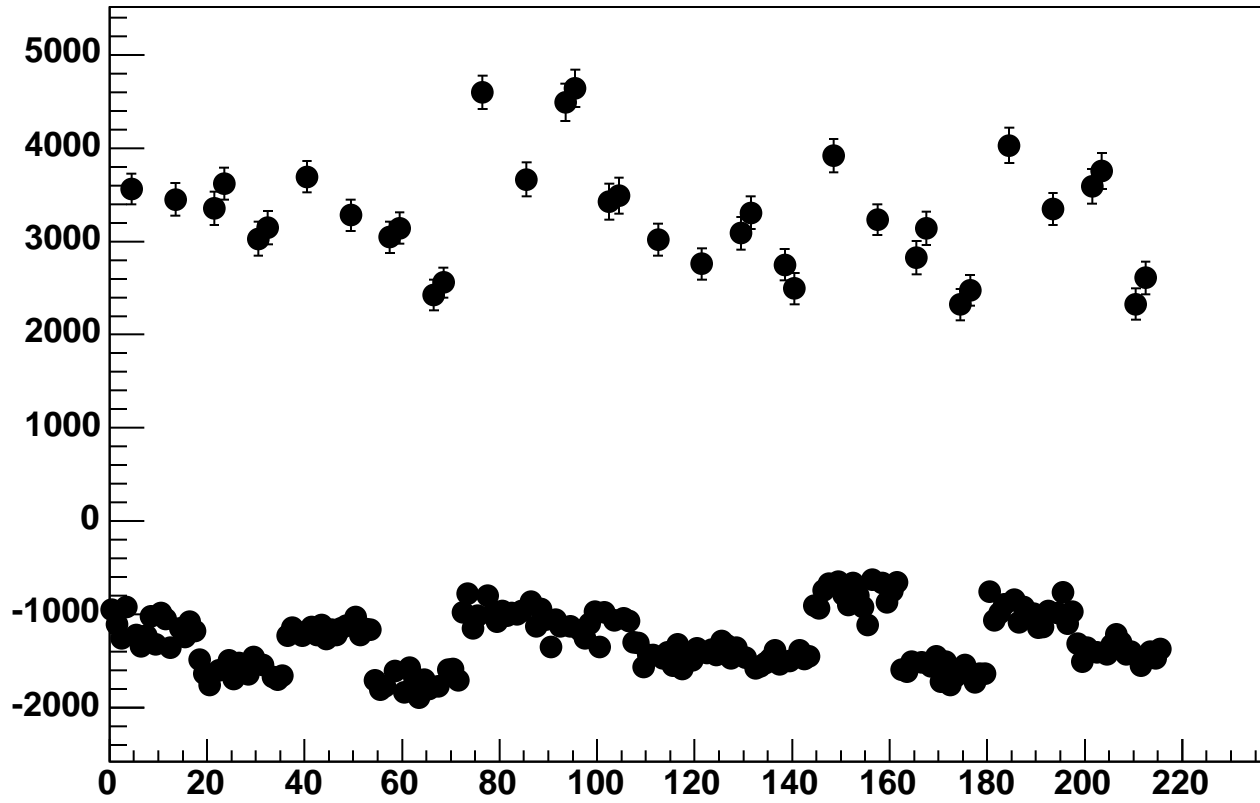
Enable 4, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan



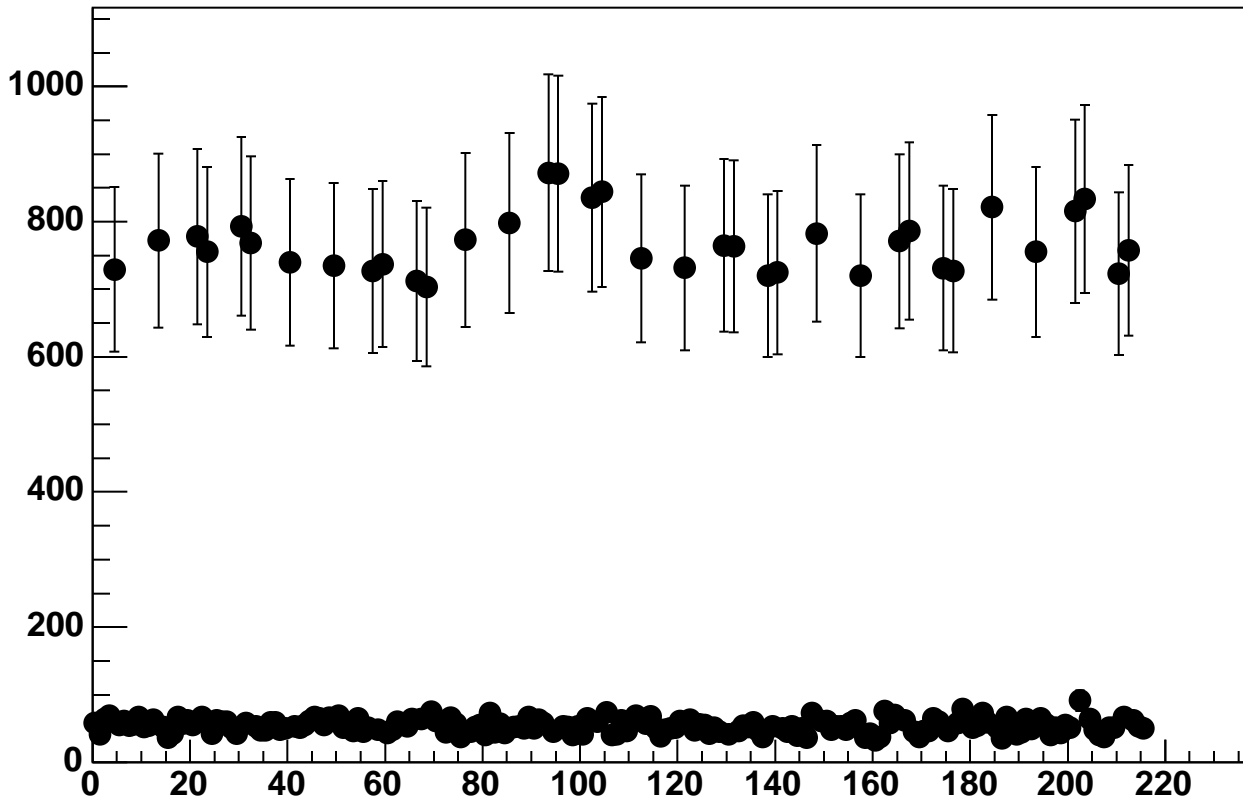
Enable 4, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan



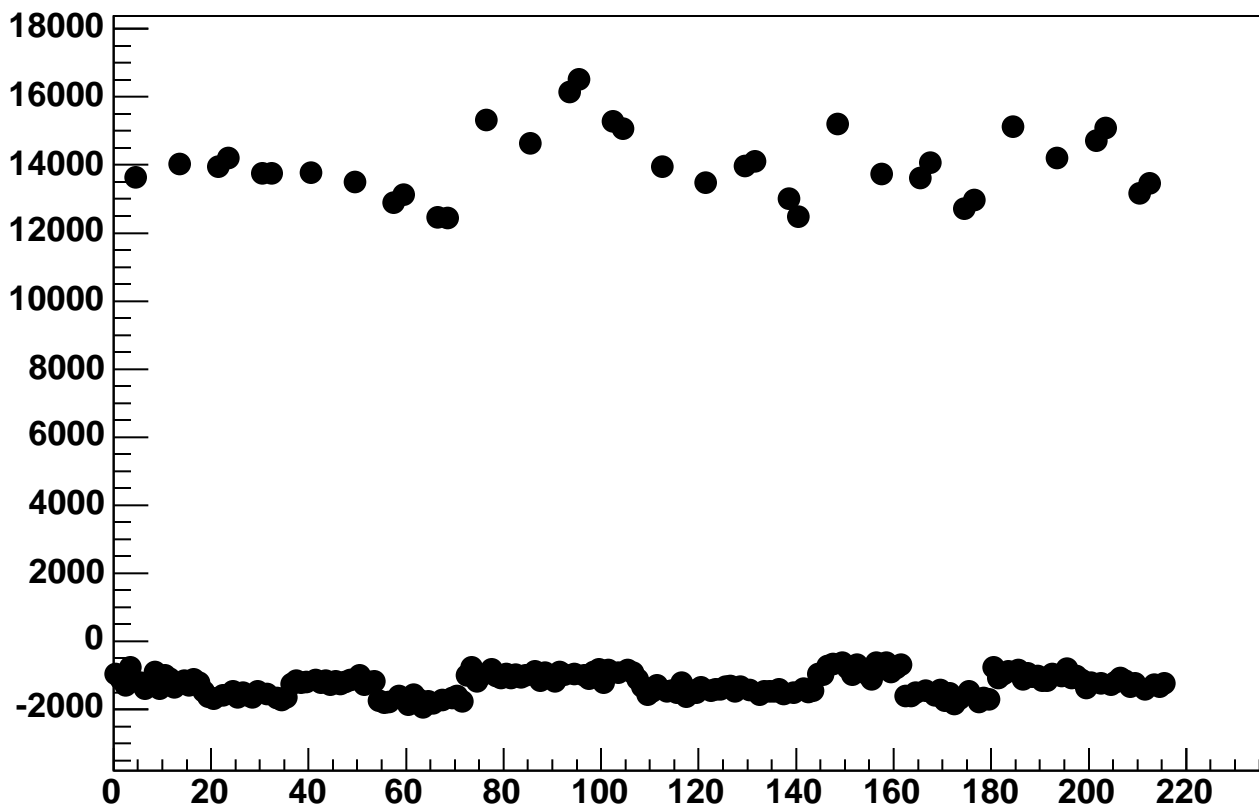
Enable 4, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



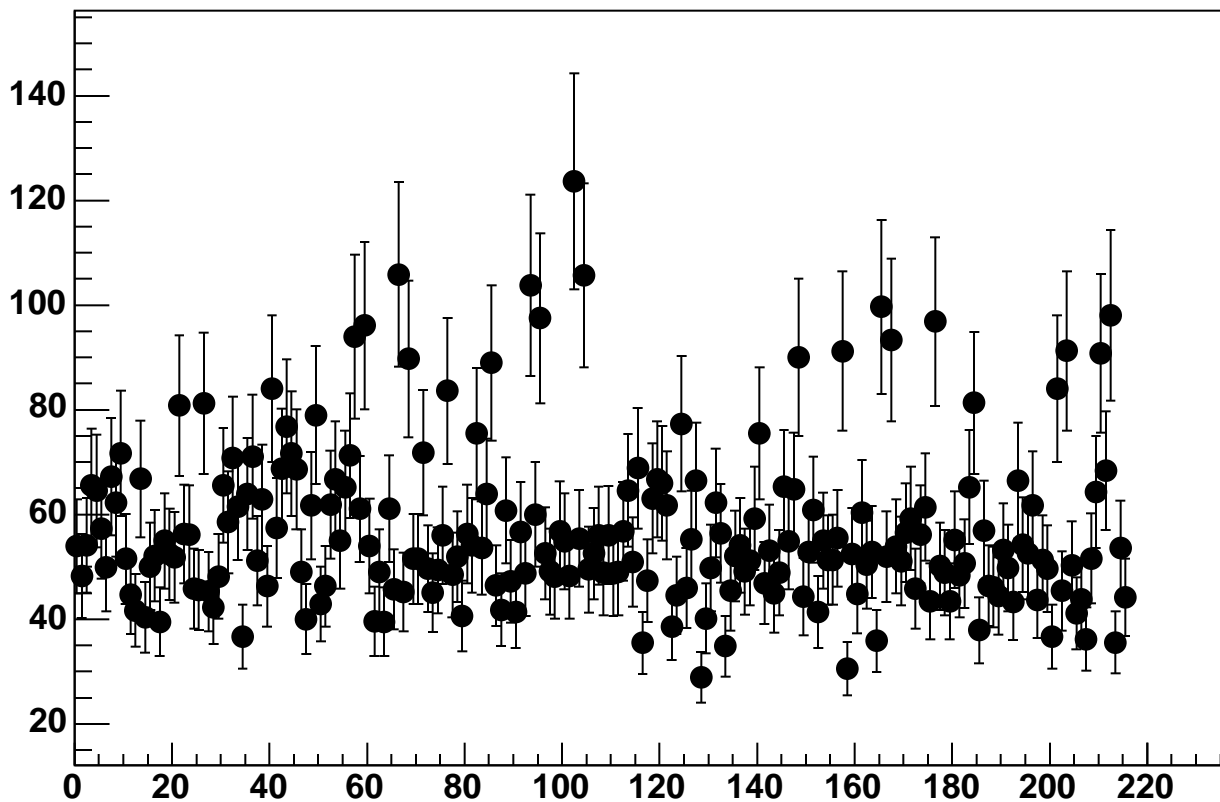
Enable 4, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



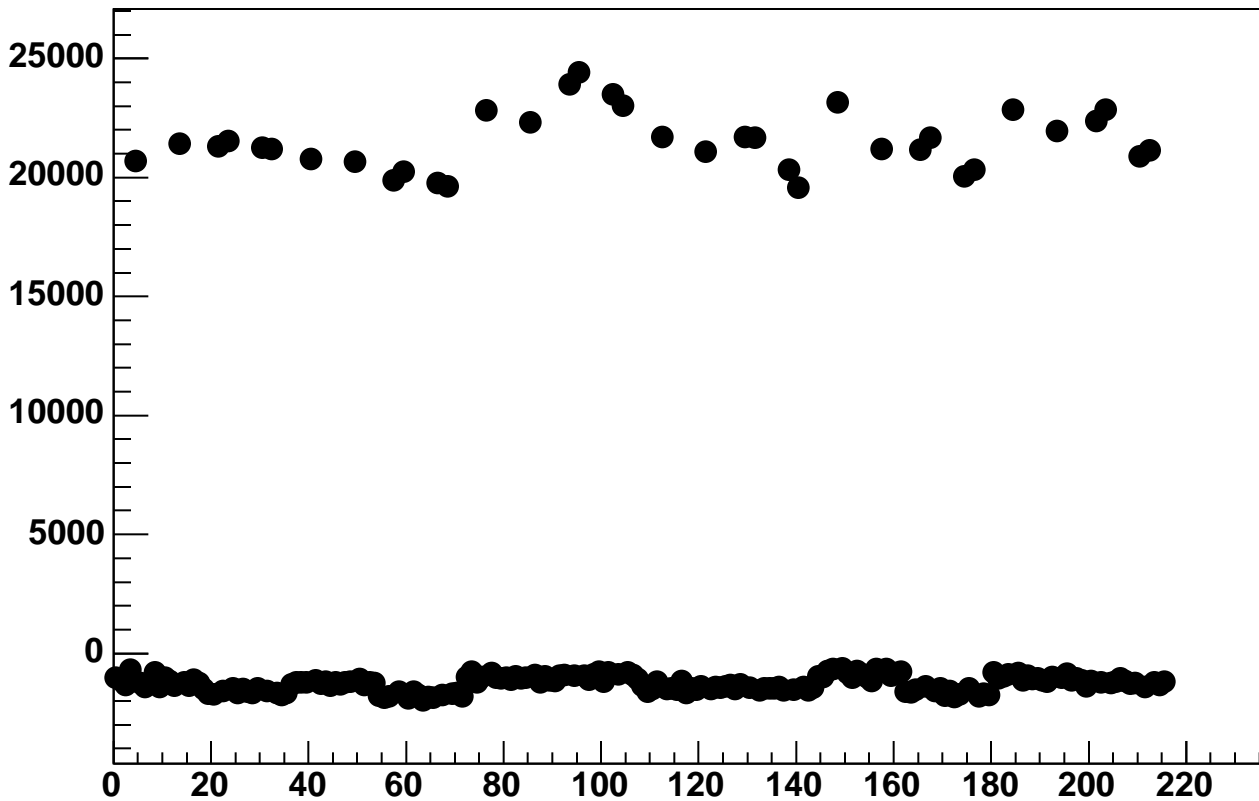
Enable 4, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan



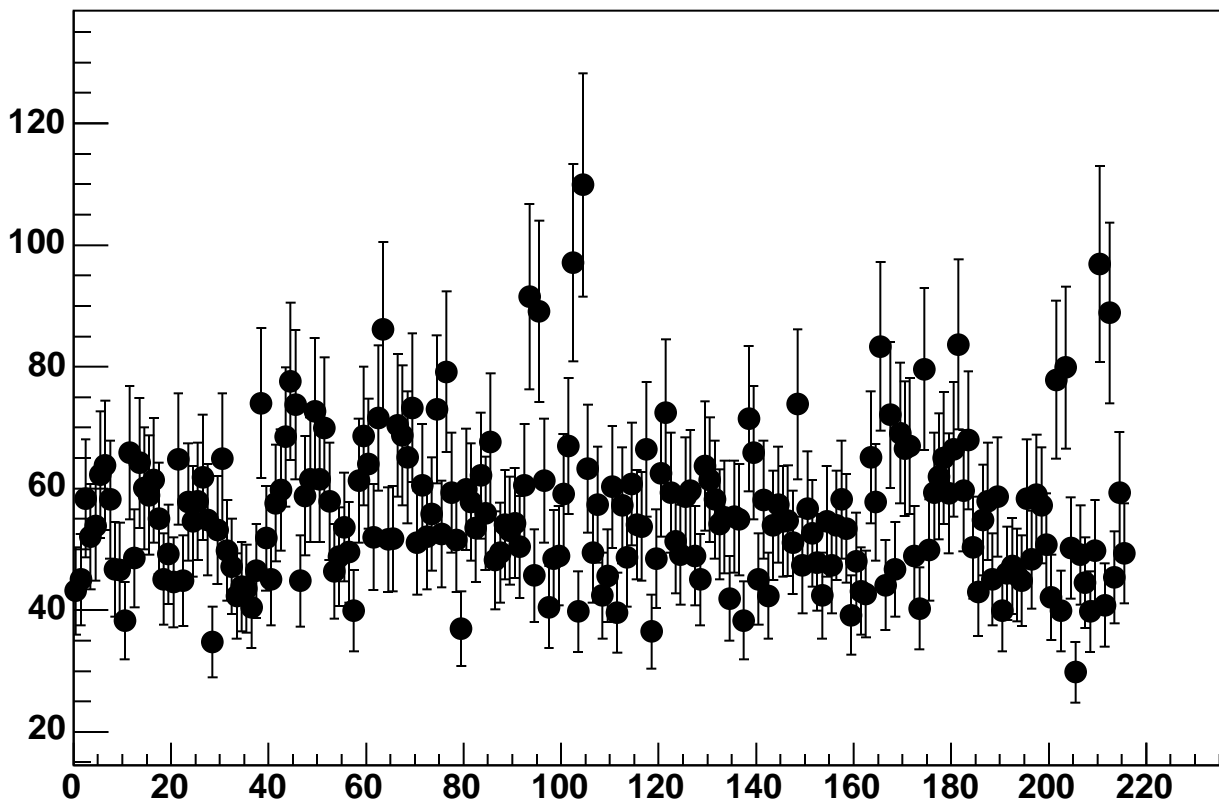
Enable 4, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan



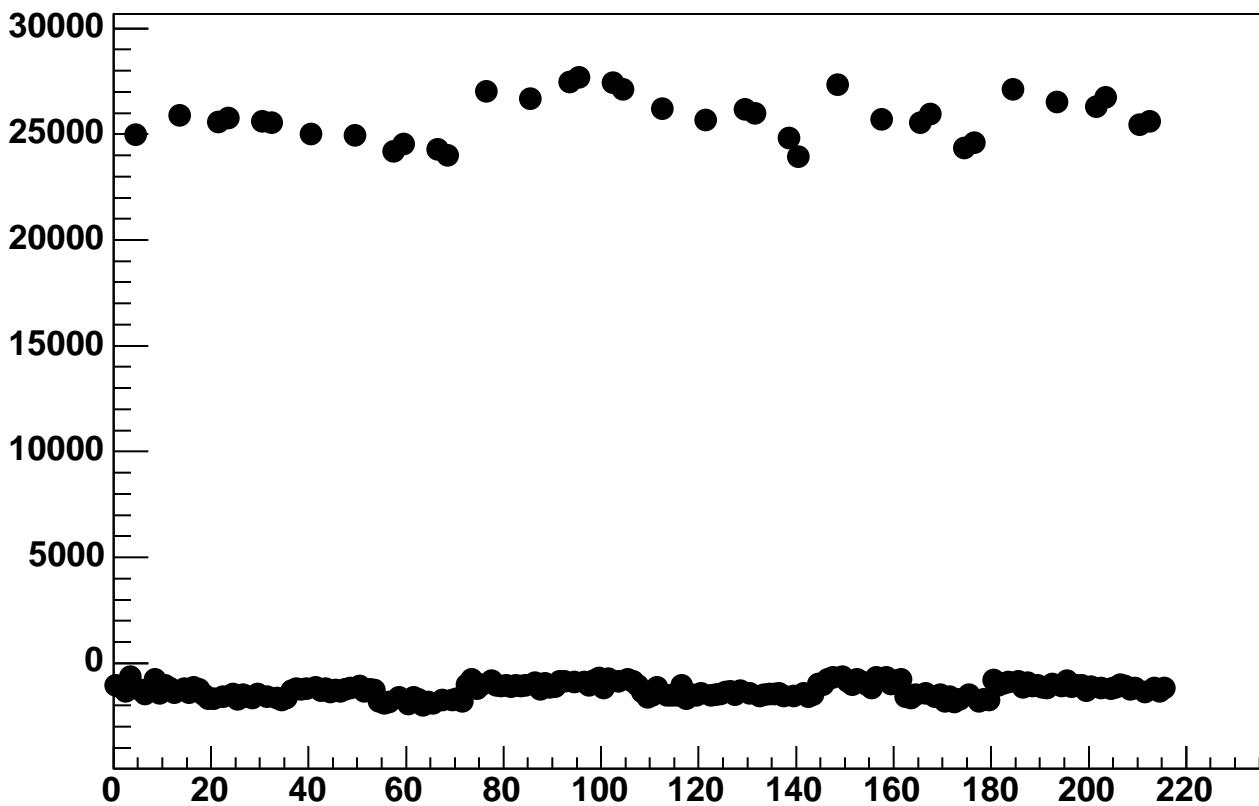
Enable 4, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



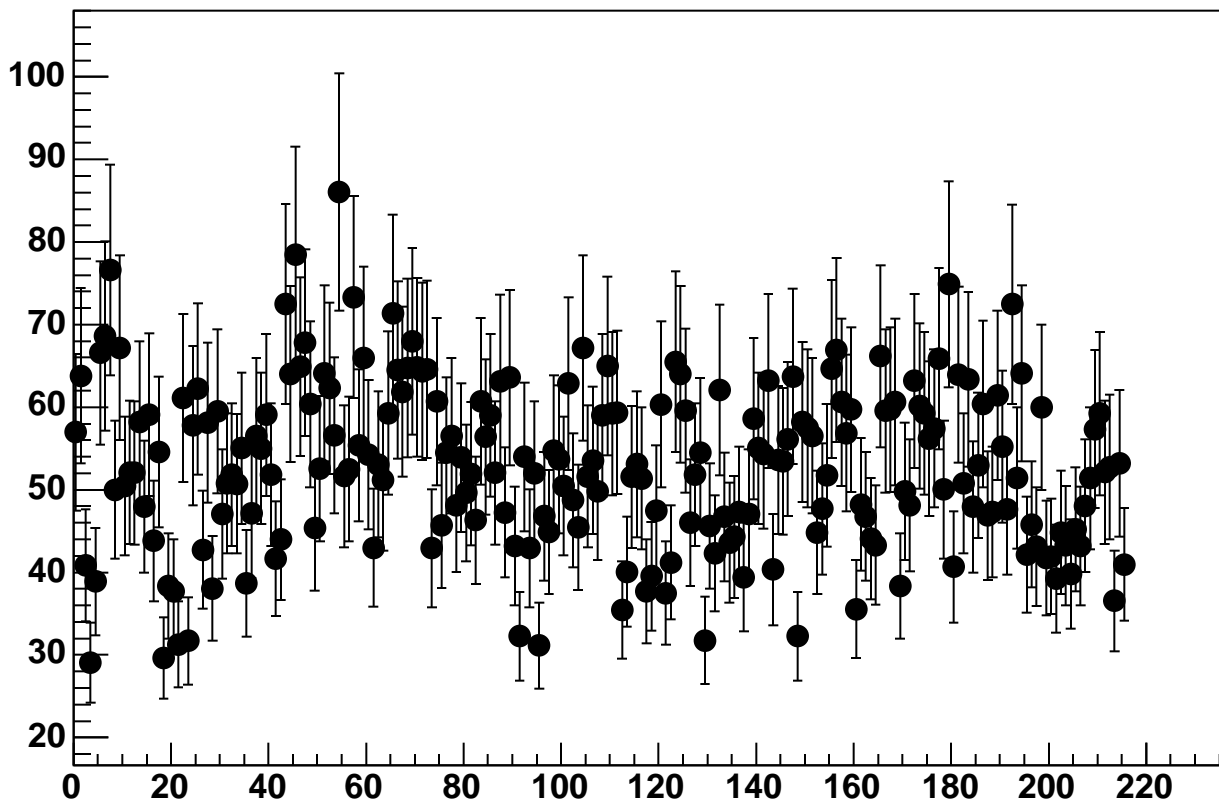
Enable 4, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan

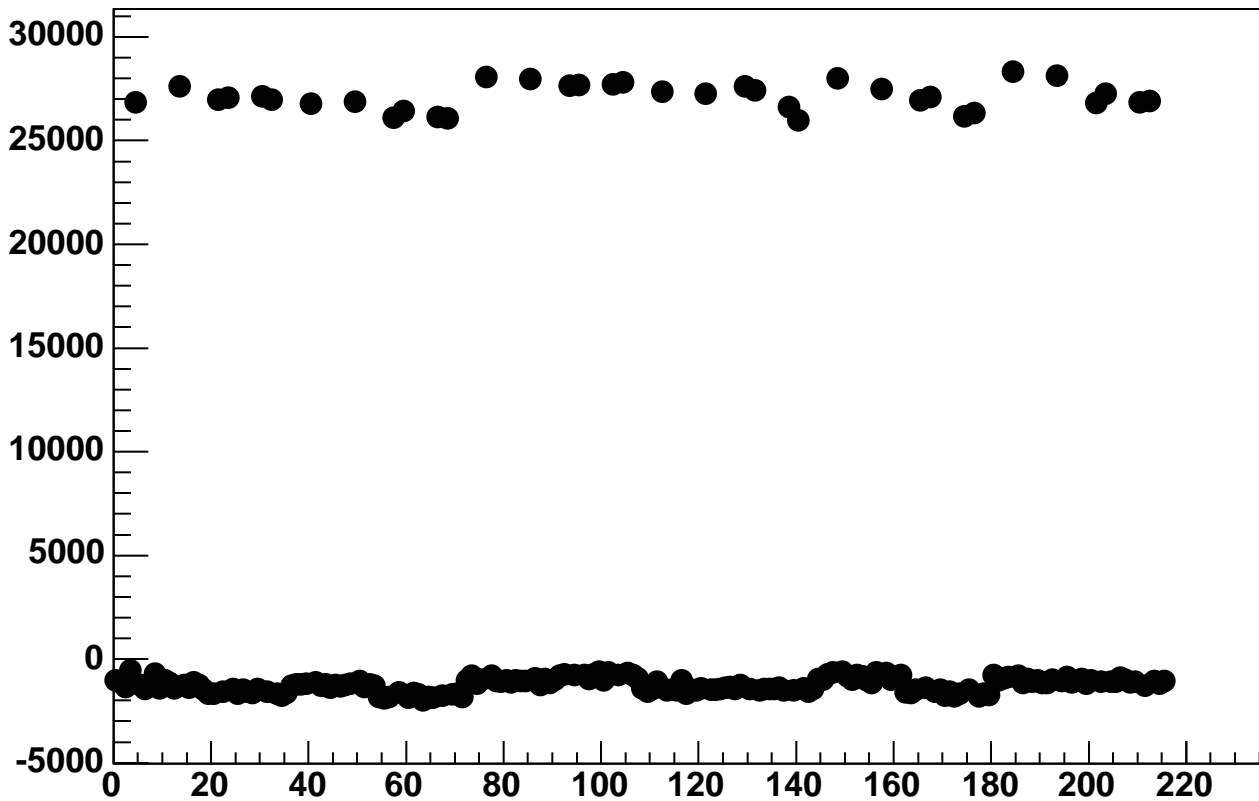


Enable 4, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan

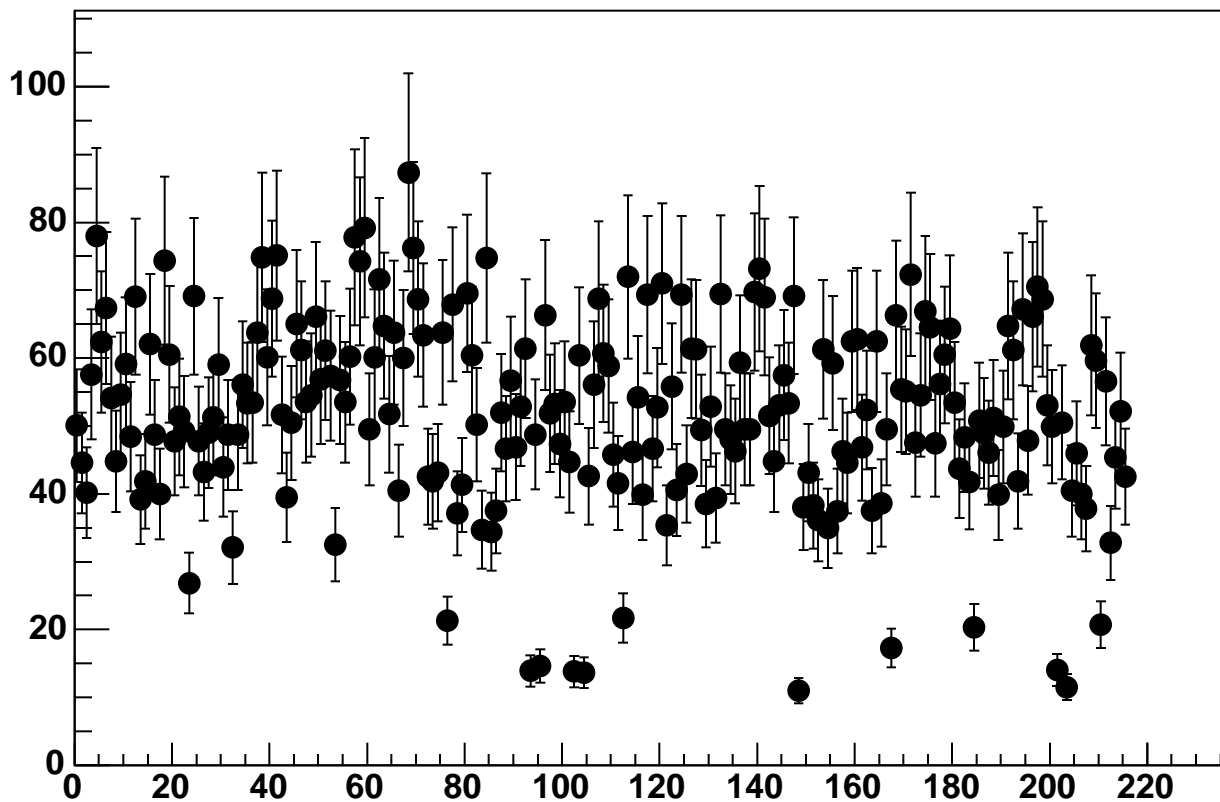




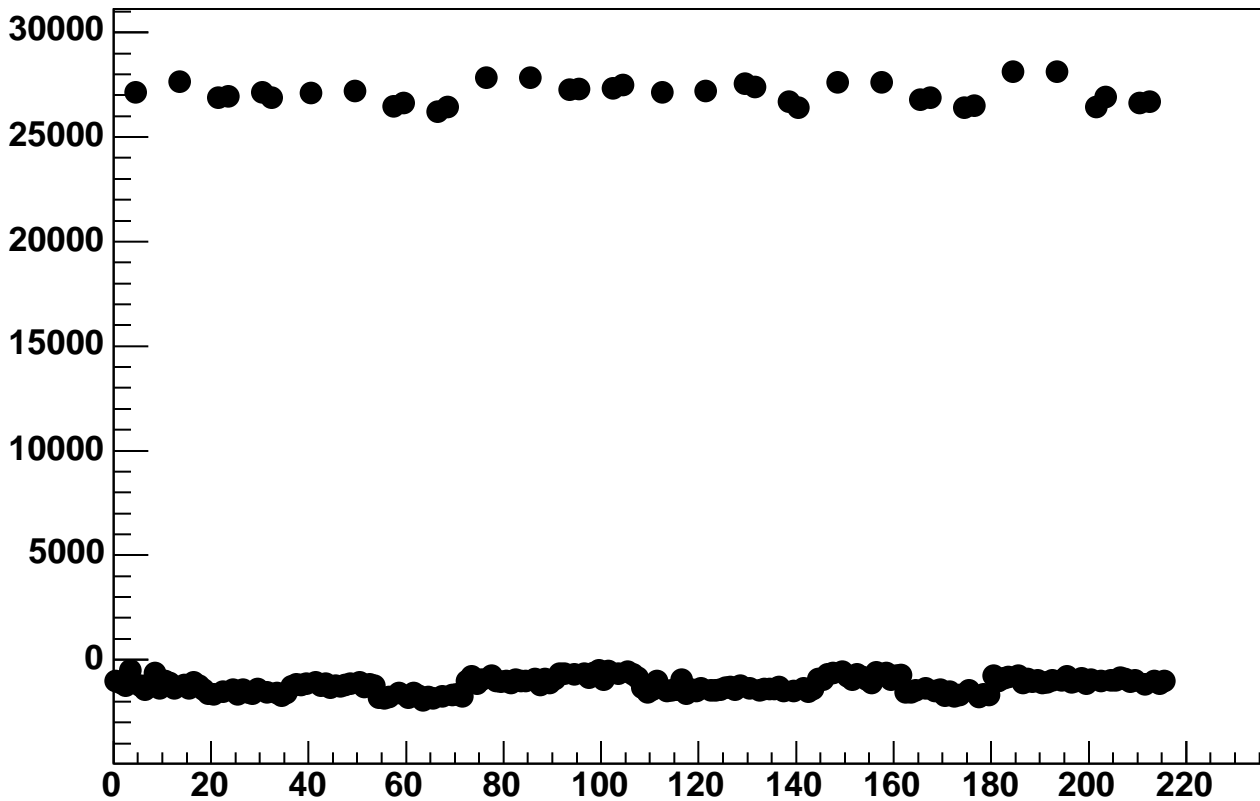
Enable 4, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



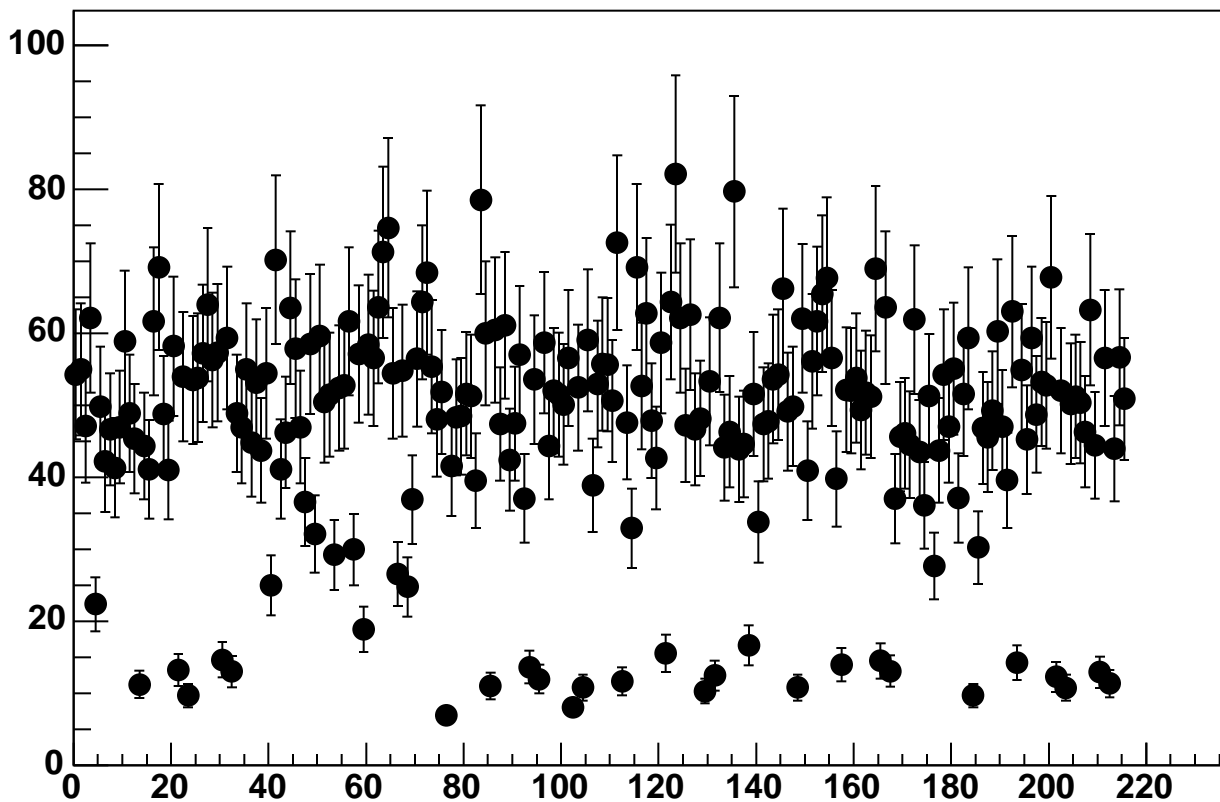
Enable 4, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



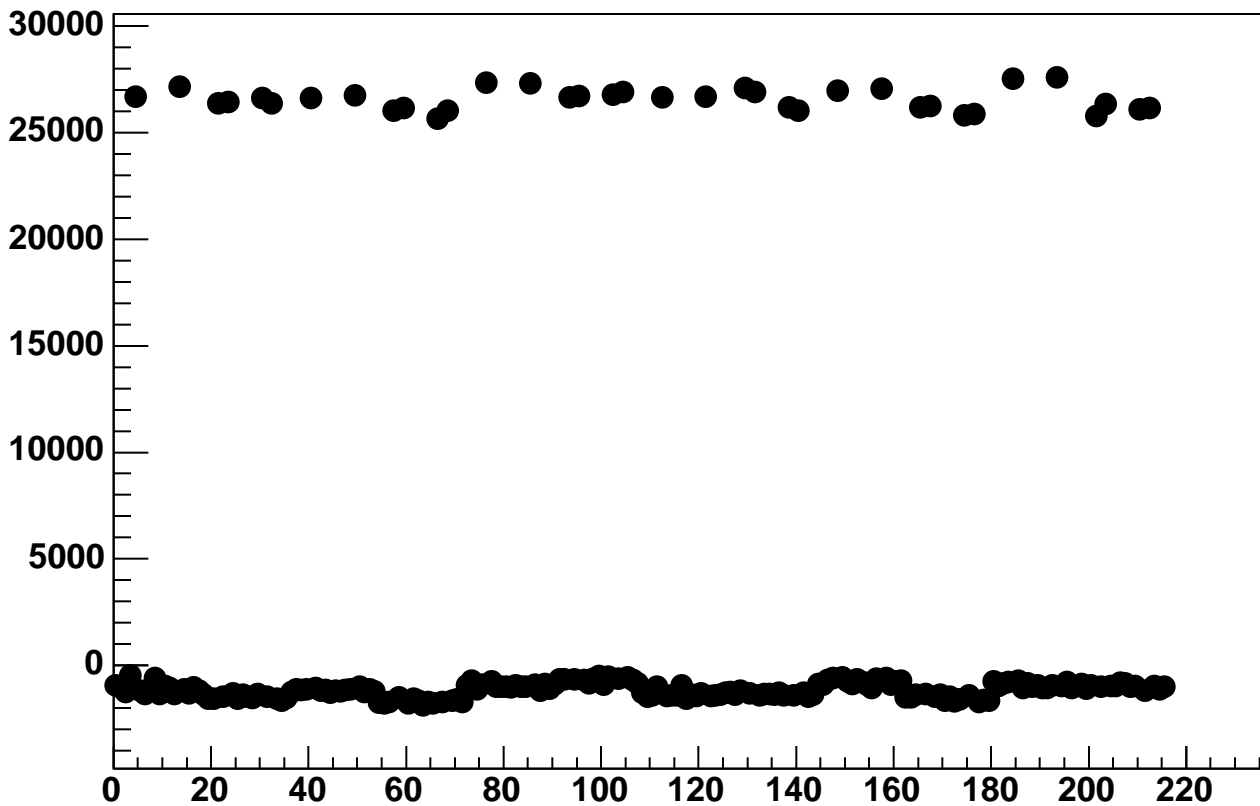
Enable 4, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan



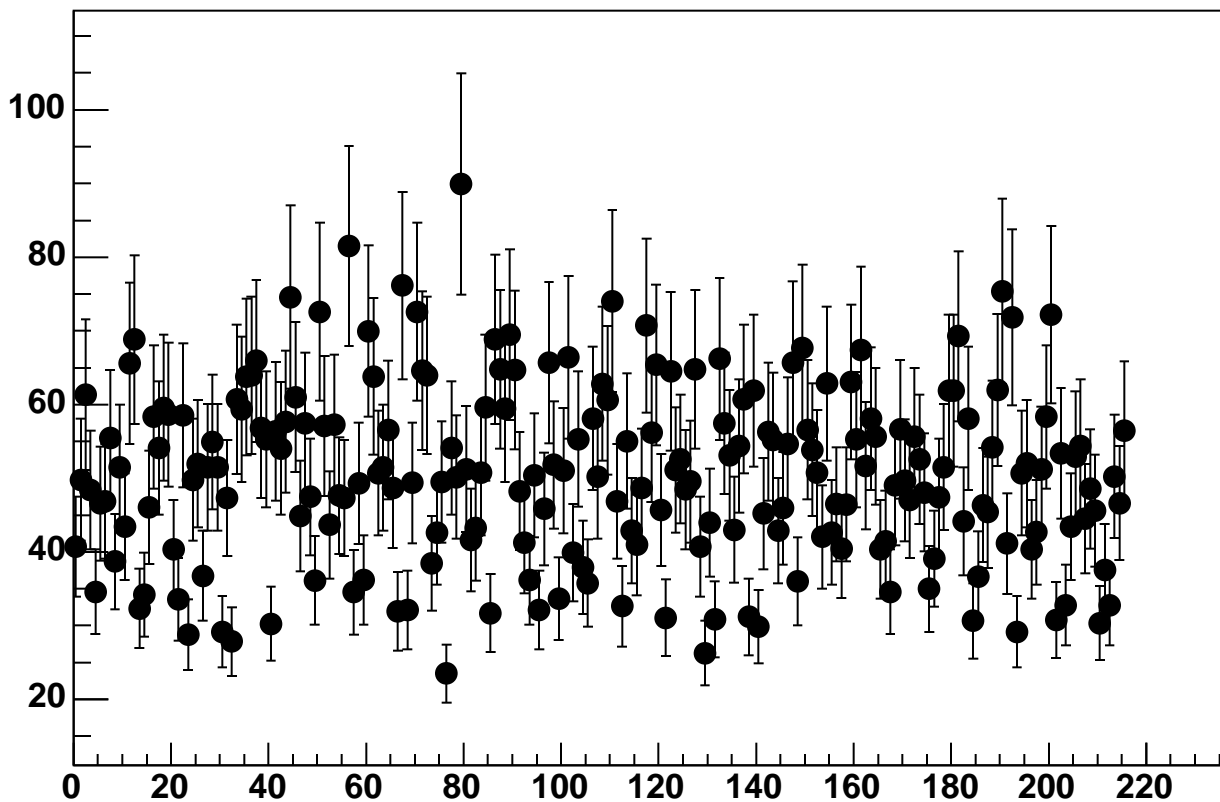
Enable 4, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan



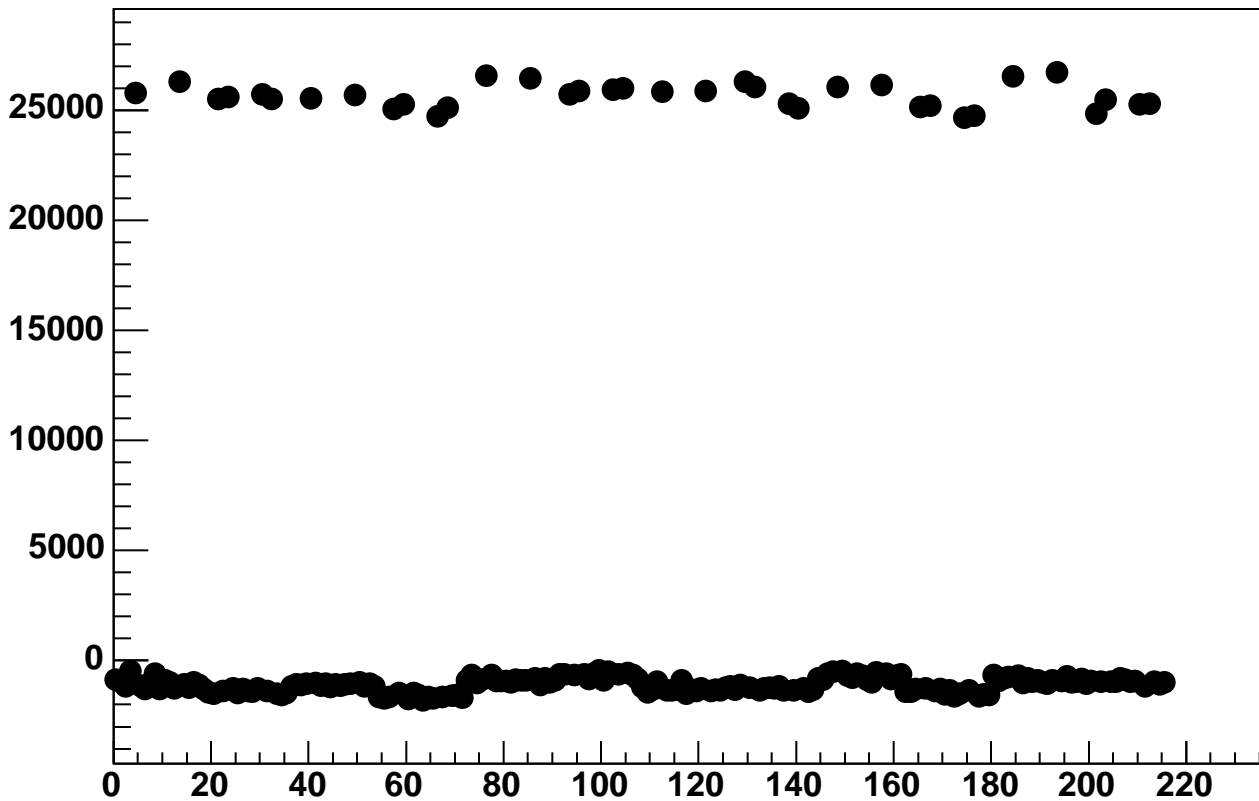
Enable 4, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



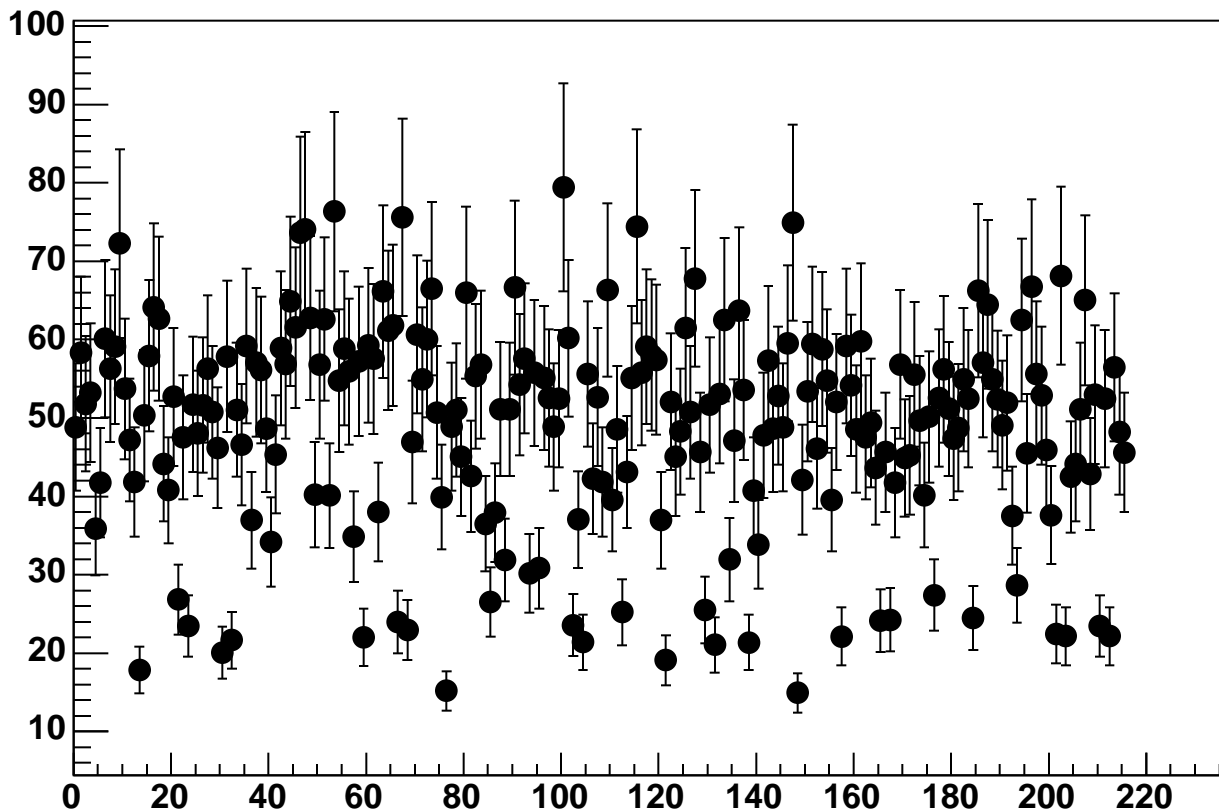
Enable 4, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



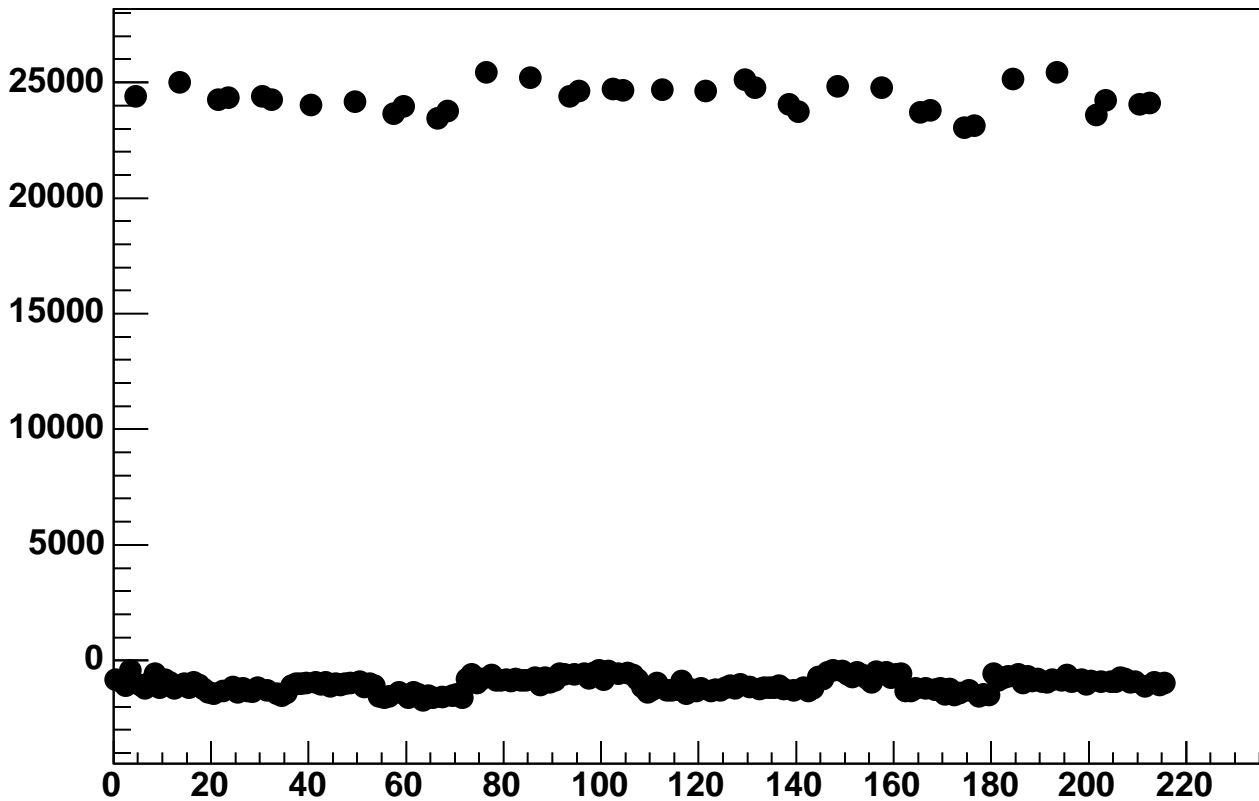
Enable 4, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan



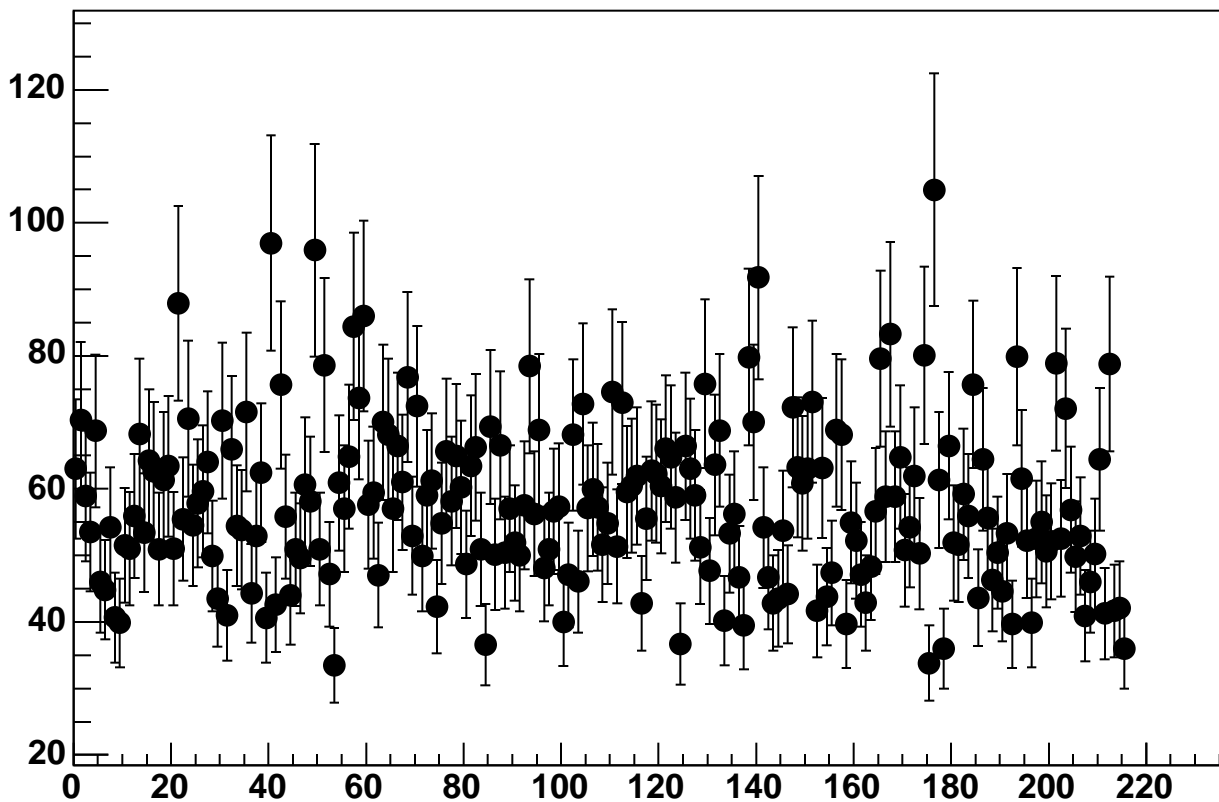
Enable 4, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan



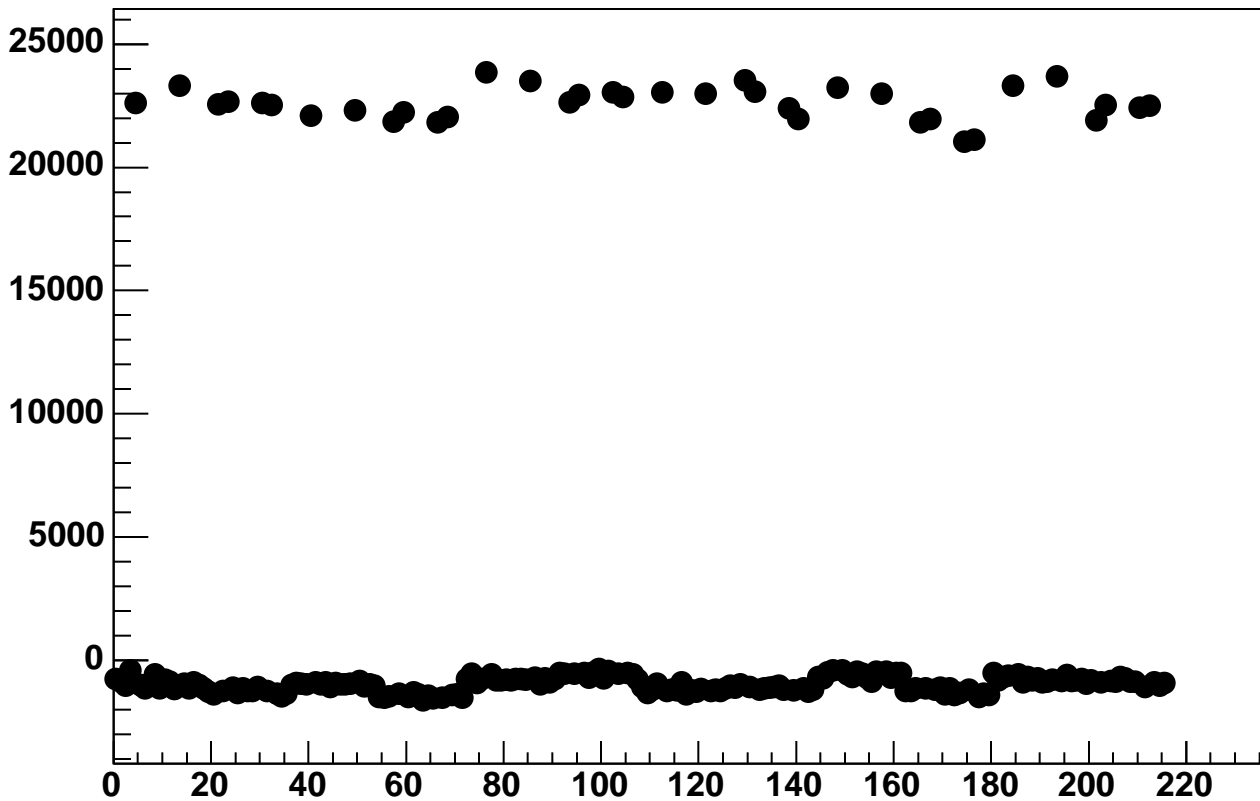
Enable 4, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



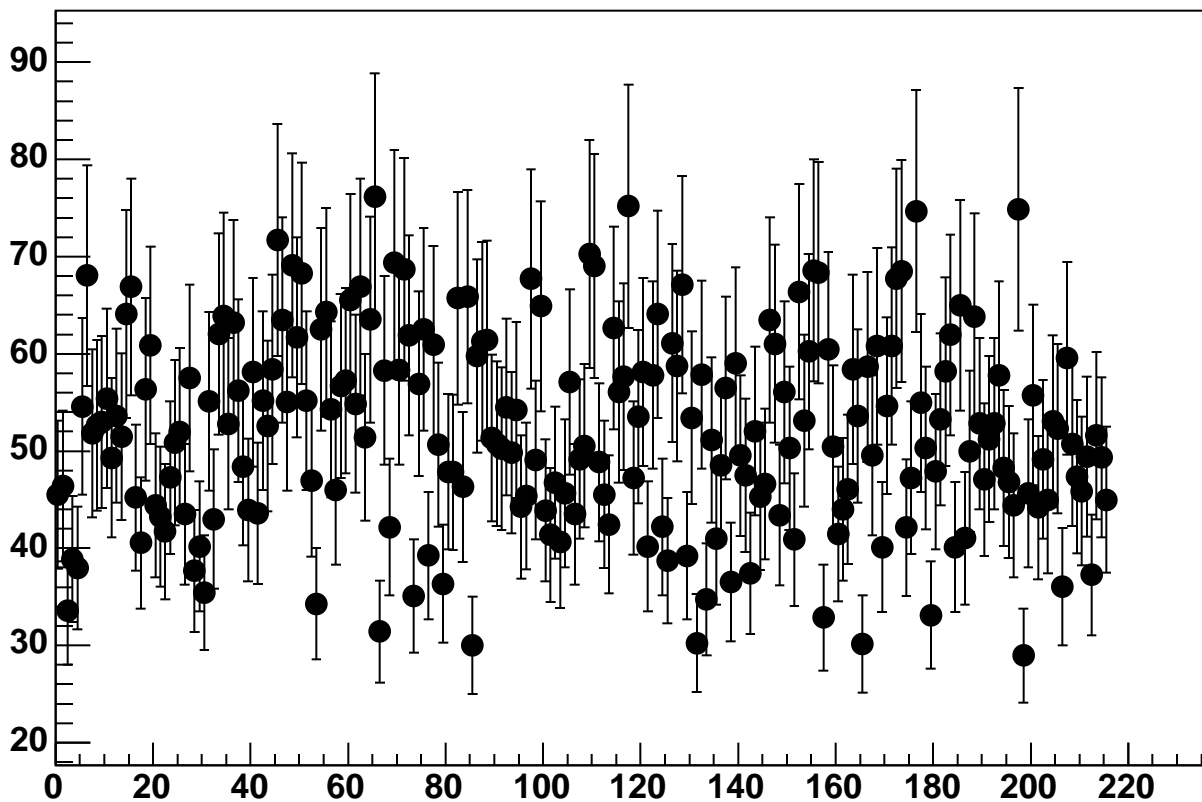
Enable 4, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



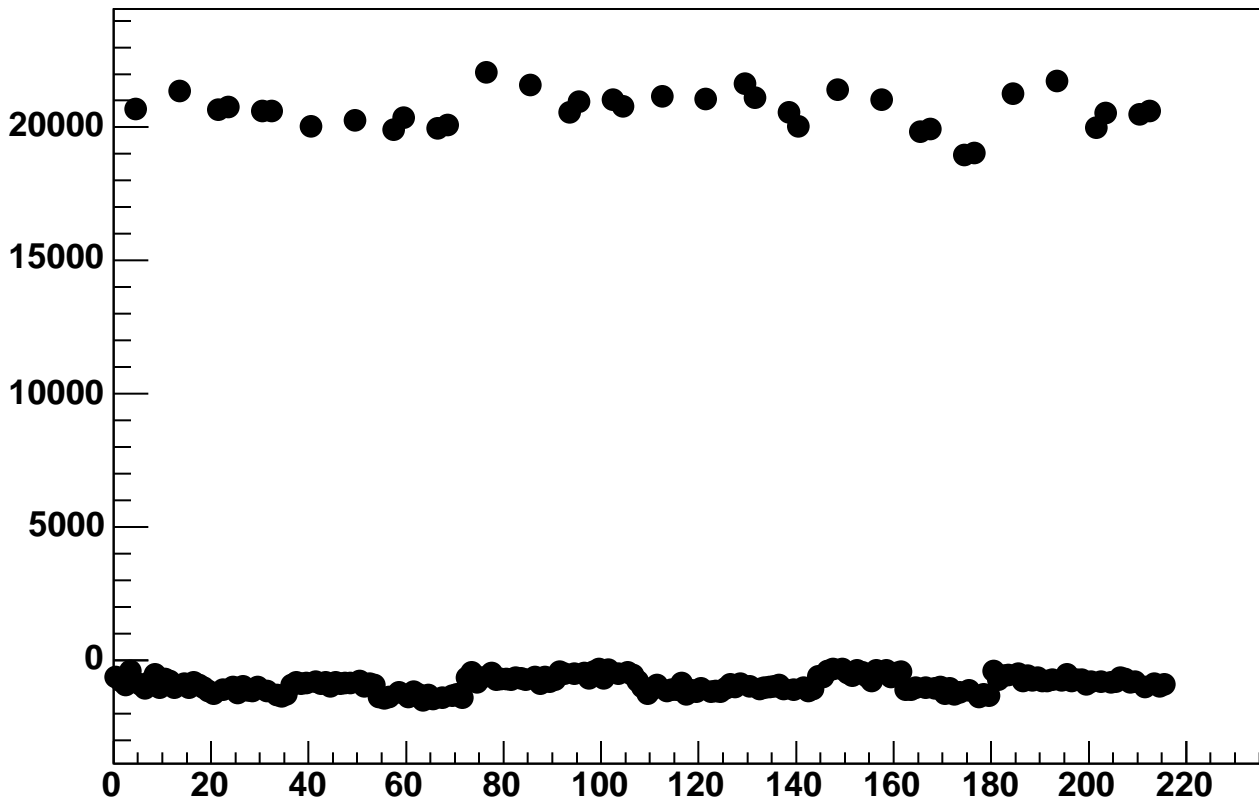
Enable 4, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan



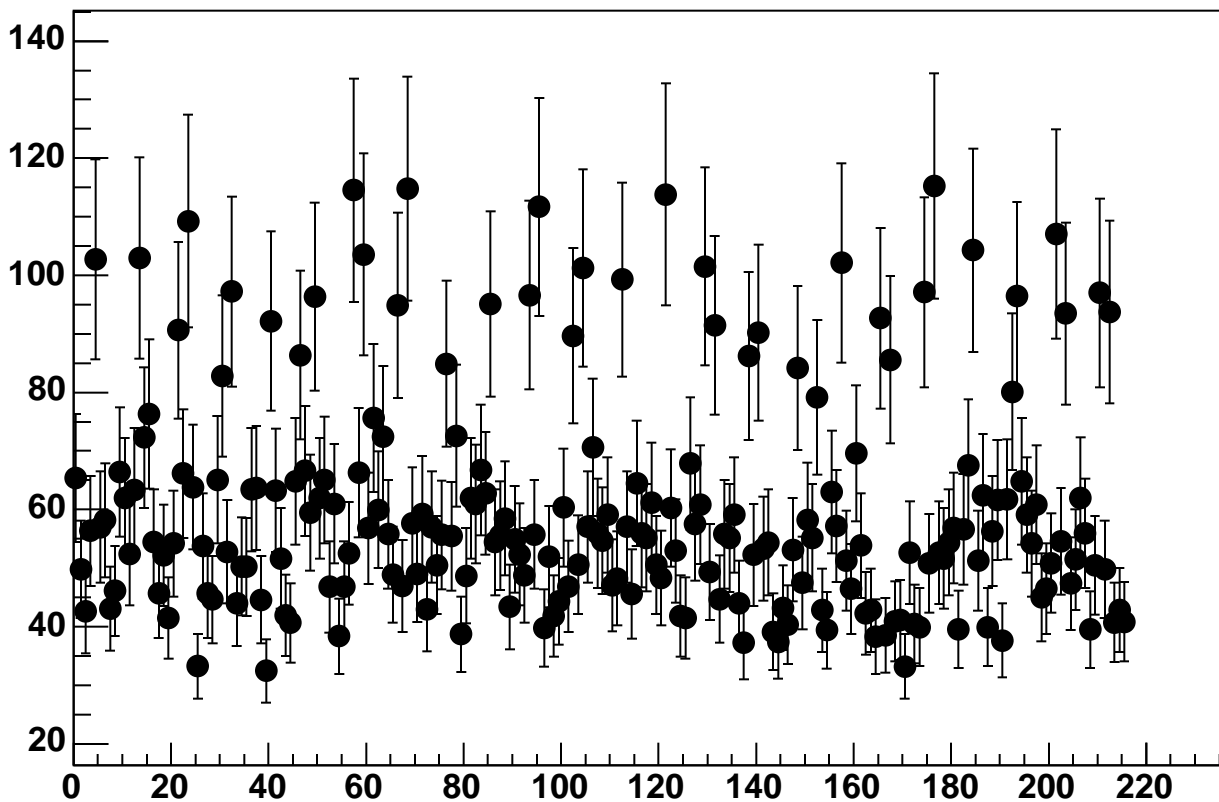
Enable 4, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan



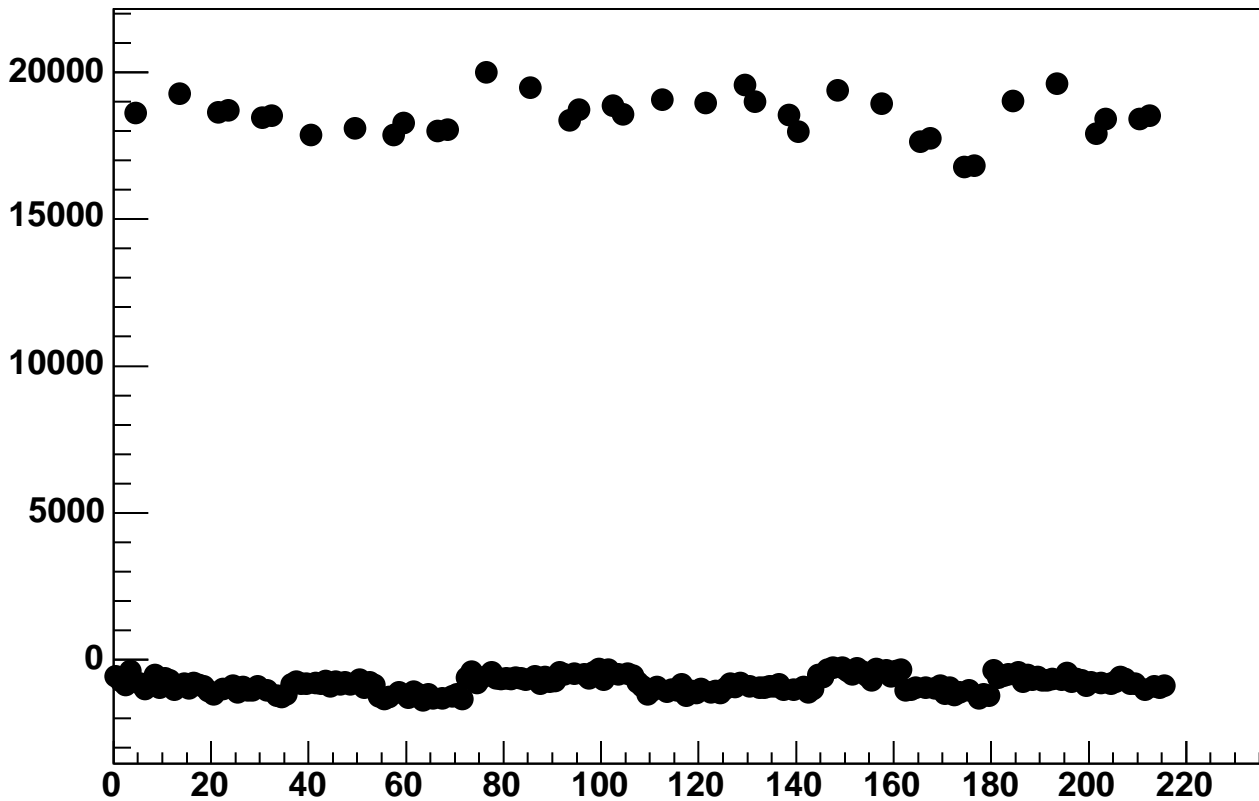
Enable 4, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



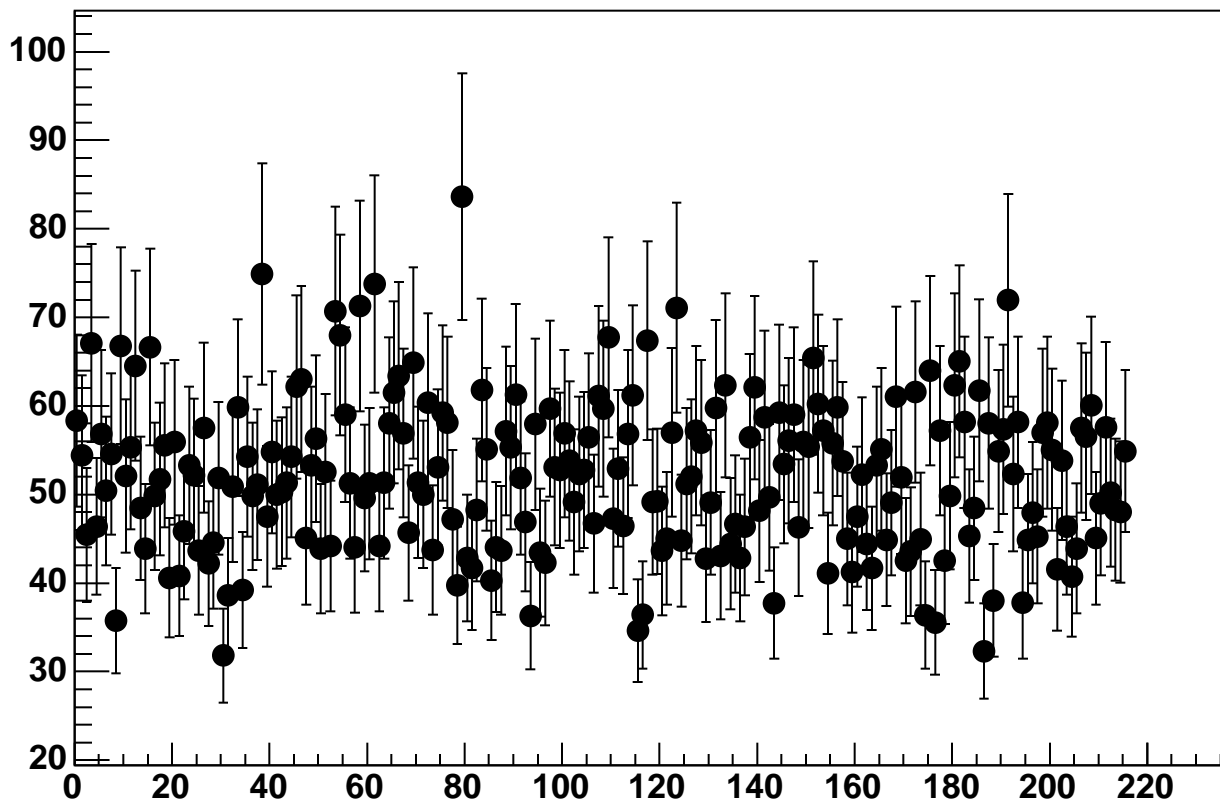
Enable 4, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan

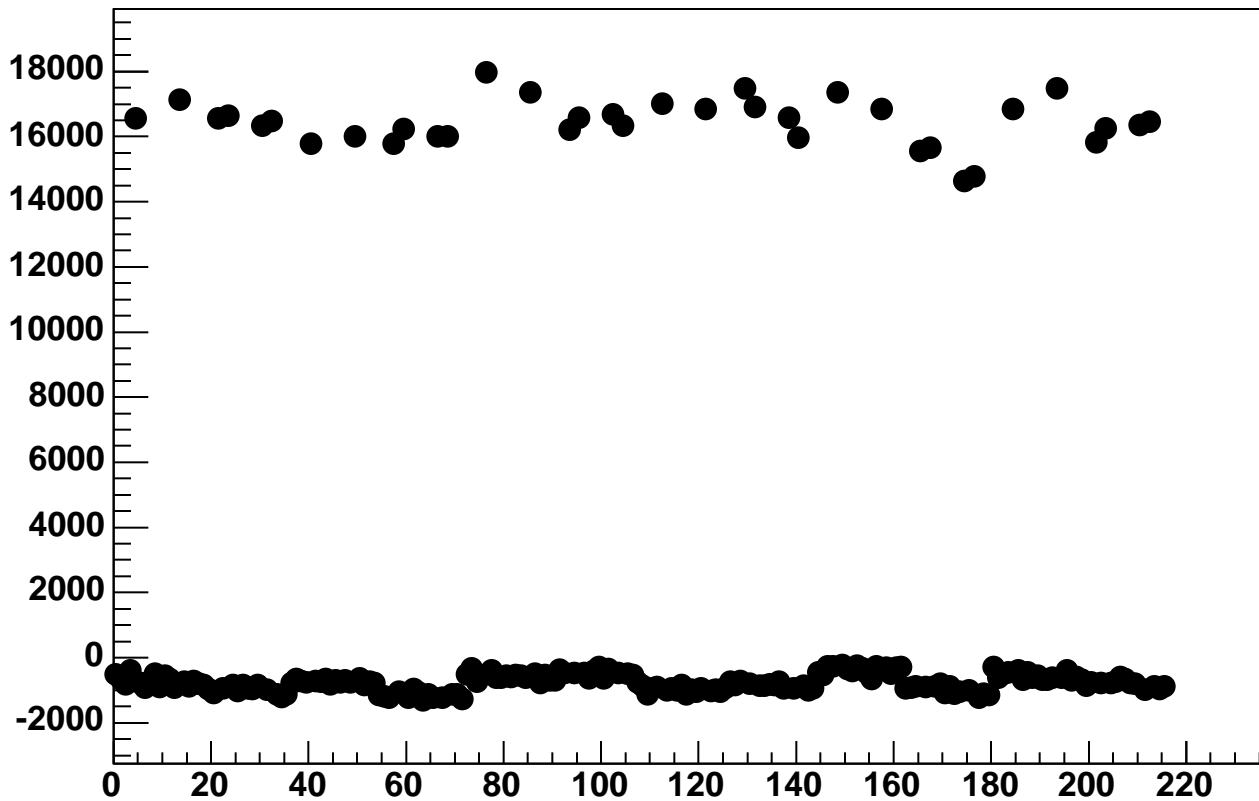


Enable 4, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan

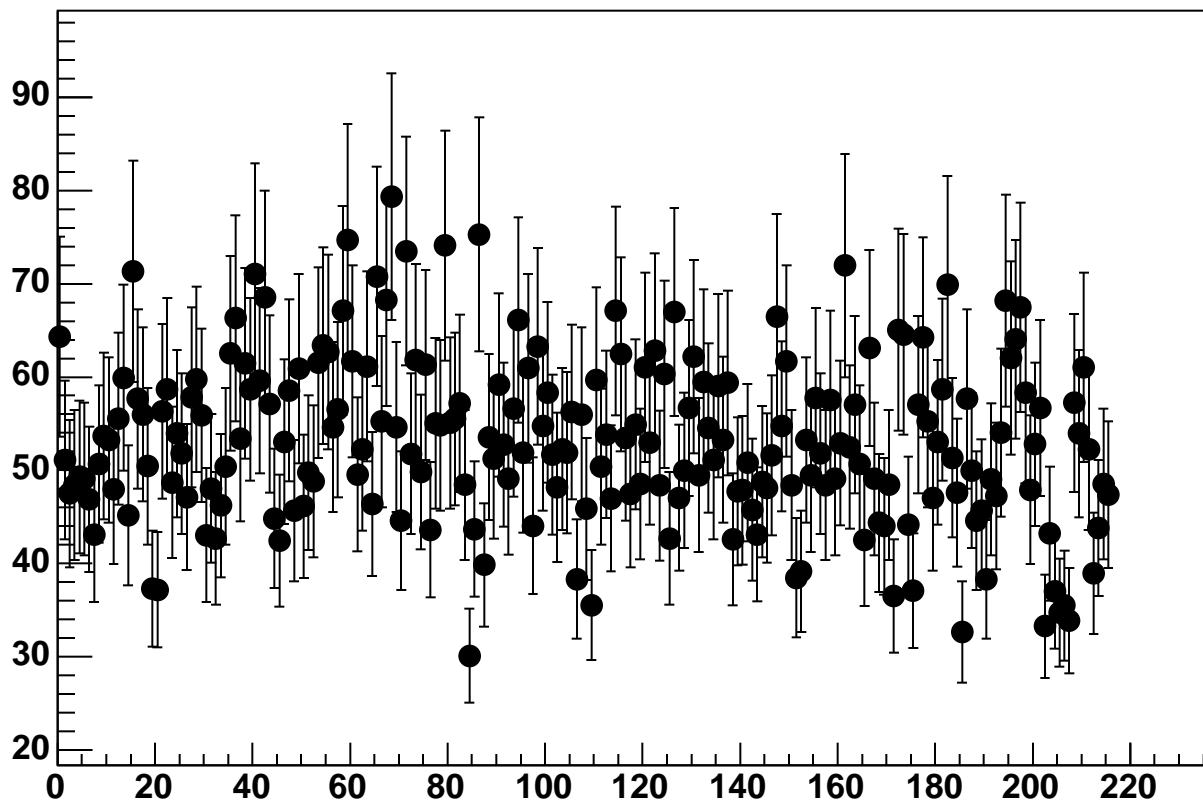




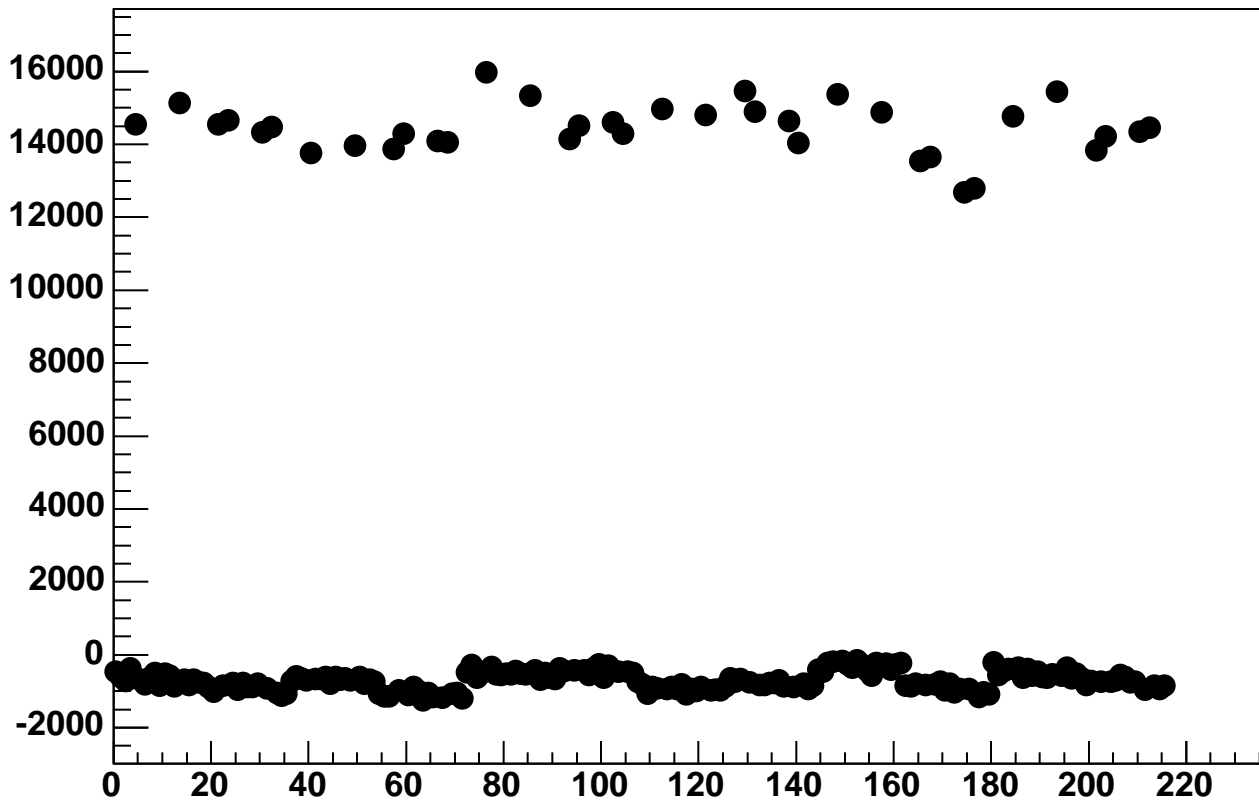
Enable 4, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



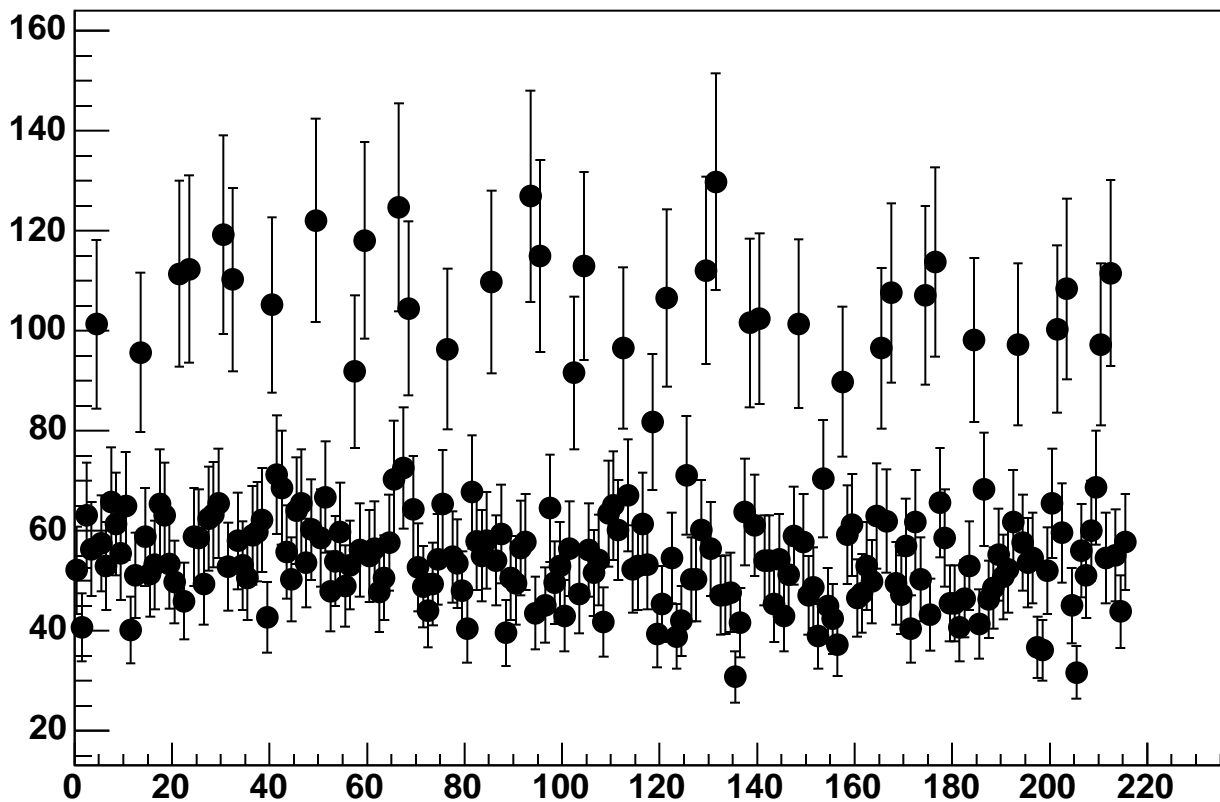
Enable 4, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



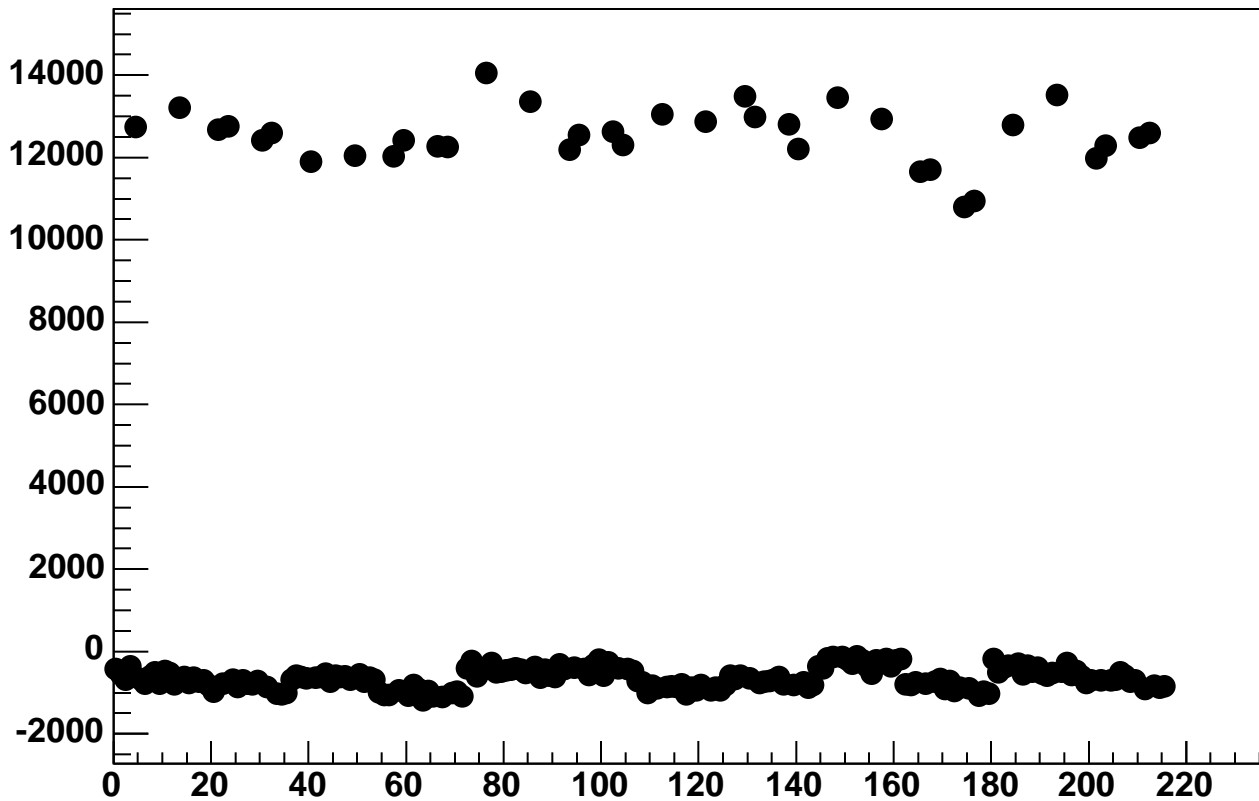
Enable 4, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan



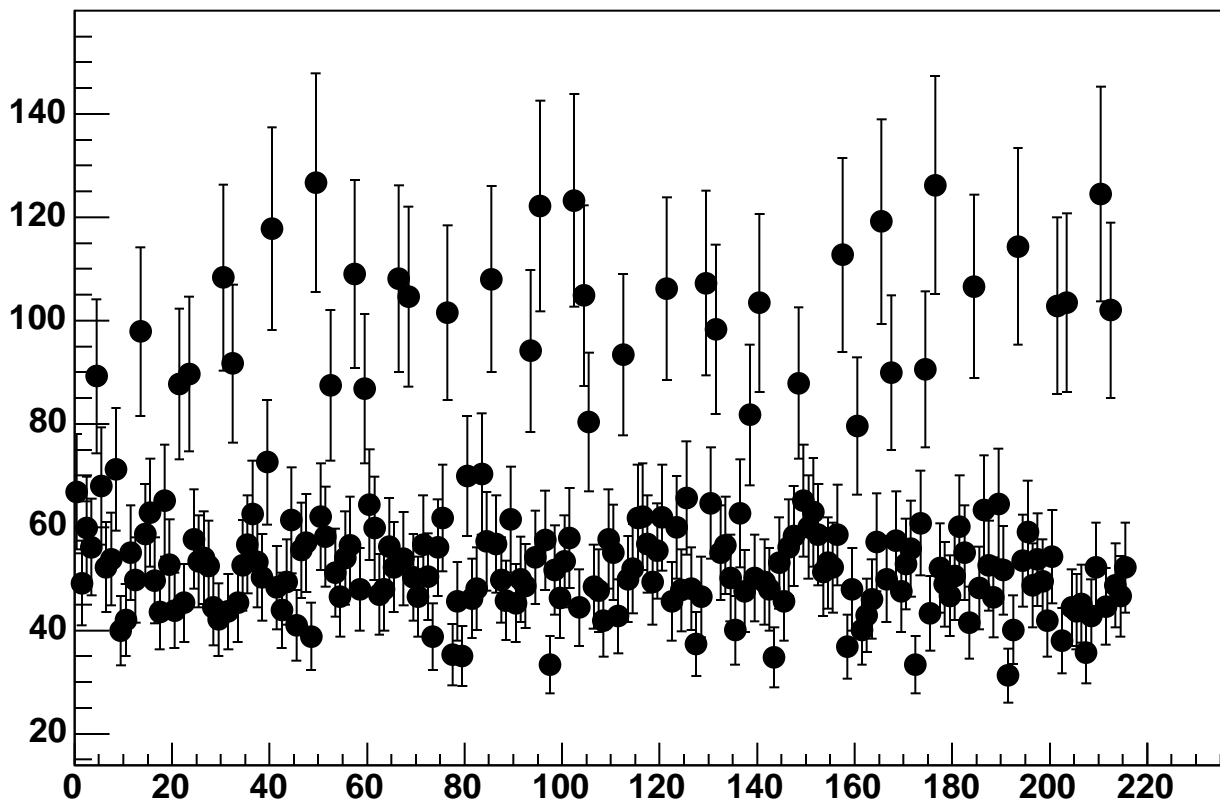
Enable 4, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan



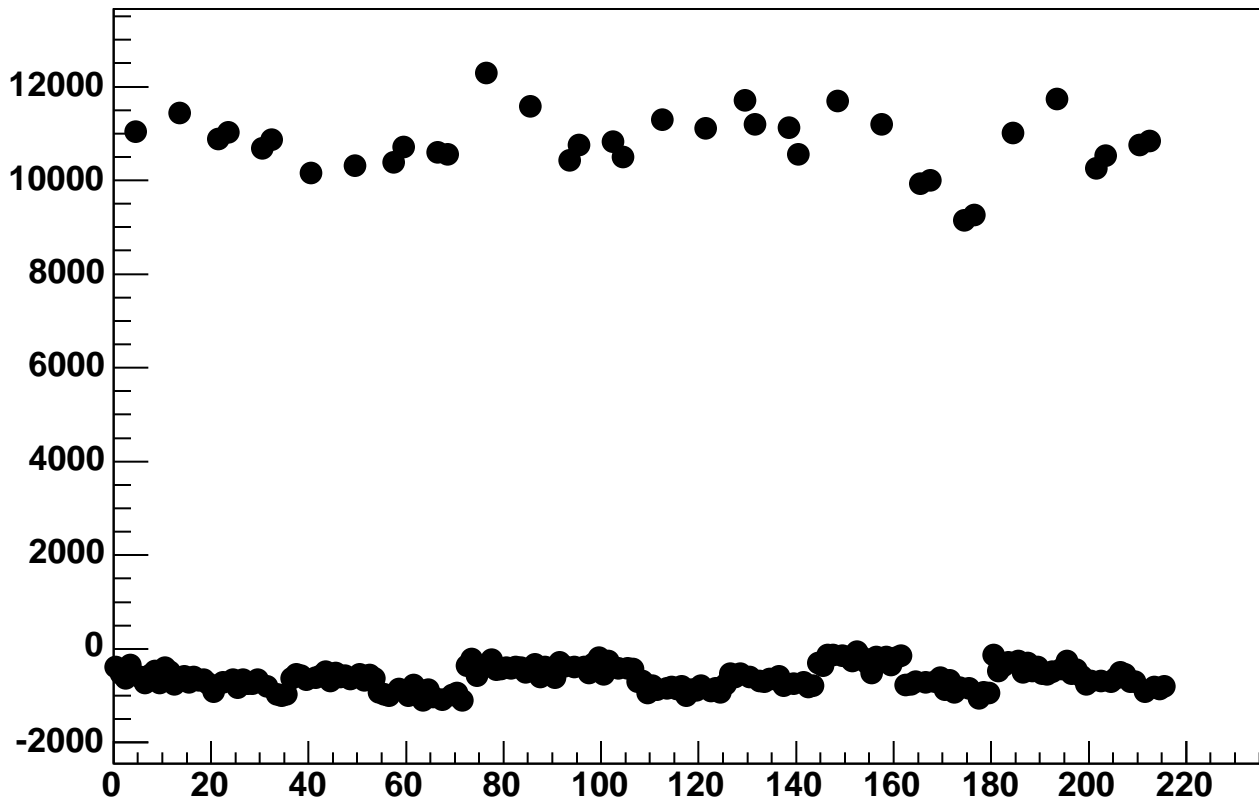
Enable 4, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



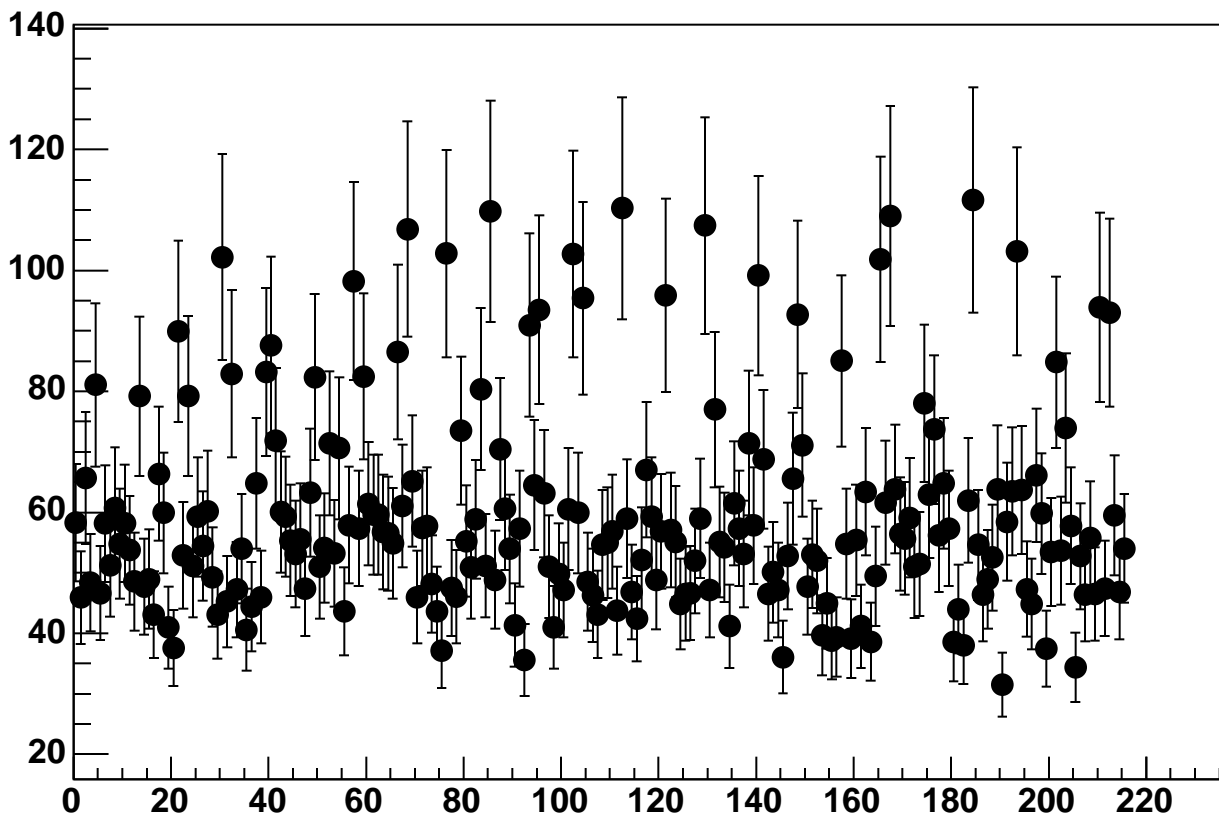
Enable 4, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



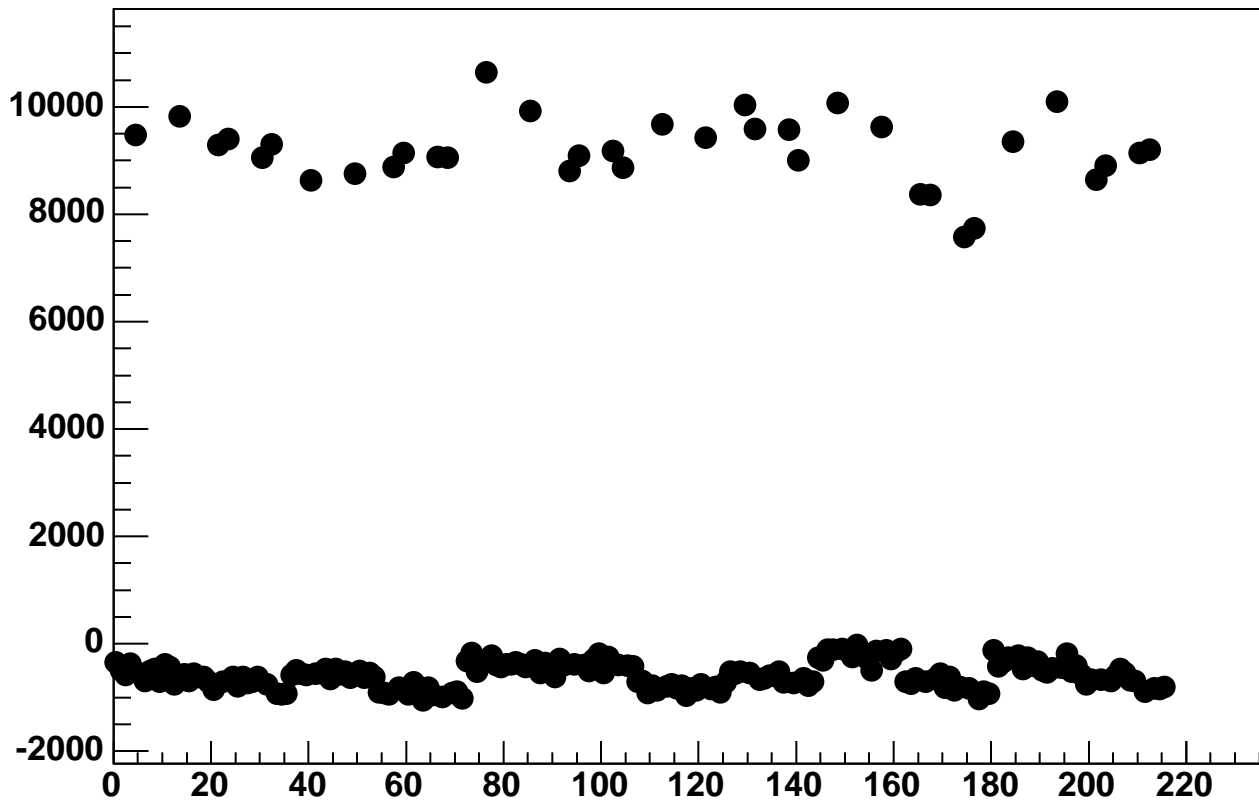
Enable 4, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan



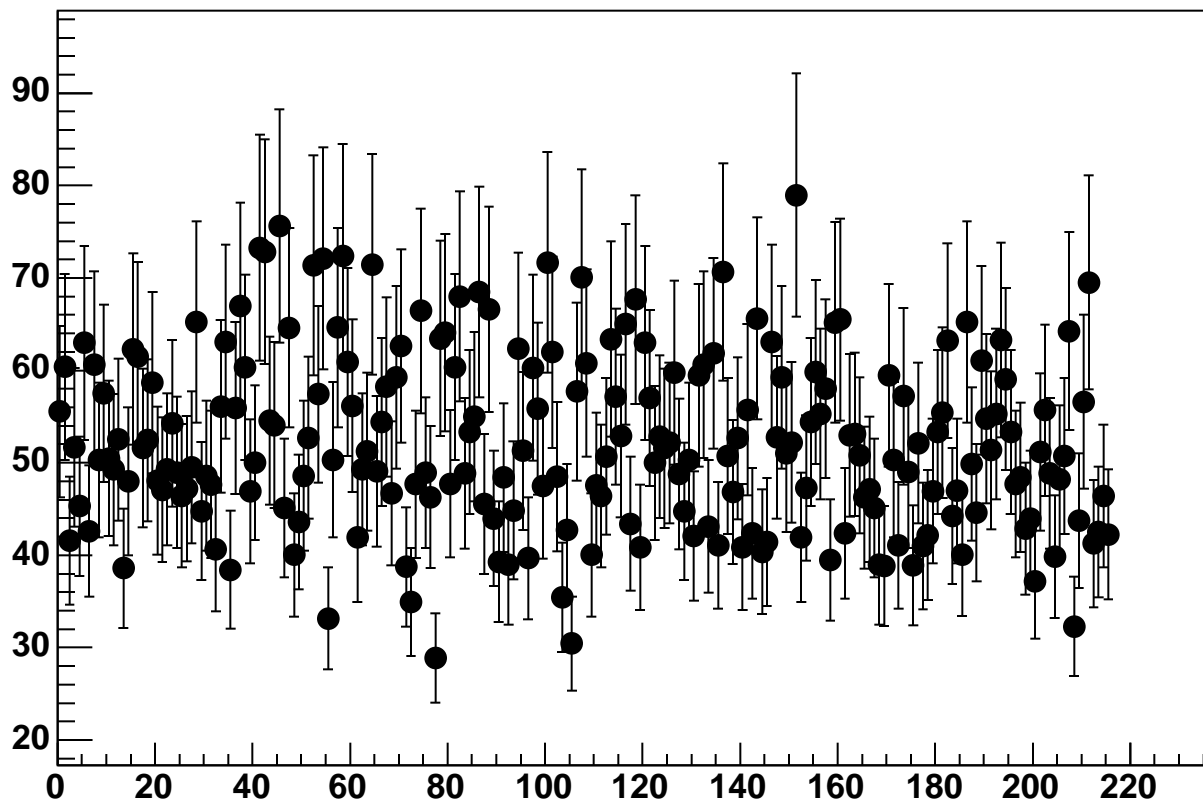
Enable 4, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan



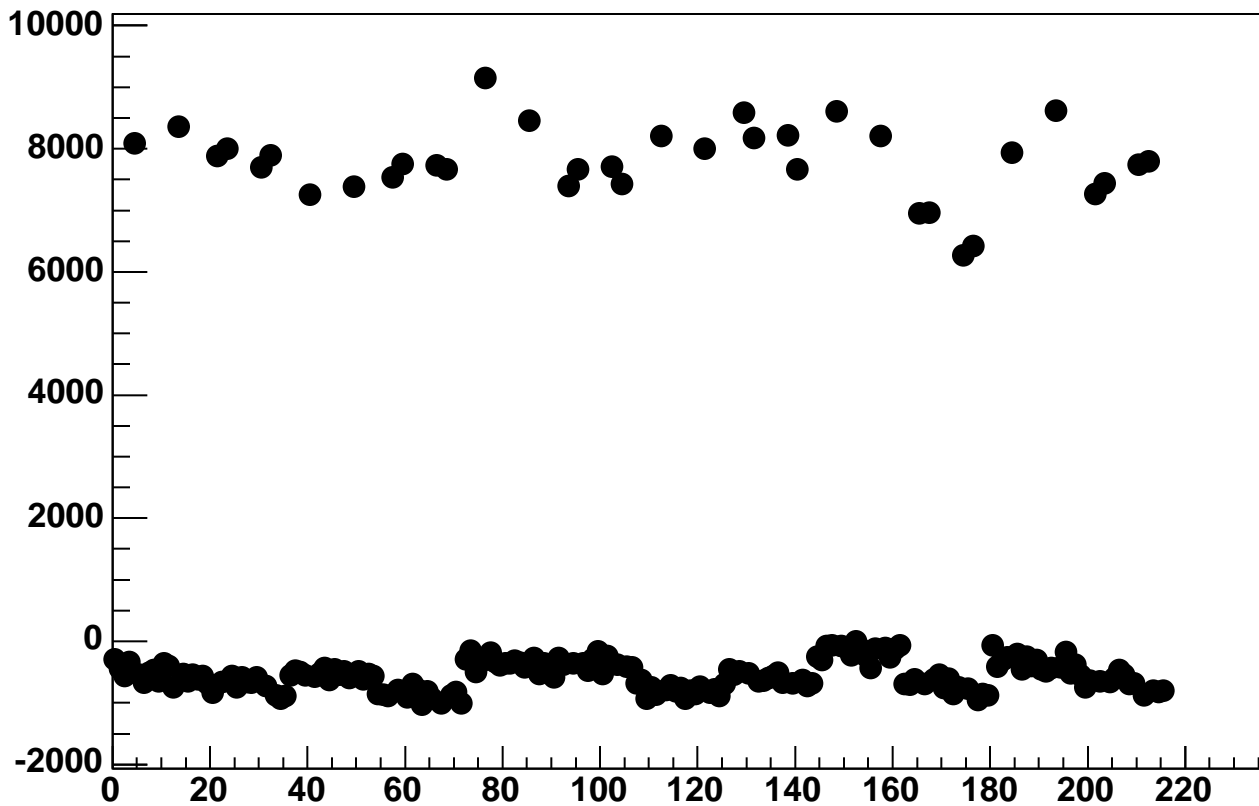
Enable 4, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



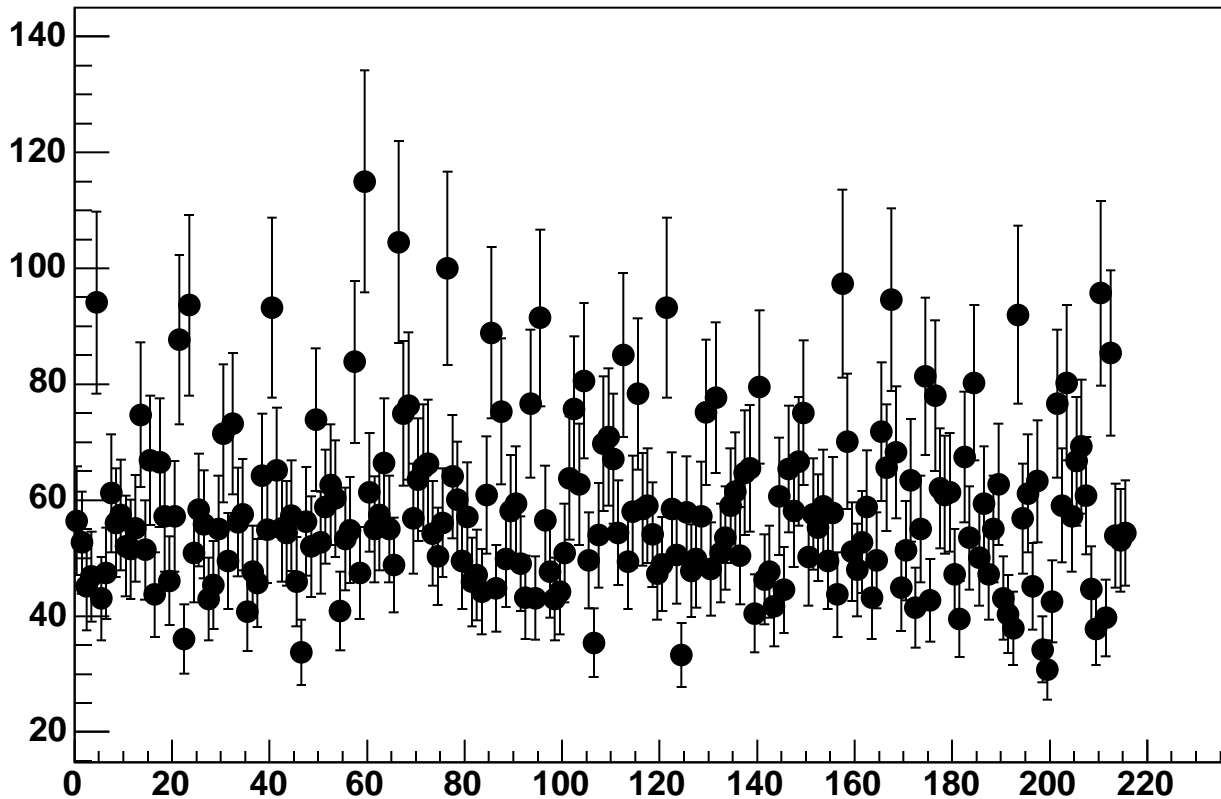
Enable 4, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



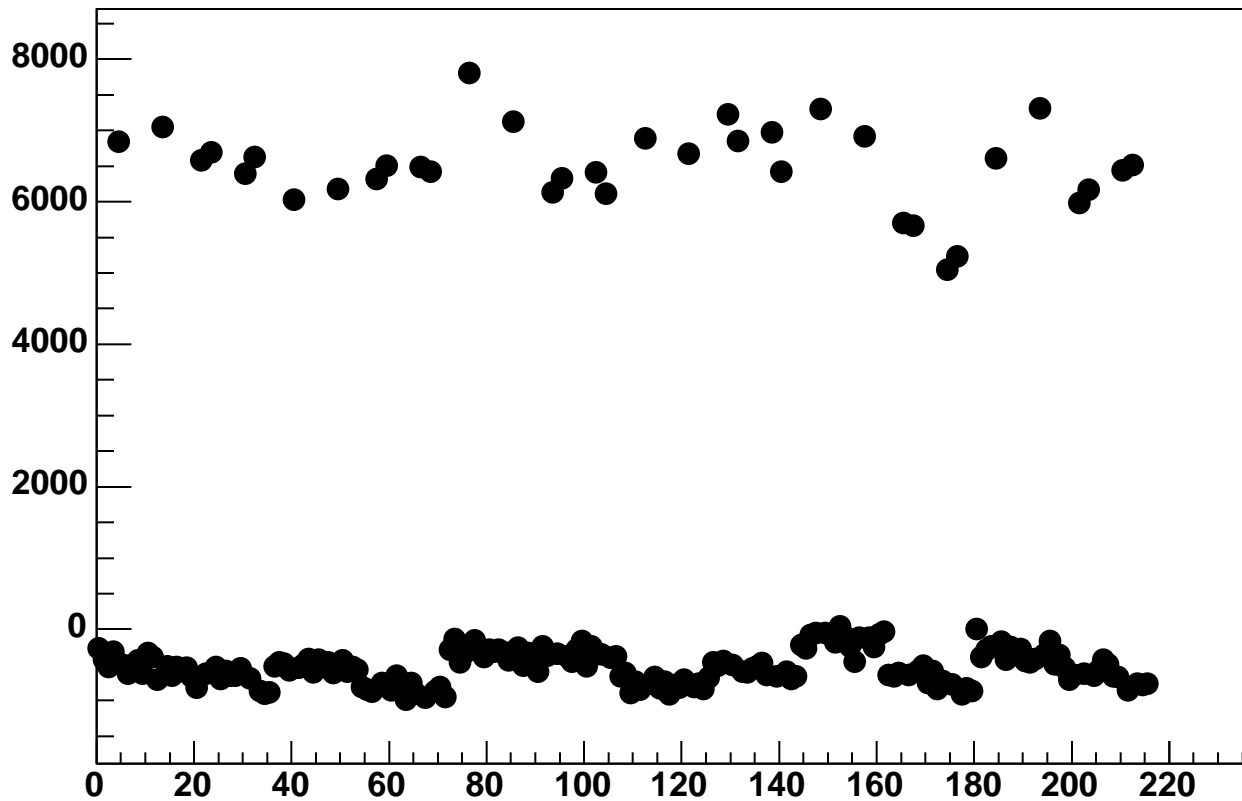
Enable 4, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan



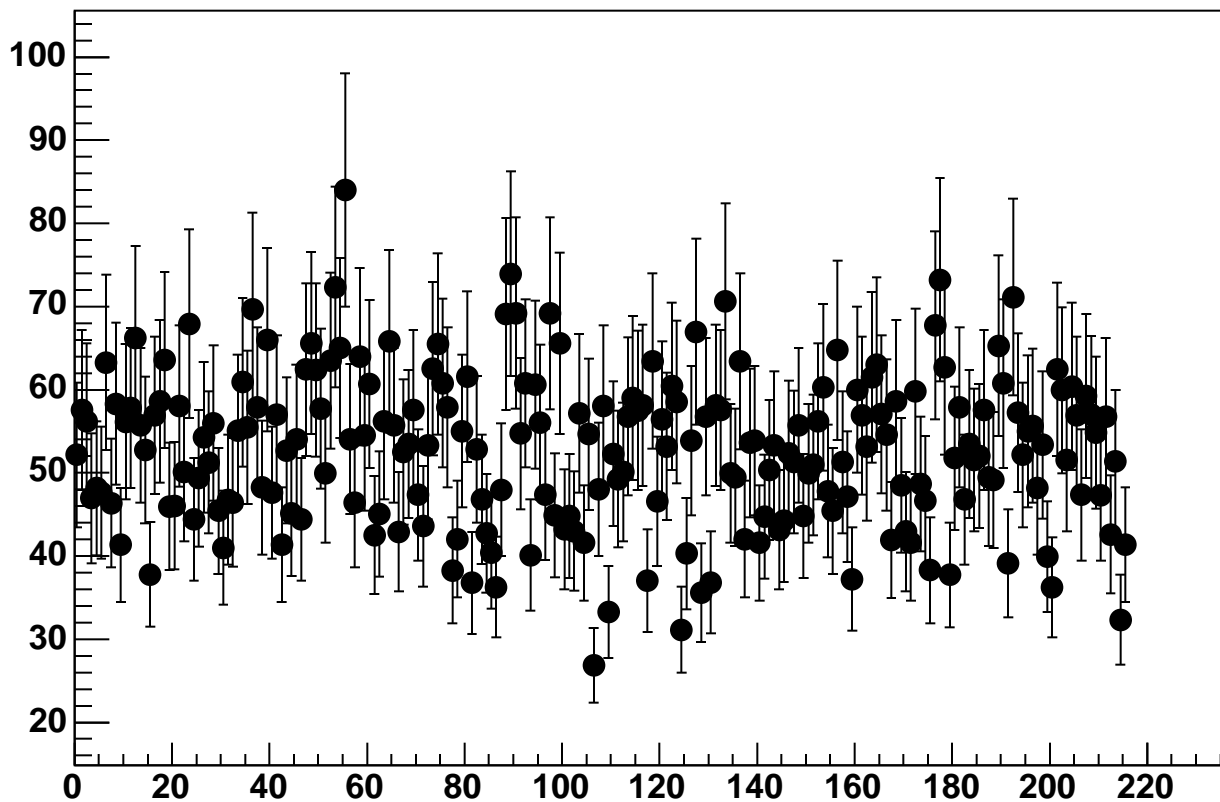
Enable 4, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan



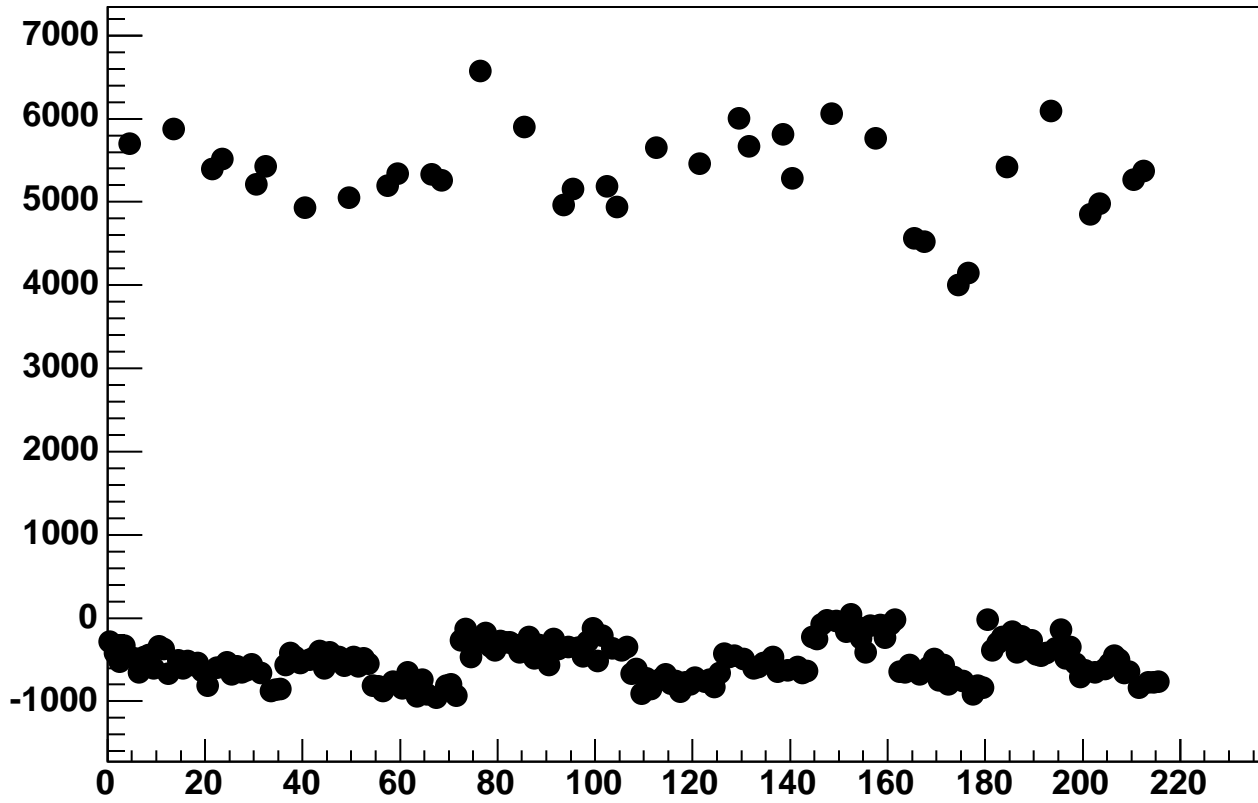
Enable 4, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



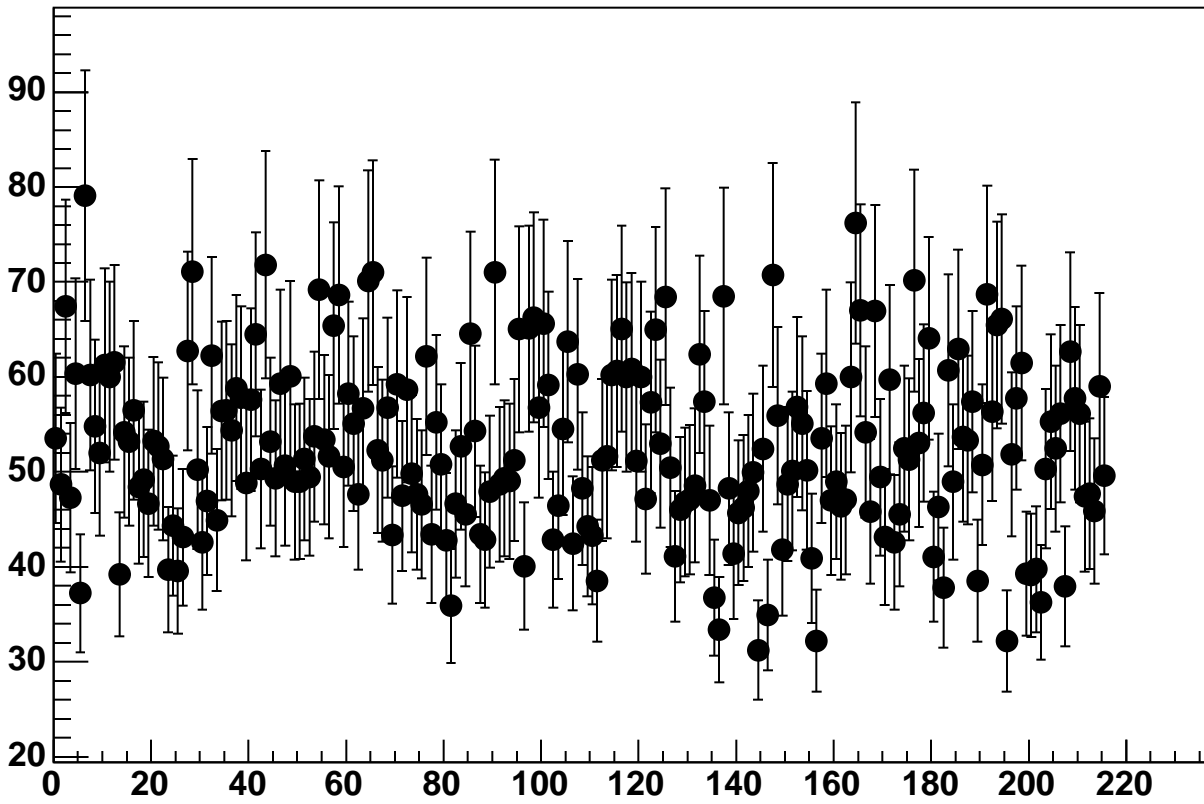
Enable 4, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan

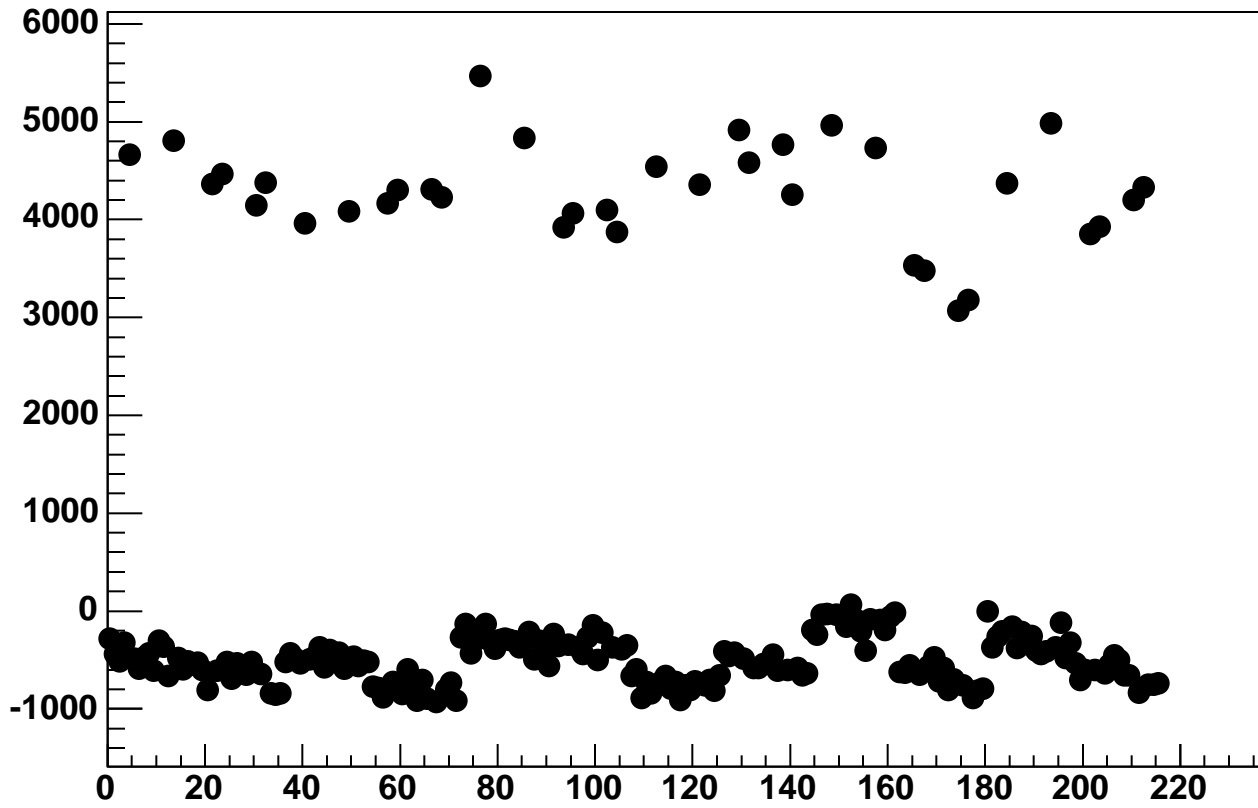


Enable 4, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan

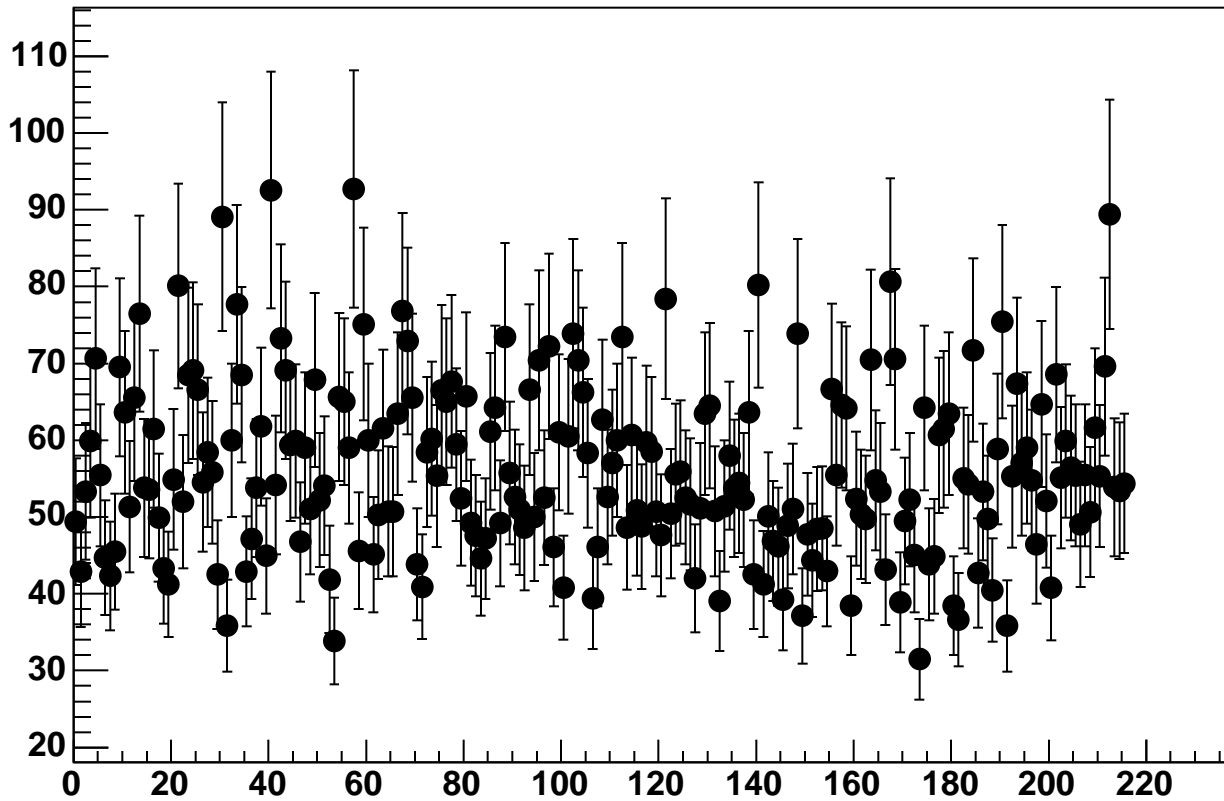




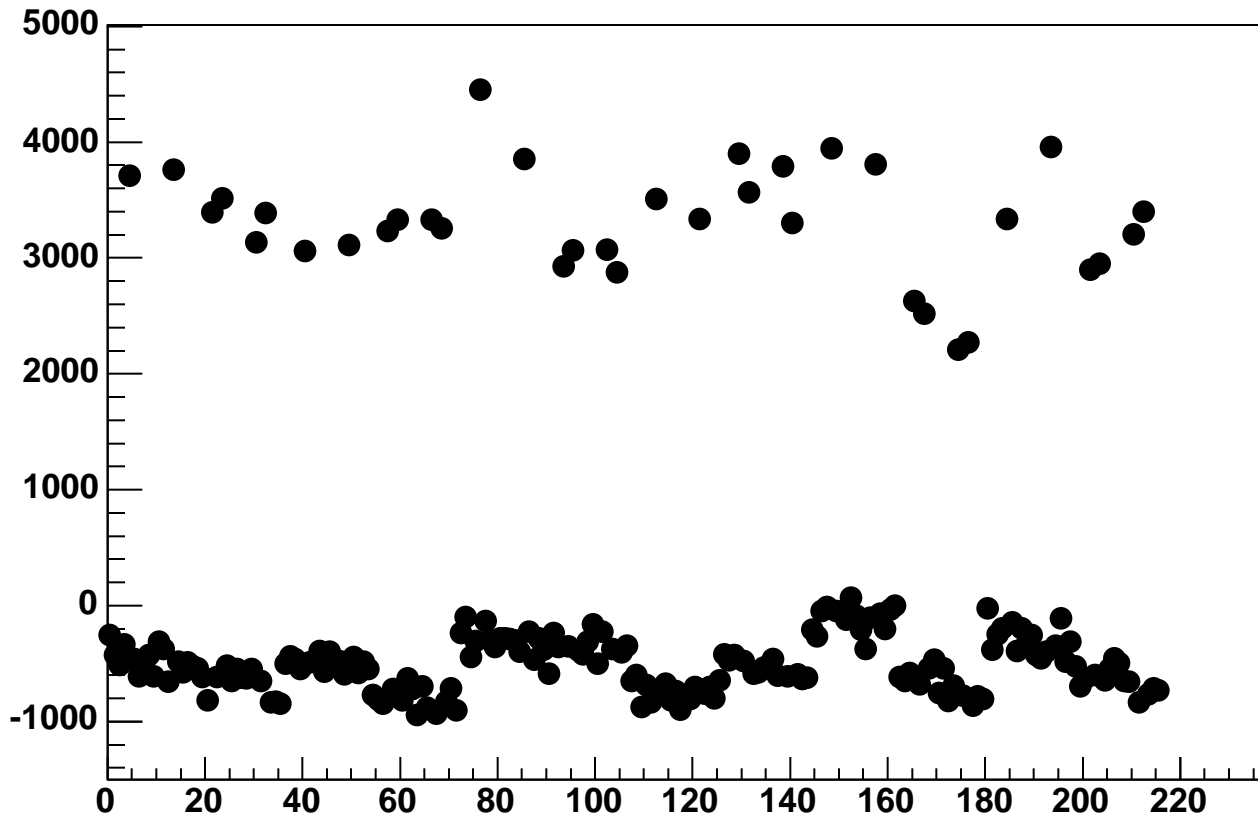
Enable 4, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



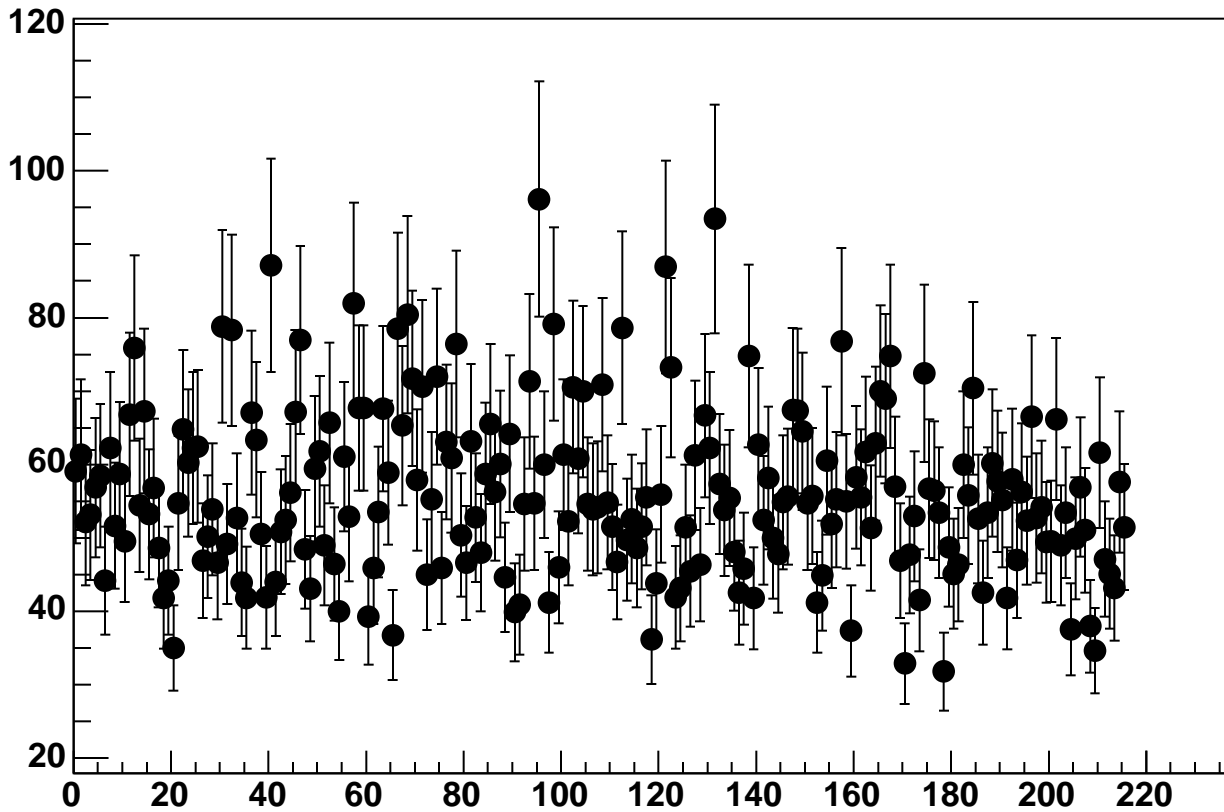
Enable 4, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



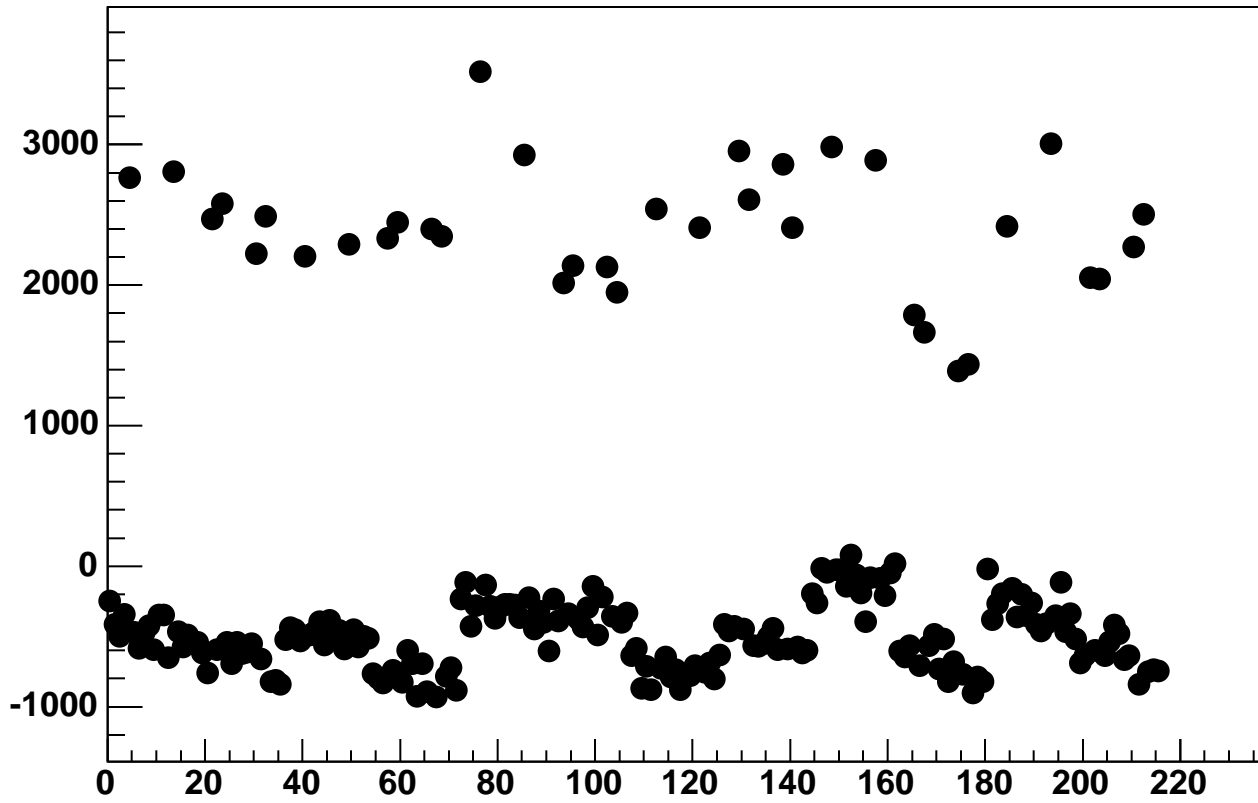
Enable 4, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan



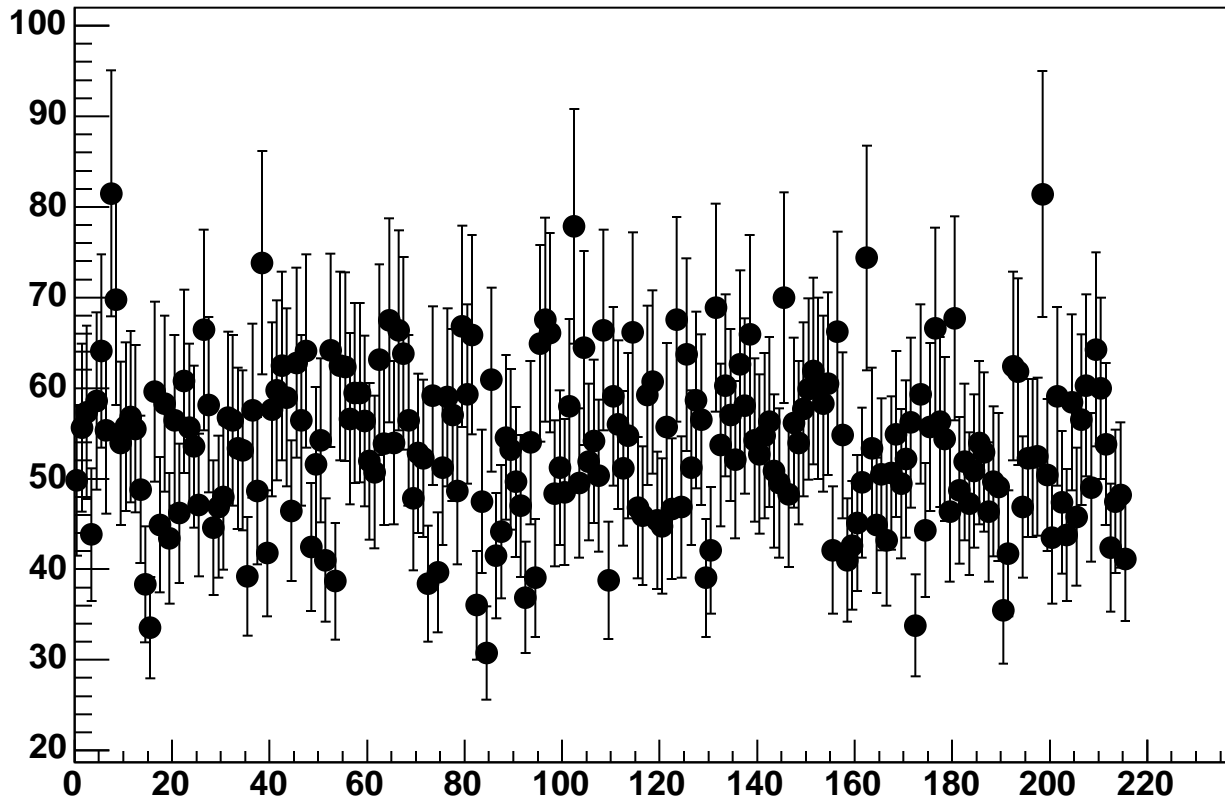
Enable 4, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan



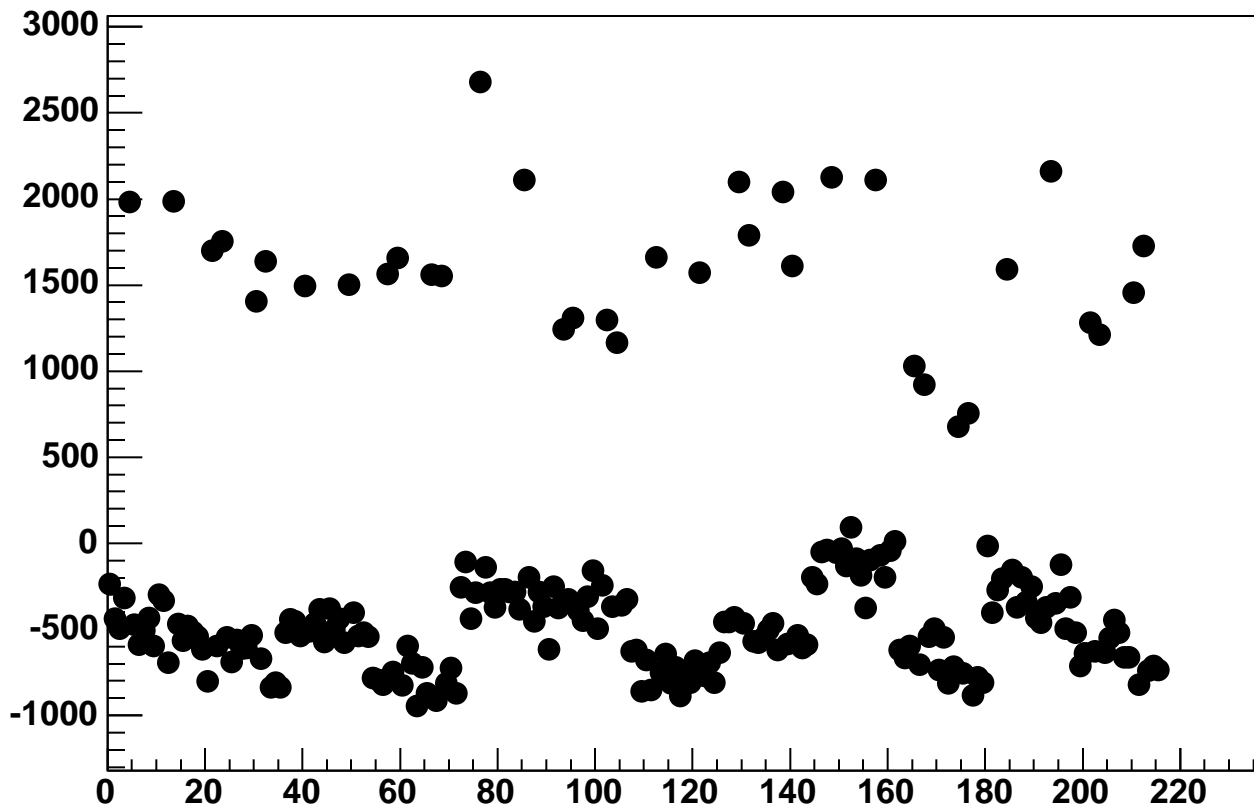
Enable 4, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



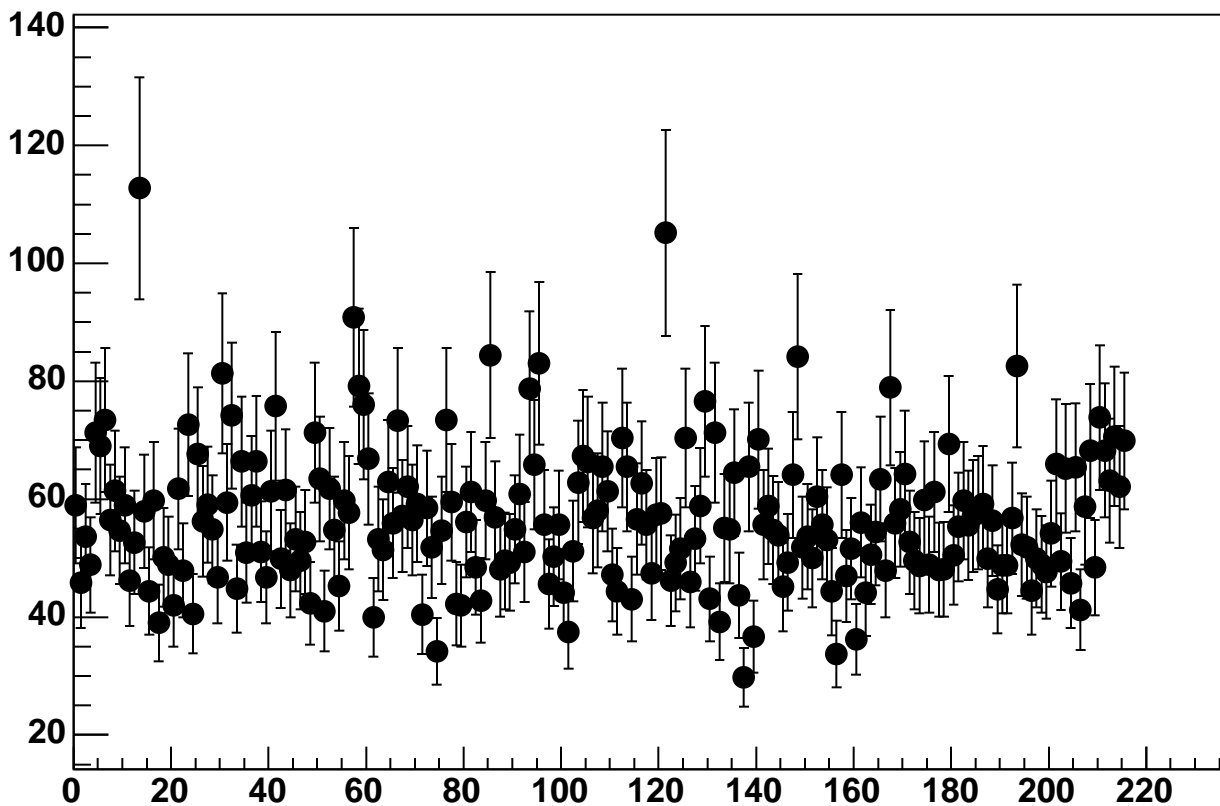
Enable 4, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



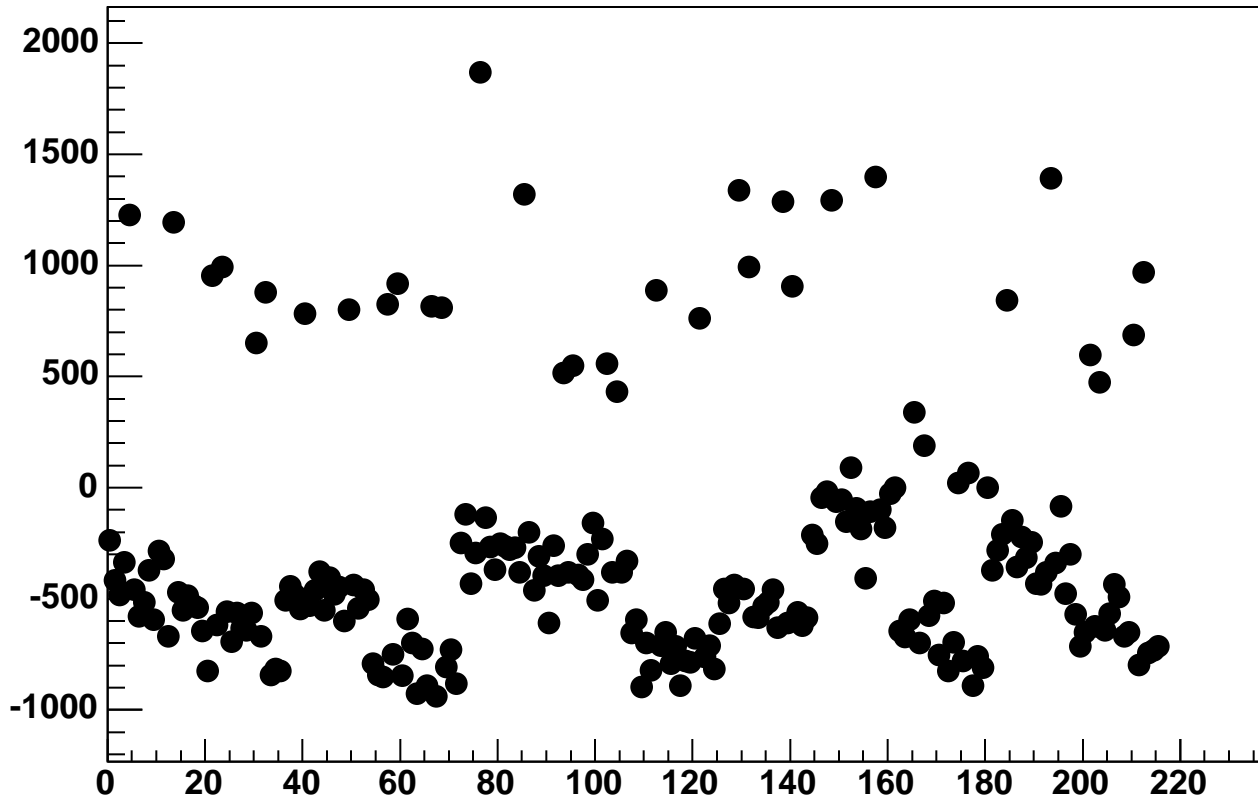
Enable 4, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan



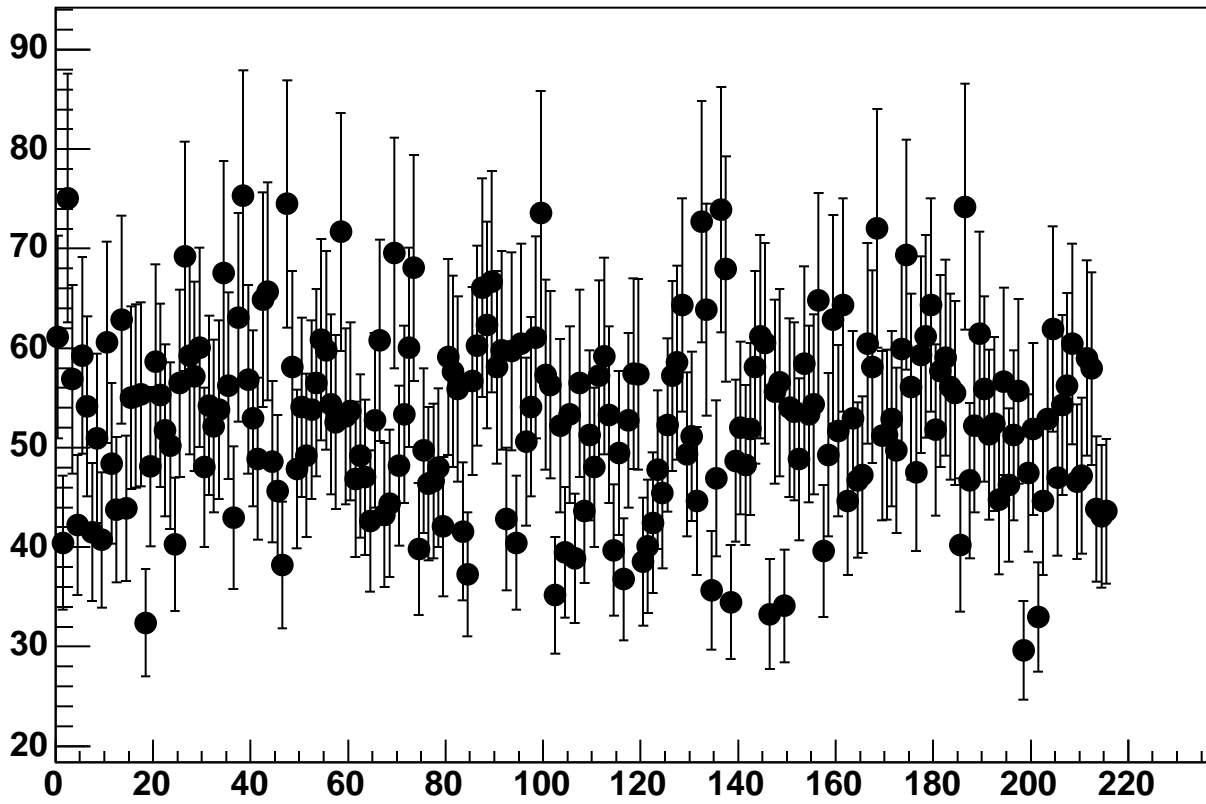
Enable 4, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan



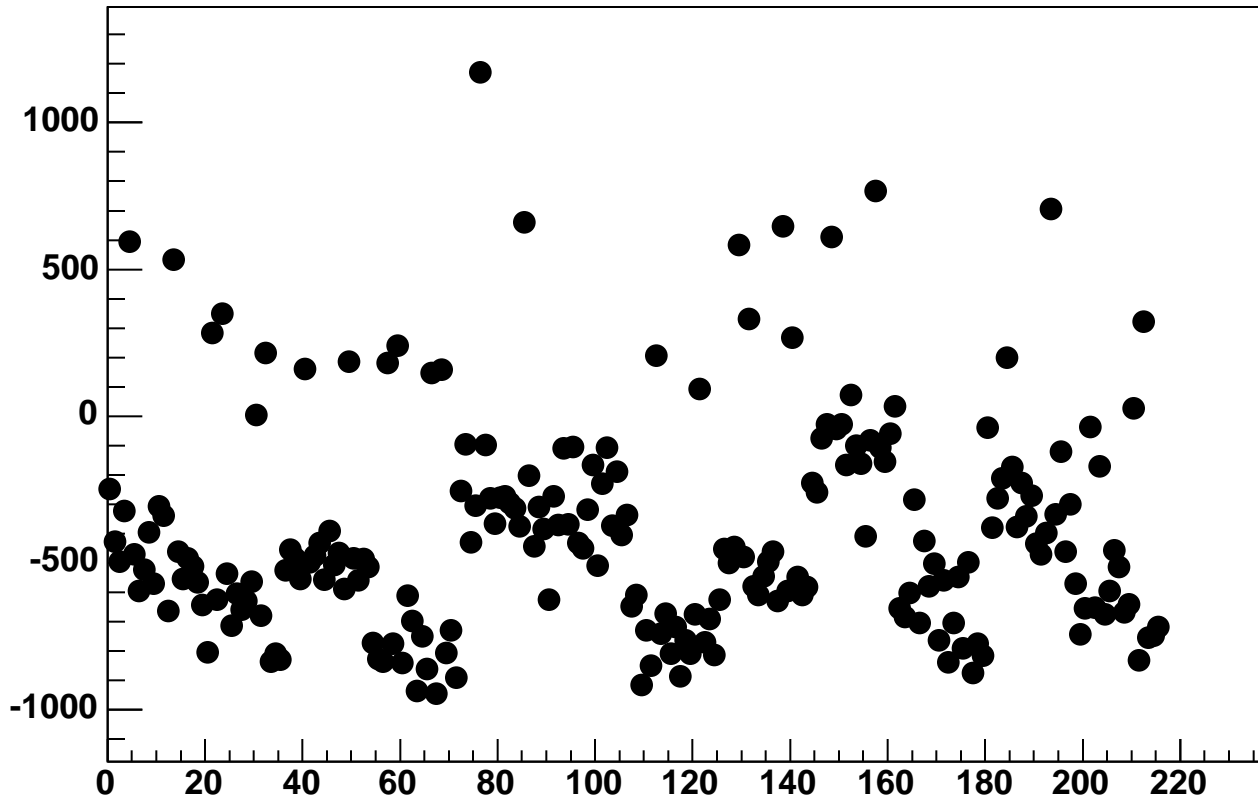
Enable 4, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



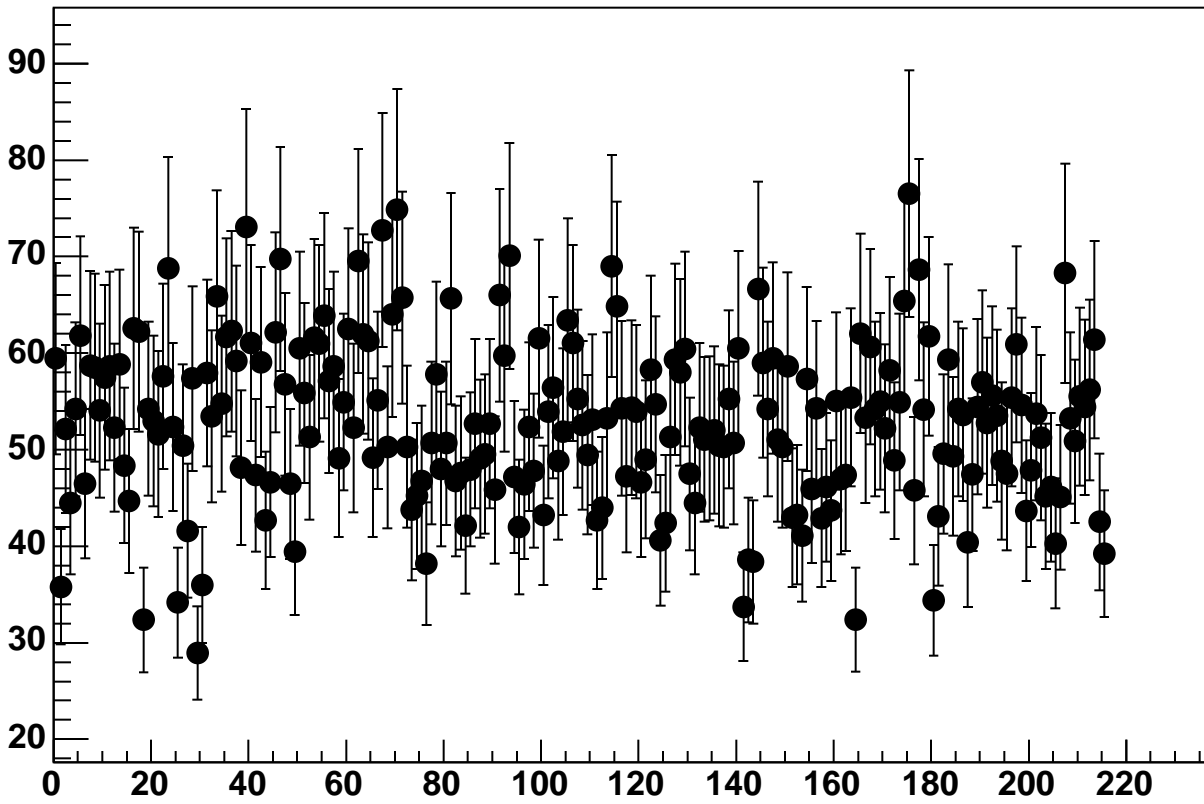
Enable 4, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



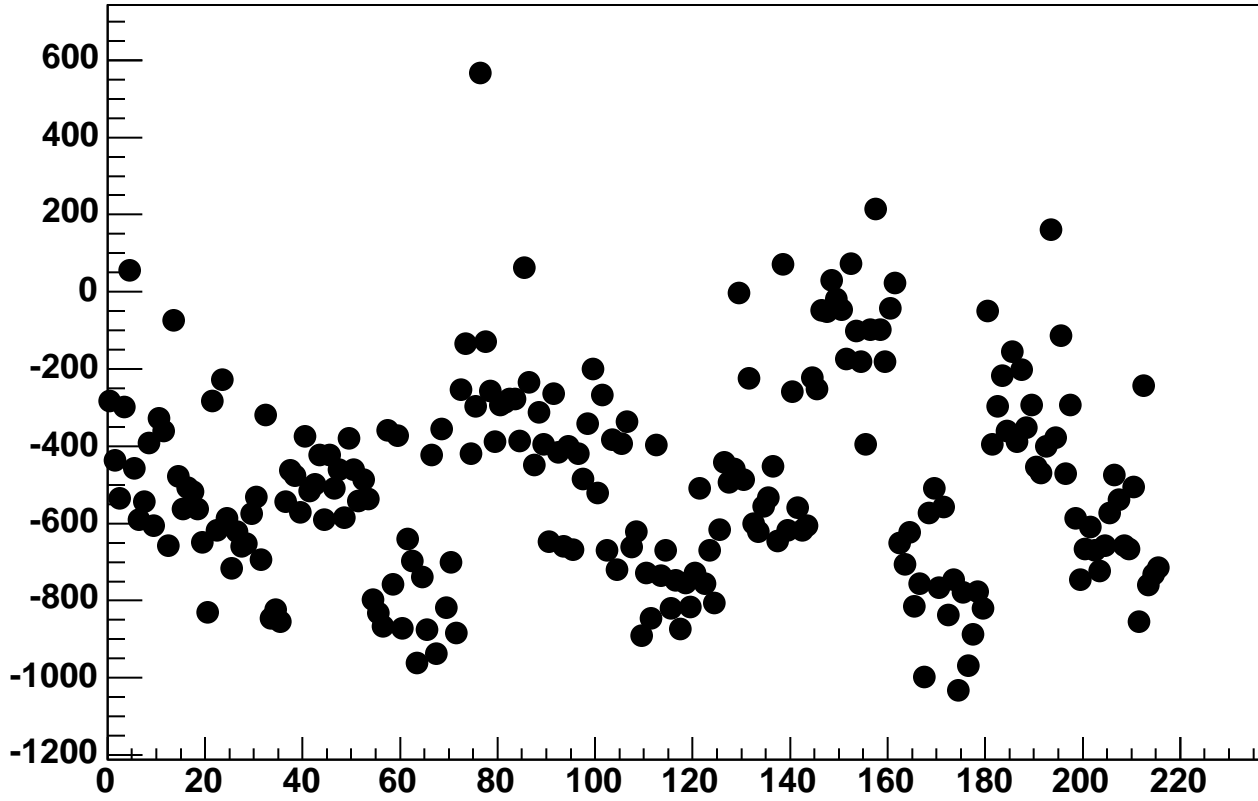
Enable 4, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan



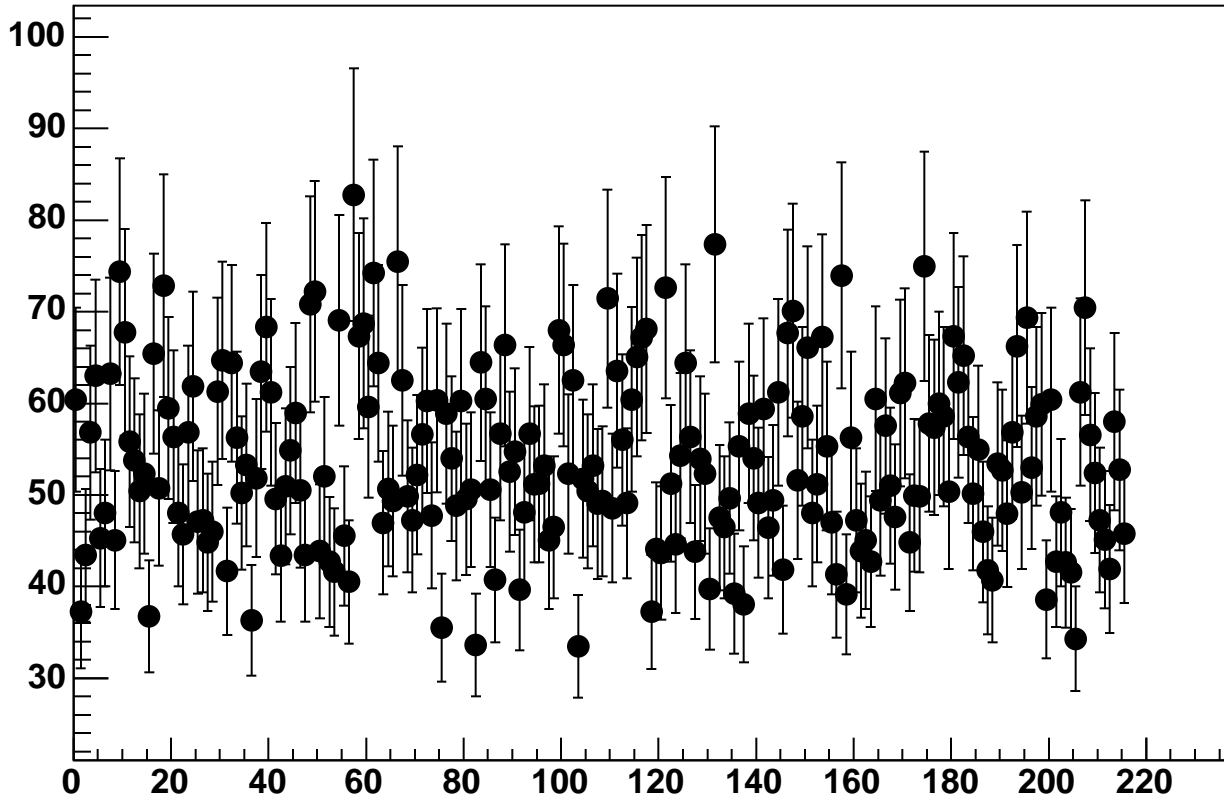
Enable 4, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan



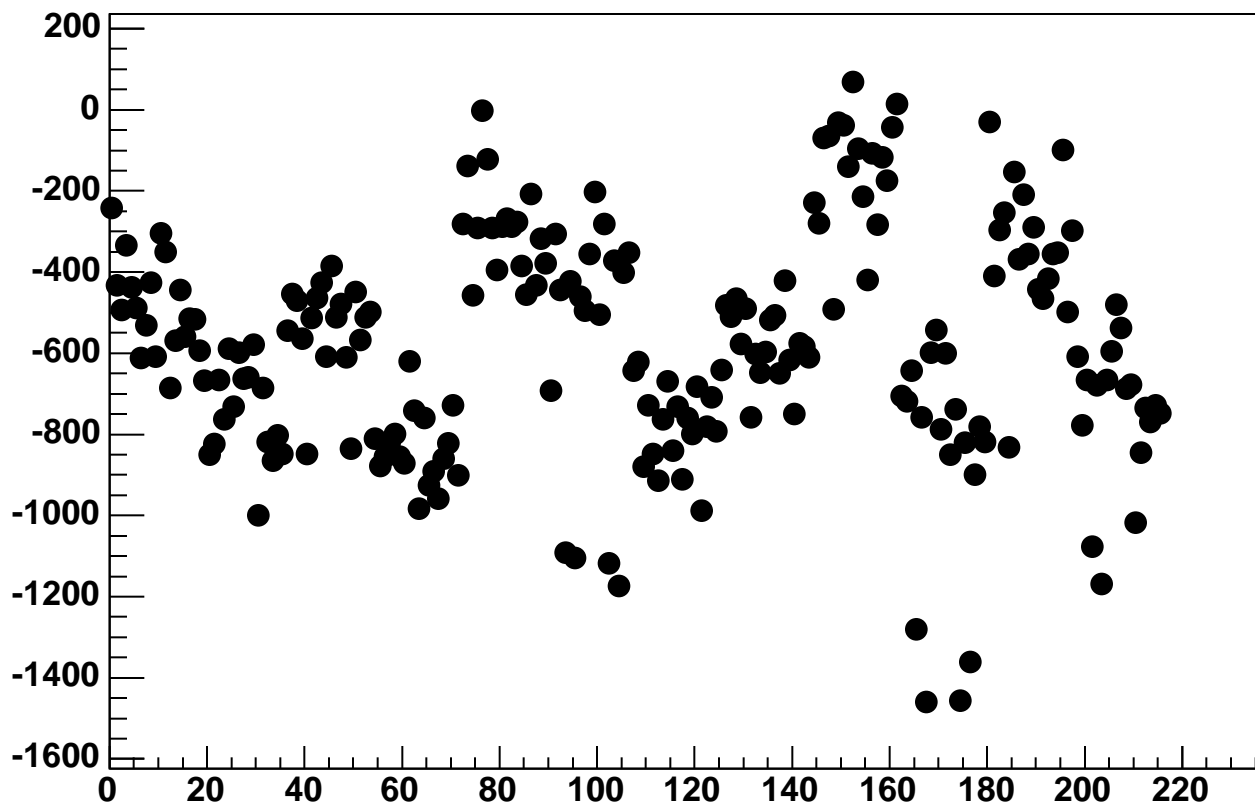
Enable 4, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



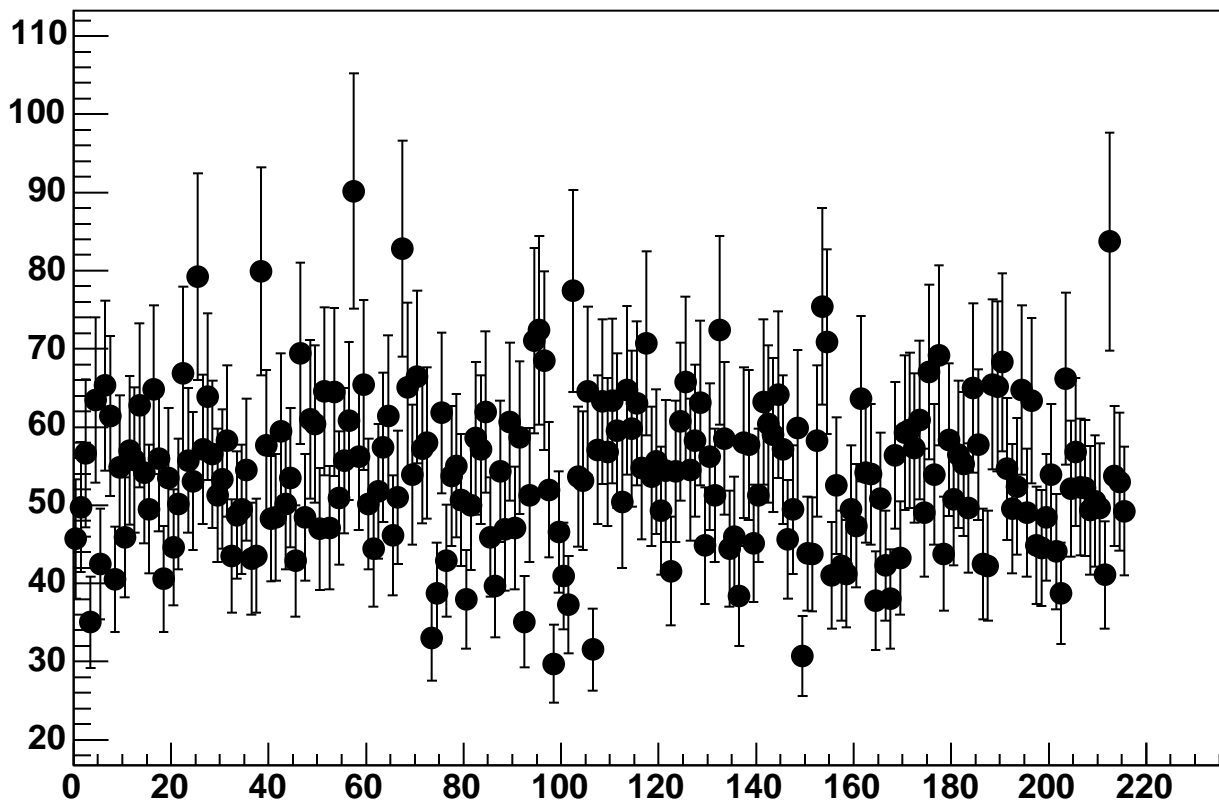
Enable 4, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan

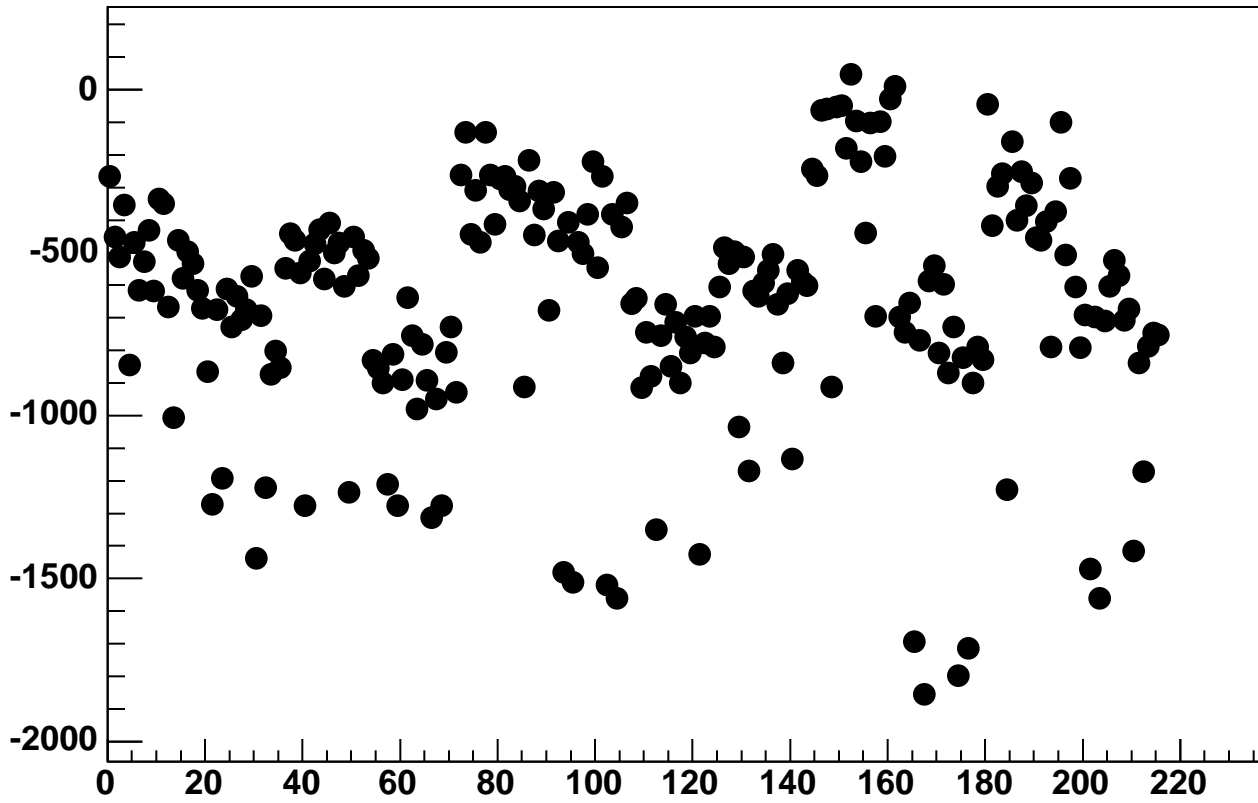


Enable 4, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan

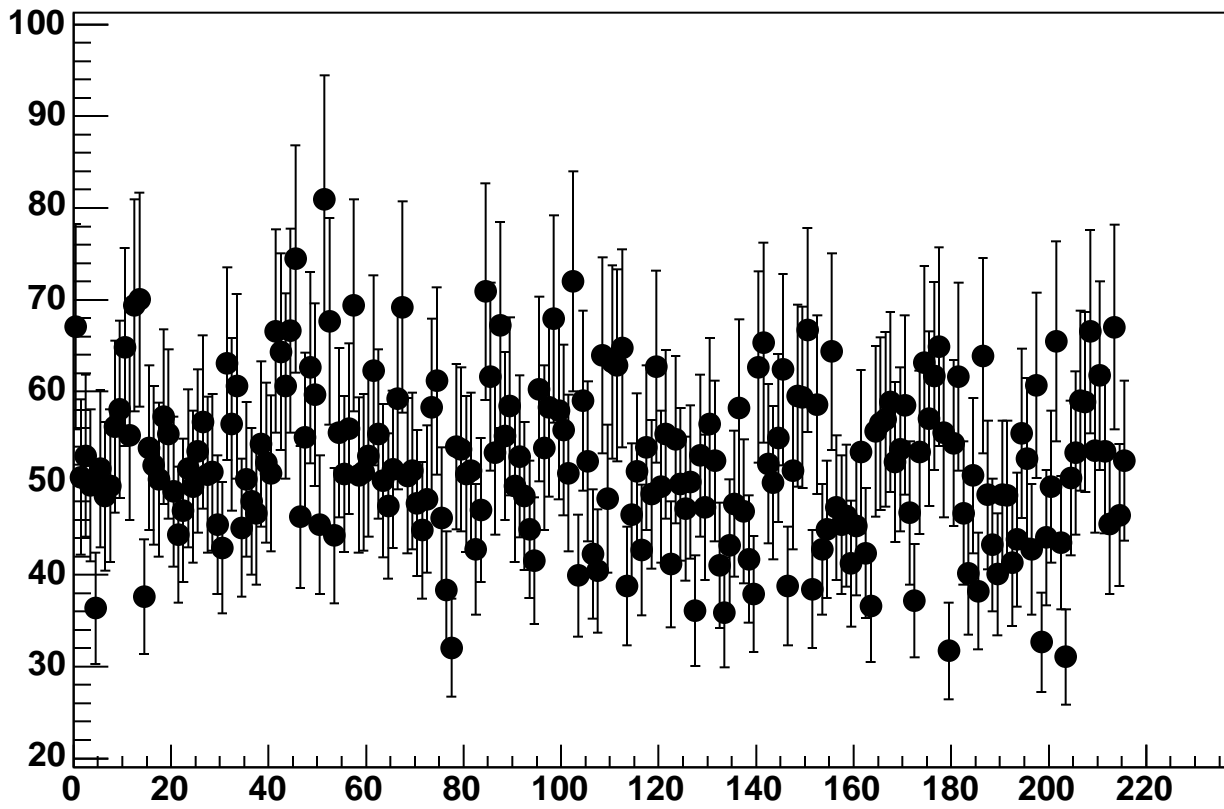




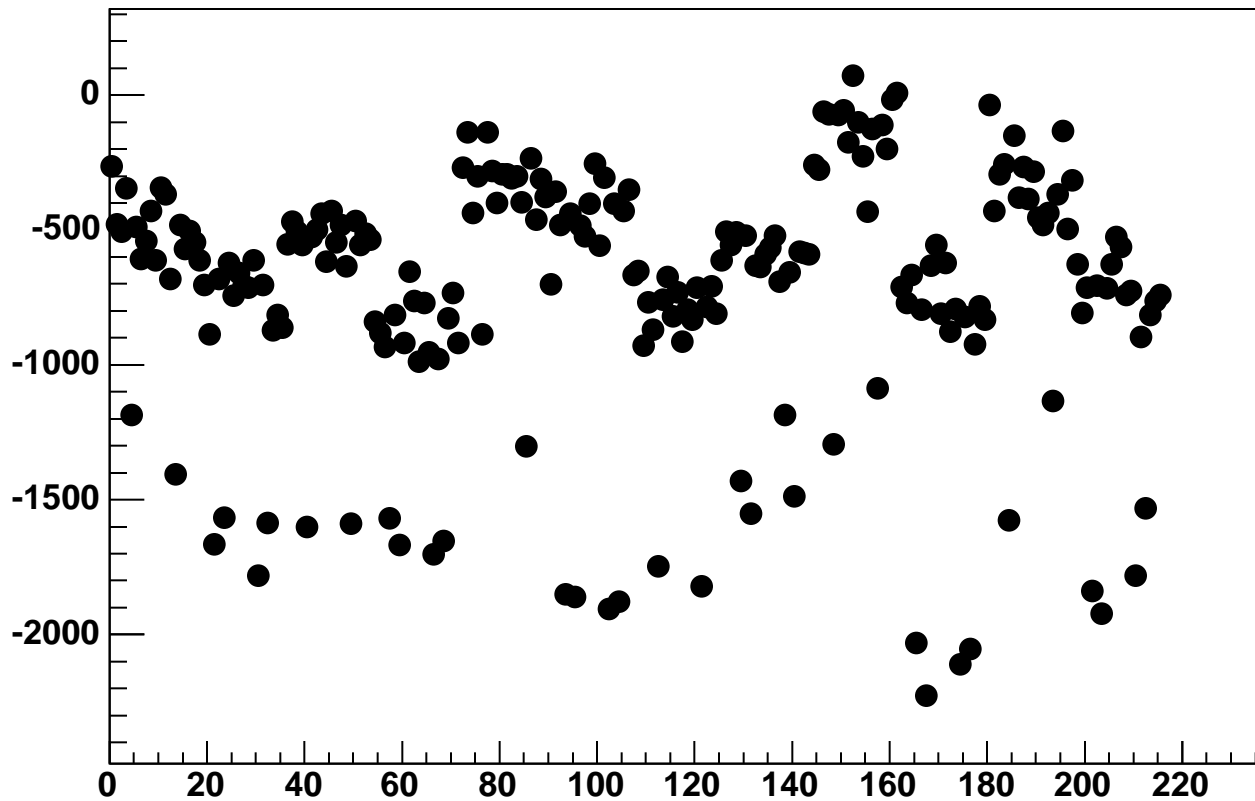
Enable 4, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



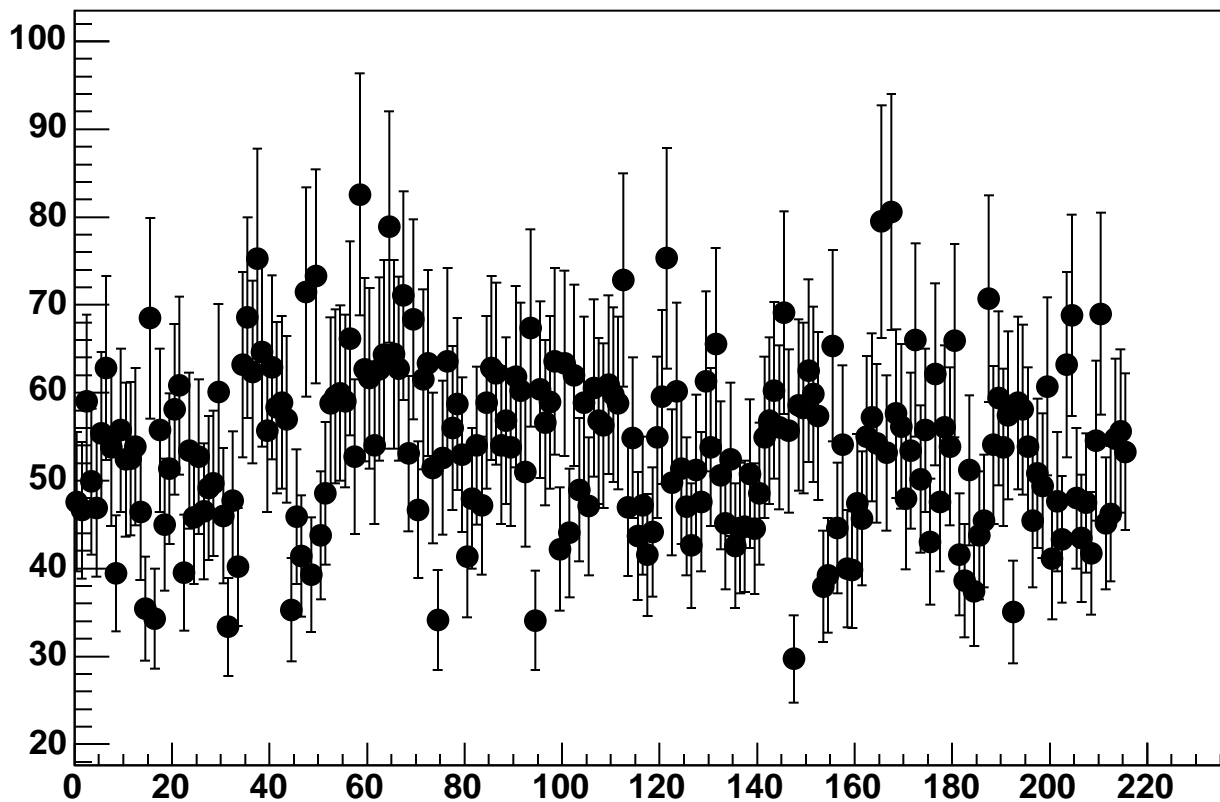
Enable 4, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



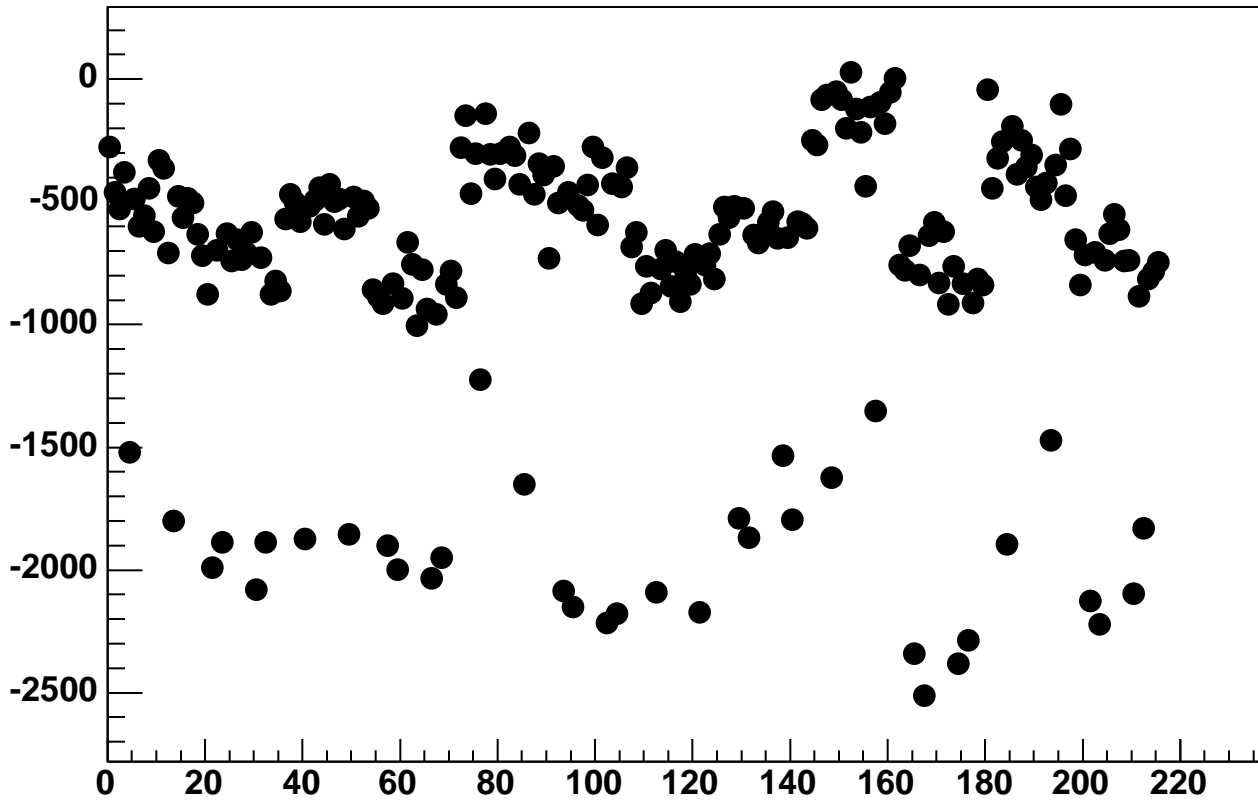
Enable 4, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan



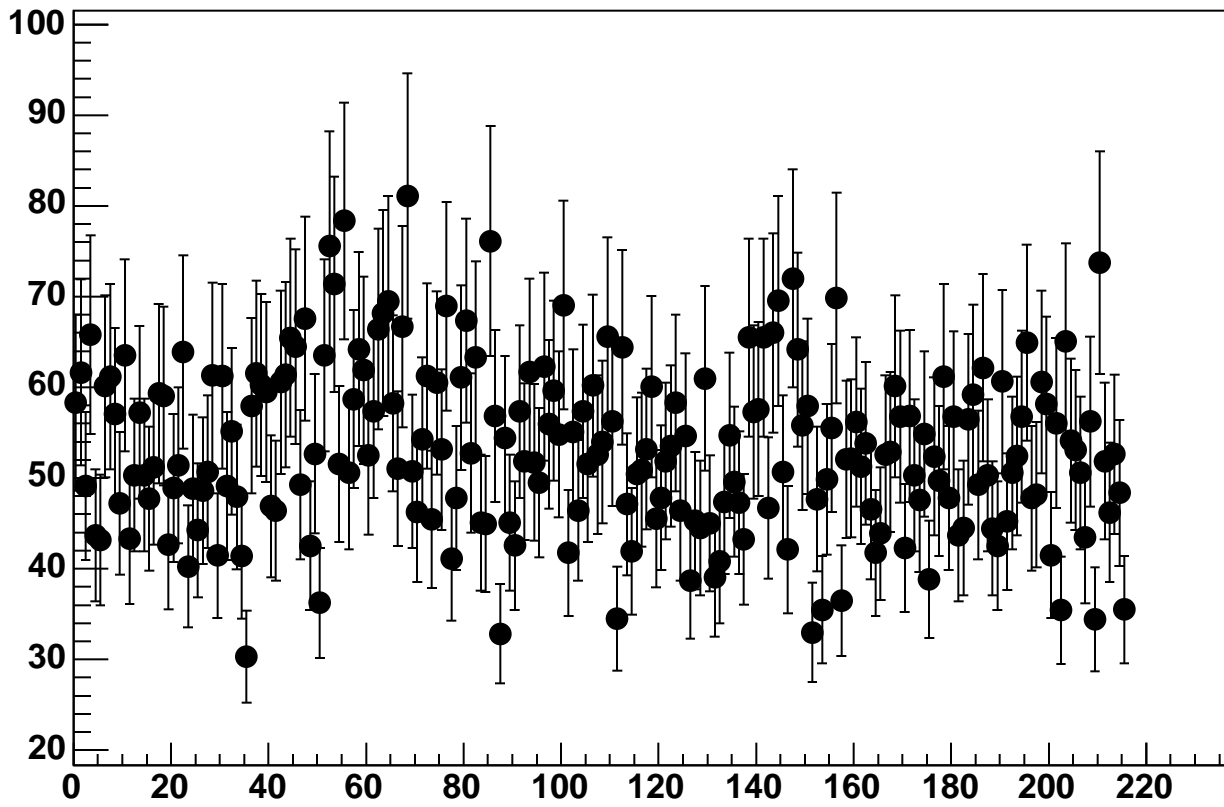
Enable 4, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan



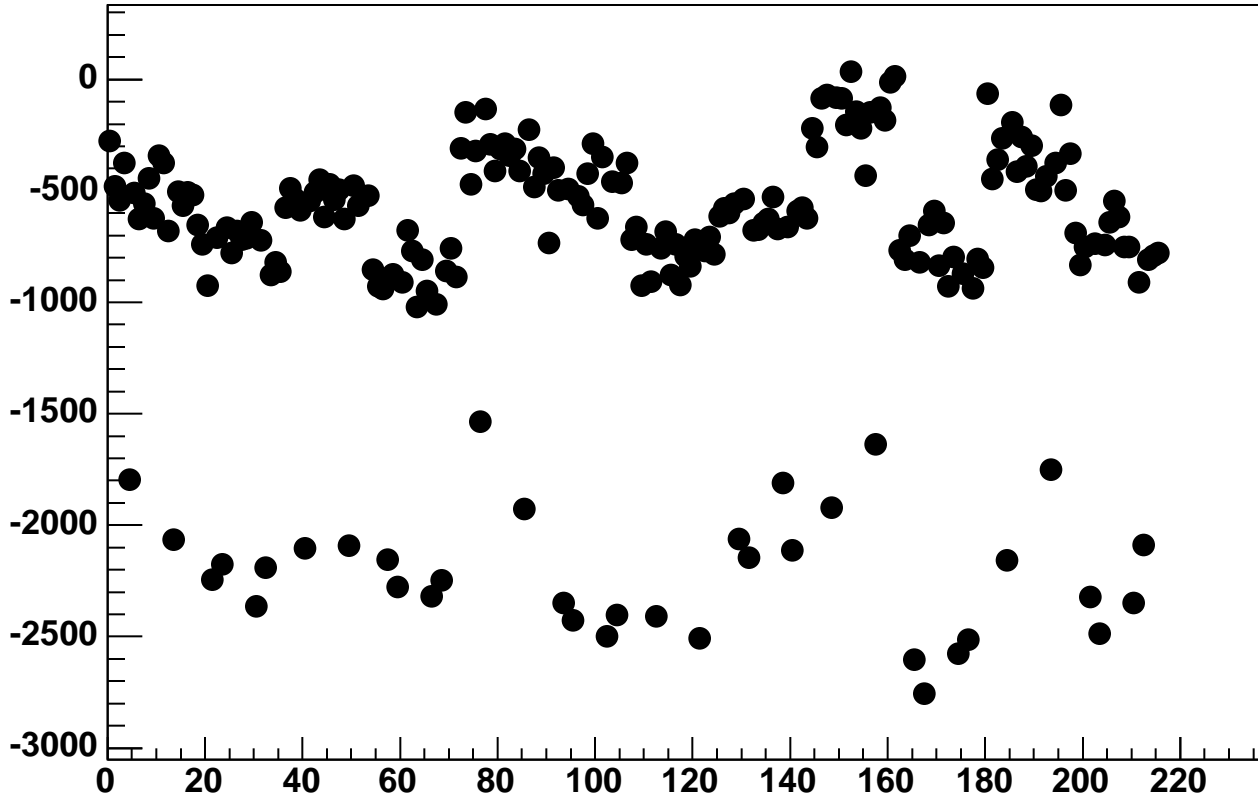
Enable 4, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



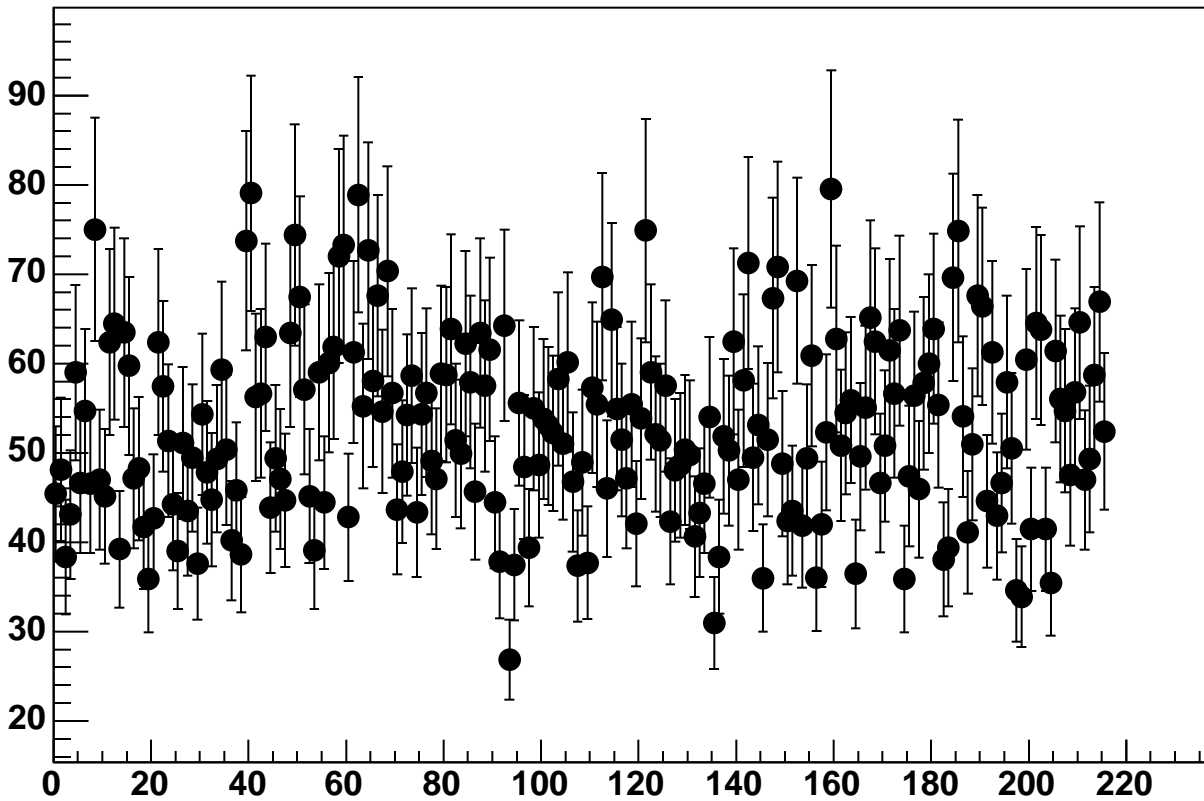
Enable 4, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



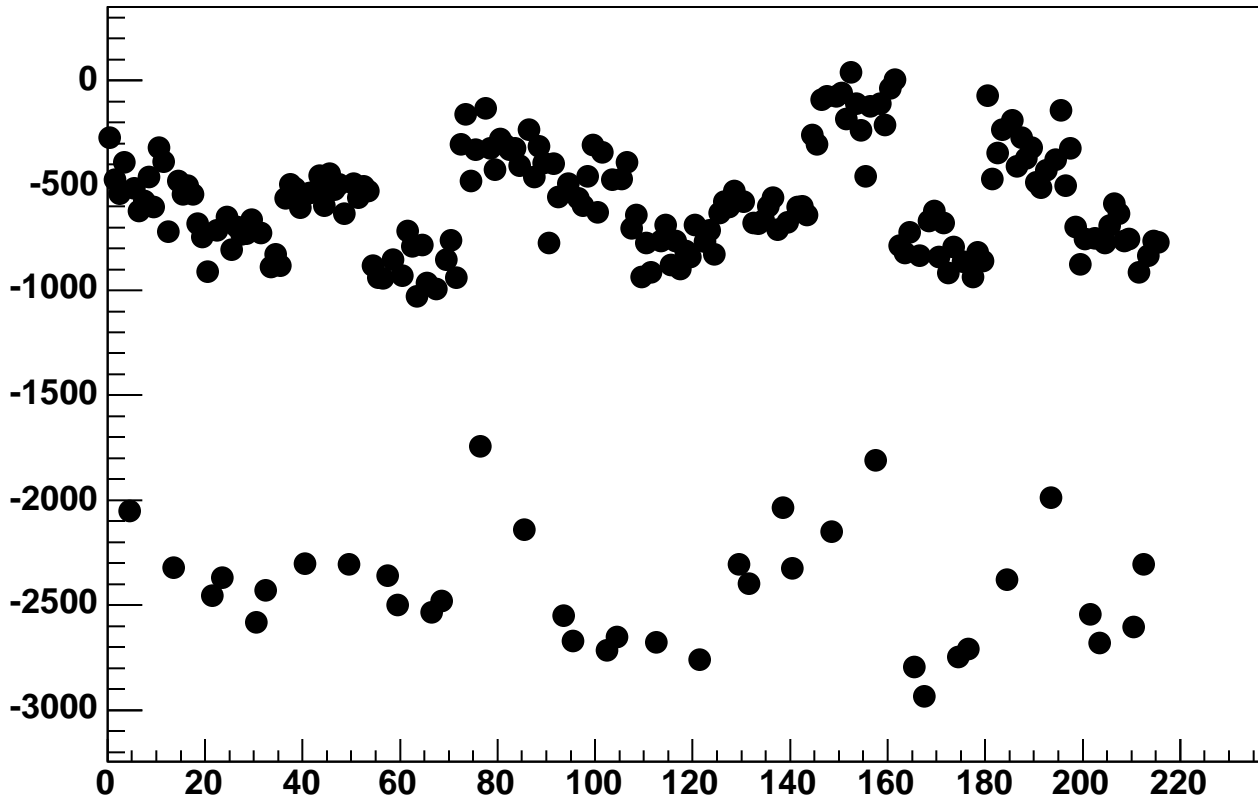
Enable 4, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan



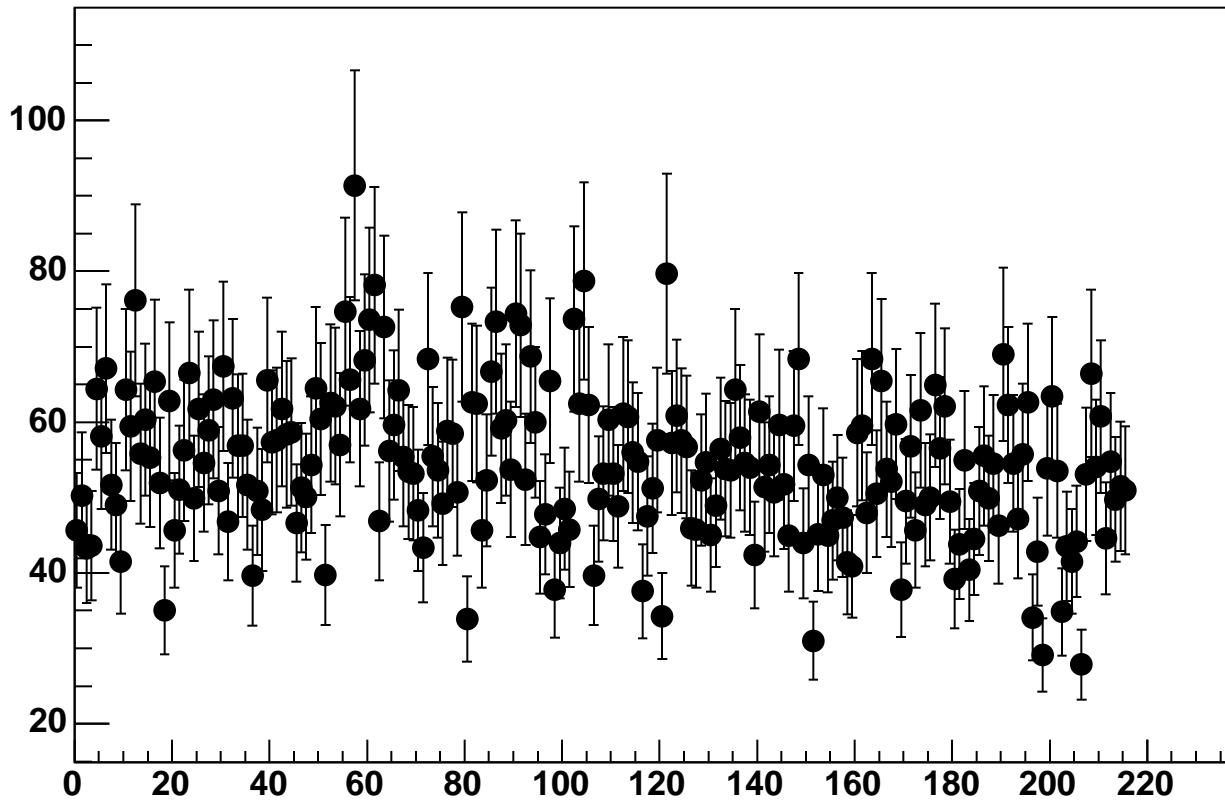
Enable 4, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan



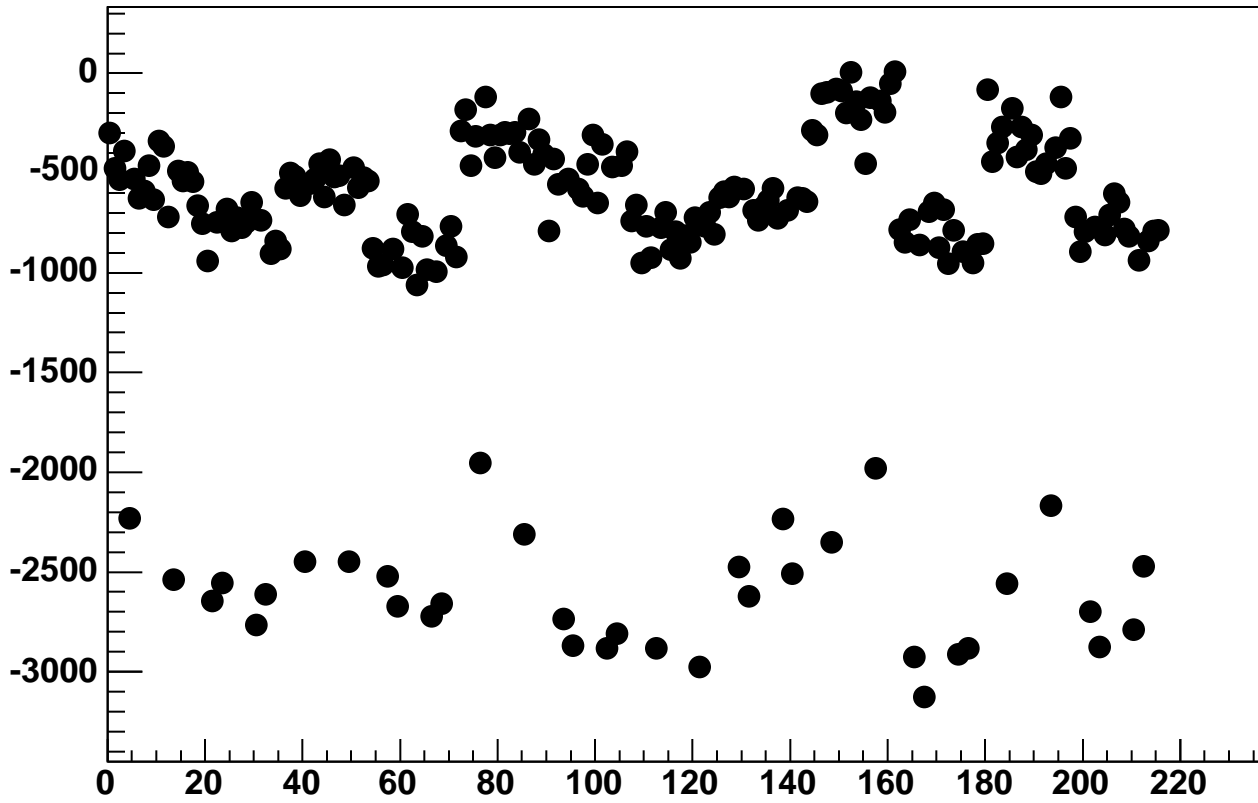
Enable 4, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



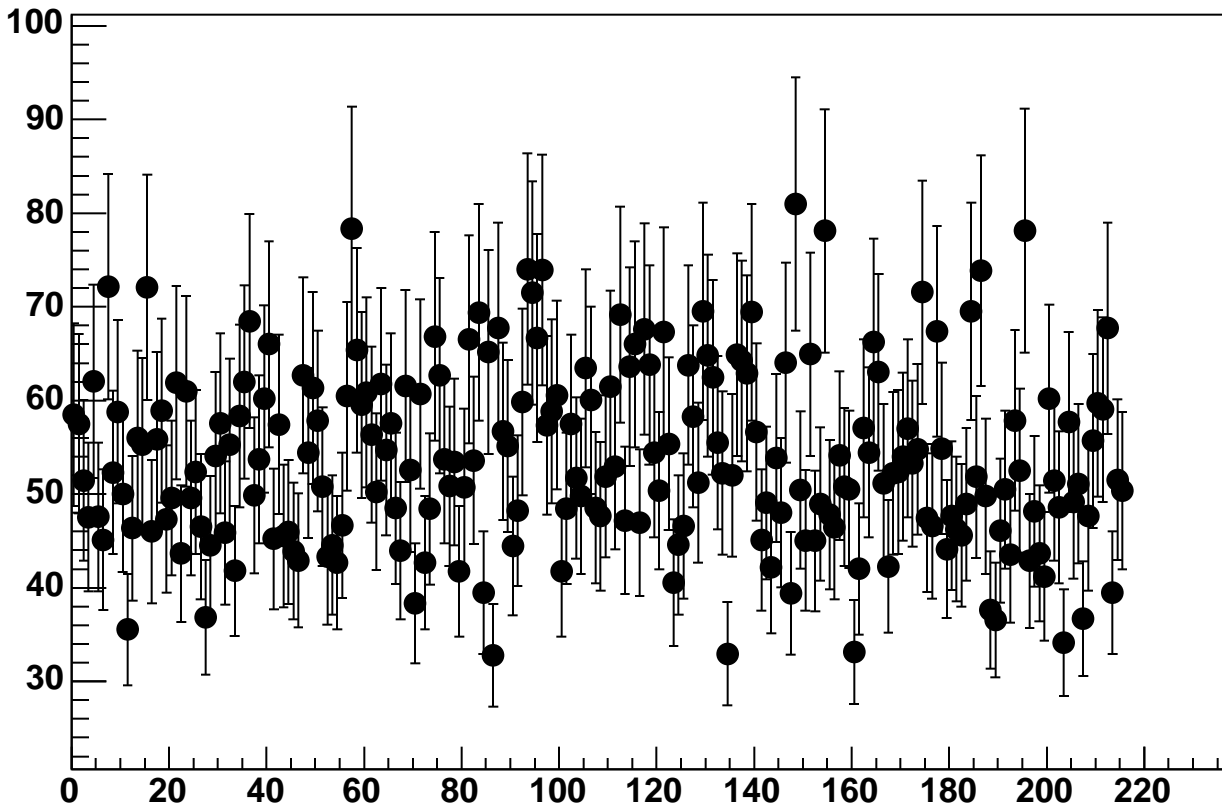
Enable 4, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



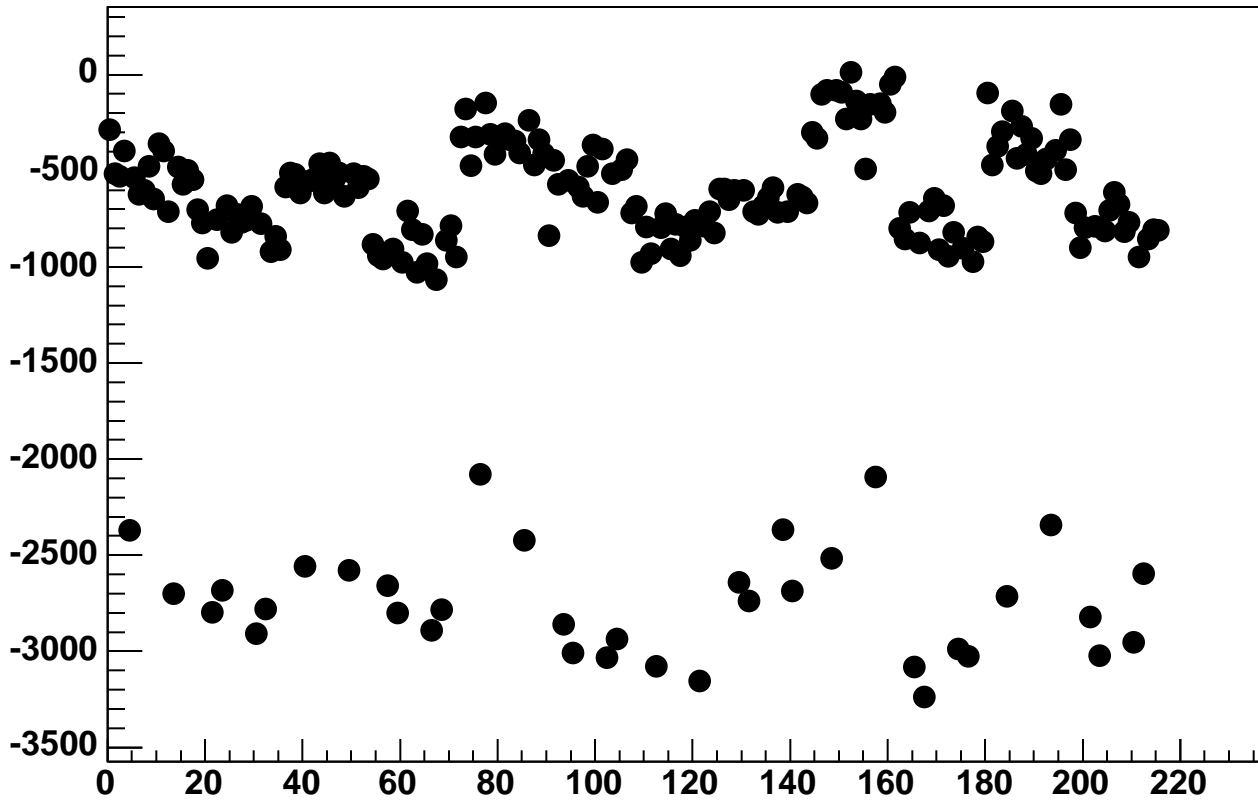
Enable 4, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan



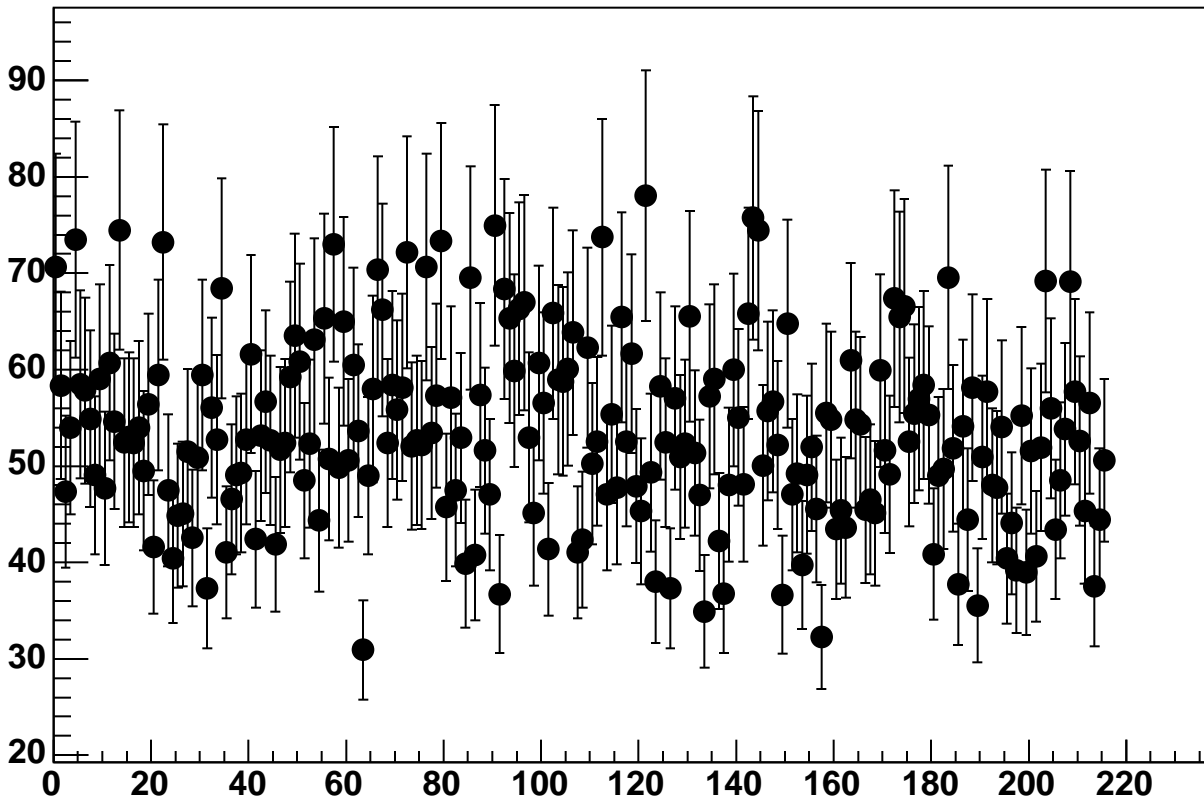
Enable 4, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan



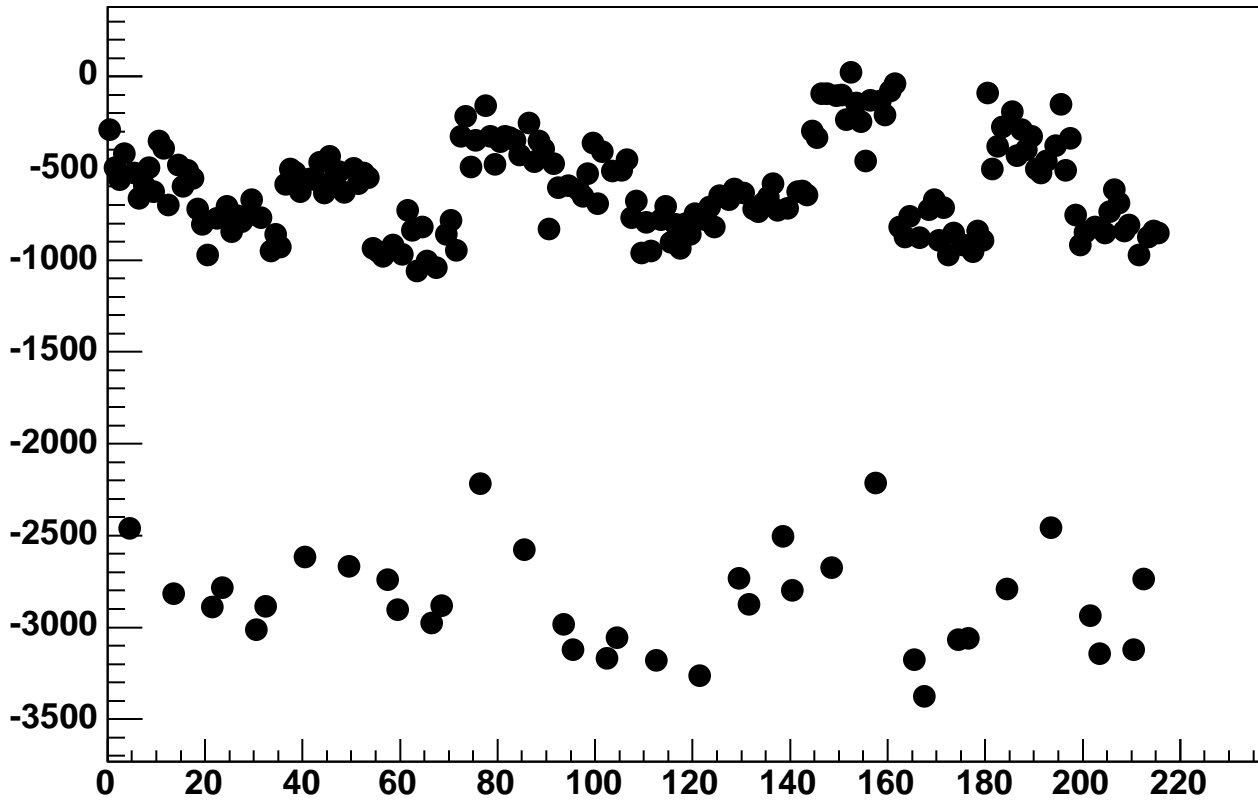
Enable 4, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



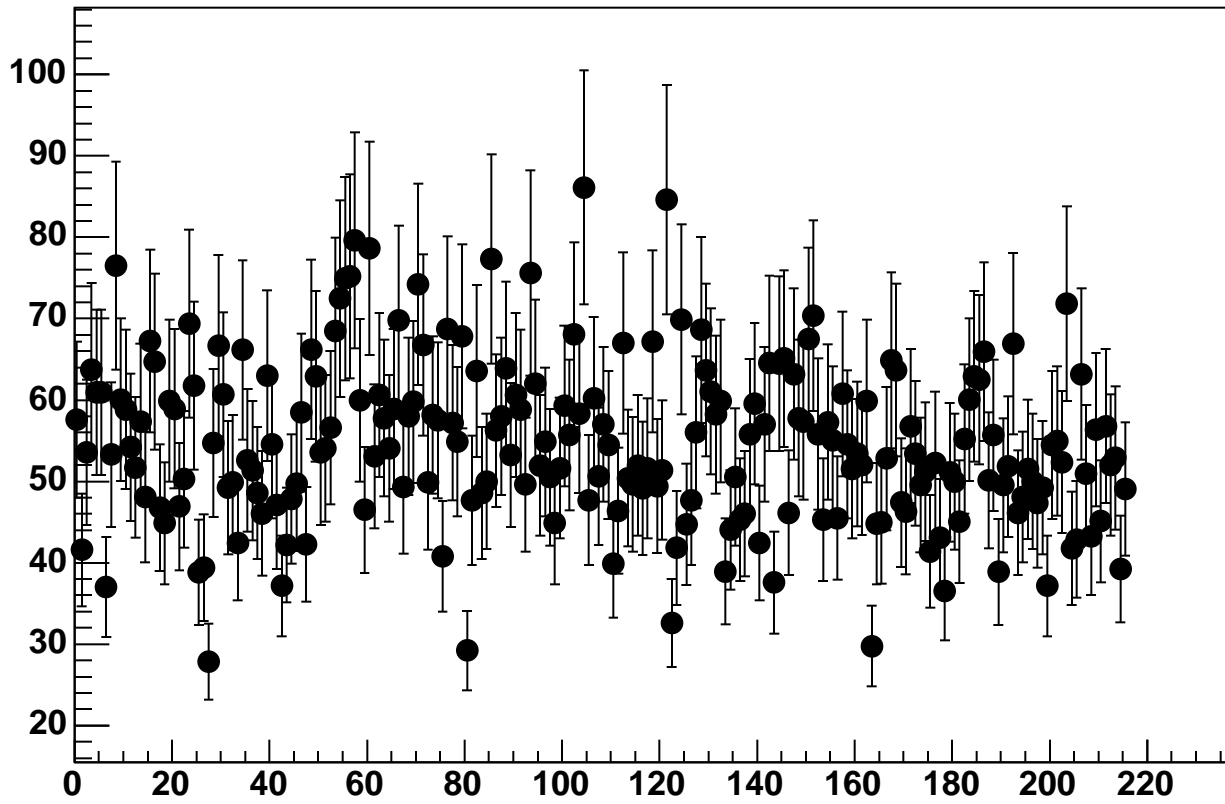
Enable 4, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan

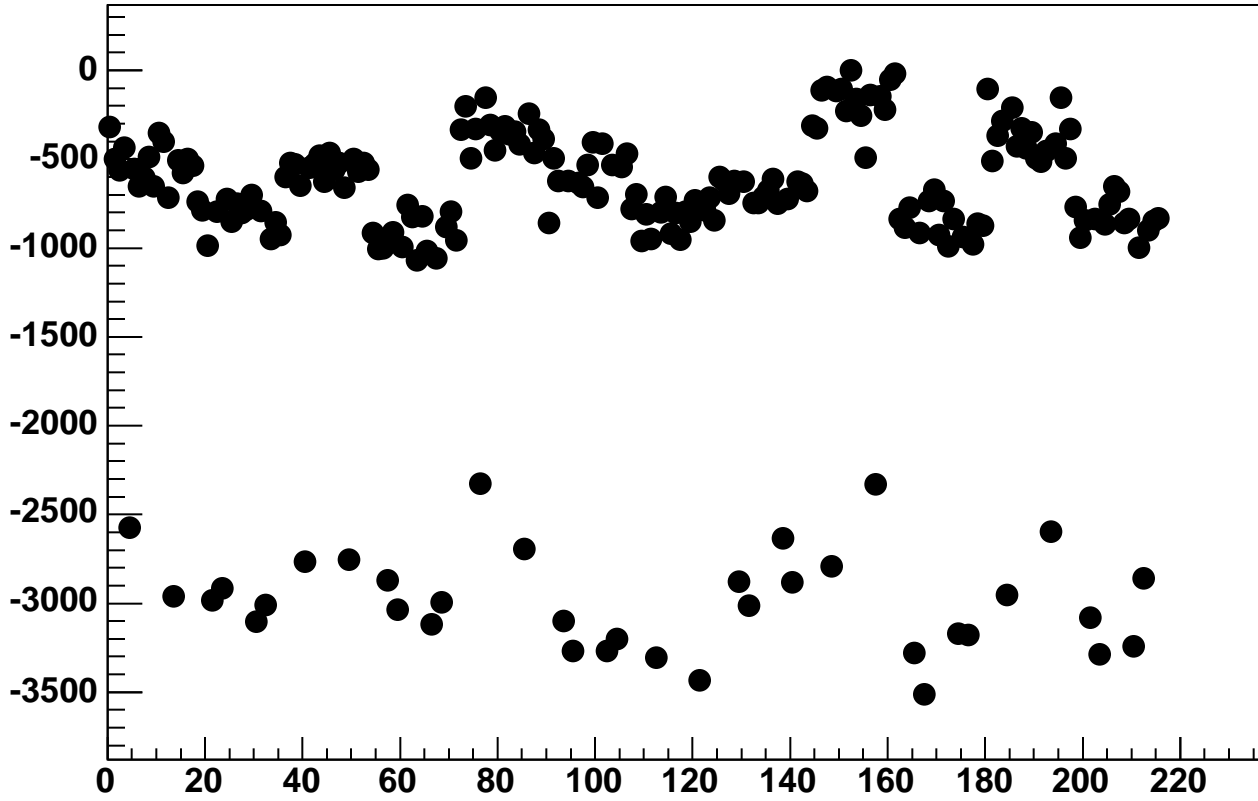


Enable 4, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan

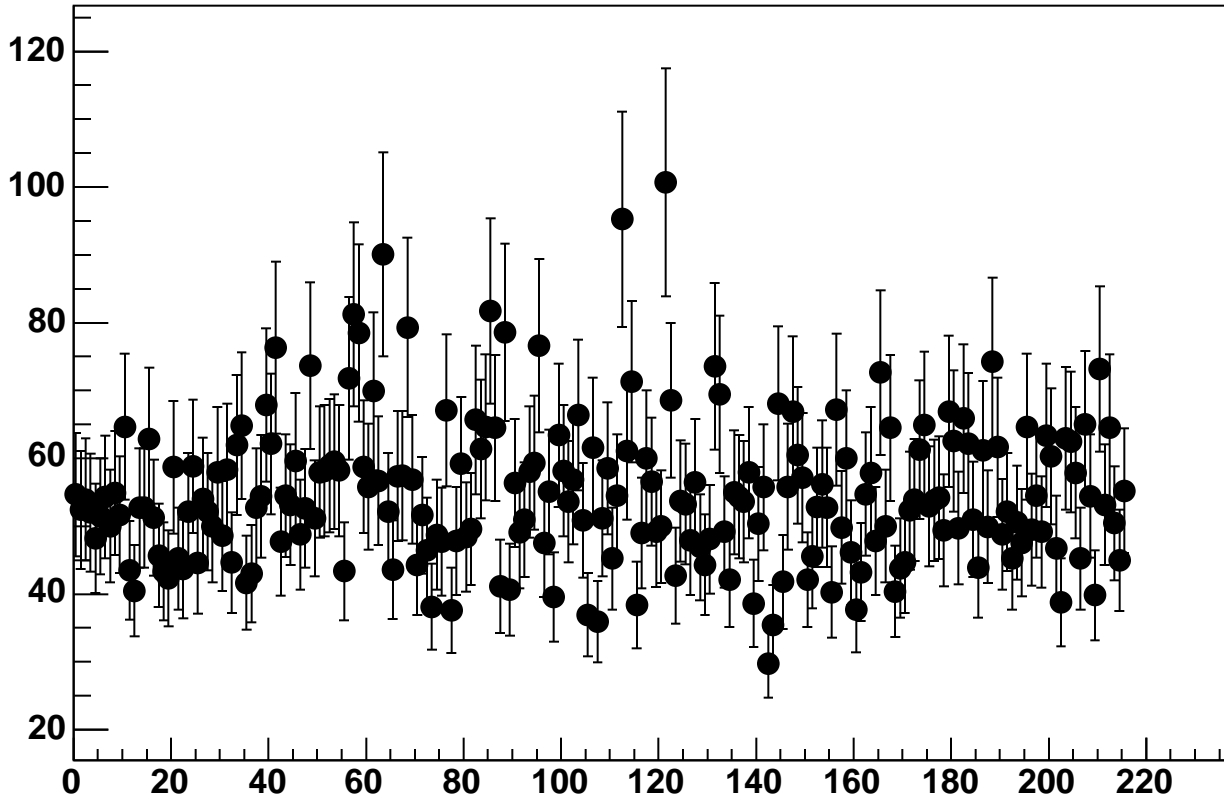




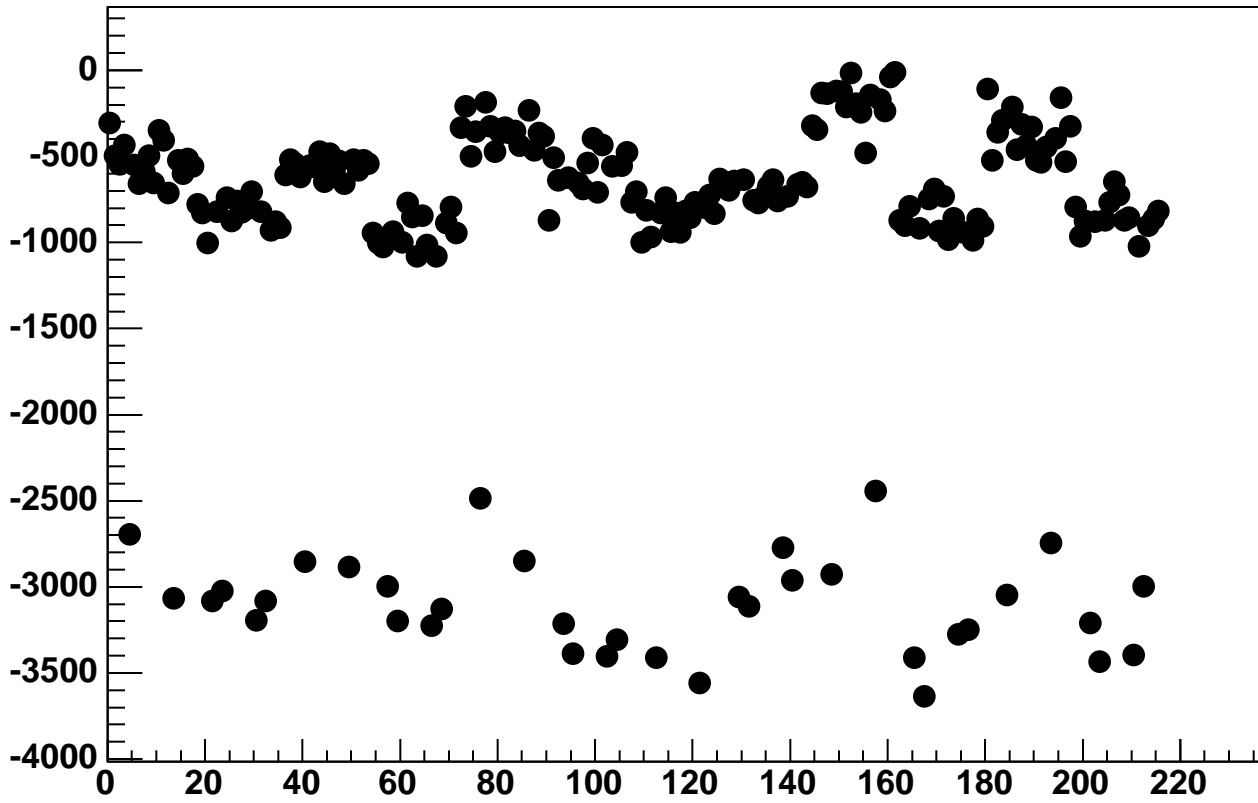
Enable 4, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



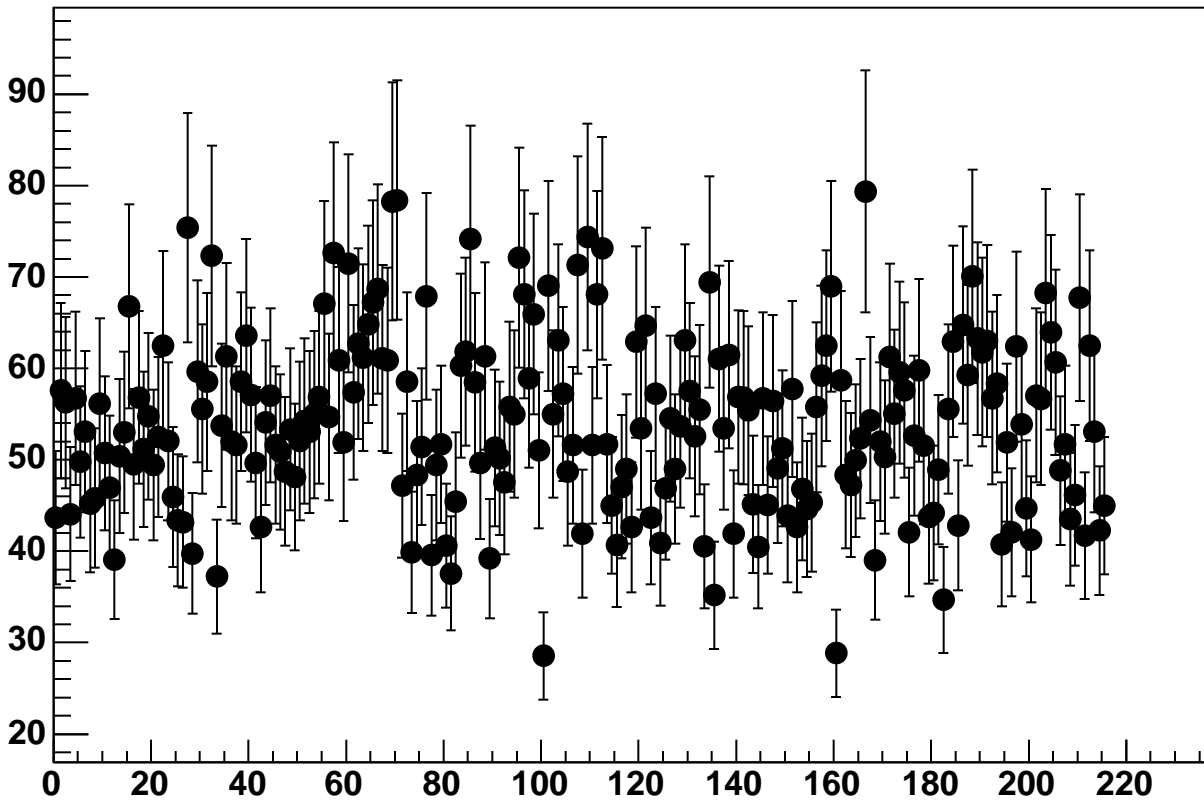
Enable 4, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



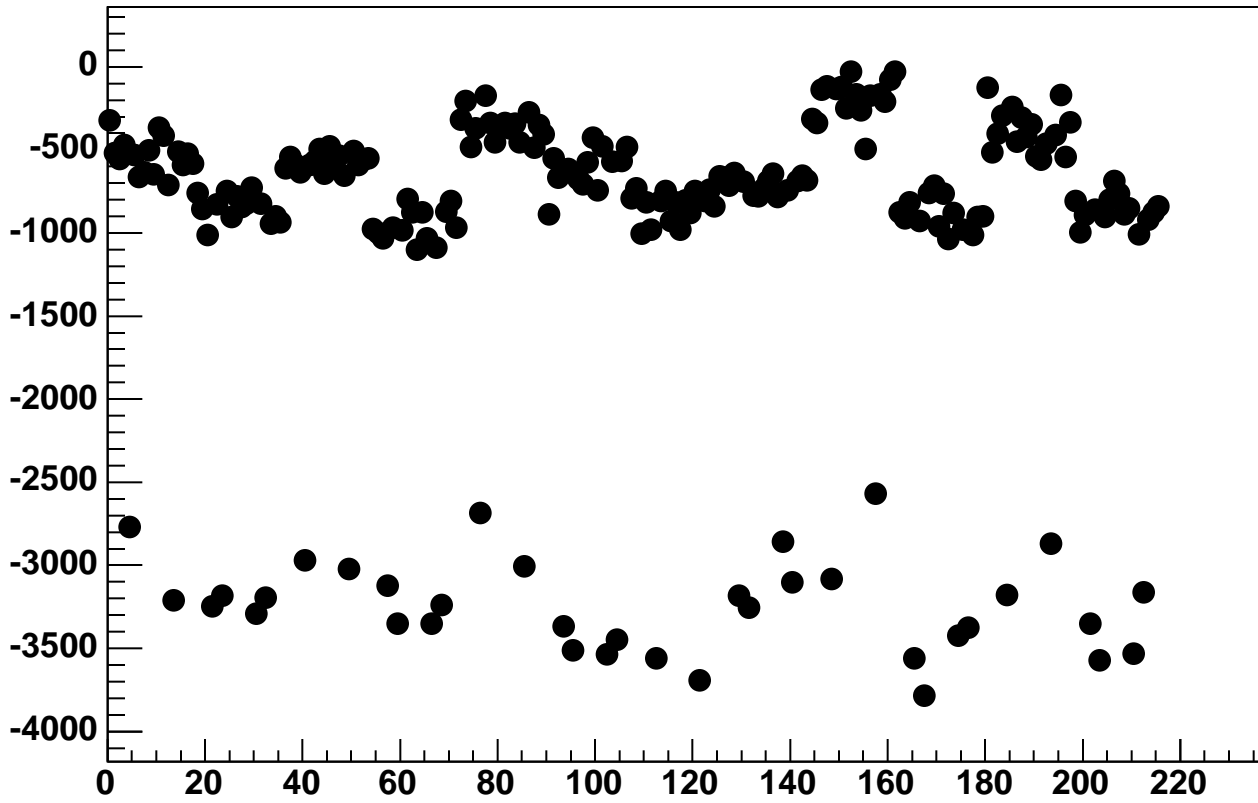
Enable 4, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan



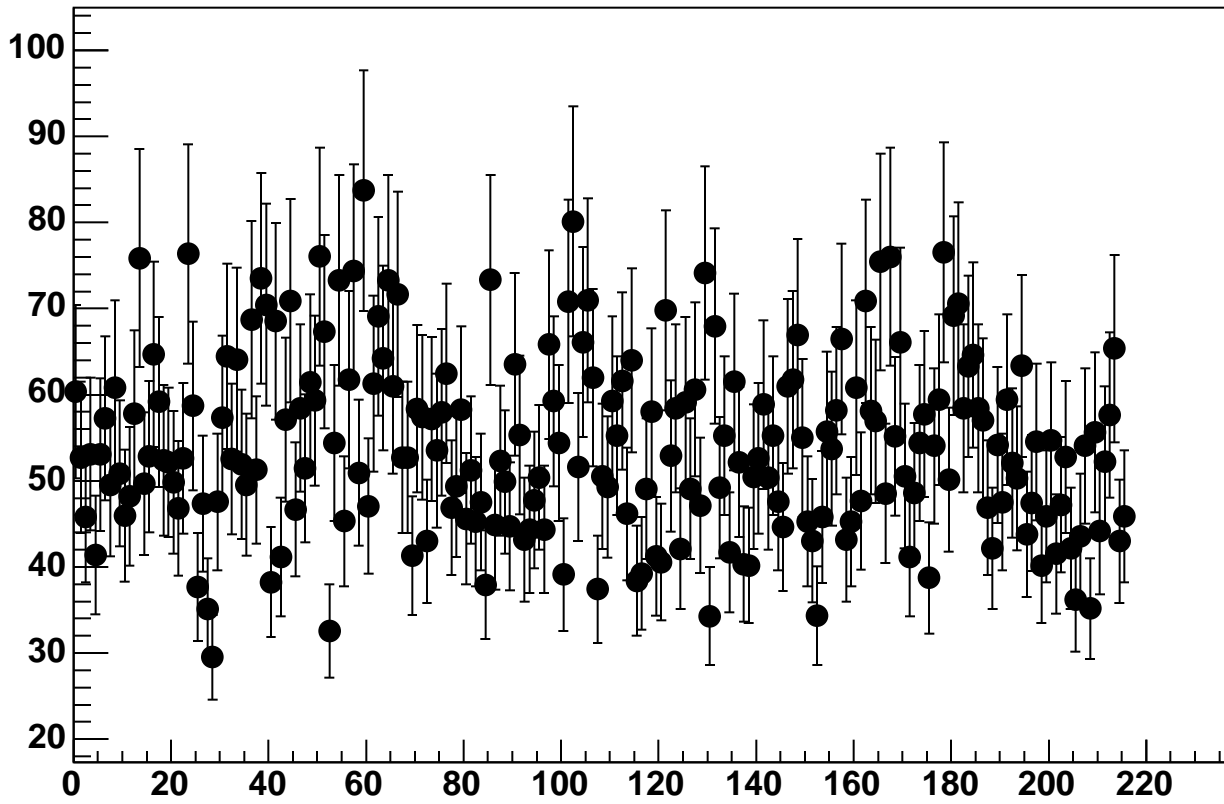
Enable 4, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan



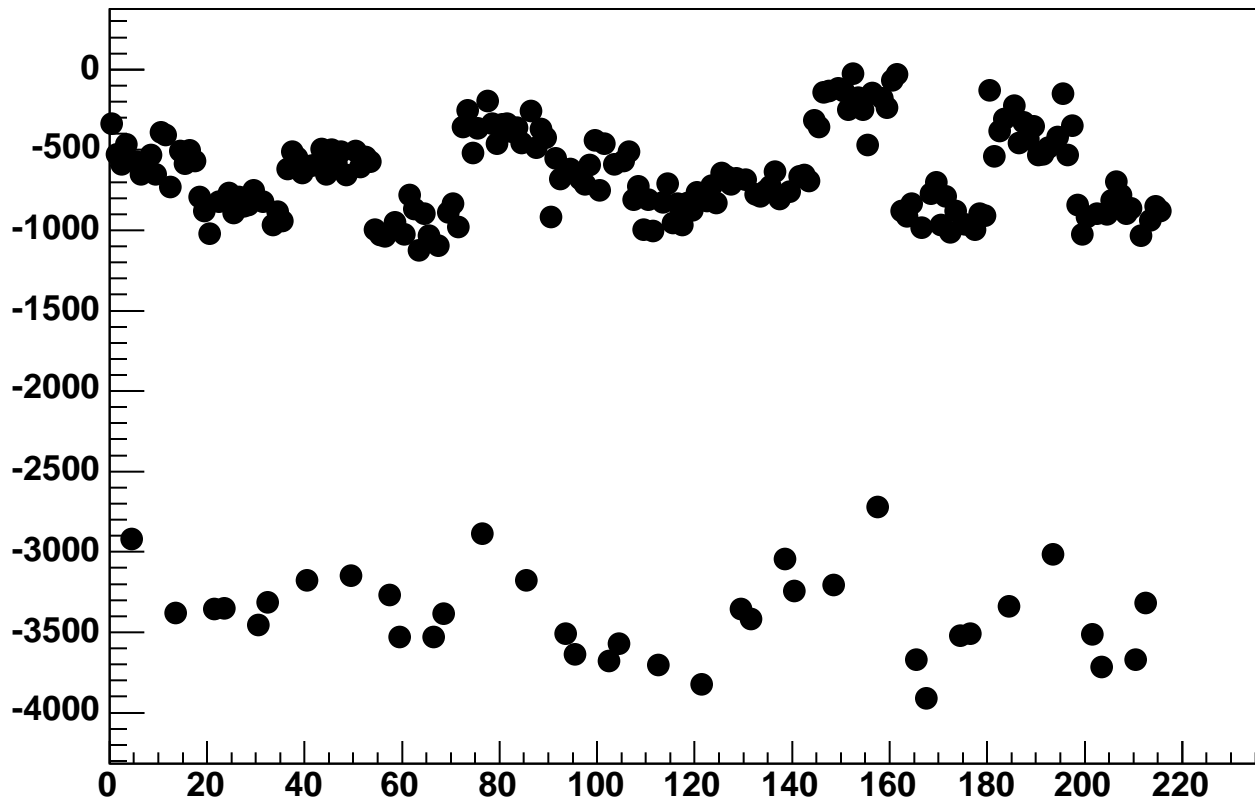
Enable 4, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



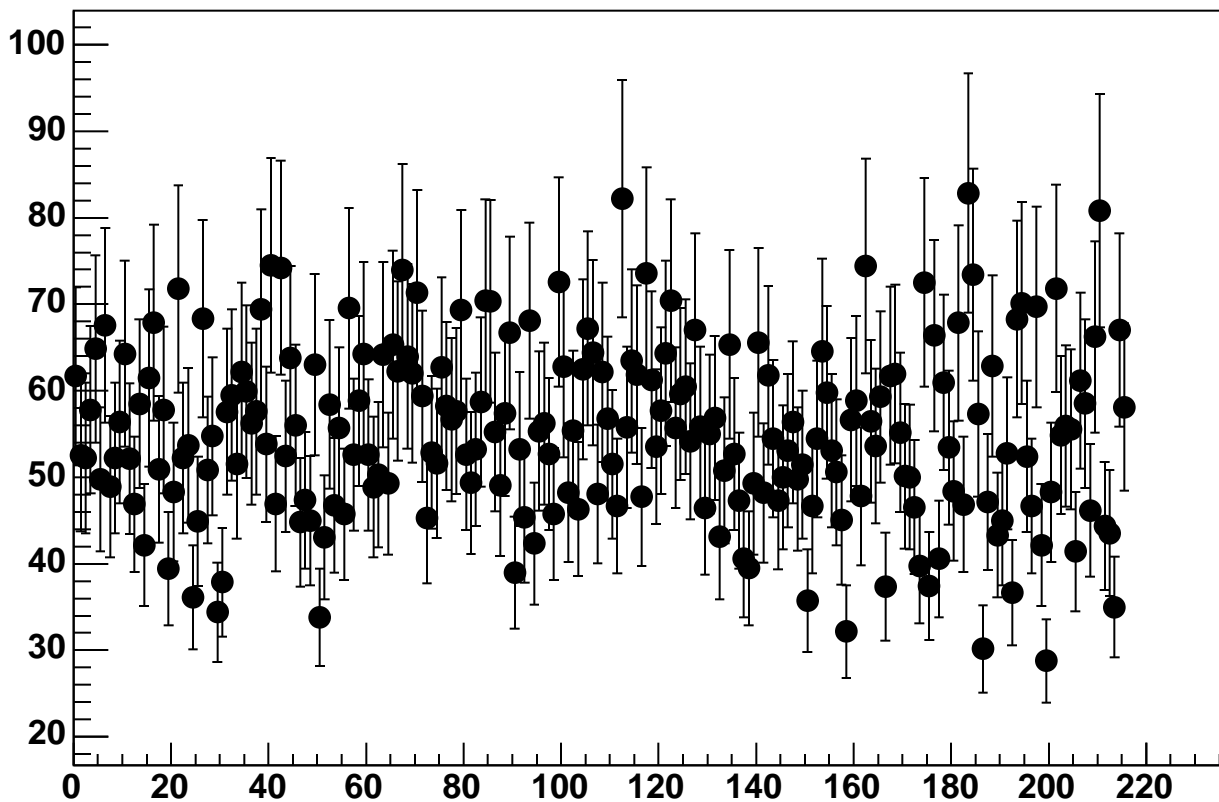
Enable 4, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



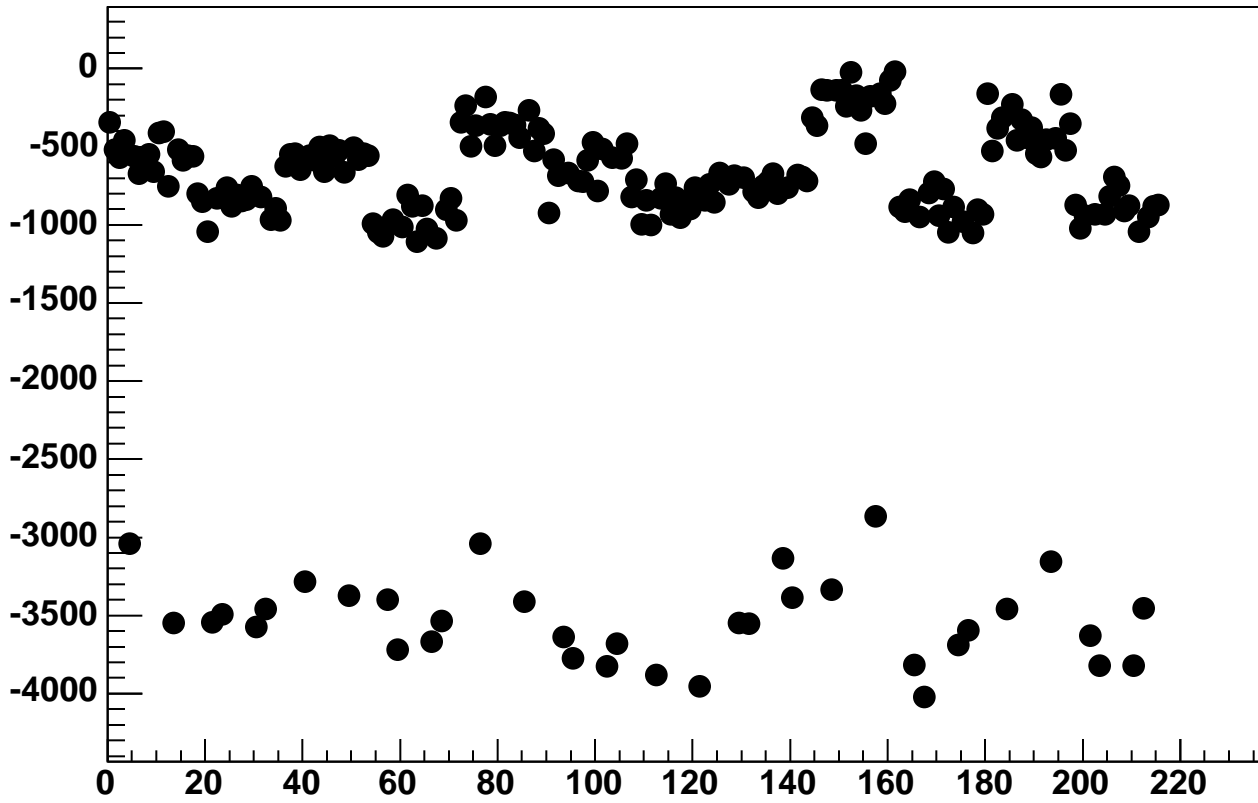
Enable 4, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan



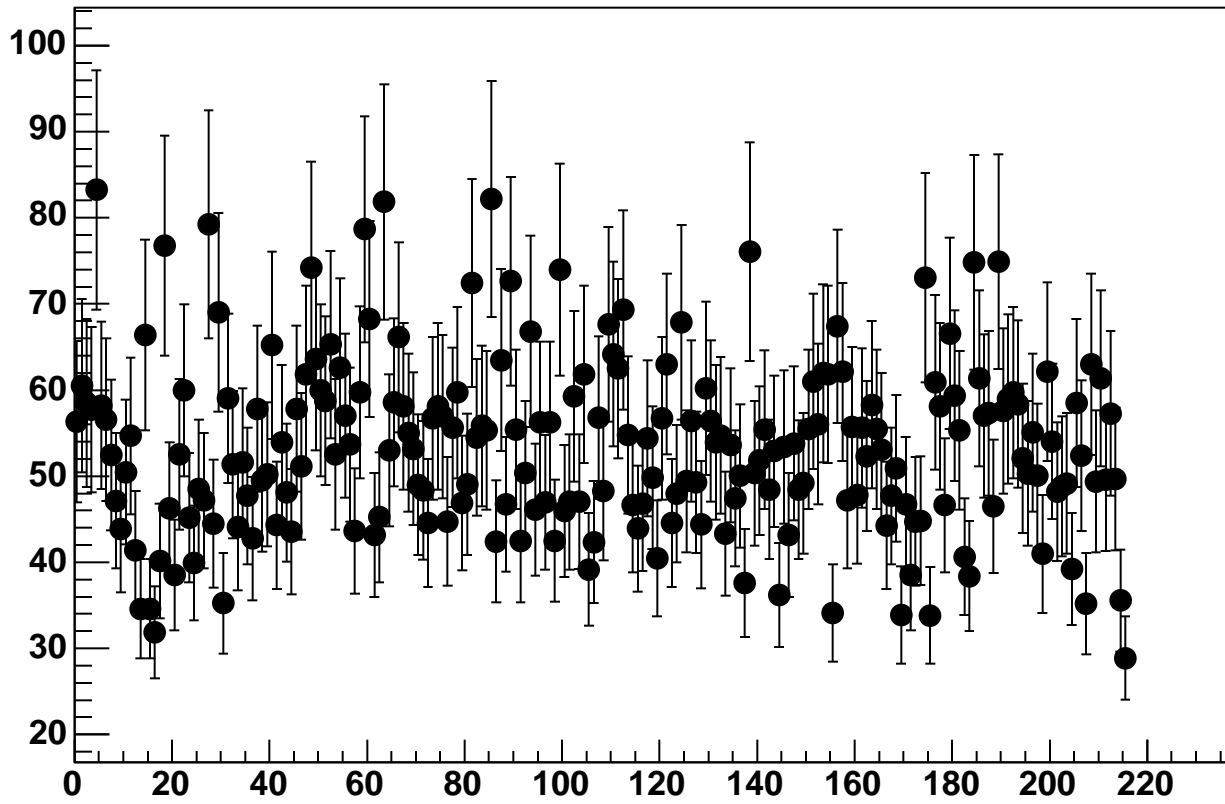
Enable 4, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan



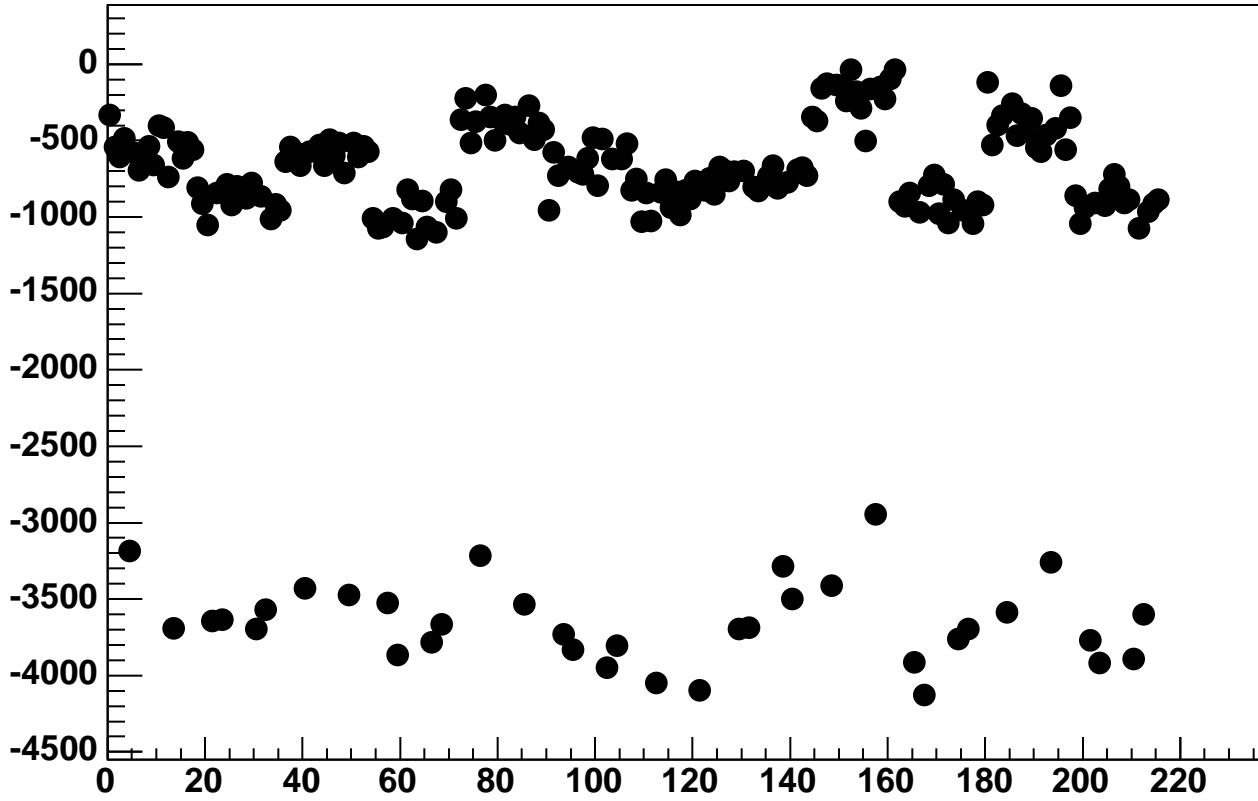
Enable 4, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



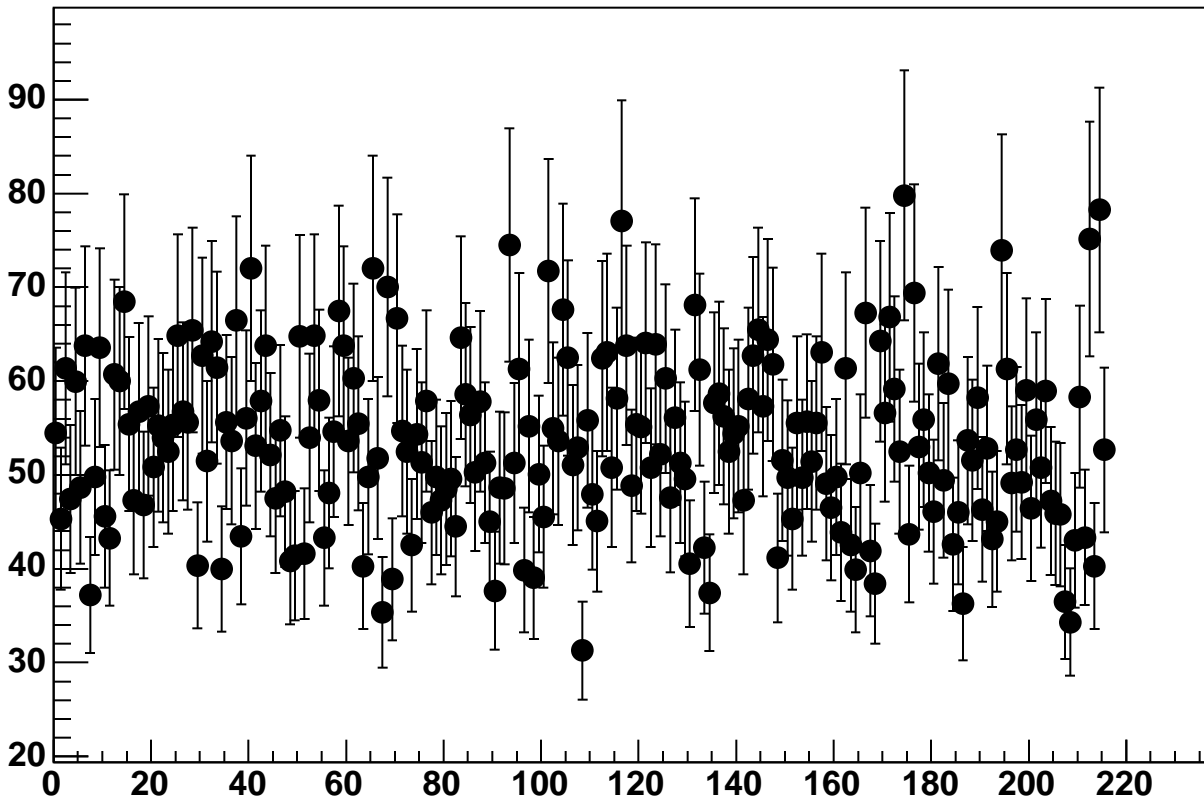
Enable 4, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



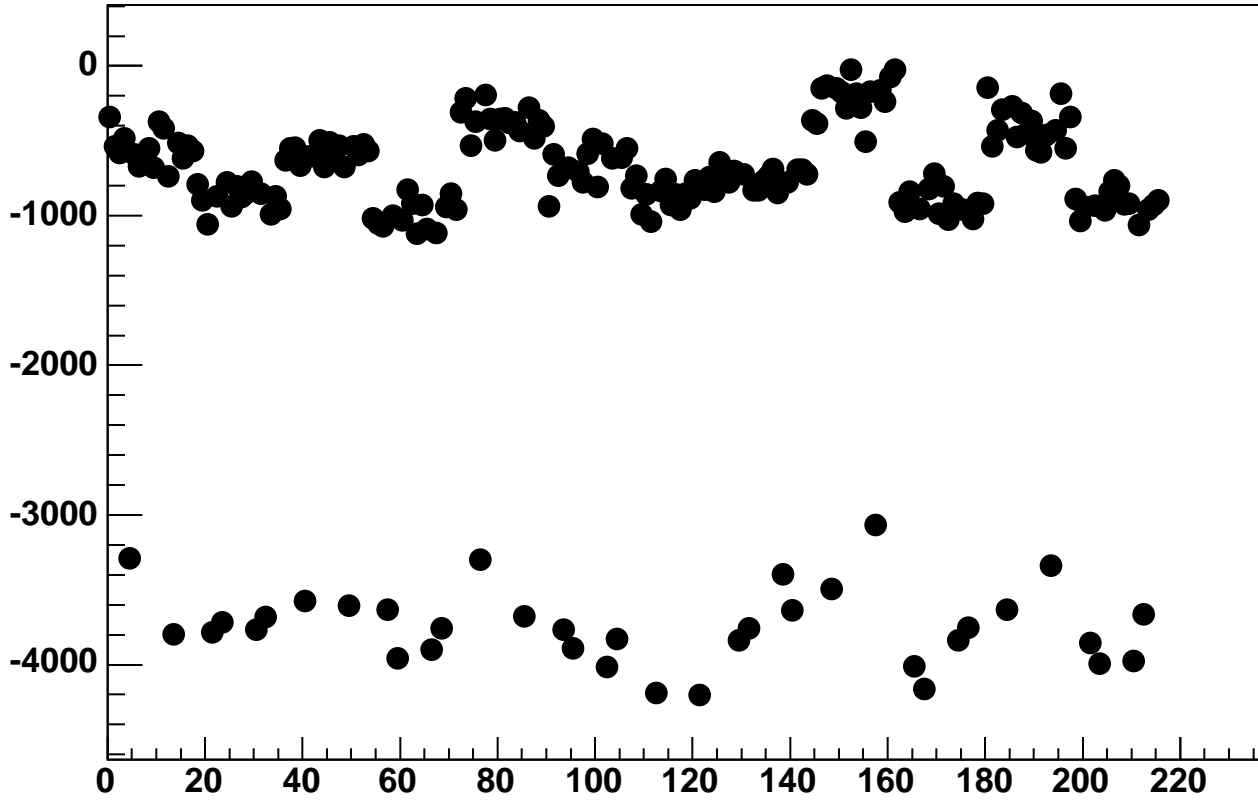
Enable 4, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan



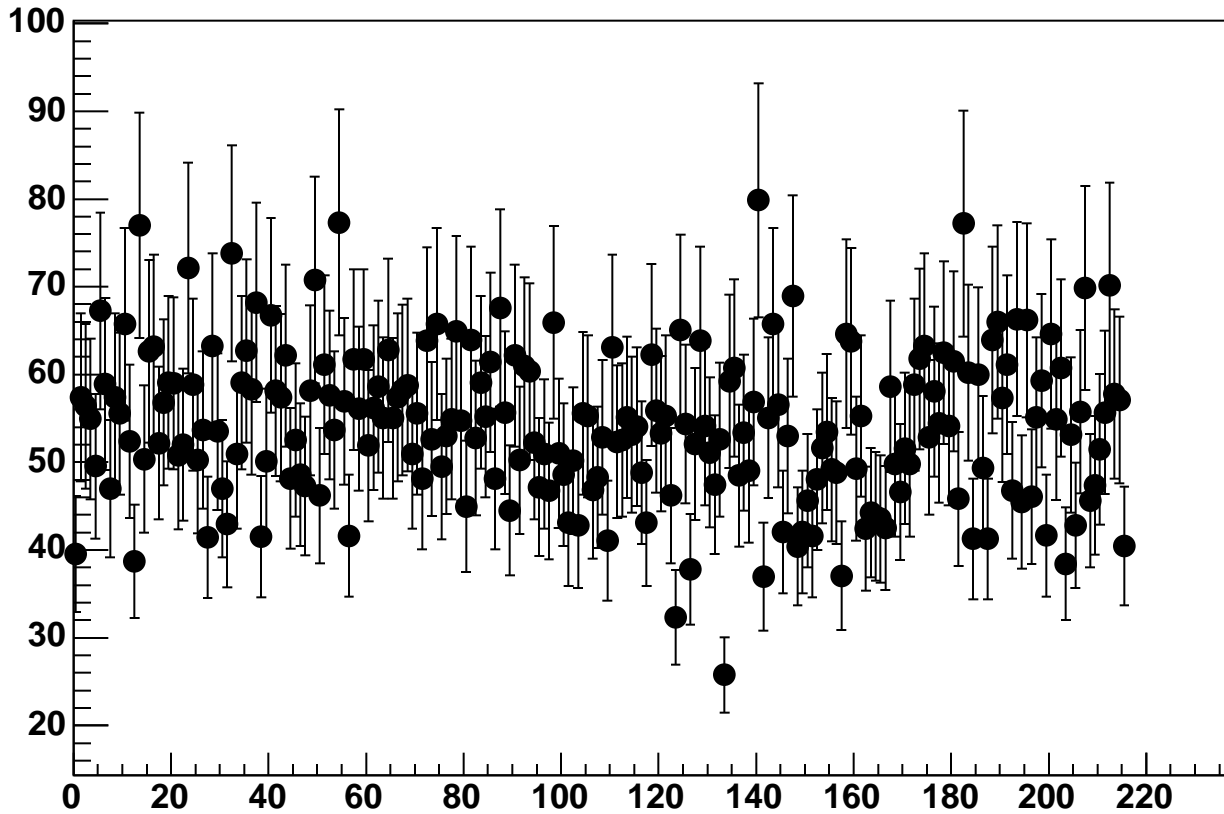
Enable 4, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan



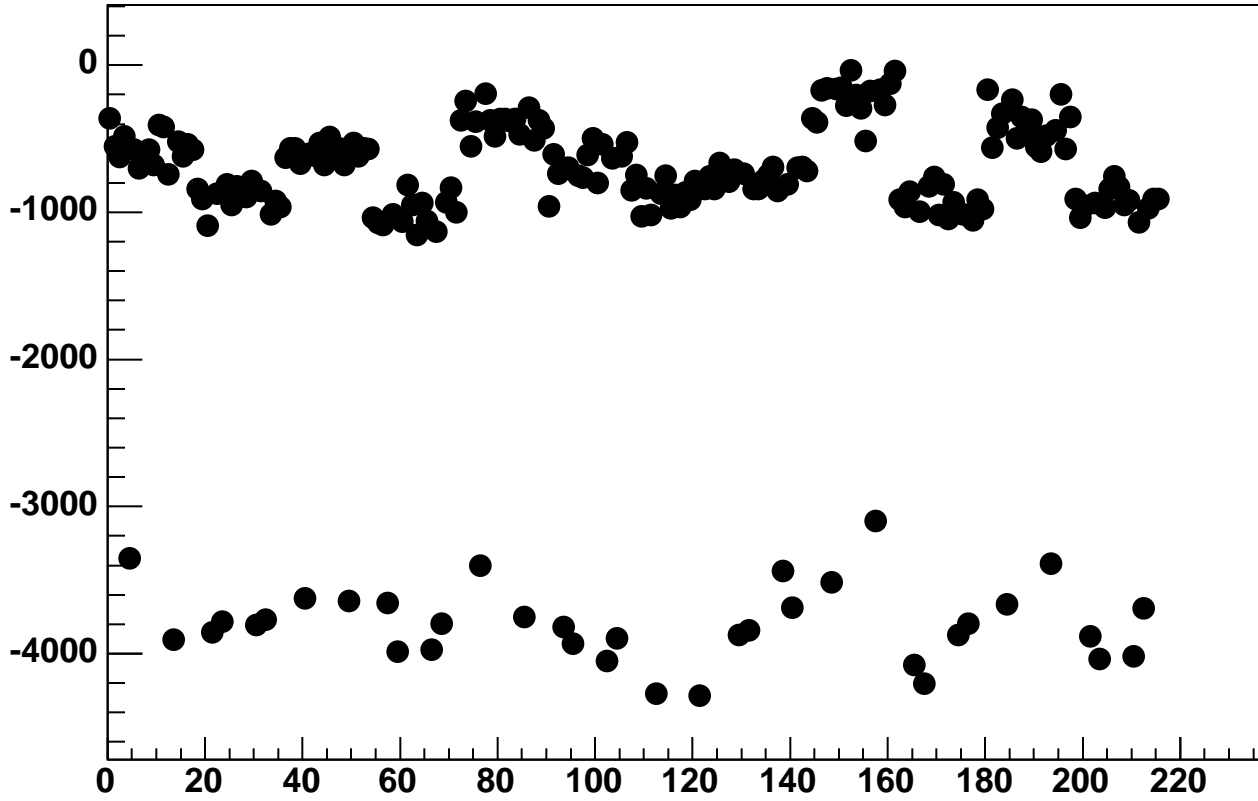
Enable 4, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



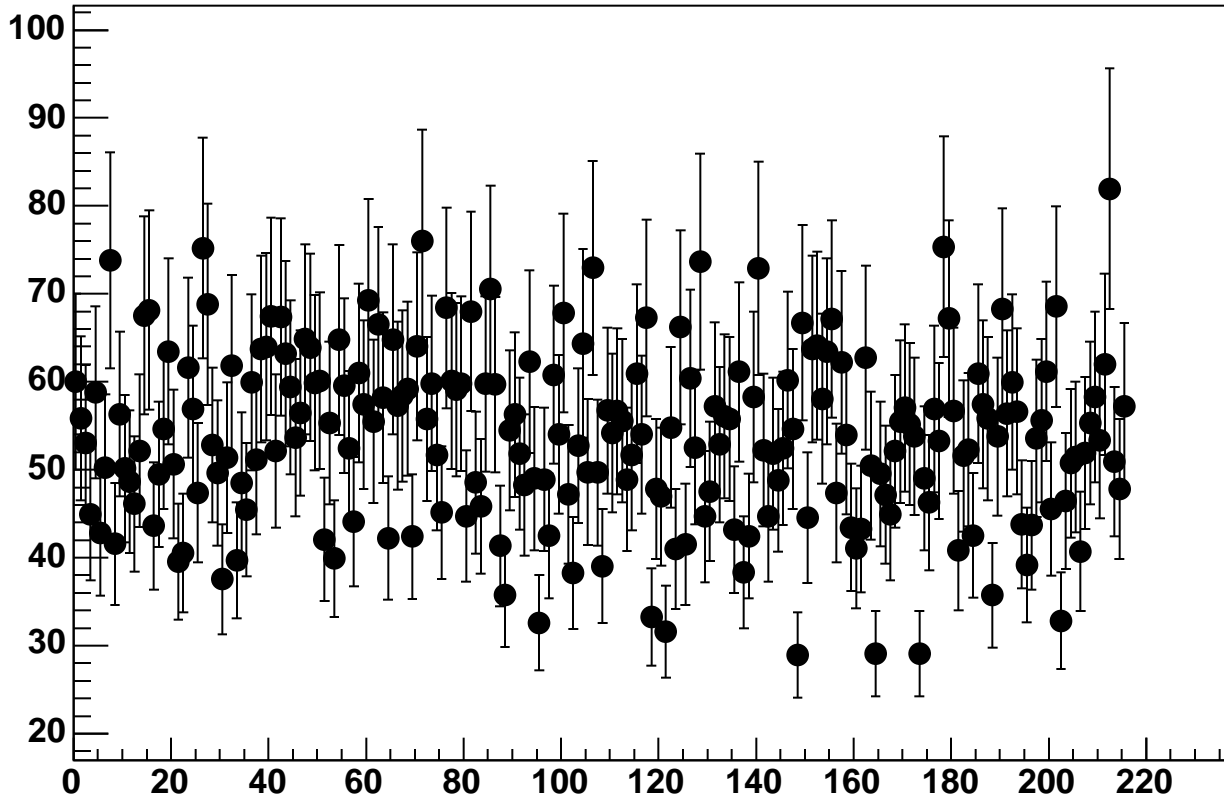
Enable 4, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



Enable 4, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan

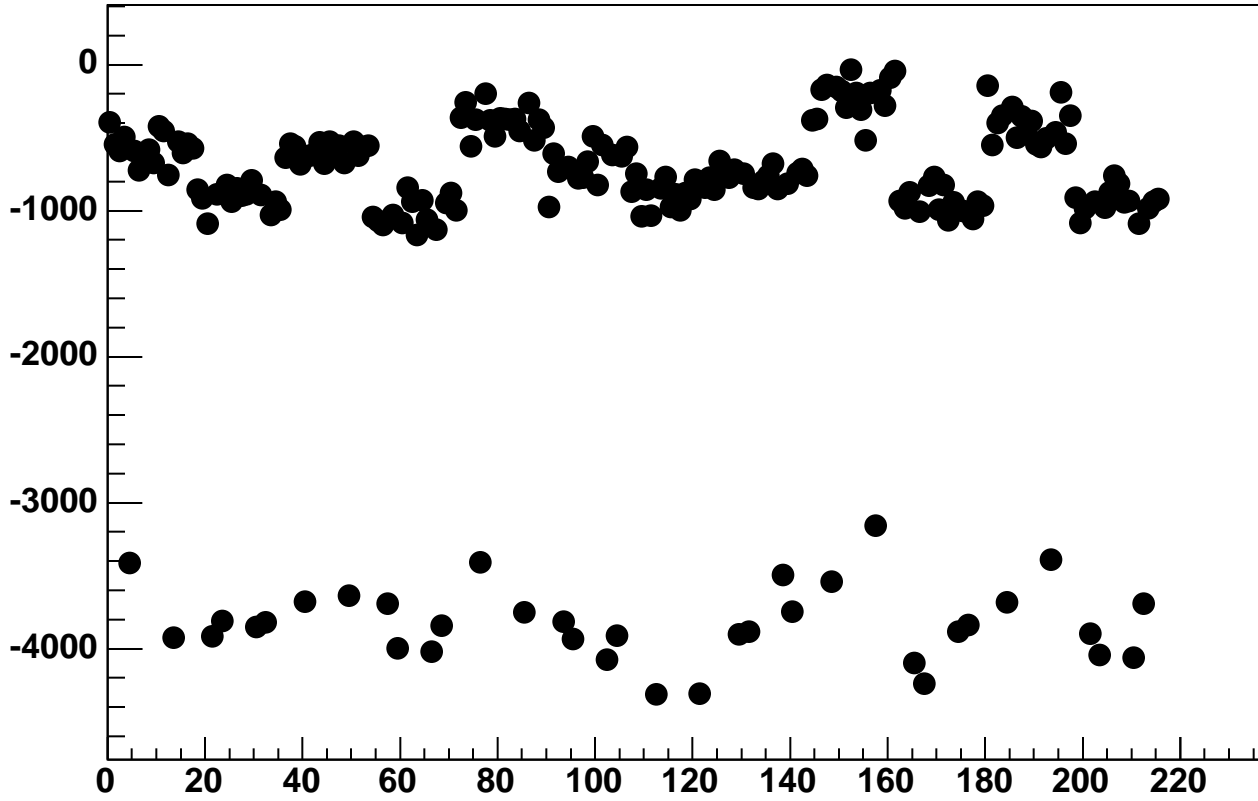


Enable 4, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan

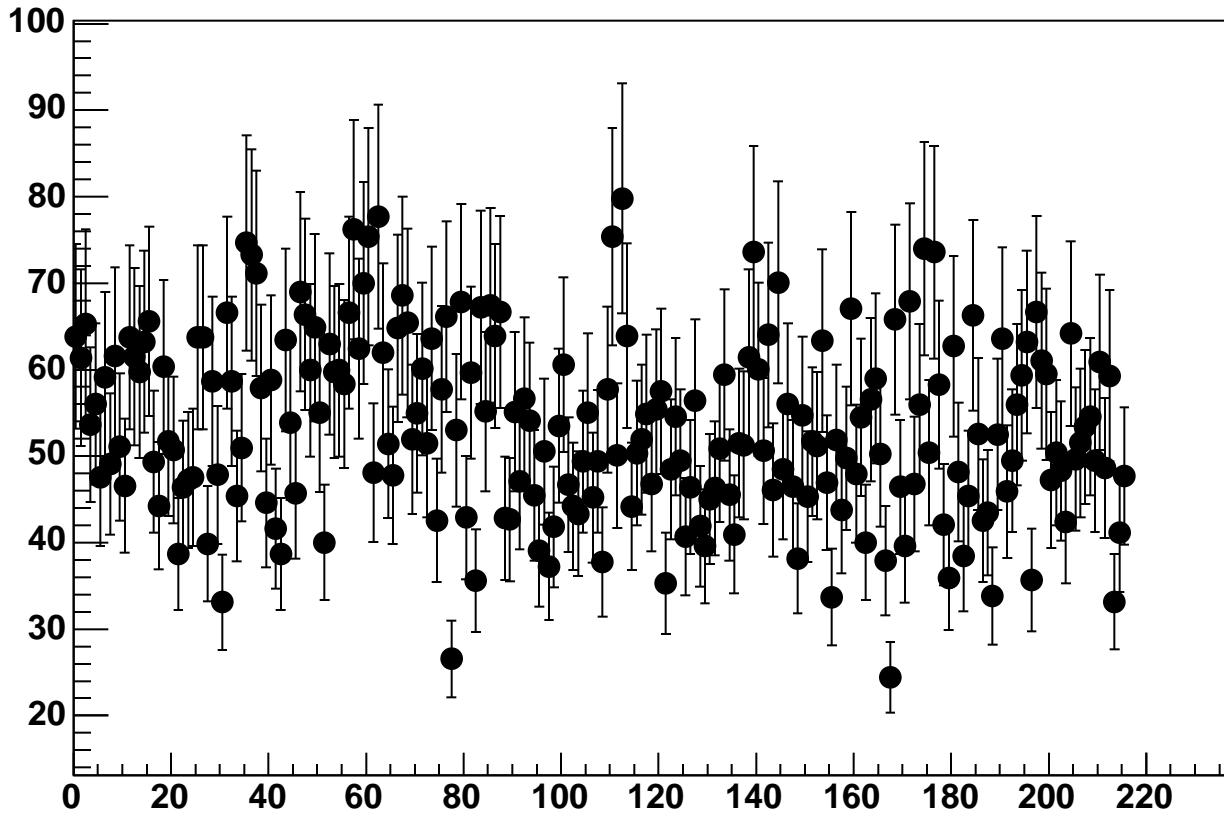




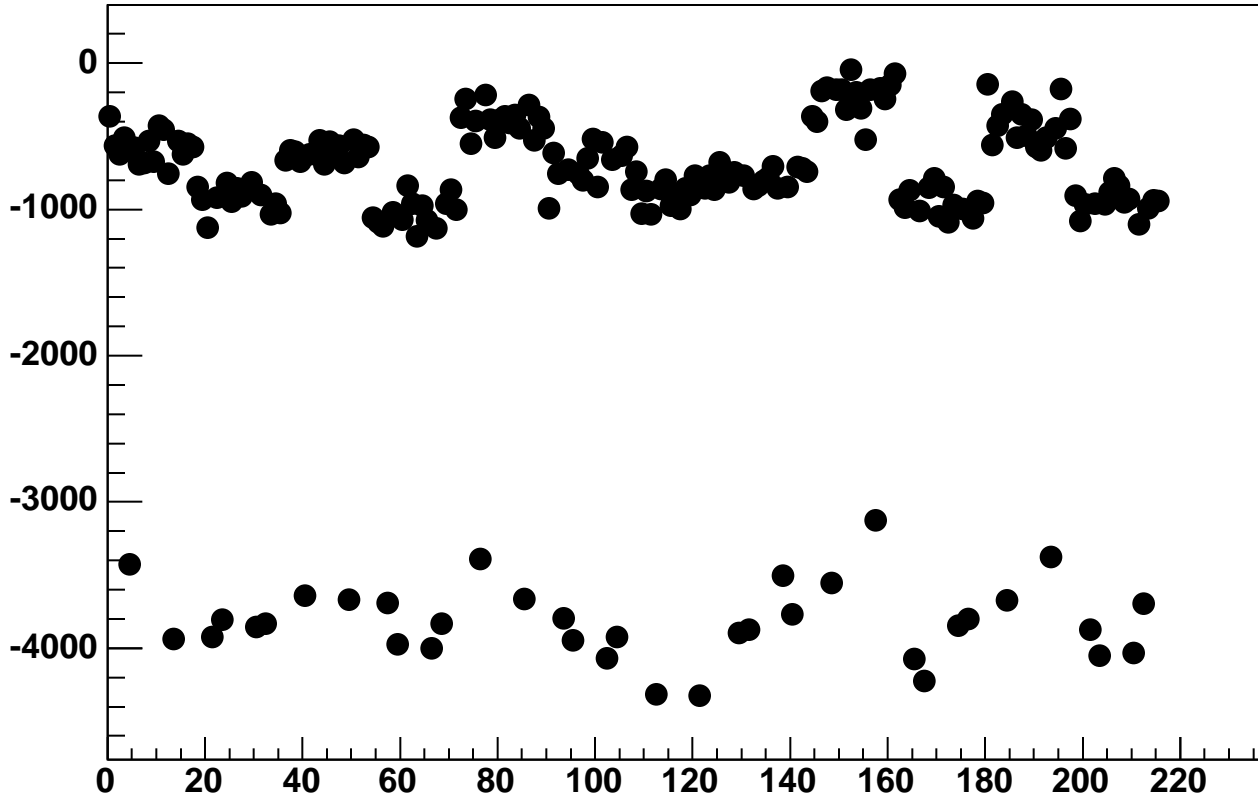
Enable 4, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



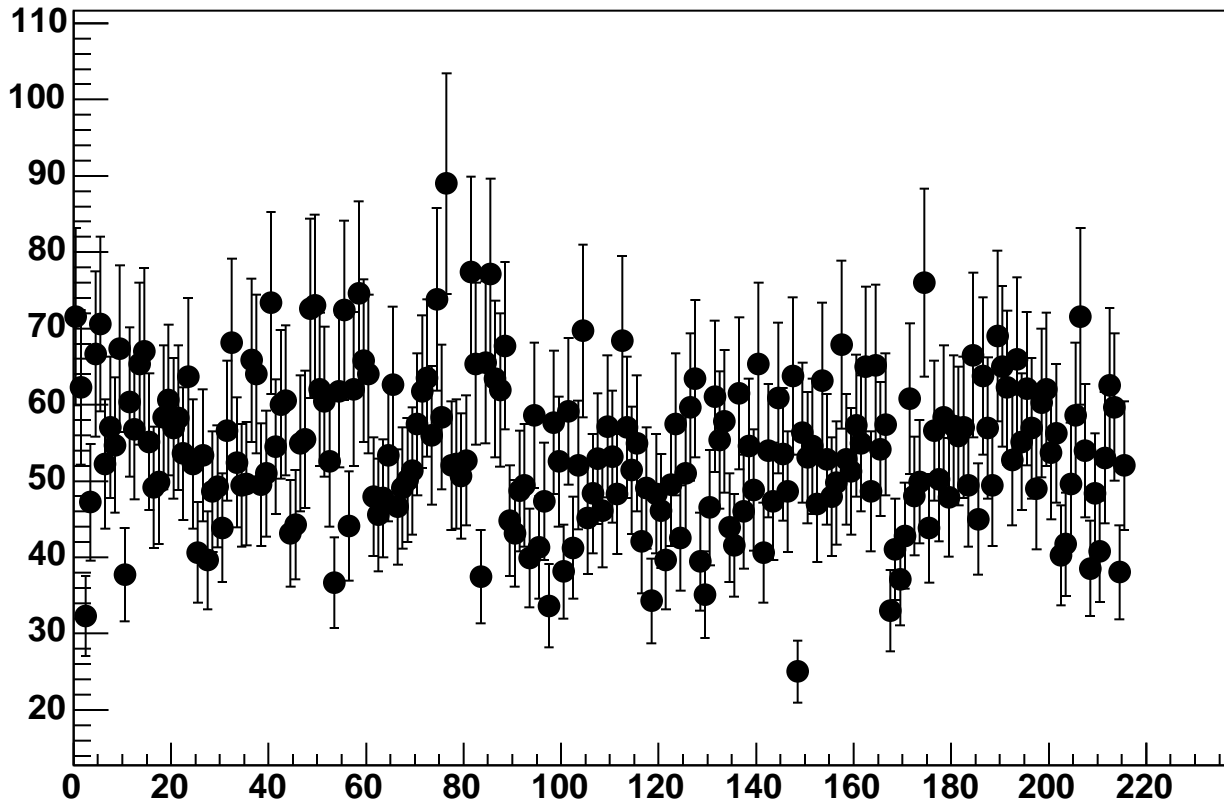
Enable 4, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



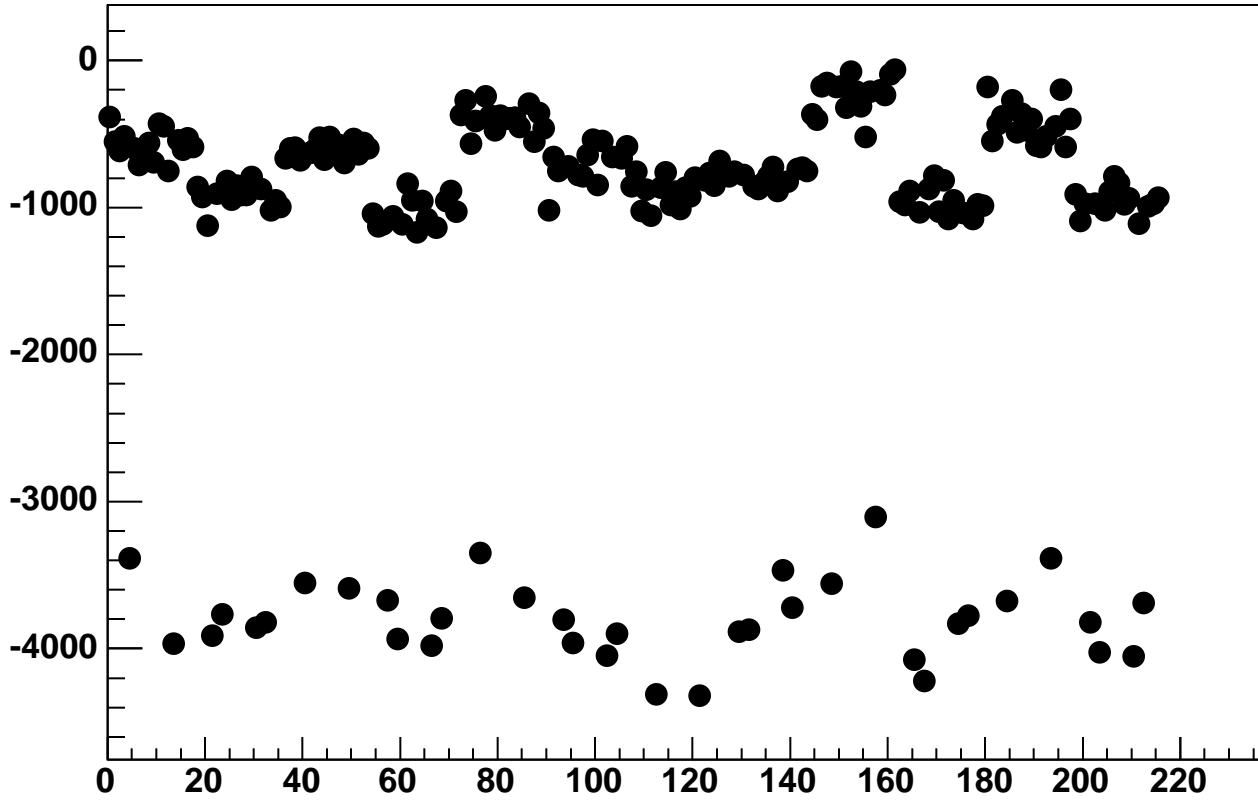
Enable 4, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan



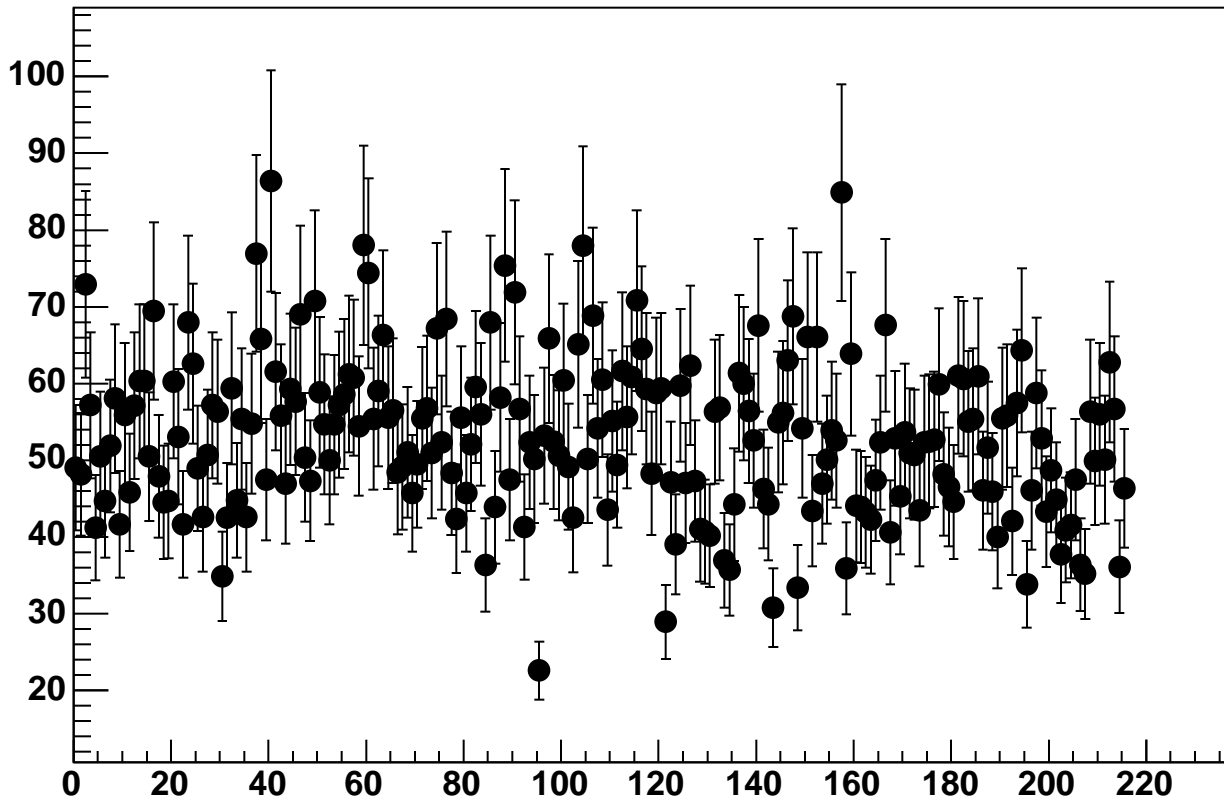
Enable 4, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan



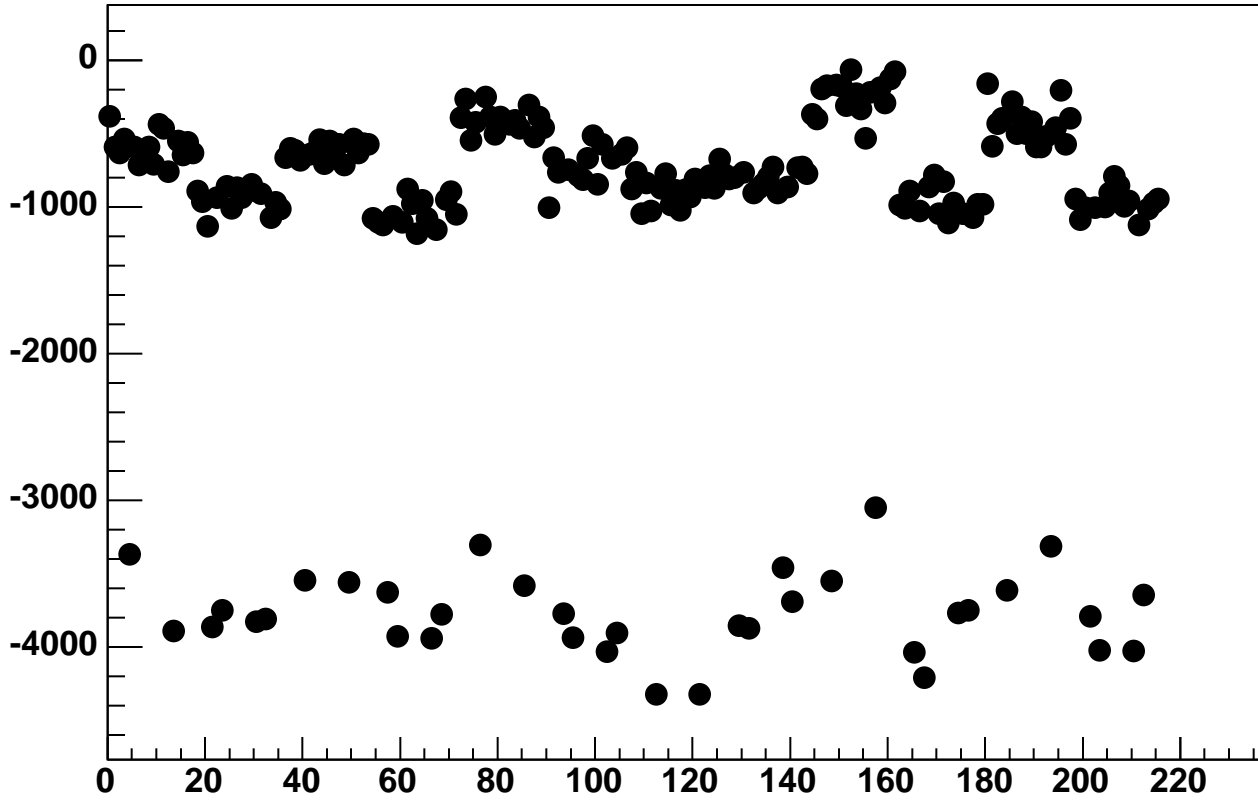
Enable 4, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



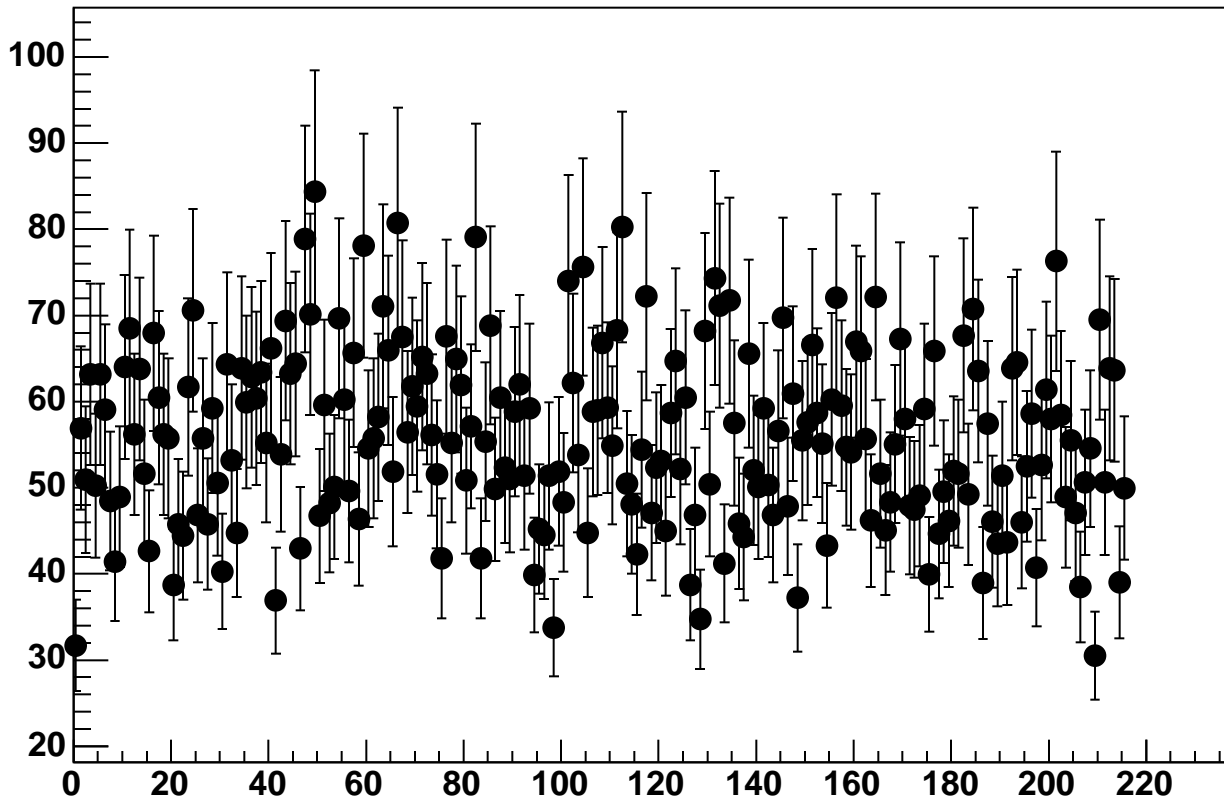
Enable 4, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



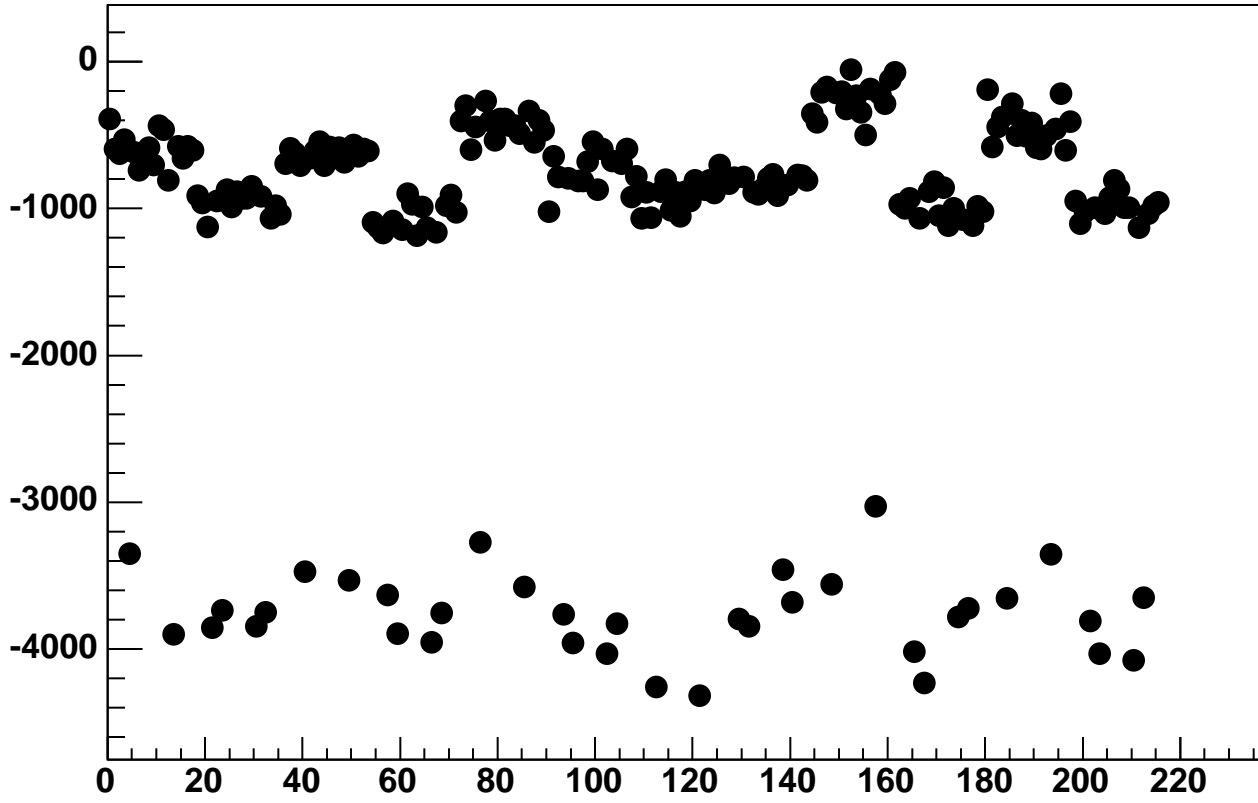
Enable 4, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan



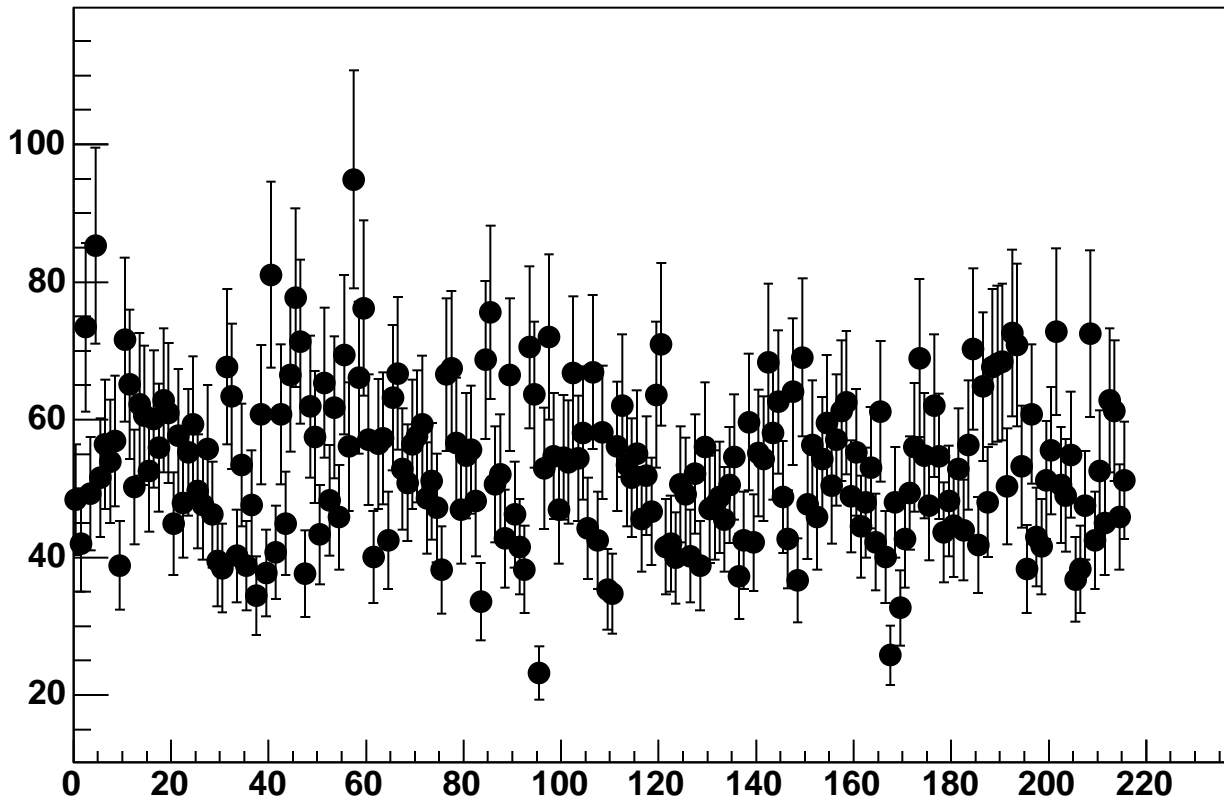
Enable 4, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan



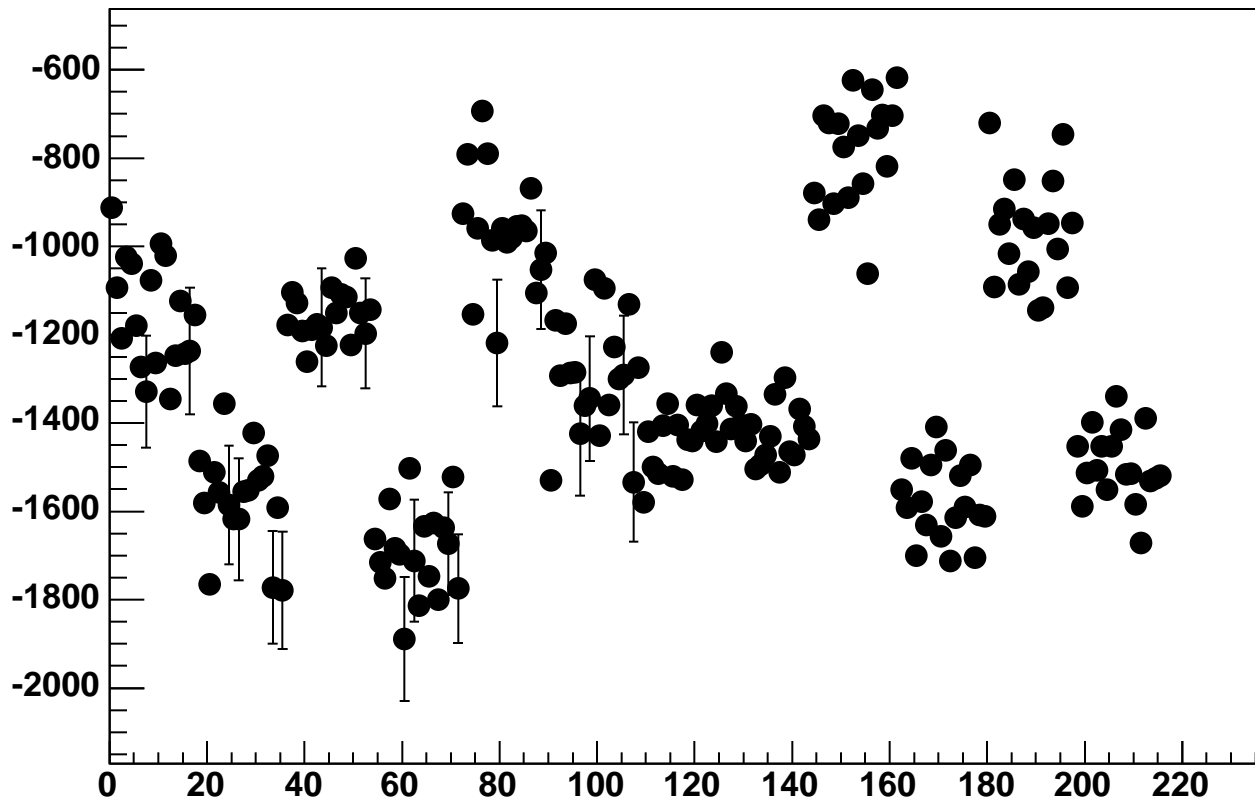
Enable 4, DAC=1600, Hold=245, ADC Mean vs 18\*Chip+Chan



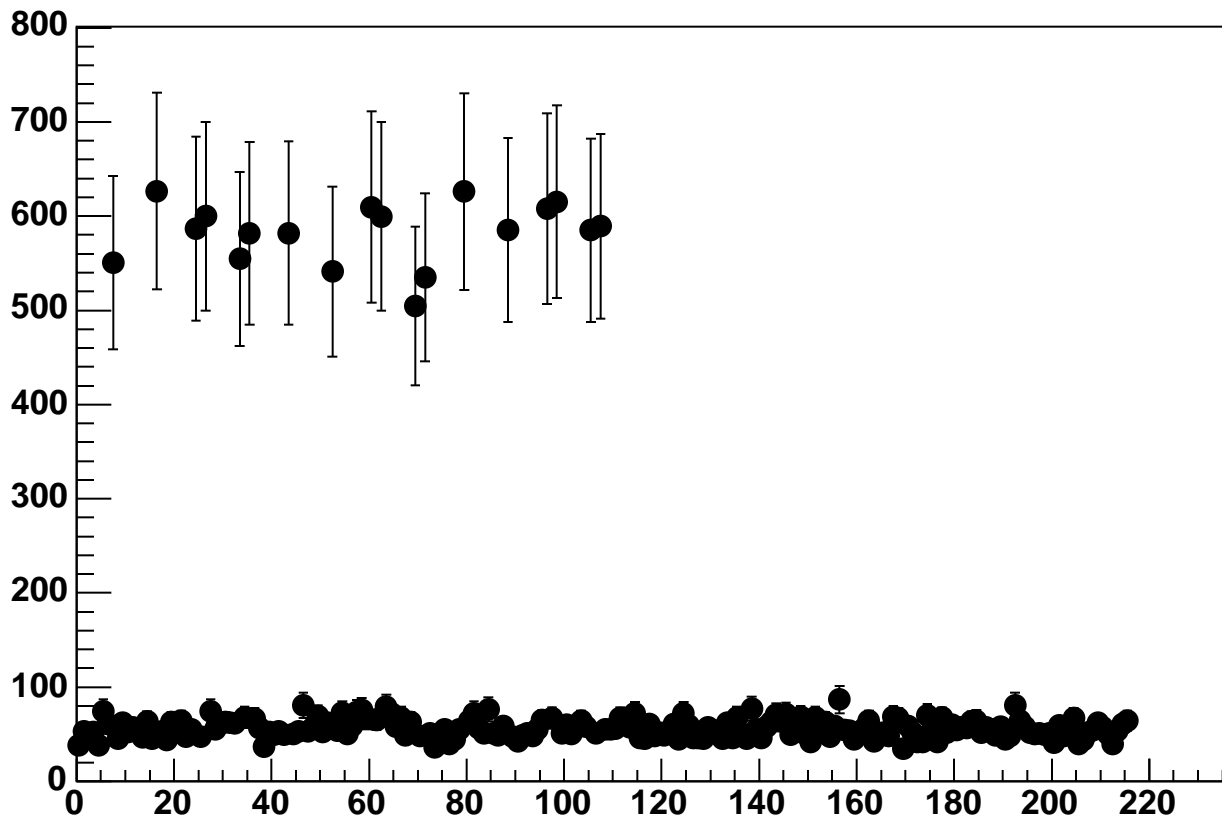
Enable 4, DAC=1600, Hold=245, ADC Noise vs 18\*Chip+Chan



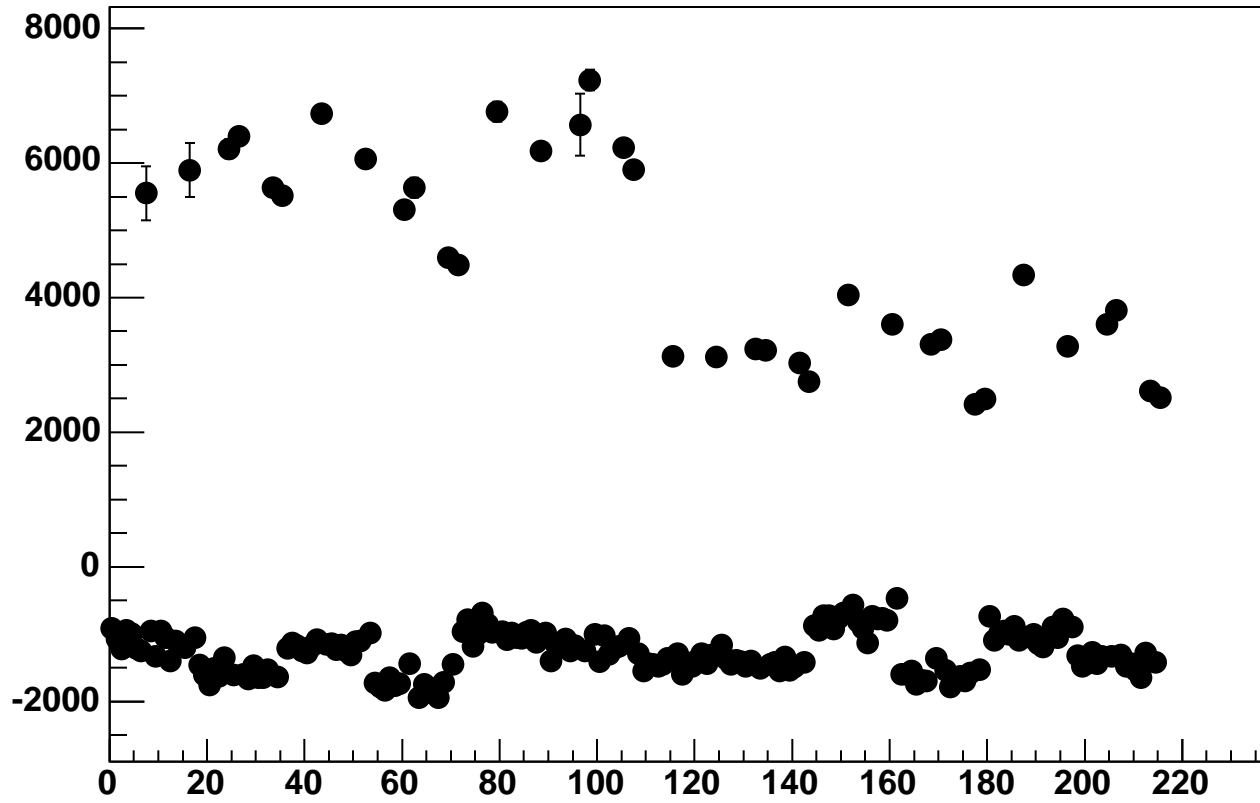
Enable 5, DAC=1600, Hold=0, ADC Mean vs 18\*Chip+Chan



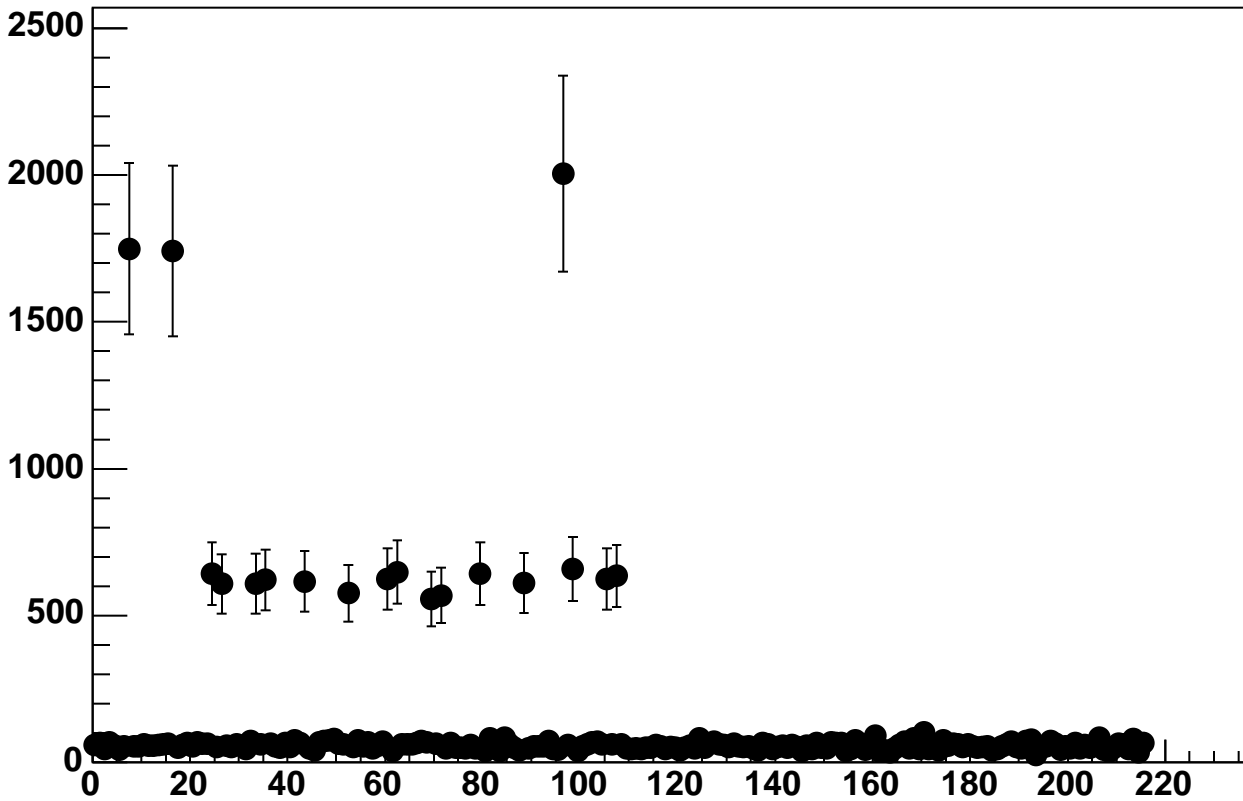
Enable 5, DAC=1600, Hold=0, ADC Noise vs 18\*Chip+Chan



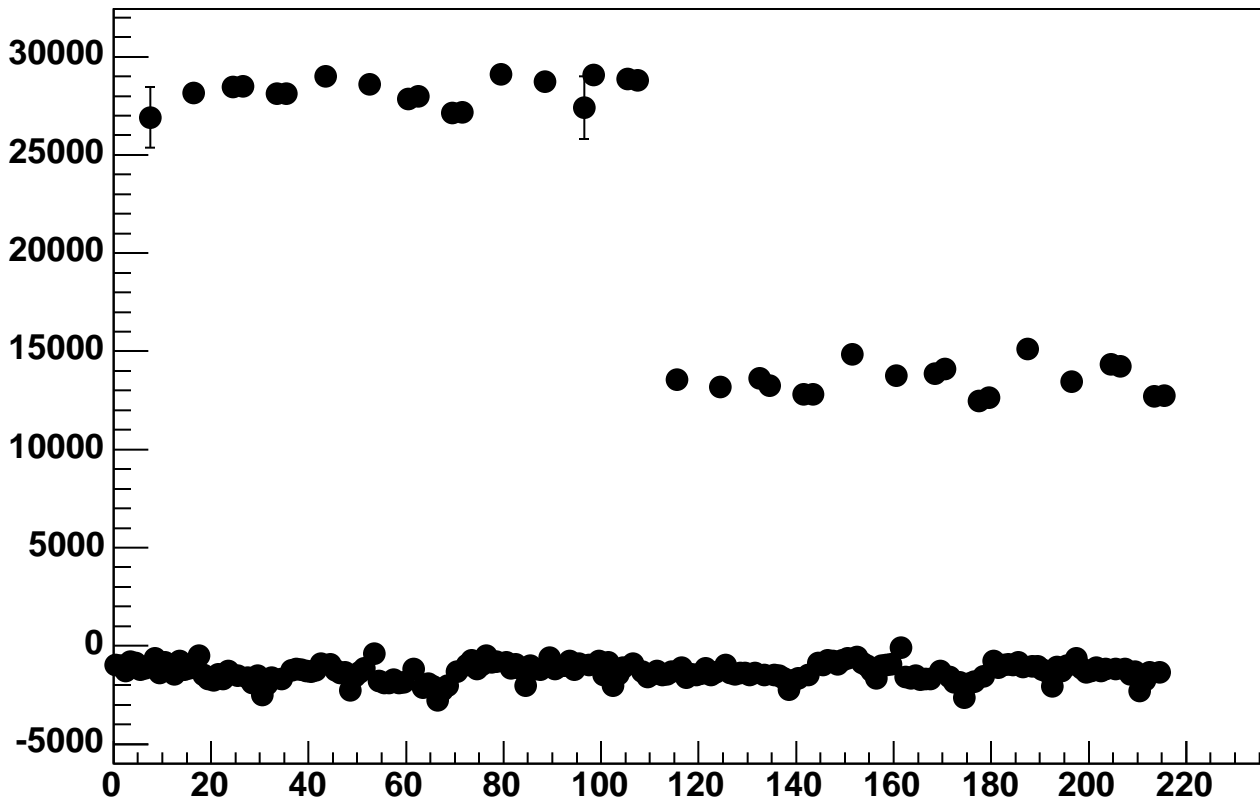
Enable 5, DAC=1600, Hold=5, ADC Mean vs 18\*Chip+Chan



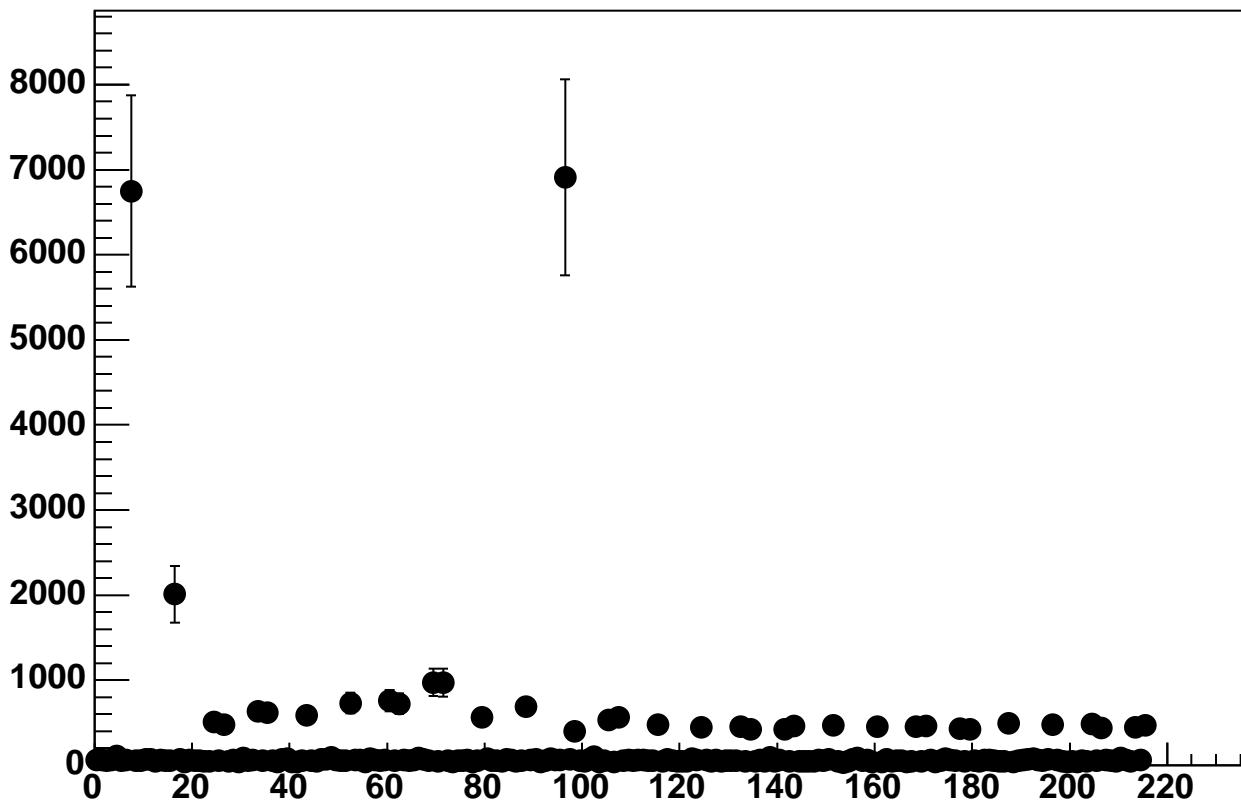
Enable 5, DAC=1600, Hold=5, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=10, ADC Mean vs 18\*Chip+Chan

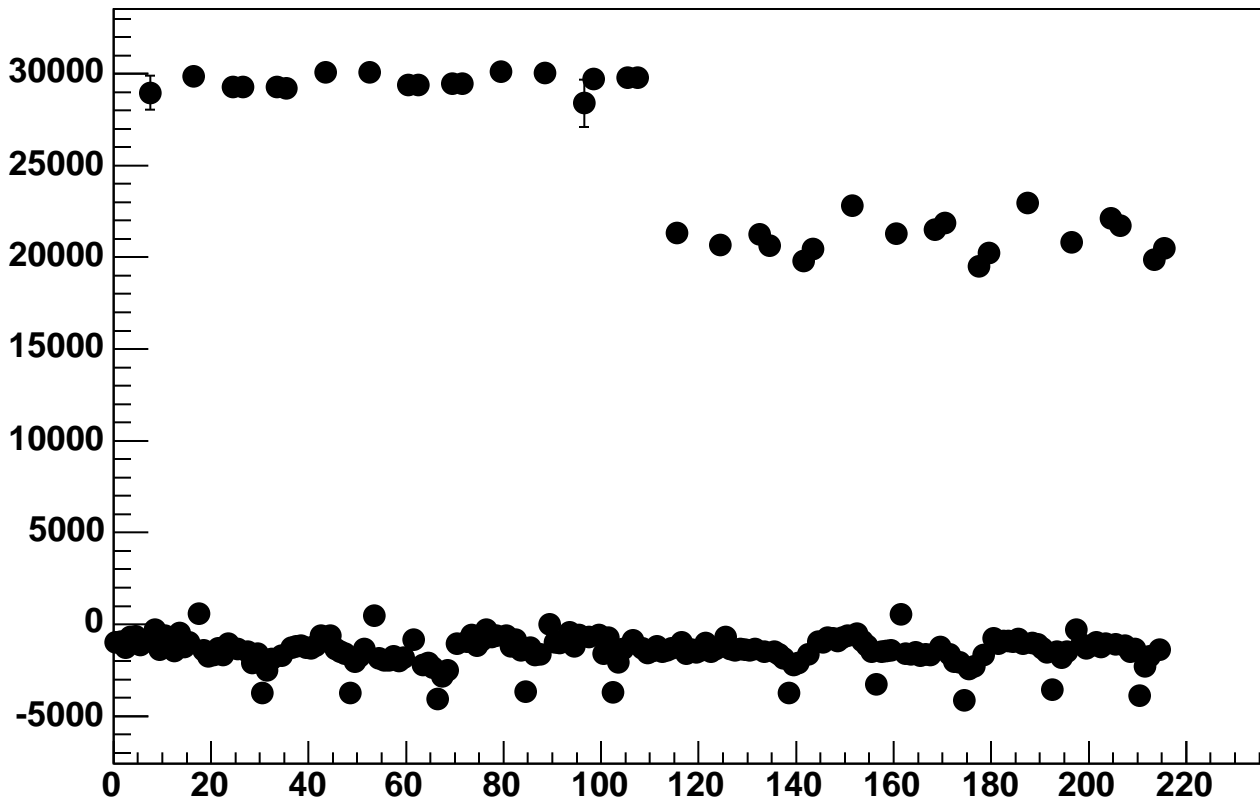


Enable 5, DAC=1600, Hold=10, ADC Noise vs 18\*Chip+Chan

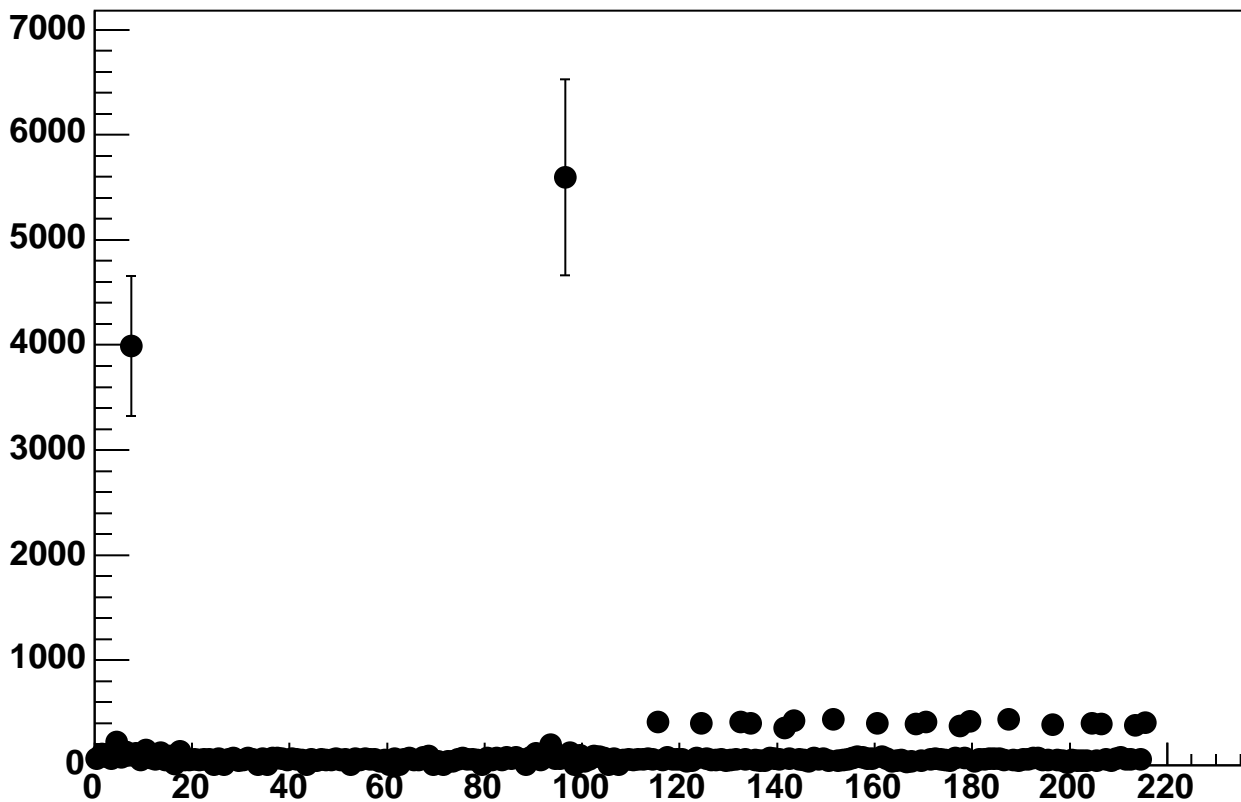




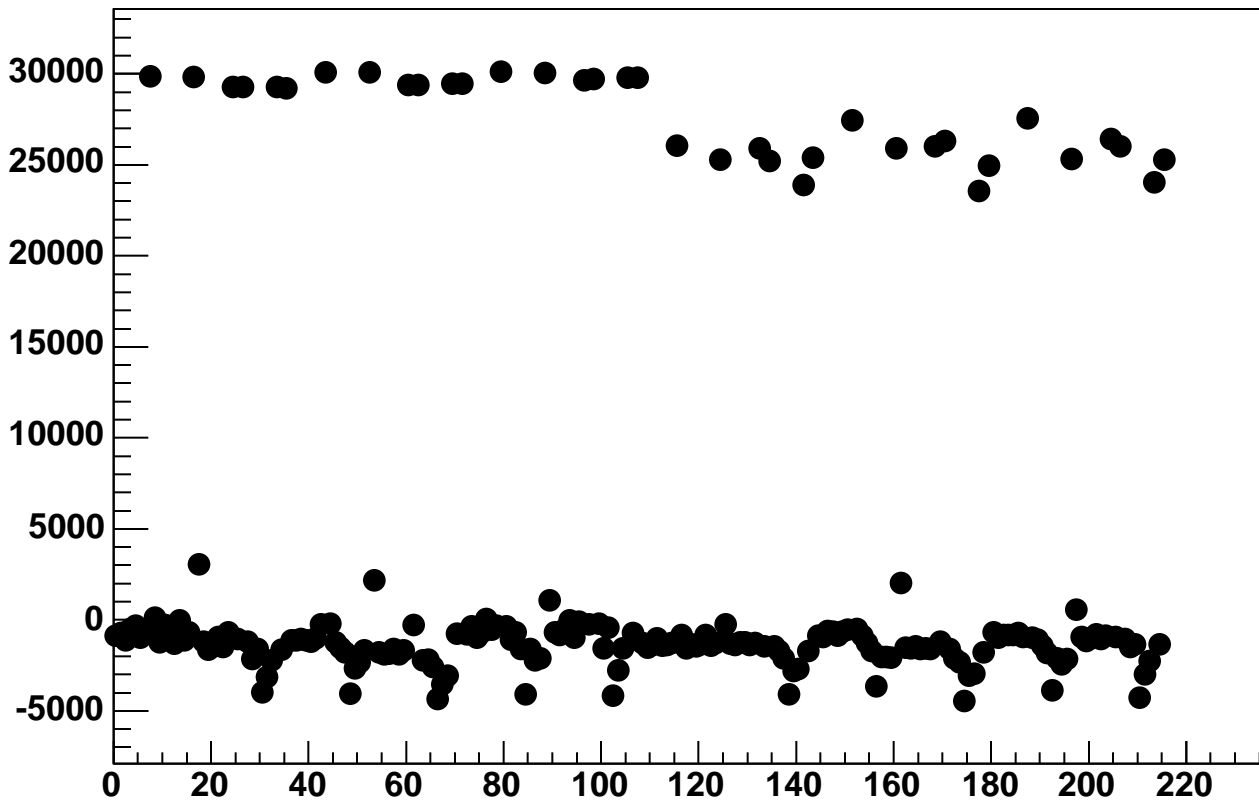
Enable 5, DAC=1600, Hold=15, ADC Mean vs 18\*Chip+Chan



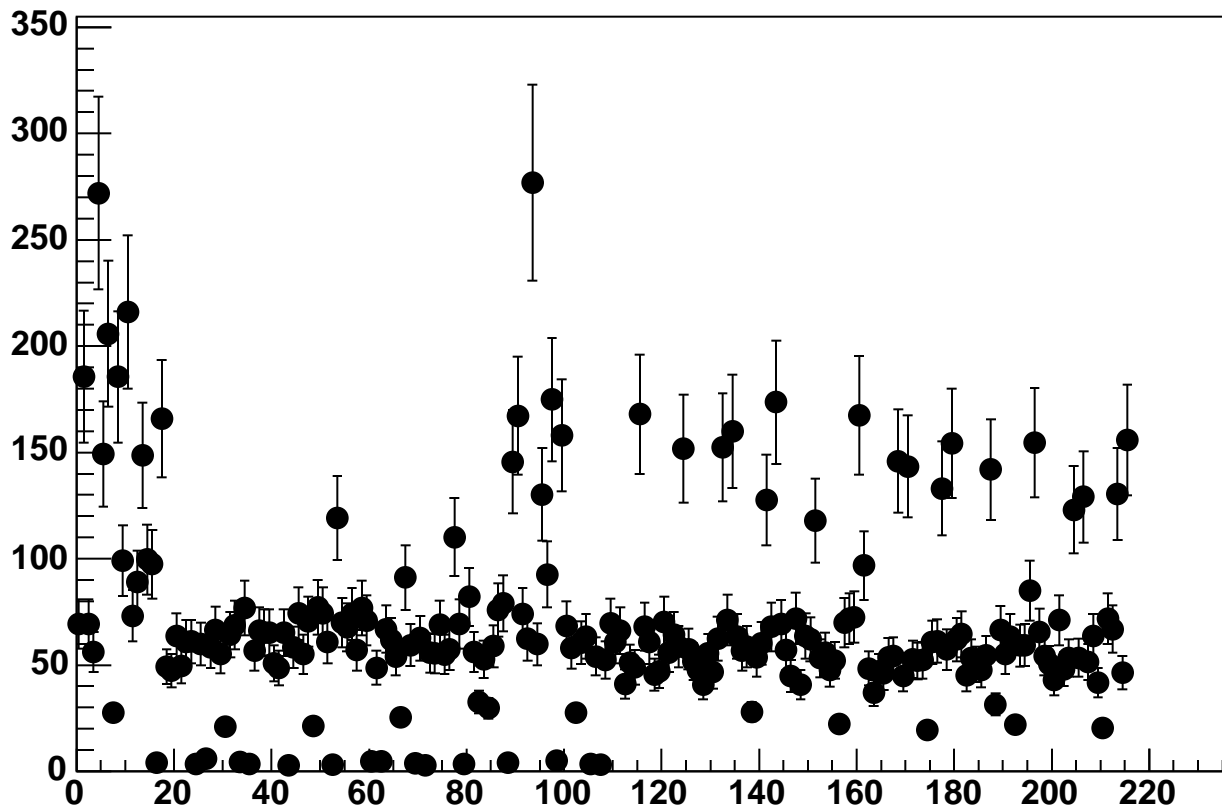
Enable 5, DAC=1600, Hold=15, ADC Noise vs 18\*Chip+Chan



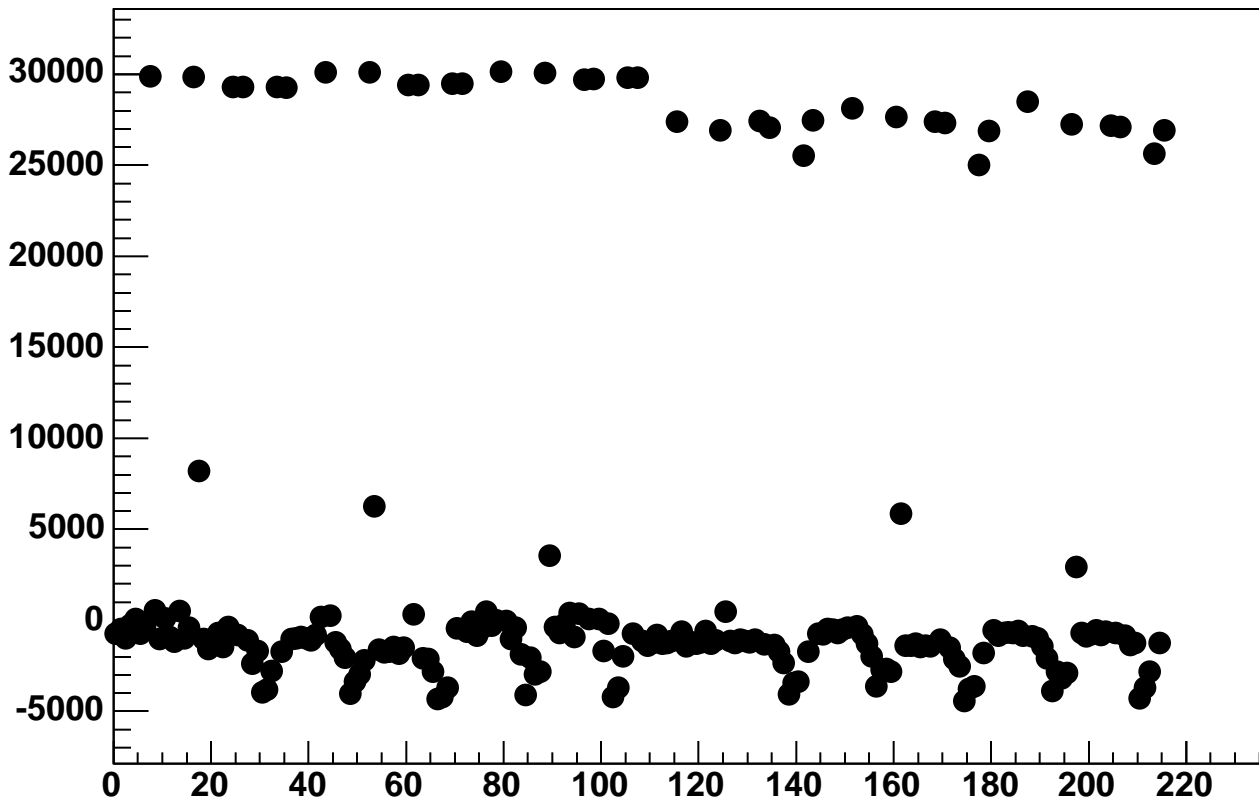
Enable 5, DAC=1600, Hold=20, ADC Mean vs 18\*Chip+Chan



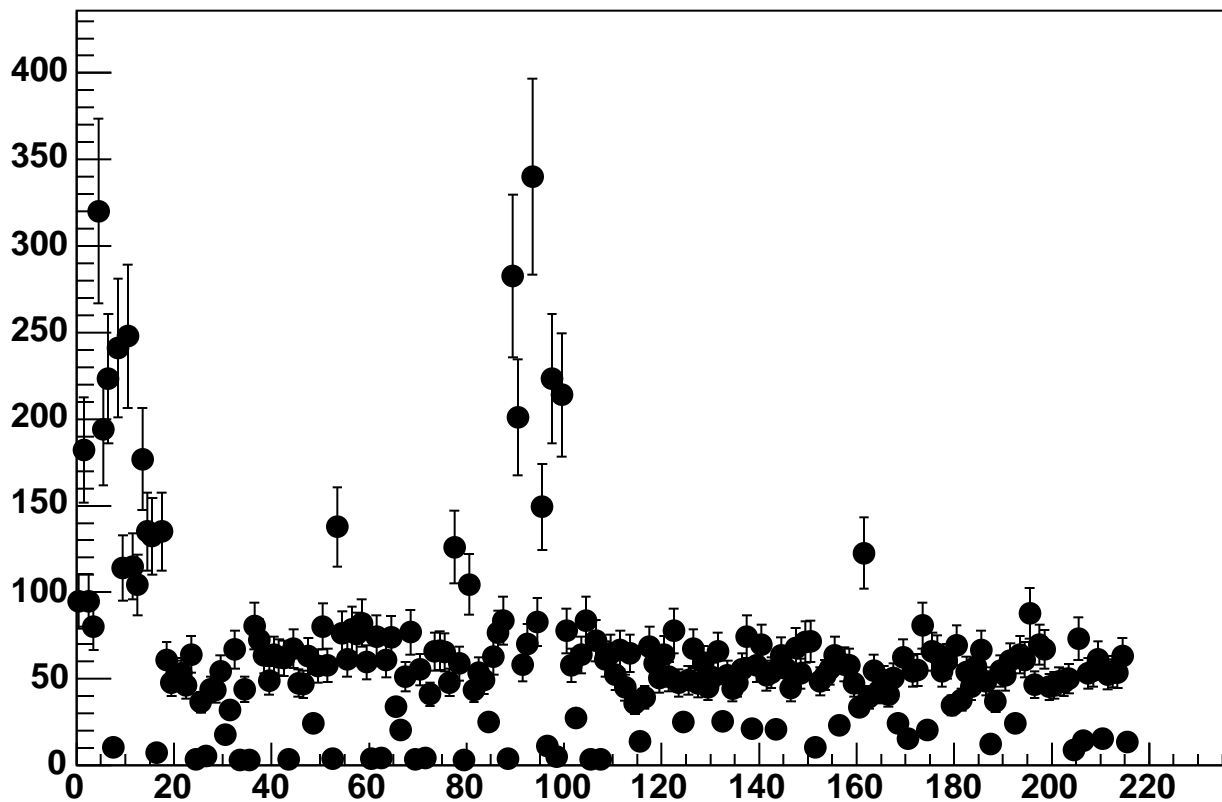
Enable 5, DAC=1600, Hold=20, ADC Noise vs 18\*Chip+Chan



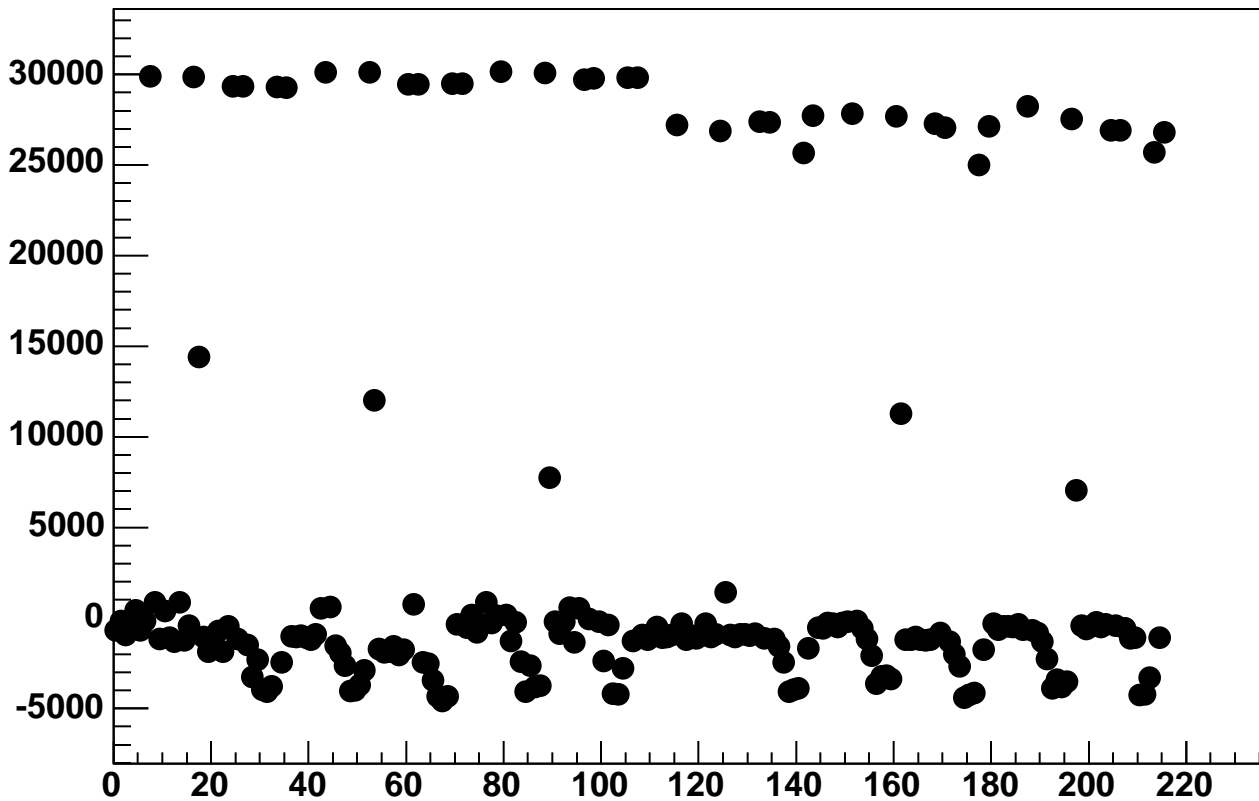
Enable 5, DAC=1600, Hold=25, ADC Mean vs 18\*Chip+Chan



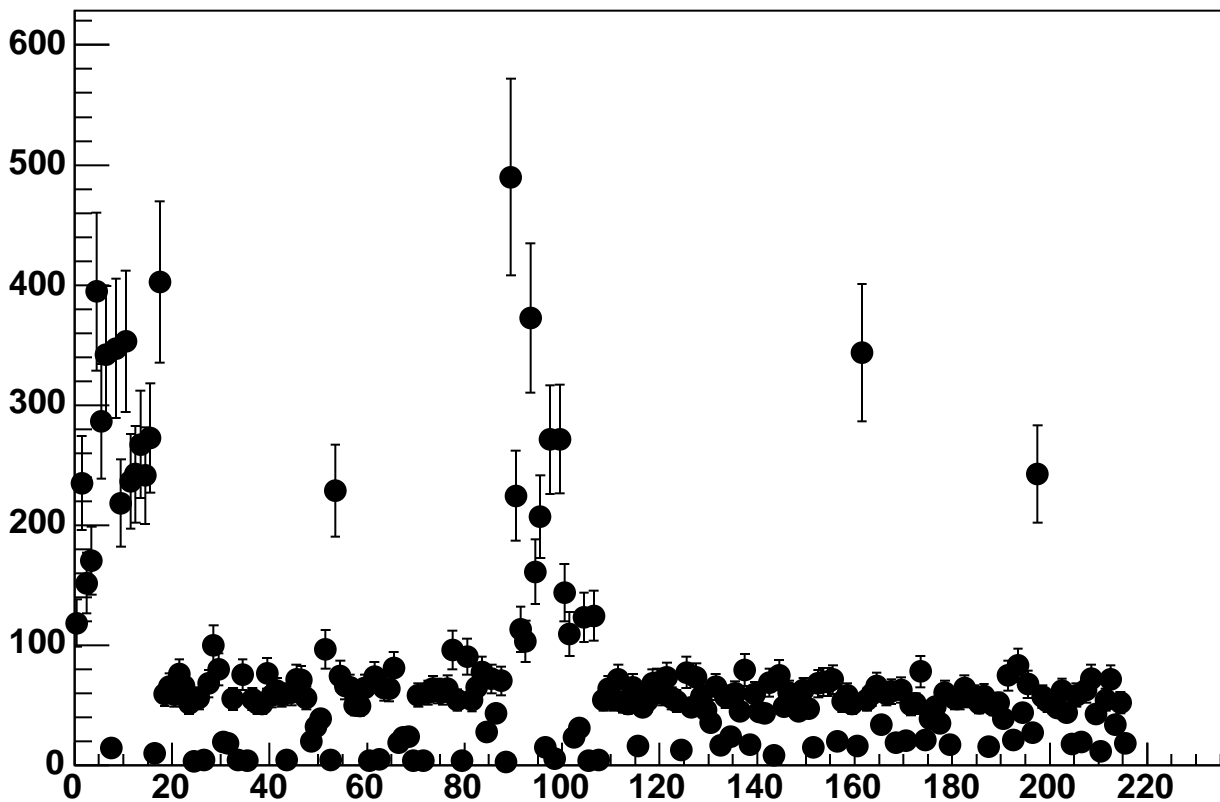
Enable 5, DAC=1600, Hold=25, ADC Noise vs 18\*Chip+Chan



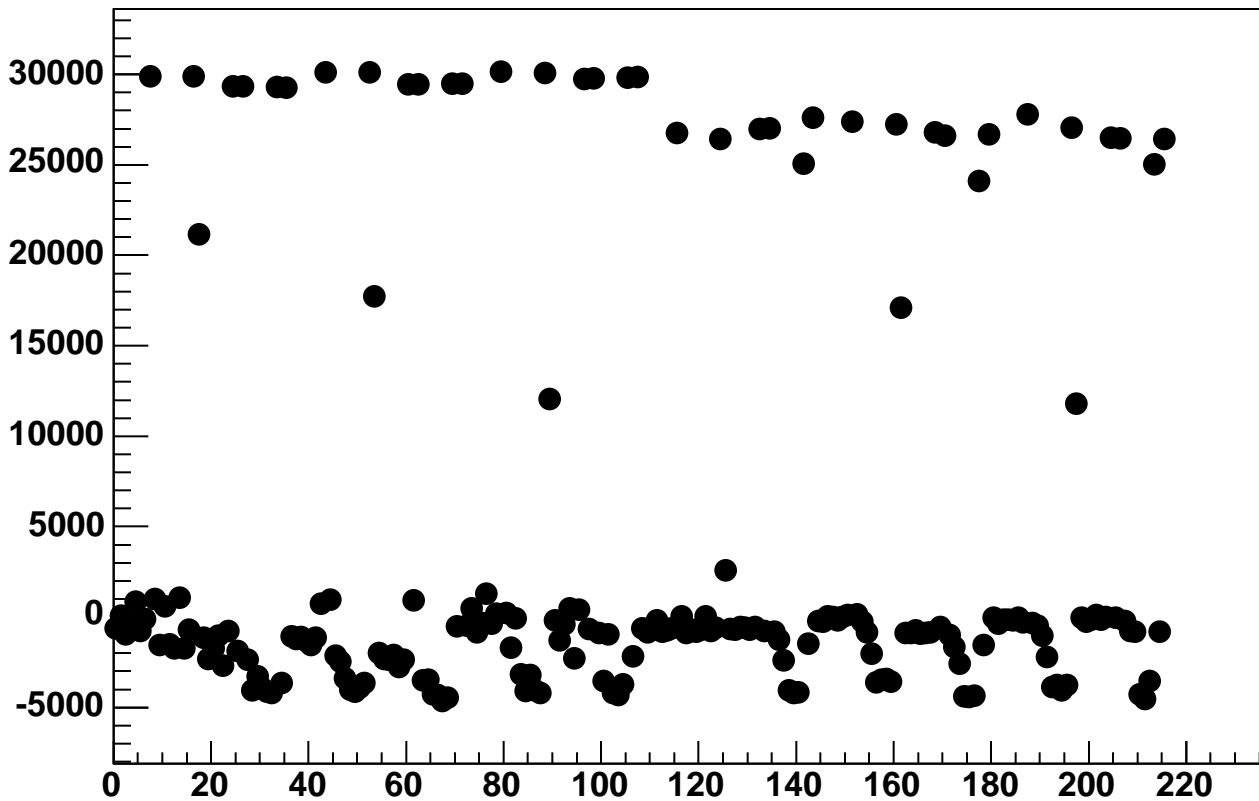
Enable 5, DAC=1600, Hold=30, ADC Mean vs 18\*Chip+Chan



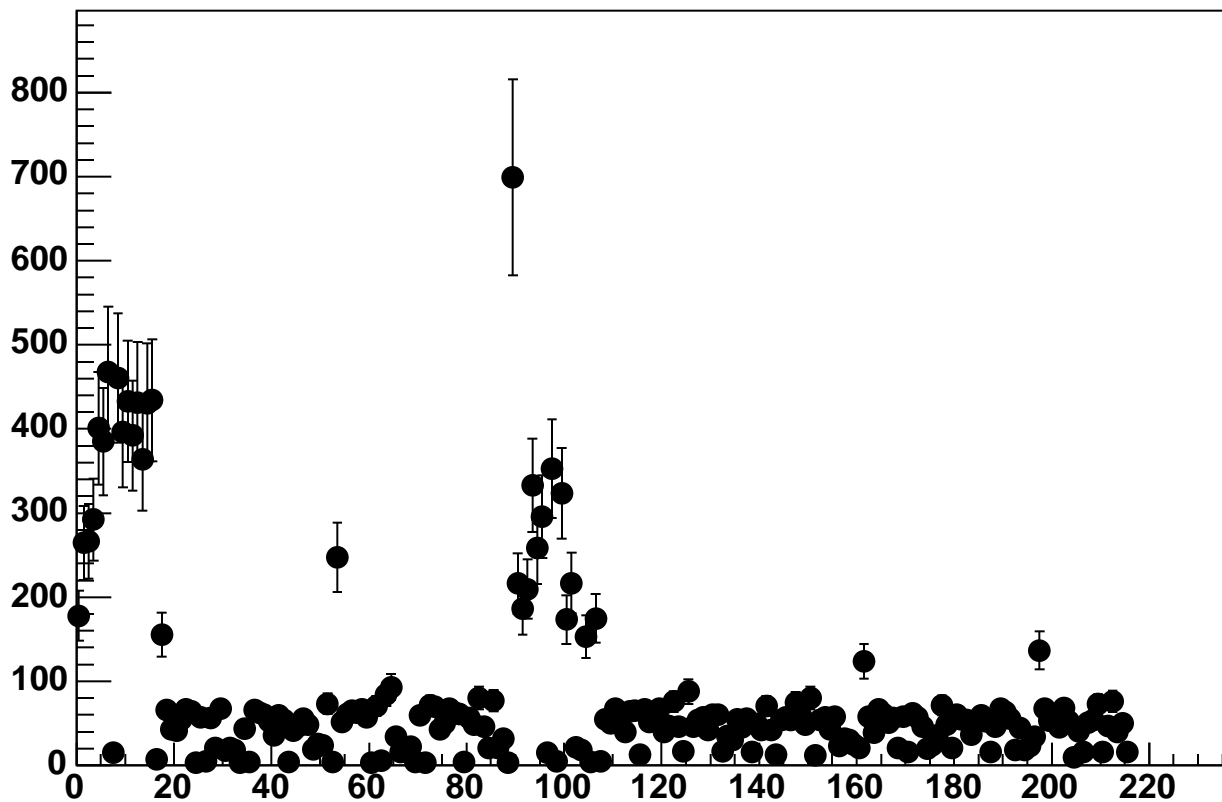
Enable 5, DAC=1600, Hold=30, ADC Noise vs 18\*Chip+Chan



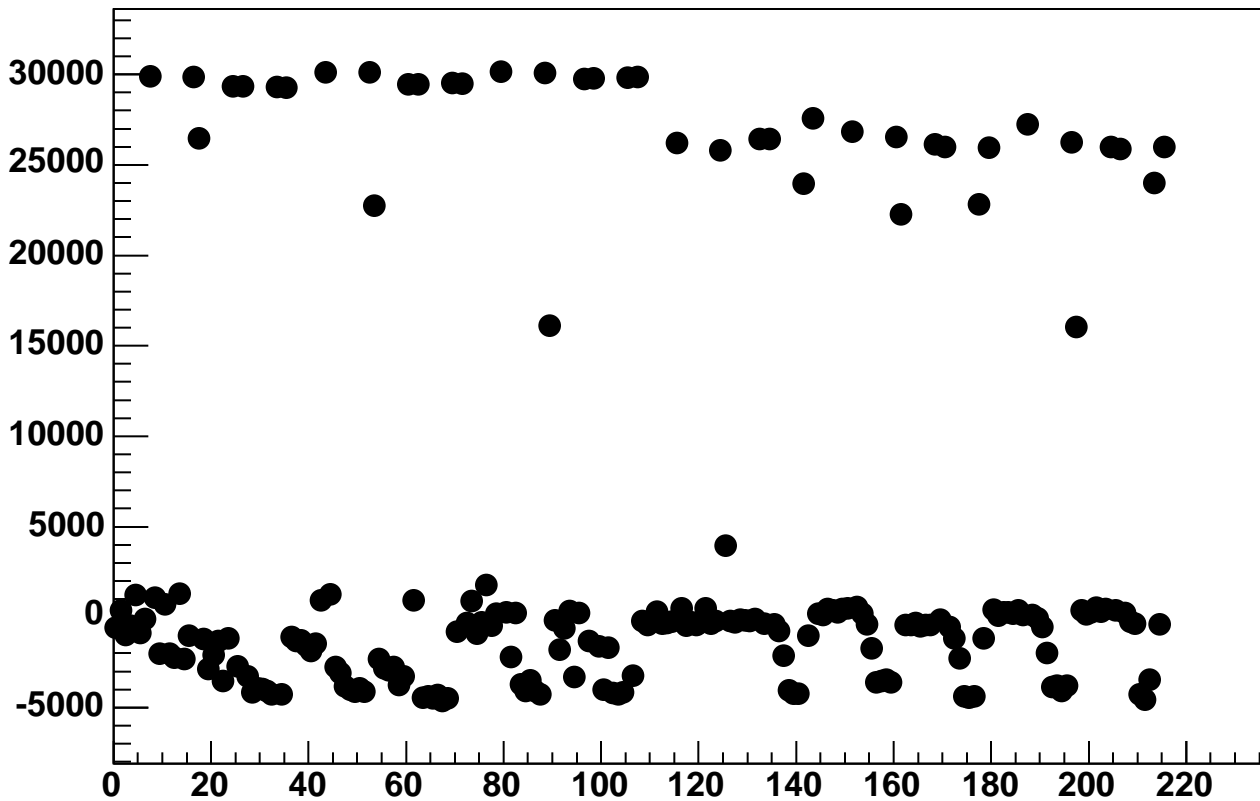
Enable 5, DAC=1600, Hold=35, ADC Mean vs 18\*Chip+Chan



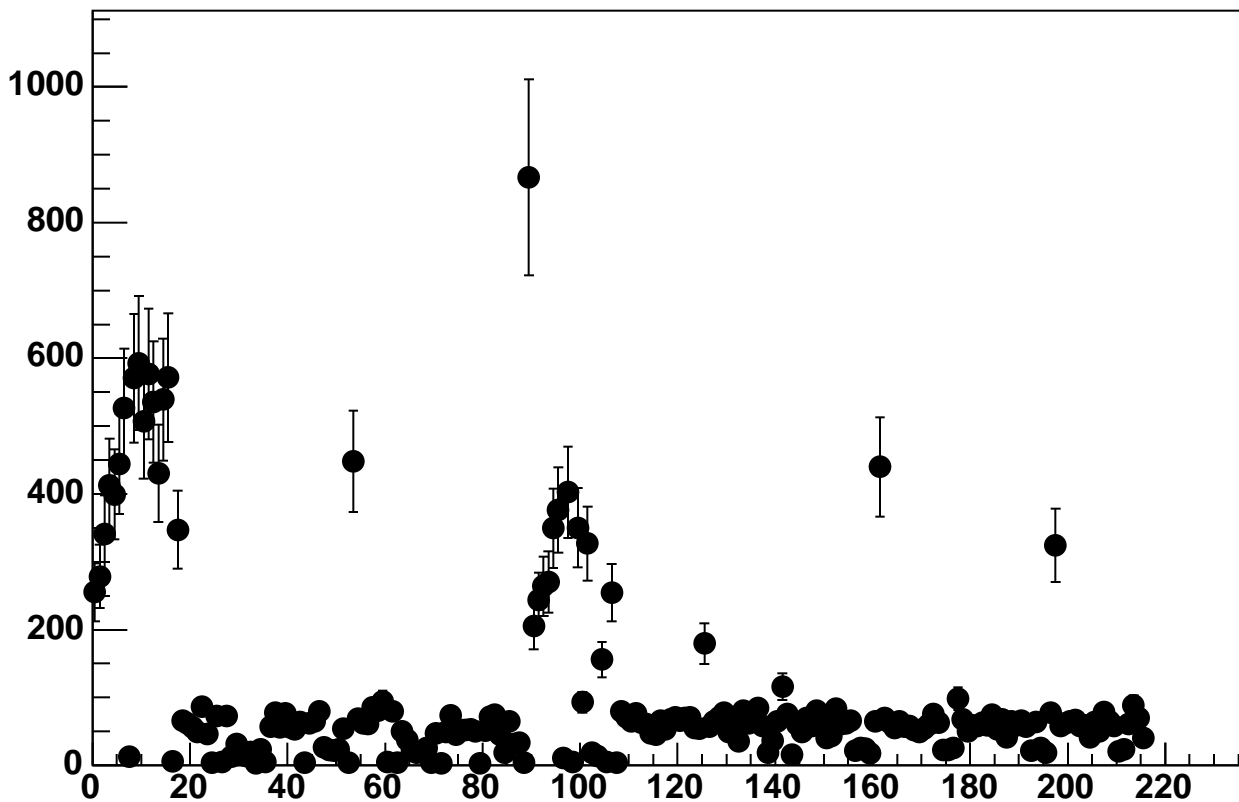
Enable 5, DAC=1600, Hold=35, ADC Noise vs 18\*Chip+Chan



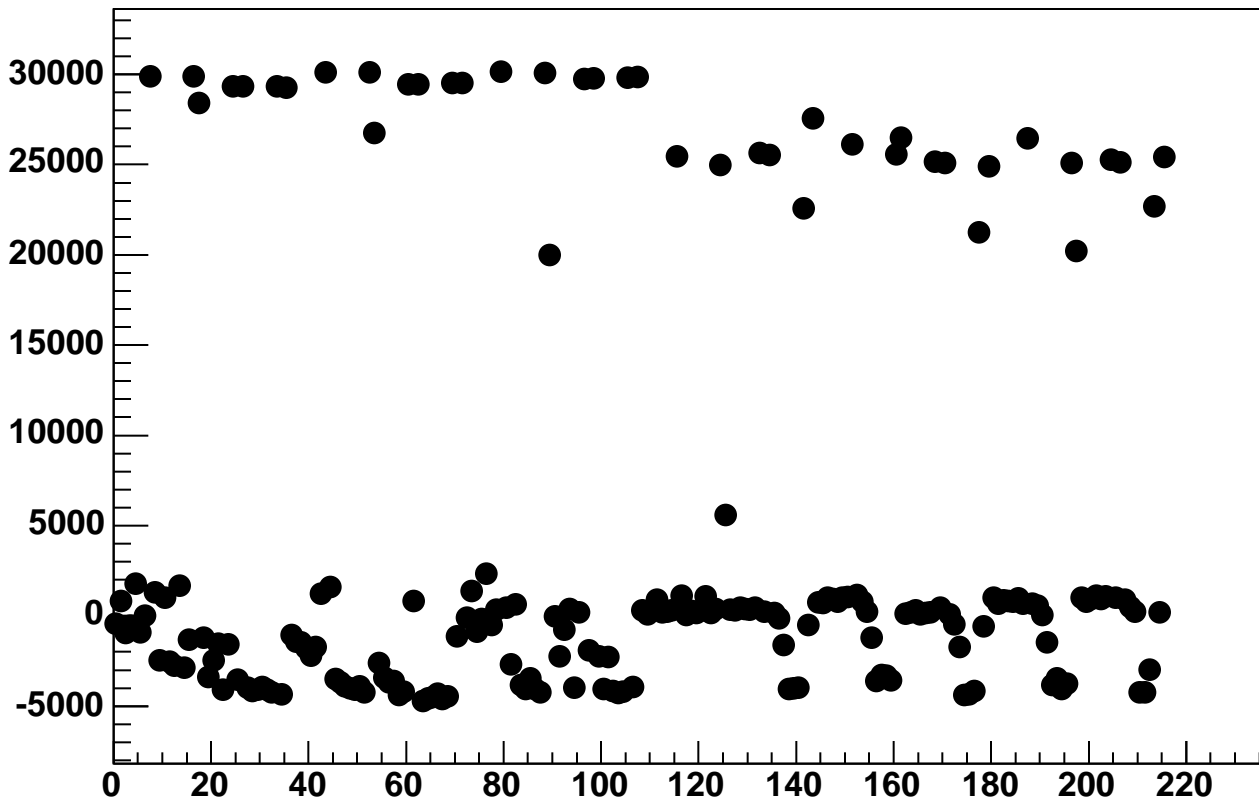
Enable 5, DAC=1600, Hold=40, ADC Mean vs 18\*Chip+Chan



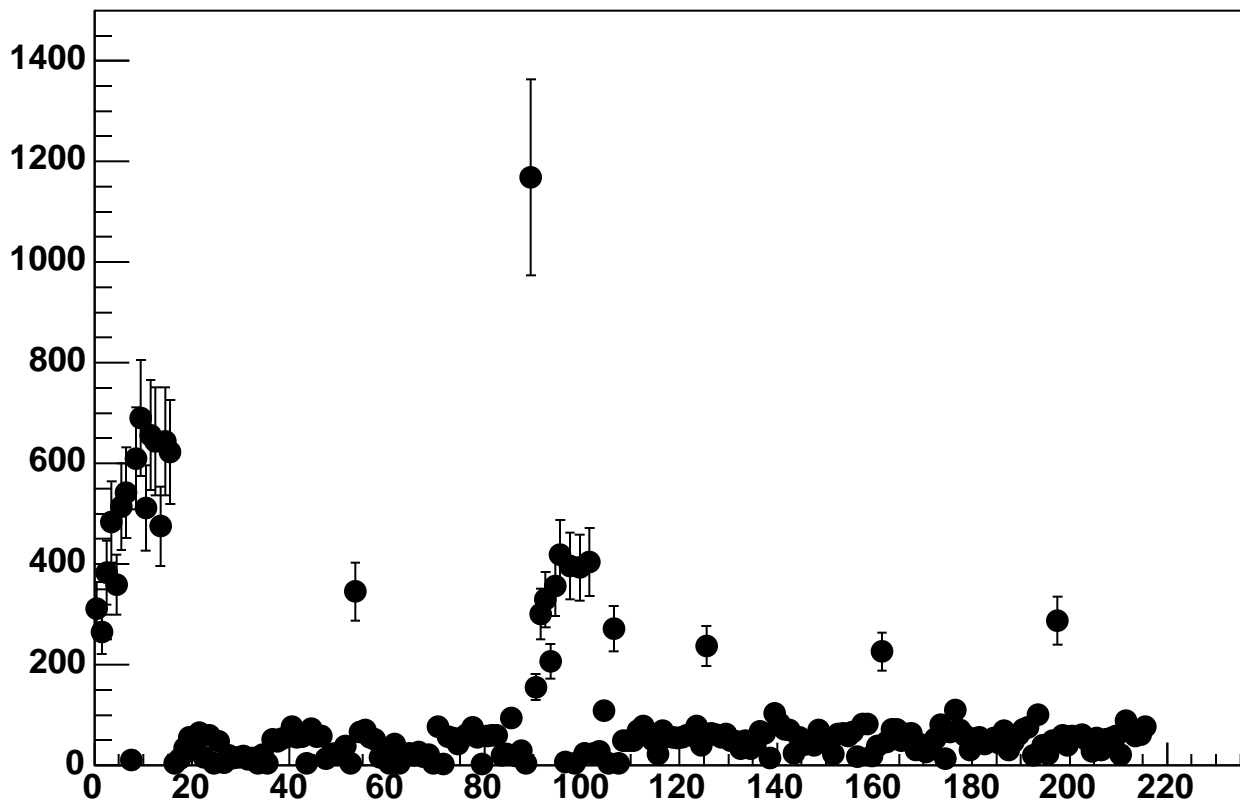
Enable 5, DAC=1600, Hold=40, ADC Noise vs 18\*Chip+Chan



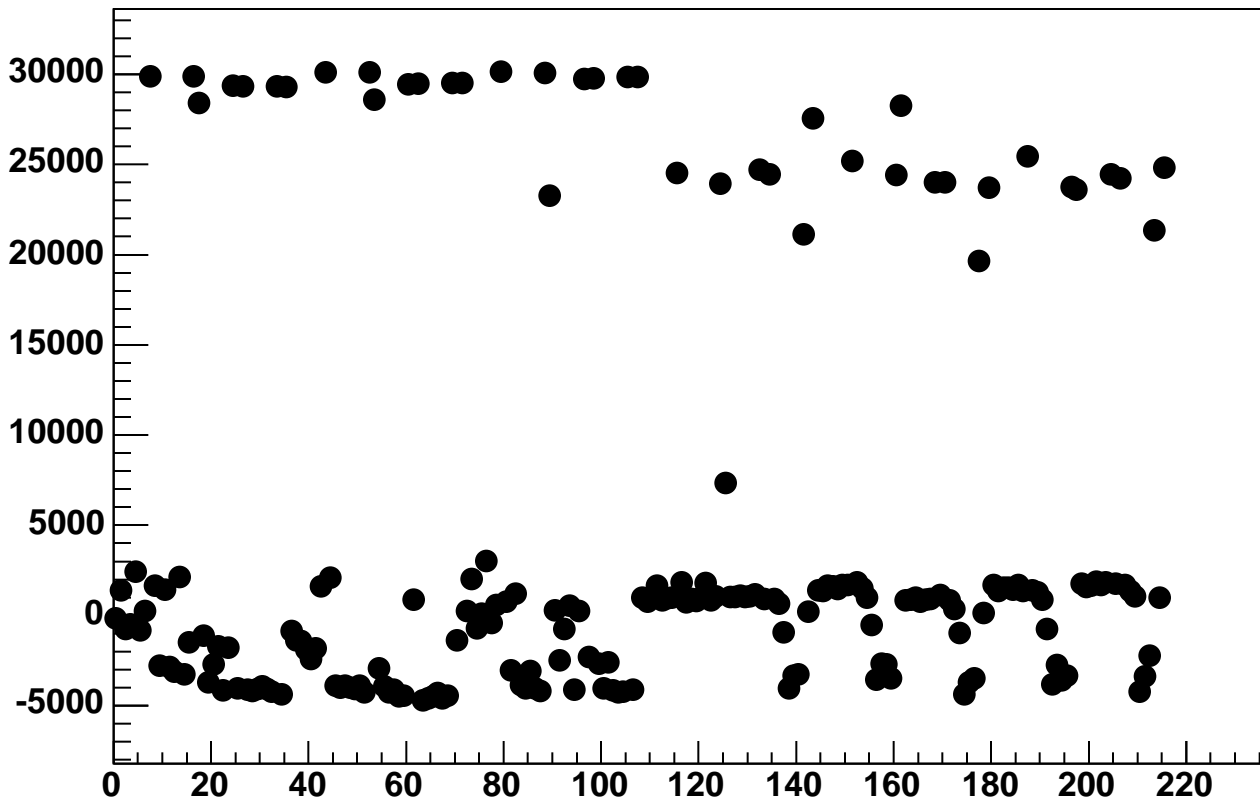
Enable 5, DAC=1600, Hold=45, ADC Mean vs 18\*Chip+Chan



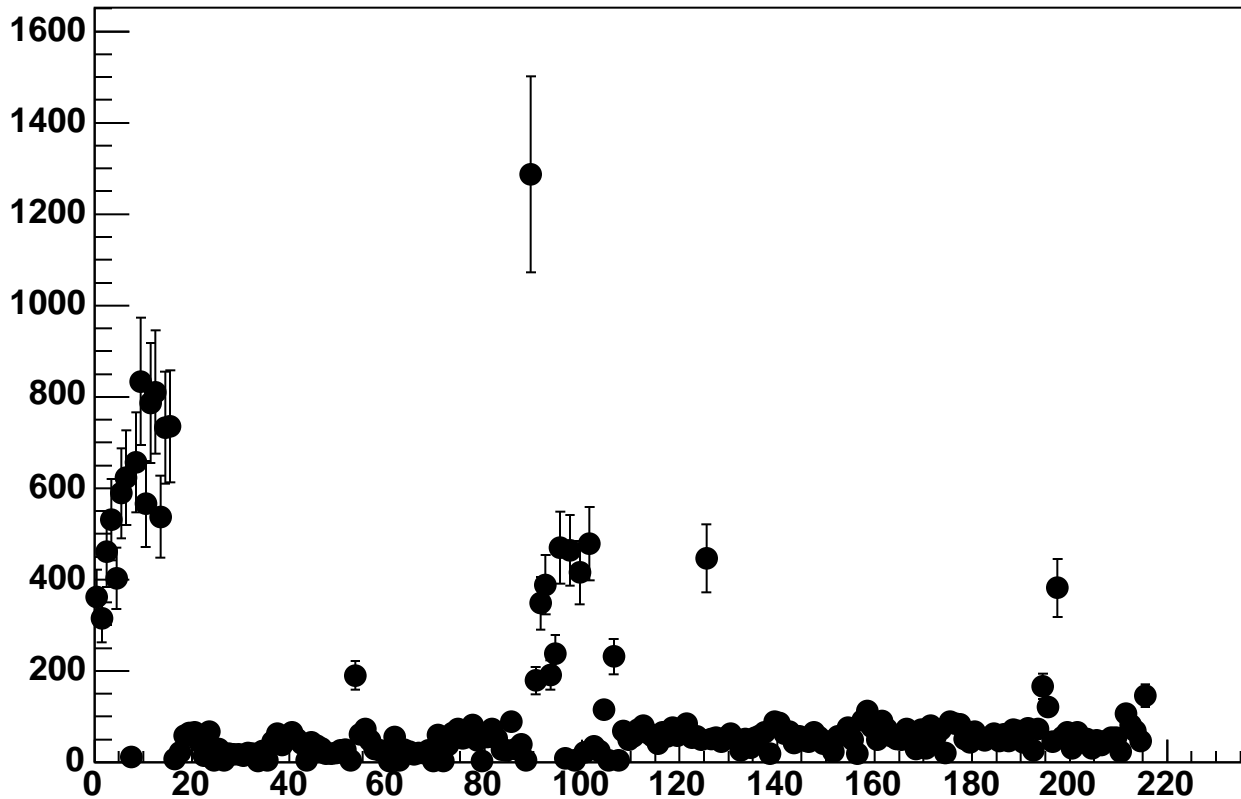
Enable 5, DAC=1600, Hold=45, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=50, ADC Mean vs 18\*Chip+Chan

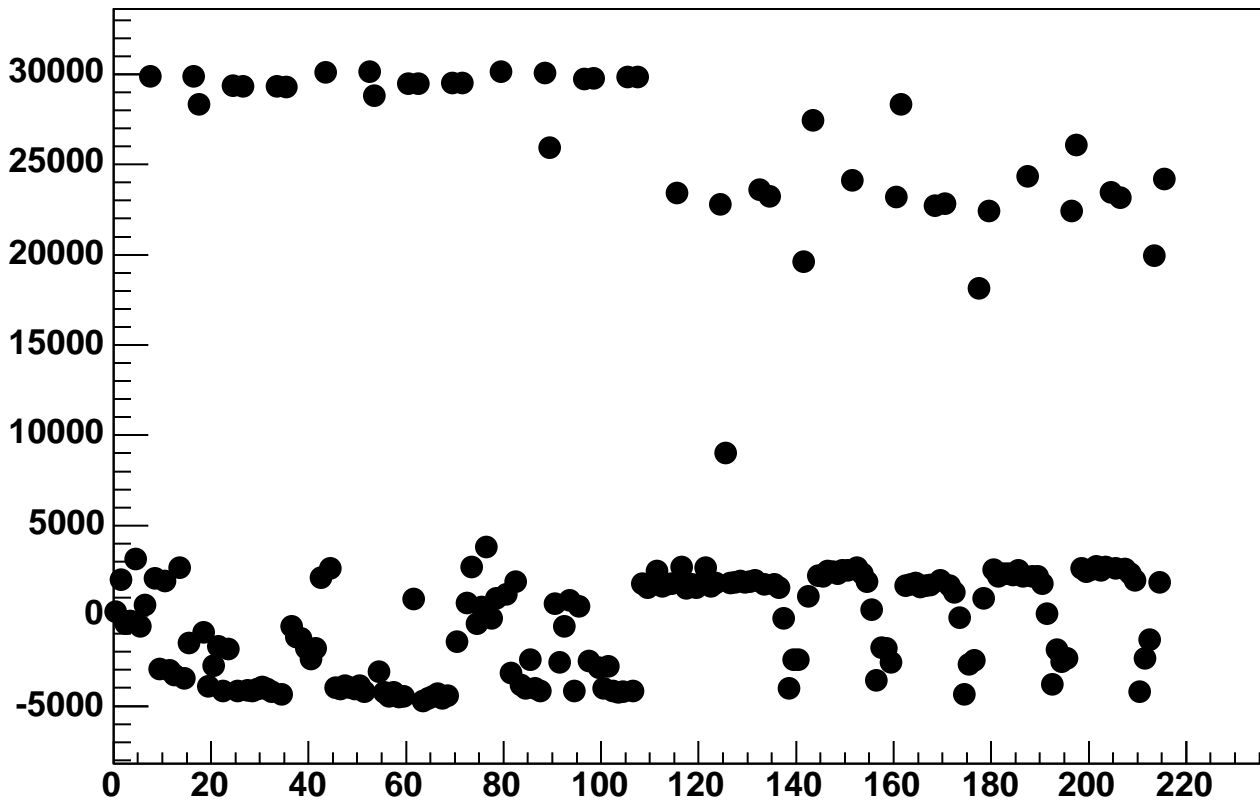


Enable 5, DAC=1600, Hold=50, ADC Noise vs 18\*Chip+Chan

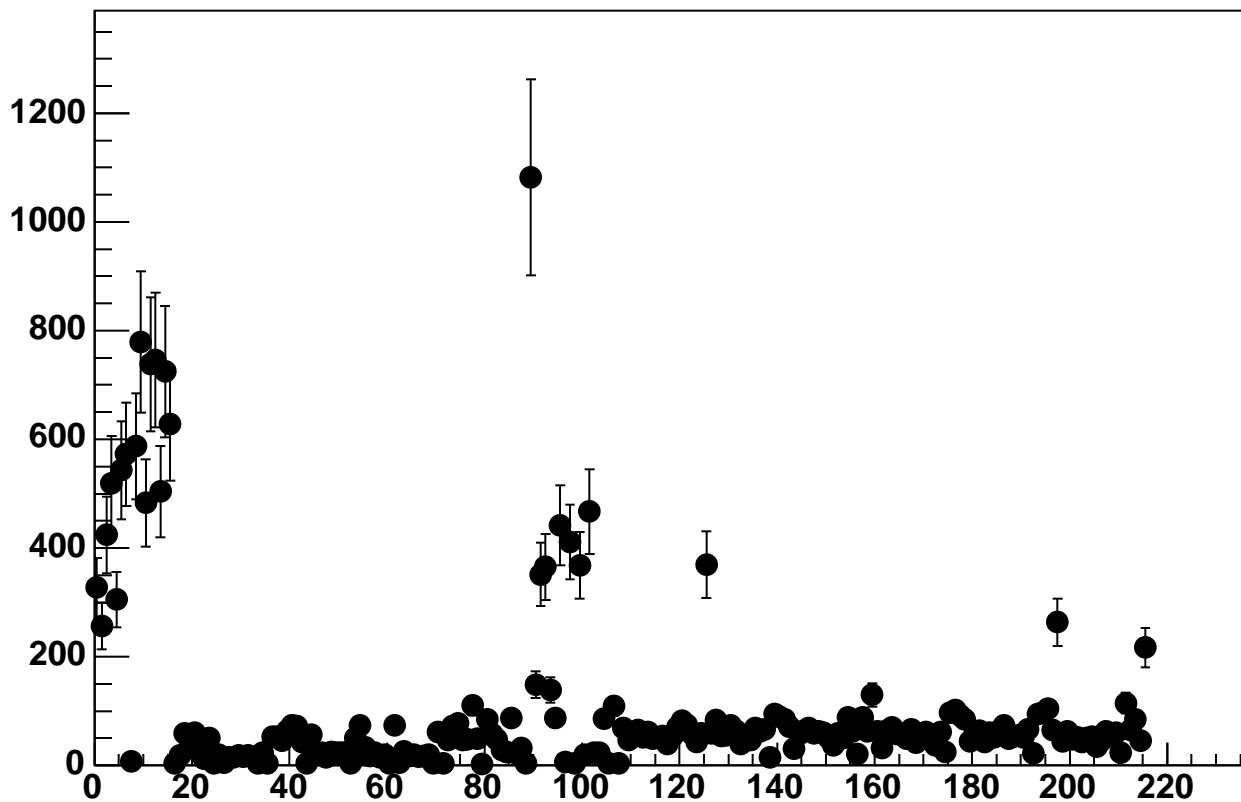




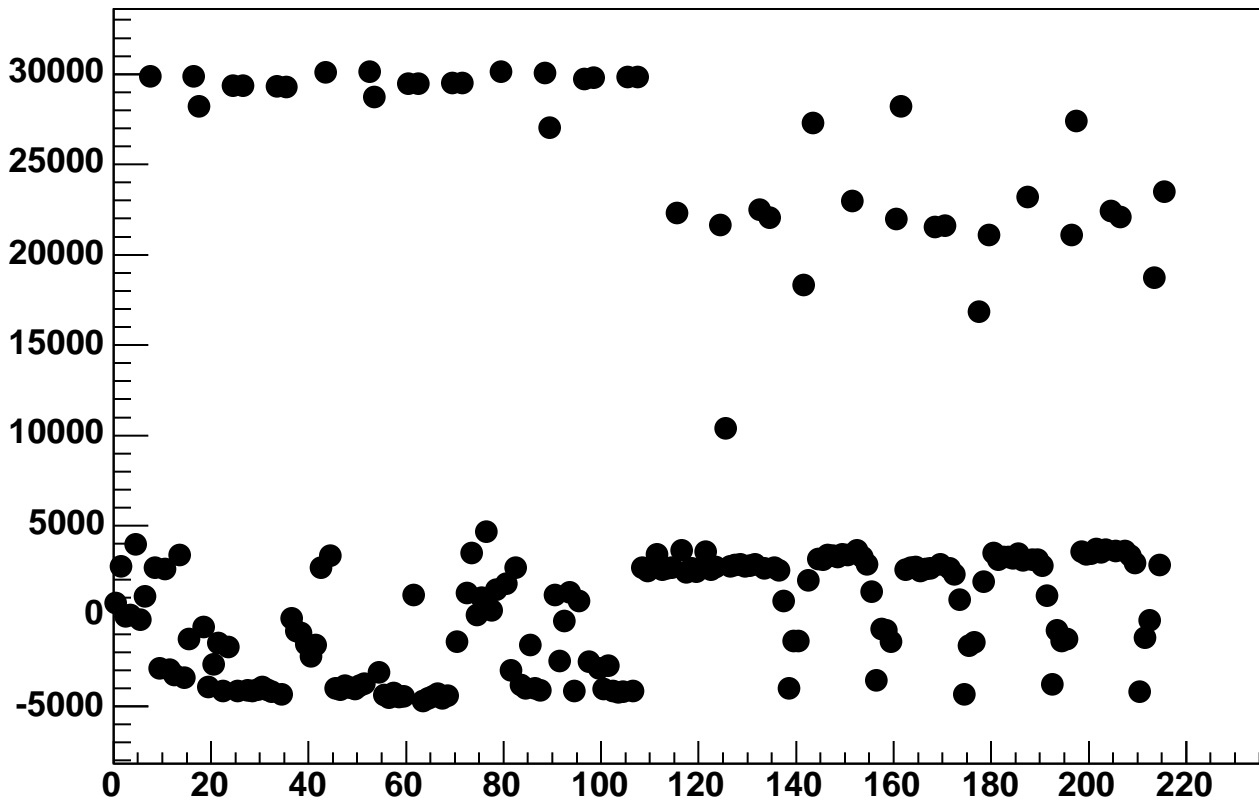
Enable 5, DAC=1600, Hold=55, ADC Mean vs 18\*Chip+Chan



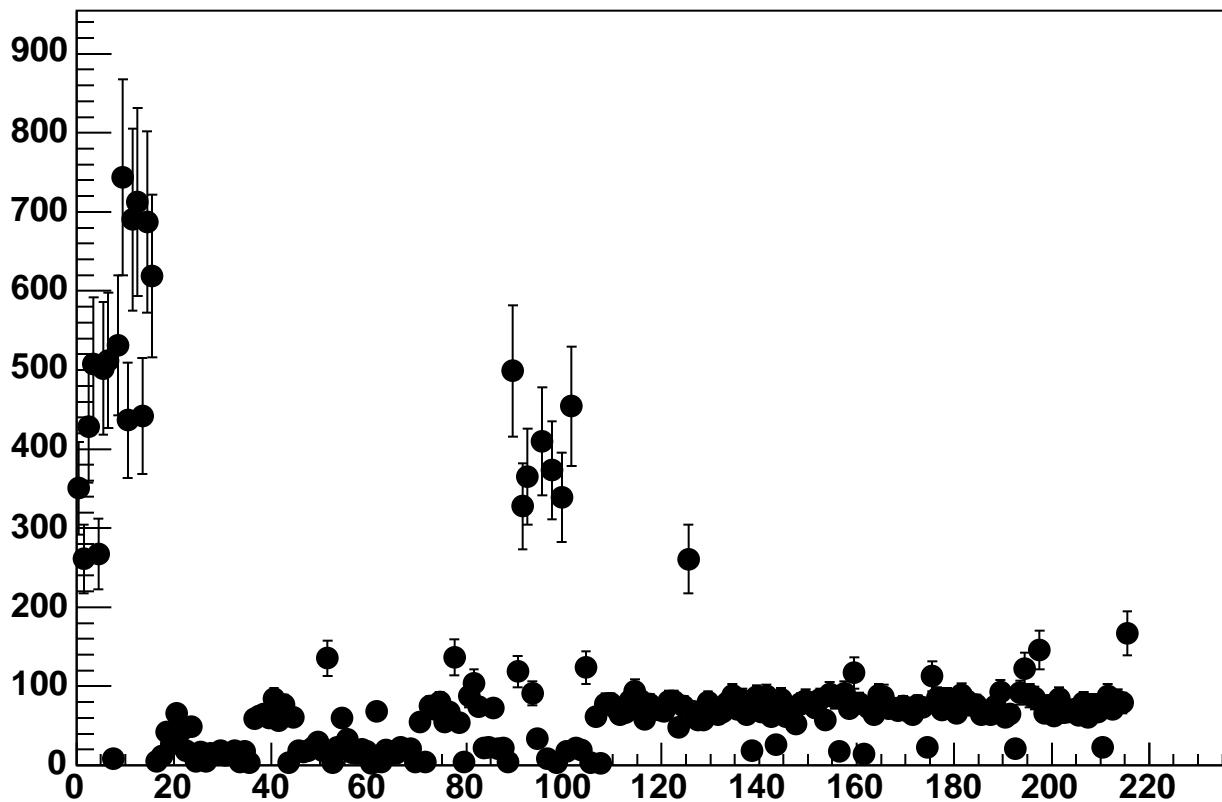
Enable 5, DAC=1600, Hold=55, ADC Noise vs 18\*Chip+Chan



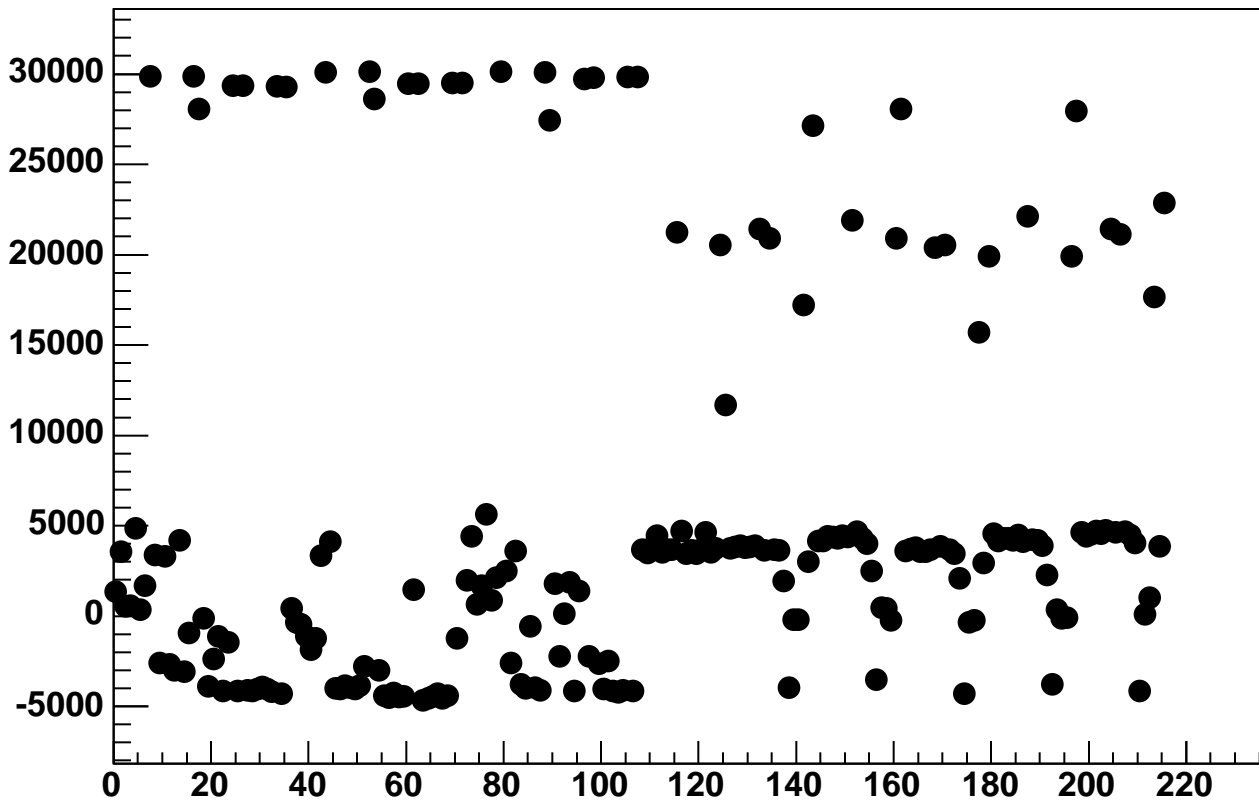
Enable 5, DAC=1600, Hold=60, ADC Mean vs 18\*Chip+Chan



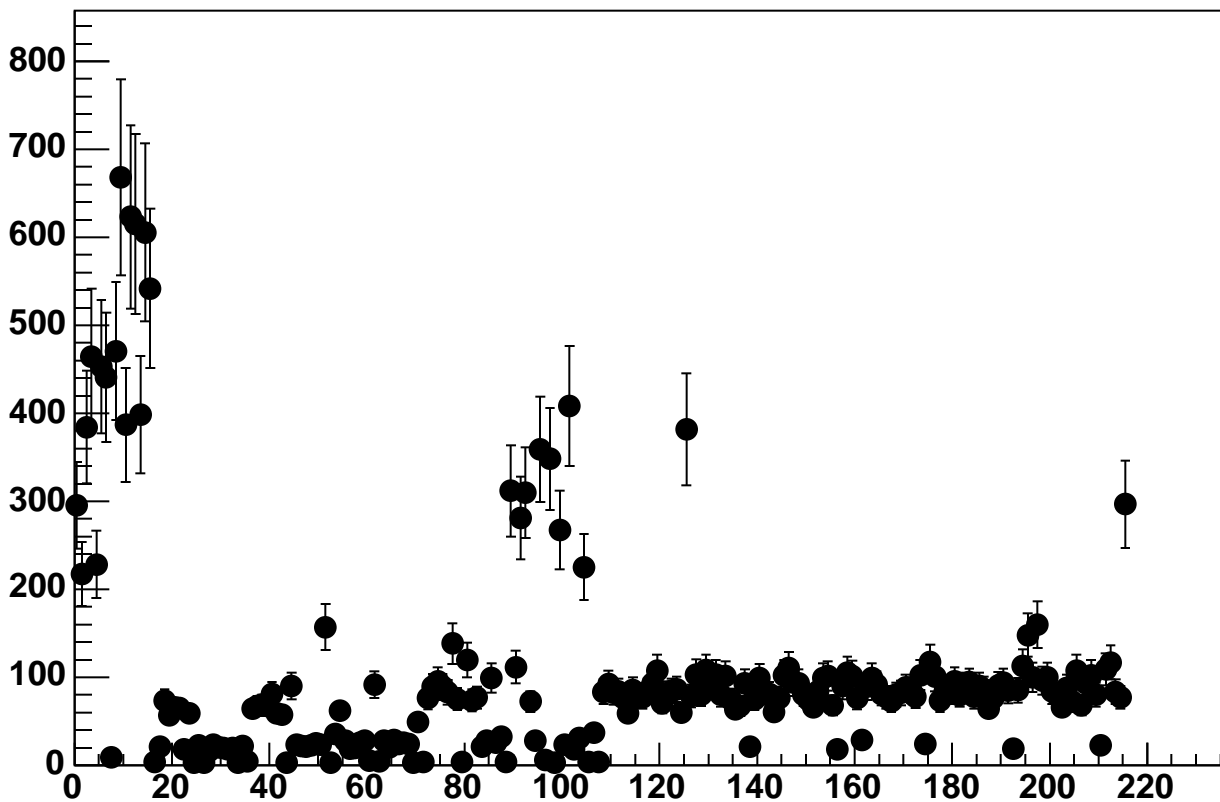
Enable 5, DAC=1600, Hold=60, ADC Noise vs 18\*Chip+Chan



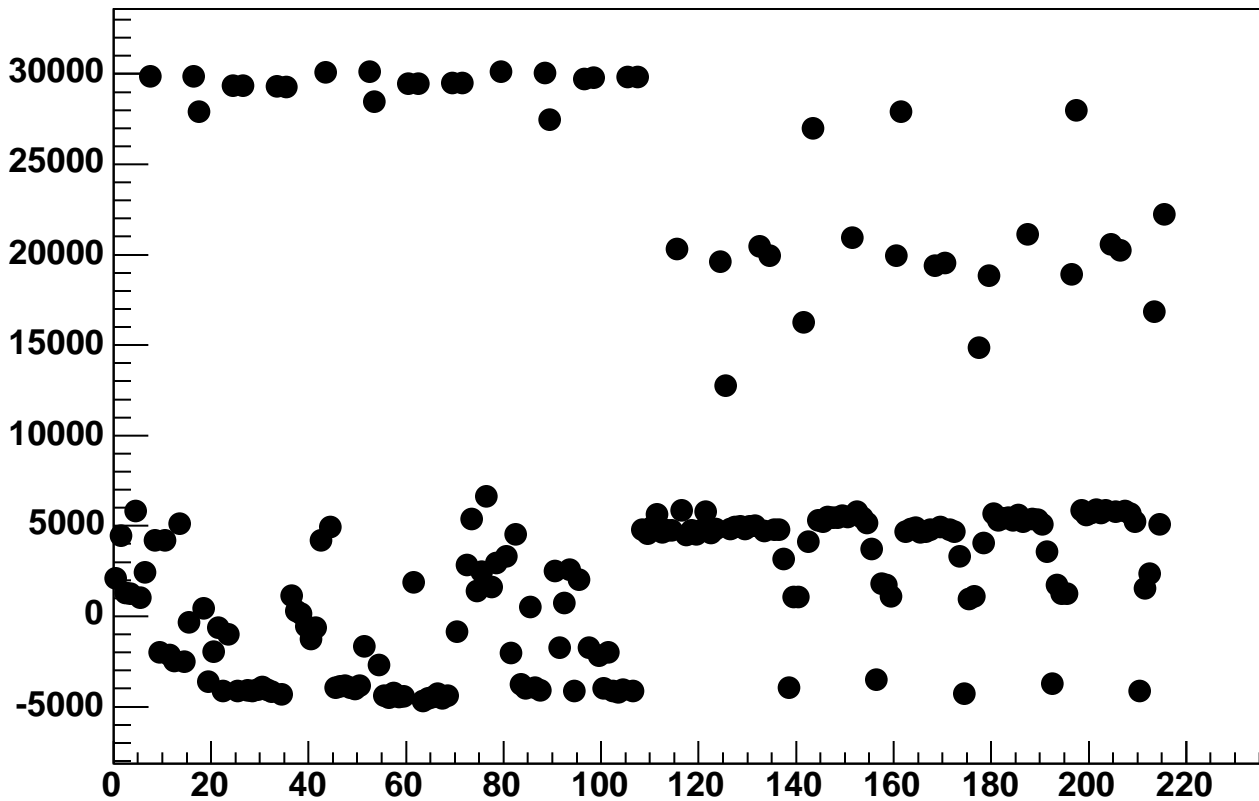
Enable 5, DAC=1600, Hold=65, ADC Mean vs 18\*Chip+Chan



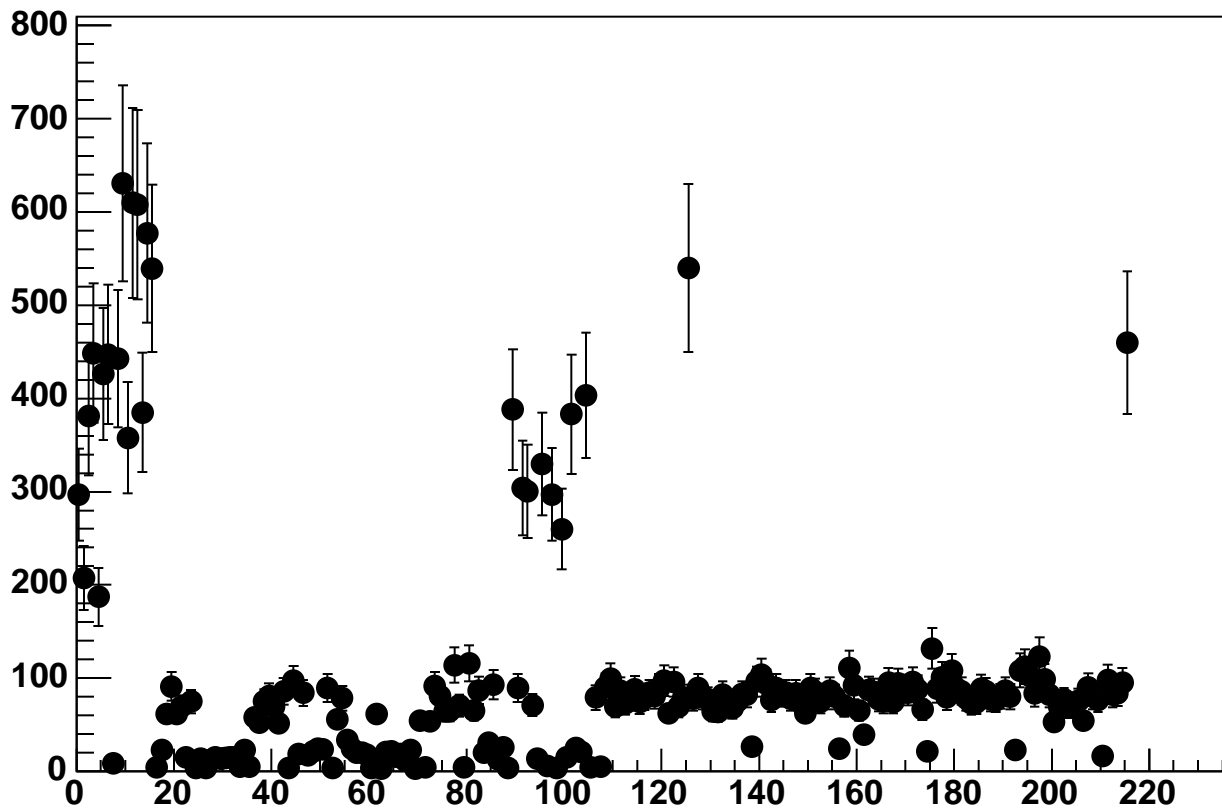
Enable 5, DAC=1600, Hold=65, ADC Noise vs 18\*Chip+Chan



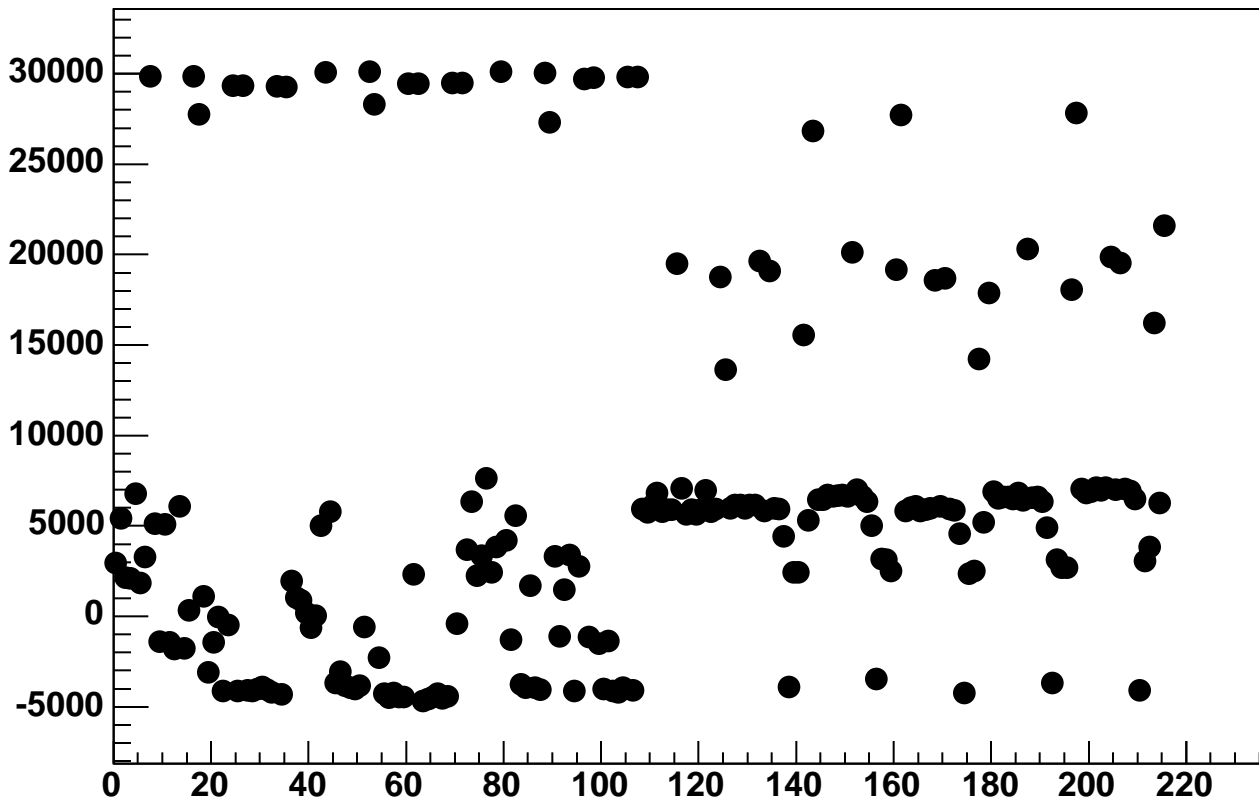
Enable 5, DAC=1600, Hold=70, ADC Mean vs 18\*Chip+Chan



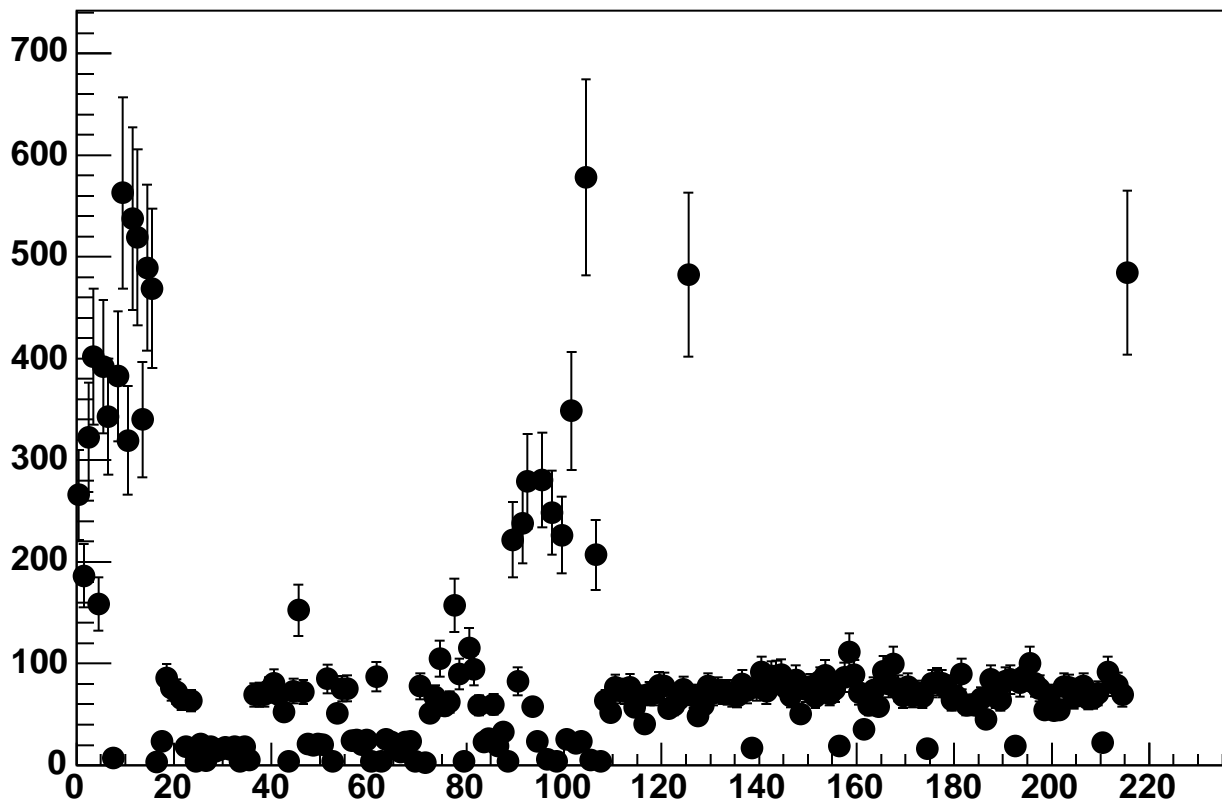
Enable 5, DAC=1600, Hold=70, ADC Noise vs 18\*Chip+Chan



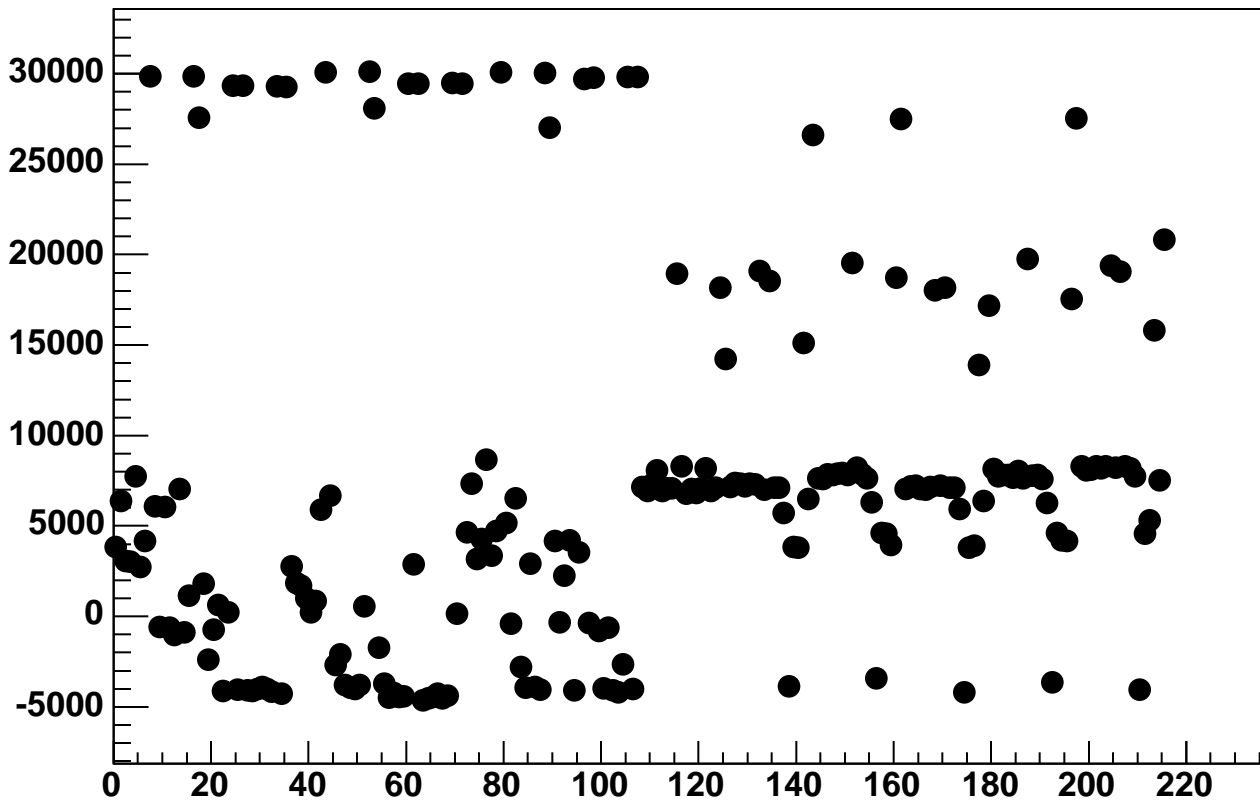
Enable 5, DAC=1600, Hold=75, ADC Mean vs 18\*Chip+Chan



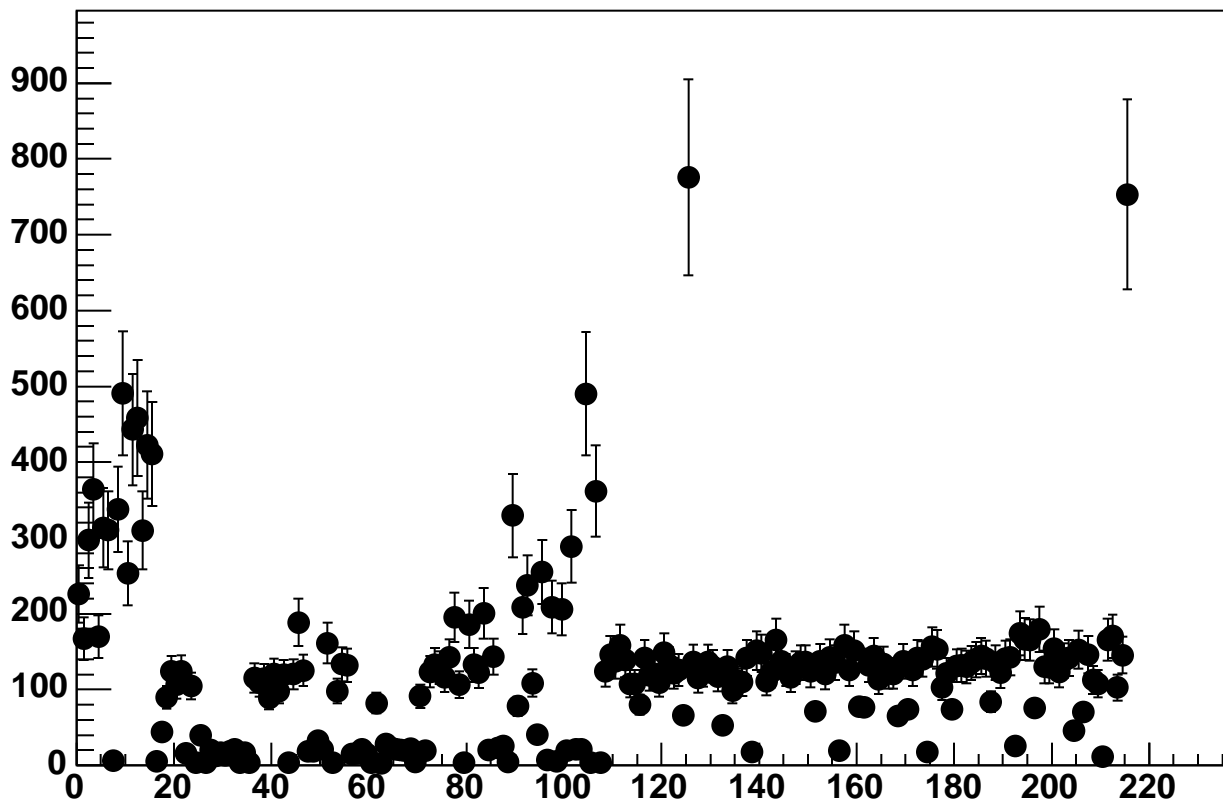
Enable 5, DAC=1600, Hold=75, ADC Noise vs 18\*Chip+Chan



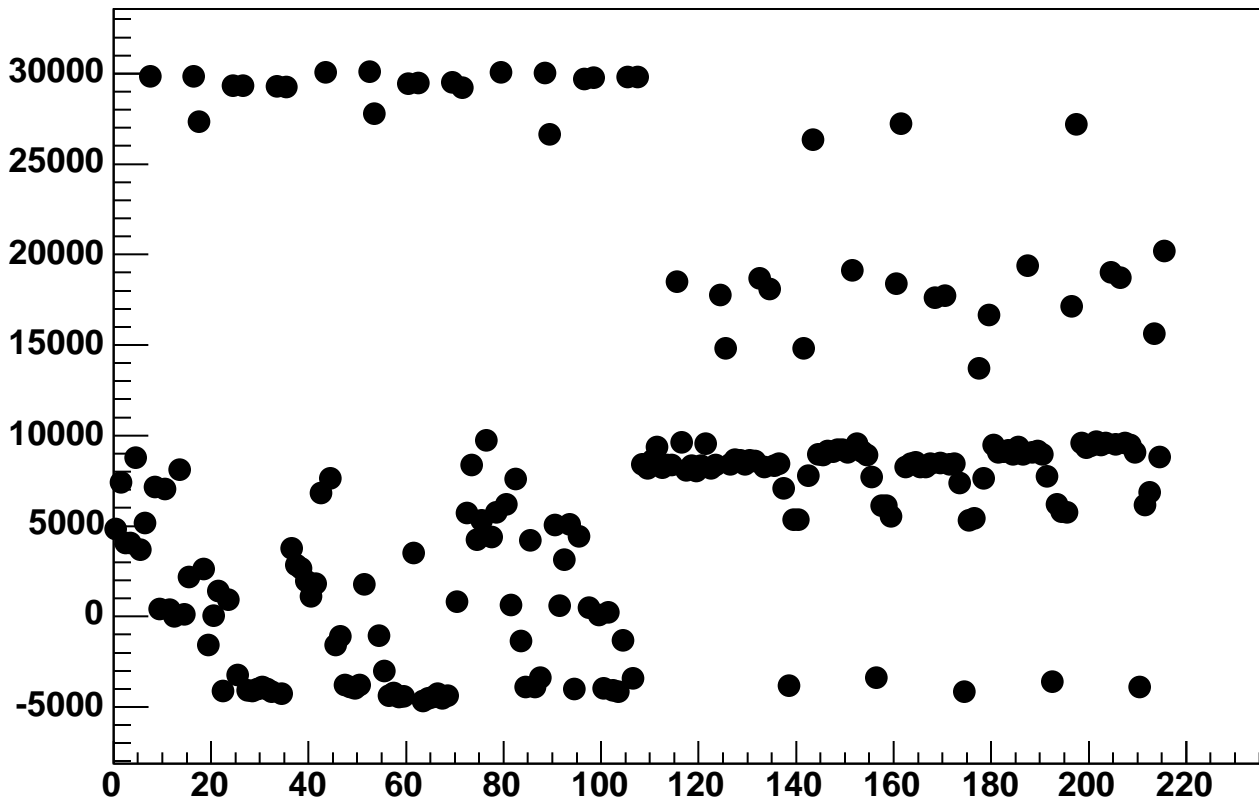
Enable 5, DAC=1600, Hold=80, ADC Mean vs 18\*Chip+Chan



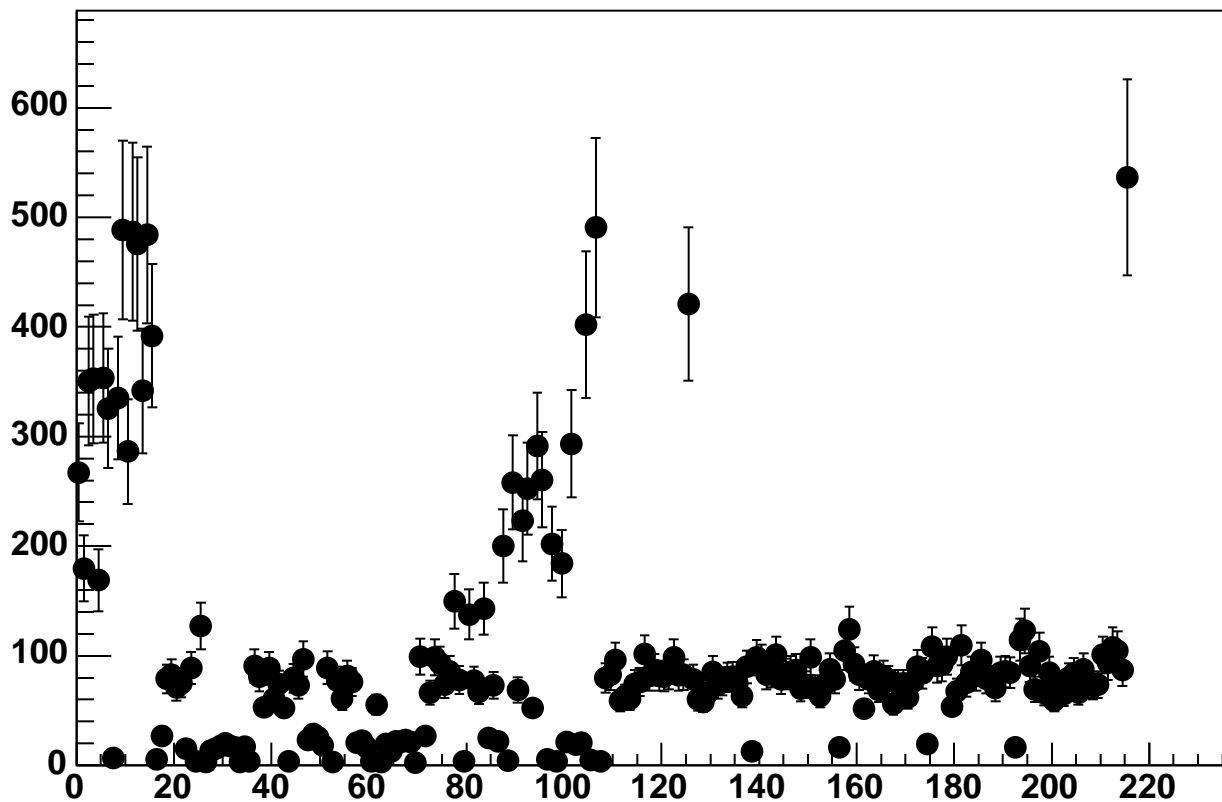
Enable 5, DAC=1600, Hold=80, ADC Noise vs 18\*Chip+Chan



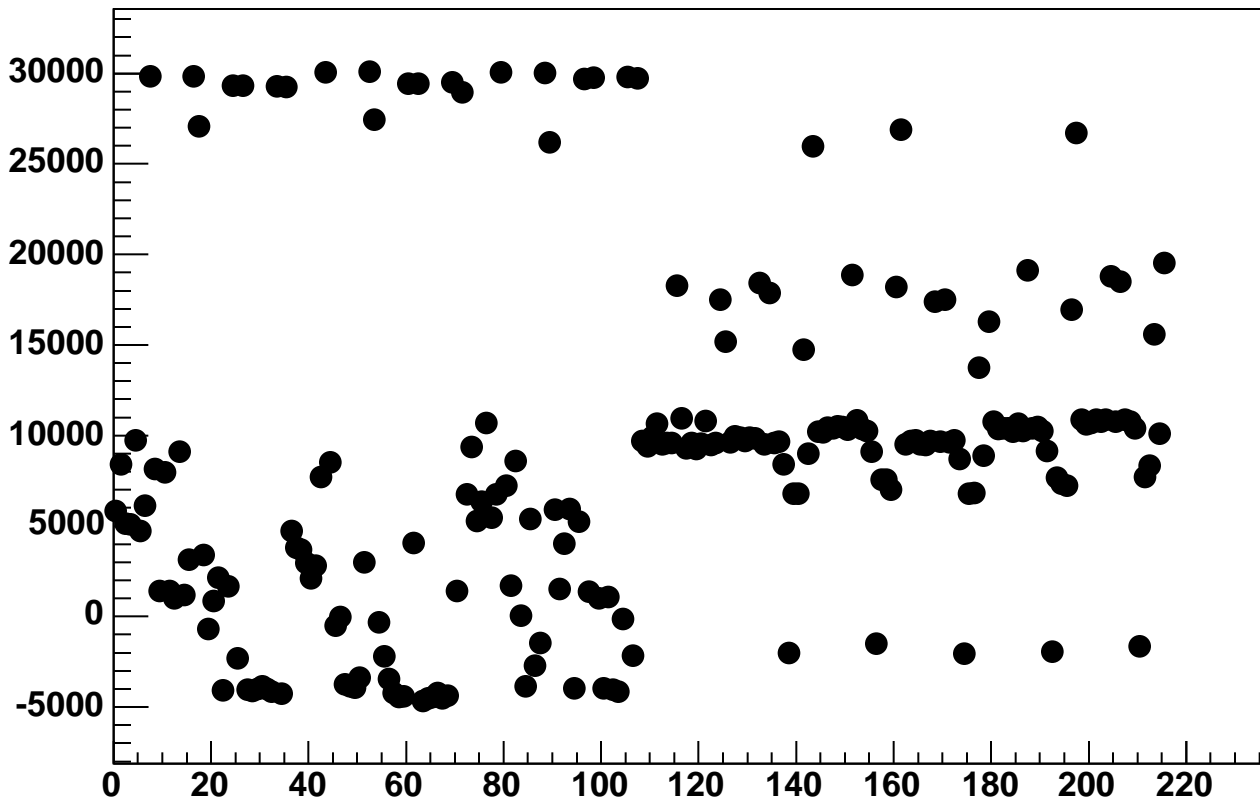
Enable 5, DAC=1600, Hold=85, ADC Mean vs 18\*Chip+Chan



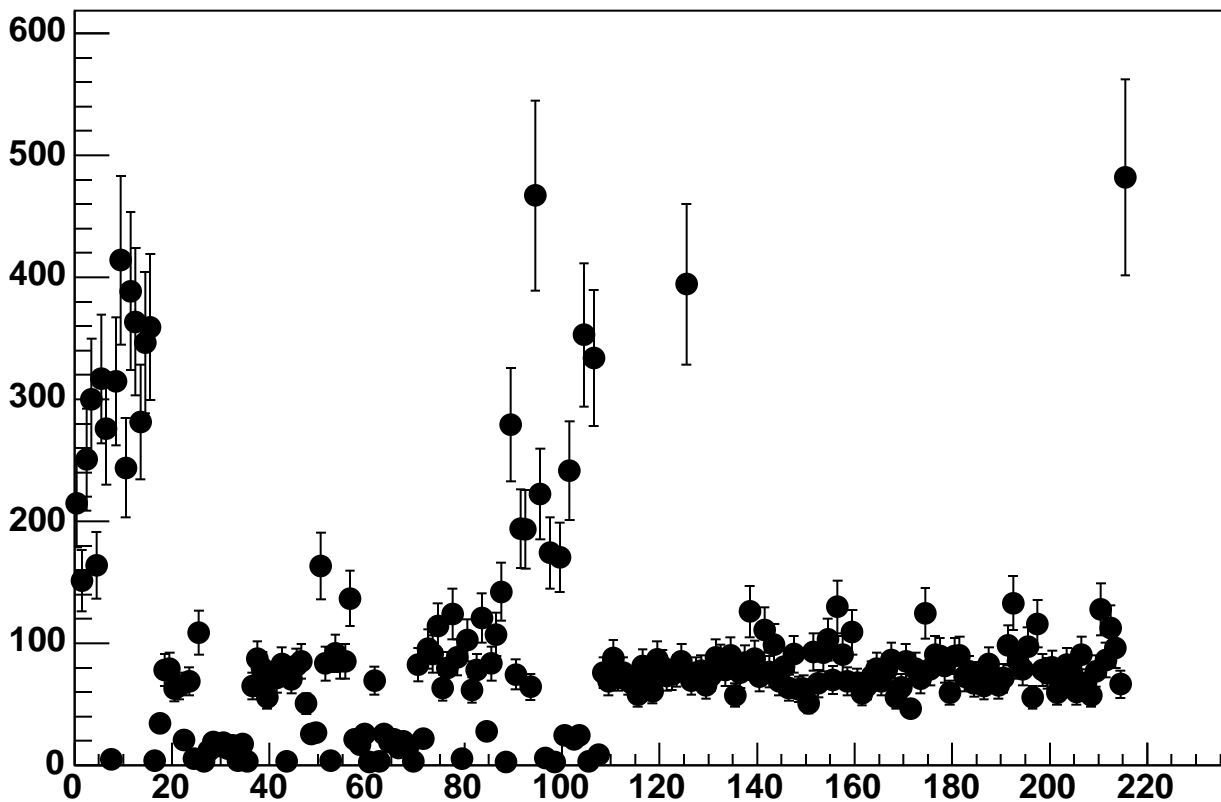
Enable 5, DAC=1600, Hold=85, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=90, ADC Mean vs 18\*Chip+Chan

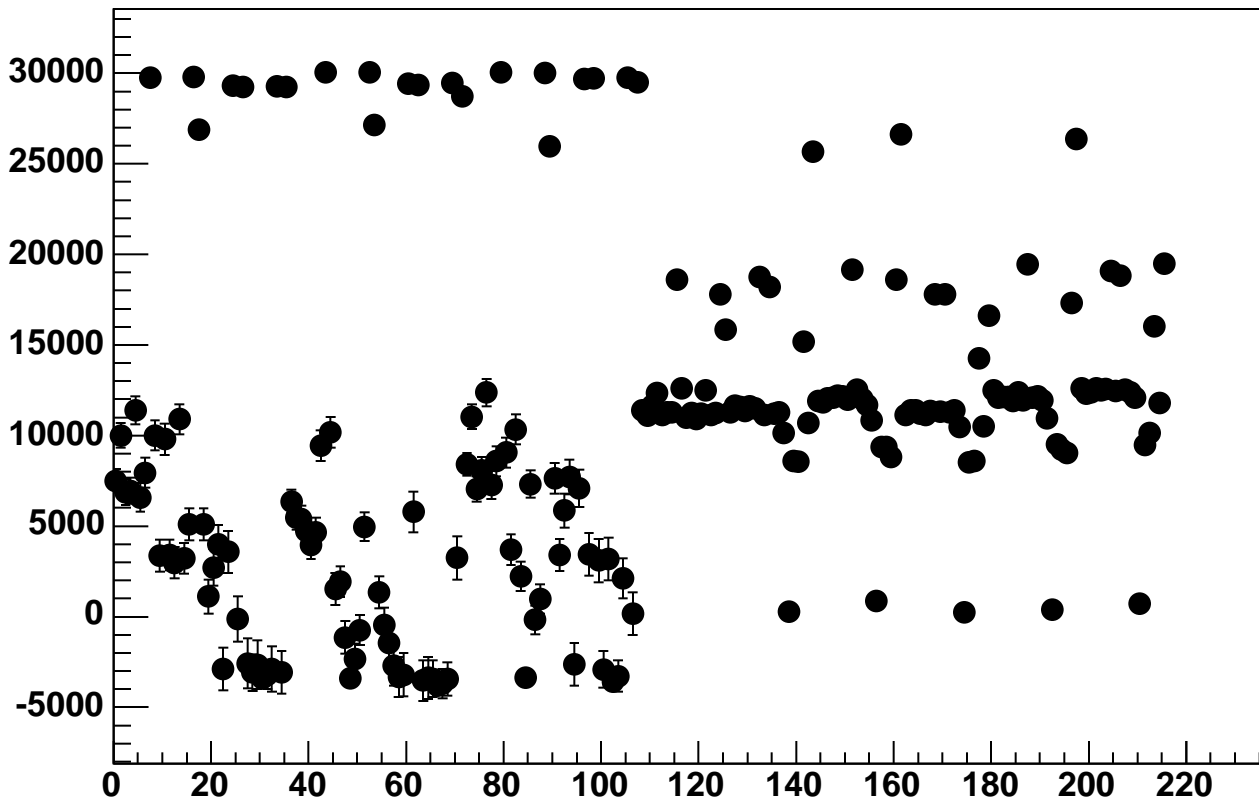


Enable 5, DAC=1600, Hold=90, ADC Noise vs 18\*Chip+Chan

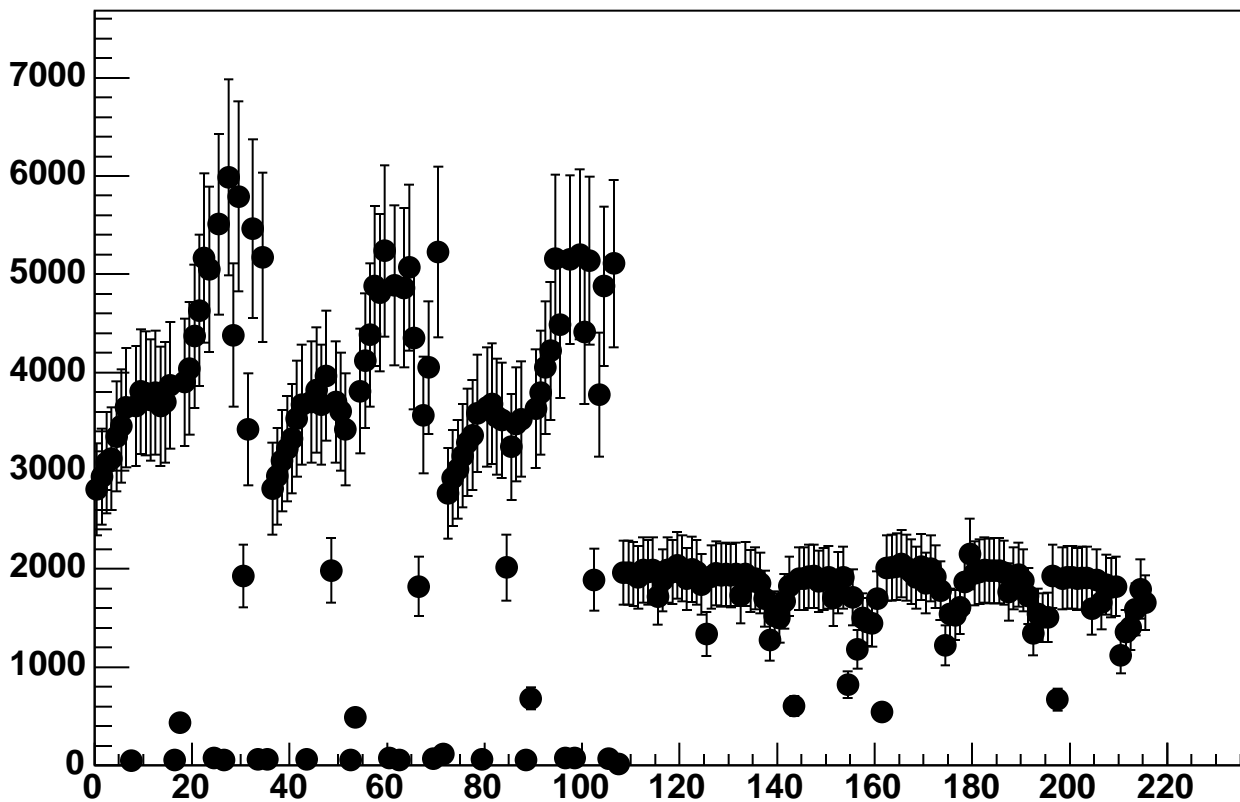




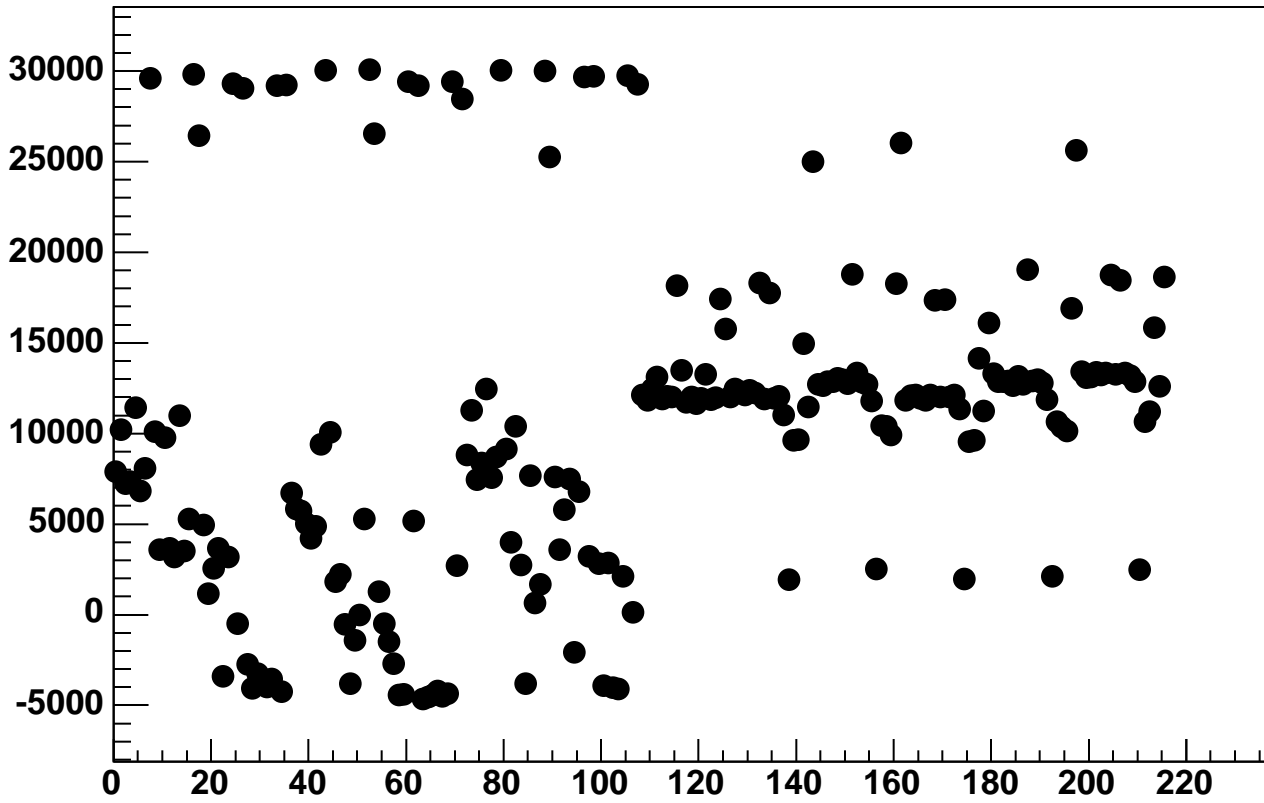
Enable 5, DAC=1600, Hold=95, ADC Mean vs 18\*Chip+Chan



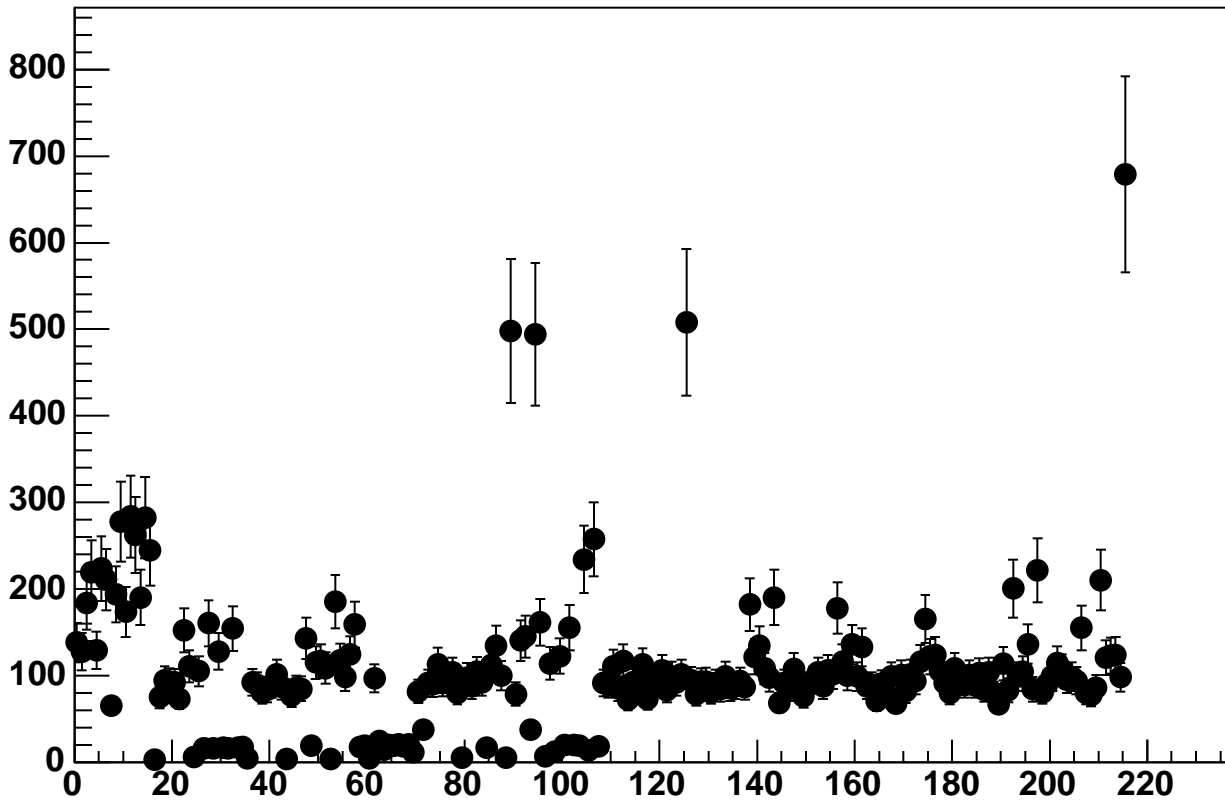
Enable 5, DAC=1600, Hold=95, ADC Noise vs 18\*Chip+Chan



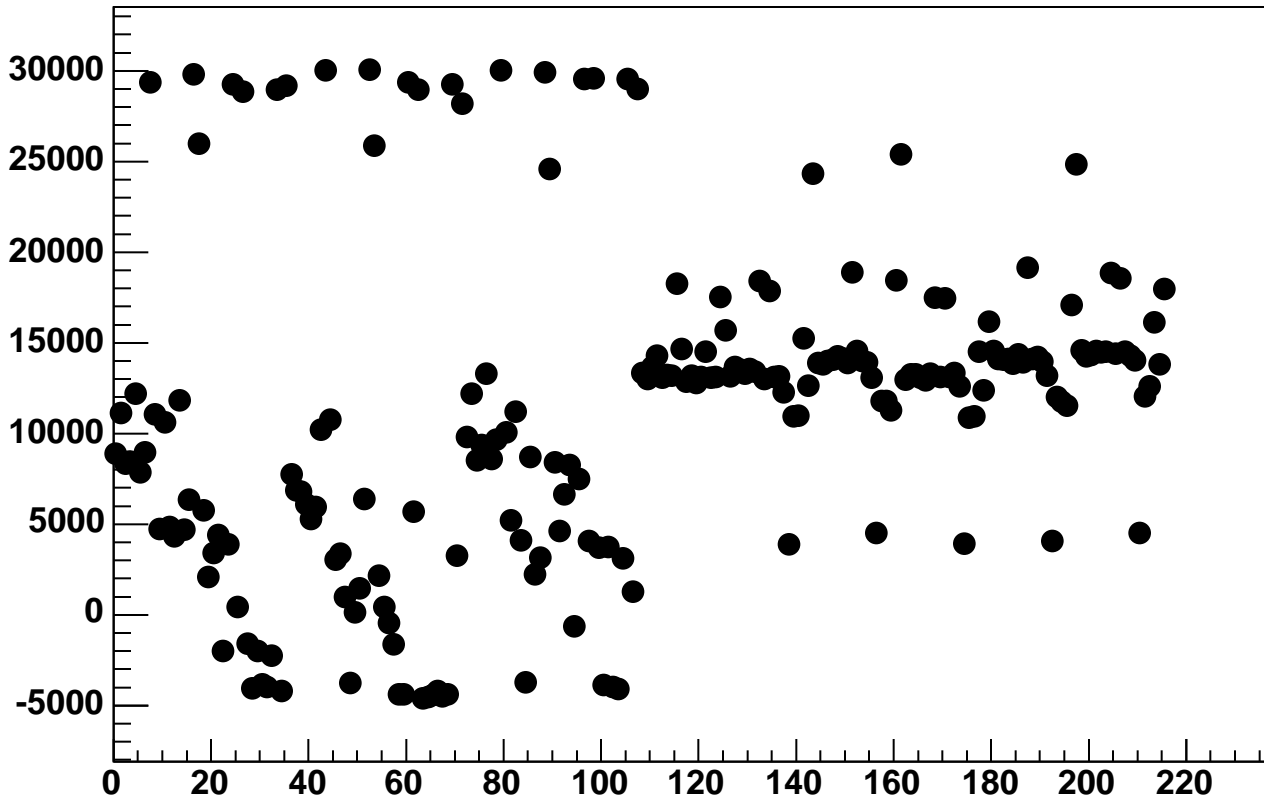
Enable 5, DAC=1600, Hold=100, ADC Mean vs 18\*Chip+Chan



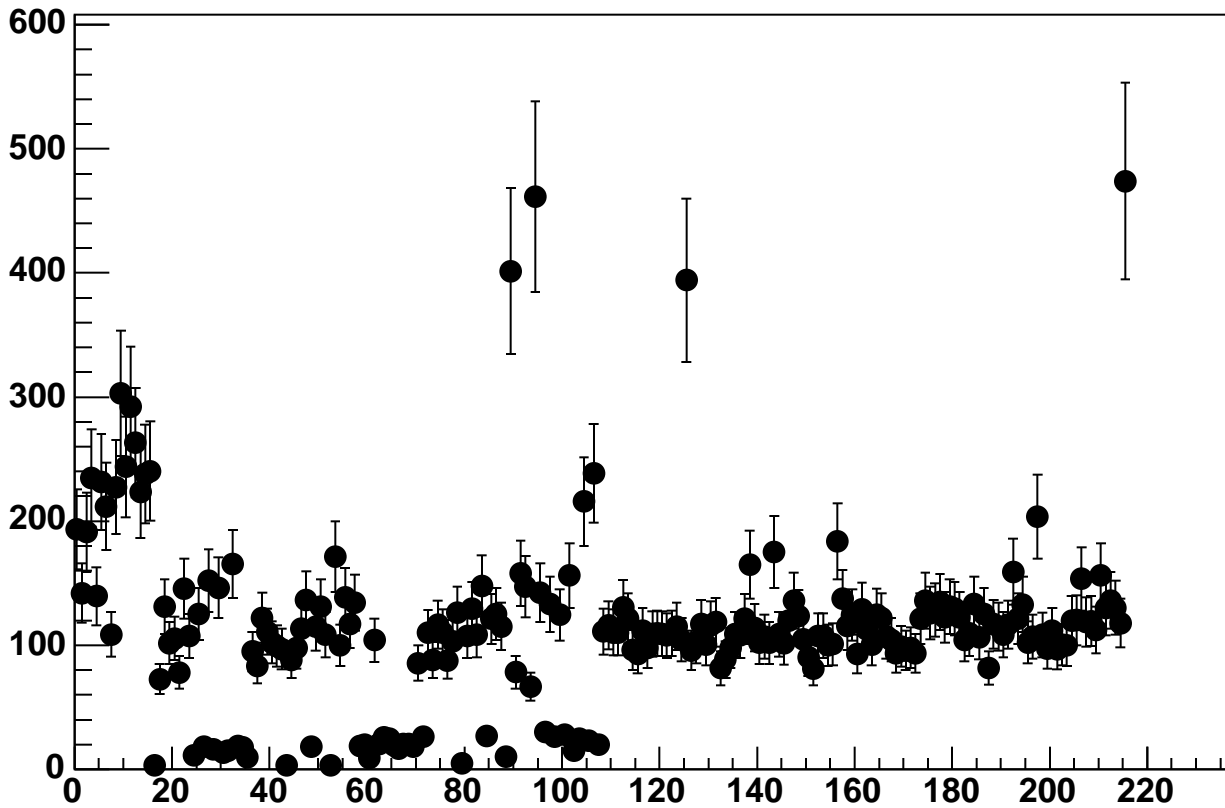
Enable 5, DAC=1600, Hold=100, ADC Noise vs 18\*Chip+Chan



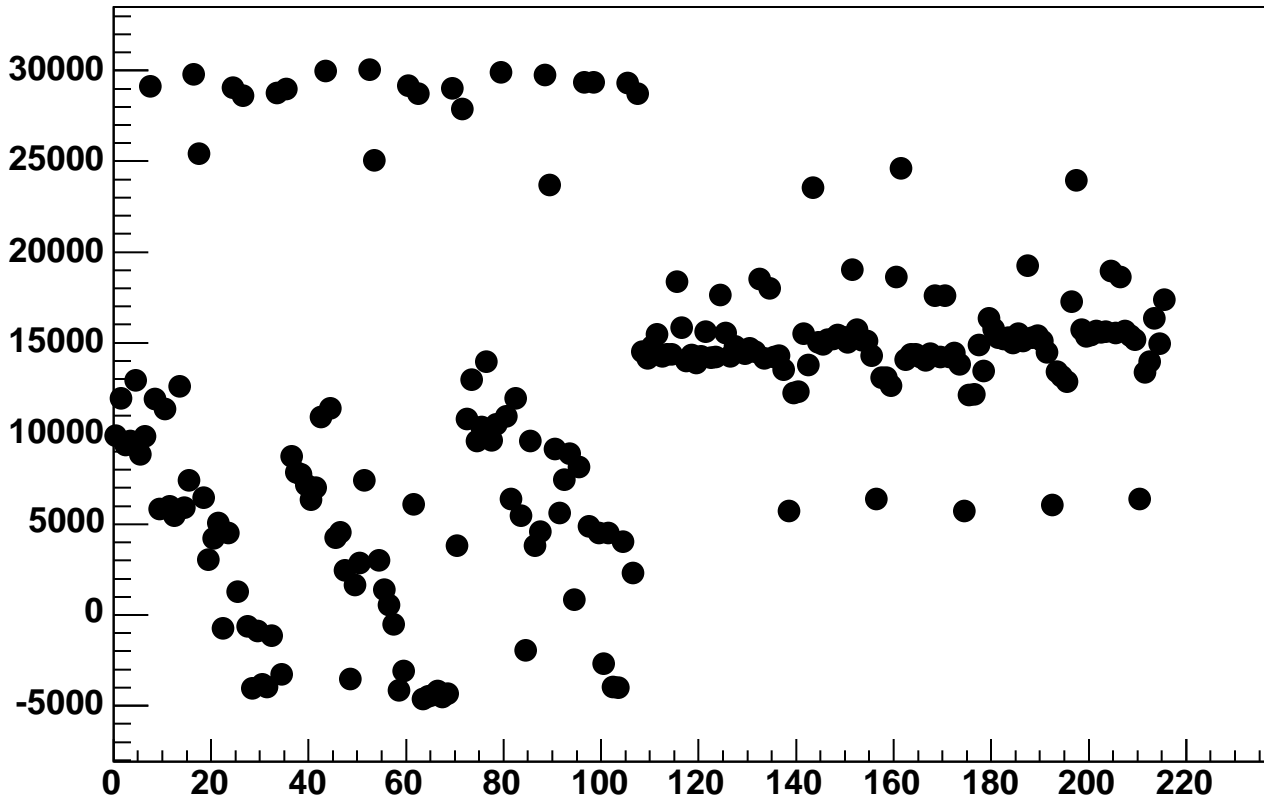
Enable 5, DAC=1600, Hold=105, ADC Mean vs 18\*Chip+Chan



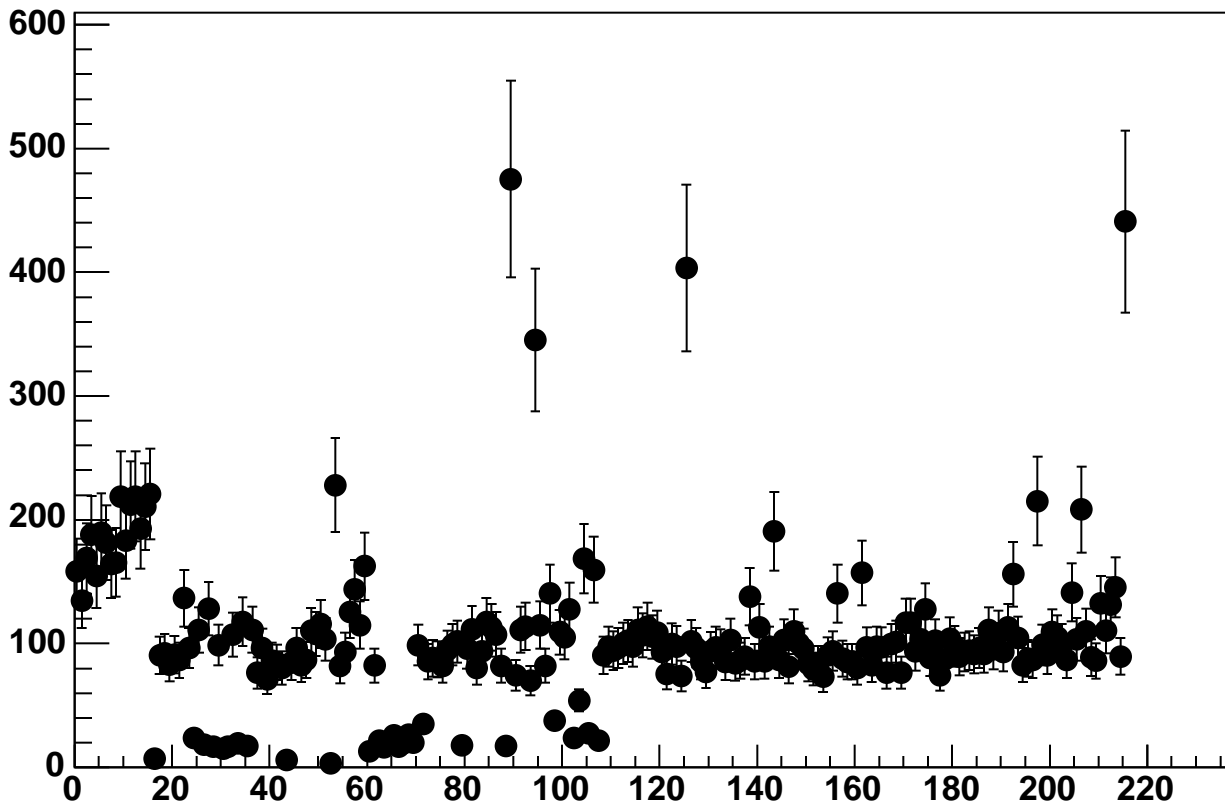
Enable 5, DAC=1600, Hold=105, ADC Noise vs 18\*Chip+Chan



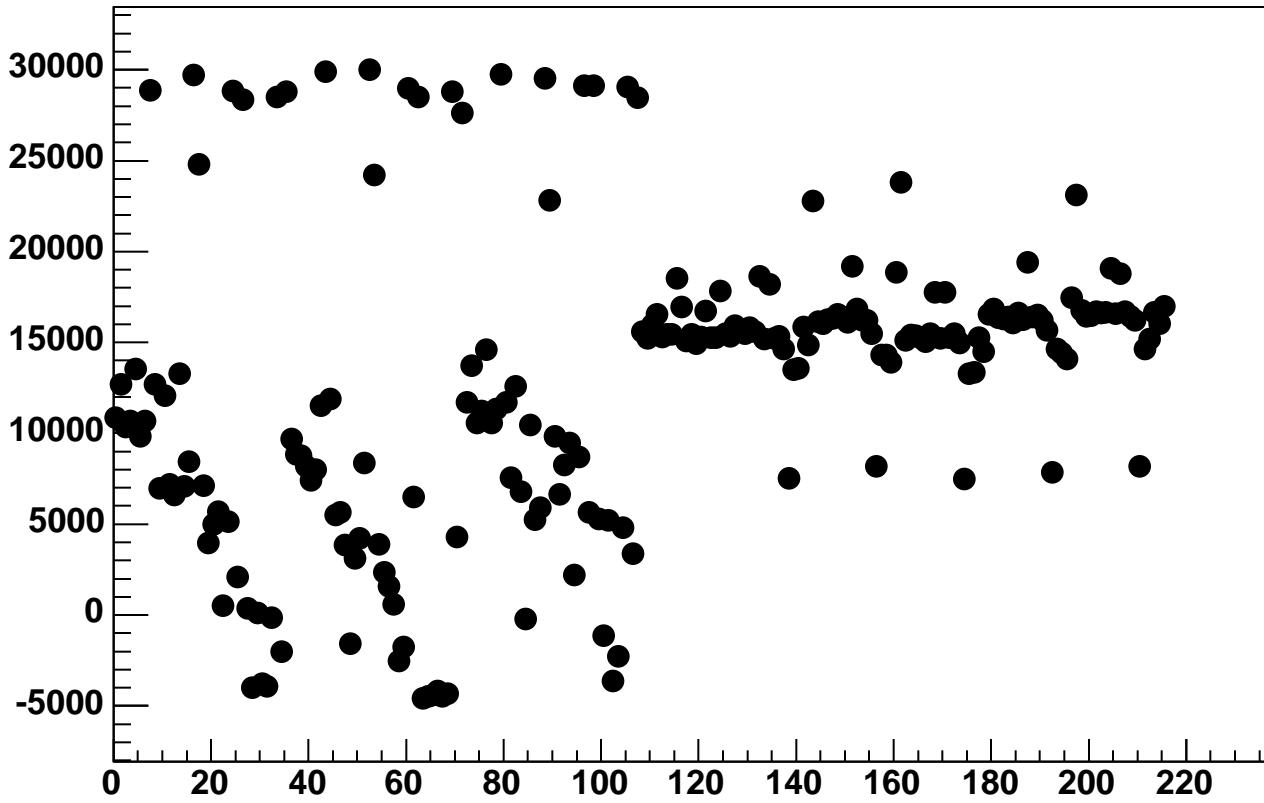
Enable 5, DAC=1600, Hold=110, ADC Mean vs 18\*Chip+Chan



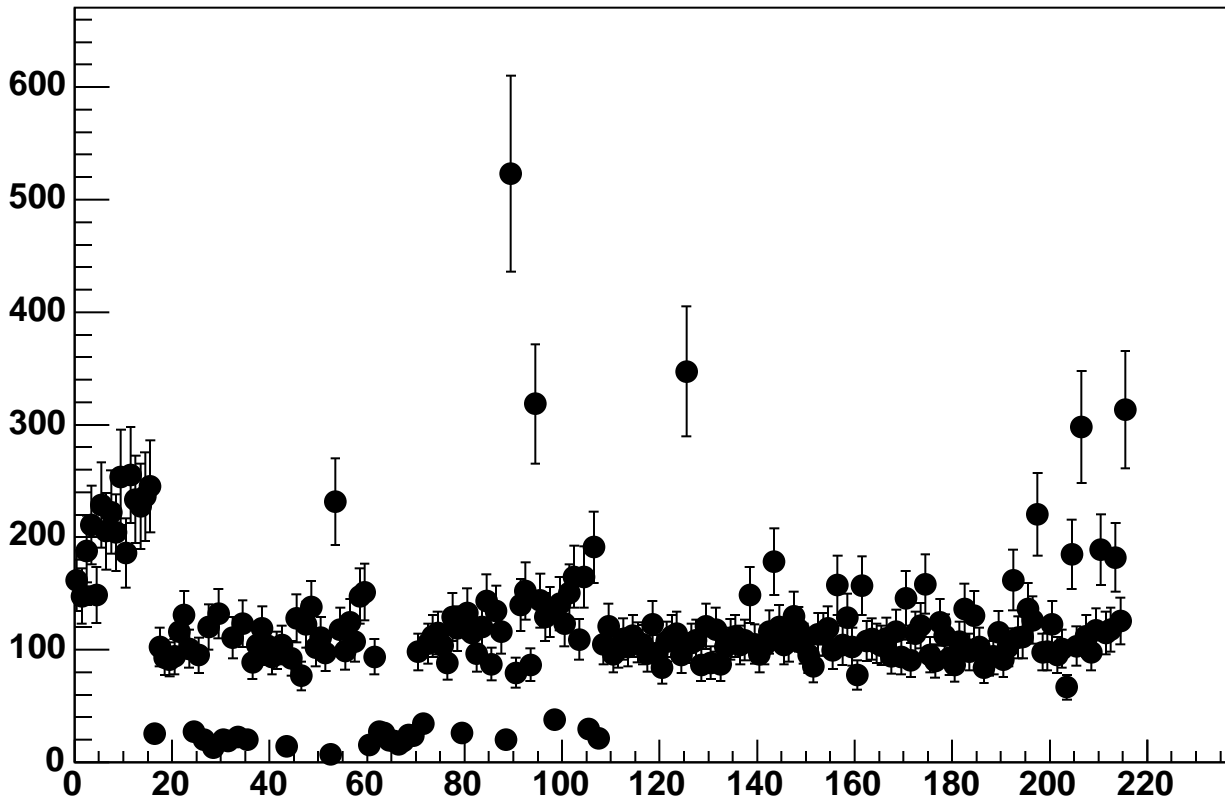
Enable 5, DAC=1600, Hold=110, ADC Noise vs 18\*Chip+Chan



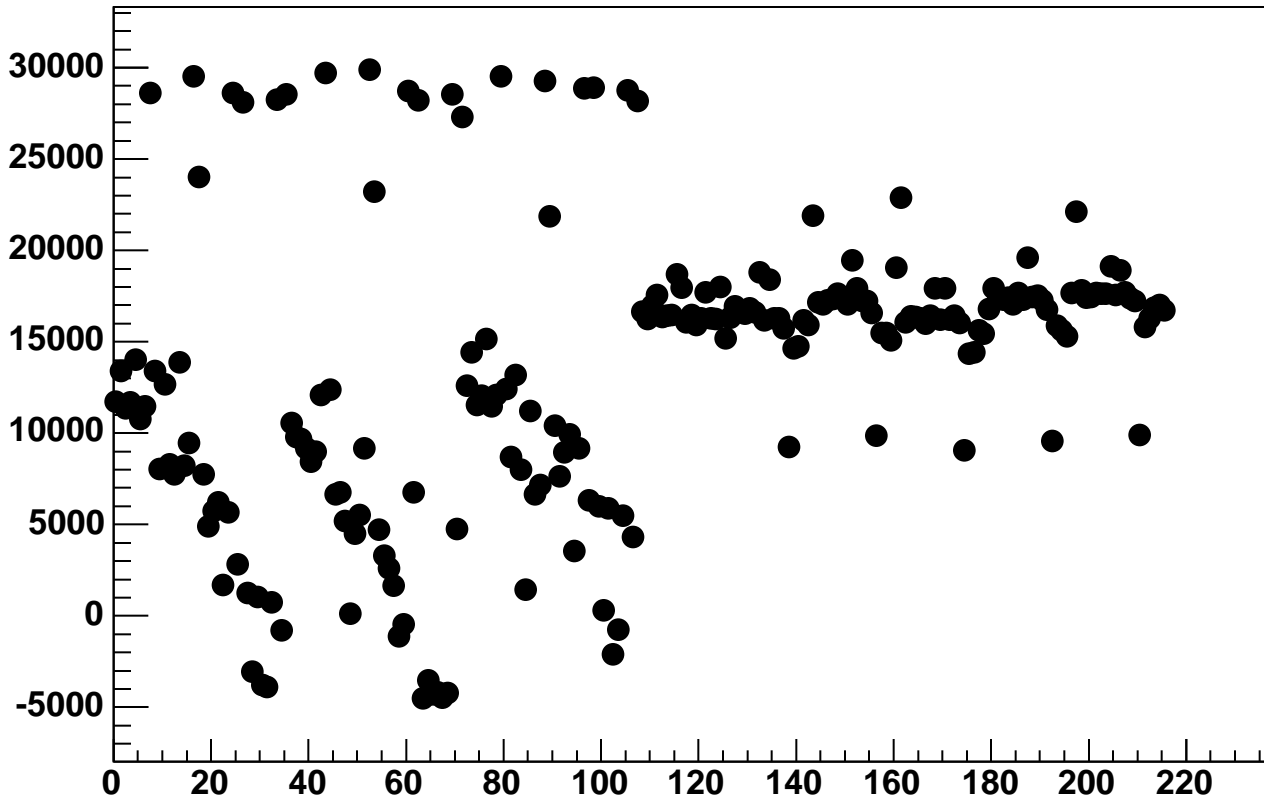
Enable 5, DAC=1600, Hold=115, ADC Mean vs 18\*Chip+Chan



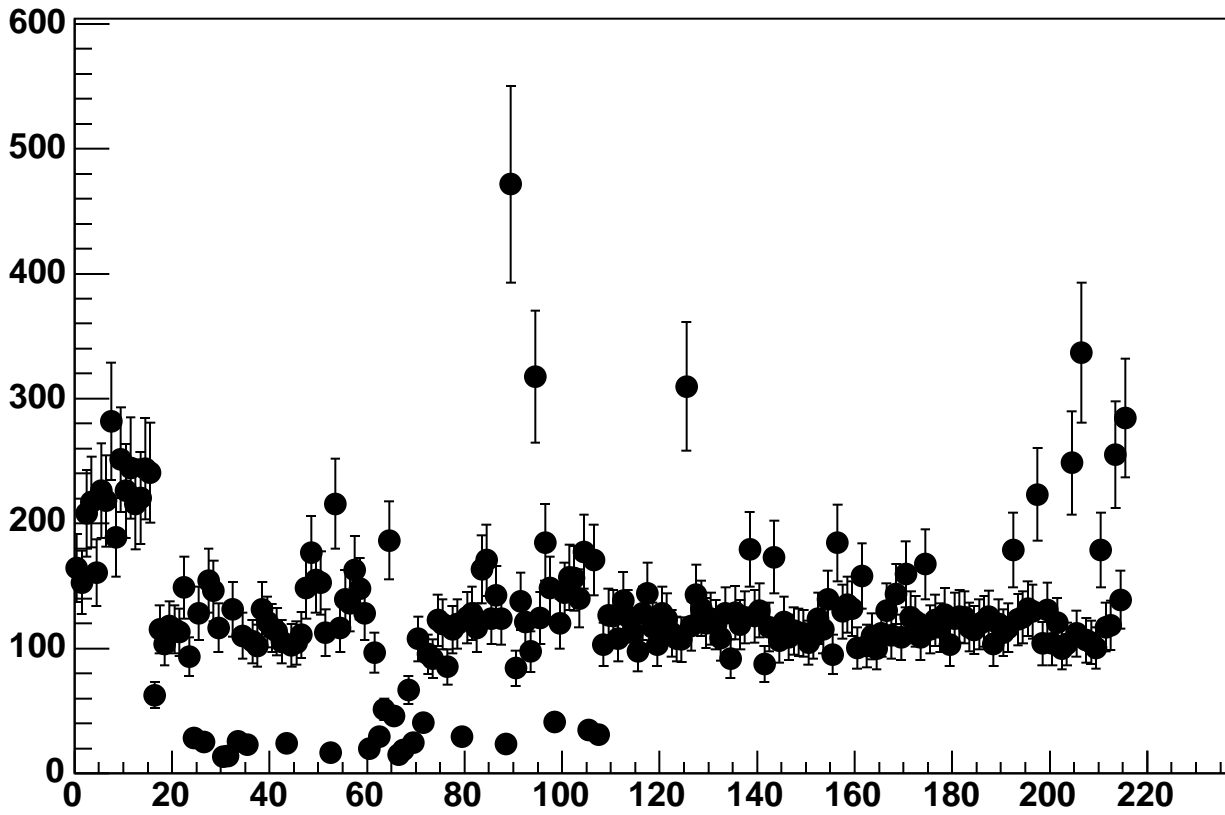
Enable 5, DAC=1600, Hold=115, ADC Noise vs 18\*Chip+Chan



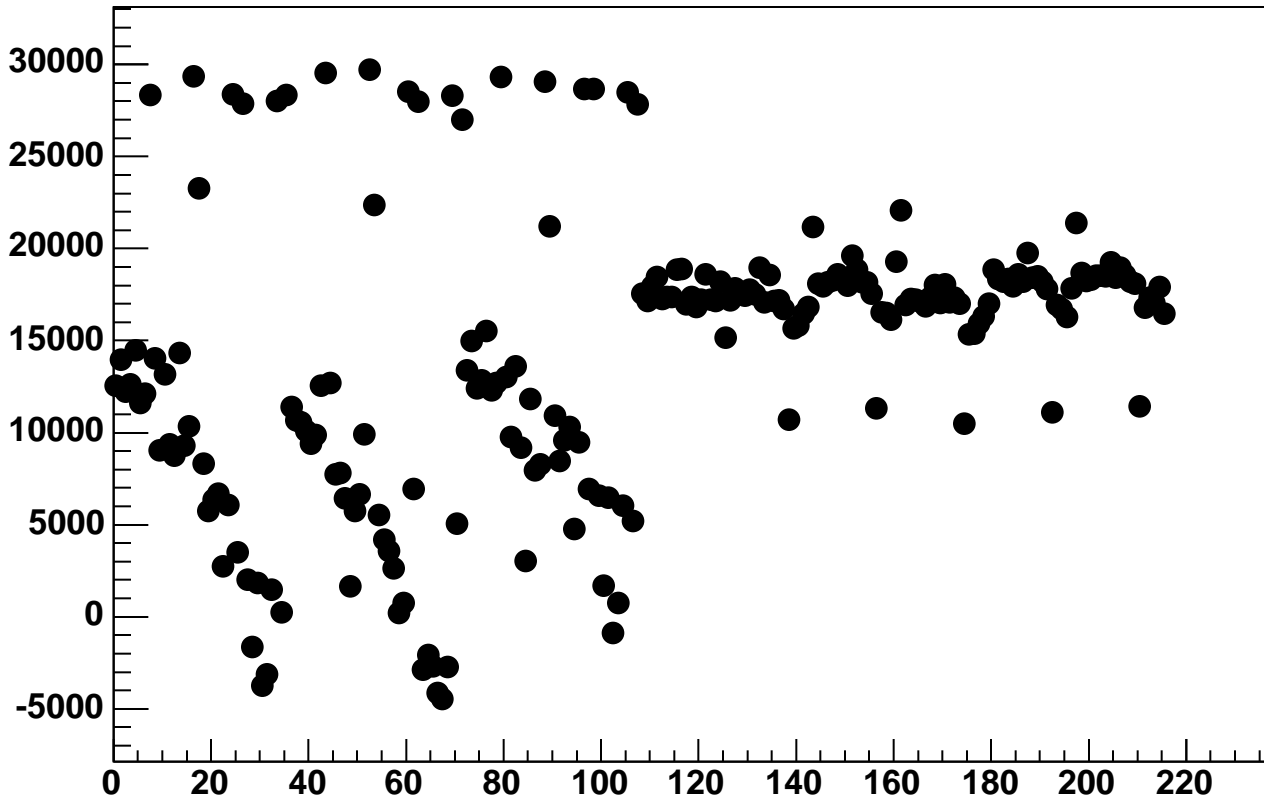
Enable 5, DAC=1600, Hold=120, ADC Mean vs 18\*Chip+Chan



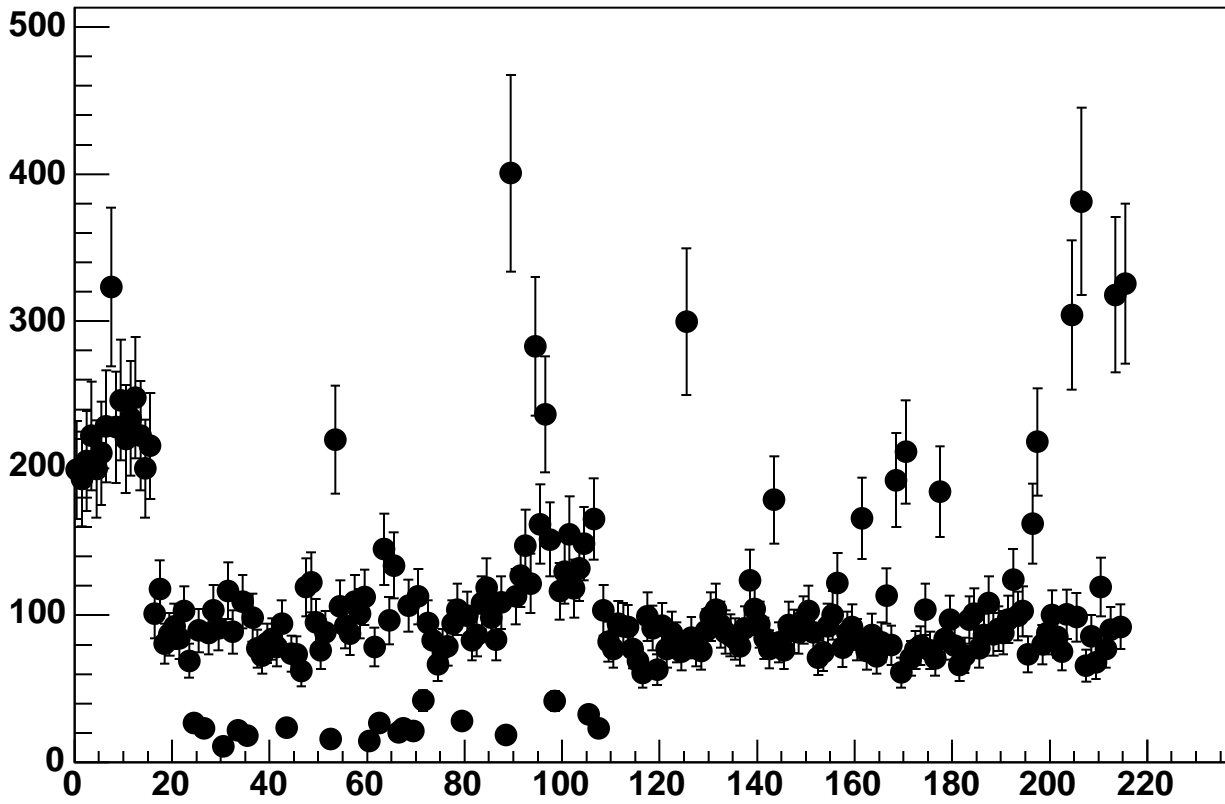
Enable 5, DAC=1600, Hold=120, ADC Noise vs 18\*Chip+Chan



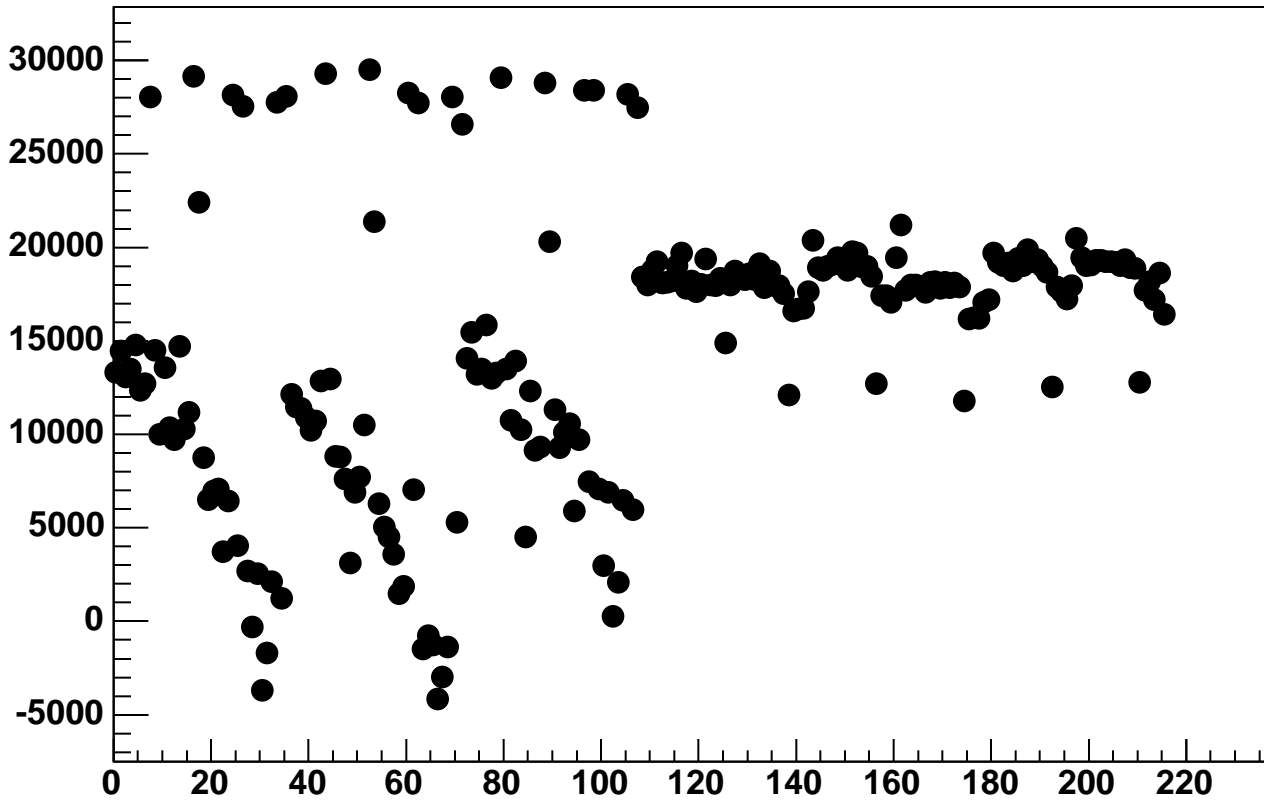
Enable 5, DAC=1600, Hold=125, ADC Mean vs 18\*Chip+Chan



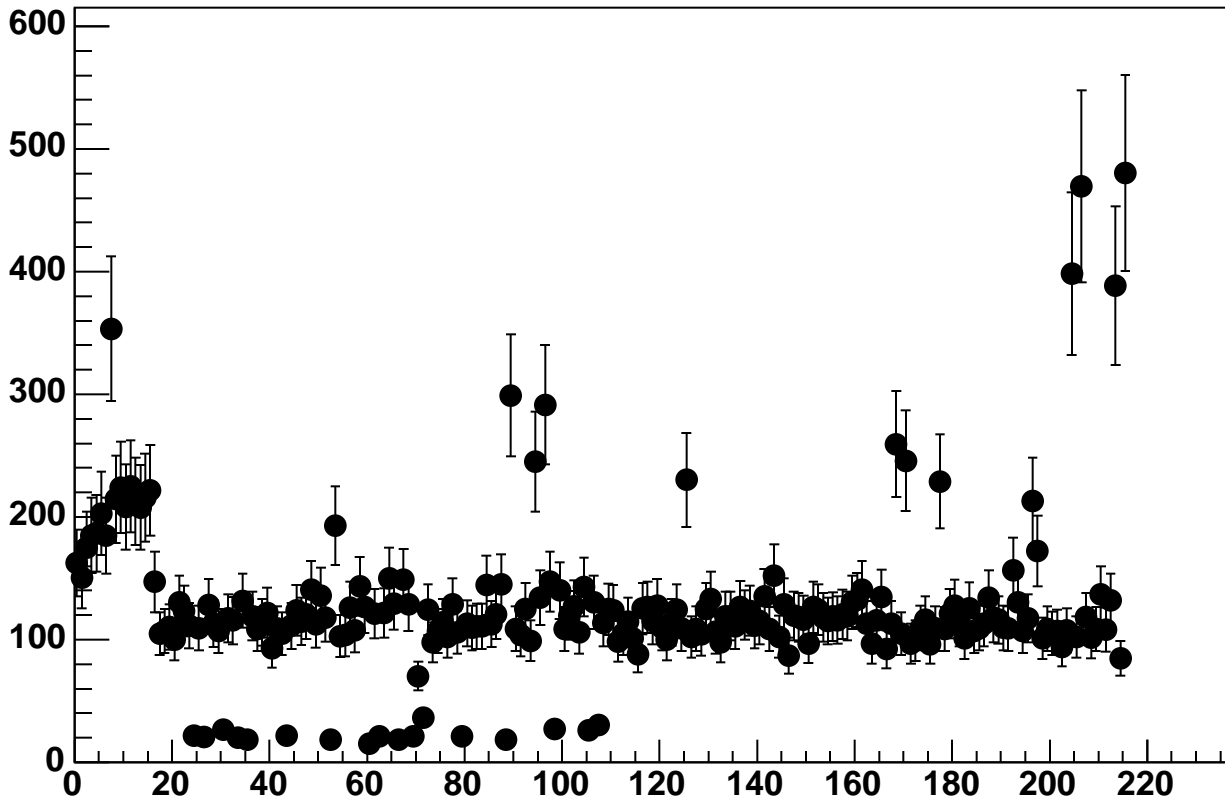
Enable 5, DAC=1600, Hold=125, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=130, ADC Mean vs 18\*Chip+Chan

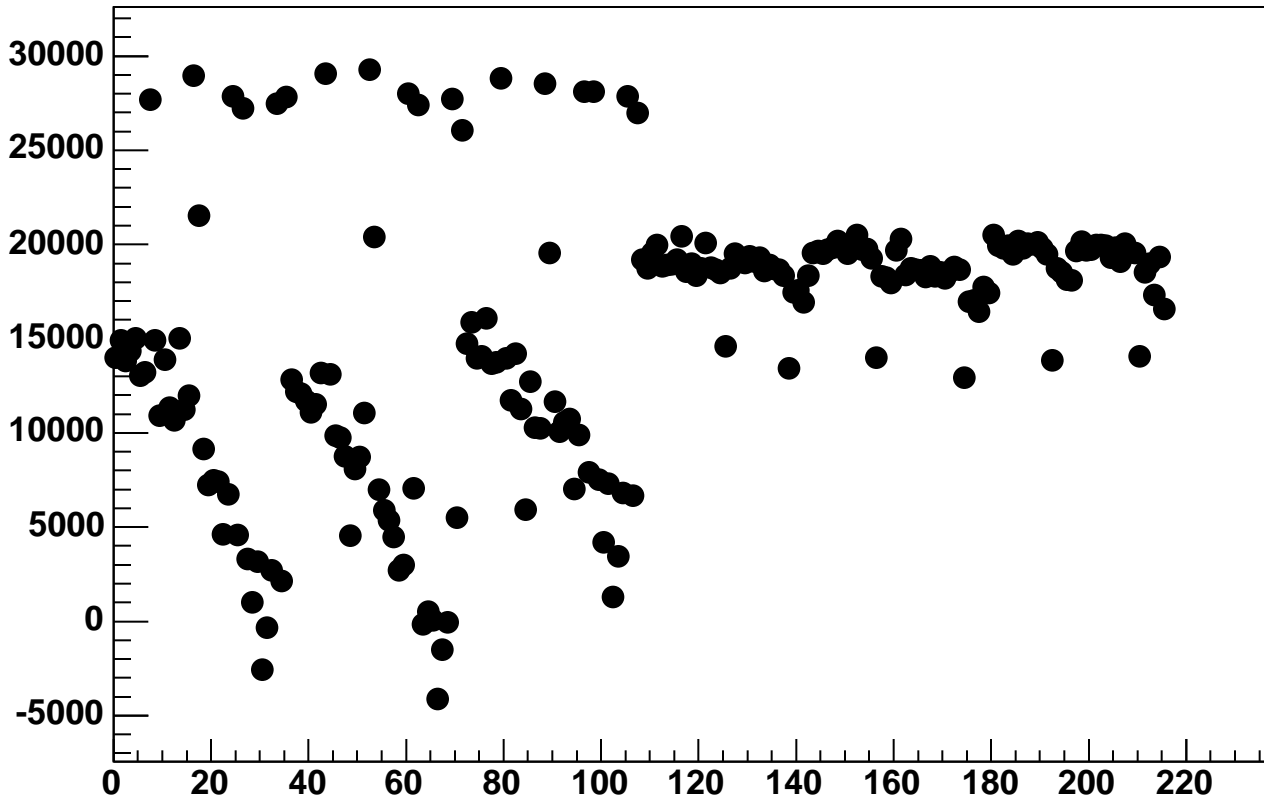


Enable 5, DAC=1600, Hold=130, ADC Noise vs 18\*Chip+Chan

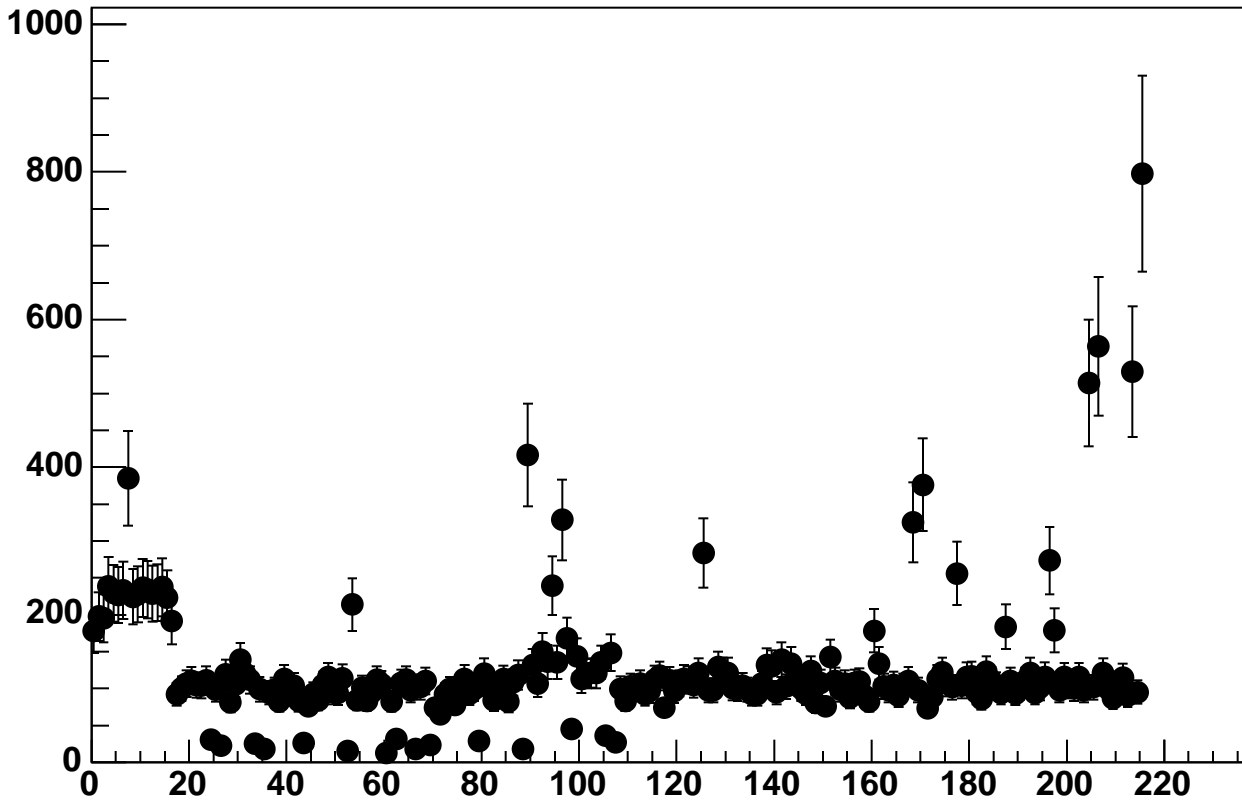




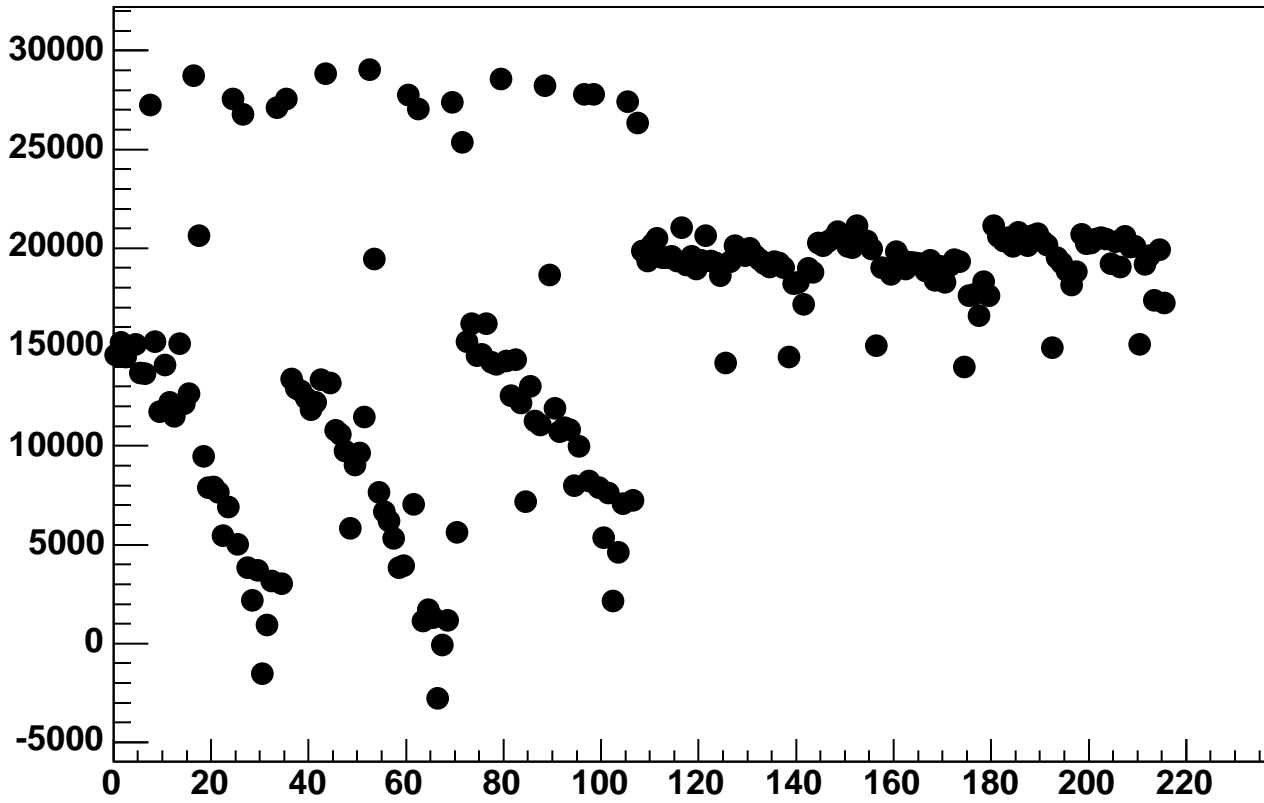
Enable 5, DAC=1600, Hold=135, ADC Mean vs 18\*Chip+Chan



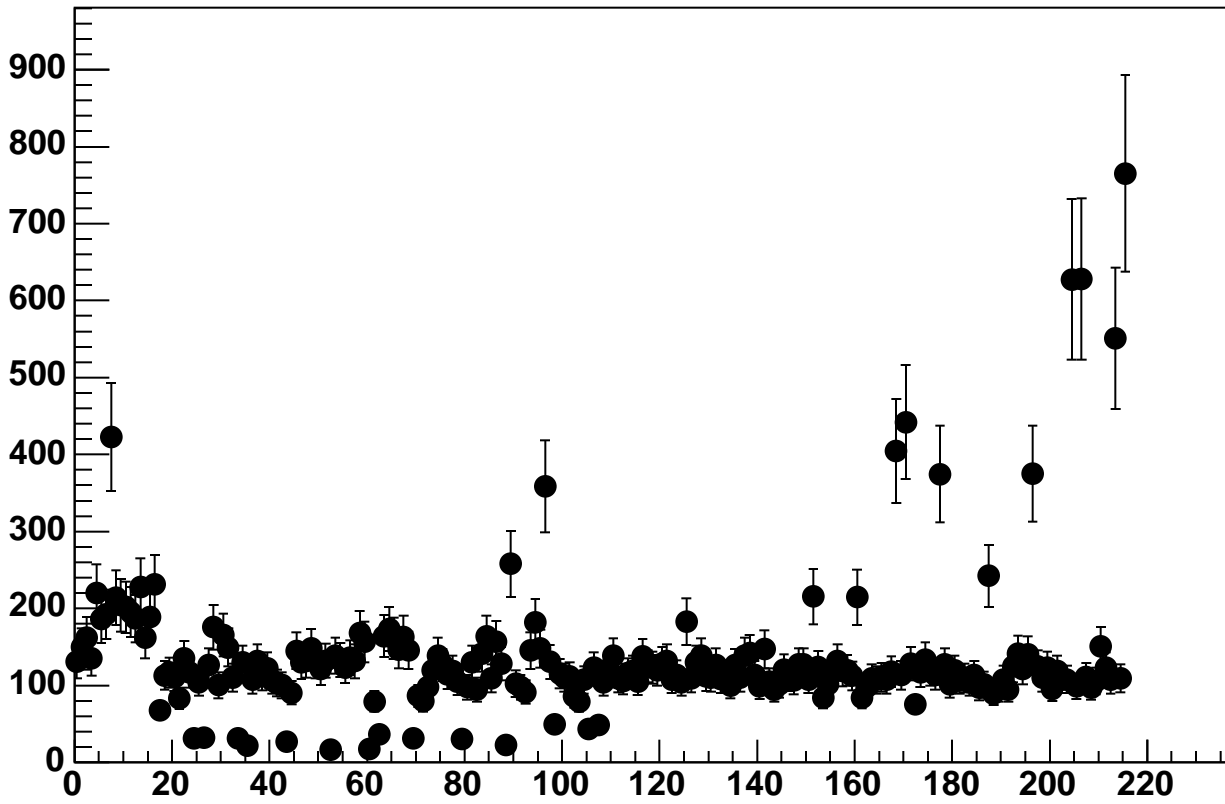
Enable 5, DAC=1600, Hold=135, ADC Noise vs 18\*Chip+Chan



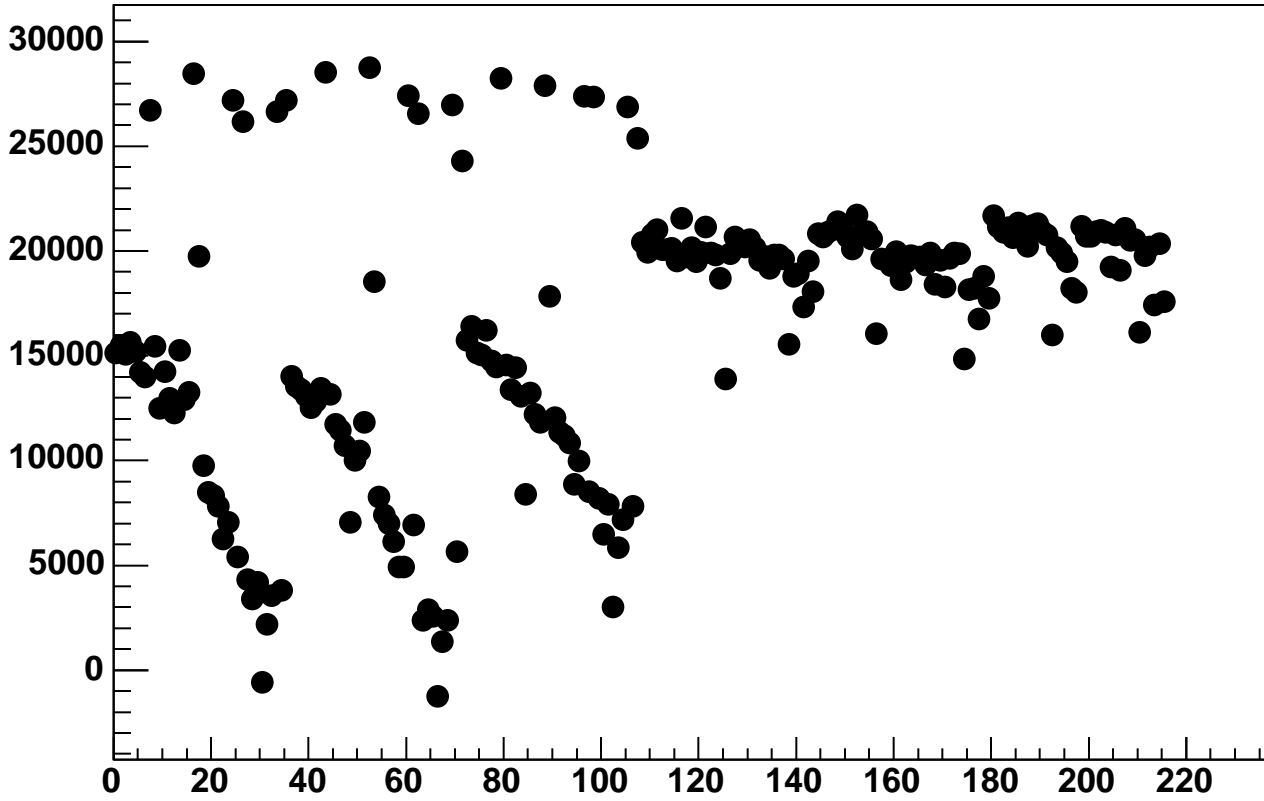
Enable 5, DAC=1600, Hold=140, ADC Mean vs 18\*Chip+Chan



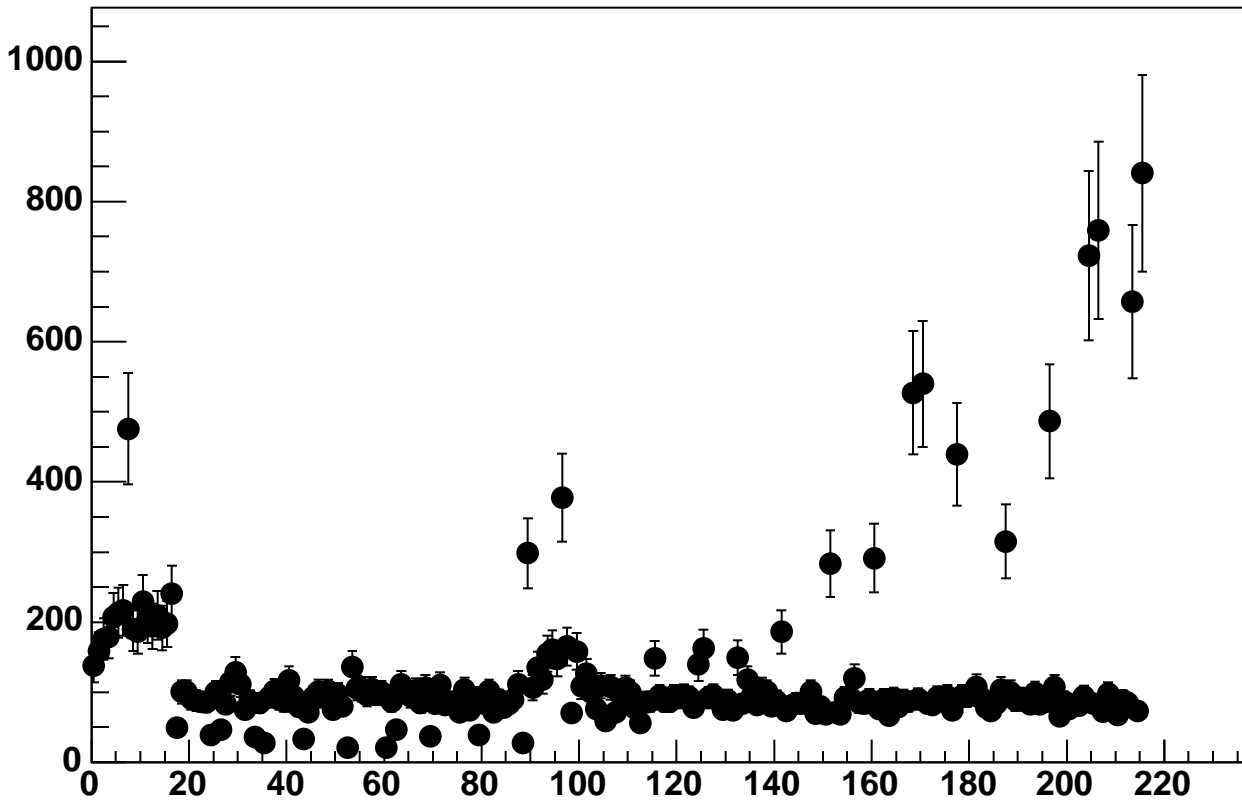
Enable 5, DAC=1600, Hold=140, ADC Noise vs 18\*Chip+Chan



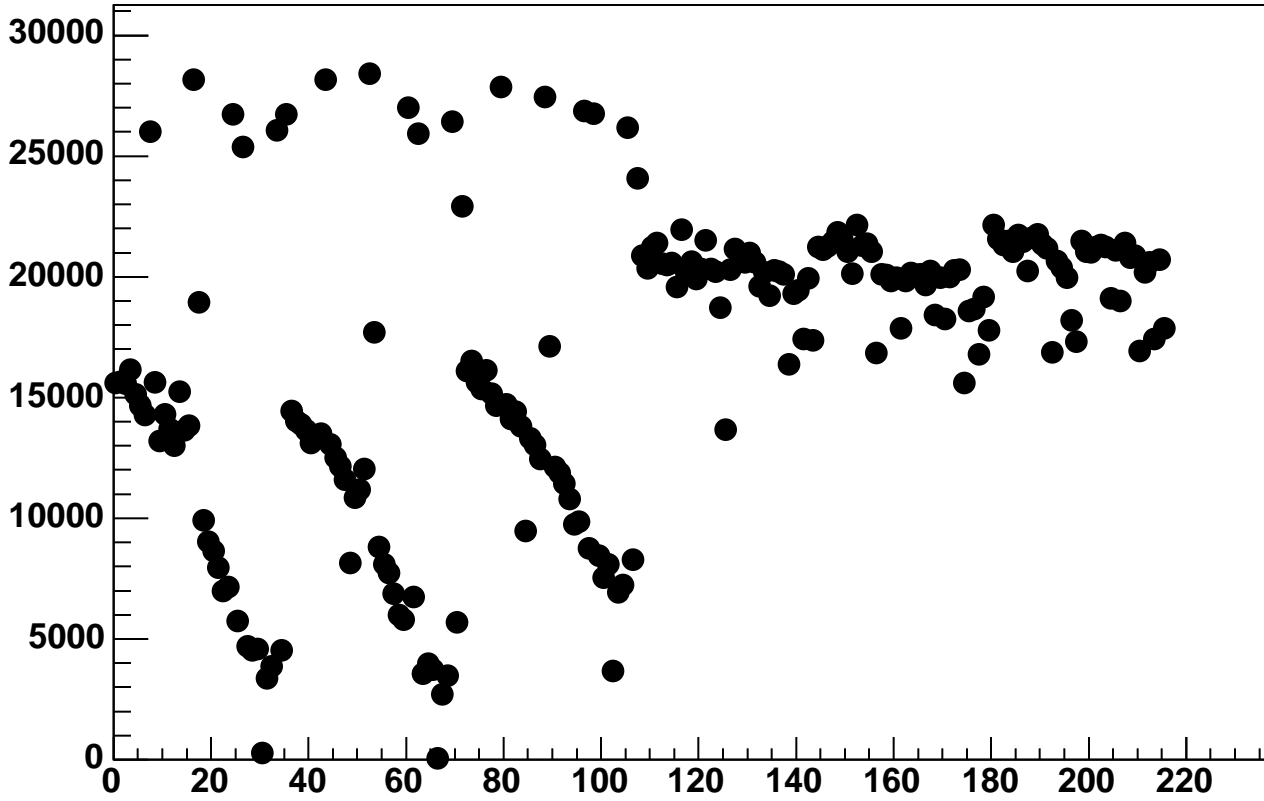
Enable 5, DAC=1600, Hold=145, ADC Mean vs 18\*Chip+Chan



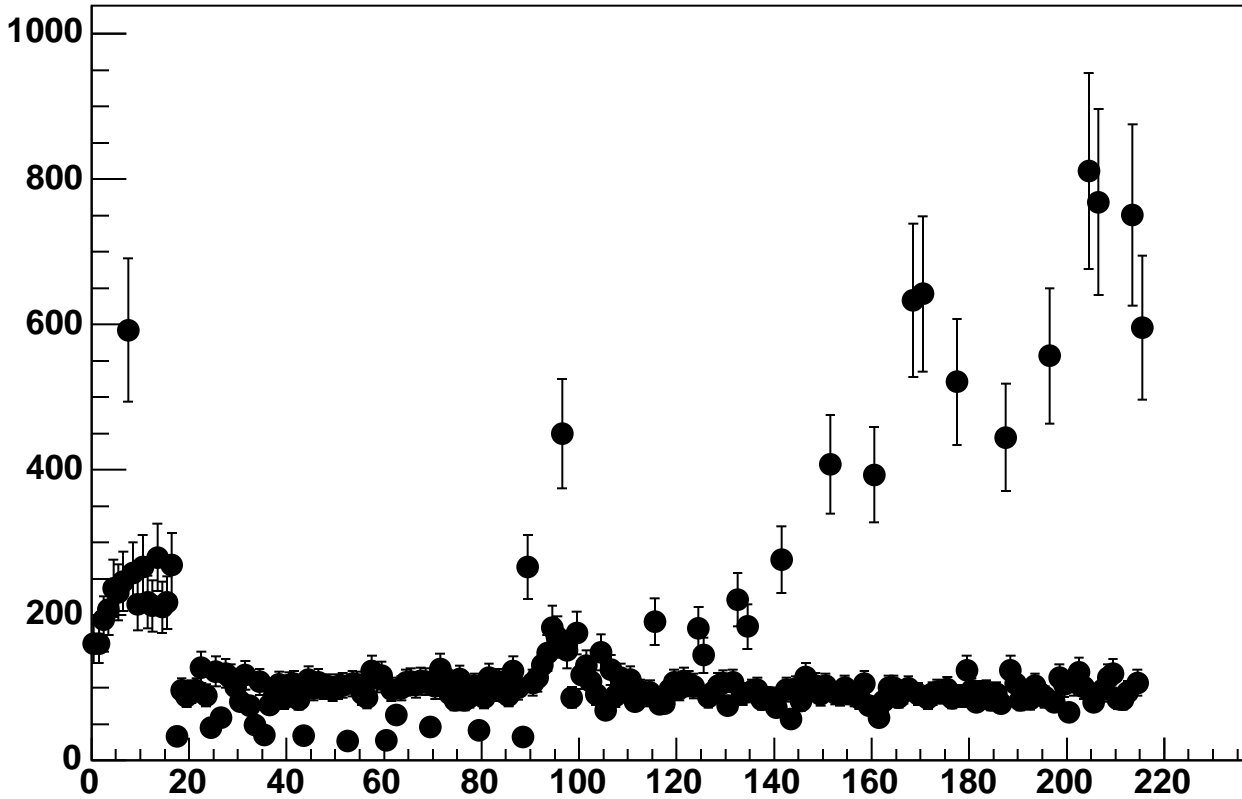
Enable 5, DAC=1600, Hold=145, ADC Noise vs 18\*Chip+Chan



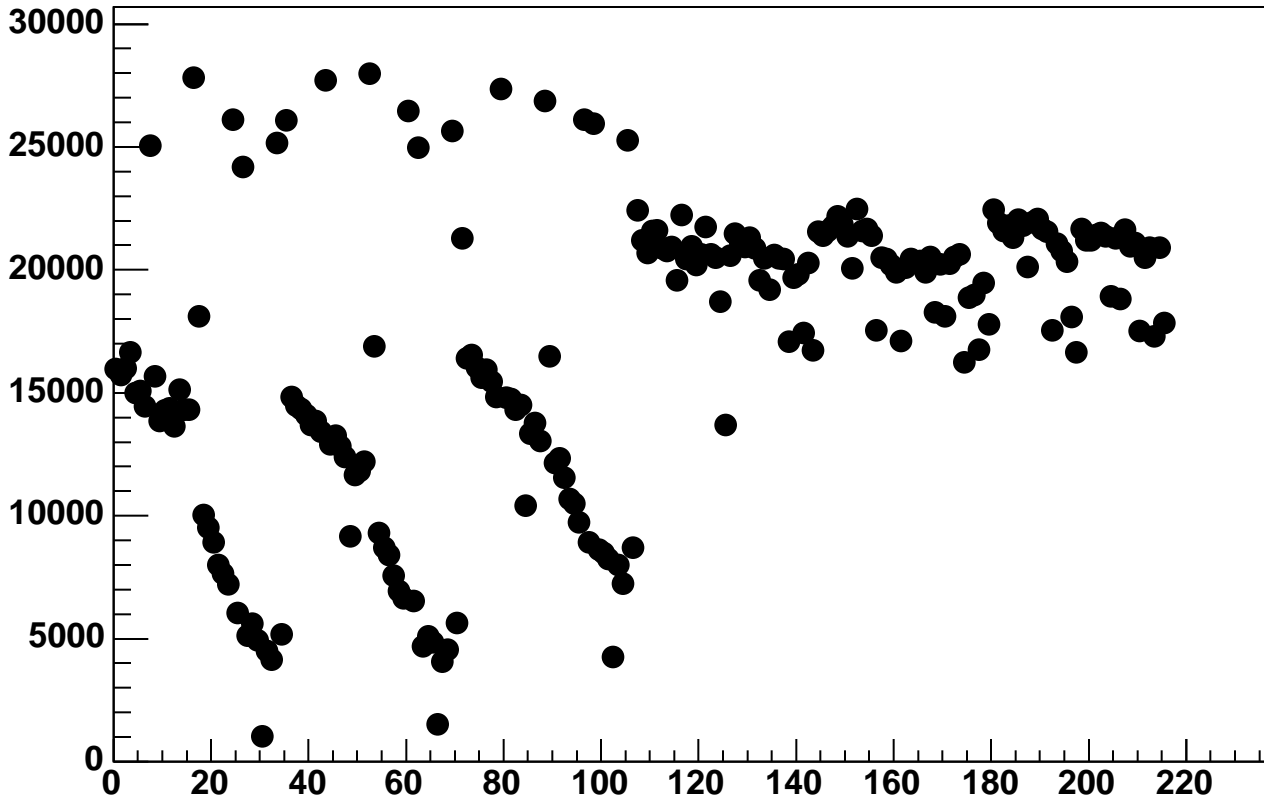
Enable 5, DAC=1600, Hold=150, ADC Mean vs 18\*Chip+Chan



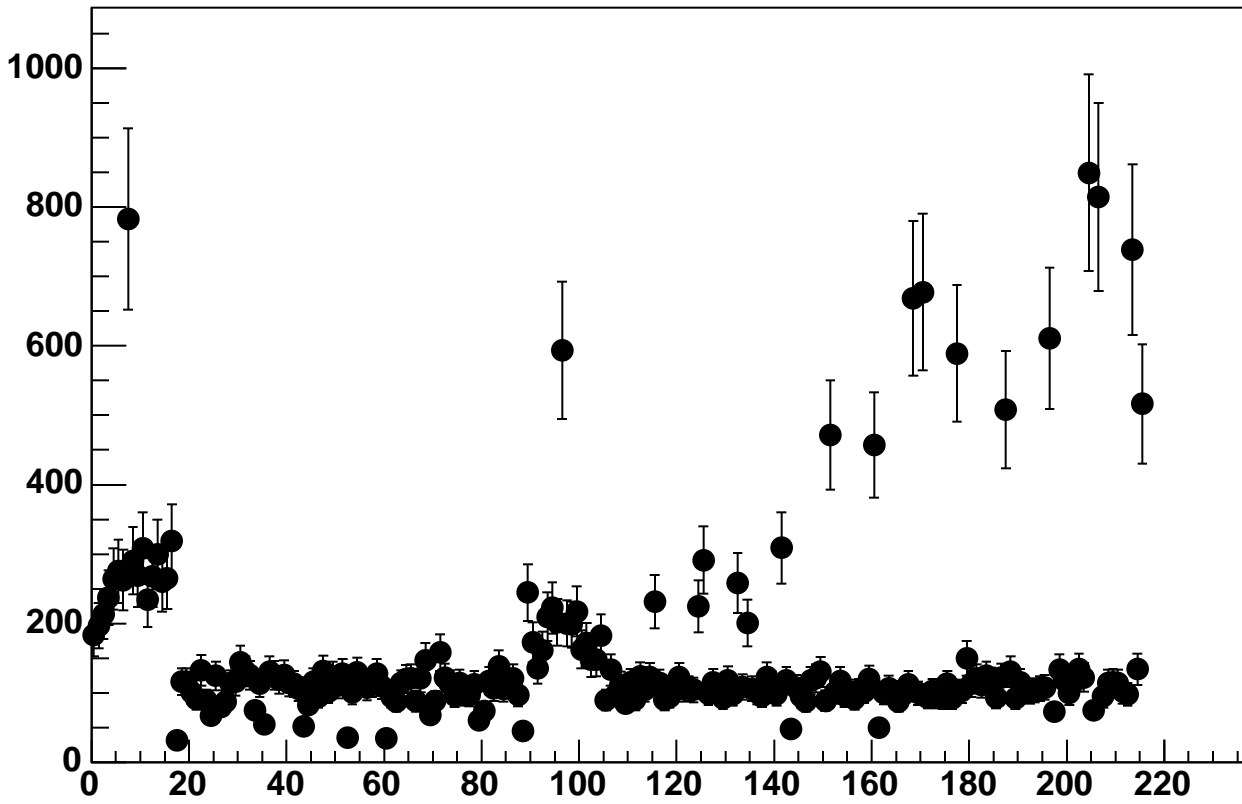
Enable 5, DAC=1600, Hold=150, ADC Noise vs 18\*Chip+Chan



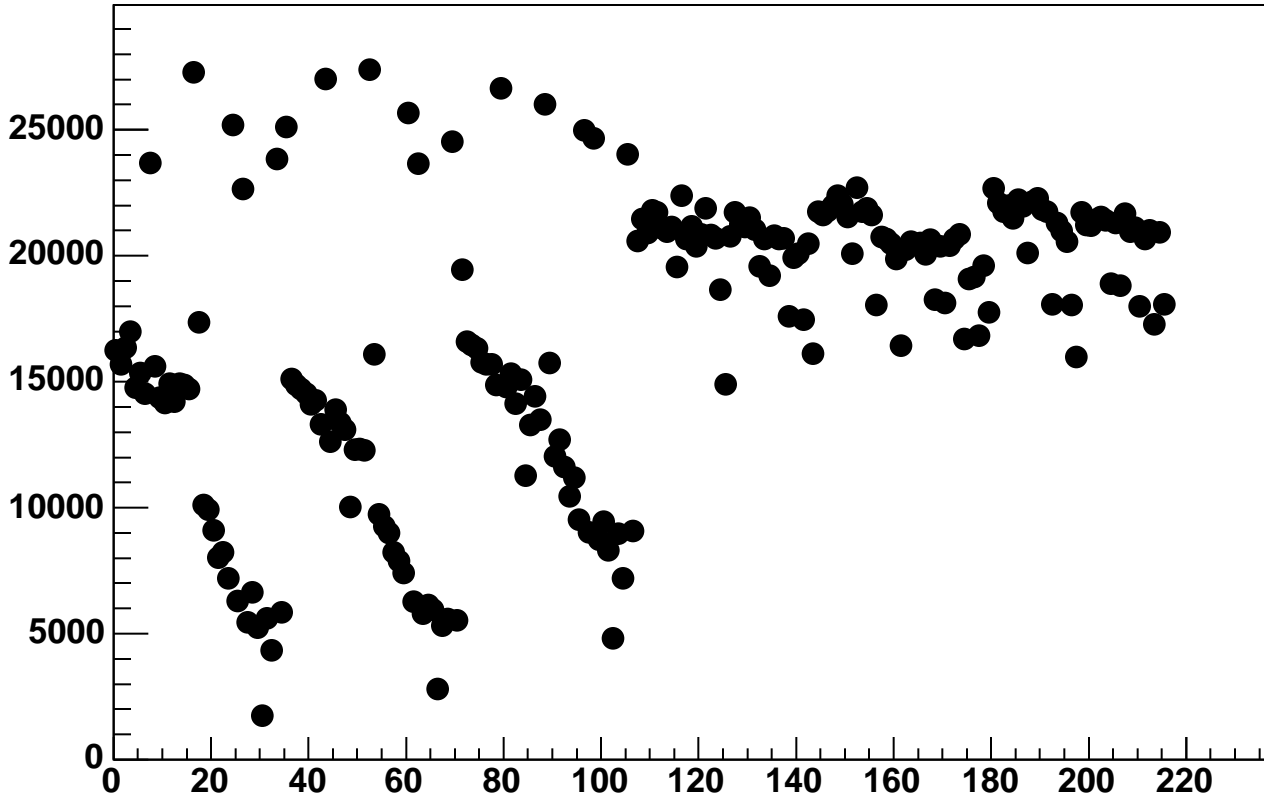
Enable 5, DAC=1600, Hold=155, ADC Mean vs 18\*Chip+Chan



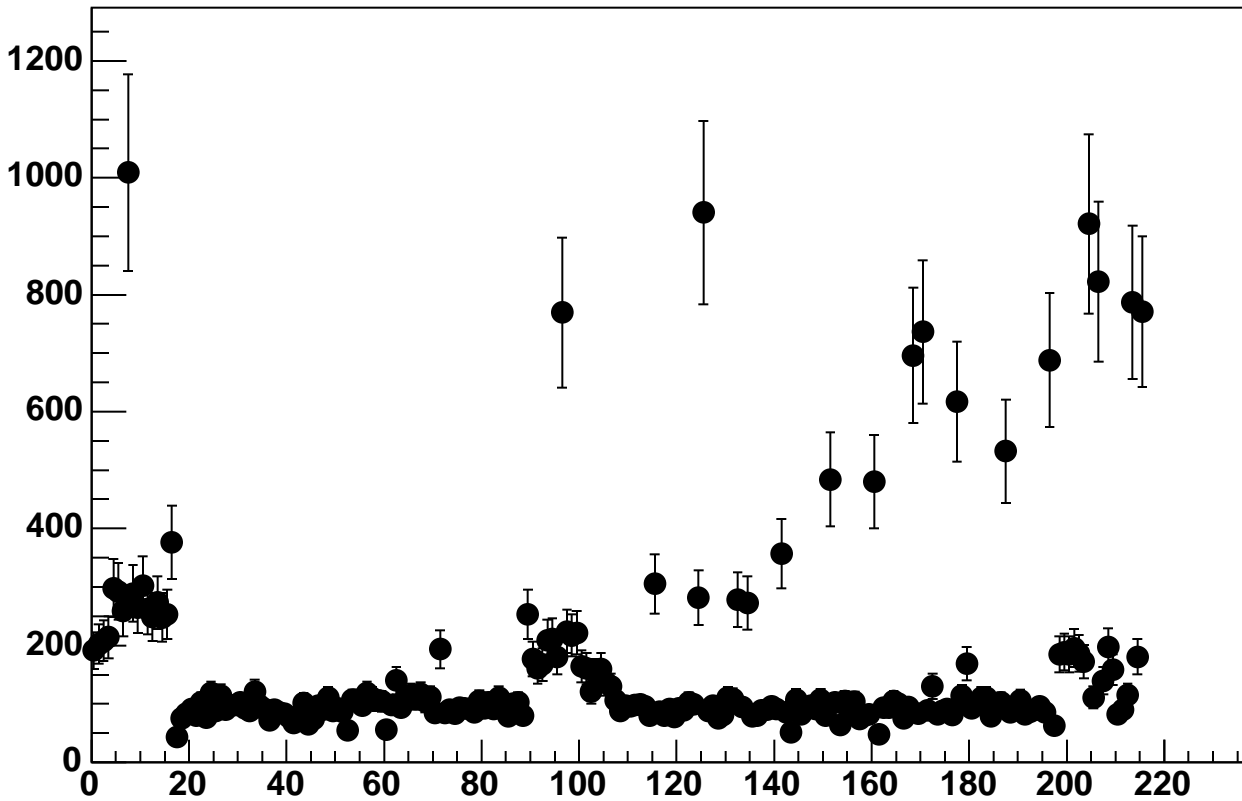
Enable 5, DAC=1600, Hold=155, ADC Noise vs 18\*Chip+Chan



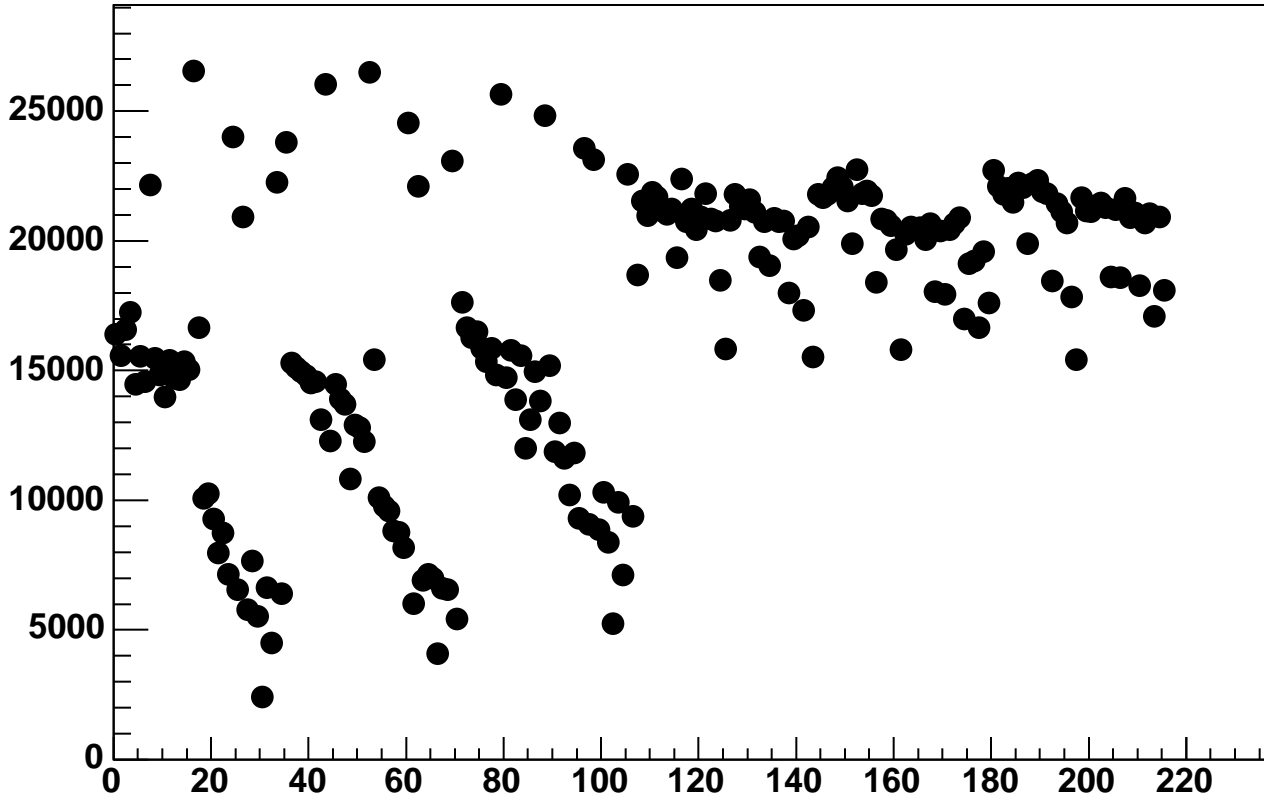
Enable 5, DAC=1600, Hold=160, ADC Mean vs 18\*Chip+Chan



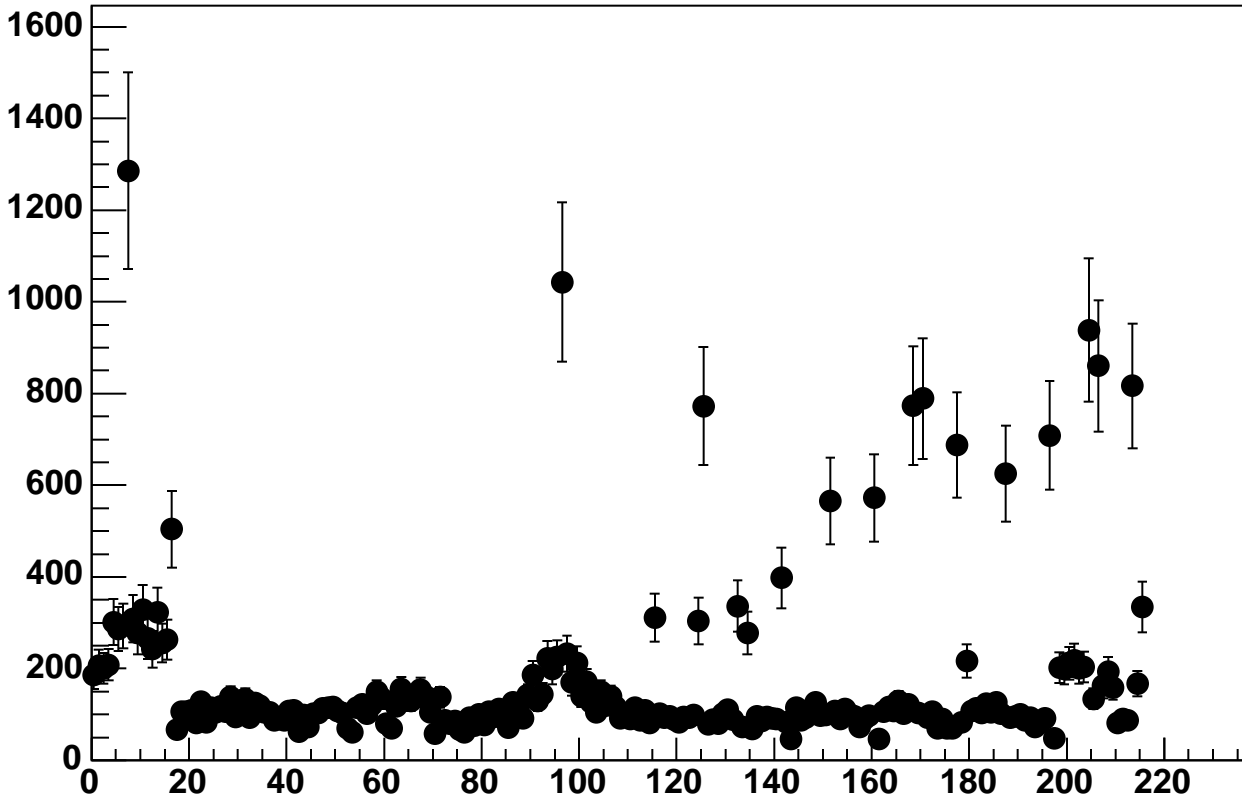
Enable 5, DAC=1600, Hold=160, ADC Noise vs 18\*Chip+Chan



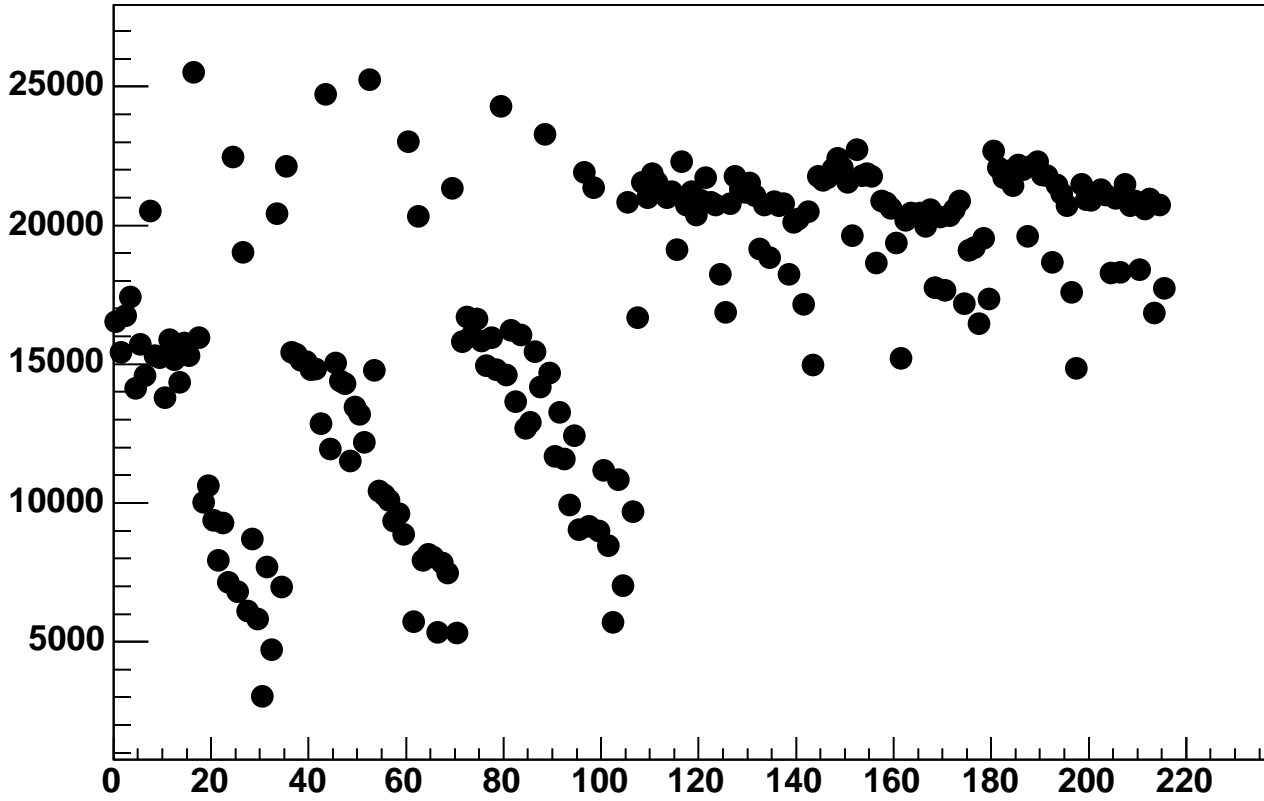
Enable 5, DAC=1600, Hold=165, ADC Mean vs 18\*Chip+Chan



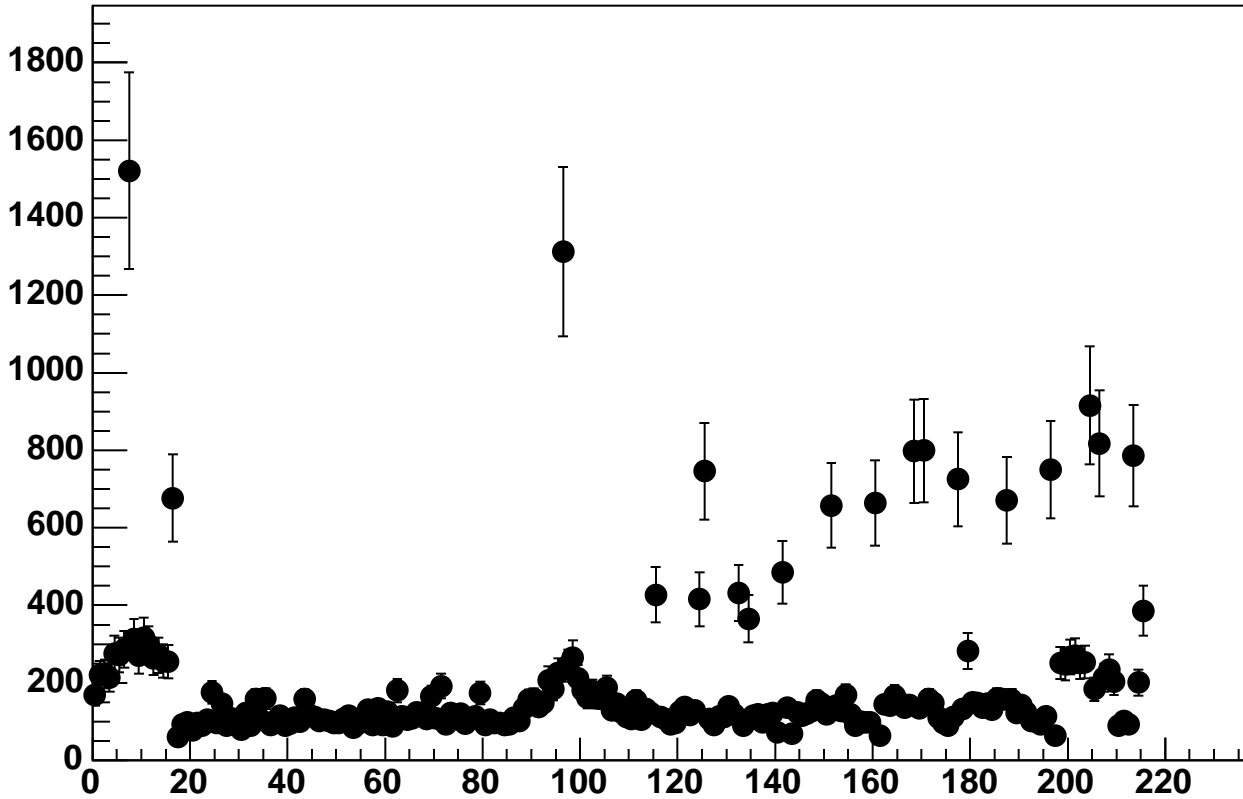
Enable 5, DAC=1600, Hold=165, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=170, ADC Mean vs 18\*Chip+Chan

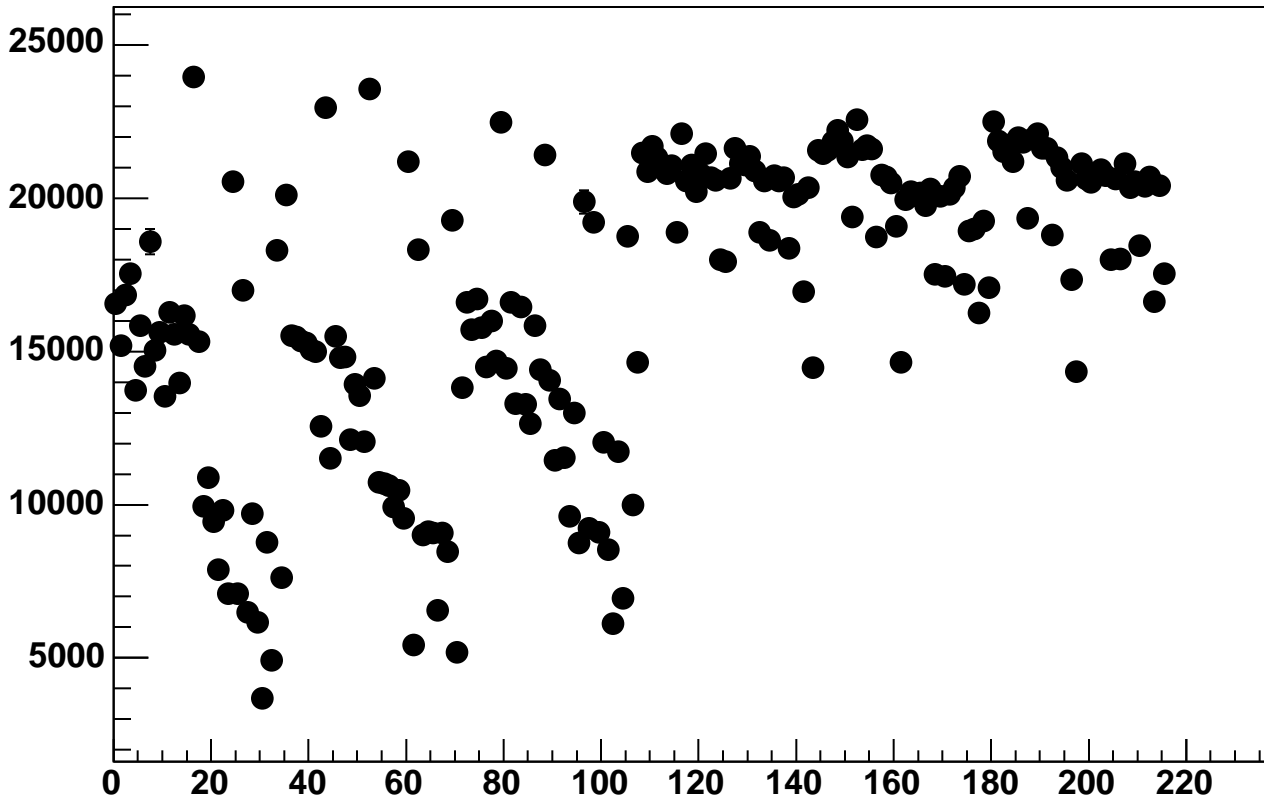


Enable 5, DAC=1600, Hold=170, ADC Noise vs 18\*Chip+Chan

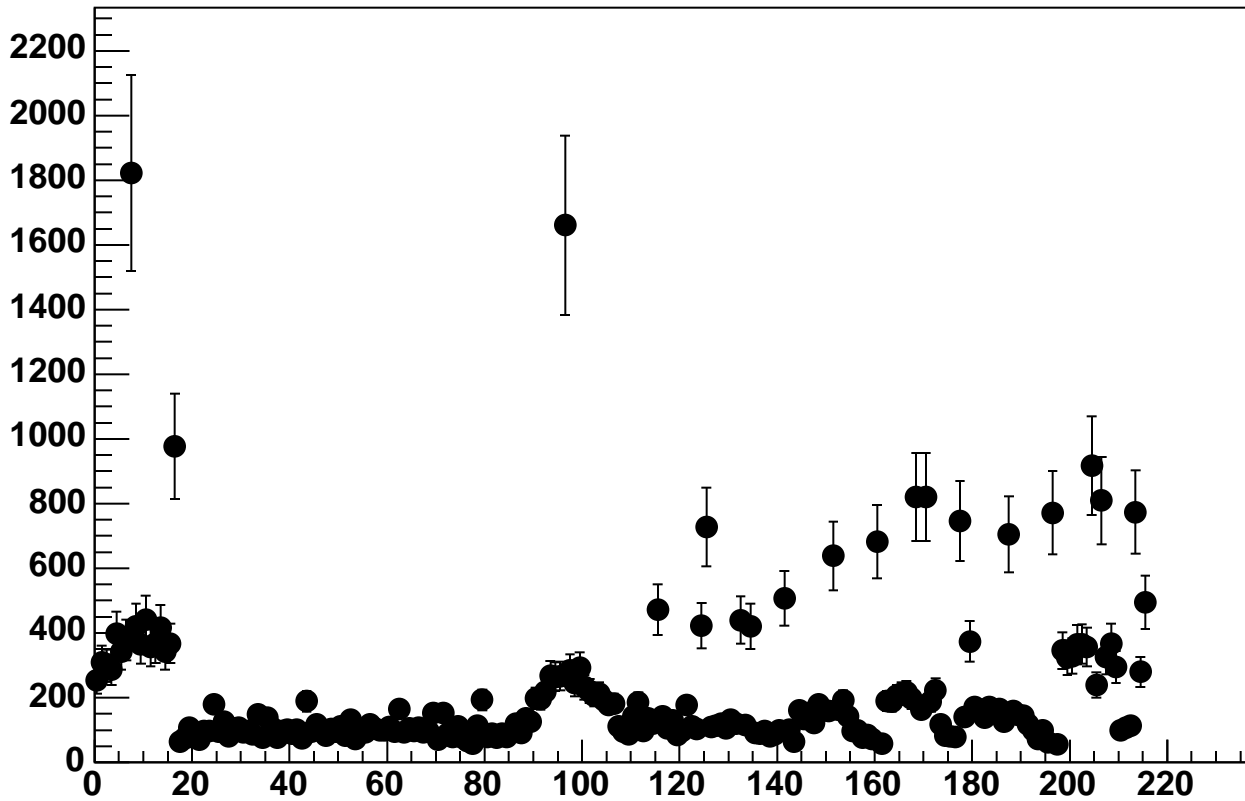




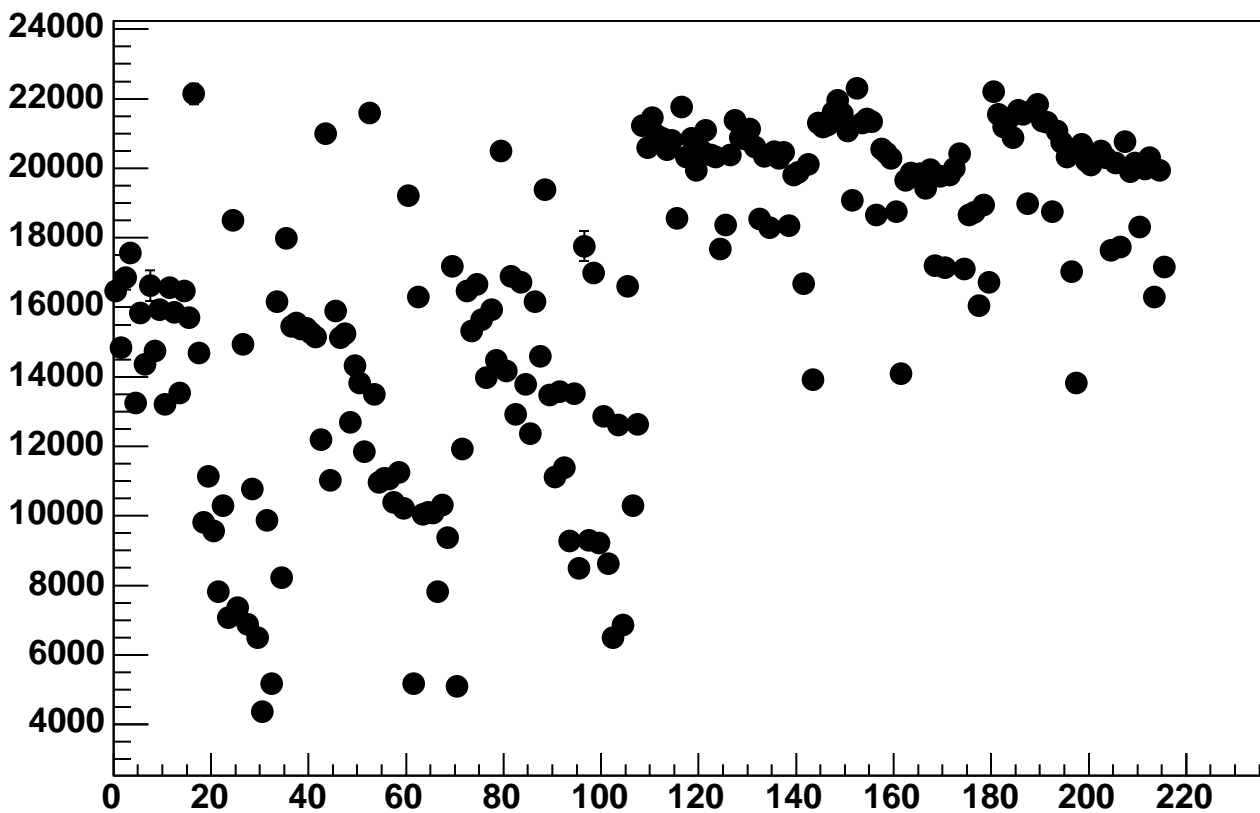
Enable 5, DAC=1600, Hold=175, ADC Mean vs 18\*Chip+Chan



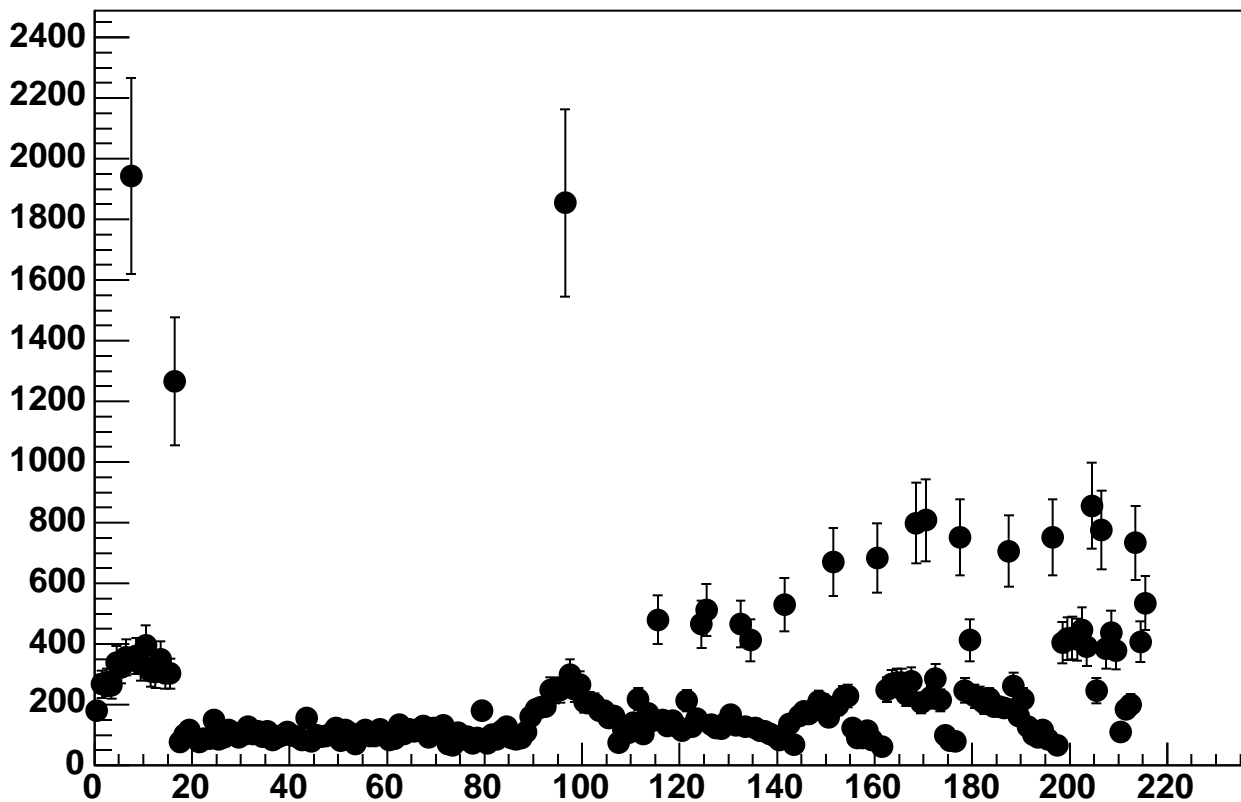
Enable 5, DAC=1600, Hold=175, ADC Noise vs 18\*Chip+Chan



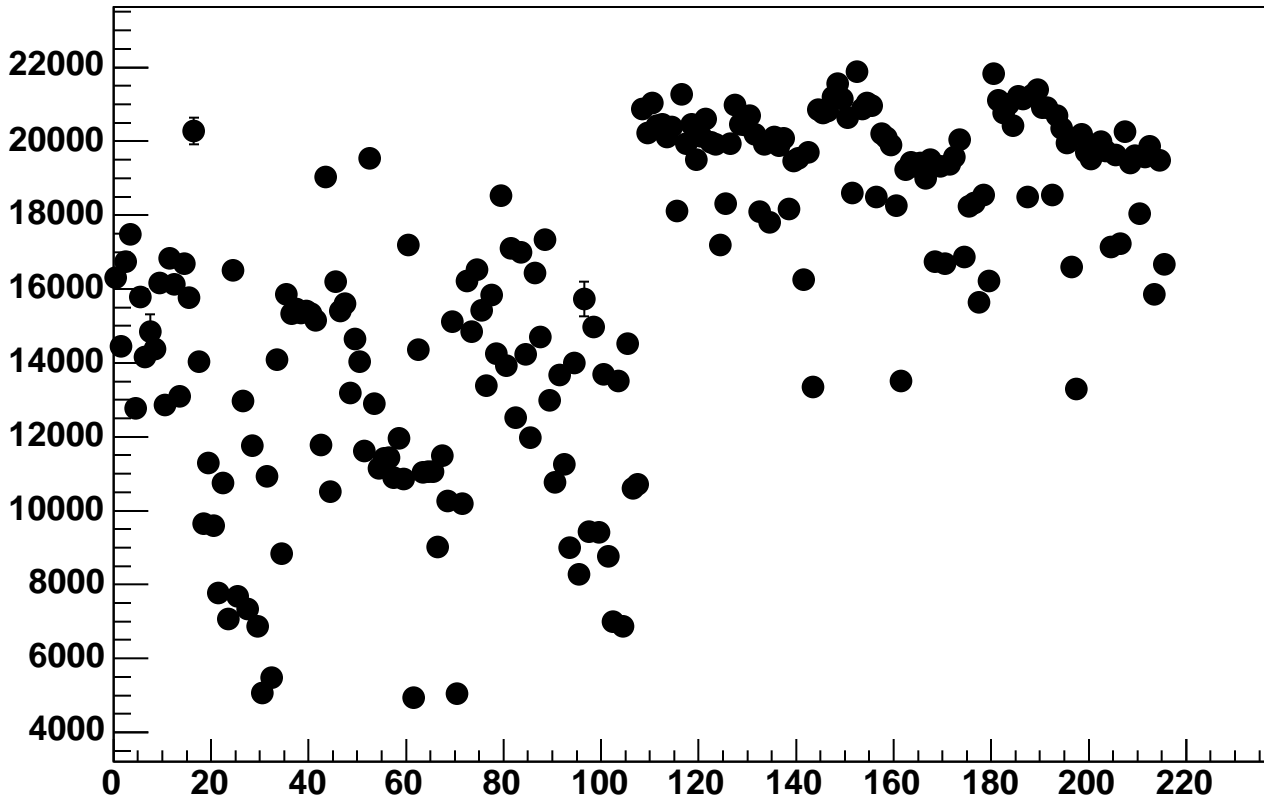
Enable 5, DAC=1600, Hold=180, ADC Mean vs 18\*Chip+Chan



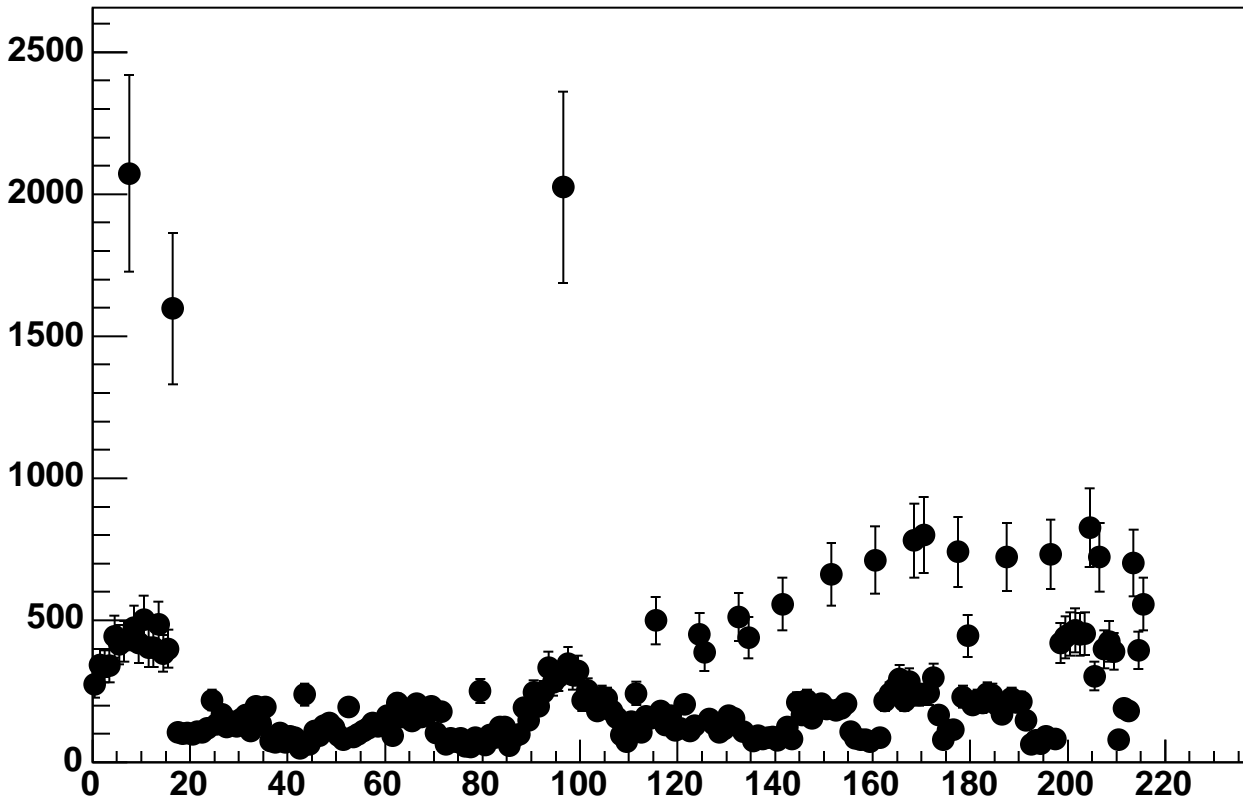
Enable 5, DAC=1600, Hold=180, ADC Noise vs 18\*Chip+Chan



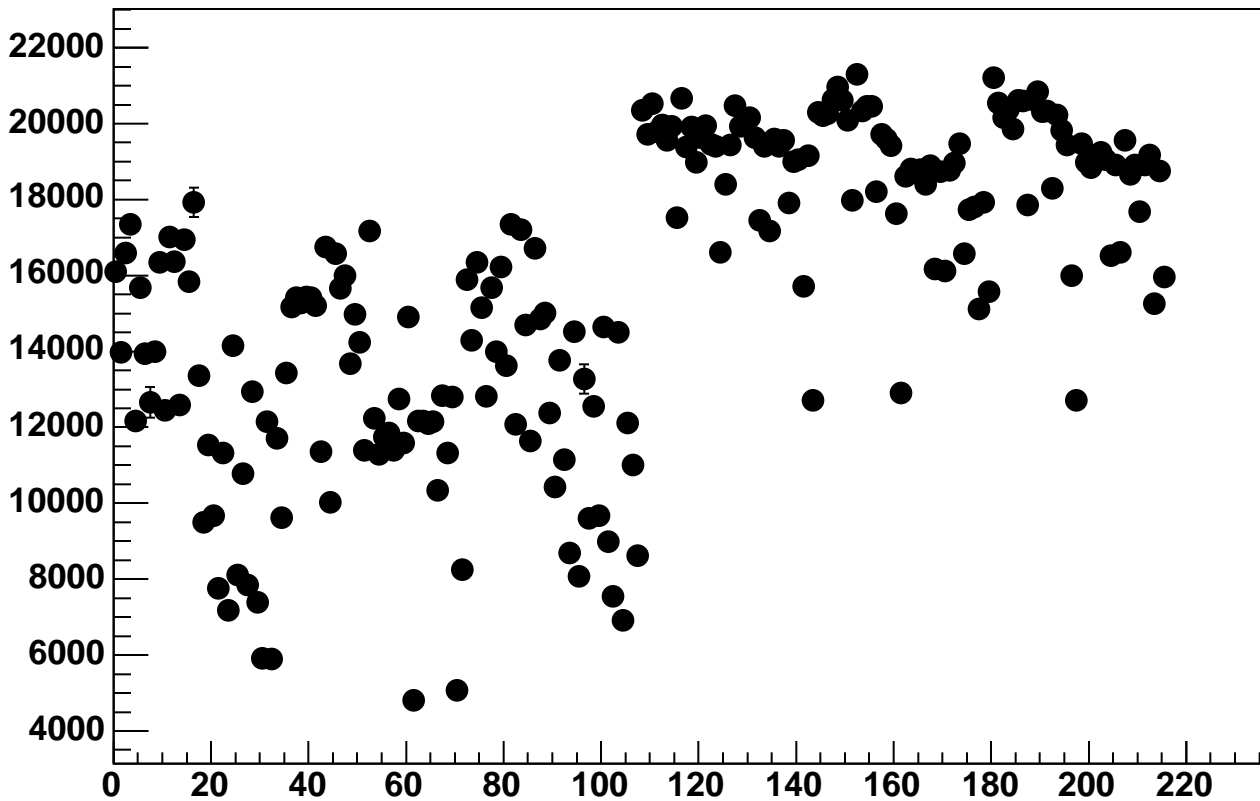
Enable 5, DAC=1600, Hold=185, ADC Mean vs 18\*Chip+Chan



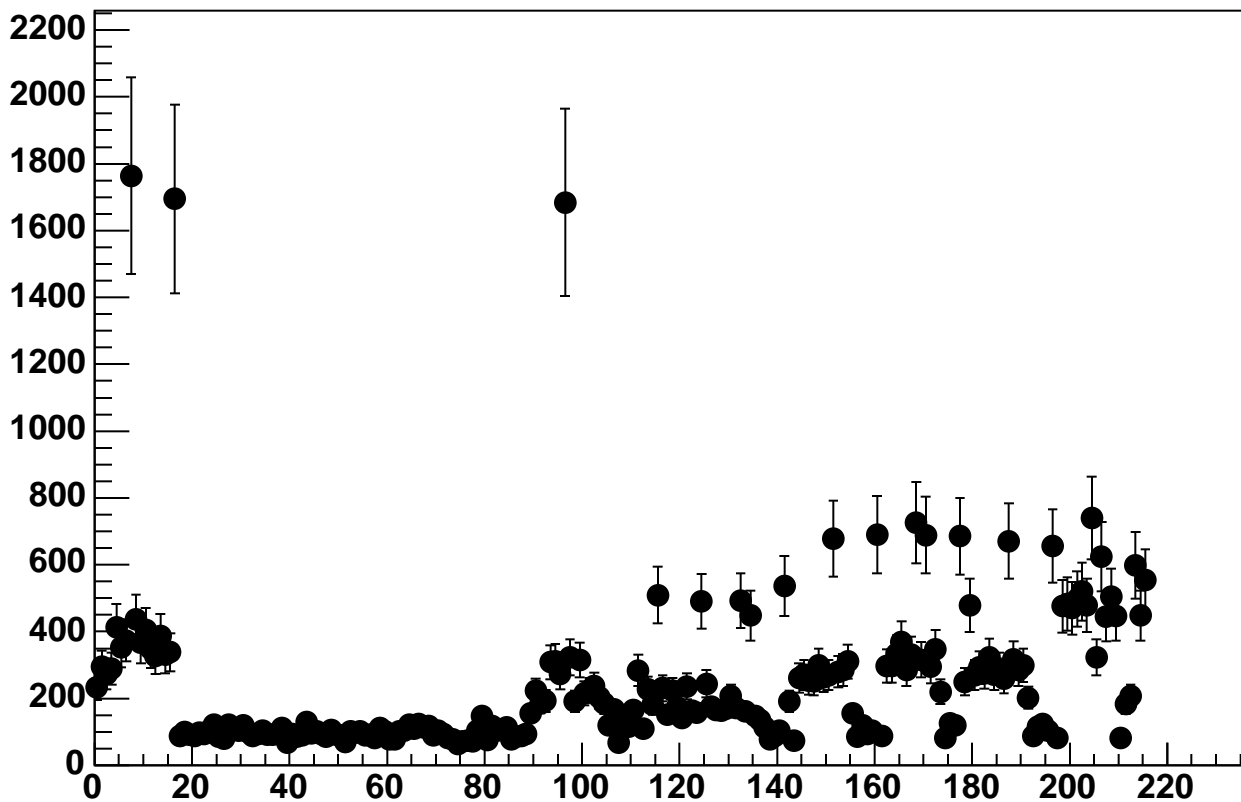
Enable 5, DAC=1600, Hold=185, ADC Noise vs 18\*Chip+Chan



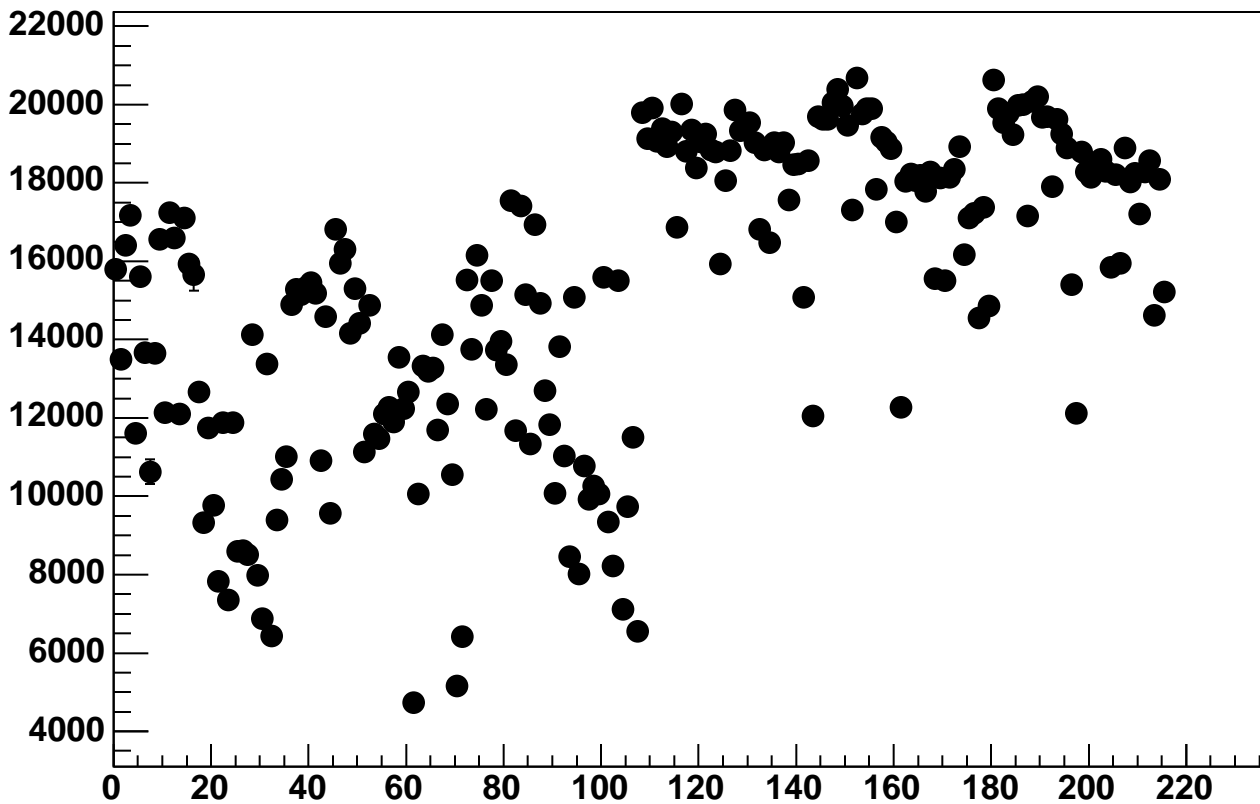
Enable 5, DAC=1600, Hold=190, ADC Mean vs 18\*Chip+Chan



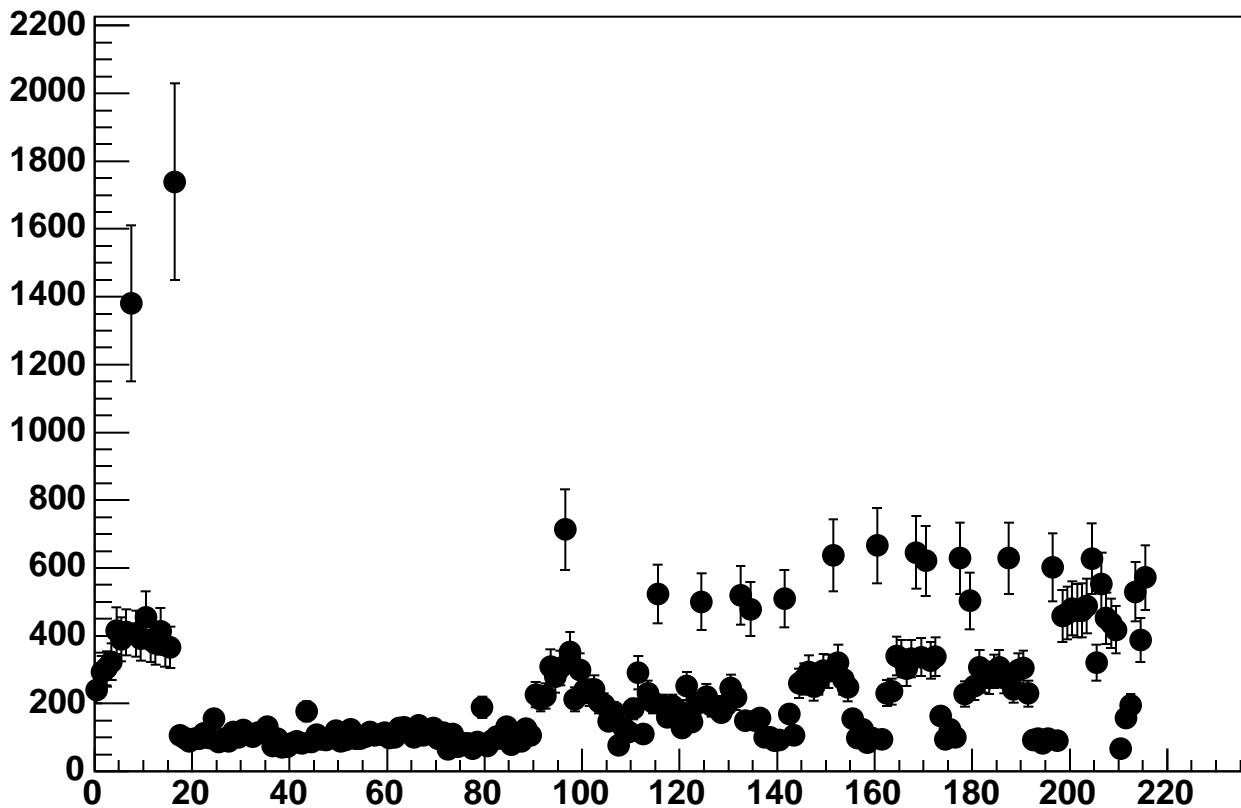
Enable 5, DAC=1600, Hold=190, ADC Noise vs 18\*Chip+Chan



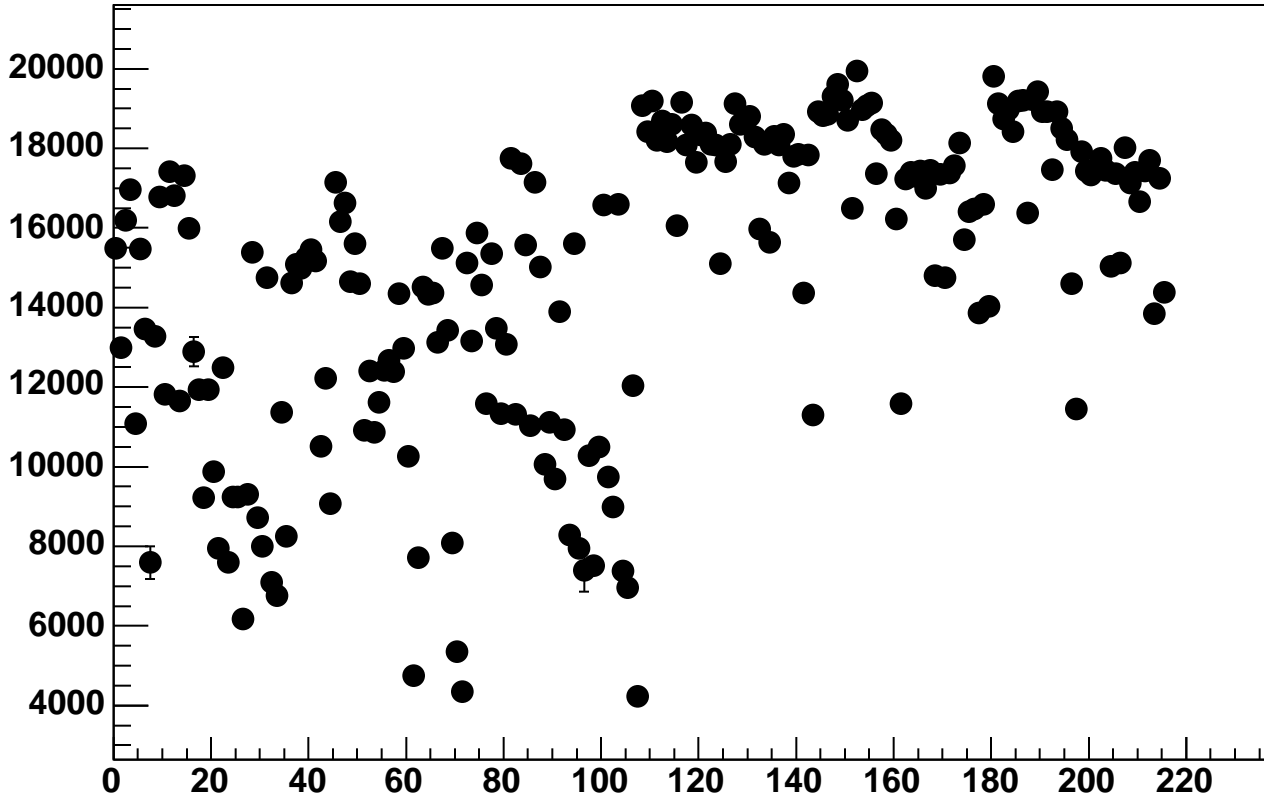
Enable 5, DAC=1600, Hold=195, ADC Mean vs 18\*Chip+Chan



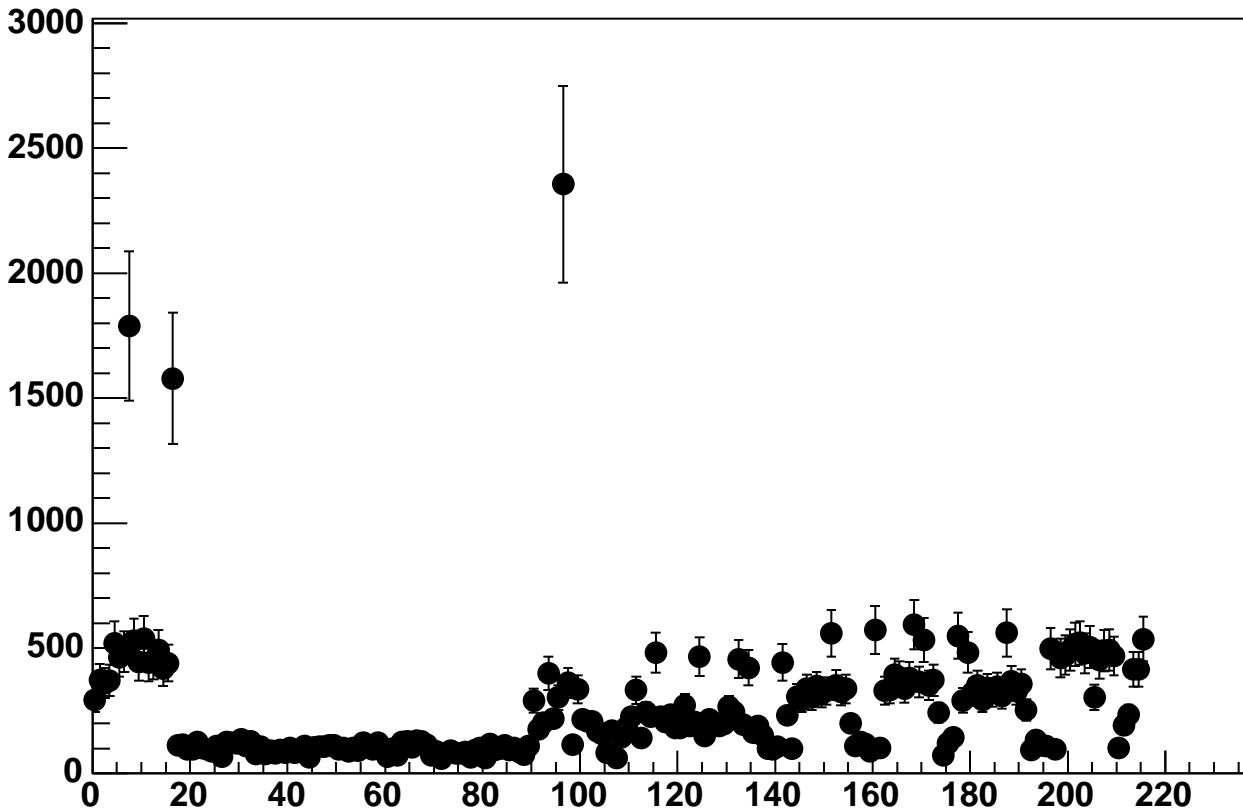
Enable 5, DAC=1600, Hold=195, ADC Noise vs 18\*Chip+Chan



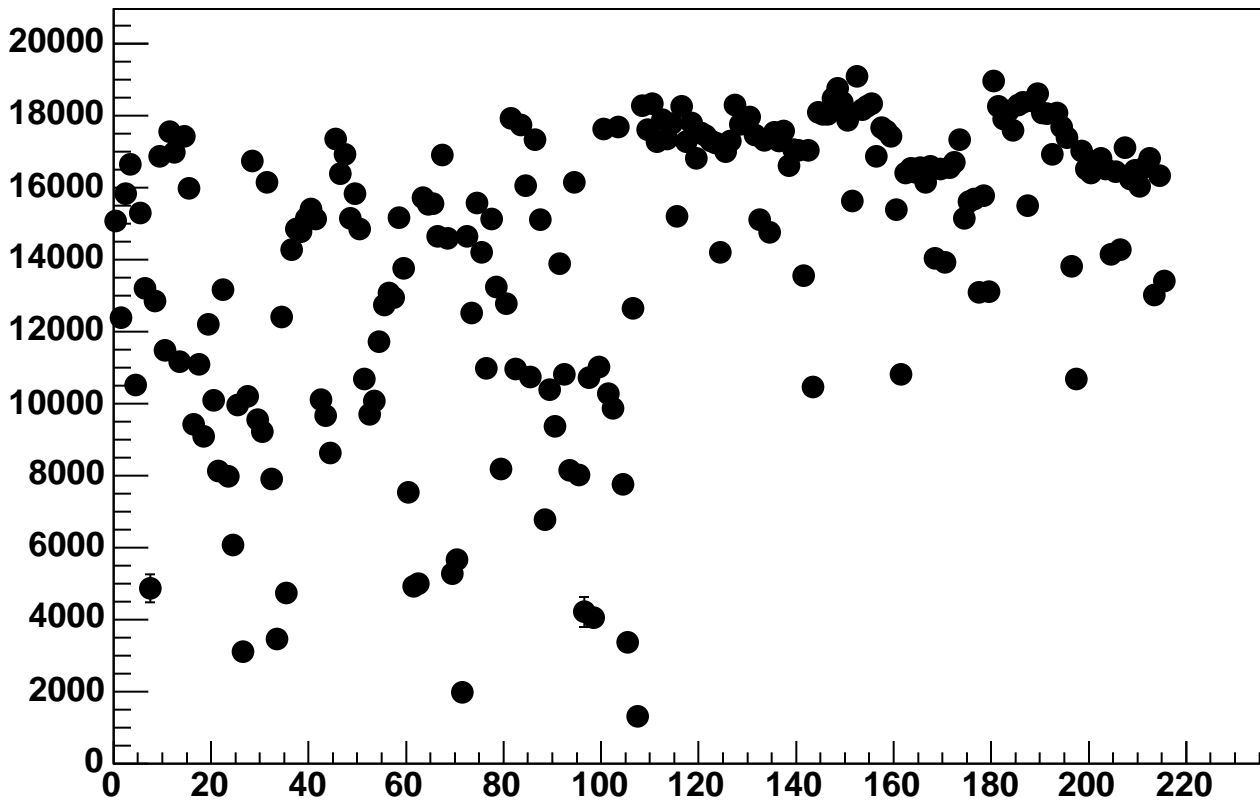
Enable 5, DAC=1600, Hold=200, ADC Mean vs 18\*Chip+Chan



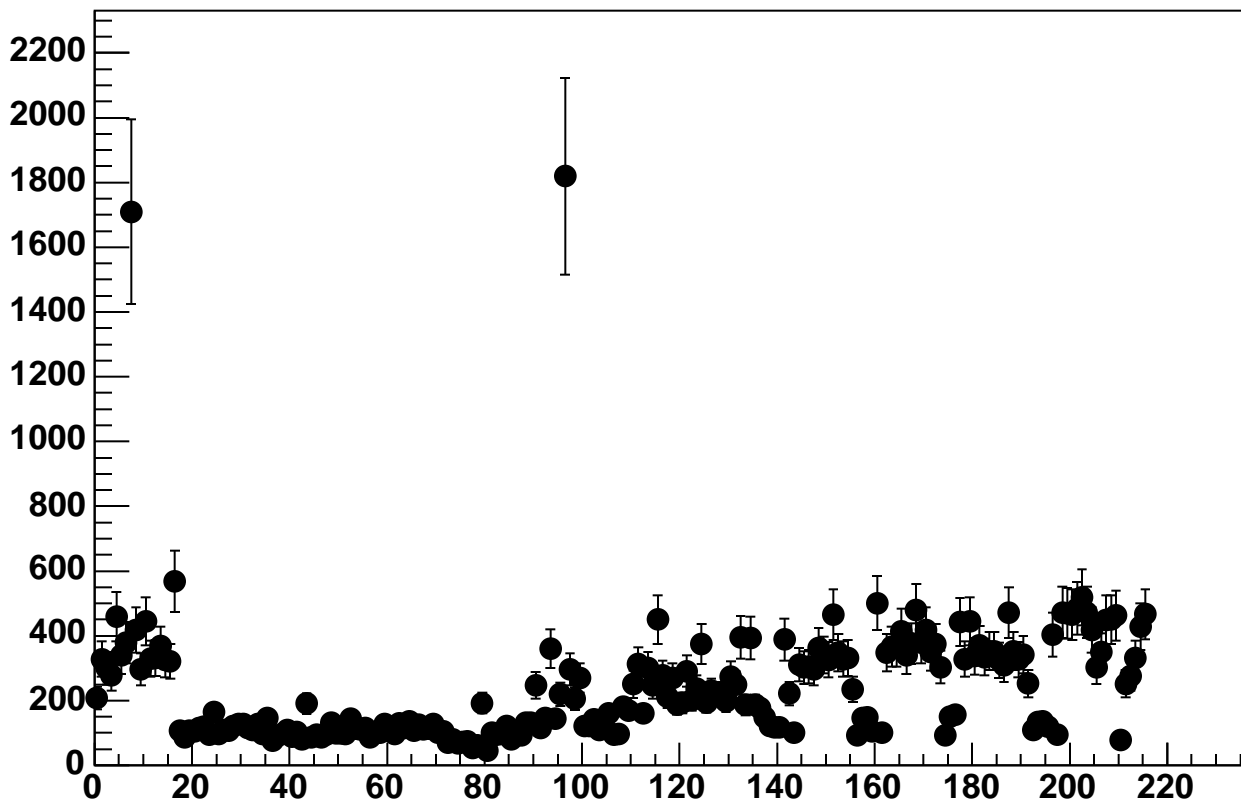
Enable 5, DAC=1600, Hold=200, ADC Noise vs 18\*Chip+Chan



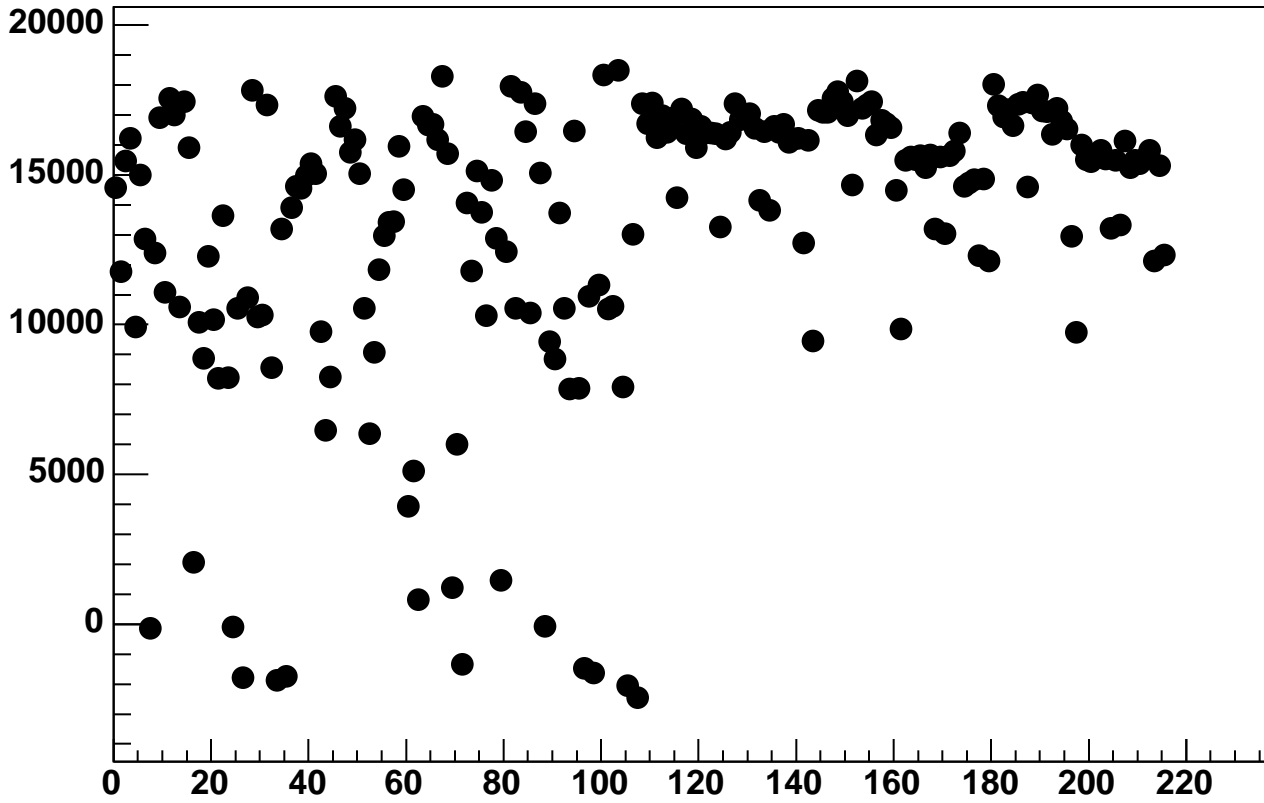
Enable 5, DAC=1600, Hold=205, ADC Mean vs 18\*Chip+Chan



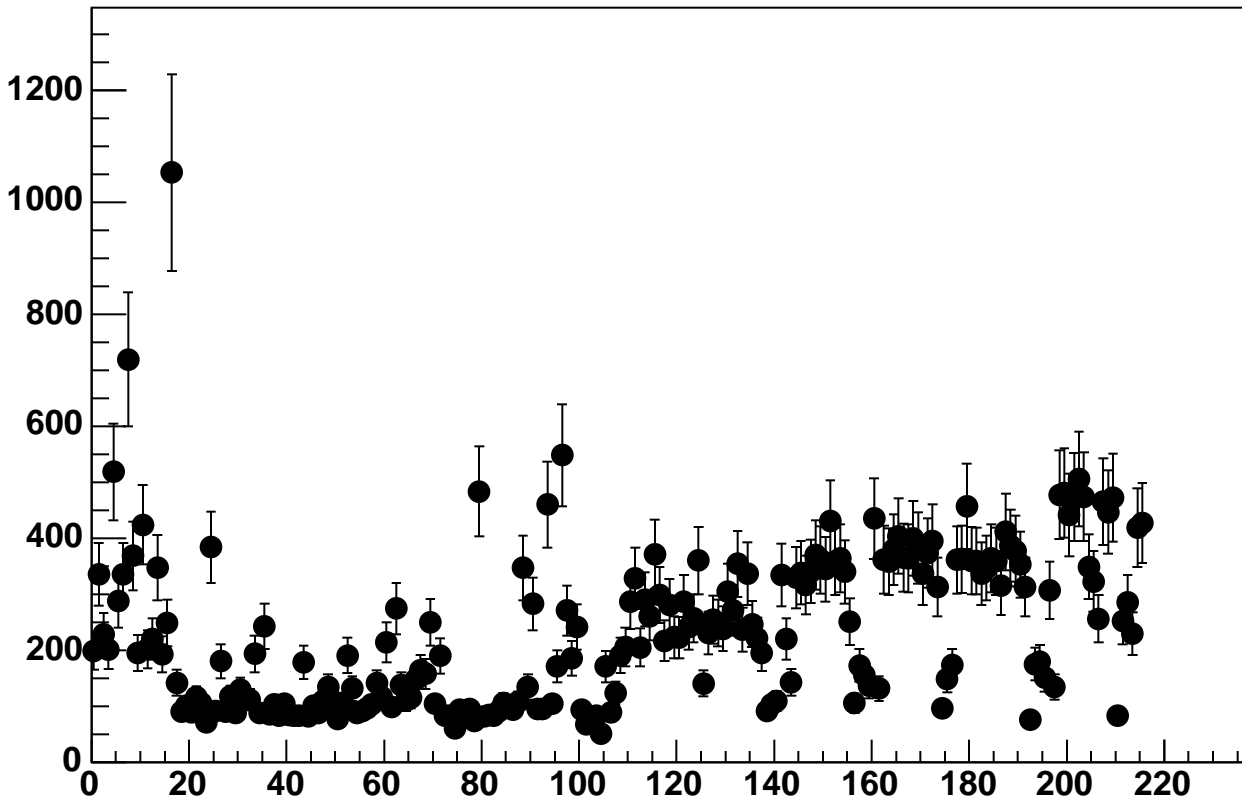
Enable 5, DAC=1600, Hold=205, ADC Noise vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=210, ADC Mean vs 18\*Chip+Chan

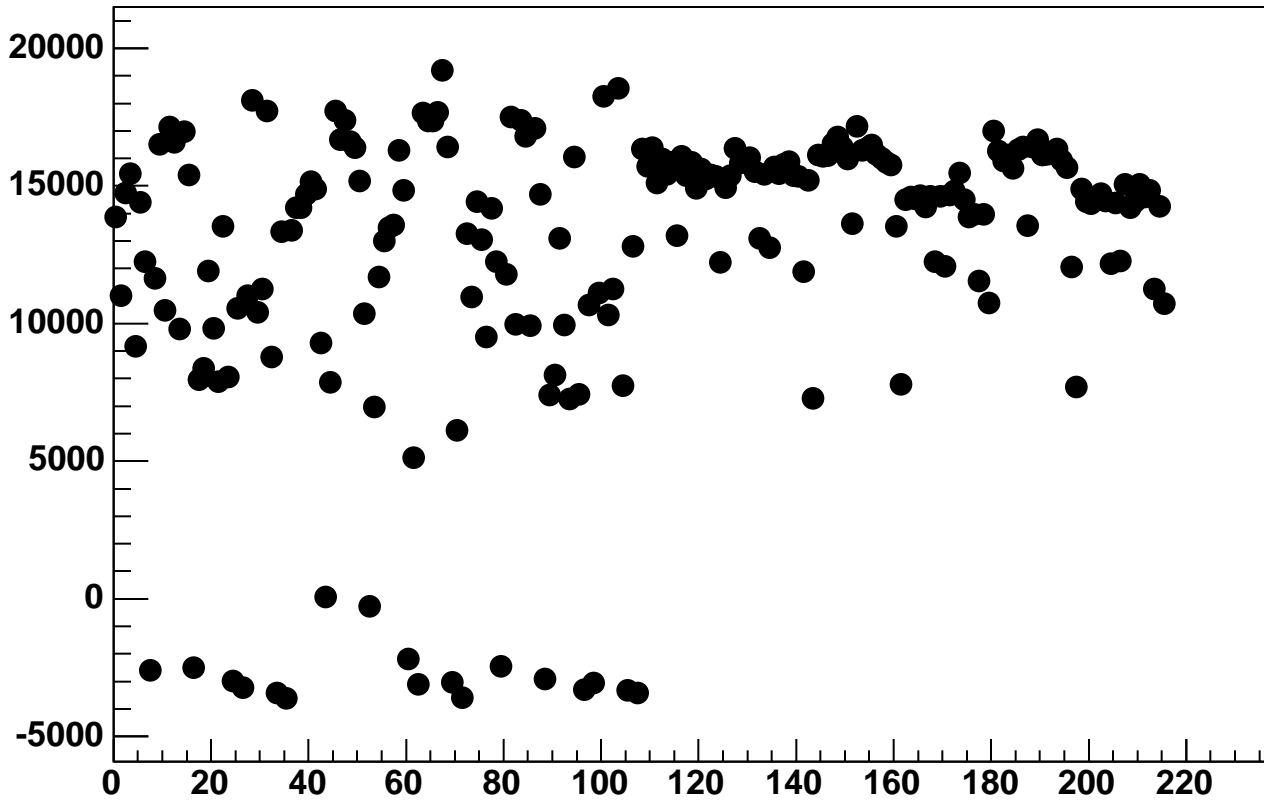


Enable 5, DAC=1600, Hold=210, ADC Noise vs 18\*Chip+Chan

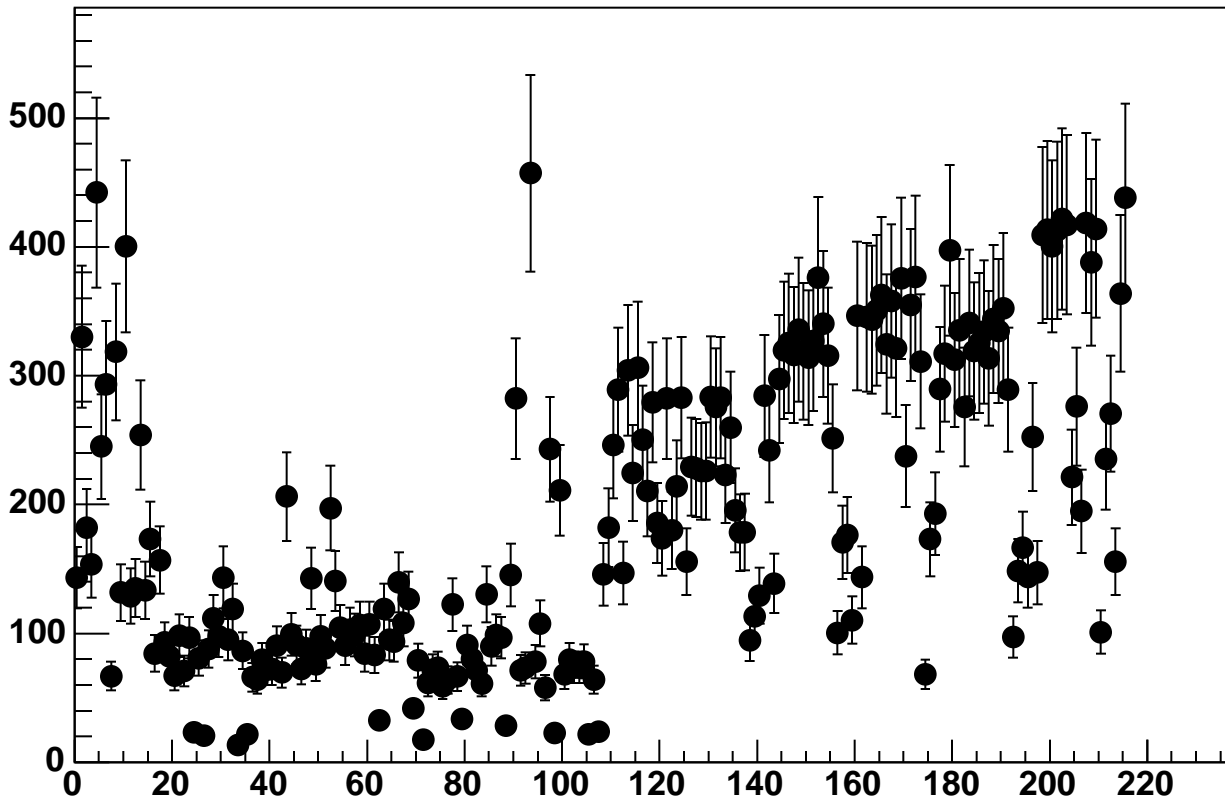




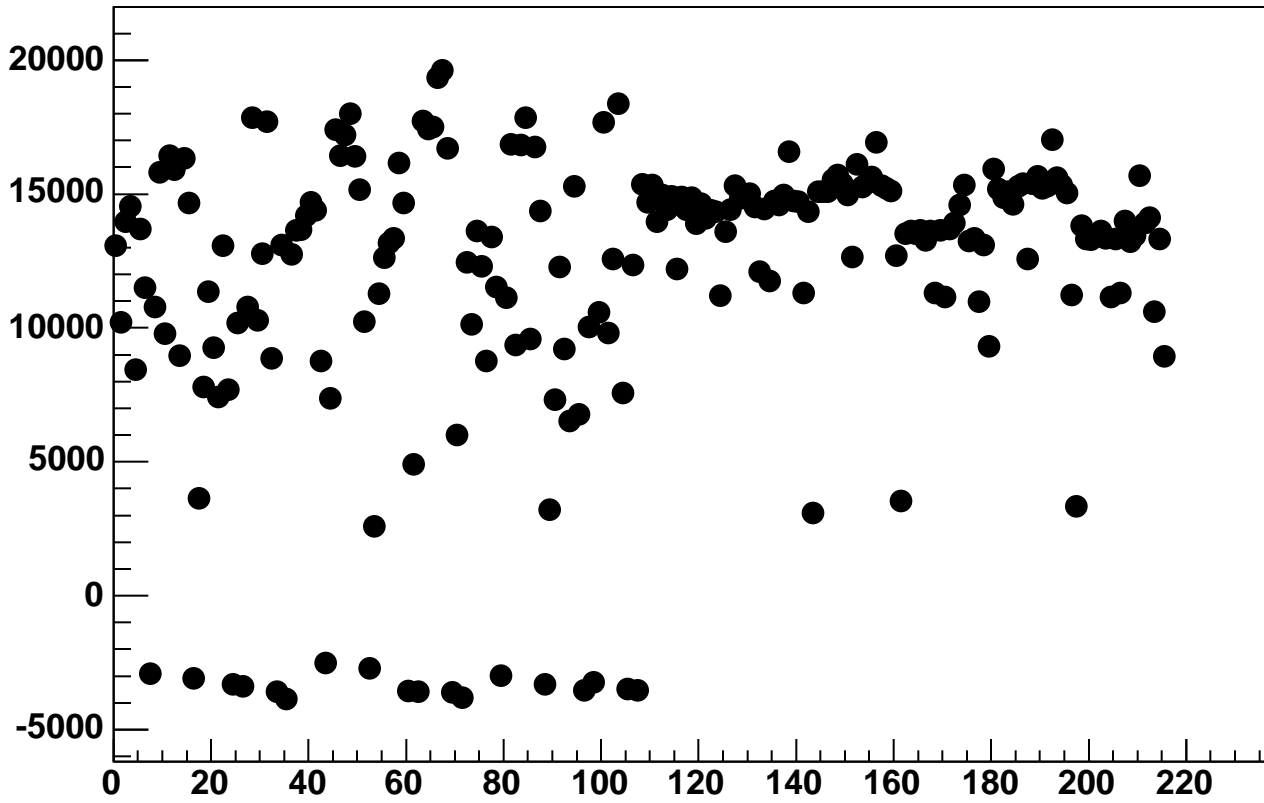
Enable 5, DAC=1600, Hold=215, ADC Mean vs 18\*Chip+Chan



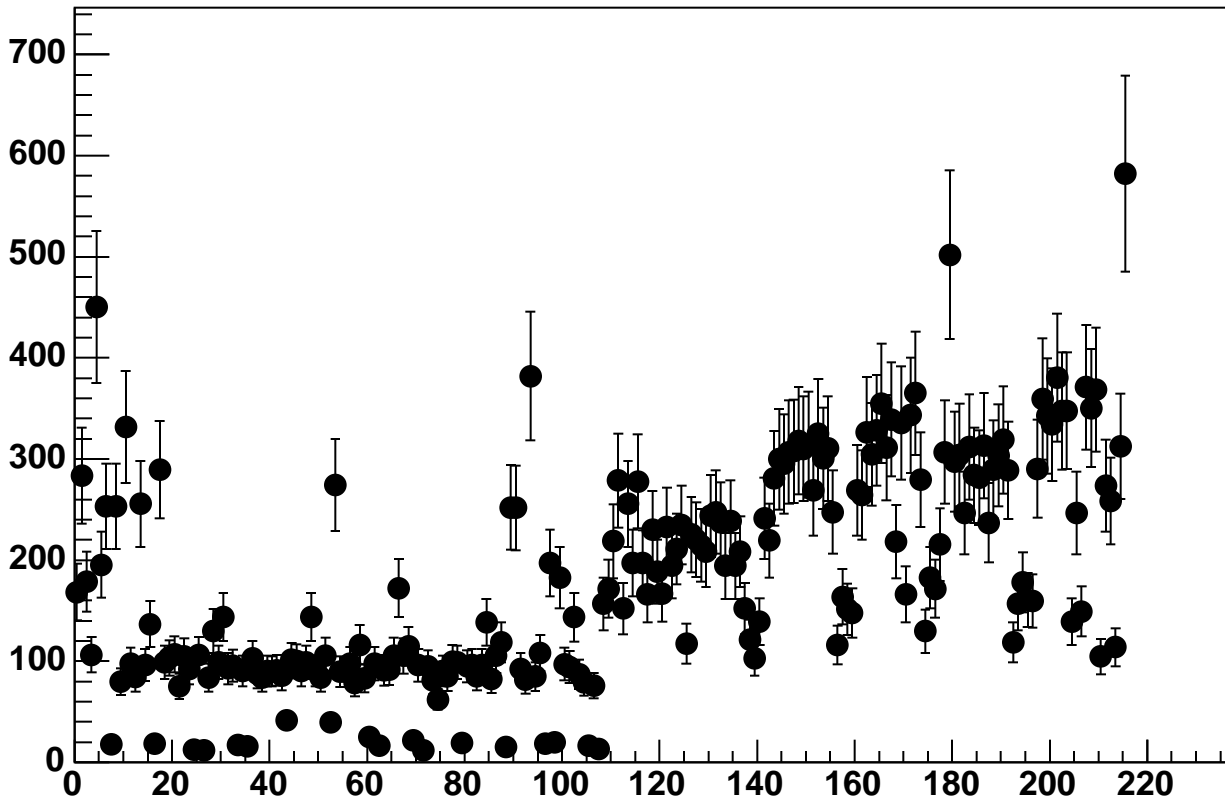
Enable 5, DAC=1600, Hold=215, ADC Noise vs 18\*Chip+Chan



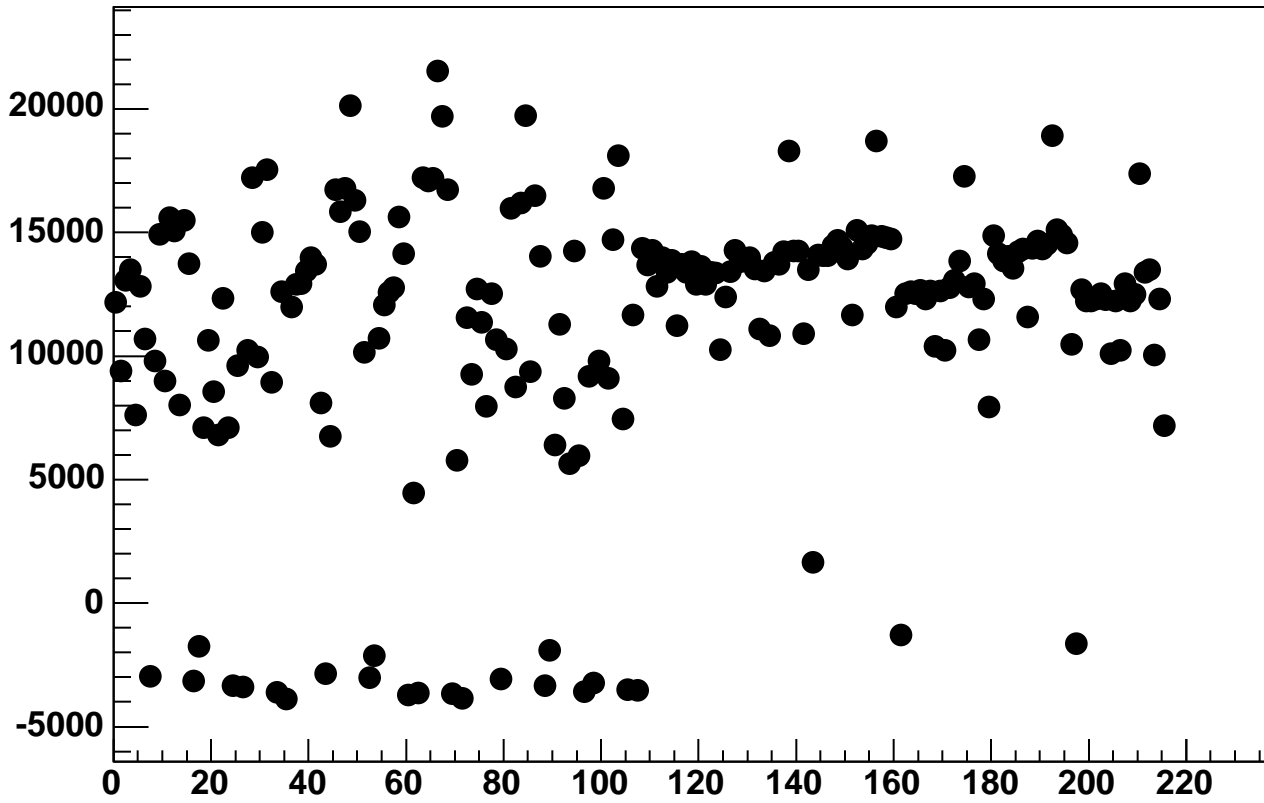
Enable 5, DAC=1600, Hold=220, ADC Mean vs 18\*Chip+Chan



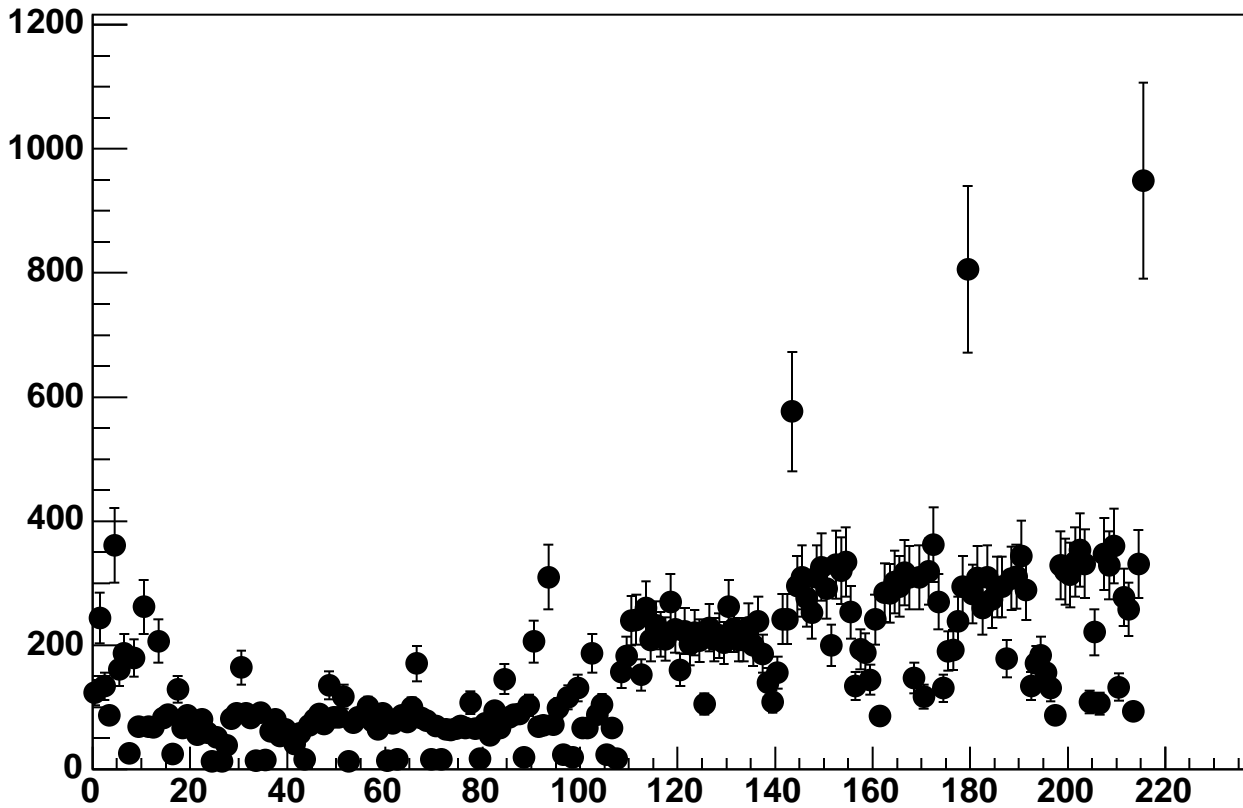
Enable 5, DAC=1600, Hold=220, ADC Noise vs 18\*Chip+Chan



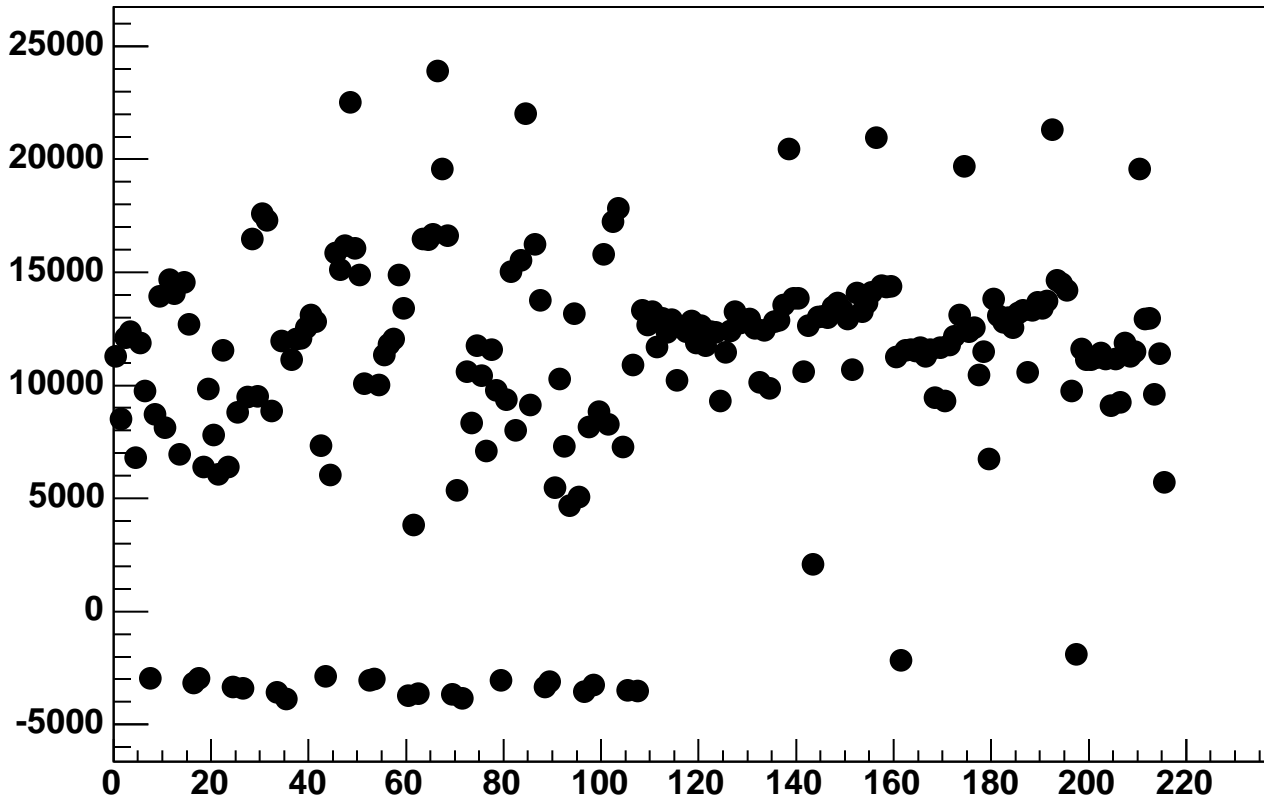
Enable 5, DAC=1600, Hold=225, ADC Mean vs 18\*Chip+Chan



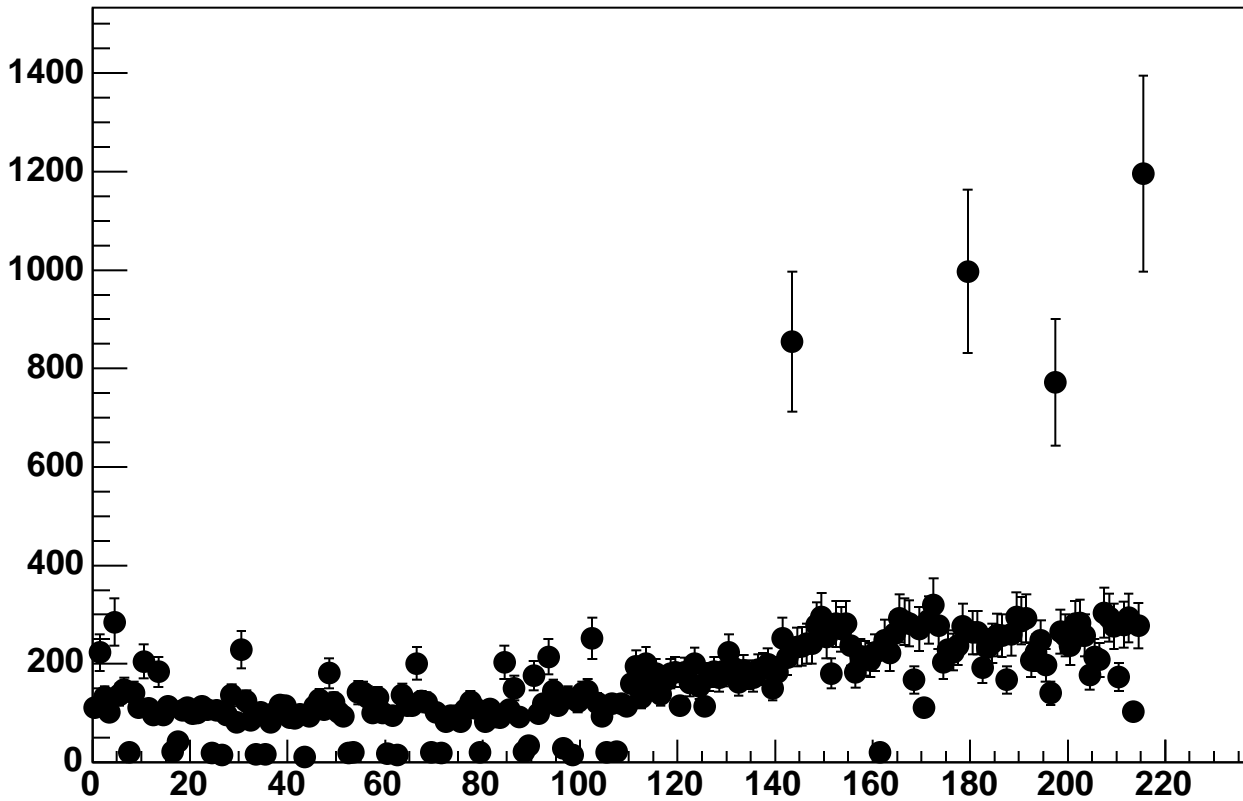
Enable 5, DAC=1600, Hold=225, ADC Noise vs 18\*Chip+Chan



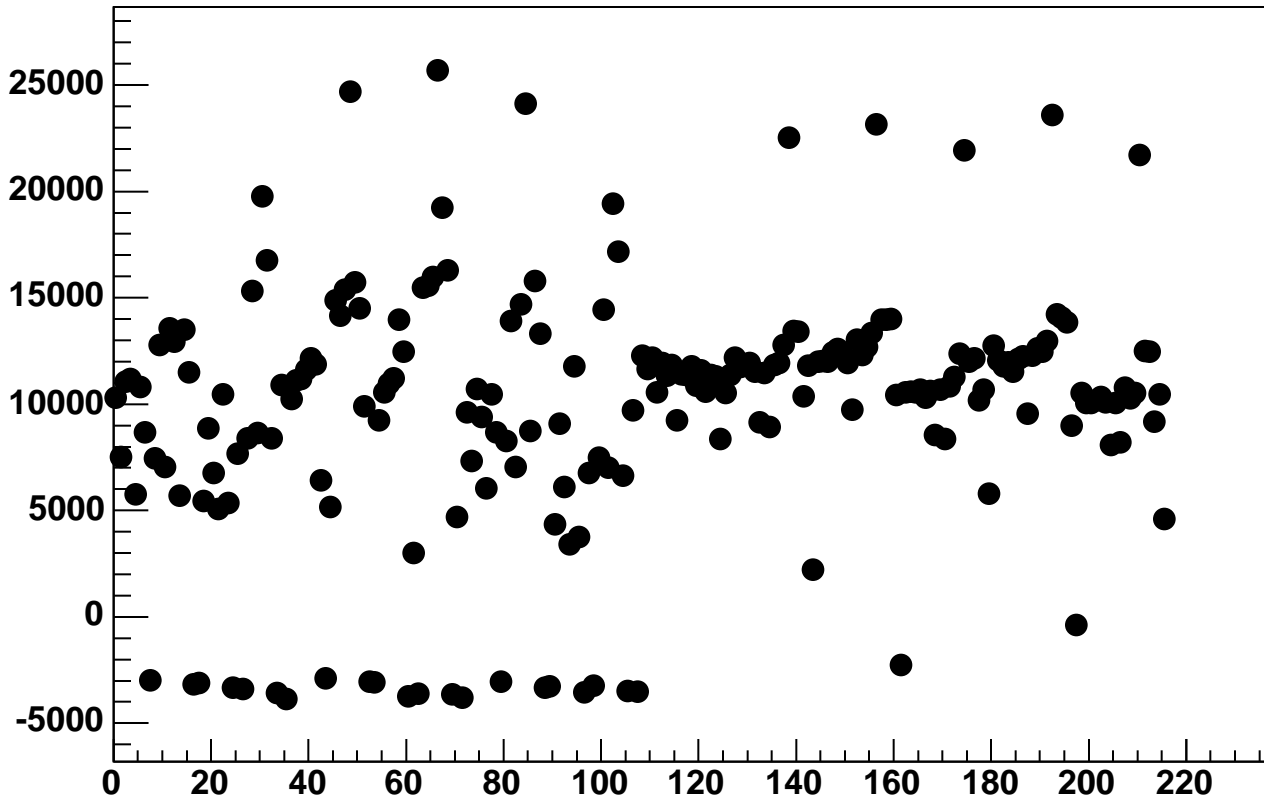
Enable 5, DAC=1600, Hold=230, ADC Mean vs 18\*Chip+Chan



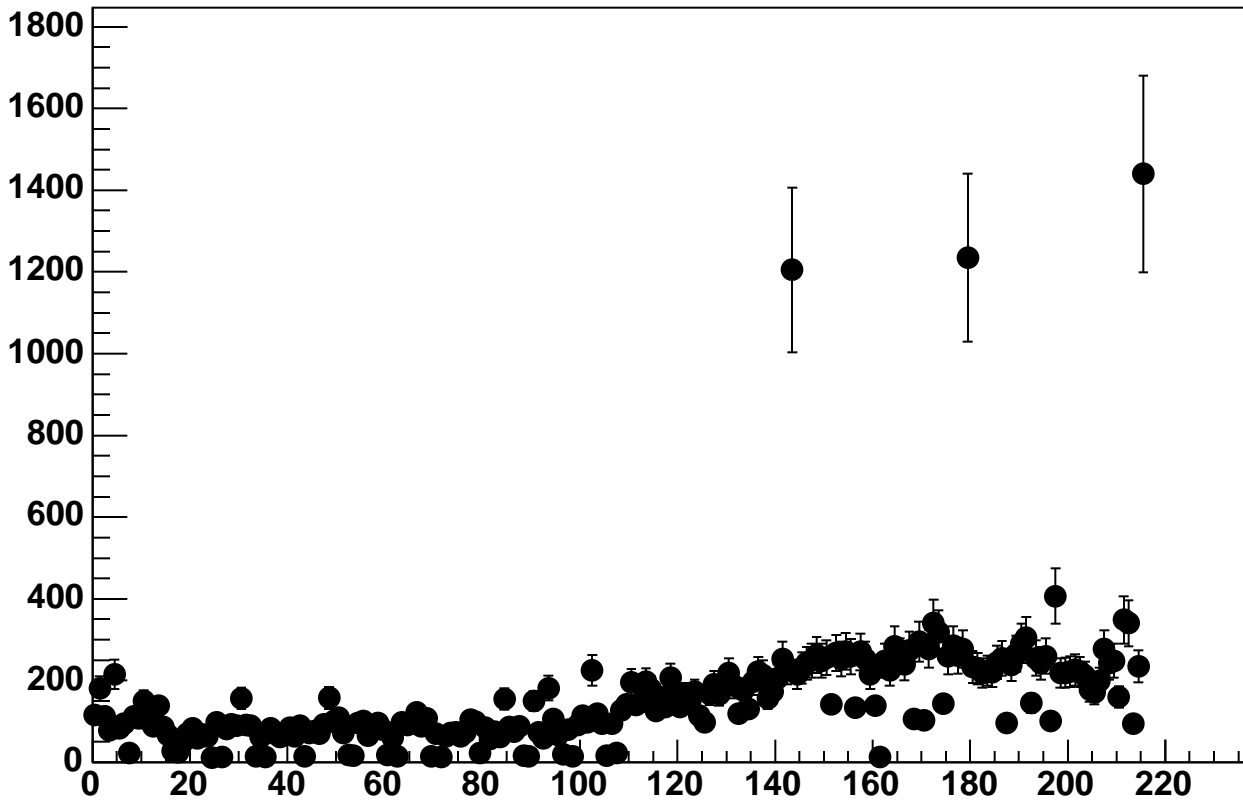
Enable 5, DAC=1600, Hold=230, ADC Noise vs 18\*Chip+Chan



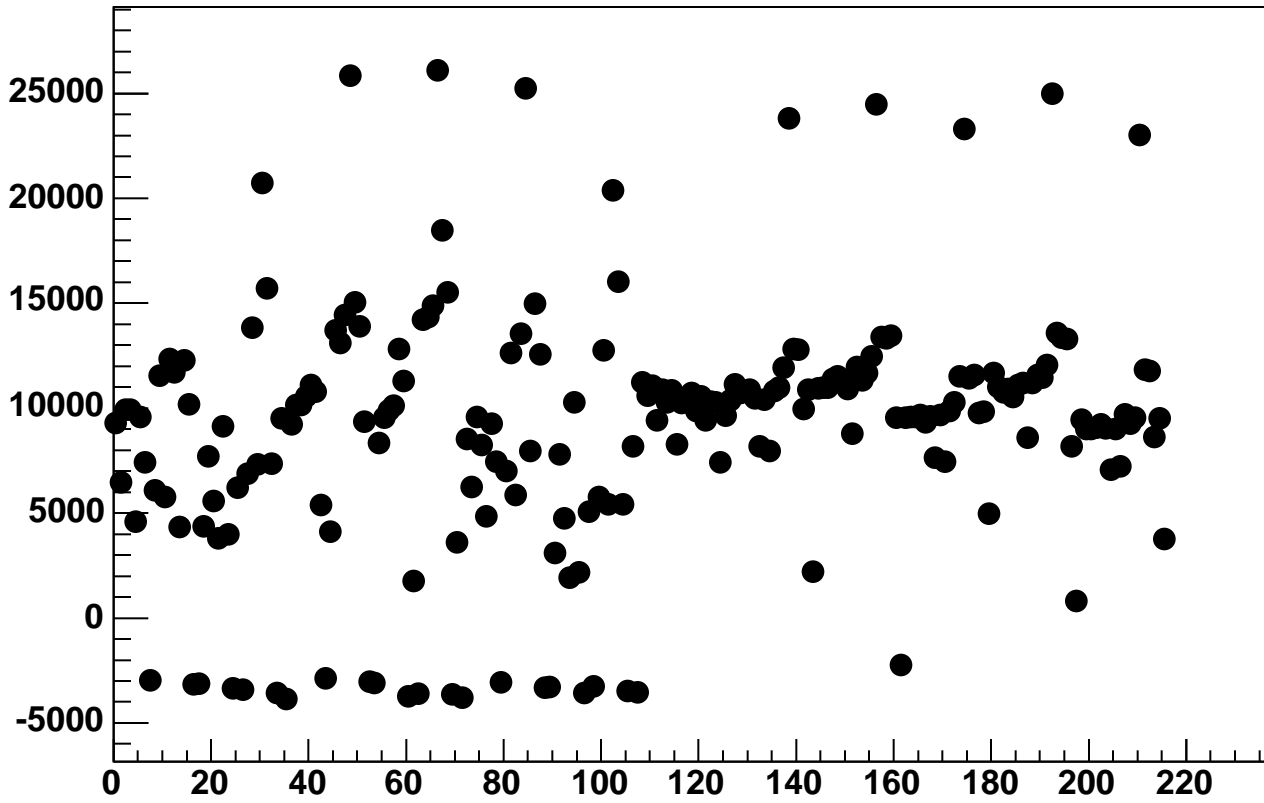
Enable 5, DAC=1600, Hold=235, ADC Mean vs 18\*Chip+Chan



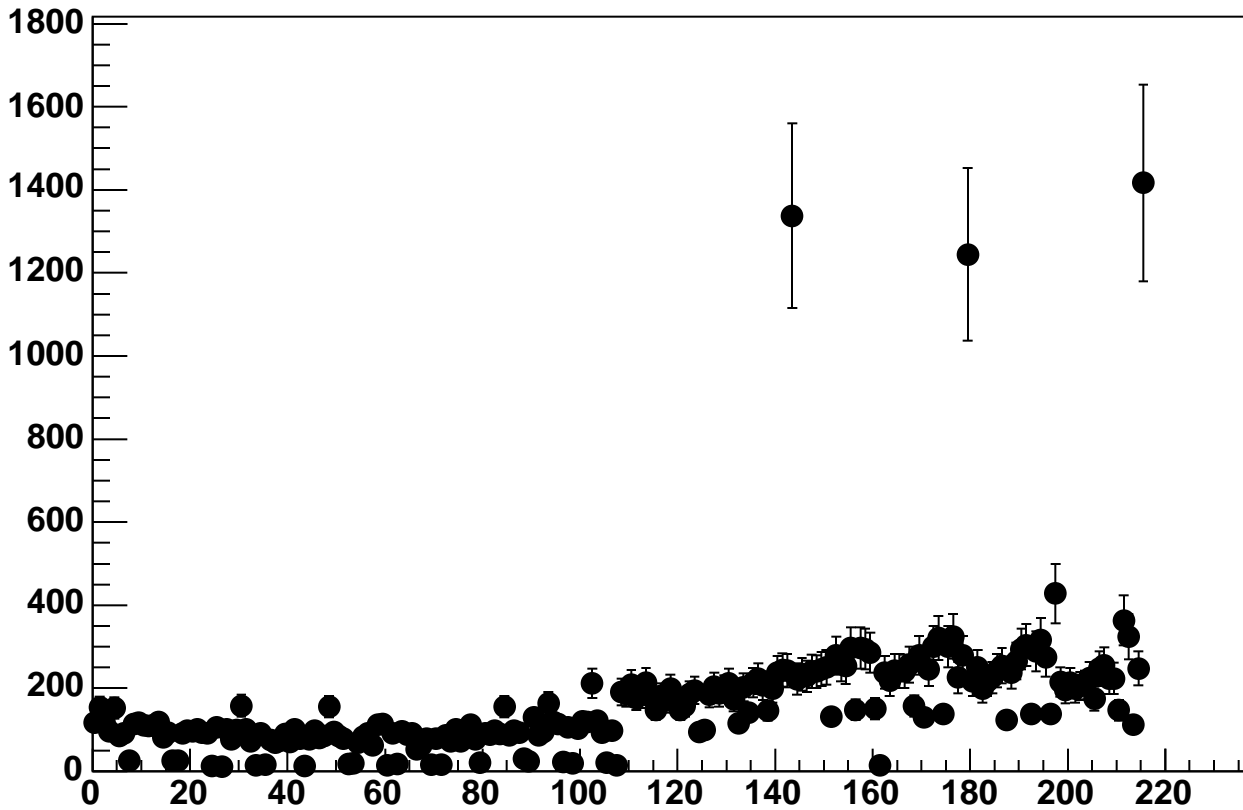
Enable 5, DAC=1600, Hold=235, ADC Noise vs 18\*Chip+Chan



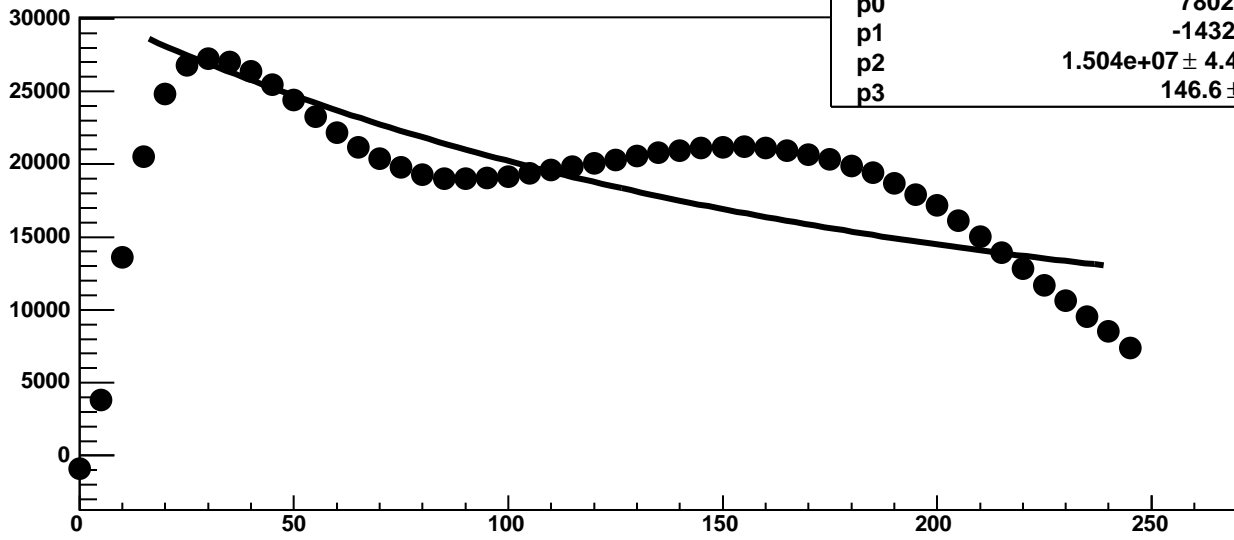
Enable 5, DAC=1600, Hold=240, ADC Mean vs 18\*Chip+Chan



Enable 5, DAC=1600, Hold=240, ADC Noise vs 18\*Chip+Chan

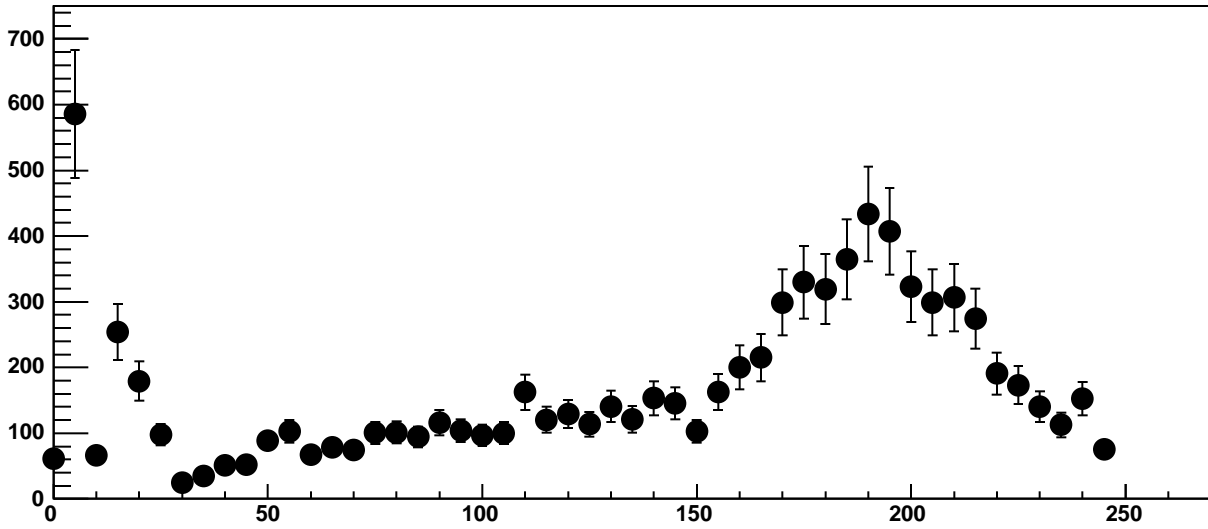


Chip 0, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold

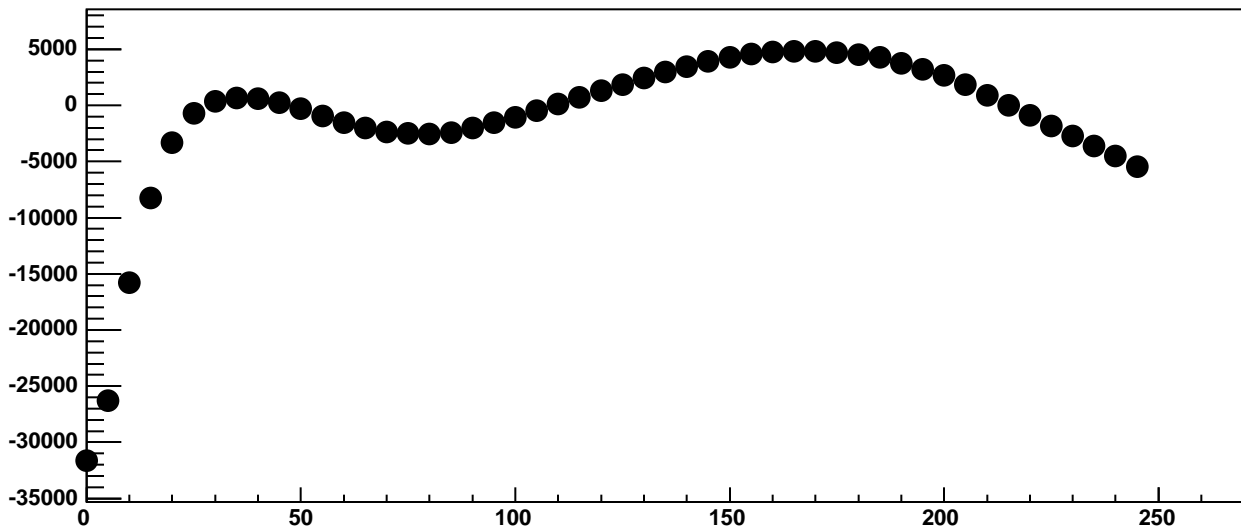


$\chi^2 / \text{ndf}$	3.158e+05 / 42
p0	7802 ± 76.37
p1	-1432 ± 8.353
p2	1.504e+07 ± 4.492e+05
p3	146.6 ± 0.8772

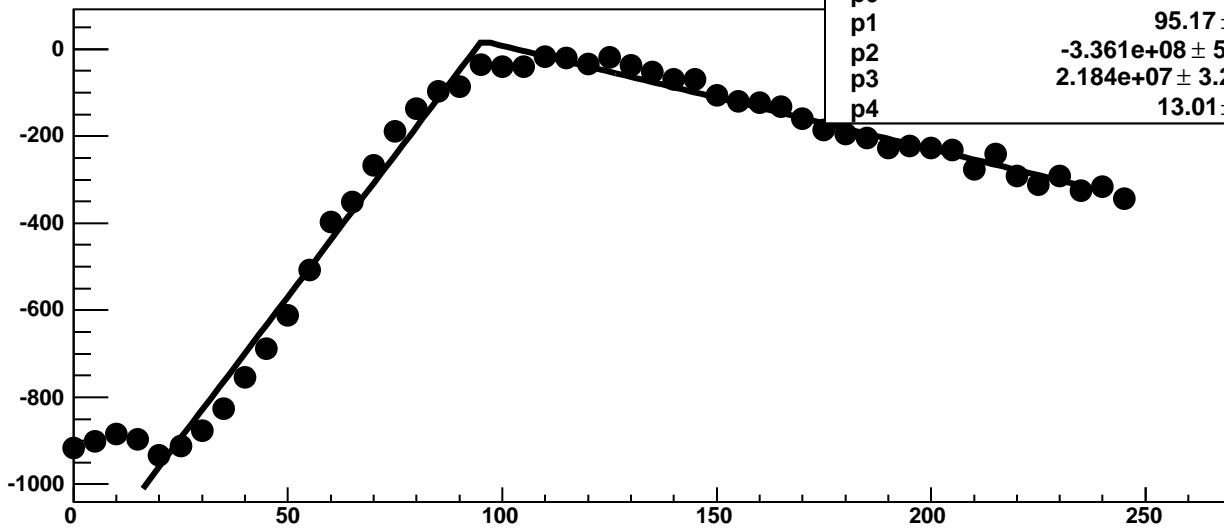
Chip 0, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



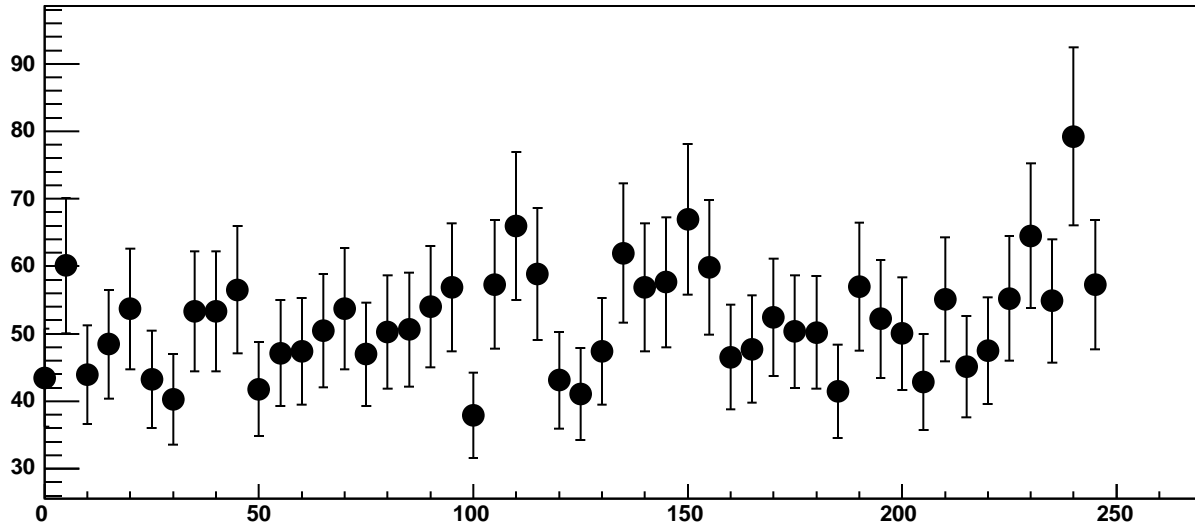
Chip 0, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold



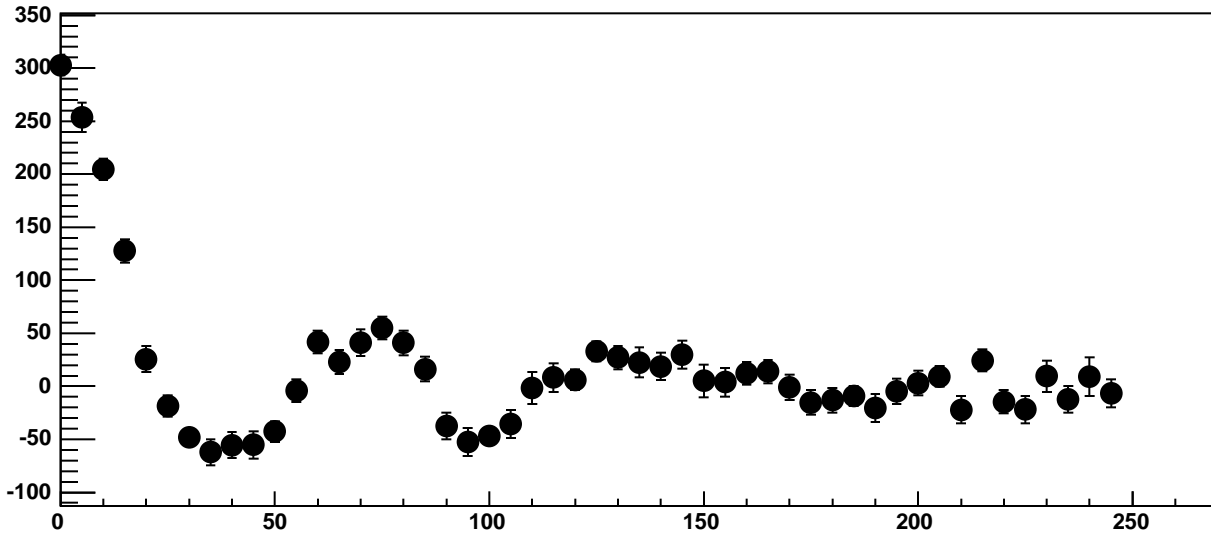
Chip 0, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 0, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

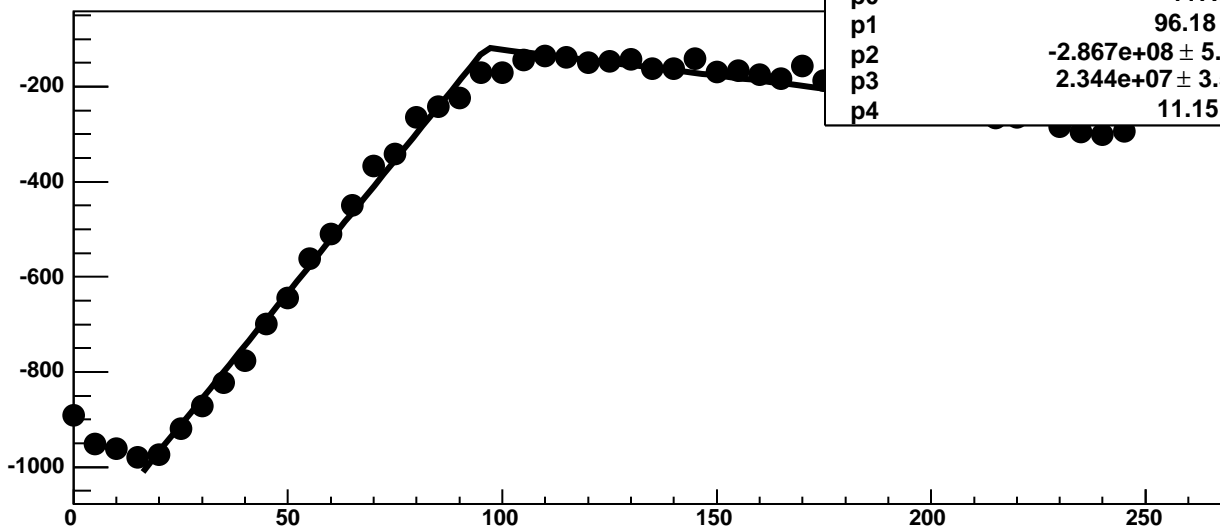


Chip 0, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



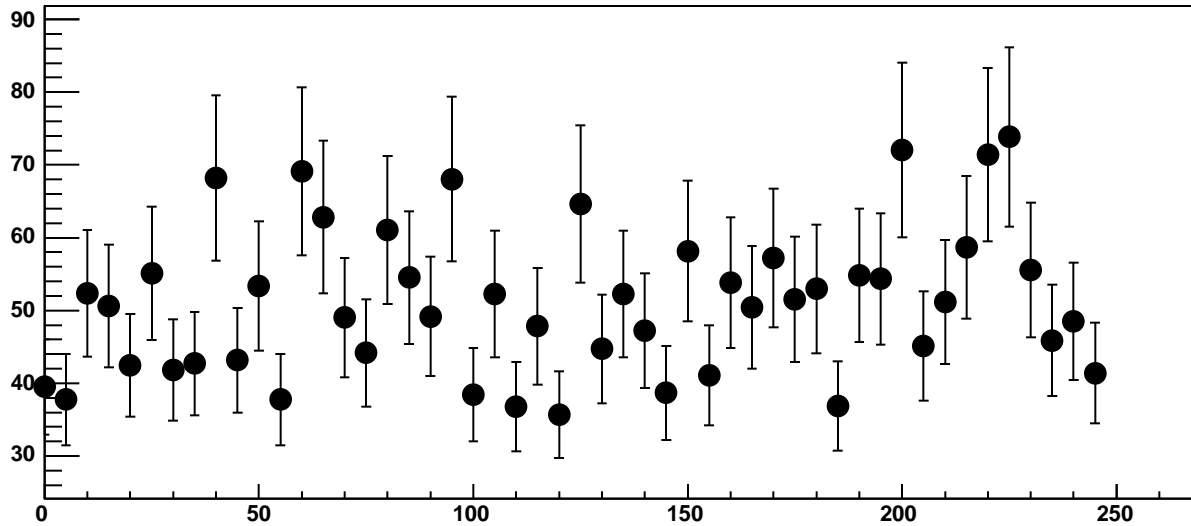


Chip 0, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

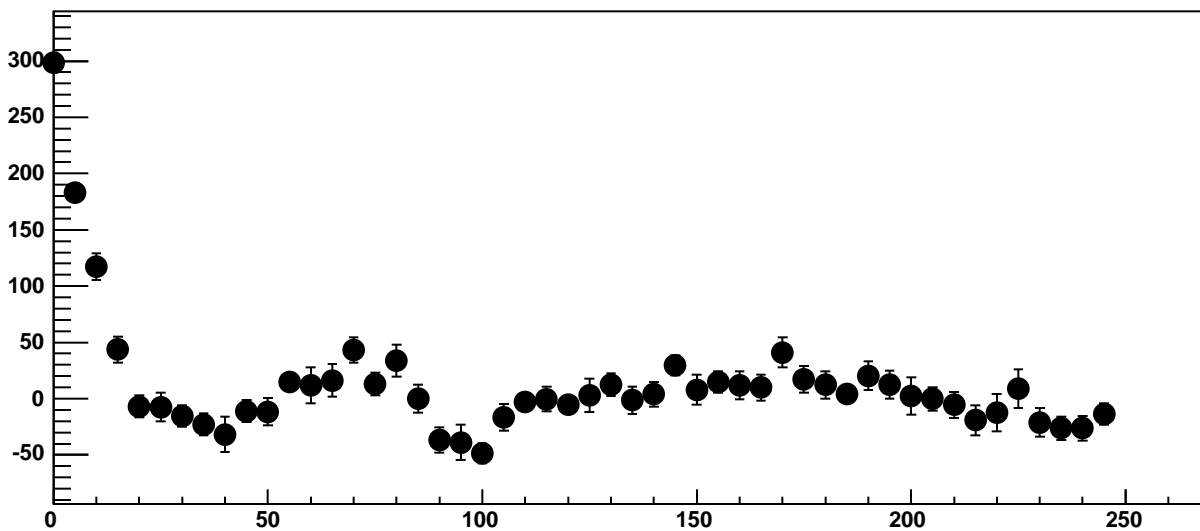


$\chi^2 / \text{ndf}$	157.5 / 41
p0	-117.9 ± 3.561
p1	96.18 ± 0.5648
p2	-2.867e+08 ± 5.613e+06
p3	2.344e+07 ± 3.556e+05
p4	11.15 ± 0.1154

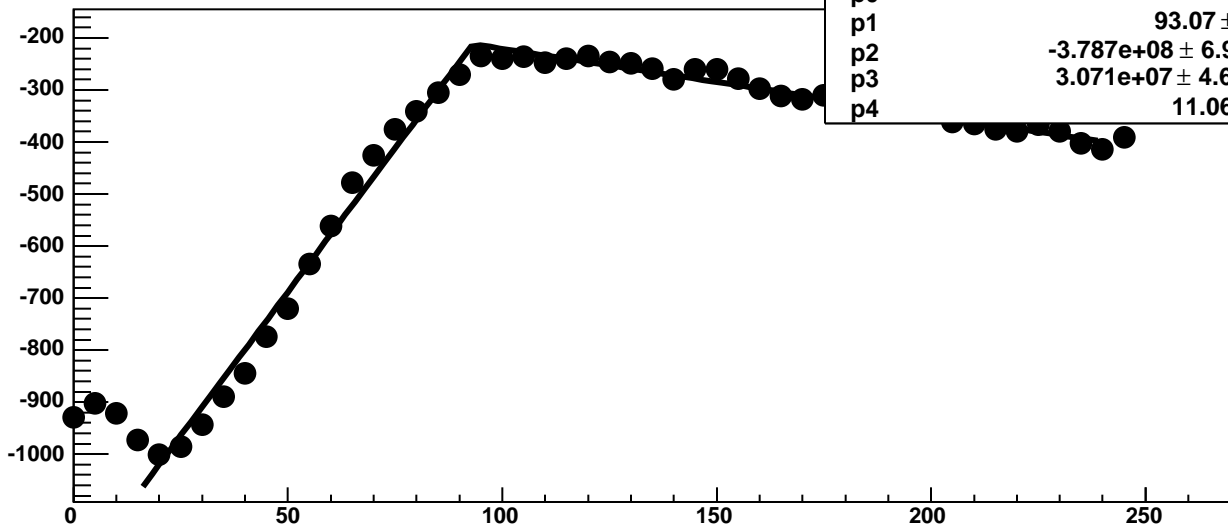
Chip 0, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold

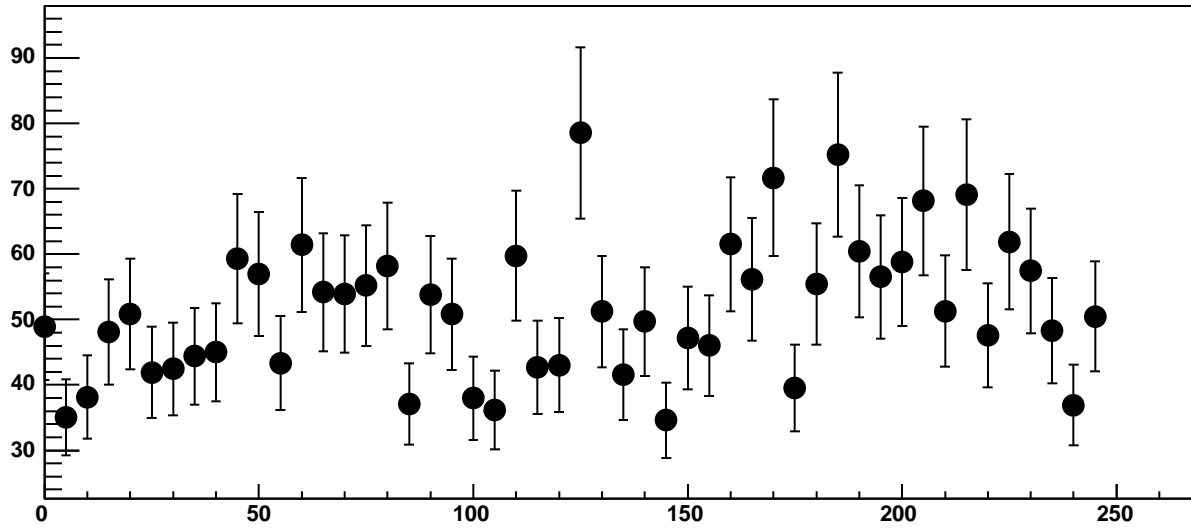


Chip 0, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold

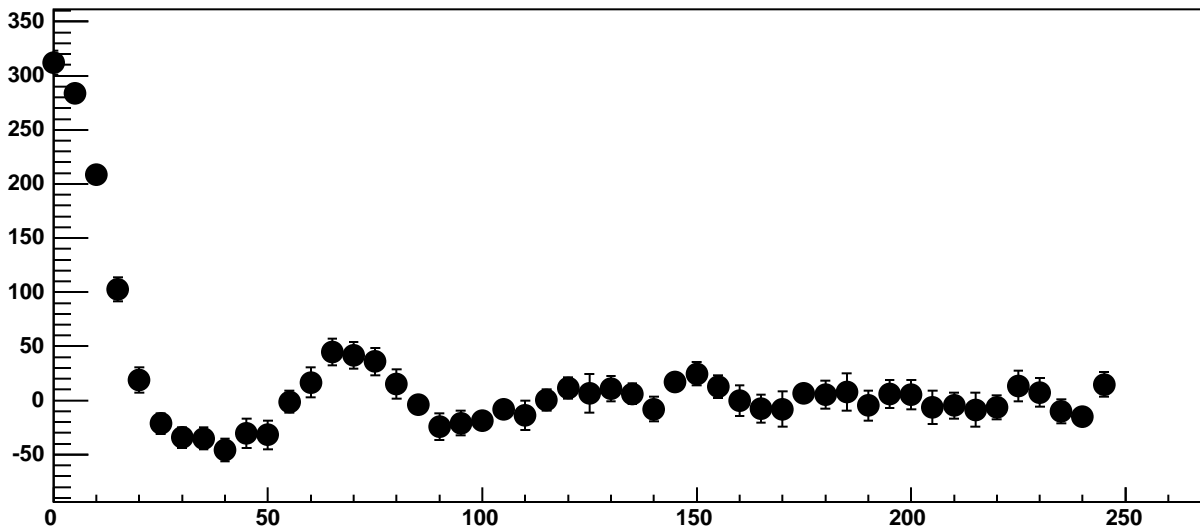


$\chi^2 / \text{ndf}$	220.3 / 41
p0	$-211.9 \pm 3.426$
p1	$93.07 \pm 0.5538$
p2	$-3.787\text{e}+08 \pm 6.986\text{e}+06$
p3	$3.071\text{e}+07 \pm 4.608\text{e}+05$
p4	$11.06 \pm 0.118$

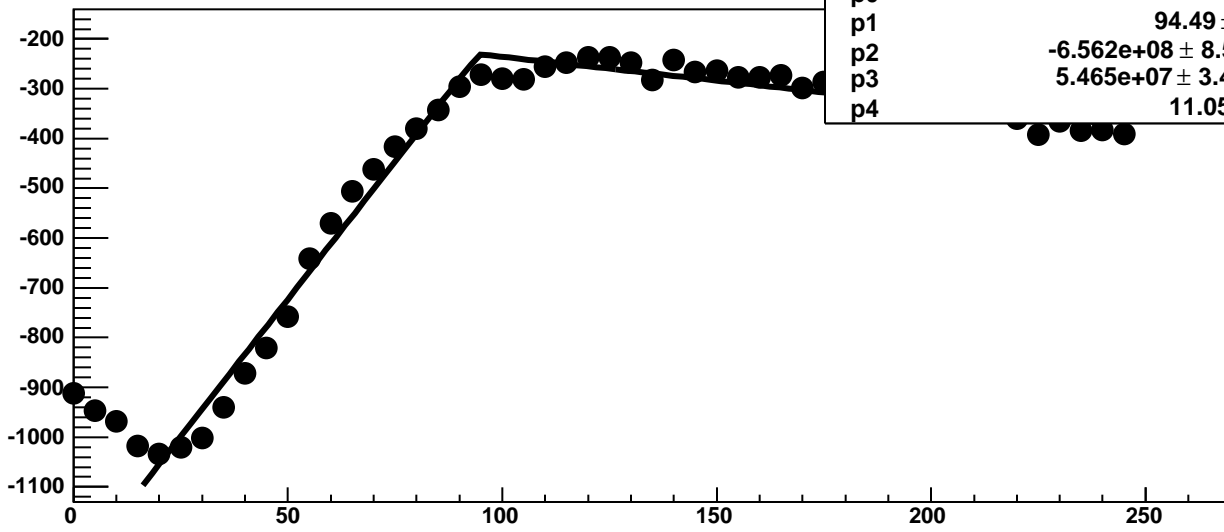
Chip 0, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold

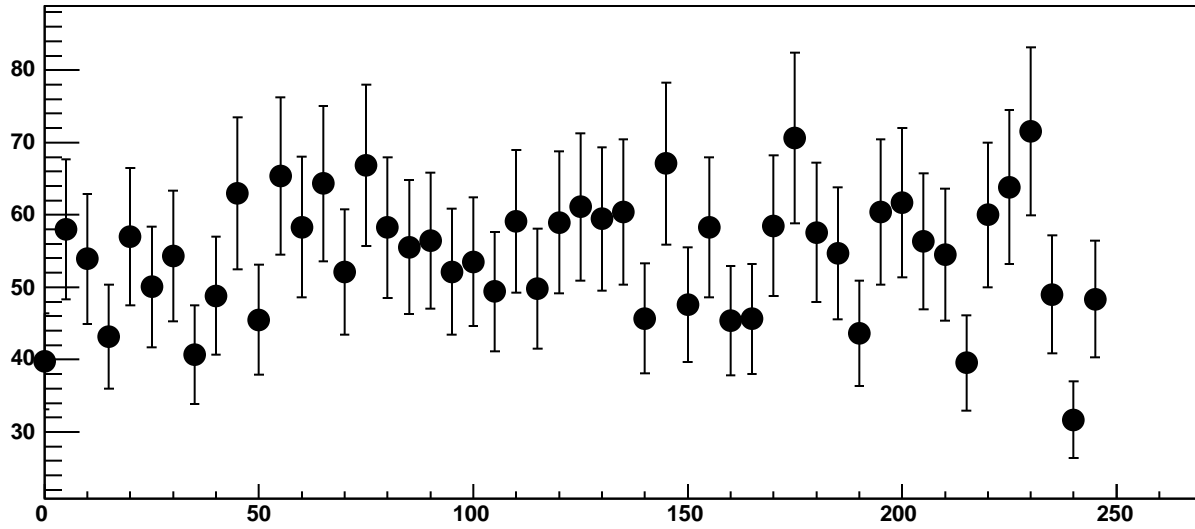


Chip 0, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

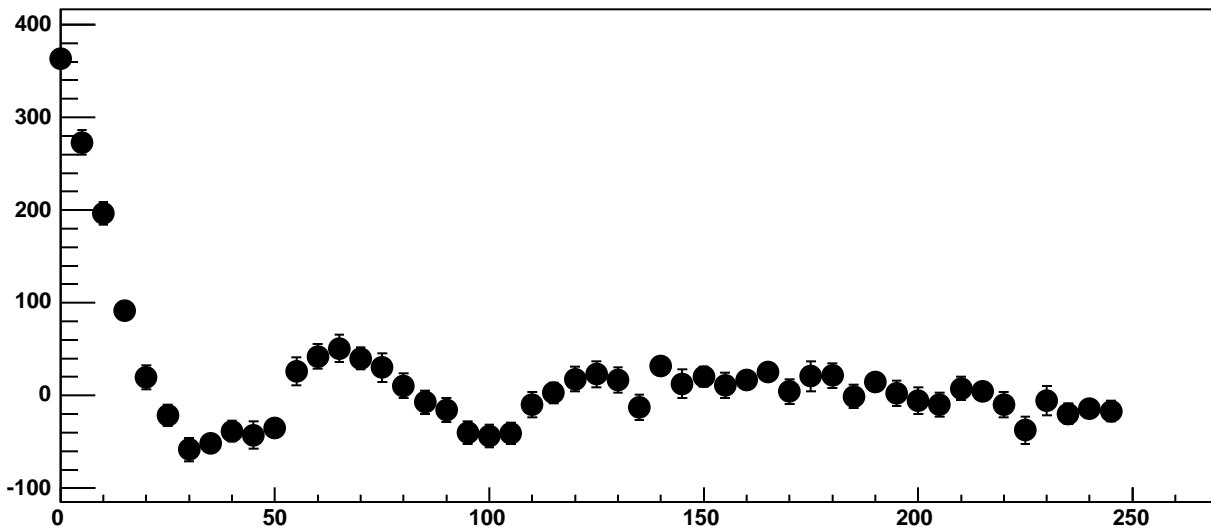


$\chi^2 / \text{ndf}$	306.3 / 41
p0	$-230.6 \pm 4.03$
p1	$94.49 \pm 0.6697$
p2	$-6.562\text{e}+08 \pm 8.529\text{e}+06$
p3	$5.465\text{e}+07 \pm 3.496\text{e}+05$
p4	$11.05 \pm 0.132$

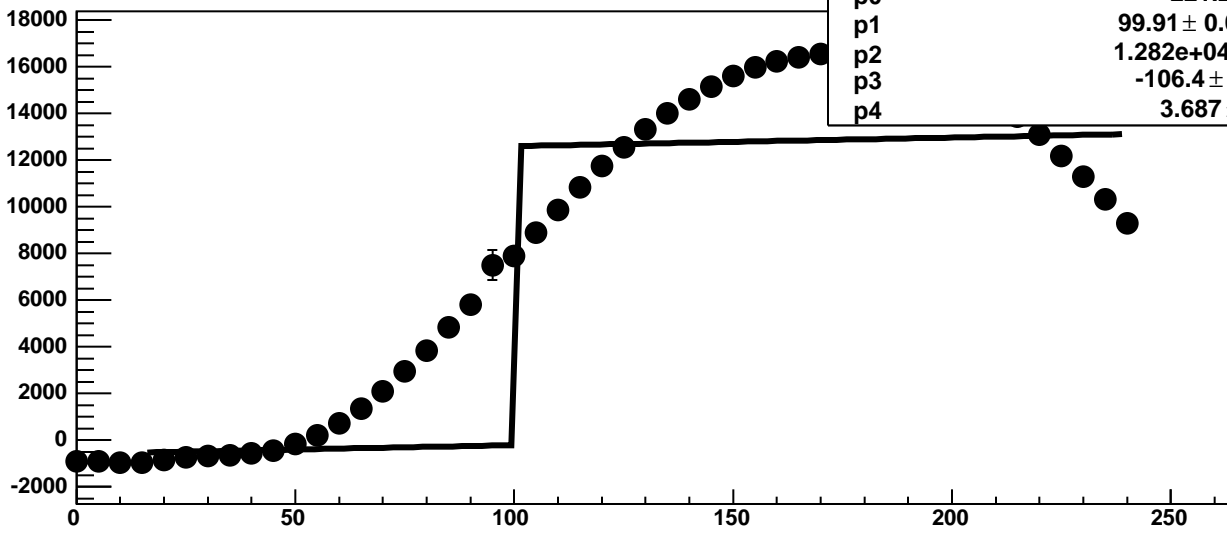
Chip 0, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

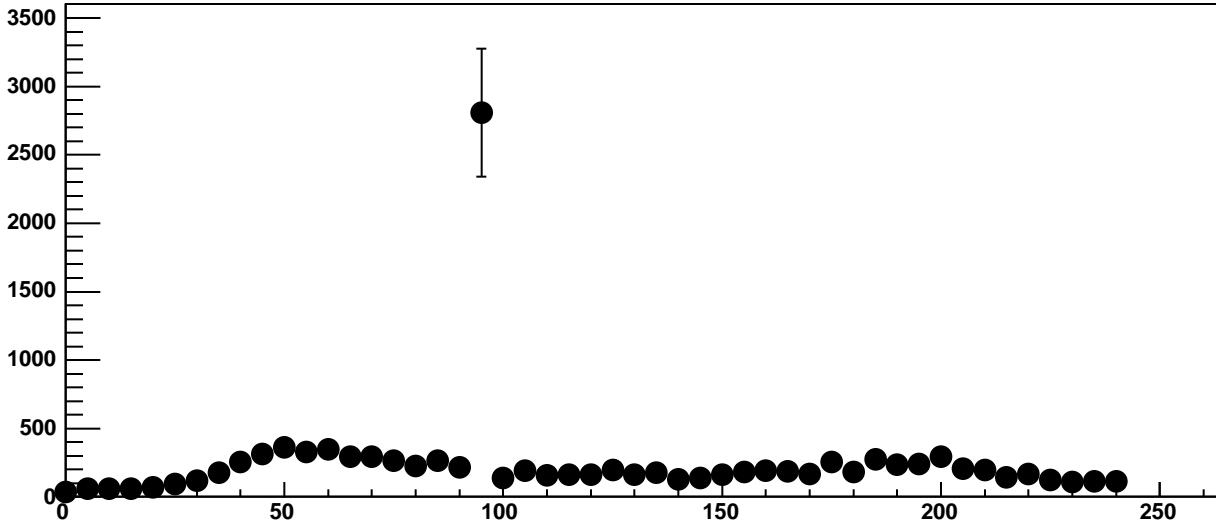


Chip 0, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

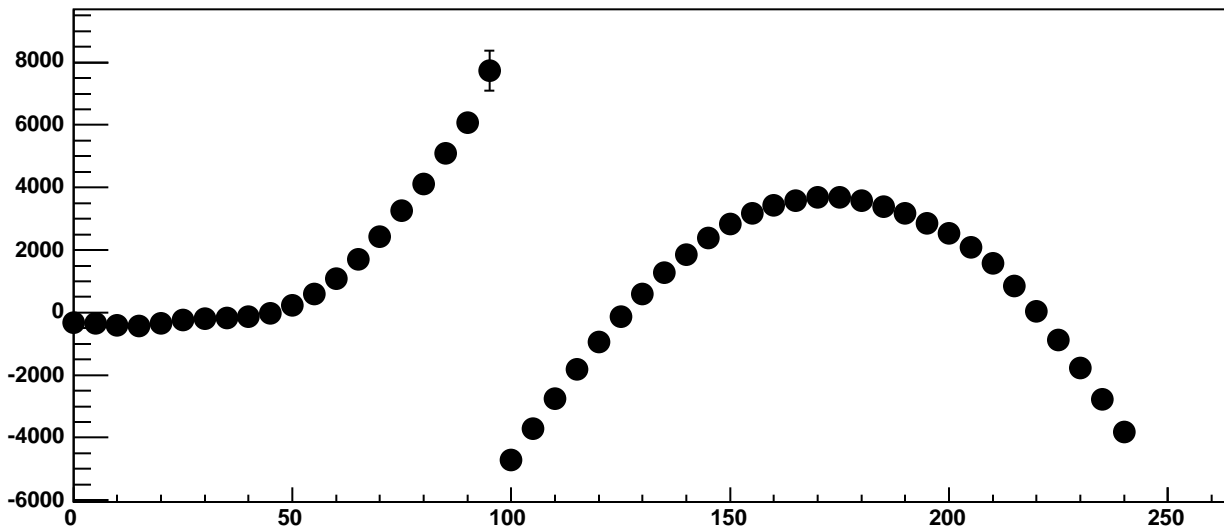


$\chi^2 / \text{ndf}$	1.808e+05 / 41
p0	-221.2 ± 7.965
p1	99.91 ± 0.0005962
p2	1.282e+04 ± 21.88
p3	-106.4 ± 0.04089
p4	3.687 ± 0.1291

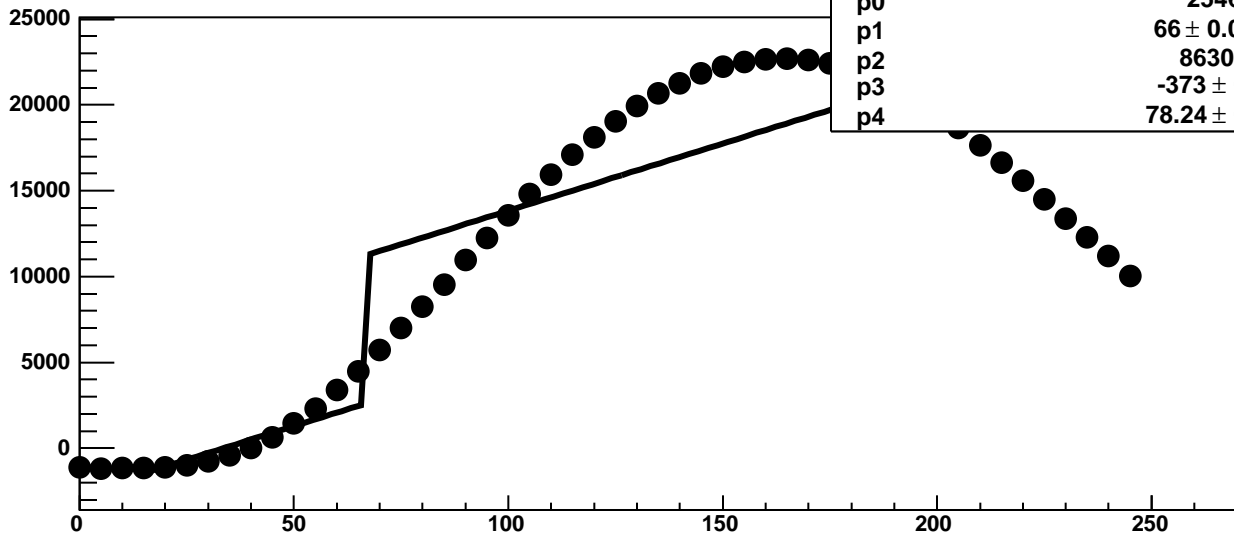
Chip 0, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

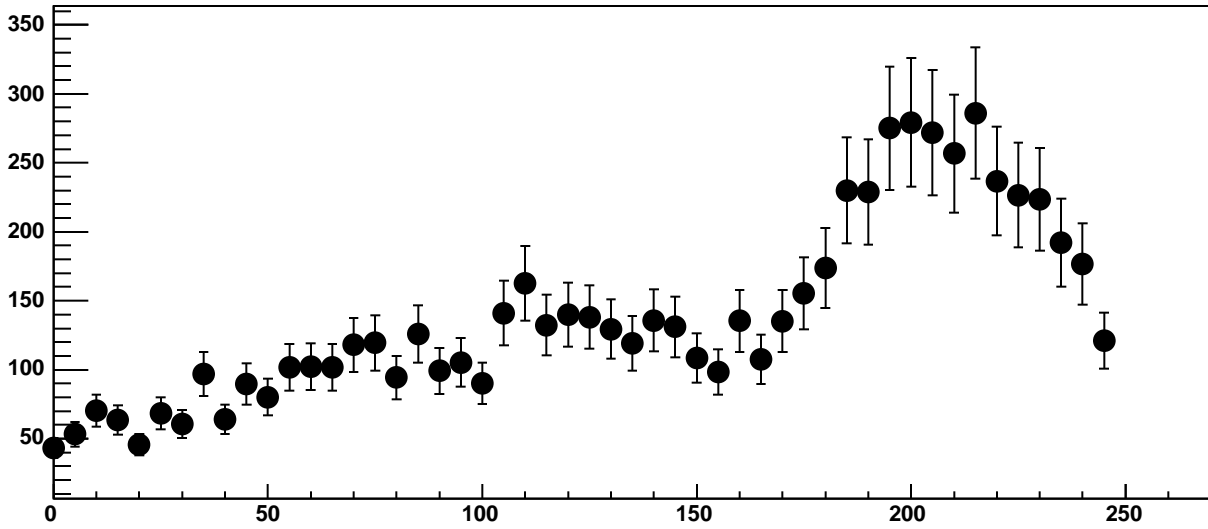


Chip 0, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

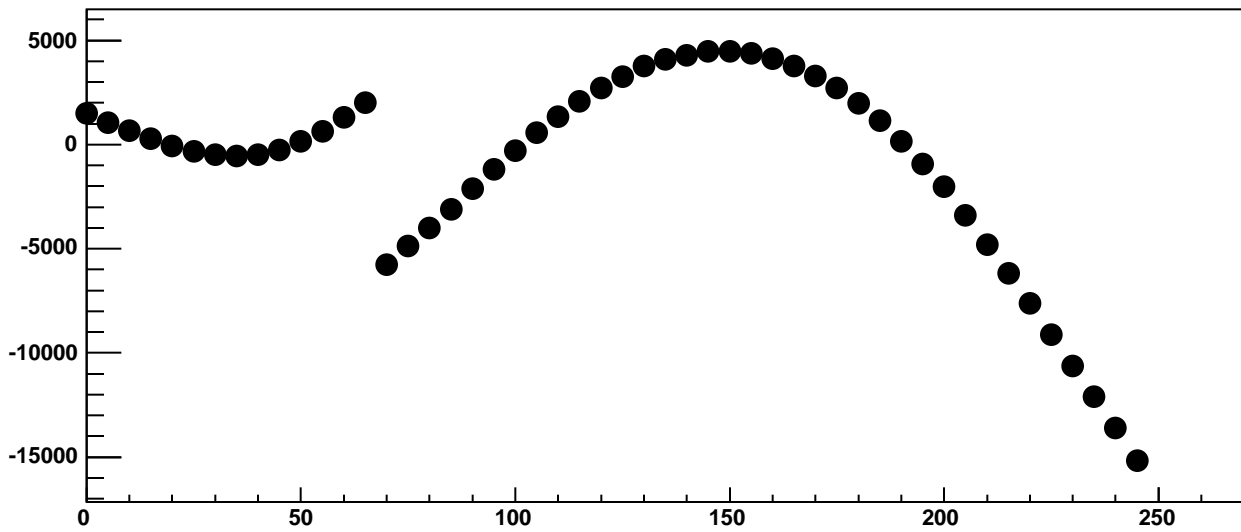


$\chi^2 / \text{ndf}$	6.86e+05 / 41
p0	2546 ± 5.66
p1	66 ± 0.0001224
p2	8630 ± 6.247
p3	-373 ± 0.04282
p4	78.24 ± 0.08908

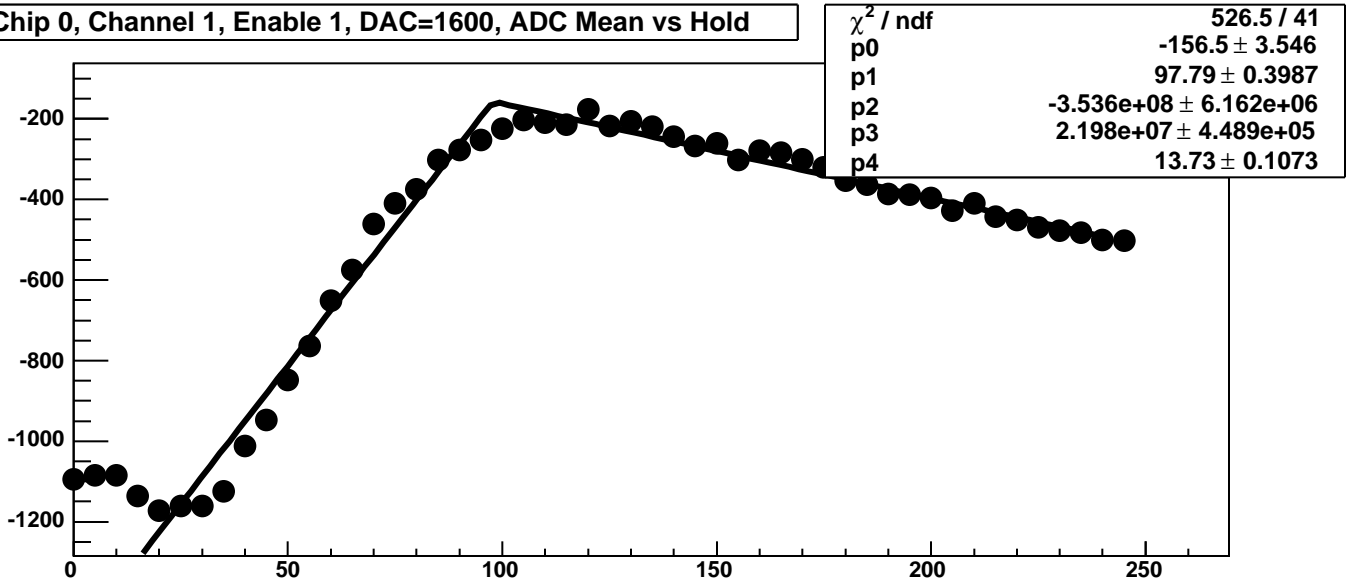
Chip 0, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



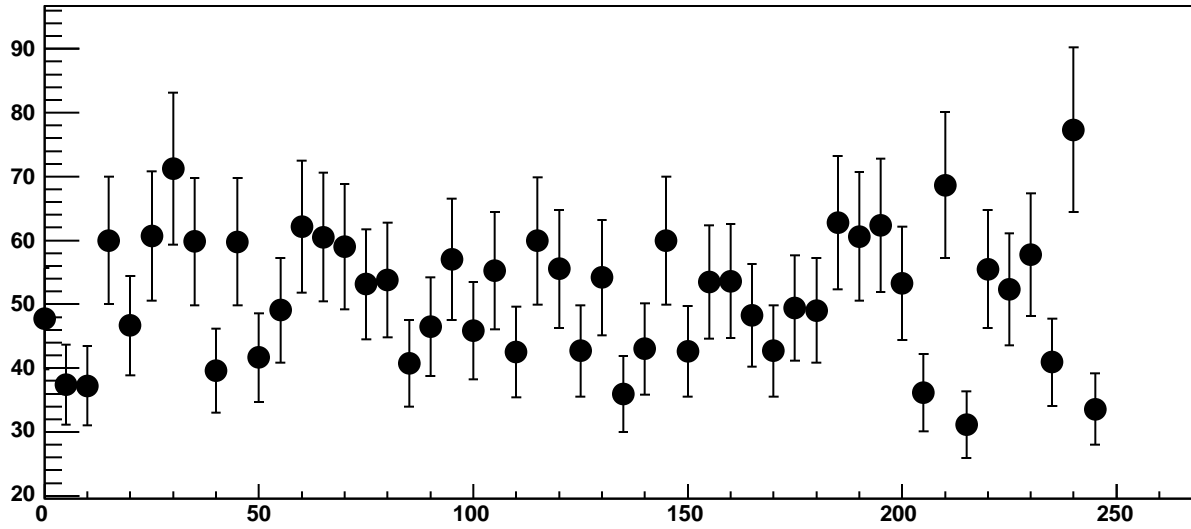
Chip 0, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold



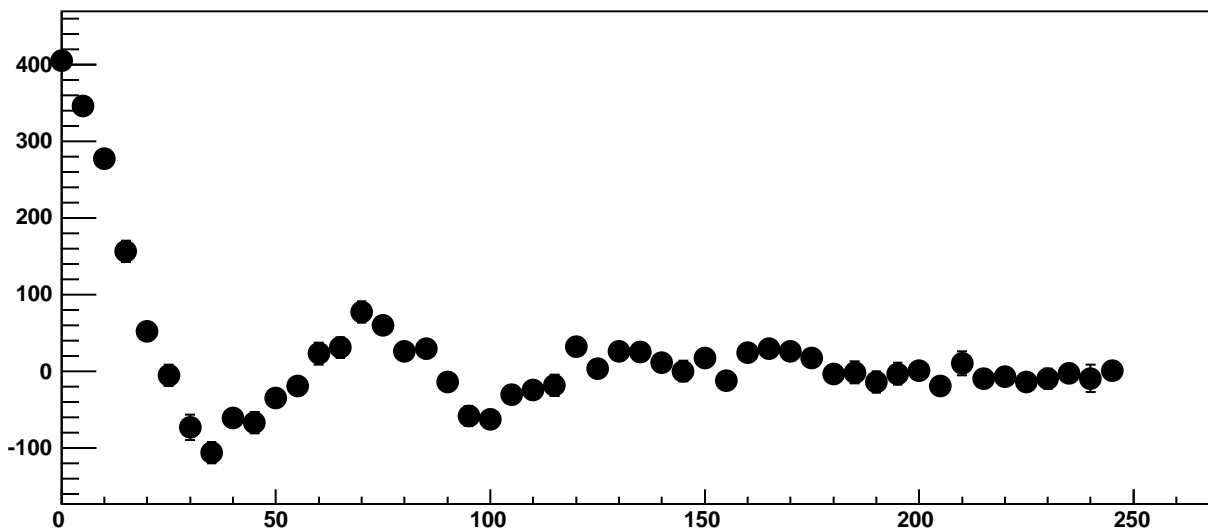
Chip 0, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold



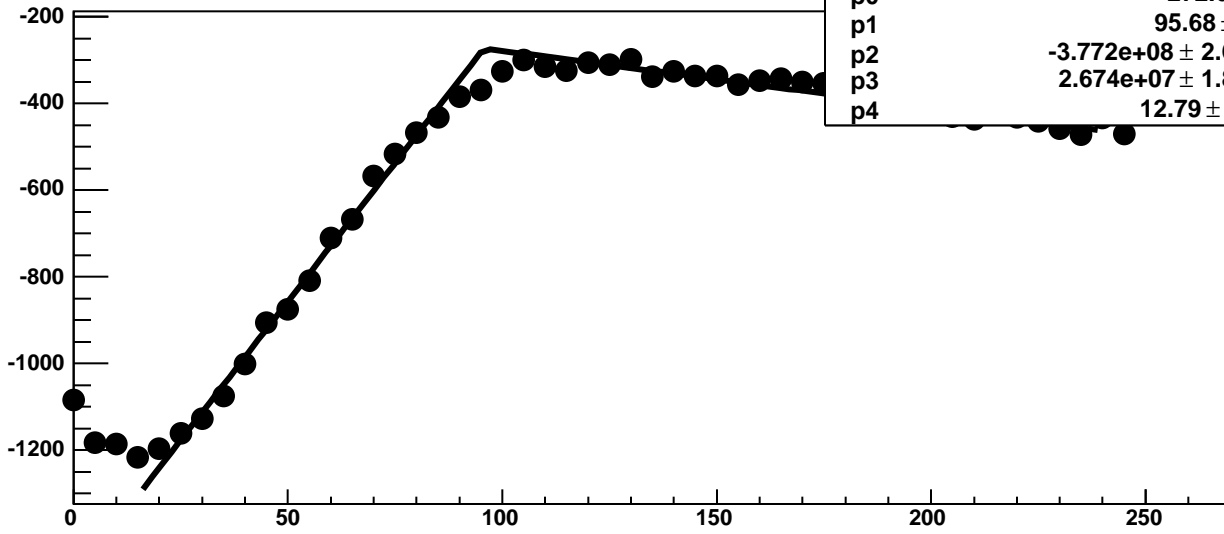
Chip 0, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

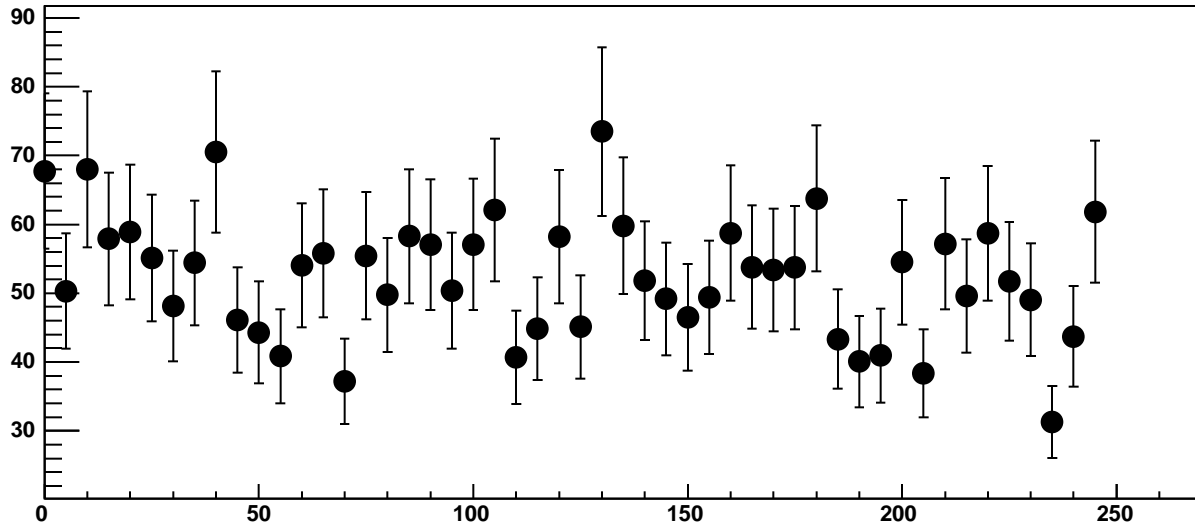


Chip 0, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

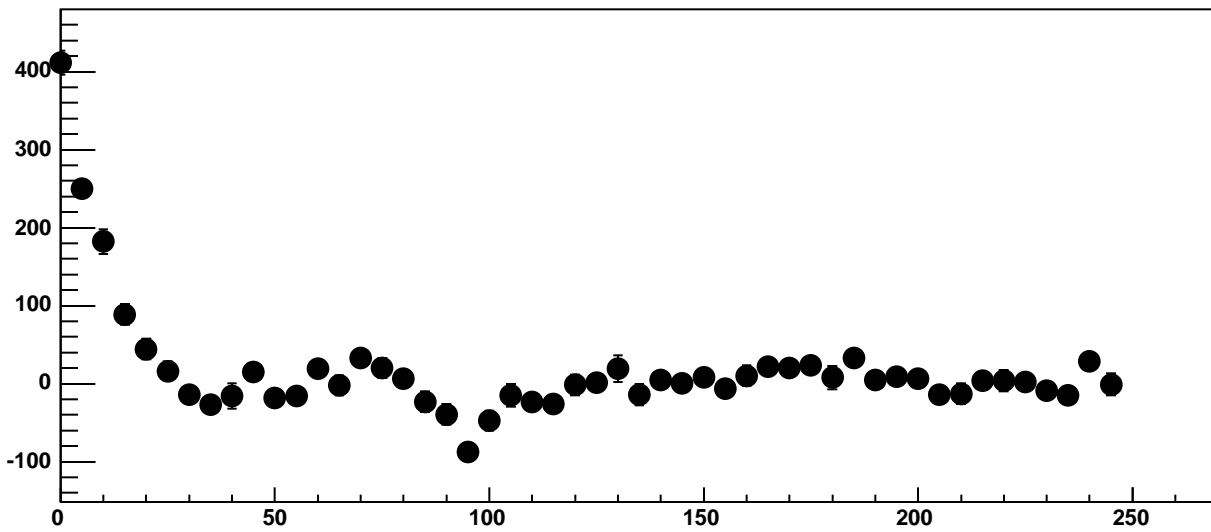


$\chi^2 / \text{ndf}$	232.3 / 41
p0	$-272.6 \pm 3.022$
p1	$95.68 \pm 0.3753$
p2	$-3.772\text{e}+08 \pm 2.603\text{e}+09$
p3	$2.674\text{e}+07 \pm 1.845\text{e}+08$
p4	$12.79 \pm 0.03078$

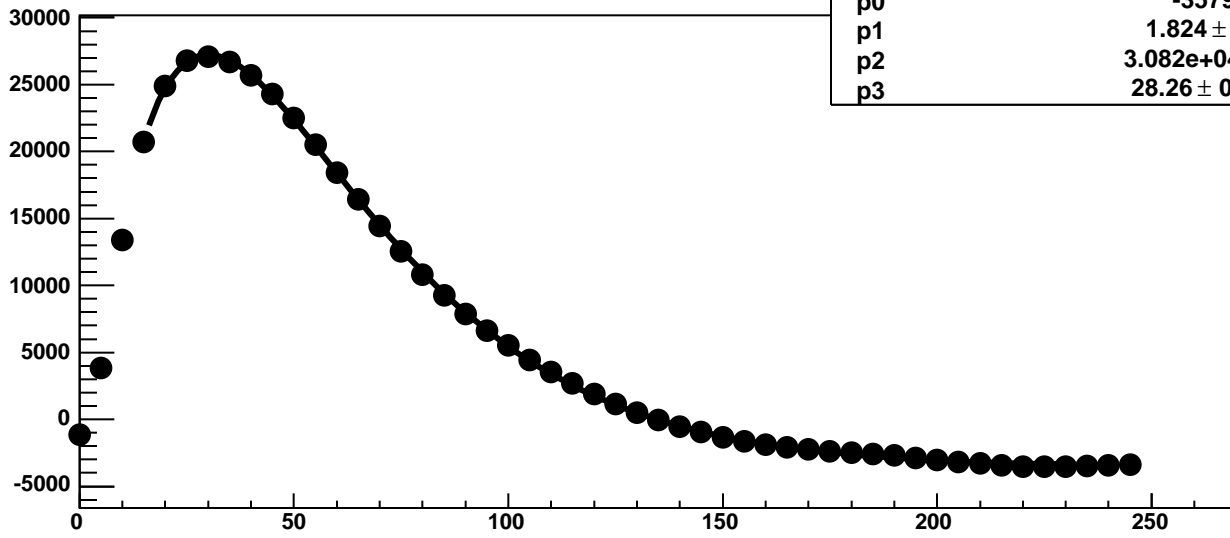
Chip 0, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

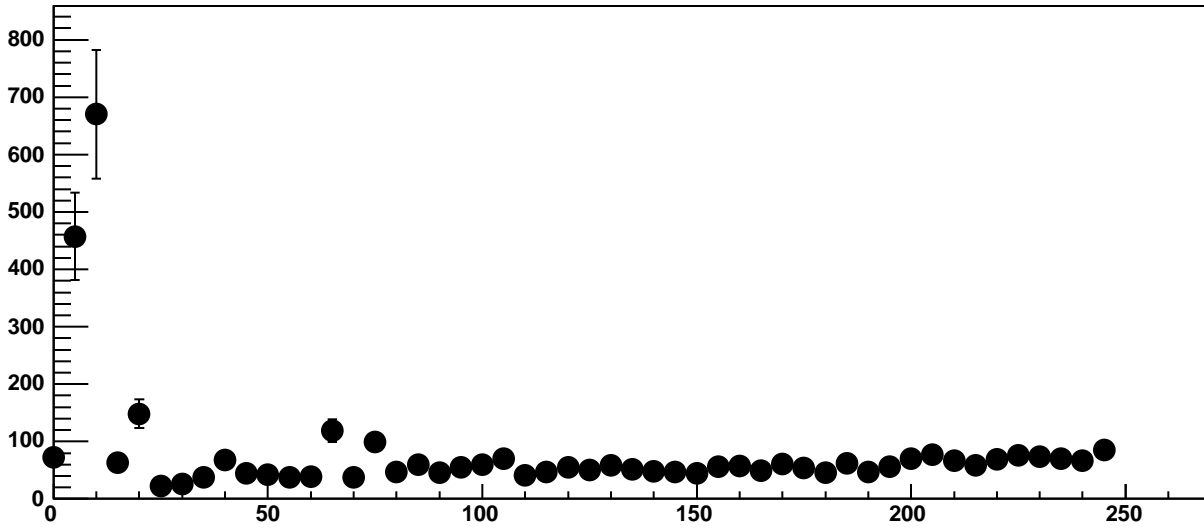


Chip 0, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

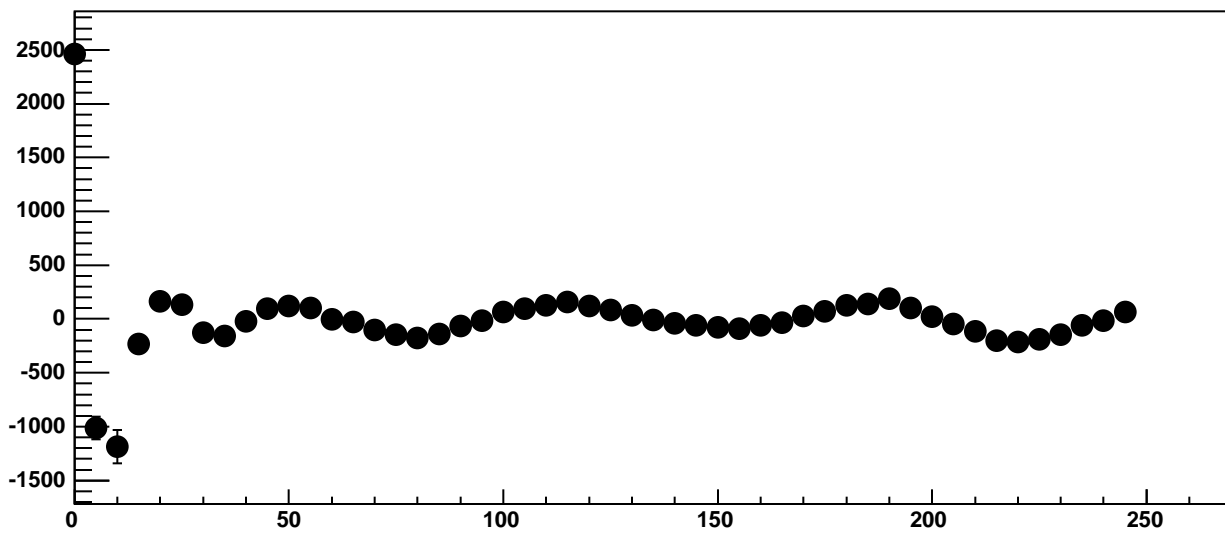


$\chi^2 / \text{ndf}$	4853 / 42
p0	$-3579 \pm 3.753$
p1	$1.824 \pm 0.01562$
p2	$3.082e+04 \pm 4.37$
p3	$28.26 \pm 0.009736$

Chip 0, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

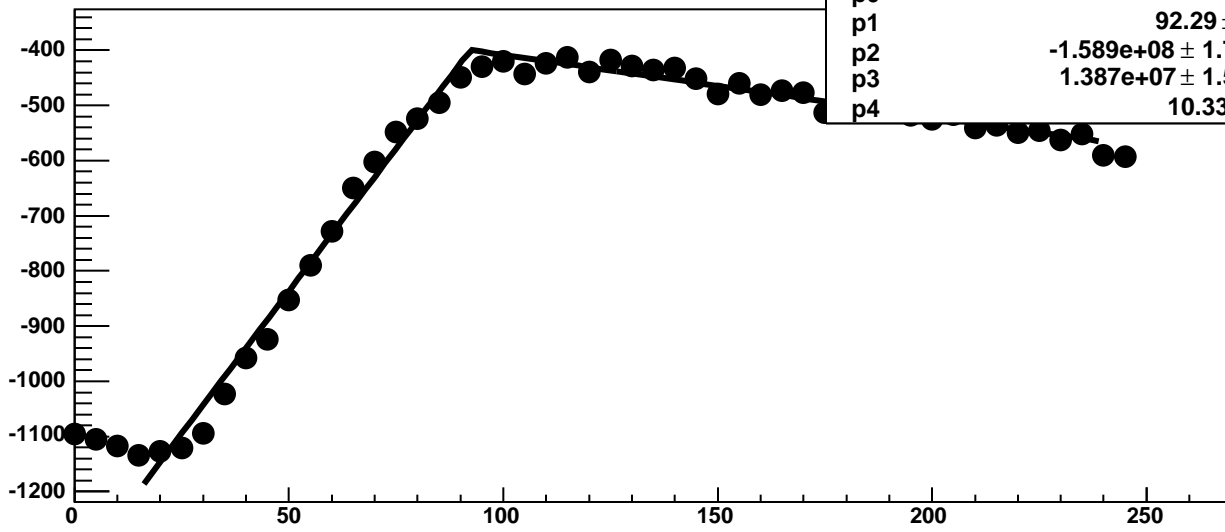


Chip 0, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold



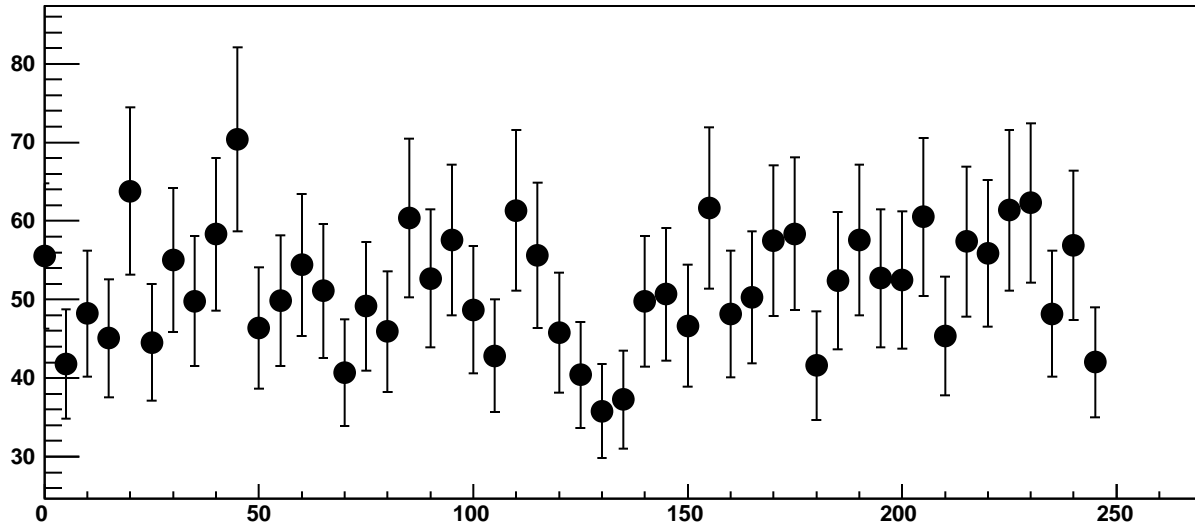


Chip 0, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

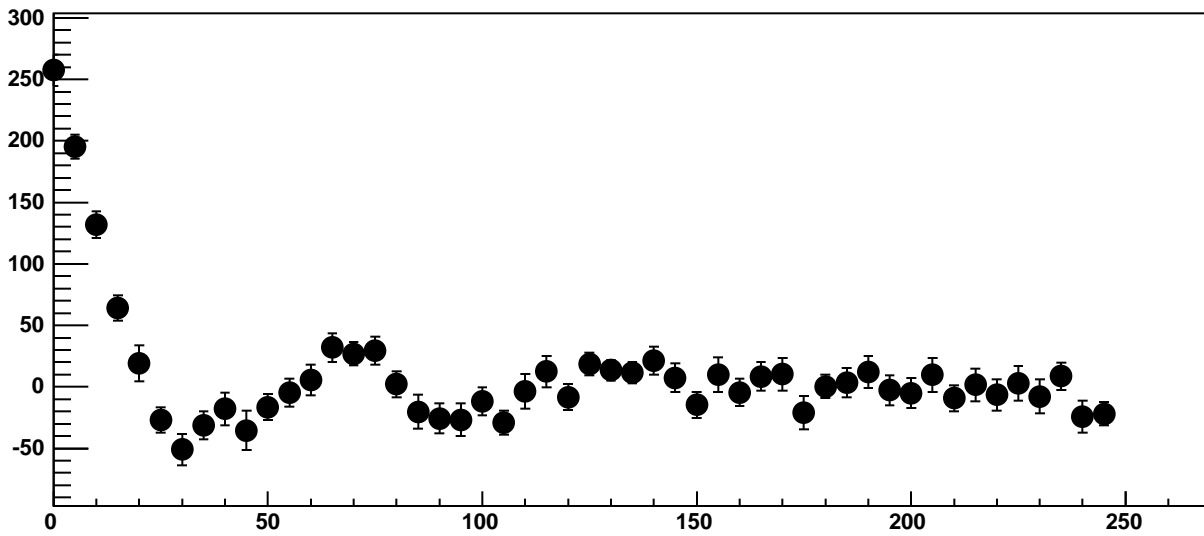


$\chi^2 / \text{ndf}$	150.8 / 41
p0	$-399.6 \pm 3.71$
p1	$92.29 \pm 0.6153$
p2	$-1.589\text{e}+08 \pm 1.781\text{e}+07$
p3	$1.387\text{e}+07 \pm 1.548\text{e}+06$
p4	$10.33 \pm 0.126$

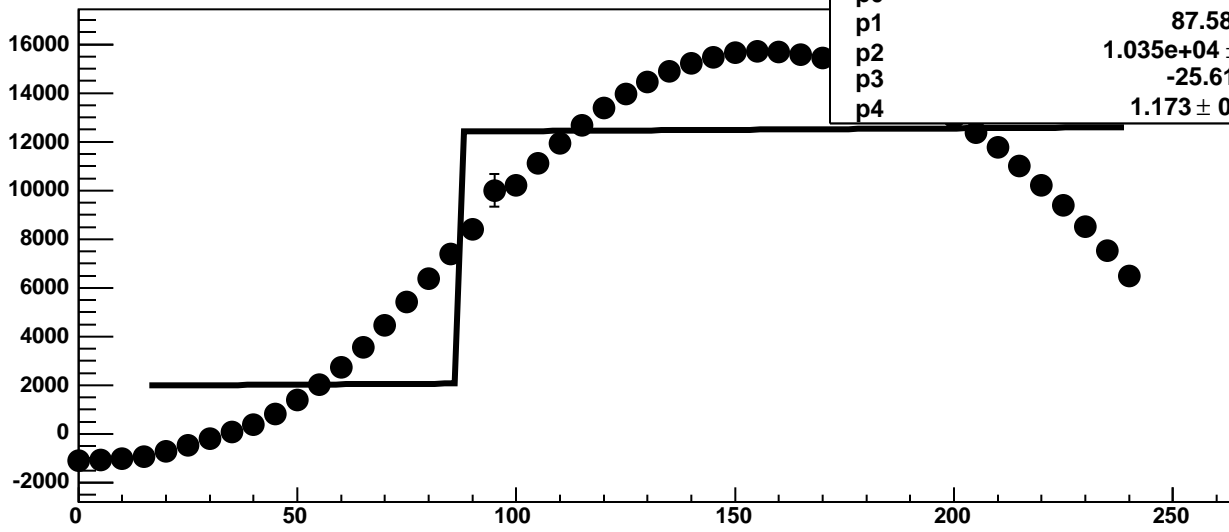
Chip 0, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

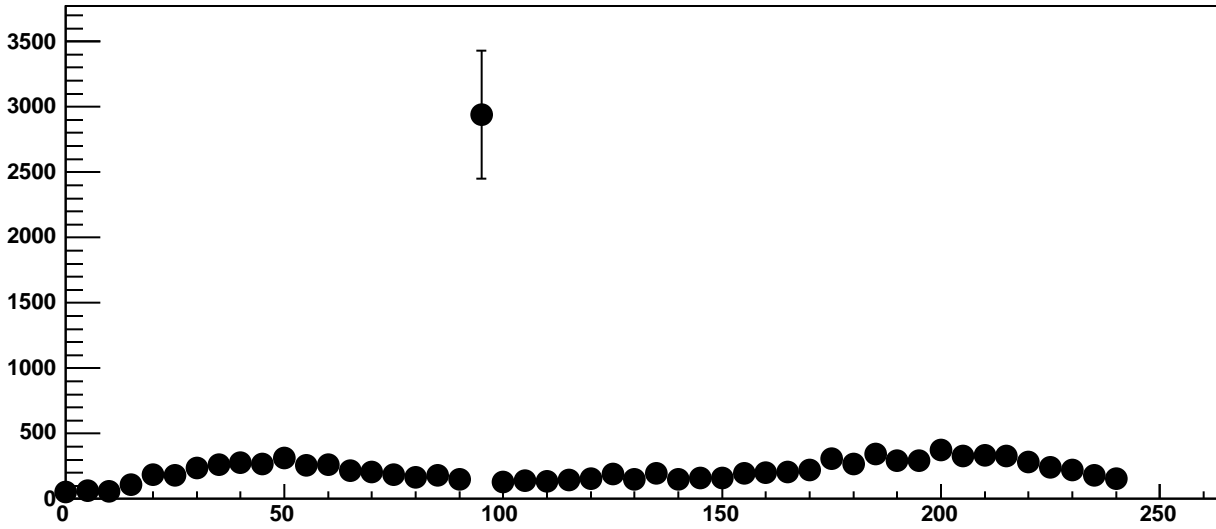


Chip 0, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

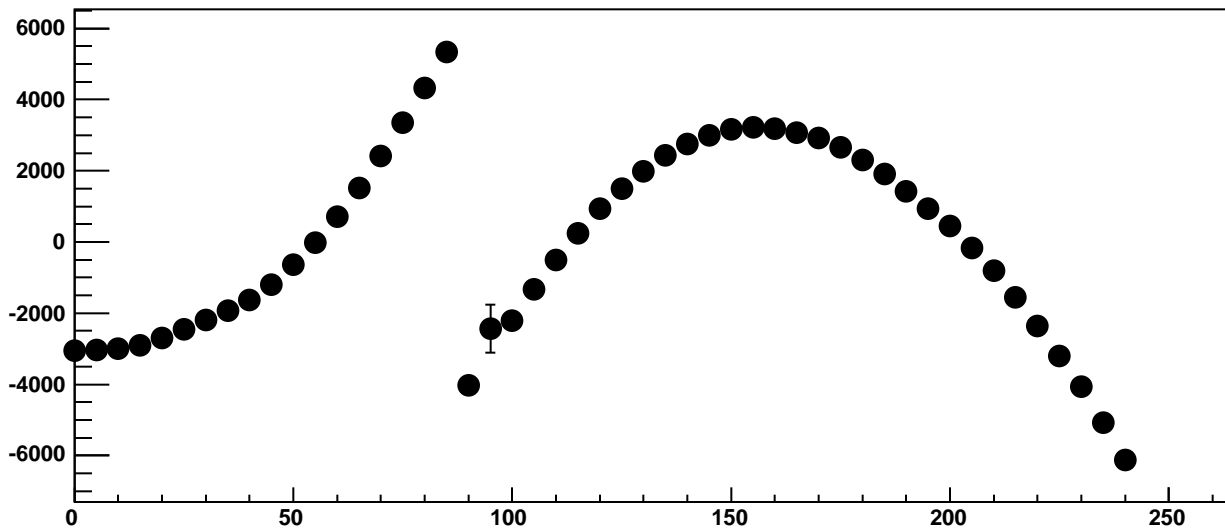


$\chi^2 / \text{ndf}$	1.918e+05 / 41
p0	2069 ± 0.1093
p1	87.58 ± 2.076
p2	1.035e+04 ± 0.1322
p3	-25.61 ± 2.082
p4	1.173 ± 0.001574

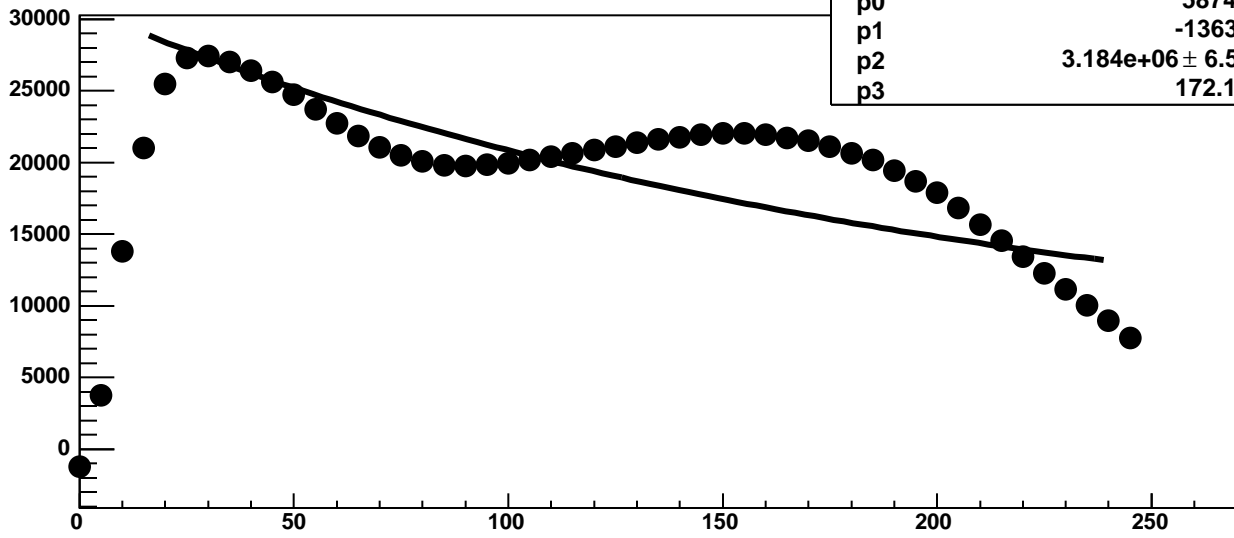
Chip 0, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

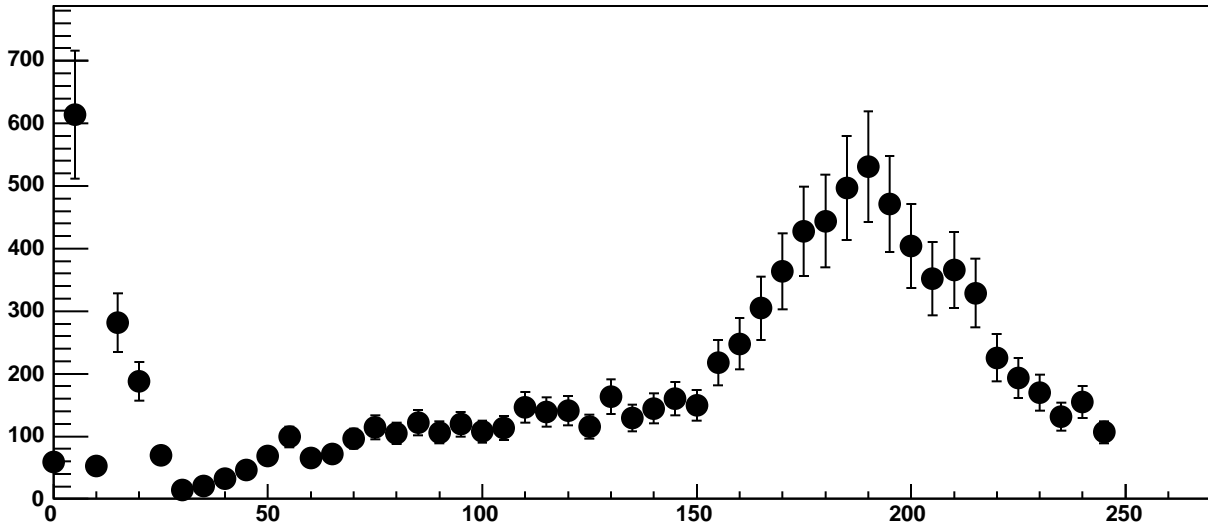


Chip 0, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold

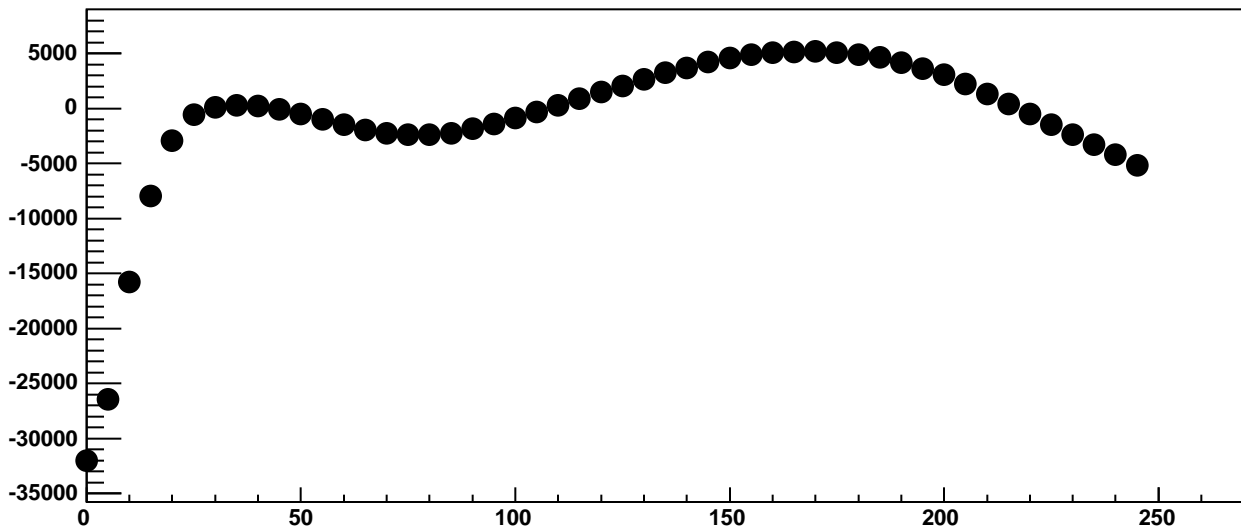


$\chi^2 / \text{ndf}$	2.354e+05 / 42
p0	5874 ± 111.7
p1	-1363 ± 11.99
p2	3.184e+06 ± 6.526e+04
p3	172.1 ± 1.279

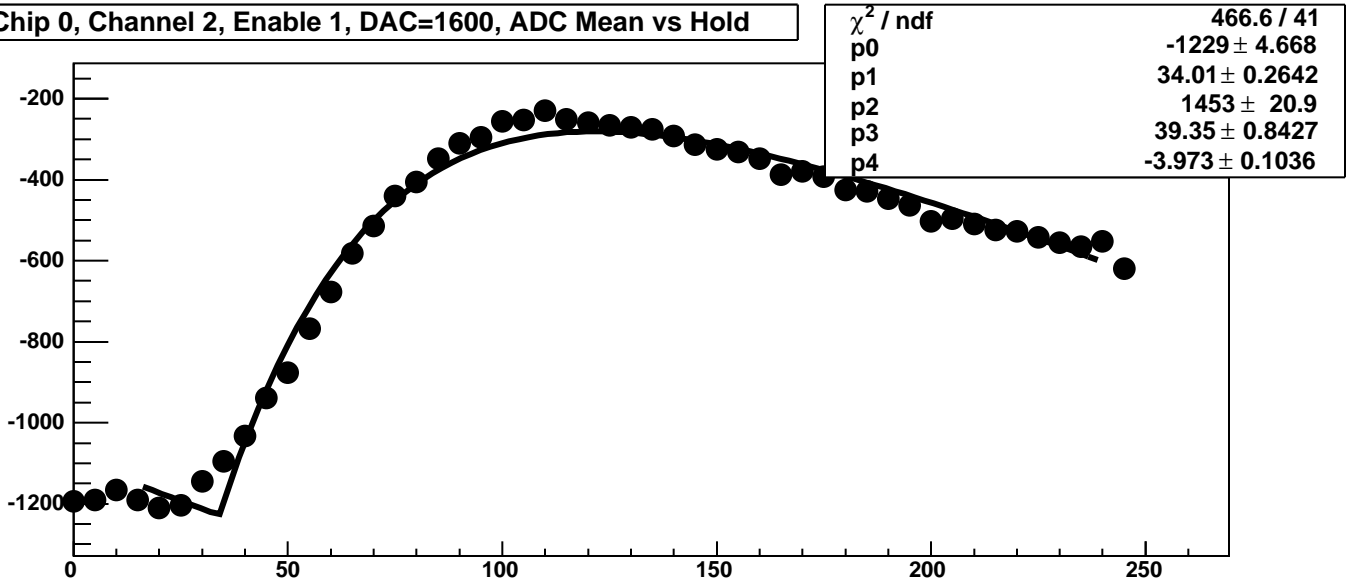
Chip 0, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



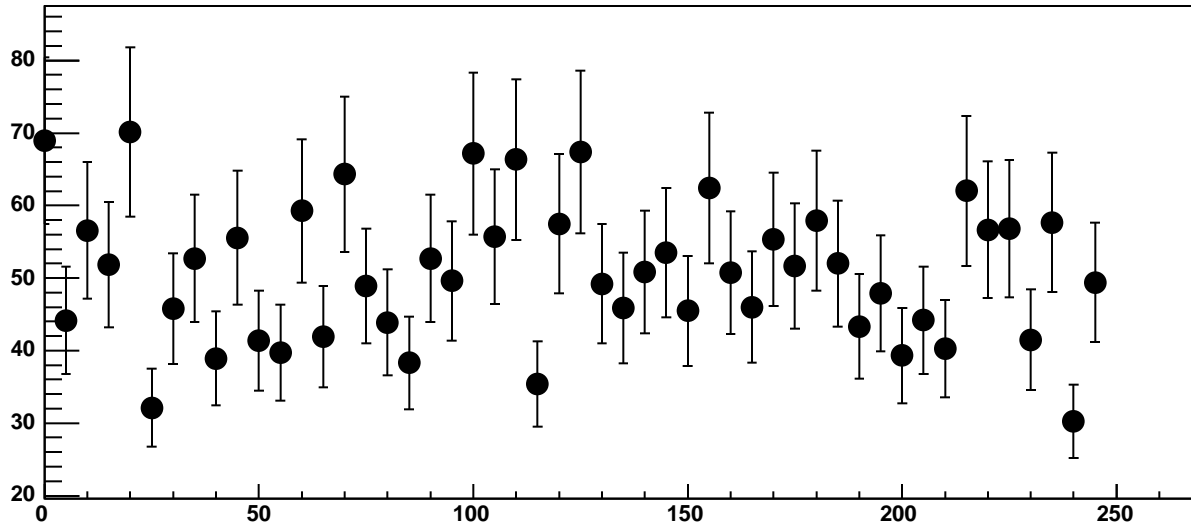
Chip 0, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold



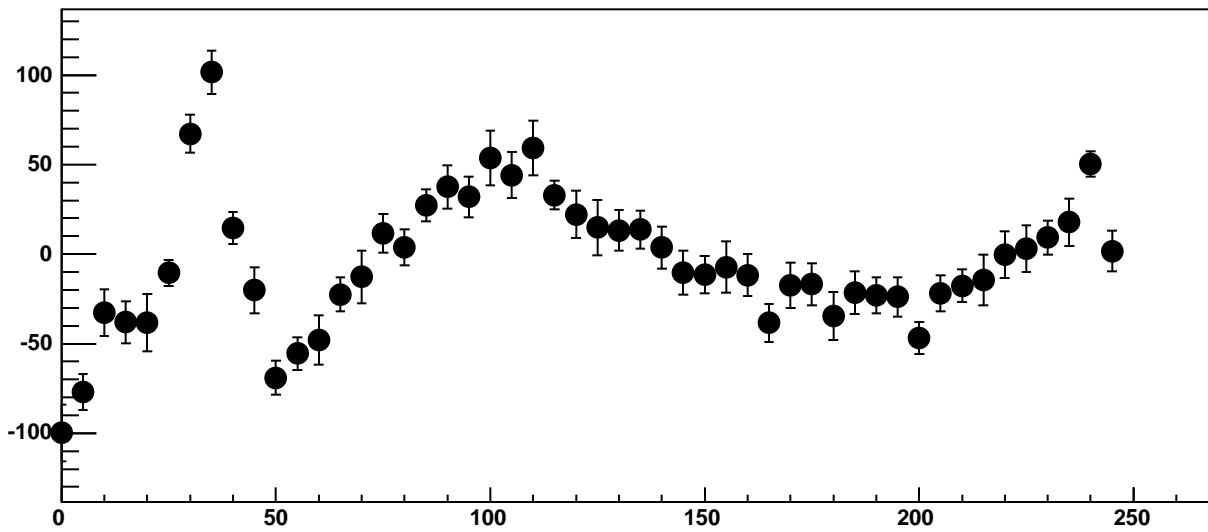
Chip 0, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold



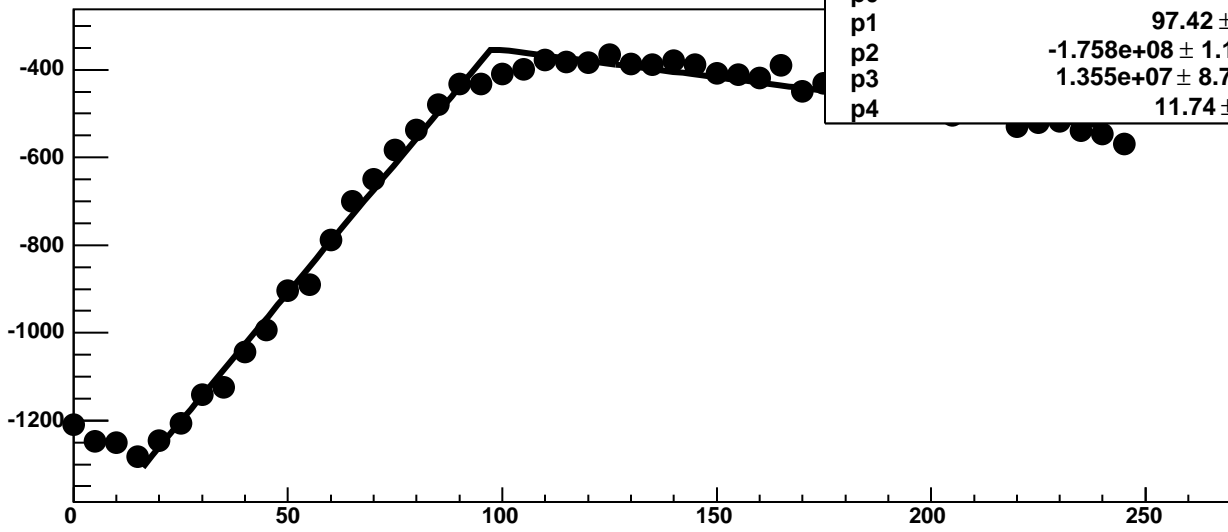
Chip 0, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



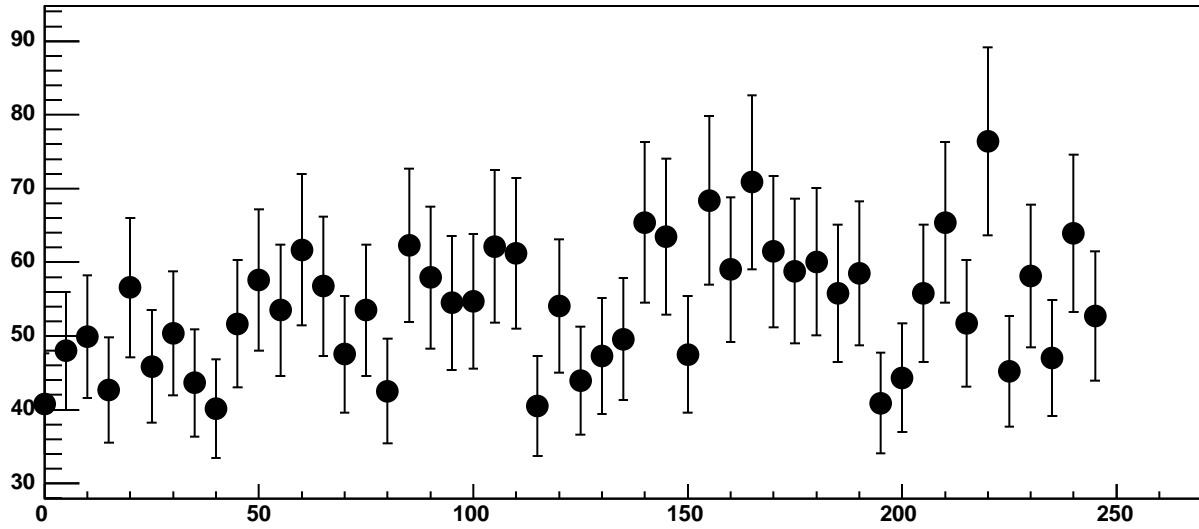
Chip 0, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



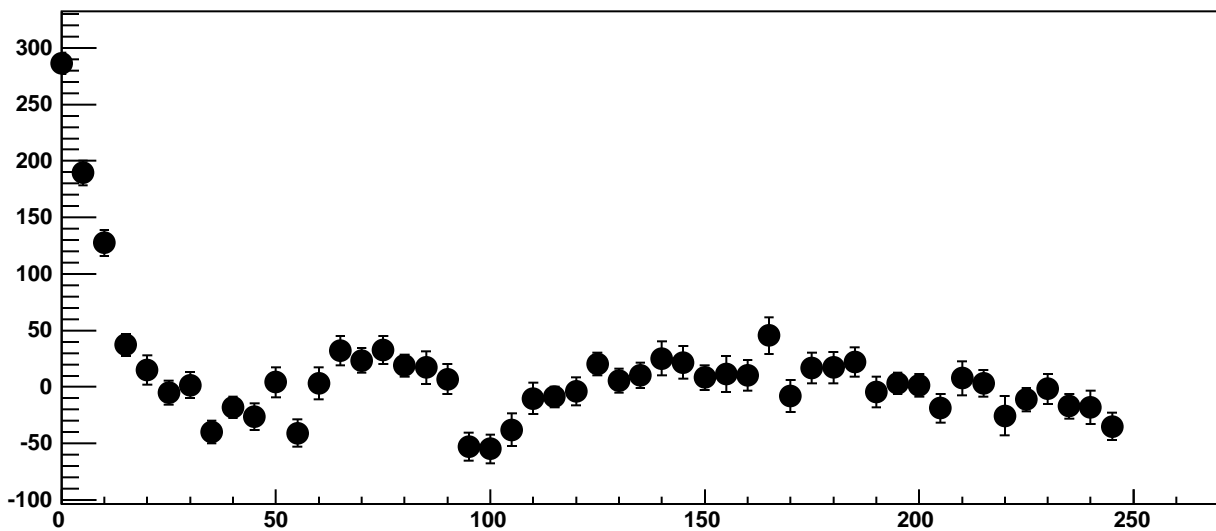
Chip 0, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold



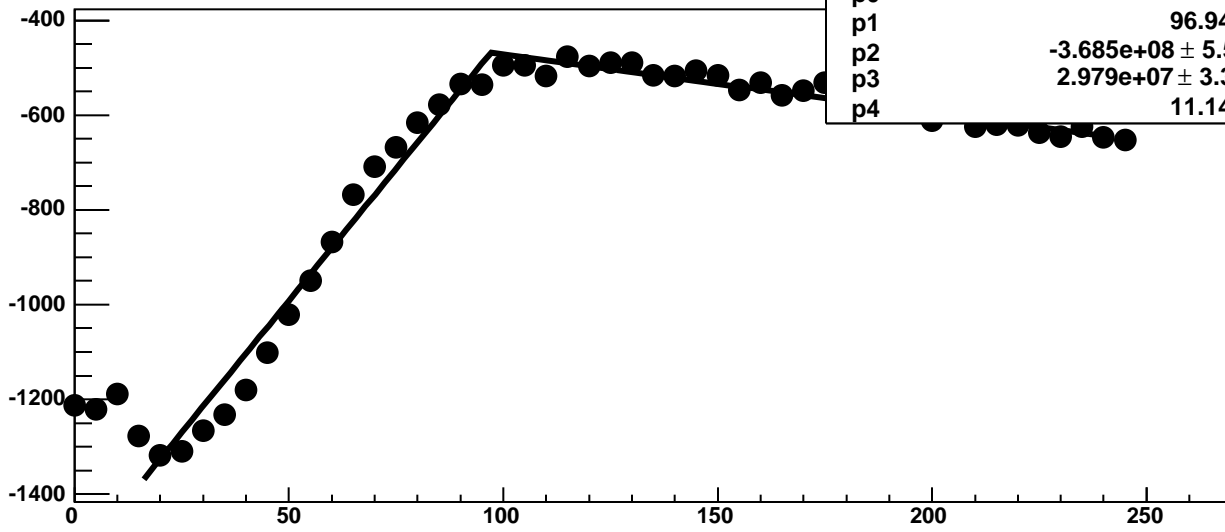
Chip 0, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

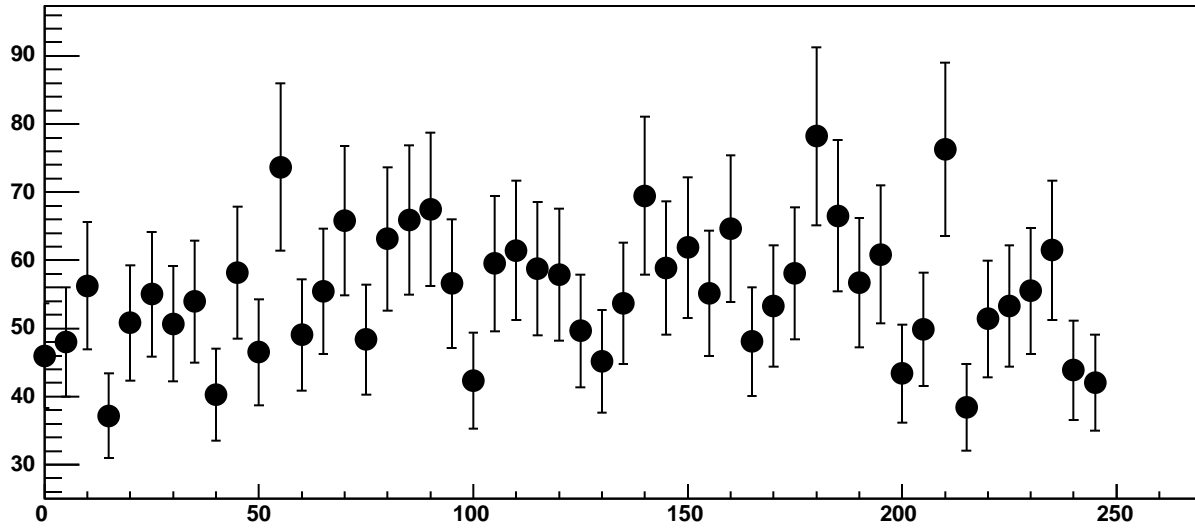


Chip 0, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

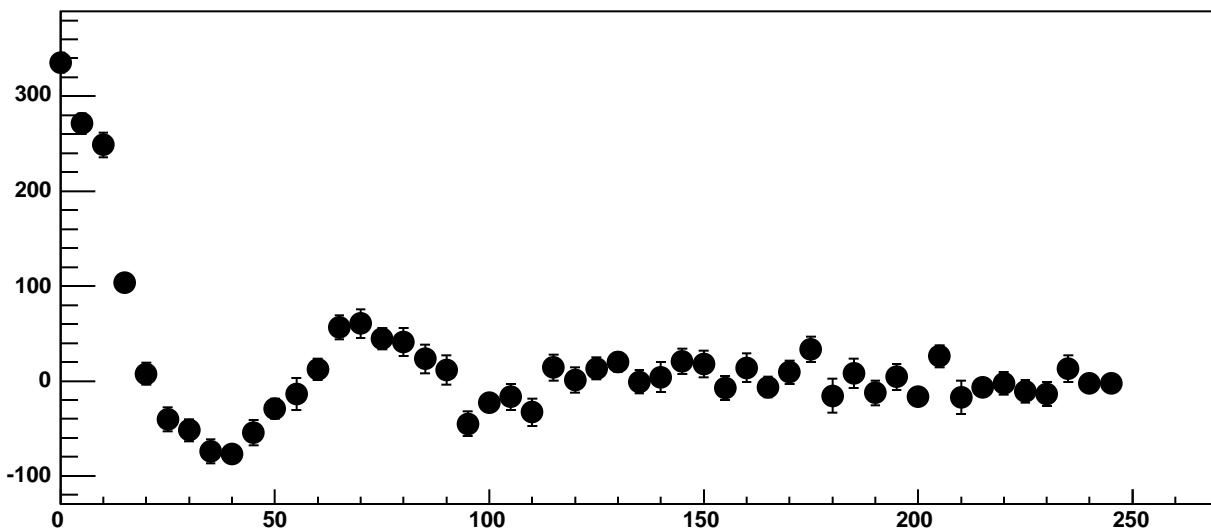


$\chi^2 / \text{ndf}$	428.8 / 41
p0	-468.3 ± 4.151
p1	96.94 ± 0.631
p2	-3.685e+08 ± 5.598e+06
p3	2.979e+07 ± 3.315e+05
p4	11.14 ± 0.119

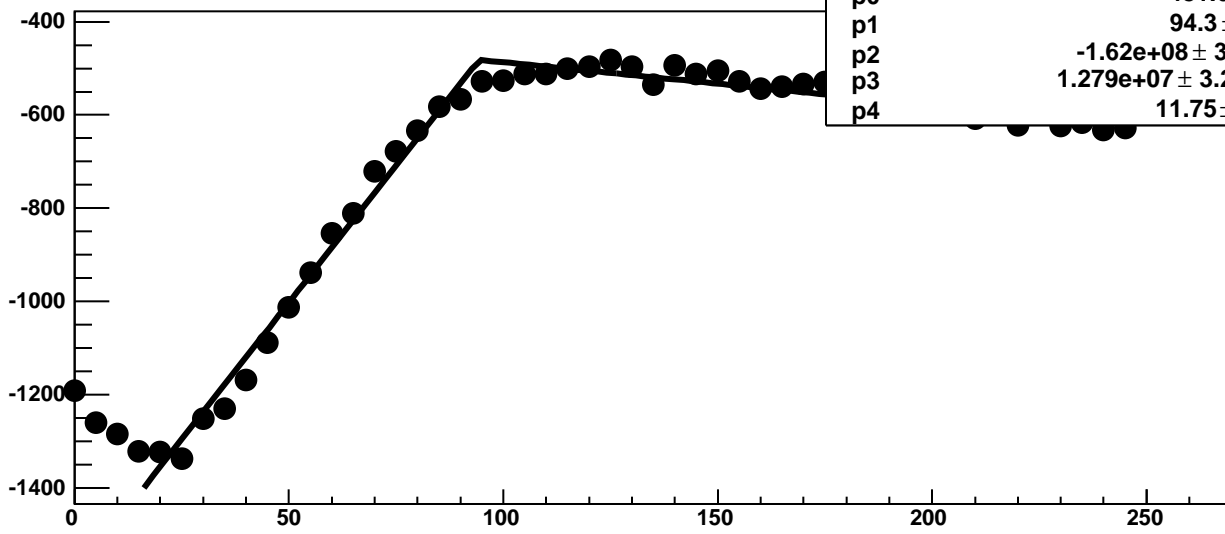
Chip 0, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold

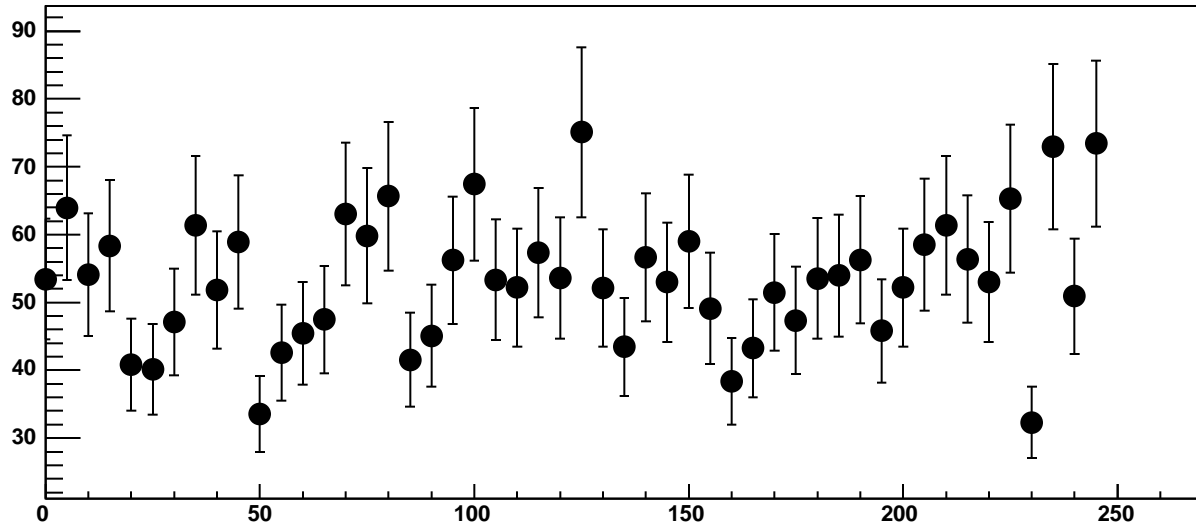


Chip 0, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

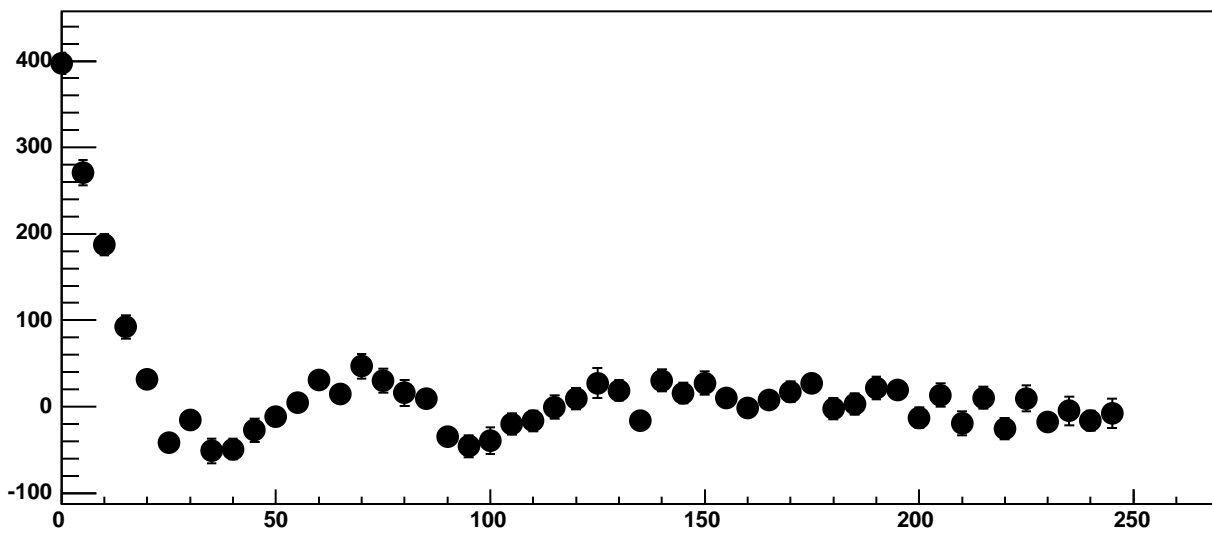


$\chi^2 / \text{ndf}$	233.1 / 41
p0	$-481.6 \pm 4.057$
p1	$94.3 \pm 0.5362$
p2	$-1.62\text{e}+08 \pm 3.78\text{e}+06$
p3	$1.279\text{e}+07 \pm 3.236\text{e}+05$
p4	$11.75 \pm 0.1076$

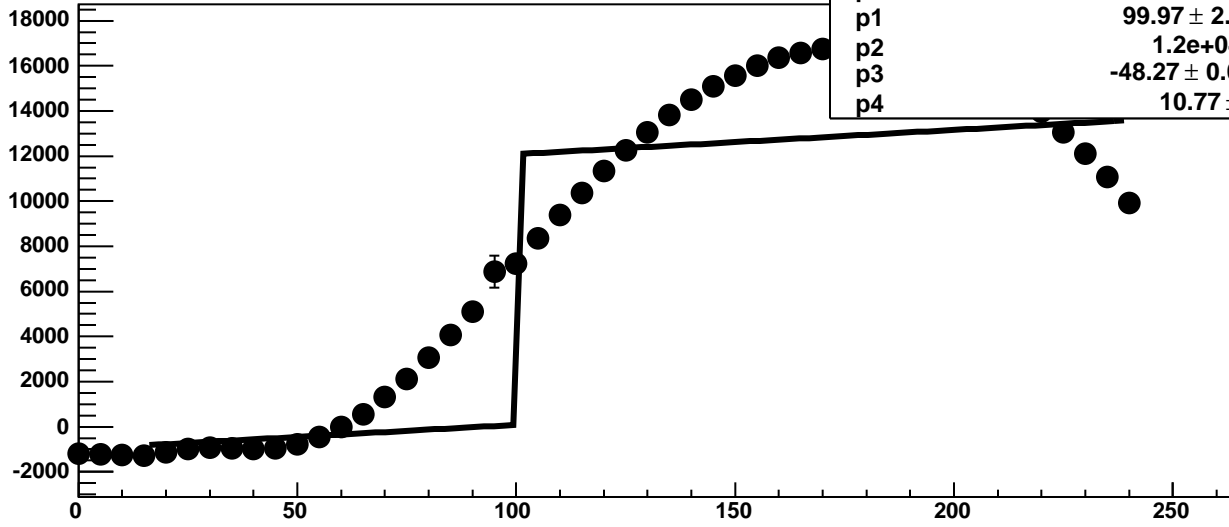
Chip 0, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

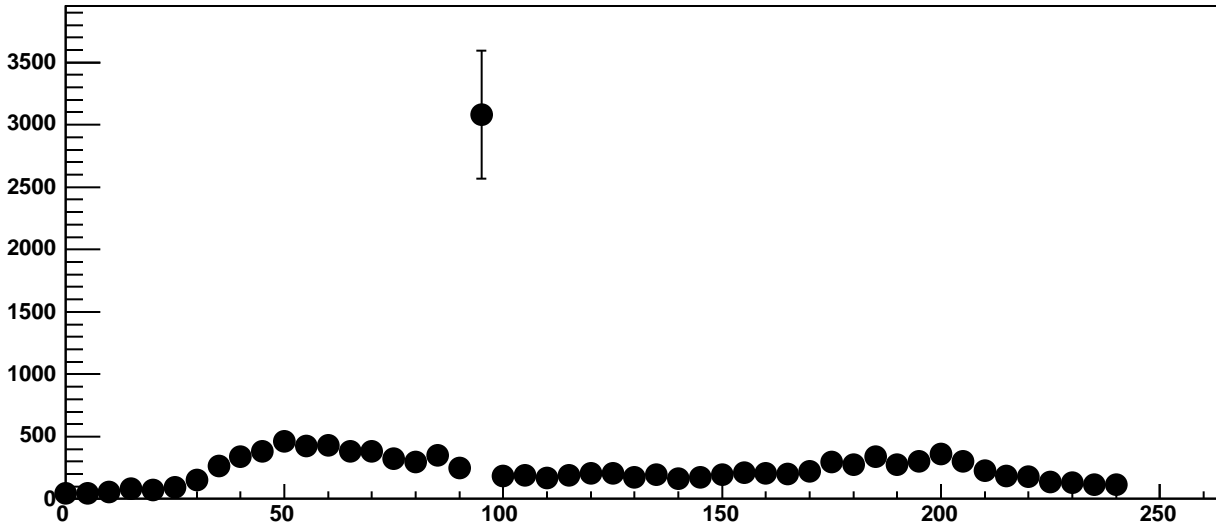


Chip 0, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

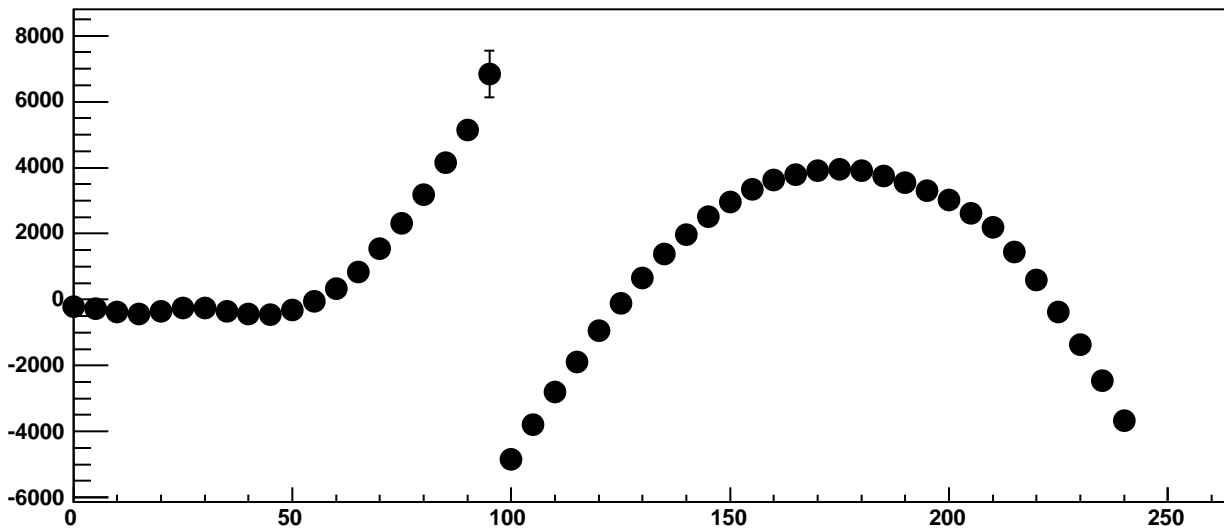


$\chi^2 / \text{ndf}$	1.307e+05 / 41
p0	85.3 ± 15.01
p1	99.97 ± 2.636e-05
p2	1.2e+04 ± 27.4
p3	-48.27 ± 0.0008338
p4	10.77 ± 0.1537

Chip 0, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

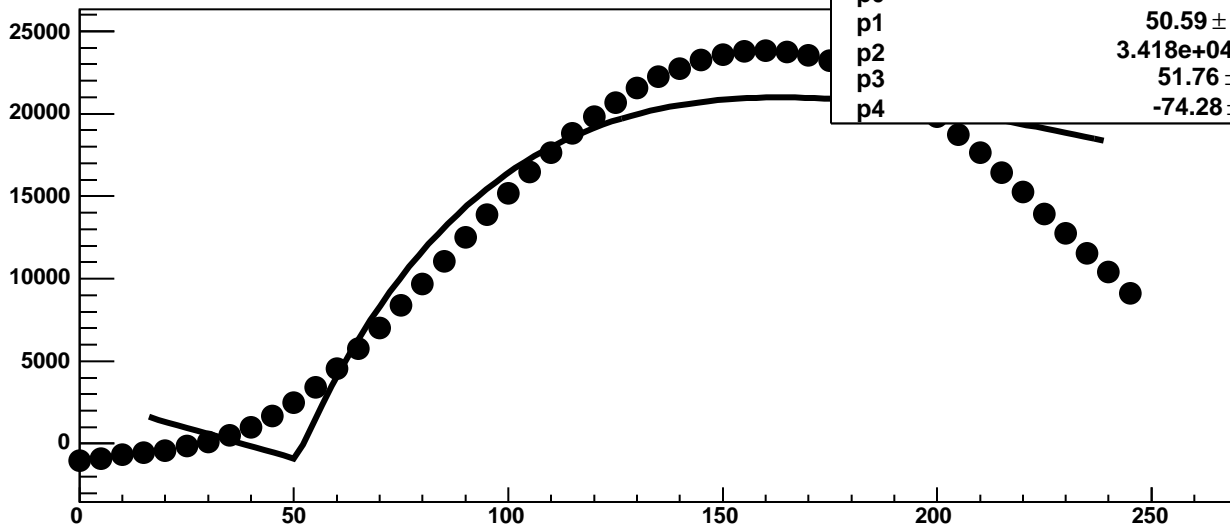


Chip 0, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



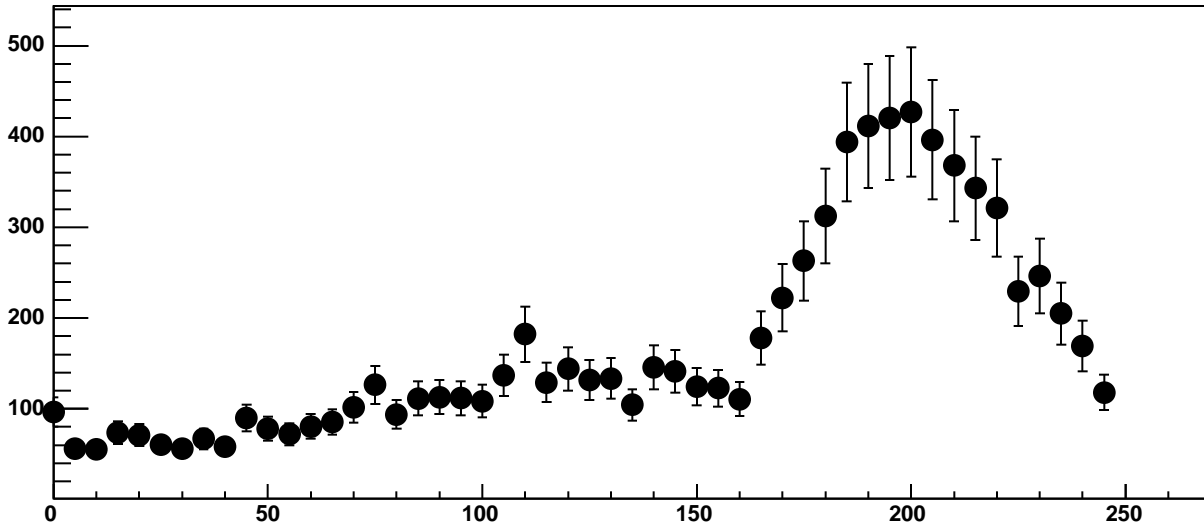


Chip 0, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

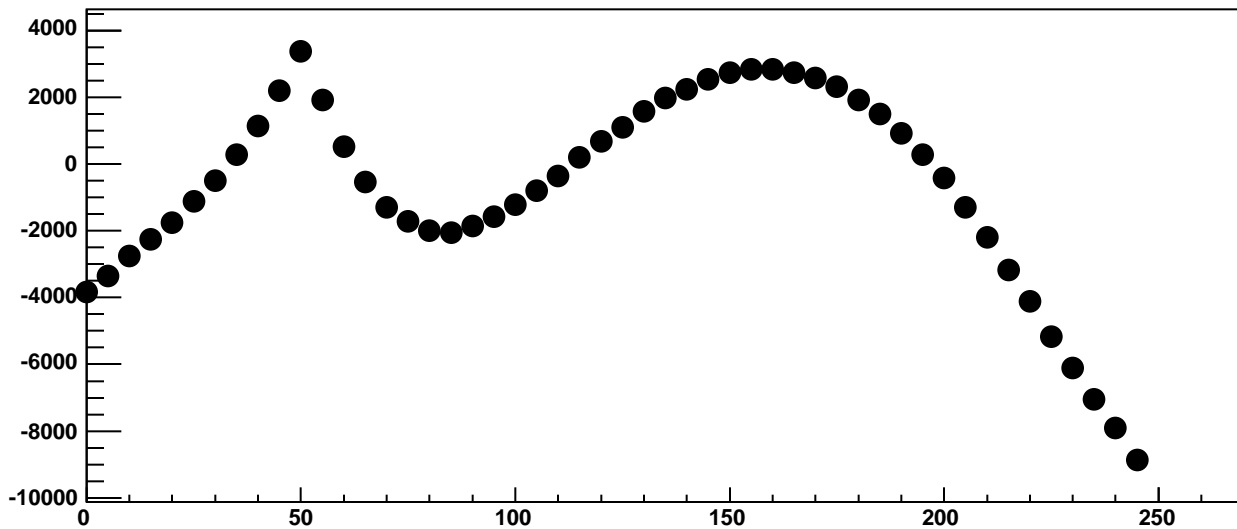


$\chi^2 / \text{ndf}$	2.948e+05 / 41
p0	-942.8 ± 7.532
p1	50.59 ± 0.02516
p2	3.418e+04 ± 65.68
p3	51.76 ± 0.1025
p4	-74.28 ± 0.3322

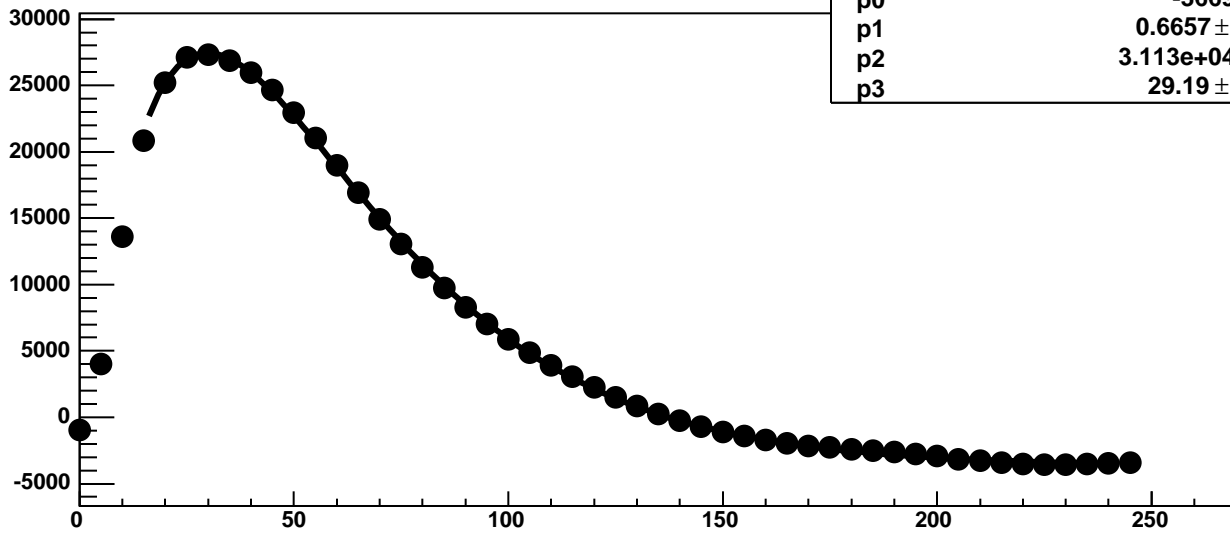
Chip 0, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

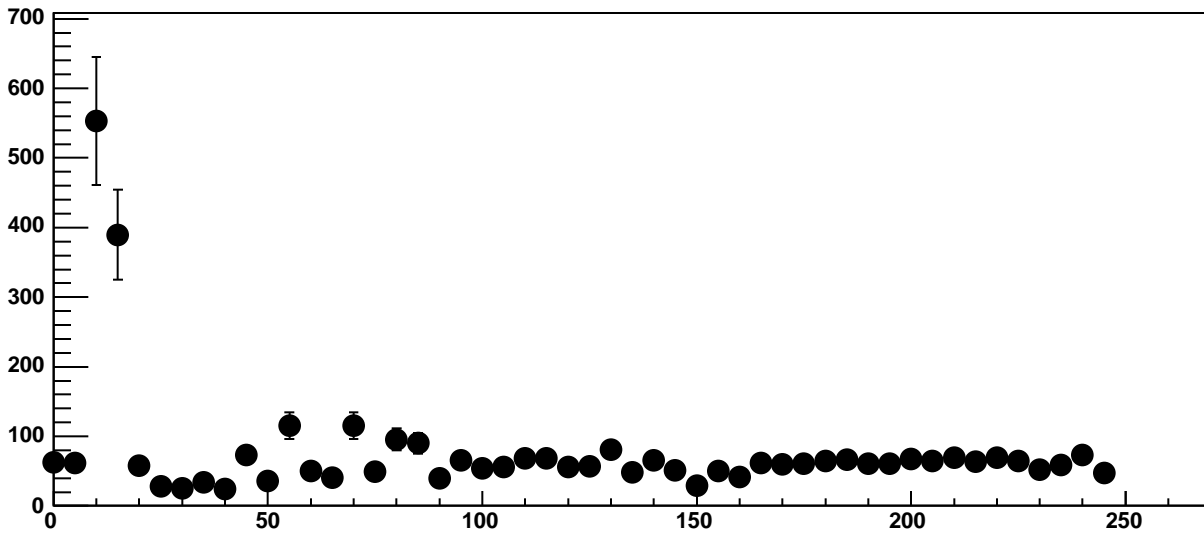


Chip 0, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold

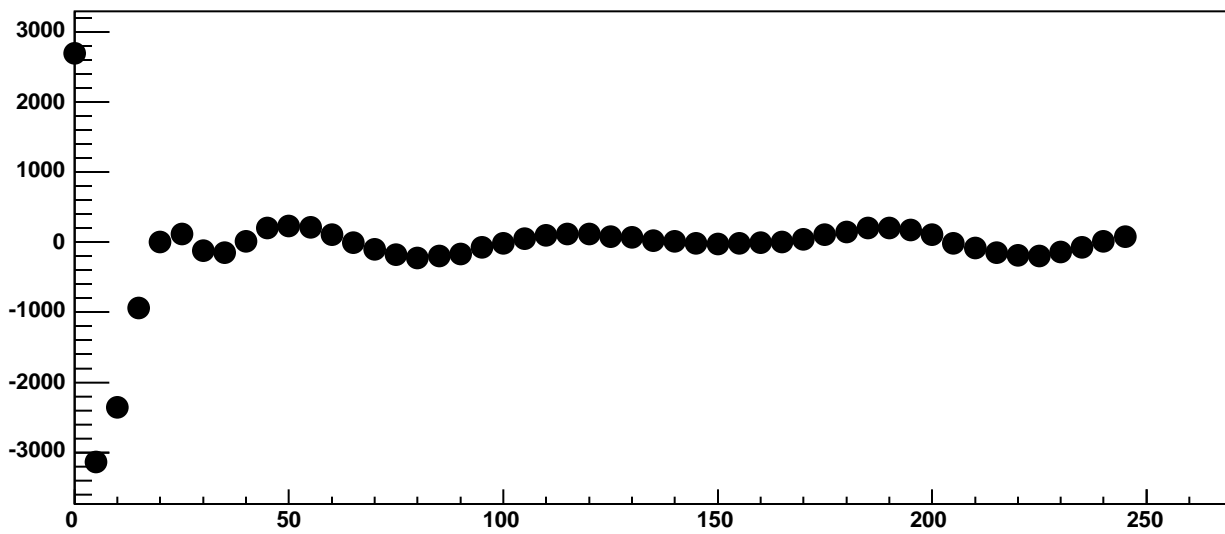


$\chi^2 / \text{ndf}$  4827 / 42  
p0  $-3669 \pm 3.998$   
p1  $0.6657 \pm 0.02141$   
p2  $3.113e+04 \pm 4.655$   
p3  $29.19 \pm 0.01193$

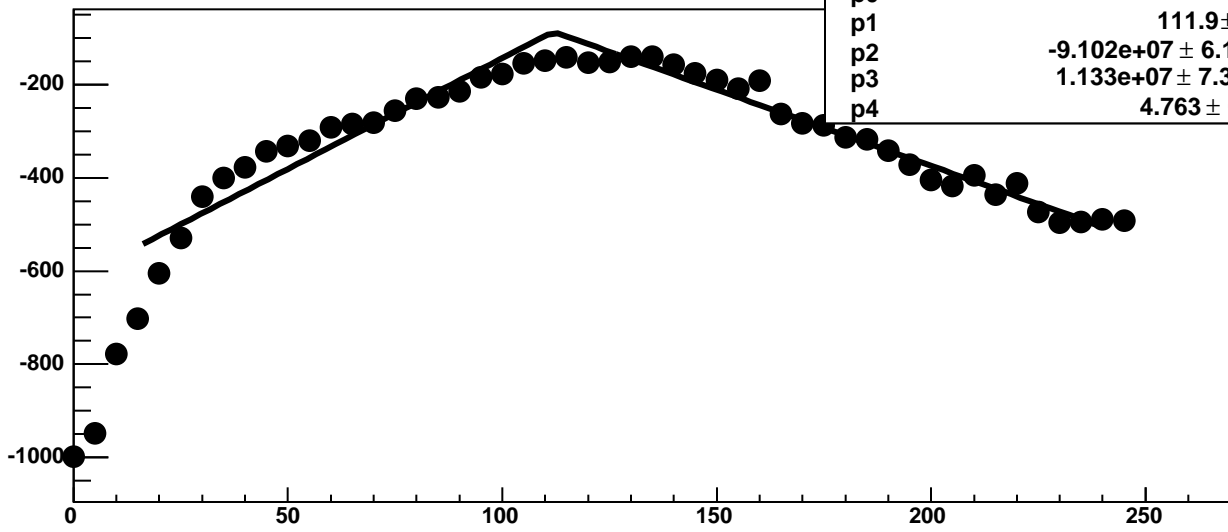
Chip 0, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold

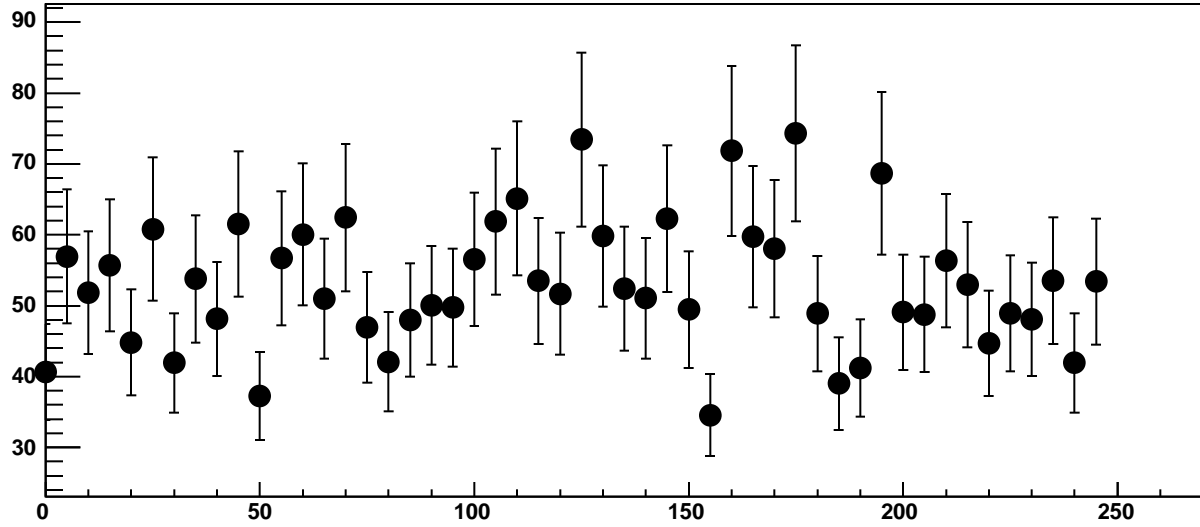


Chip 0, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

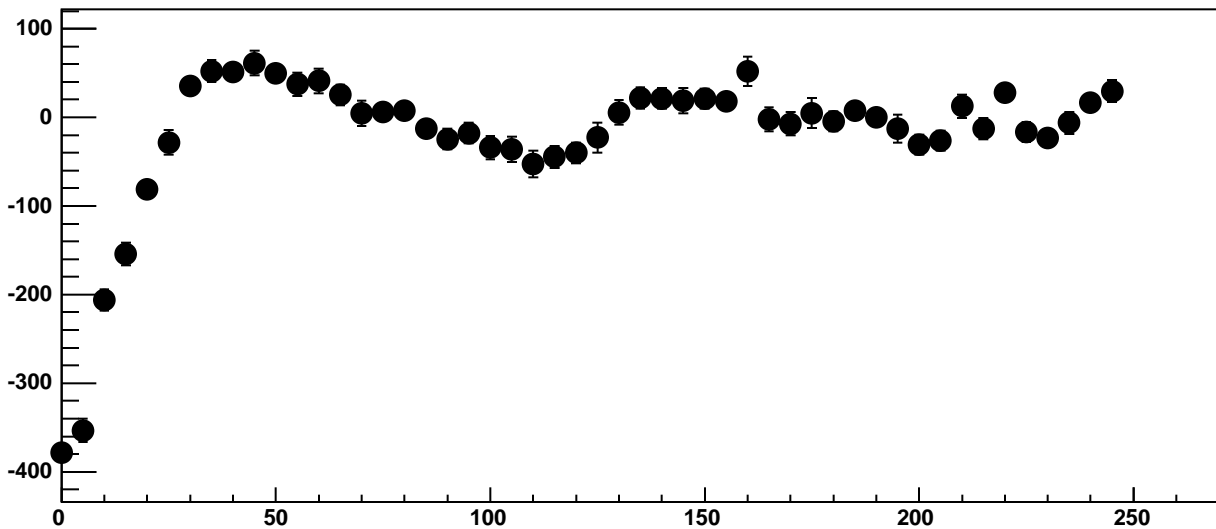


$\chi^2 / \text{ndf}$	463.4 / 41
p0	$-86.47 \pm 3.64$
p1	$111.9 \pm 0.9012$
p2	$-9.102\text{e}+07 \pm 6.154\text{e}+06$
p3	$1.133\text{e}+07 \pm 7.328\text{e}+05$
p4	$4.763 \pm 0.09413$

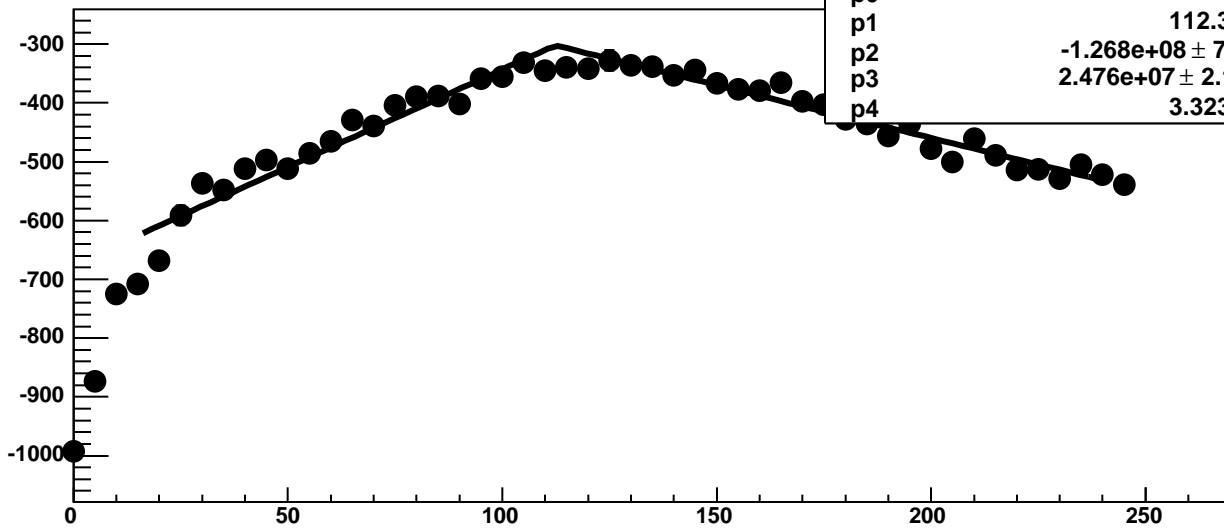
Chip 0, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

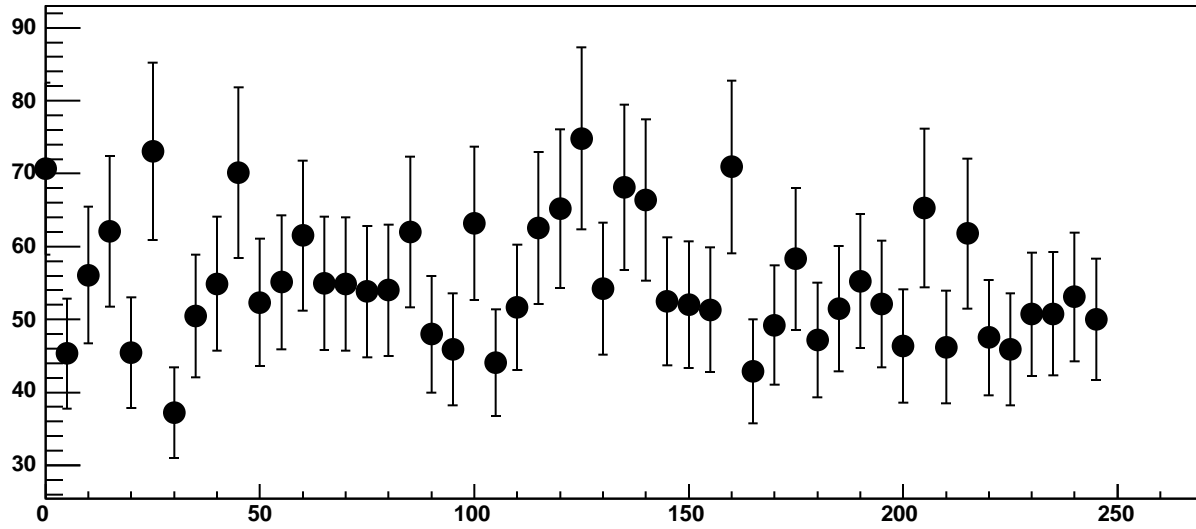


Chip 0, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

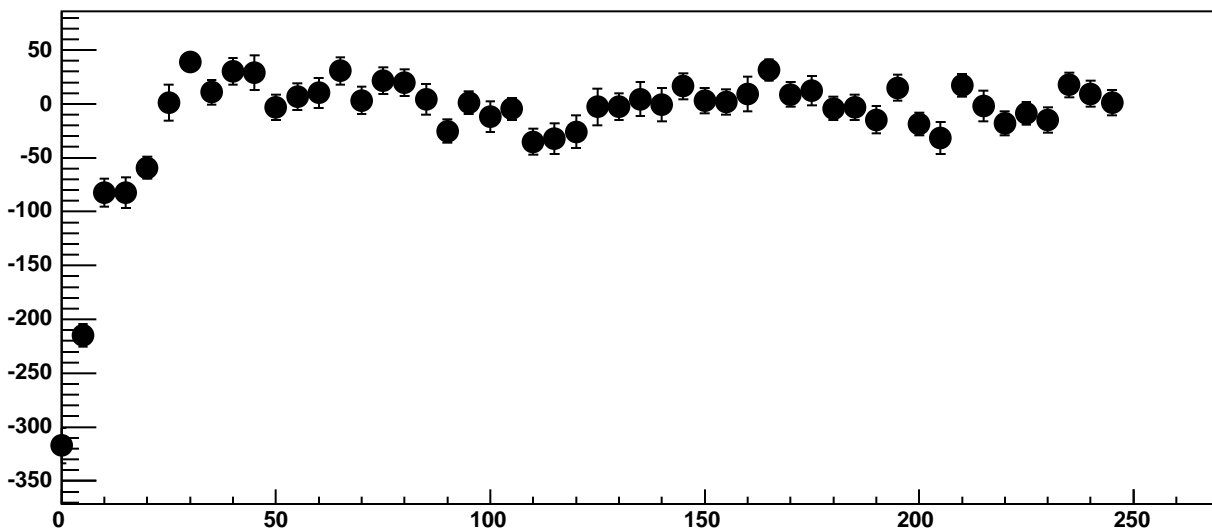


$\chi^2 / \text{ndf}$	167.3 / 41
p0	-302.1 ± 5.492
p1	112.3 ± 1.178
p2	-1.268e+08 ± 7.03e+06
p3	2.476e+07 ± 2.121e+06
p4	3.323 ± 0.101

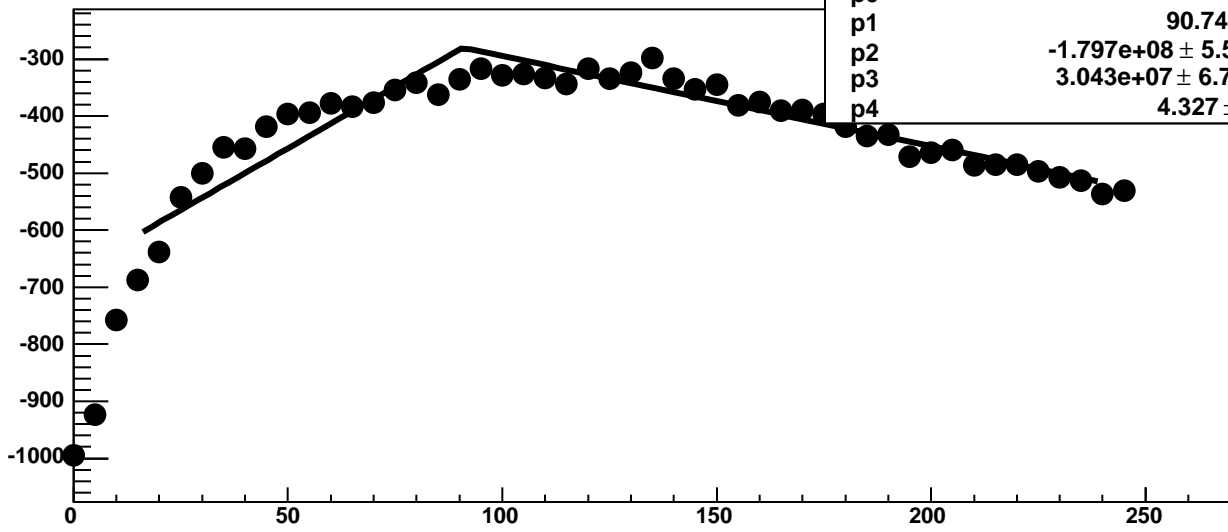
Chip 0, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



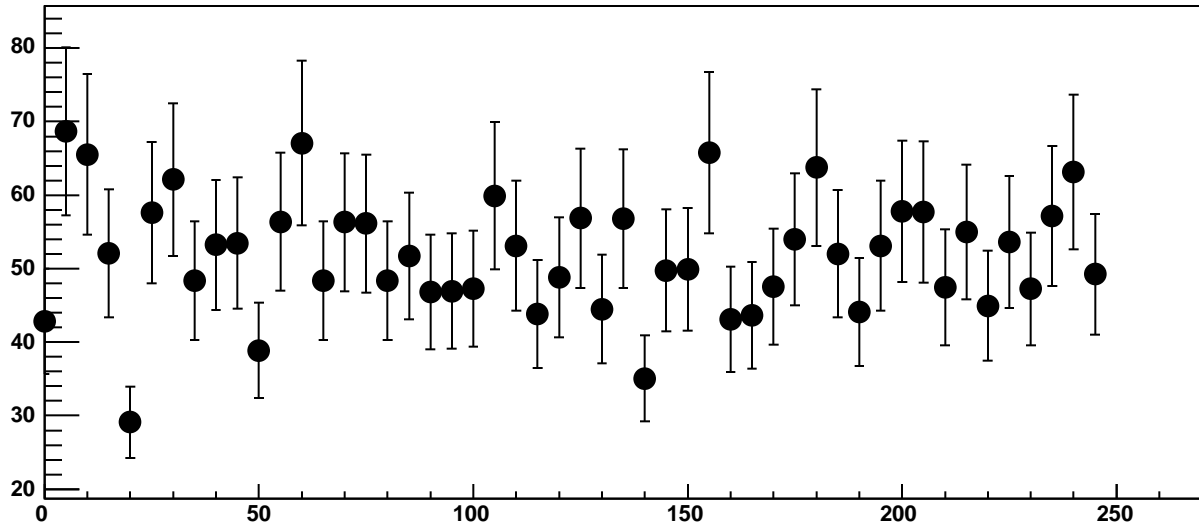
Chip 0, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



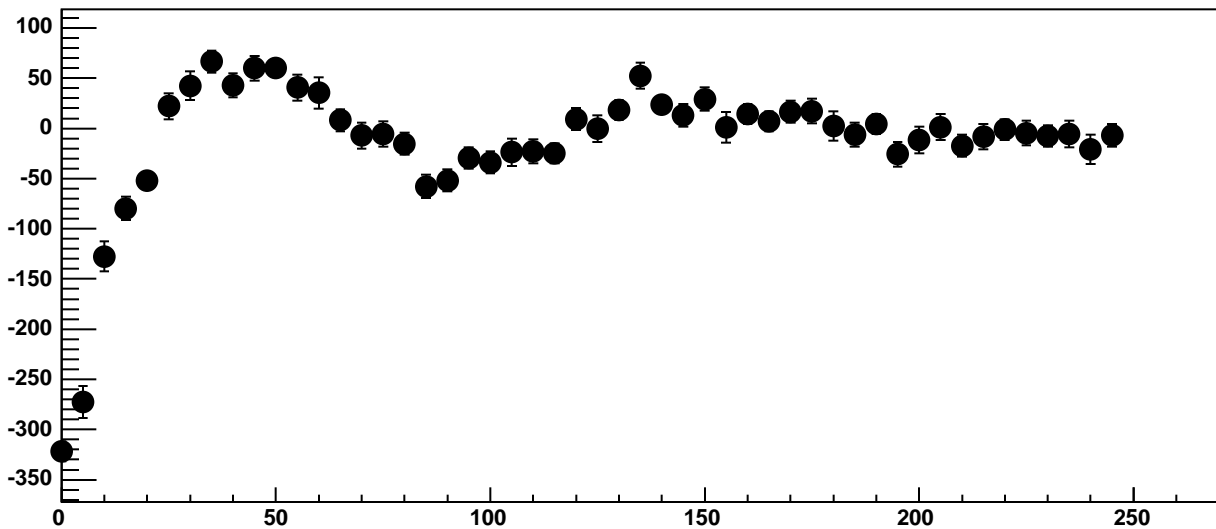
Chip 0, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold



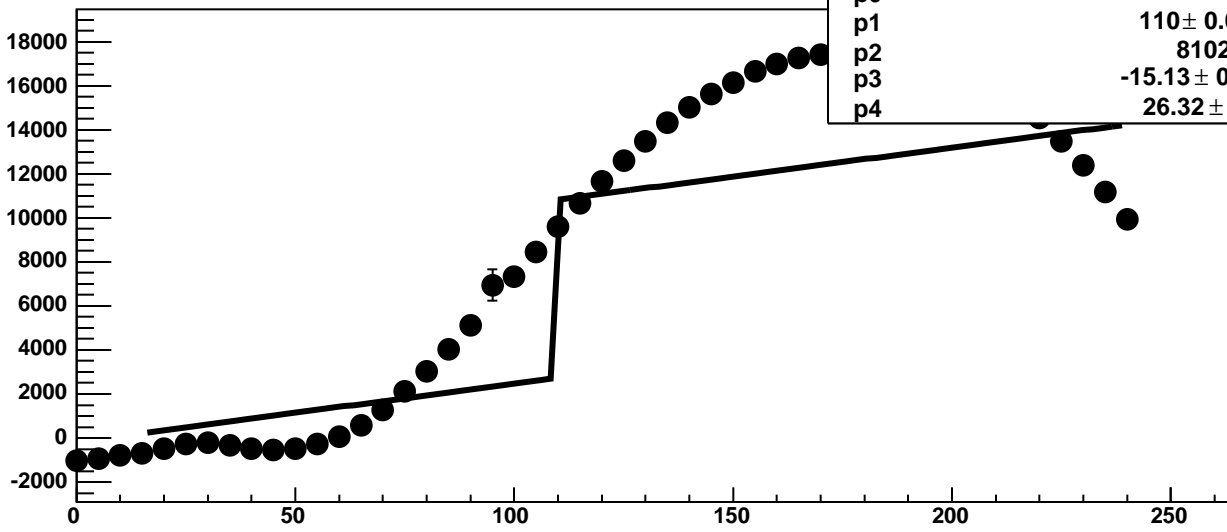
Chip 0, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold

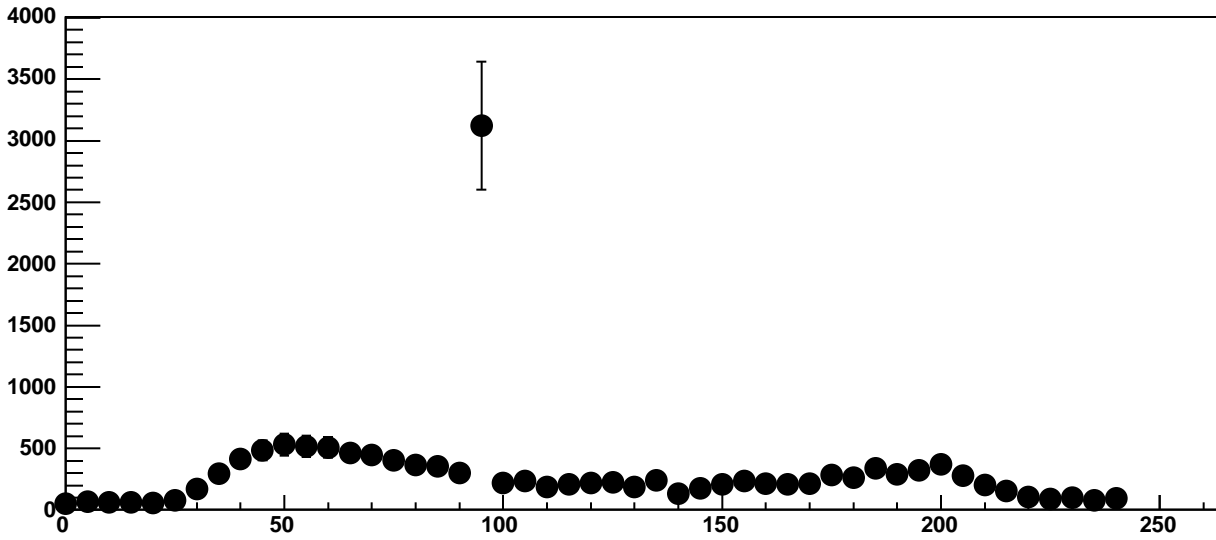


Chip 0, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

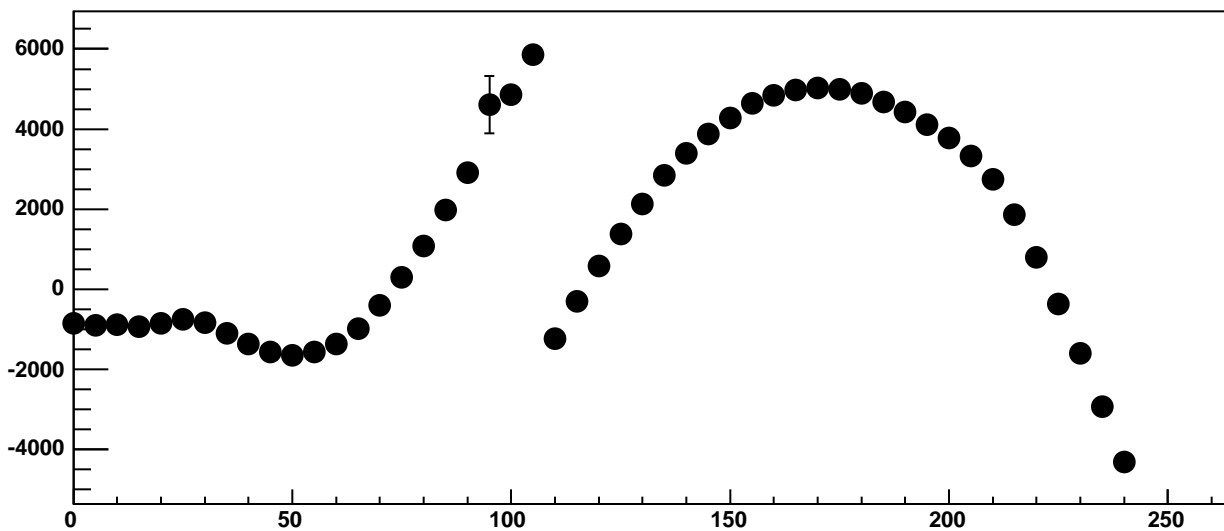


$\chi^2 / \text{ndf}$	2.149e+05 / 41
p0	2727 $\pm$ 5.346
p1	110 $\pm$ 0.0001608
p2	8102 $\pm$ 3.886
p3	-15.13 $\pm$ 0.000104
p4	26.32 $\pm$ 0.06052

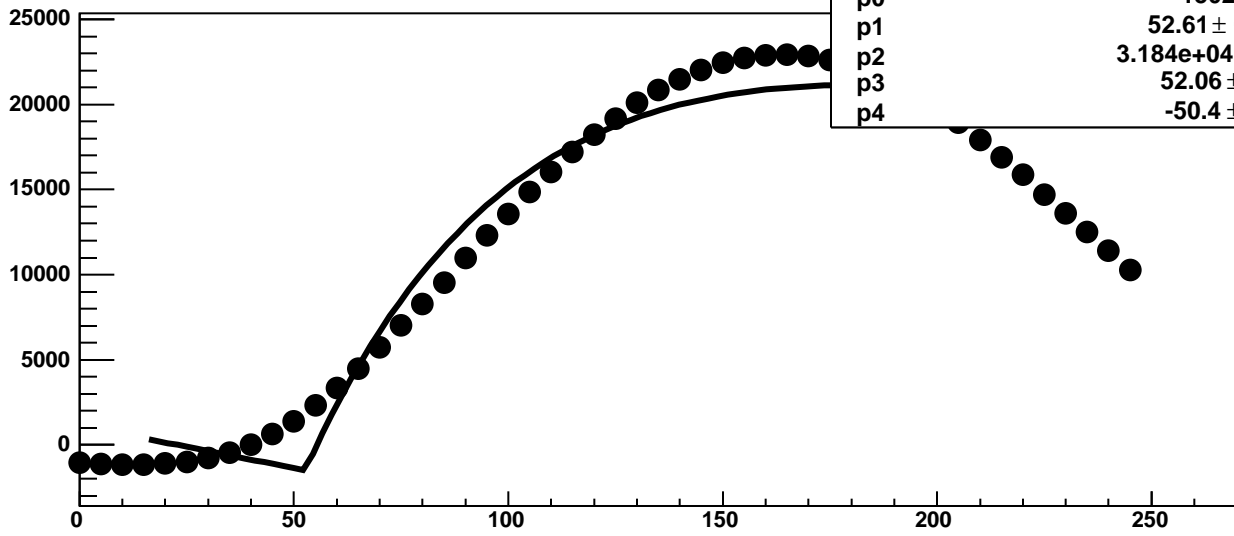
Chip 0, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

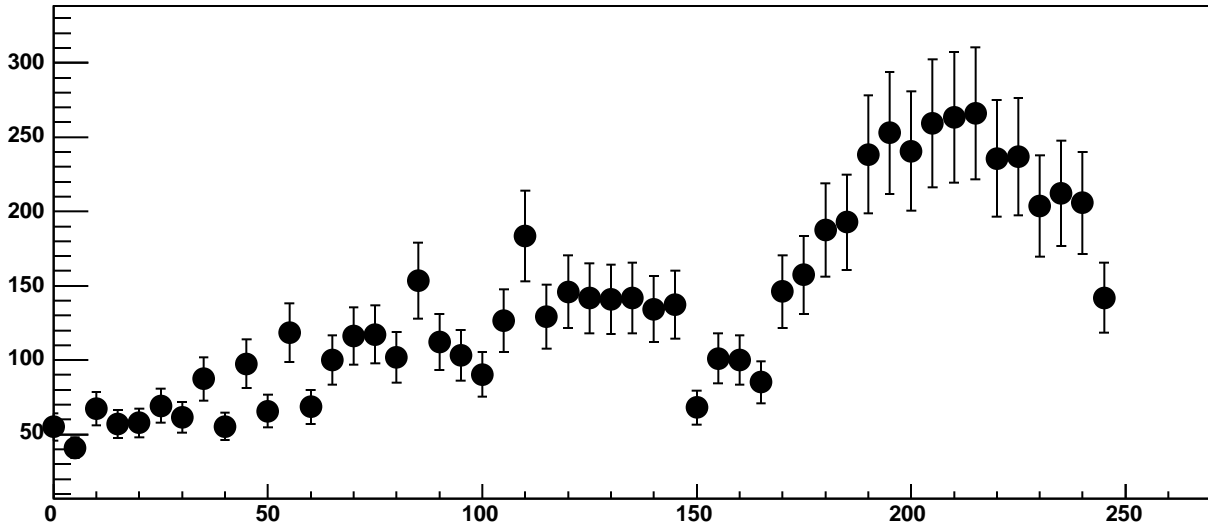


Chip 0, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

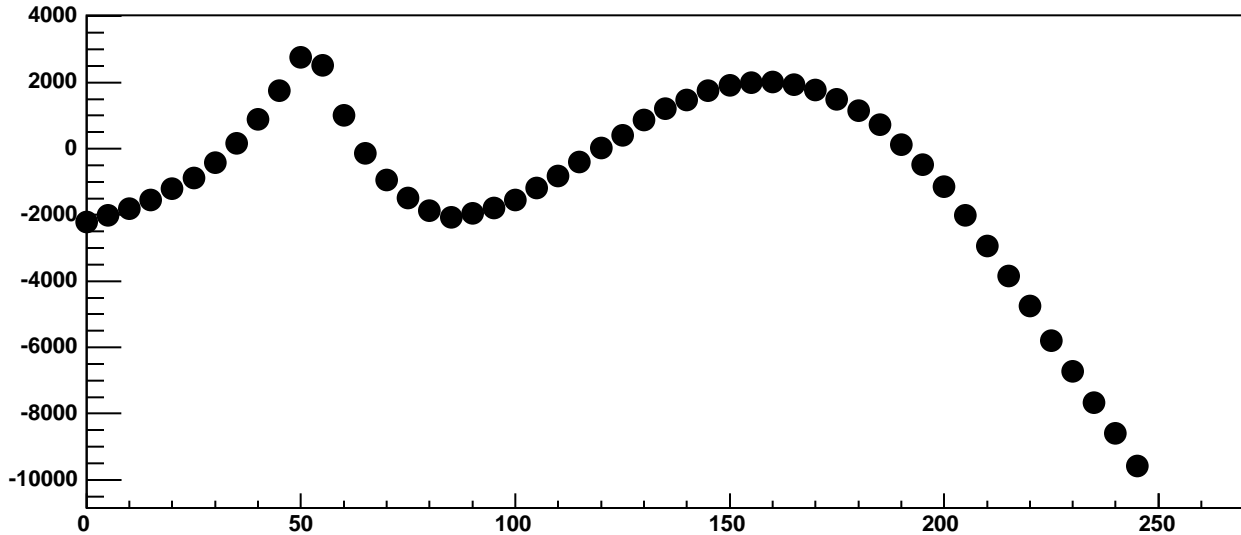


$\chi^2 / \text{ndf}$	2.765e+05 / 41
p0	-1502 ± 7.988
p1	52.61 ± 0.02795
p2	3.184e+04 ± 61.49
p3	52.06 ± 0.1037
p4	-50.4 ± 0.3098

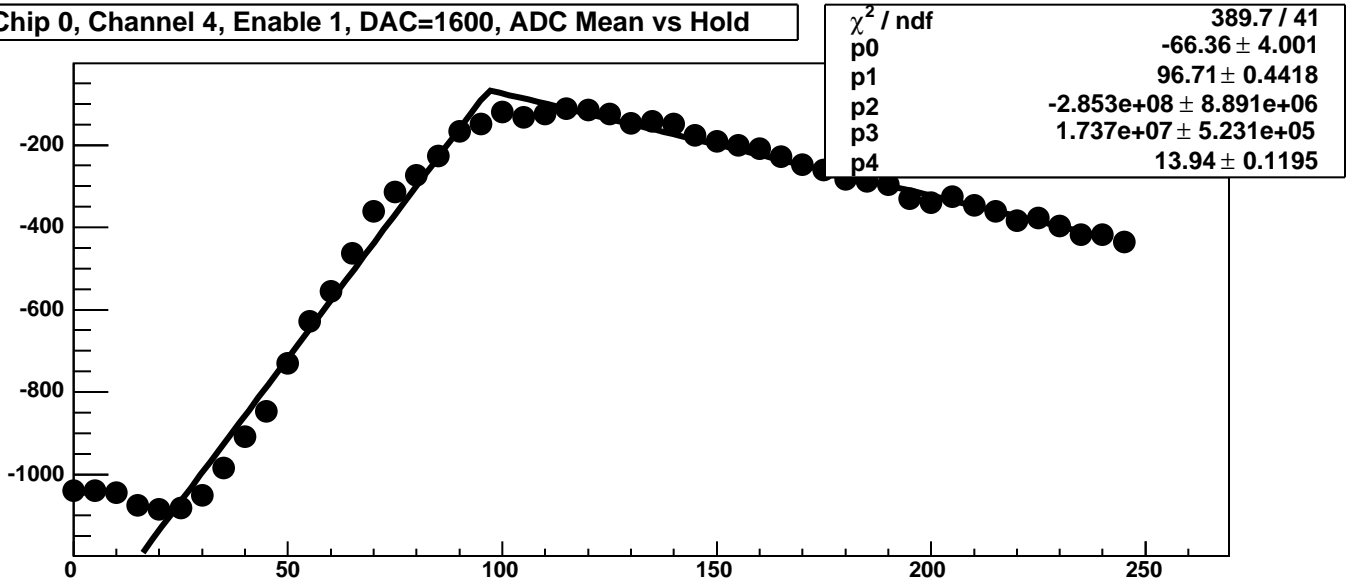
Chip 0, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



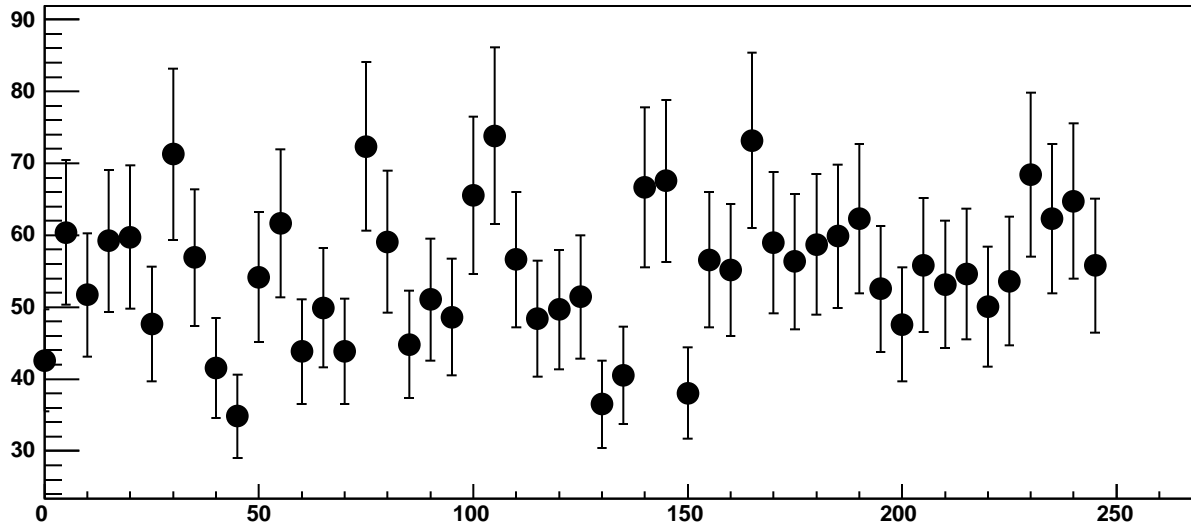
Chip 0, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



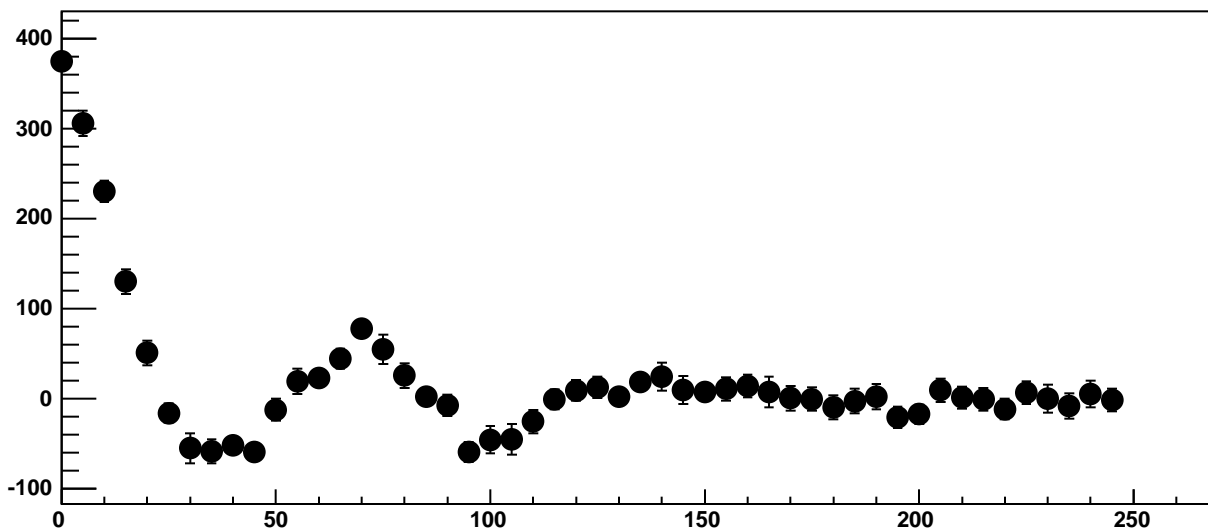
Chip 0, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 0, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

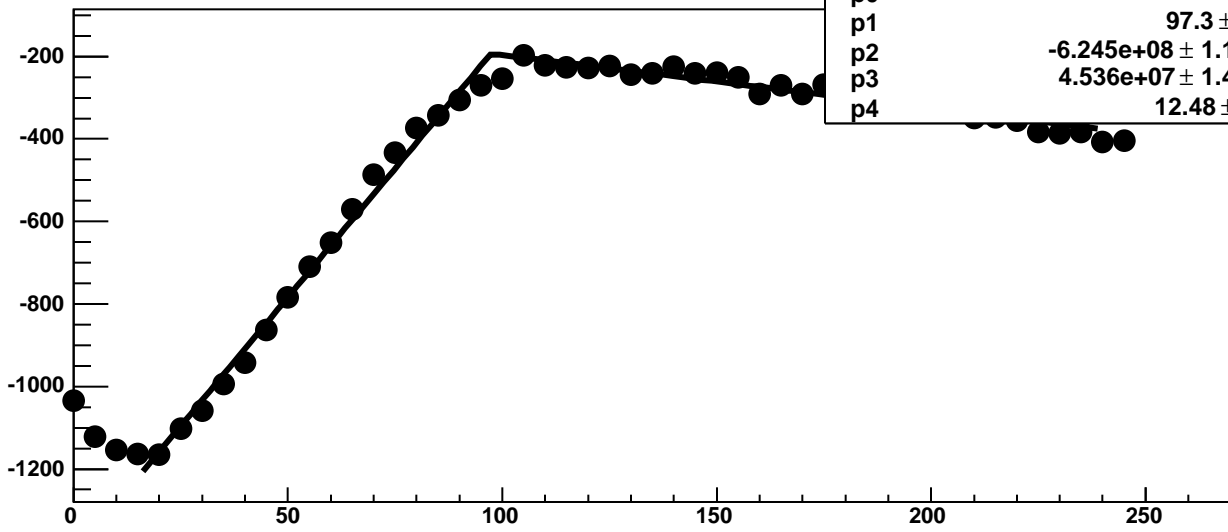


Chip 0, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold



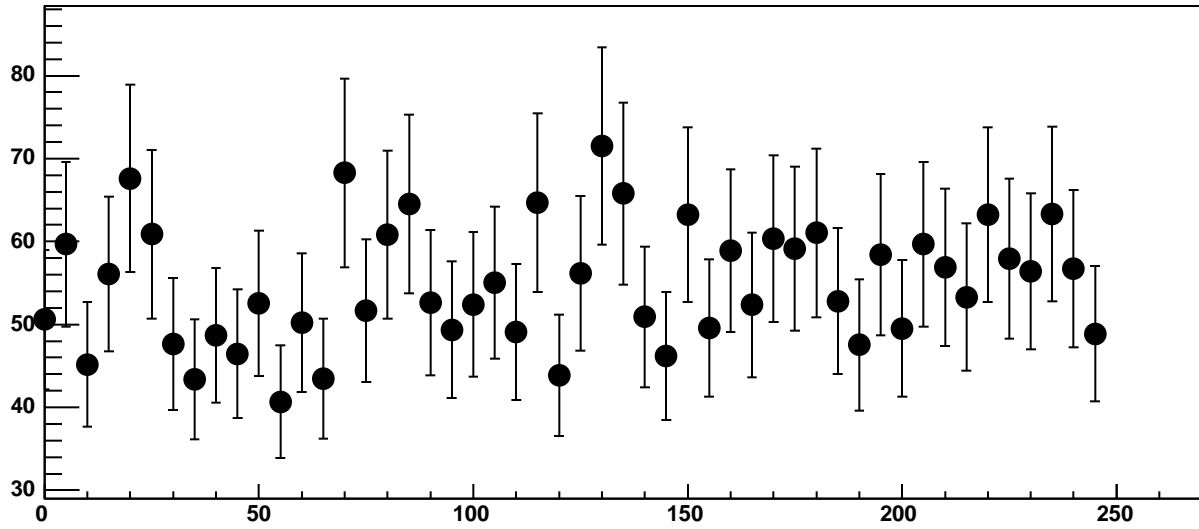


Chip 0, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

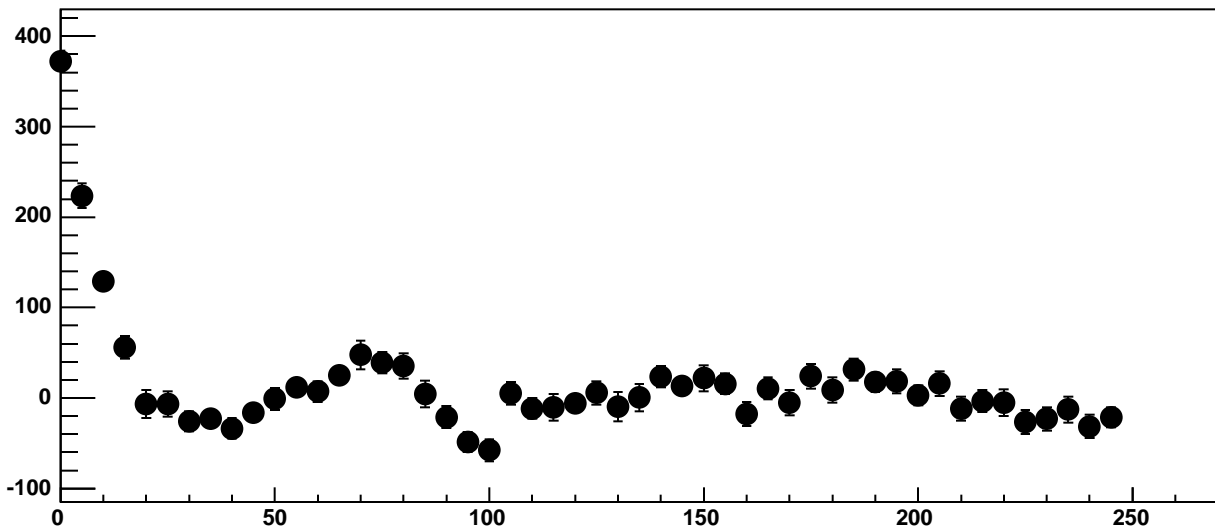


$\chi^2 / \text{ndf}$	167.1 / 41
p0	$-193.1 \pm 5.356$
p1	$97.3 \pm 0.3794$
p2	$-6.245\text{e}+08 \pm 1.167\text{e}+07$
p3	$4.536\text{e}+07 \pm 1.402\text{e}+06$
p4	$12.48 \pm 0.1289$

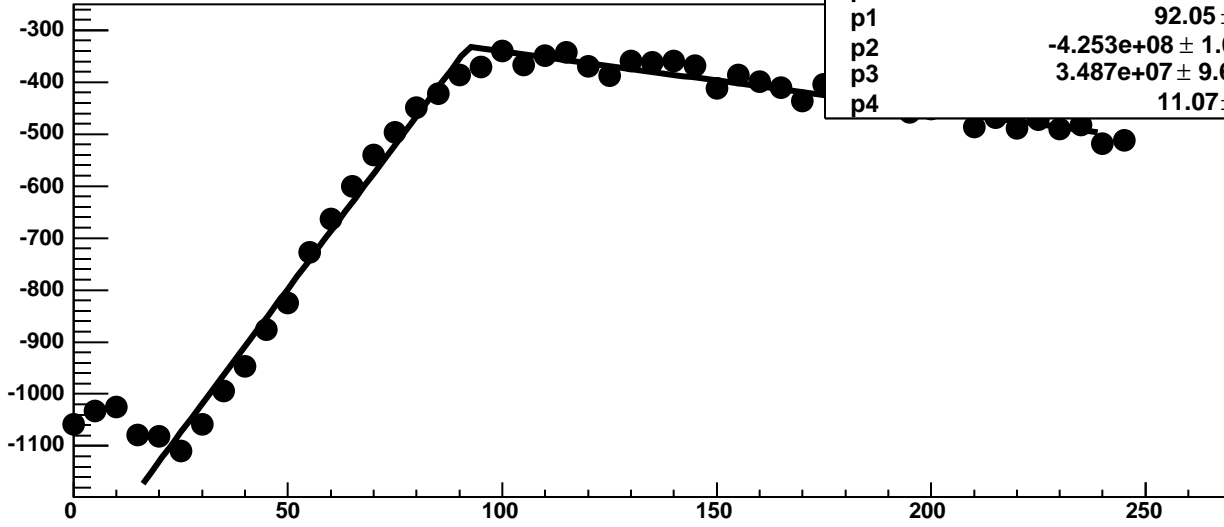
Chip 0, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

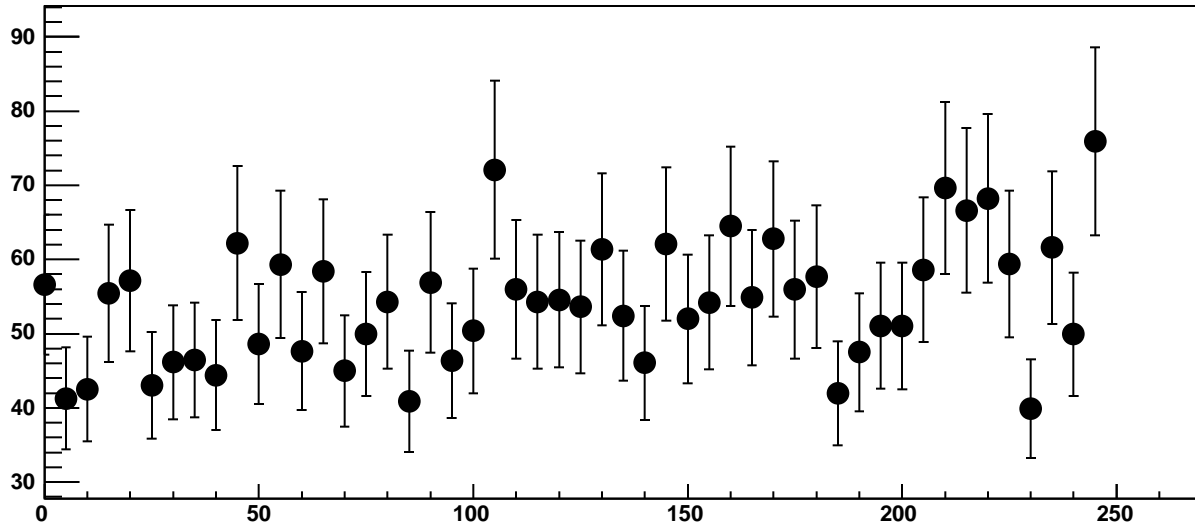


Chip 0, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

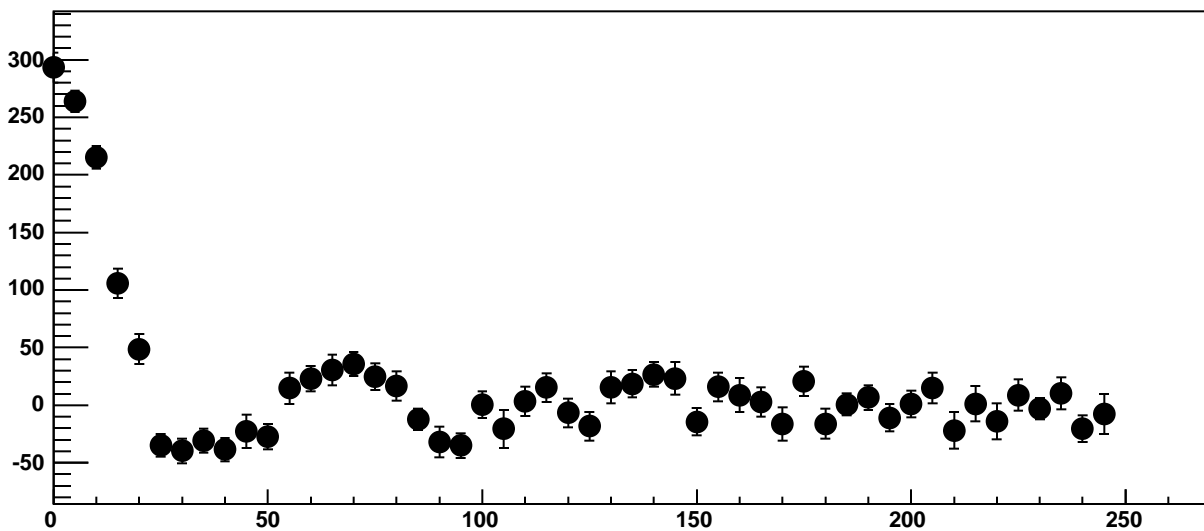


$\chi^2 / \text{ndf}$	224.8 / 41
p0	-331.9 ± 4.008
p1	92.05 ± 0.5749
p2	-4.253e+08 ± 1.077e+07
p3	3.487e+07 ± 9.618e+05
p4	11.07 ± 0.1166

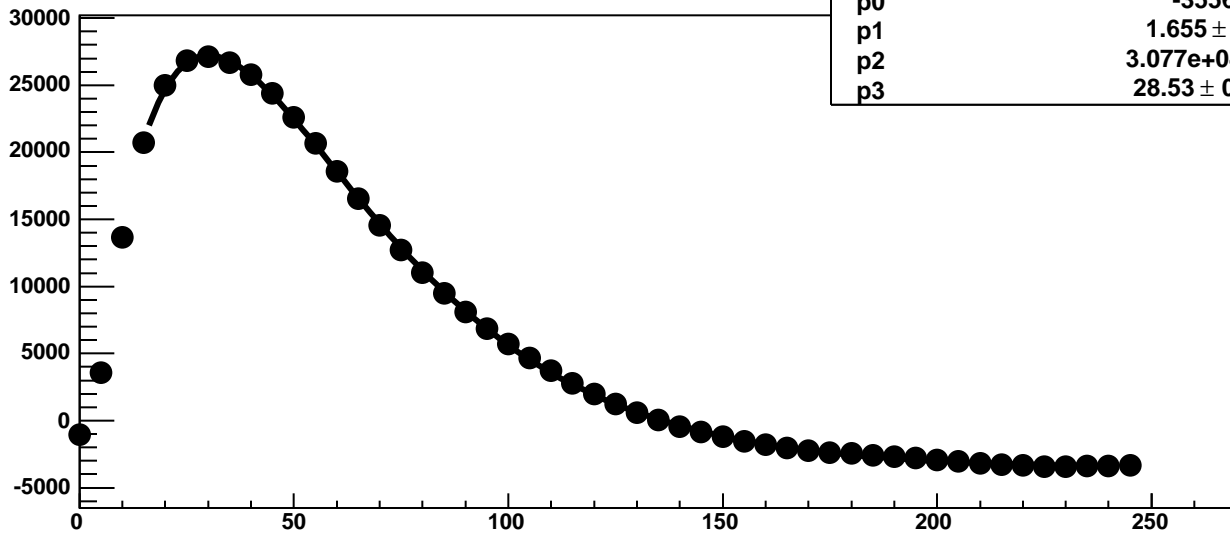
Chip 0, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

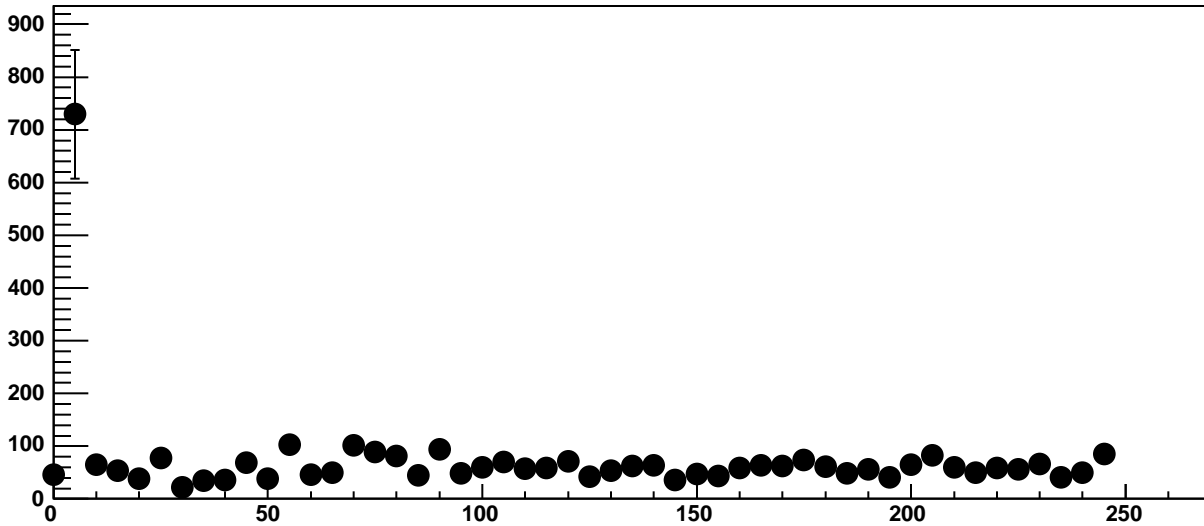


Chip 0, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

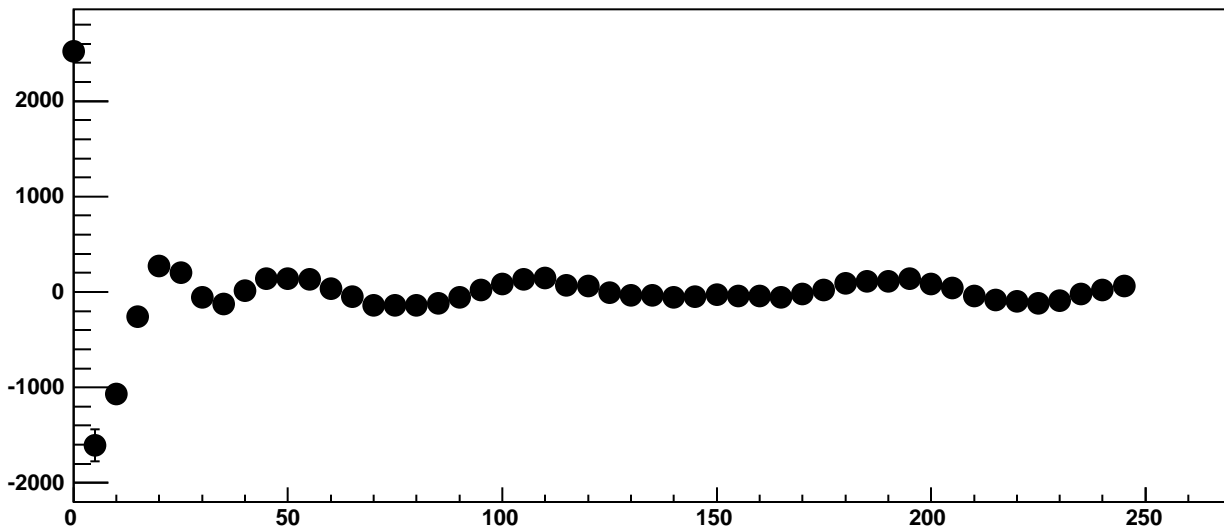


$\chi^2 / \text{ndf}$	3689 / 42
p0	$-3556 \pm 3.441$
p1	$1.655 \pm 0.01329$
p2	$3.077\text{e}+04 \pm 4.31$
p3	$28.53 \pm 0.009372$

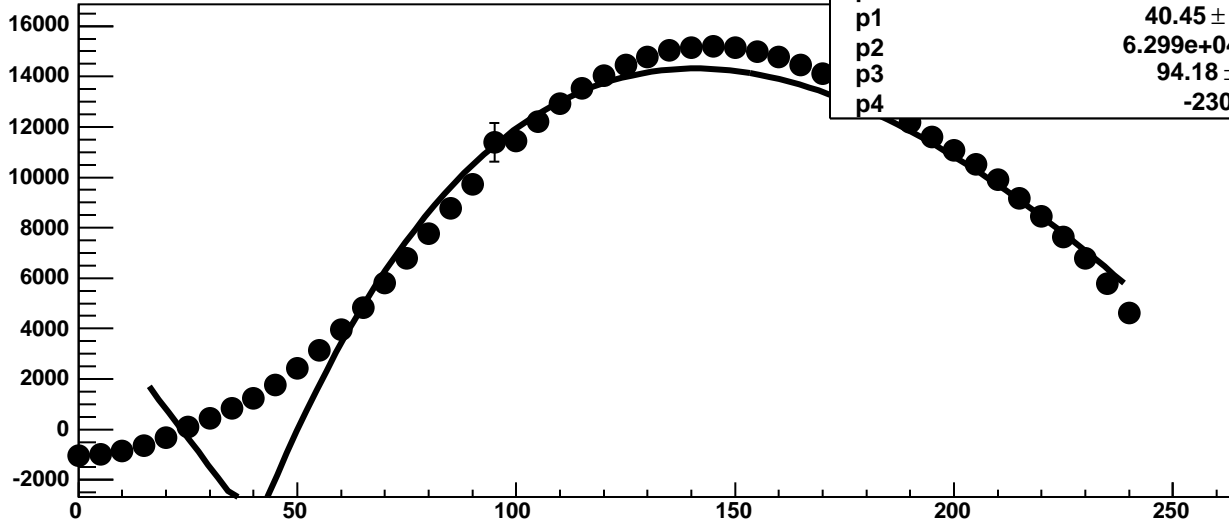
Chip 0, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

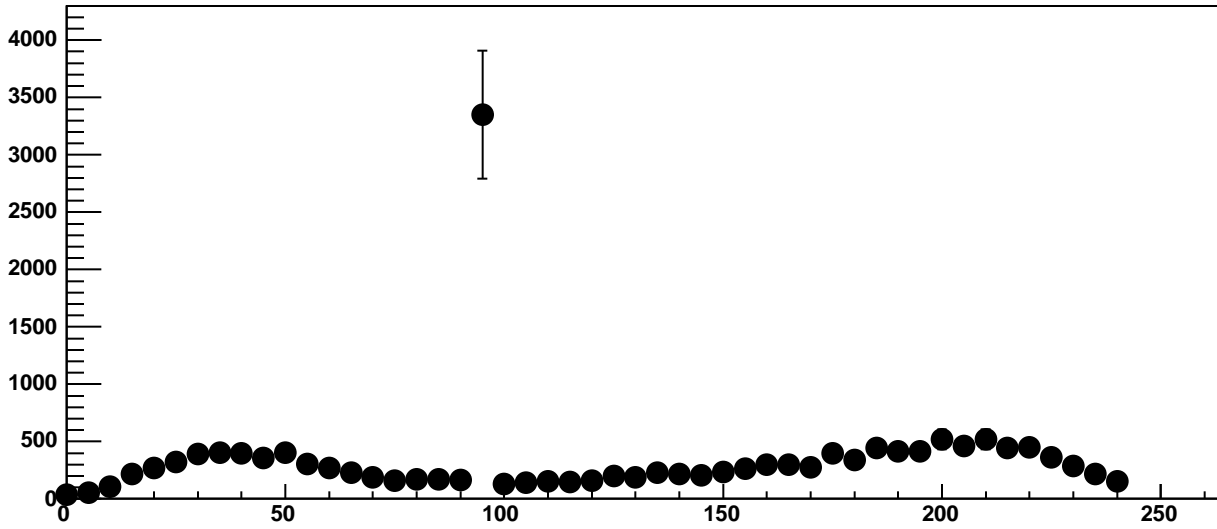


Chip 0, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

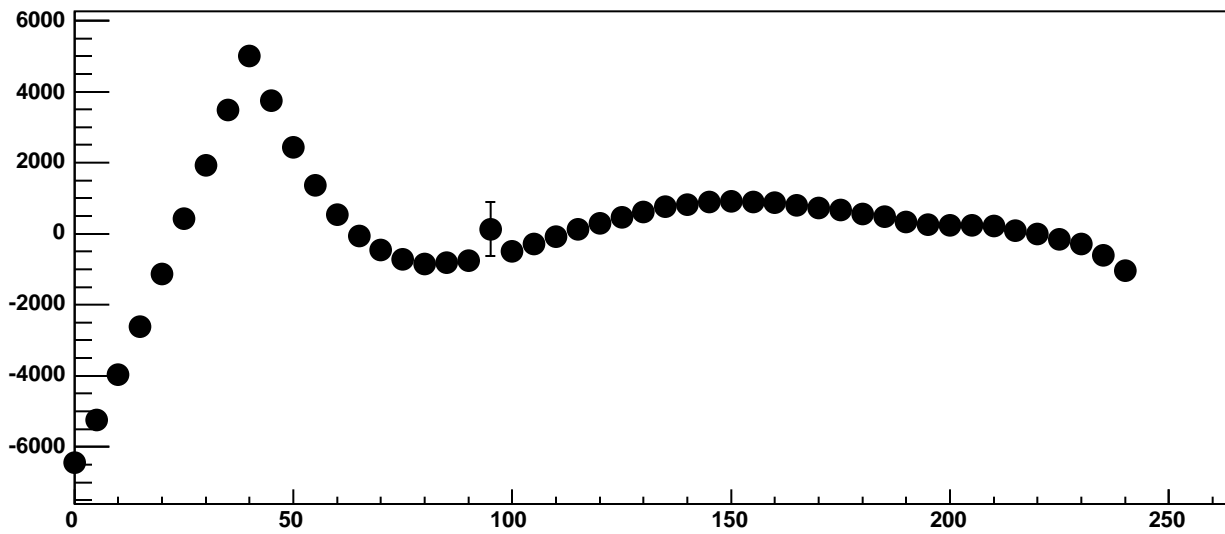


$\chi^2 / \text{ndf}$	1.67e+04 / 41
p0	-3894 ± 26.9
p1	40.45 ± 0.09487
p2	6.299e+04 ± 496
p3	94.18 ± 0.6185
p4	-230 ± 1.609

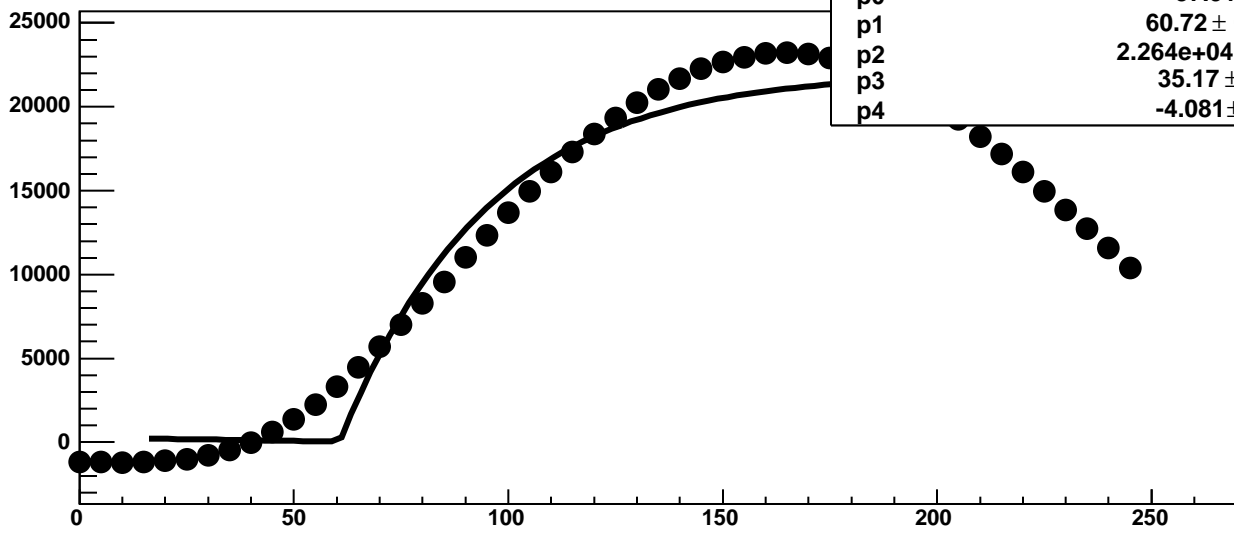
Chip 0, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold

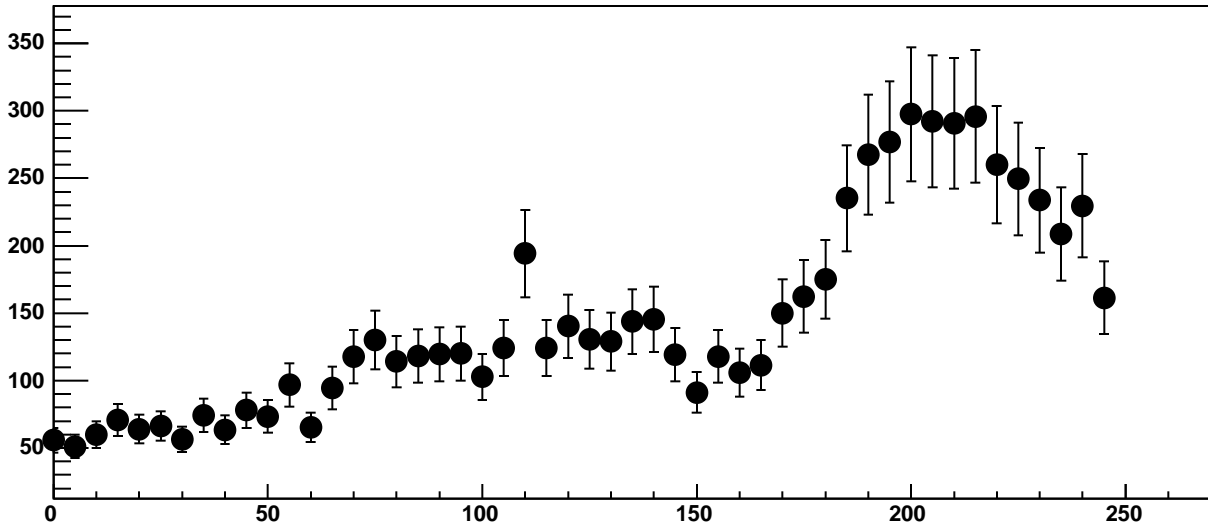


Chip 0, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

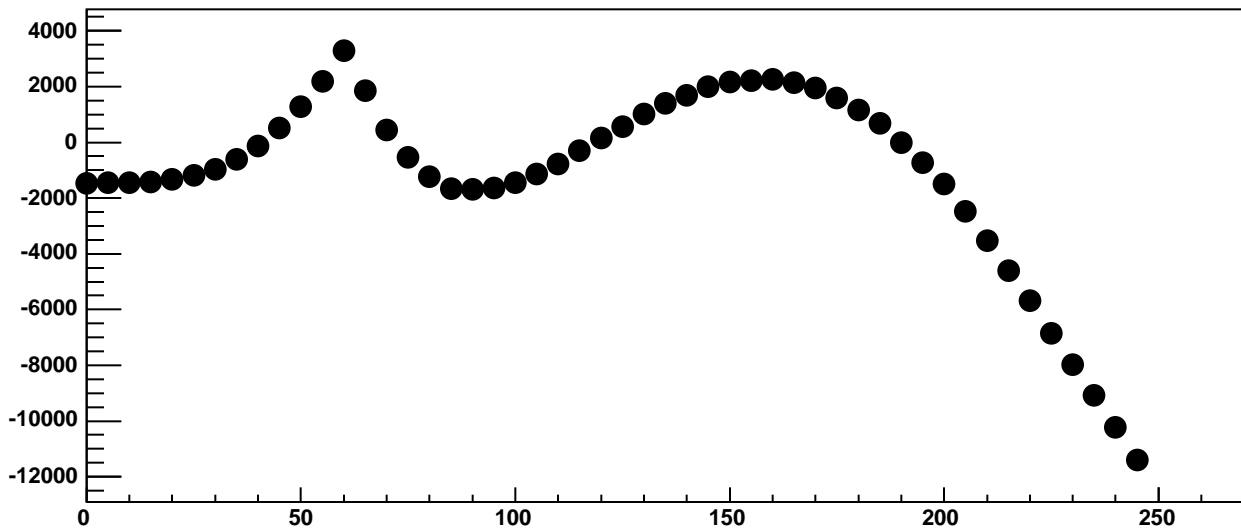


$\chi^2 / \text{ndf}$	2.987e+05 / 41
p0	37.91 ± 7.837
p1	60.72 ± 0.03415
p2	2.264e+04 ± 40.74
p3	35.17 ± 0.0806
p4	-4.081 ± 0.2472

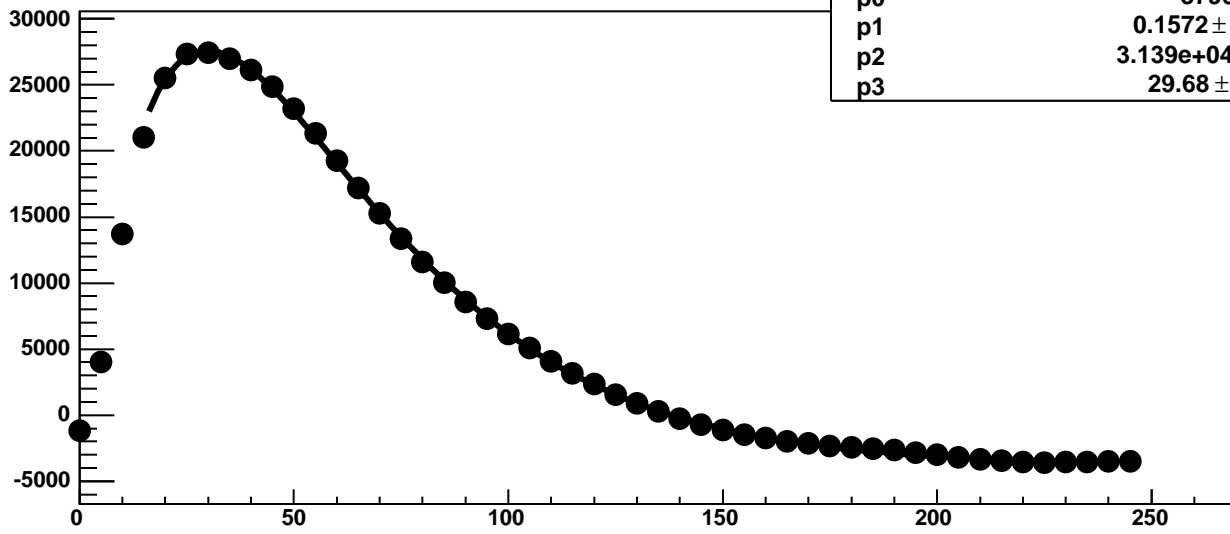
Chip 0, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

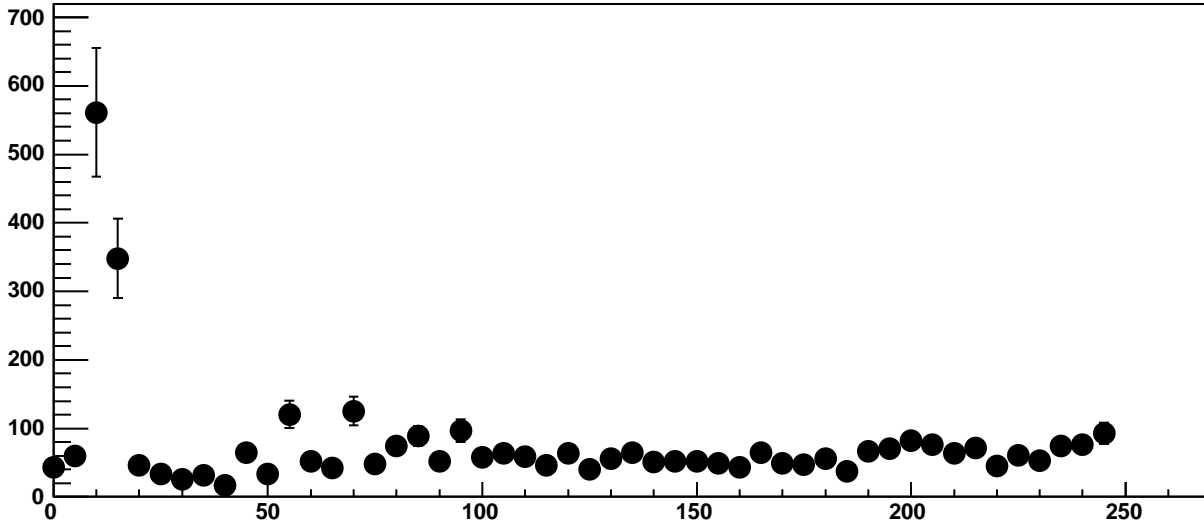


Chip 0, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold

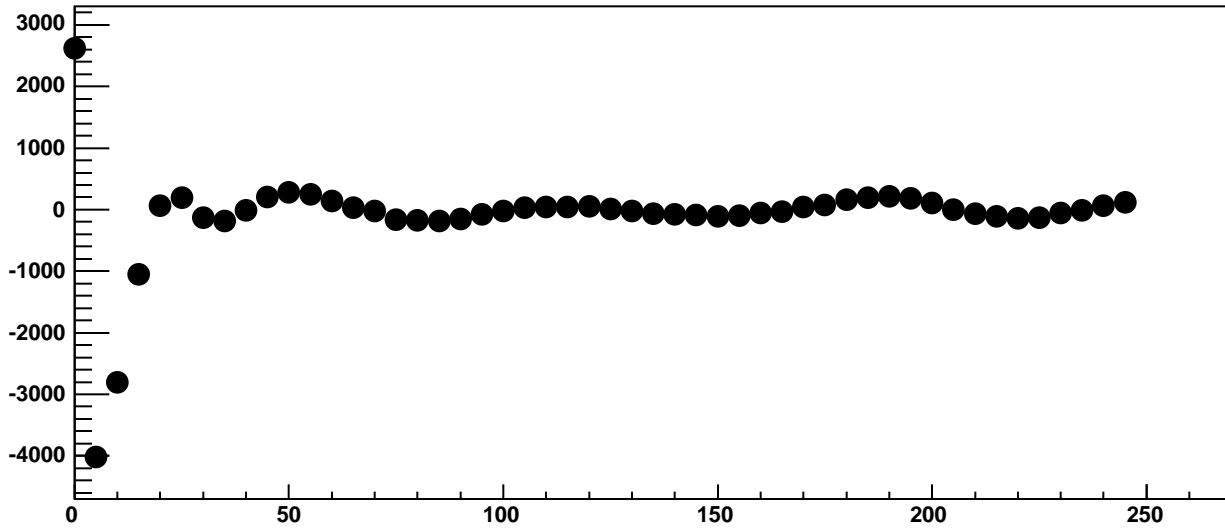


$\chi^2 / \text{ndf}$  6094 / 42  
p0  $-3790 \pm 3.903$   
p1  $0.1572 \pm 0.01956$   
p2  $3.139\text{e}+04 \pm 4.557$   
p3  $29.68 \pm 0.01139$

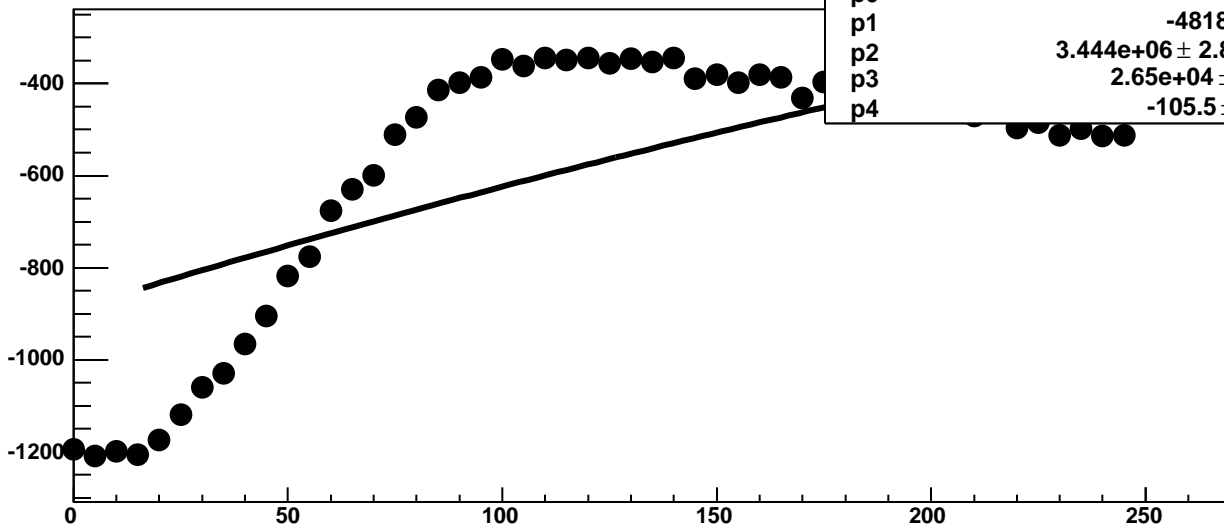
Chip 0, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

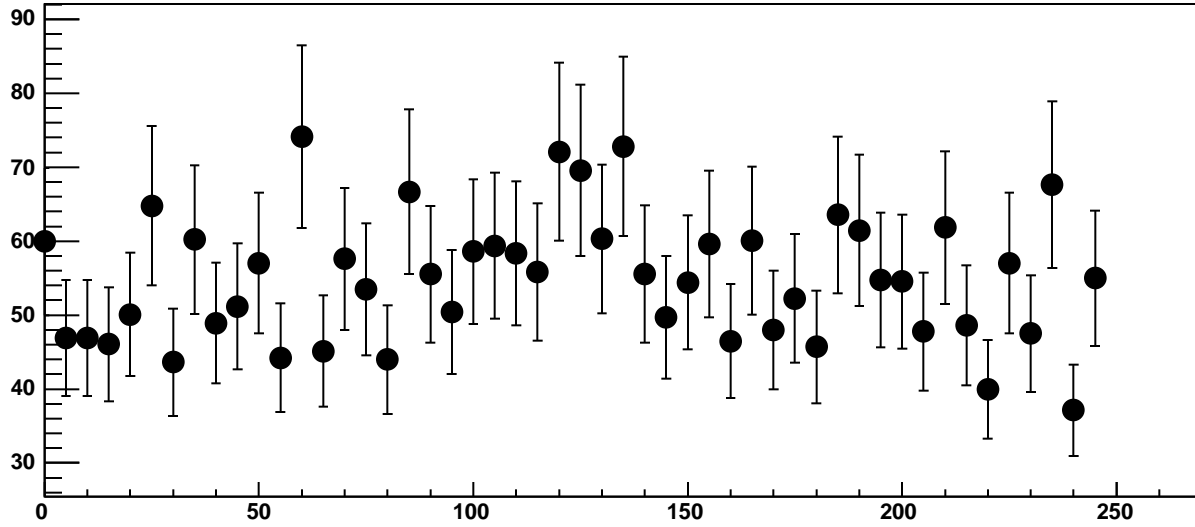


Chip 0, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

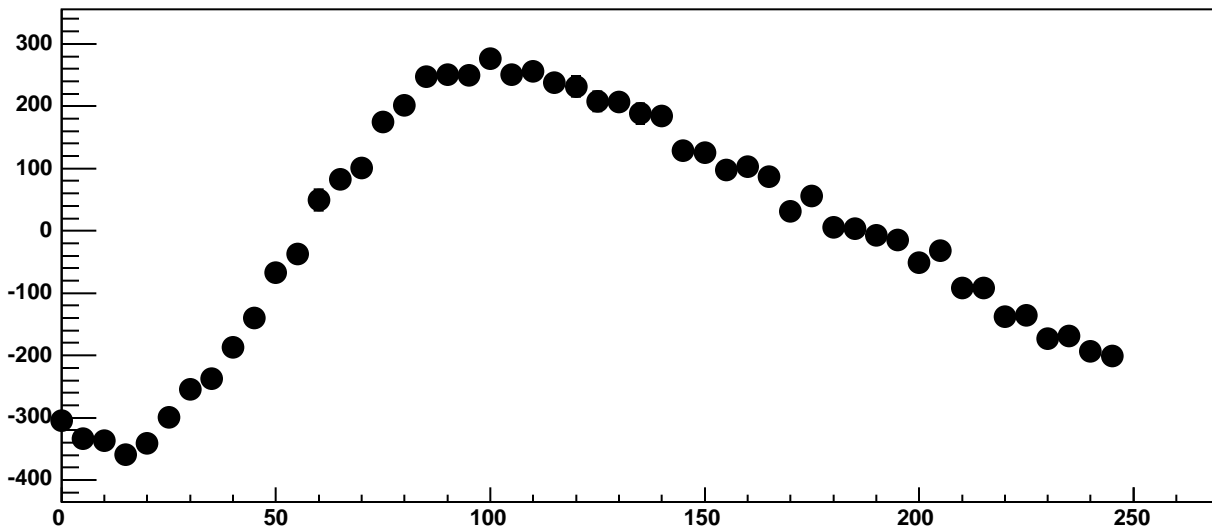


$\chi^2 / \text{ndf}$	9878 / 41
p0	$-6.513\text{e}+04 \pm 471.2$
p1	$-4818 \pm 6.606$
p2	$3.444\text{e}+06 \pm 2.848\text{e}+04$
p3	$2.65\text{e}+04 \pm 0.8164$
p4	$-105.5 \pm 0.8852$

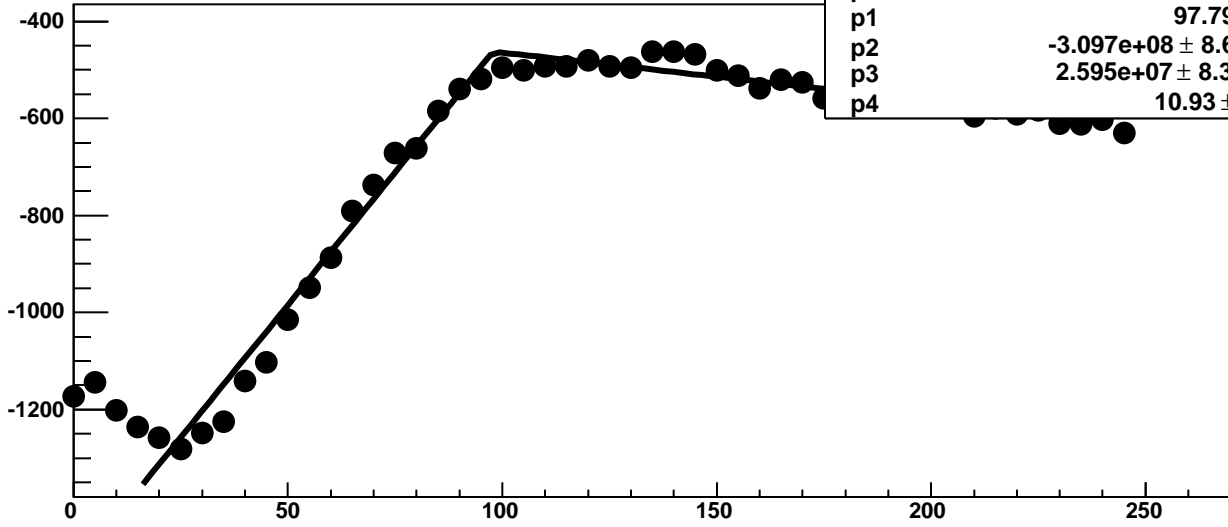
Chip 0, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

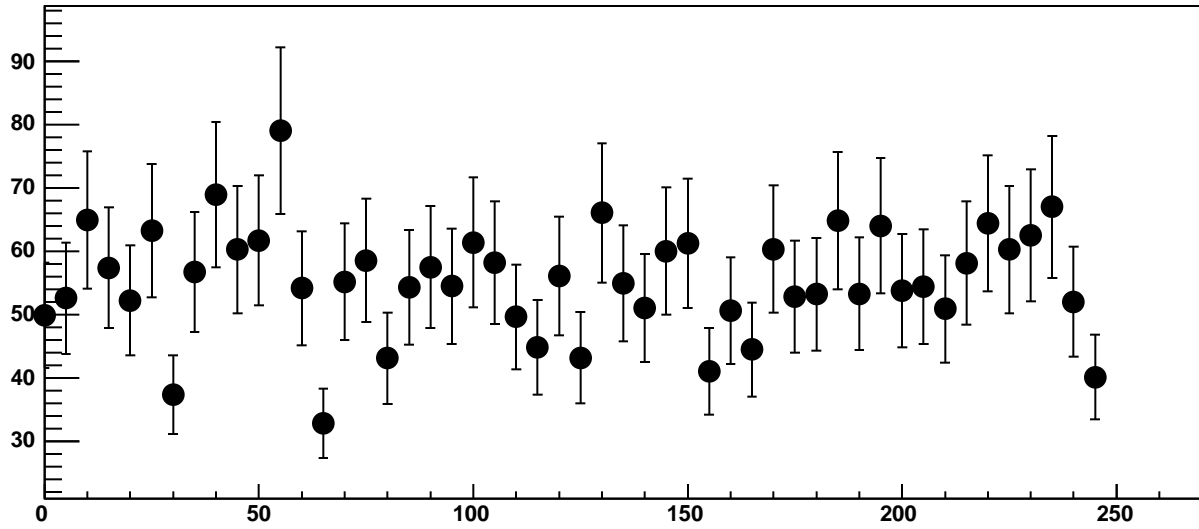


Chip 0, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

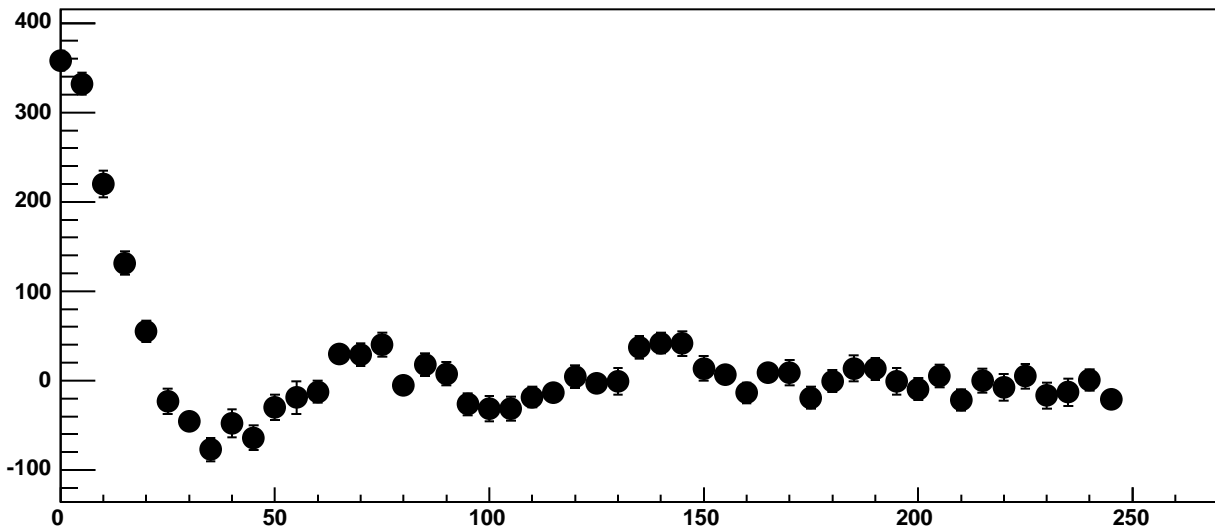


$\chi^2 / \text{ndf}$	321.5 / 41
p0	-461.9 ± 4.07
p1	97.79 ± 0.57
p2	-3.097e+08 ± 8.617e+06
p3	2.595e+07 ± 8.383e+05
p4	10.93 ± 0.1124

Chip 0, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

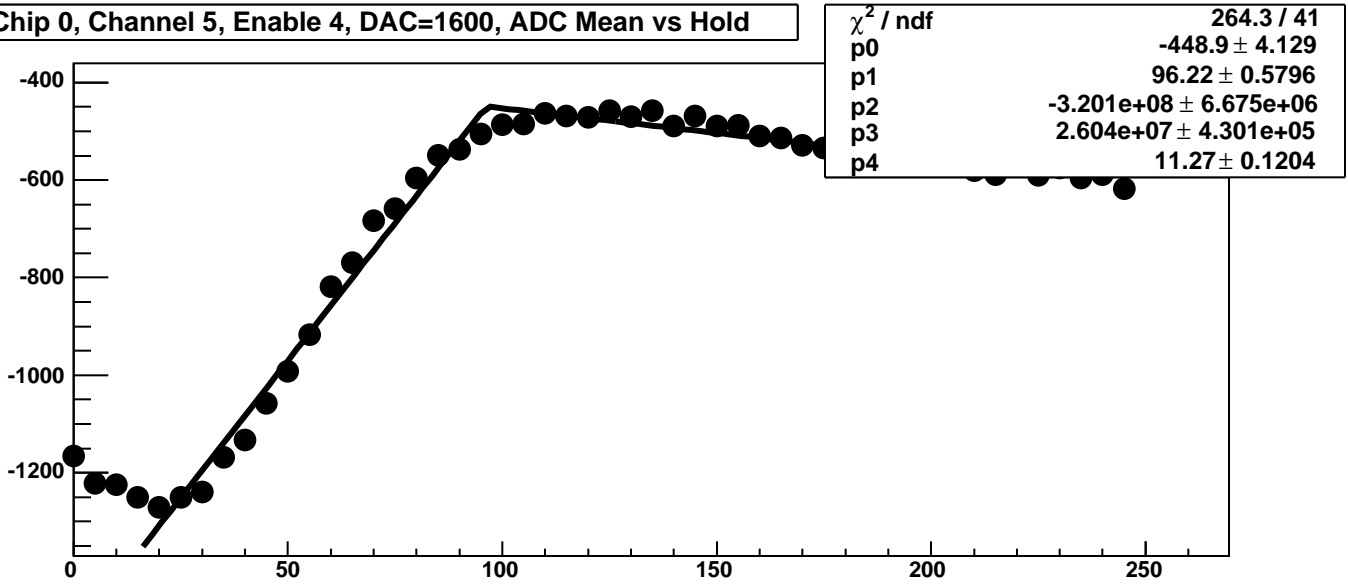


Chip 0, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

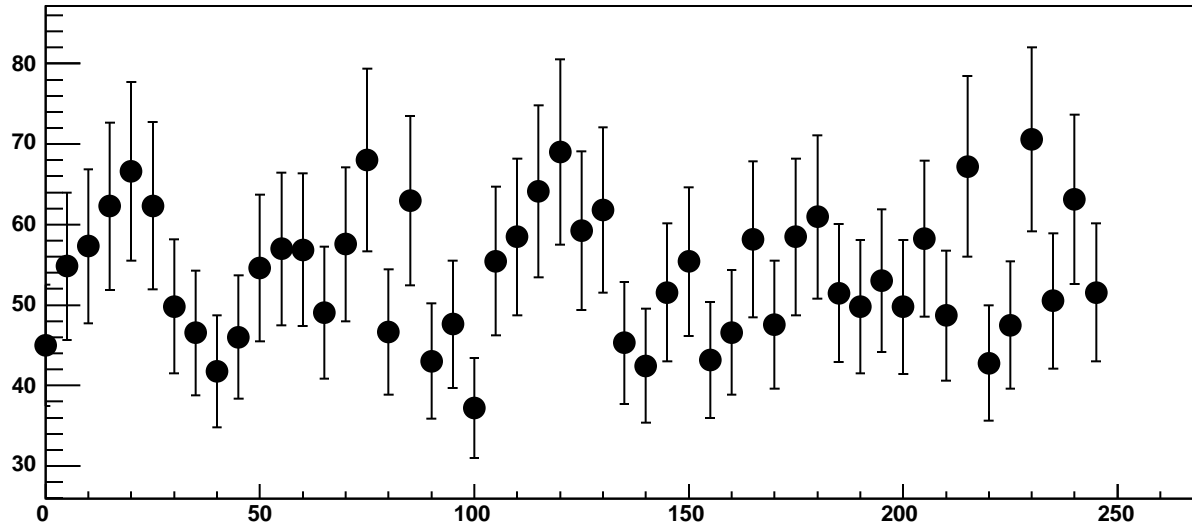




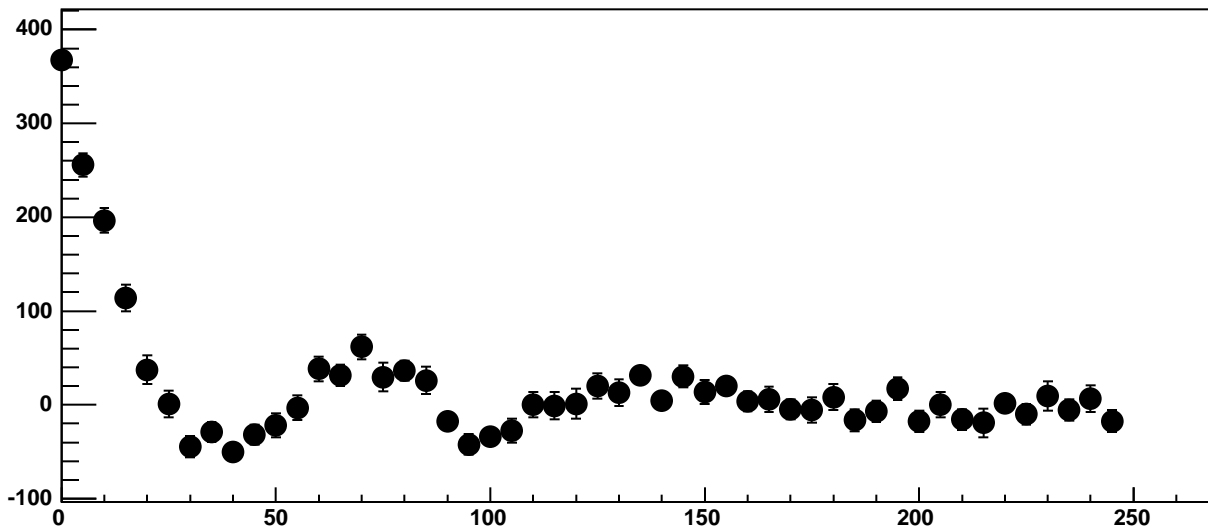
Chip 0, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold



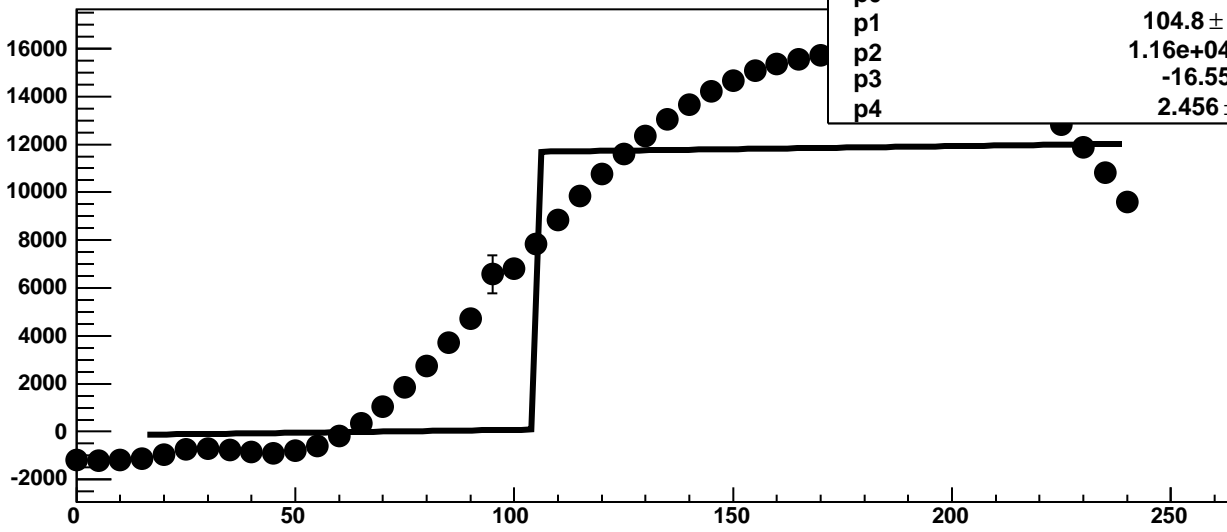
Chip 0, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



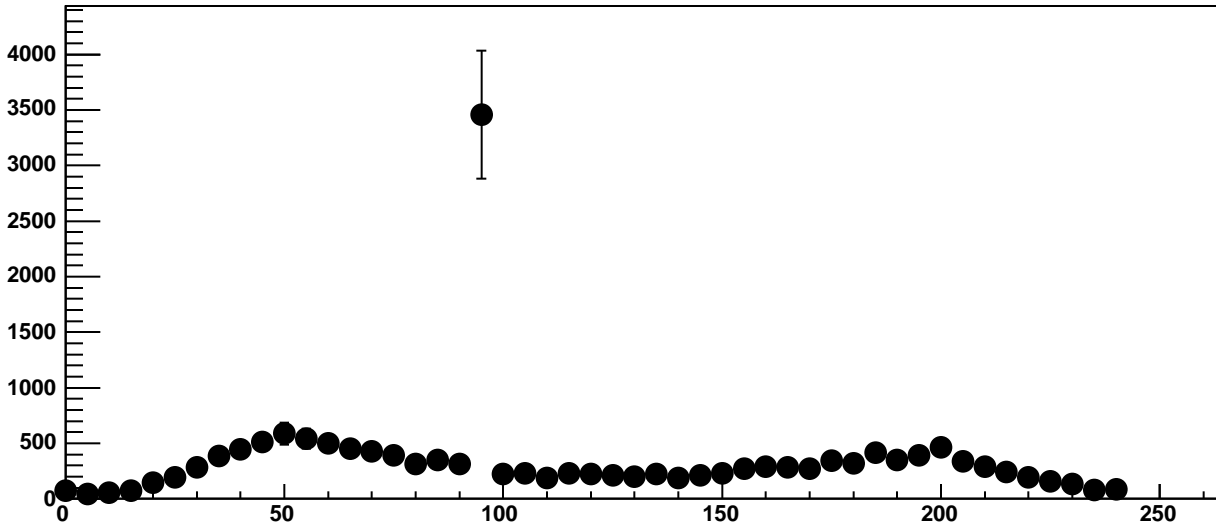
Chip 0, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold



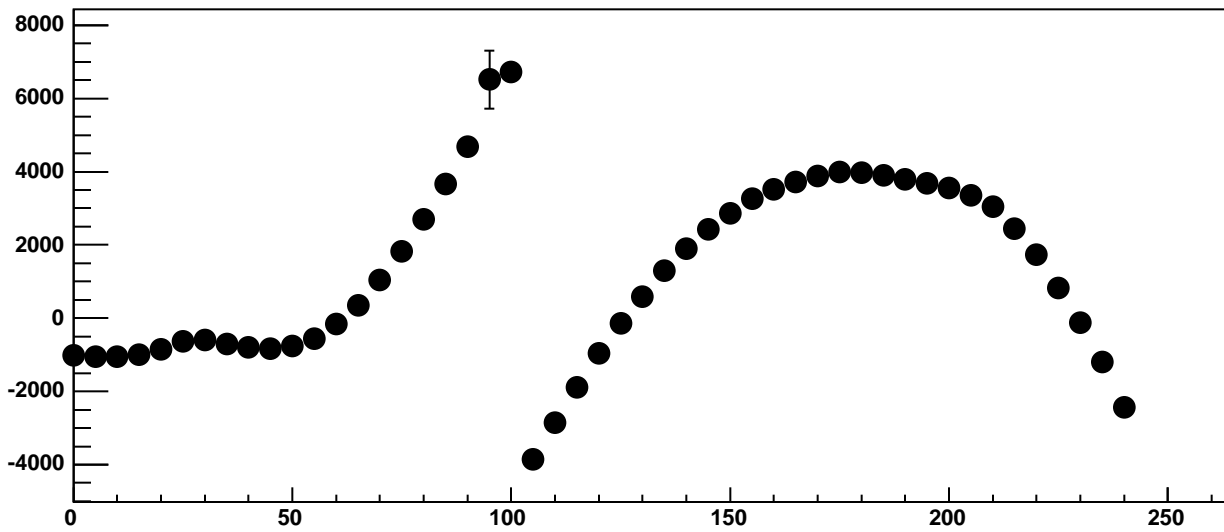
Chip 0, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold



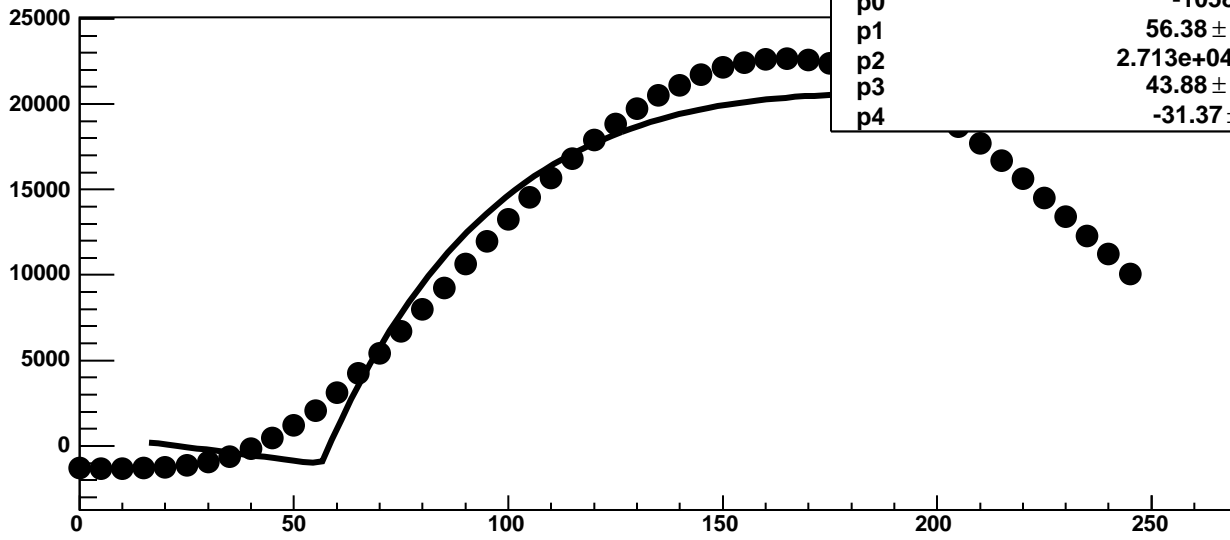
Chip 0, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

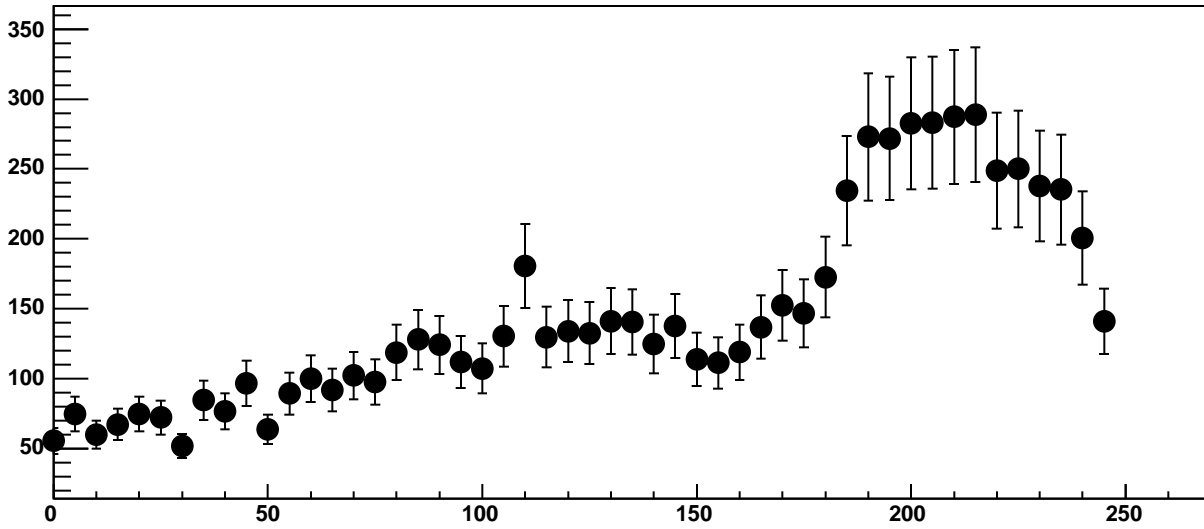


Chip 0, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

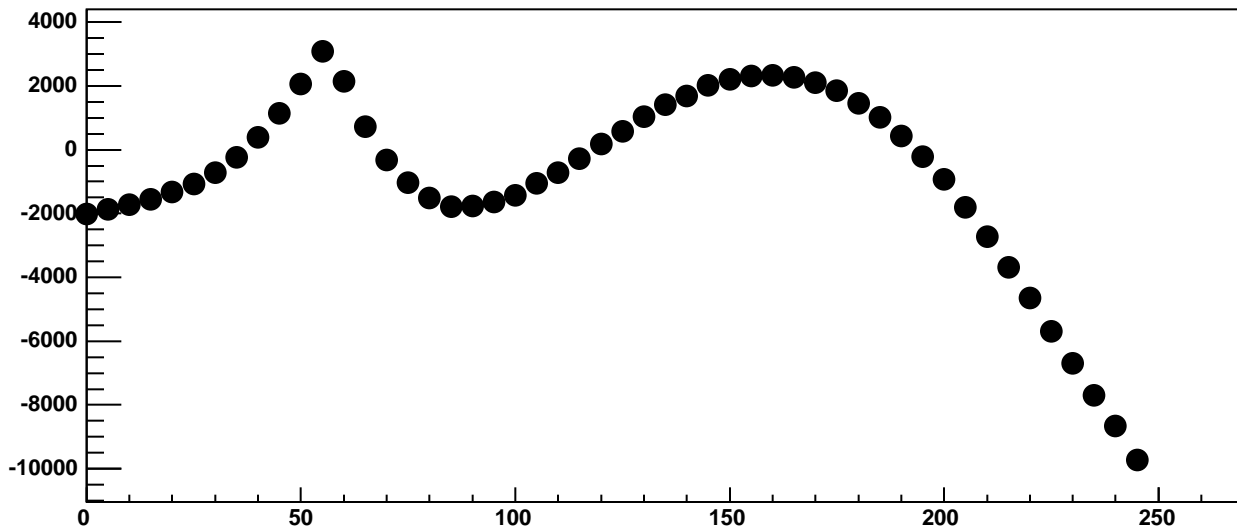


$\chi^2 / \text{ndf}$	2.422e+05 / 41
p0	-1058 ± 8.036
p1	56.38 ± 0.03158
p2	2.713e+04 ± 53.14
p3	43.88 ± 0.09842
p4	-31.37 ± 0.2913

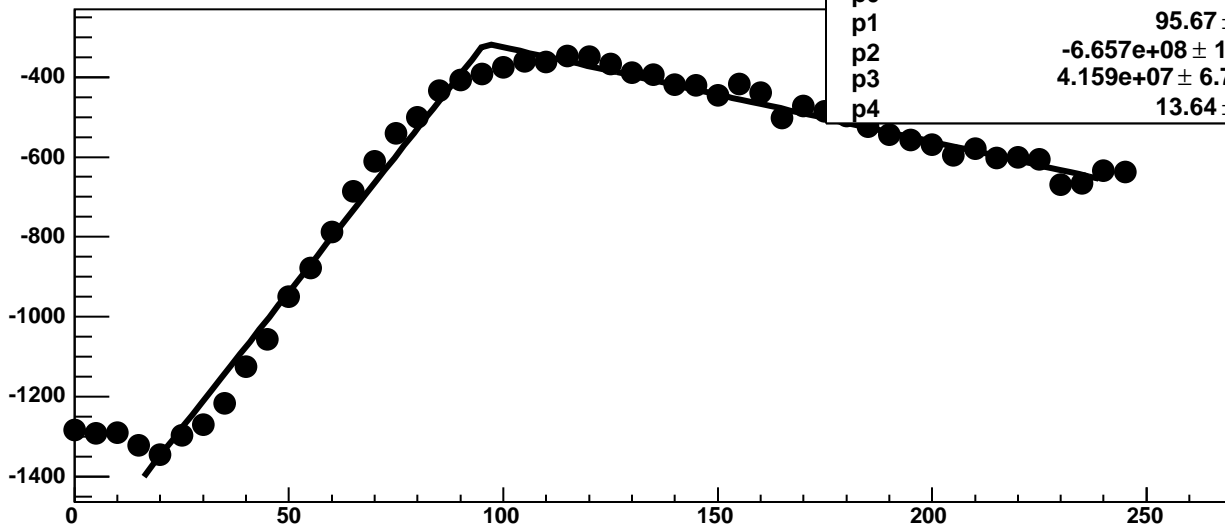
Chip 0, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



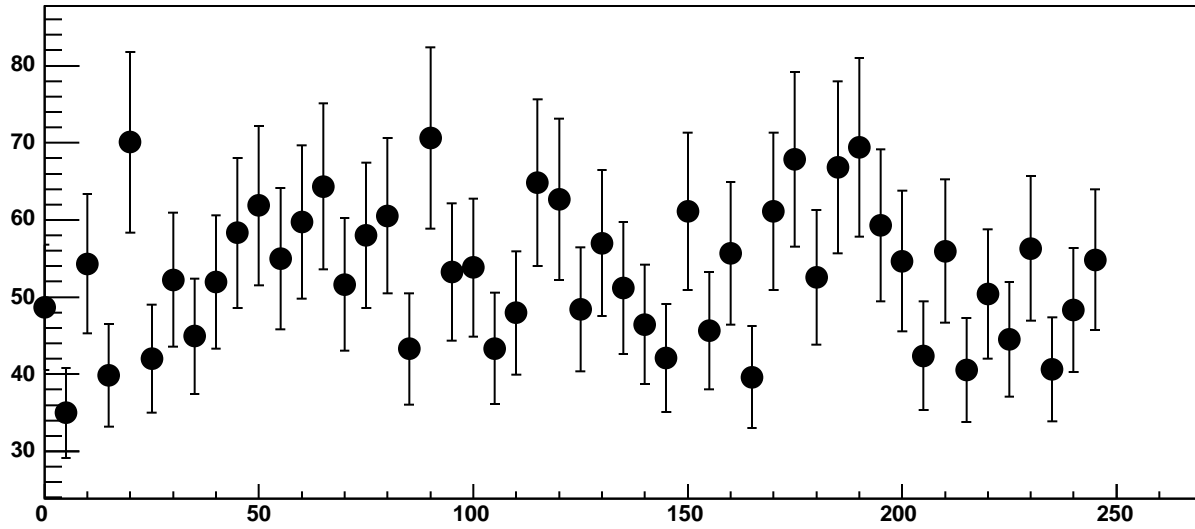
Chip 0, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



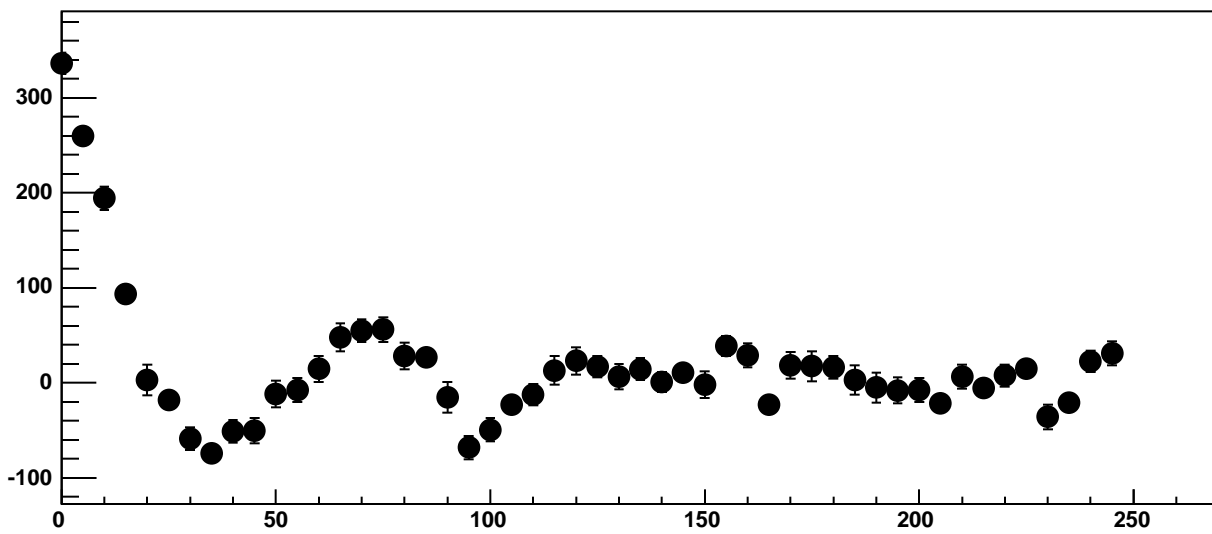
Chip 0, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



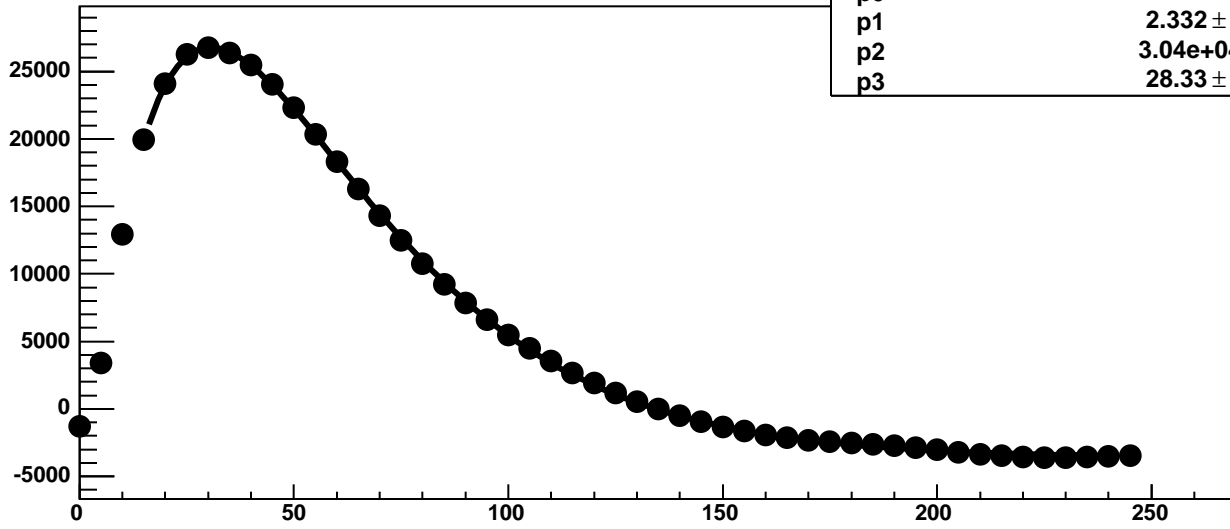
Chip 0, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

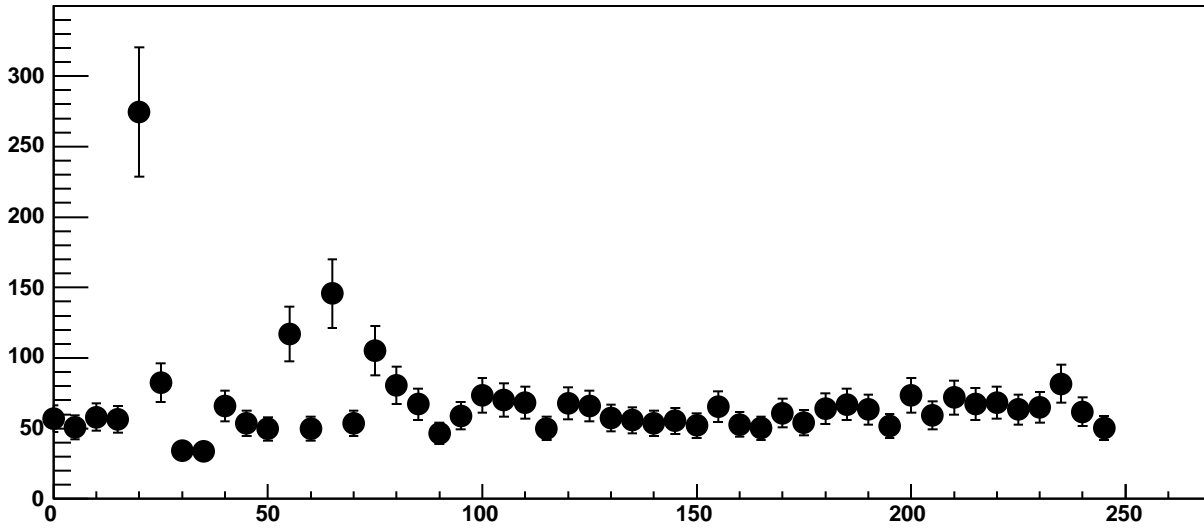


Chip 0, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold

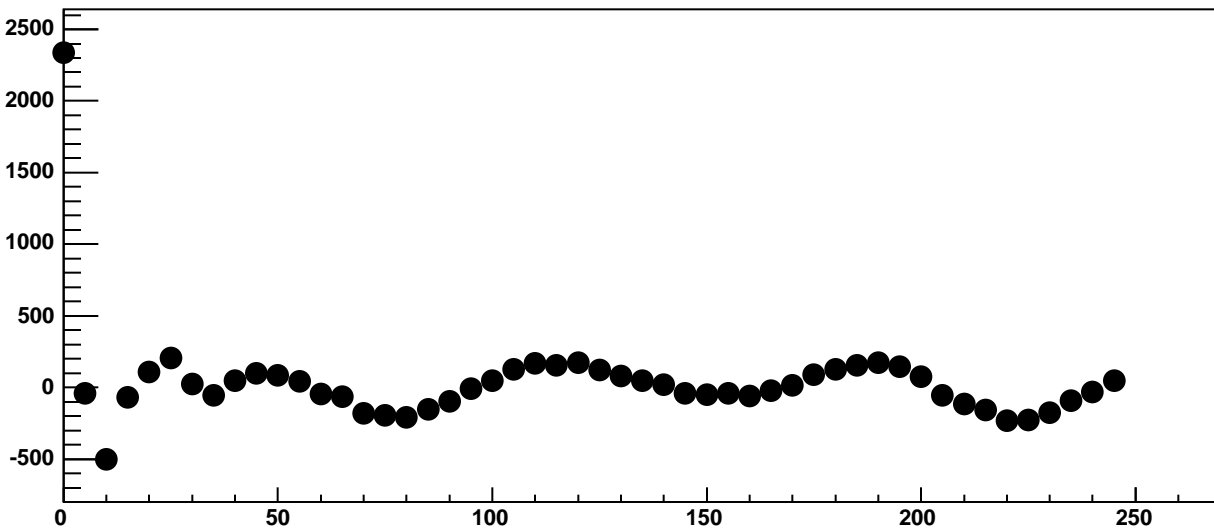


$\chi^2 / \text{ndf}$	2948 / 42
p0	$-3638 \pm 3.961$
p1	$2.332 \pm 0.01527$
p2	$3.04\text{e}+04 \pm 5.38$
p3	$28.33 \pm 0.01053$

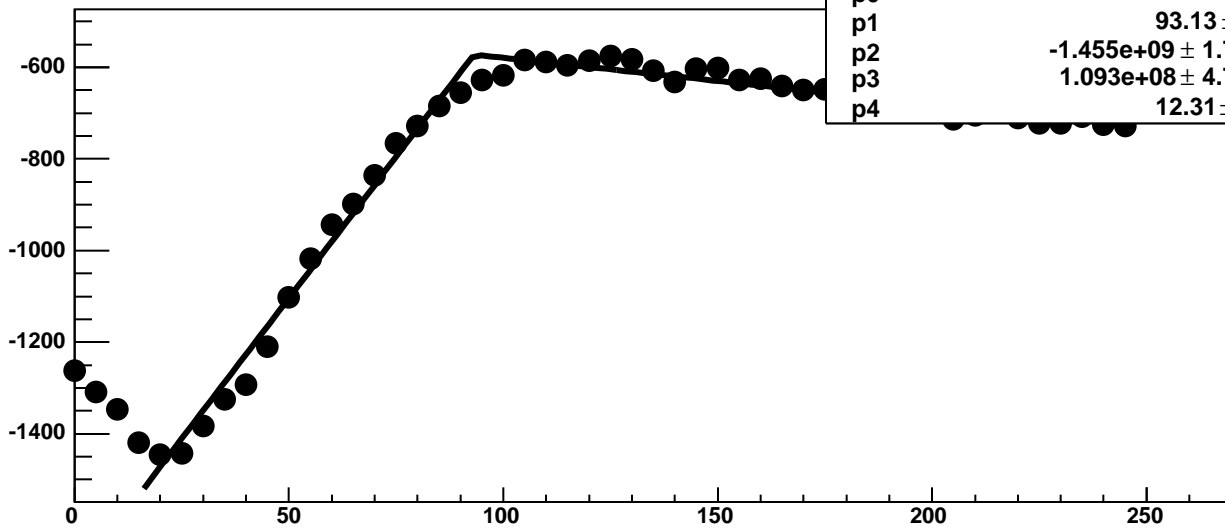
Chip 0, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold

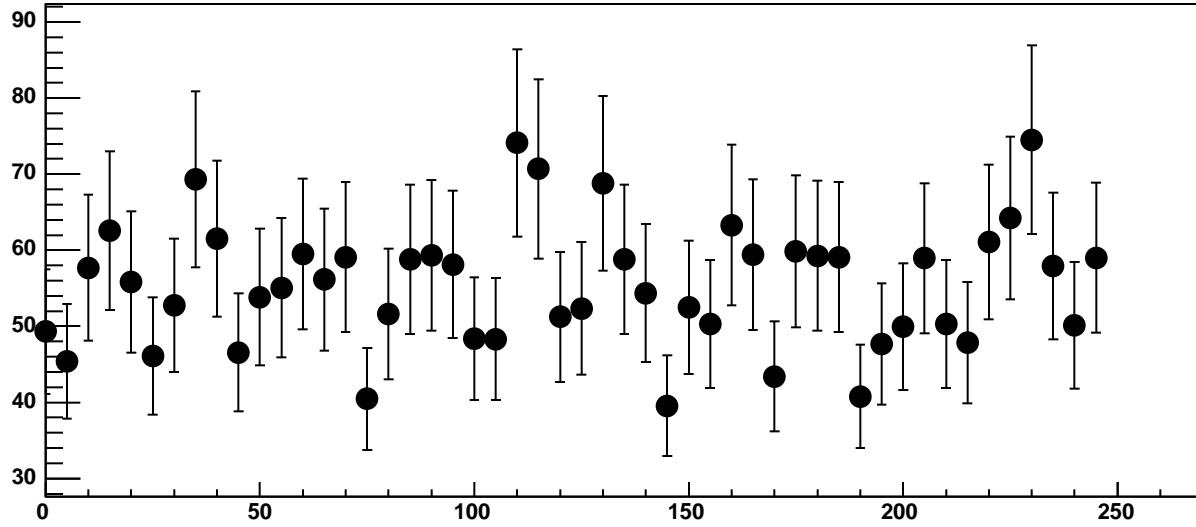


Chip 0, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

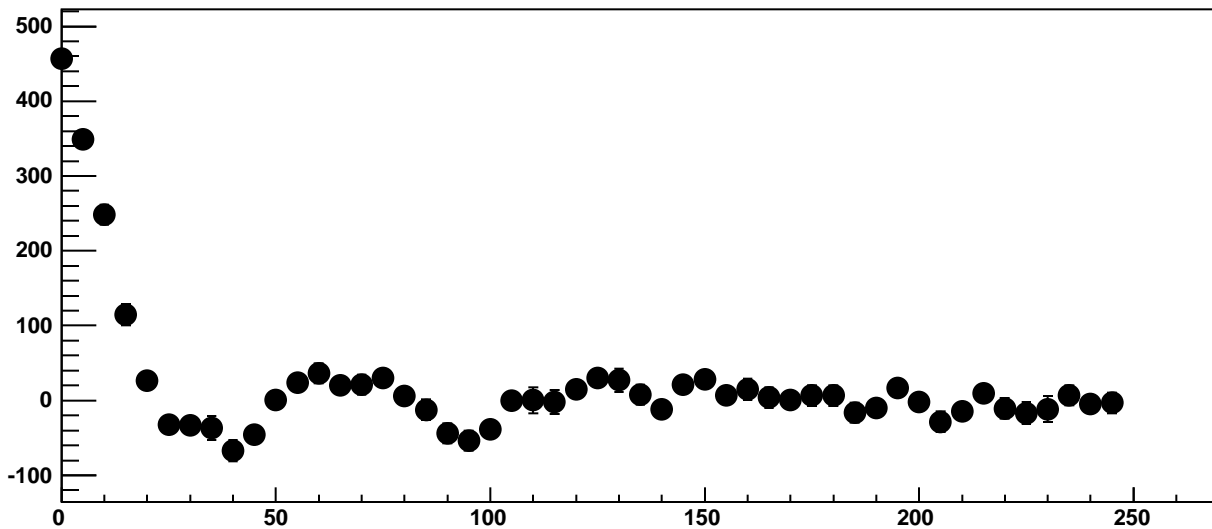


$\chi^2 / \text{ndf}$	236 / 41
p0	$-572.2 \pm 6.988$
p1	$93.13 \pm 0.2022$
p2	$-1.455\text{e}+09 \pm 1.742\text{e}+07$
p3	$1.093\text{e}+08 \pm 4.754\text{e}+06$
p4	$12.31 \pm 0.1356$

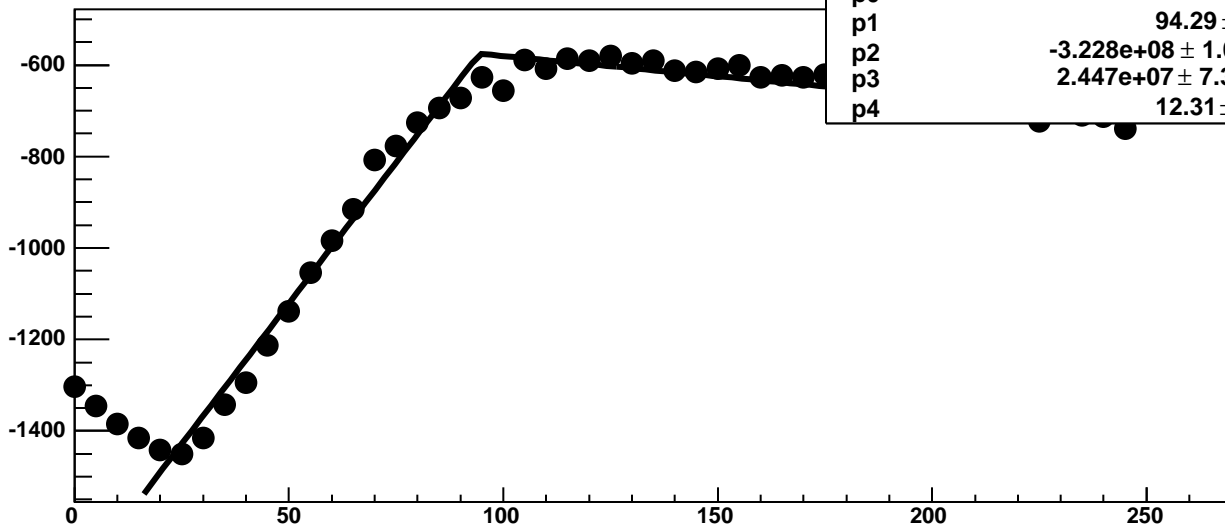
Chip 0, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

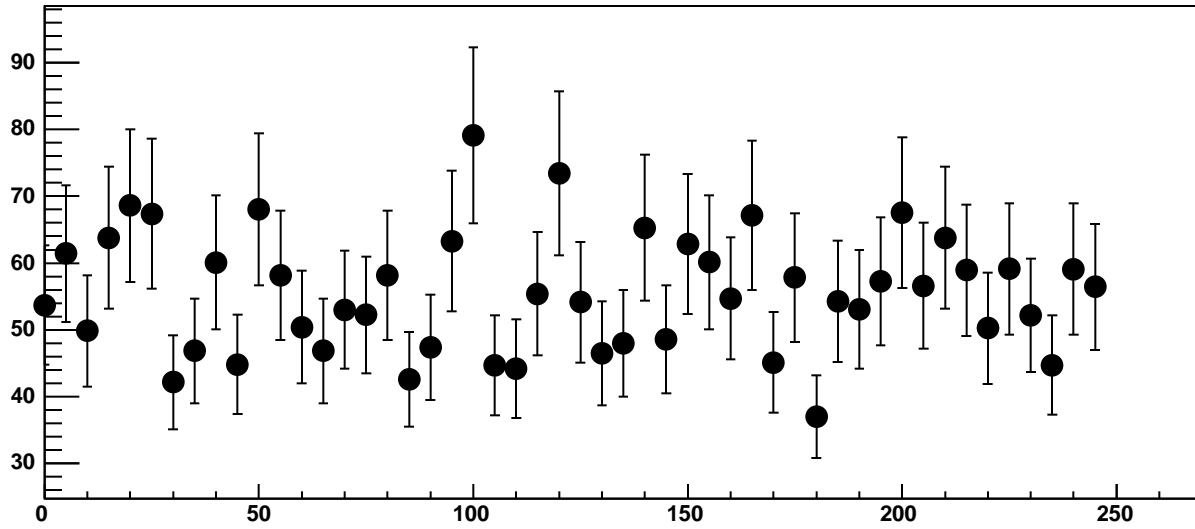


Chip 0, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

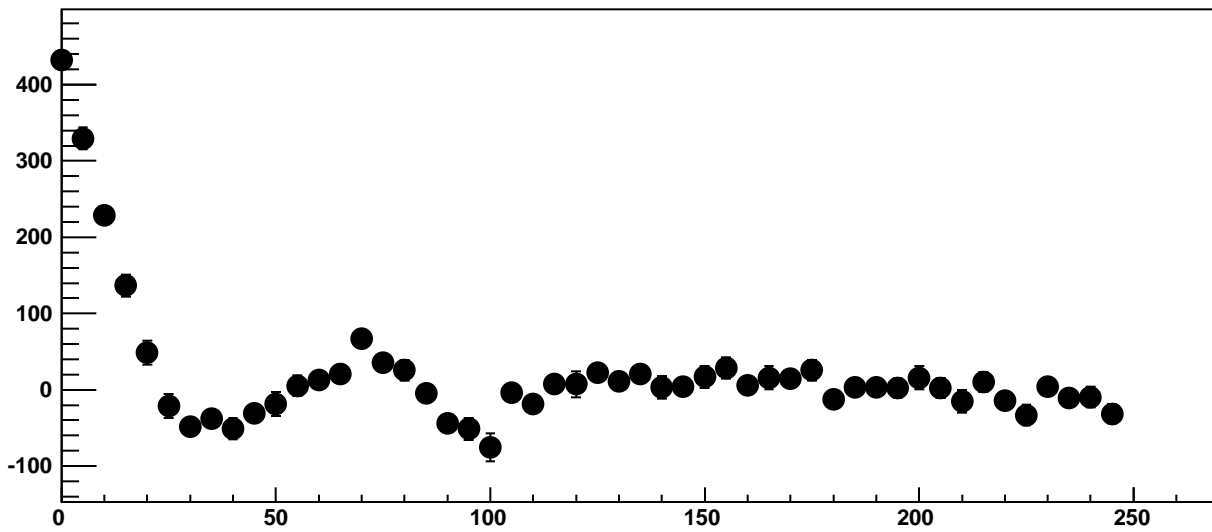


$\chi^2 / \text{ndf}$	292.7 / 41
p0	-575.4 ± 4.233
p1	94.29 ± 0.5658
p2	-3.228e+08 ± 1.069e+07
p3	2.447e+07 ± 7.352e+05
p4	12.31 ± 0.1324

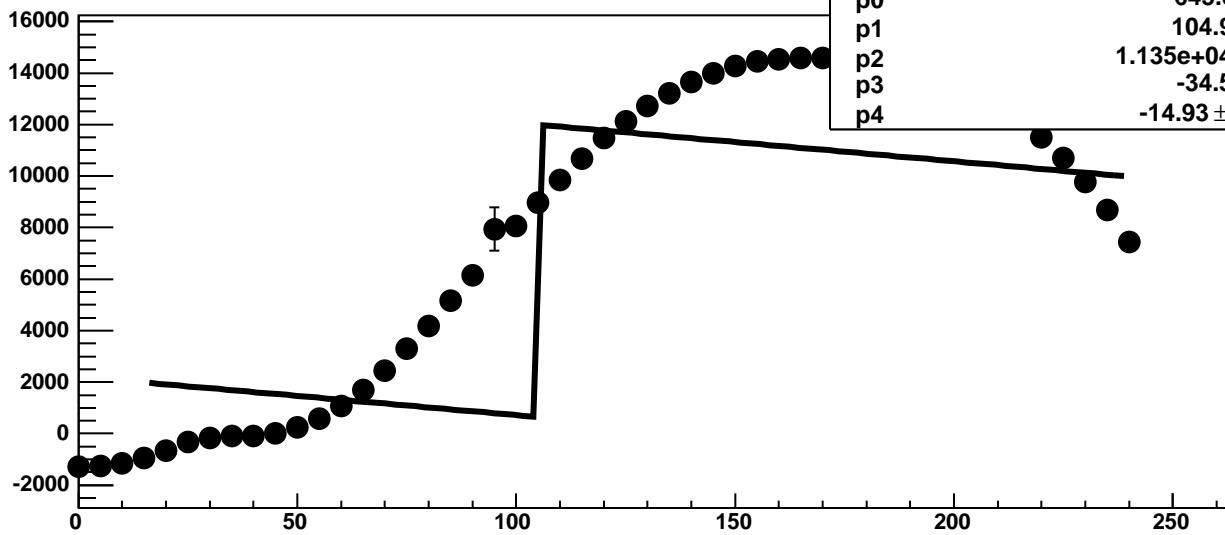
Chip 0, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

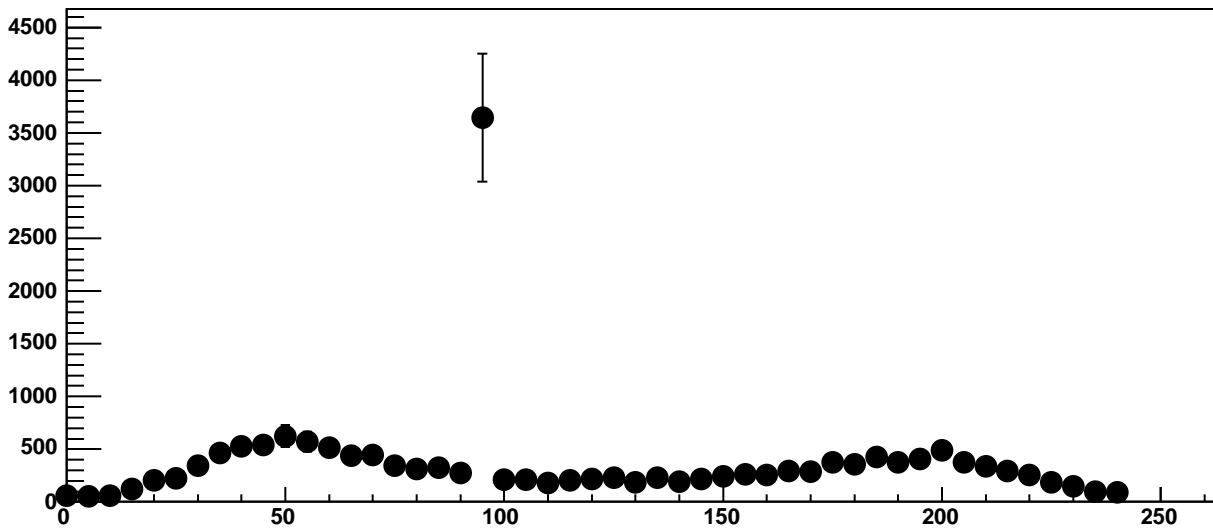


Chip 0, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold

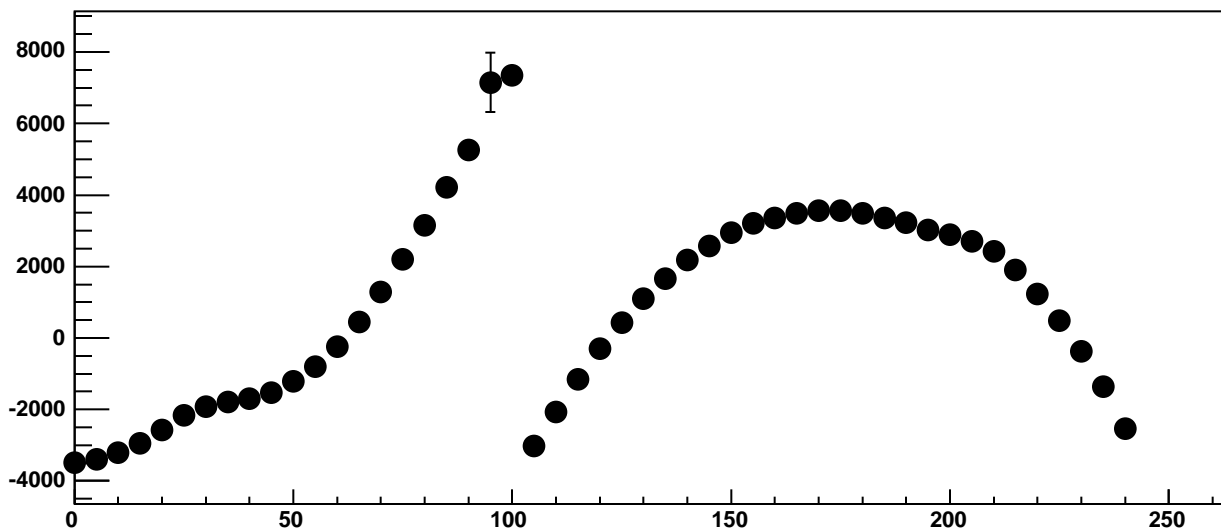


$\chi^2 / \text{ndf}$	1.106e+05 / 41
p0	645.8 ± 1.501
p1	104.9 ± 1.745
p2	1.135e+04 ± 1.579
p3	-34.5 ± 1.256
p4	-14.93 ± 0.01341

Chip 0, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

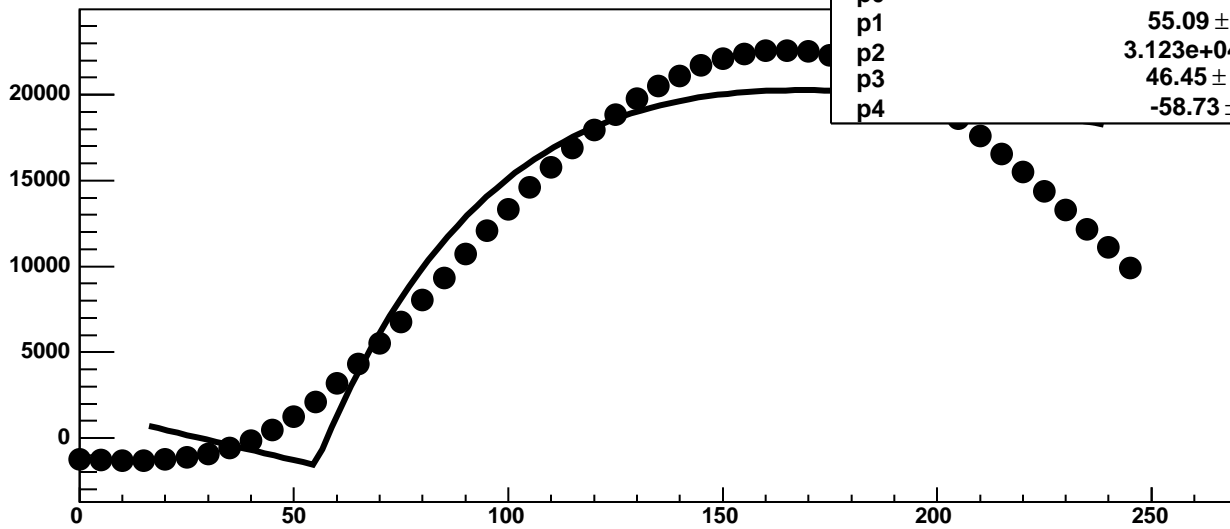


Chip 0, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold



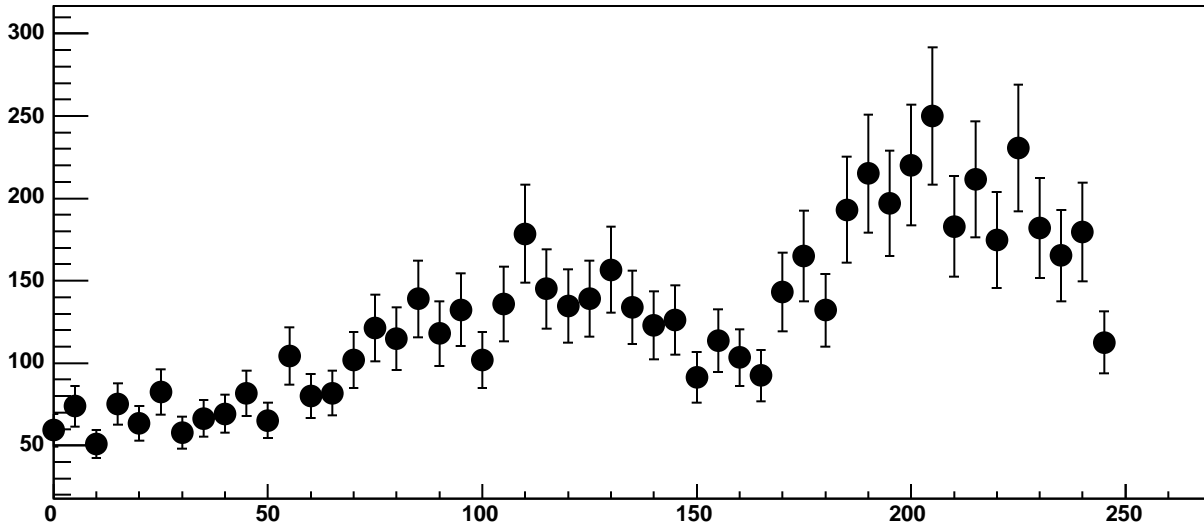


Chip 0, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

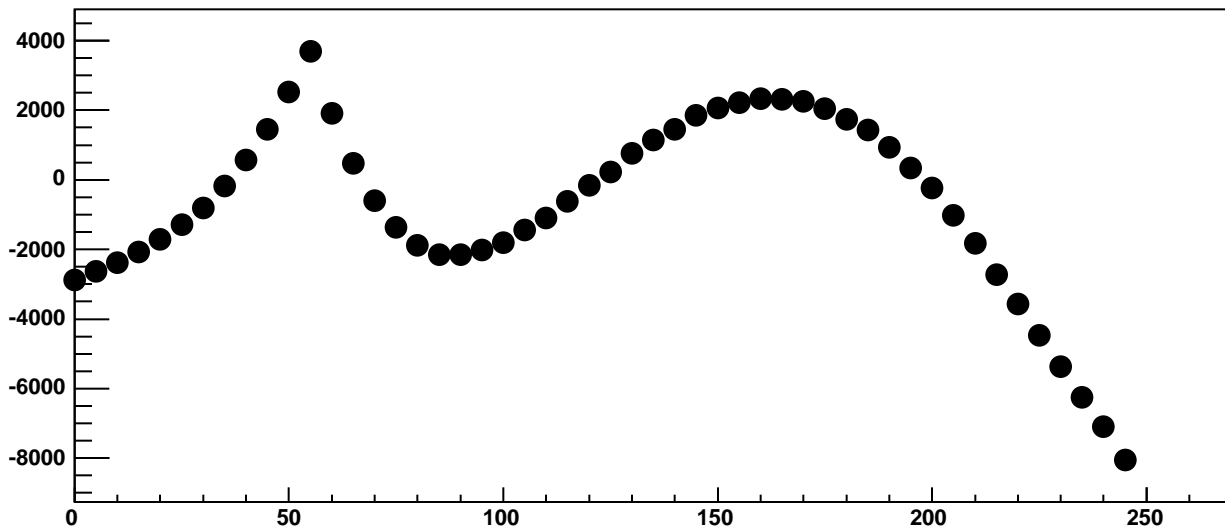


$\chi^2 / \text{ndf}$	2.936e+05 / 41
p0	-1588 ± 7.581
p1	55.09 ± 0.02721
p2	3.123e+04 ± 54.9
p3	46.45 ± 0.09096
p4	-58.73 ± 0.2876

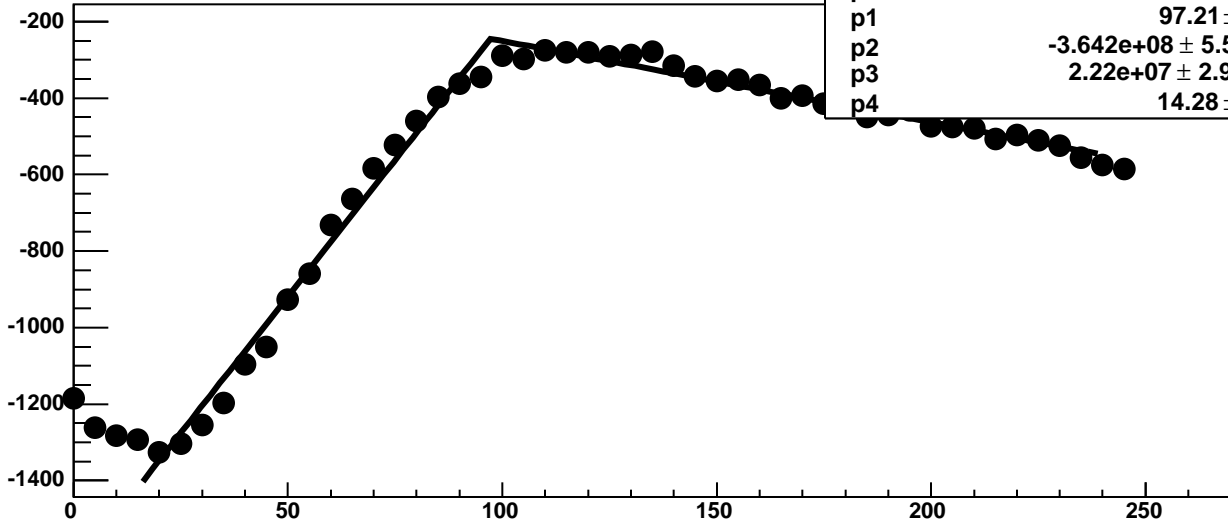
Chip 0, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

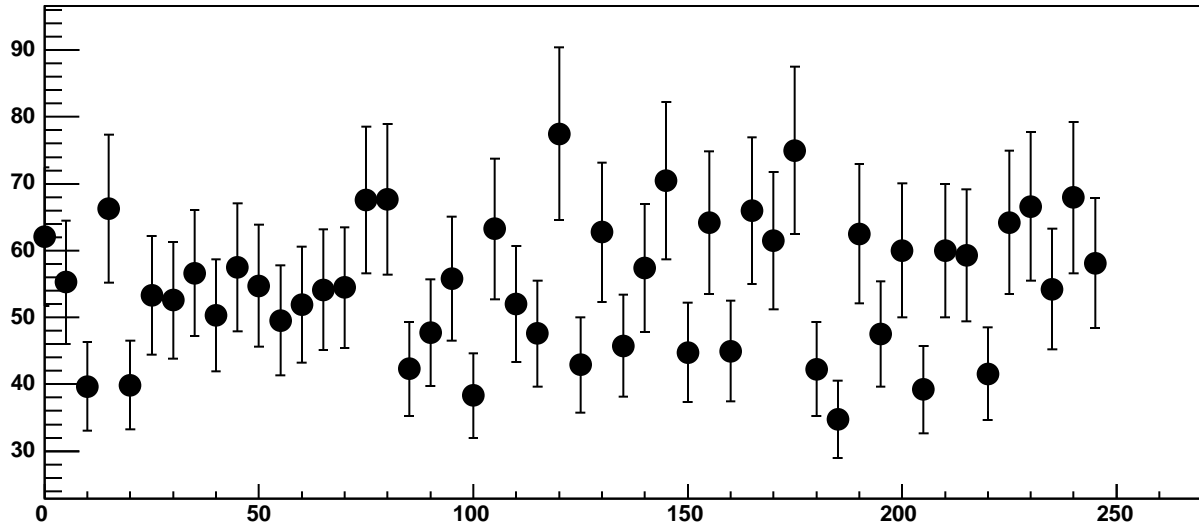


Chip 0, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

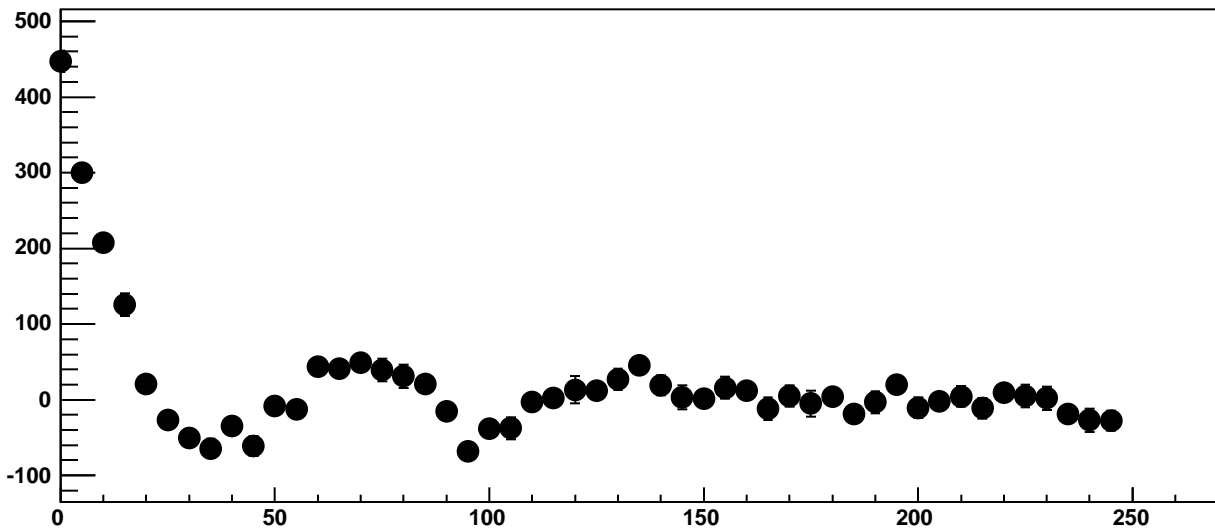


$\chi^2 / \text{ndf}$	311.1 / 41
p0	-244.6 ± 3.889
p1	97.21 ± 0.4421
p2	-3.642e+08 ± 5.594e+06
p3	2.22e+07 ± 2.949e+05
p4	14.28 ± 0.1171

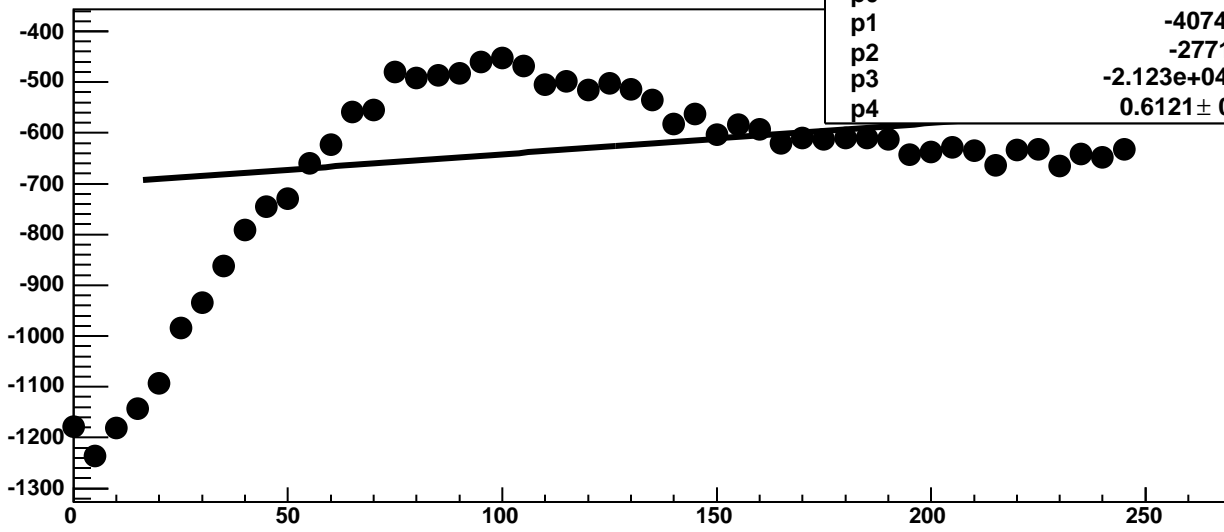
Chip 0, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

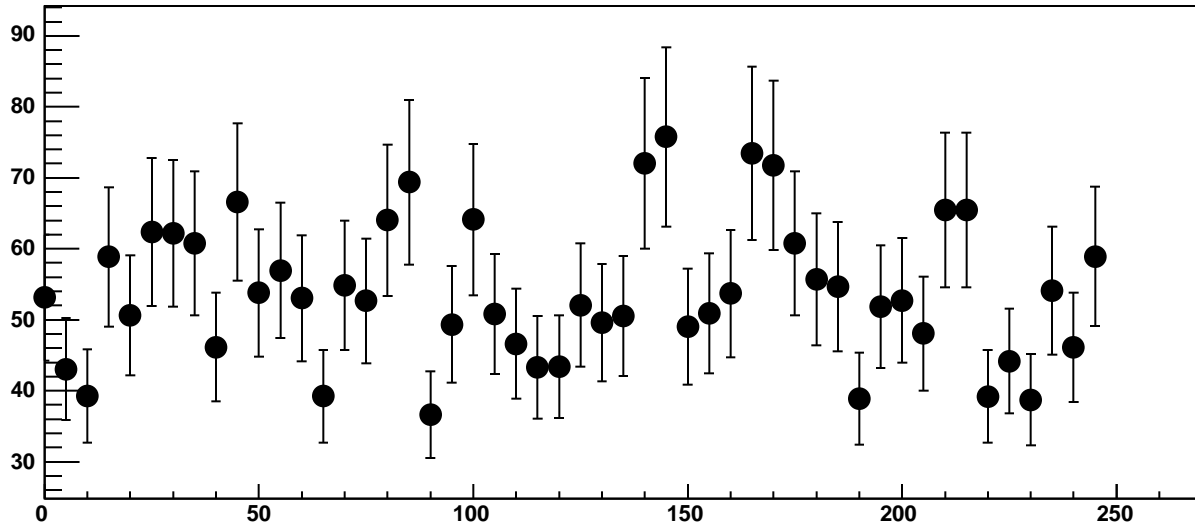


Chip 0, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold

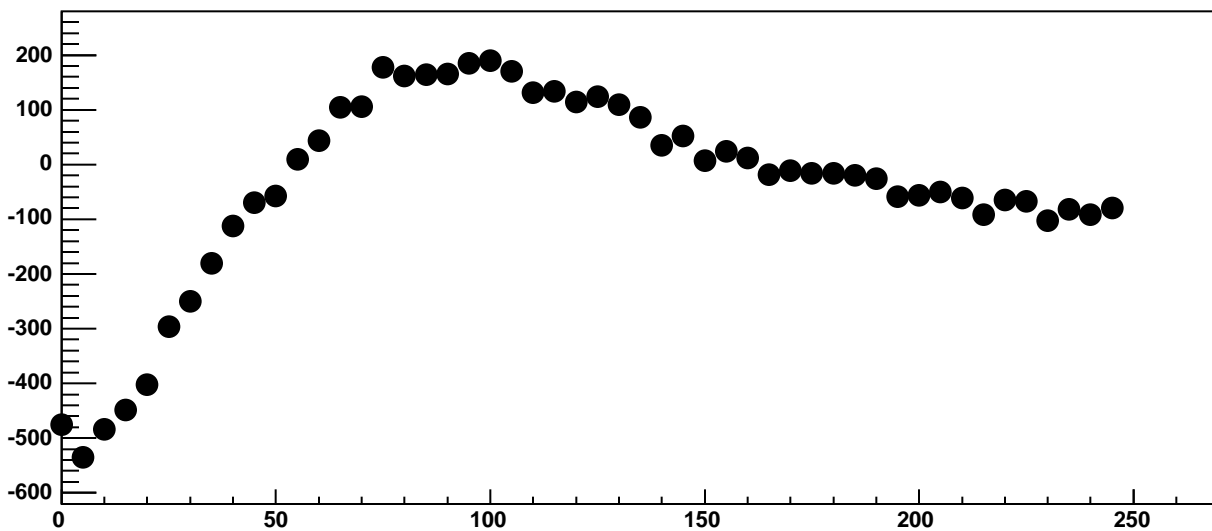


$\chi^2 / \text{ndf}$	6283 / 41
p0	$-426 \pm 7.66$
p1	$-4074 \pm 5.087$
p2	$-2771 \pm 6.398$
p3	$-2.123\text{e}+04 \pm 7686$
p4	$0.6121 \pm 0.001811$

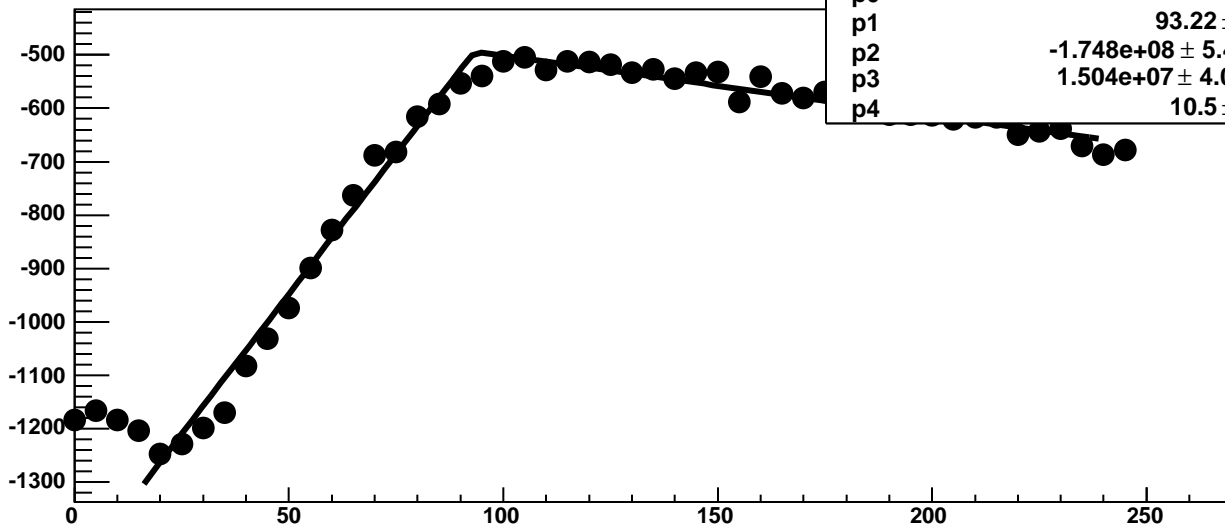
Chip 0, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold

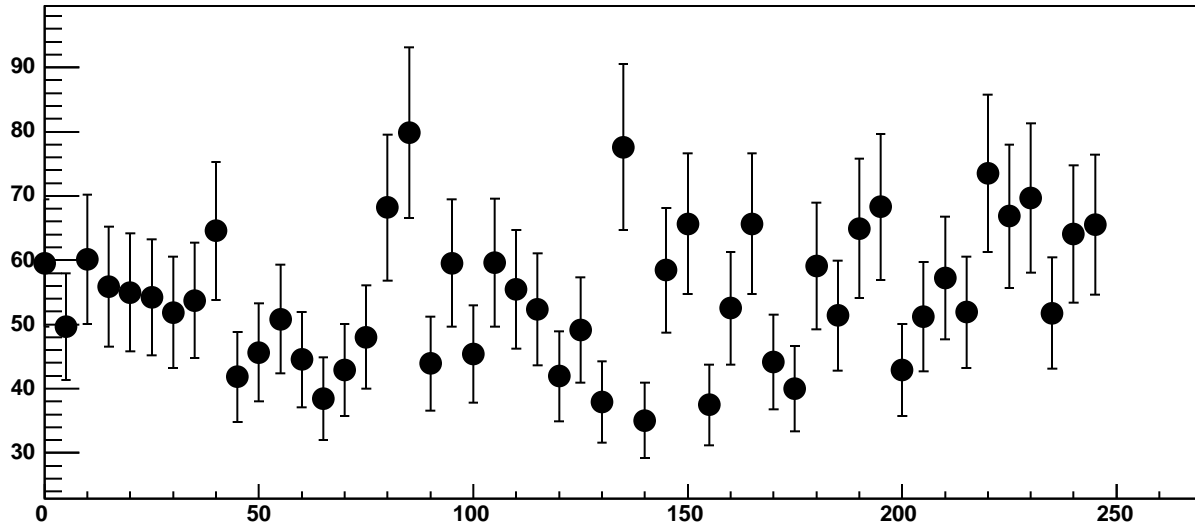


Chip 0, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

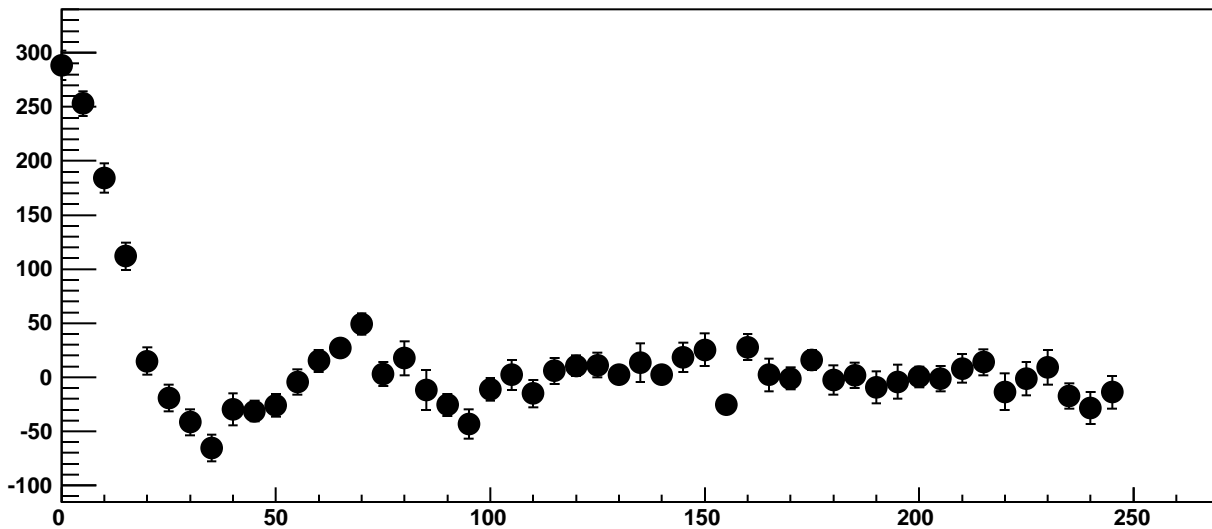


$\chi^2 / \text{ndf}$	232.5 / 41
p0	-493.9 ± 3.895
p1	93.22 ± 0.6297
p2	-1.748e+08 ± 5.473e+06
p3	1.504e+07 ± 4.095e+05
p4	10.5 ± 0.1328

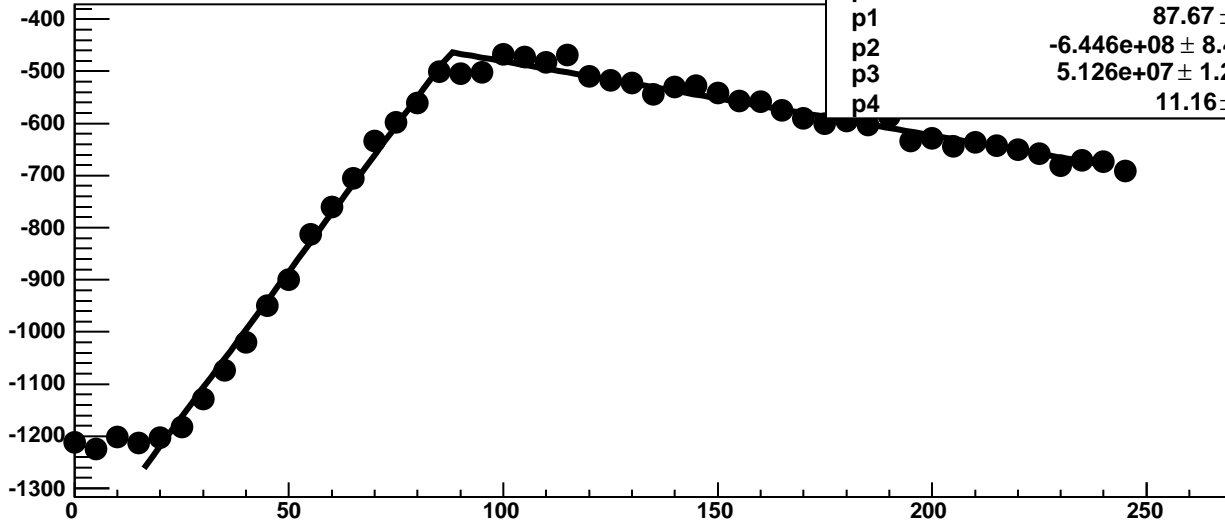
Chip 0, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

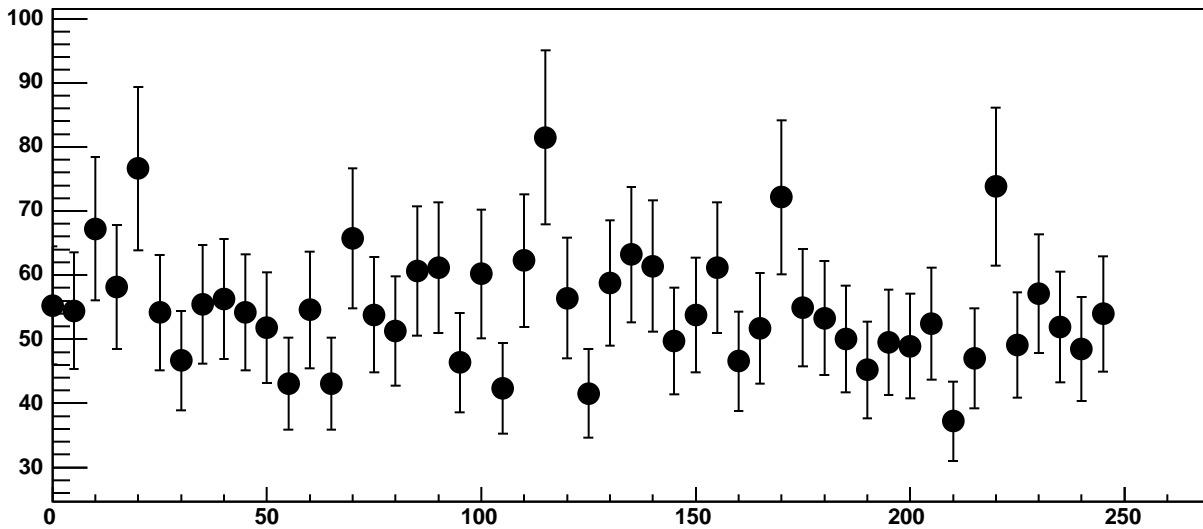


Chip 0, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

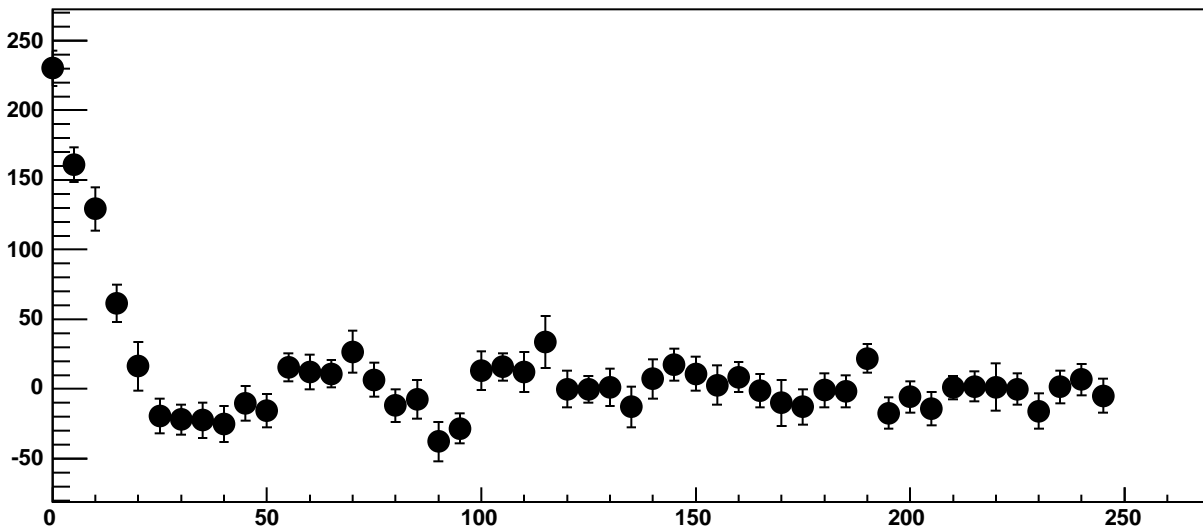


$\chi^2 / \text{ndf}$	85.81 / 41
p0	-463.6 ± 3.984
p1	87.67 ± 0.6245
p2	-6.446e+08 ± 8.456e+06
p3	5.126e+07 ± 1.287e+05
p4	11.16 ± 0.1554

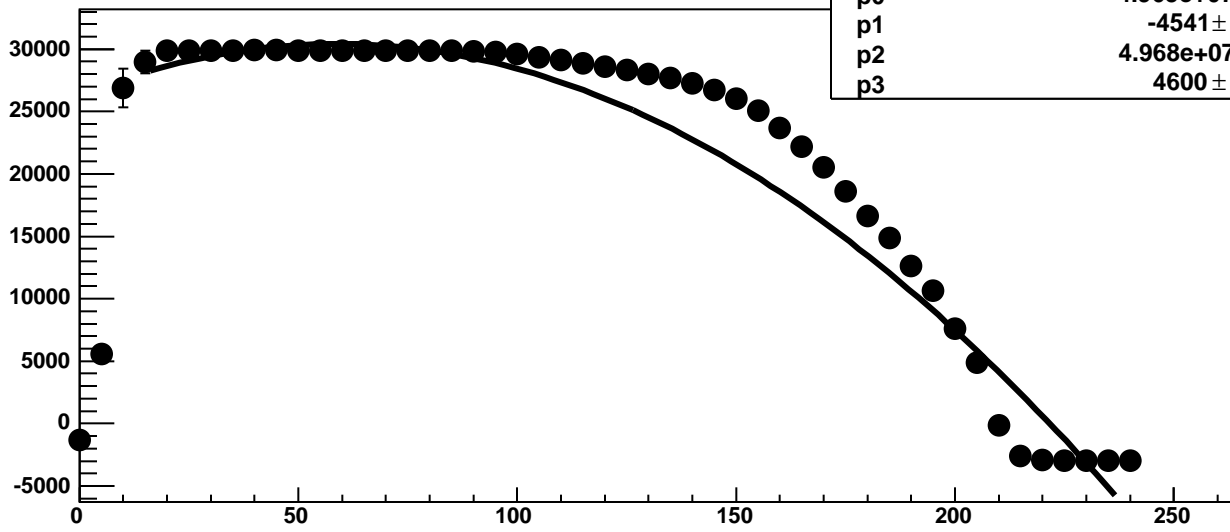
Chip 0, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

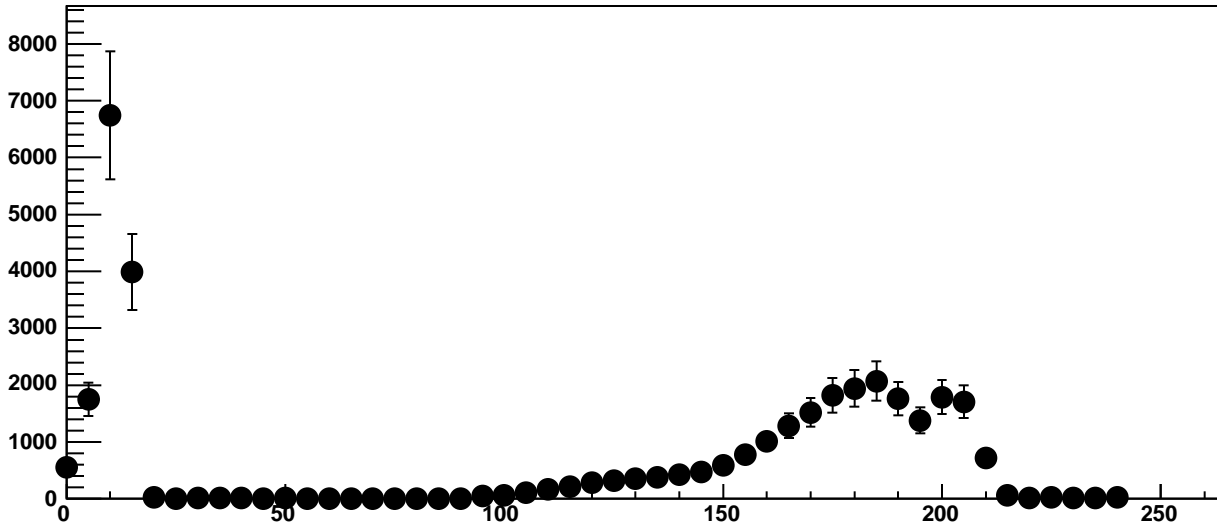


Chip 0, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold

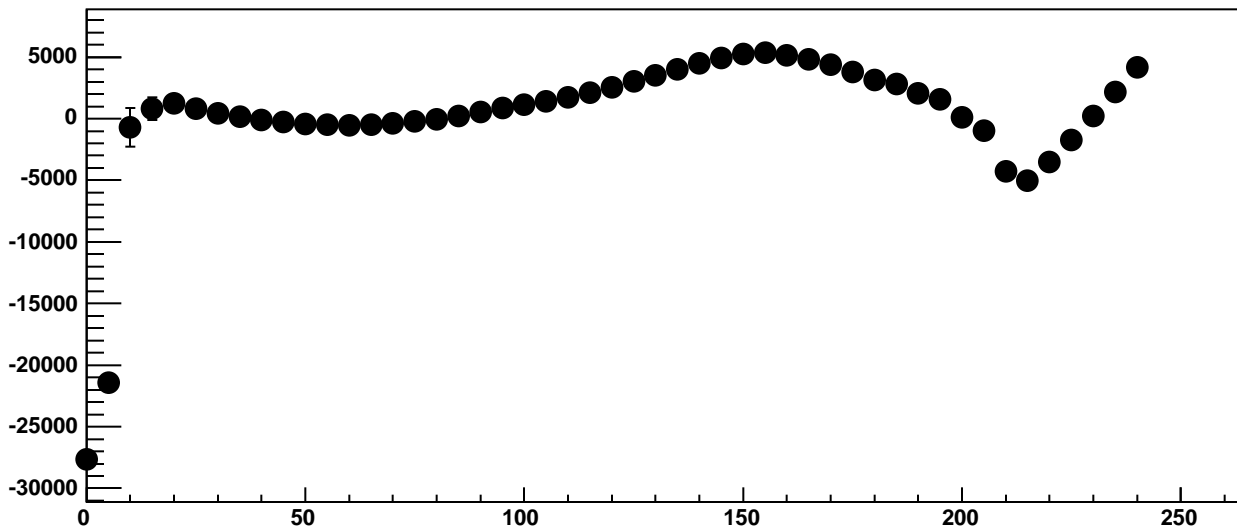


$\chi^2 / \text{ndf}$	2.44e+06 / 42
p0	-4.965e+07 ± 6.546
p1	-4541 ± 0.06335
p2	4.968e+07 ± 6.545
p3	4600 ± 0.06154

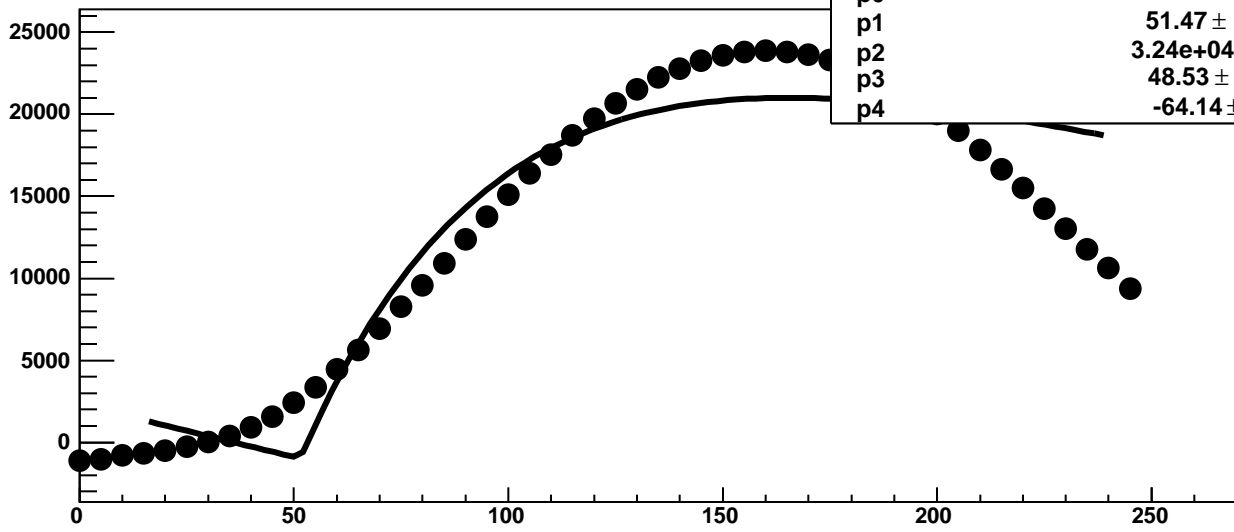
Chip 0, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold

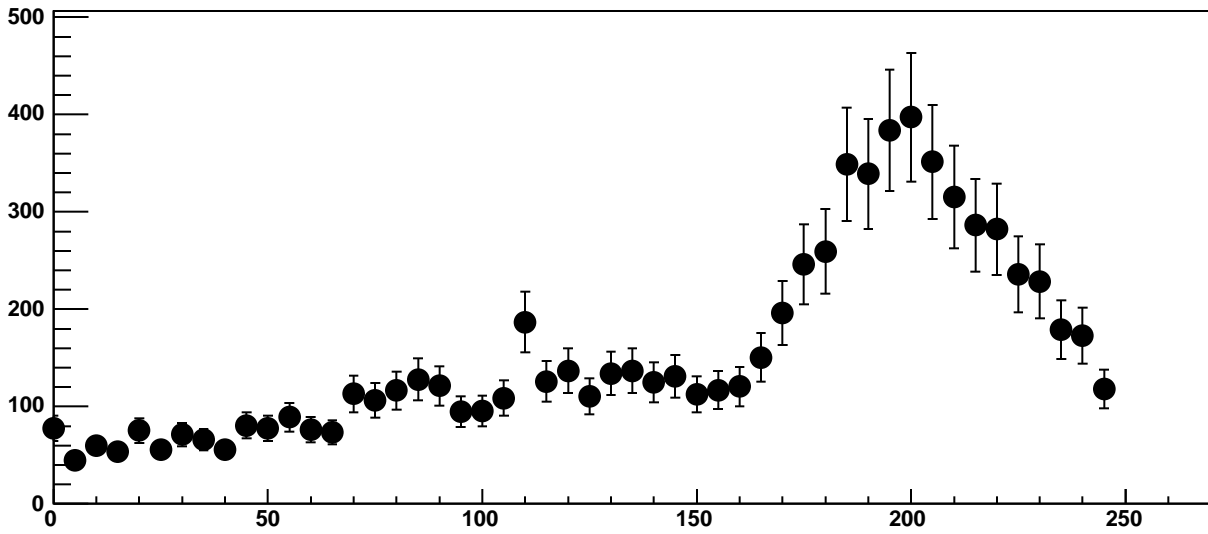


Chip 0, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

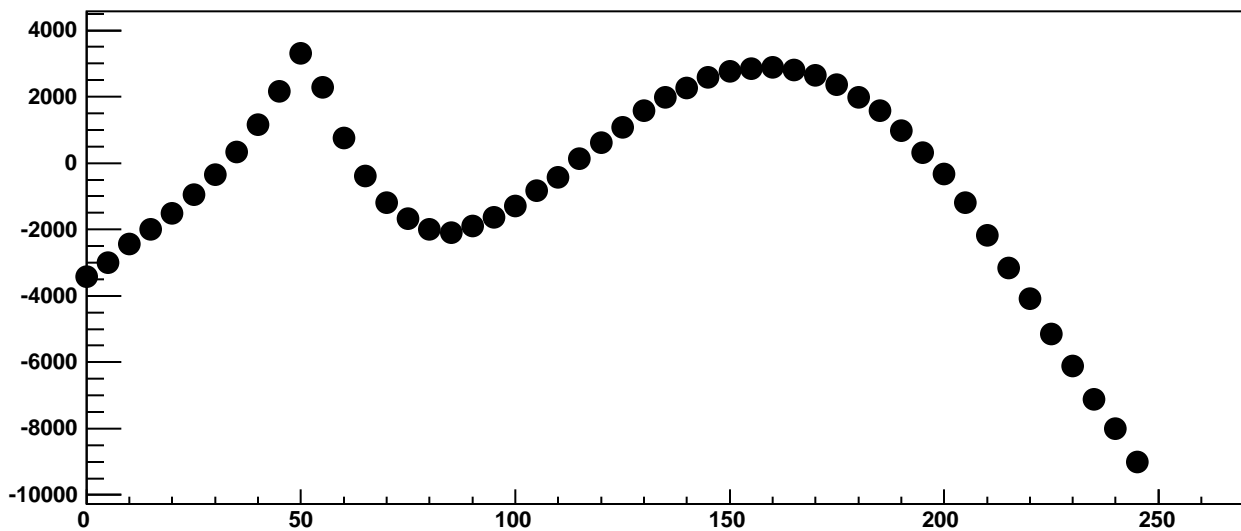


$\chi^2 / \text{ndf}$	3.141e+05 / 41
p0	-991.1 ± 7.468
p1	51.47 ± 0.02458
p2	3.24e+04 ± 58.19
p3	48.53 ± 0.09331
p4	-64.14 ± 0.2998

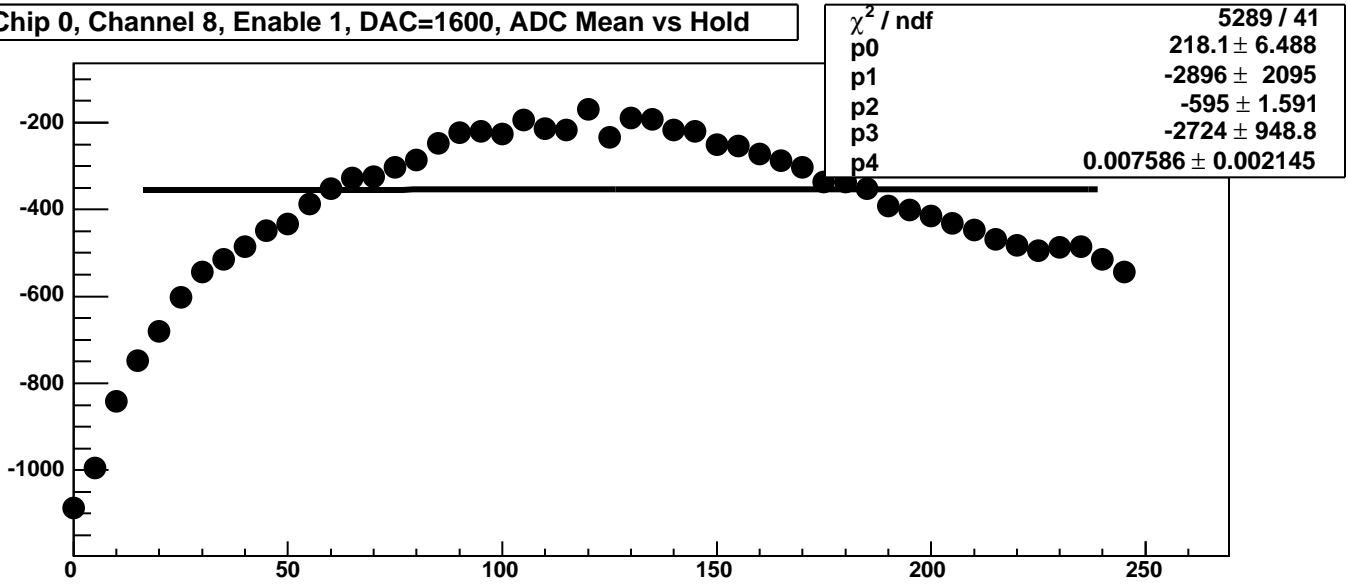
Chip 0, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



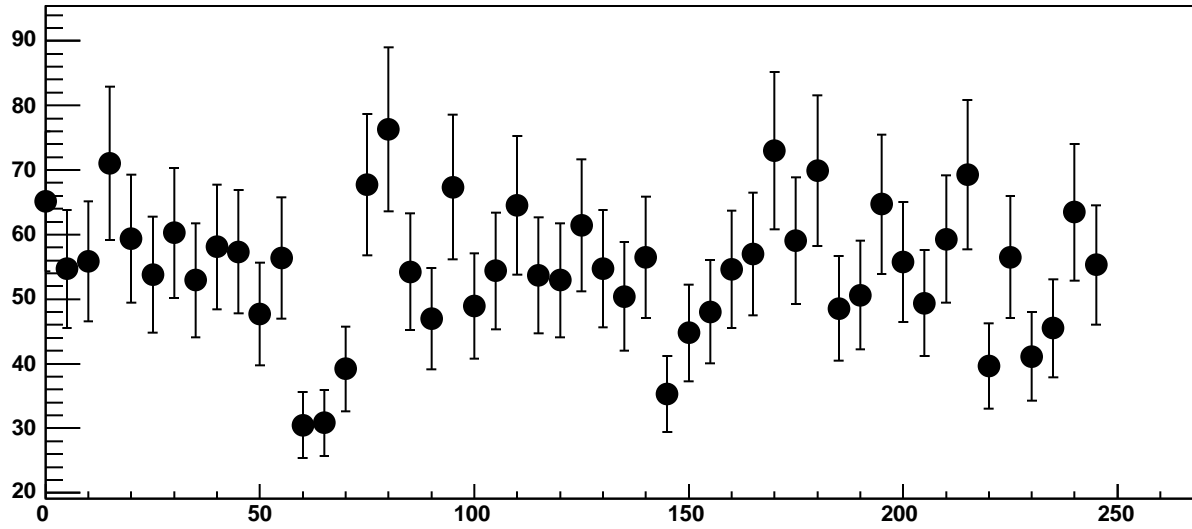
Chip 0, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold



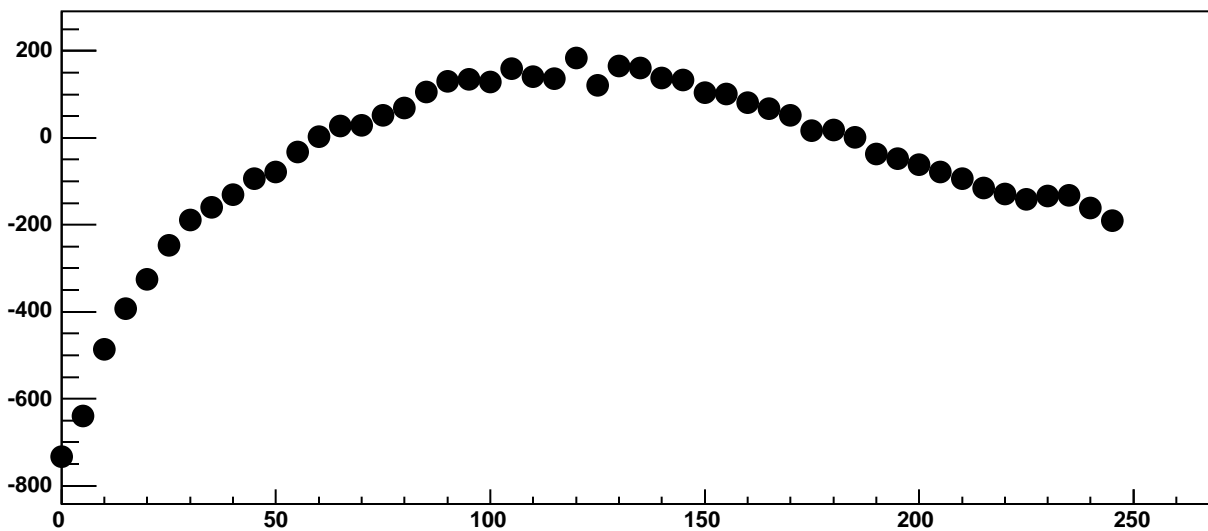
Chip 0, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 0, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

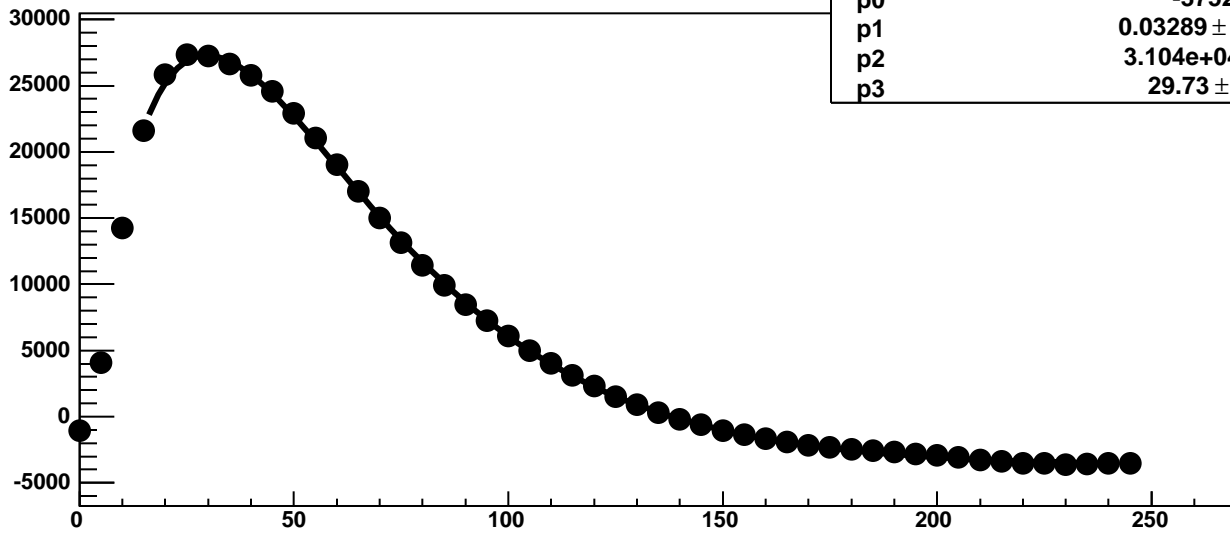


Chip 0, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

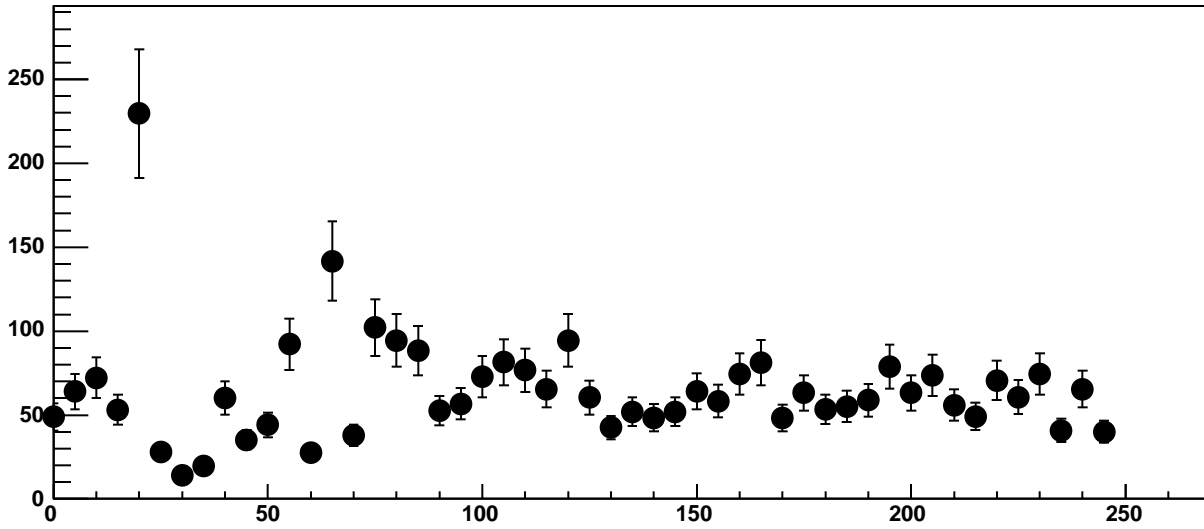




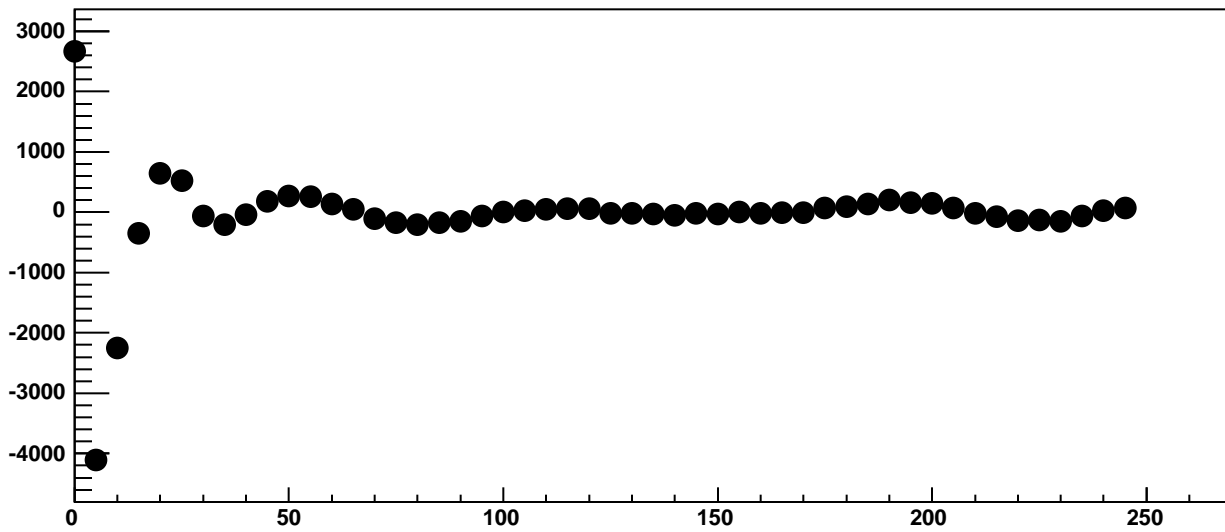
Chip 0, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold



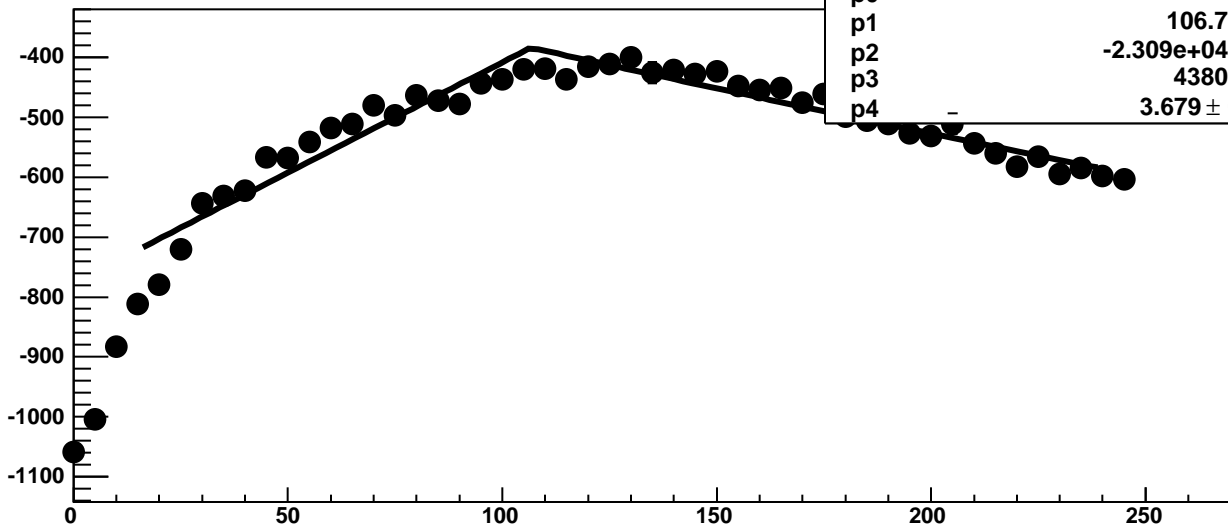
Chip 0, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



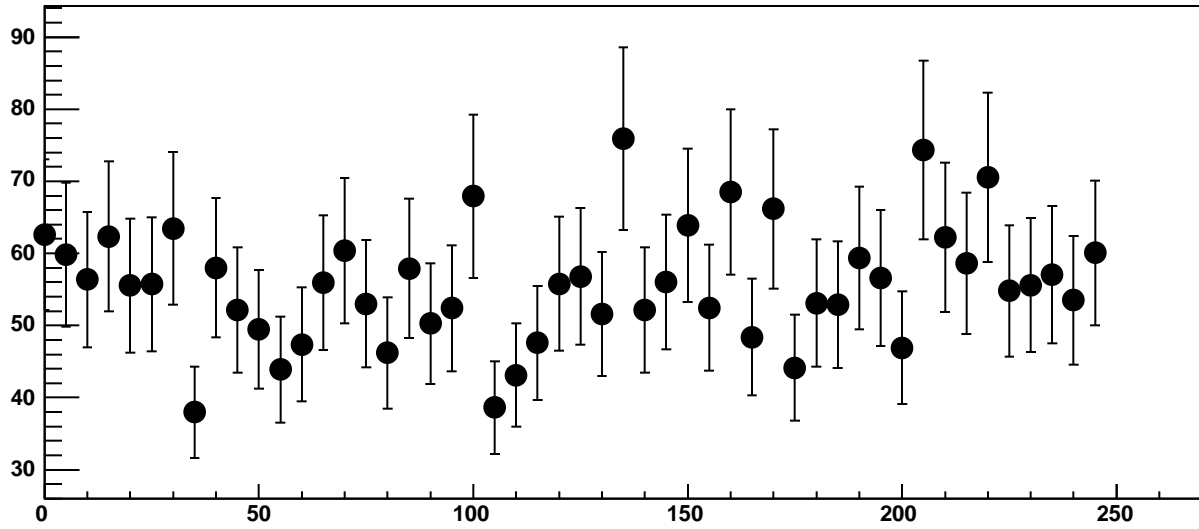
Chip 0, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold



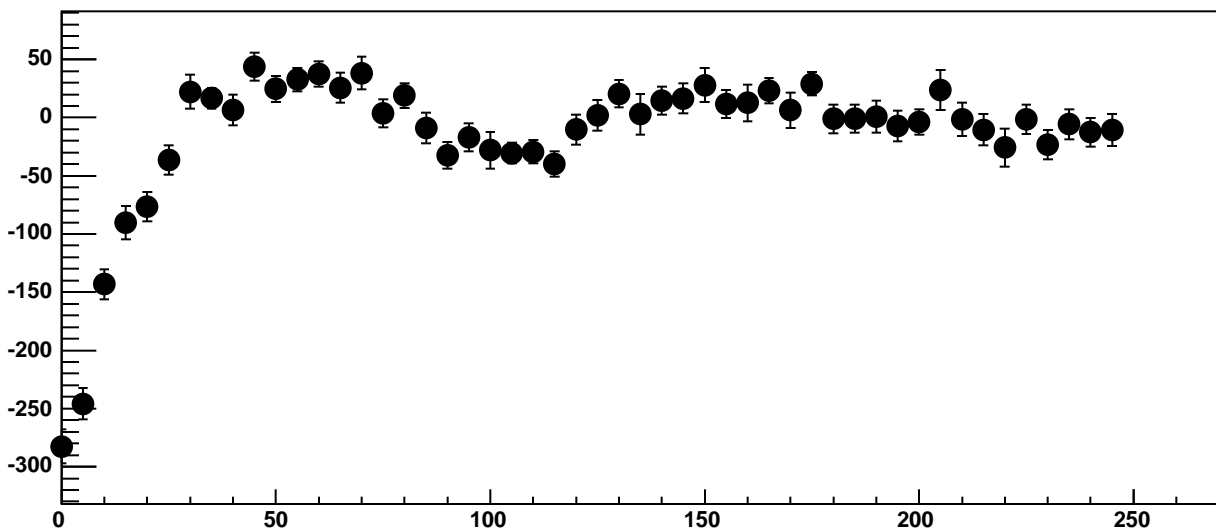
Chip 0, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold



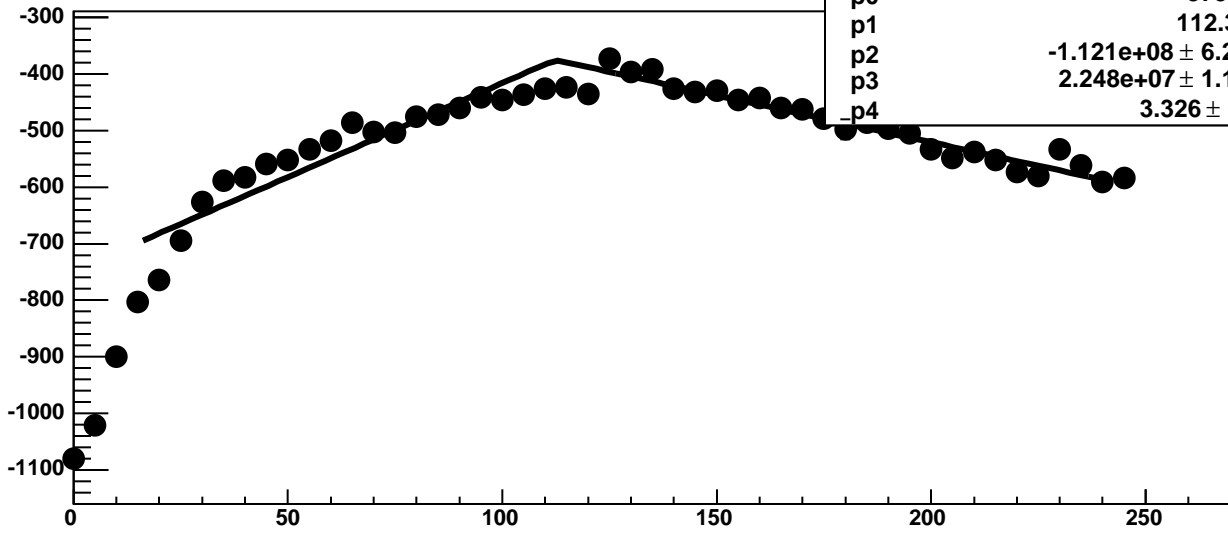
Chip 0, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



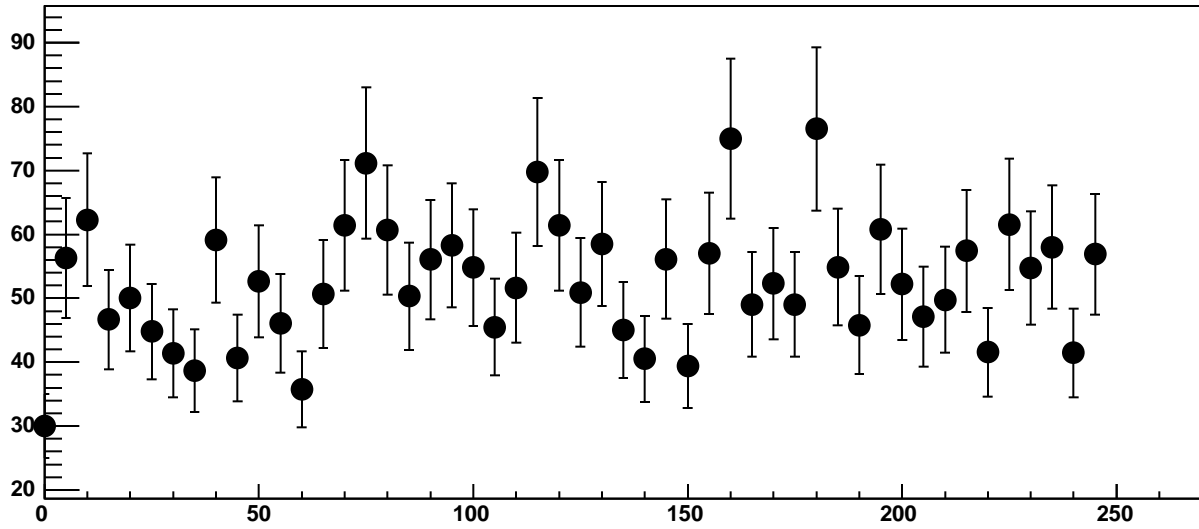
Chip 0, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold



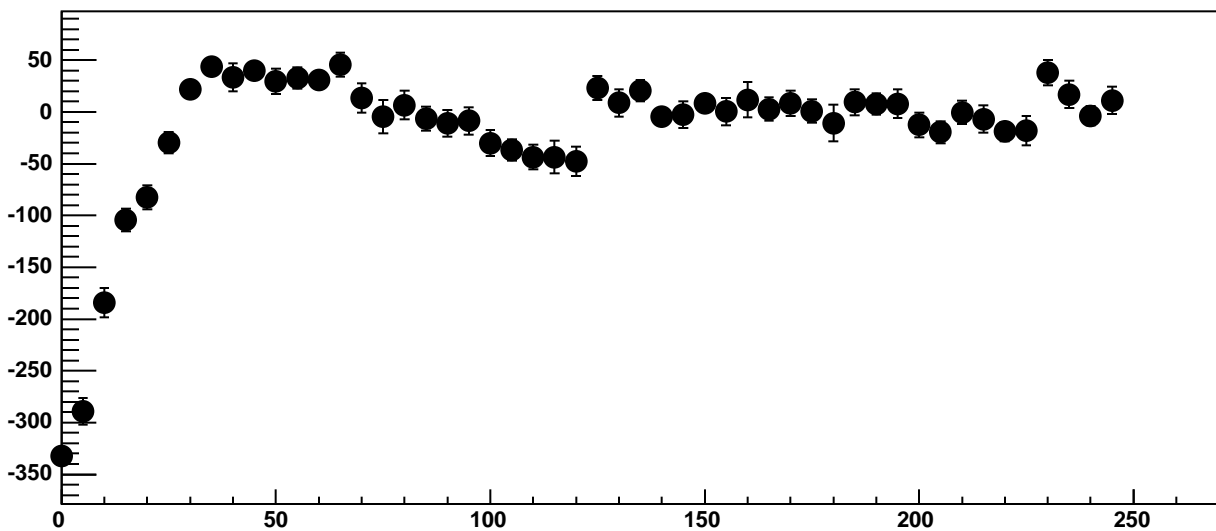
Chip 0, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold



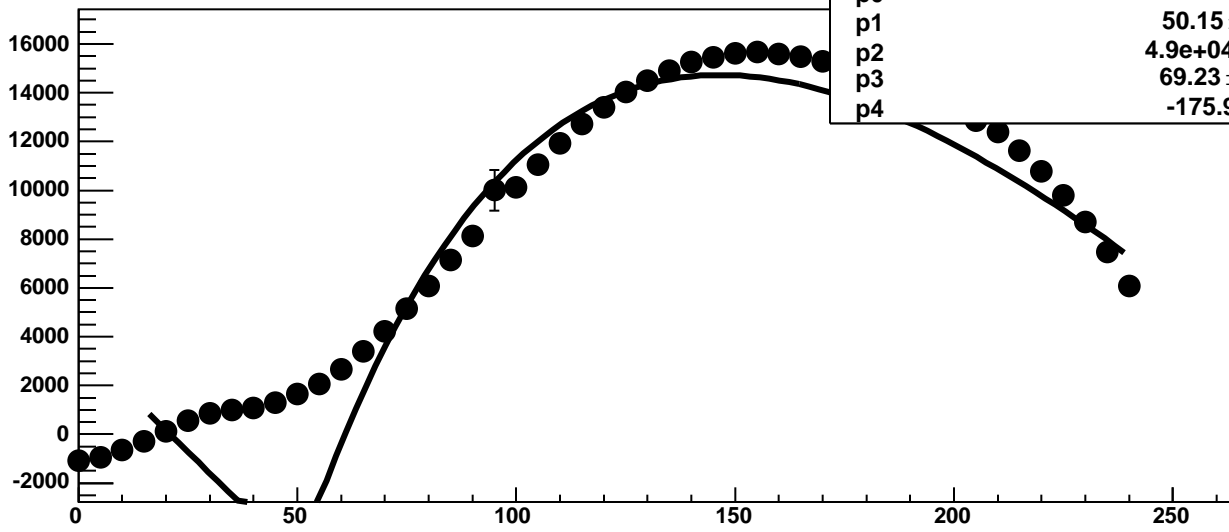
Chip 0, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

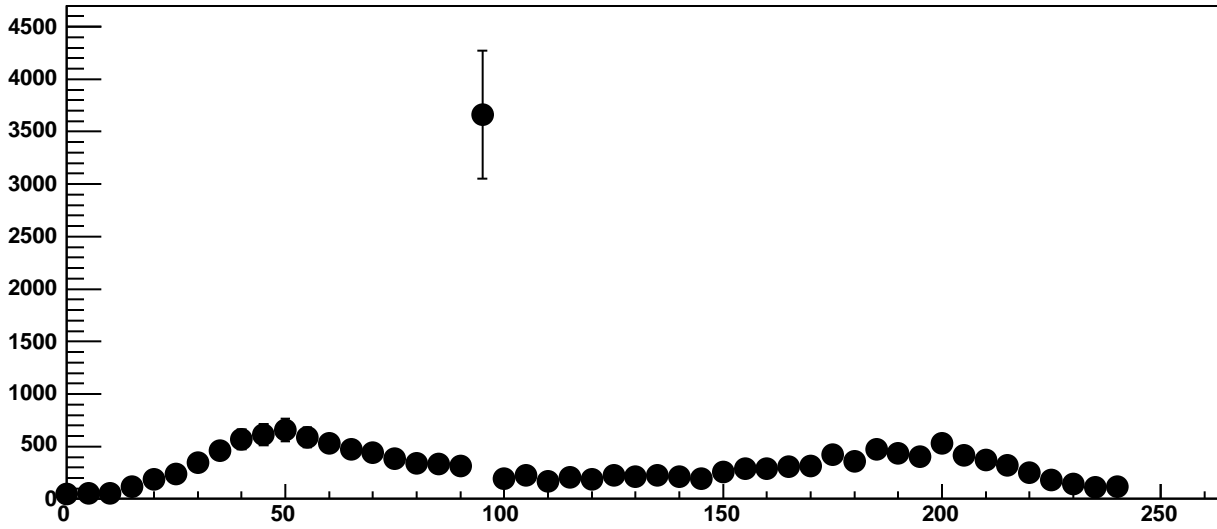


Chip 0, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold

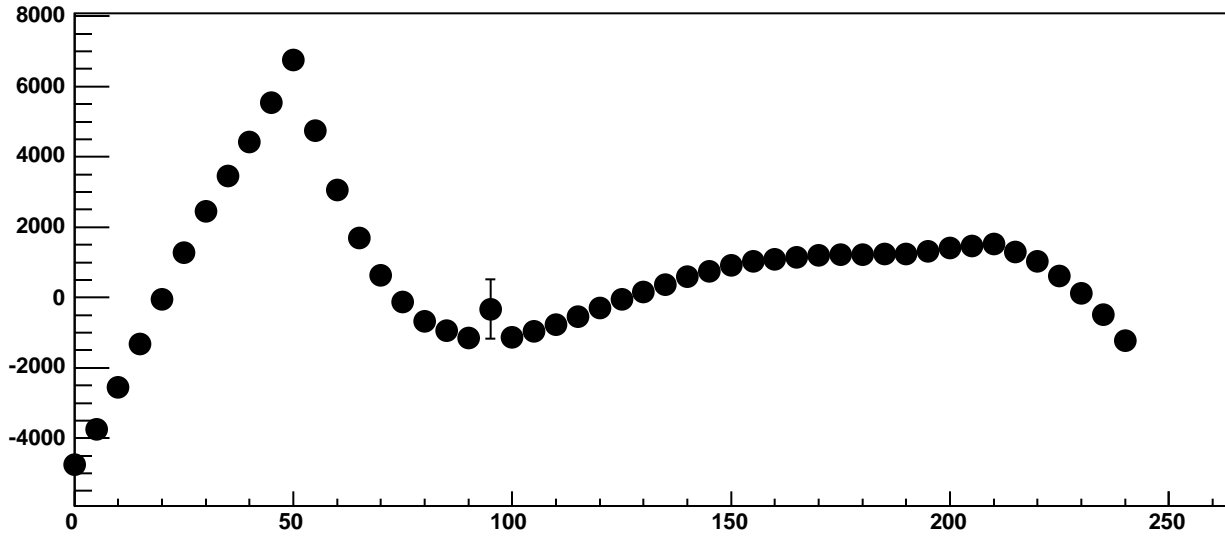


$\chi^2 / \text{ndf}$	2.076e+04 / 41
p0	-5145 ± 31.16
p1	50.15 ± 0.1211
p2	4.9e+04 ± 317.7
p3	69.23 ± 0.4342
p4	-175.9 ± 1.161

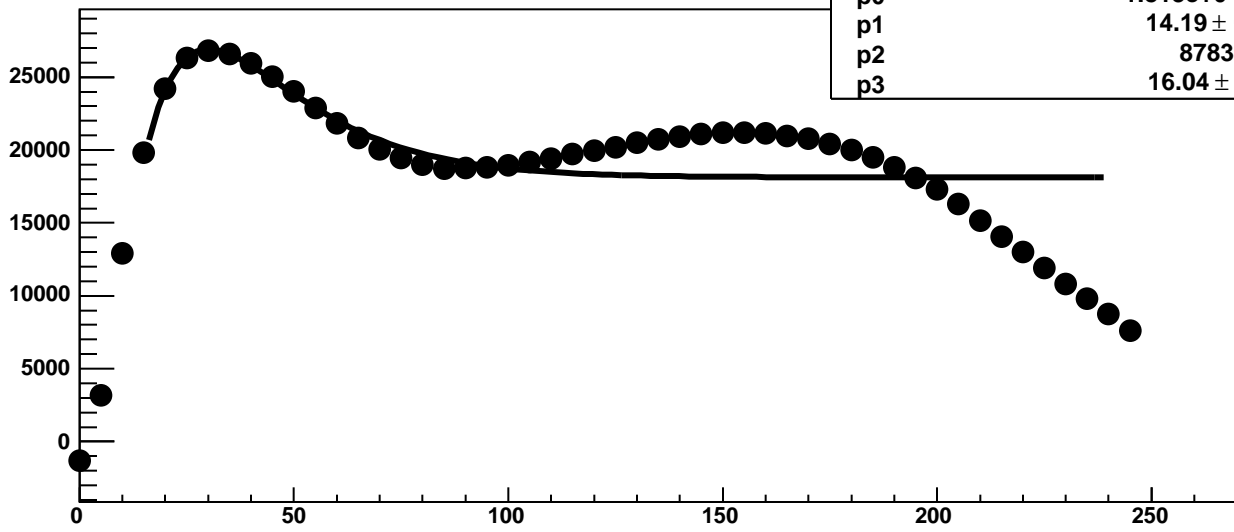
Chip 0, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold

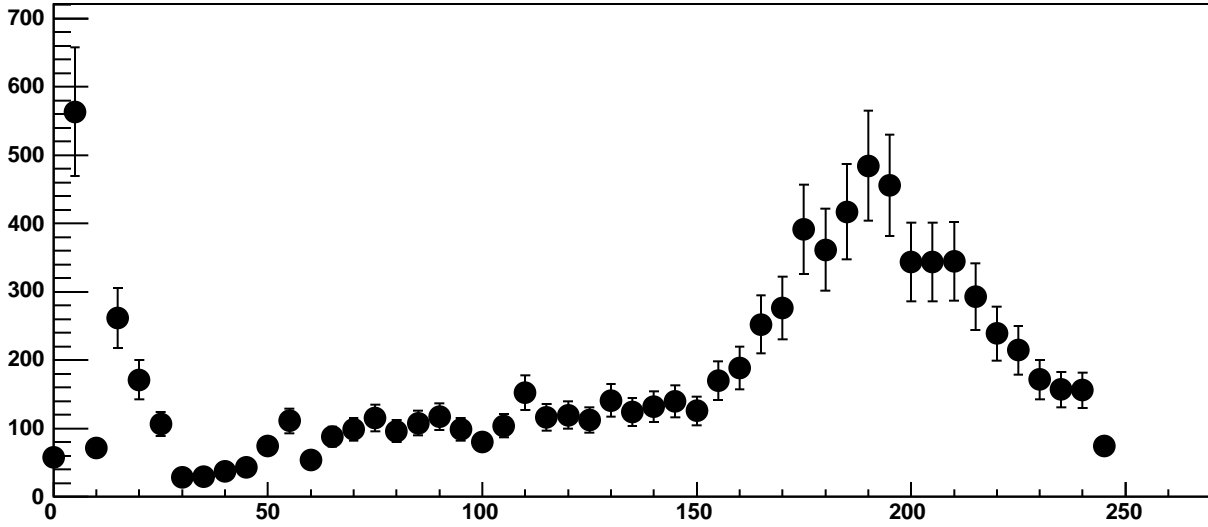


Chip 0, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold

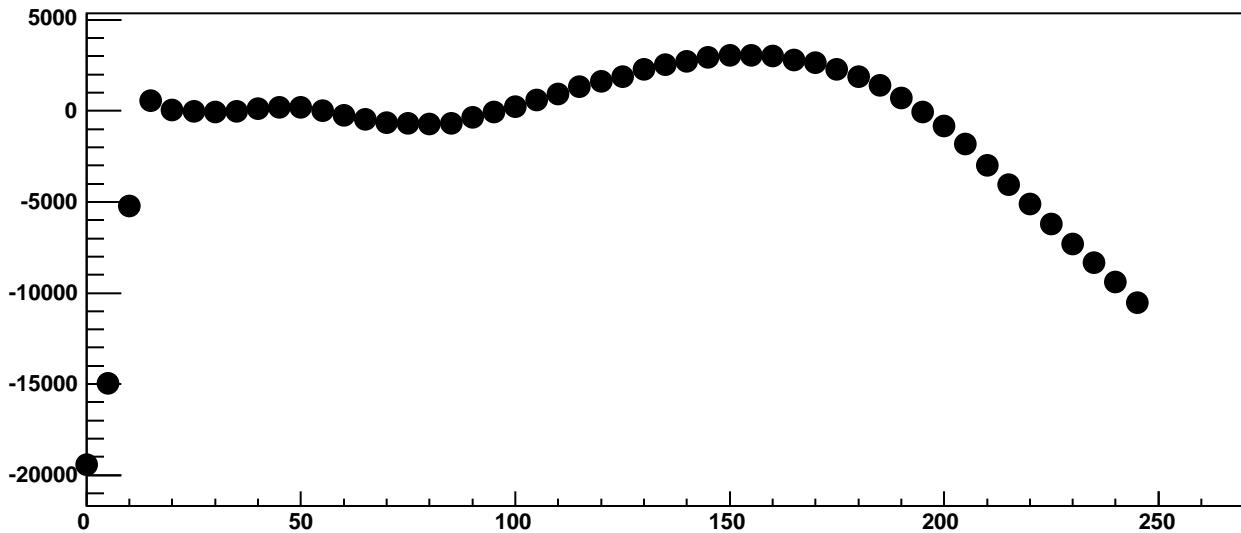


$\chi^2 / \text{ndf}$	2.612e+05 / 42
p0	1.813e+04 $\pm$ 7.49
p1	14.19 $\pm$ 0.03692
p2	8783 $\pm$ 8.353
p3	16.04 $\pm$ 0.02771

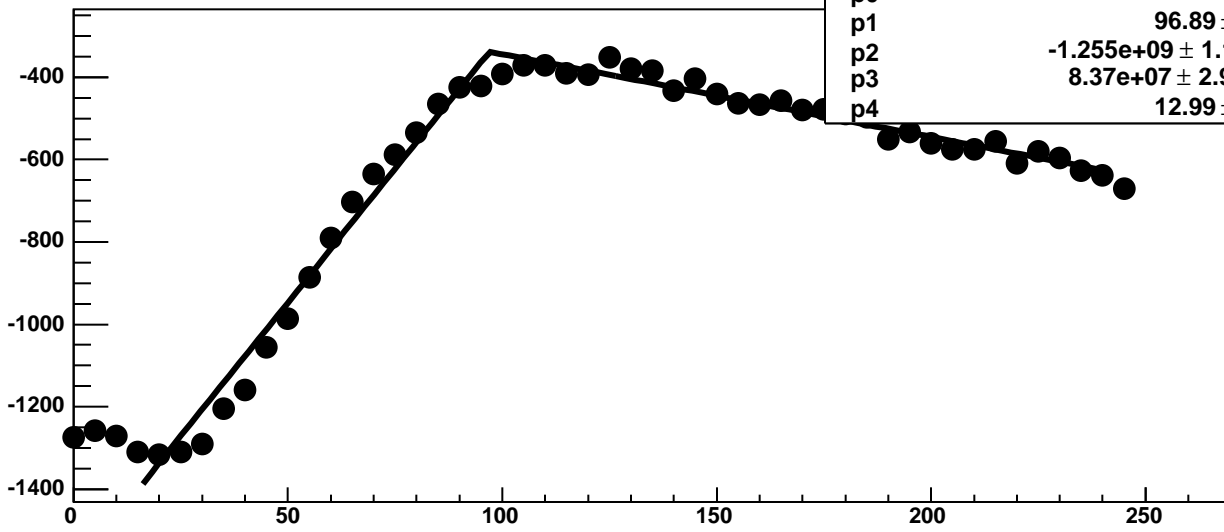
Chip 0, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold

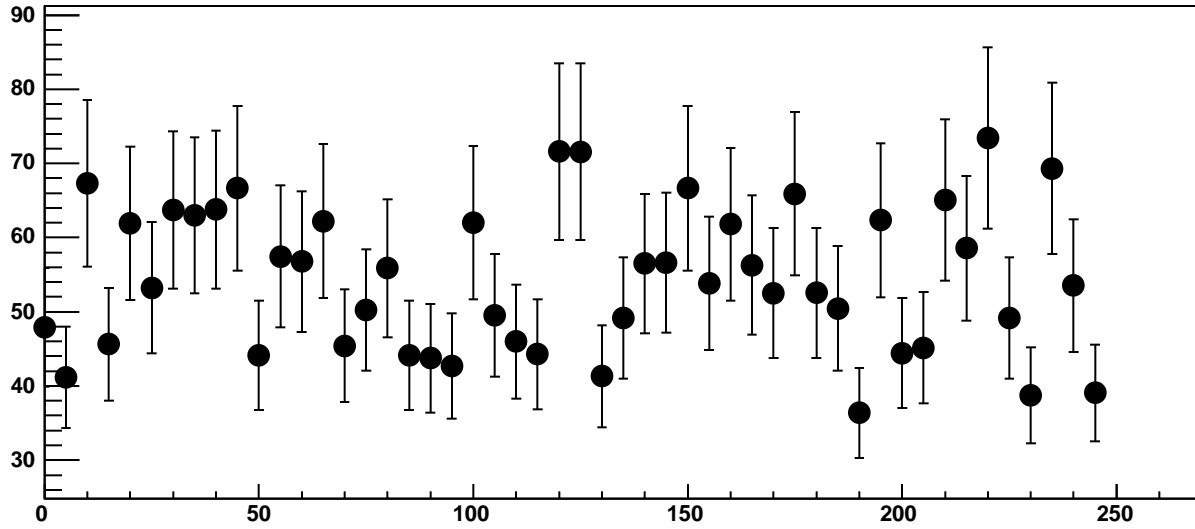


Chip 0, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

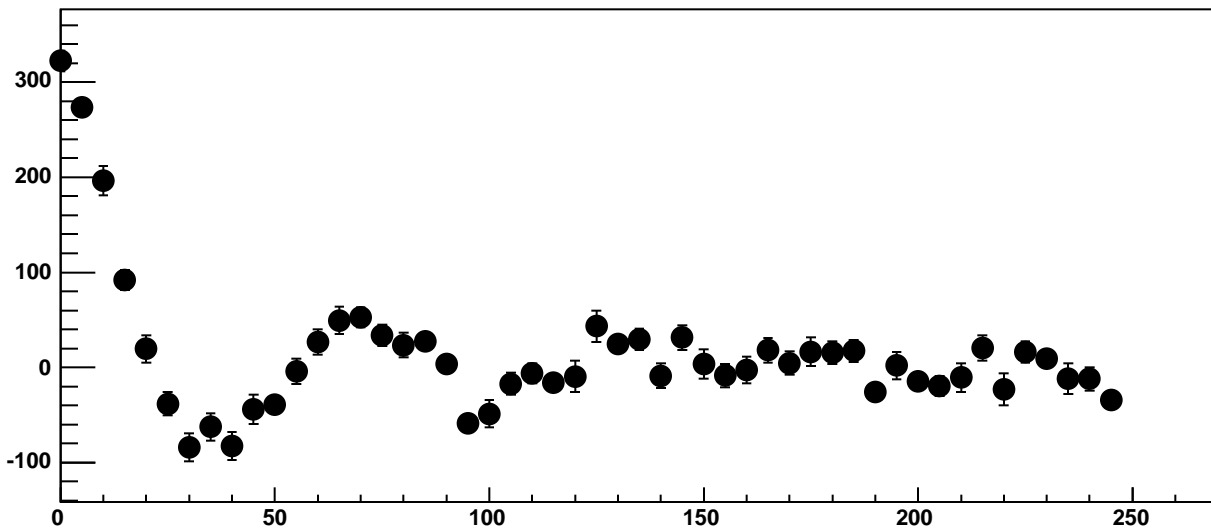


$\chi^2 / \text{ndf}$	370.6 / 41
p0	$-337.9 \pm 3.979$
p1	$96.89 \pm 0.4573$
p2	$-1.255\text{e}+09 \pm 1.127\text{e}+07$
p3	$8.37\text{e}+07 \pm 2.912\text{e}+05$
p4	$12.99 \pm 0.1127$

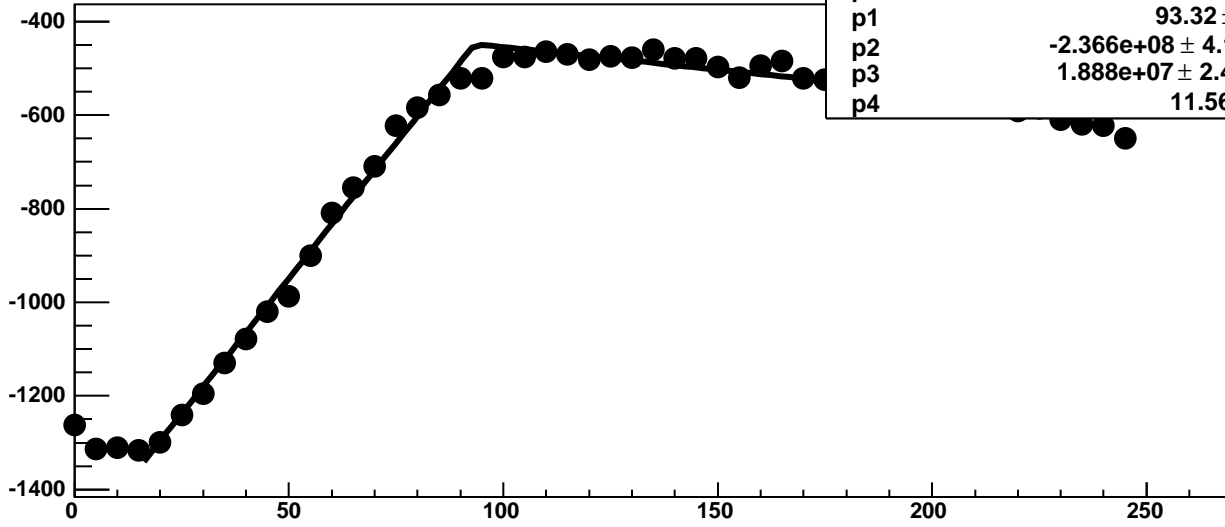
Chip 0, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

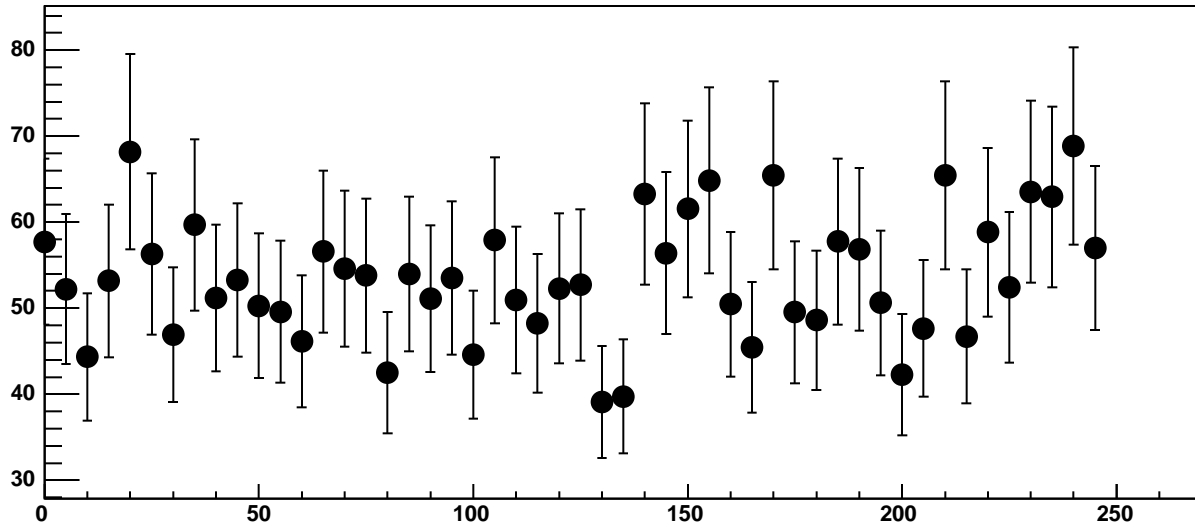


Chip 0, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

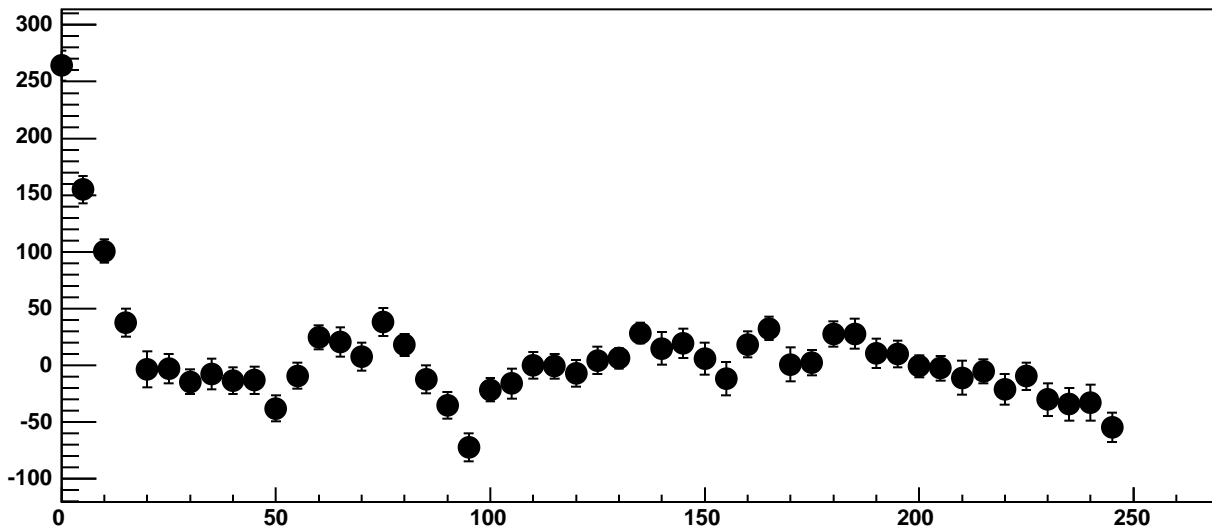


$\chi^2 / \text{ndf}$	154.5 / 41
p0	$-447.7 \pm 3.948$
p1	$93.32 \pm 0.5842$
p2	$-2.366\text{e}+08 \pm 4.172\text{e}+06$
p3	$1.888\text{e}+07 \pm 2.482\text{e}+05$
p4	$11.56 \pm 0.132$

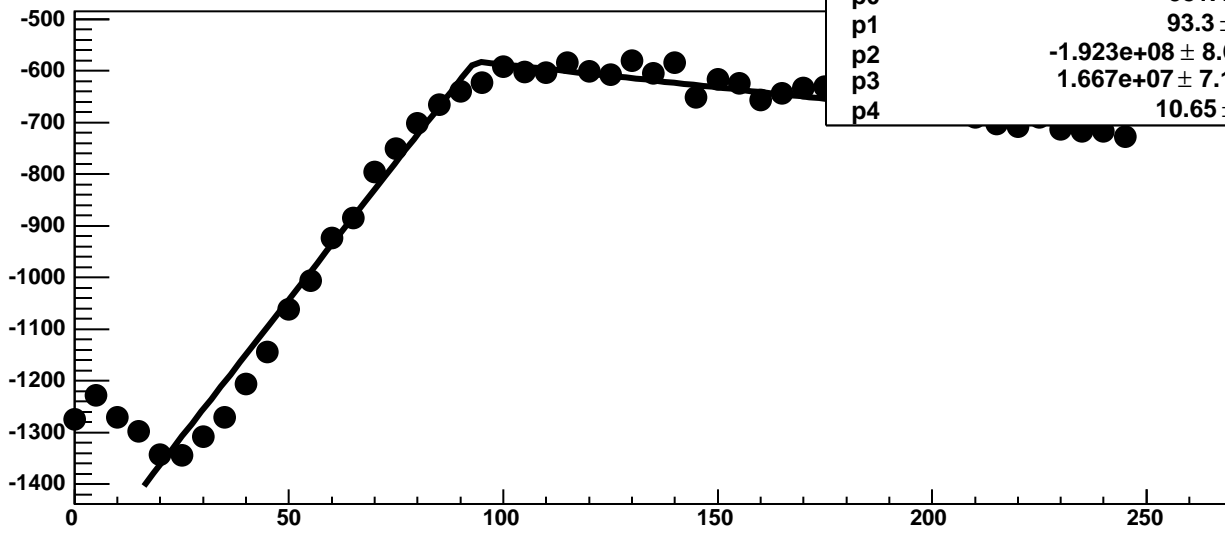
Chip 0, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

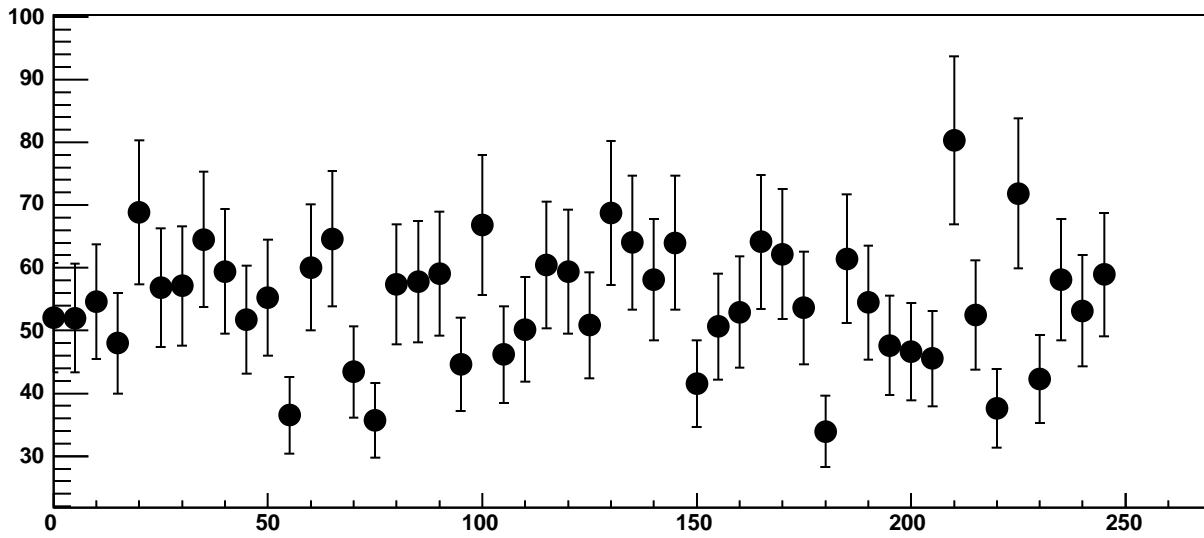


Chip 0, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold

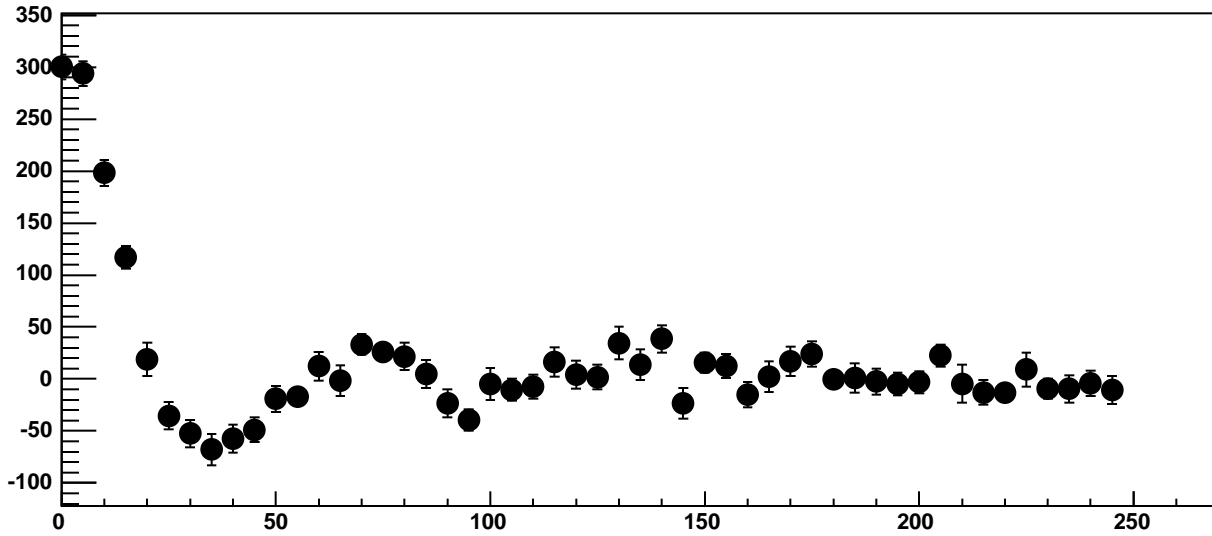


$\chi^2 / \text{ndf}$	283.2 / 41
p0	-581.4 ± 4.109
p1	93.3 ± 0.6456
p2	-1.923e+08 ± 8.697e+06
p3	1.667e+07 ± 7.135e+05
p4	10.65 ± 0.1347

Chip 0, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

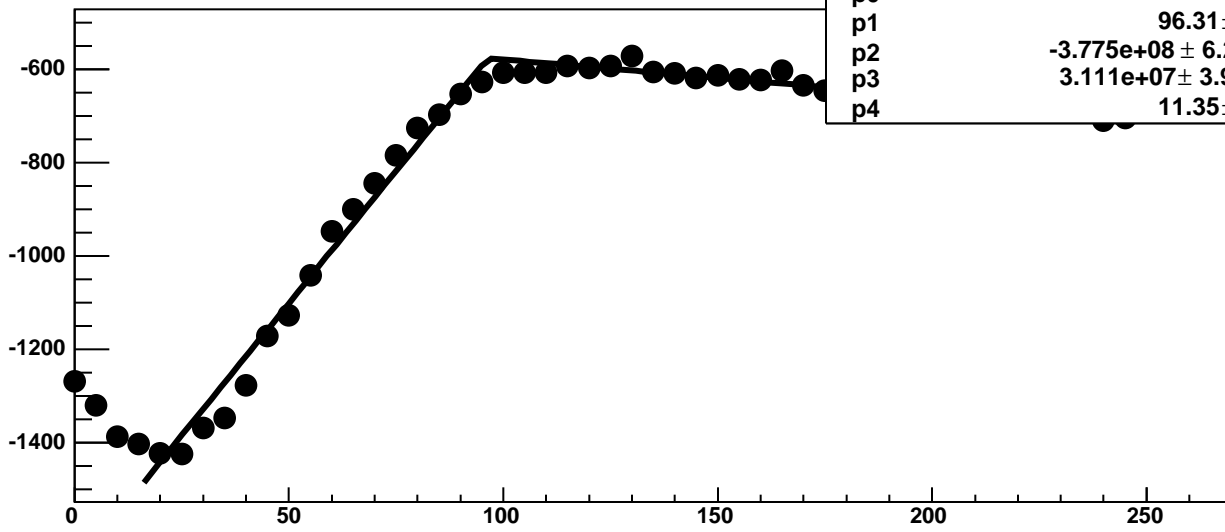


Chip 0, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold



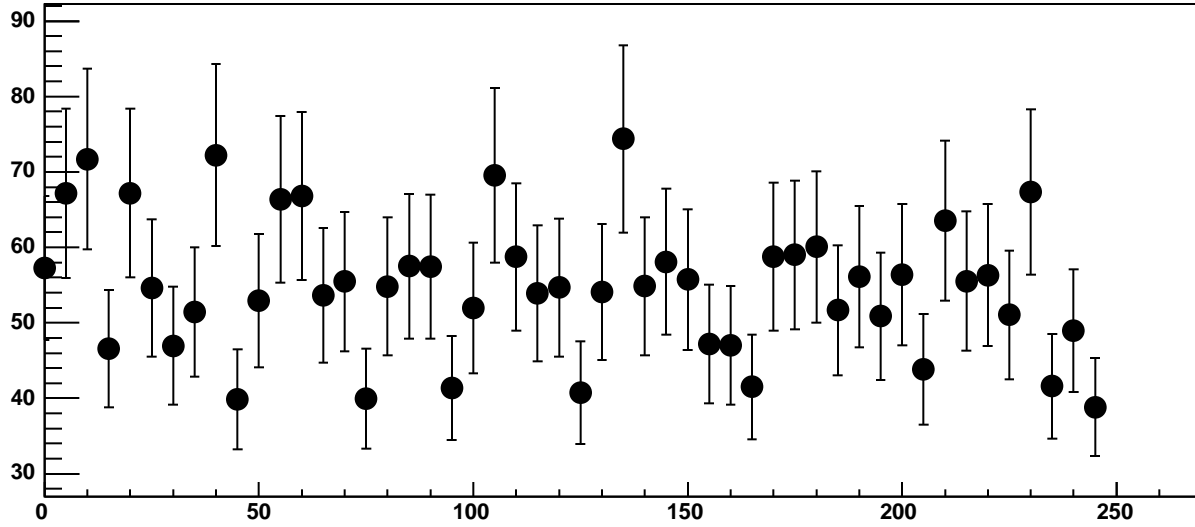


Chip 0, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

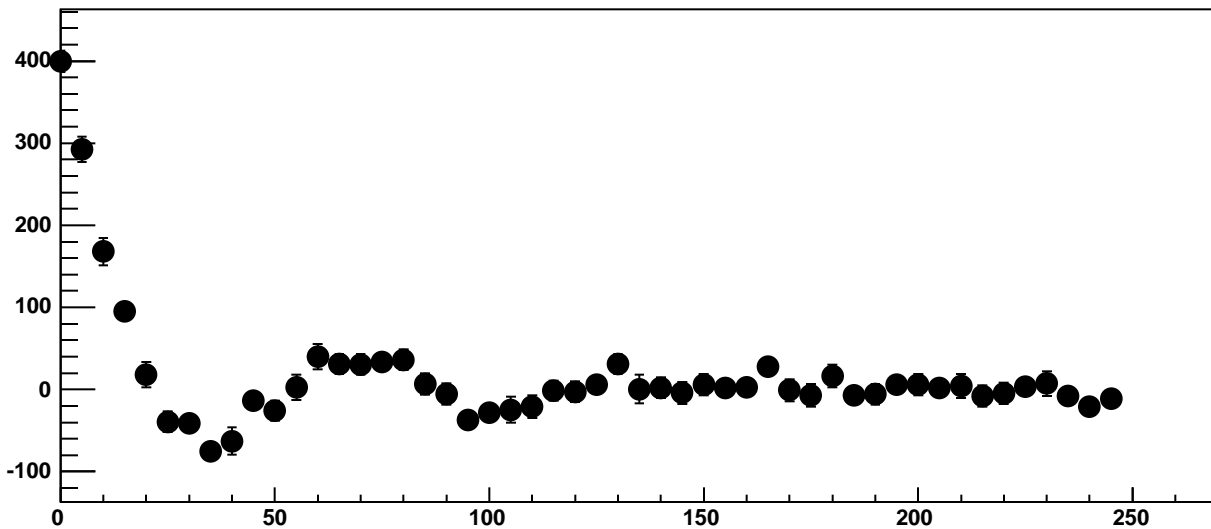


$\chi^2 / \text{ndf}$	257.7 / 41
p0	-576.2 ± 4.365
p1	96.31 ± 0.5899
p2	-3.775e+08 ± 6.203e+06
p3	3.111e+07 ± 3.998e+05
p4	11.35 ± 0.1147

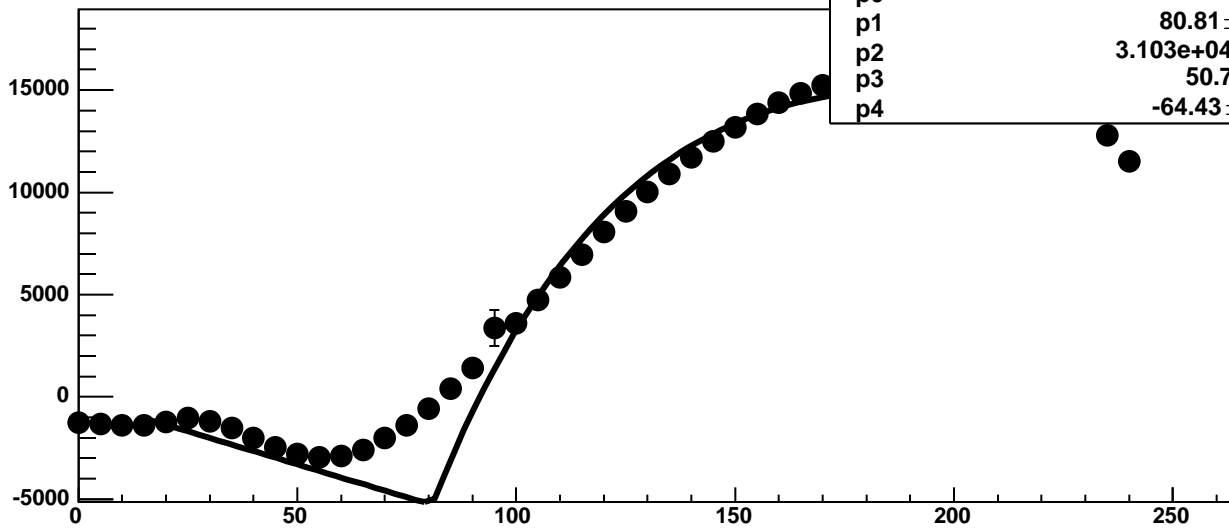
Chip 0, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

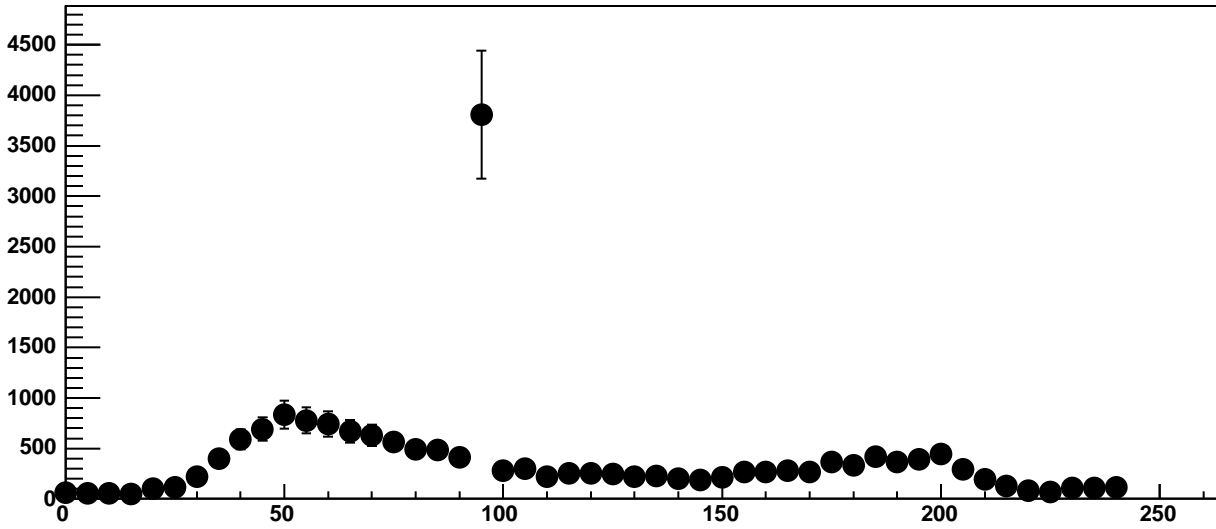


Chip 0, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

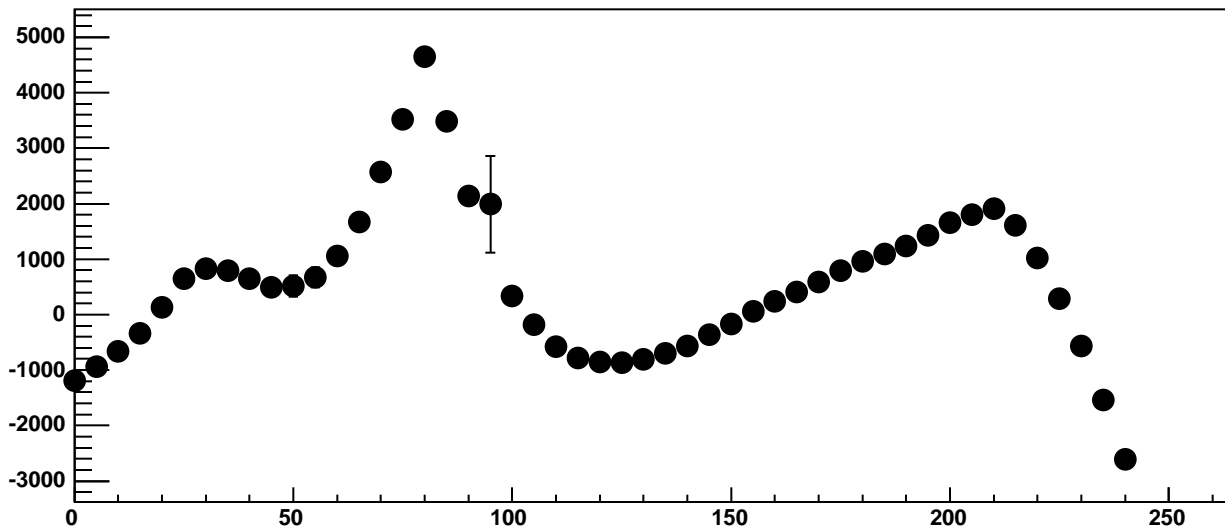


$\chi^2 / \text{ndf}$	3.17e+04 / 41
p0	-5280 ± 39.95
p1	80.81 ± 0.1325
p2	3.103e+04 ± 175.3
p3	50.7 ± 0.278
p4	-64.43 ± 0.7079

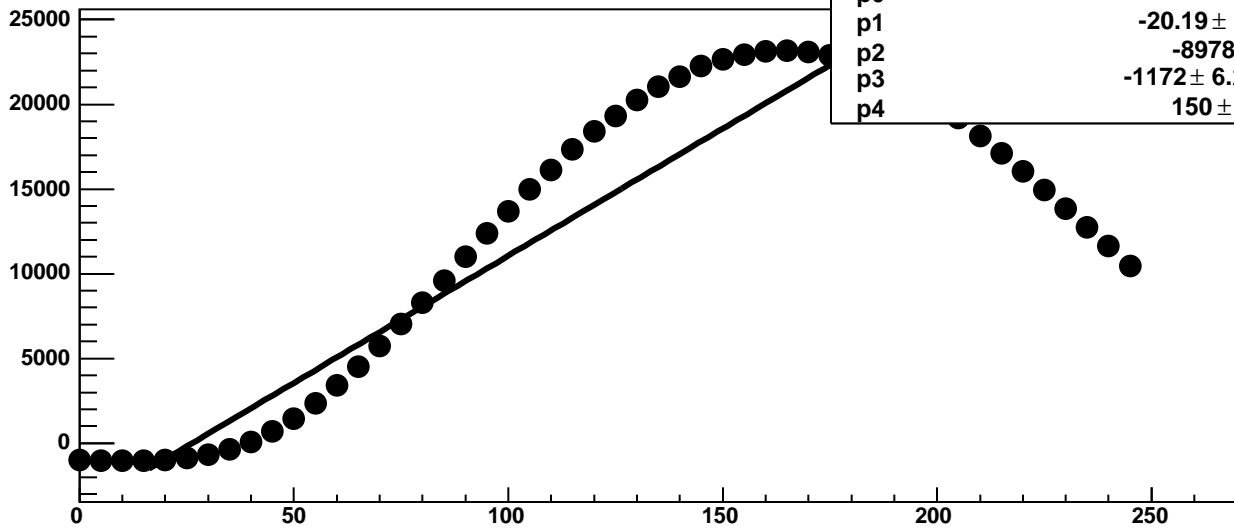
Chip 0, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

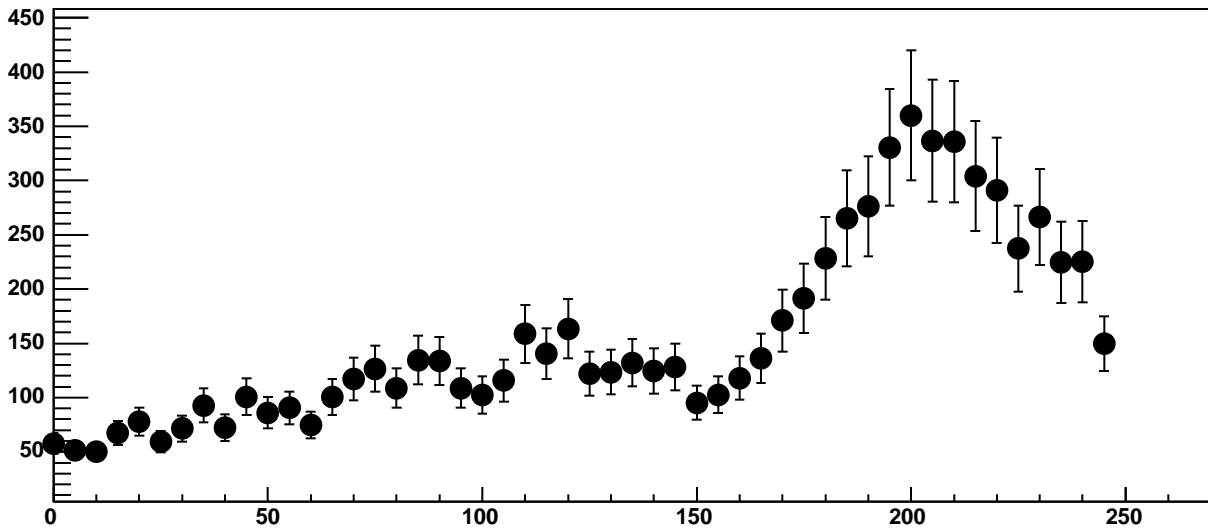


Chip 0, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold

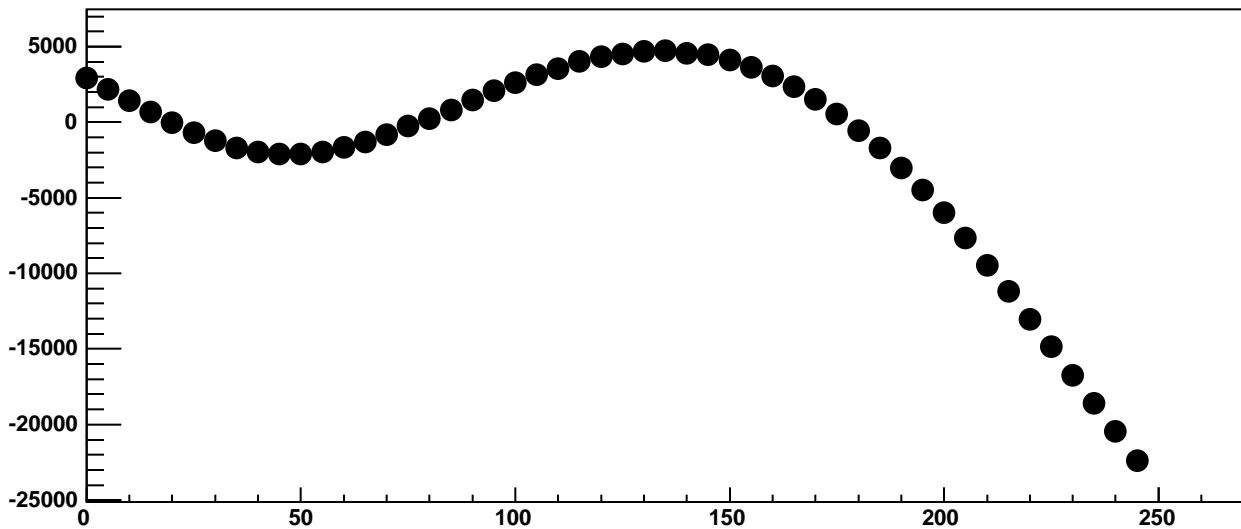


$\chi^2 / \text{ndf}$	8.885e+05 / 41
p0	2007 ± 4.168
p1	-20.19 ± 0.02765
p2	-8978 ± 4.168
p3	-1172 ± 6.208e-06
p4	150 ± 0.07411

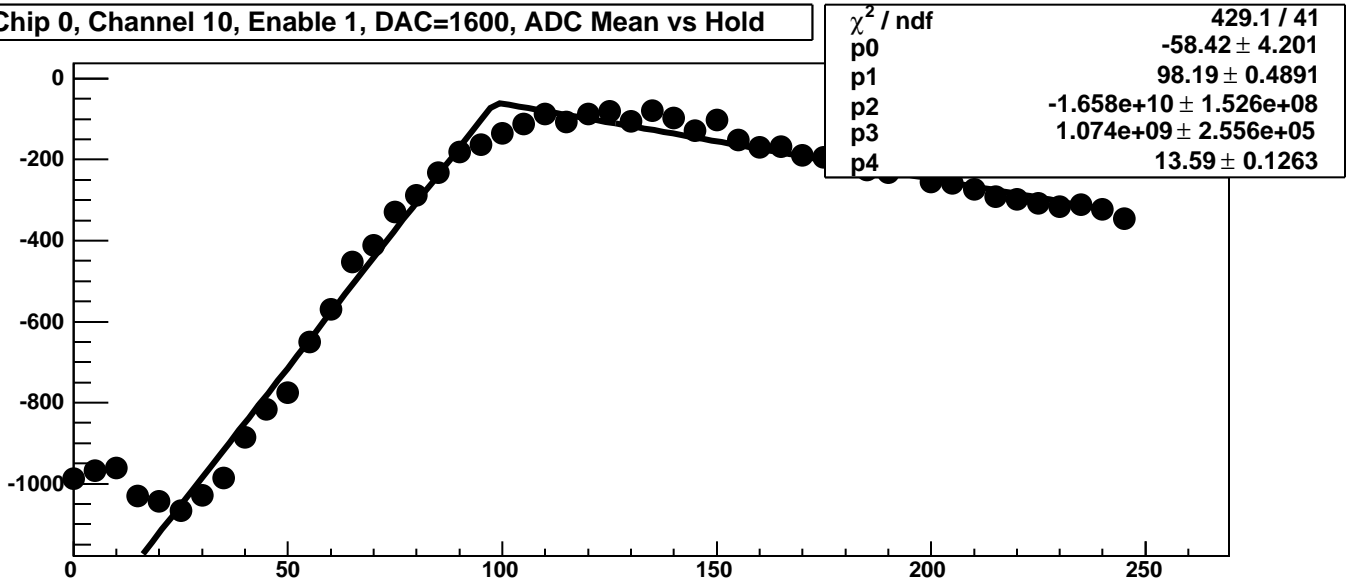
Chip 0, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



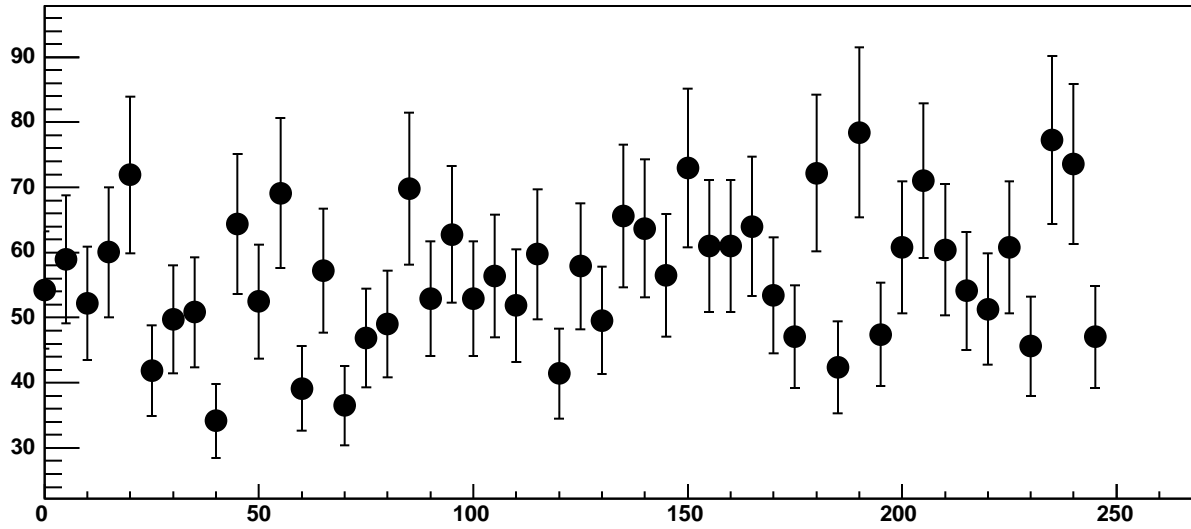
Chip 0, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold



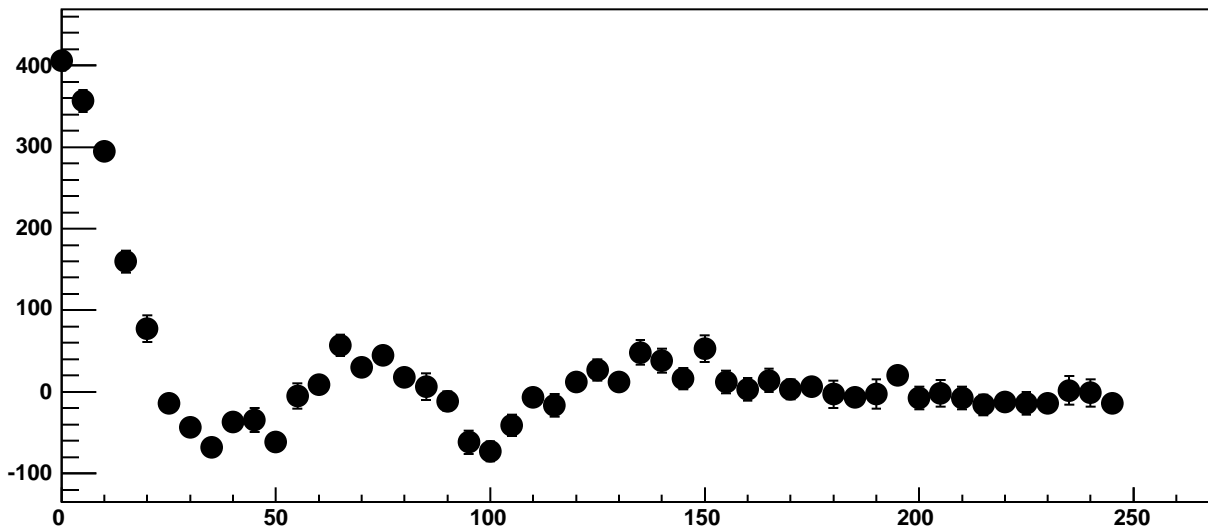
Chip 0, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold



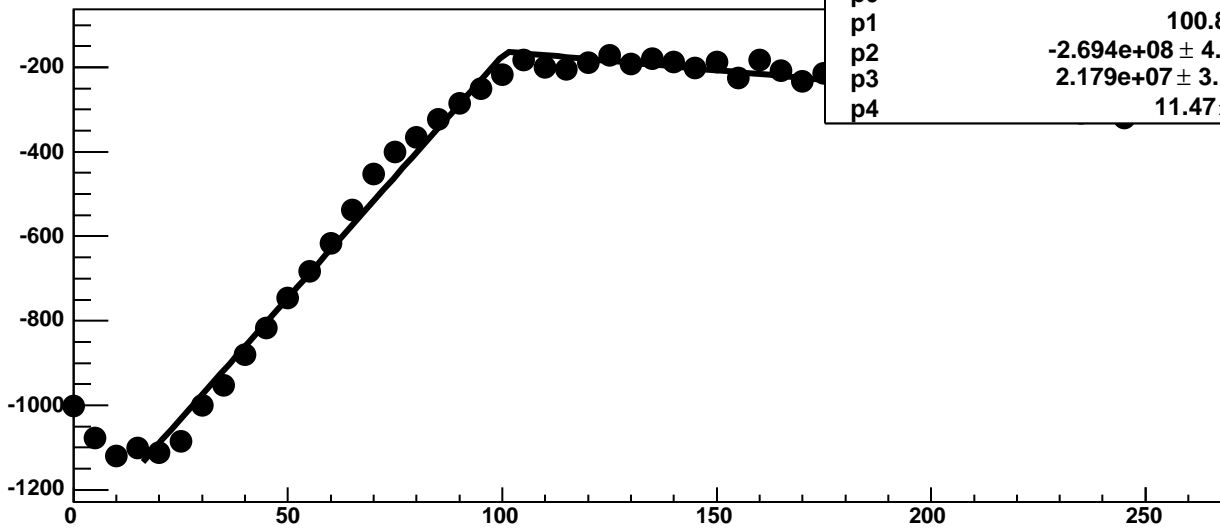
Chip 0, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

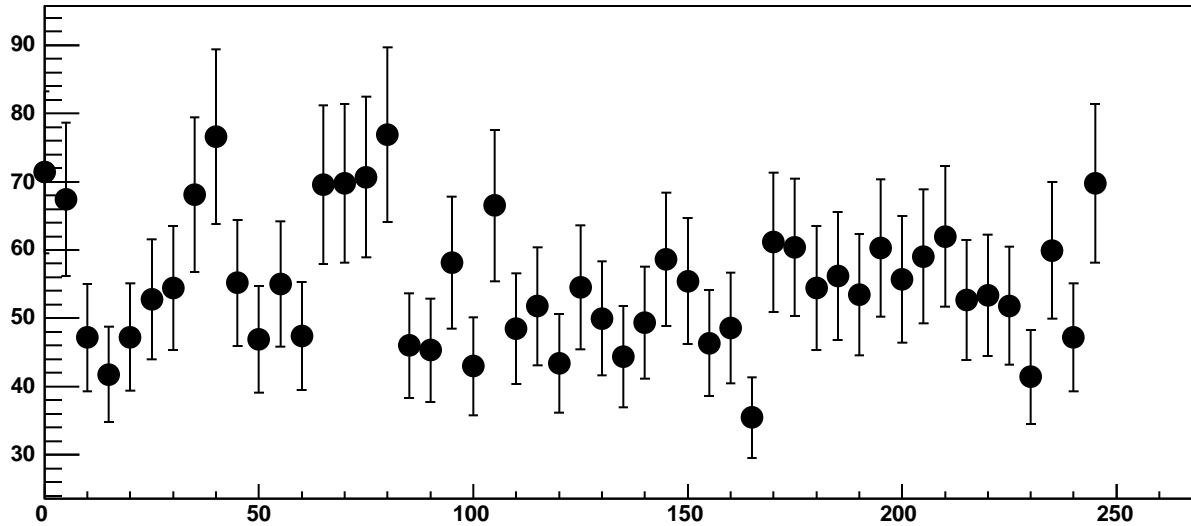


Chip 0, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

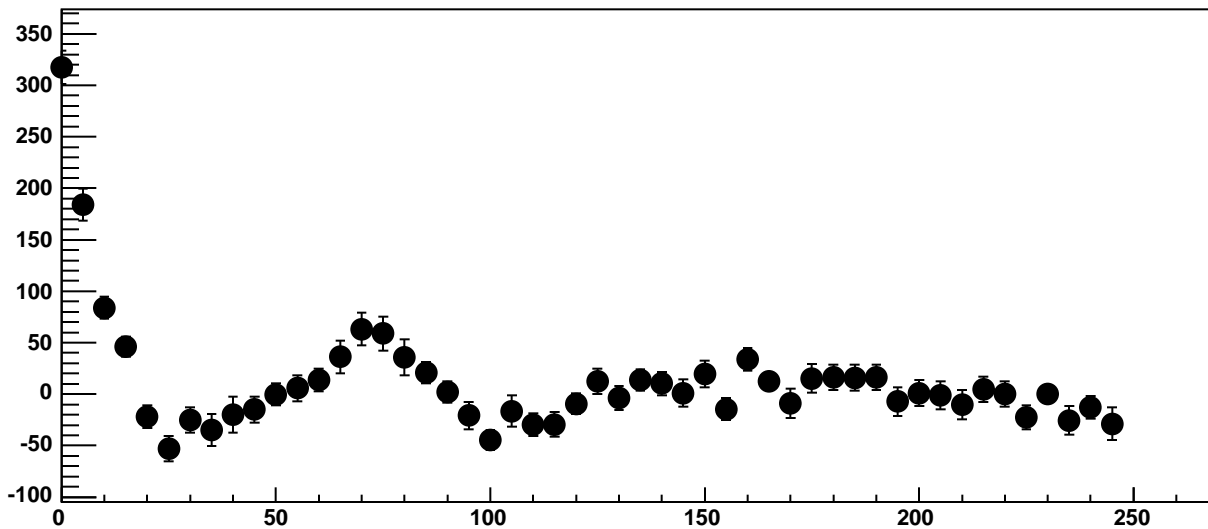


$\chi^2 / \text{ndf}$	175.5 / 41
p0	$-163.2 \pm 4.171$
p1	$100.8 \pm 0.564$
p2	$-2.694\text{e}+08 \pm 4.658\text{e}+06$
p3	$2.179\text{e}+07 \pm 3.181\text{e}+05$
p4	$11.47 \pm 0.1026$

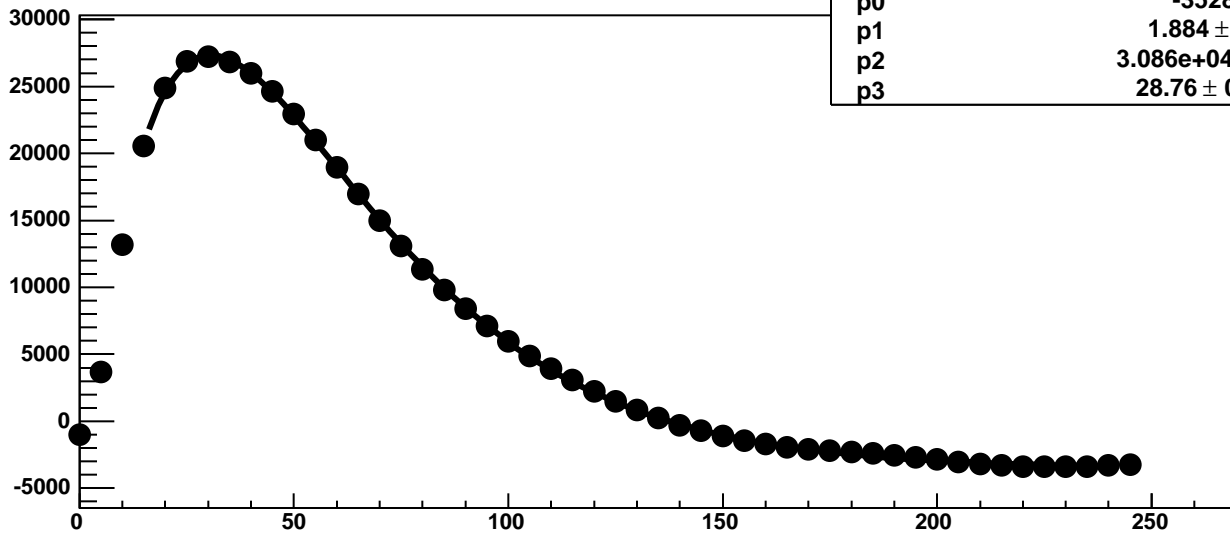
Chip 0, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

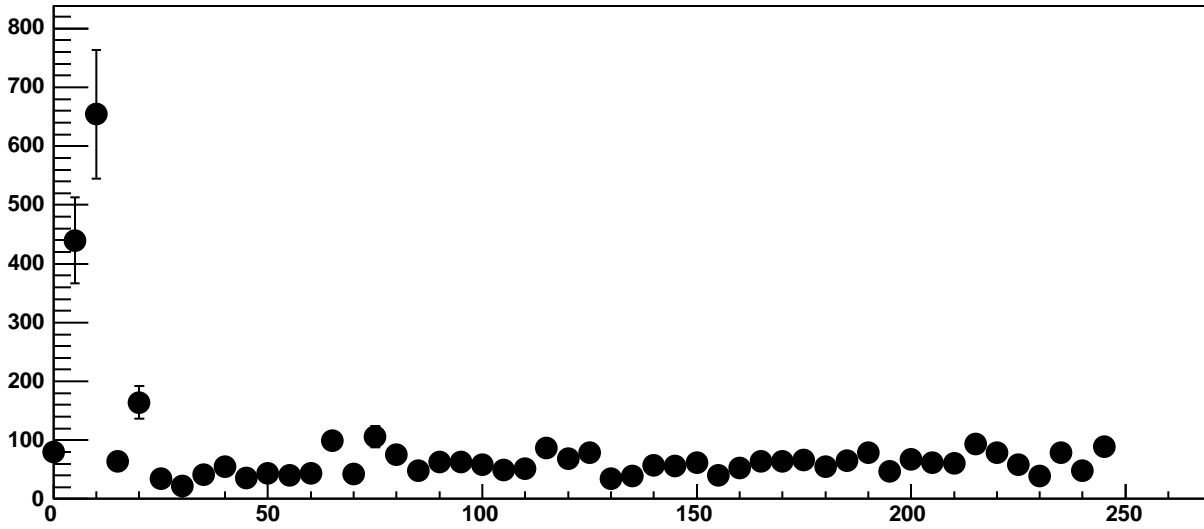


Chip 0, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold

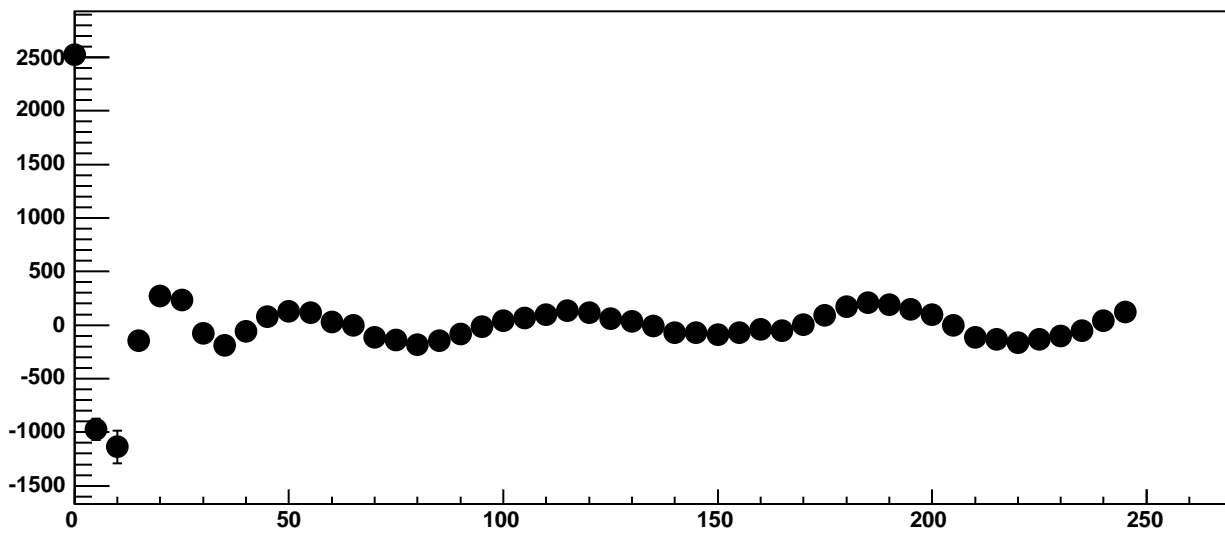


$\chi^2 / \text{ndf}$	4222 / 42
p0	-3528 ± 3.657
p1	1.884 ± 0.01561
p2	3.086e+04 ± 4.386
p3	28.76 ± 0.009861

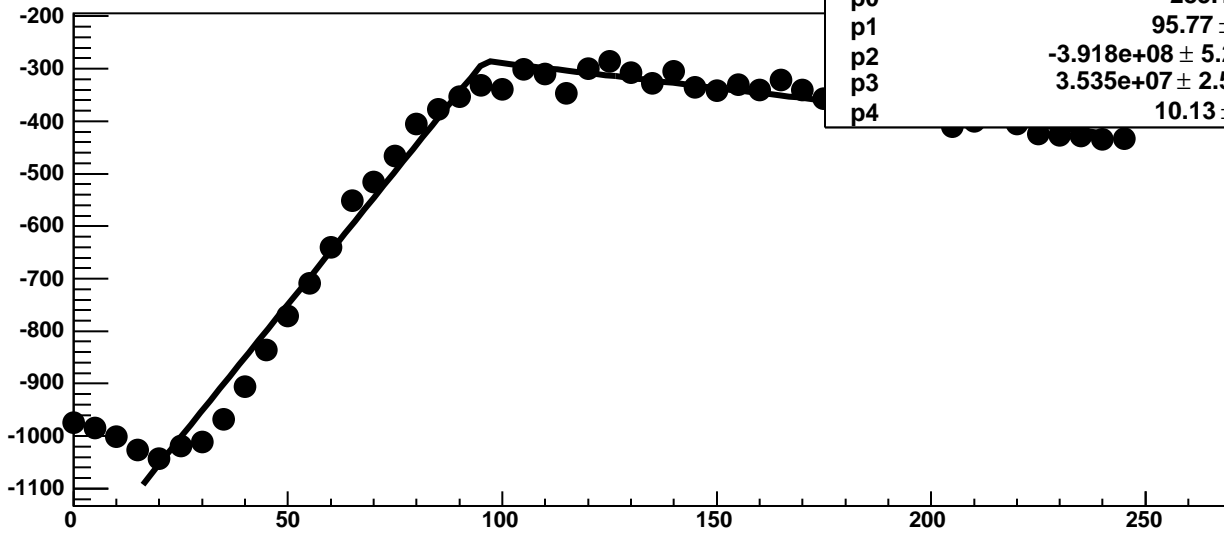
Chip 0, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold

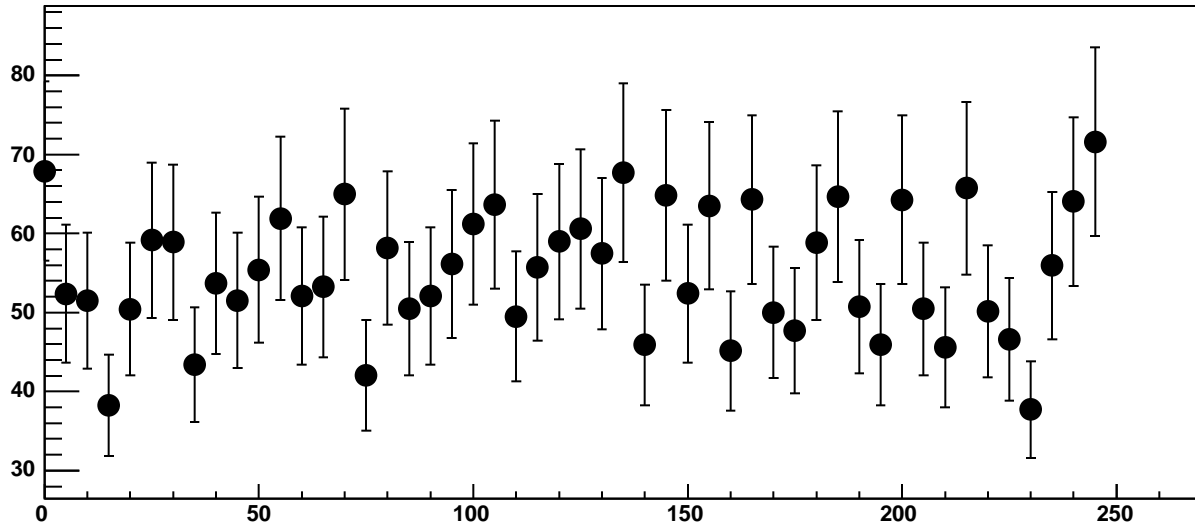


Chip 0, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

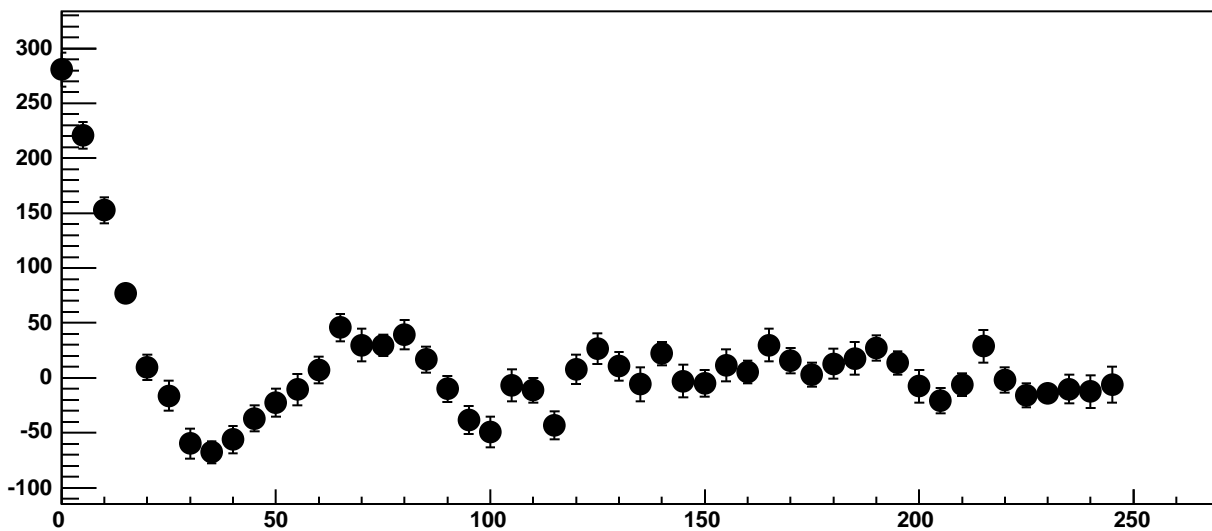


$\chi^2 / \text{ndf}$	292.1 / 41
p0	$-285.1 \pm 4.487$
p1	$95.77 \pm 0.6706$
p2	$-3.918\text{e}+08 \pm 5.212\text{e}+06$
p3	$3.535\text{e}+07 \pm 2.523\text{e}+05$
p4	$10.13 \pm 0.1127$

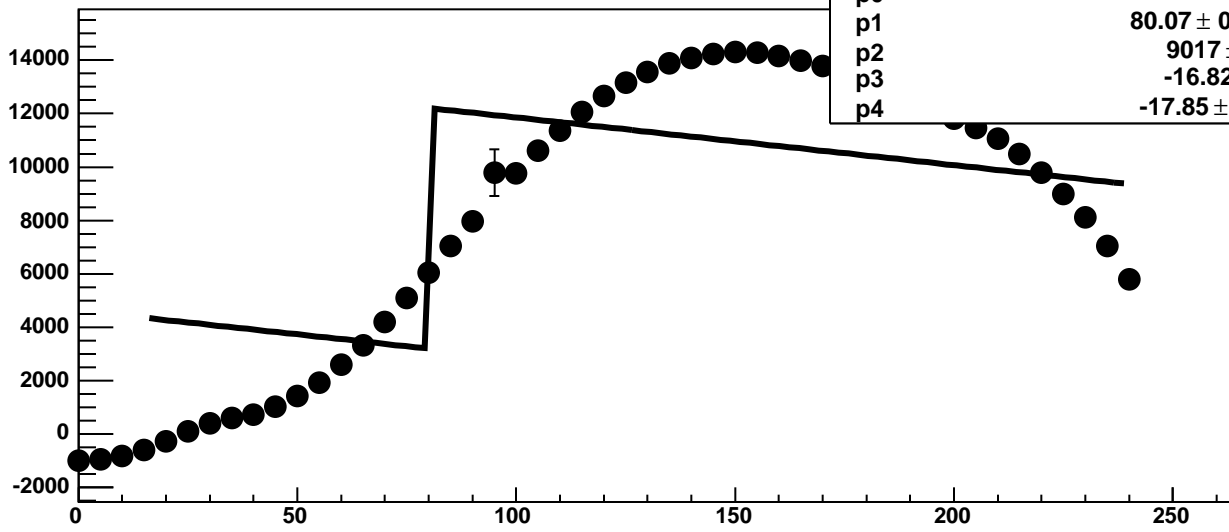
Chip 0, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

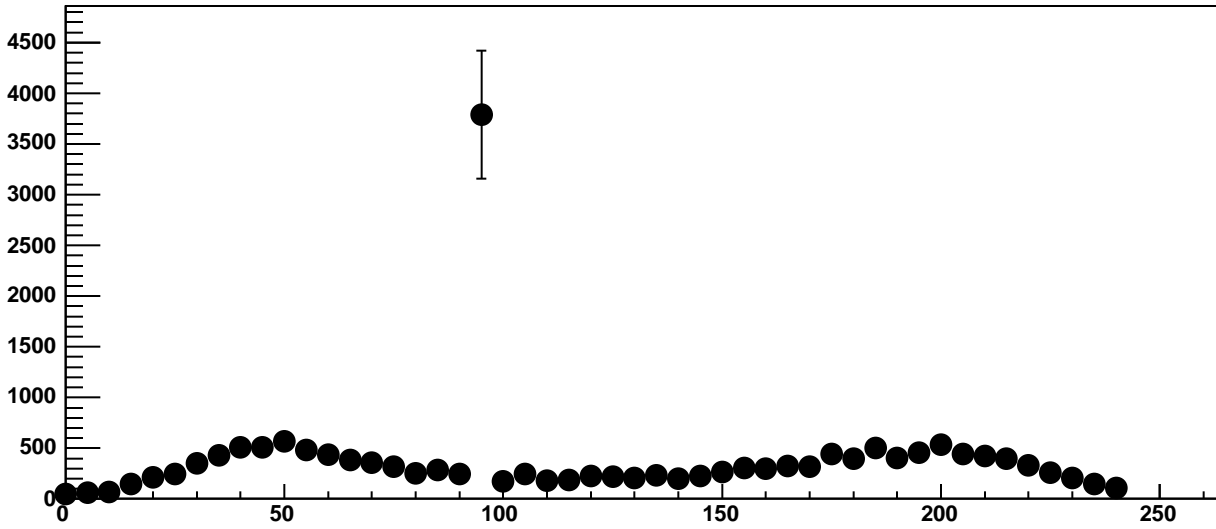


Chip 0, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

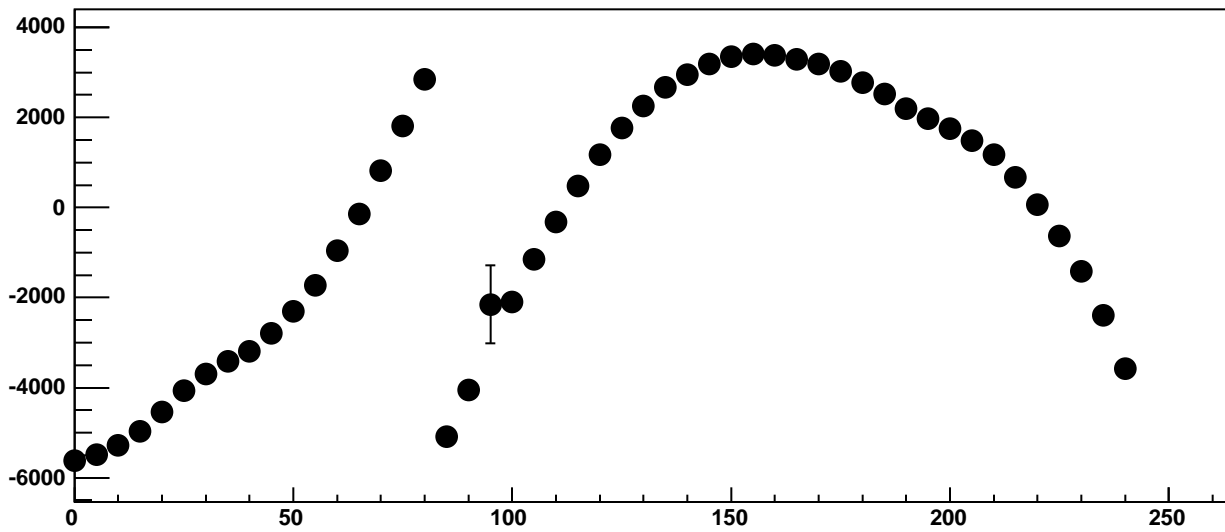


$\chi^2 / \text{ndf}$	1.135e+05 / 41
p0	3194 ± 0.3087
p1	80.07 ± 0.001204
p2	9017 ± 0.3089
p3	-16.82 ± 1.435
p4	-17.85 ± 0.09119

Chip 0, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



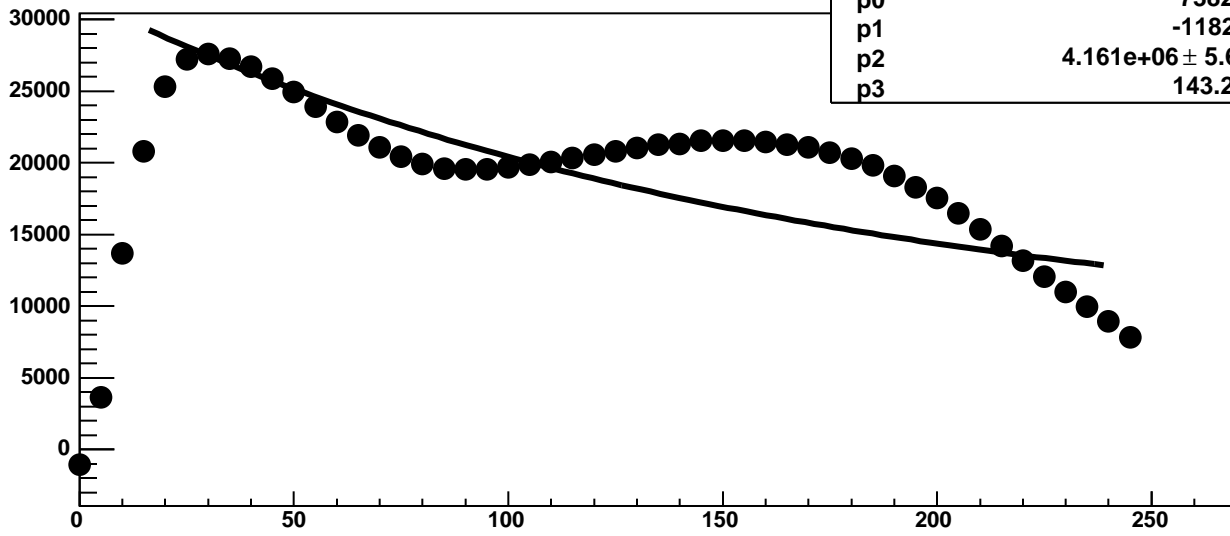
Chip 0, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



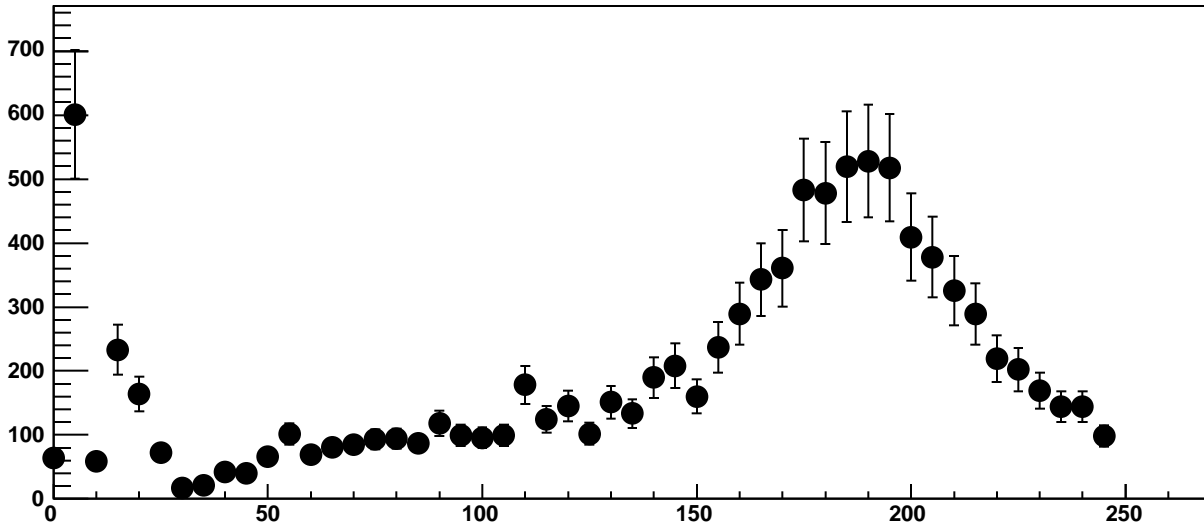


Chip 0, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold

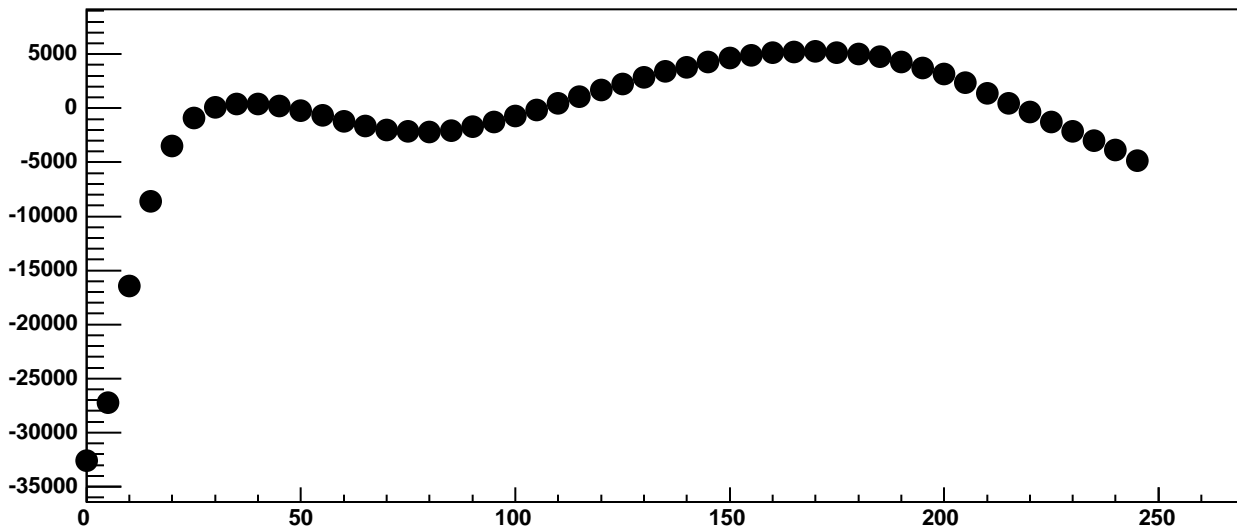
$\chi^2 / \text{ndf}$	2.346e+05 / 42
p0	7382 ± 72.35
p1	-1182 ± 6.978
p2	4.161e+06 ± 5.664e+04
p3	143.2 ± 0.759



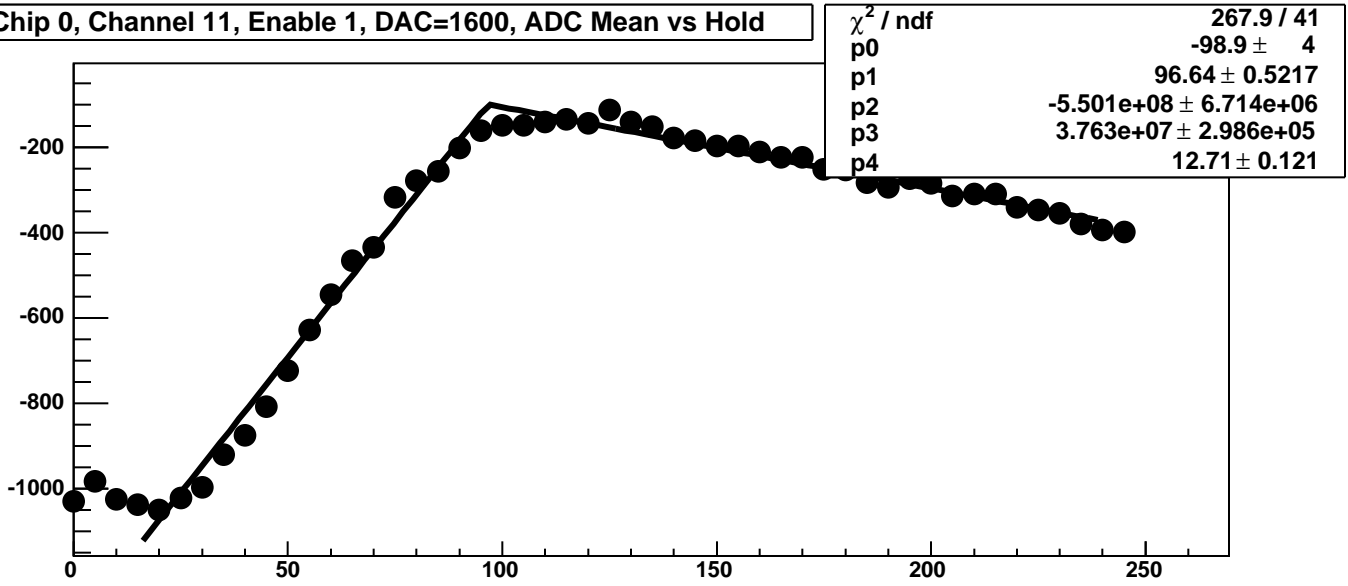
Chip 0, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



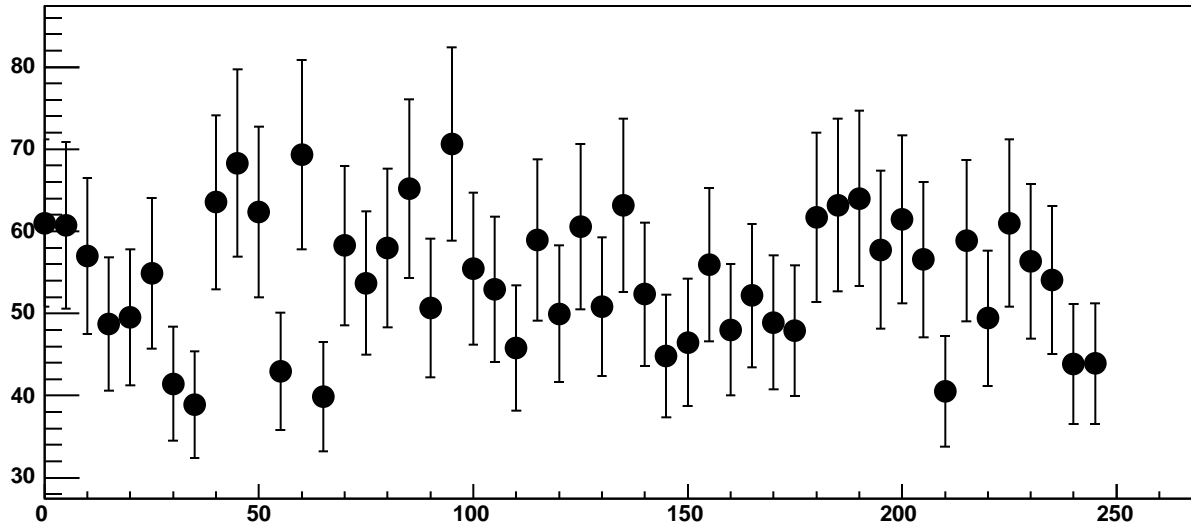
Chip 0, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold



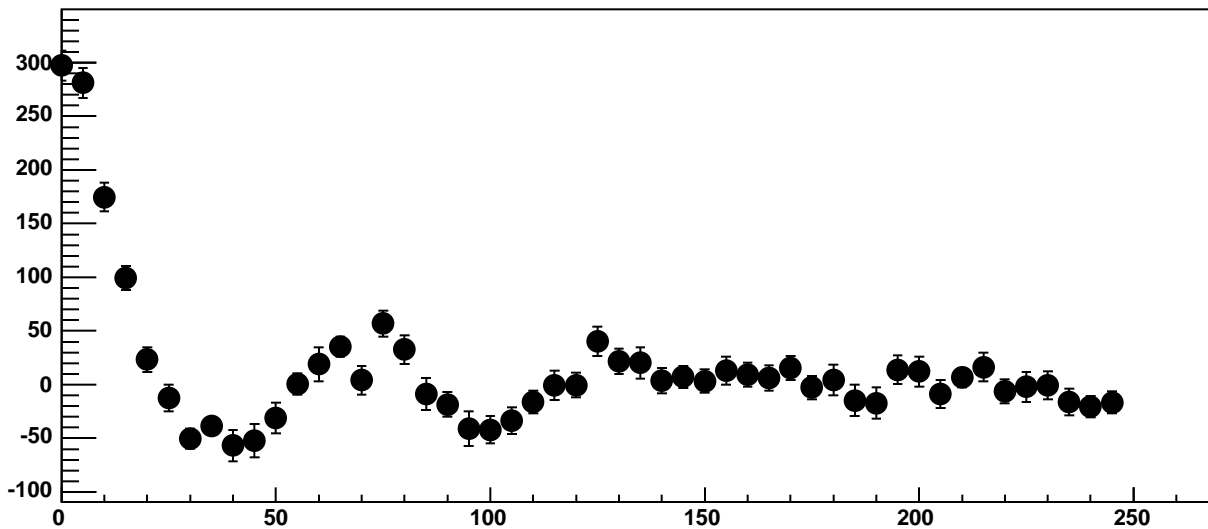
Chip 0, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold



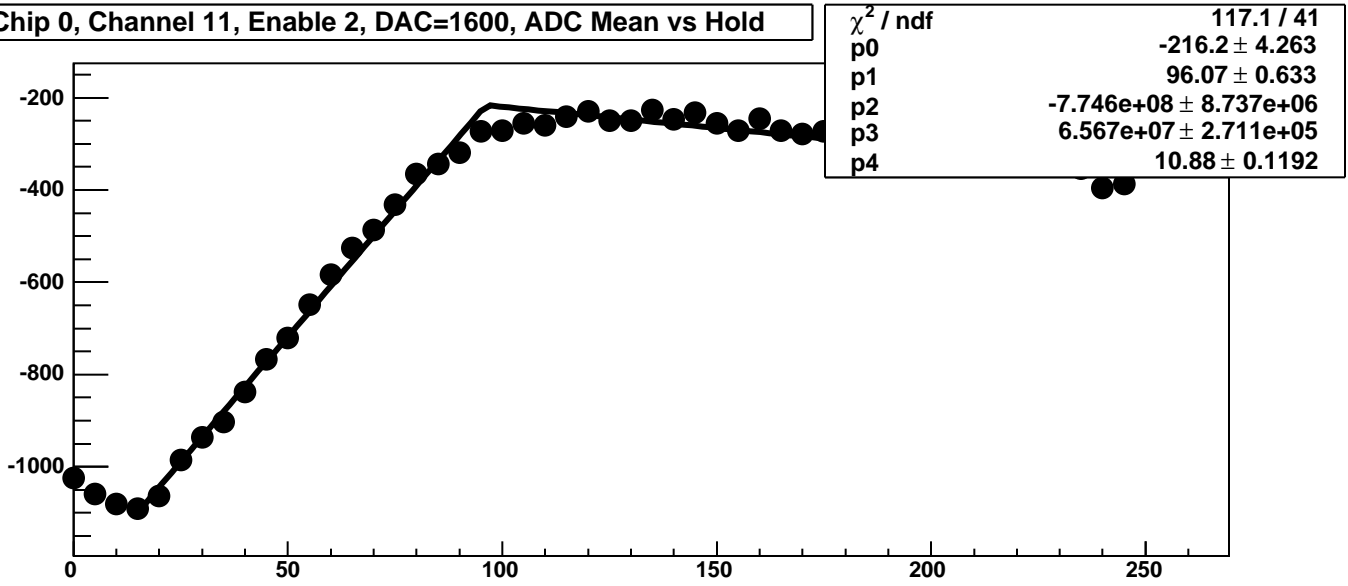
Chip 0, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



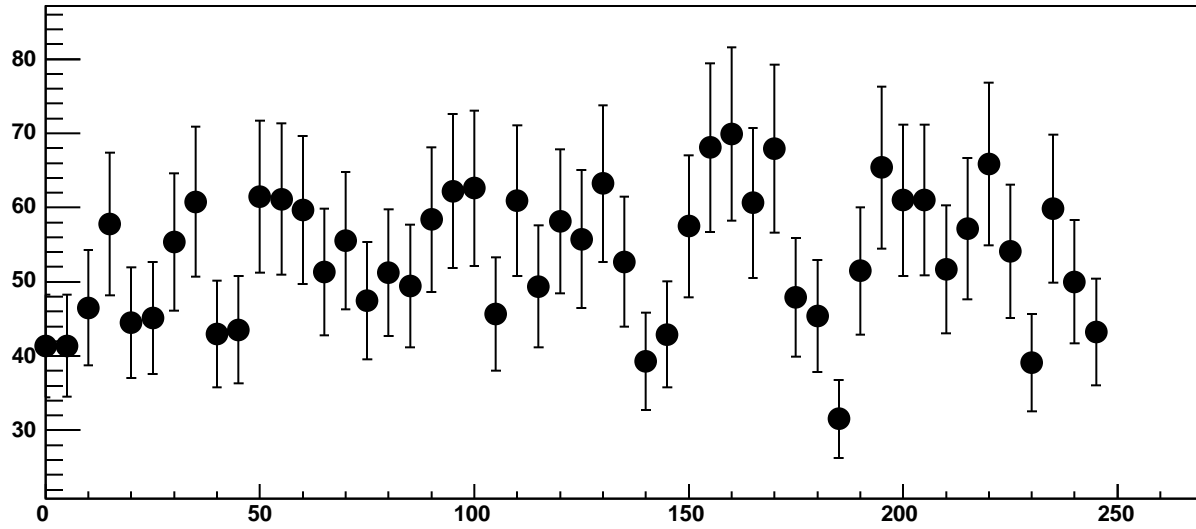
Chip 0, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold



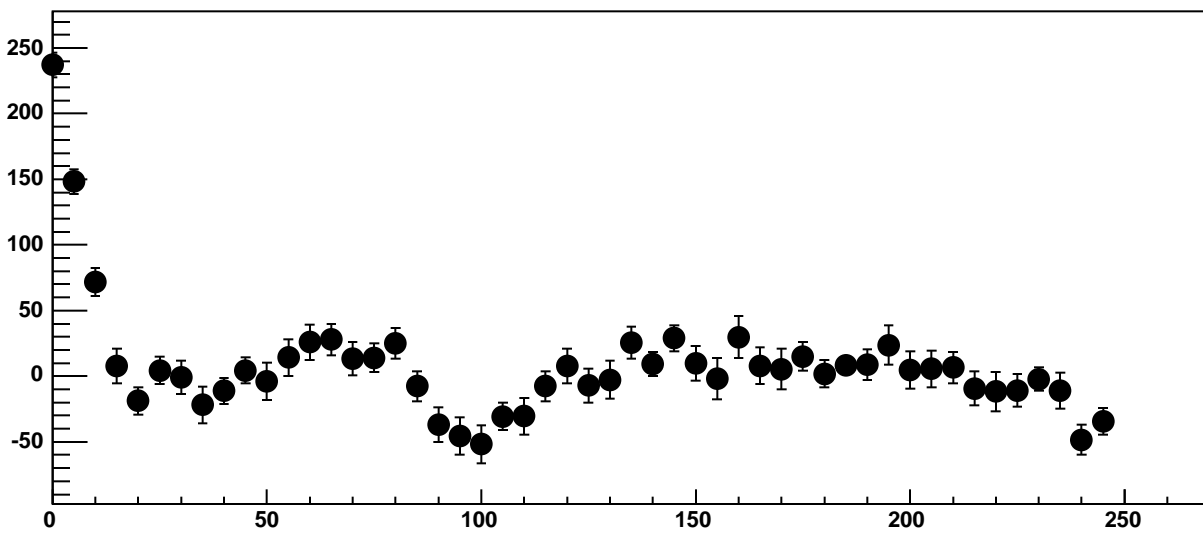
Chip 0, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold



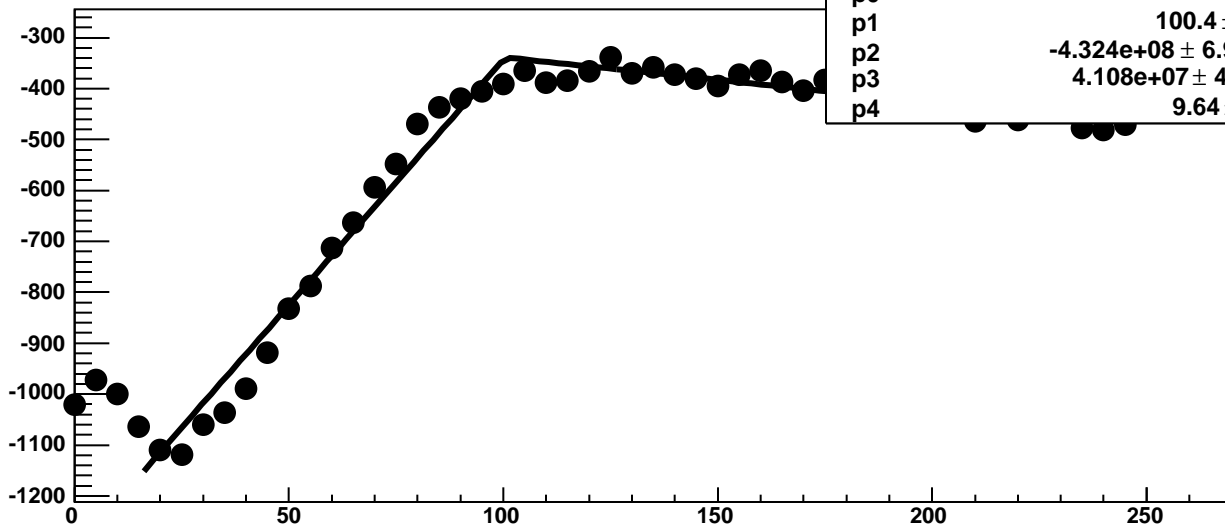
Chip 0, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

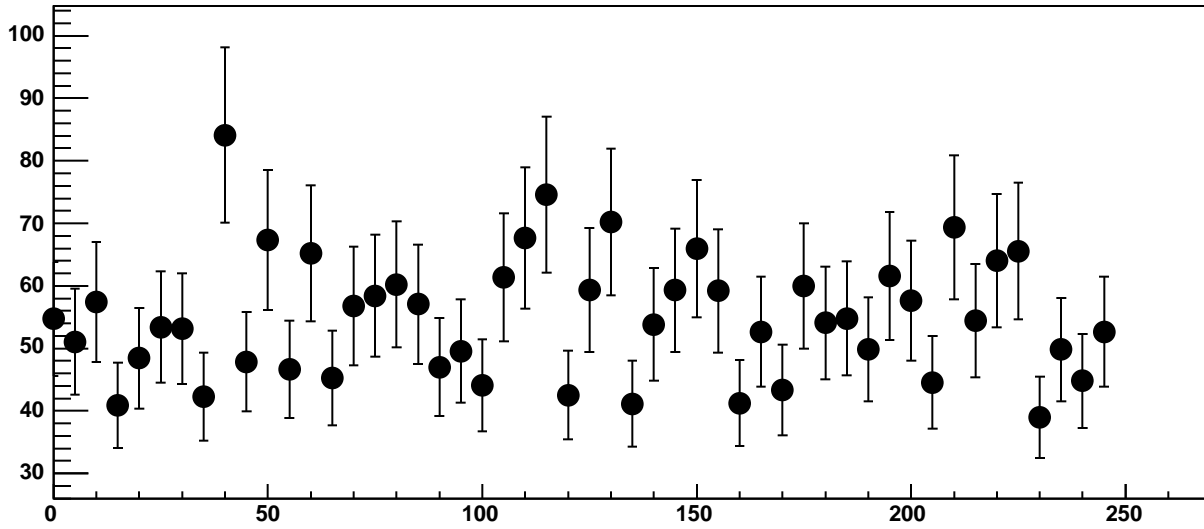


Chip 0, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold

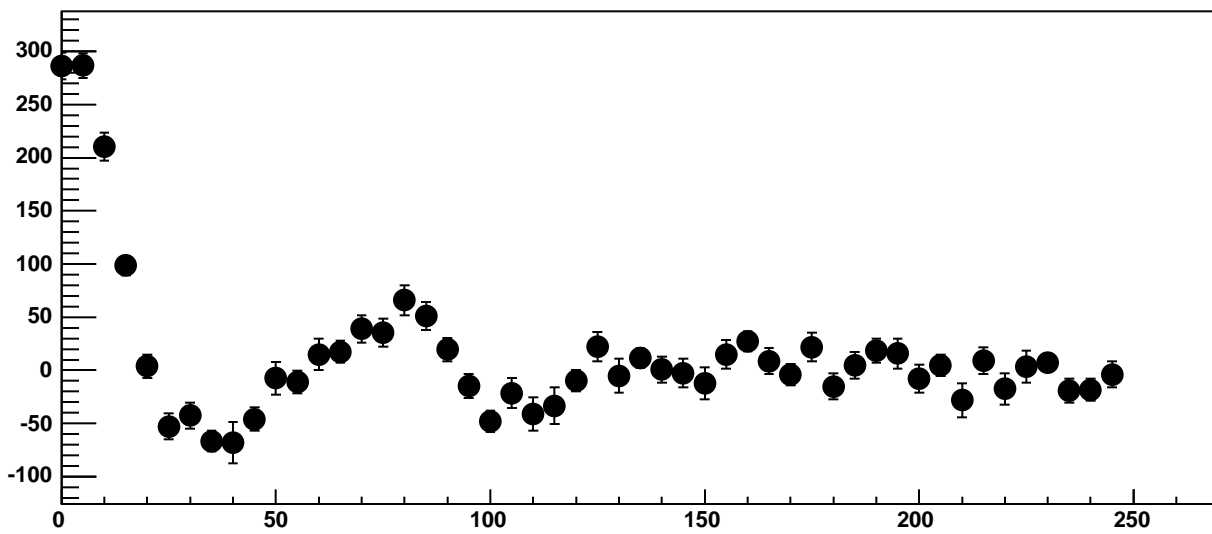


$\chi^2 / \text{ndf}$	354 / 41
p0	$-338.7 \pm 4.515$
p1	$100.4 \pm 0.6788$
p2	$-4.324\text{e}+08 \pm 6.998\text{e}+06$
p3	$4.108\text{e}+07 \pm 4.74\text{e}+05$
p4	$9.64 \pm 0.1001$

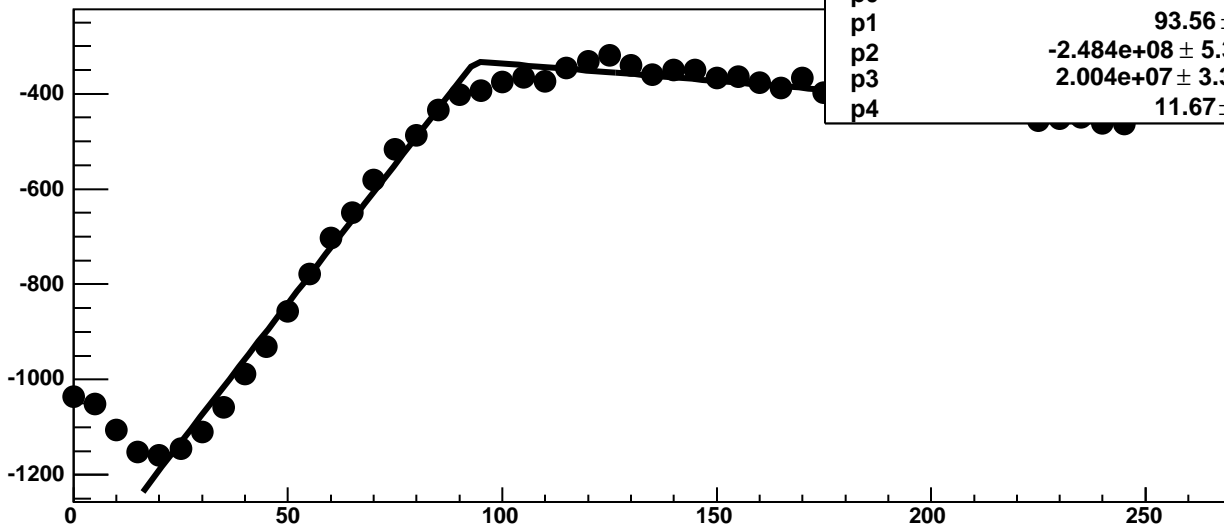
Chip 0, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

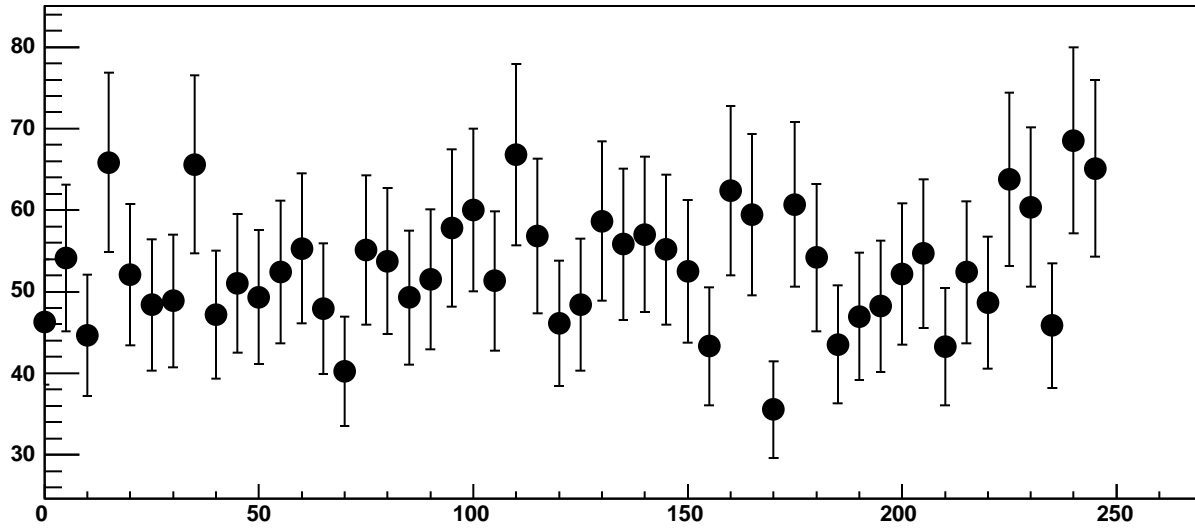


Chip 0, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

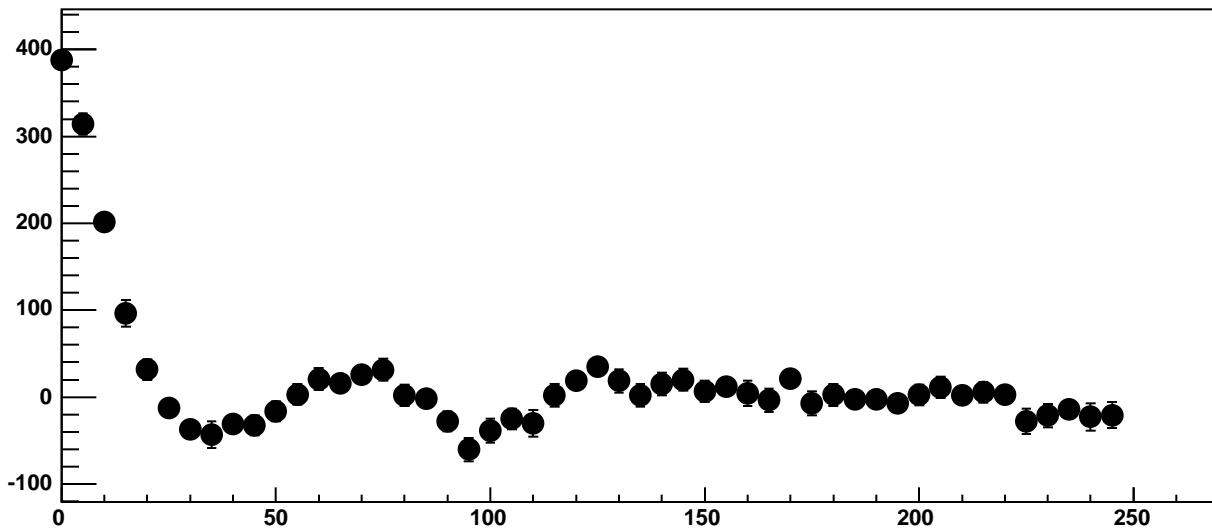


$\chi^2 / \text{ndf}$	187.7 / 41
p0	$-331.9 \pm 4.319$
p1	$93.56 \pm 0.6053$
p2	$-2.484\text{e}+08 \pm 5.366\text{e}+06$
p3	$2.004\text{e}+07 \pm 3.393\text{e}+05$
p4	$11.67 \pm 0.1315$

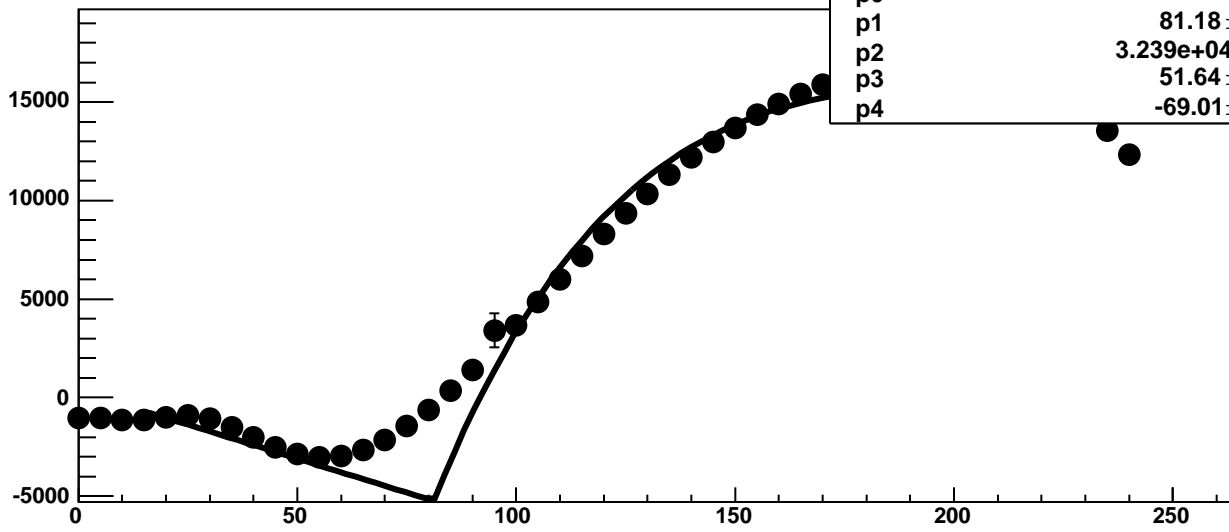
Chip 0, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

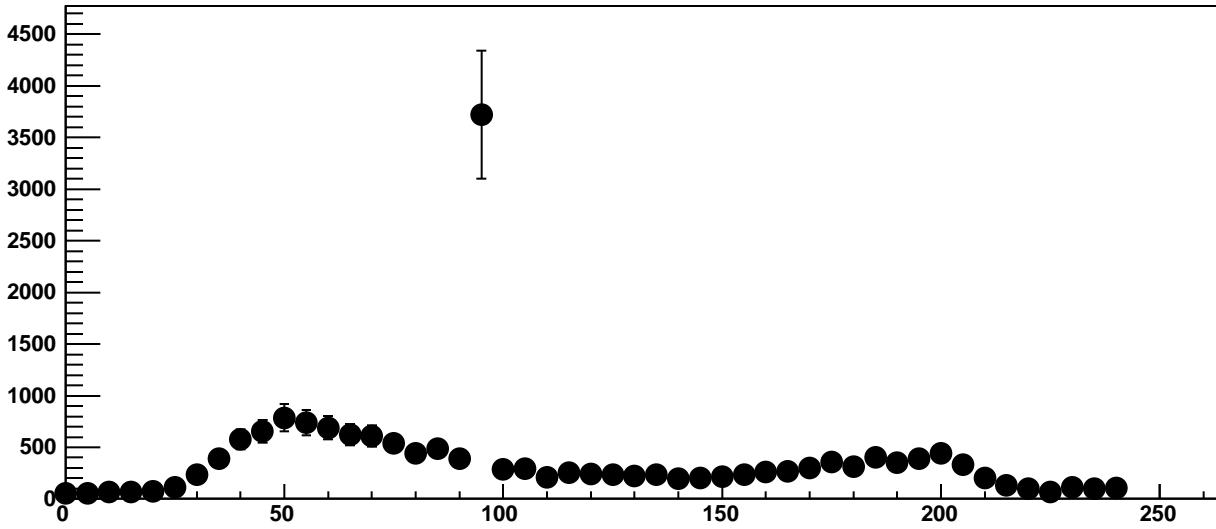


Chip 0, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

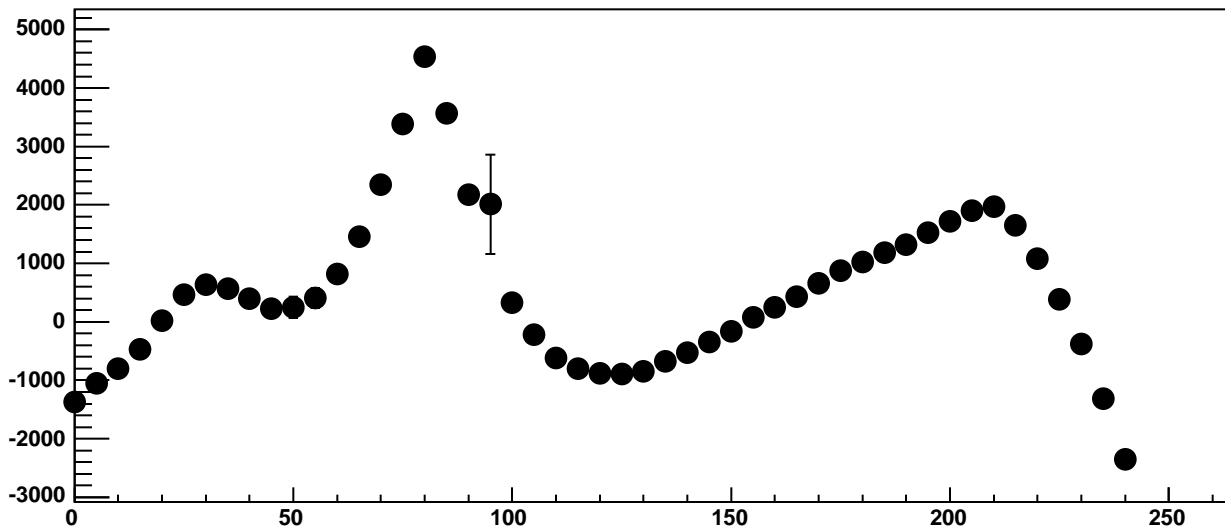


$\chi^2 / \text{ndf}$	2.994e+04 / 41
p0	-5249 ± 39.14
p1	81.18 ± 0.1257
p2	3.239e+04 ± 176.4
p3	51.64 ± 0.2718
p4	-69.01 ± 0.7098

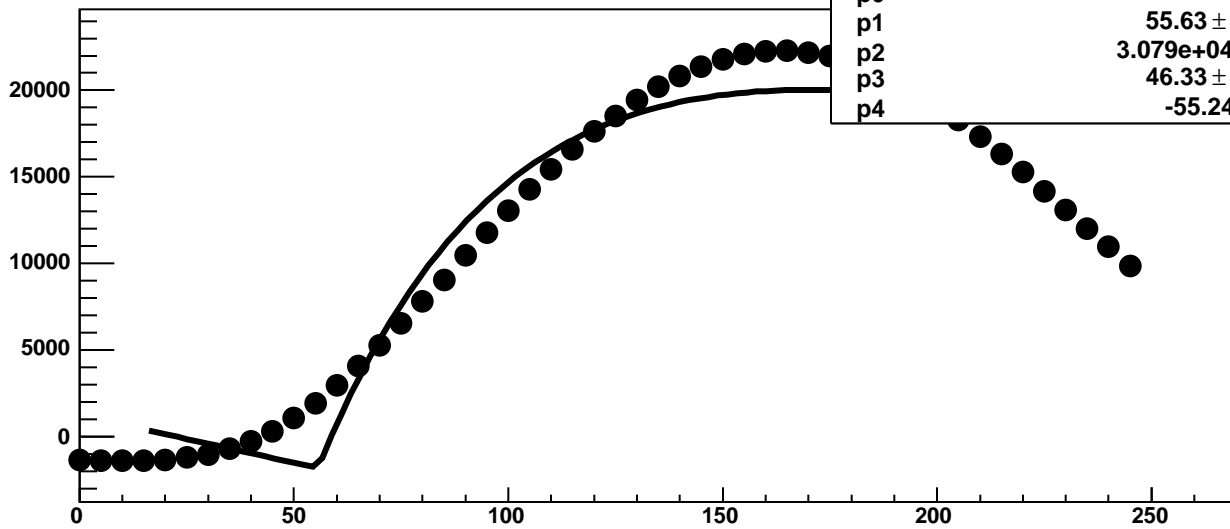
Chip 0, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



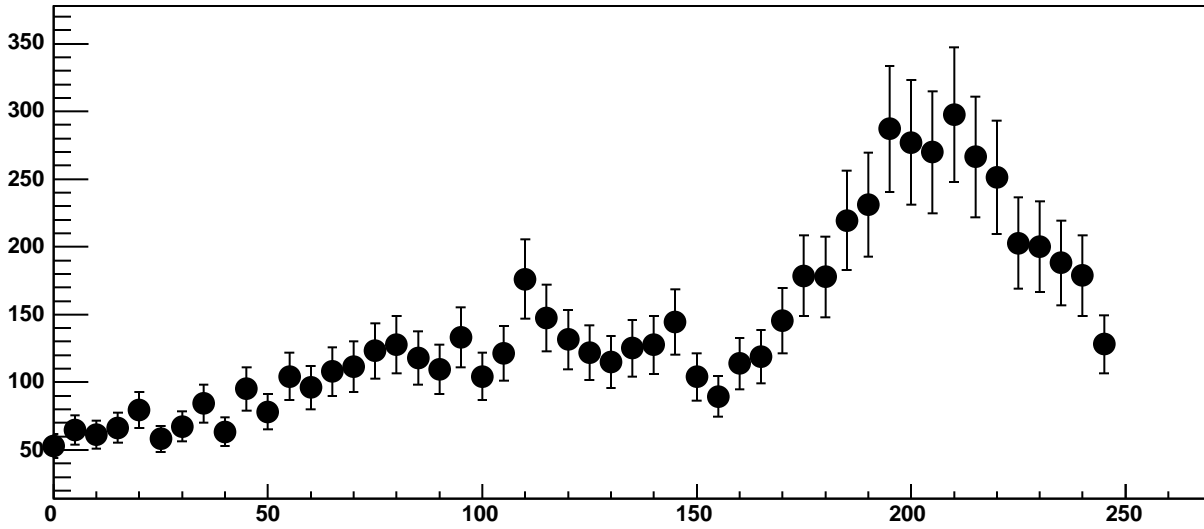
Chip 0, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



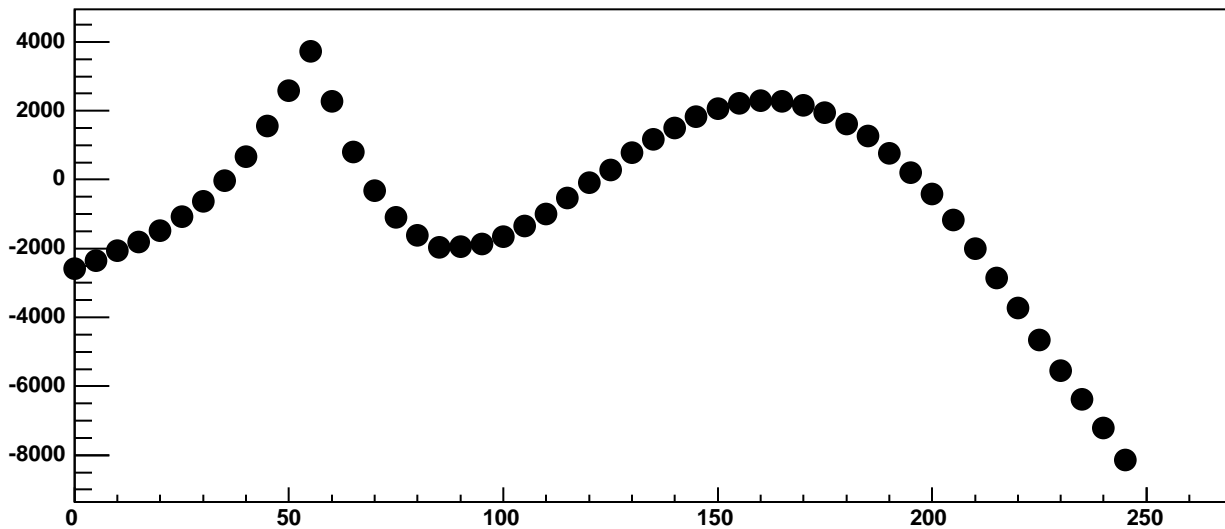
Chip 0, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



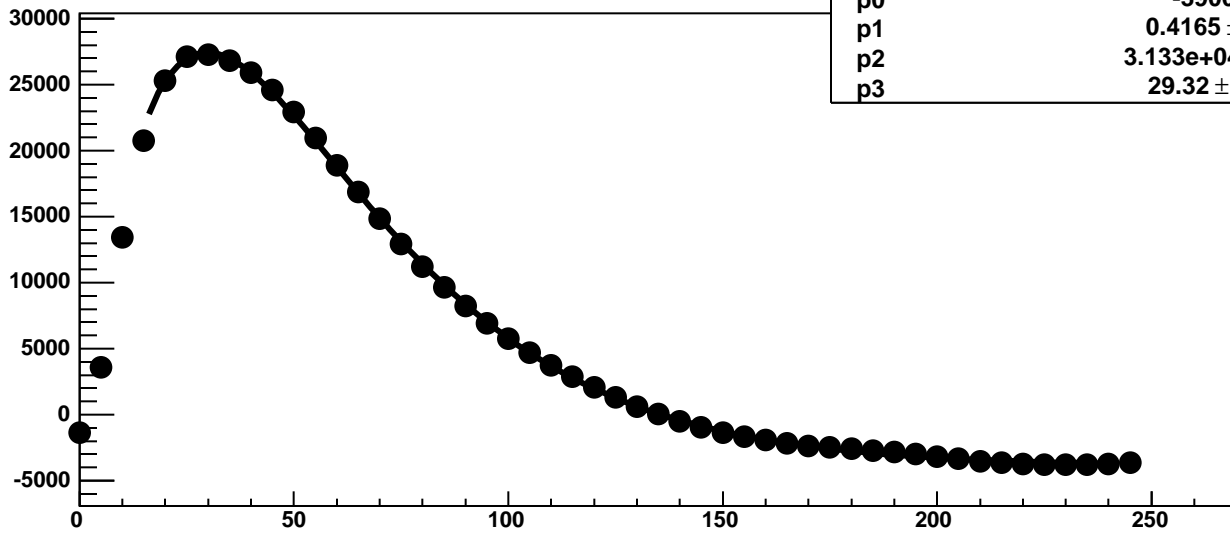
Chip 0, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

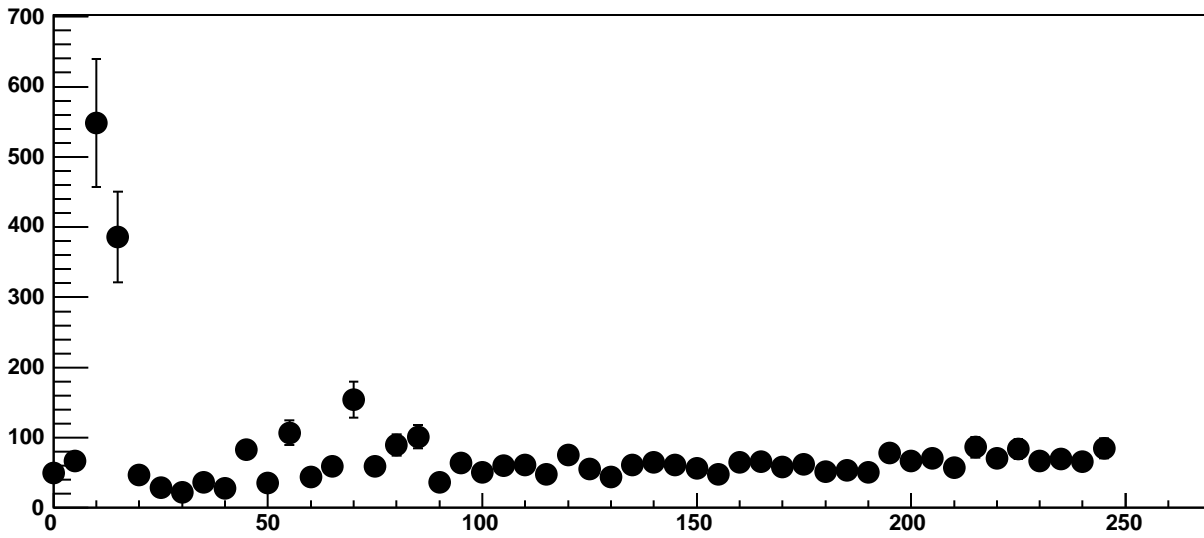


Chip 0, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

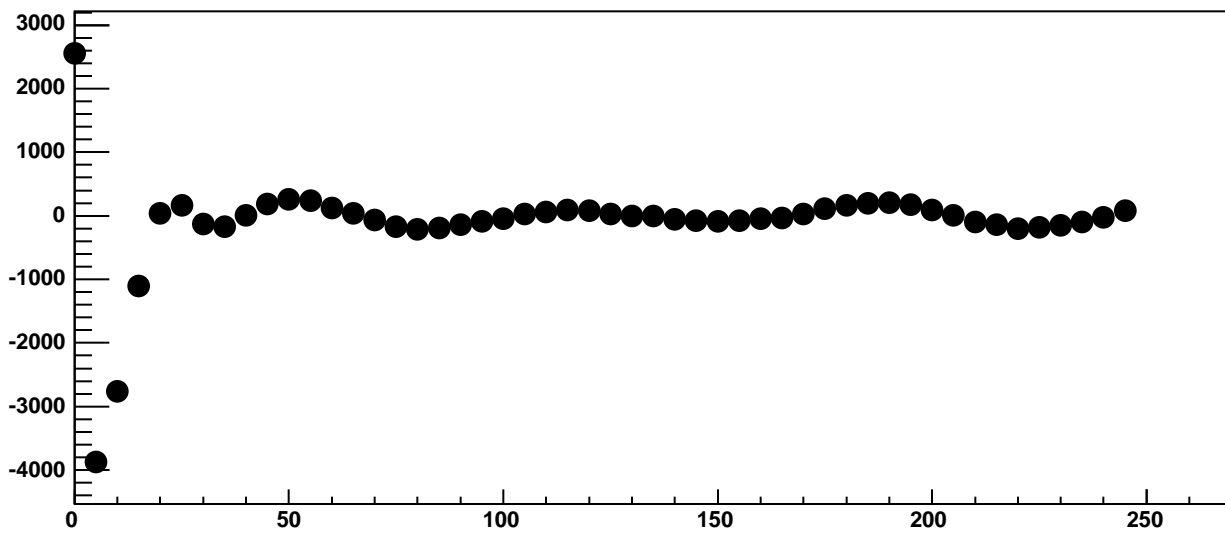


$\chi^2 / \text{ndf}$	5633 / 42
p0	$-3900 \pm 4.235$
p1	$0.4165 \pm 0.0207$
p2	$3.133\text{e}+04 \pm 4.78$
p3	$29.32 \pm 0.01179$

Chip 0, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

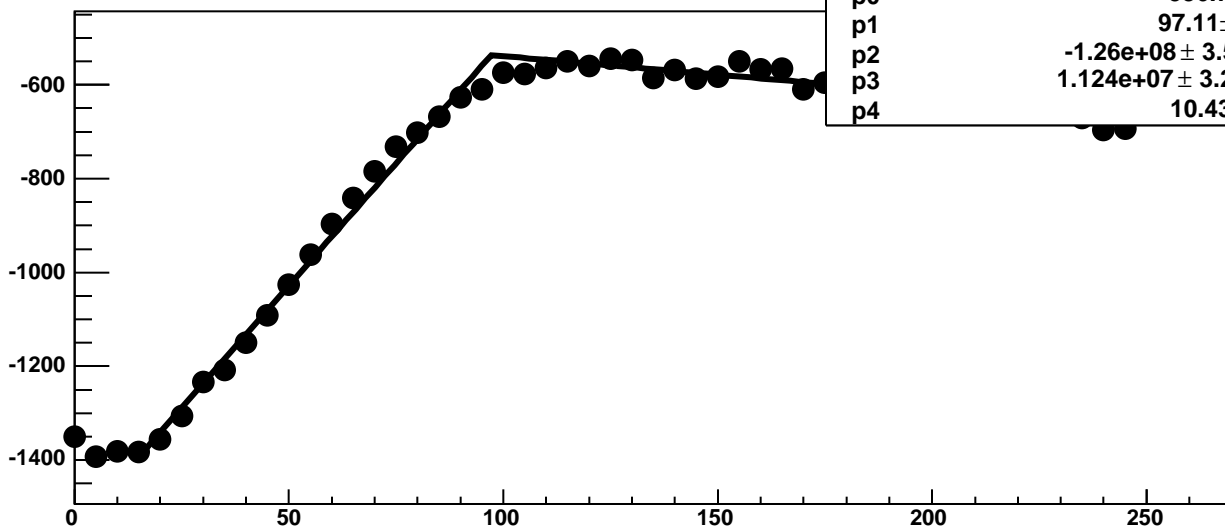


Chip 0, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



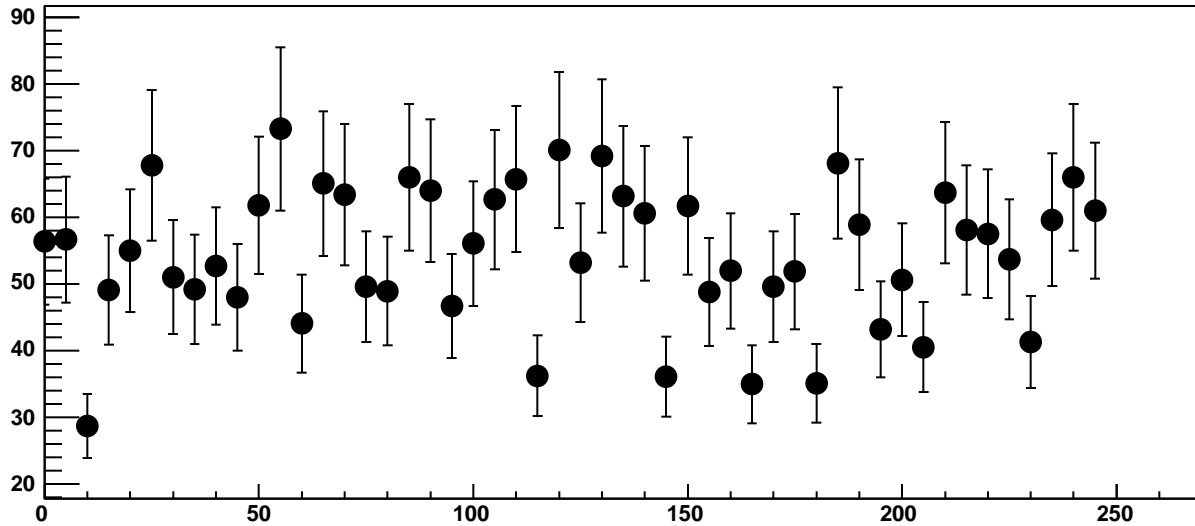


Chip 0, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

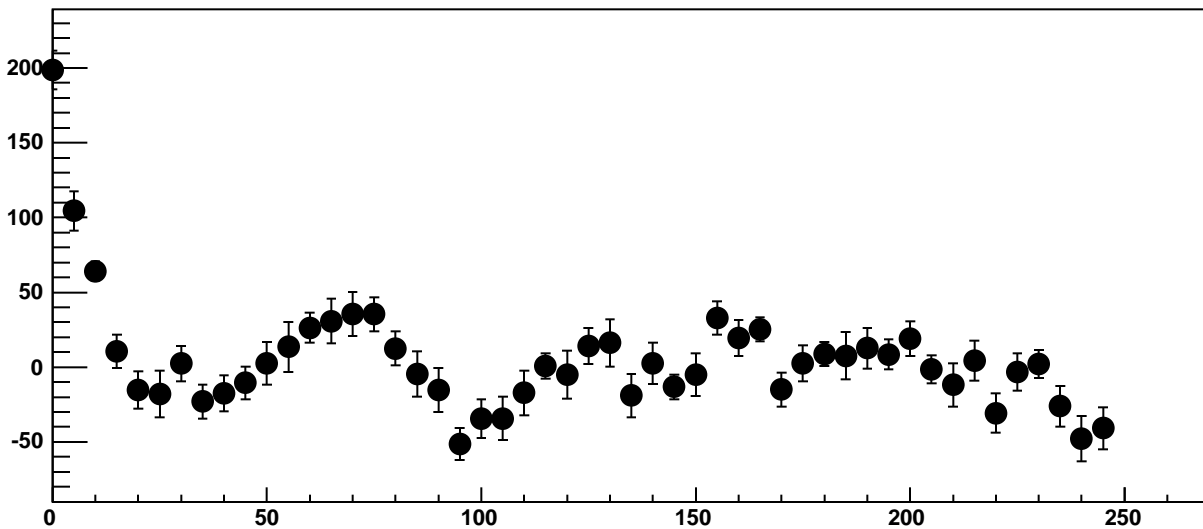


$\chi^2 / \text{ndf}$	133.4 / 41
p0	$-536.7 \pm 4.178$
p1	$97.11 \pm 0.6445$
p2	$-1.26\text{e}+08 \pm 3.522\text{e}+06$
p3	$1.124\text{e}+07 \pm 3.238\text{e}+05$
p4	$10.43 \pm 0.113$

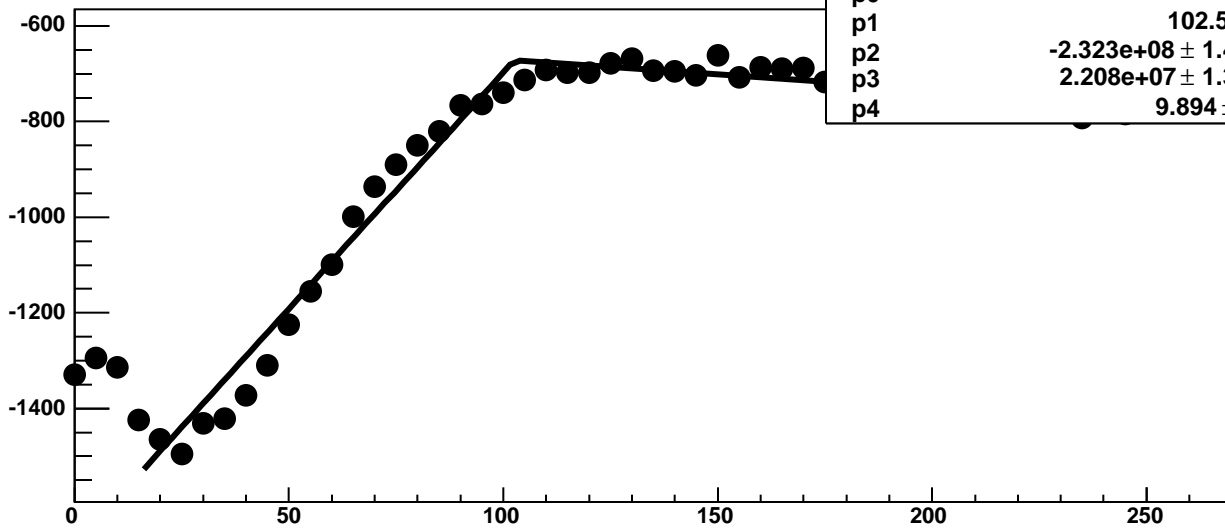
Chip 0, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

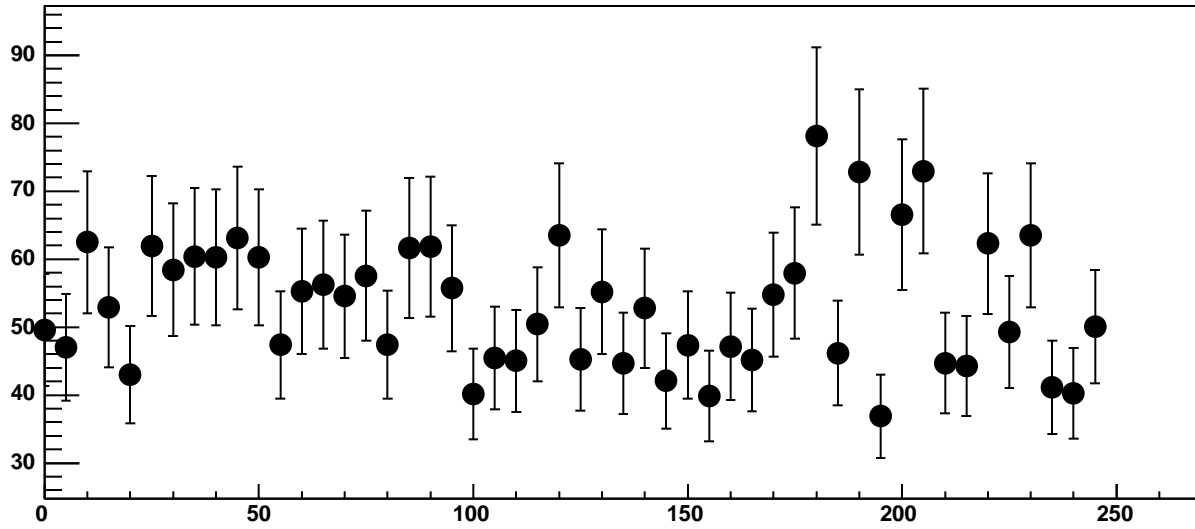


Chip 0, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

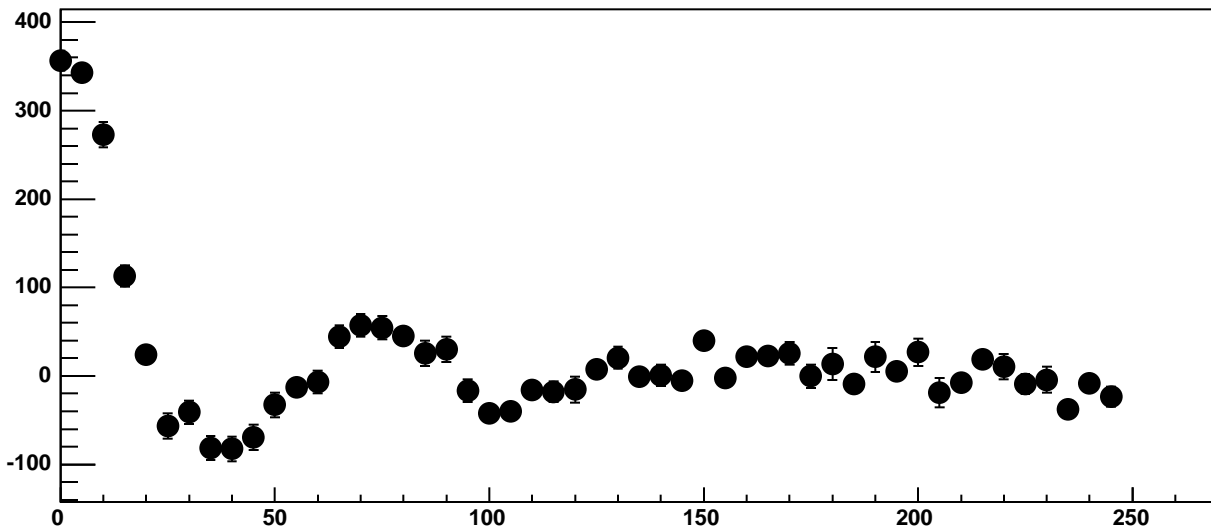


$\chi^2 / \text{ndf}$	396 / 41
p0	$-671.7 \pm 3.918$
p1	$102.5 \pm 0.657$
p2	$-2.323\text{e}+08 \pm 1.478\text{e}+07$
p3	$2.208\text{e}+07 \pm 1.386\text{e}+06$
p4	$9.894 \pm 0.1068$

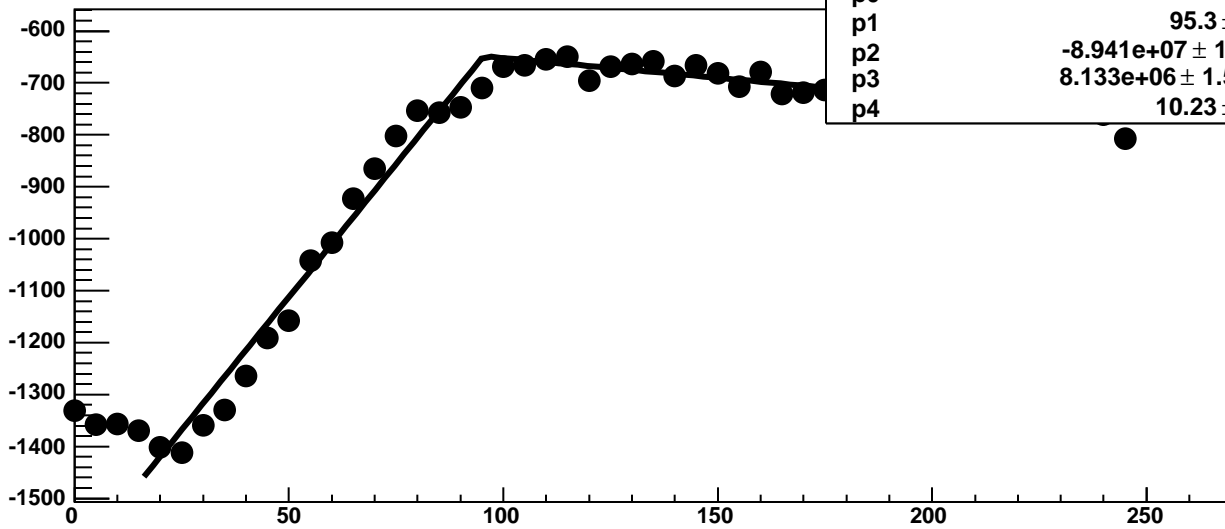
Chip 0, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

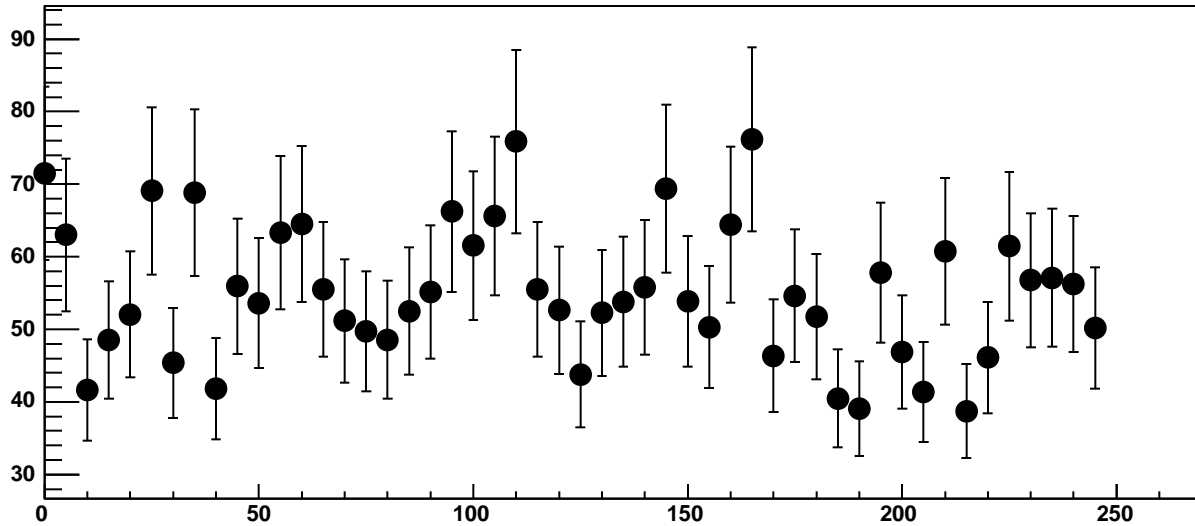


Chip 0, Channel 12, Enable 4, DAC=1600, ADC Mean vs Hold

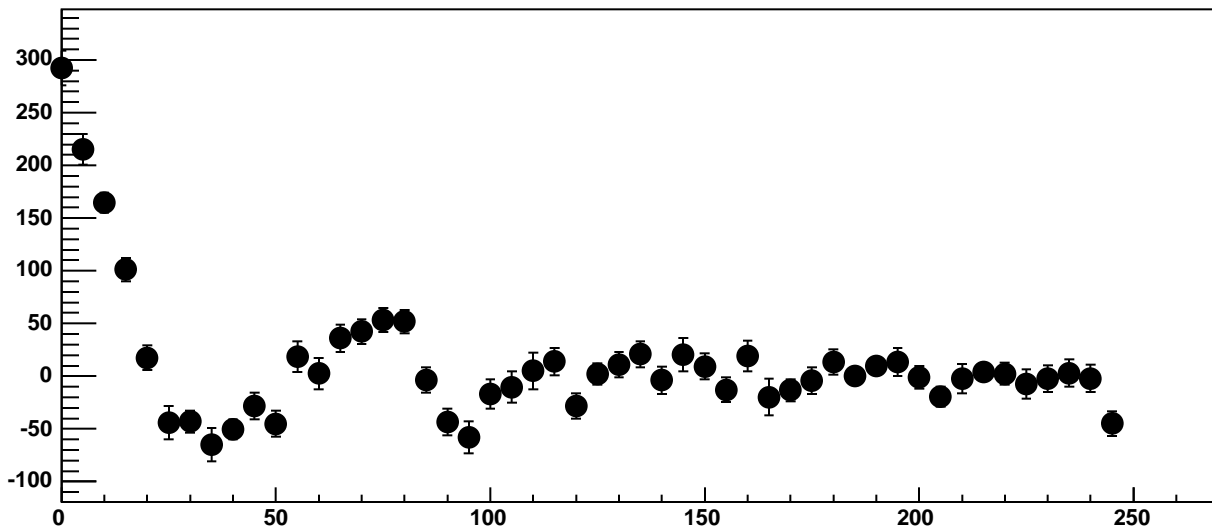


$\chi^2 / \text{ndf}$	294.5 / 41
p0	$-648.6 \pm 4.632$
p1	$95.3 \pm 0.6989$
p2	$-8.941\text{e}+07 \pm 1.72\text{e}+07$
p3	$8.133\text{e}+06 \pm 1.561\text{e}+06$
p4	$10.23 \pm 0.1223$

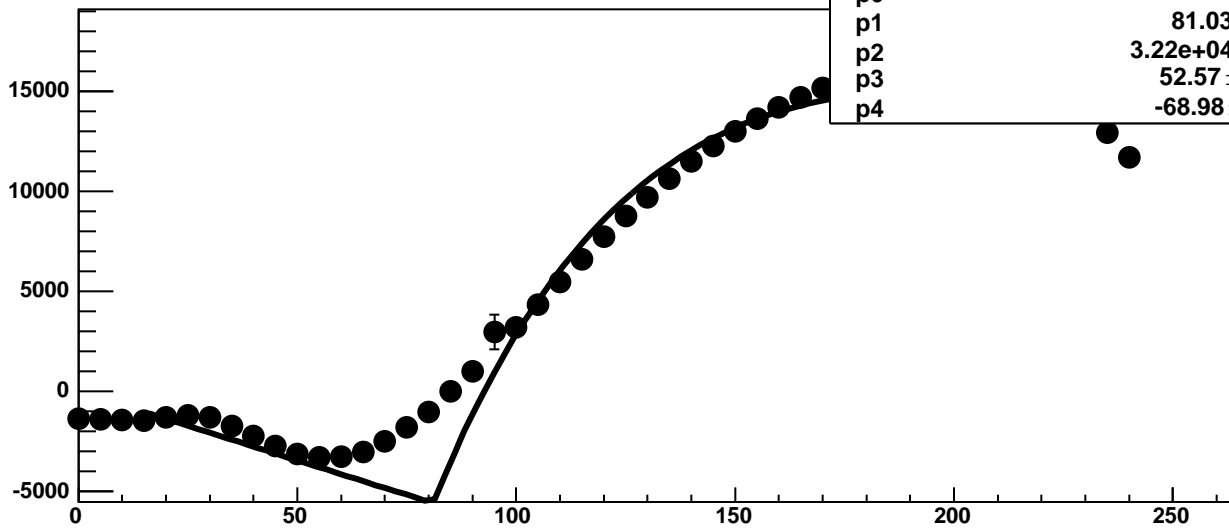
Chip 0, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold

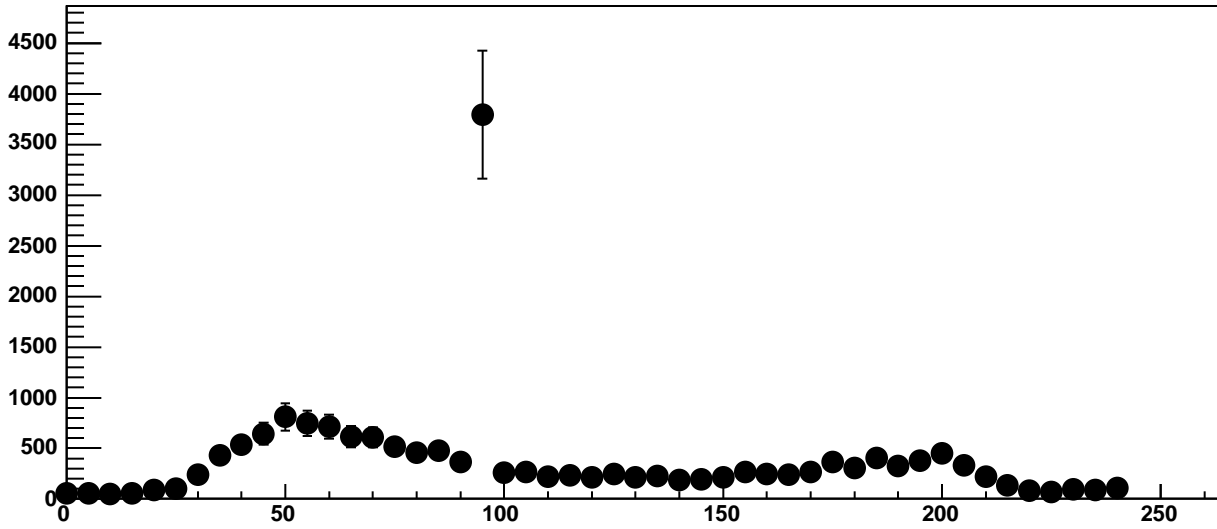


Chip 0, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

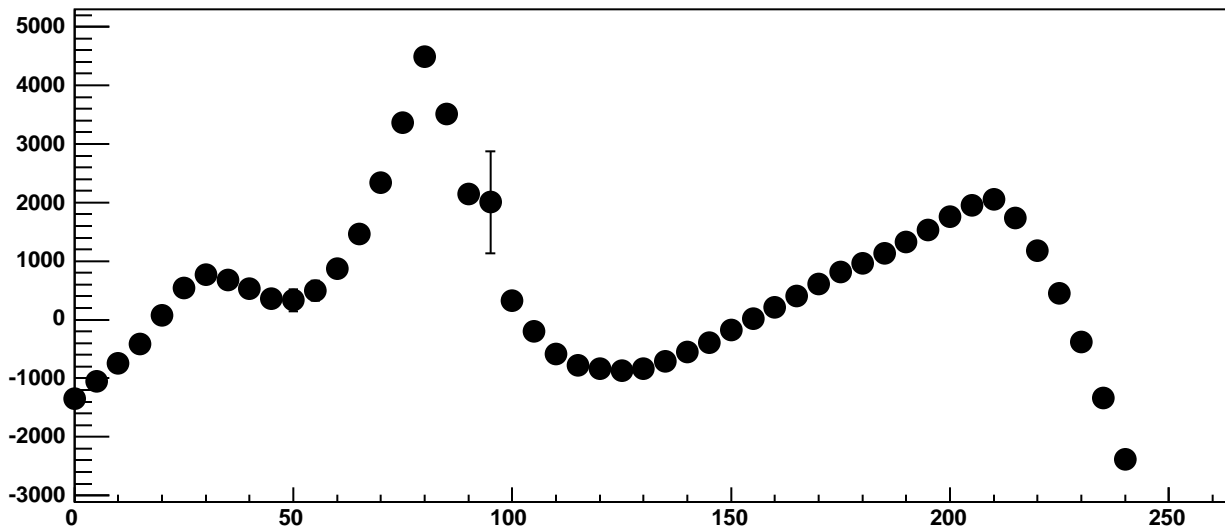


$\chi^2 / \text{ndf}$	3.327e+04 / 41
p0	-5586 ± 38.57
p1	81.03 ± 0.124
p2	3.22e+04 ± 174.6
p3	52.57 ± 0.2719
p4	-68.98 ± 0.6961

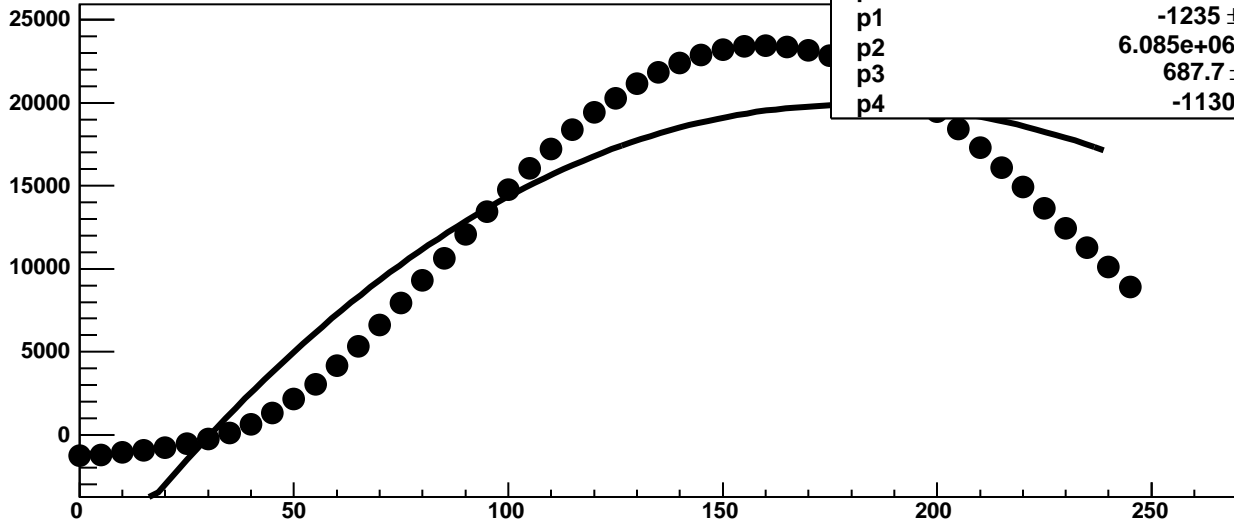
Chip 0, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold



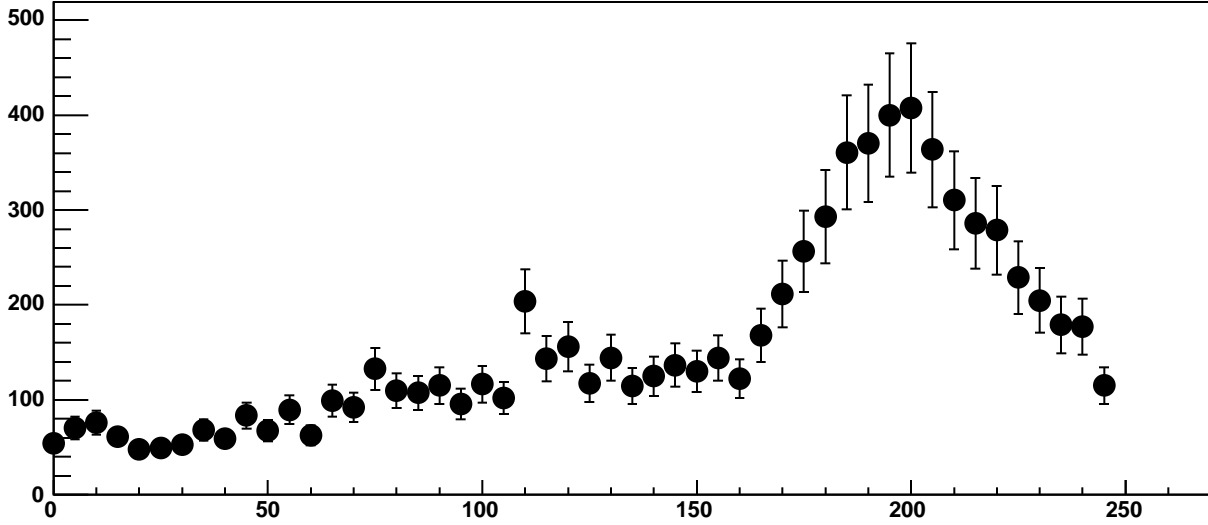
Chip 0, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



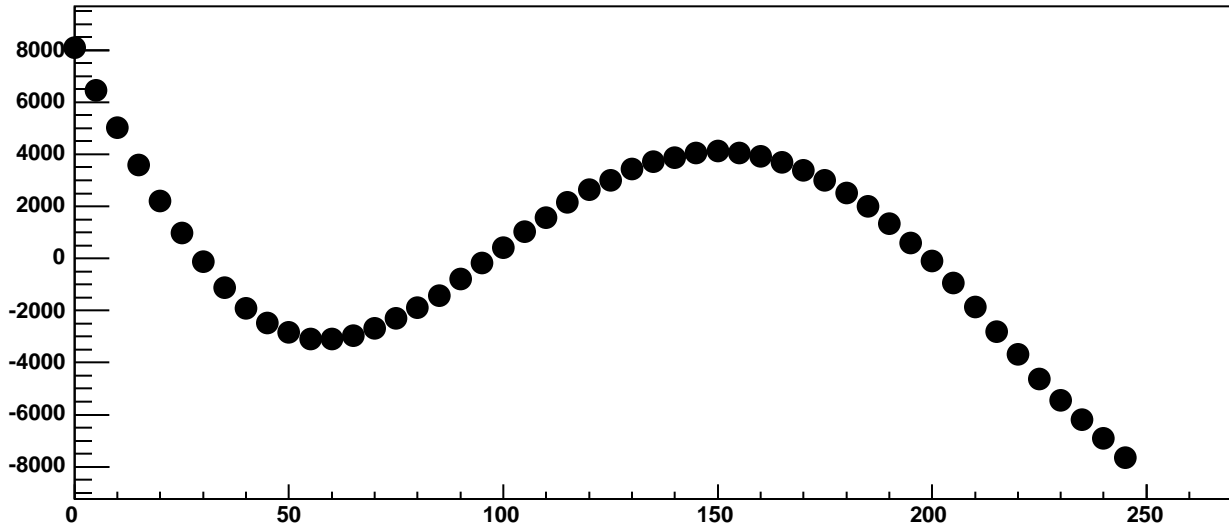
Chip 0, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold



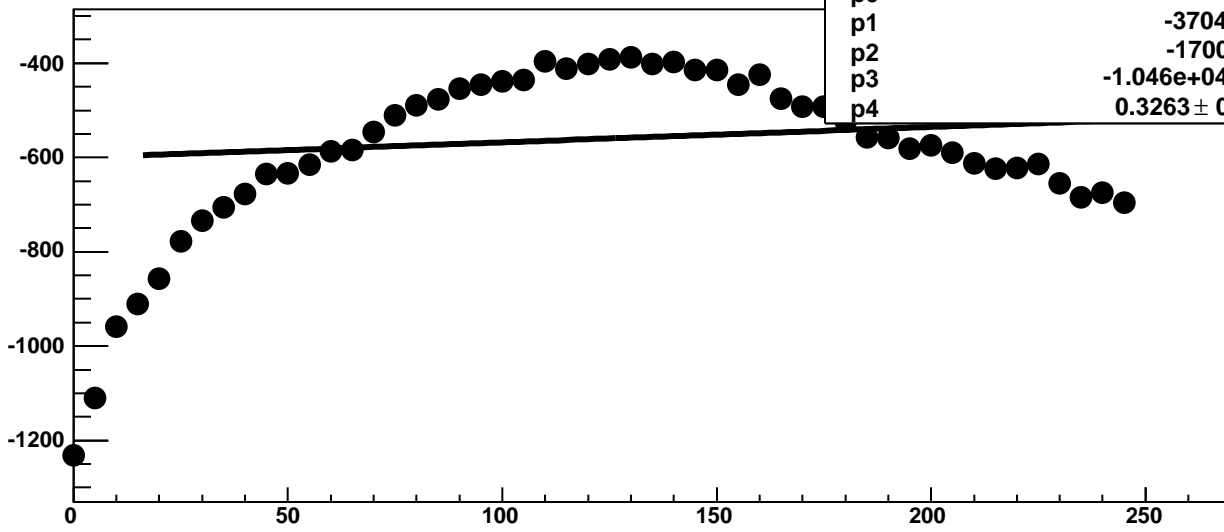
Chip 0, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

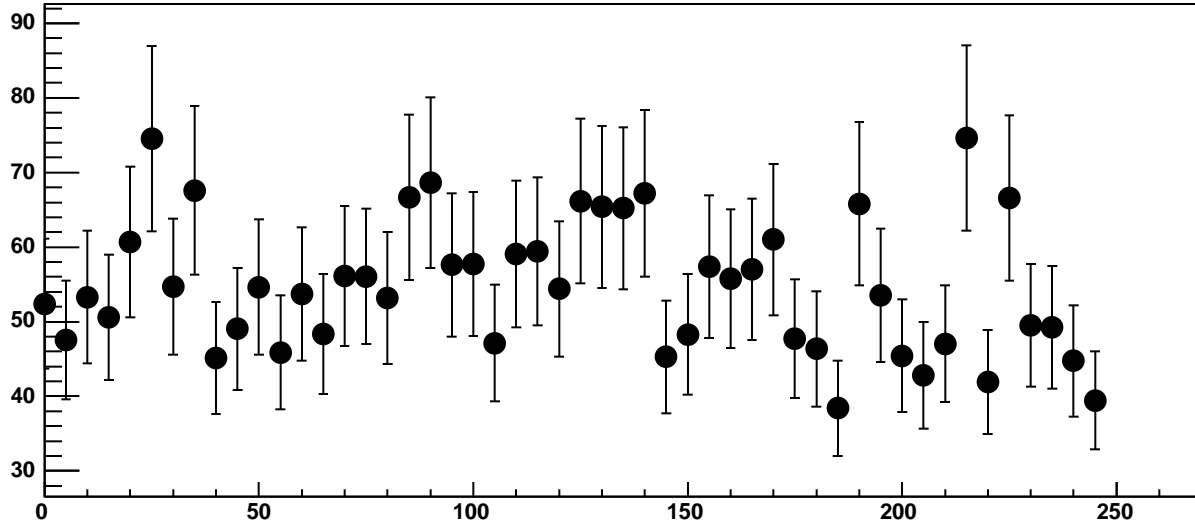


Chip 0, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold

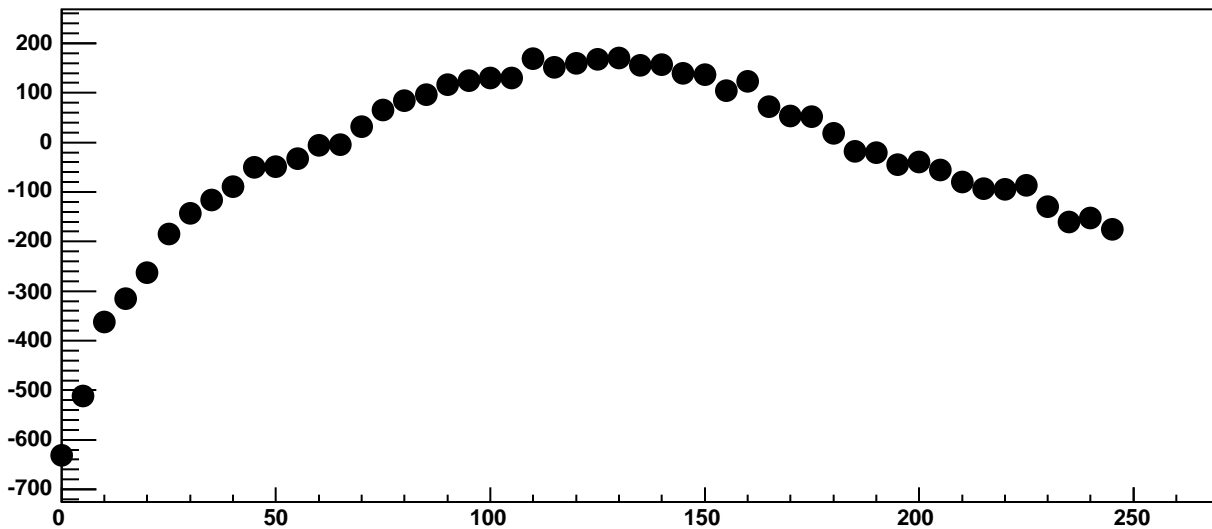


$\chi^2 / \text{ndf}$	4317 / 41
p0	$-108.7 \pm 12.11$
p1	$-3704 \pm 6.402$
p2	$-1700 \pm 8.354$
p3	$-1.046e+04 \pm 413.5$
p4	$0.3263 \pm 0.003152$

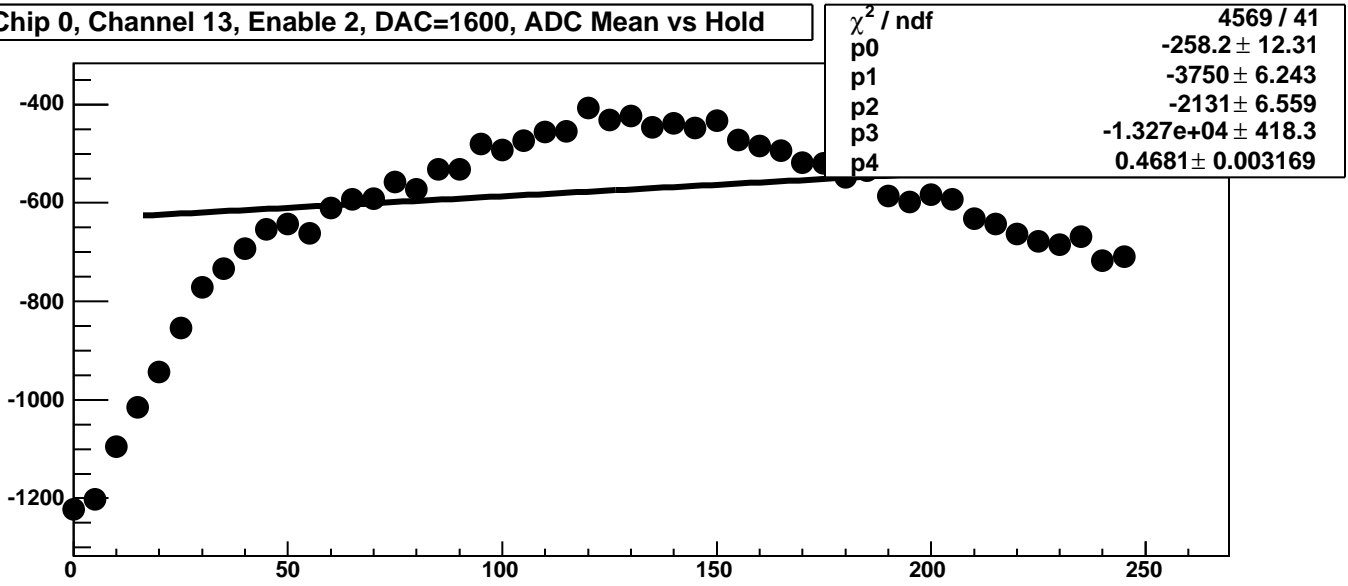
Chip 0, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



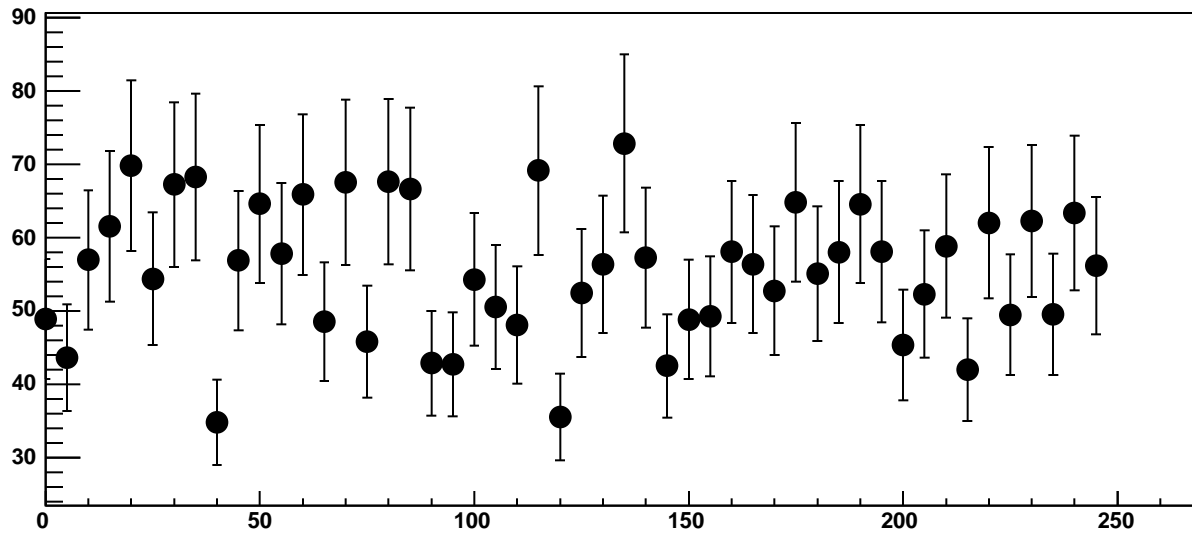
Chip 0, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold



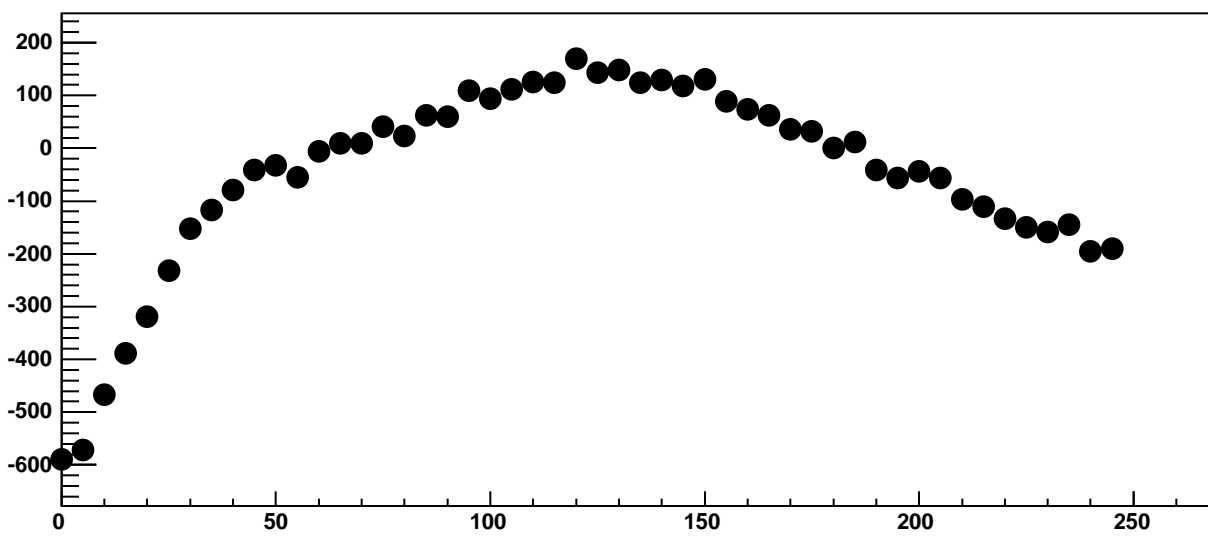
Chip 0, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold



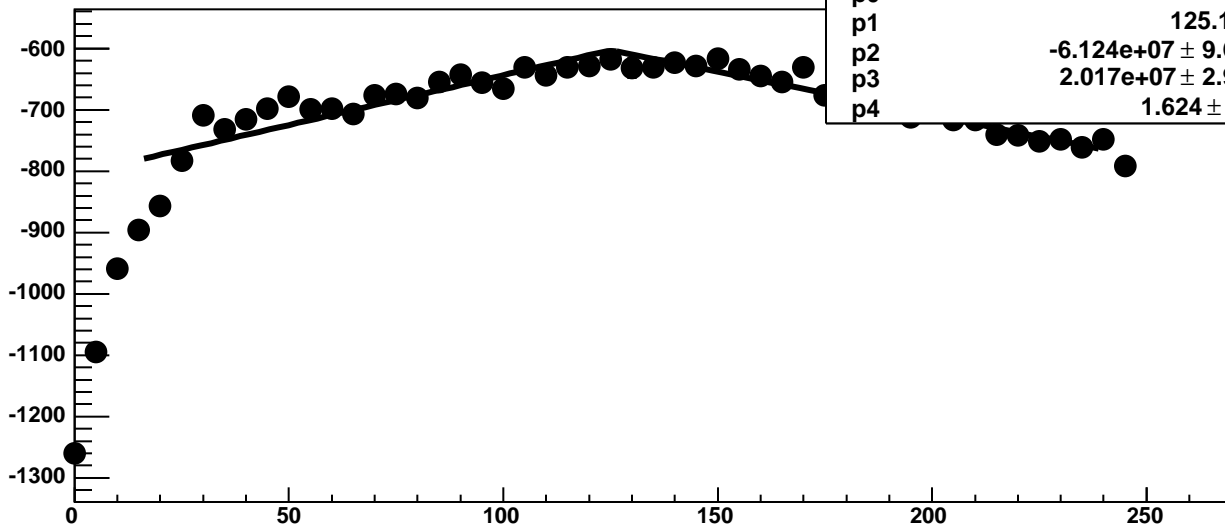
Chip 0, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

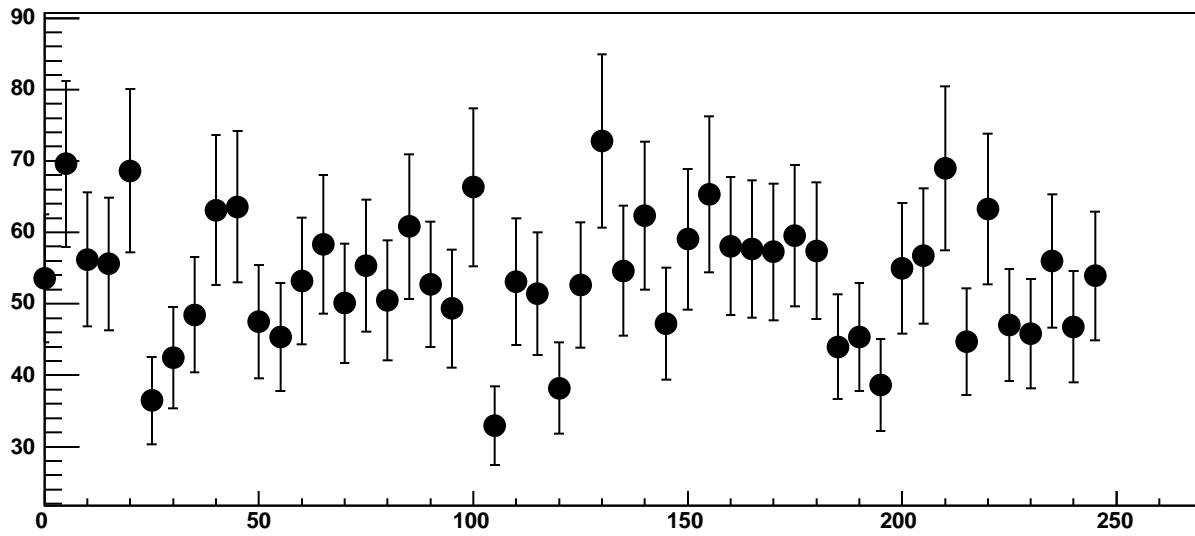


Chip 0, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

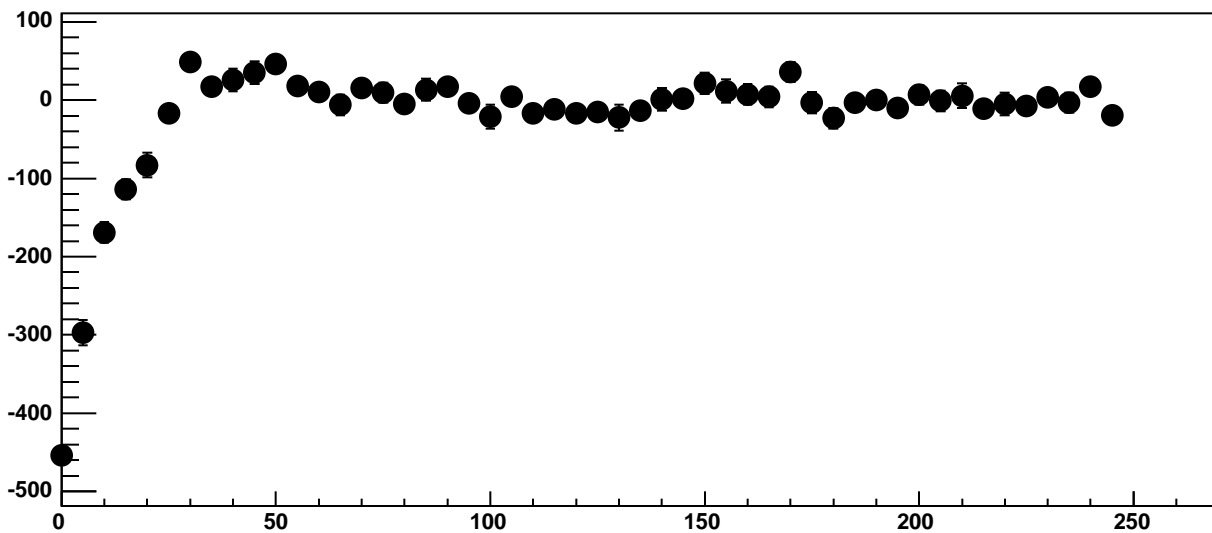


$\chi^2 / \text{ndf}$	209.5 / 41
p0	$-602.7 \pm 3.636$
p1	$125.1 \pm 2.347$
p2	$-6.124\text{e}+07 \pm 9.697\text{e}+06$
p3	$2.017\text{e}+07 \pm 2.997\text{e}+06$
p4	$1.624 \pm 0.06903$

Chip 0, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

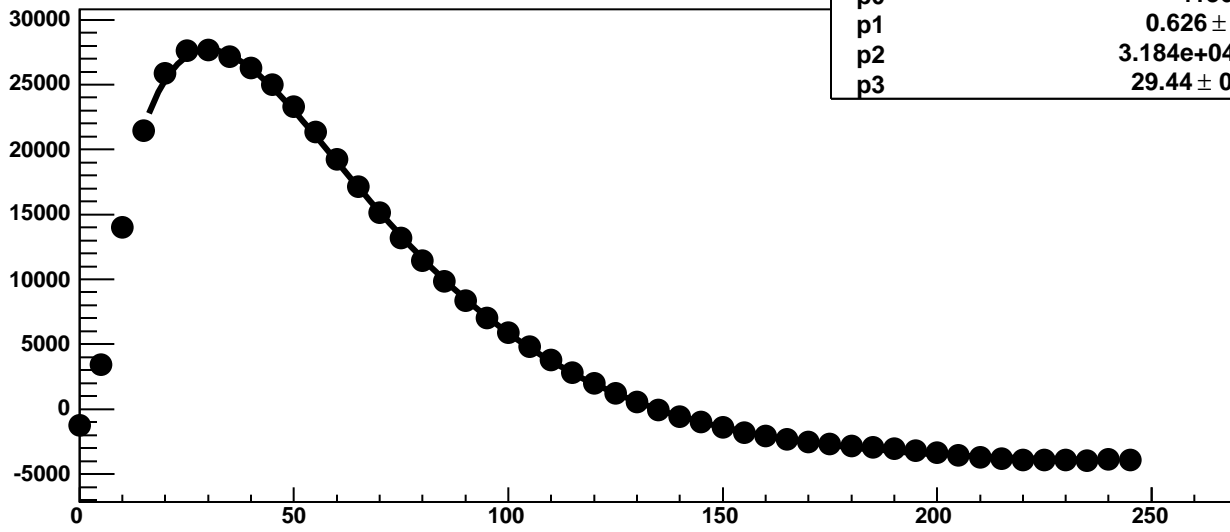


Chip 0, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

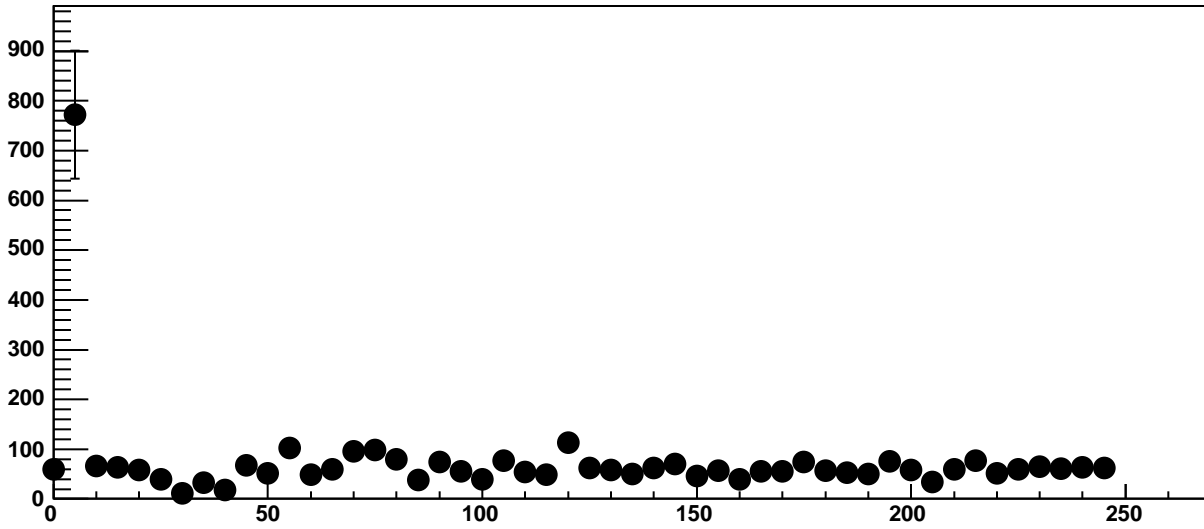




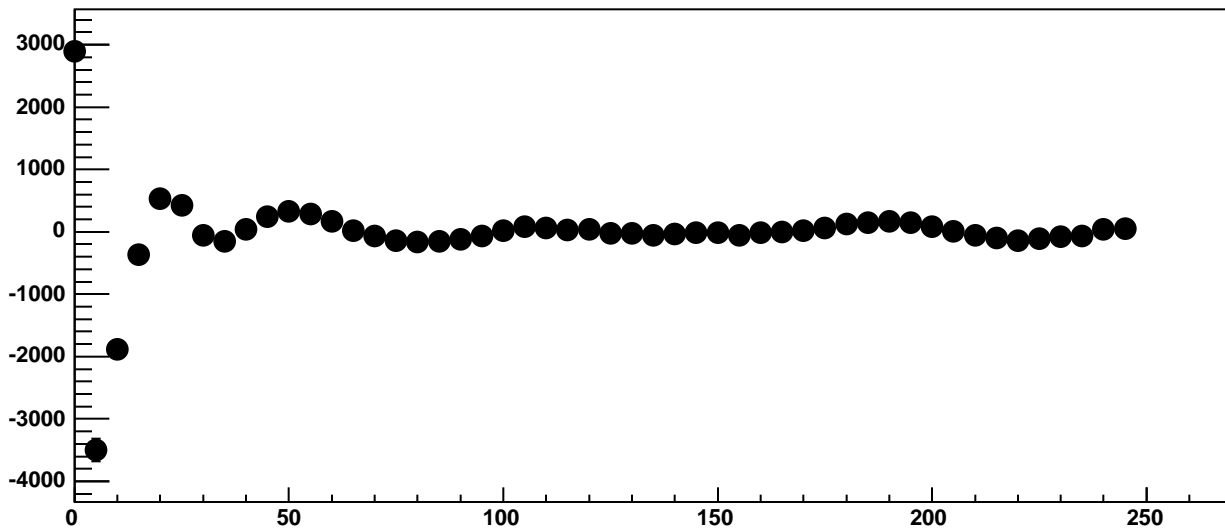
Chip 0, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold



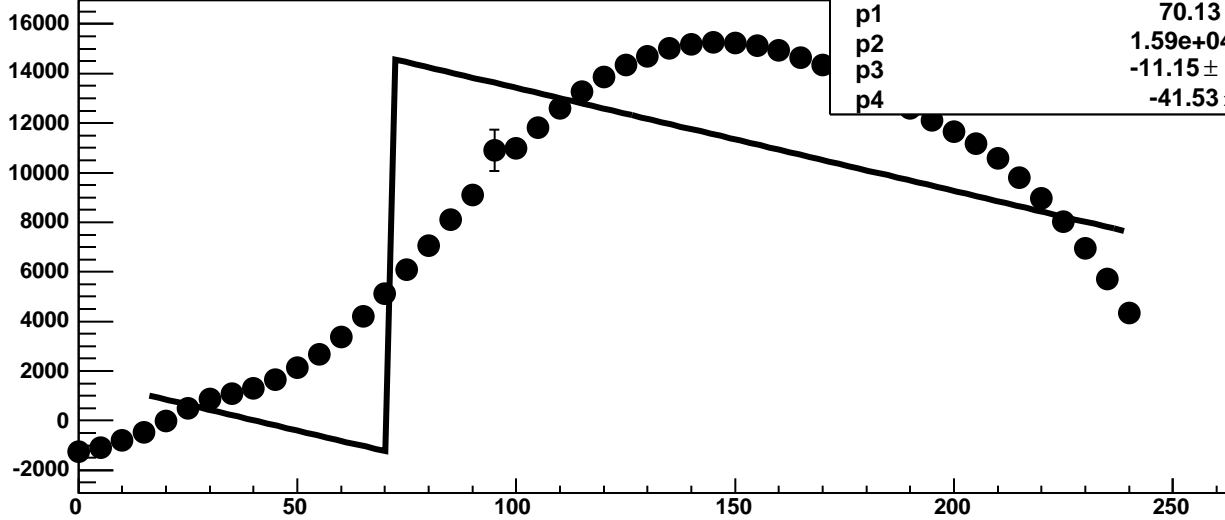
Chip 0, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



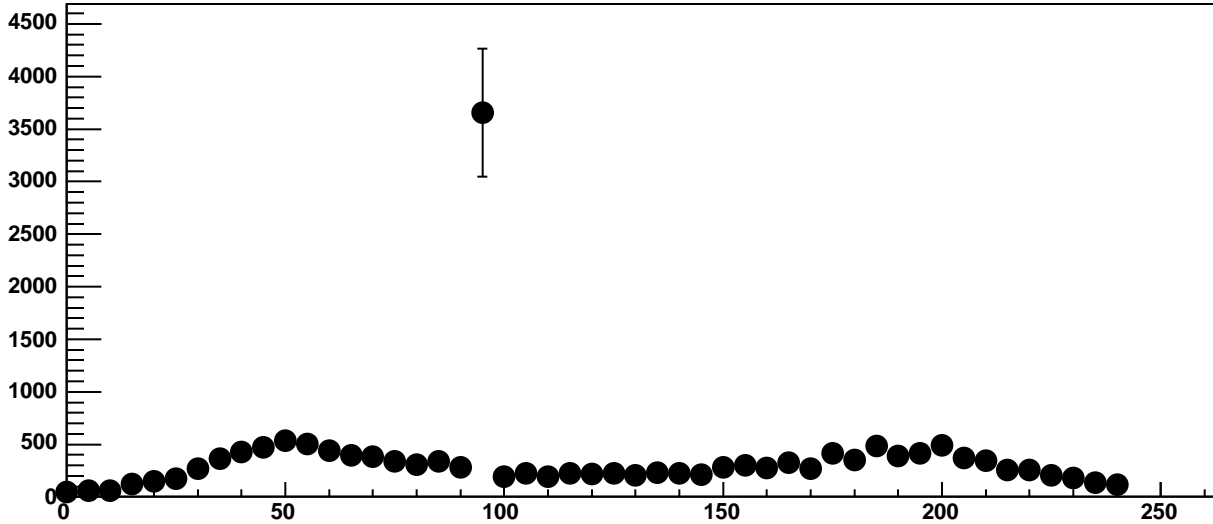
Chip 0, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold



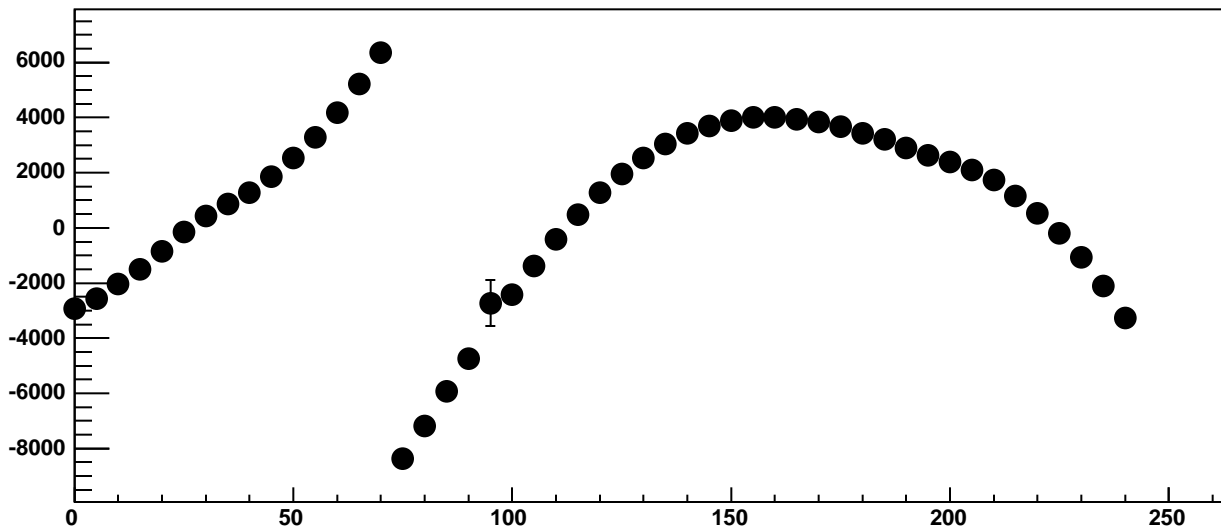
Chip 0, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold



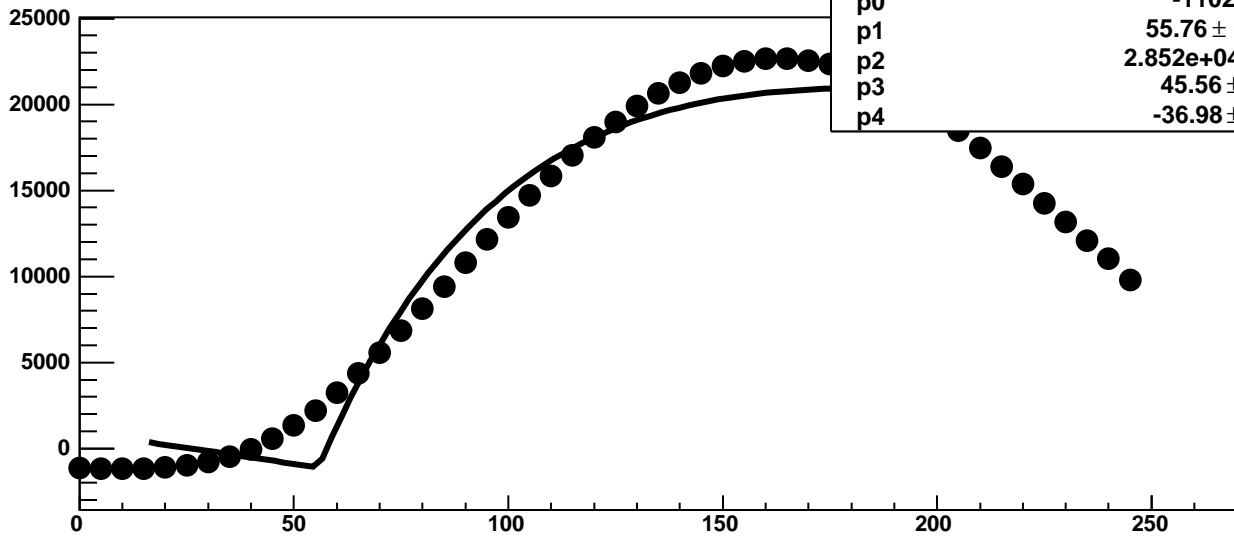
Chip 0, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

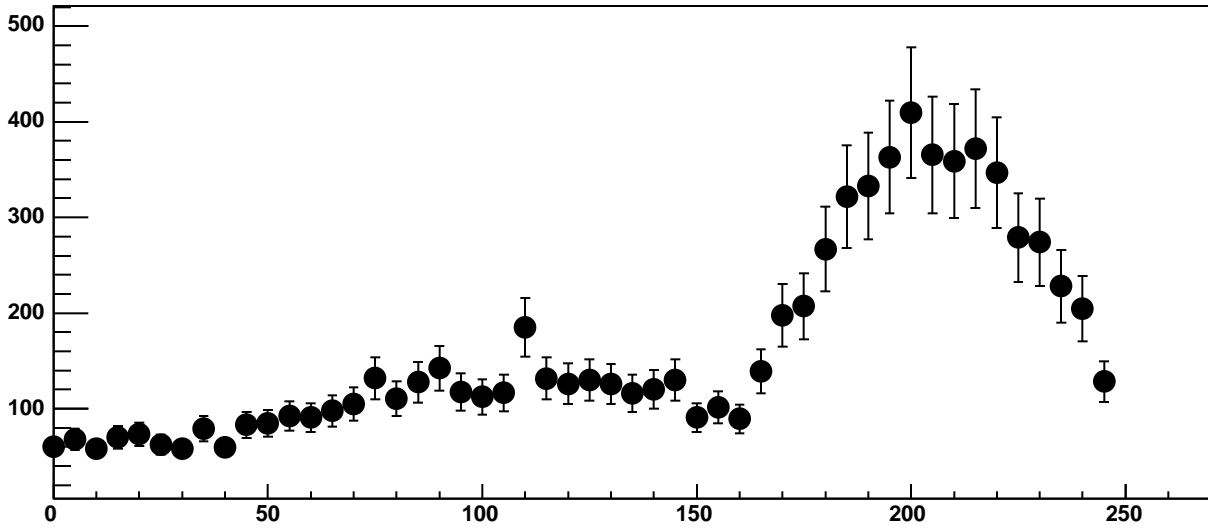


Chip 0, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

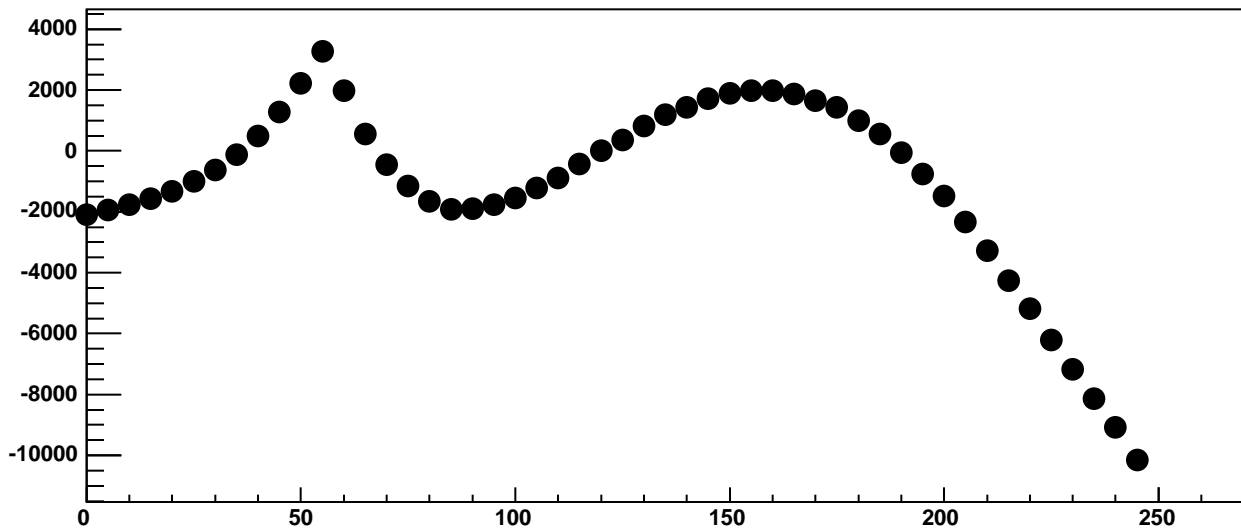


$\chi^2 / \text{ndf}$	2.333e+05 / 41
p0	-1102 ± 8.502
p1	55.76 ± 0.03153
p2	2.852e+04 ± 57.6
p3	45.56 ± 0.1022
p4	-36.98 ± 0.3142

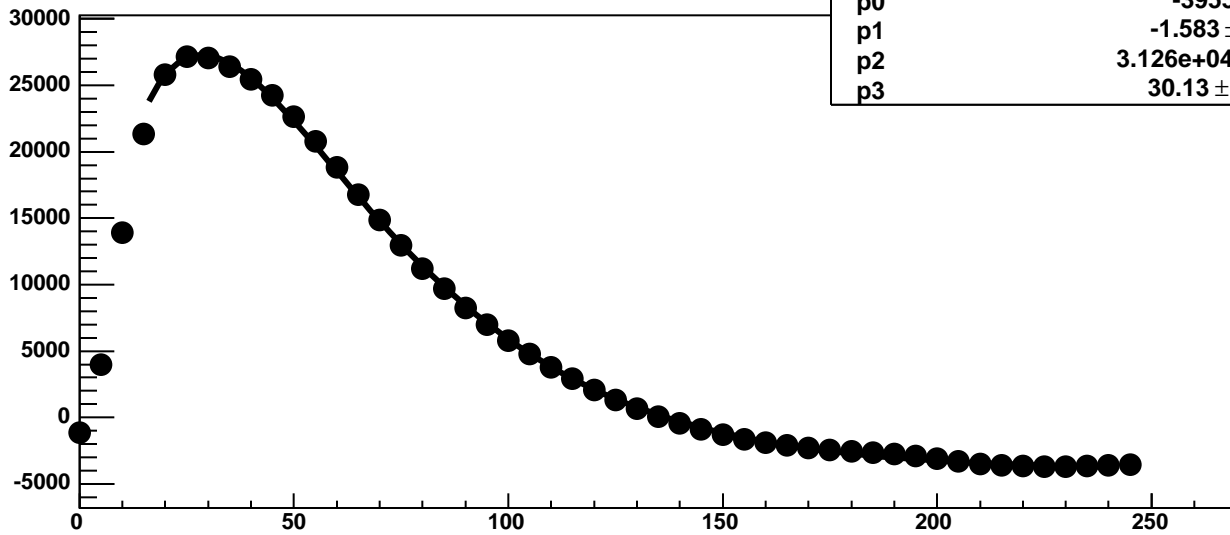
Chip 0, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

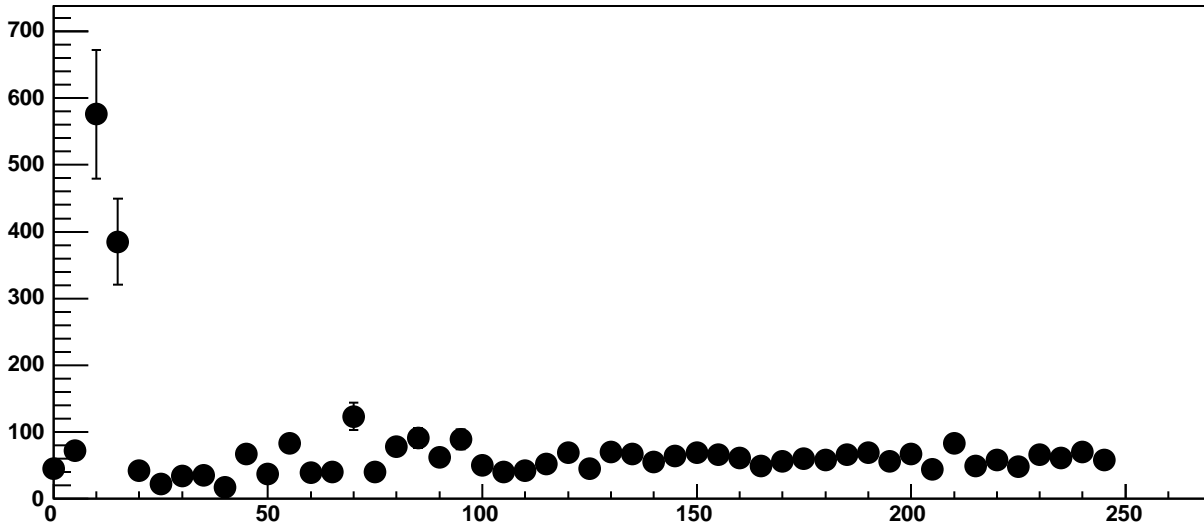


Chip 0, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold

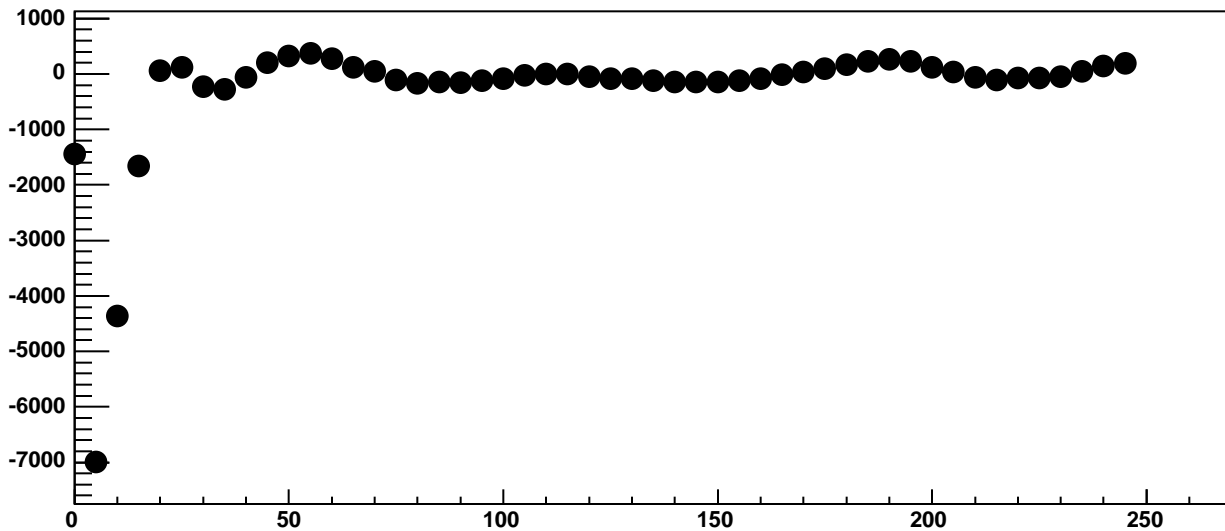


$\chi^2 / \text{ndf}$	8657 / 42
p0	$-3955 \pm 3.951$
p1	$-1.583 \pm 0.0206$
p2	$3.126\text{e}+04 \pm 4.572$
p3	$30.13 \pm 0.01157$

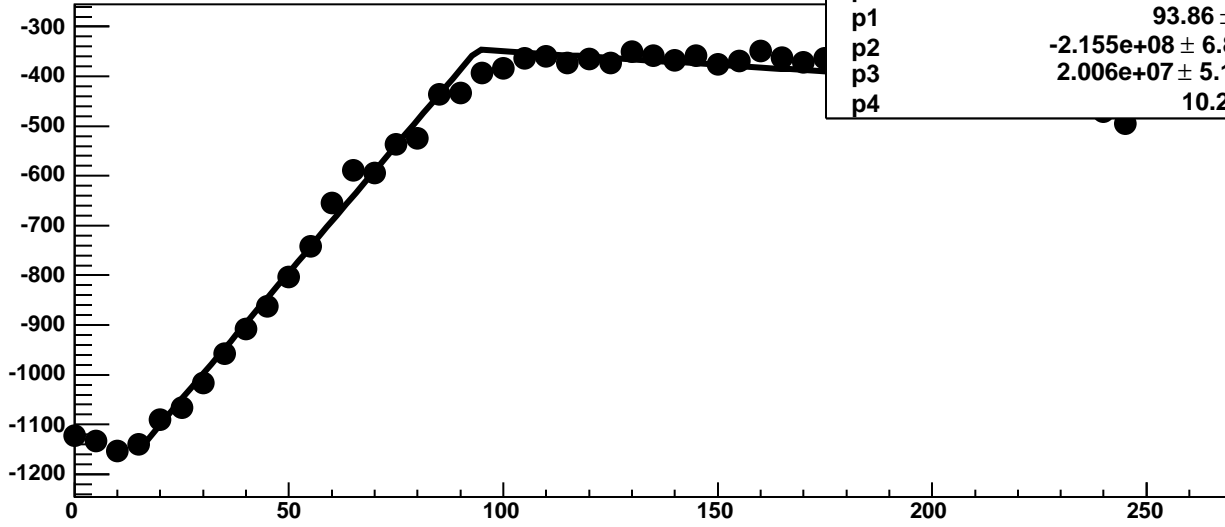
Chip 0, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

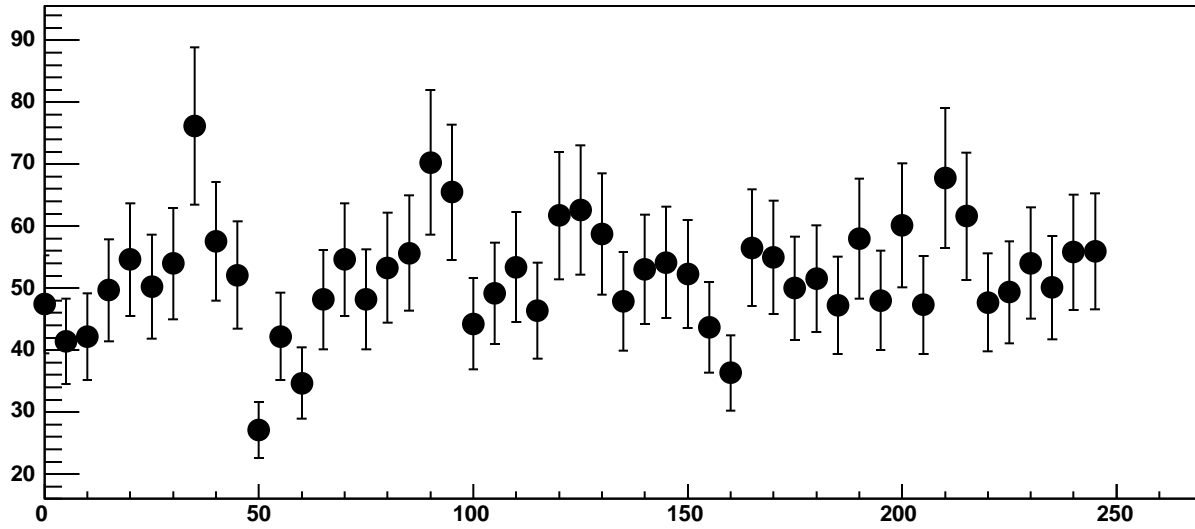


Chip 0, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

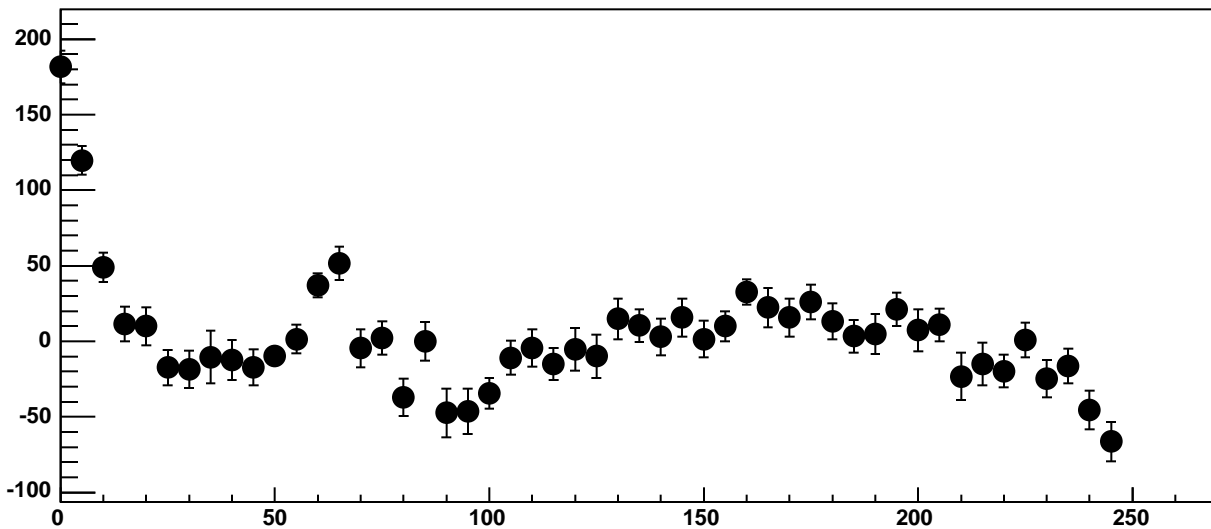


$\chi^2 / \text{ndf}$	159.4 / 41
p0	$-346.3 \pm 4.179$
p1	$93.86 \pm 0.7315$
p2	$-2.155\text{e}+08 \pm 6.868\text{e}+06$
p3	$2.006\text{e}+07 \pm 5.191\text{e}+05$
p4	$10.2 \pm 0.142$

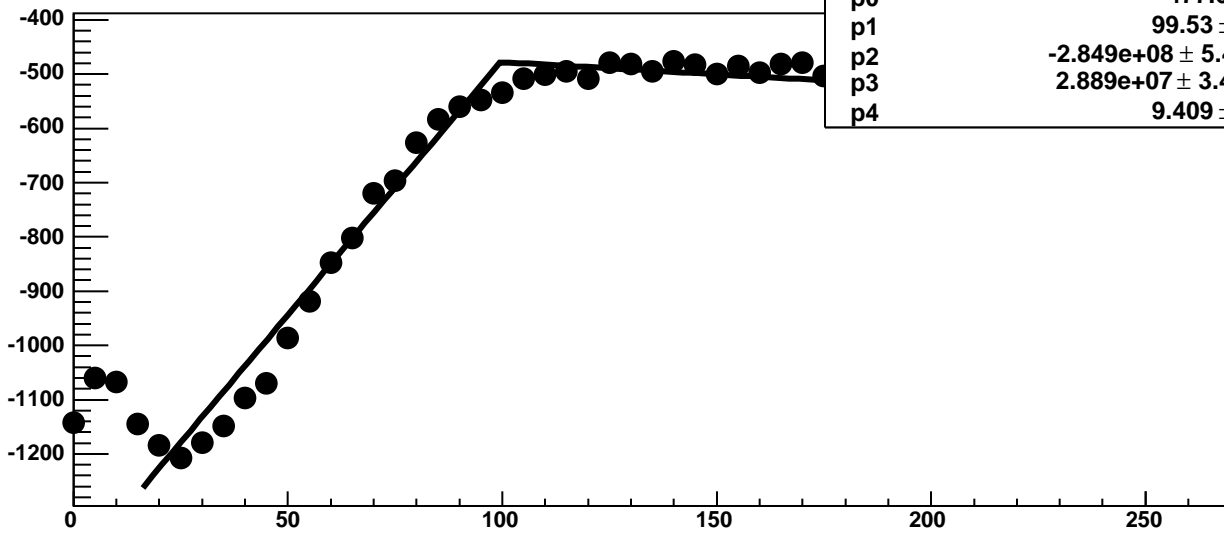
Chip 0, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



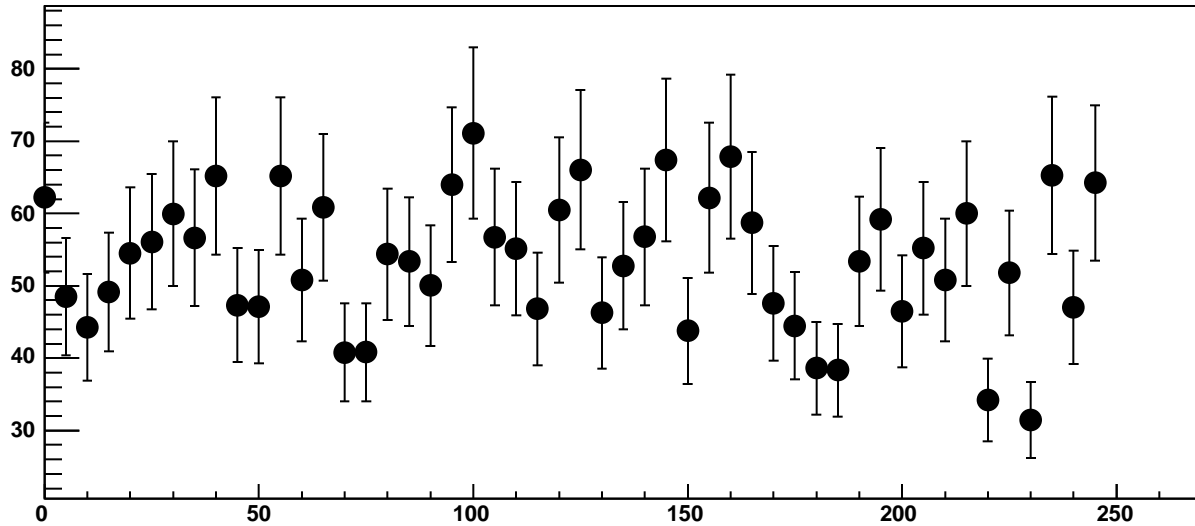
Chip 0, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold



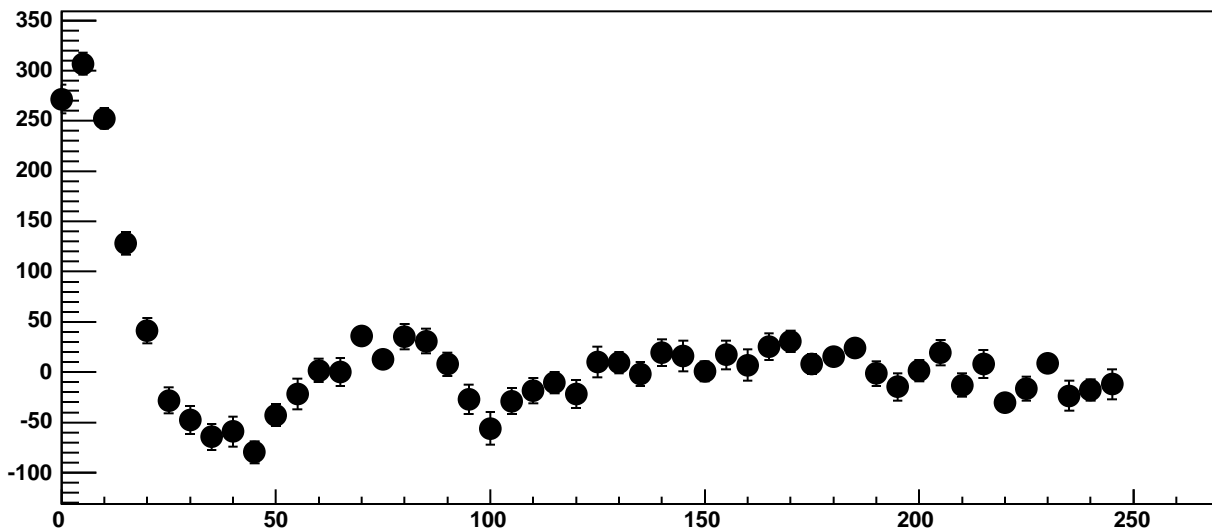
Chip 0, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold



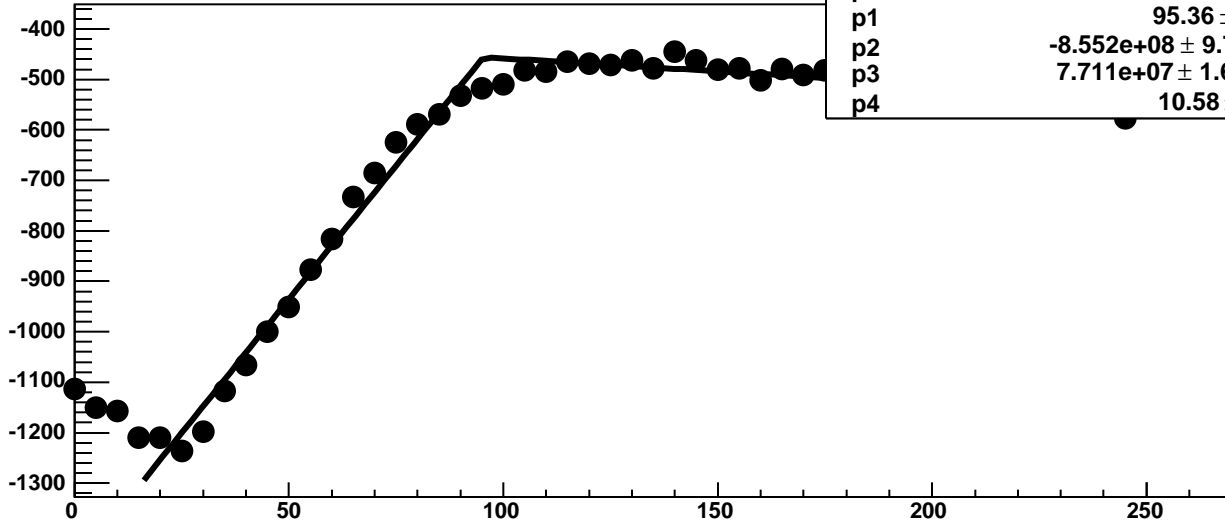
Chip 0, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

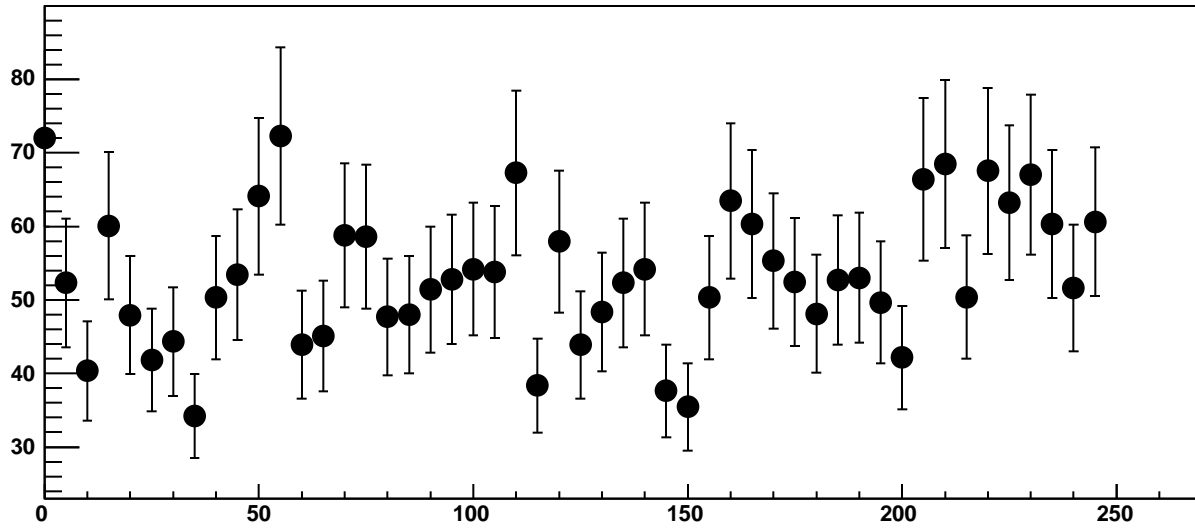


Chip 0, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold

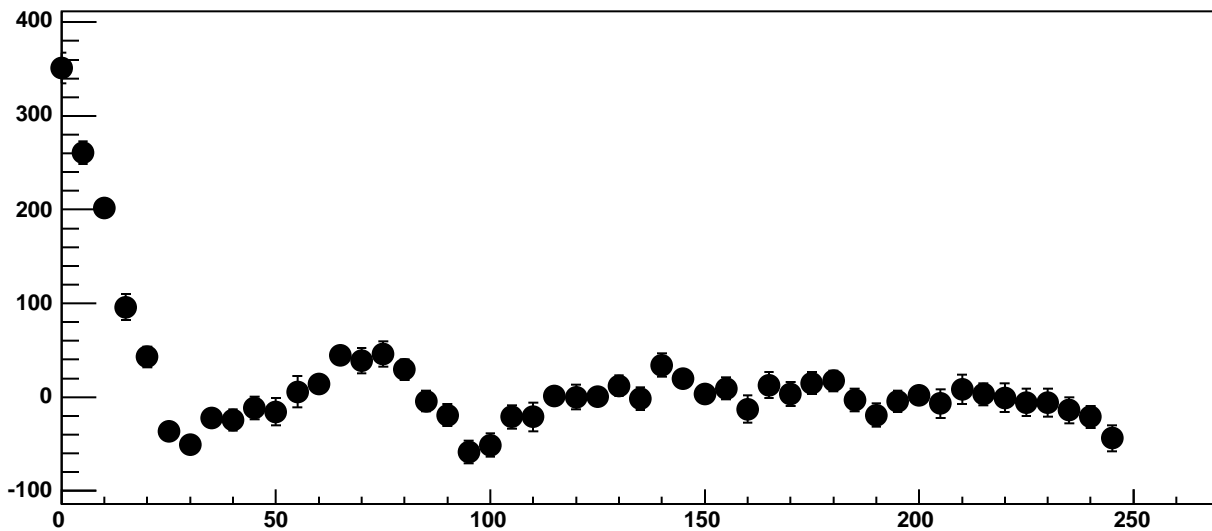


$\chi^2 / \text{ndf}$	240.7 / 41
p0	-455.9 $\pm$ 4.198
p1	95.36 $\pm$ 0.6325
p2	-8.552e+08 $\pm$ 9.744e+06
p3	7.711e+07 $\pm$ 1.623e+05
p4	10.58 $\pm$ 0.1119

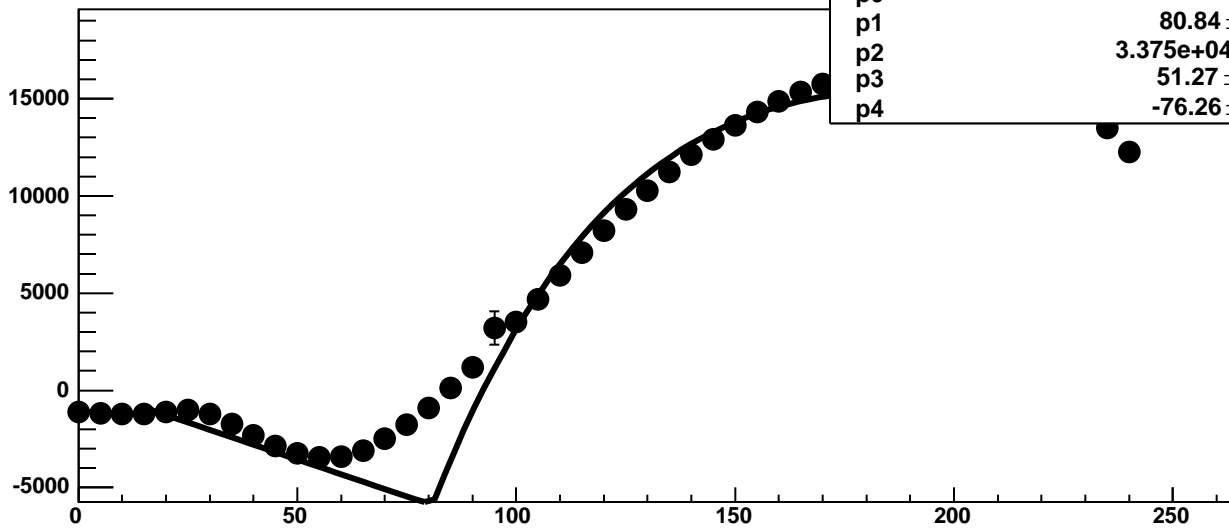
Chip 0, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

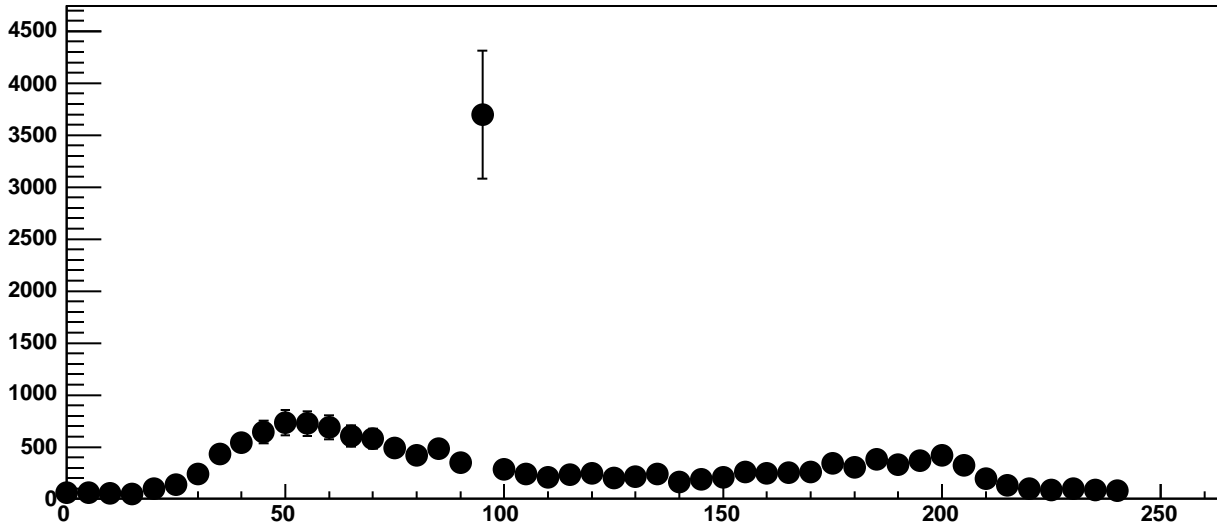


Chip 0, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

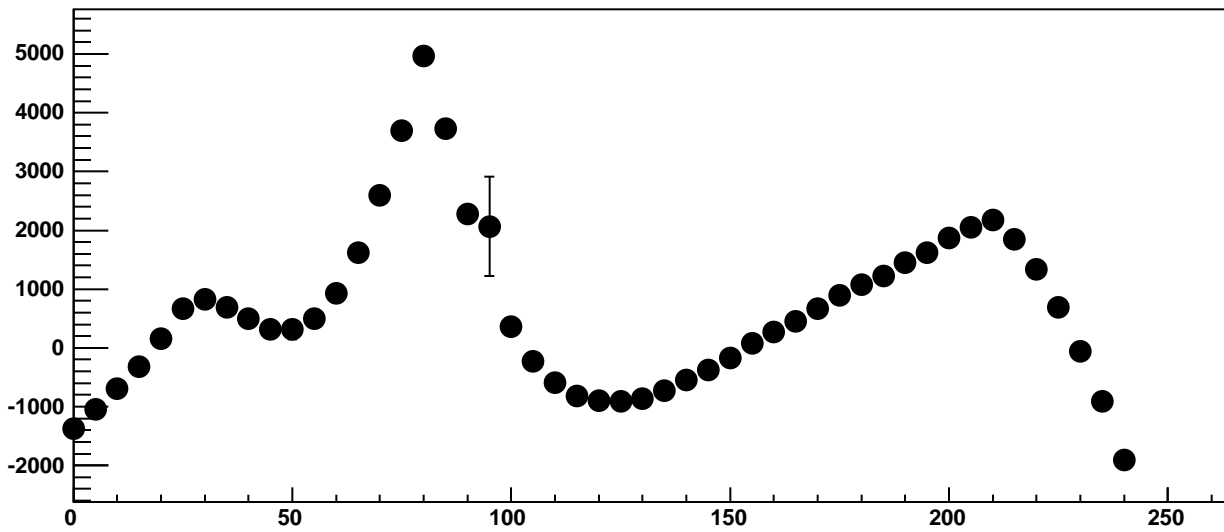


$\chi^2 / \text{ndf}$	3.585e+04 / 41
p0	-5918 ± 36.65
p1	80.84 ± 0.1145
p2	3.375e+04 ± 164.2
p3	51.27 ± 0.2435
p4	-76.26 ± 0.6553

Chip 0, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

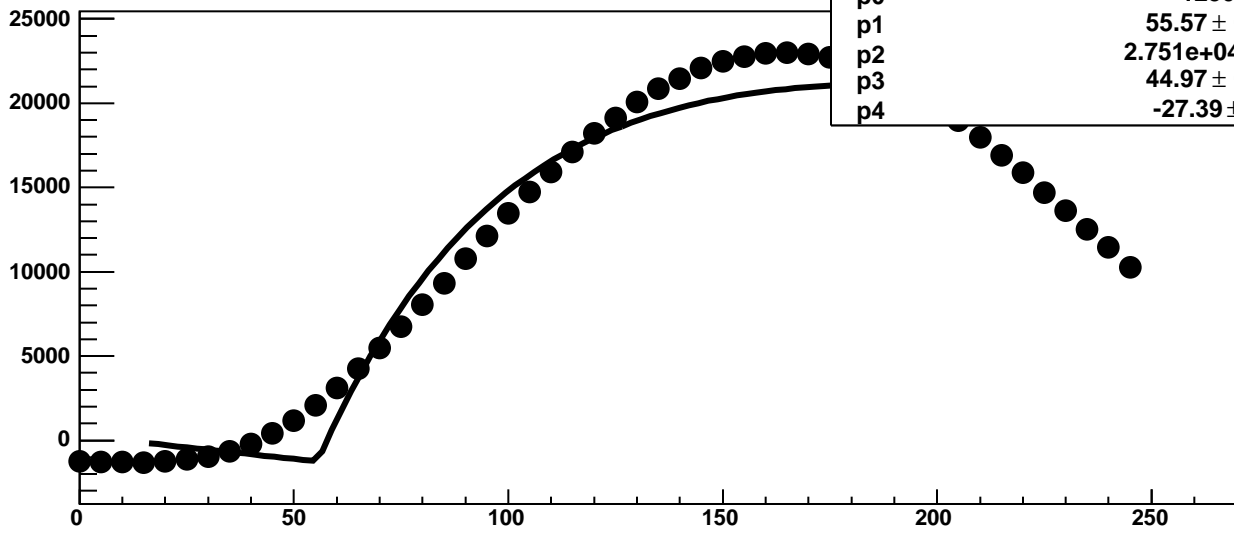


Chip 0, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

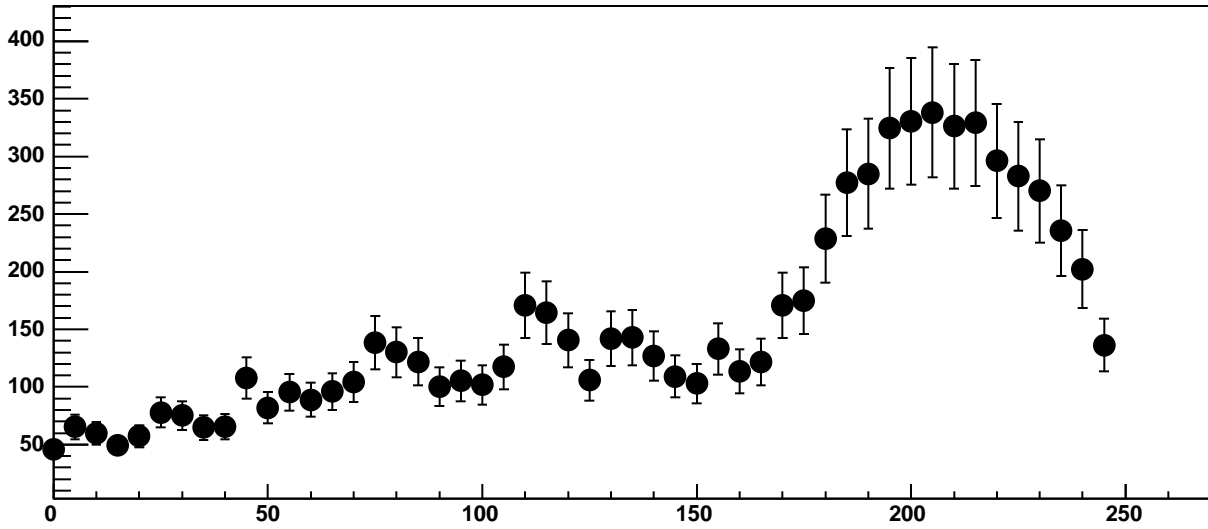




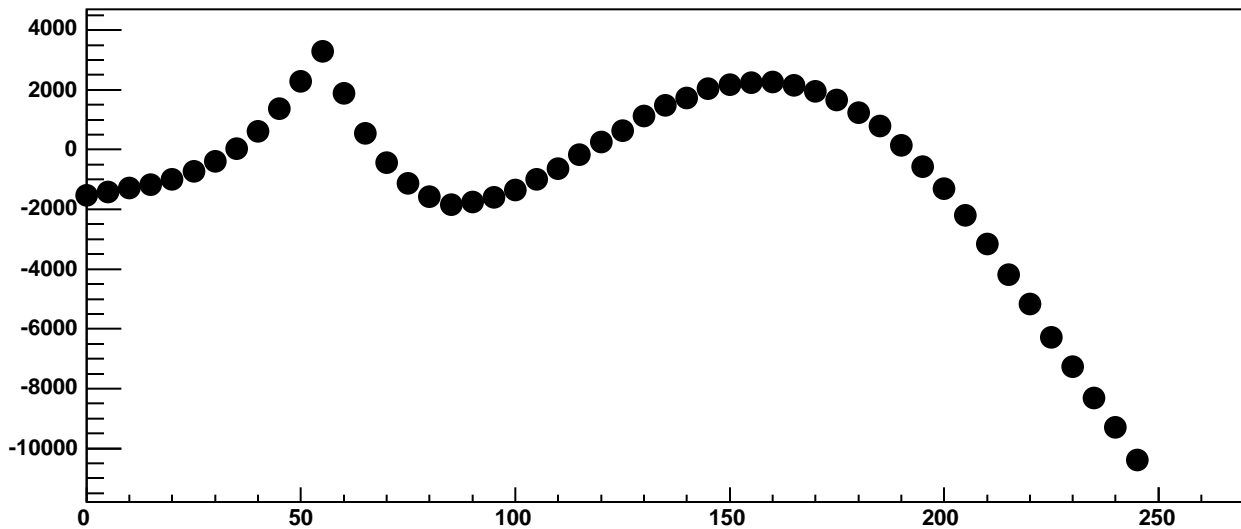
Chip 0, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold



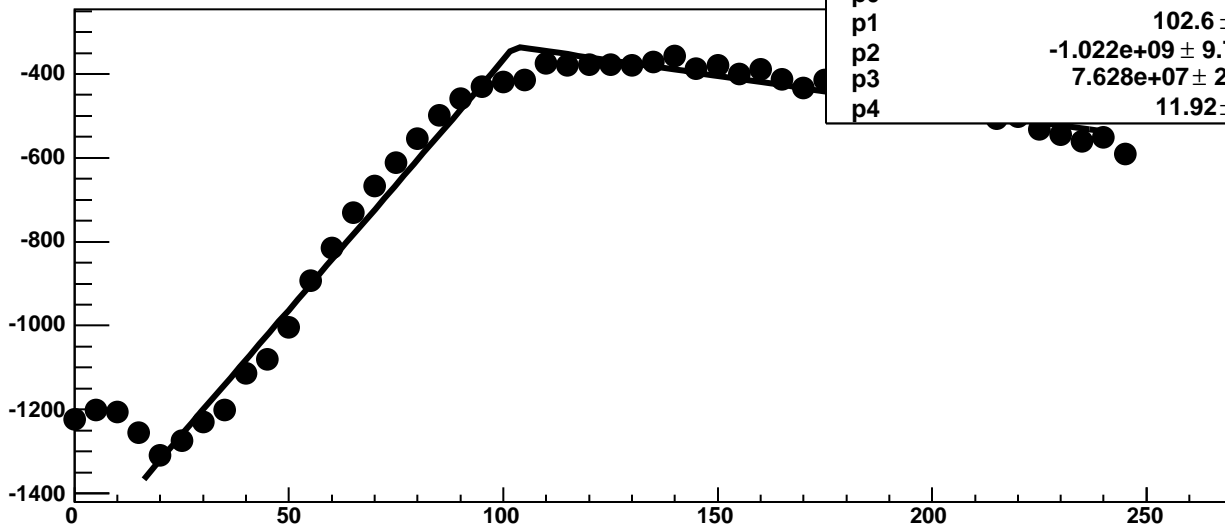
Chip 0, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

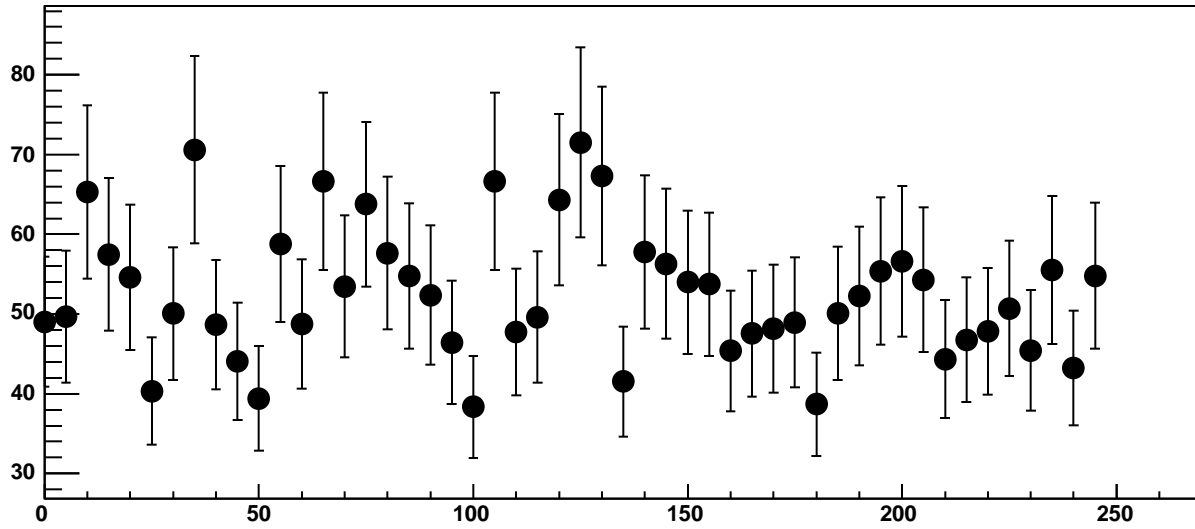


Chip 0, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

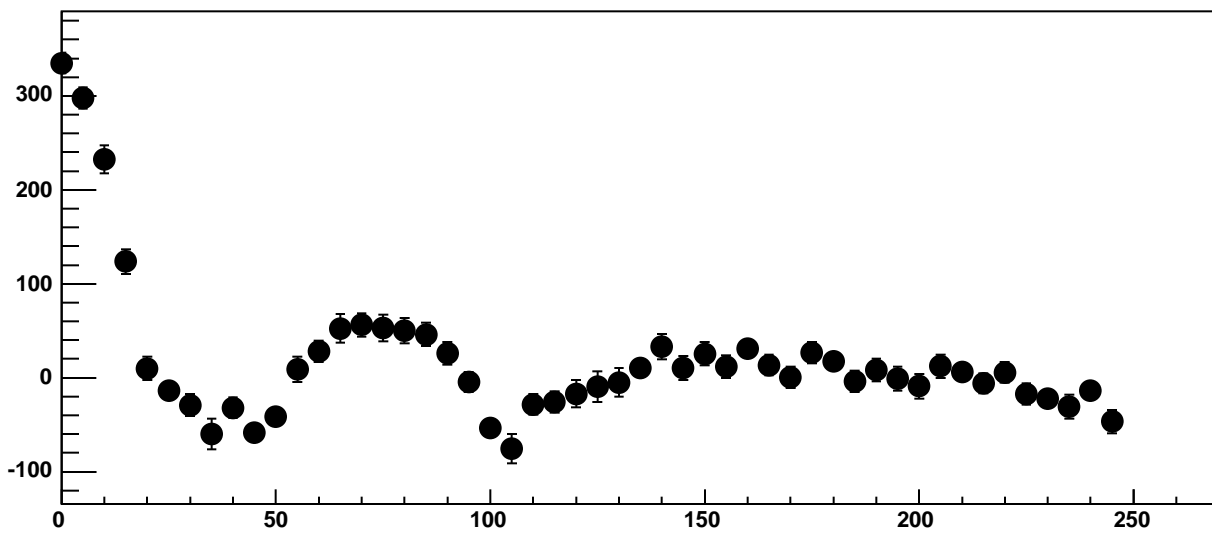


$\chi^2 / \text{ndf}$	385 / 41
p0	$-334.6 \pm 4.203$
p1	$102.6 \pm 0.5245$
p2	$-1.022\text{e}+09 \pm 9.779\text{e}+06$
p3	$7.628\text{e}+07 \pm 2.92\text{e}+05$
p4	$11.92 \pm 0.1014$

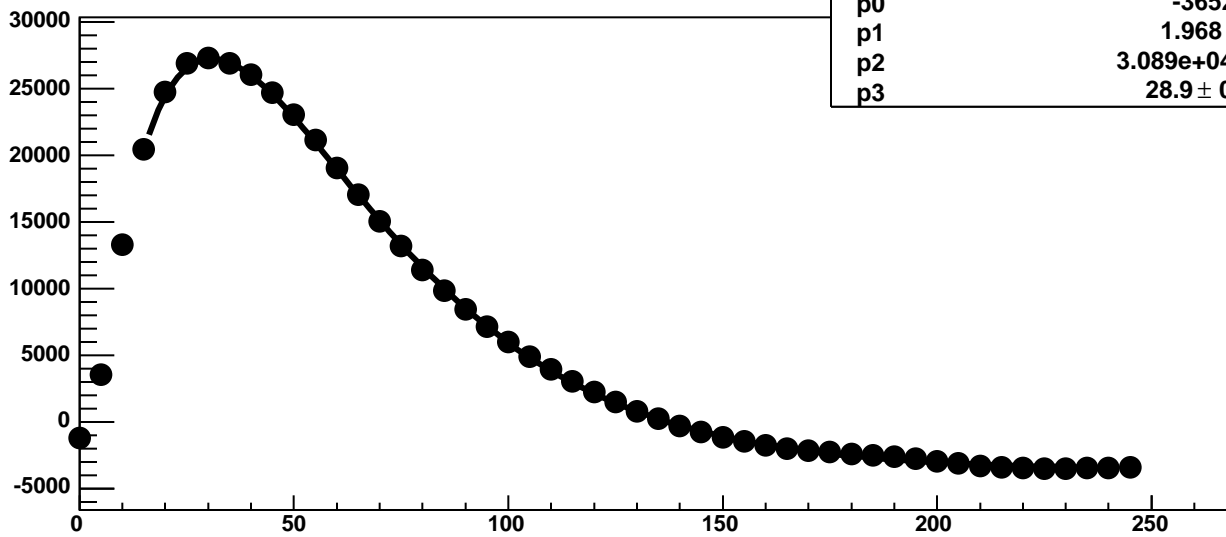
Chip 0, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

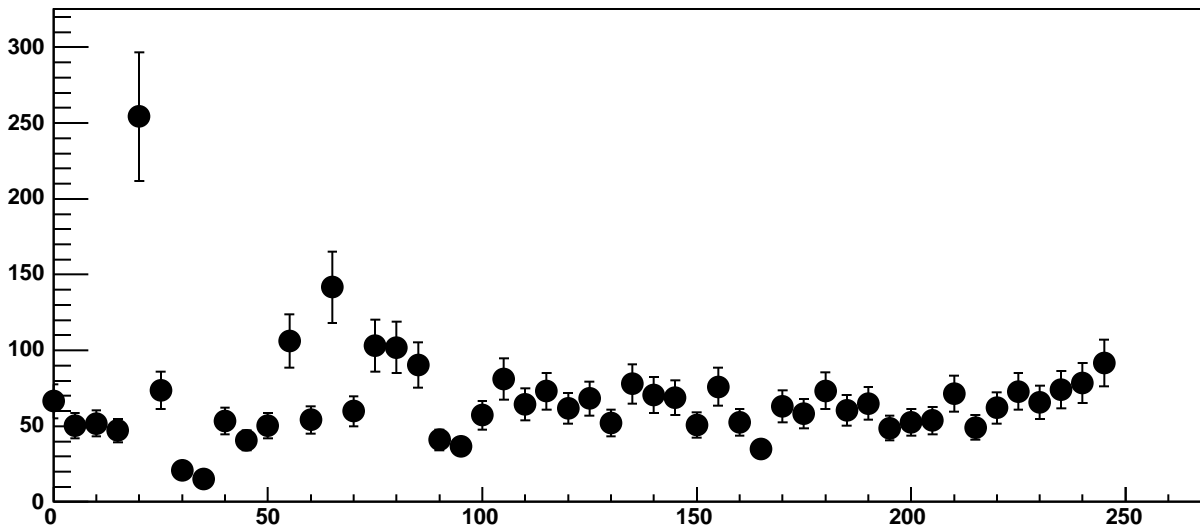


Chip 0, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold

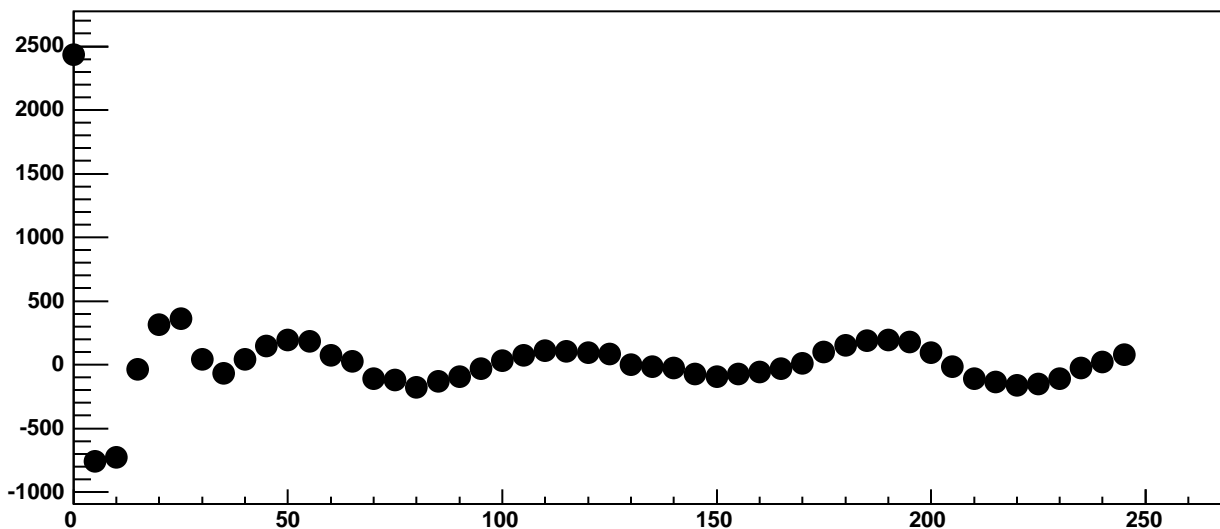


$\chi^2 / \text{ndf}$	3494 / 42
p0	$-3652 \pm 3.798$
p1	$1.968 \pm 0.0128$
p2	$3.089\text{e}+04 \pm 4.283$
p3	$28.9 \pm 0.009195$

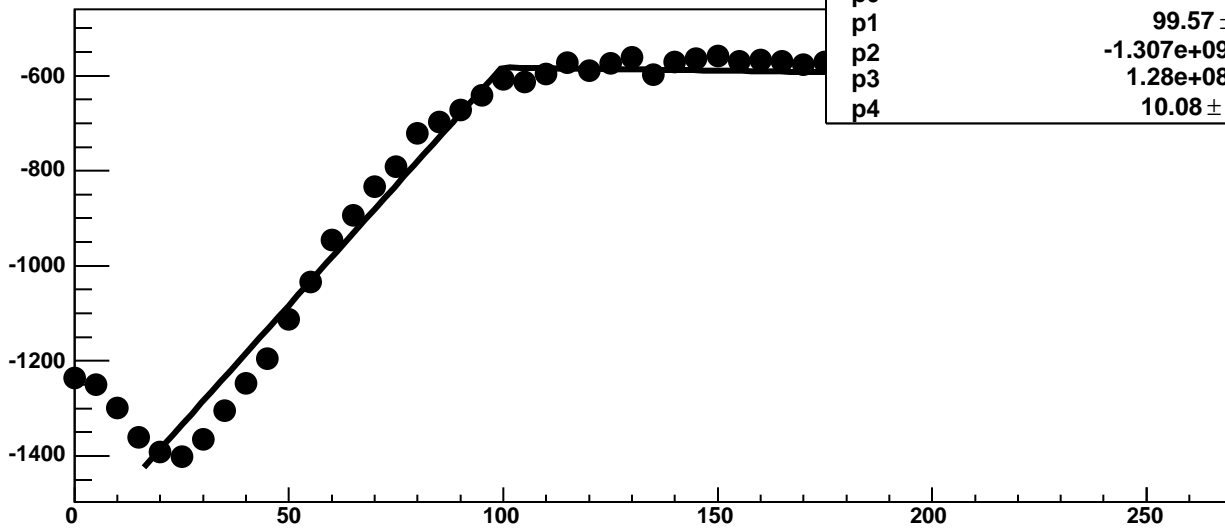
Chip 0, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

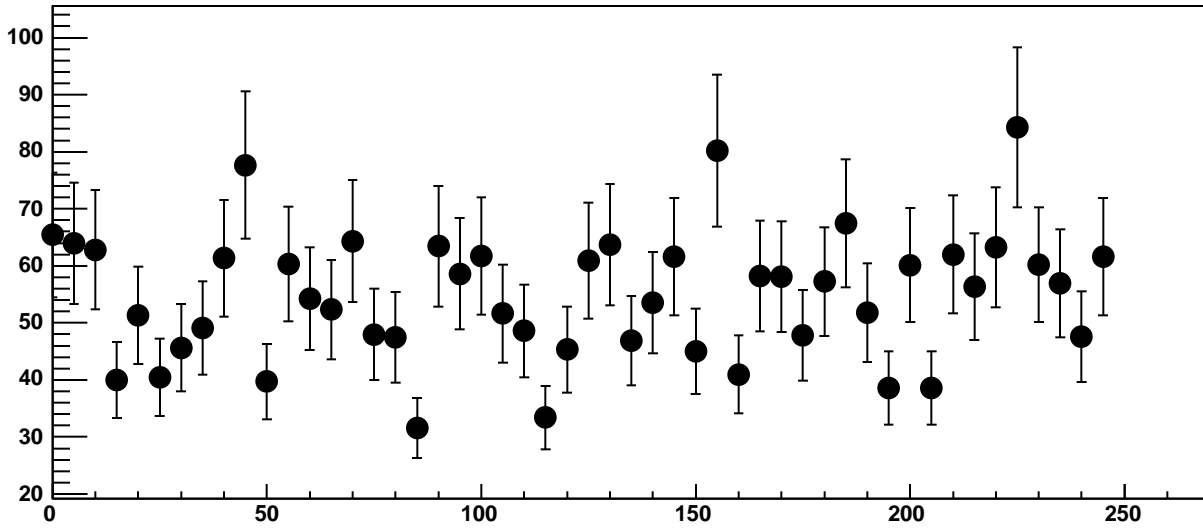


Chip 0, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

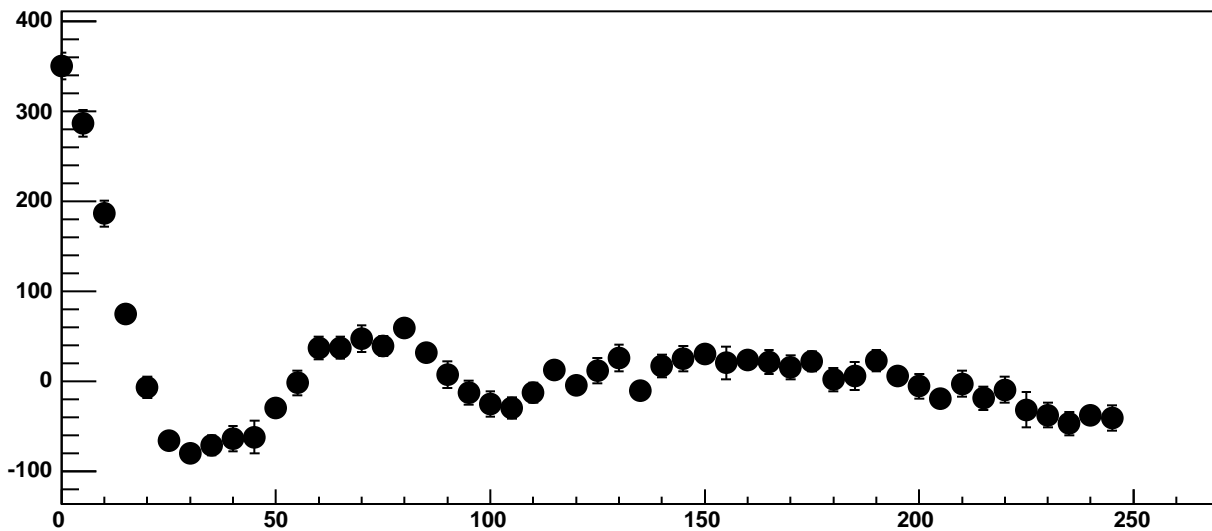


$\chi^2 / \text{ndf}$	445.6 / 41
p0	$-582.8 \pm 3.78$
p1	$99.57 \pm 0.6185$
p2	$-1.307\text{e}+09 \pm 1.414$
p3	$1.28\text{e}+08 \pm 1.414$
p4	$10.08 \pm 0.04716$

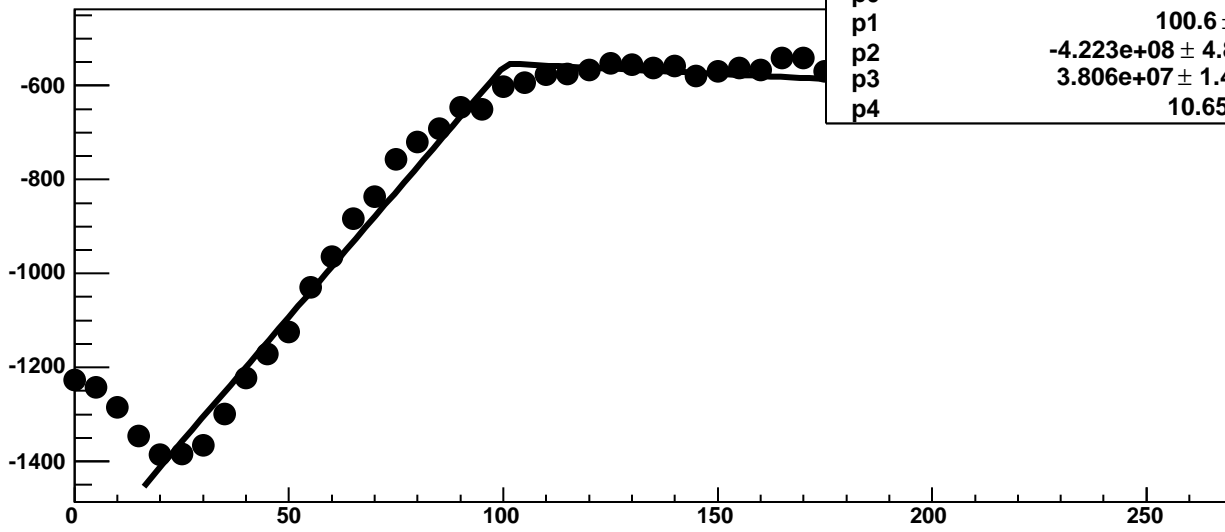
Chip 0, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

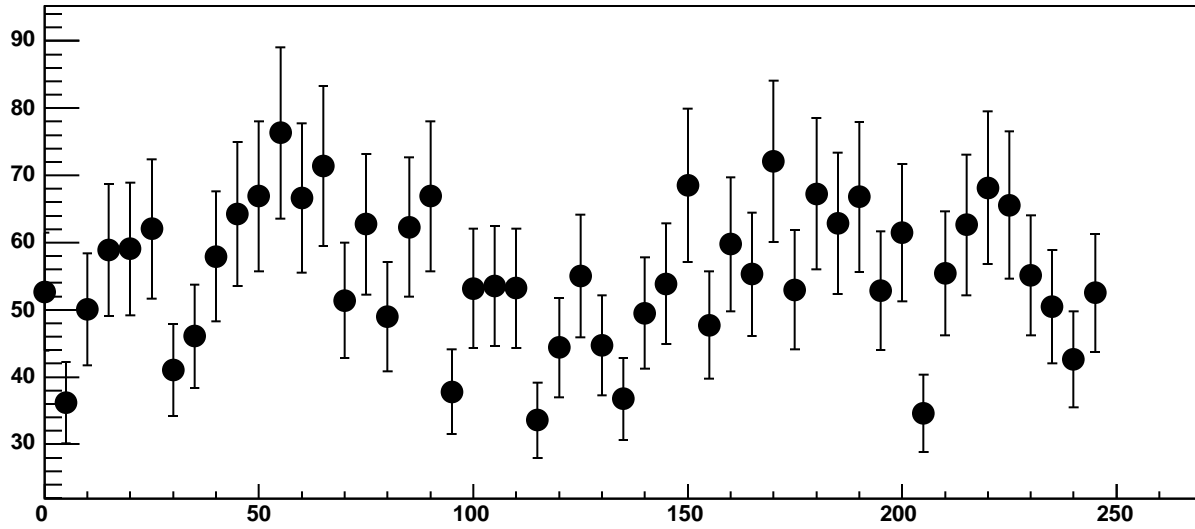


Chip 0, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

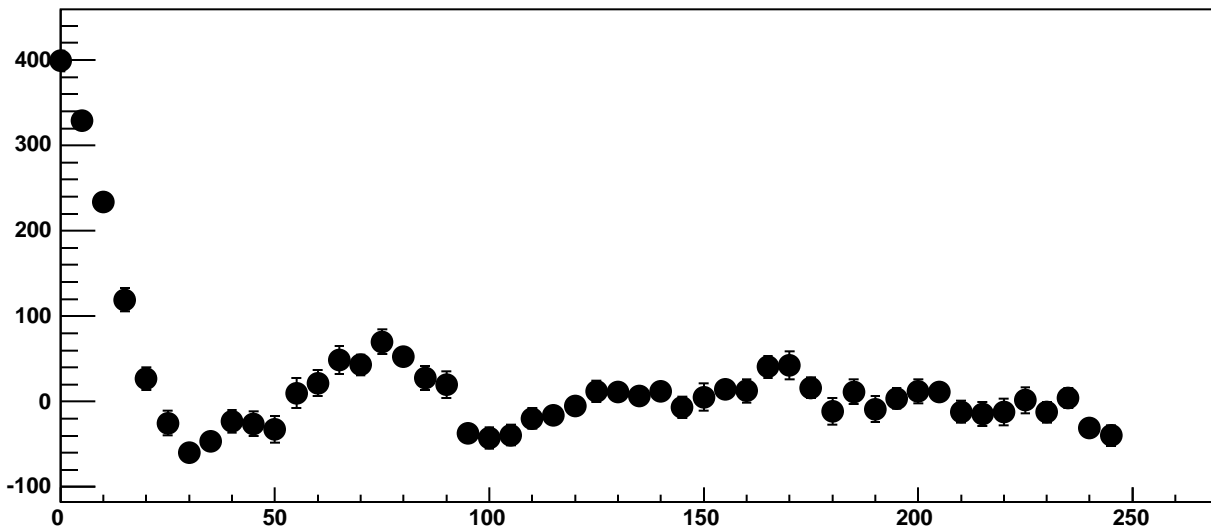


$\chi^2 / \text{ndf}$	322.2 / 41
p0	-553.3 ± 3.985
p1	100.6 ± 0.6179
p2	-4.223e+08 ± 4.878e+06
p3	3.806e+07 ± 1.468e+05
p4	10.65 ± 0.109

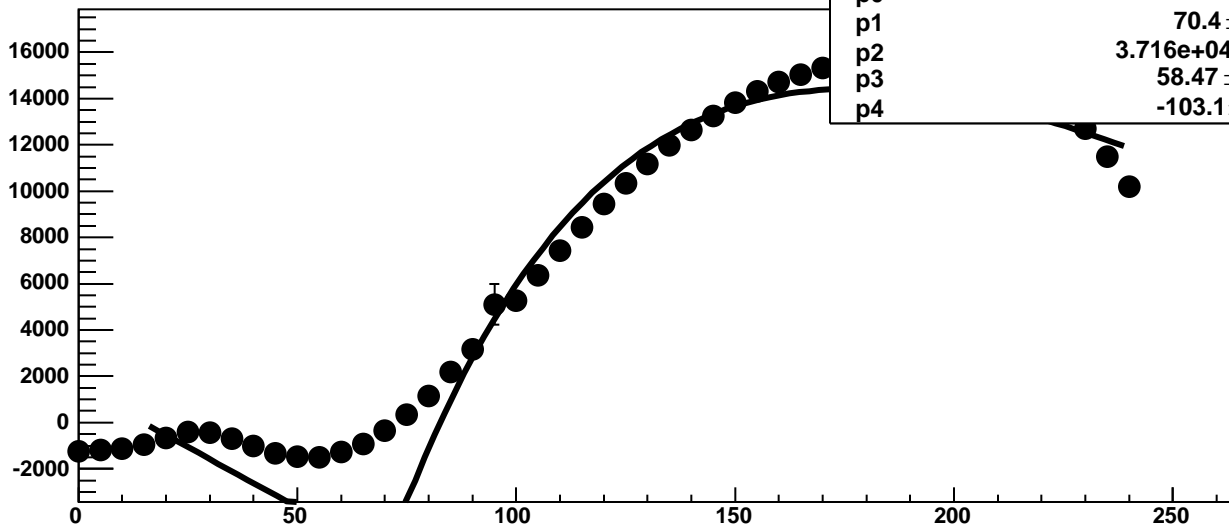
Chip 0, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

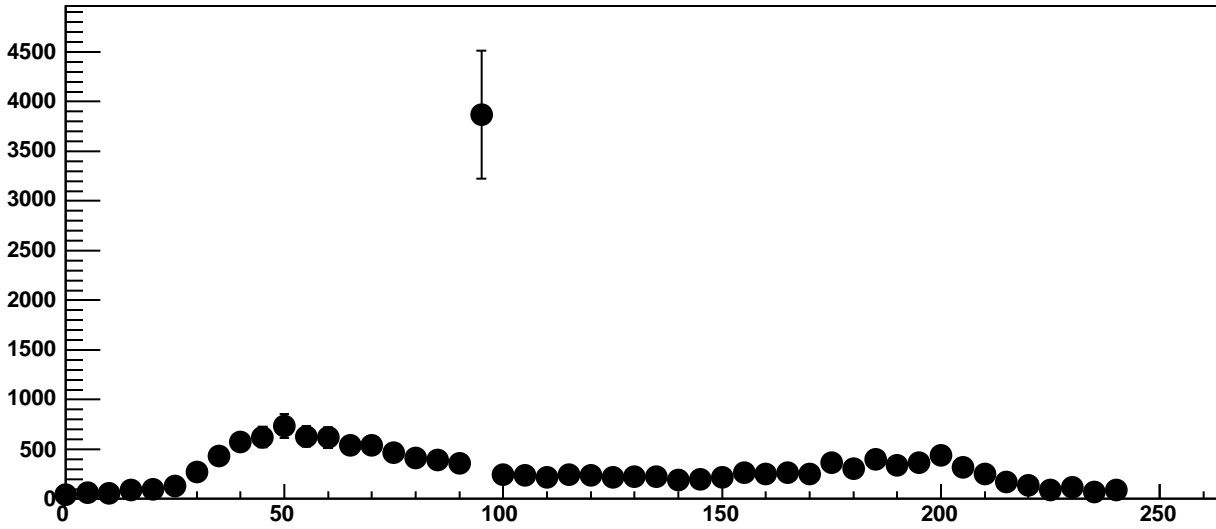


Chip 0, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

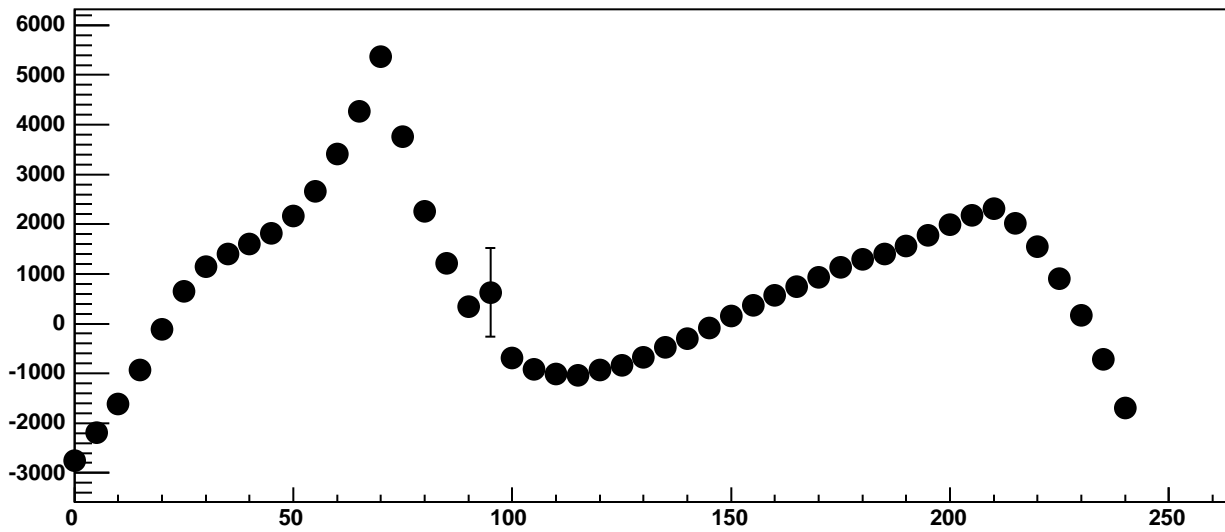


$\chi^2 / \text{ndf}$	3.207e+04 / 41
p0	-5750 ± 35.51
p1	70.4 ± 0.1217
p2	3.716e+04 ± 212.2
p3	58.47 ± 0.3156
p4	-103.1 ± 0.8201

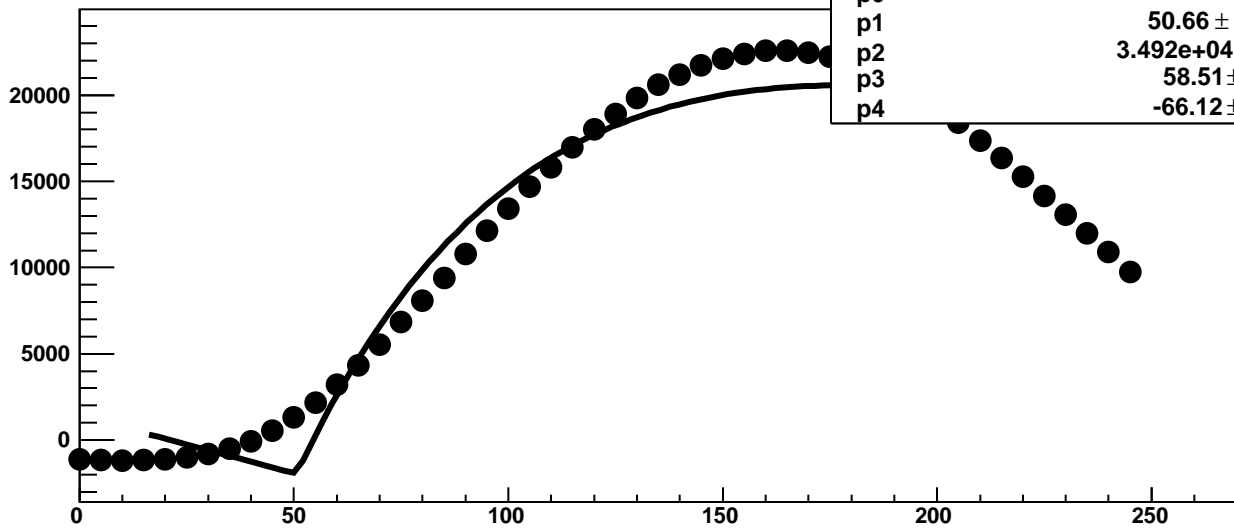
Chip 0, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



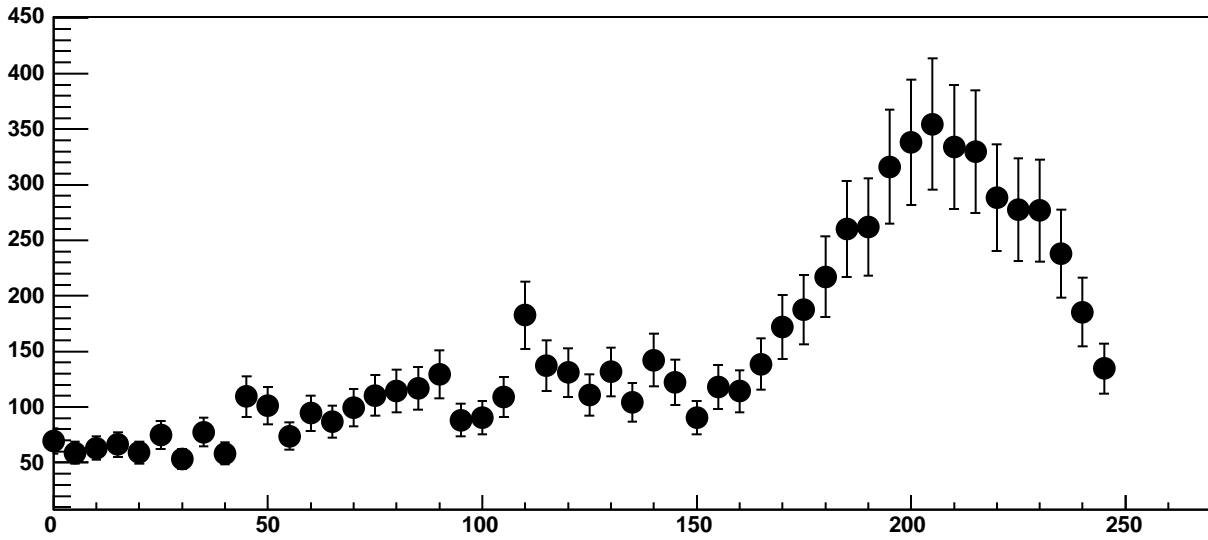
Chip 0, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold



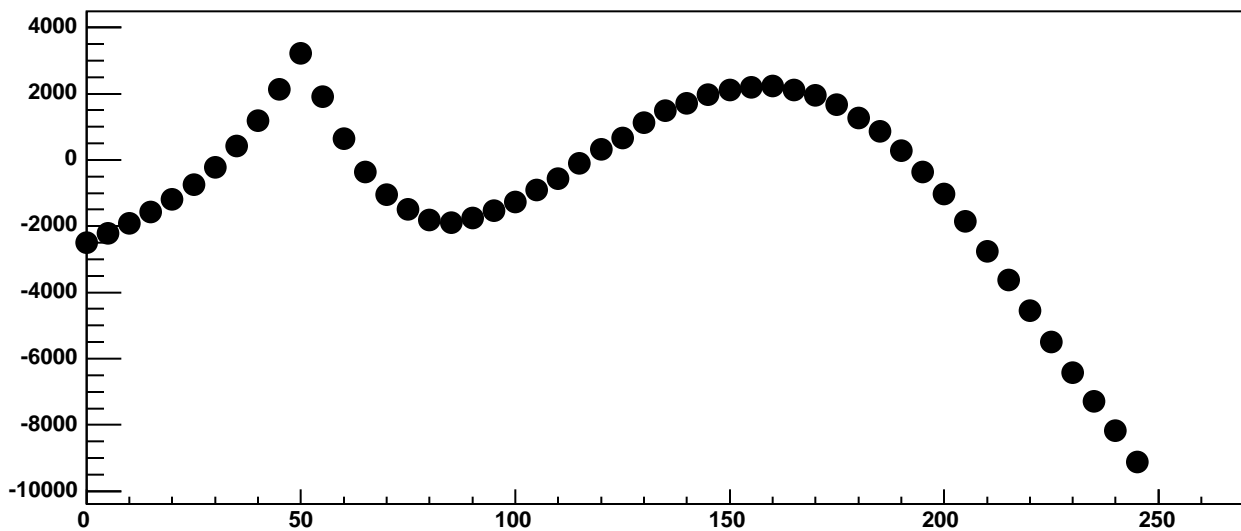
Chip 0, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold



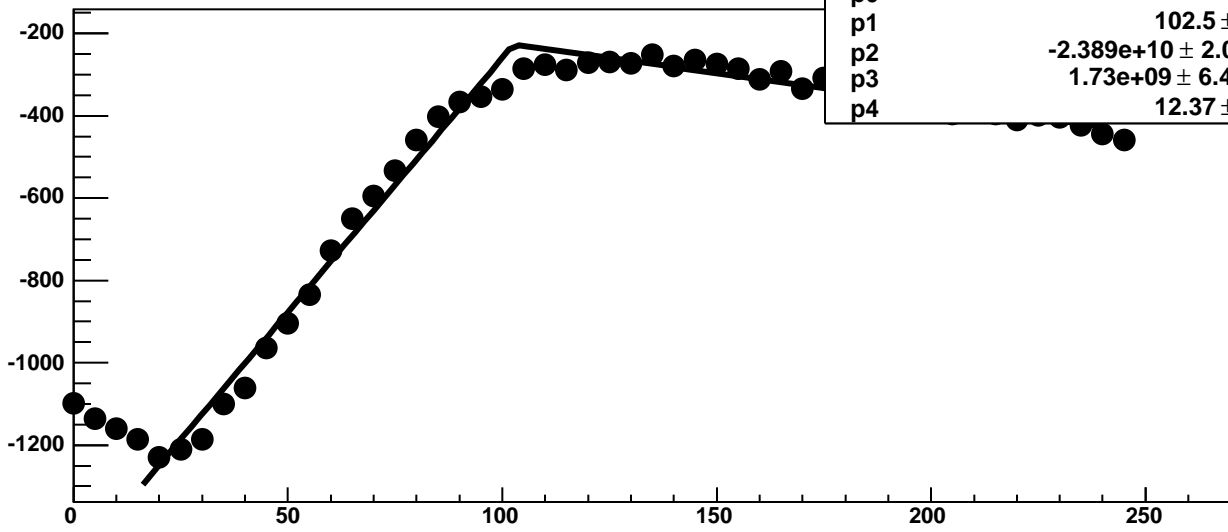
Chip 0, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

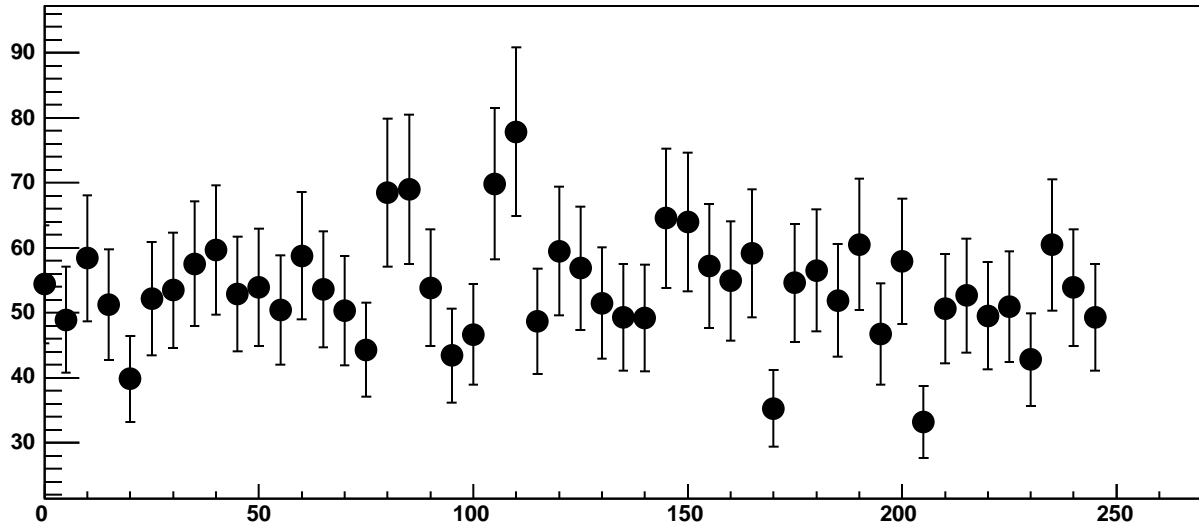


Chip 0, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

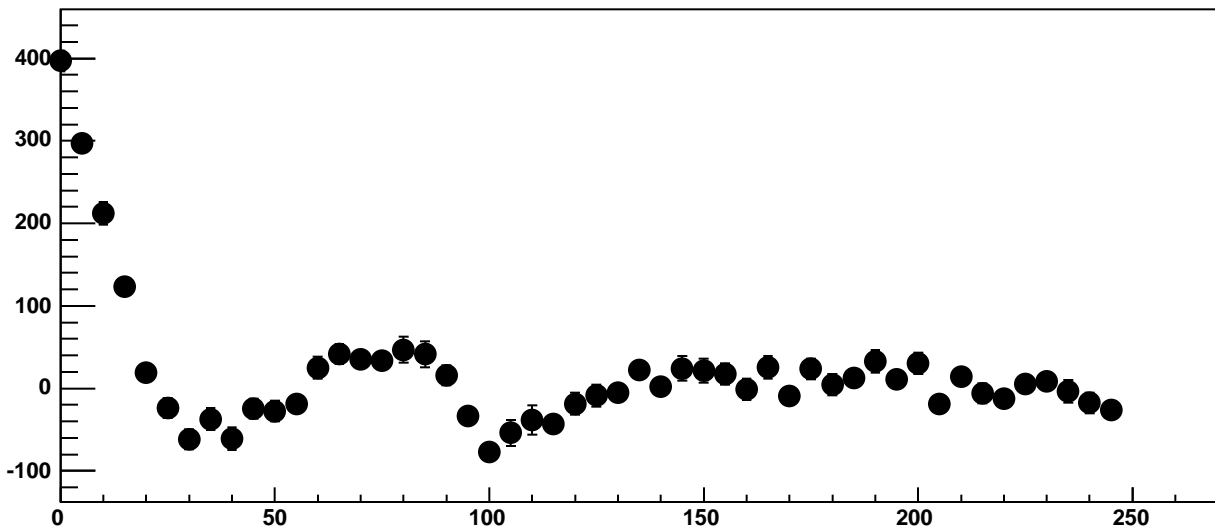


$\chi^2 / \text{ndf}$	377.7 / 41
p0	-227.4 ± 4.419
p1	102.5 ± 0.5253
p2	-2.389e+10 ± 2.043e+08
p3	1.73e+09 ± 6.493e+05
p4	12.37 ± 0.1023

Chip 0, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

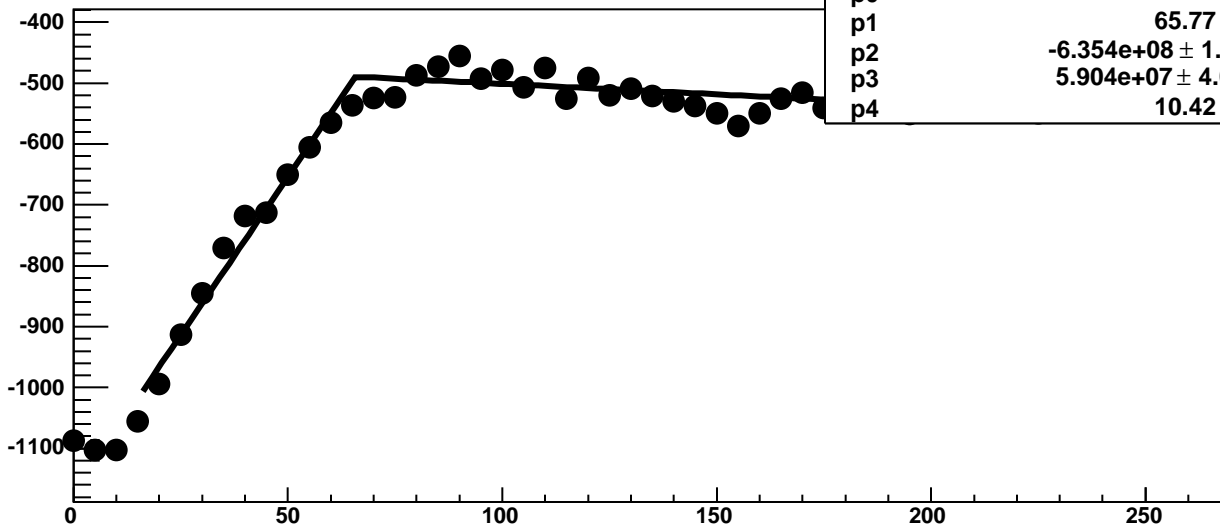


Chip 0, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



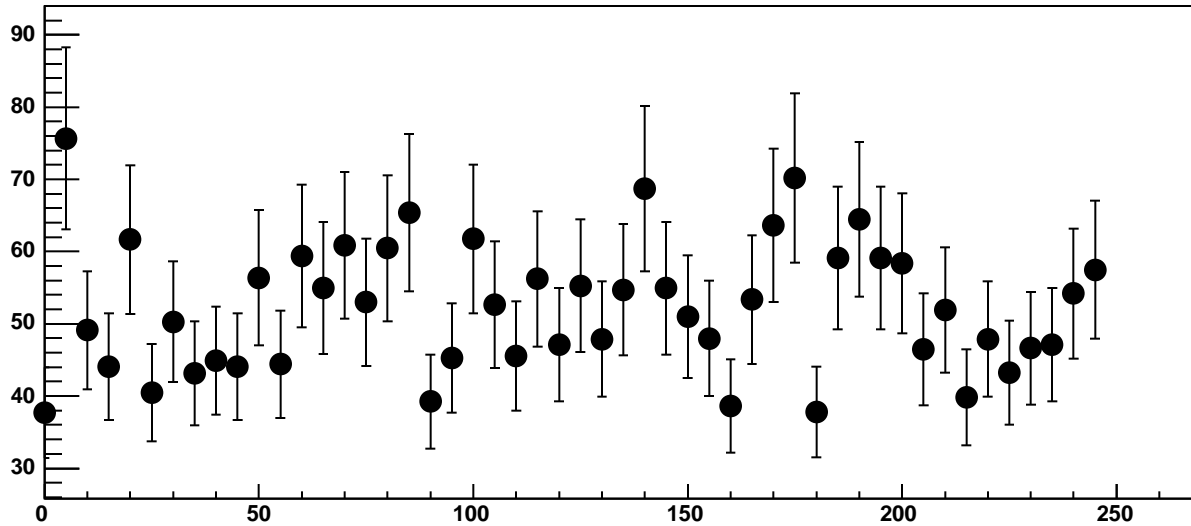


Chip 0, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold

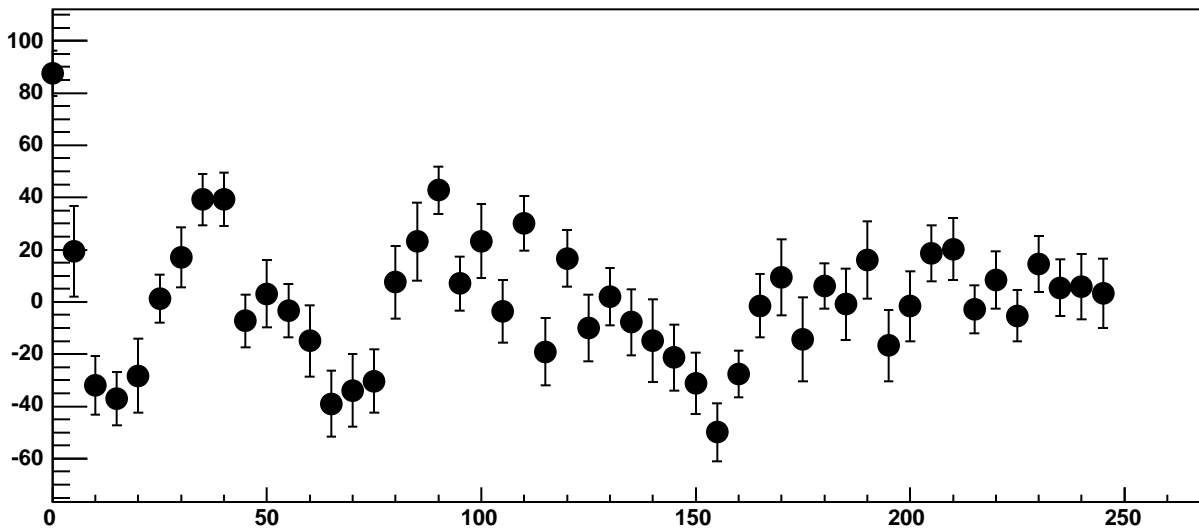


$\chi^2 / \text{ndf}$	170.4 / 41
p0	$-489.4 \pm 3.949$
p1	$65.77 \pm 0.7532$
p2	$-6.354\text{e}+08 \pm 1.379\text{e}+07$
p3	$5.904\text{e}+07 \pm 4.098\text{e}+05$
p4	$10.42 \pm 0.2227$

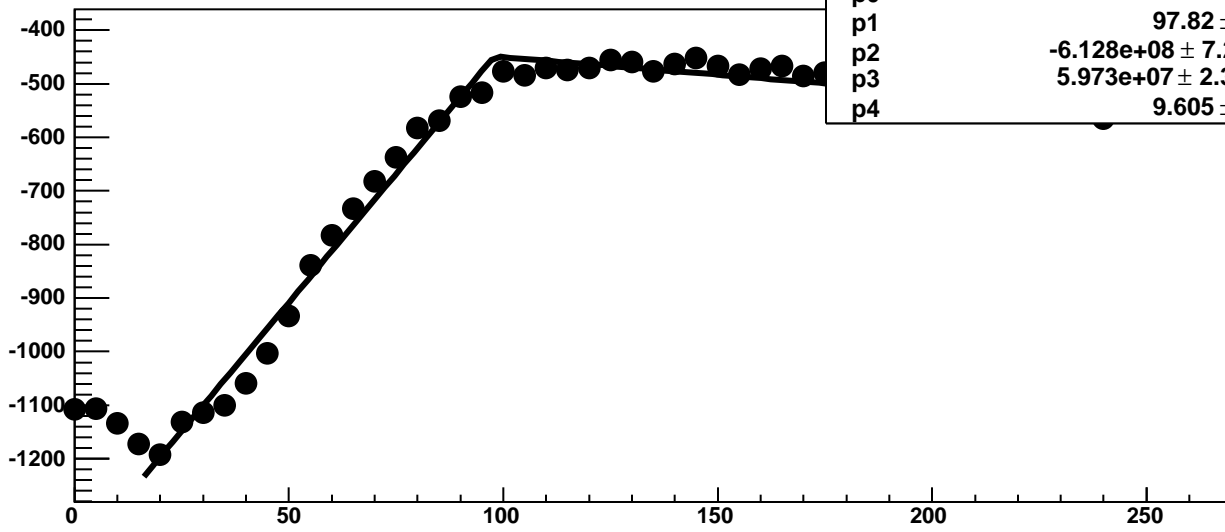
Chip 0, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

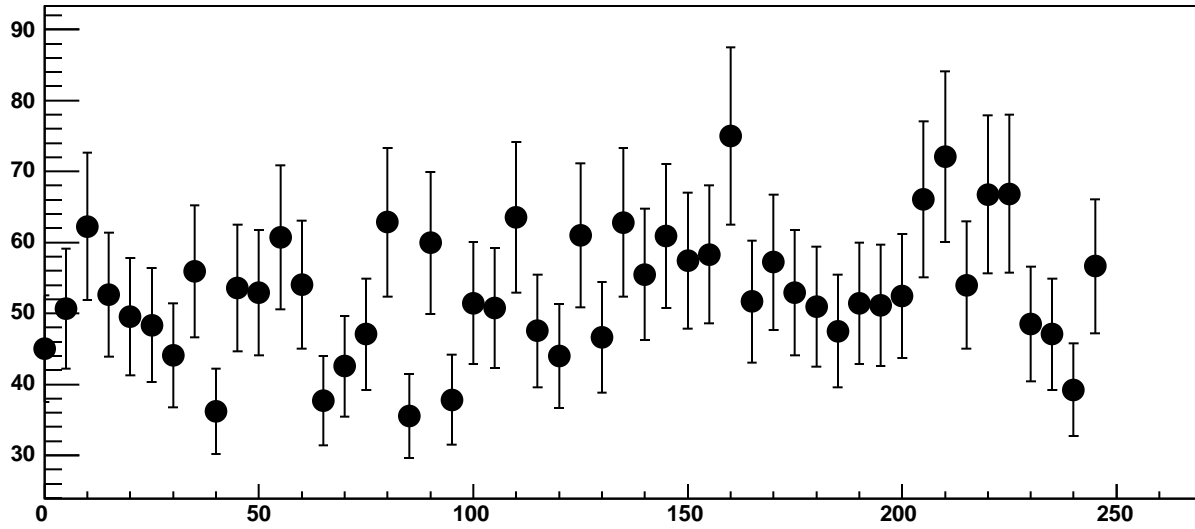


Chip 0, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

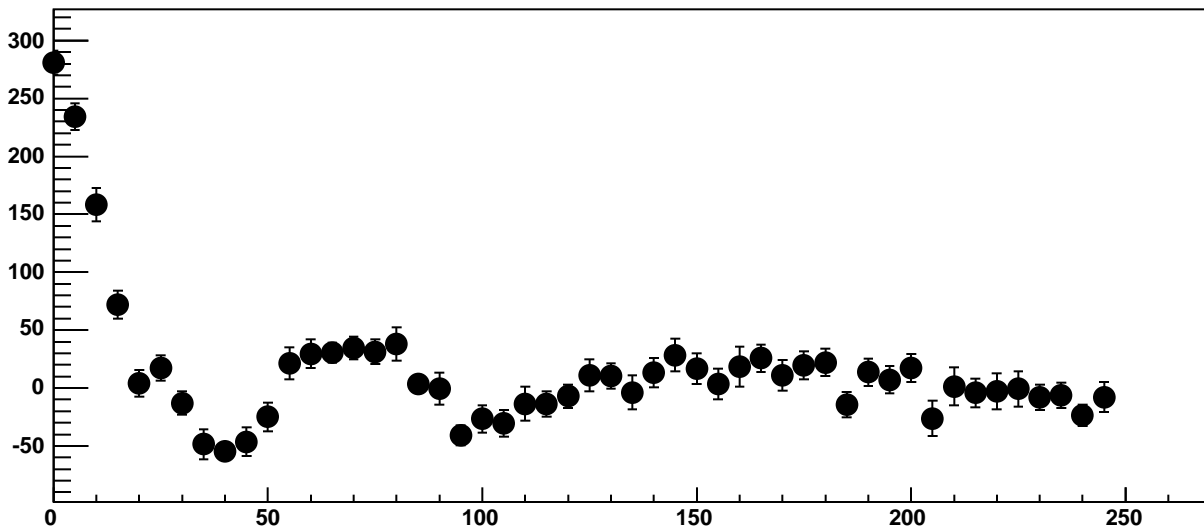


$\chi^2 / \text{ndf}$	239 / 41
p0	-448.9 ± 4.179
p1	97.82 ± 0.6515
p2	-6.128e+08 ± 7.229e+06
p3	5.973e+07 ± 2.308e+05
p4	9.605 ± 0.1046

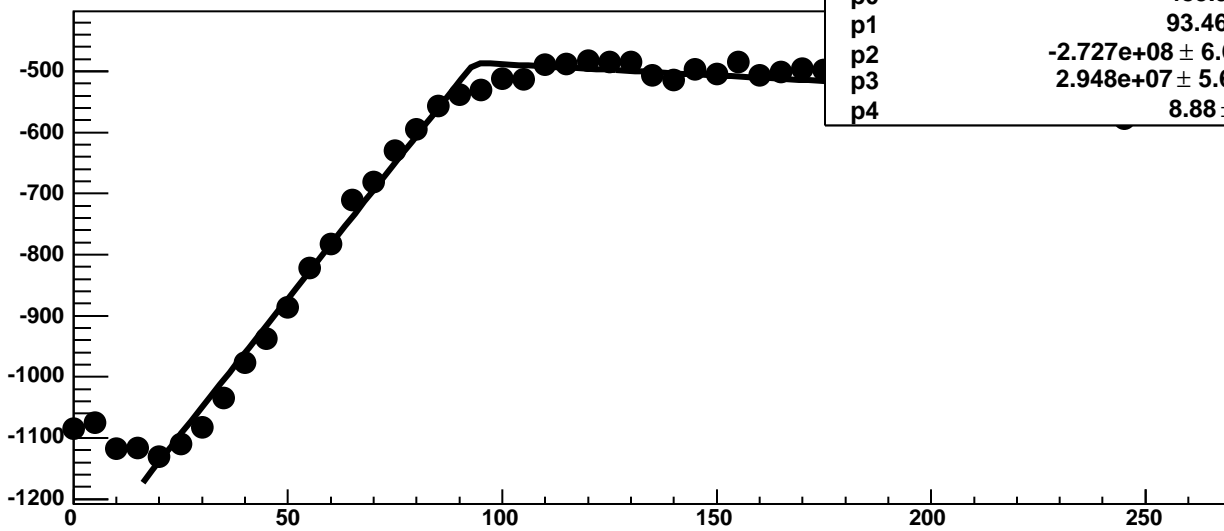
Chip 0, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

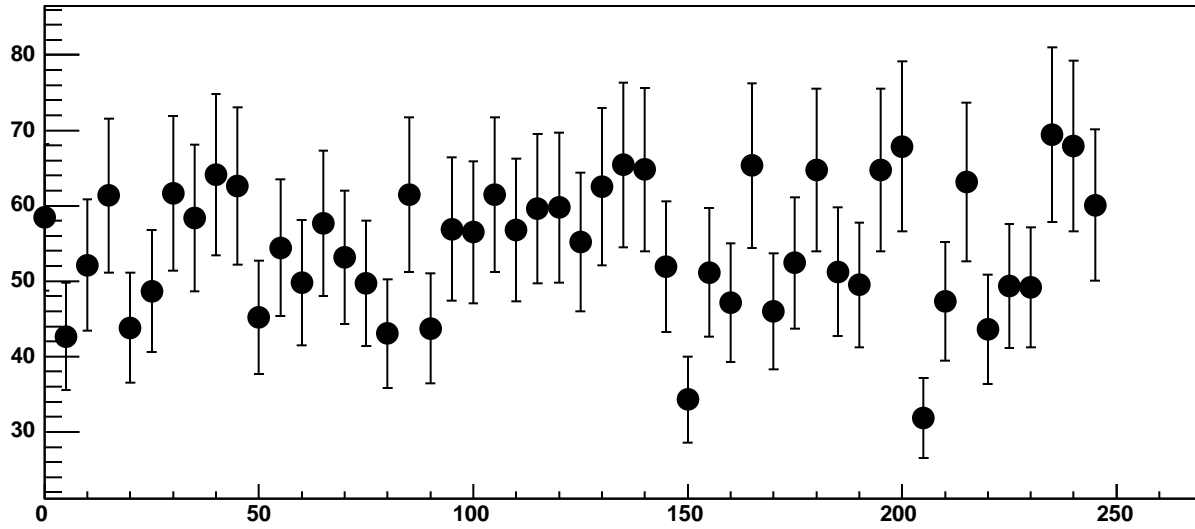


Chip 0, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

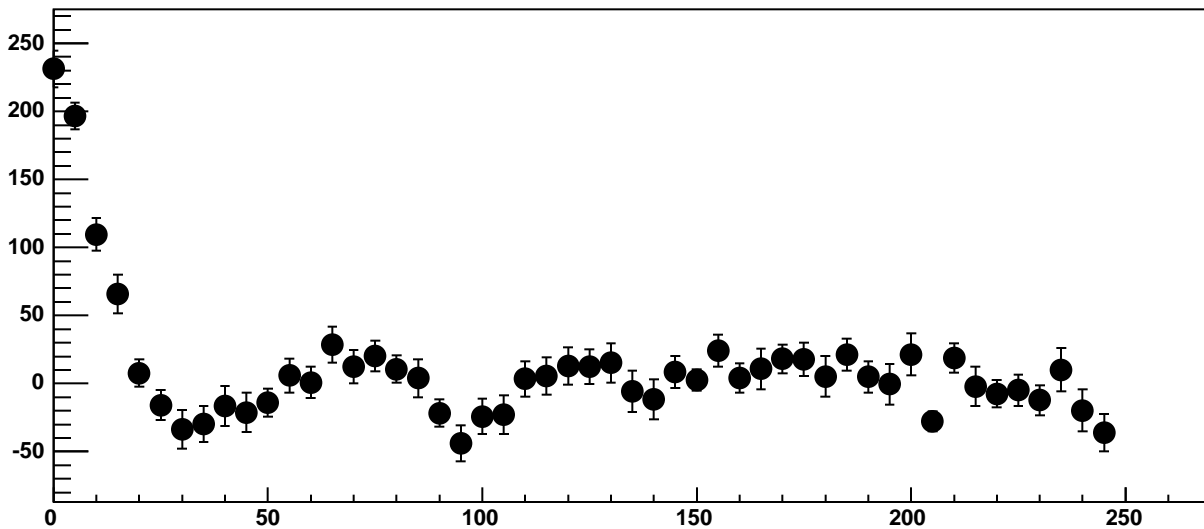


$\chi^2 / \text{ndf}$	114.6 / 41
p0	$-485.9 \pm 4.509$
p1	$93.46 \pm 0.804$
p2	$-2.727\text{e}+08 \pm 6.689\text{e}+06$
p3	$2.948\text{e}+07 \pm 5.661\text{e}+05$
p4	$8.88 \pm 0.1259$

Chip 0, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold

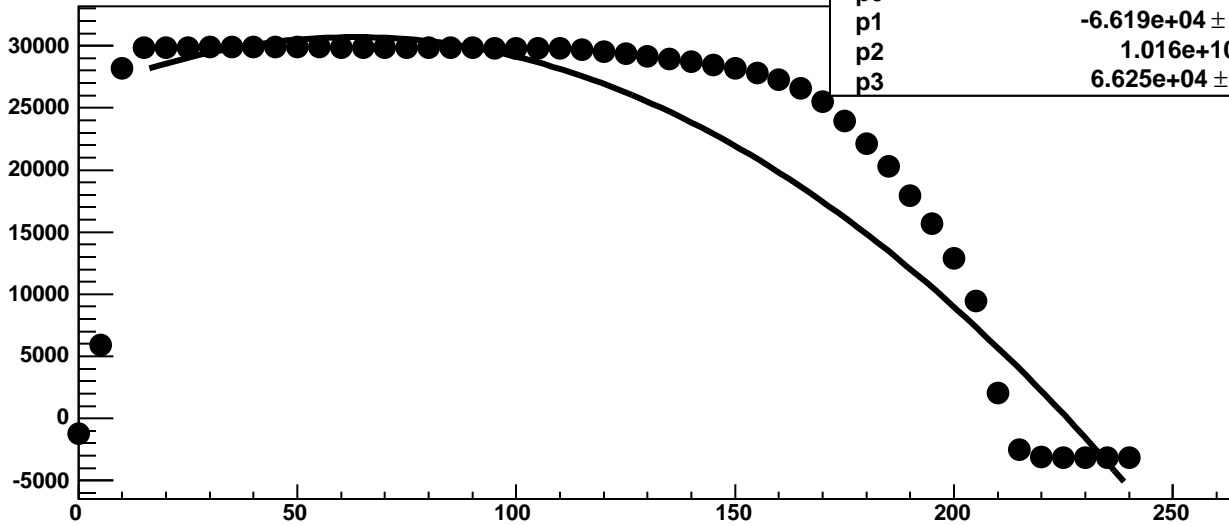


Chip 0, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

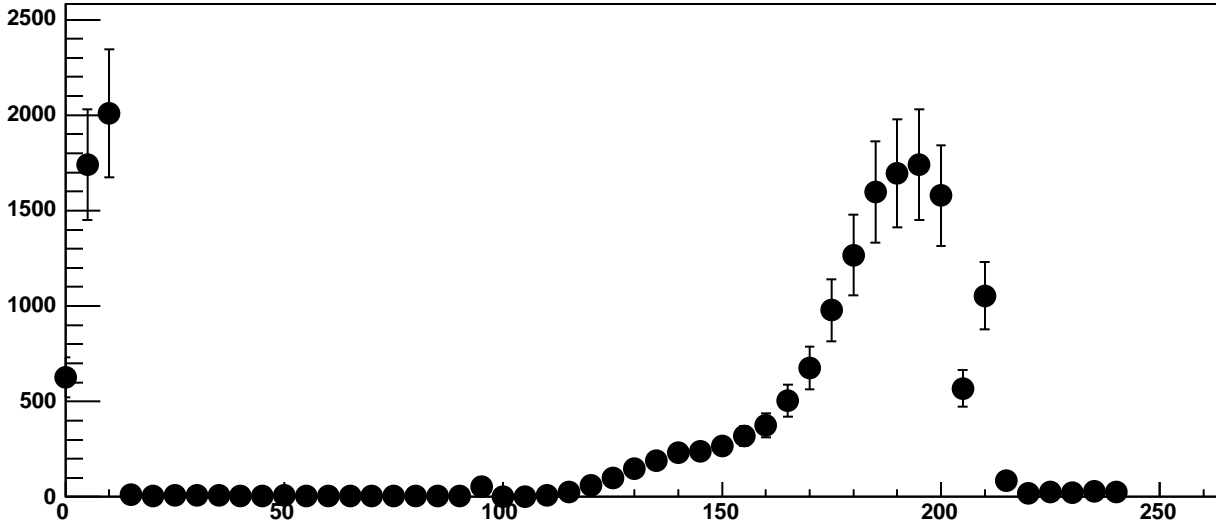


Chip 0, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

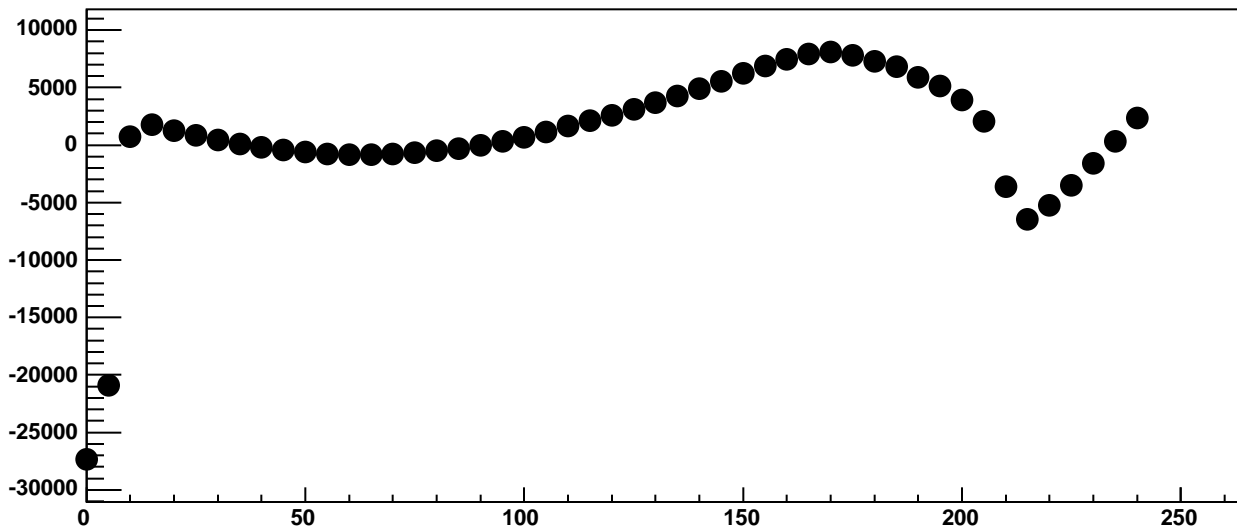
$\chi^2 / \text{ndf}$	1.32e+07 / 42
p0	-1.016e+10 $\pm$ 3.441
p1	-6.619e+04 $\pm$ 0.03924
p2	1.016e+10 $\pm$ 3.441
p3	6.625e+04 $\pm$ 0.03921



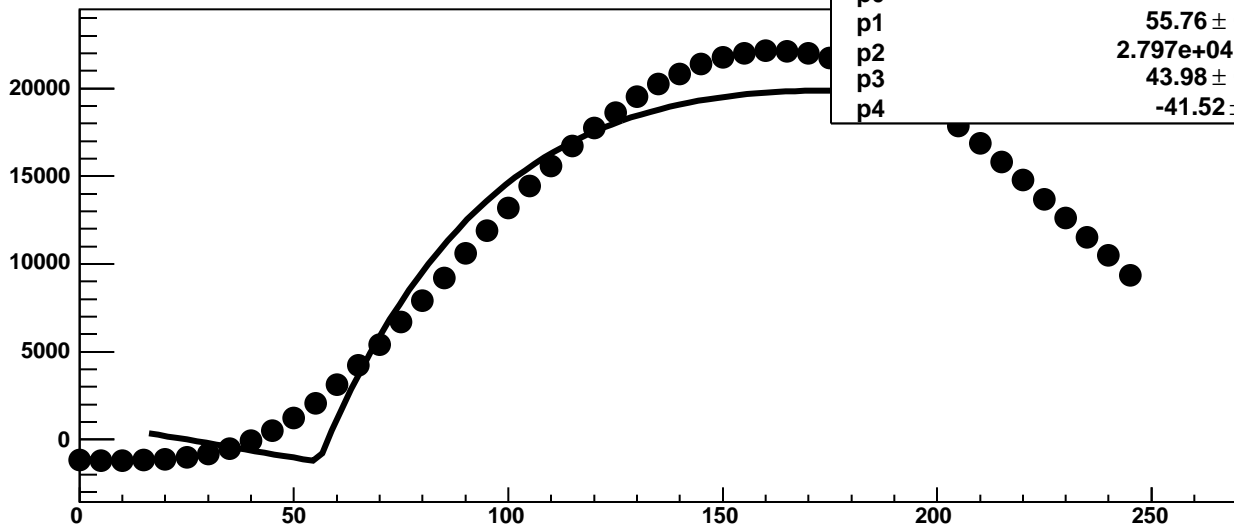
Chip 0, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

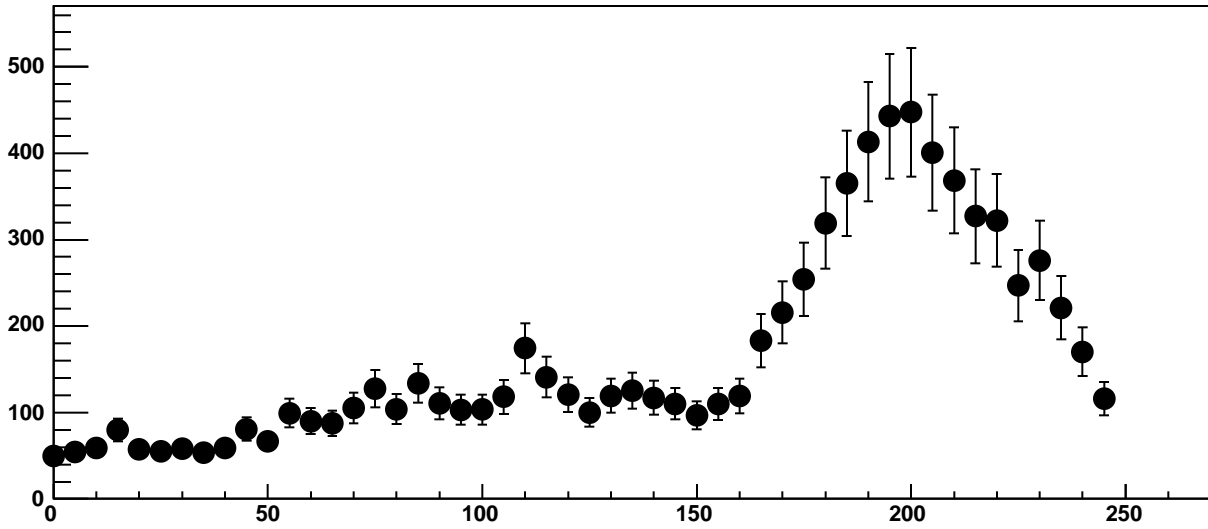


Chip 0, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

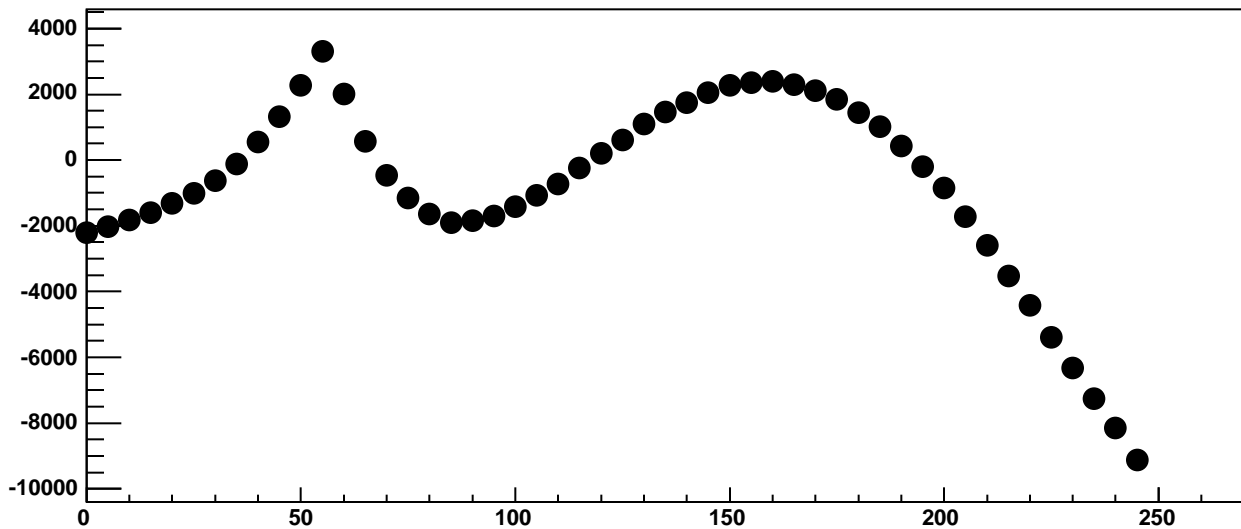


$\chi^2 / \text{ndf}$	2.513e+05 / 41
p0	-1271 ± 7.753
p1	55.76 ± 0.02996
p2	2.797e+04 ± 53.08
p3	43.98 ± 0.09505
p4	-41.52 ± 0.2911

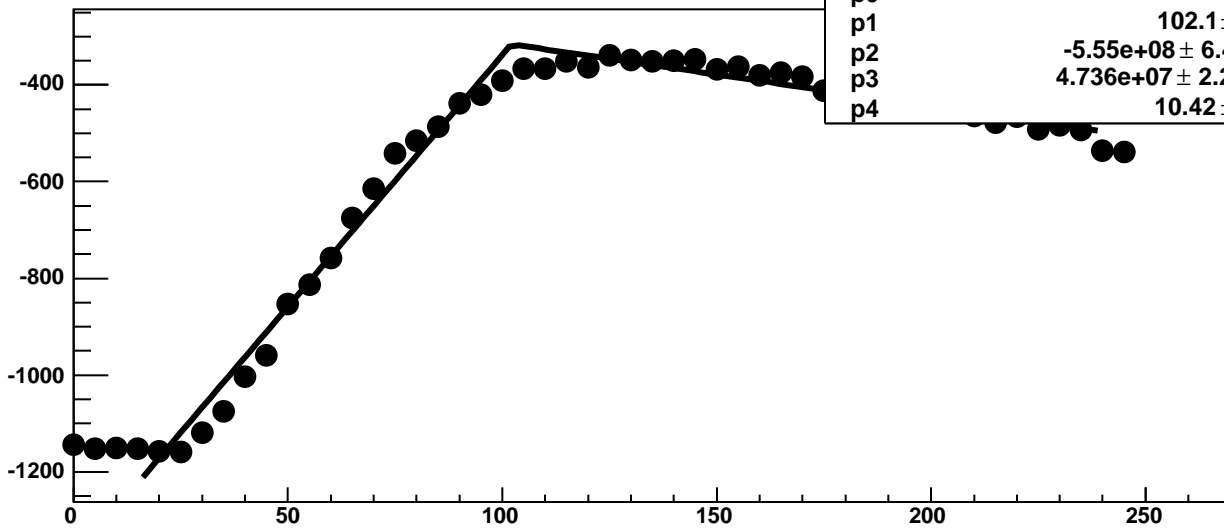
Chip 0, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

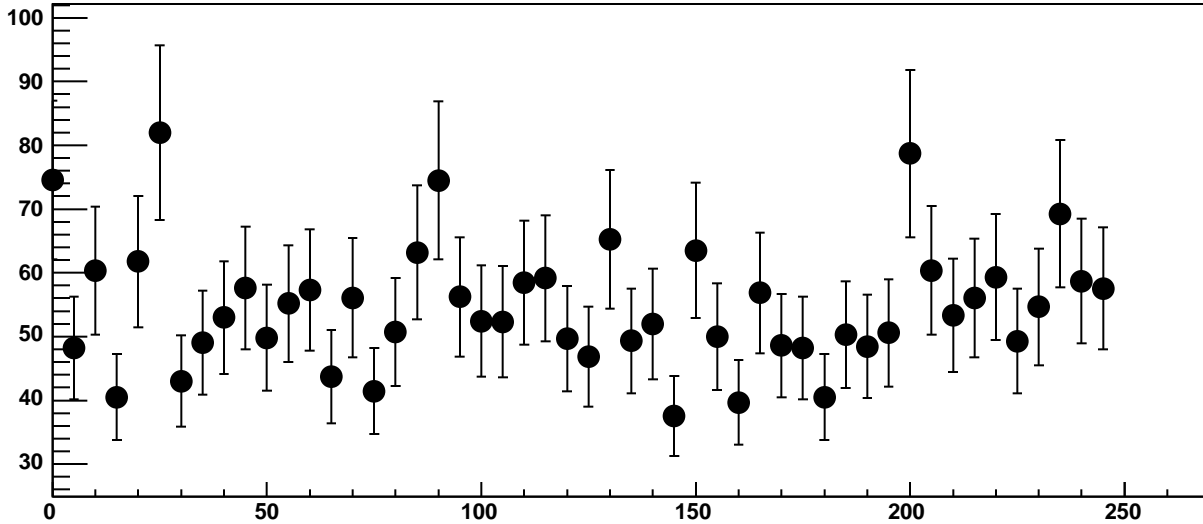


Chip 0, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

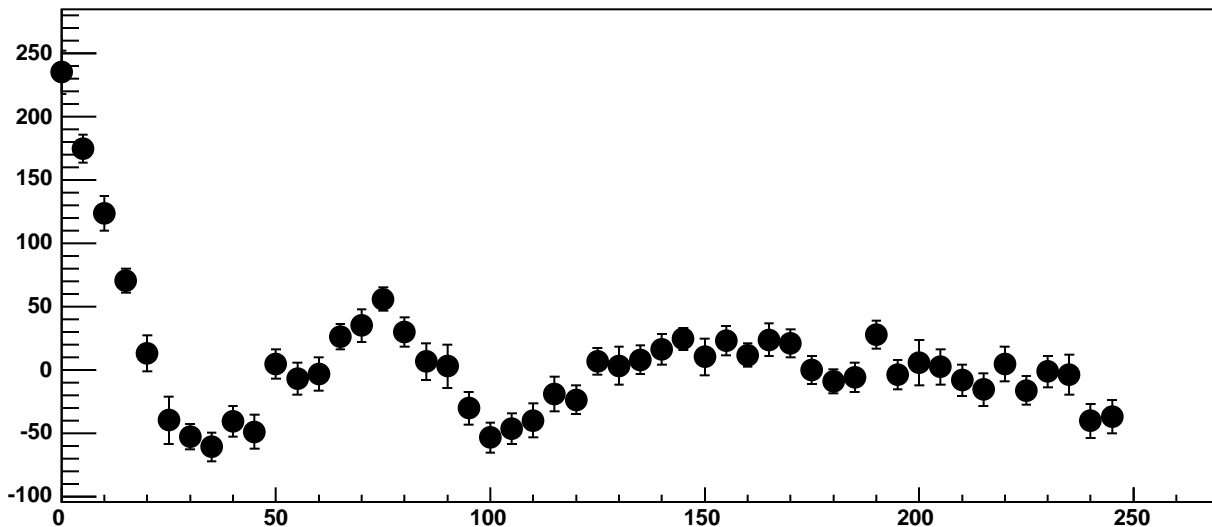


$\chi^2 / \text{ndf}$	303.5 / 41
p0	$-315.9 \pm 4.141$
p1	$102.1 \pm 0.6312$
p2	$-5.55e+08 \pm 6.451e+06$
p3	$4.736e+07 \pm 2.296e+05$
p4	$10.42 \pm 0.1098$

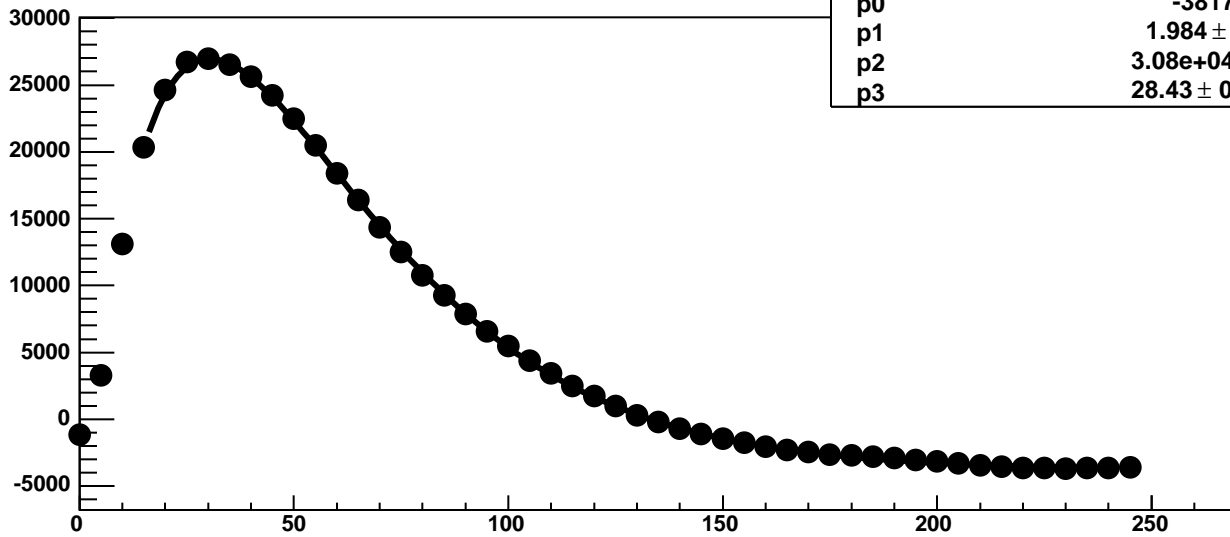
Chip 0, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

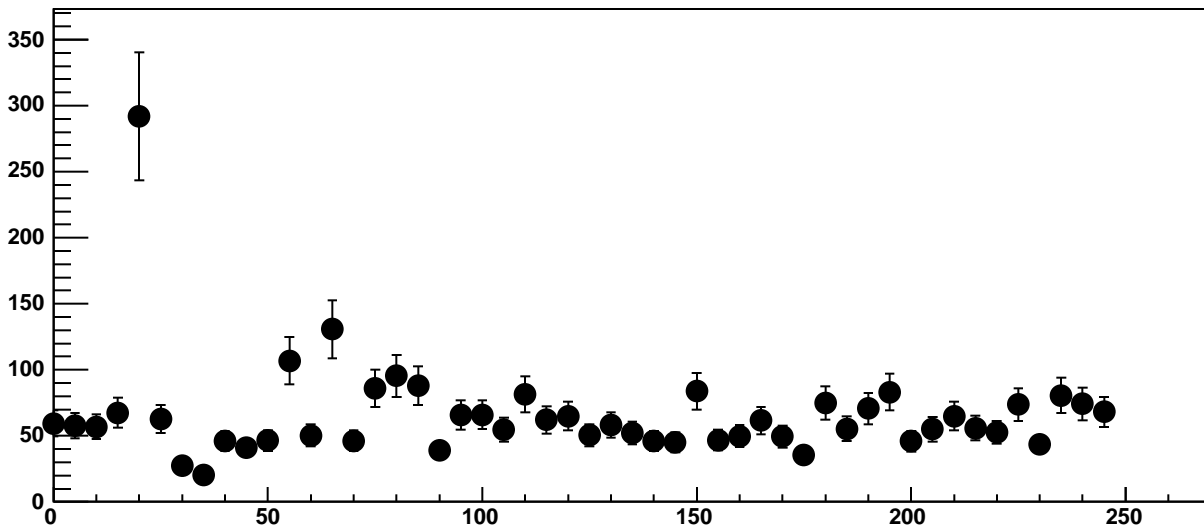


Chip 0, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

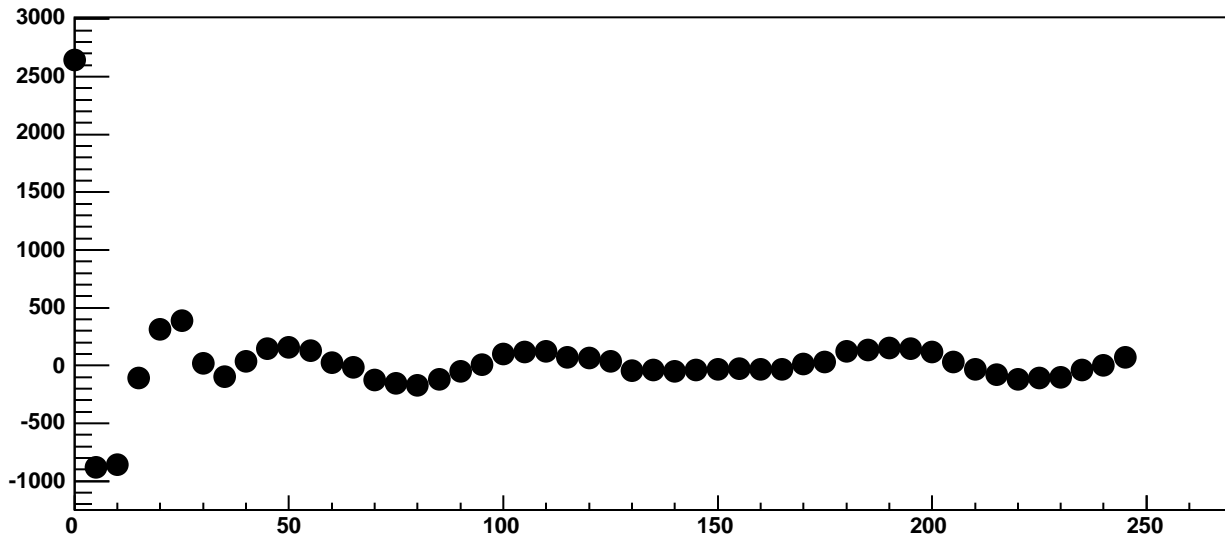


$\chi^2 / \text{ndf}$	3093 / 42
p0	-3817 ± 3.605
p1	1.984 ± 0.01647
p2	3.08e+04 ± 4.553
p3	28.43 ± 0.009913

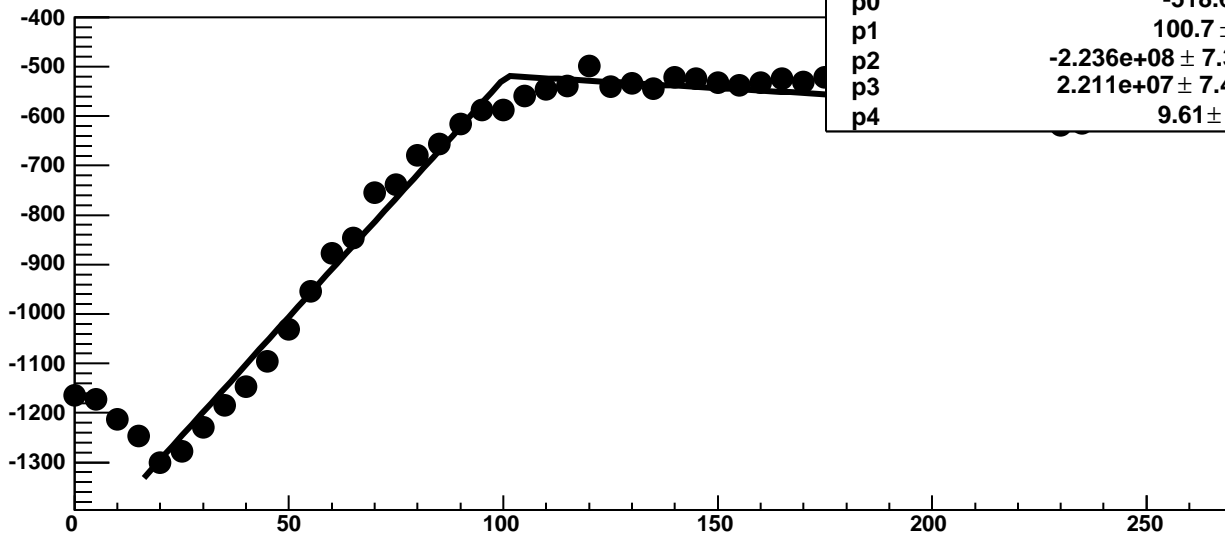
Chip 0, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

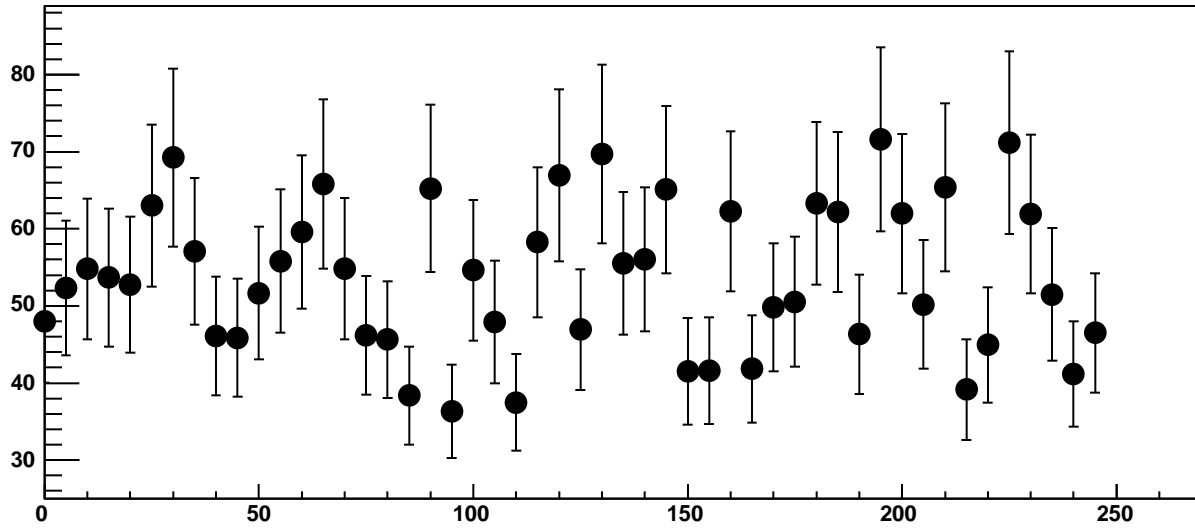


Chip 0, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

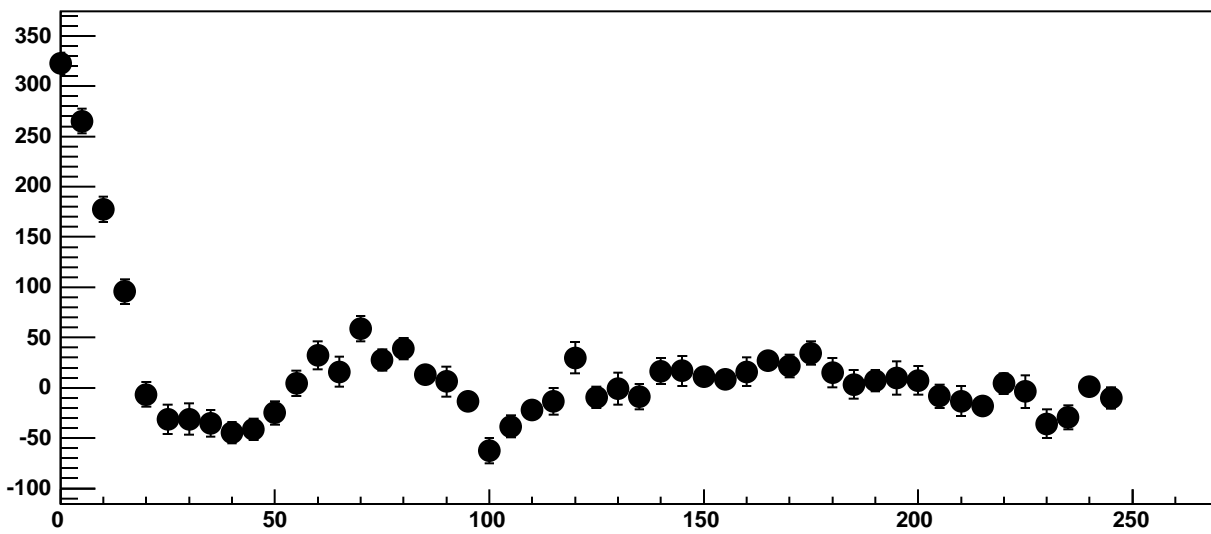


$\chi^2 / \text{ndf}$	265.5 / 41
p0	$-518.6 \pm 4.119$
p1	$100.7 \pm 0.6325$
p2	$-2.236\text{e}+08 \pm 7.321\text{e}+06$
p3	$2.211\text{e}+07 \pm 7.466\text{e}+05$
p4	$9.61 \pm 0.09912$

Chip 0, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold

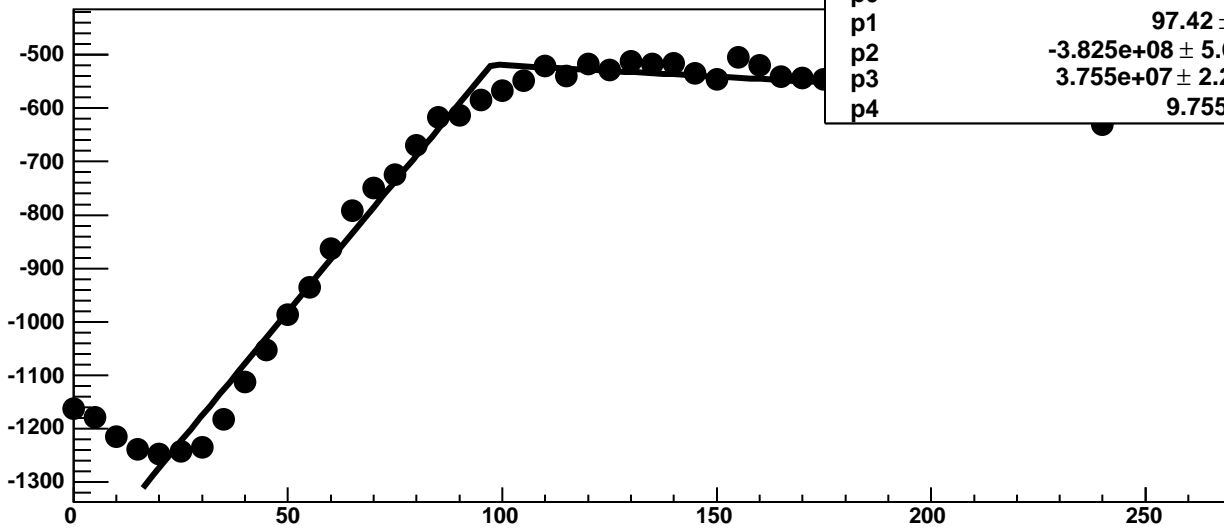


Chip 0, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



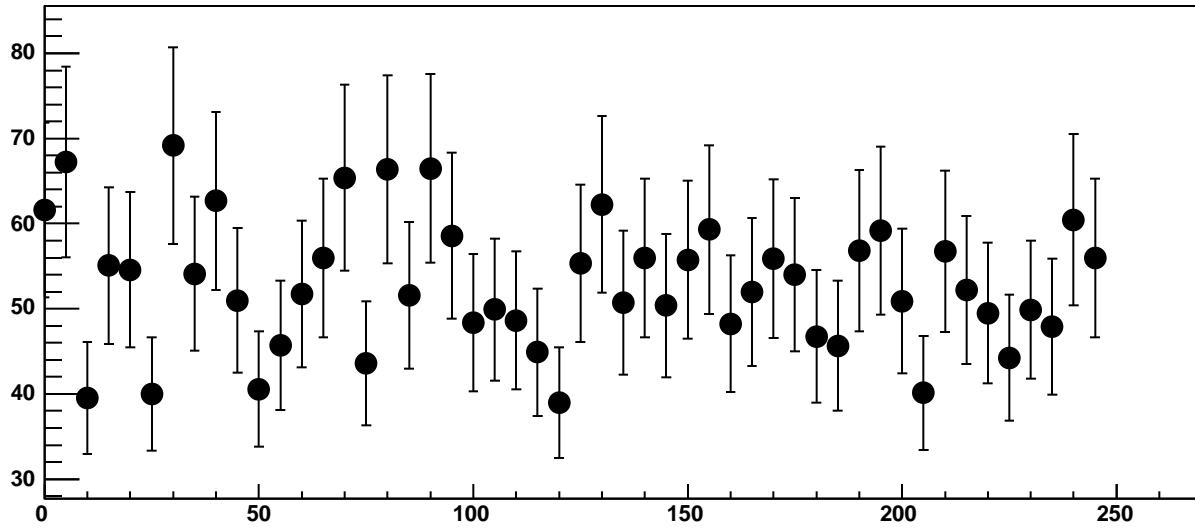


Chip 0, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

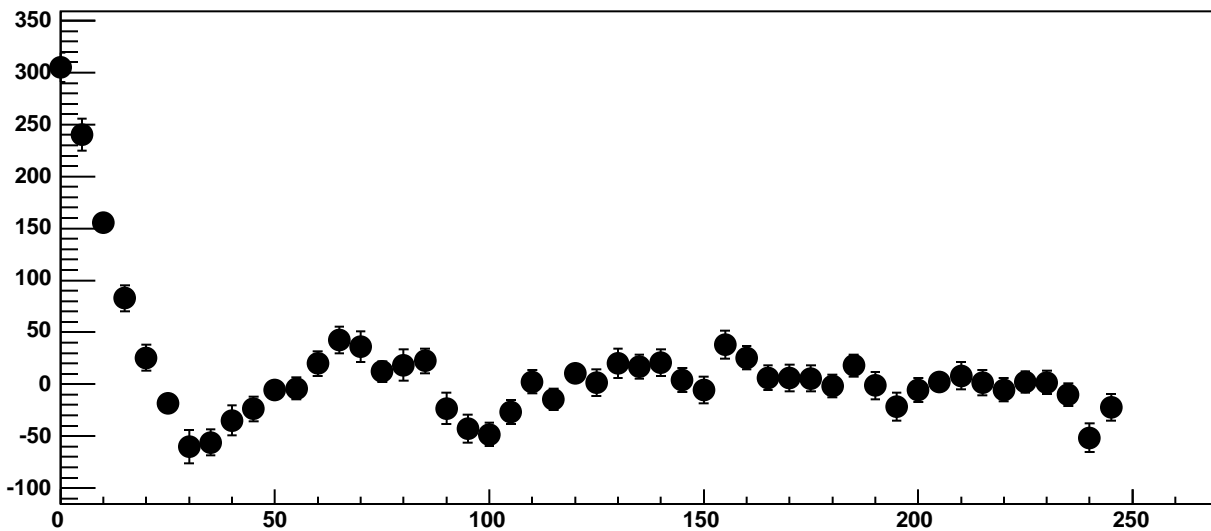


$\chi^2 / \text{ndf}$	204.9 / 41
p0	$-518 \pm 4.055$
p1	$97.42 \pm 0.7385$
p2	$-3.825\text{e}+08 \pm 5.695\text{e}+06$
p3	$3.755\text{e}+07 \pm 2.291\text{e}+05$
p4	$9.755 \pm 0.125$

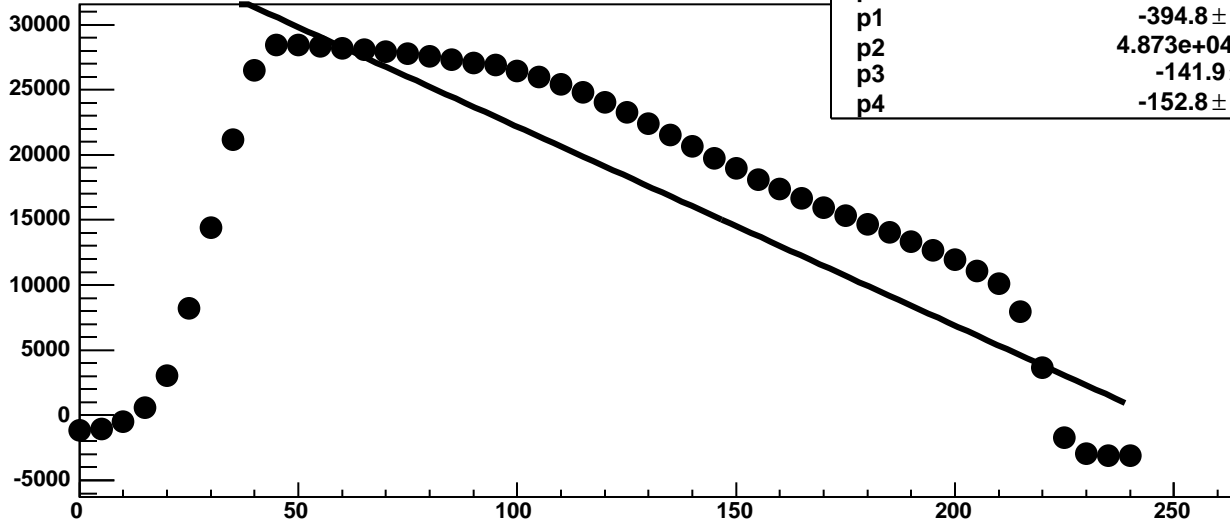
Chip 0, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



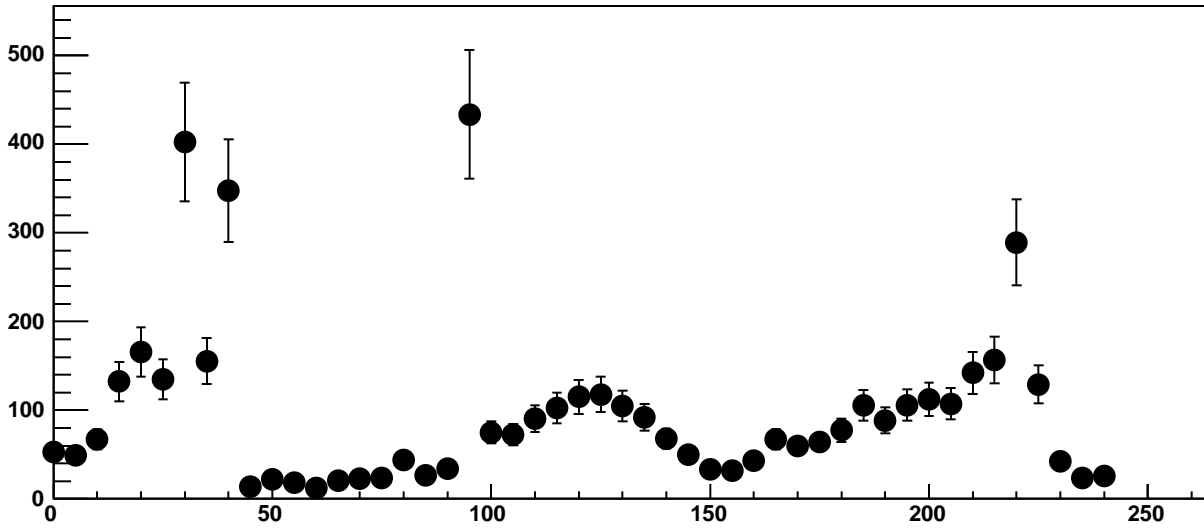
Chip 0, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold



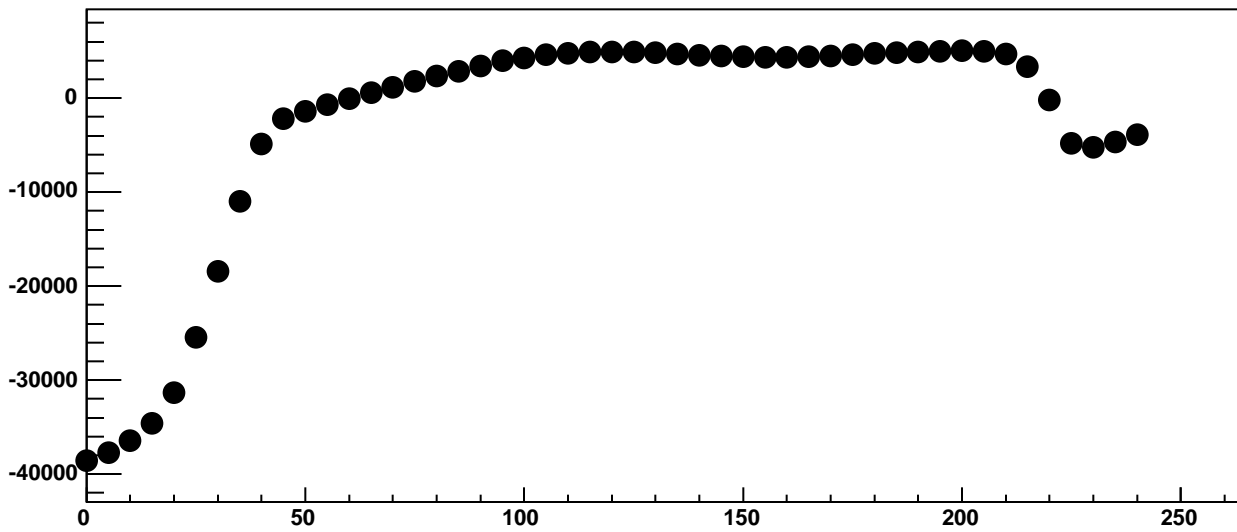
Chip 0, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold



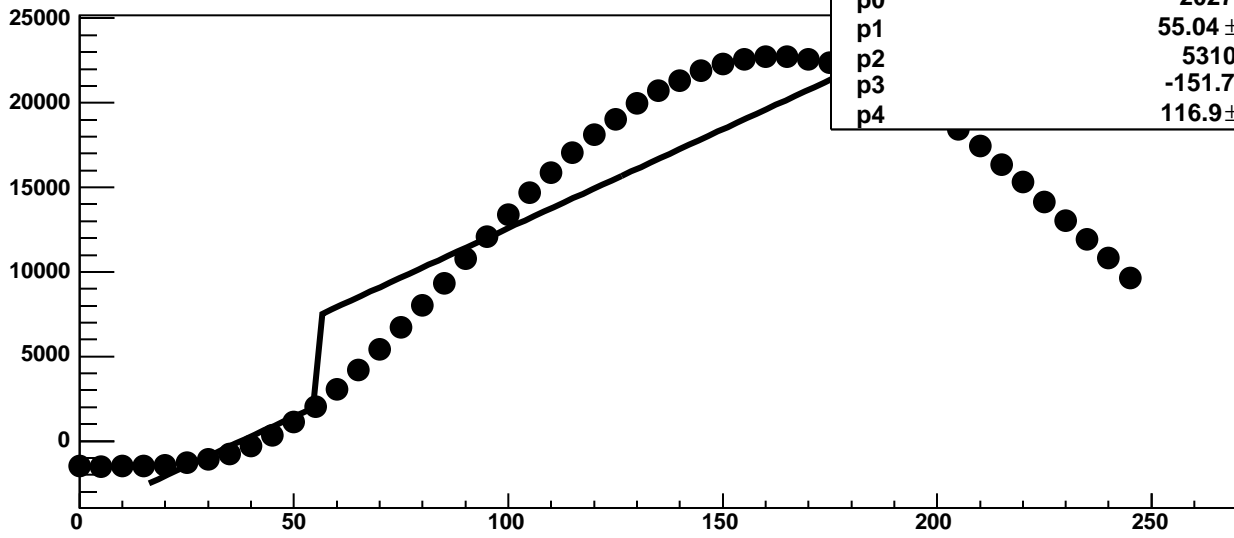
Chip 0, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 0, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold

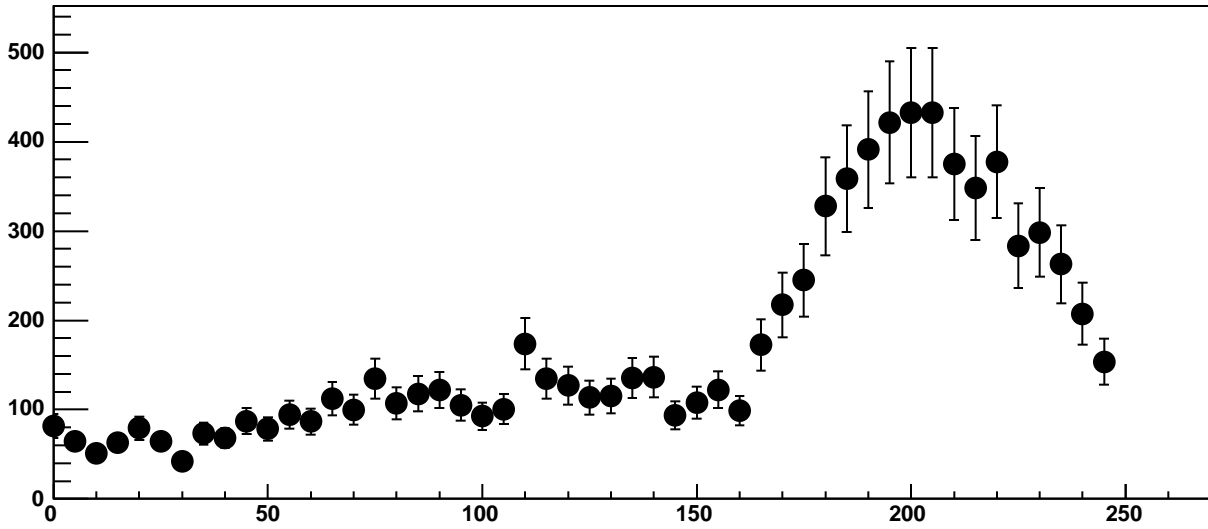


Chip 1, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold

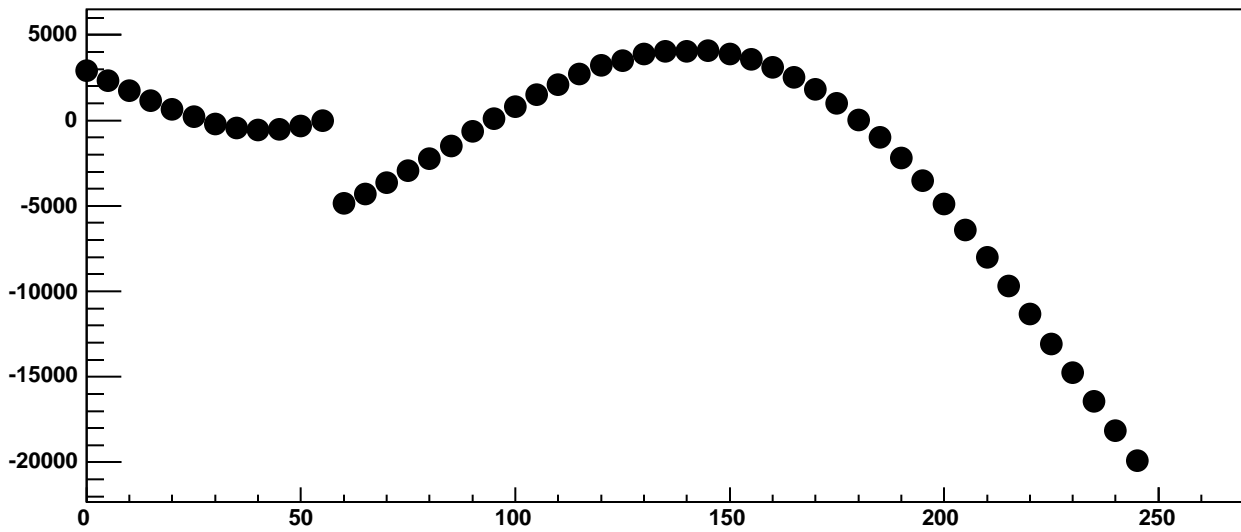


$\chi^2 / \text{ndf}$	7.032e+05 / 41
p0	2027 ± 16.09
p1	55.04 ± 0.1614
p2	5310 ± 36.81
p3	-151.7 ± 14.97
p4	116.9 ± 0.5274

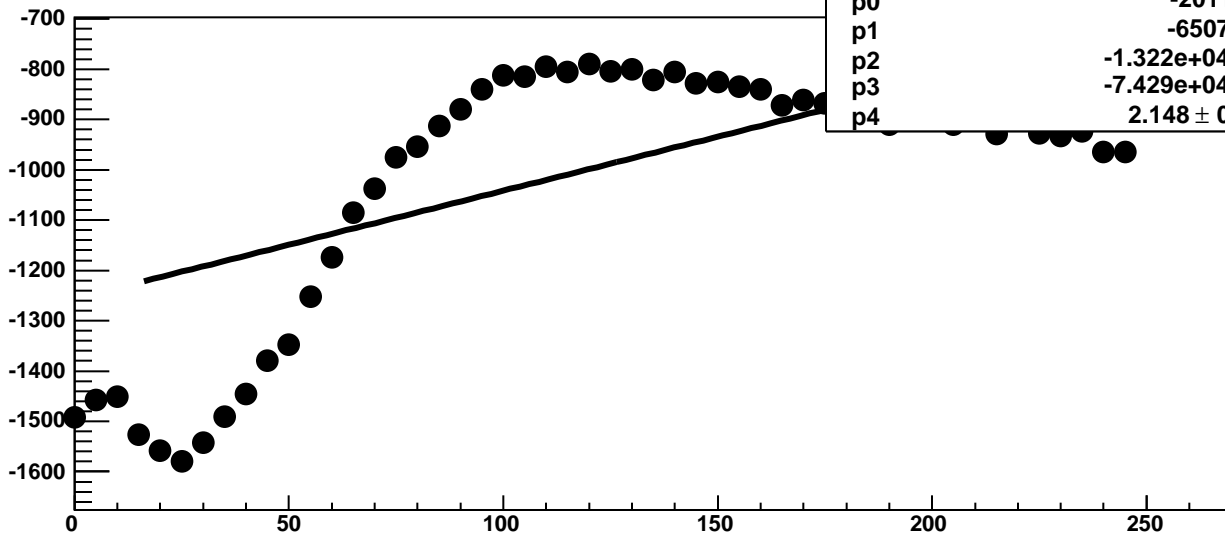
Chip 1, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold

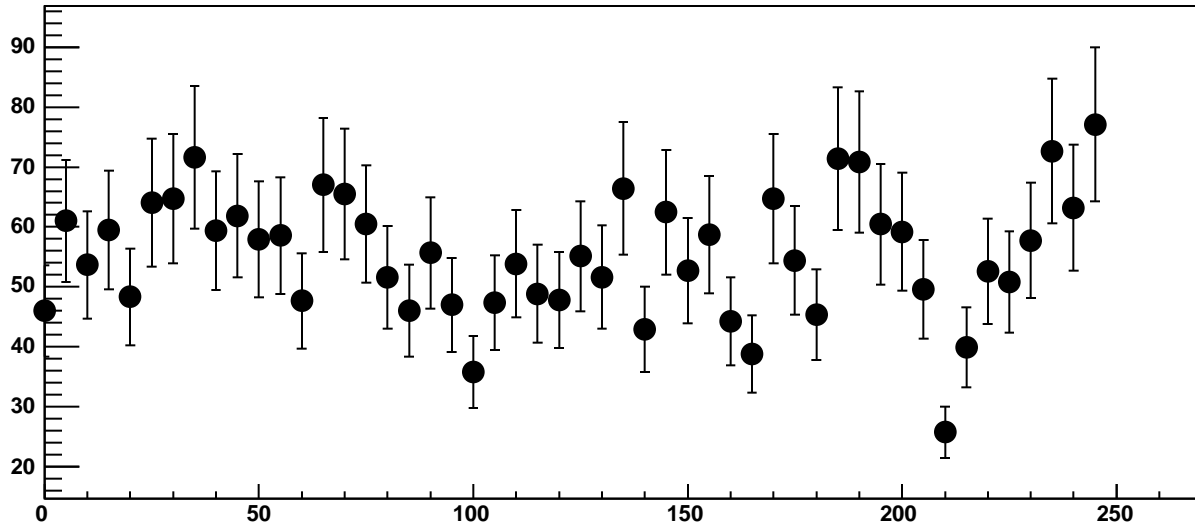


Chip 1, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

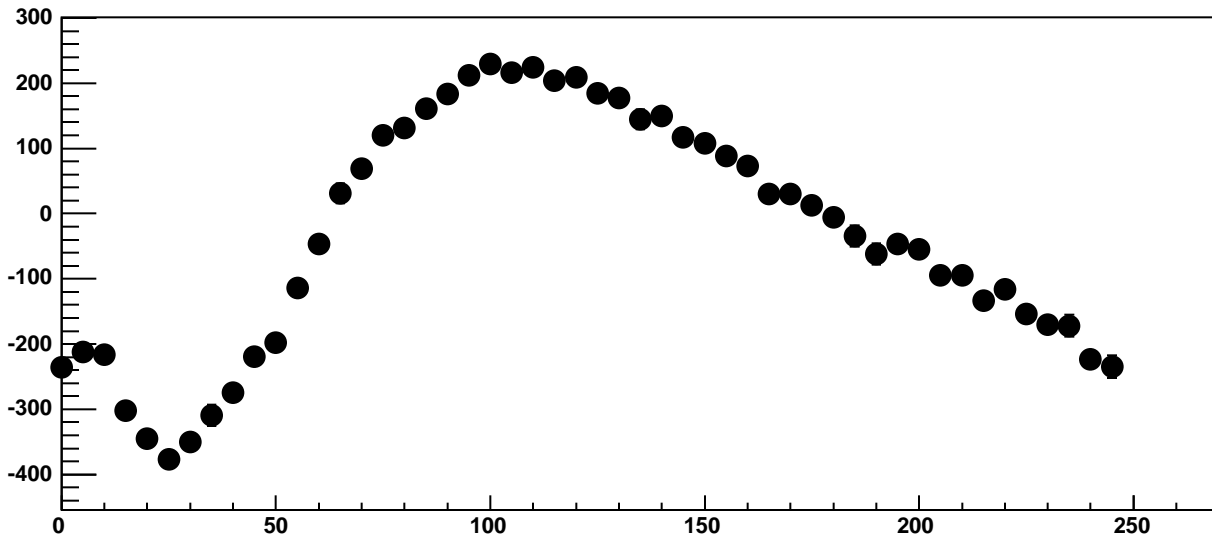


$\chi^2 / \text{ndf}$	9612 / 41
p0	$-2011 \pm 8.519$
p1	$-6507 \pm 3.693$
p2	$-1.322\text{e}+04 \pm 11.34$
p3	$-7.429\text{e}+04 \pm 492.7$
p4	$2.148 \pm 0.001282$

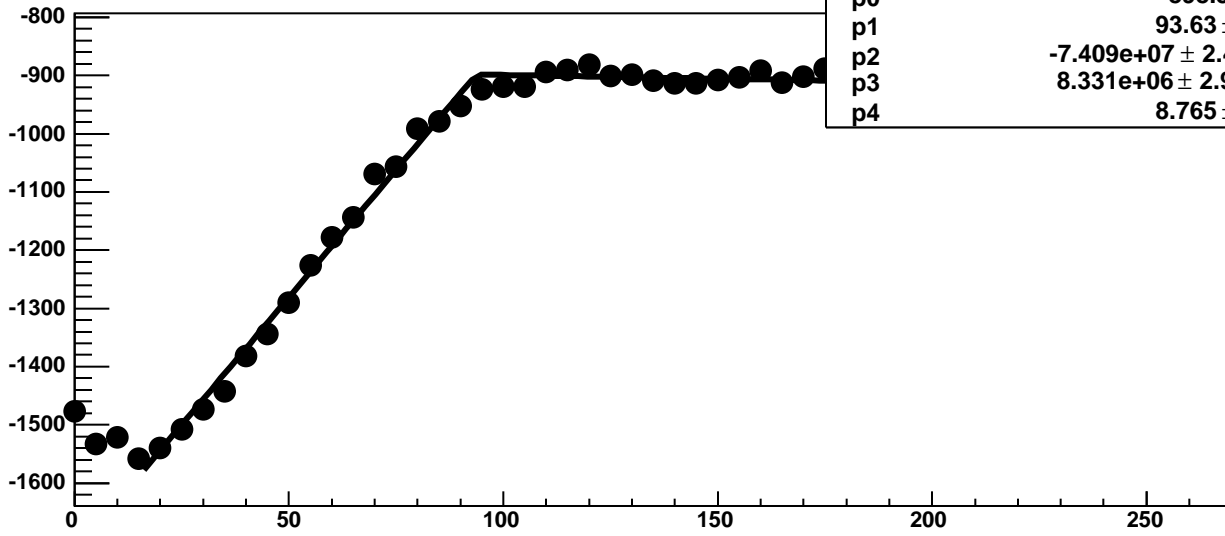
Chip 1, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold

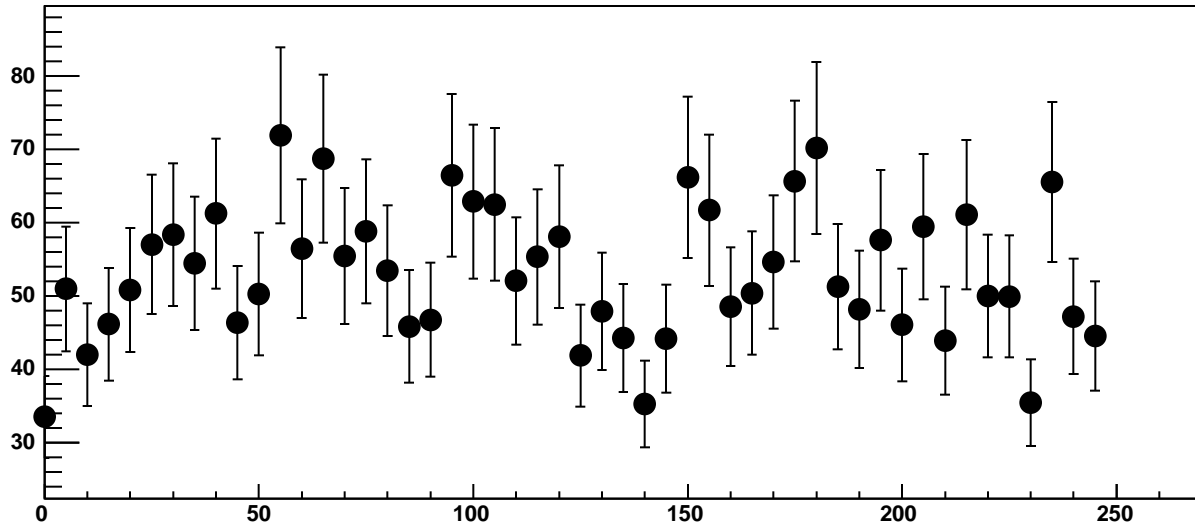


Chip 1, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

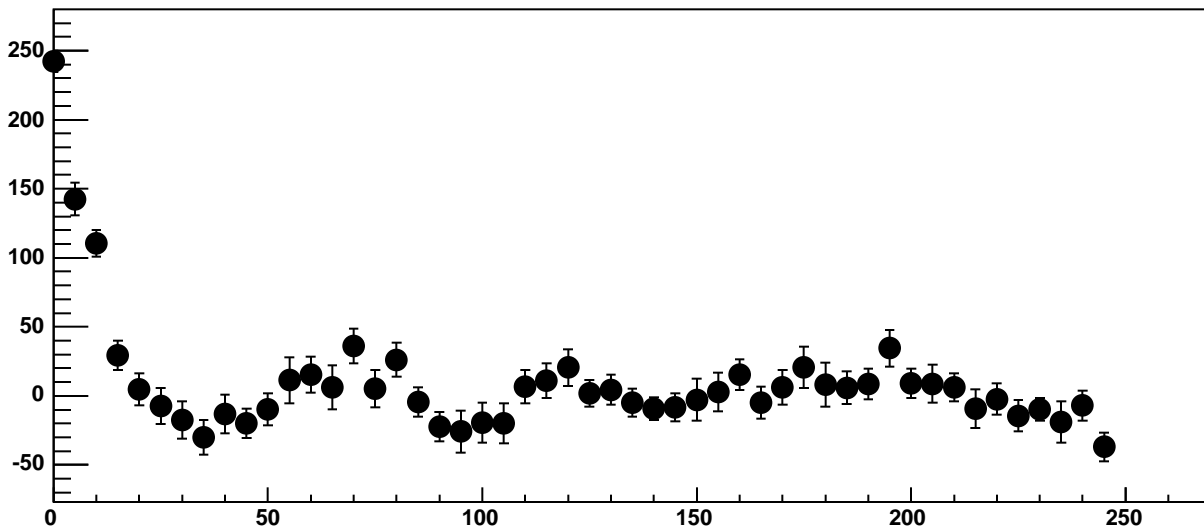


$\chi^2 / \text{ndf}$	71.74 / 41
p0	-898.3 ± 4.192
p1	93.63 ± 0.7813
p2	-7.409e+07 ± 2.418e+06
p3	8.331e+06 ± 2.907e+05
p4	8.765 ± 0.1133

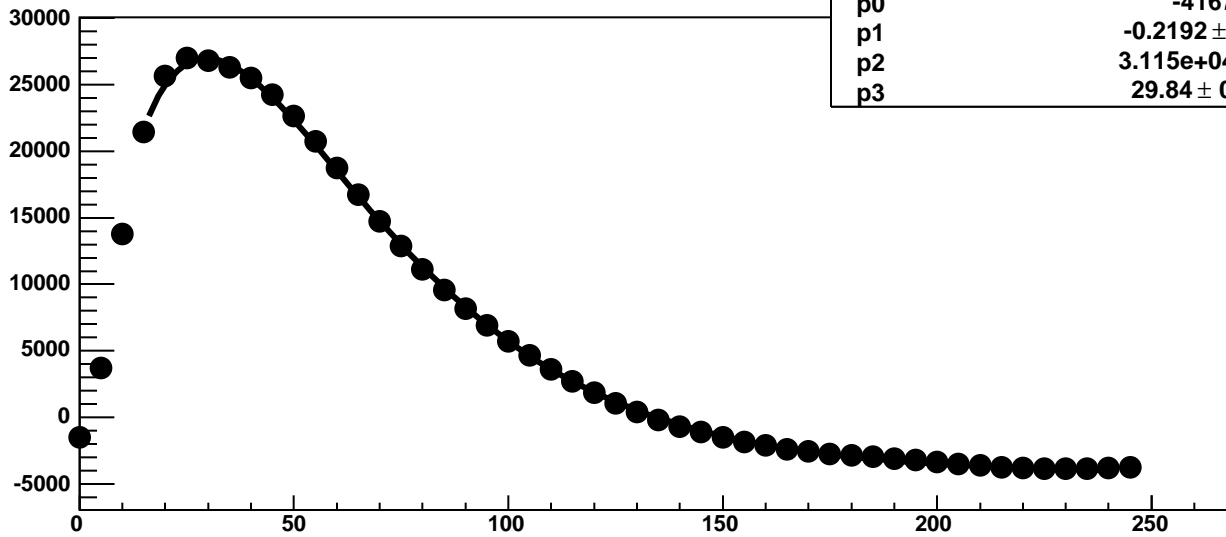
Chip 1, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



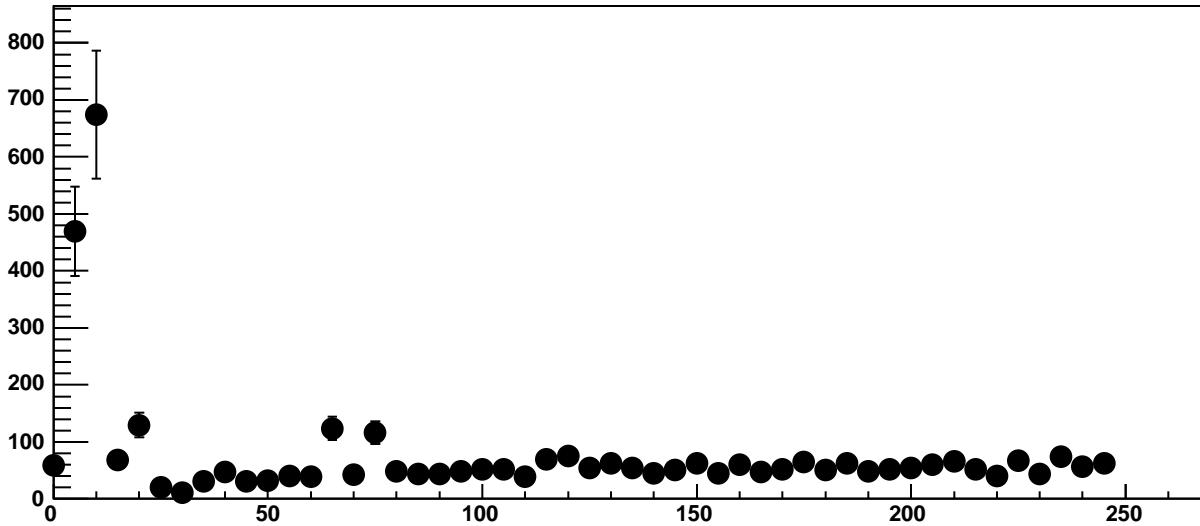
Chip 1, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



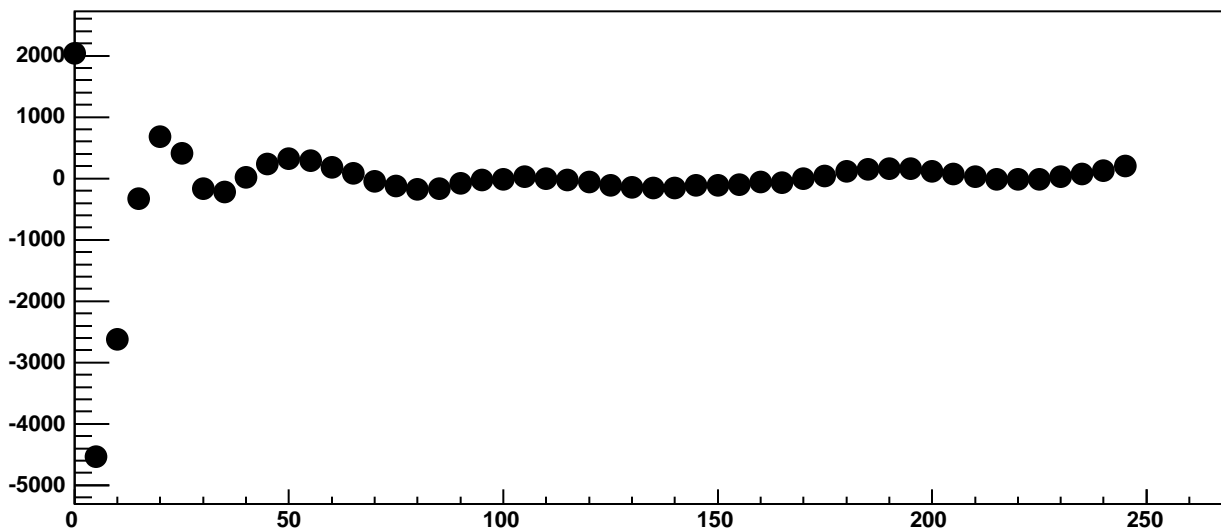
Chip 1, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold



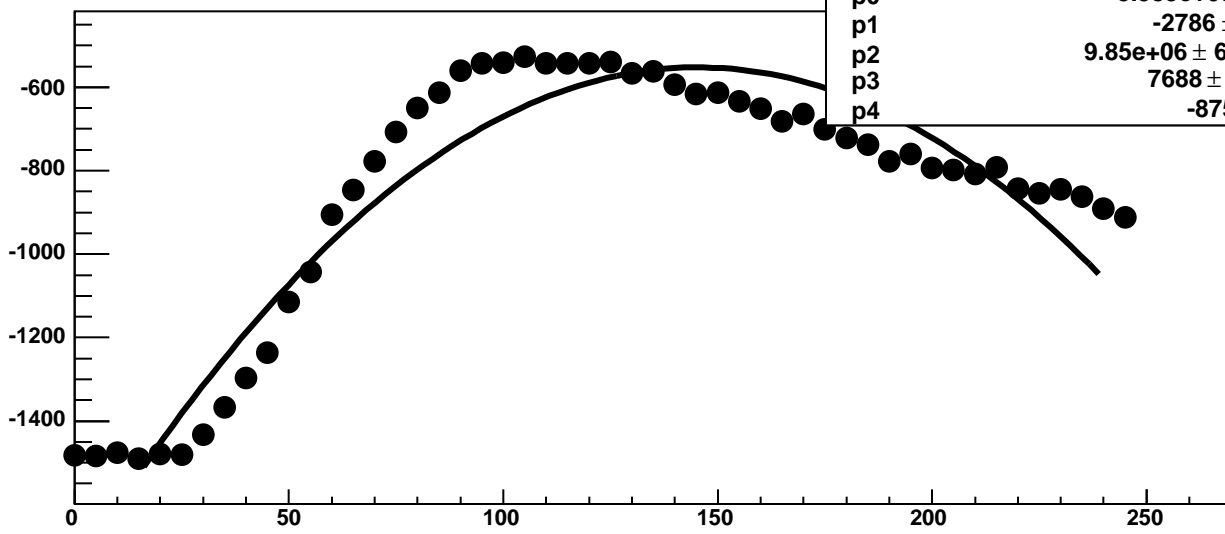
Chip 1, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold

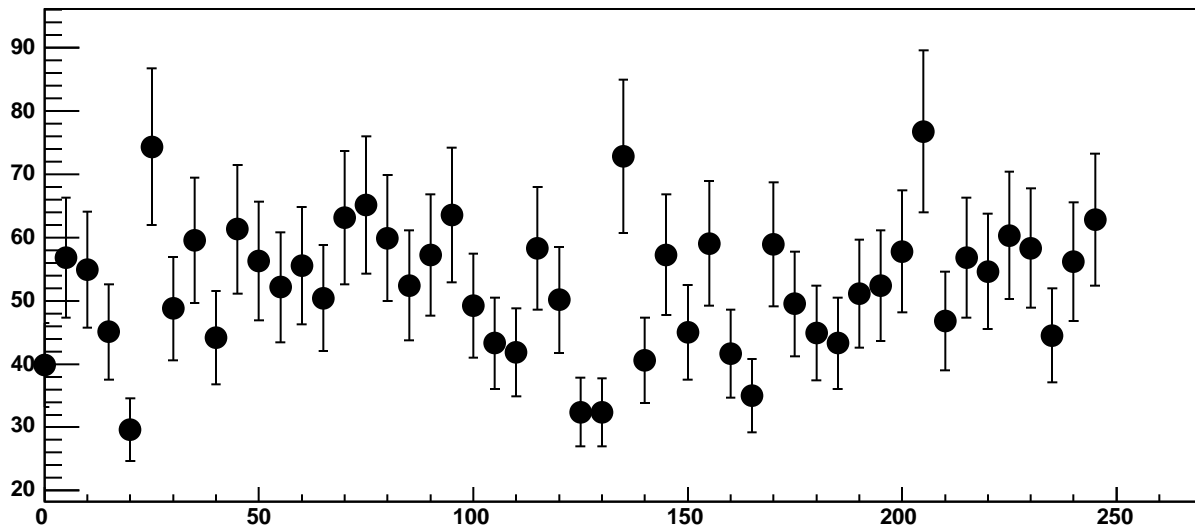


Chip 1, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

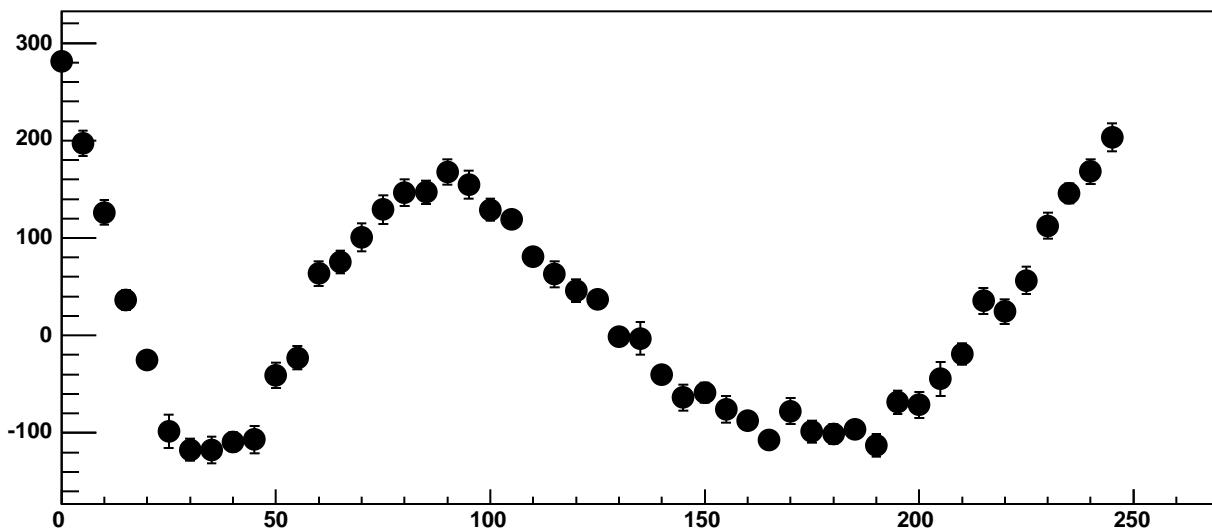


$\chi^2 / \text{ndf}$	2876 / 41
p0	$-5.583\text{e}+05 \pm 3911$
p1	$-2786 \pm 0.2438$
p2	$9.85\text{e}+06 \pm 6.95\text{e}+04$
p3	$7688 \pm 0.02264$
p4	$-875 \pm 6.18$

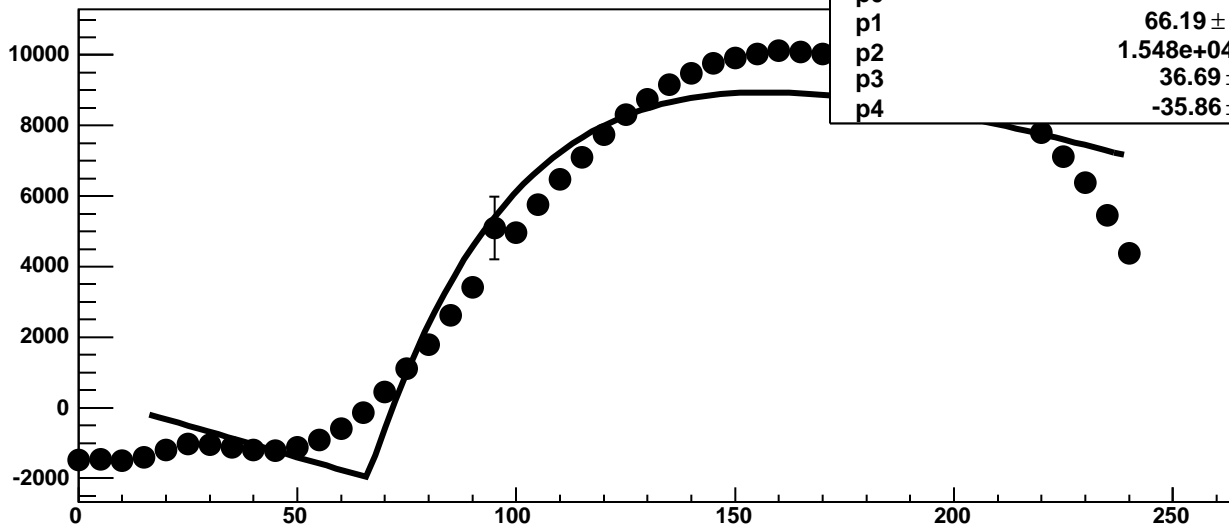
Chip 1, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

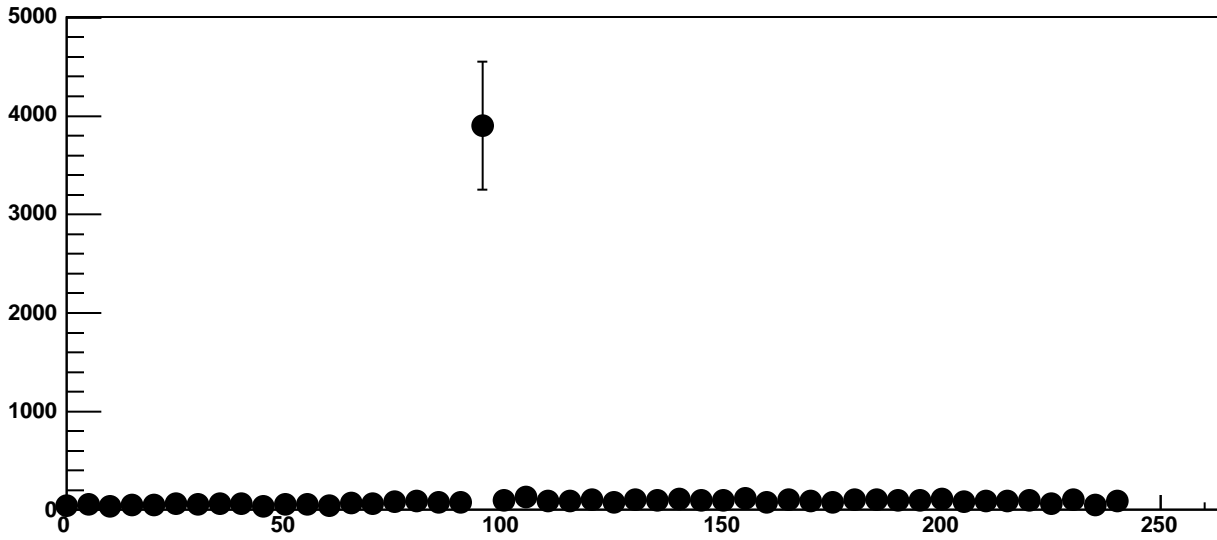


Chip 1, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

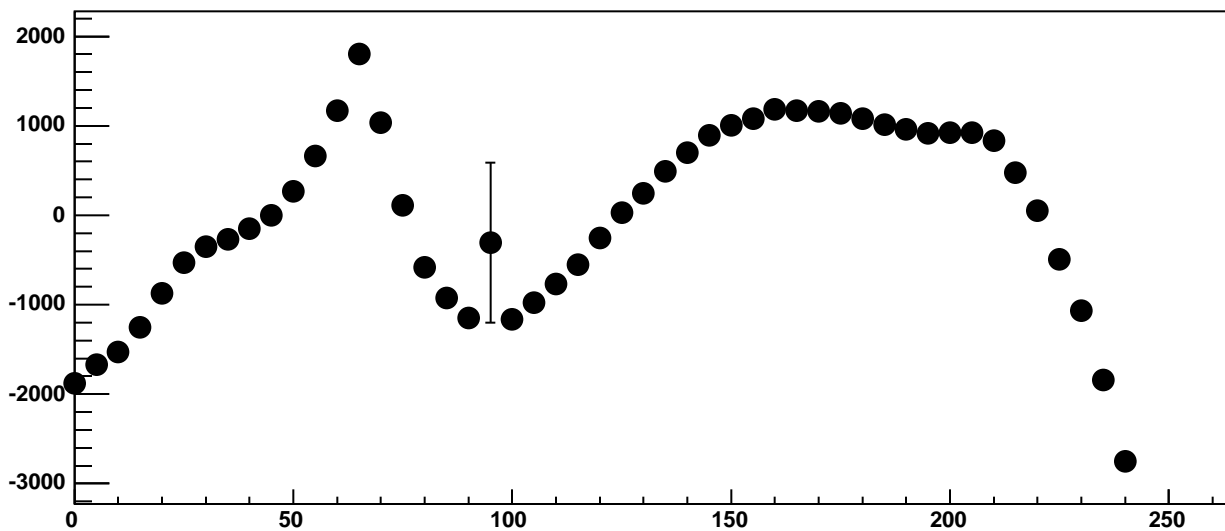


$\chi^2 / \text{ndf}$	1.506e+05 / 41
p0	-1982 ± 5.004
p1	66.19 ± 0.03455
p2	1.548e+04 ± 28.41
p3	36.69 ± 0.0898
p4	-35.86 ± 0.1513

Chip 1, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

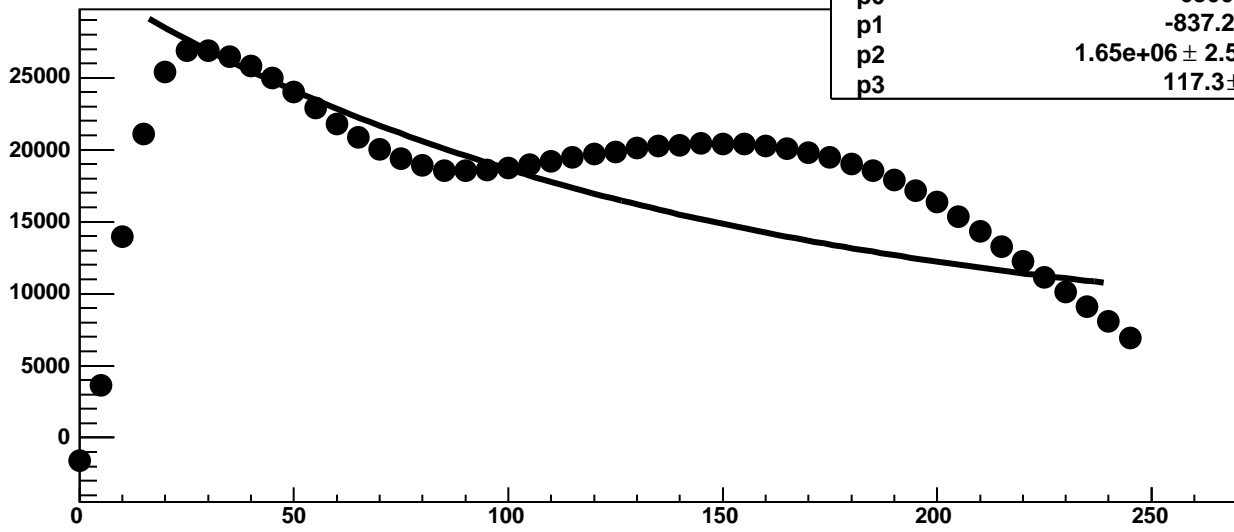


Chip 1, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold



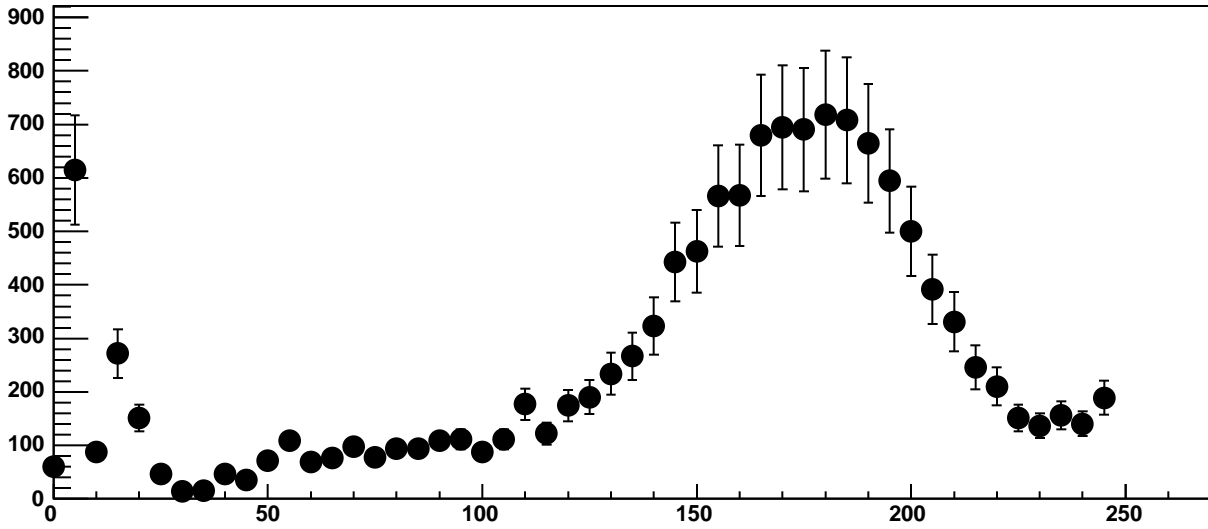


Chip 1, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold

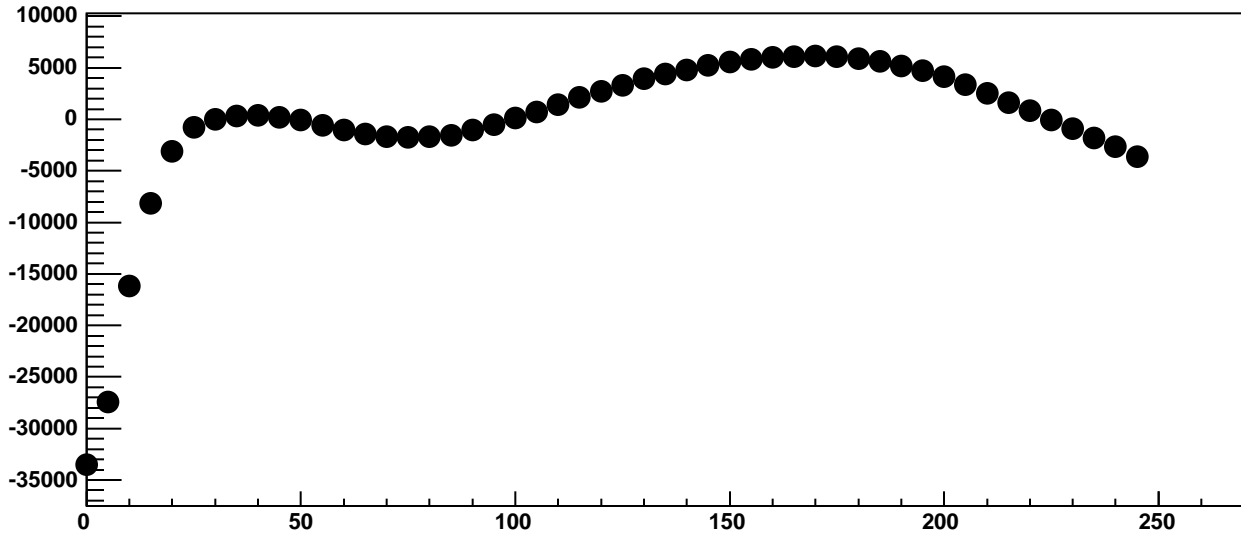


$\chi^2 / \text{ndf}$	1.449e+05 / 42
p0	6500 ± 44.74
p1	-837.2 ± 3.953
p2	1.65e+06 ± 2.502e+04
p3	117.3 ± 0.4077

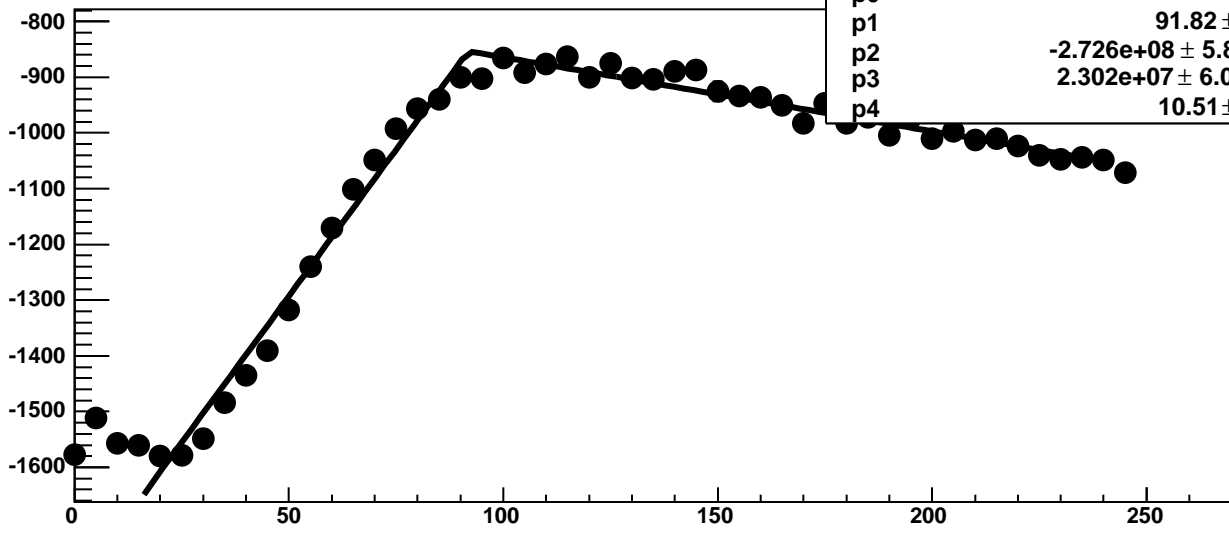
Chip 1, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold

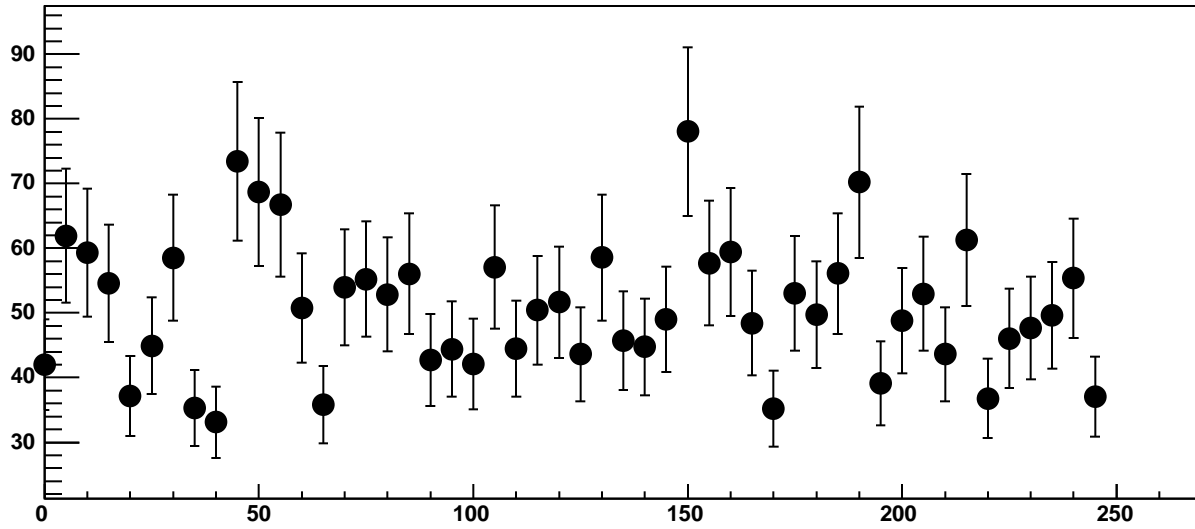


Chip 1, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

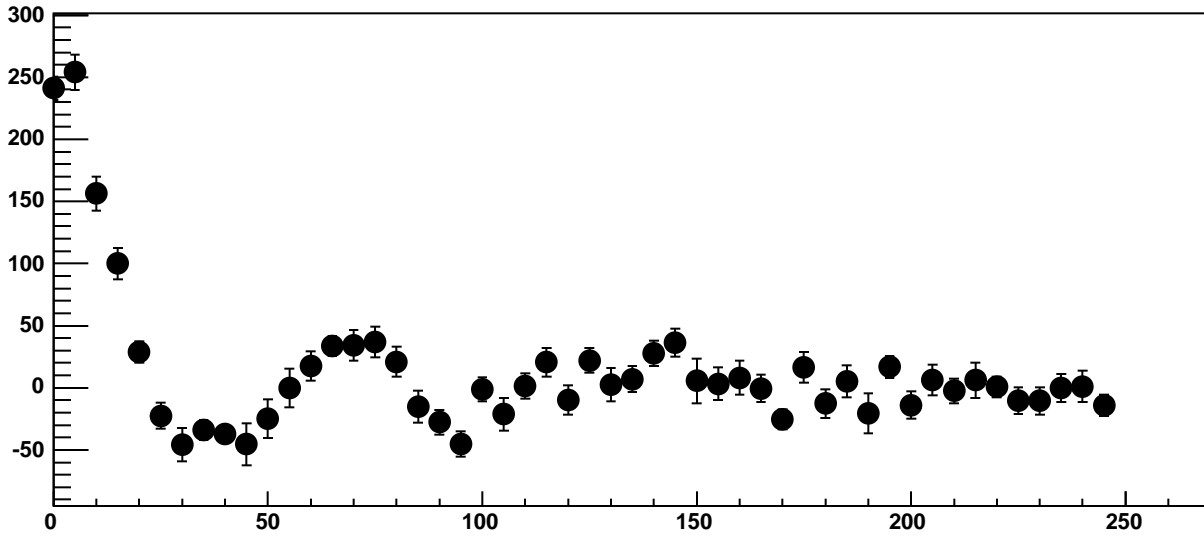


$\chi^2 / \text{ndf}$	263.5 / 41
p0	-853 ± 3.615
p1	91.82 ± 0.5103
p2	-2.726e+08 ± 5.849e+06
p3	2.302e+07 ± 6.071e+05
p4	10.51 ± 0.1033

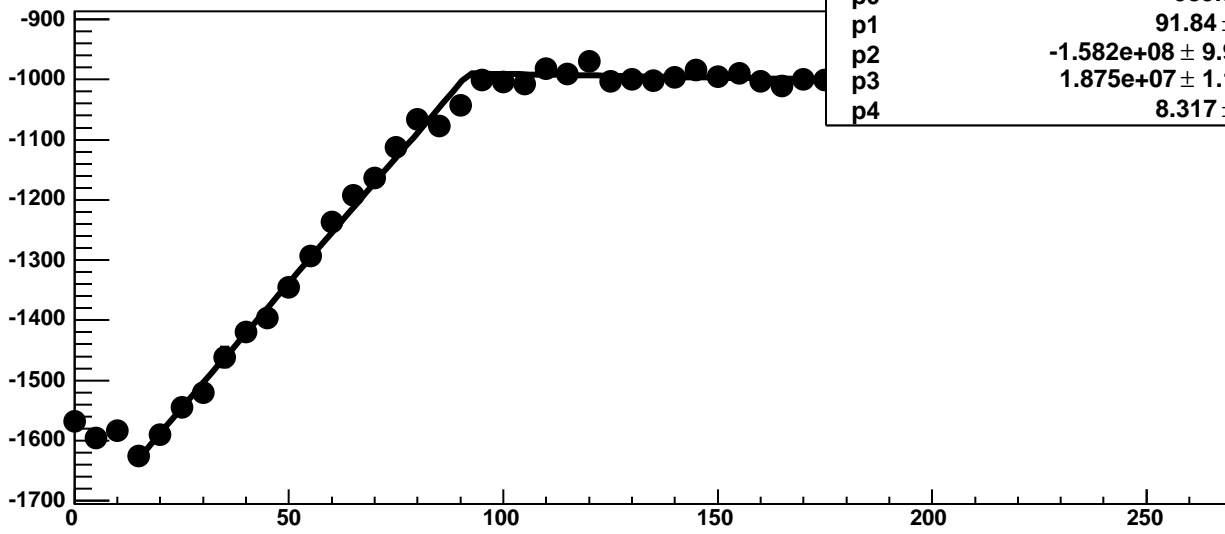
Chip 1, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

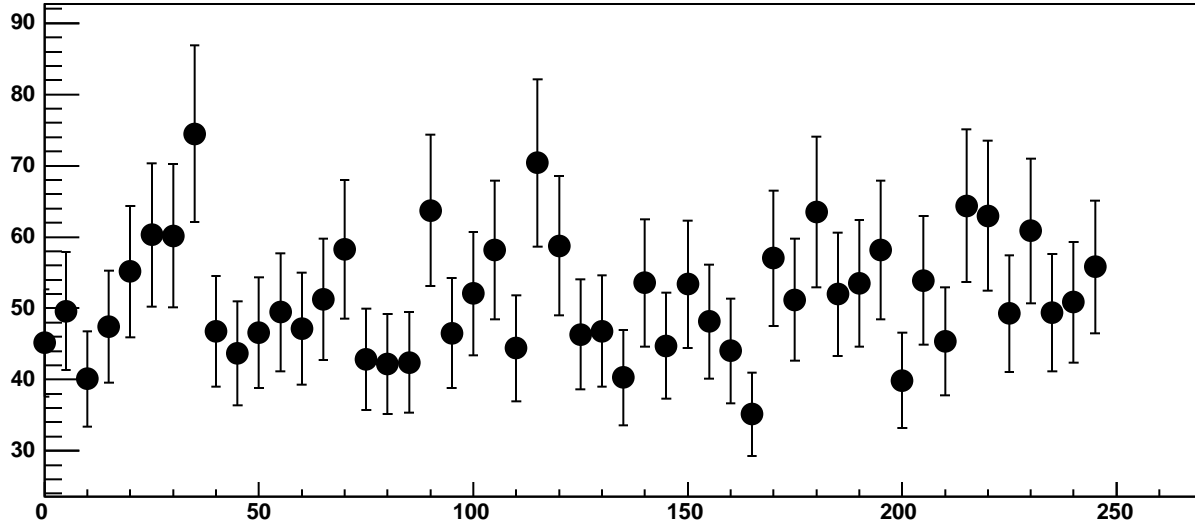


Chip 1, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

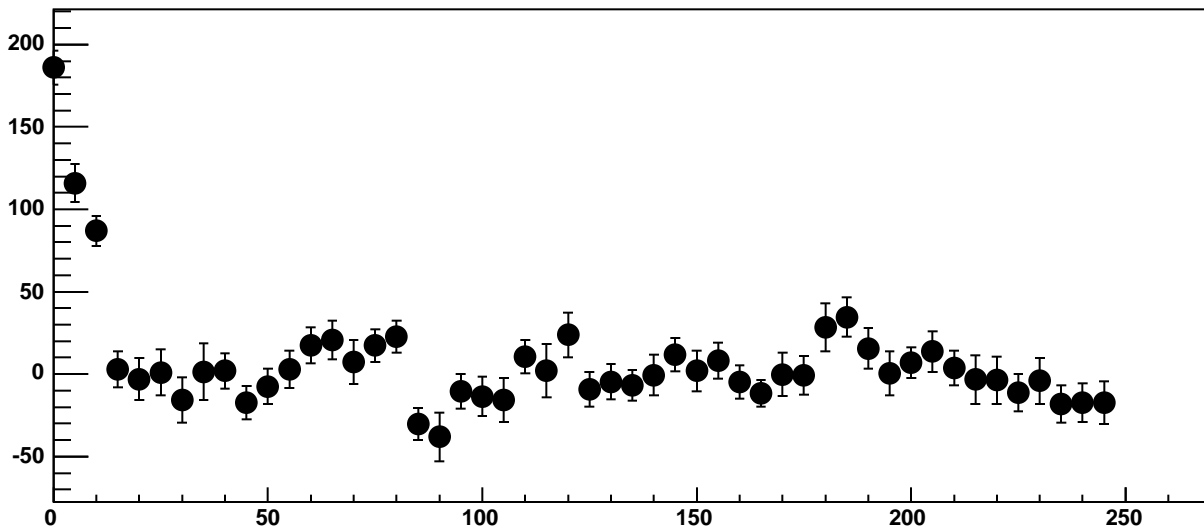


$\chi^2 / \text{ndf}$	71.38 / 41
p0	$-989.8 \pm 4.211$
p1	$91.84 \pm 0.8427$
p2	$-1.582\text{e}+08 \pm 9.973\text{e}+06$
p3	$1.875\text{e}+07 \pm 1.171\text{e}+06$
p4	$8.317 \pm 0.1283$

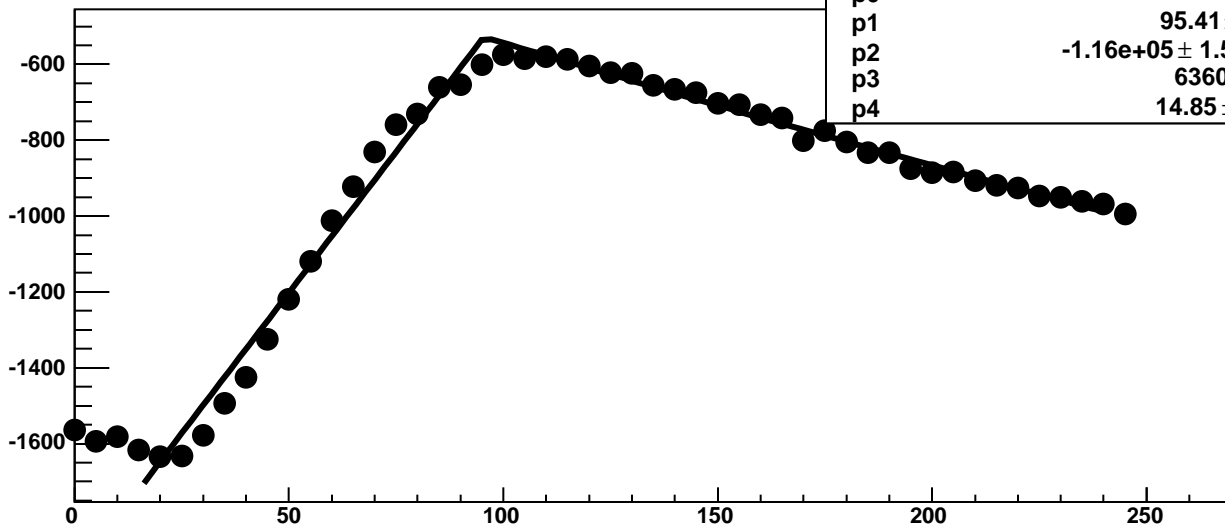
Chip 1, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

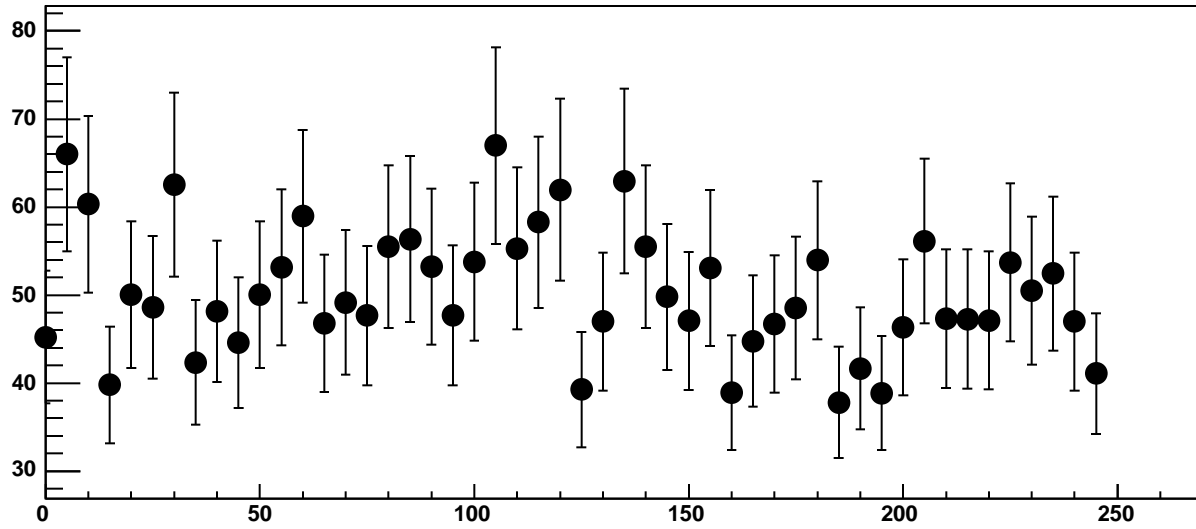


Chip 1, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold

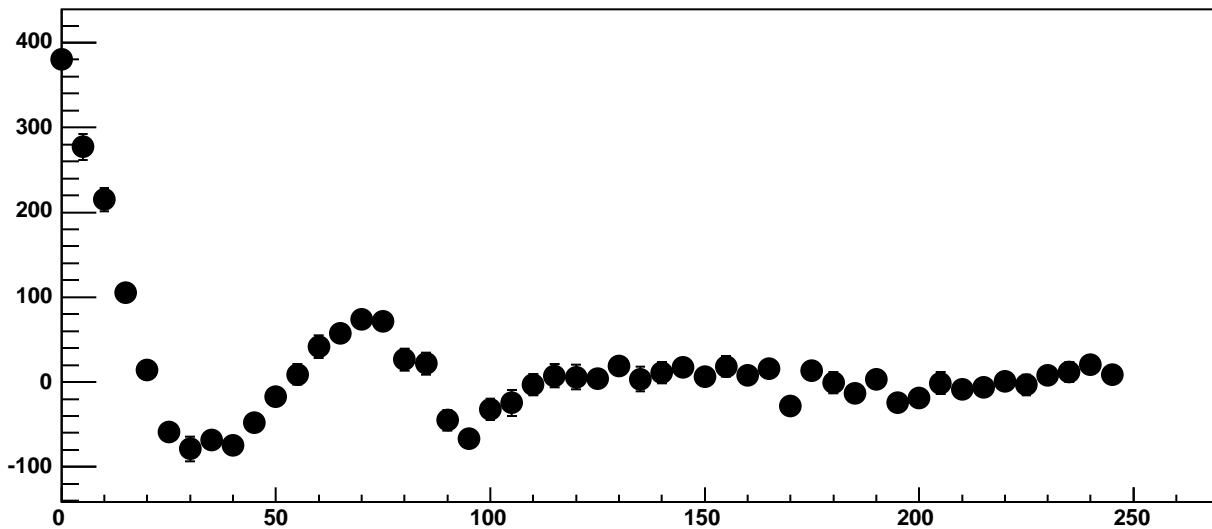


$\chi^2 / \text{ndf}$	544.7 / 41
p0	-527.6 ± 3.949
p1	95.41 ± 0.3911
p2	-1.16e+05 ± 1.585e+04
p3	6360 ± 878.9
p4	14.85 ± 0.1102

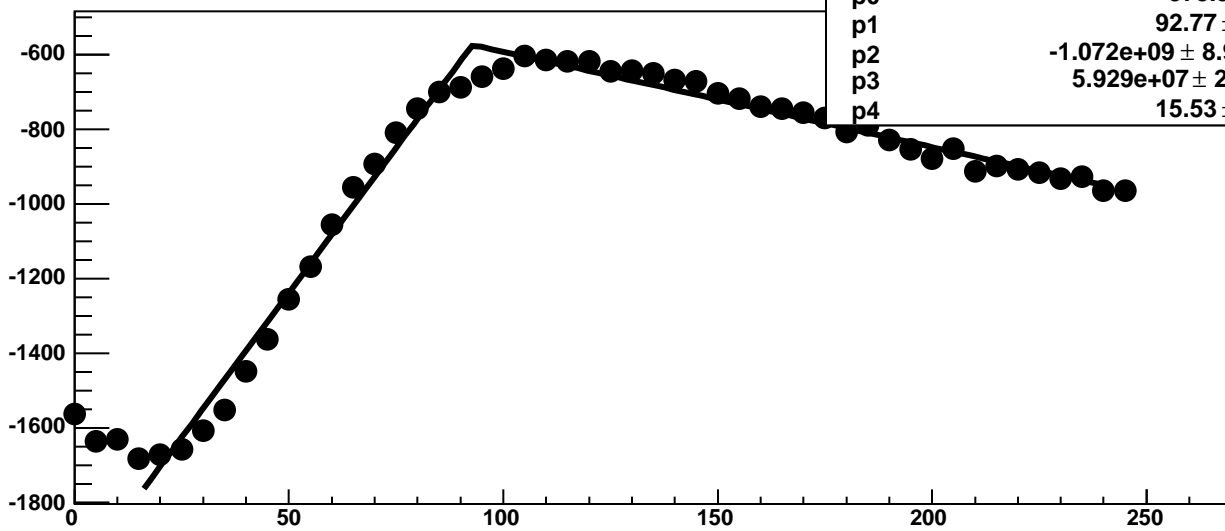
Chip 1, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold

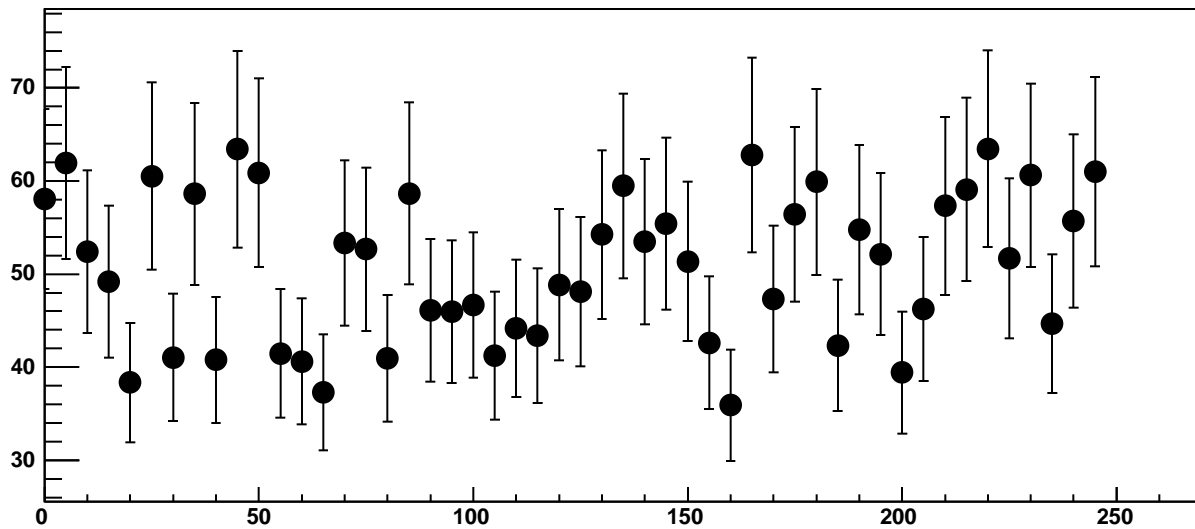


Chip 1, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

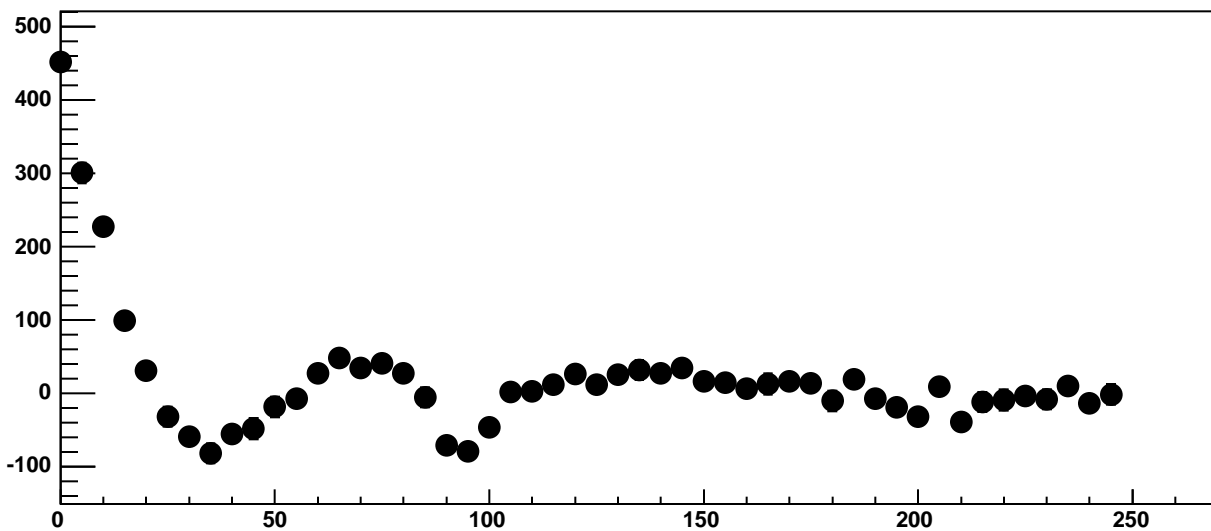


$\chi^2 / \text{ndf}$	481 / 41
p0	$-573.3 \pm 3.473$
p1	$92.77 \pm 0.3697$
p2	$-1.072\text{e}+09 \pm 8.907\text{e}+06$
p3	$5.929\text{e}+07 \pm 2.92\text{e}+05$
p4	$15.53 \pm 0.1163$

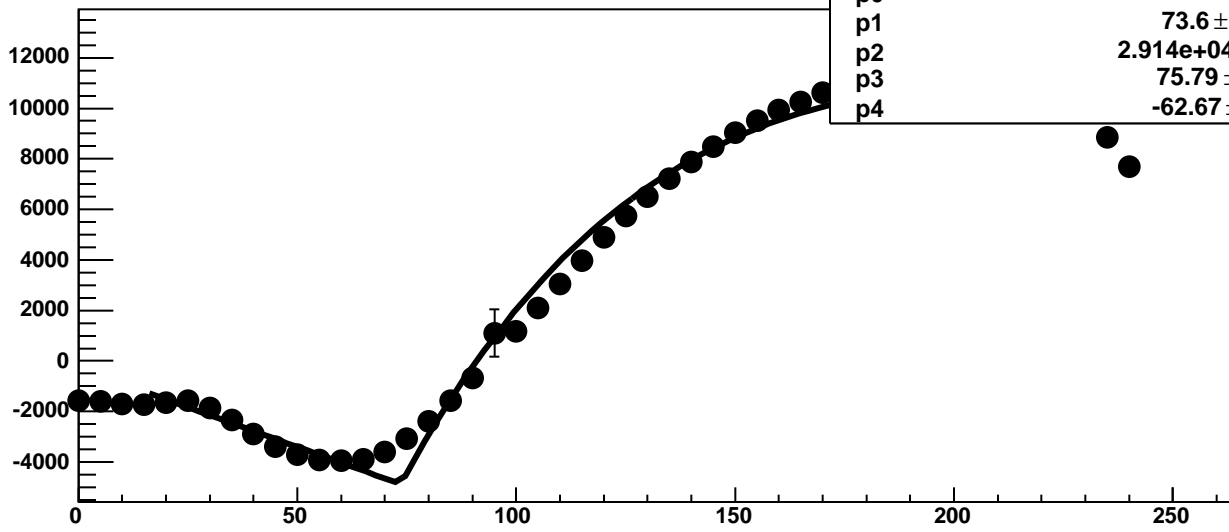
Chip 1, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

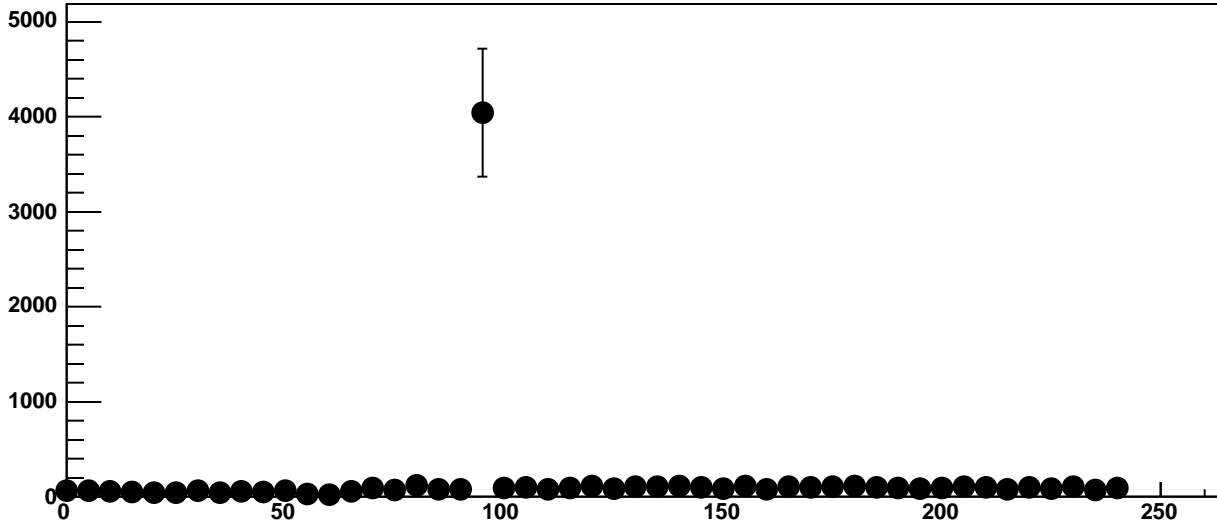


Chip 1, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

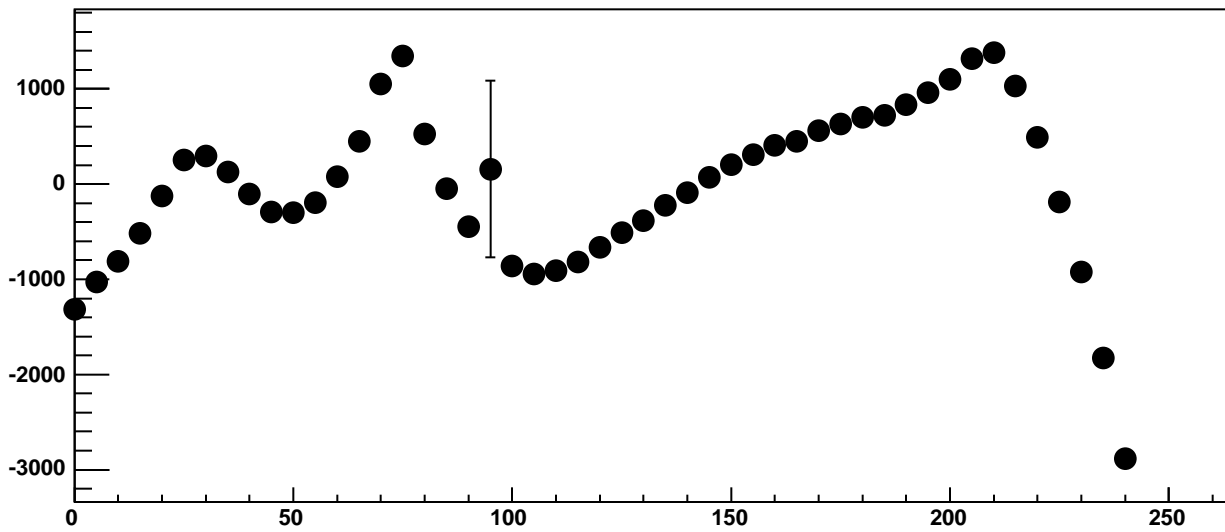


$\chi^2 / \text{ndf}$	7.494e+04 / 41
p0	-4877 ± 5.391
p1	73.6 ± 0.03591
p2	2.914e+04 ± 50.31
p3	75.79 ± 0.1576
p4	-62.67 ± 0.1803

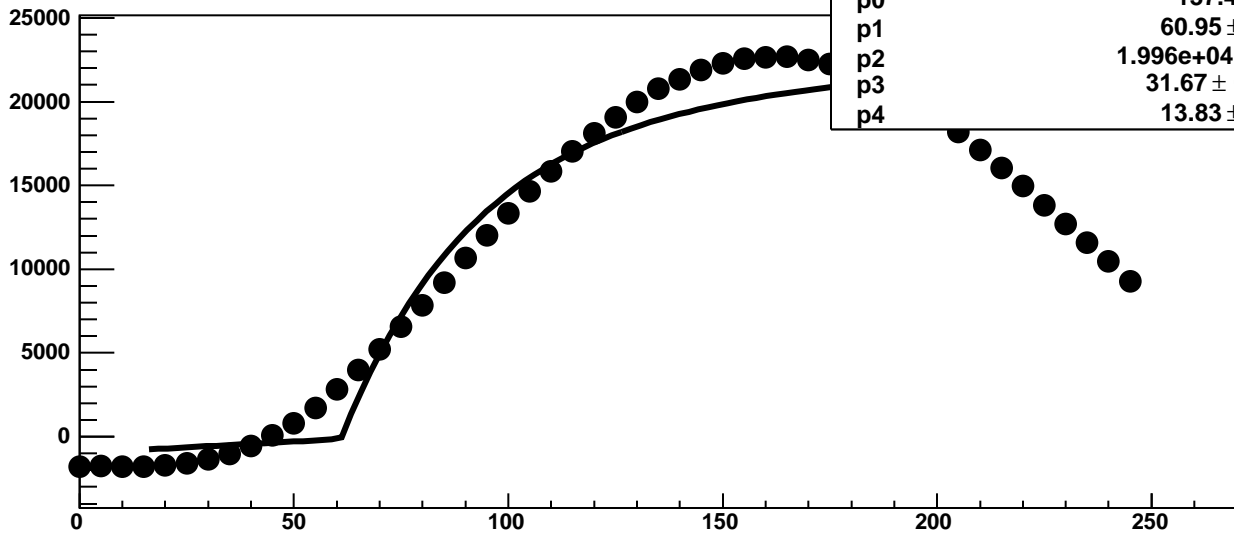
Chip 1, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

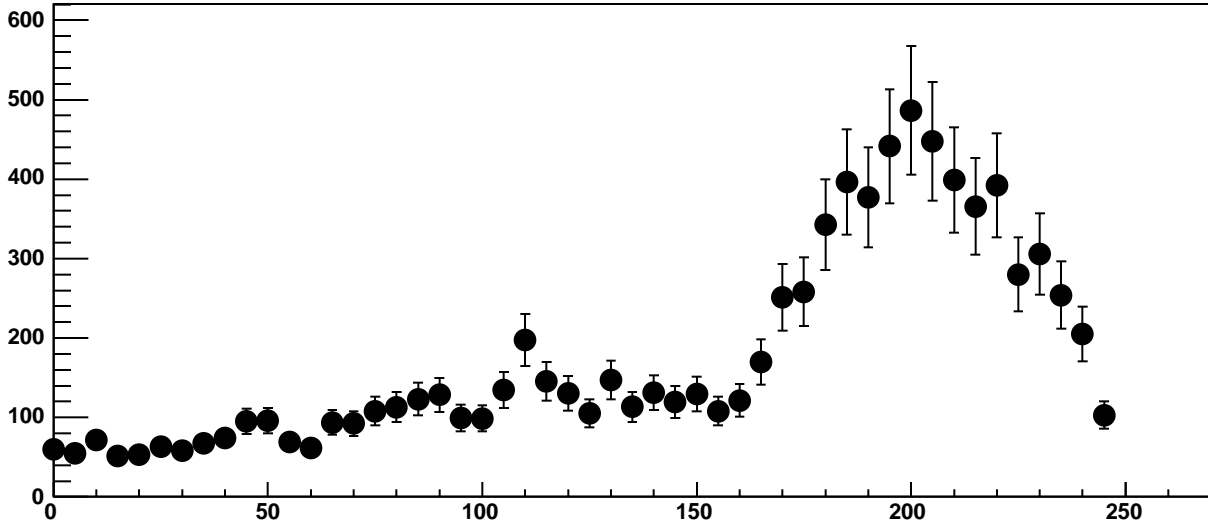


Chip 1, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold

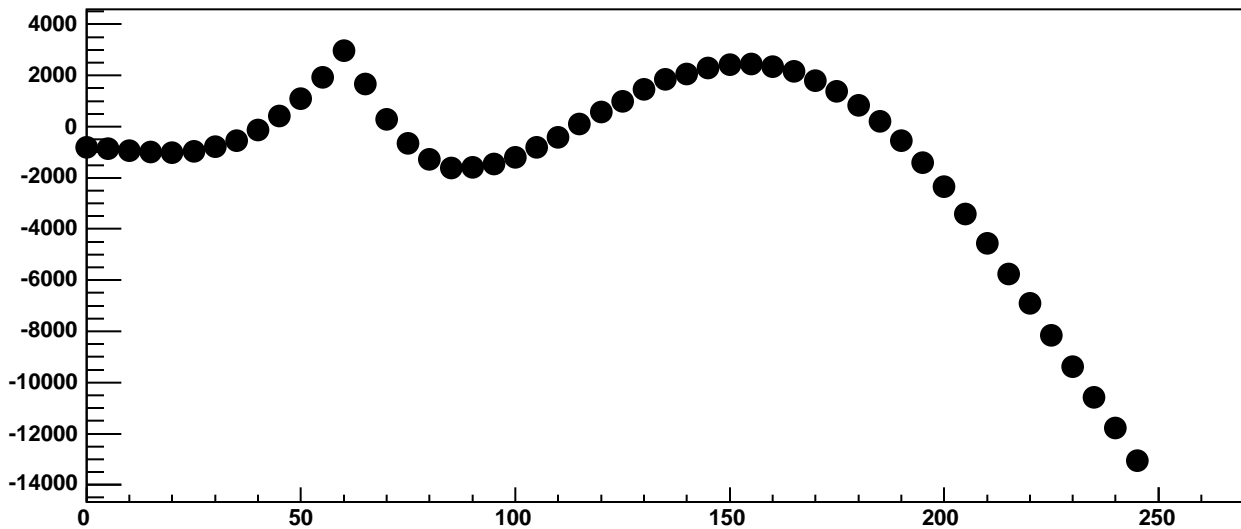


$\chi^2 / \text{ndf}$	3.016e+05 / 41
p0	-137.4 ± 7.871
p1	60.95 ± 0.0333
p2	1.996e+04 ± 35.12
p3	31.67 ± 0.07532
p4	13.83 ± 0.2263

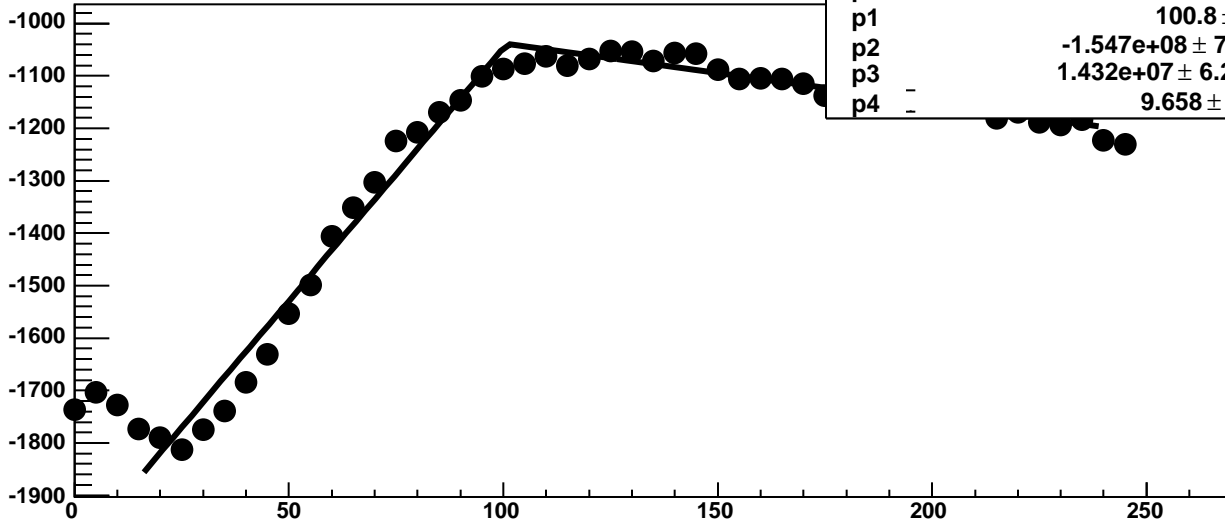
Chip 1, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

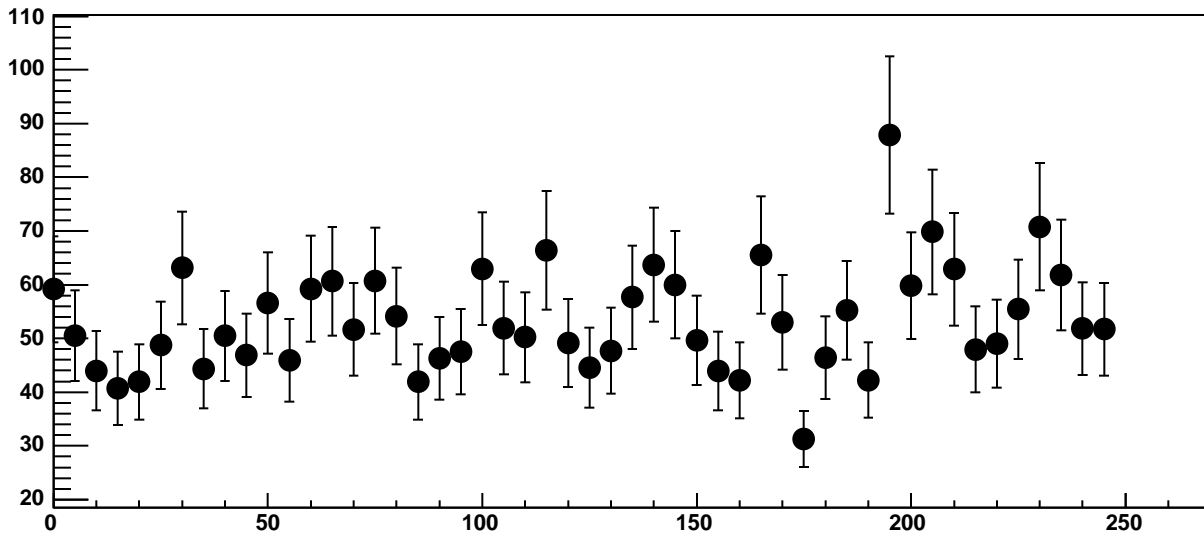


Chip 1, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

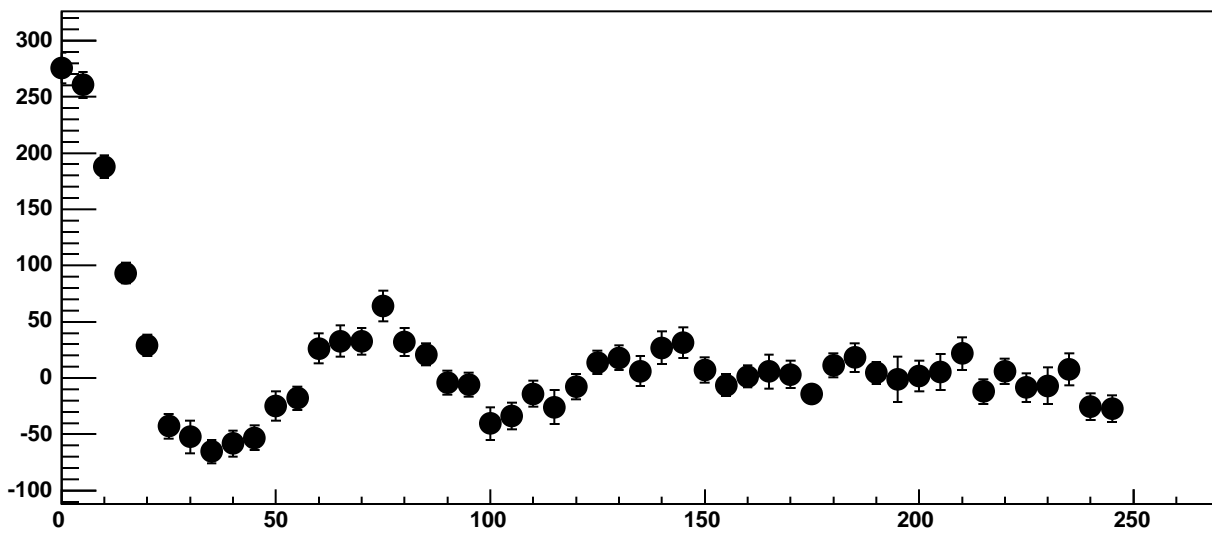


$\chi^2 / \text{ndf}$	337 / 41
p0	-1038 ± 4.168
p1	100.8 ± 0.6399
p2	-1.547e+08 ± 7.14e+06
p3	1.432e+07 ± 6.245e+05
p4	-
	9.658 ± 0.09953

Chip 1, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

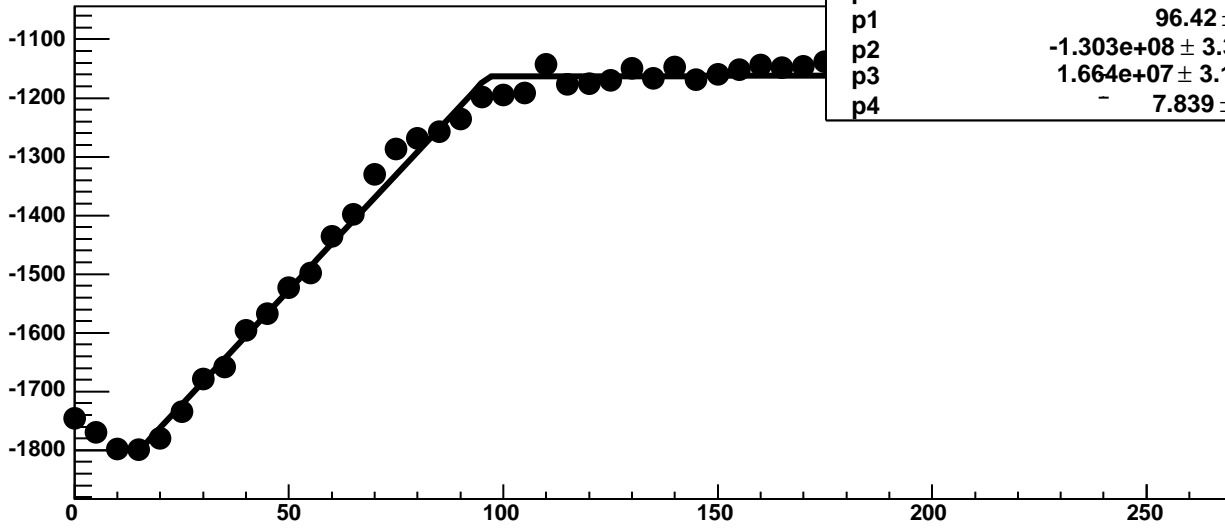


Chip 1, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



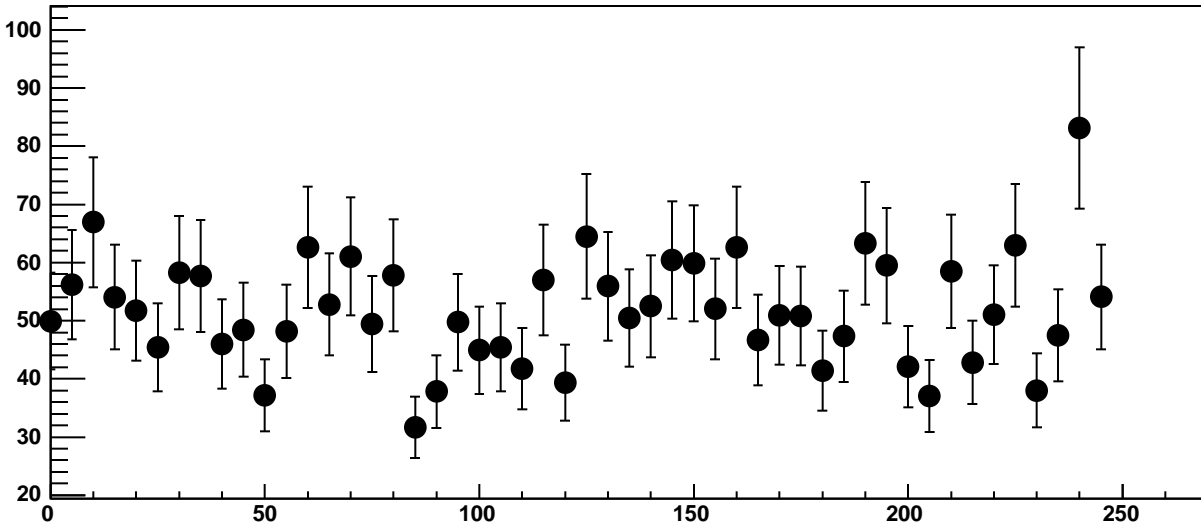


Chip 1, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

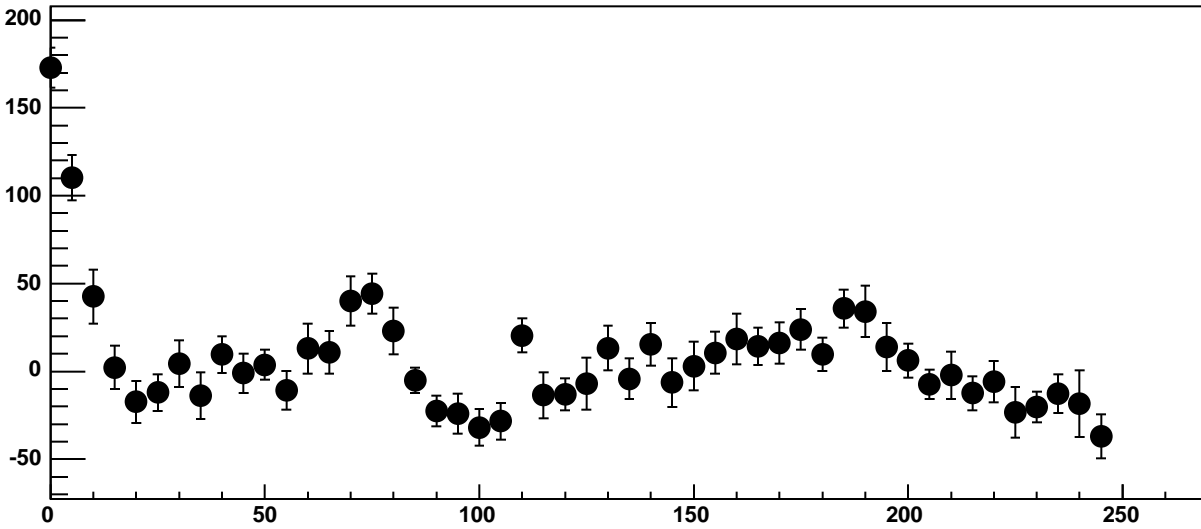


$\chi^2 / \text{ndf}$	116.4 / 41
p0	-1163 ± 4.25
p1	96.42 ± 0.8209
p2	-1.303e+08 ± 3.321e+06
p3	1.664e+07 ± 3.187e+05
p4	- 7.839 ± 0.1065

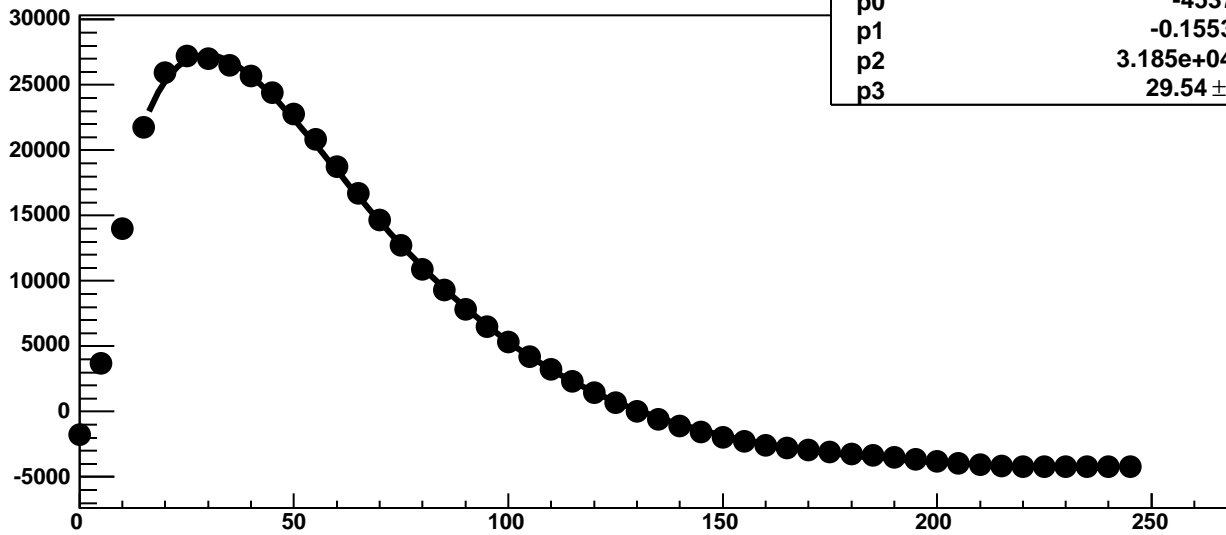
Chip 1, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

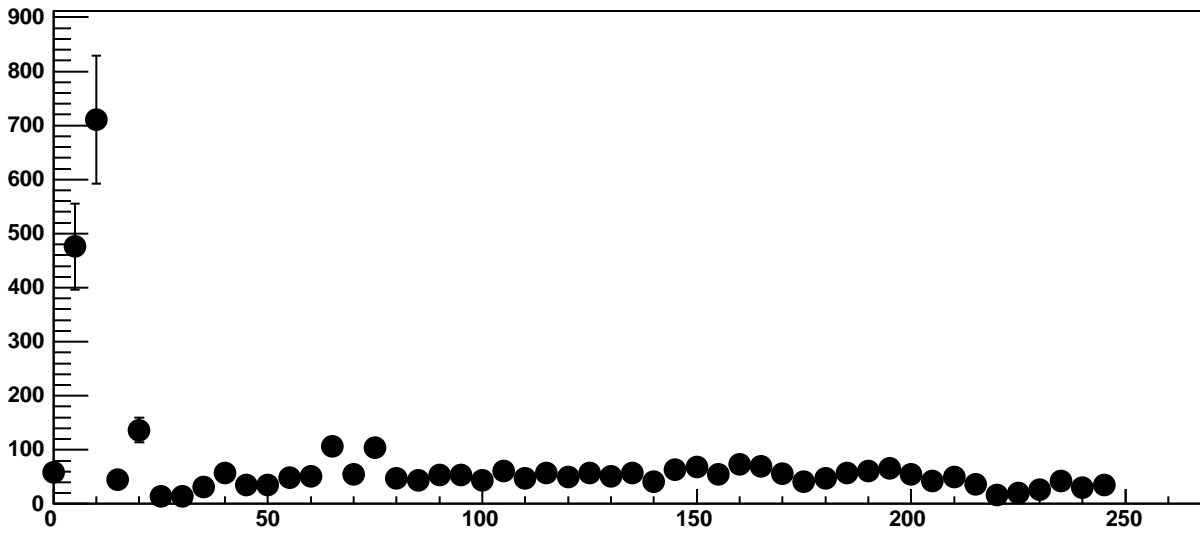


Chip 1, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

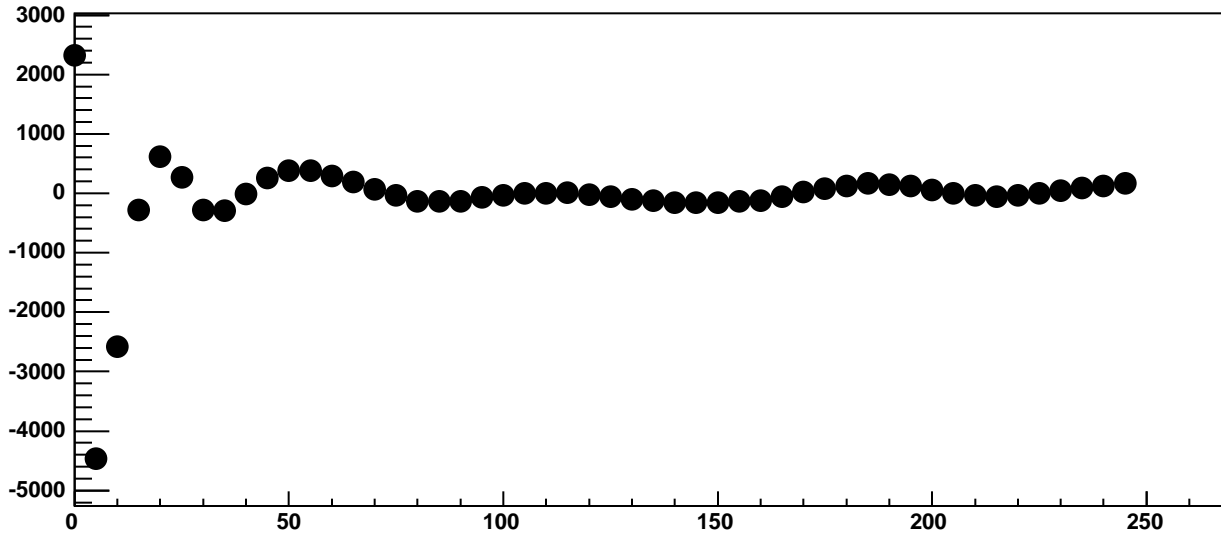


$\chi^2 / \text{ndf}$	2.436e+04 / 42
p0	-4537 $\pm$ 2.229
p1	-0.1553 $\pm$ 0.013
p2	3.185e+04 $\pm$ 2.857
p3	29.54 $\pm$ 0.00778

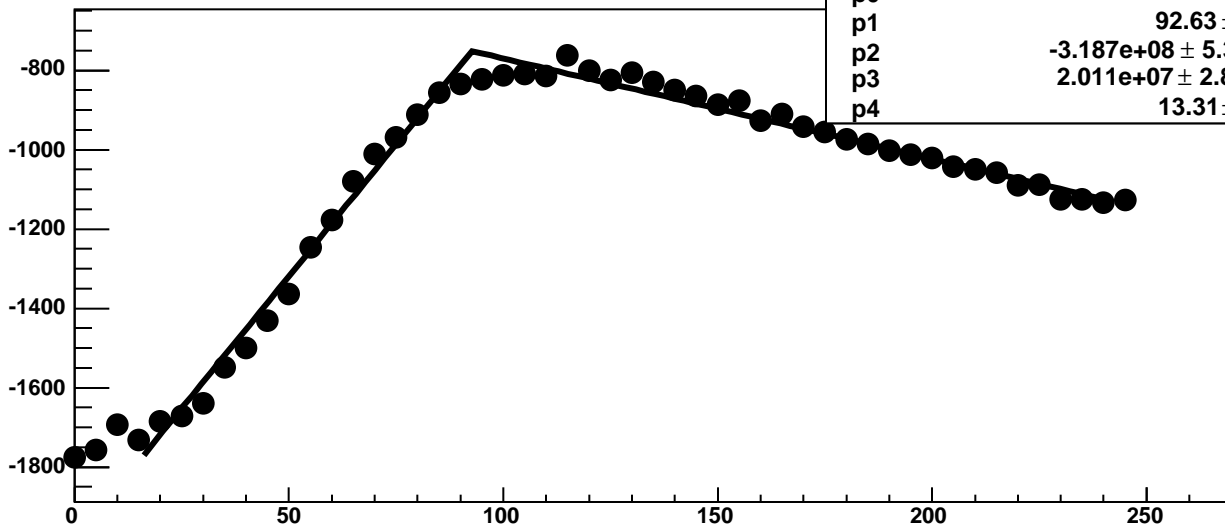
Chip 1, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold

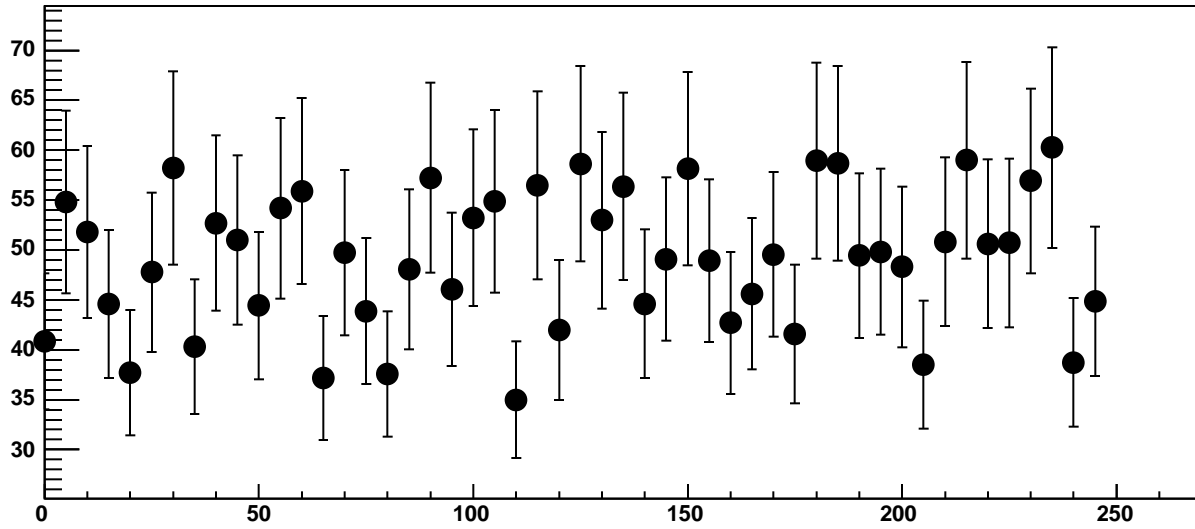


Chip 1, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

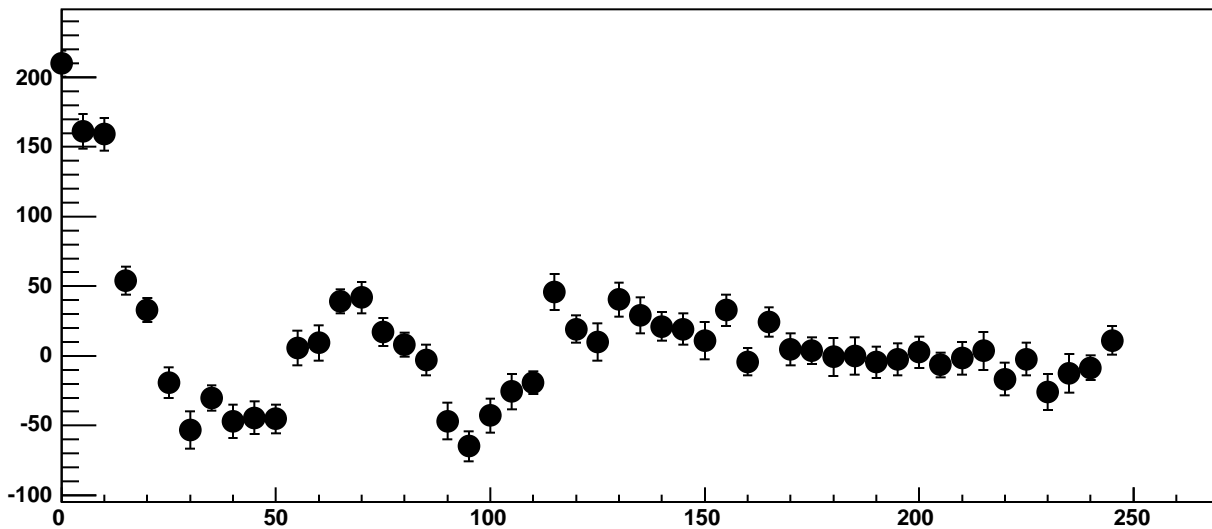


$\chi^2 / \text{ndf}$	297.6 / 41
p0	$-751.4 \pm 3.488$
p1	$92.63 \pm 0.4192$
p2	$-3.187\text{e}+08 \pm 5.307\text{e}+06$
p3	$2.011\text{e}+07 \pm 2.856\text{e}+05$
p4	$13.31 \pm 0.1128$

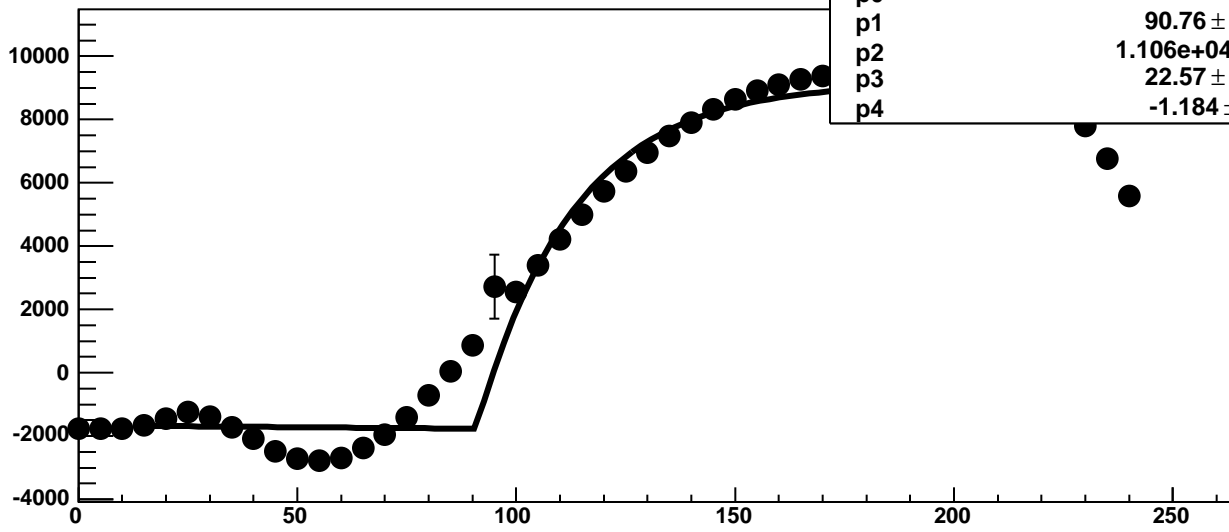
Chip 1, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

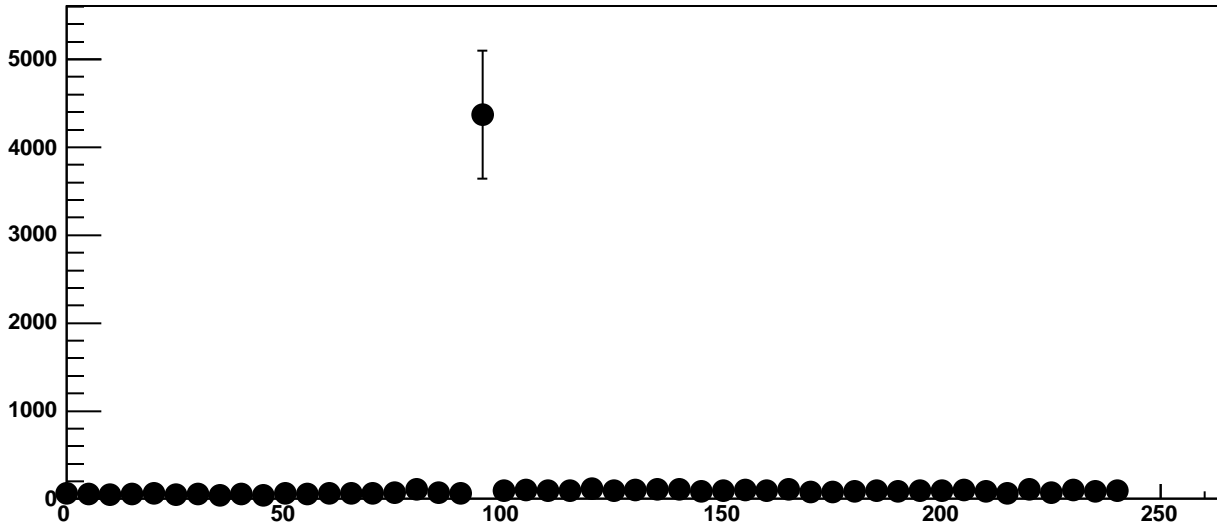


Chip 1, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

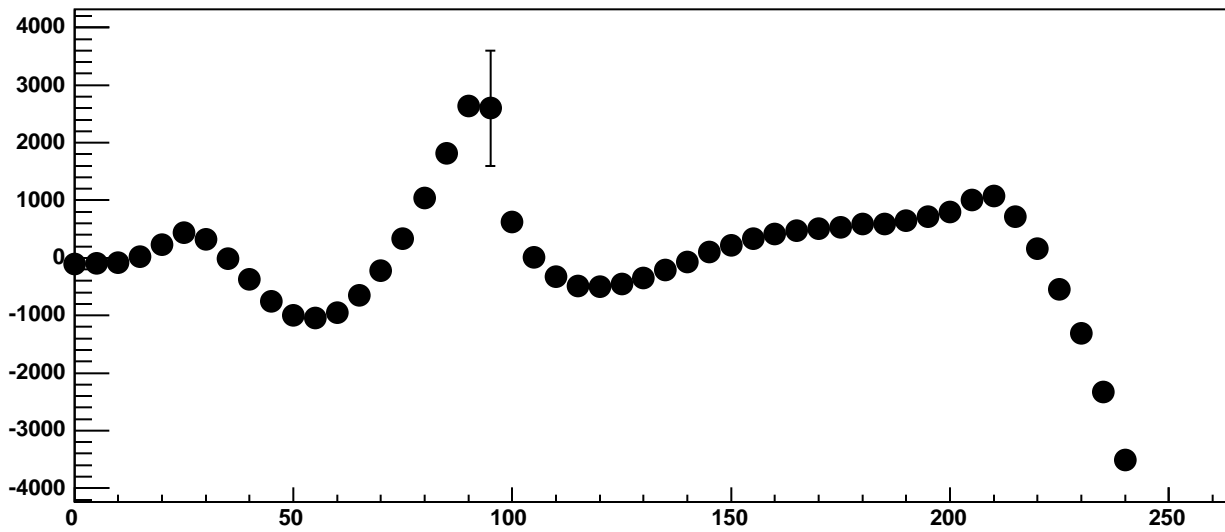


$\chi^2 / \text{ndf}$	1.346e+05 / 41
p0	-1767 ± 6.513
p1	90.76 ± 0.07509
p2	1.106e+04 ± 21.64
p3	22.57 ± 0.09958
p4	-1.184 ± 0.1285

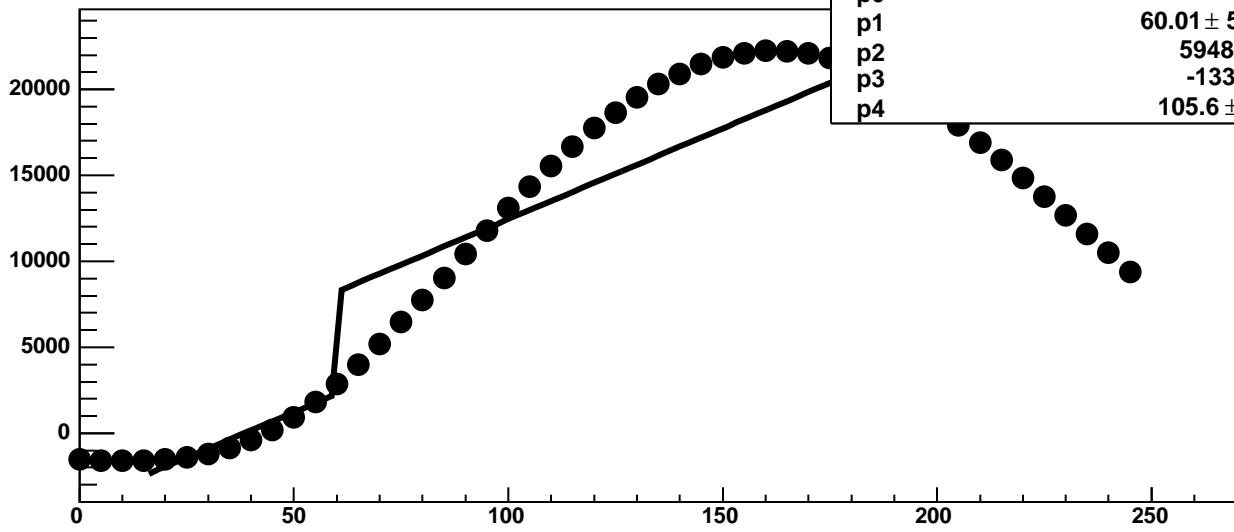
Chip 1, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

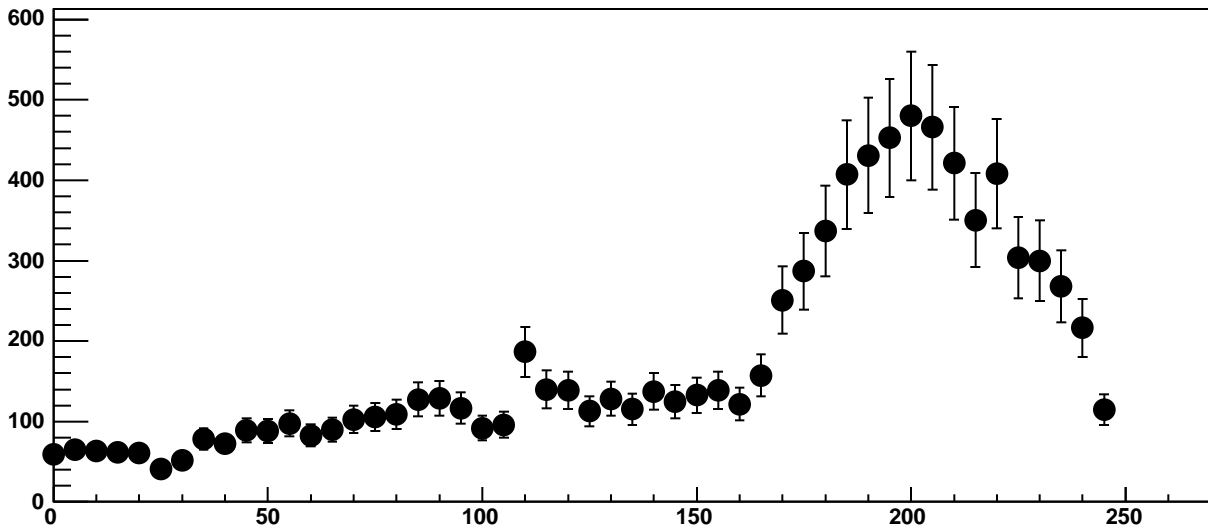


Chip 1, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

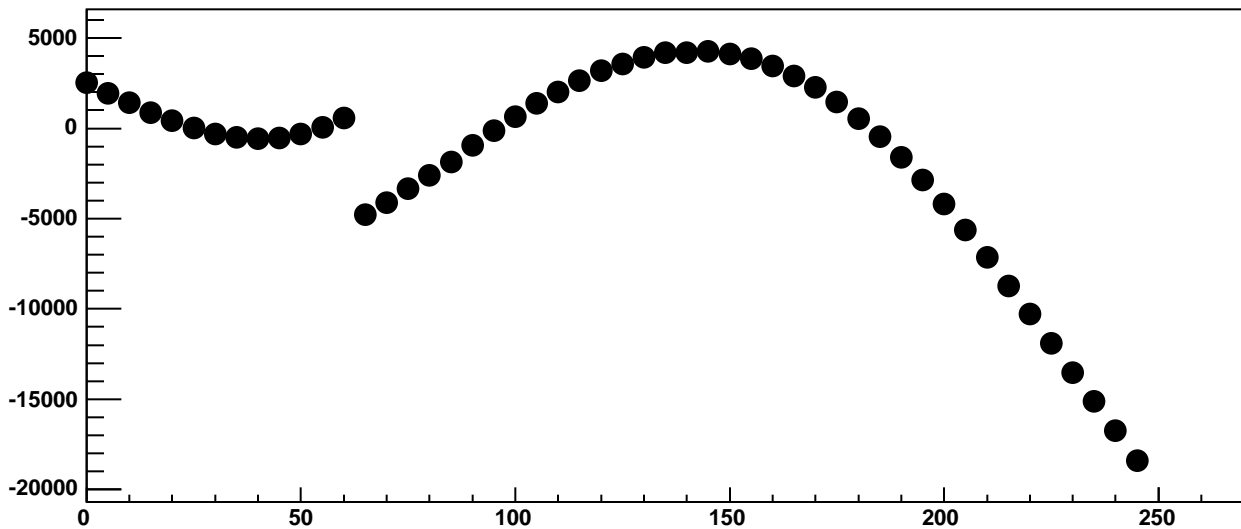


$\chi^2 / \text{ndf}$	5.875e+05 / 41
p0	2279 ± 32.76
p1	60.01 ± 5.25e-05
p2	5948 ± 42.99
p3	-133 ± 11.37
p4	105.6 ± 0.7095

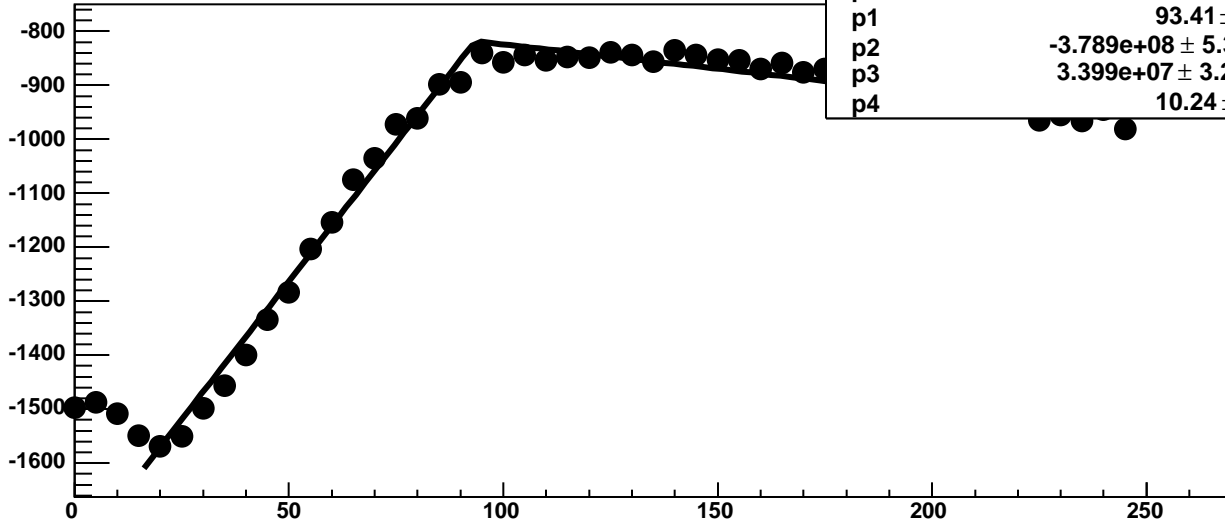
Chip 1, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

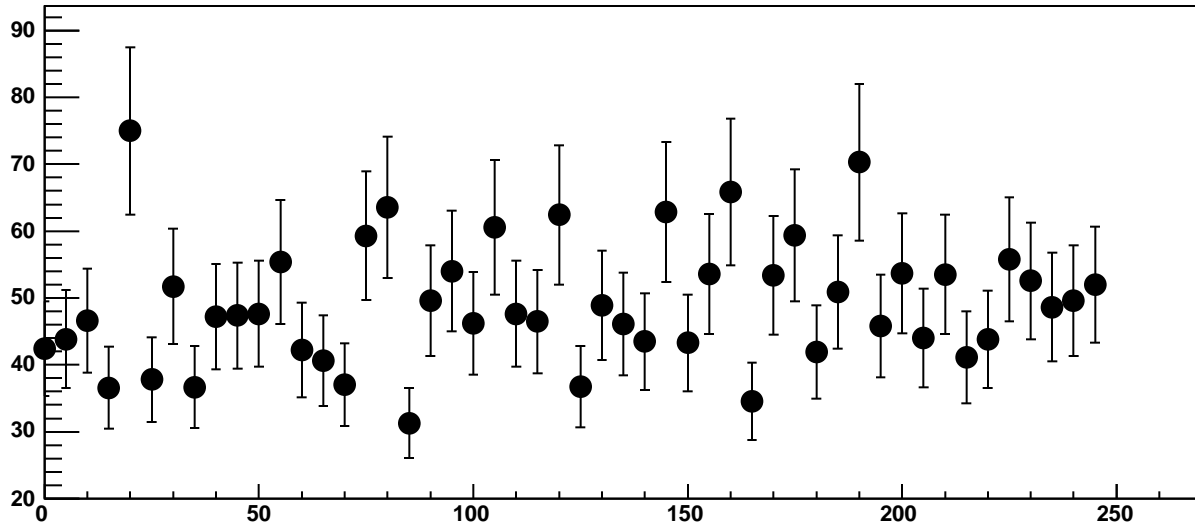


Chip 1, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

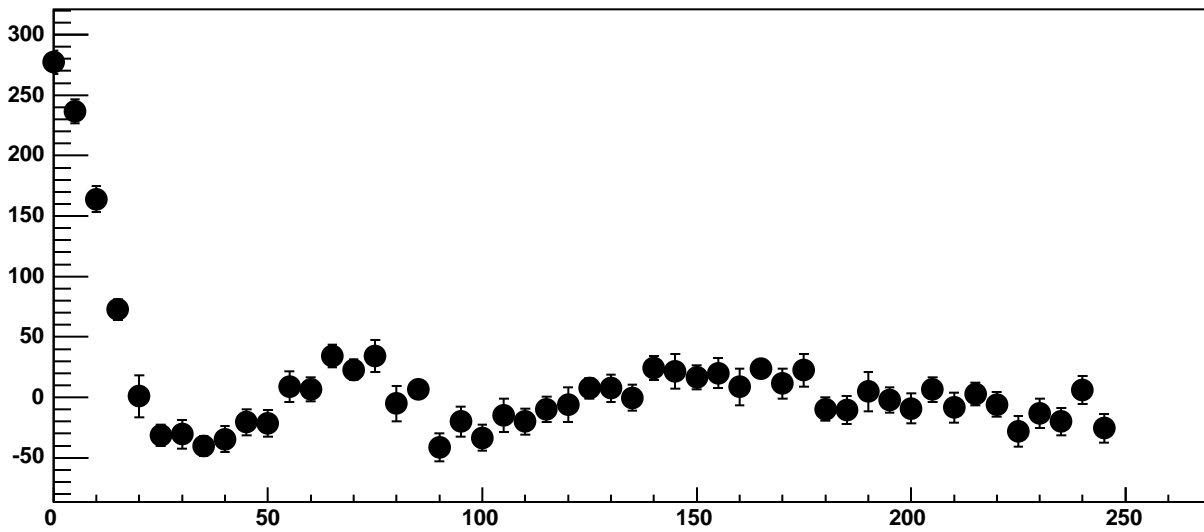


$\chi^2 / \text{ndf}$	236.5 / 41
p0	-818.2 ± 3.765
p1	93.41 ± 0.5796
p2	-3.789e+08 ± 5.388e+06
p3	3.399e+07 ± 3.234e+05
p4	10.24 ± 0.1067

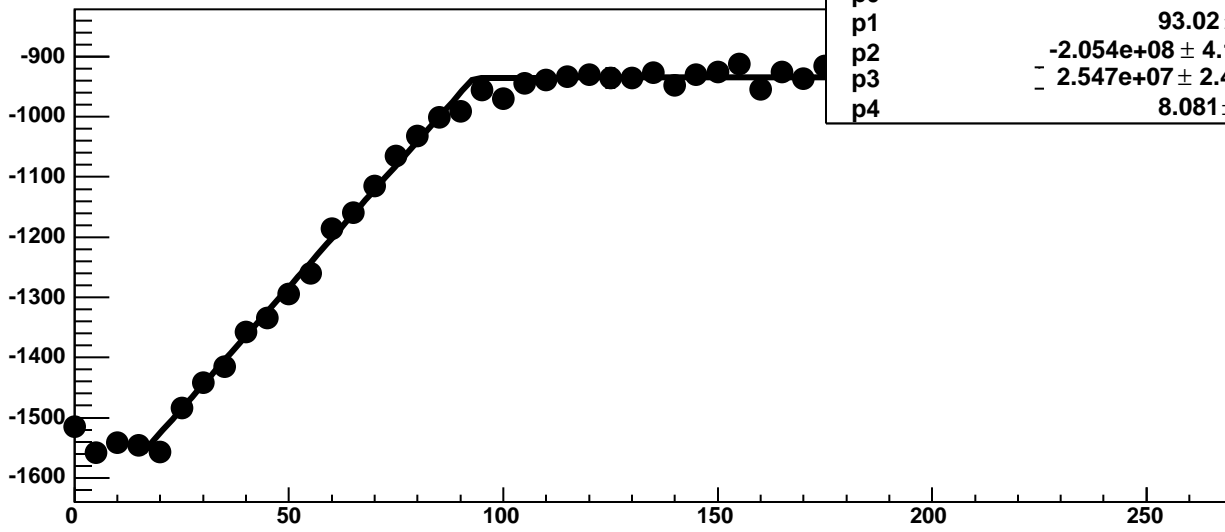
Chip 1, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold

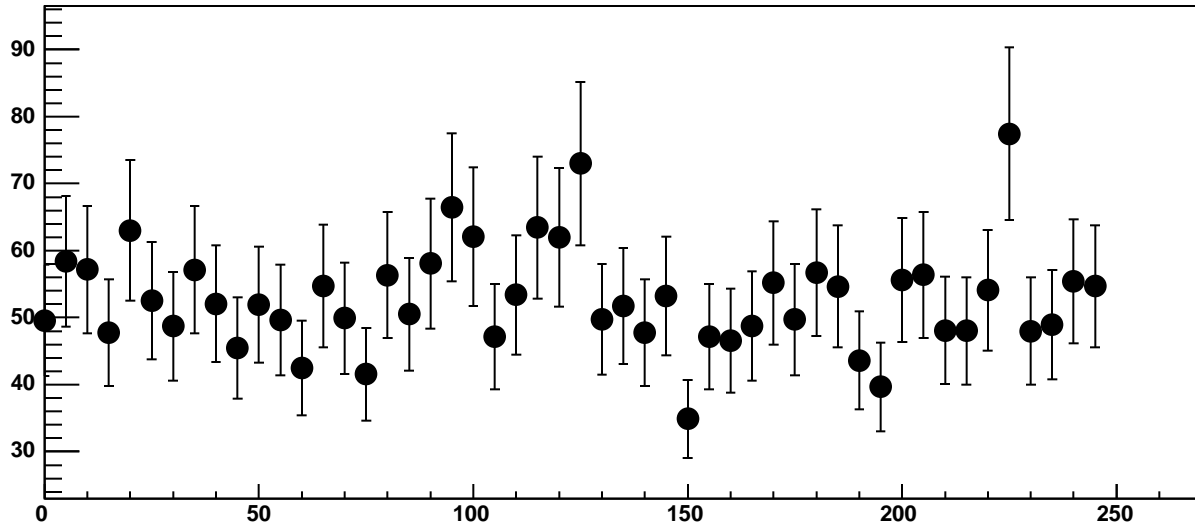


Chip 1, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

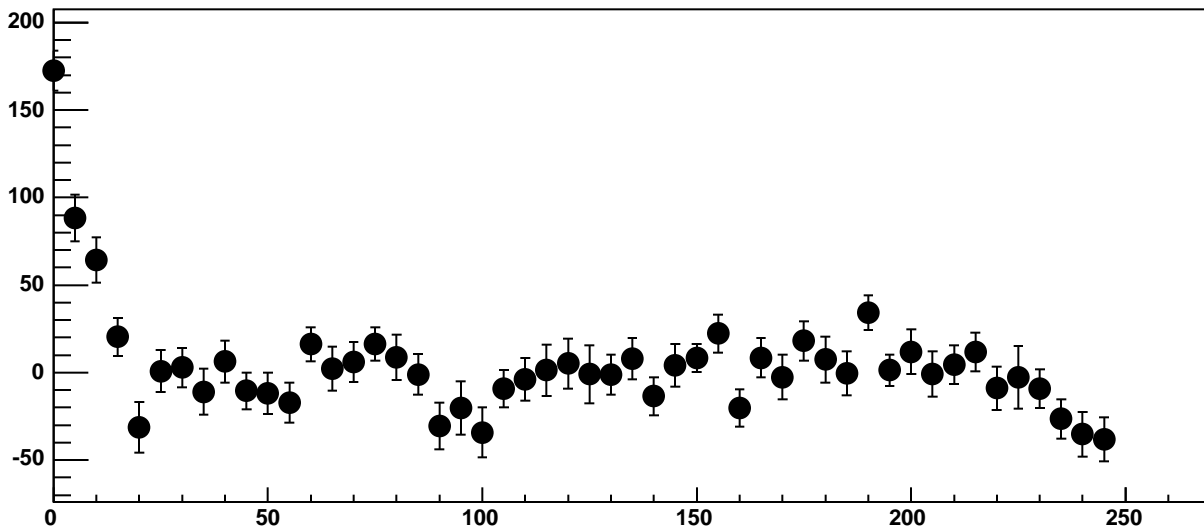


$\chi^2 / \text{ndf}$	76.47 / 41
p0	-935.3 ± 4.6
p1	93.02 ± 0.9301
p2	-2.054e+08 ± 4.188e+06
p3	-2.547e+07 ± 2.488e+05
p4	8.081 ± 0.1298

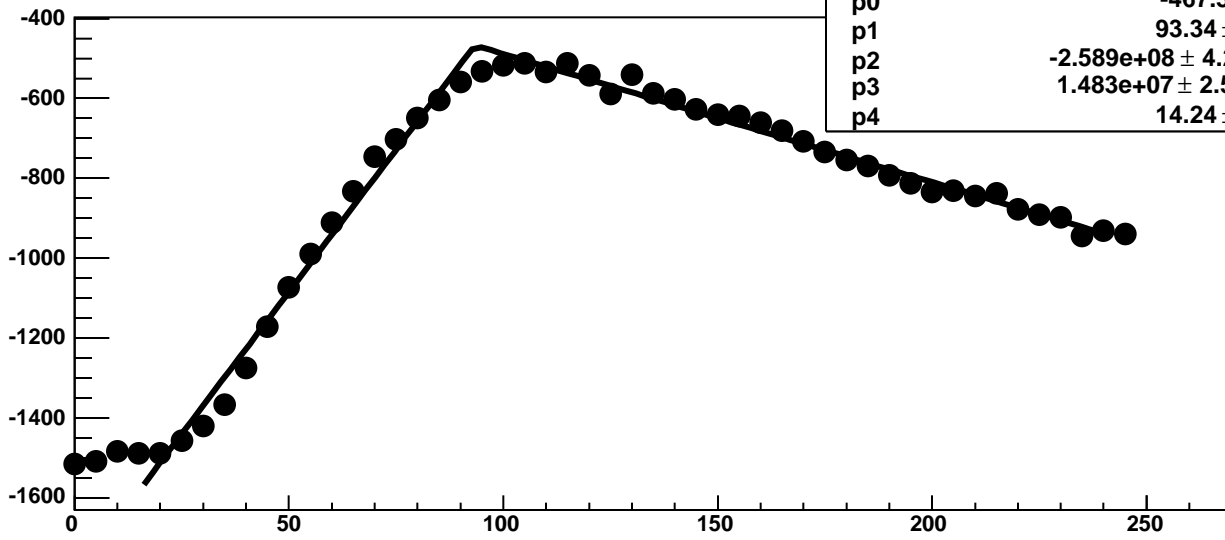
Chip 1, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

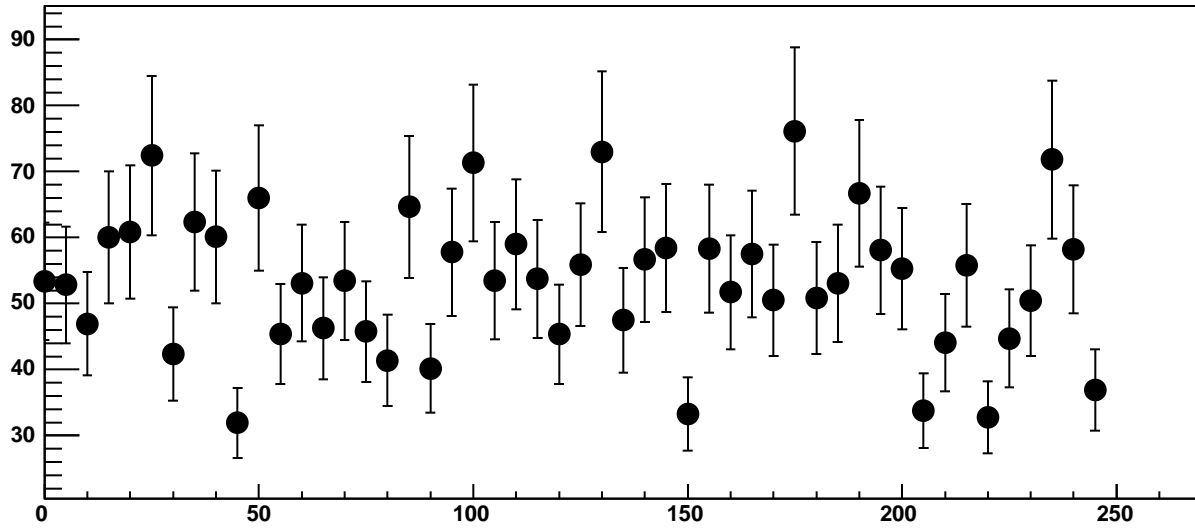


Chip 1, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

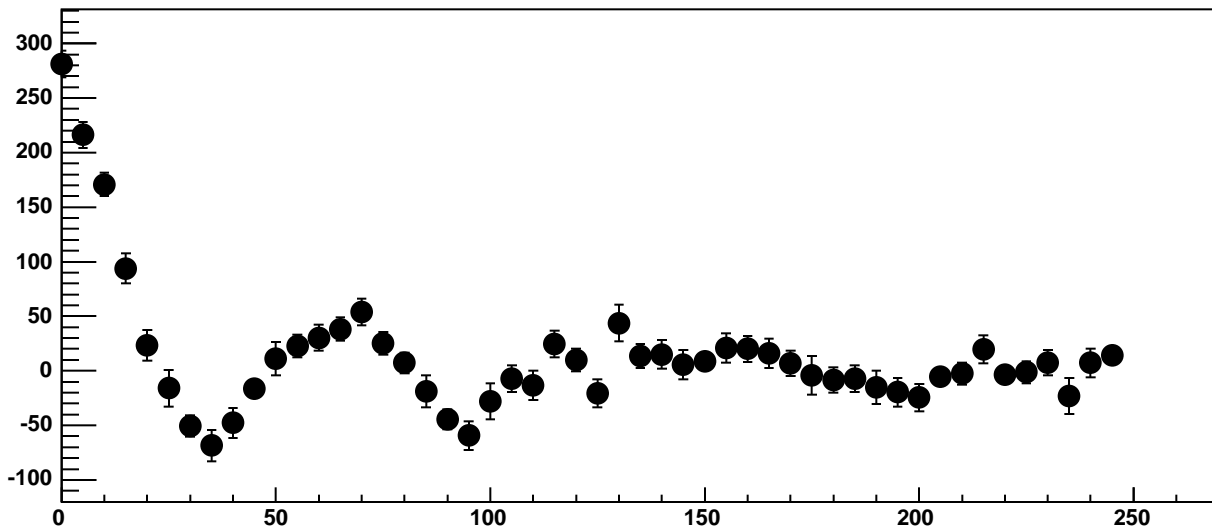


$\chi^2 / \text{ndf}$	255.3 / 41
p0	-467.3 $\pm$ 3.748
p1	93.34 $\pm$ 0.3937
p2	-2.589e+08 $\pm$ 4.272e+06
p3	1.483e+07 $\pm$ 2.522e+05
p4	14.24 $\pm$ 0.1165

Chip 1, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

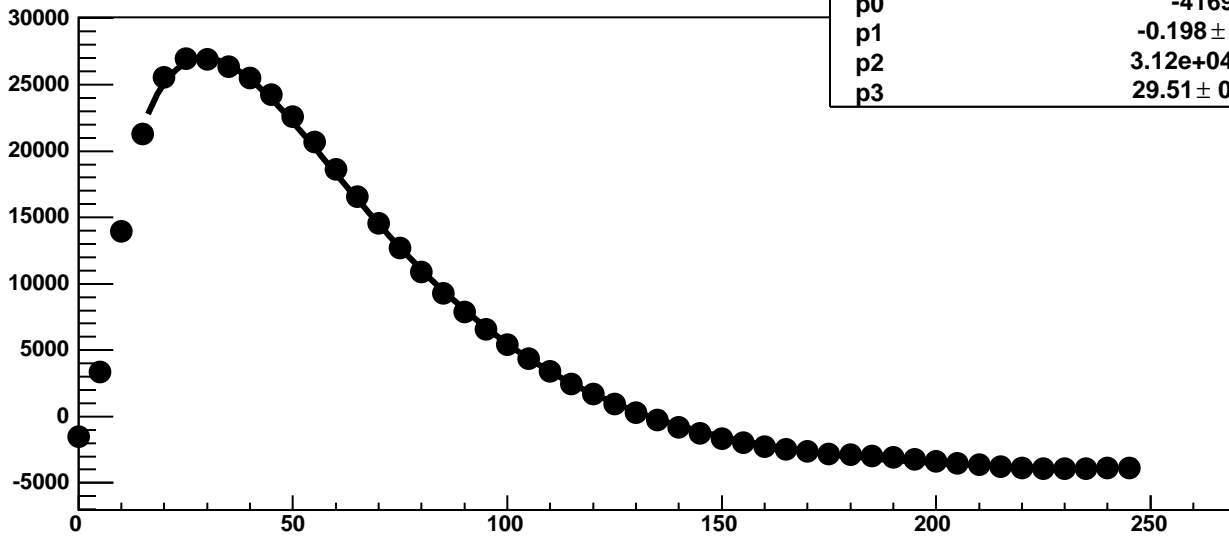


Chip 1, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



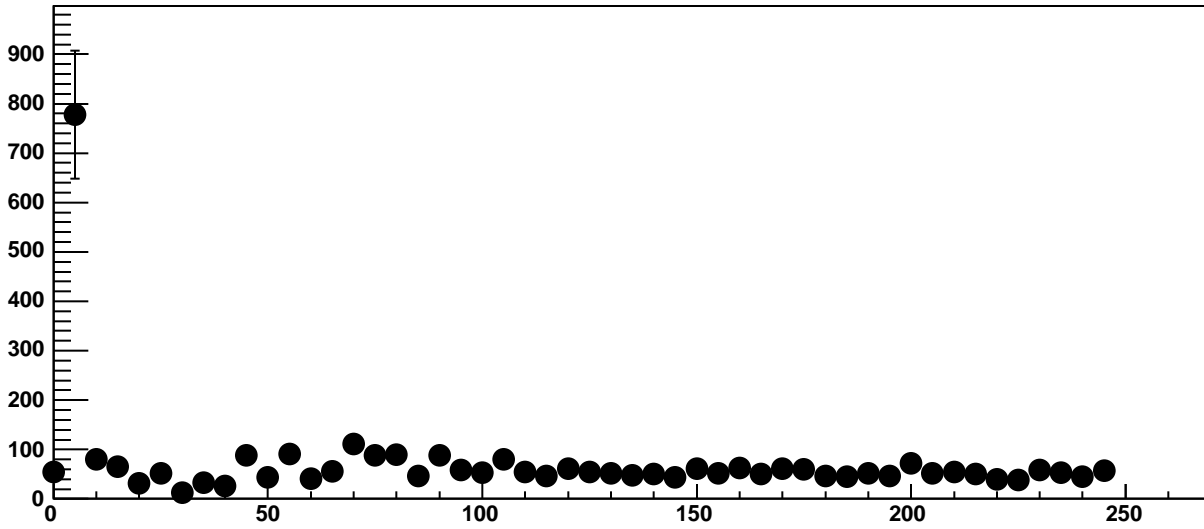


Chip 1, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold

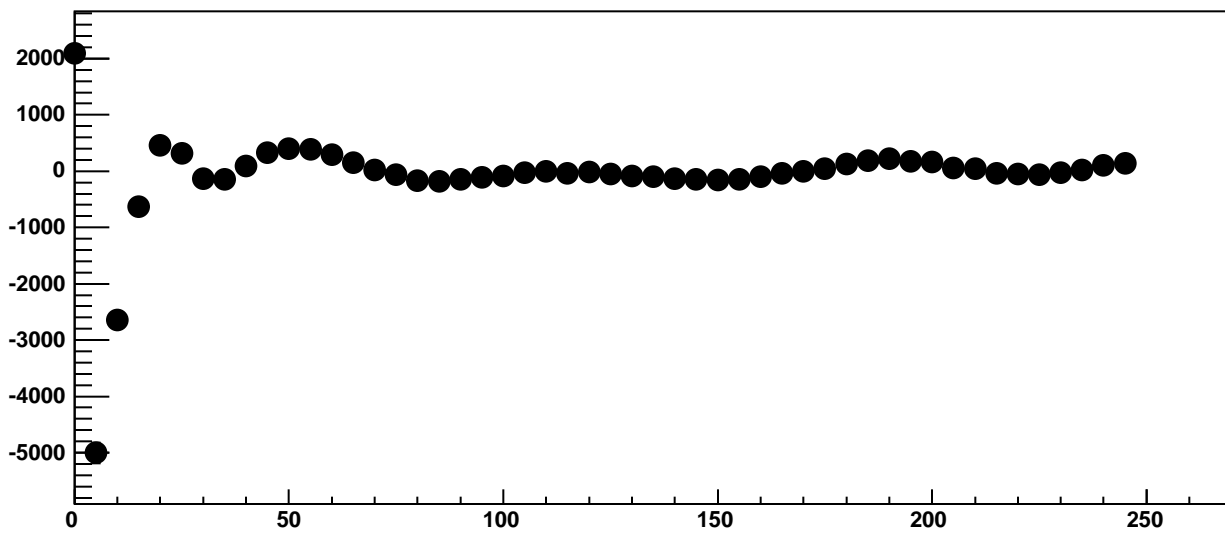


$\chi^2 / \text{ndf}$	1.505e+04 / 42
p0	-4169 ± 3.277
p1	-0.198 ± 0.01485
p2	3.12e+04 ± 3.735
p3	29.51 ± 0.009466

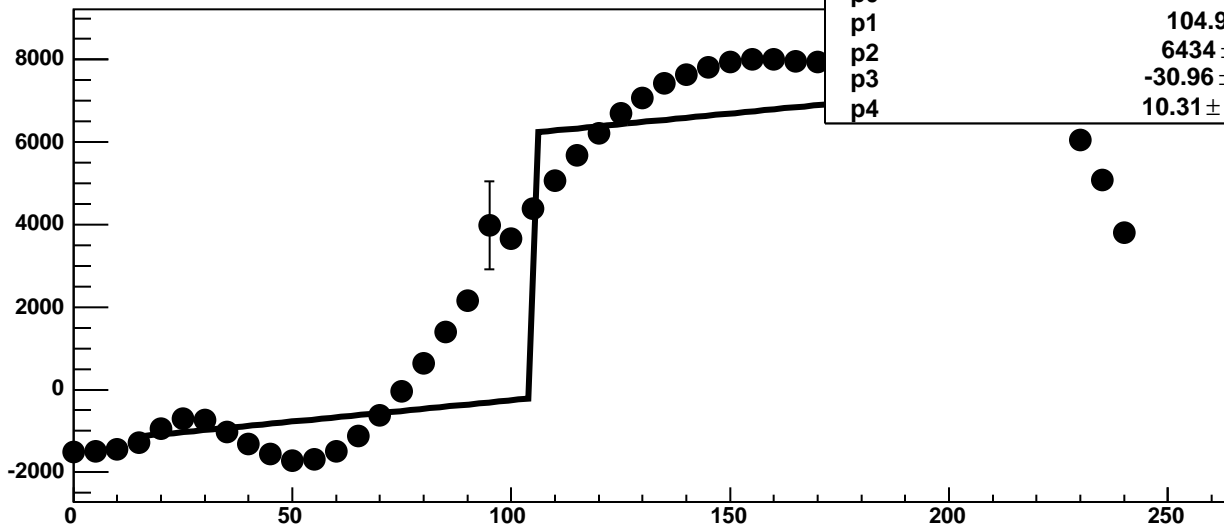
Chip 1, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



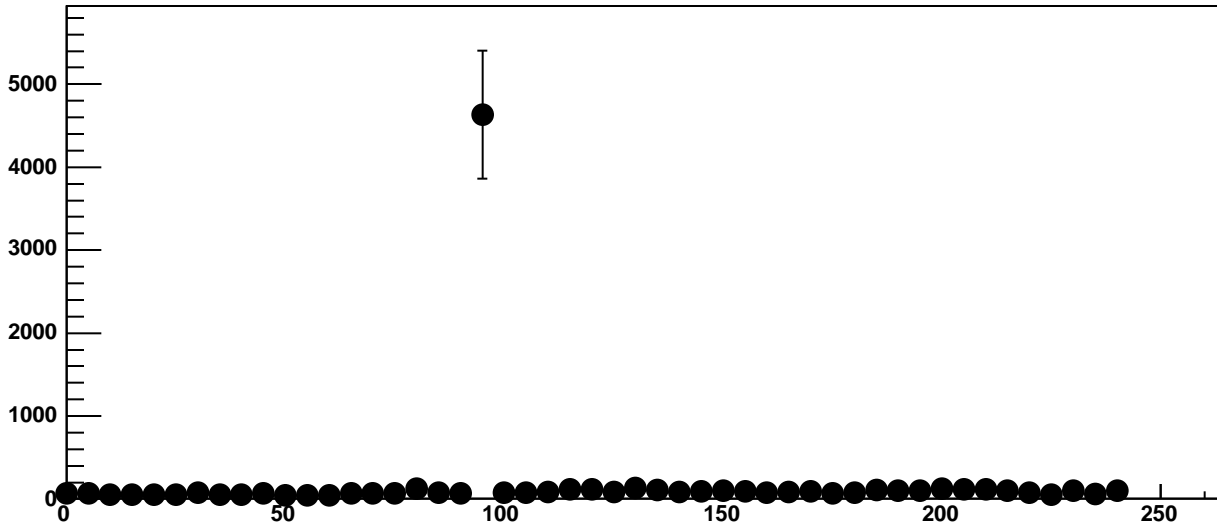
Chip 1, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold



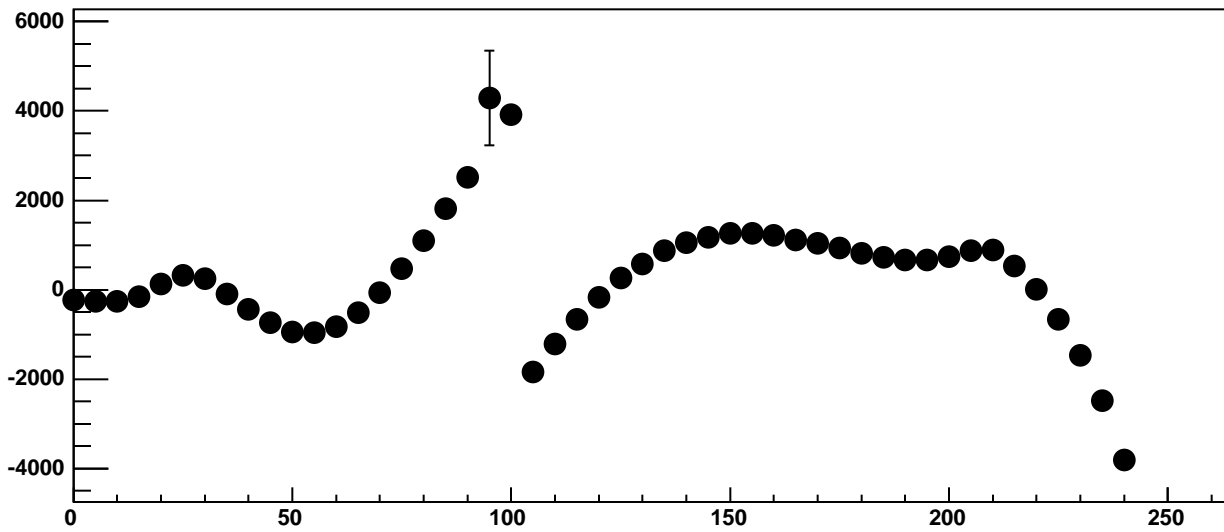
Chip 1, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold



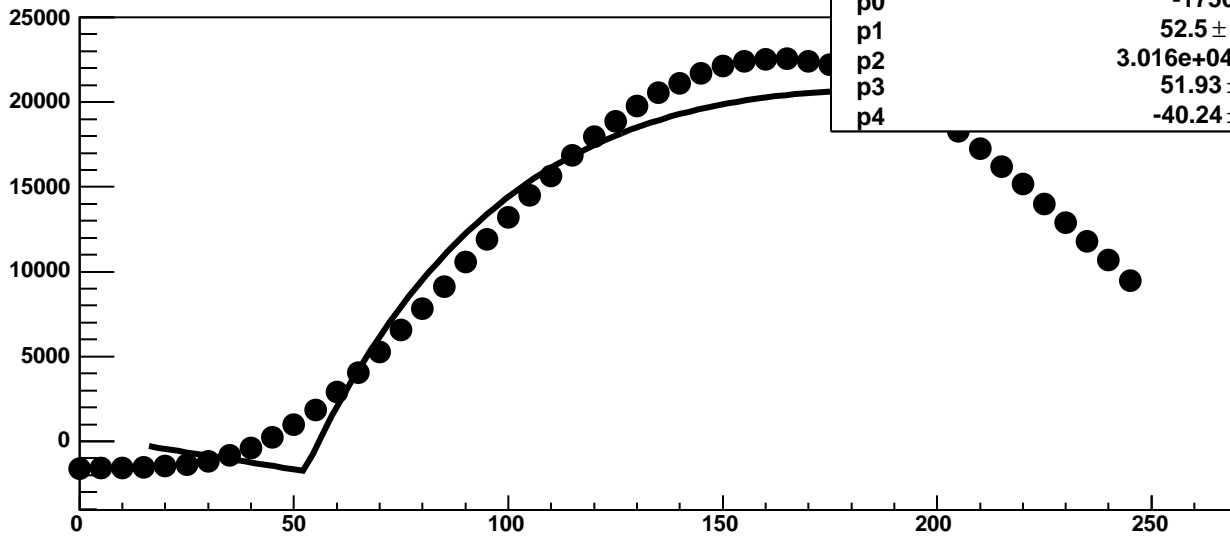
Chip 1, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

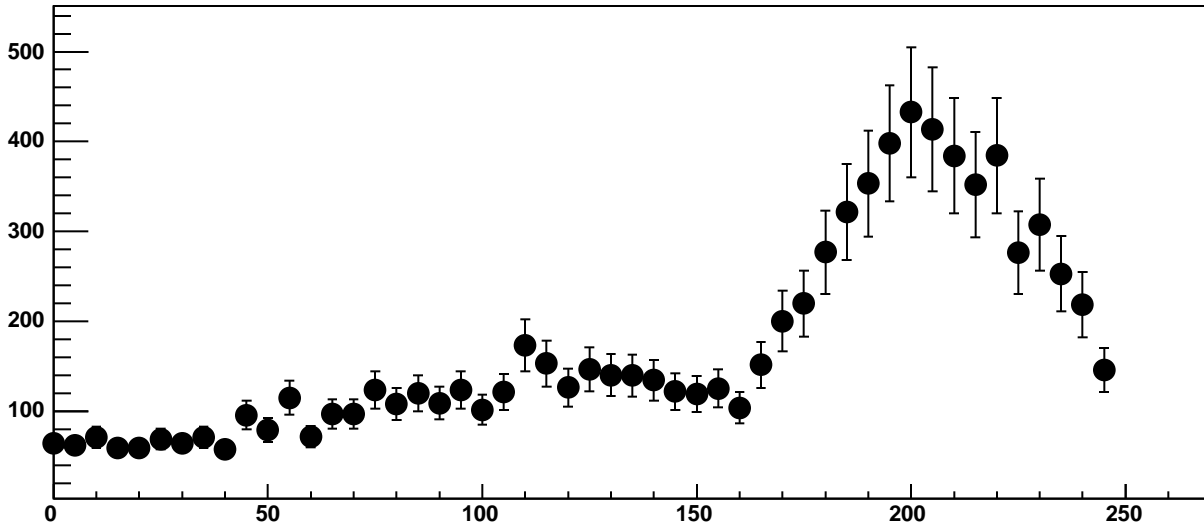


Chip 1, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

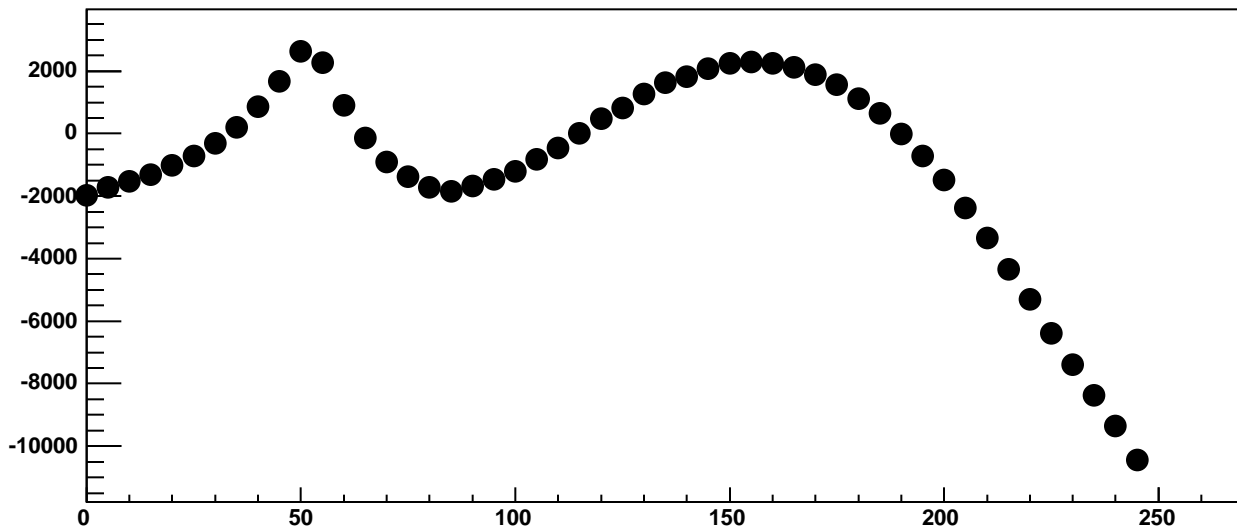


$\chi^2 / \text{ndf}$	2.118e+05 / 41
p0	-1750 ± 8.812
p1	52.5 ± 0.03067
p2	3.016e+04 ± 67.84
p3	51.93 ± 0.1192
p4	-40.24 ± 0.3453

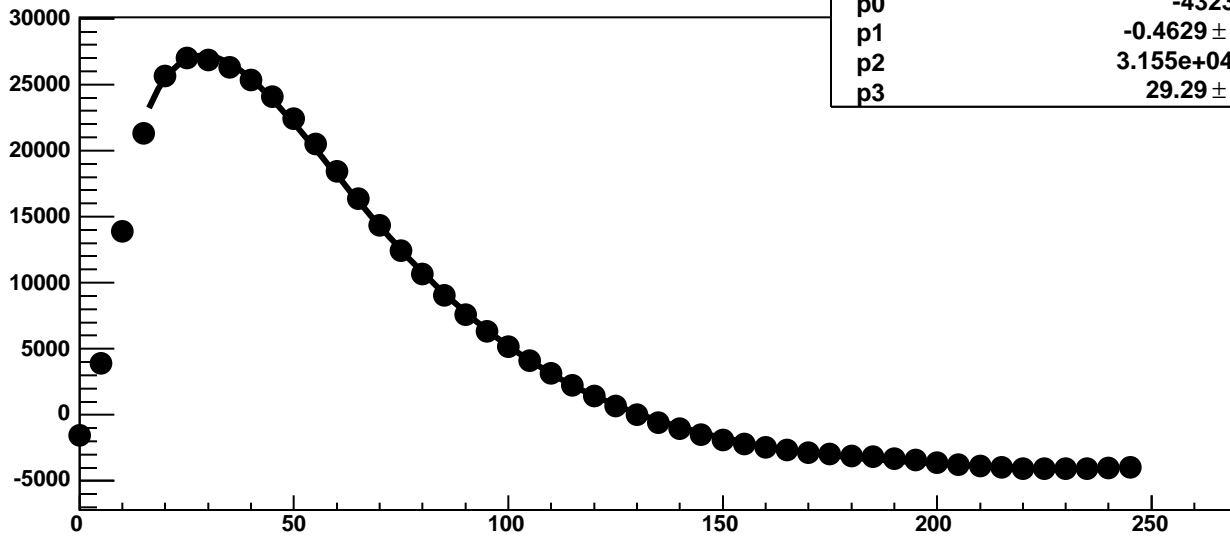
Chip 1, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

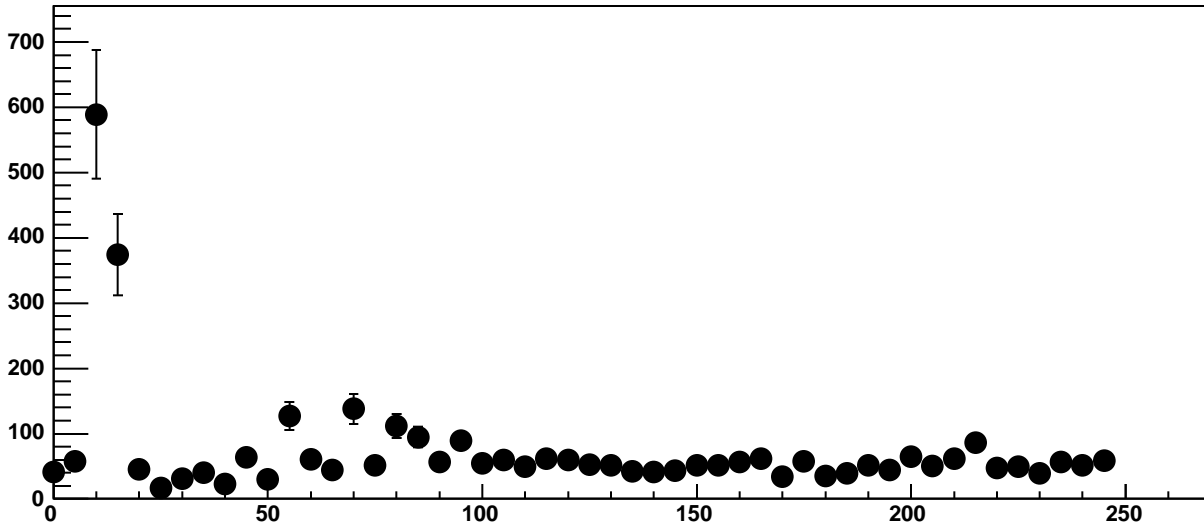


Chip 1, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold

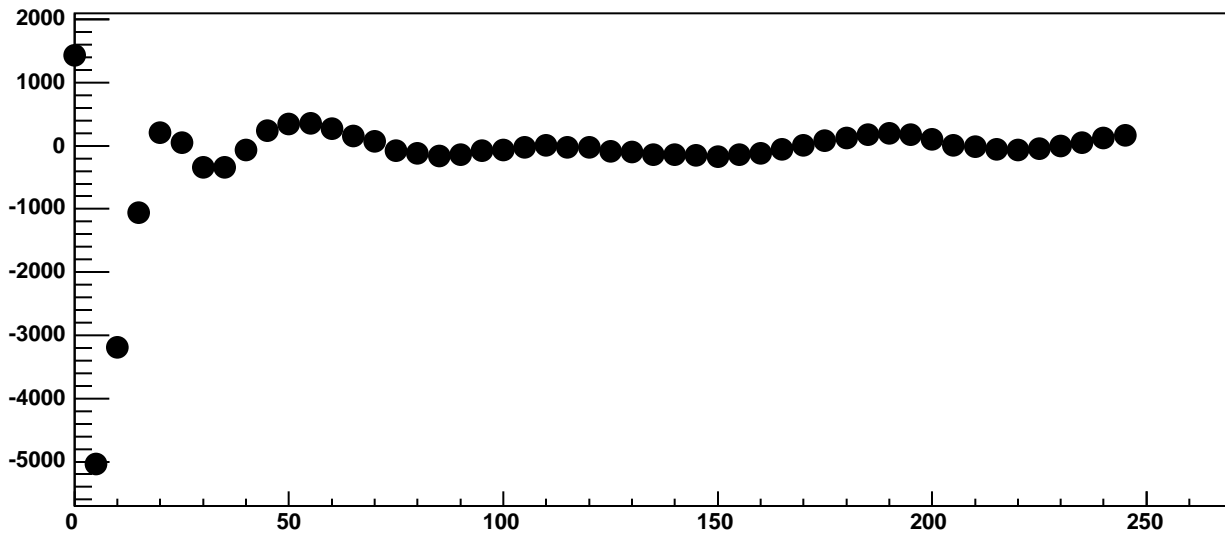


$\chi^2 / \text{ndf}$	1.099e+04 / 42
p0	-4323 ± 3.372
p1	-0.4629 ± 0.01957
p2	3.155e+04 ± 3.847
p3	29.29 ± 0.01134

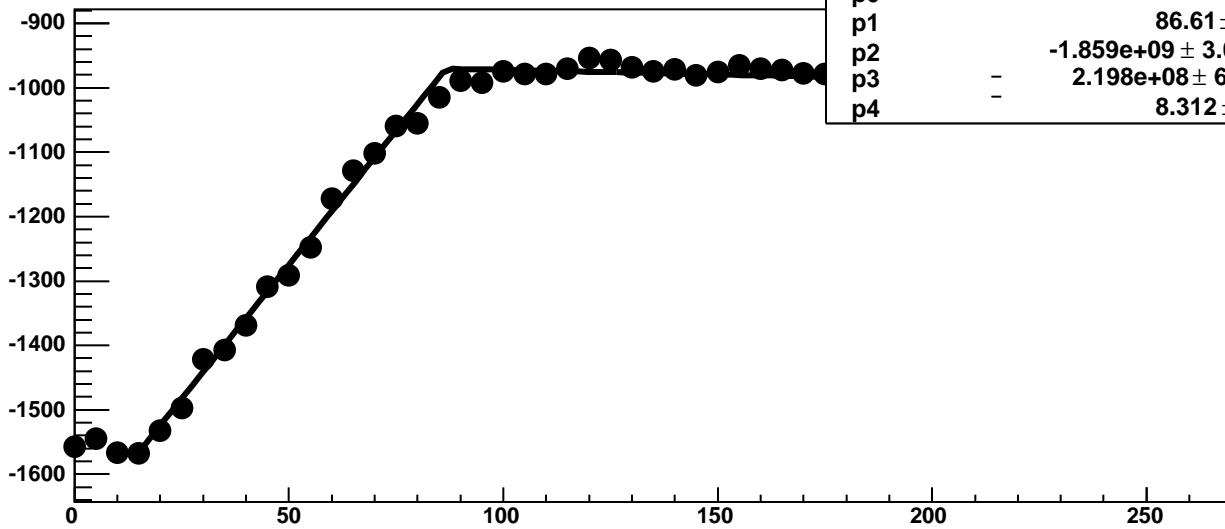
Chip 1, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold

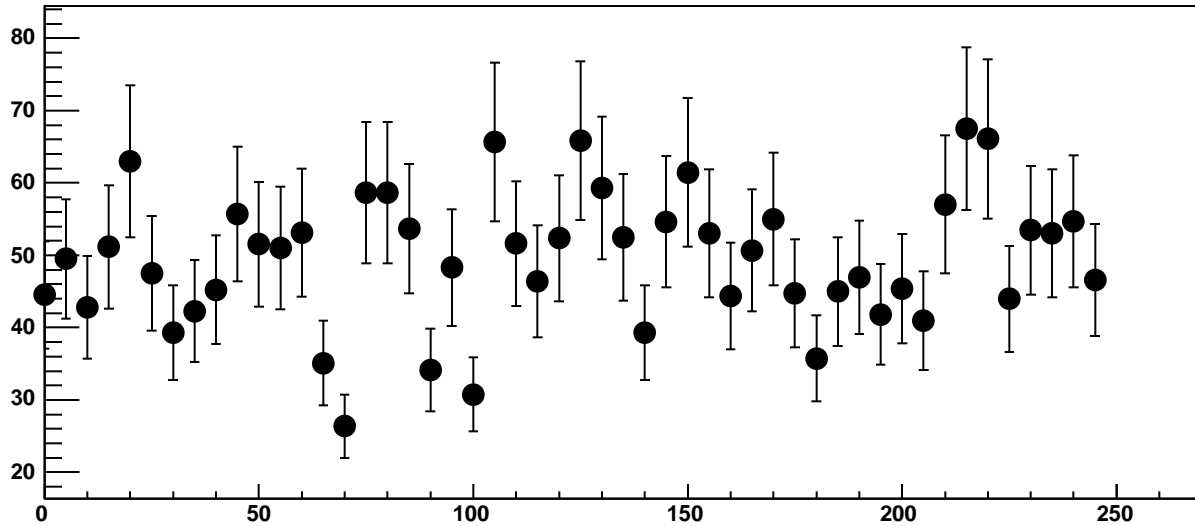


Chip 1, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

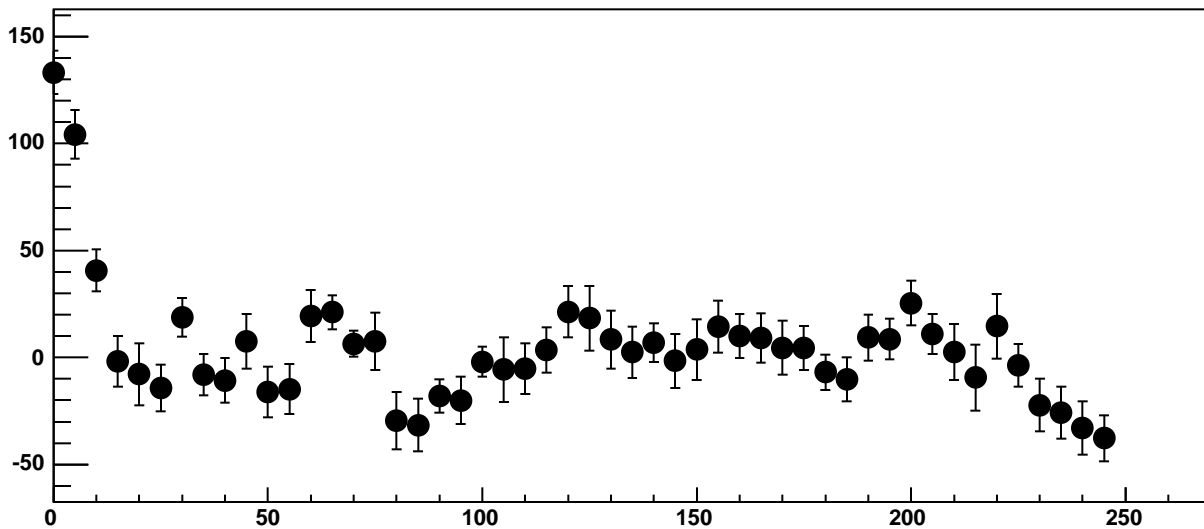


$\chi^2 / \text{ndf}$	79.29 / 41
p0	$-970.3 \pm 3.675$
p1	$86.61 \pm 0.7626$
p2	$-1.859\text{e}+09 \pm 3.057\text{e}+07$
p3	$2.198\text{e}+08 \pm 6.54\text{e}+05$
p4	$8.312 \pm 0.1309$

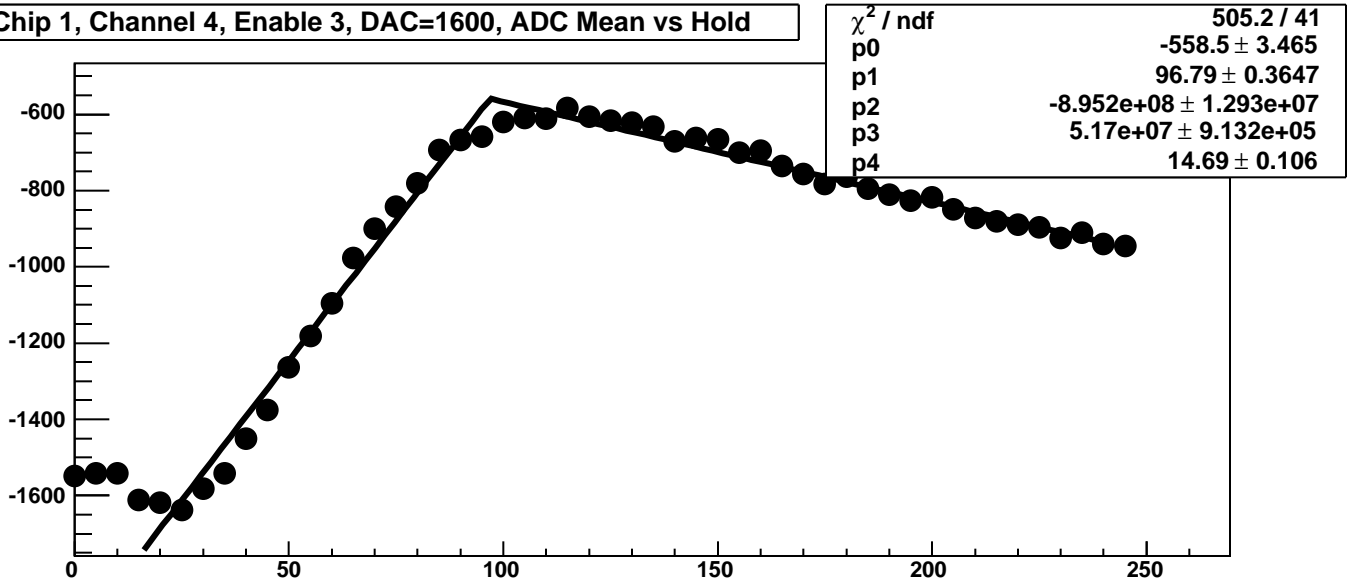
Chip 1, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



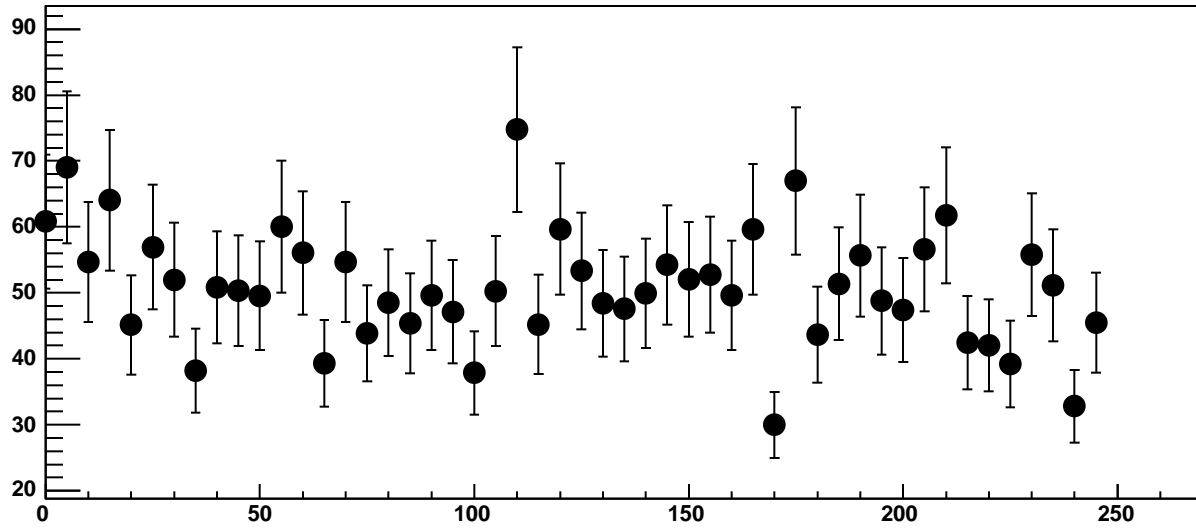
Chip 1, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold



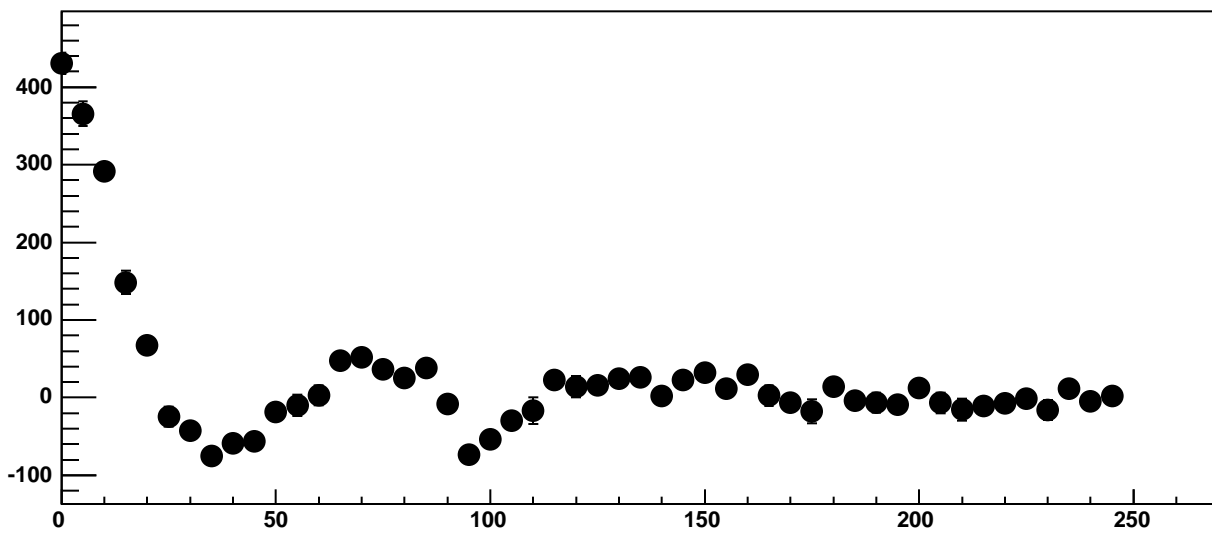
Chip 1, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold



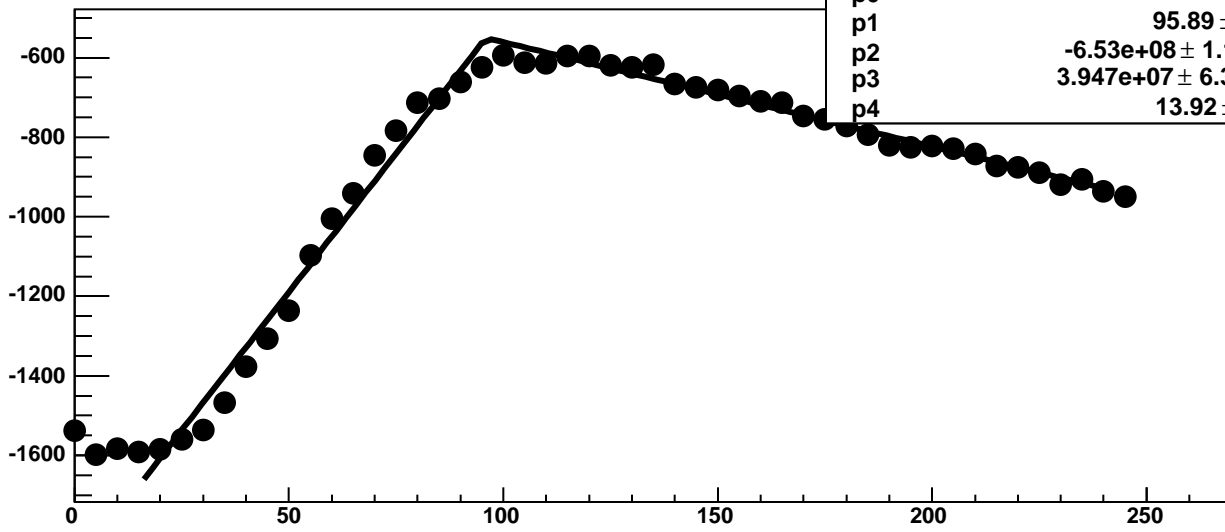
Chip 1, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

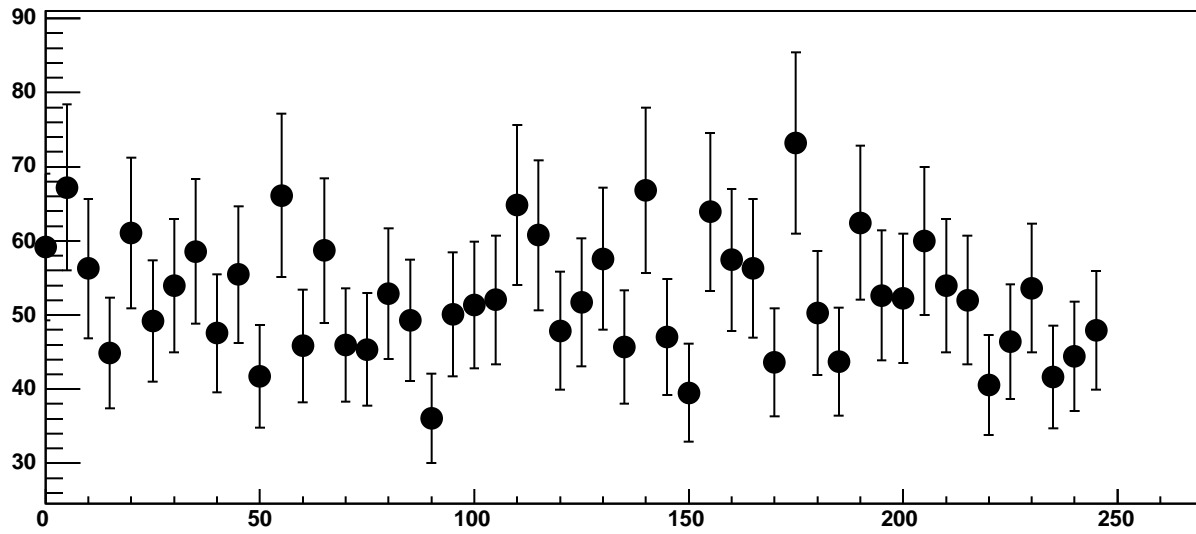


Chip 1, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold

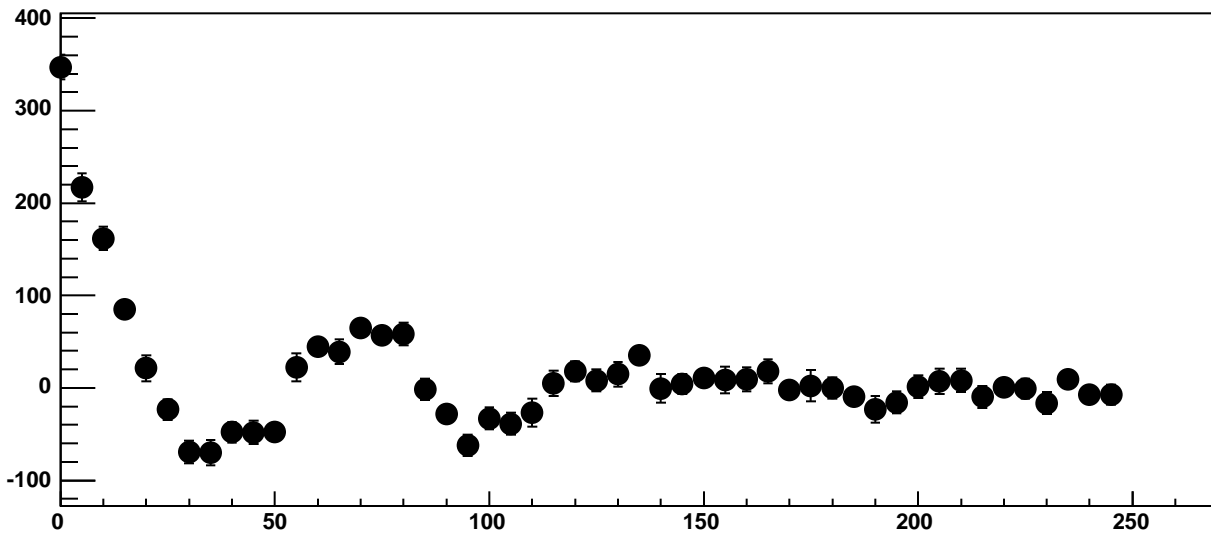


$\chi^2 / \text{ndf}$	404 / 41
p0	$-550.3 \pm 3.894$
p1	$95.89 \pm 0.4104$
p2	$-6.53\text{e}+08 \pm 1.109\text{e}+07$
p3	$3.947\text{e}+07 \pm 6.376\text{e}+05$
p4	$13.92 \pm 0.1087$

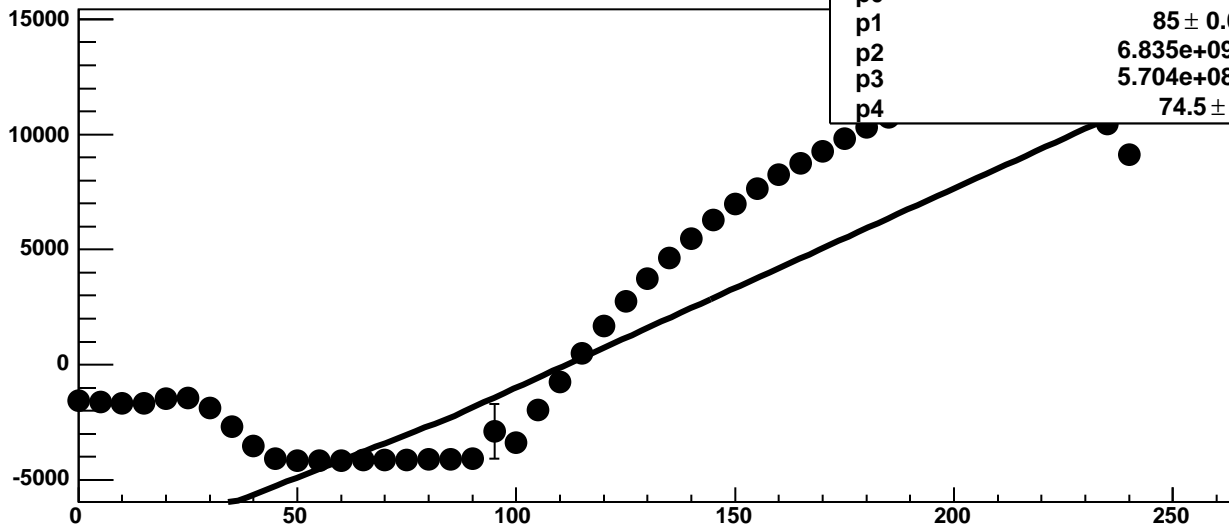
Chip 1, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold

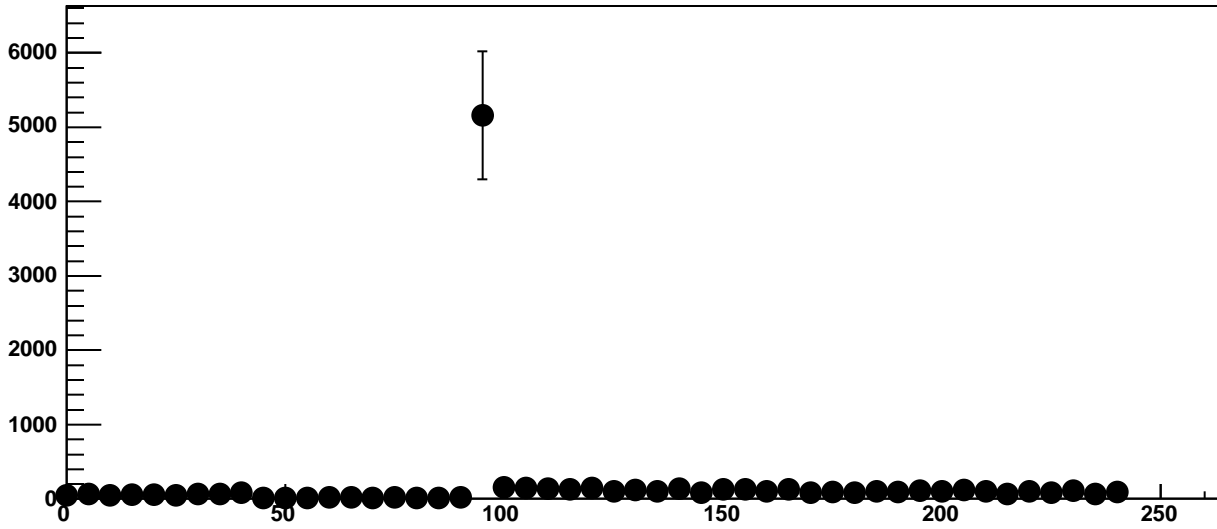


Chip 1, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

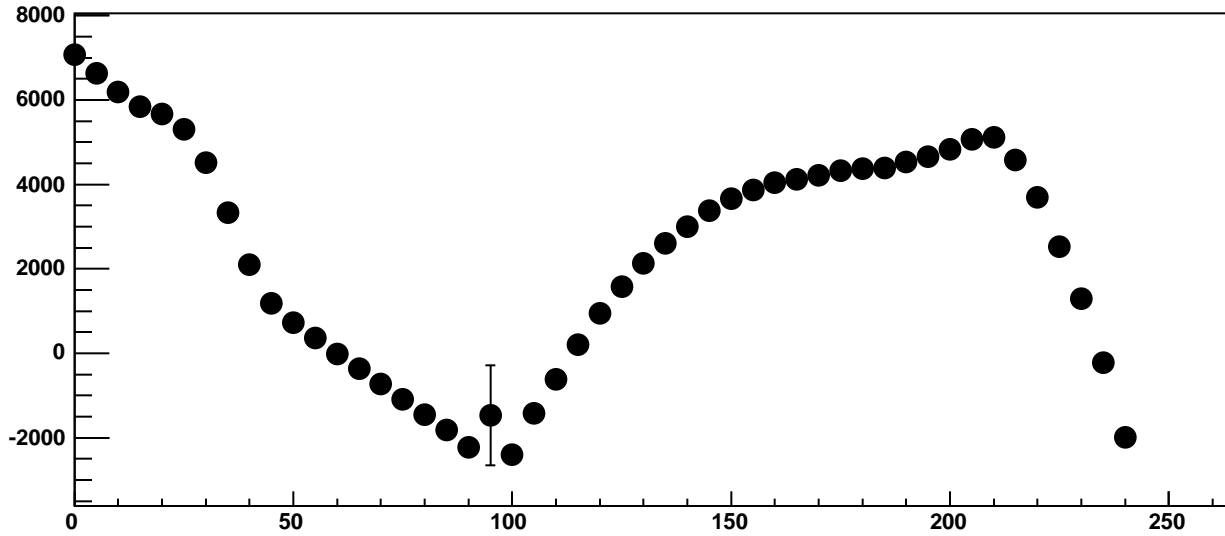


$\chi^2 / \text{ndf}$	2.329e+06 / 41
p0	-2293 ± 1.153
p1	85 ± 0.0006187
p2	6.835e+09 ± 1.414
p3	5.704e+08 ± 1.414
p4	74.5 ± 0.03285

Chip 1, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

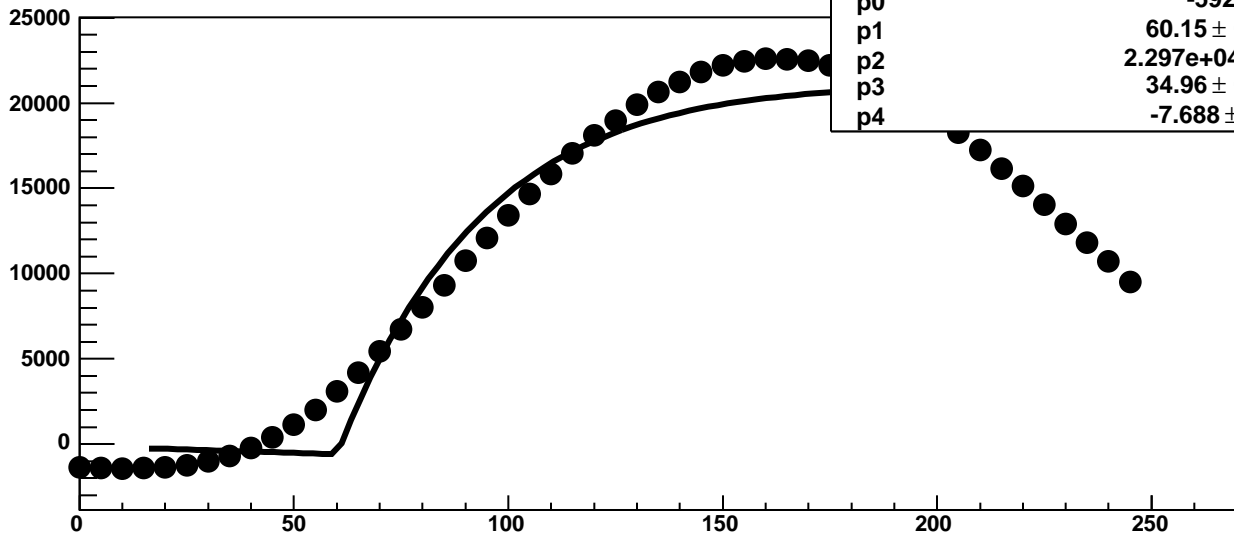


Chip 1, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



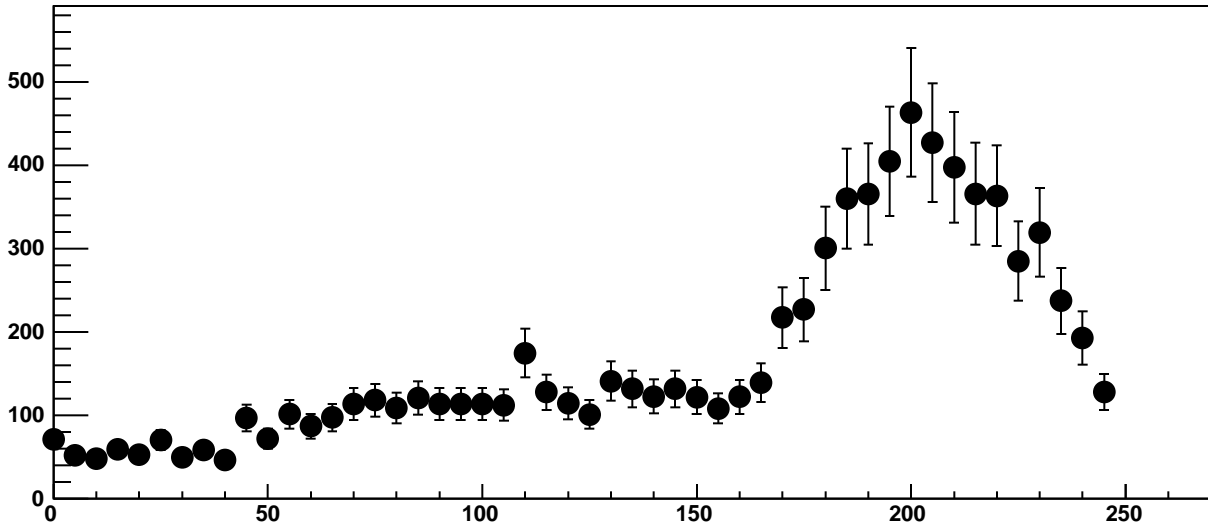


Chip 1, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

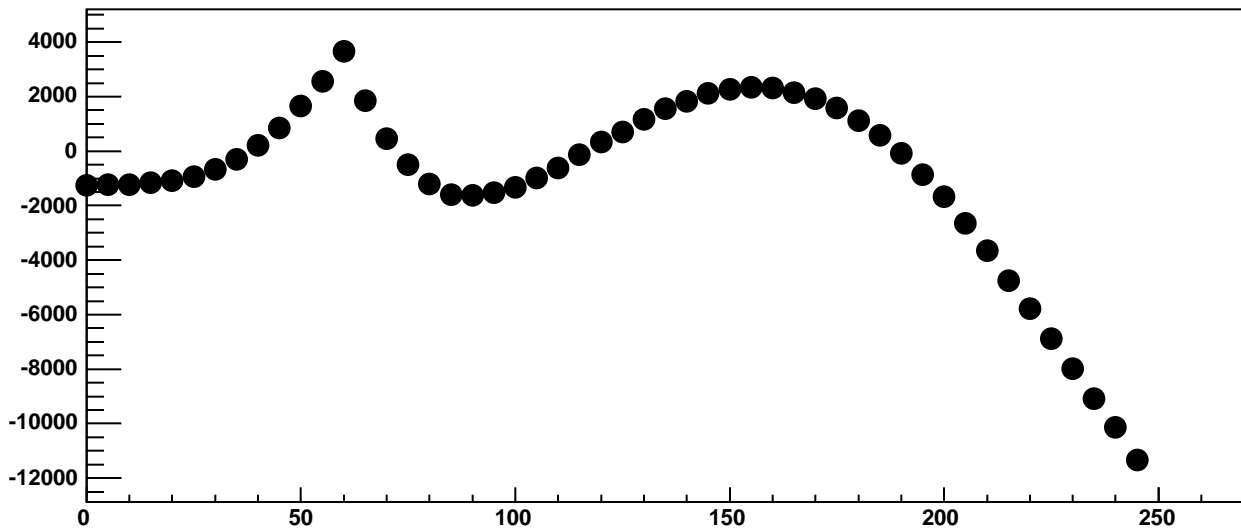


$\chi^2 / \text{ndf}$	2.618e+05 / 41
p0	-592 ± 8.081
p1	60.15 ± 0.03272
p2	2.297e+04 ± 41.5
p3	34.96 ± 0.07745
p4	-7.688 ± 0.2546

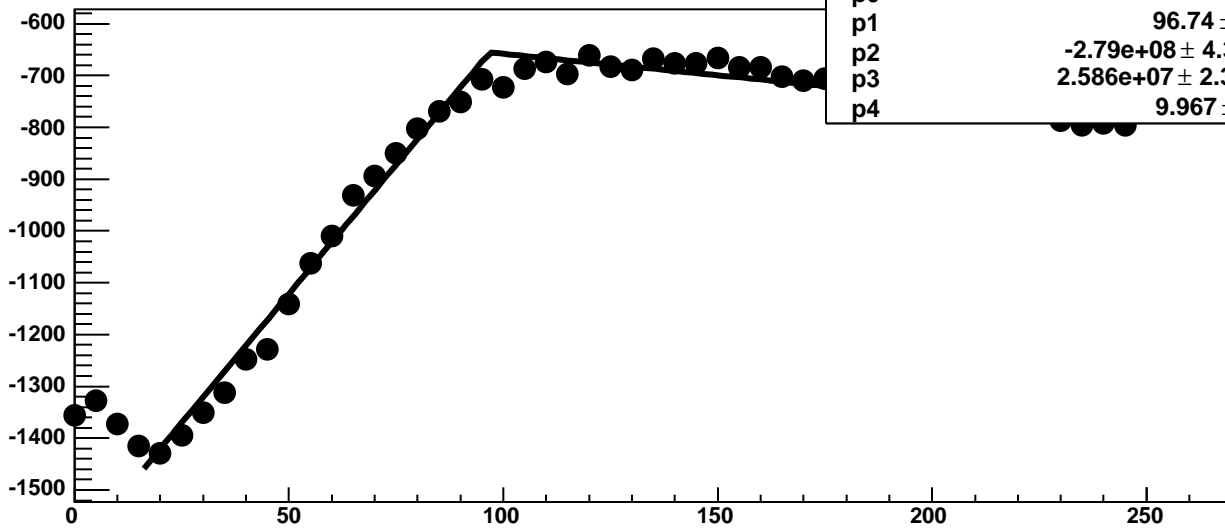
Chip 1, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

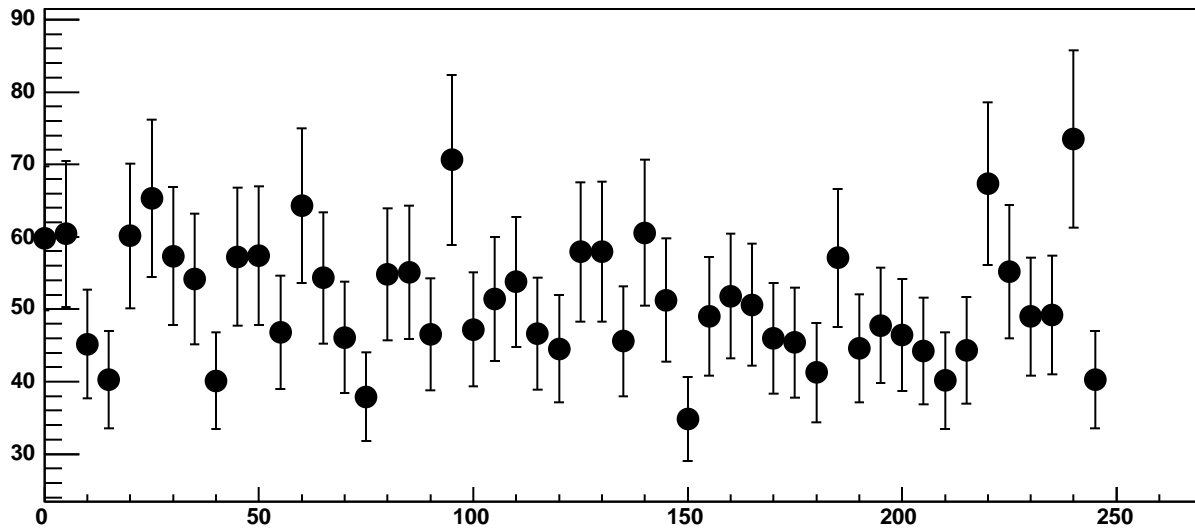


Chip 1, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

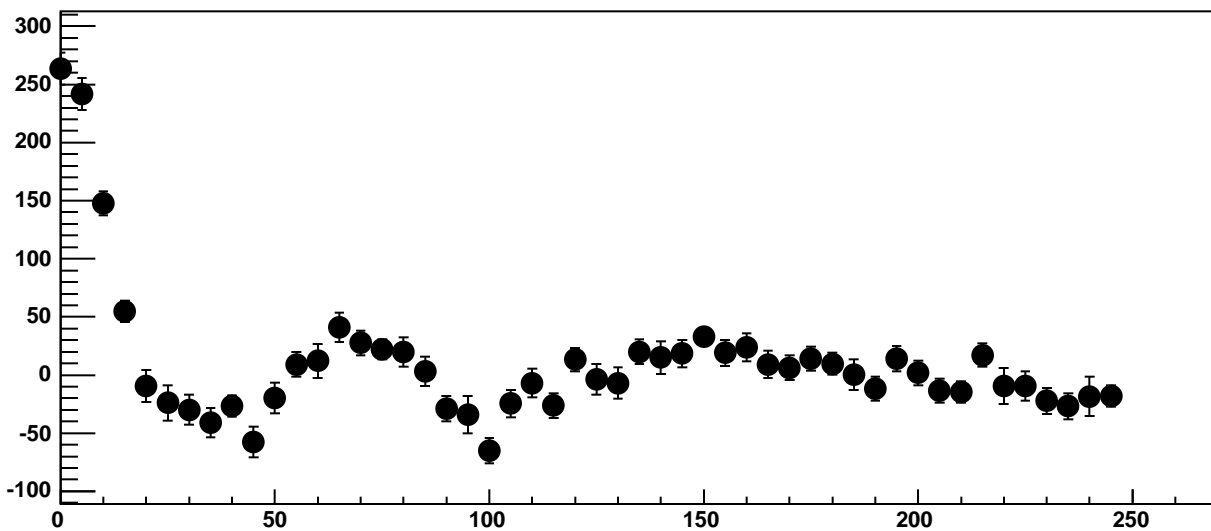


$\chi^2 / \text{ndf}$	230.2 / 41
p0	$-655.6 \pm 4.005$
p1	$96.74 \pm 0.6585$
p2	$-2.79\text{e}+08 \pm 4.371\text{e}+06$
p3	$2.586\text{e}+07 \pm 2.383\text{e}+05$
p4	$9.967 \pm 0.1167$

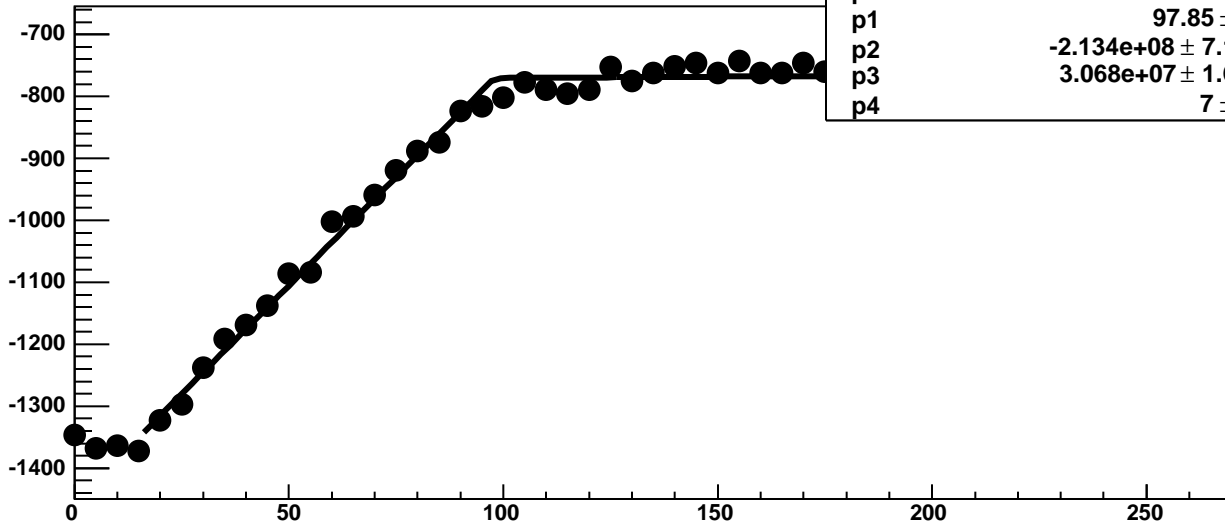
Chip 1, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold

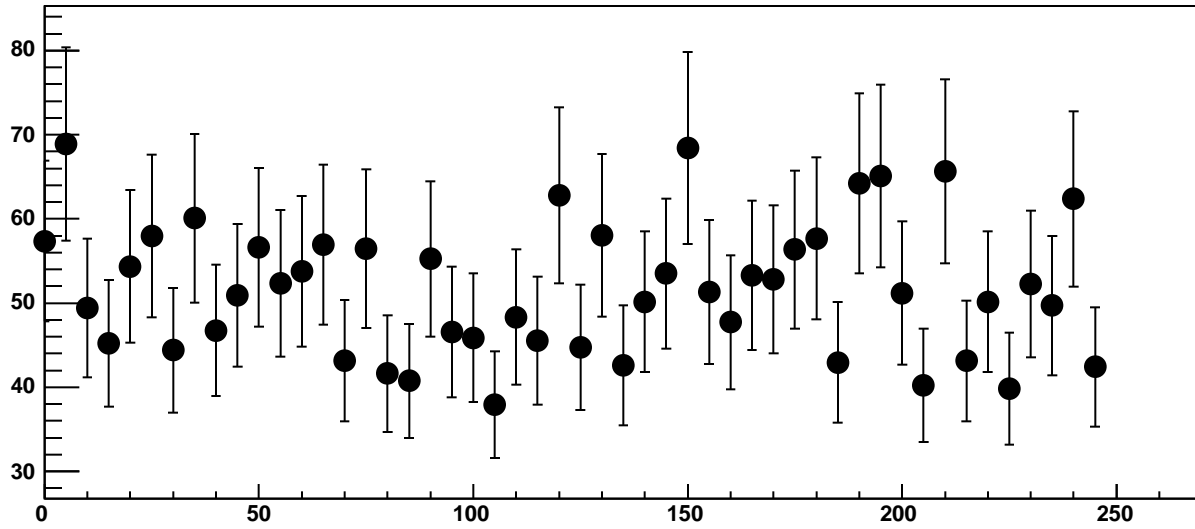


Chip 1, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

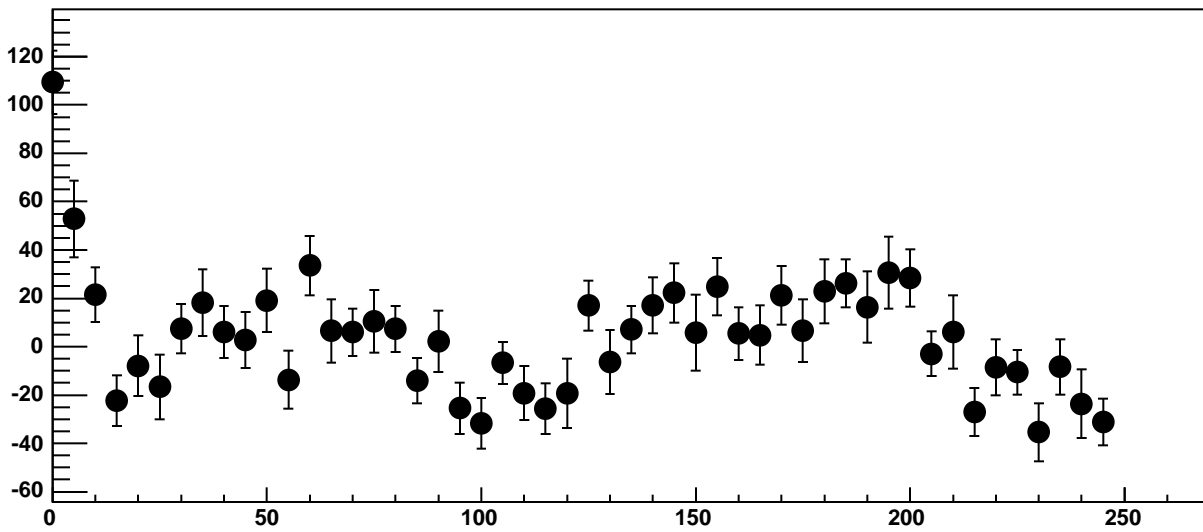


$\chi^2 / \text{ndf}$	110.5 / 41
p0	-770.4 ± 4.459
p1	97.85 ± 0.6804
p2	-2.134e+08 ± 7.109e+06
p3	3.068e+07 ± 1.669e+06
p4	7 ± 0.1204

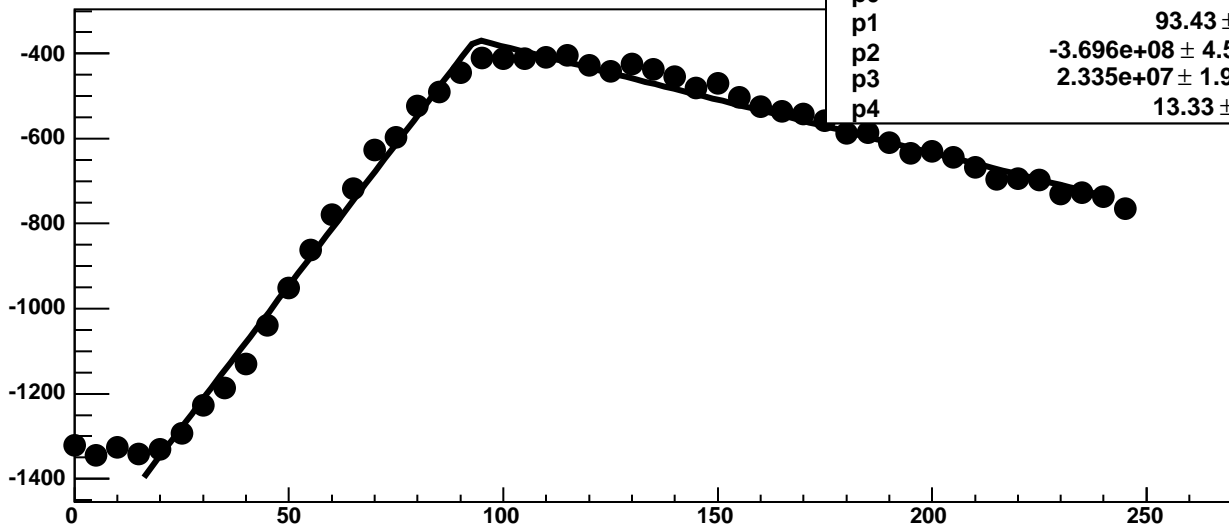
Chip 1, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



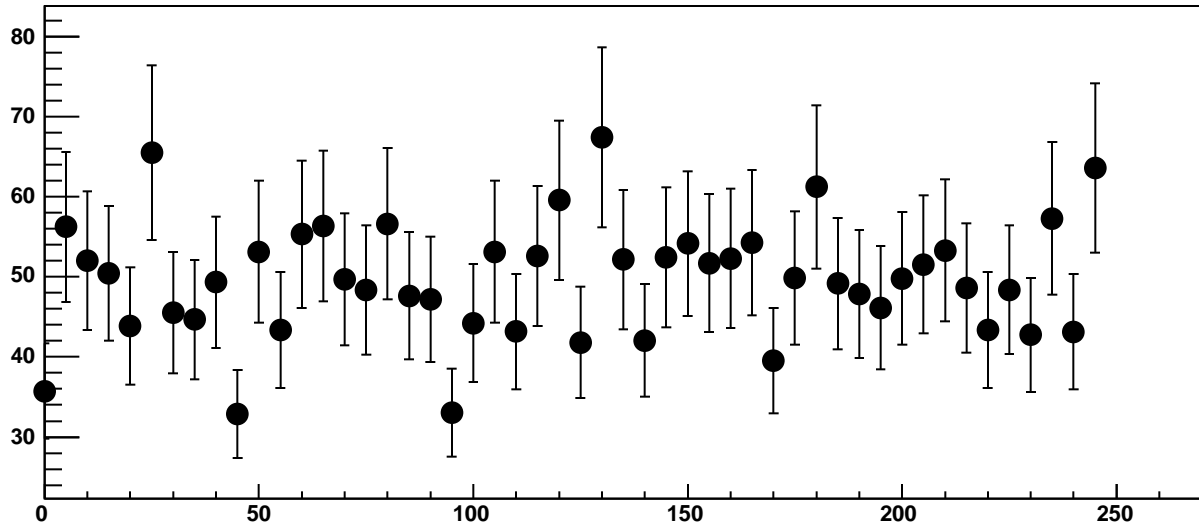
Chip 1, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold



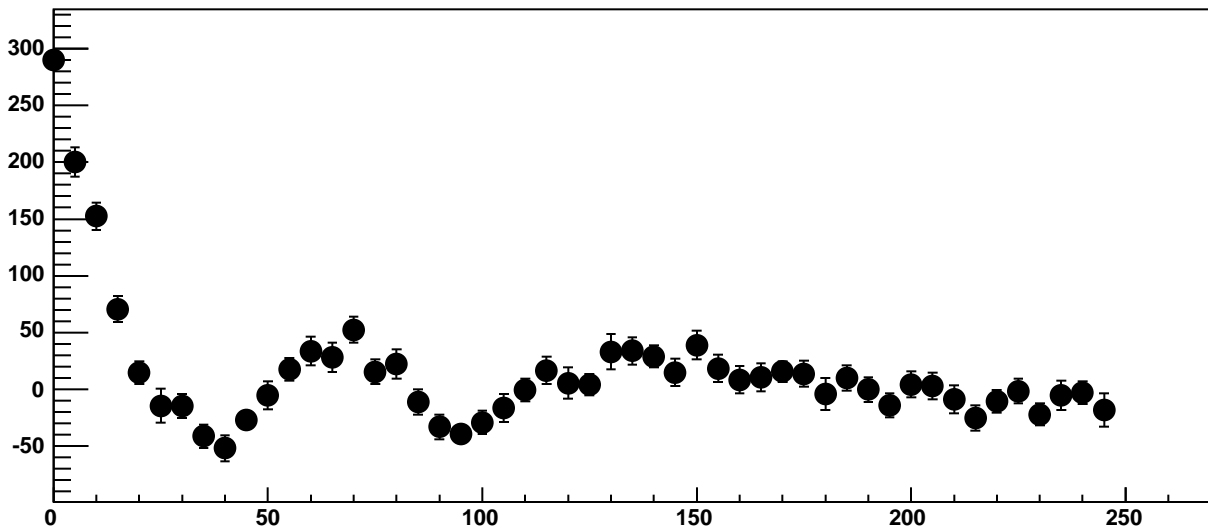
Chip 1, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold



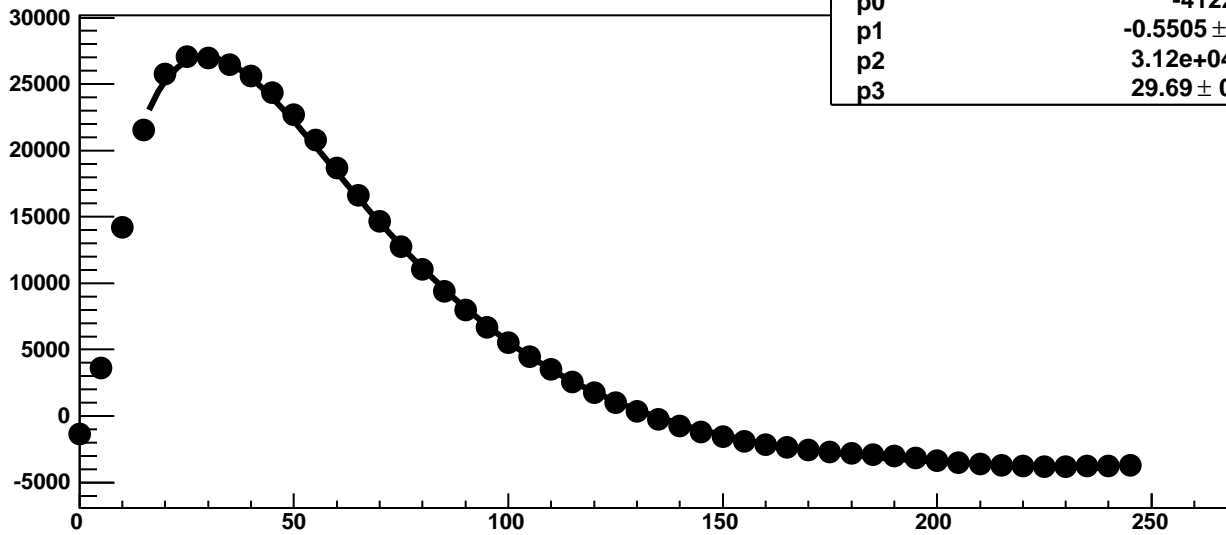
Chip 1, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

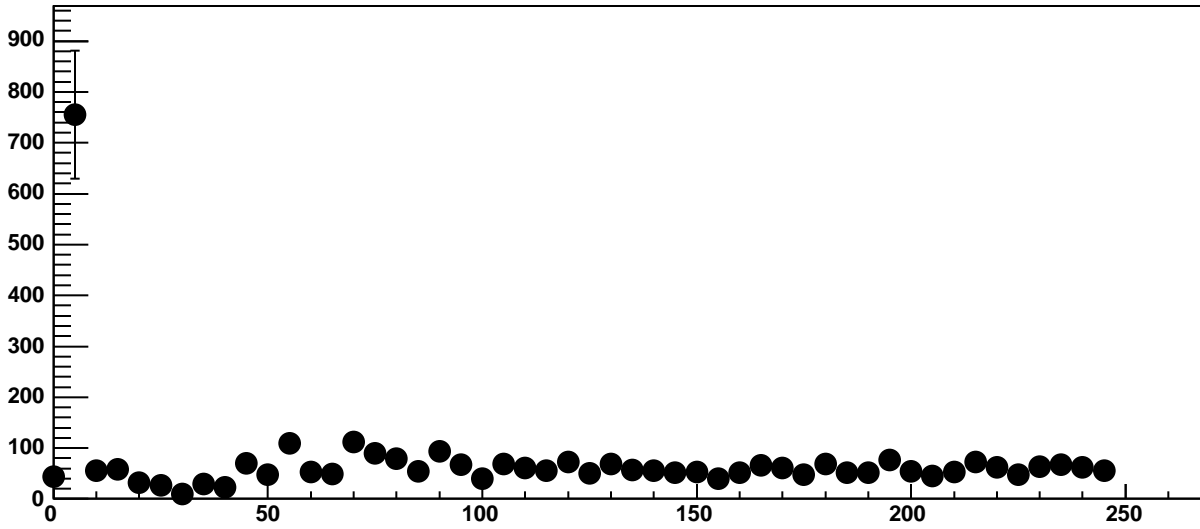


Chip 1, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

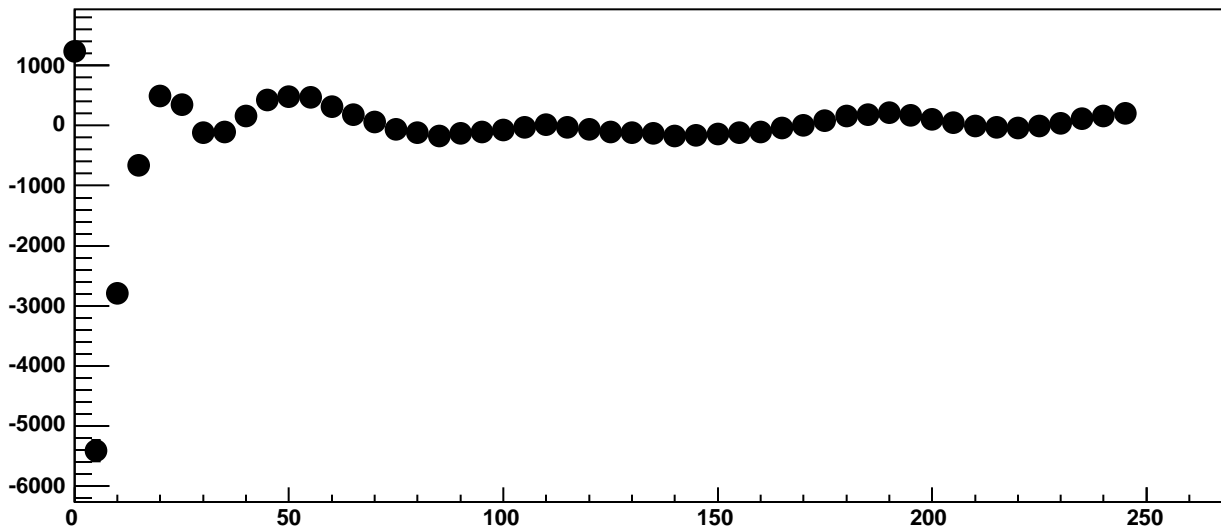


$\chi^2 / \text{ndf}$	2.063e+04 / 42
p0	-4122 ± 3.654
p1	-0.5505 ± 0.01458
p2	3.12e+04 ± 3.829
p3	29.69 ± 0.009689

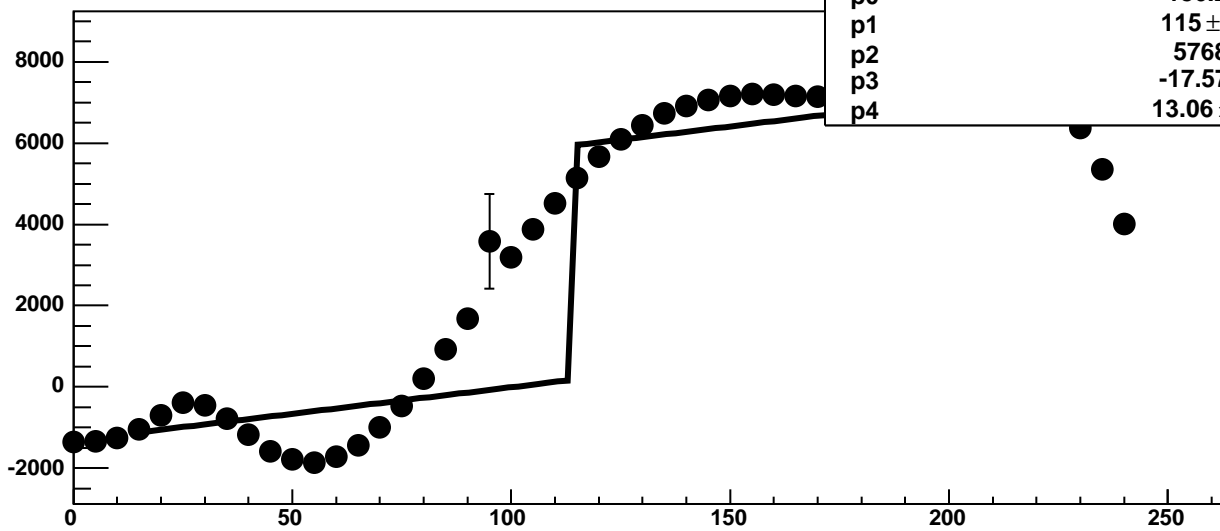
Chip 1, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold

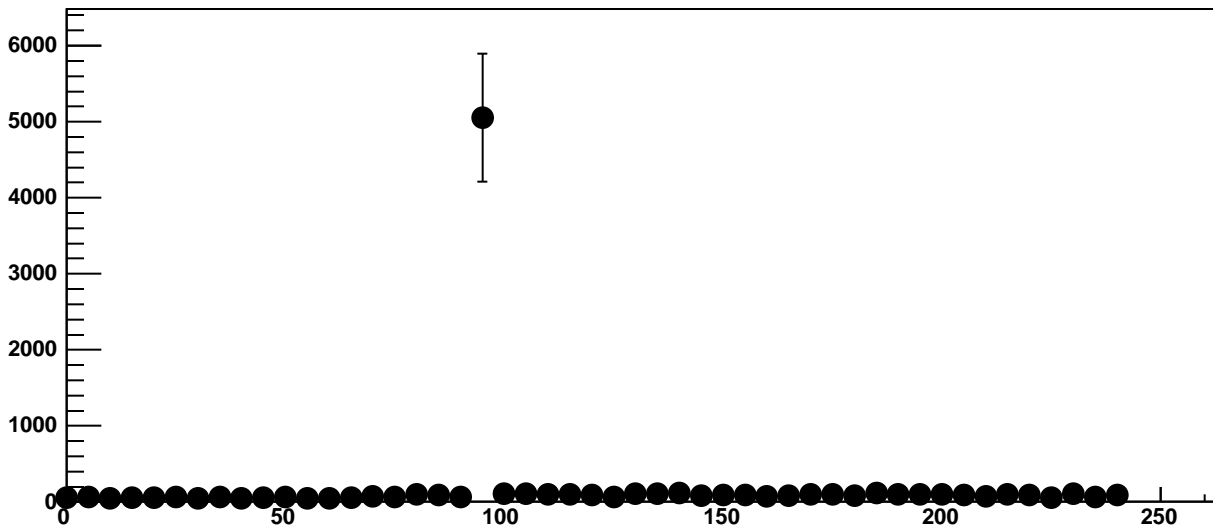


Chip 1, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

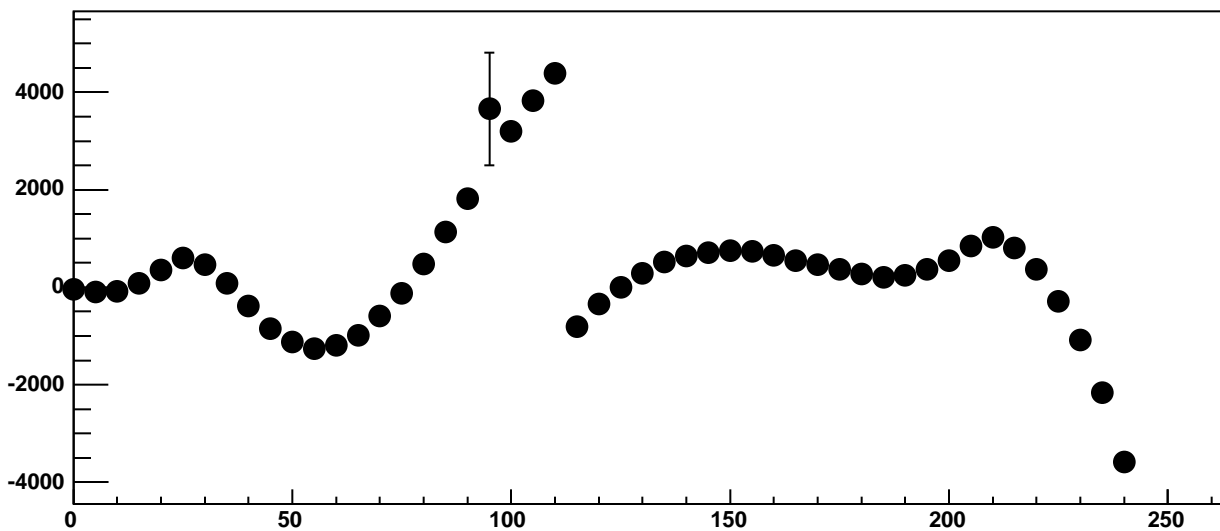


$\chi^2 / \text{ndf}$	2.115e+05 / 41
p0	186.2 ± 23.89
p1	115 ± 0.00394
p2	5768 ± 25.73
p3	-17.57 ± 1.826
p4	13.06 ± 0.1696

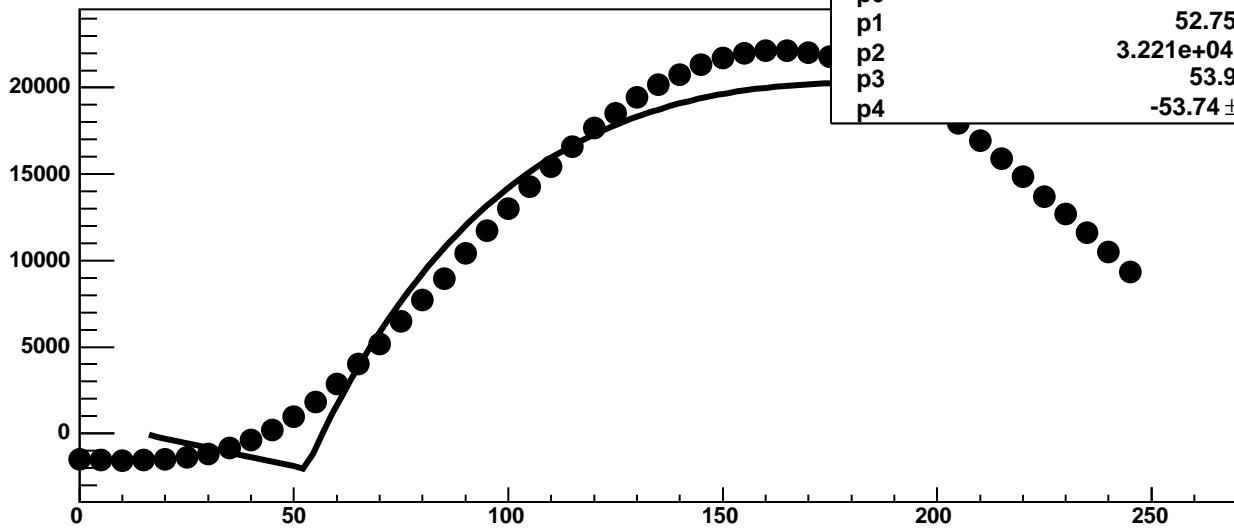
Chip 1, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

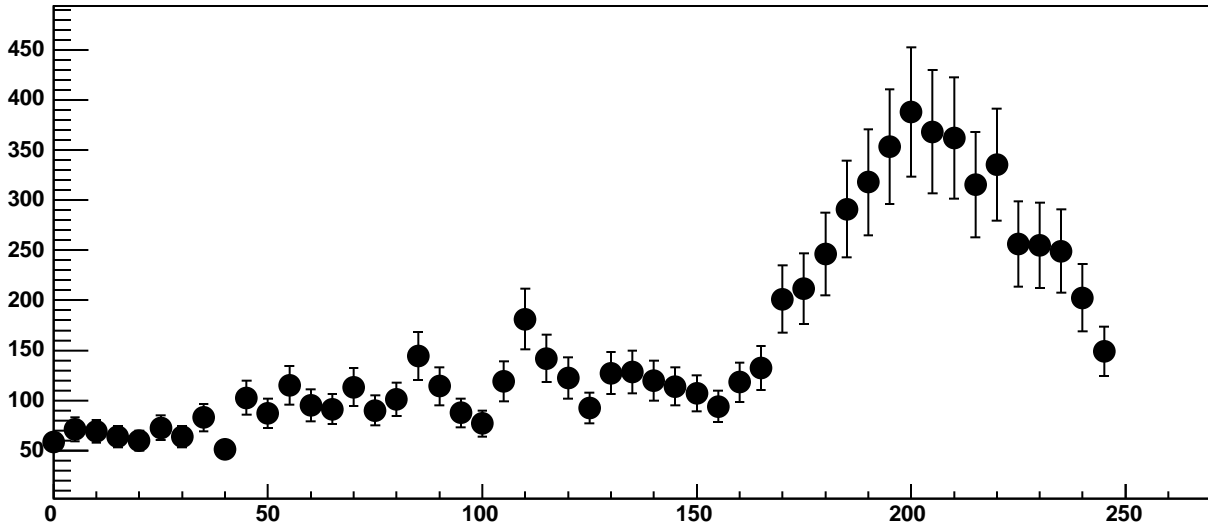


Chip 1, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

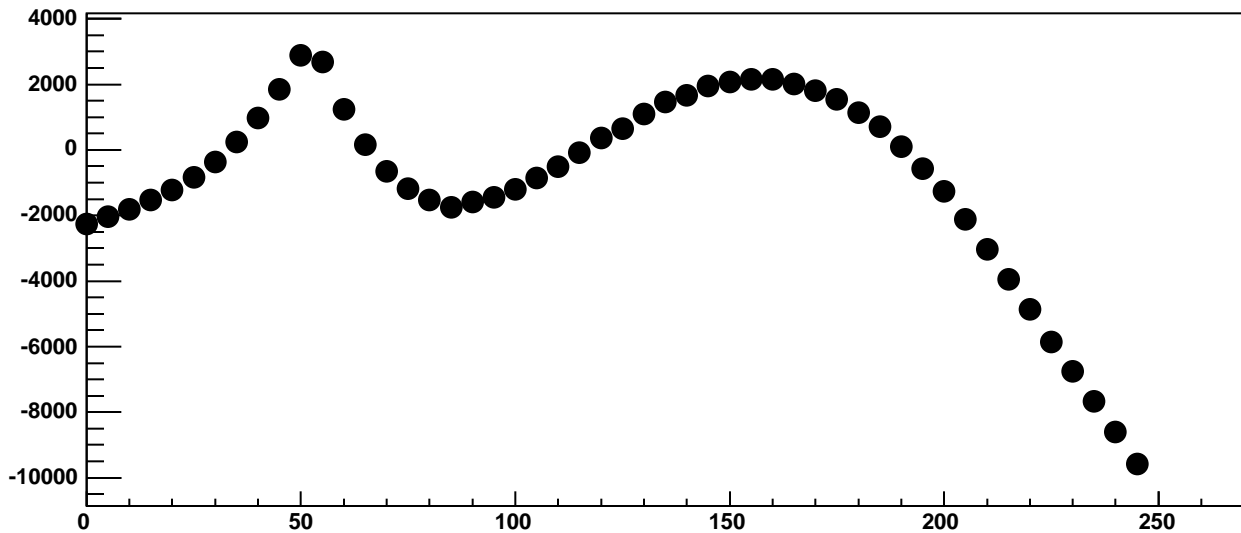


$\chi^2 / \text{ndf}$	2.254e+05 / 41
p0	-2051 ± 8.744
p1	52.75 ± 0.031
p2	3.221e+04 ± 70.04
p3	53.9 ± 0.117
p4	-53.74 ± 0.3484

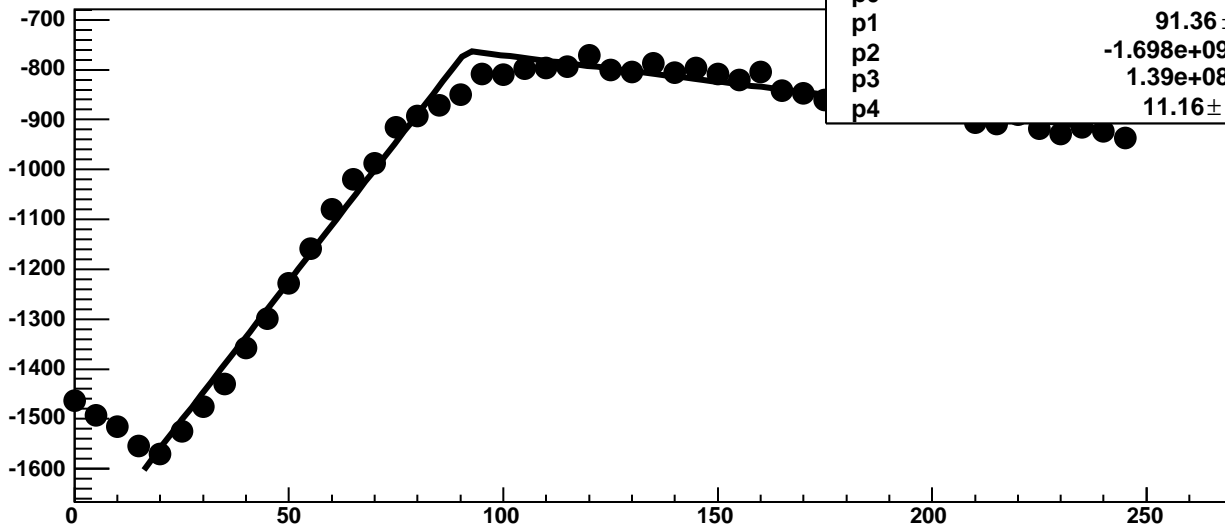
Chip 1, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

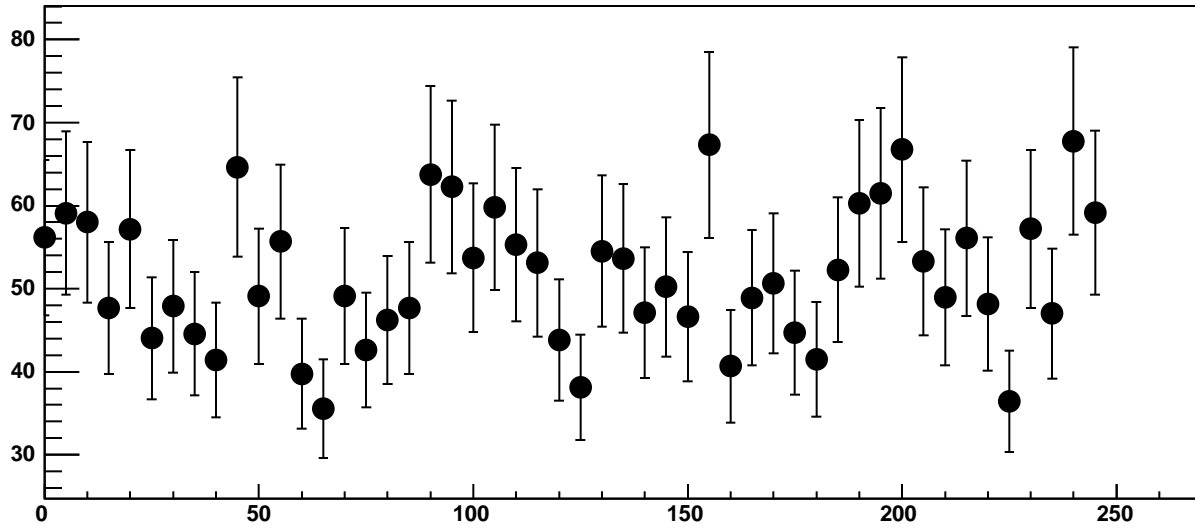


Chip 1, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

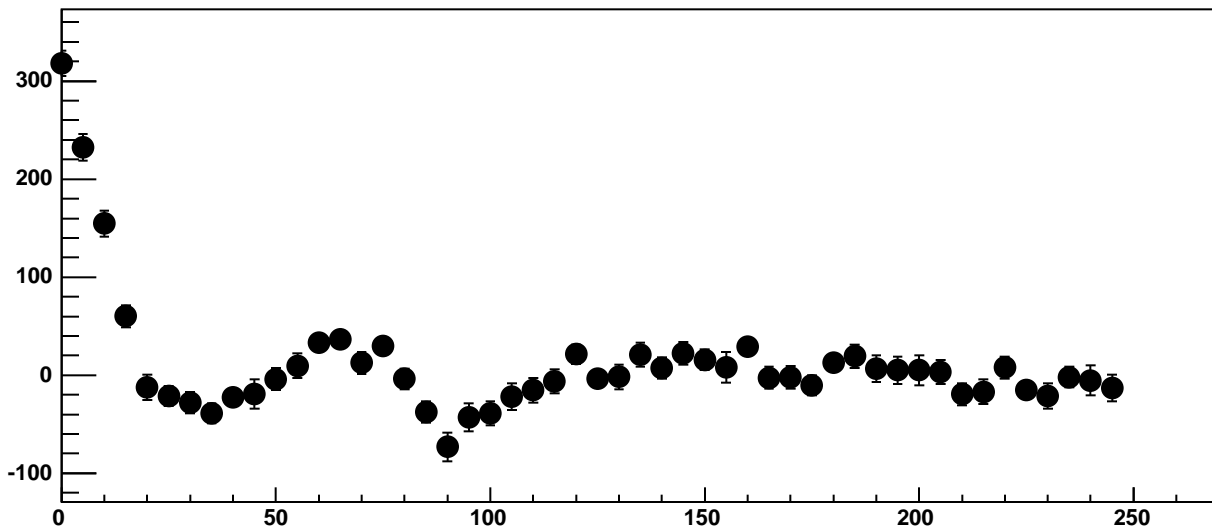


$\chi^2 / \text{ndf}$	210.7 / 41
p0	$-762.3 \pm 1.31$
p1	$91.36 \pm 0.3007$
p2	$-1.698\text{e}+09 \pm 1.414$
p3	$1.39\text{e}+08 \pm 1.414$
p4	$11.16 \pm 0.02823$

Chip 1, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

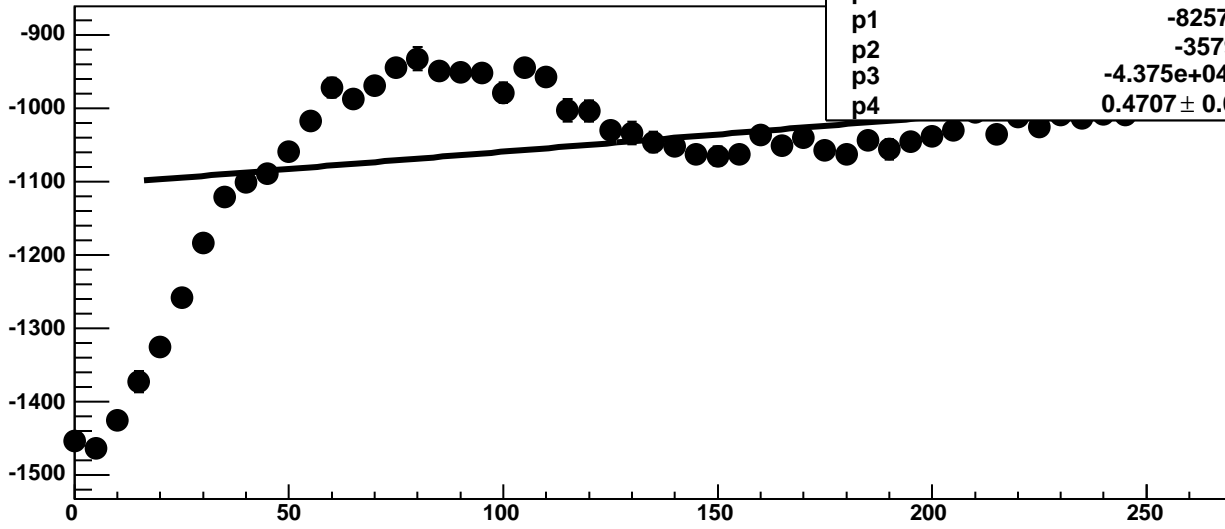


Chip 1, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



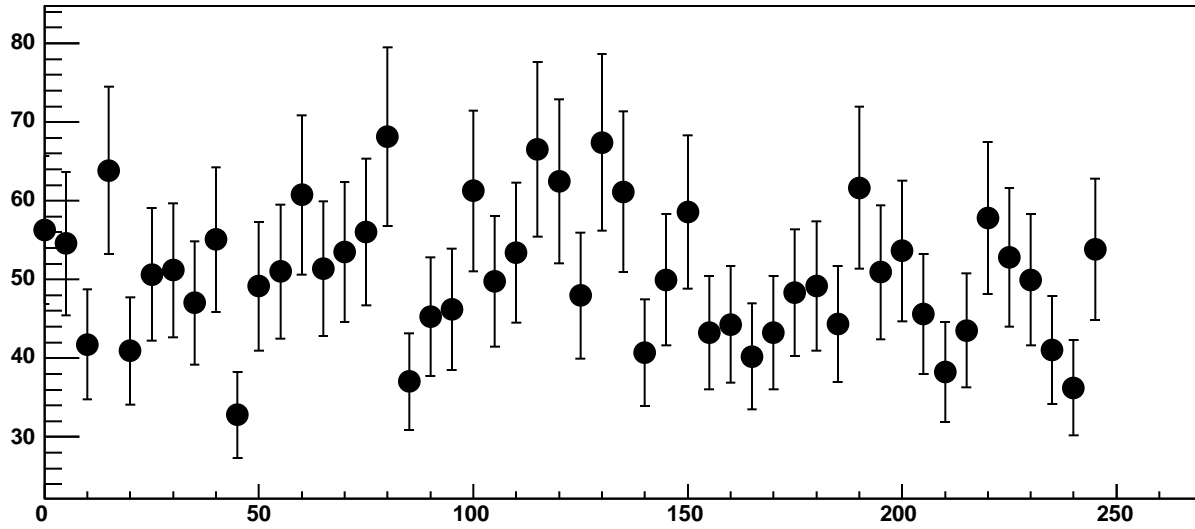


Chip 1, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold

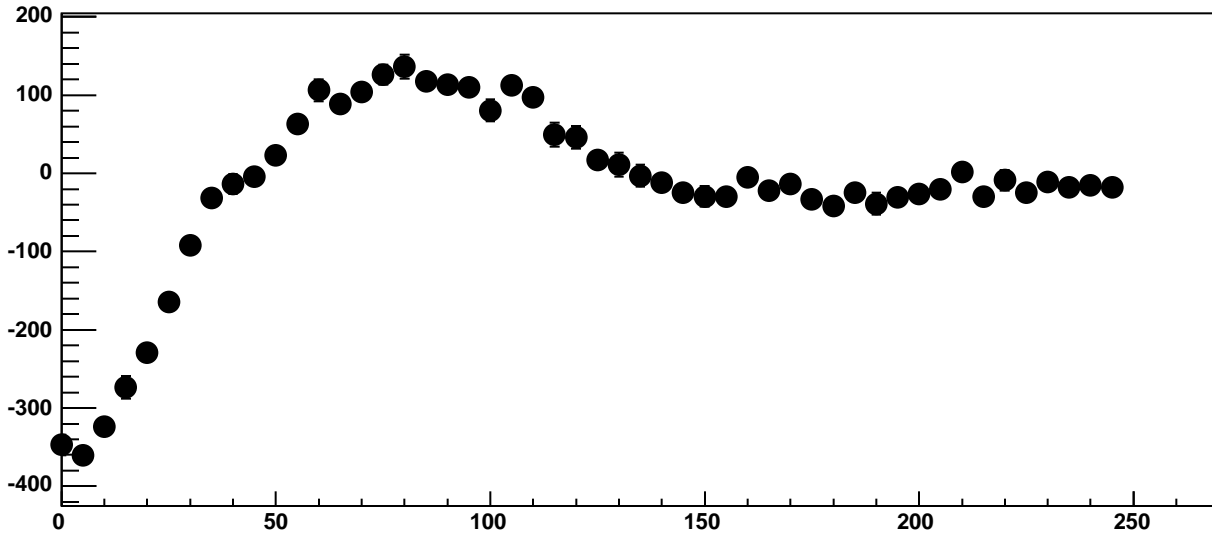


$\chi^2 / \text{ndf}$	2342 / 41
p0	-1414 ± 8.346
p1	-8257 ± 14.56
p2	-3579 ± 10.5
p3	-4.375e+04 ± 894.3
p4	0.4707 ± 0.0009949

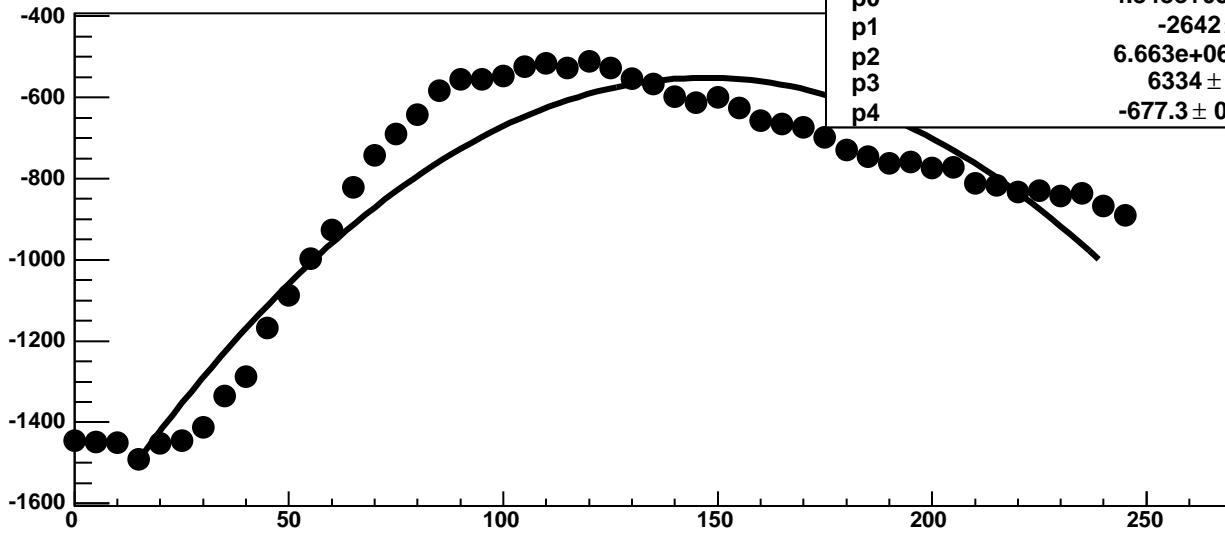
Chip 1, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



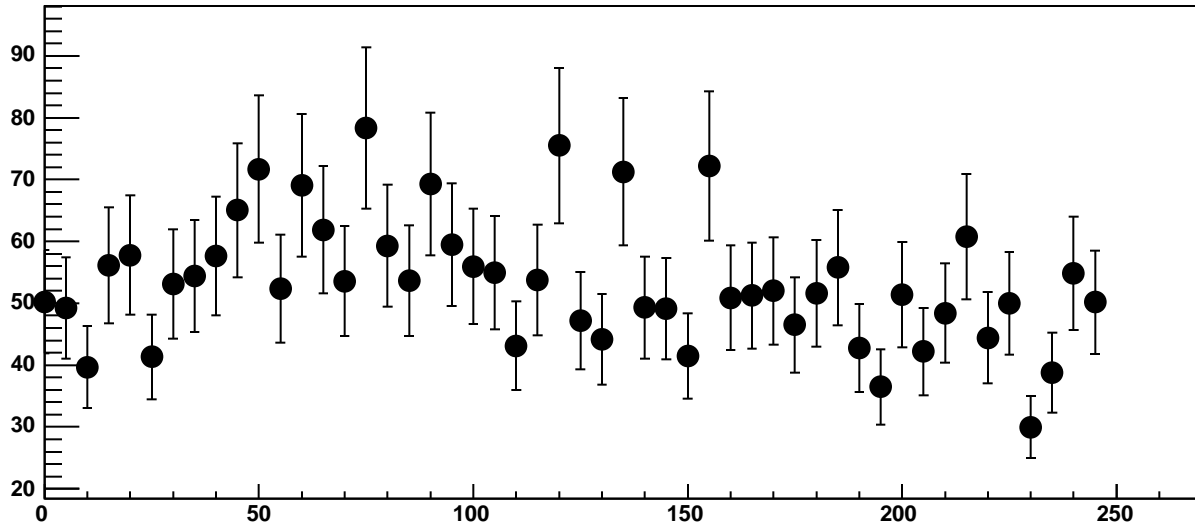
Chip 1, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold



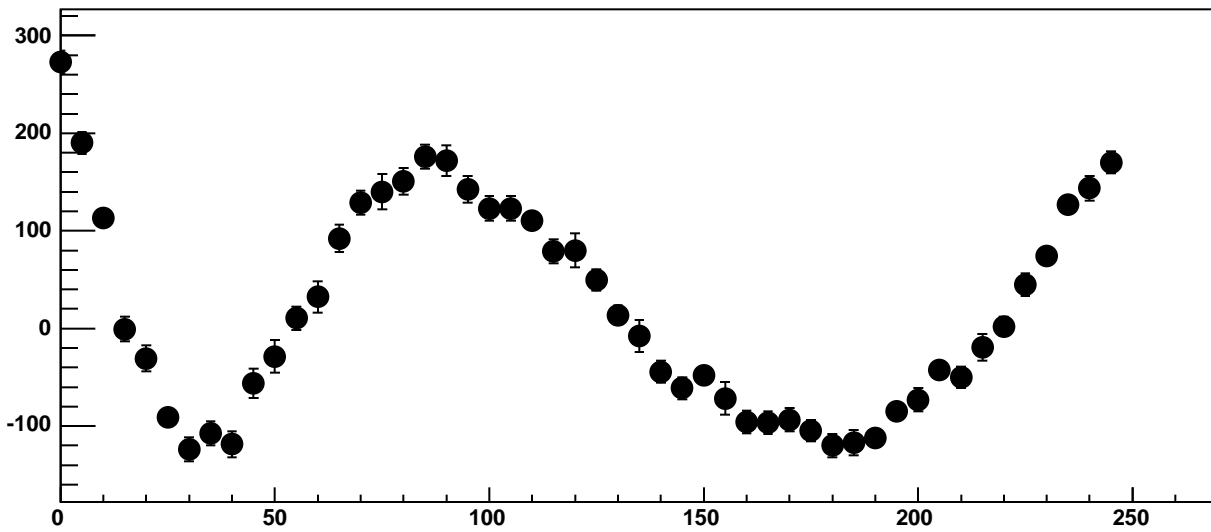
Chip 1, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold



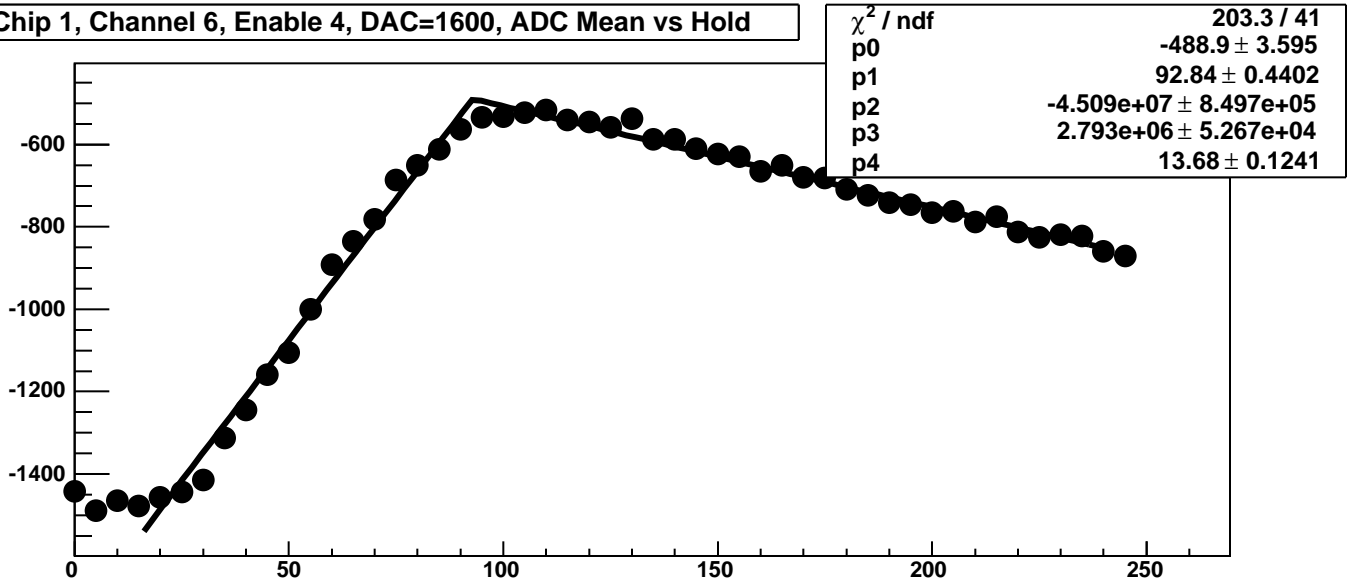
Chip 1, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



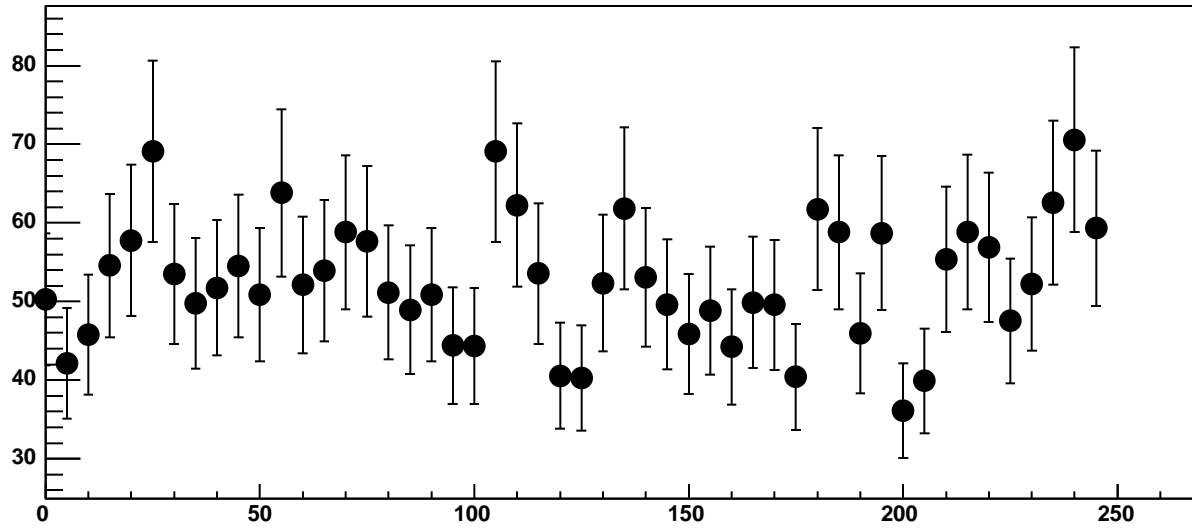
Chip 1, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold



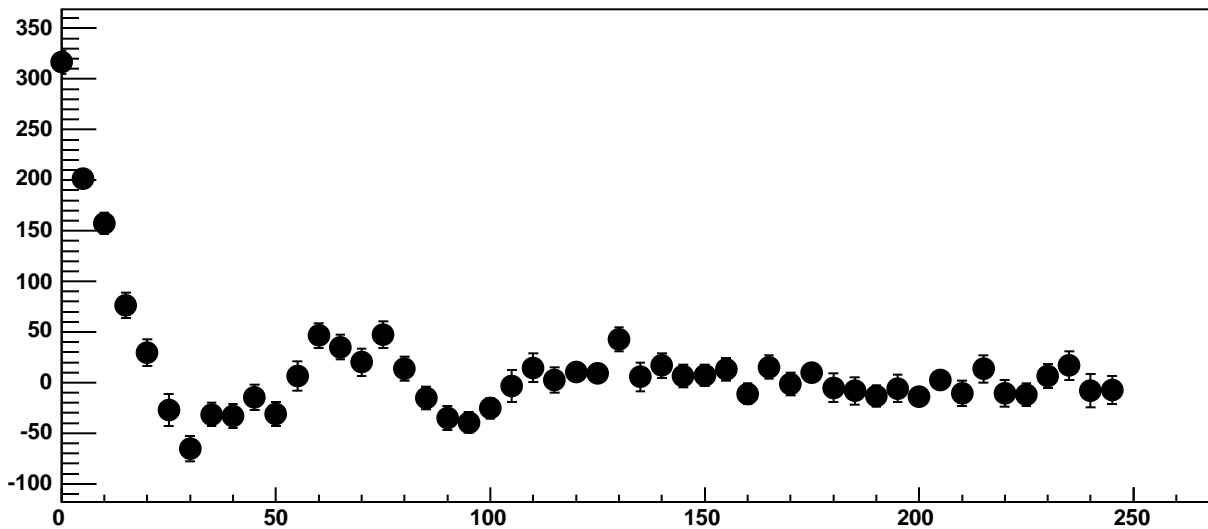
Chip 1, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold



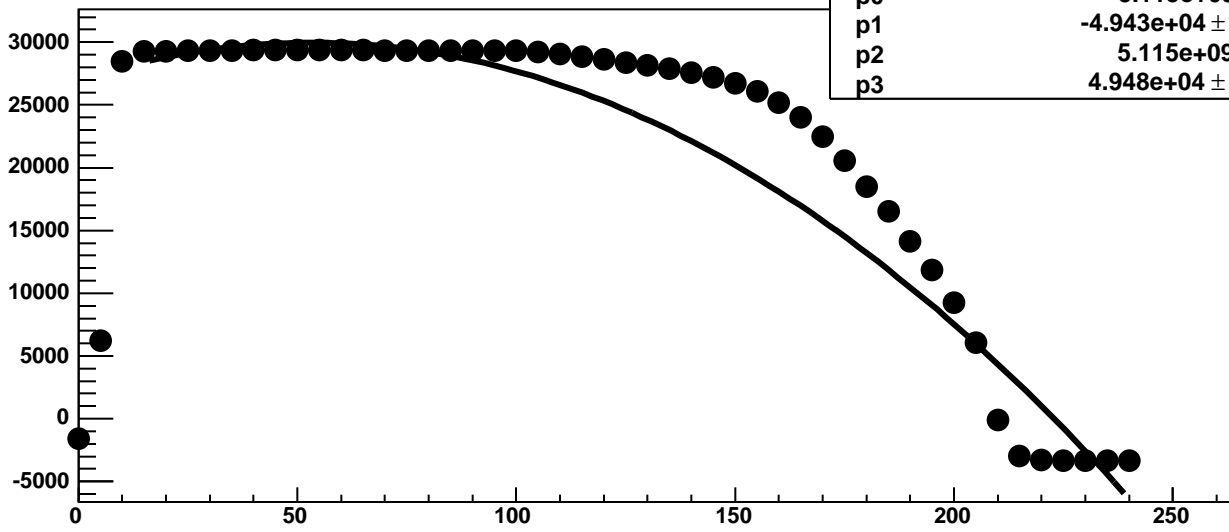
Chip 1, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

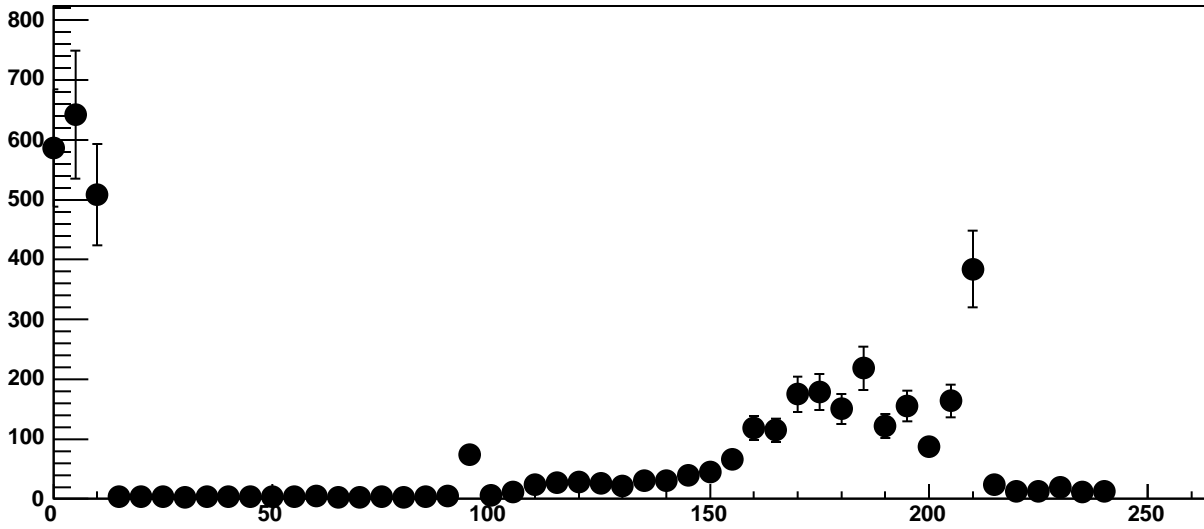


Chip 1, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

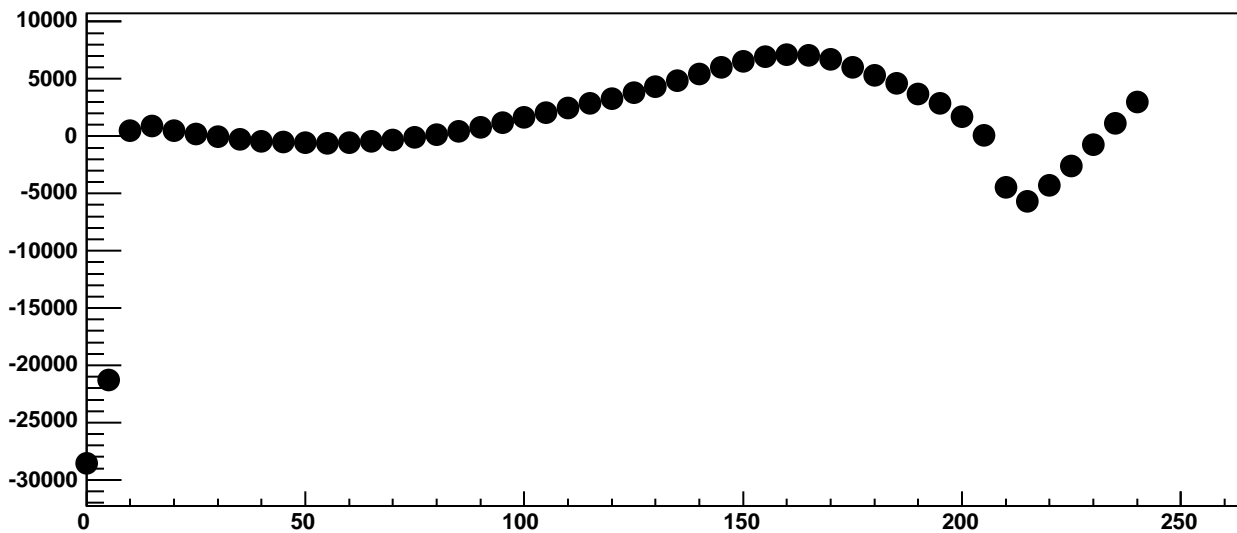


$\chi^2 / \text{ndf}$	1.628e+07 / 42
p0	-5.115e+09 ± 2.982
p1	-4.943e+04 ± 0.03736
p2	5.115e+09 ± 2.982
p3	4.948e+04 ± 0.03729

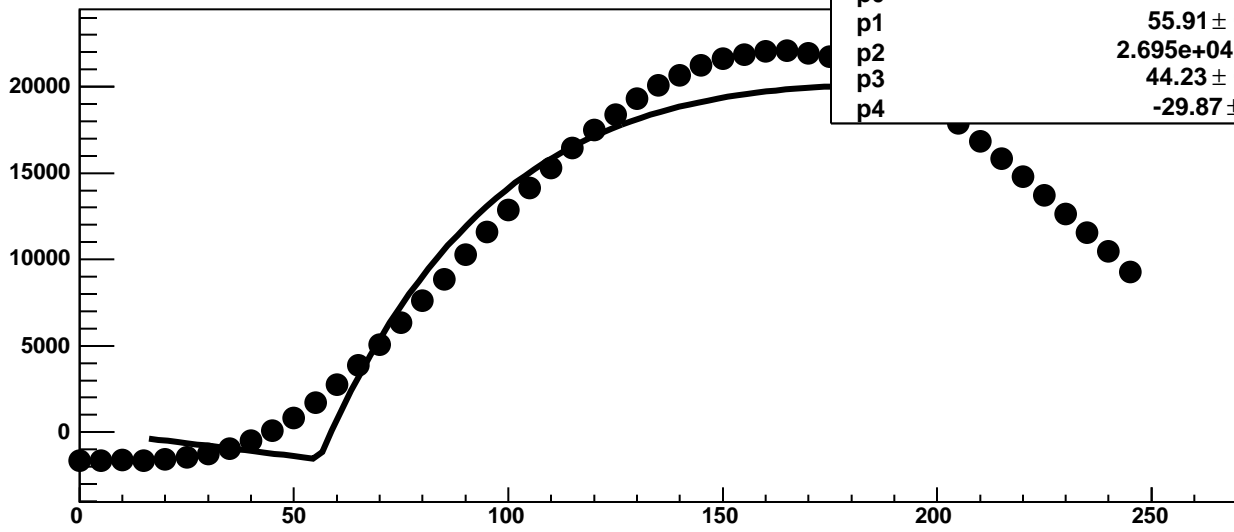
Chip 1, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold

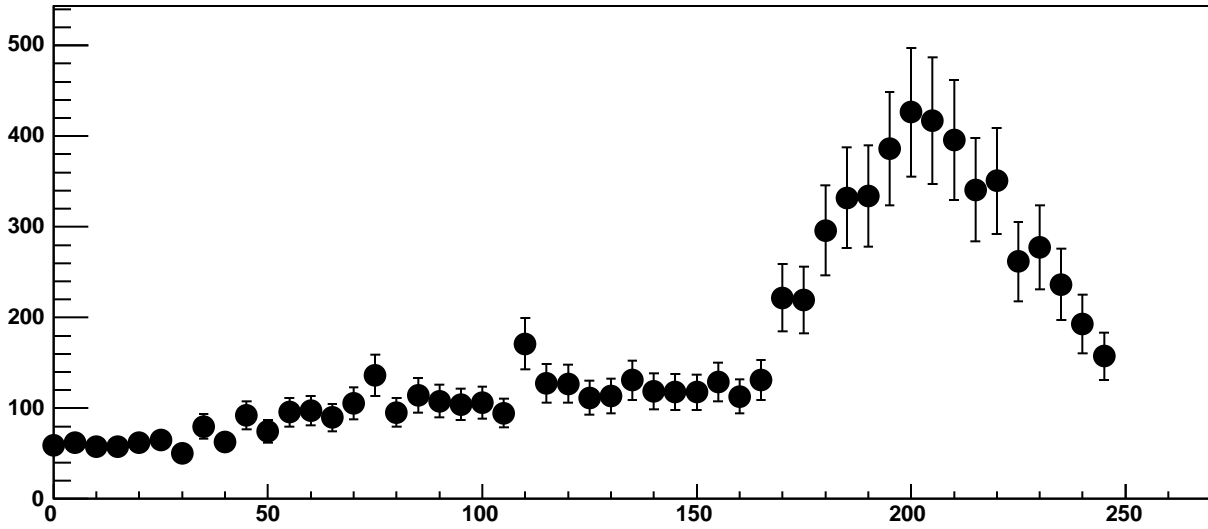


Chip 1, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

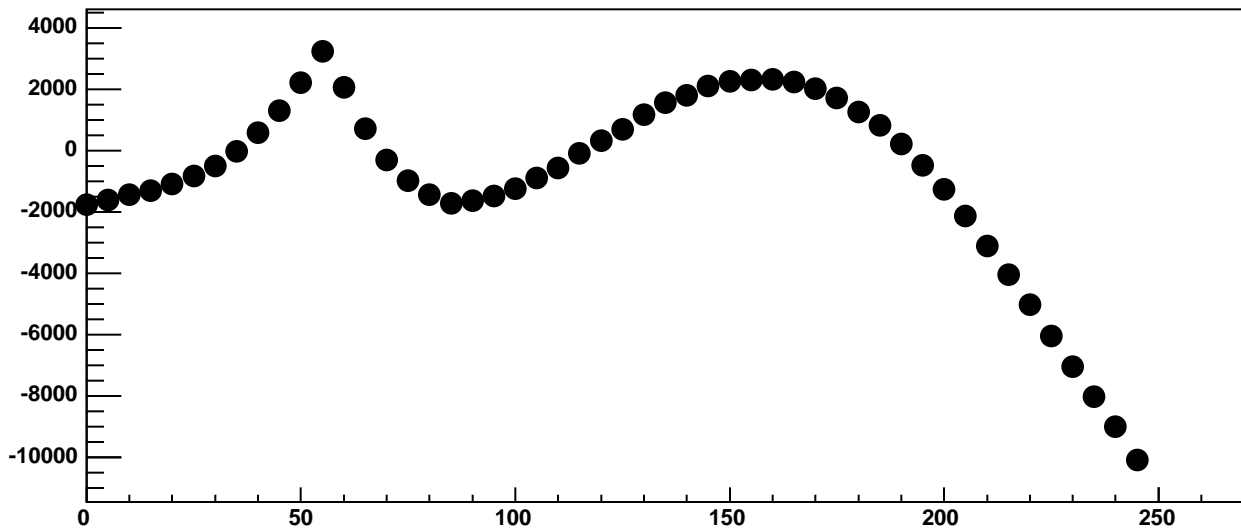


$\chi^2 / \text{ndf}$	2.364e+05 / 41
p0	-1563 ± 8.462
p1	55.91 ± 0.03244
p2	2.695e+04 ± 54.23
p3	44.23 ± 0.09929
p4	-29.87 ± 0.2959

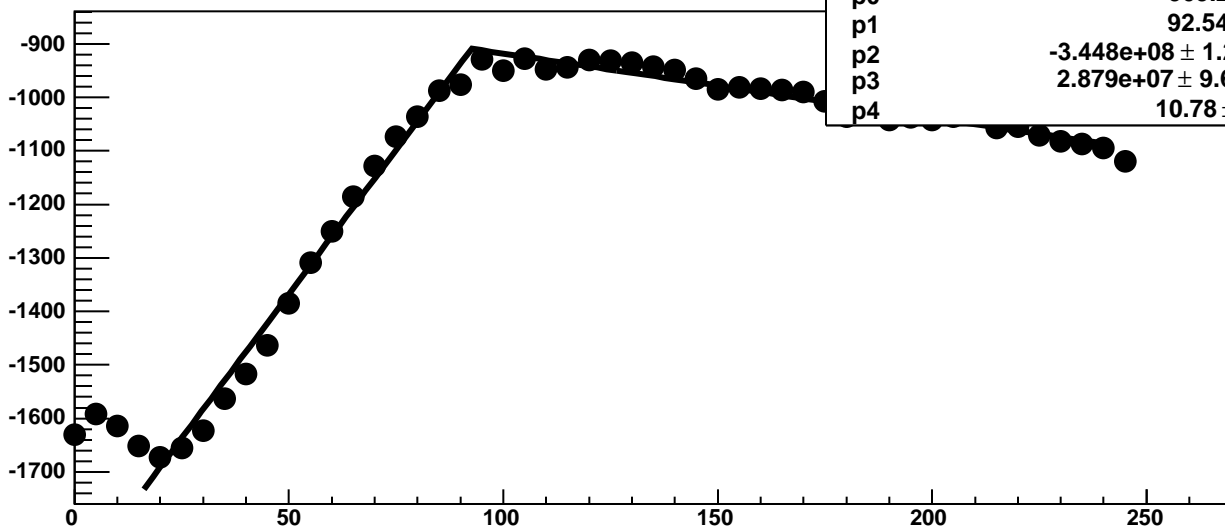
Chip 1, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

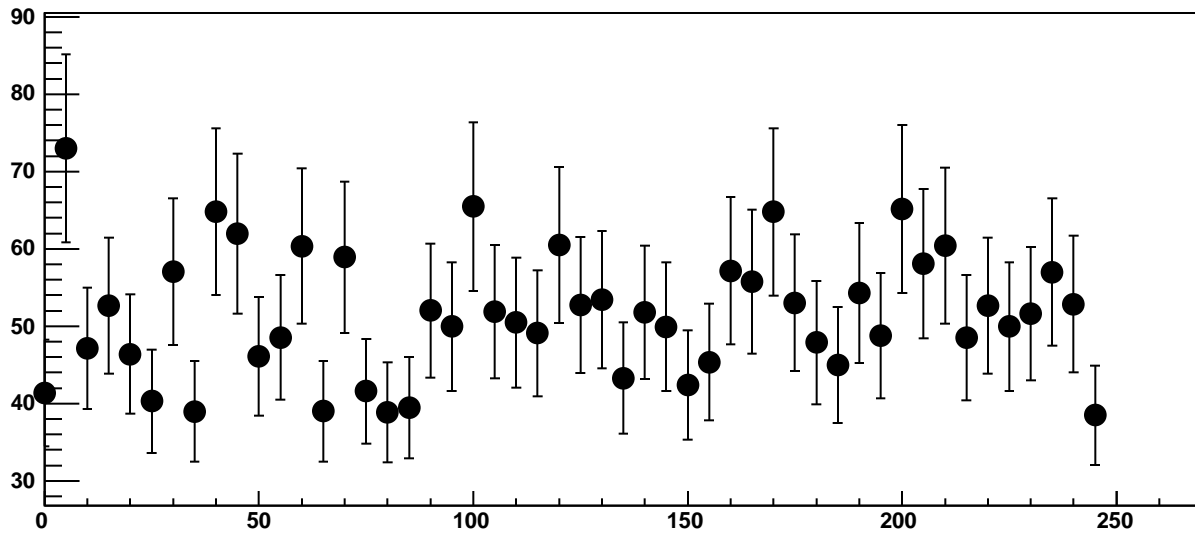


Chip 1, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

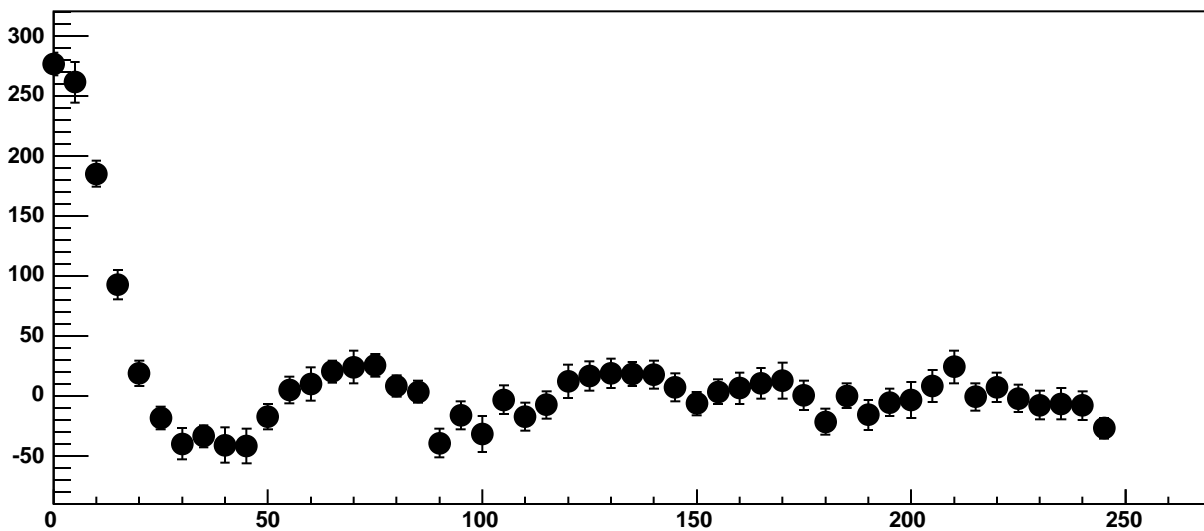


$\chi^2 / \text{ndf}$	169.7 / 41
p0	$-909.2 \pm 3.973$
p1	$92.54 \pm 0.562$
p2	$-3.448\text{e}+08 \pm 1.218\text{e}+07$
p3	$2.879\text{e}+07 \pm 9.675\text{e}+05$
p4	$10.78 \pm 0.1138$

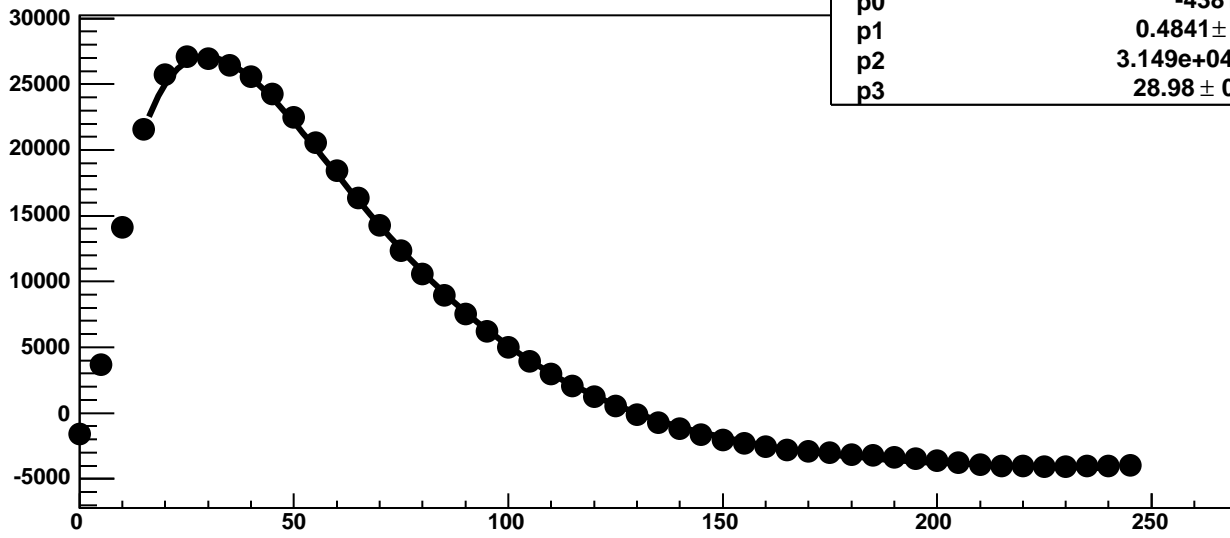
Chip 1, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



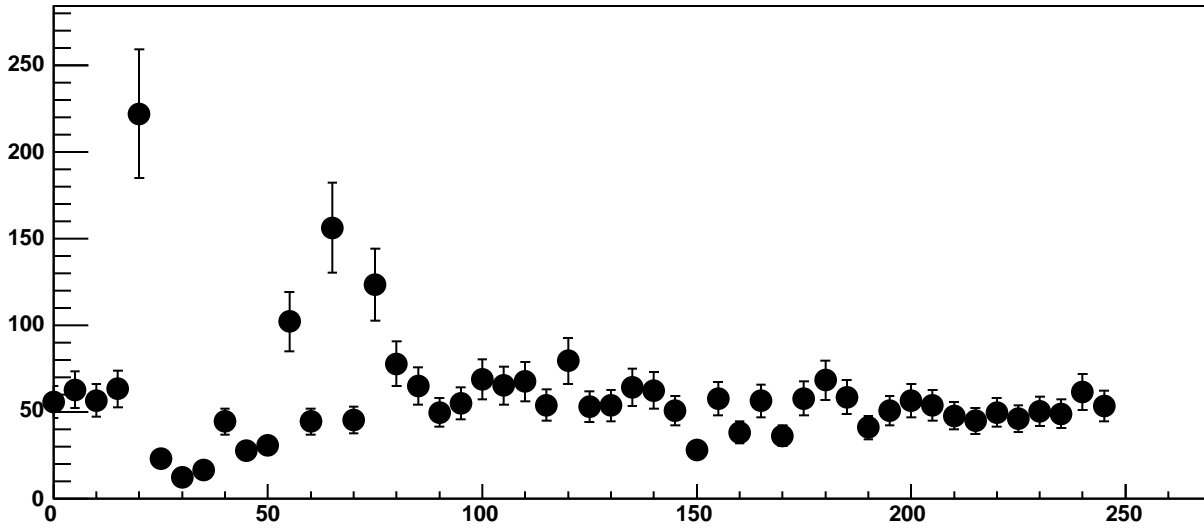
Chip 1, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold



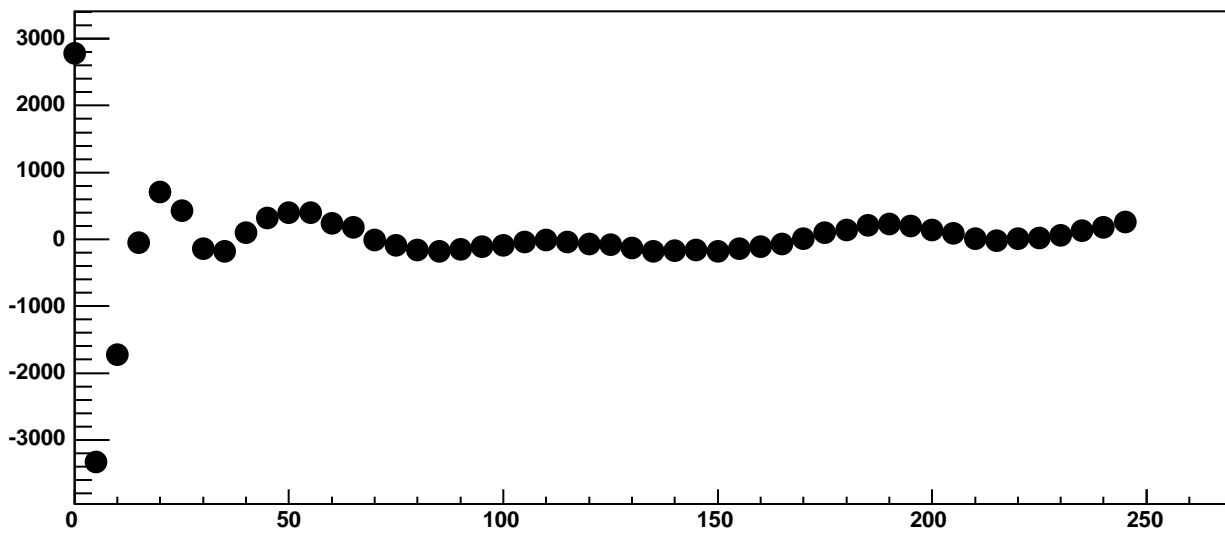
Chip 1, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold



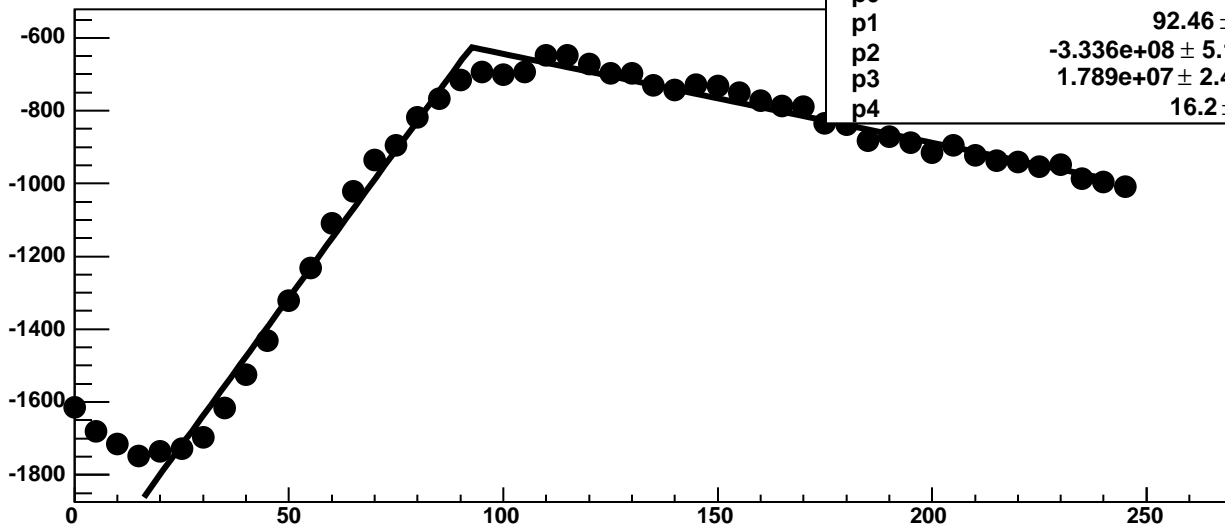
Chip 1, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold

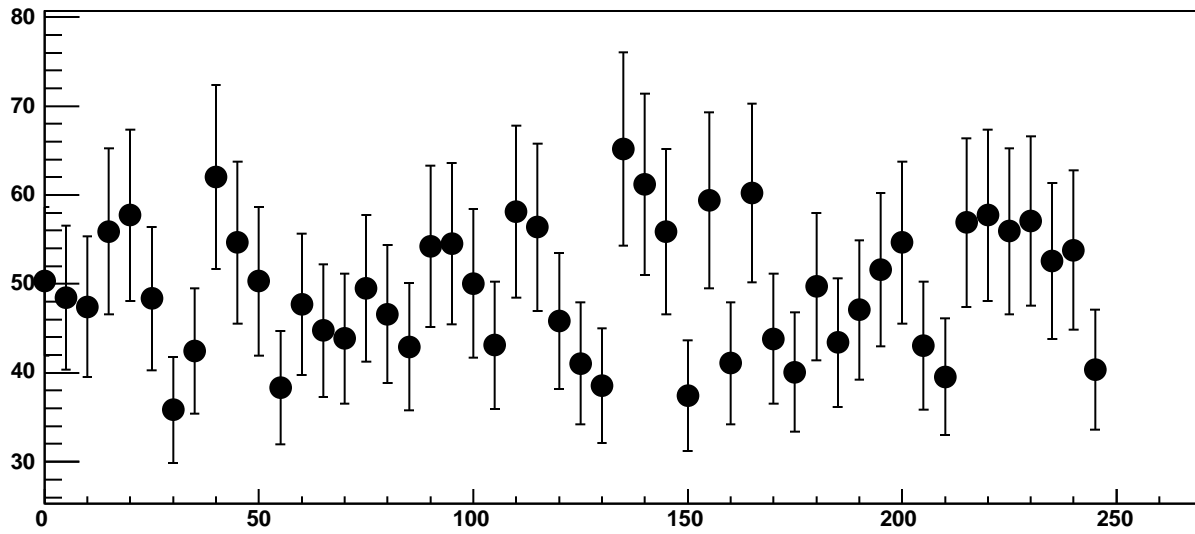


Chip 1, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

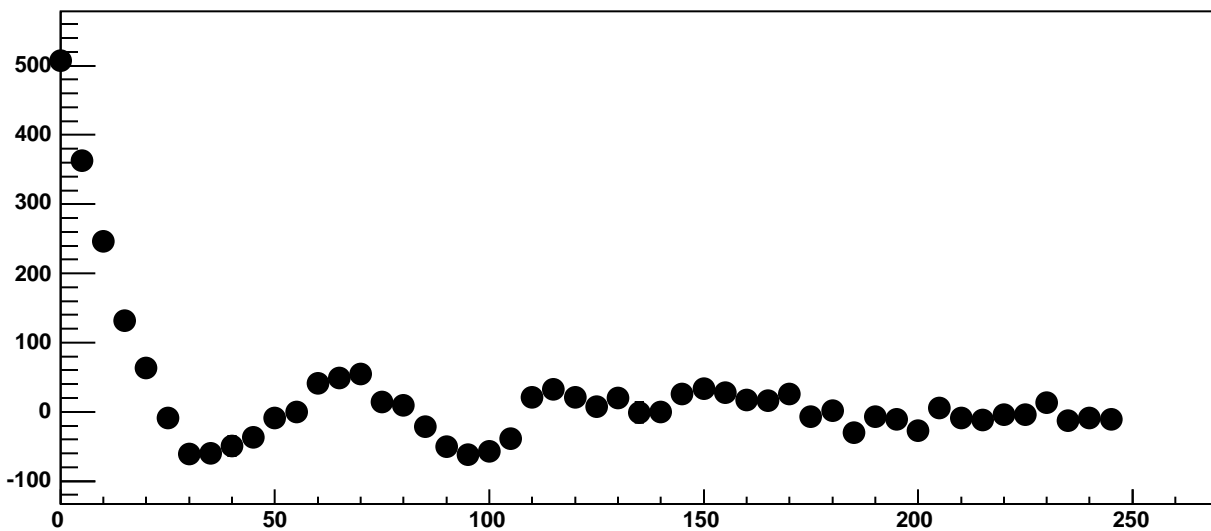


$\chi^2 / \text{ndf}$	469.6 / 41
p0	$-625.2 \pm 3.681$
p1	$92.46 \pm 0.3686$
p2	$-3.336\text{e}+08 \pm 5.113\text{e}+06$
p3	$1.789\text{e}+07 \pm 2.436\text{e}+05$
p4	$16.2 \pm 0.1213$

Chip 1, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

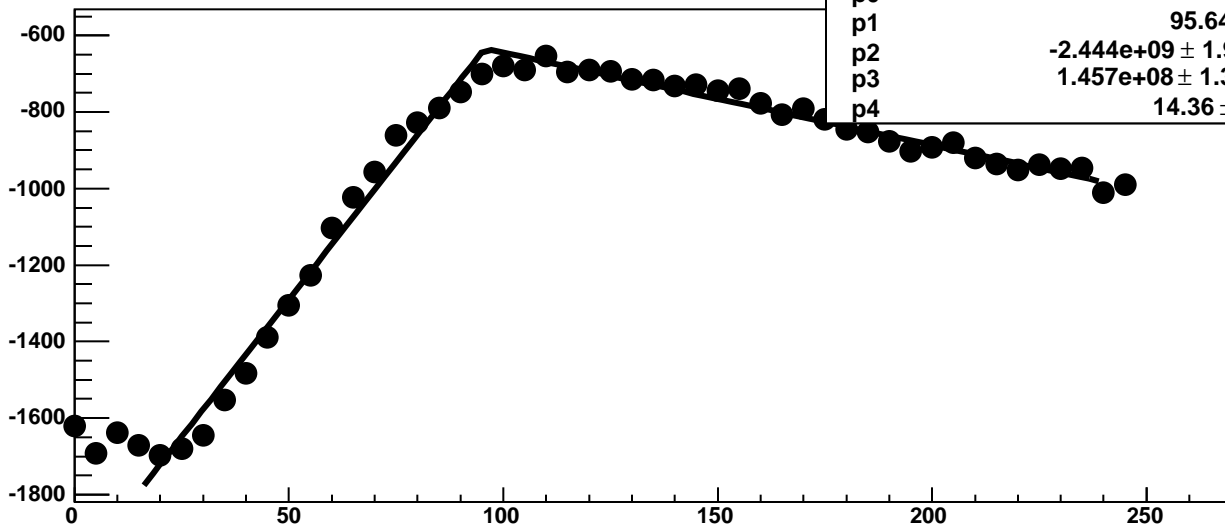


Chip 1, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

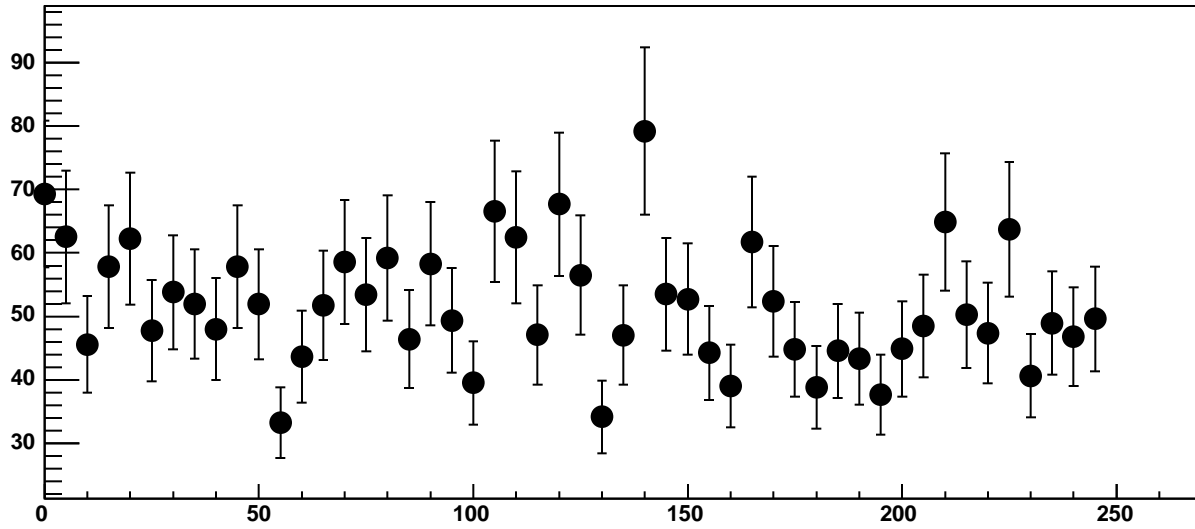




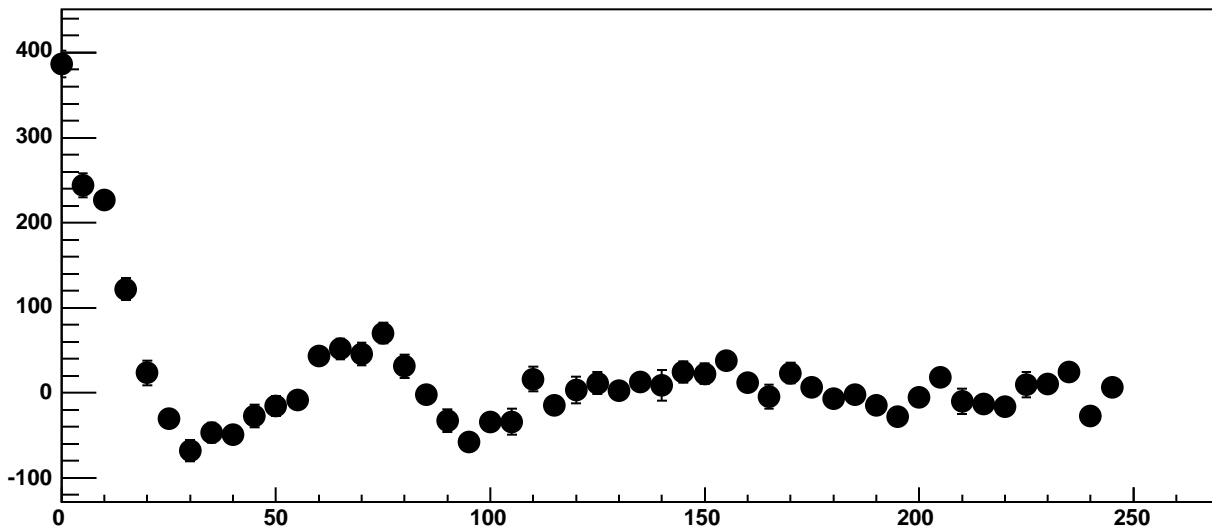
Chip 1, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold



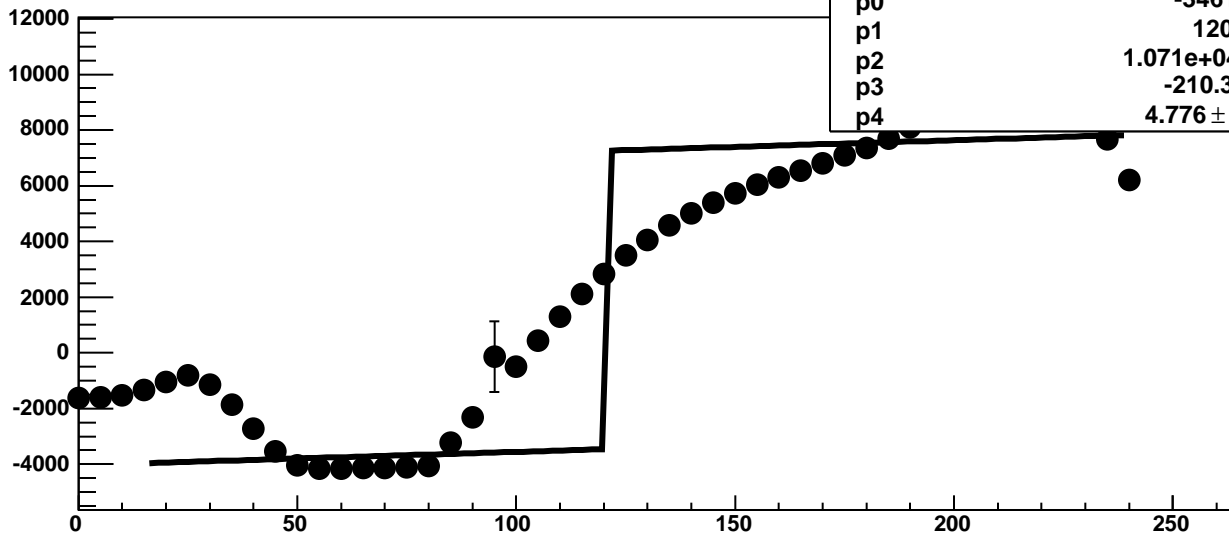
Chip 1, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



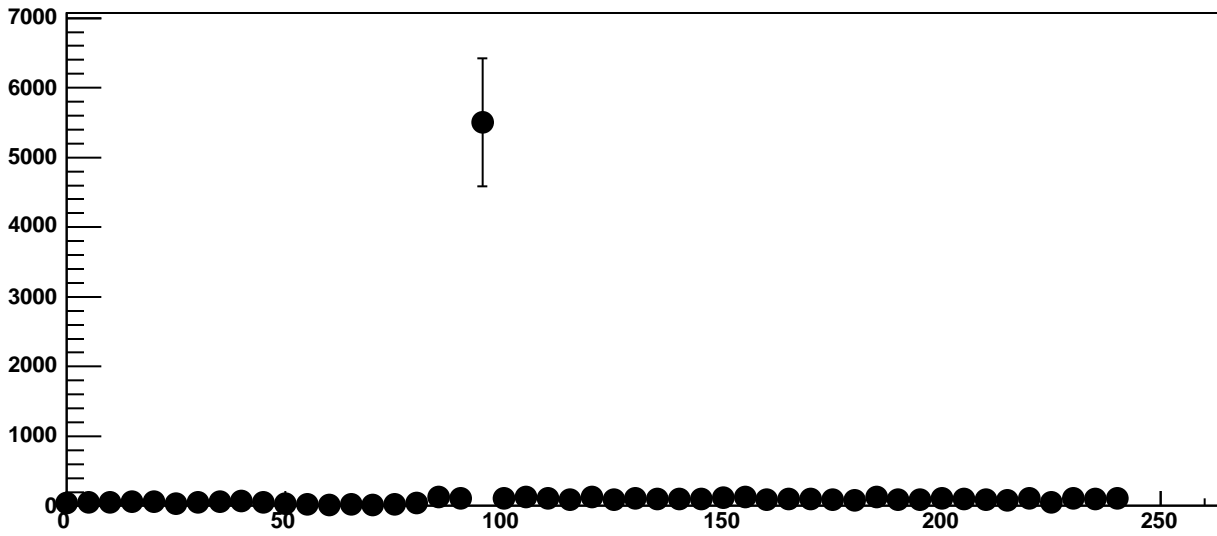
Chip 1, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold



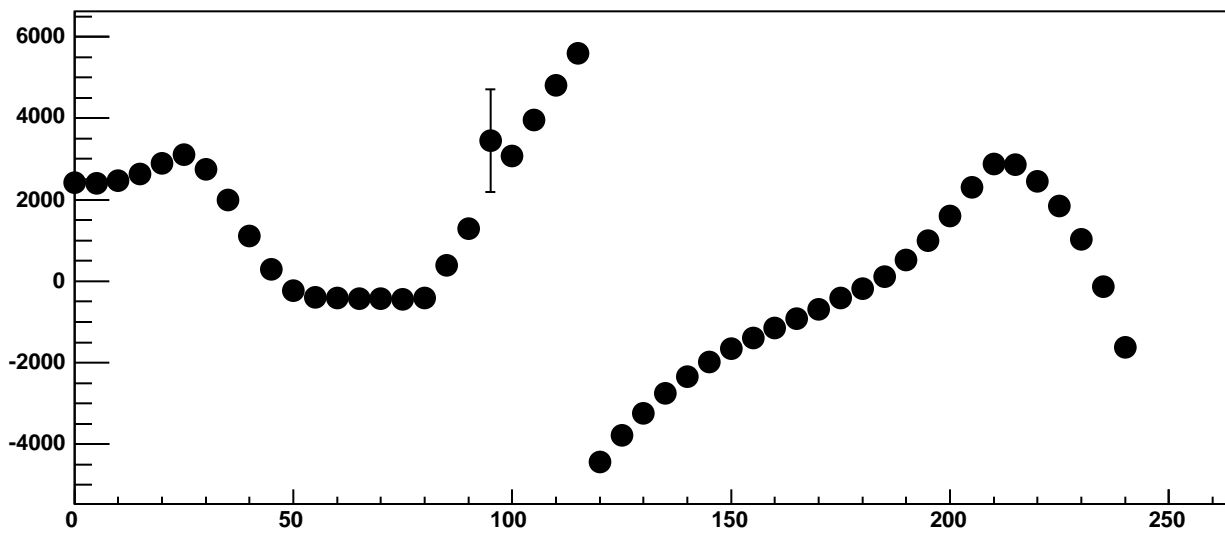
Chip 1, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold



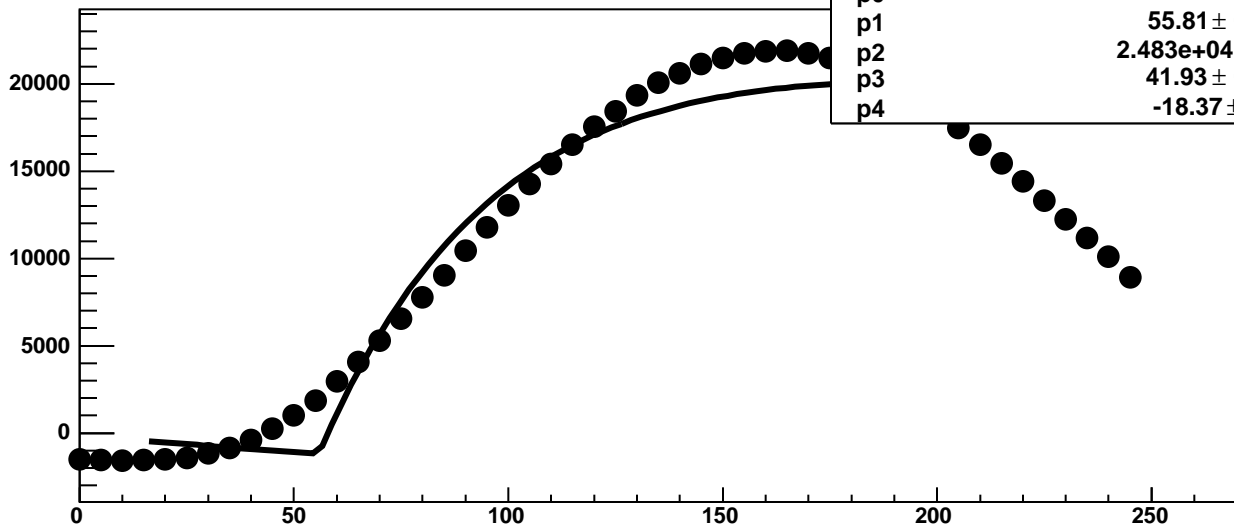
Chip 1, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold

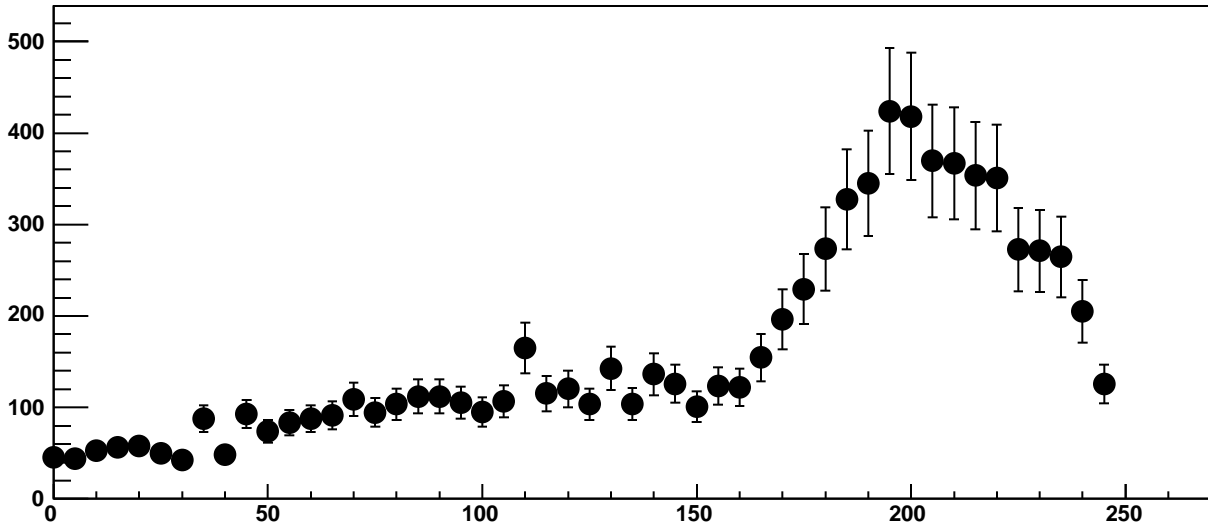


Chip 1, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

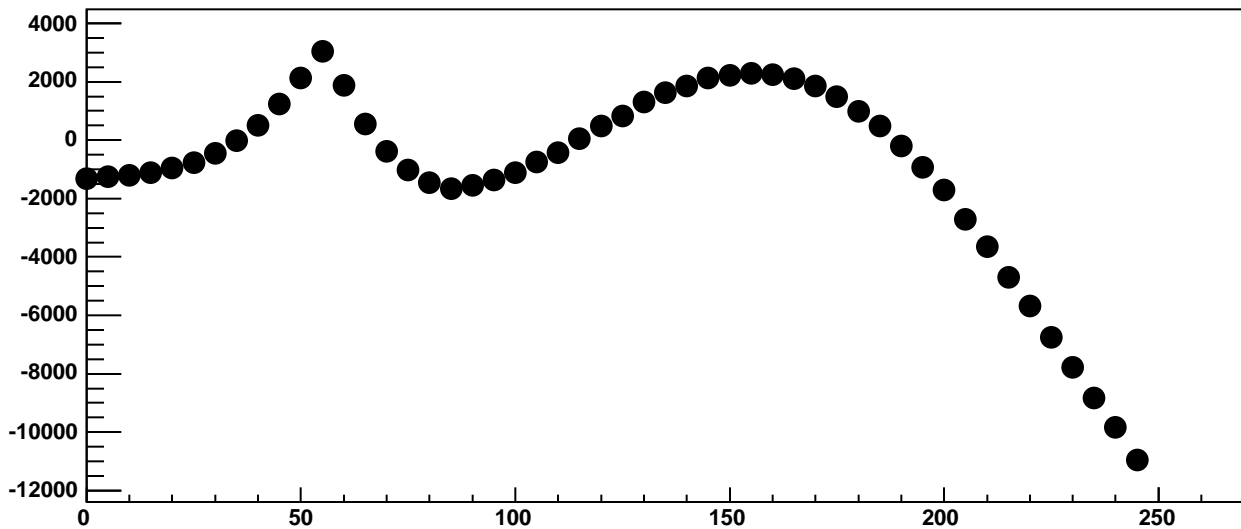


$\chi^2 / \text{ndf}$	2.453e+05 / 41
p0	-1203 ± 7.843
p1	55.81 ± 0.03184
p2	2.483e+04 ± 48.84
p3	41.93 ± 0.09525
p4	-18.37 ± 0.2753

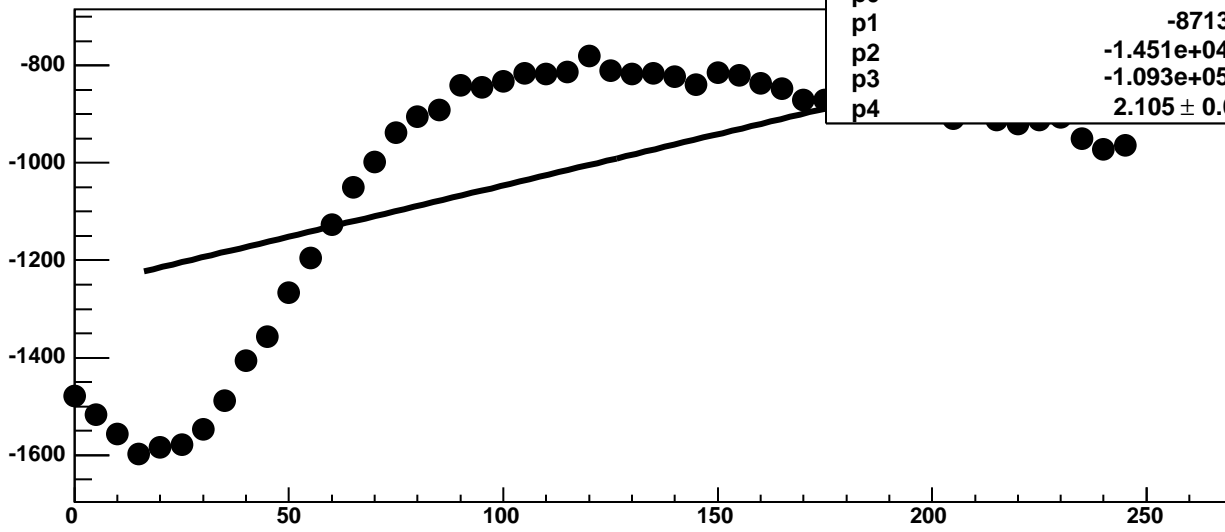
Chip 1, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

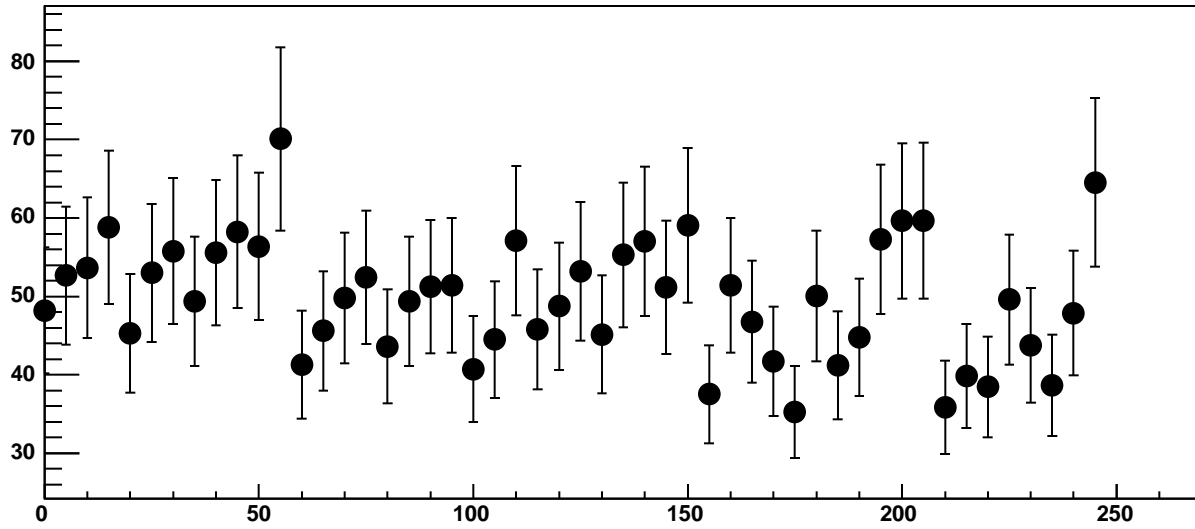


Chip 1, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

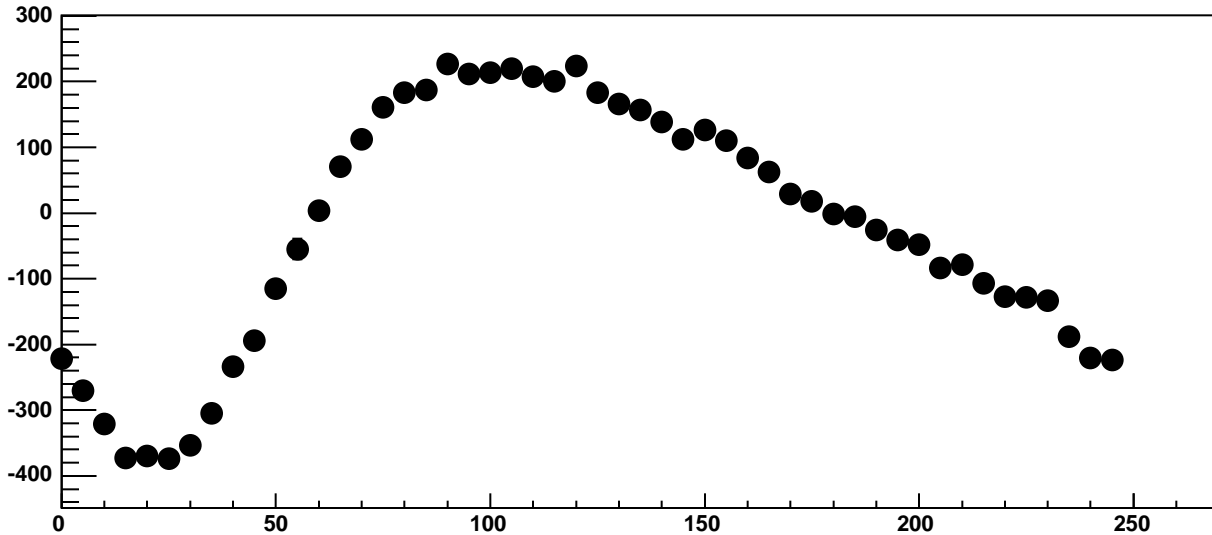


$\chi^2 / \text{ndf}$	1.158e+04 / 41
p0	-5087 ± 7.898
p1	-8713 ± 3.454
p2	-1.451e+04 ± 10.42
p3	-1.093e+05 ± 460.8
p4	2.105 ± 0.0008925

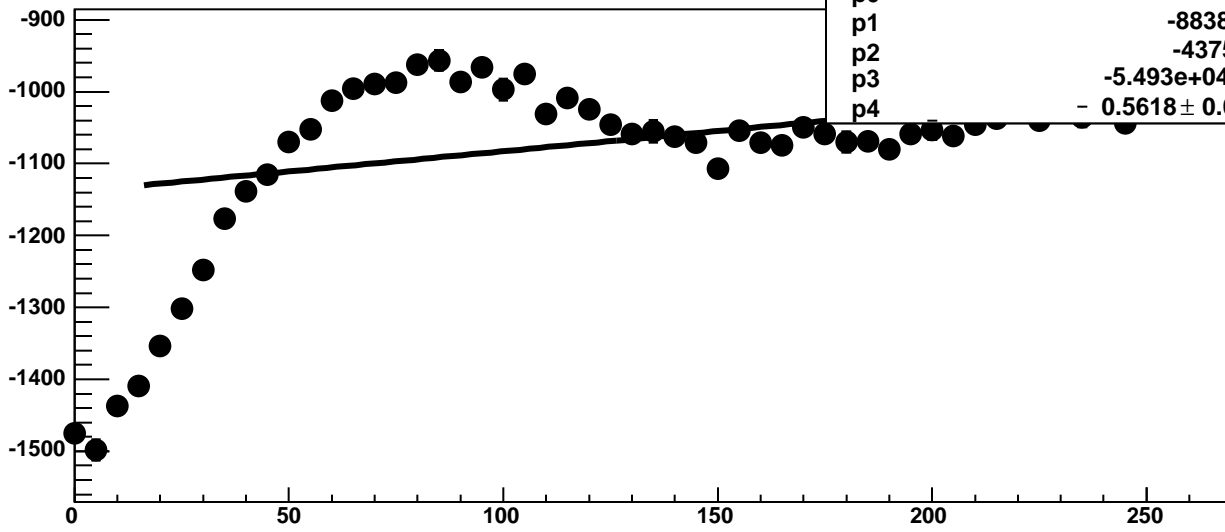
Chip 1, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

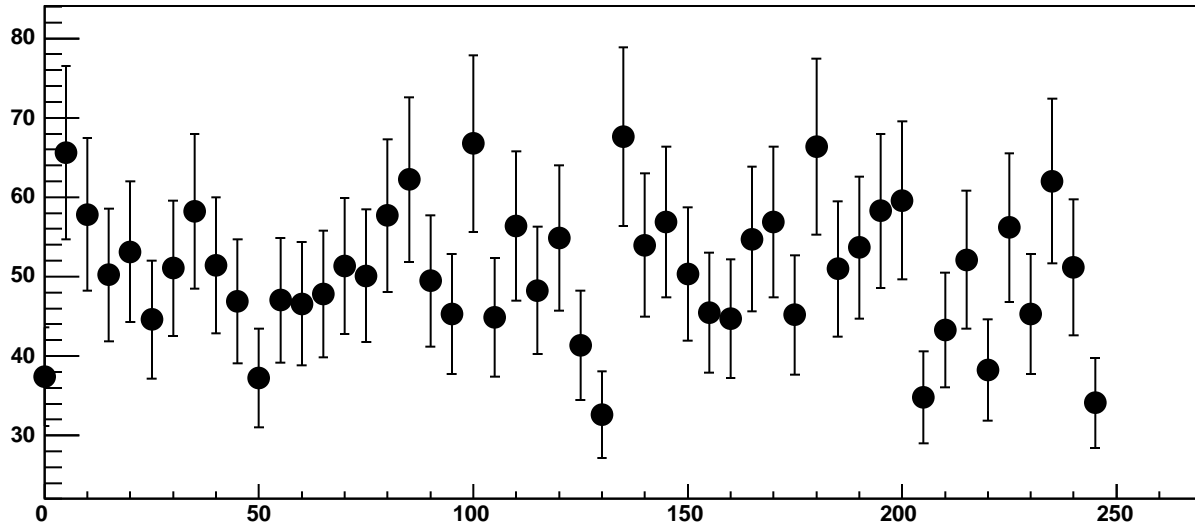


Chip 1, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold

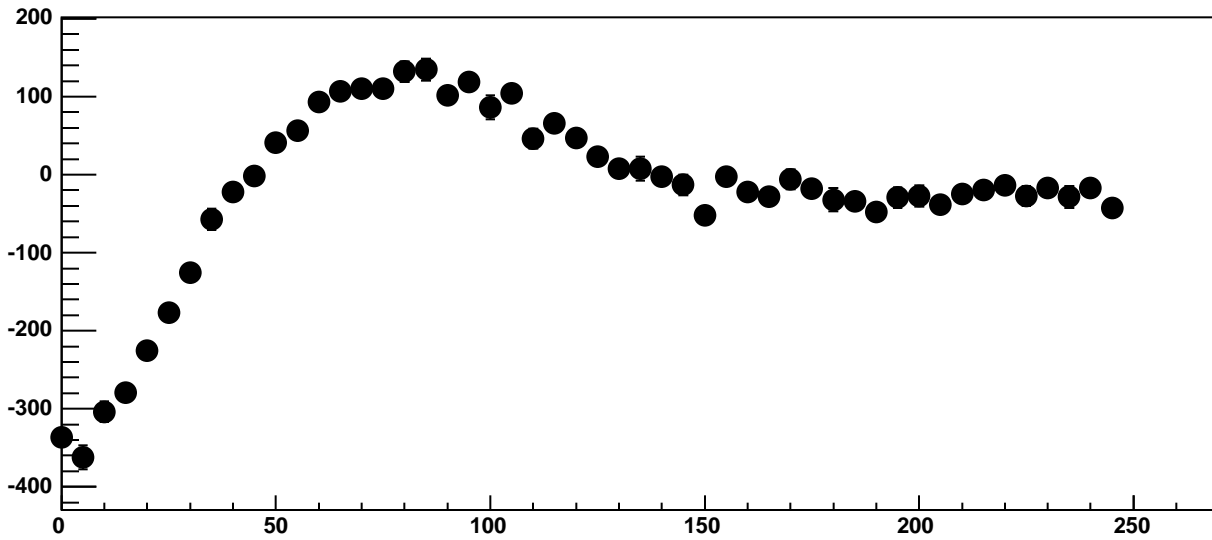


$\chi^2 / \text{ndf}$	2486 / 41
p0	-1729 ± 8.526
p1	-8838 ± 12.19
p2	-4375 ± 10.6
p3	-5.493e+04 ± 775.5
p4	-0.5618 ± 0.0009509

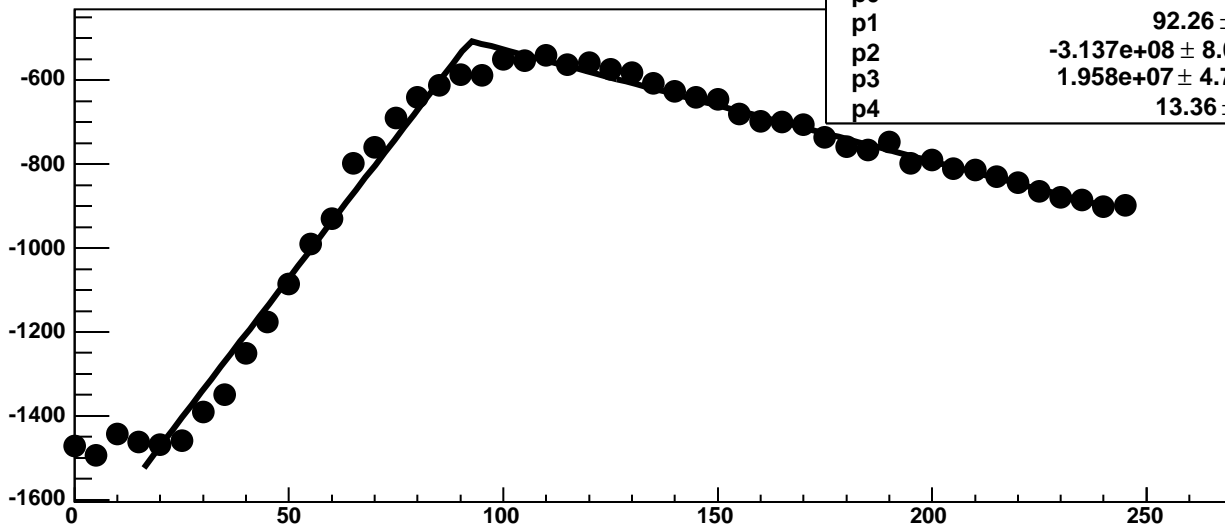
Chip 1, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



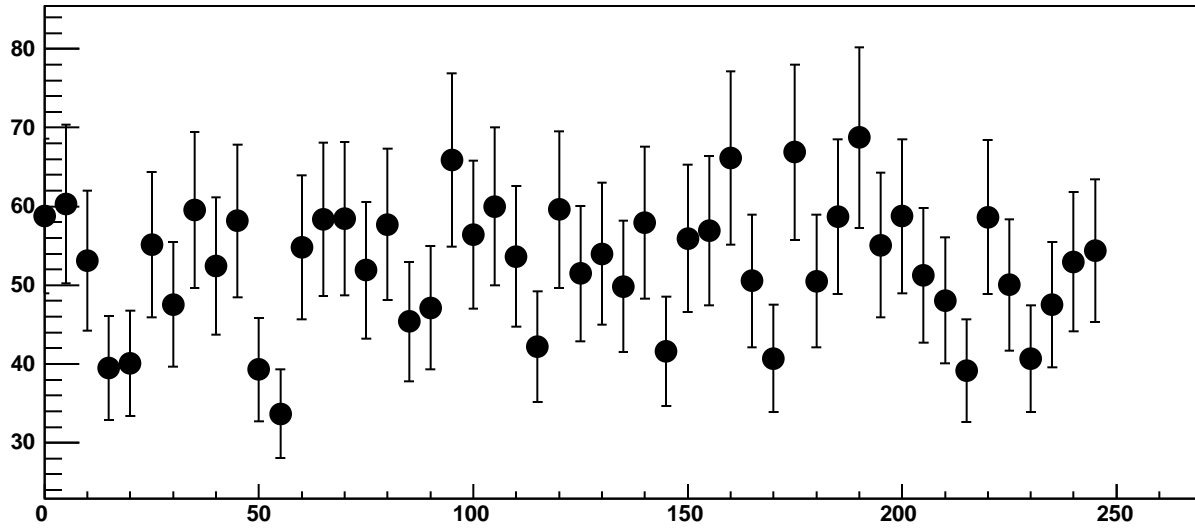
Chip 1, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold



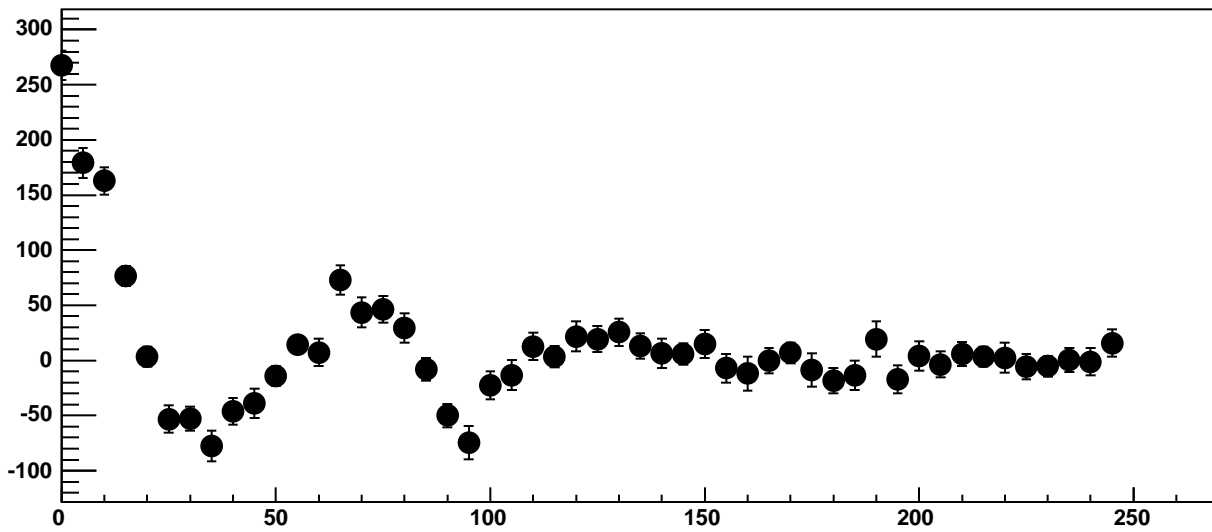
Chip 1, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold



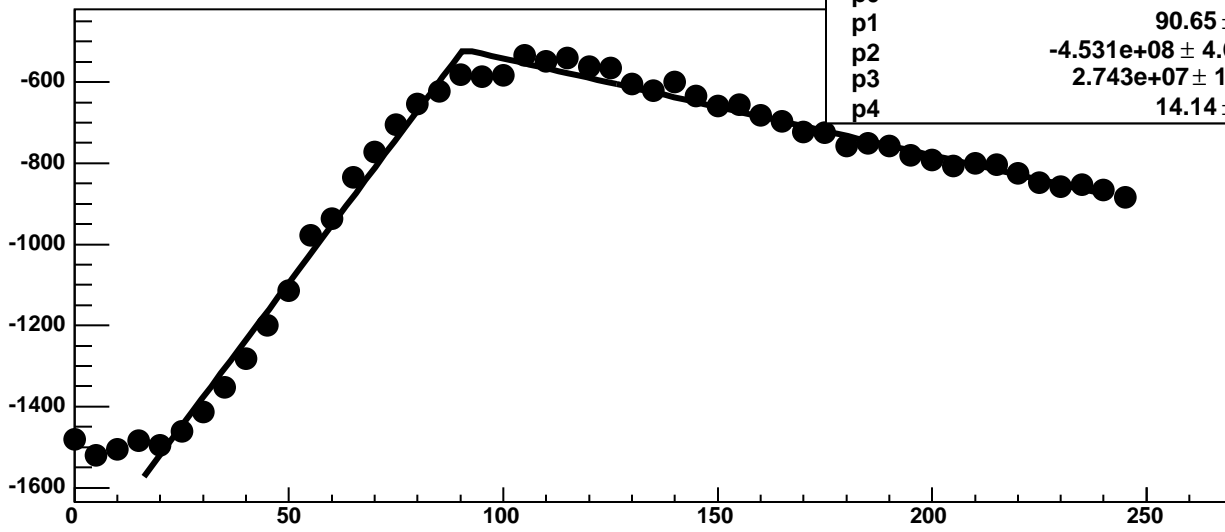
Chip 1, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

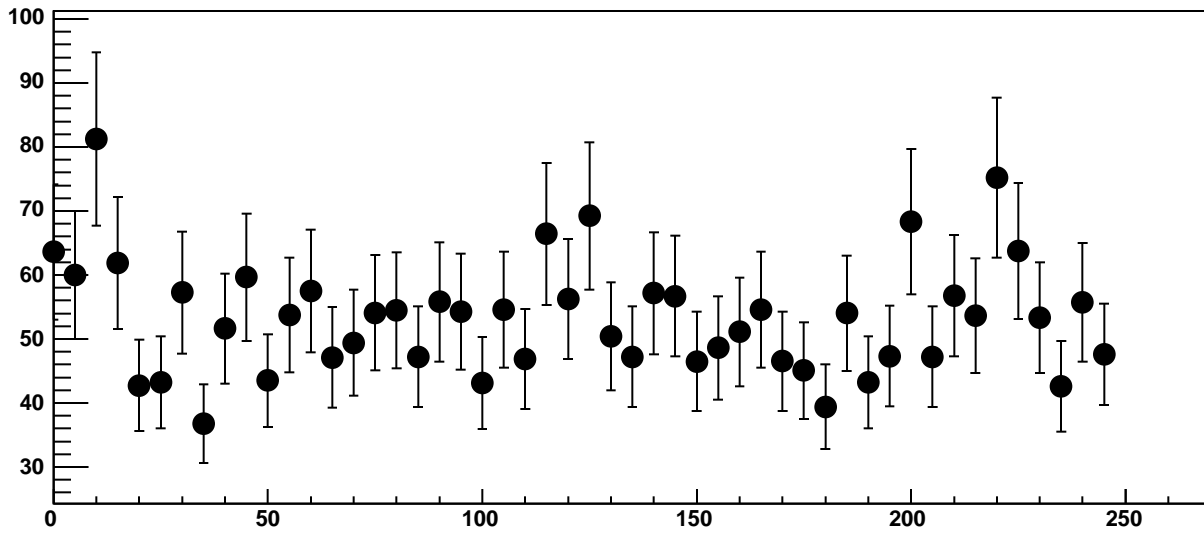


Chip 1, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

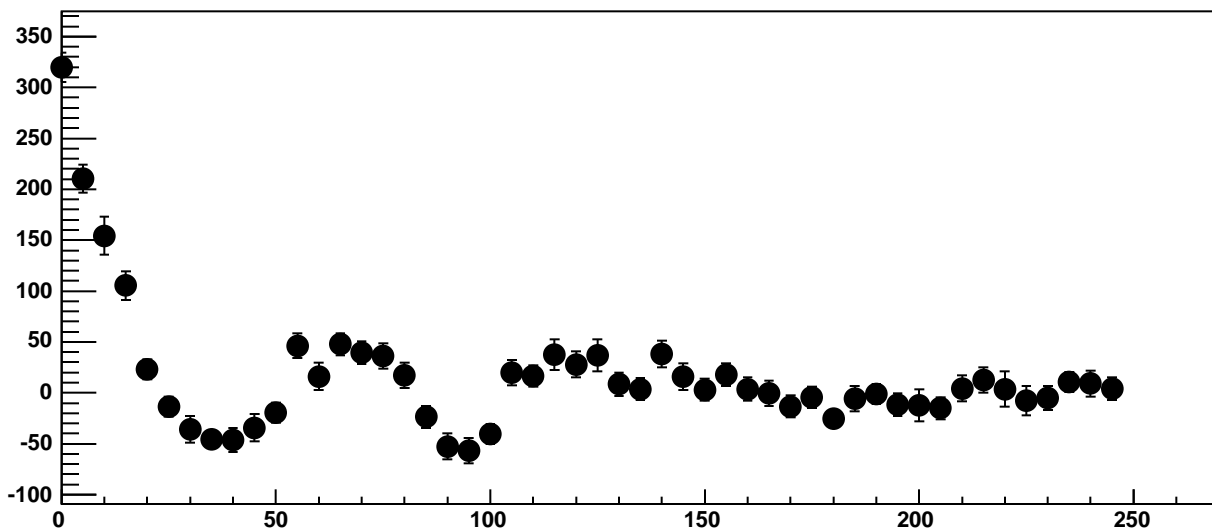


$\chi^2 / \text{ndf}$	293.2 / 41
p0	$-519.6 \pm 3.889$
p1	$90.65 \pm 0.4392$
p2	$-4.531\text{e}+08 \pm 4.665\text{e}+06$
p3	$2.743\text{e}+07 \pm 1.79\text{e}+05$
p4	$14.14 \pm 0.1252$

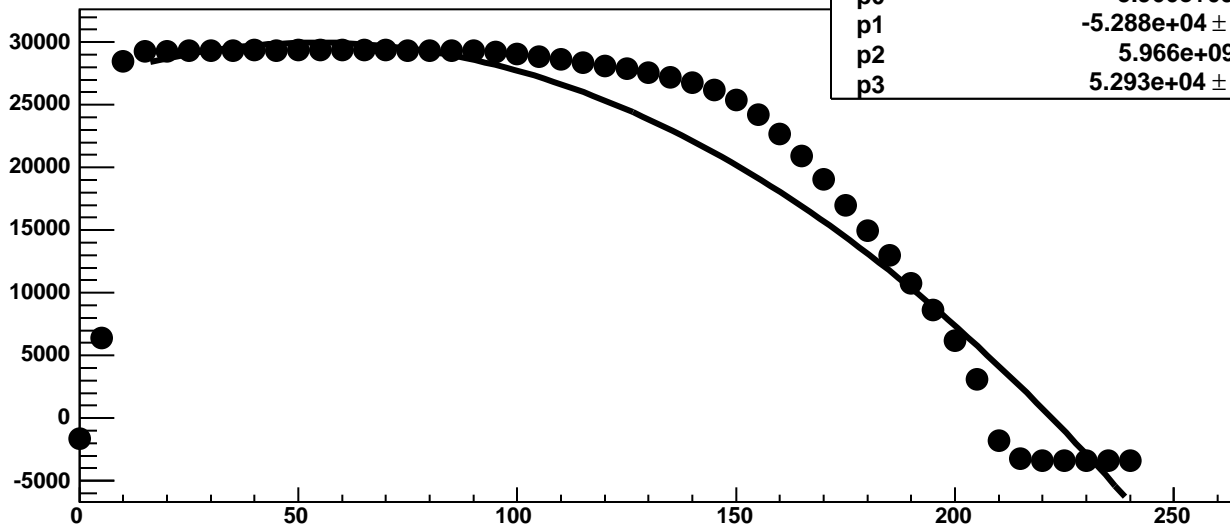
Chip 1, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



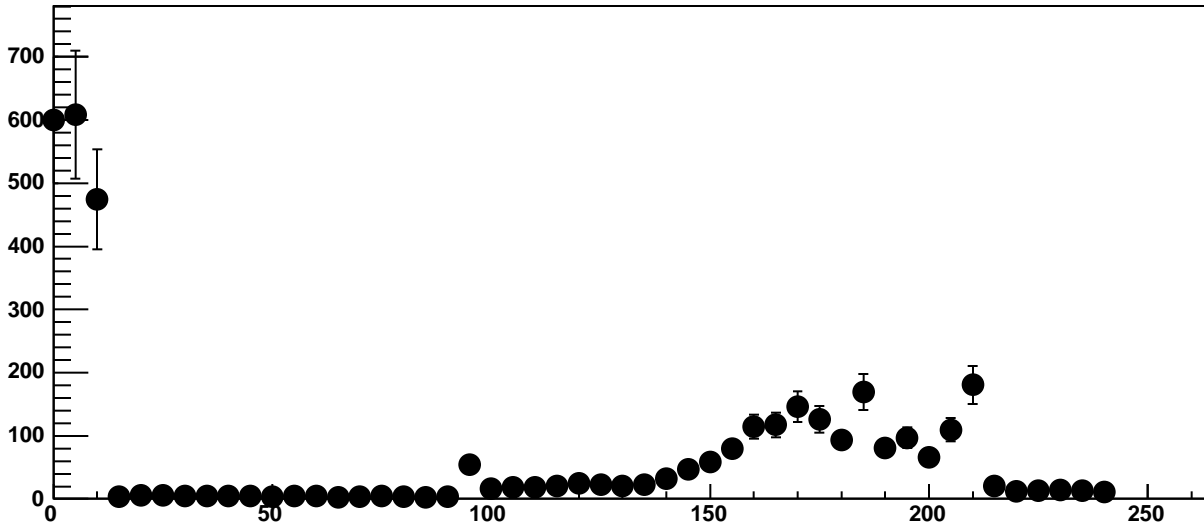
Chip 1, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold



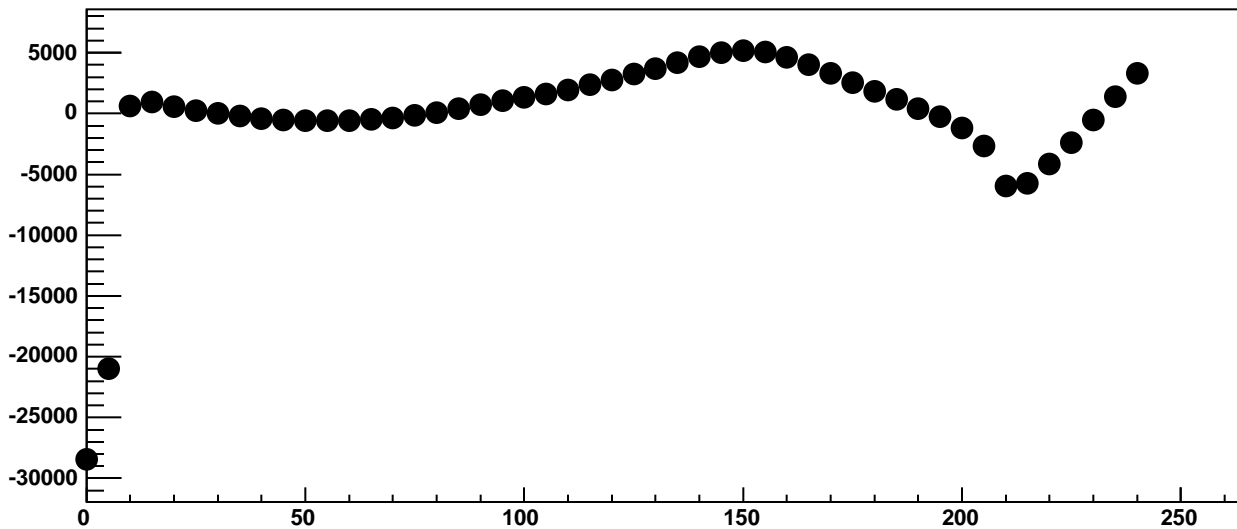
Chip 1, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold



Chip 1, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

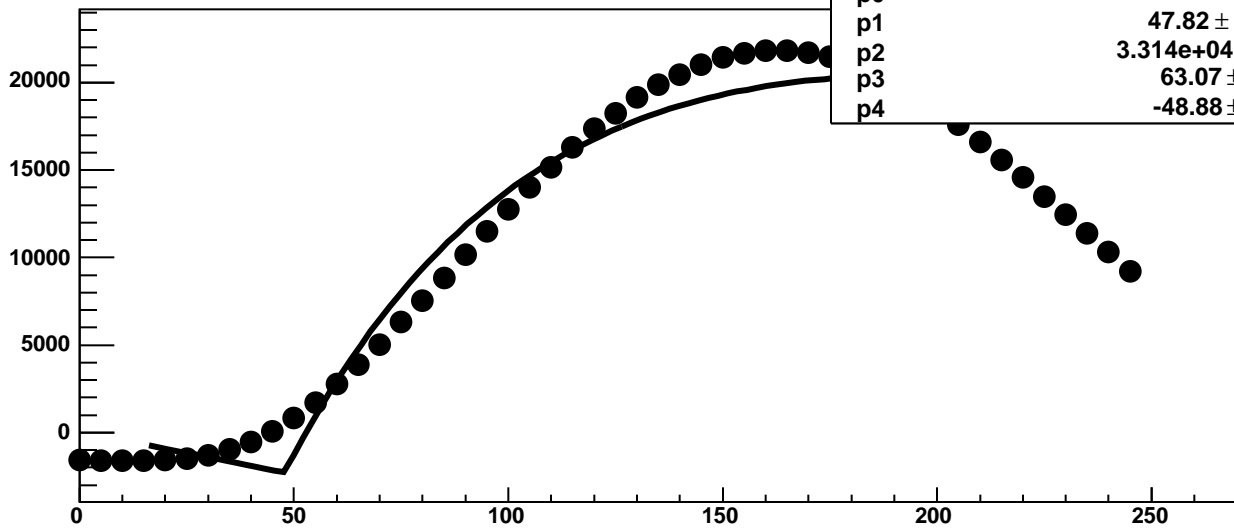


Chip 1, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold



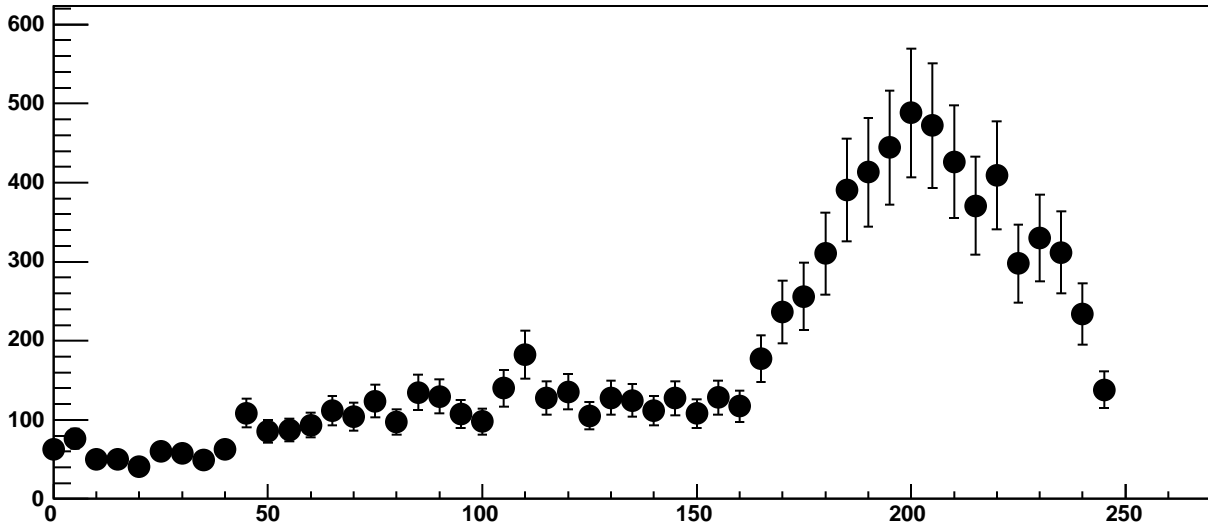


Chip 1, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold

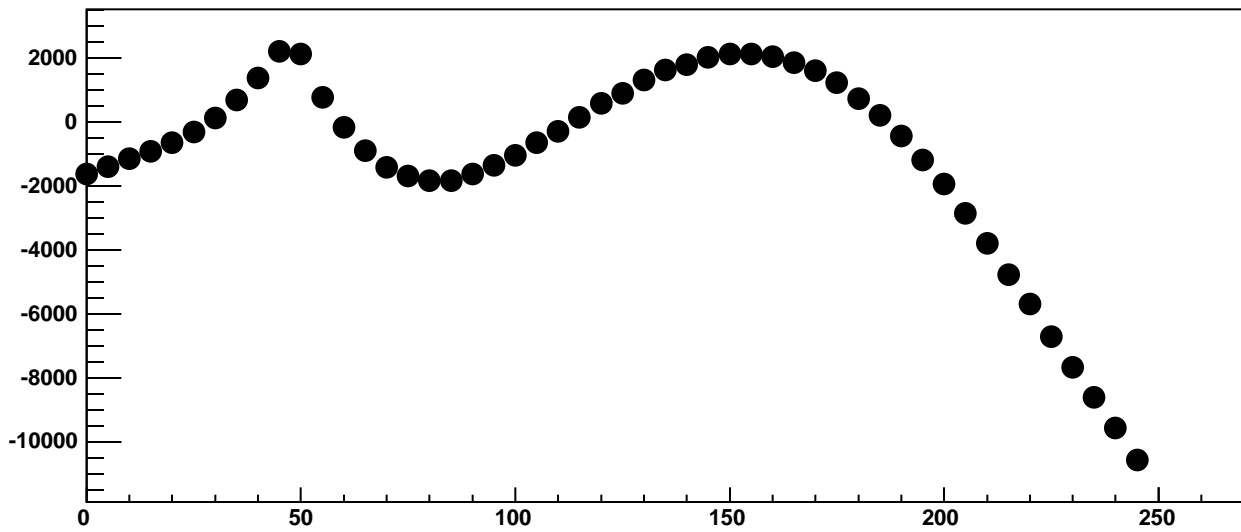


$\chi^2 / \text{ndf}$	1.867e+05 / 41
p0	-2274 ± 8.76
p1	47.82 ± 0.03141
p2	3.314e+04 ± 84.97
p3	63.07 ± 0.1512
p4	-48.88 ± 0.3919

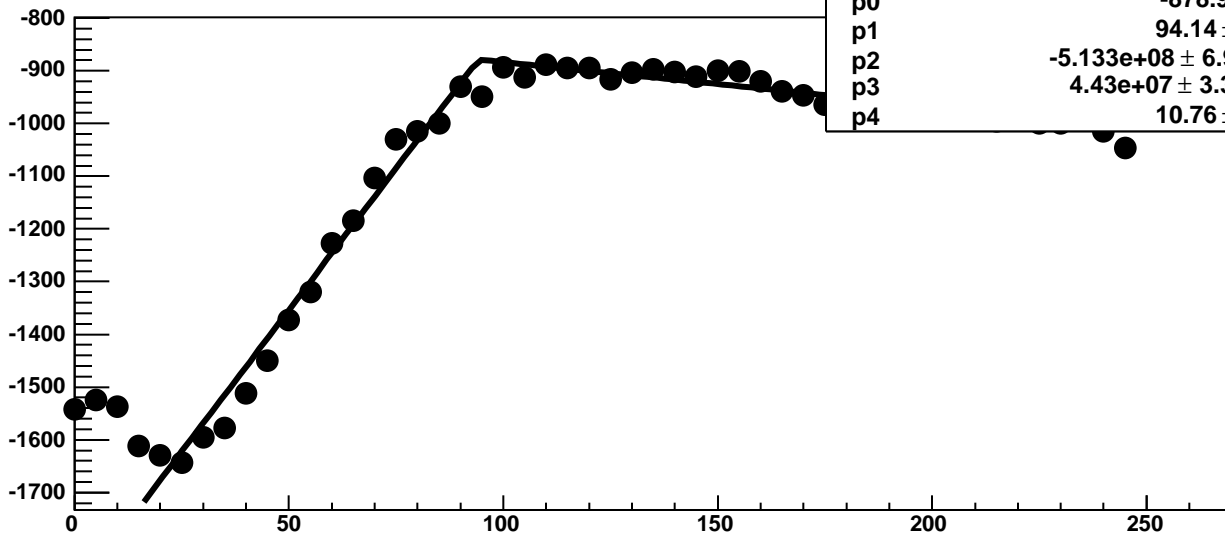
Chip 1, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold

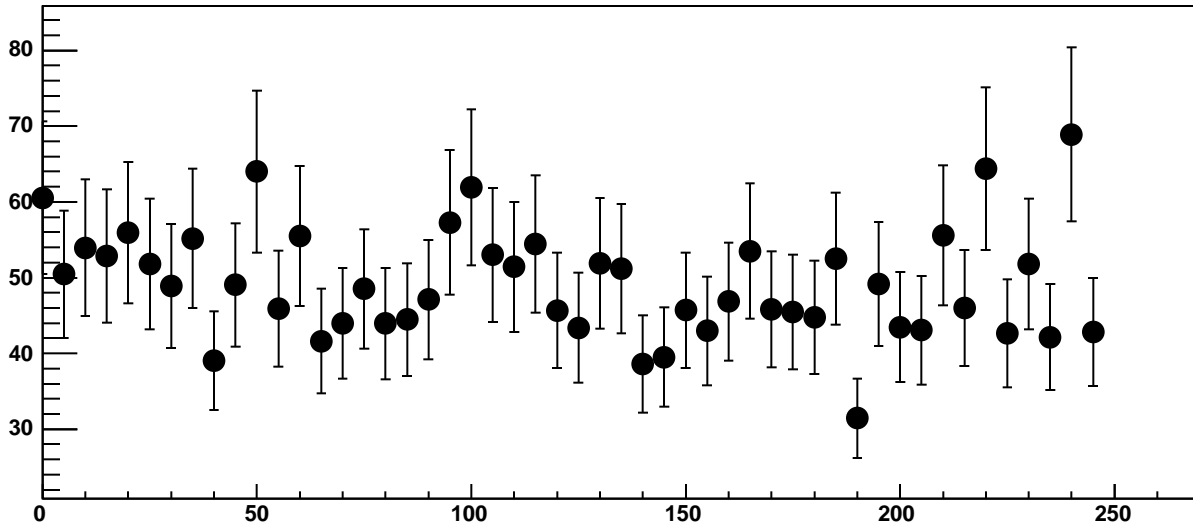


Chip 1, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

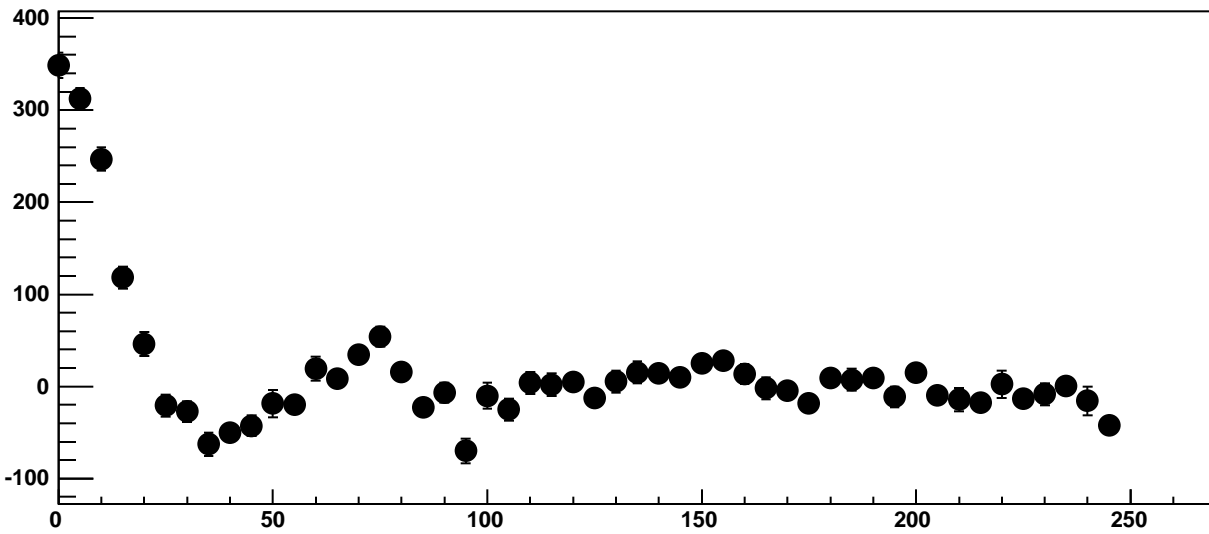


$\chi^2 / \text{ndf}$	313.9 / 41
p0	$-878.9 \pm 3.882$
p1	$94.14 \pm 0.5962$
p2	$-5.133\text{e}+08 \pm 6.914\text{e}+06$
p3	$4.43\text{e}+07 \pm 3.395\text{e}+05$
p4	$10.76 \pm 0.1213$

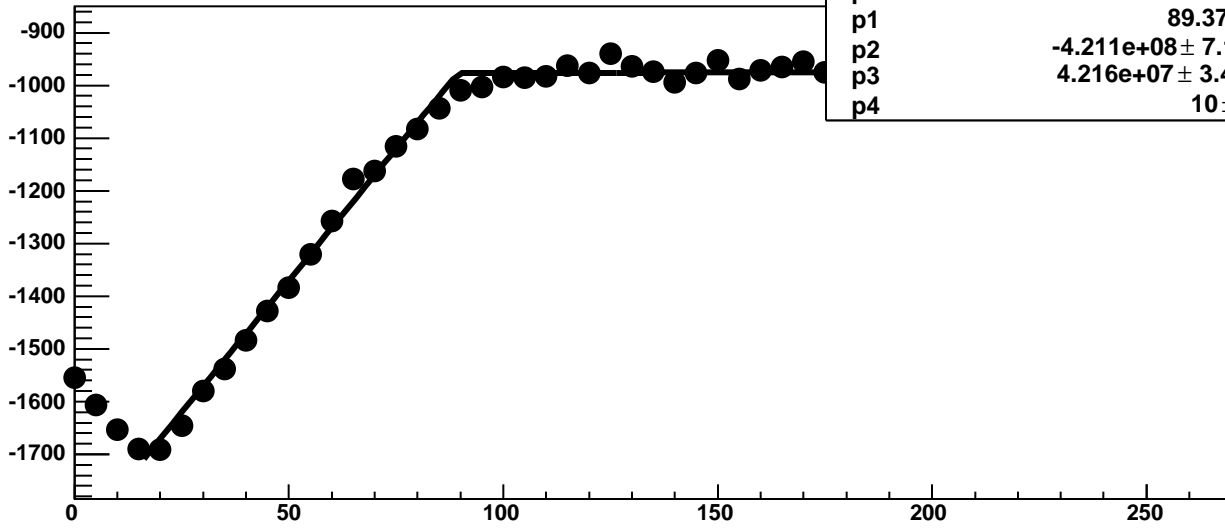
Chip 1, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

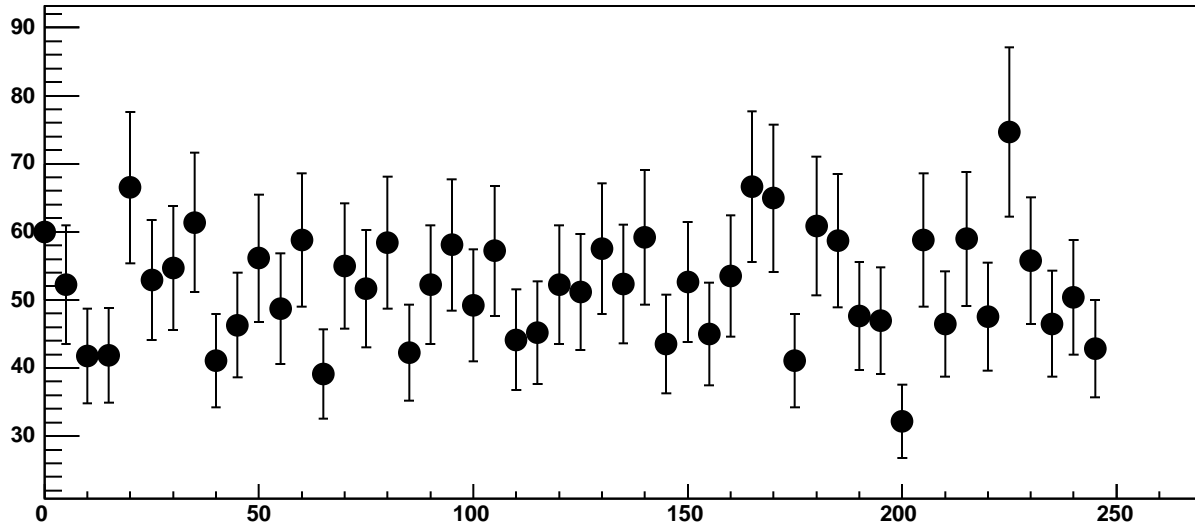


Chip 1, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

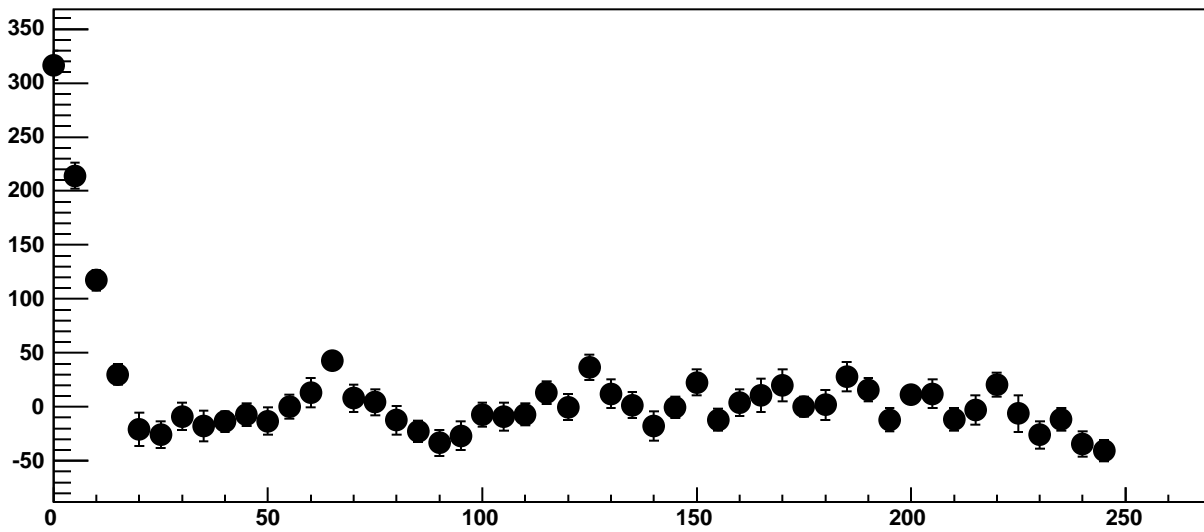


$\chi^2 / \text{ndf}$	117 / 41
p0	$-976.6 \pm 4.196$
p1	$89.37 \pm 0.729$
p2	$-4.211\text{e}+08 \pm 7.127\text{e}+06$
p3	$4.216\text{e}+07 \pm 3.479\text{e}+05$
p4	$10 \pm 0.1352$

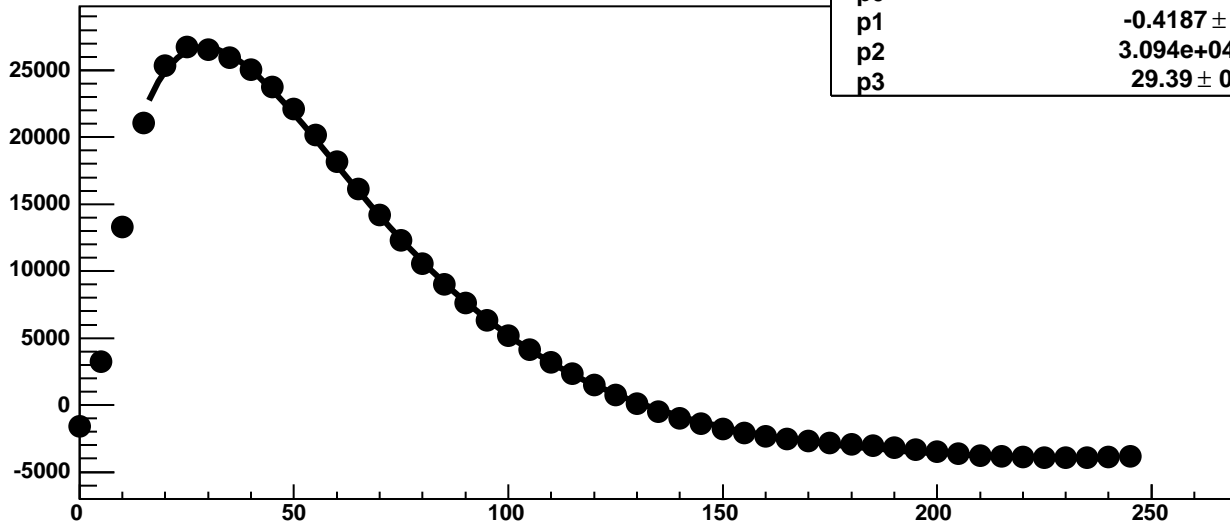
Chip 1, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

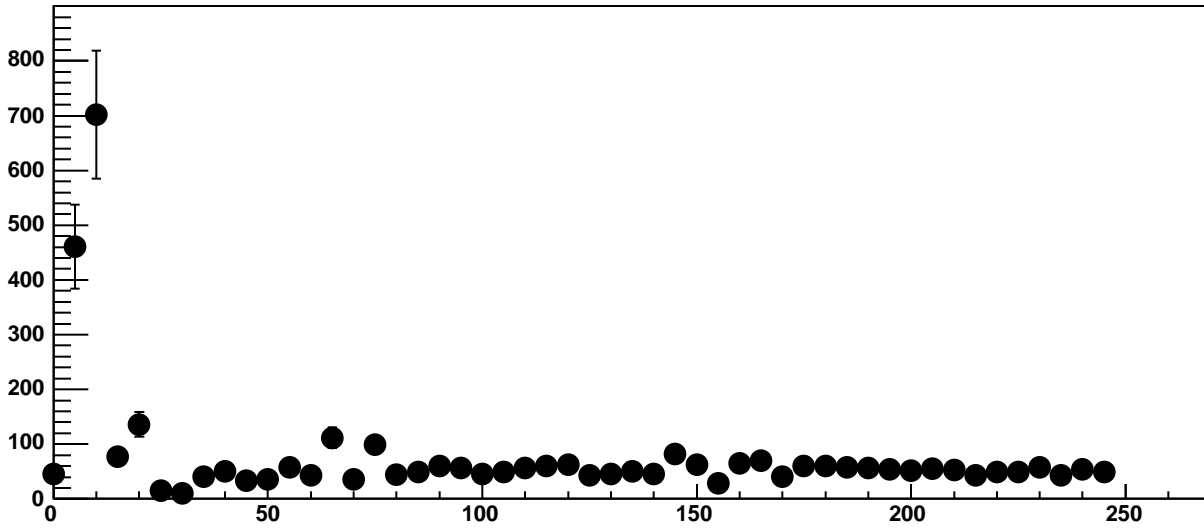


Chip 1, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold

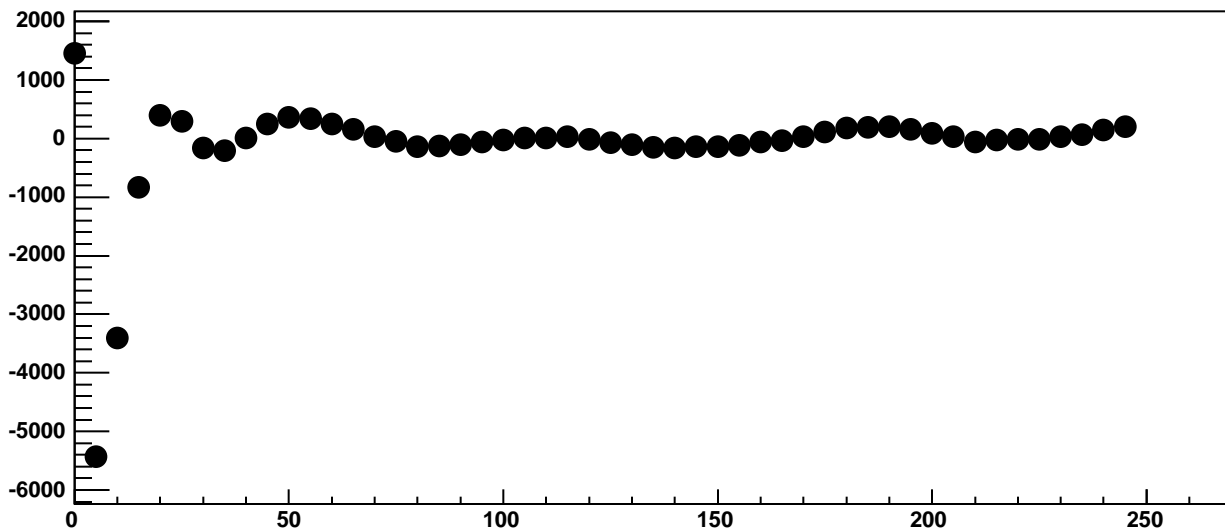


$\chi^2 / \text{ndf}$	2.234e+04 / 42
p0	-4213 ± 3.284
p1	-0.4187 ± 0.01782
p2	3.094e+04 ± 3.561
p3	29.39 ± 0.009805

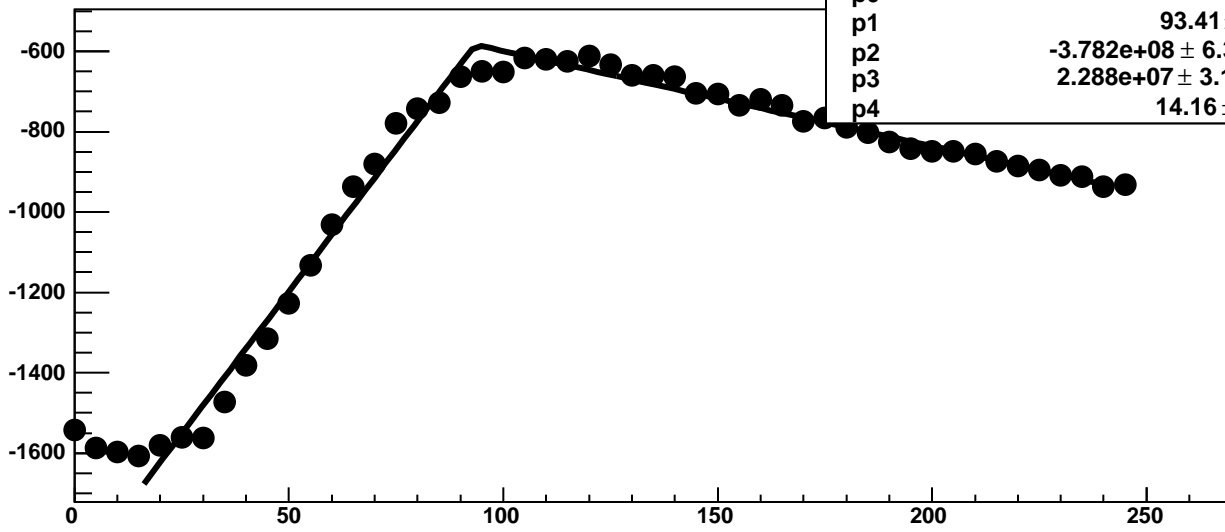
Chip 1, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



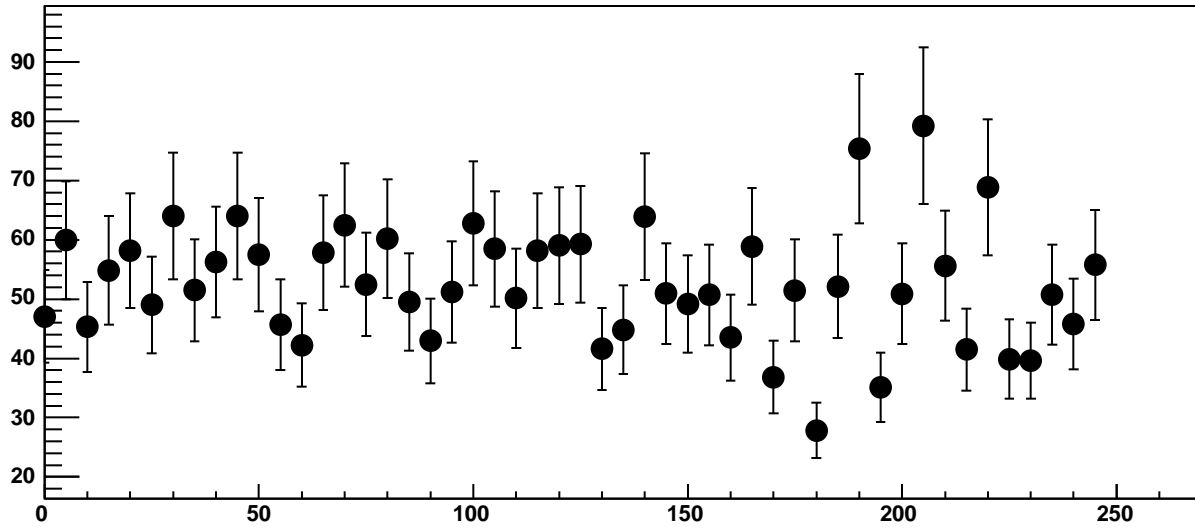
Chip 1, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold



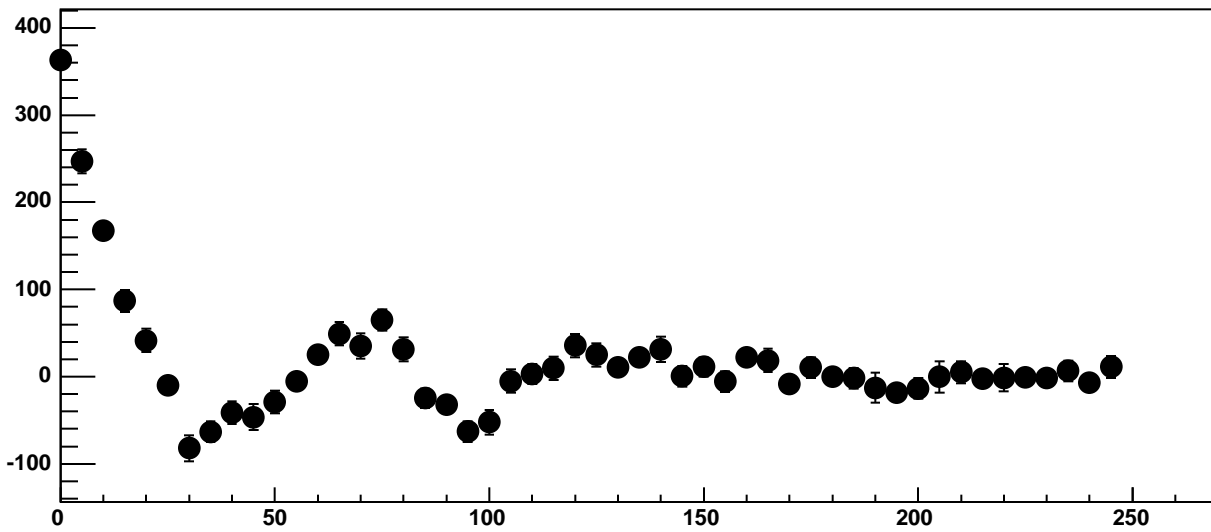
Chip 1, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold



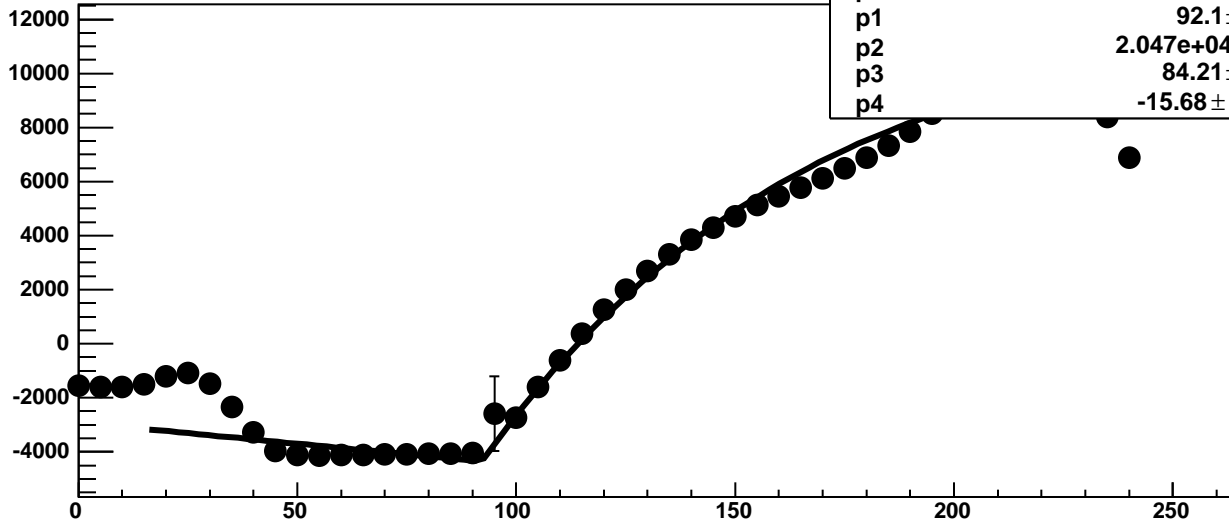
Chip 1, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

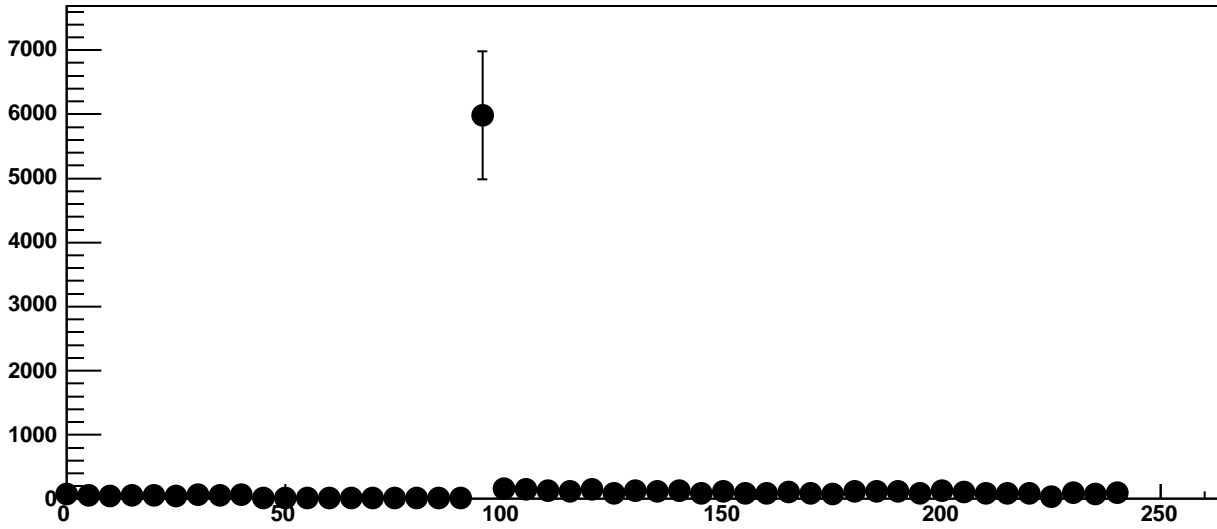


Chip 1, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

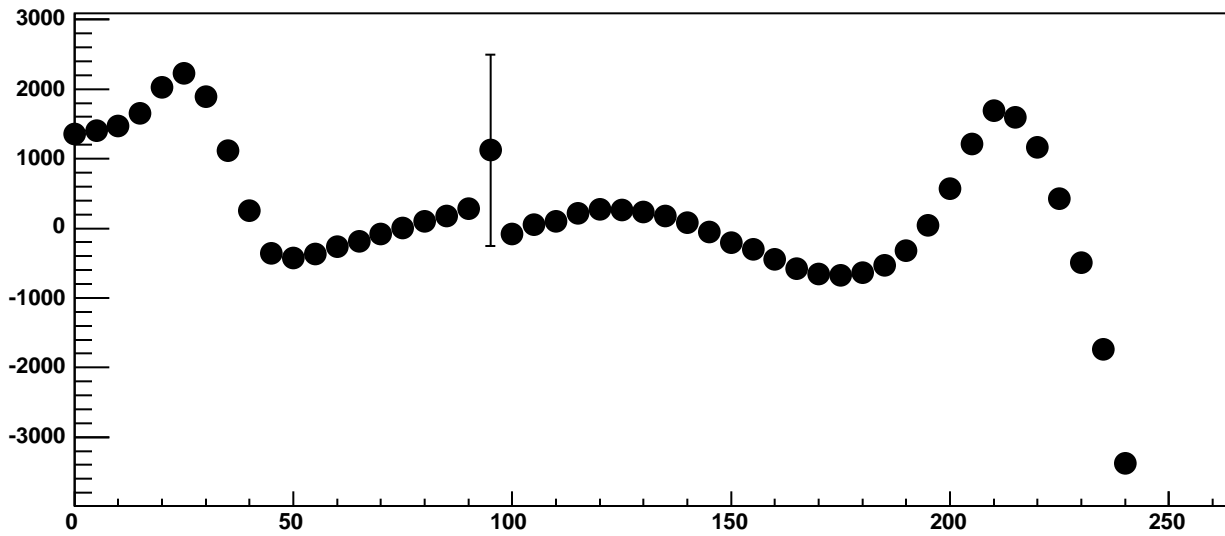


$\chi^2 / \text{ndf}$	2.204e+05 / 41
p0	-4359 ± 2.368
p1	92.1 ± 0.1009
p2	2.047e+04 ± 41.03
p3	84.21 ± 0.3883
p4	-15.68 ± 0.06549

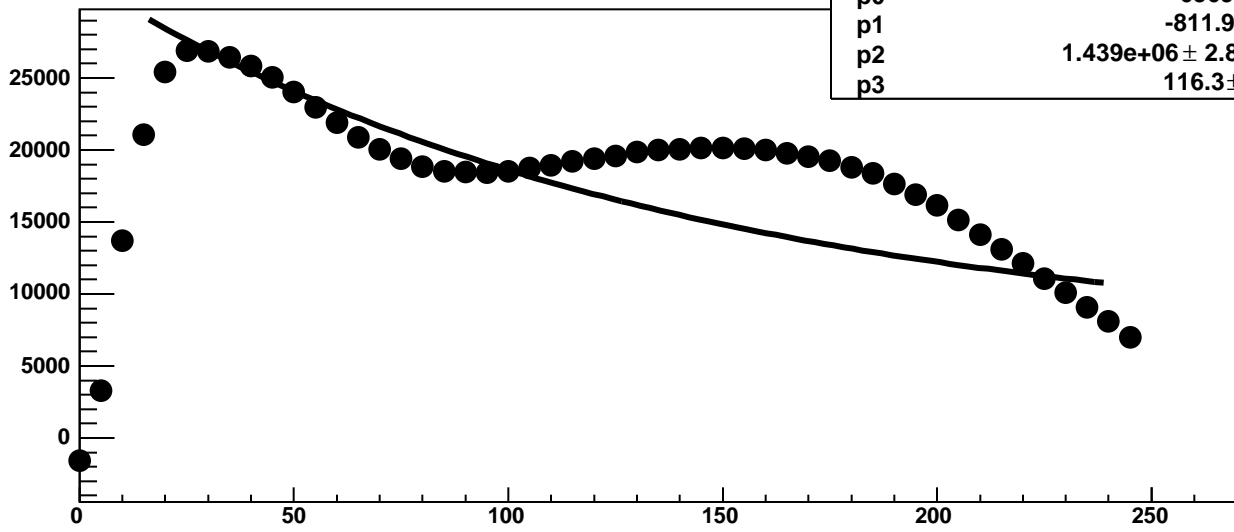
Chip 1, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

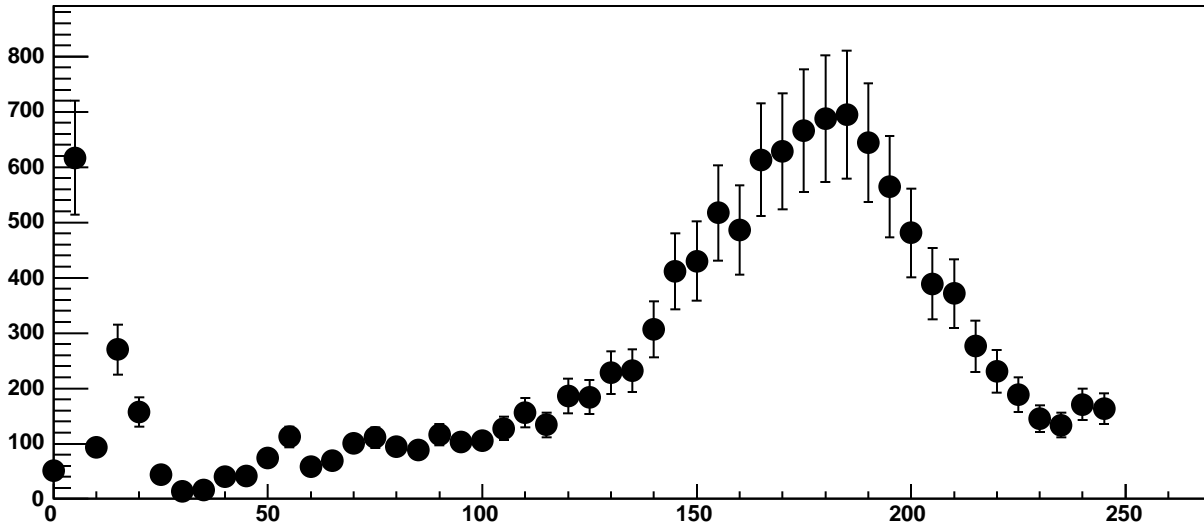


Chip 1, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

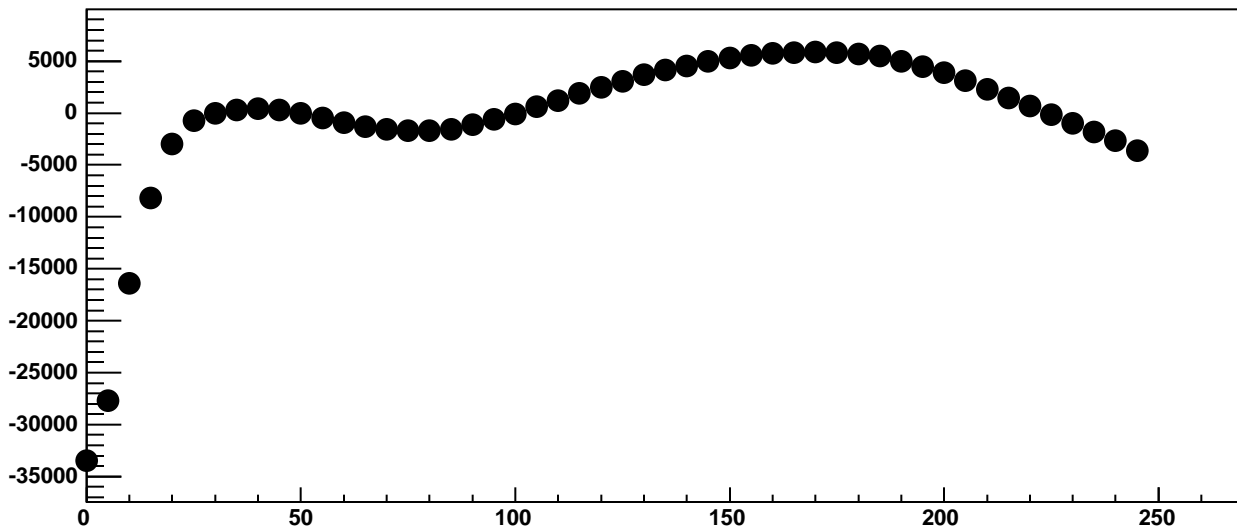


$\chi^2 / \text{ndf}$	1.369e+05 / 42
p0	6569 ± 47.23
p1	-811.9 ± 4.909
p2	1.439e+06 ± 2.889e+04
p3	116.3 ± 0.4357

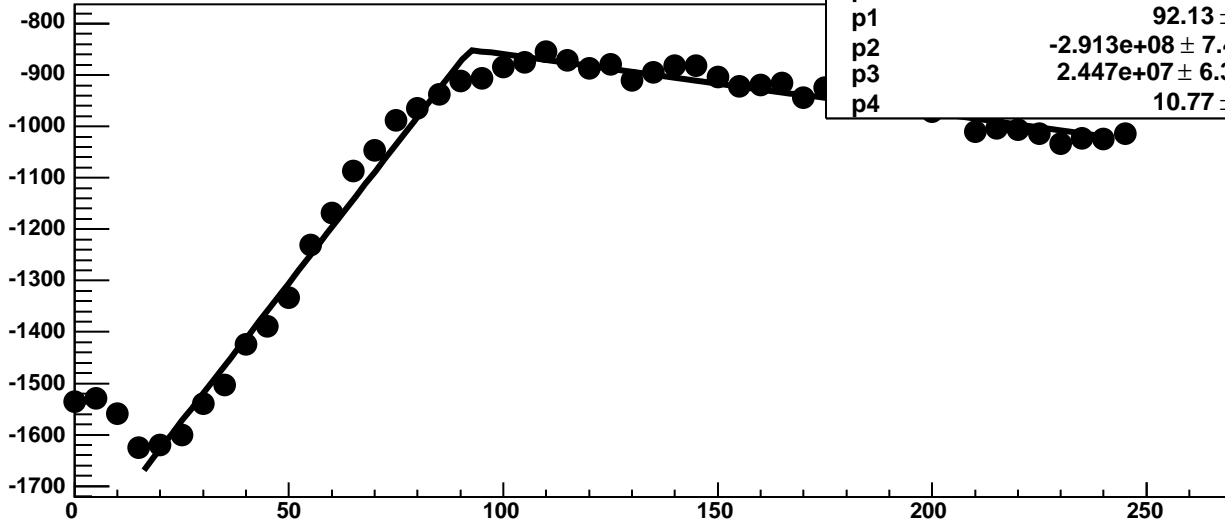
Chip 1, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

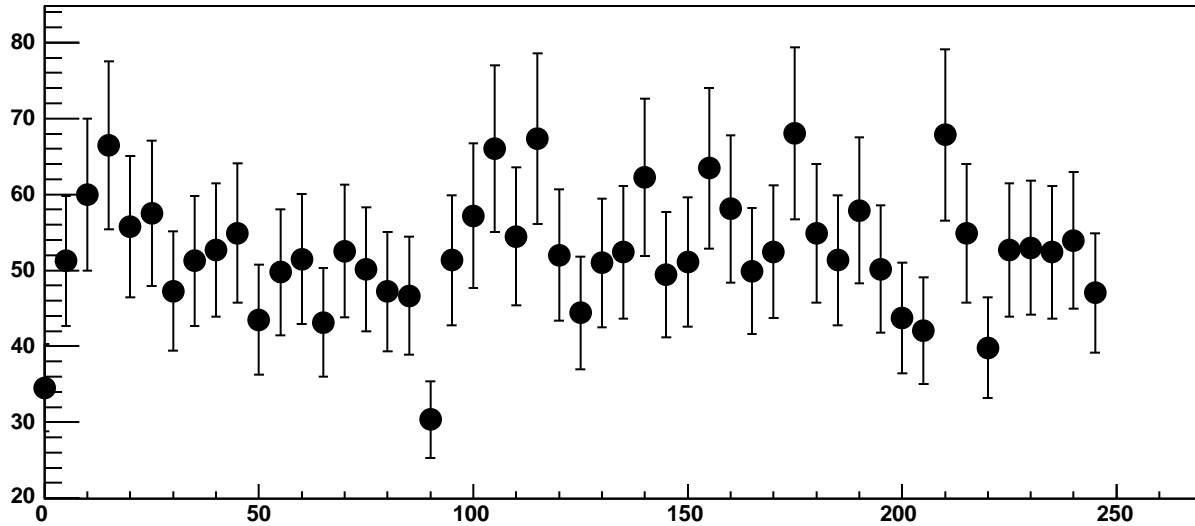


Chip 1, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

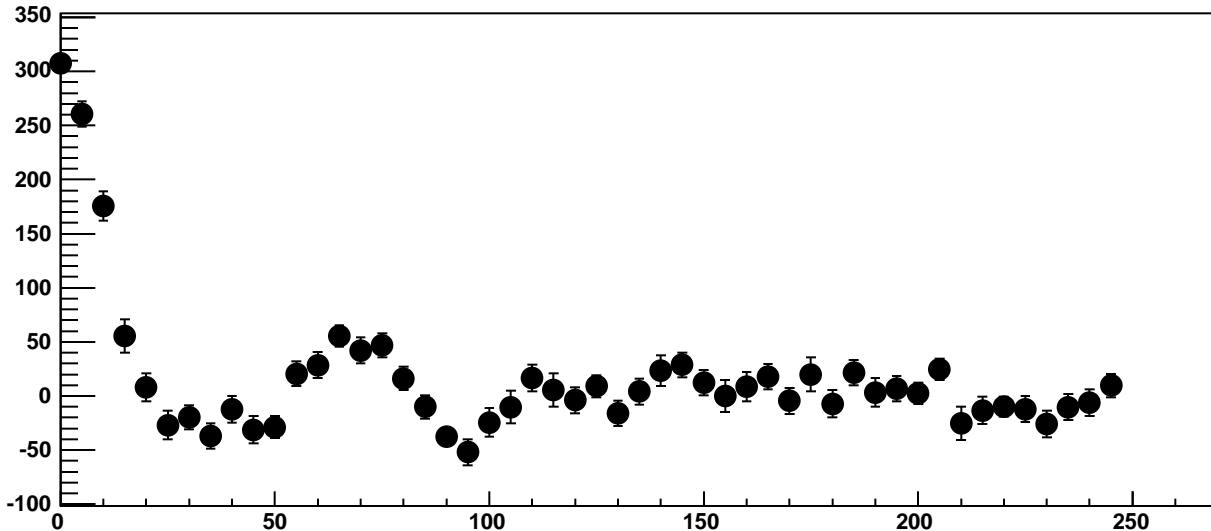


$\chi^2 / \text{ndf}$	213.5 / 41
p0	$-850.7 \pm 4.082$
p1	$92.13 \pm 0.5404$
p2	$-2.913\text{e}+08 \pm 7.427\text{e}+06$
p3	$2.447\text{e}+07 \pm 6.341\text{e}+05$
p4	$10.77 \pm 0.1096$

Chip 1, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold

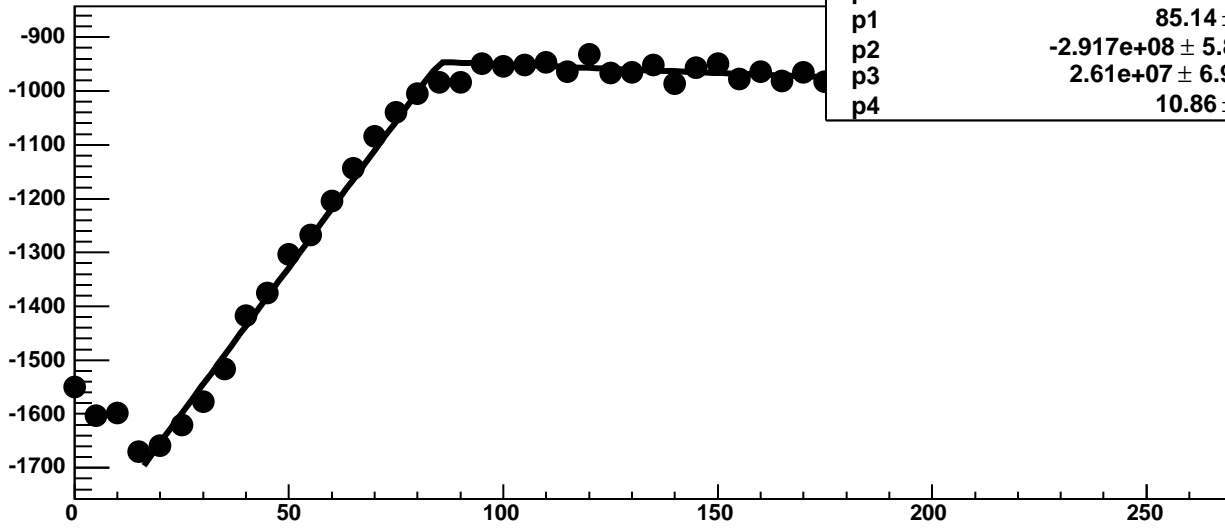


Chip 1, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold



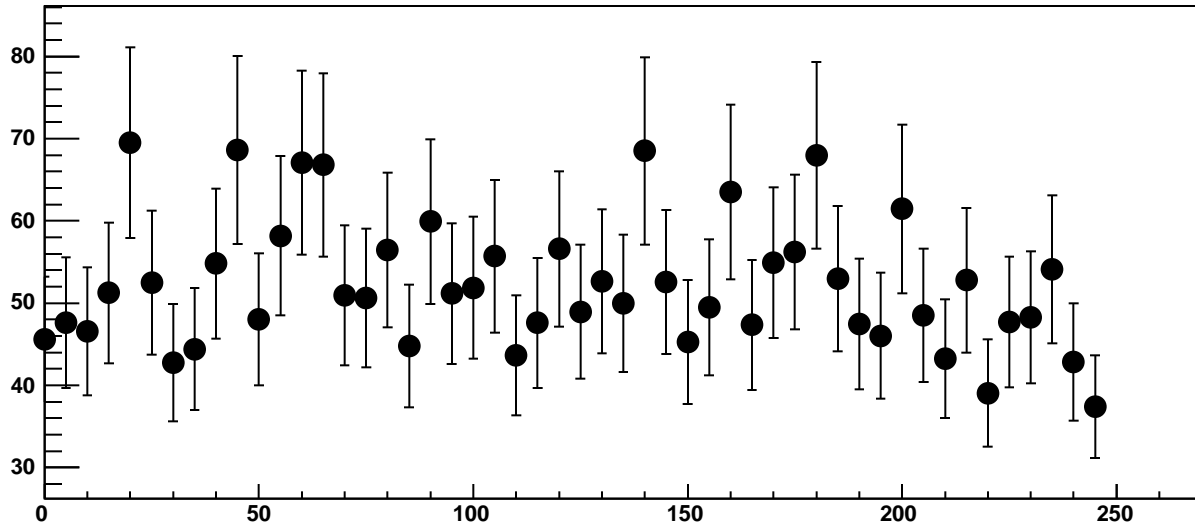


Chip 1, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

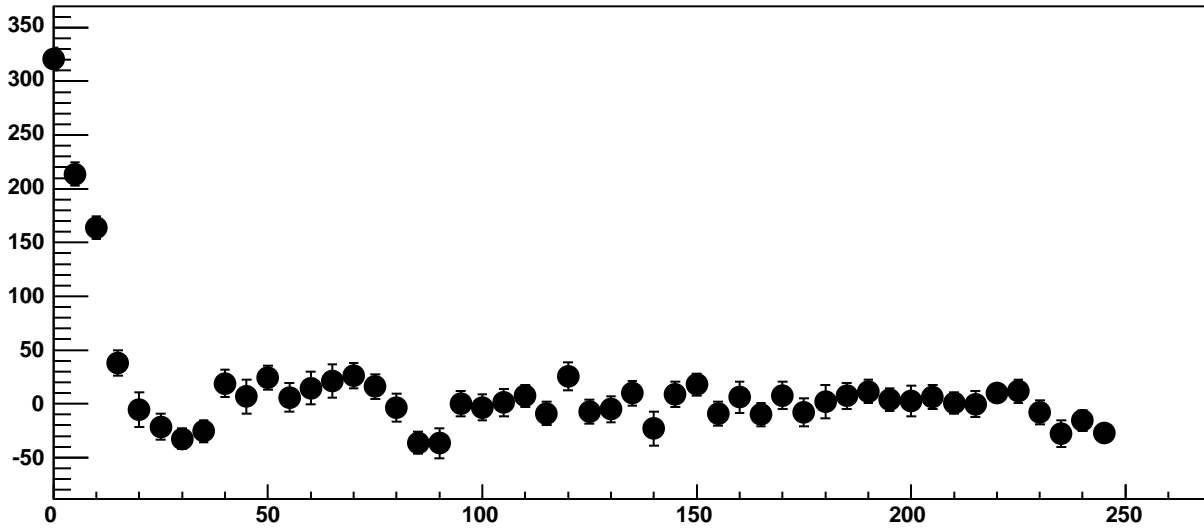


$\chi^2 / \text{ndf}$	95.08 / 41
p0	$-945.9 \pm 4.171$
p1	$85.14 \pm 0.5482$
p2	$-2.917\text{e}+08 \pm 5.816\text{e}+06$
p3	$2.61\text{e}+07 \pm 6.996\text{e}+05$
p4	$10.86 \pm 0.1173$

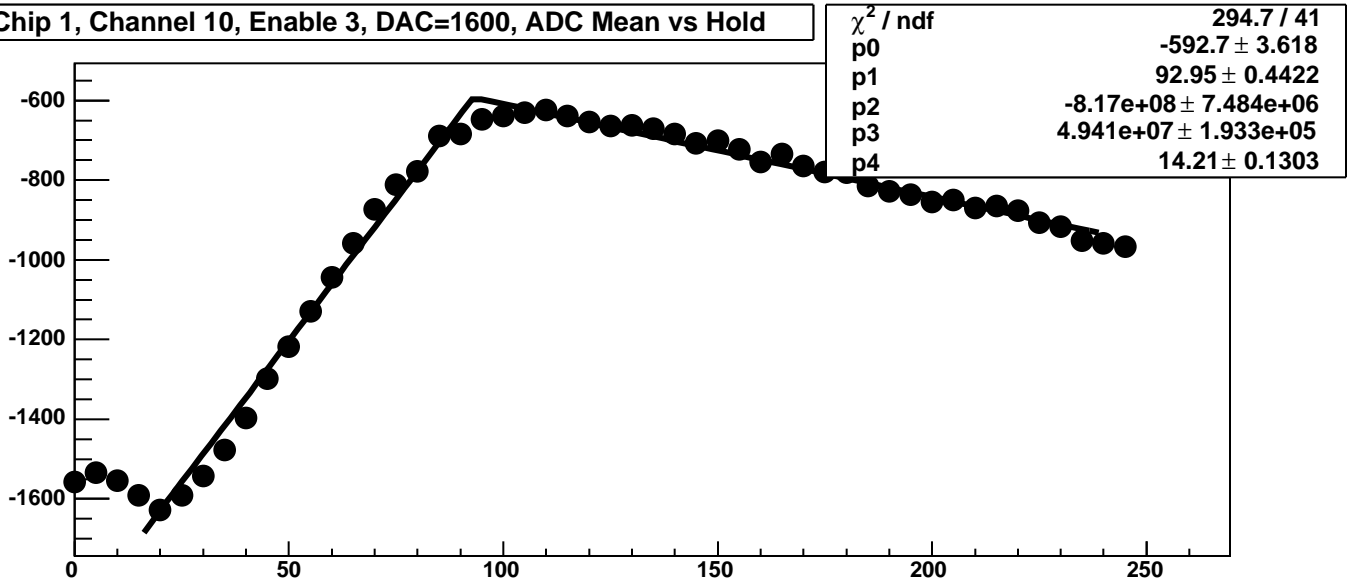
Chip 1, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



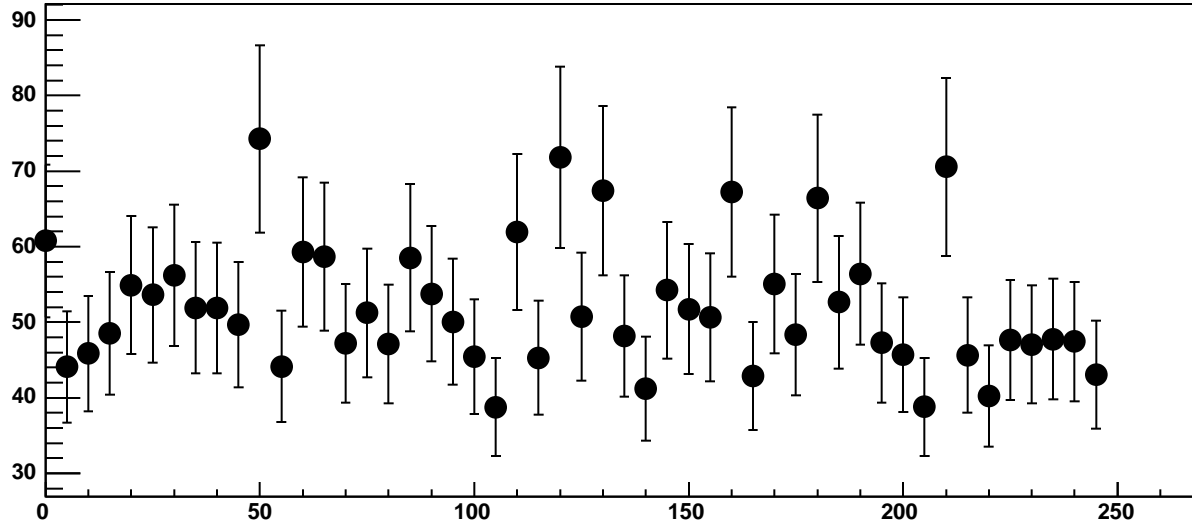
Chip 1, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold



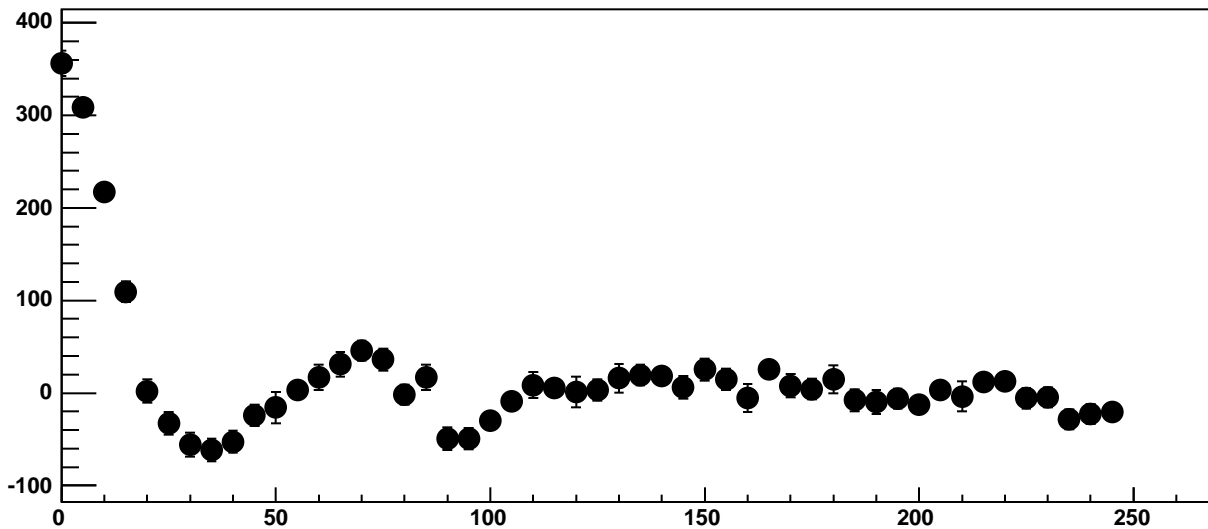
Chip 1, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold



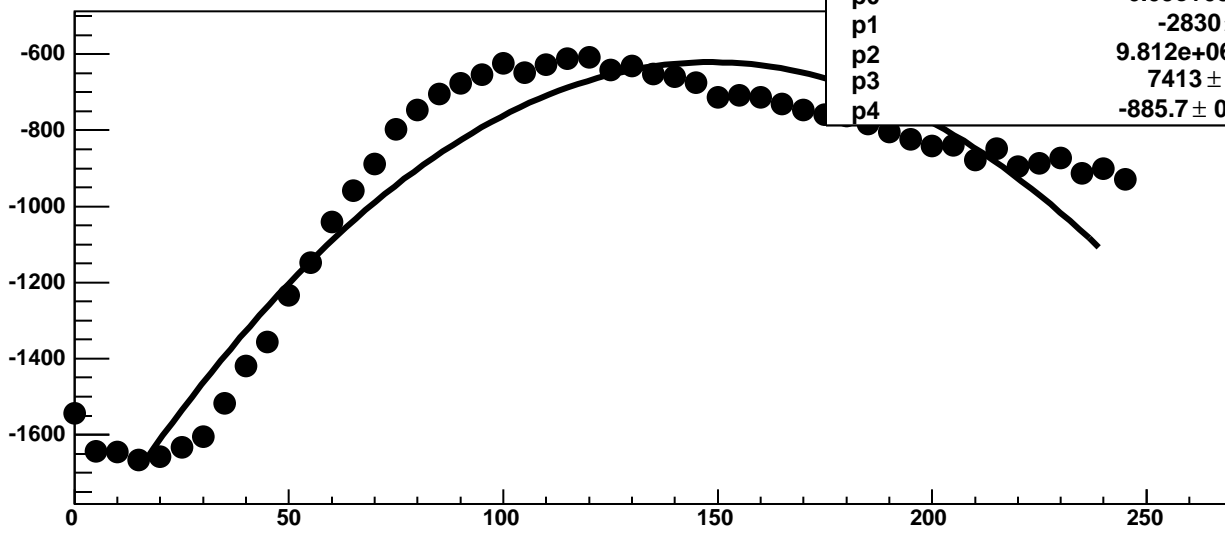
Chip 1, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold

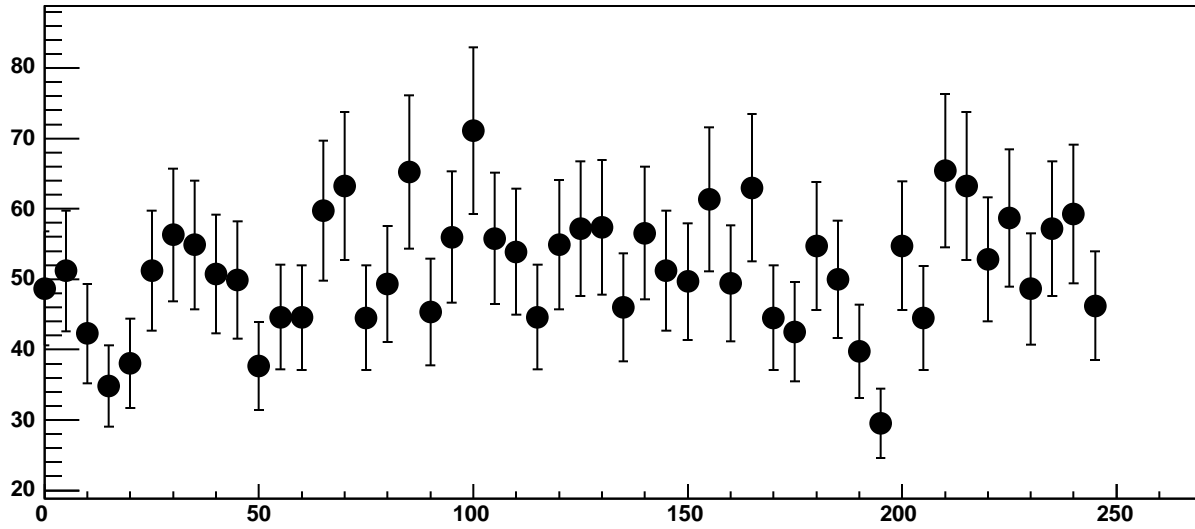


Chip 1, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

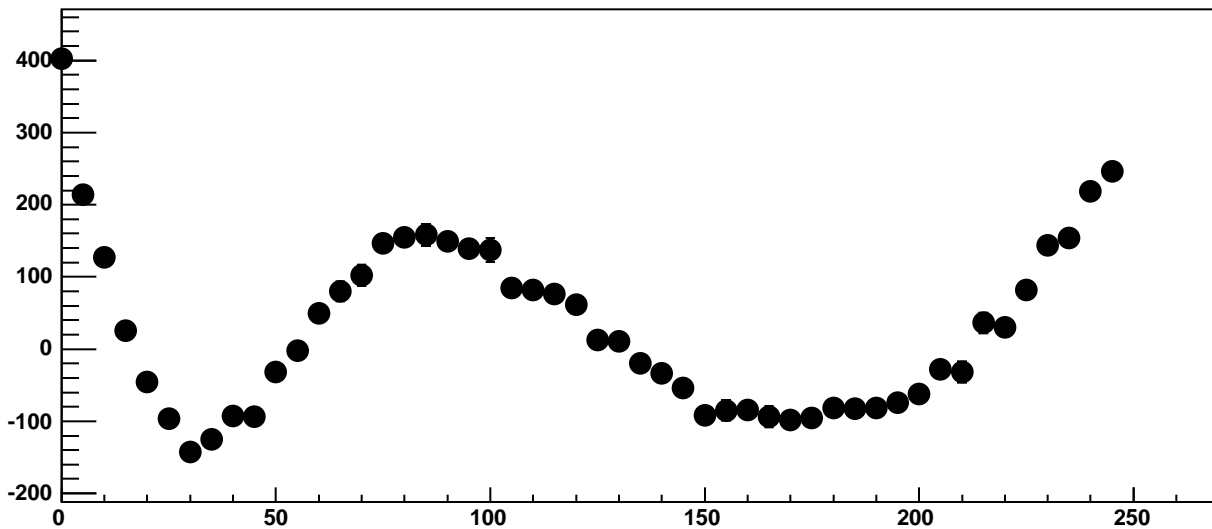


$\chi^2 / \text{ndf}$	3013 / 41
p0	$-6.09\text{e}+05 \pm 22.49$
p1	$-2830 \pm 0.2091$
p2	$9.812\text{e}+06 \pm 68.31$
p3	$7413 \pm 0.06345$
p4	$-885.7 \pm 0.007594$

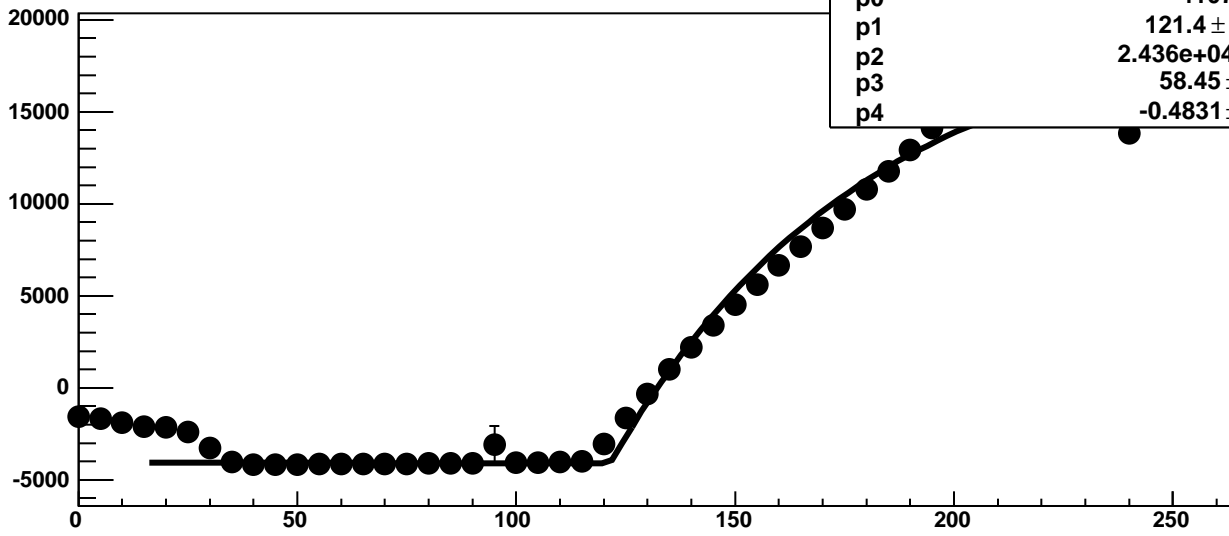
Chip 1, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

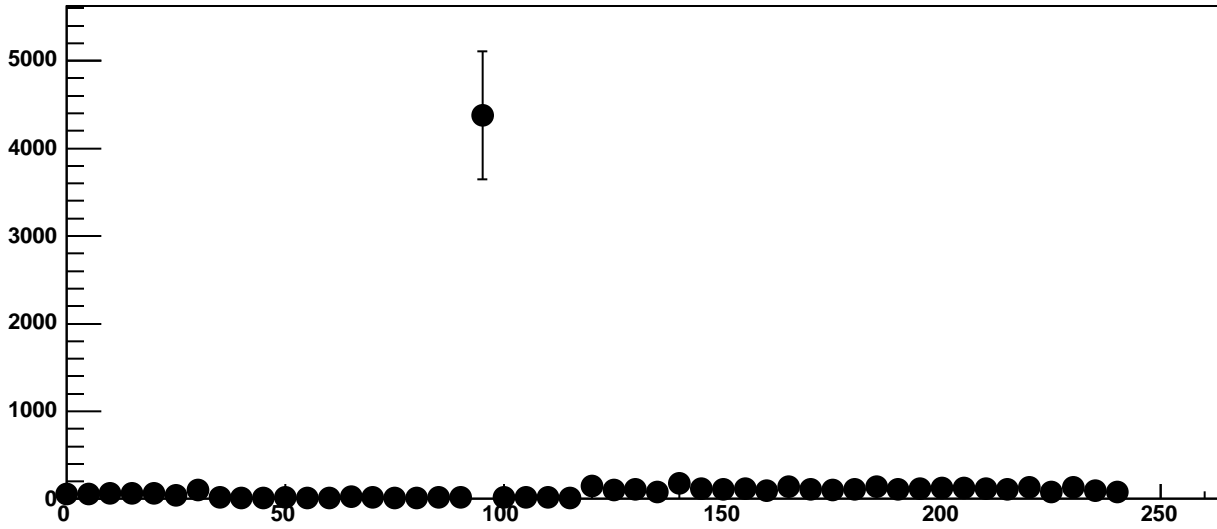


Chip 1, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

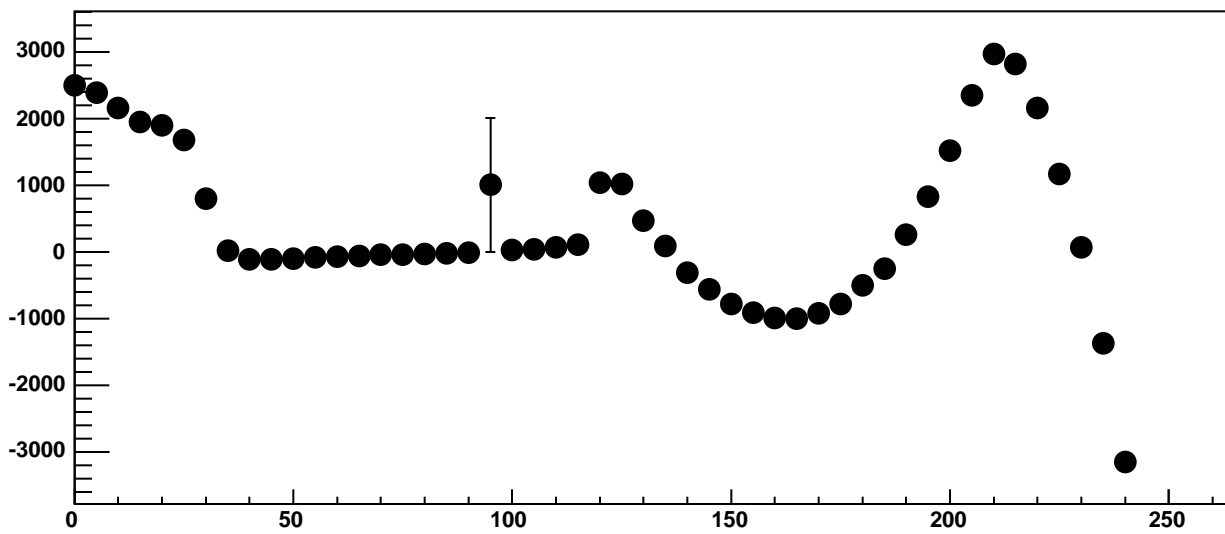


$\chi^2 / \text{ndf}$	1.586e+05 / 41
p0	-4107 ± 1.863
p1	121.4 ± 0.04385
p2	2.436e+04 ± 30.81
p3	58.45 ± 0.1802
p4	-0.4831 ± 0.0342

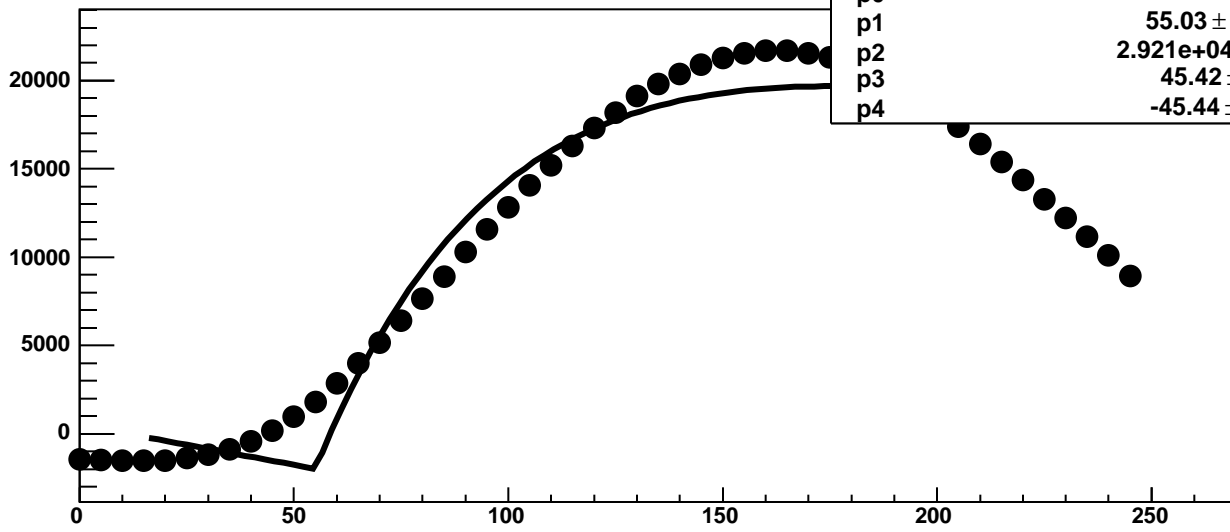
Chip 1, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



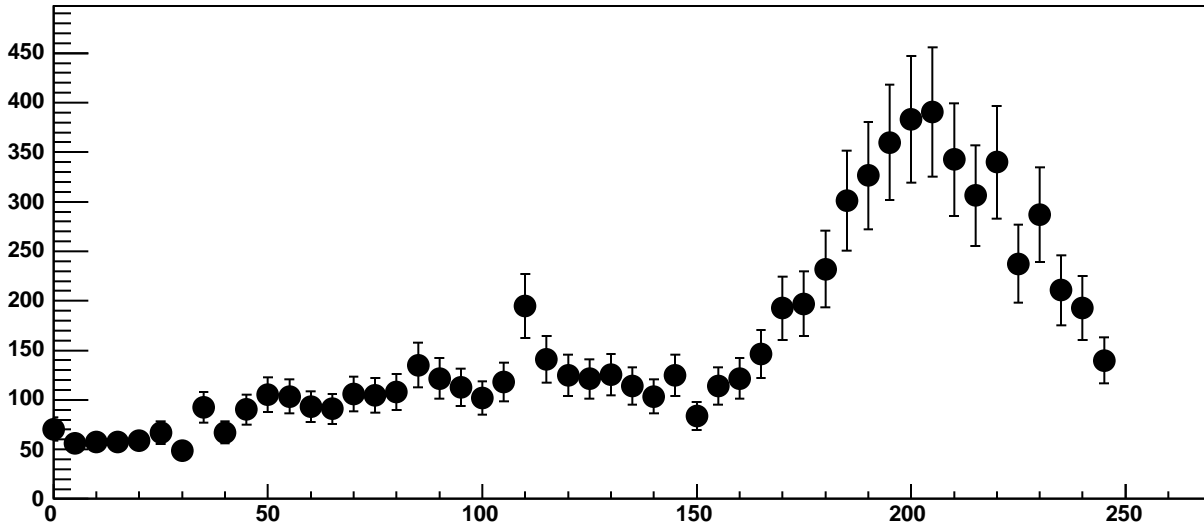
Chip 1, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



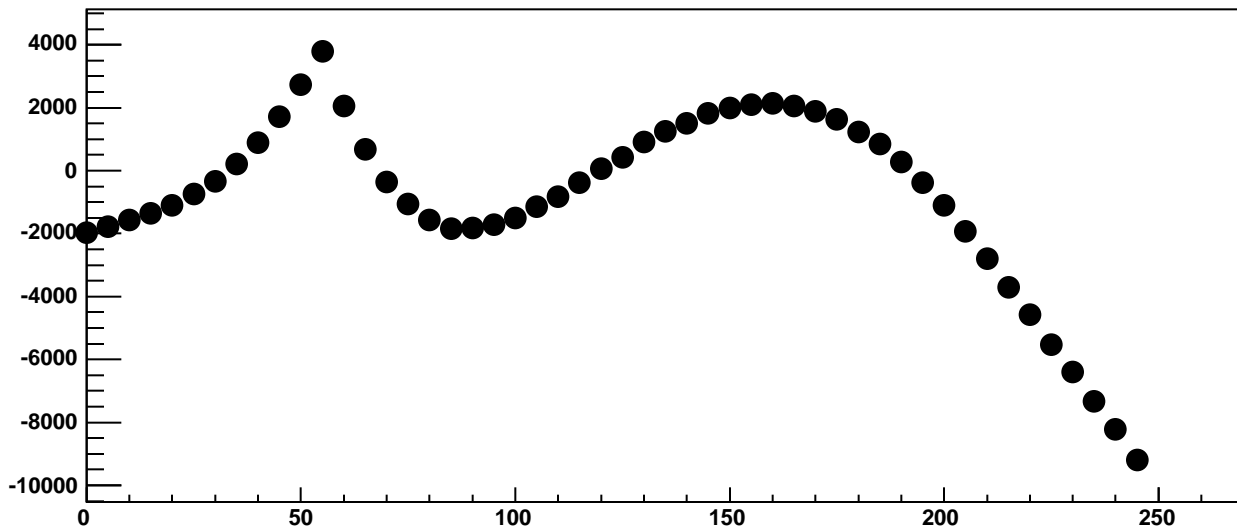
Chip 1, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold



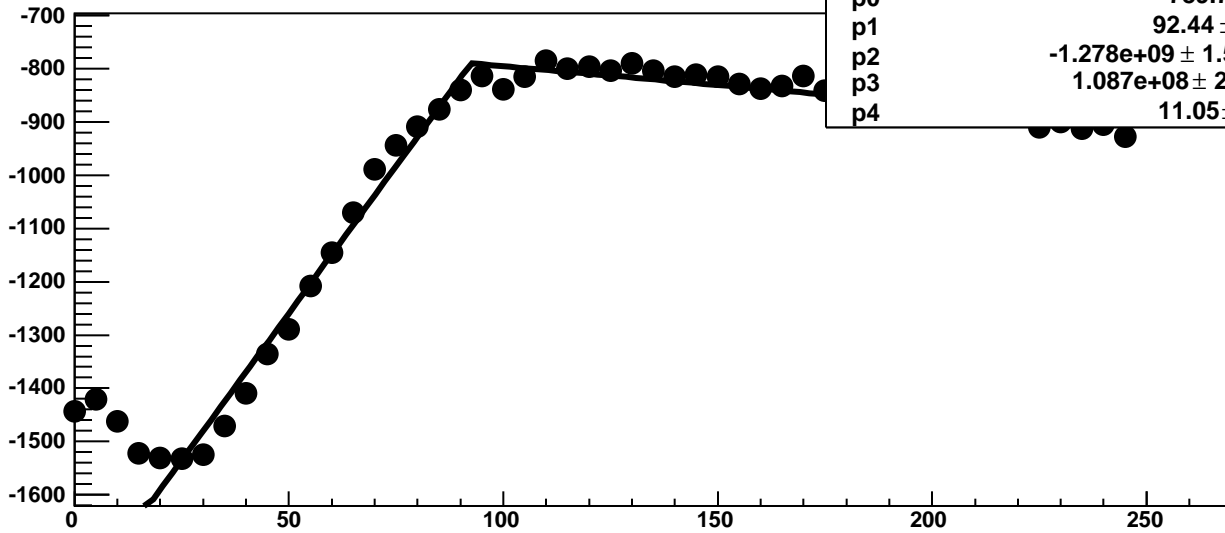
Chip 1, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold

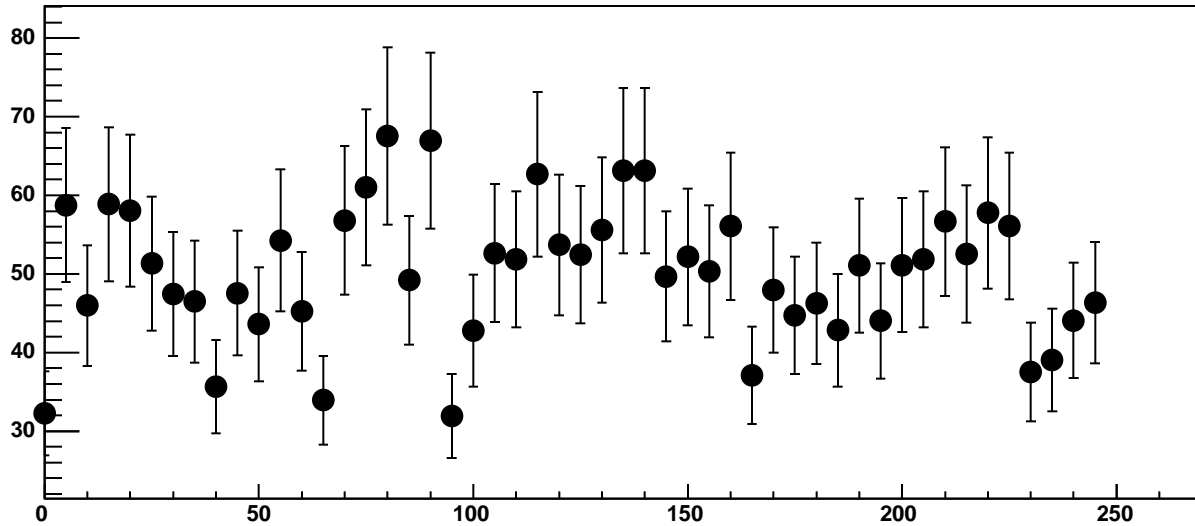


Chip 1, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

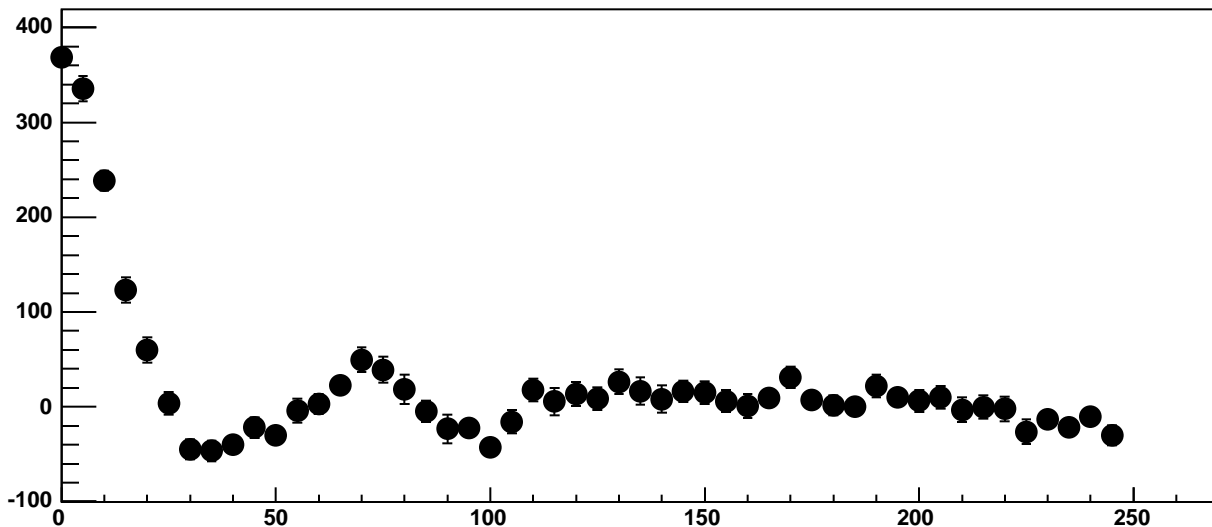


$\chi^2 / \text{ndf}$	284.6 / 41
p0	-789.7 ± 3.668
p1	92.44 ± 0.6284
p2	-1.278e+09 ± 1.566e+07
p3	1.087e+08 ± 2.06e+05
p4	11.05 ± 0.1363

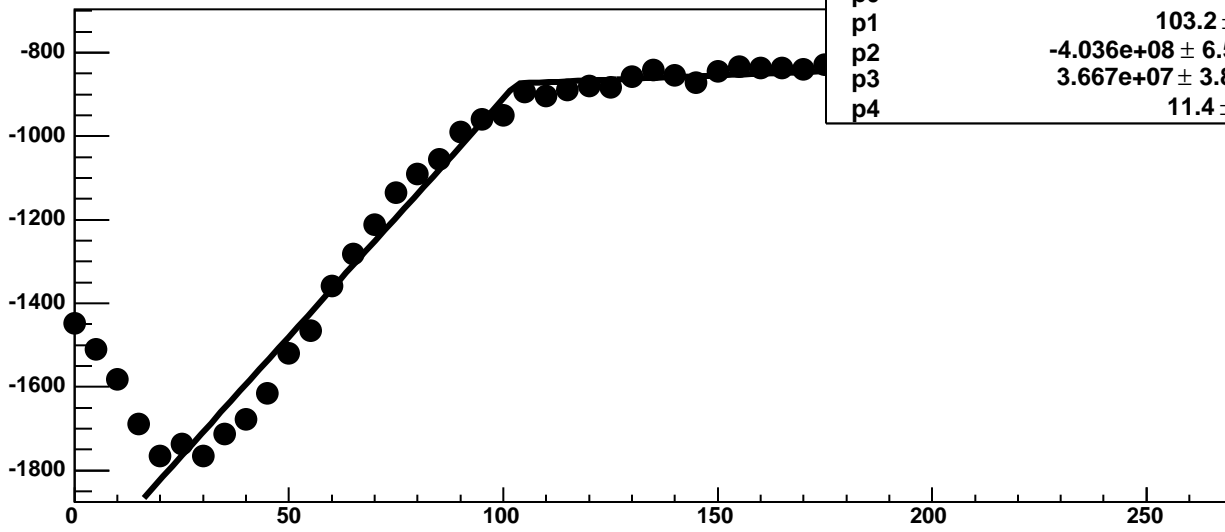
Chip 1, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

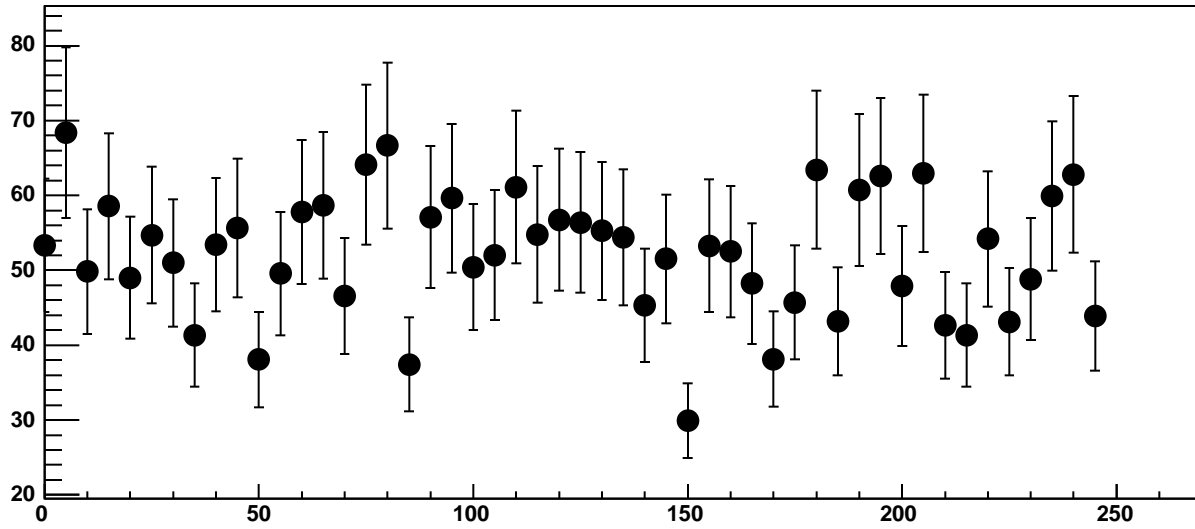


Chip 1, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

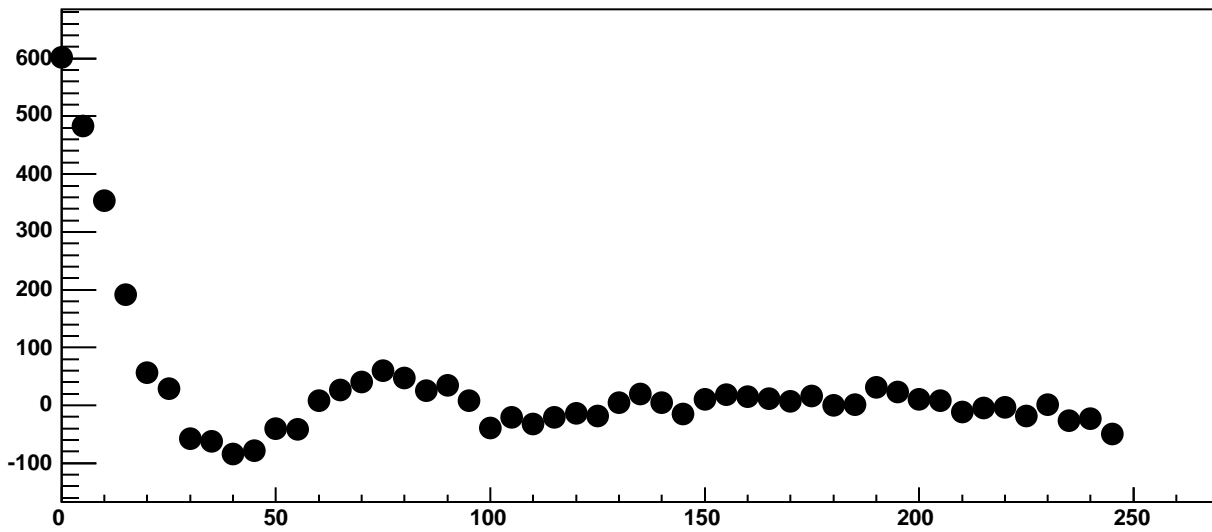


$\chi^2 / \text{ndf}$	540.3 / 41
p0	$-873.1 \pm 4.653$
p1	$103.2 \pm 0.6617$
p2	$-4.036\text{e}+08 \pm 6.543\text{e}+06$
p3	$3.667\text{e}+07 \pm 3.872\text{e}+05$
p4	$11.4 \pm 0.1086$

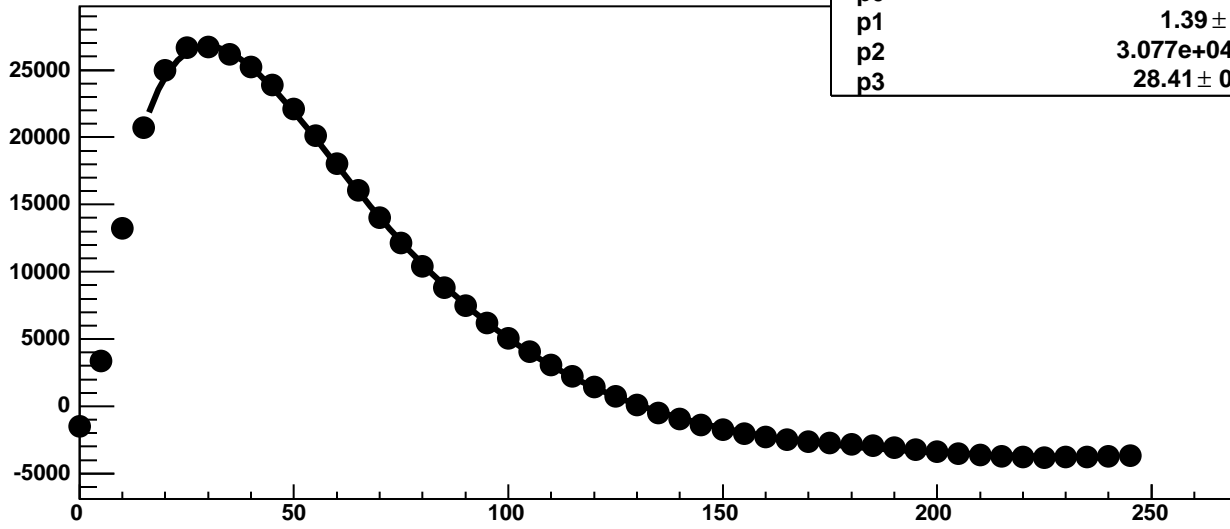
Chip 1, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

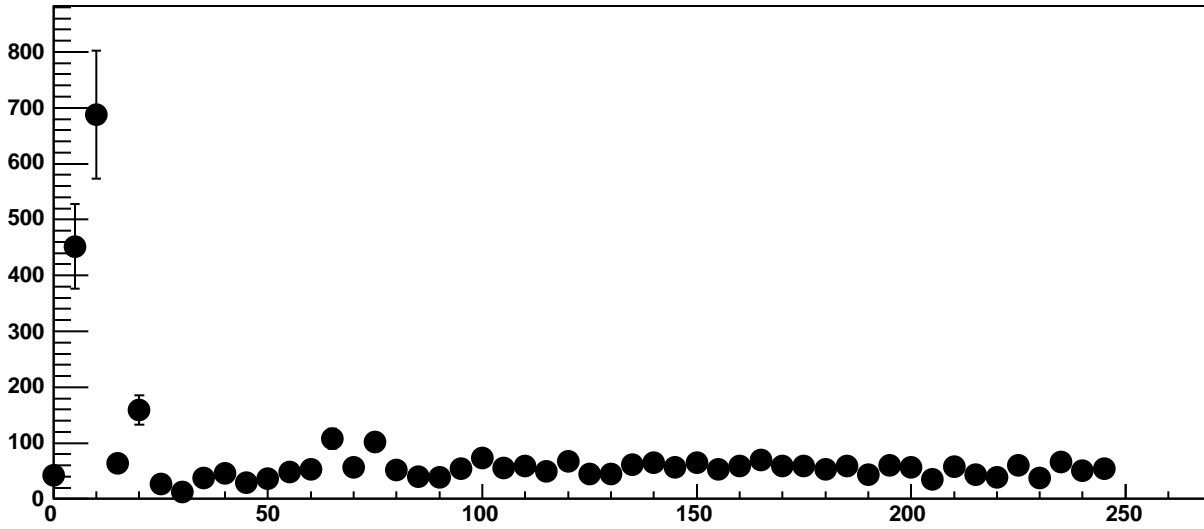


Chip 1, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

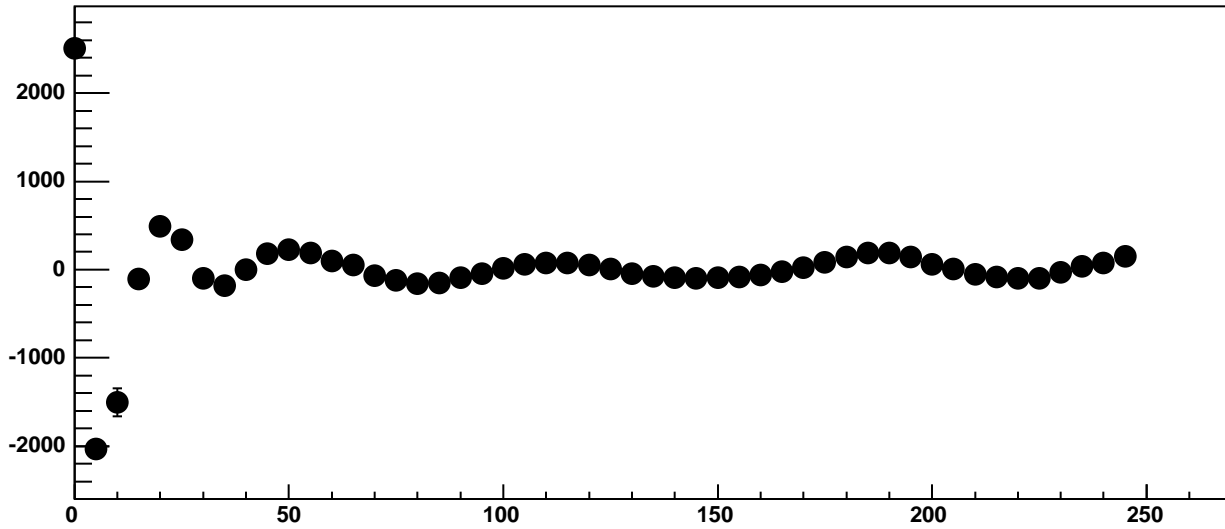


$\chi^2 / \text{ndf}$	8721 / 42
p0	$-3977 \pm 3.121$
p1	$1.39 \pm 0.01533$
p2	$3.077\text{e}+04 \pm 3.629$
p3	$28.41 \pm 0.008835$

Chip 1, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

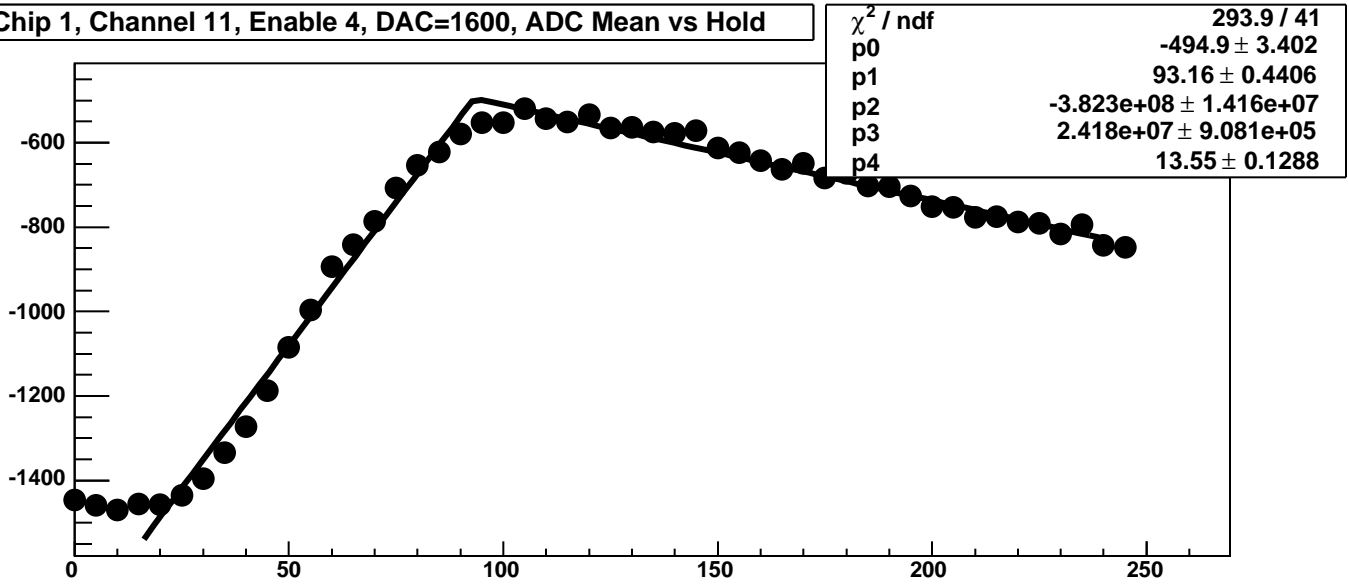


Chip 1, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold

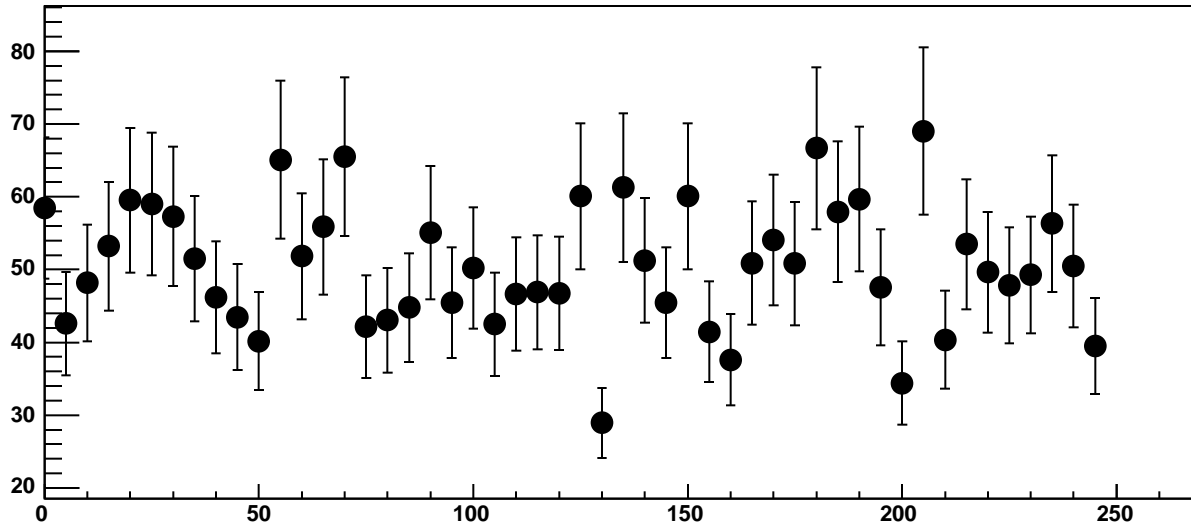




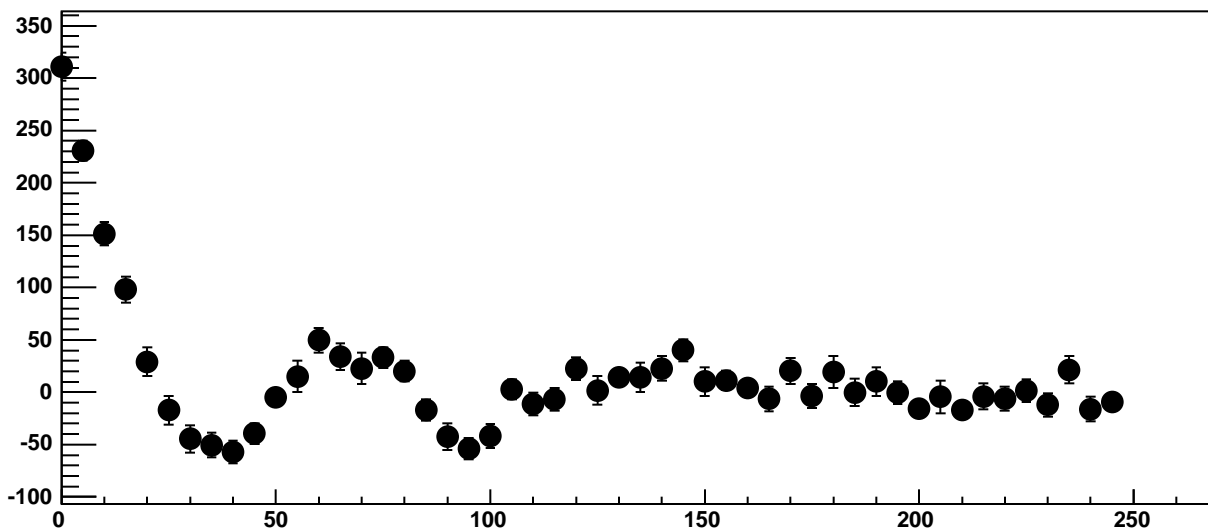
Chip 1, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold



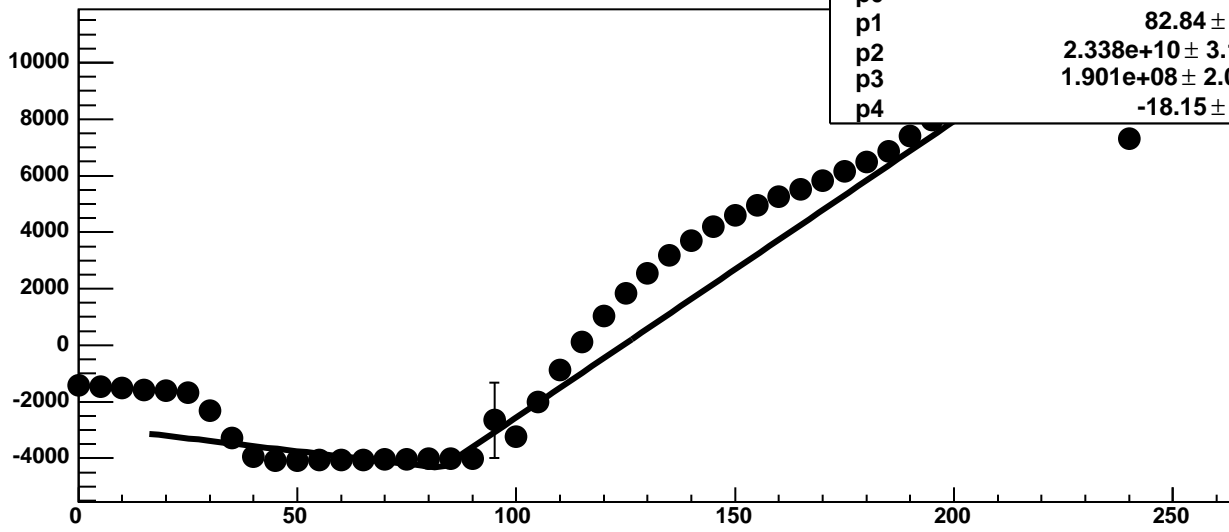
Chip 1, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

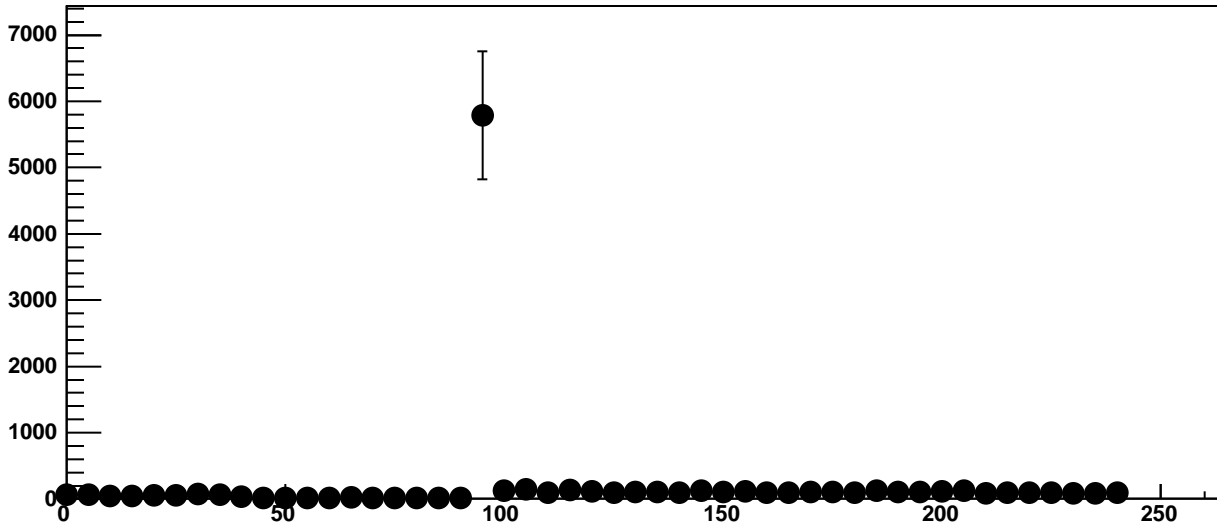


Chip 1, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

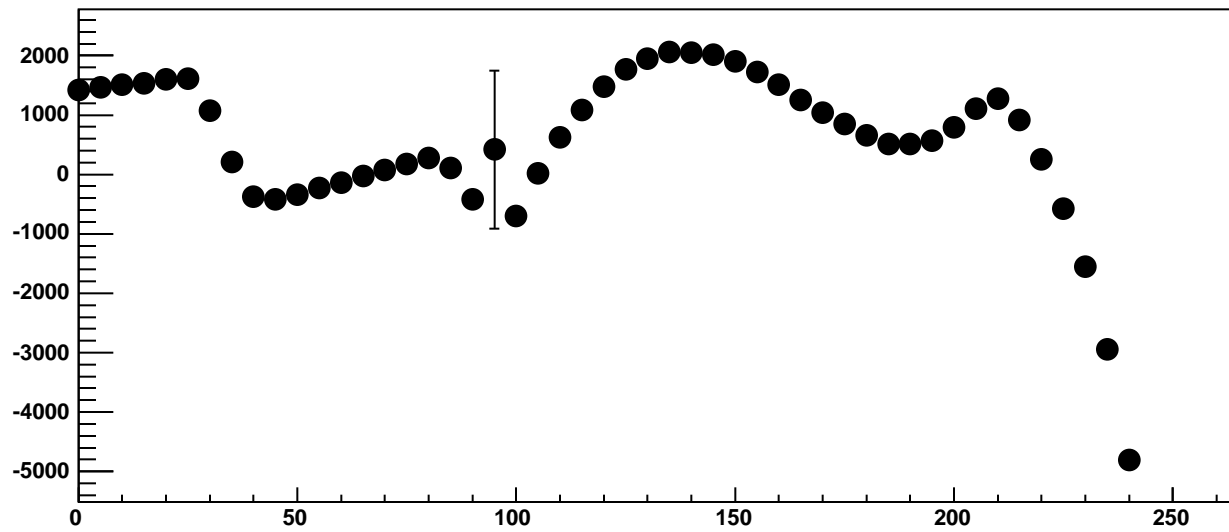


$\chi^2 / \text{ndf}$	2.499e+05 / 41
p0	-4346 ± 2.022
p1	82.84 ± 0.02926
p2	2.338e+10 ± 3.144e+07
p3	1.901e+08 ± 2.054e+05
p4	-18.15 ± 0.08746

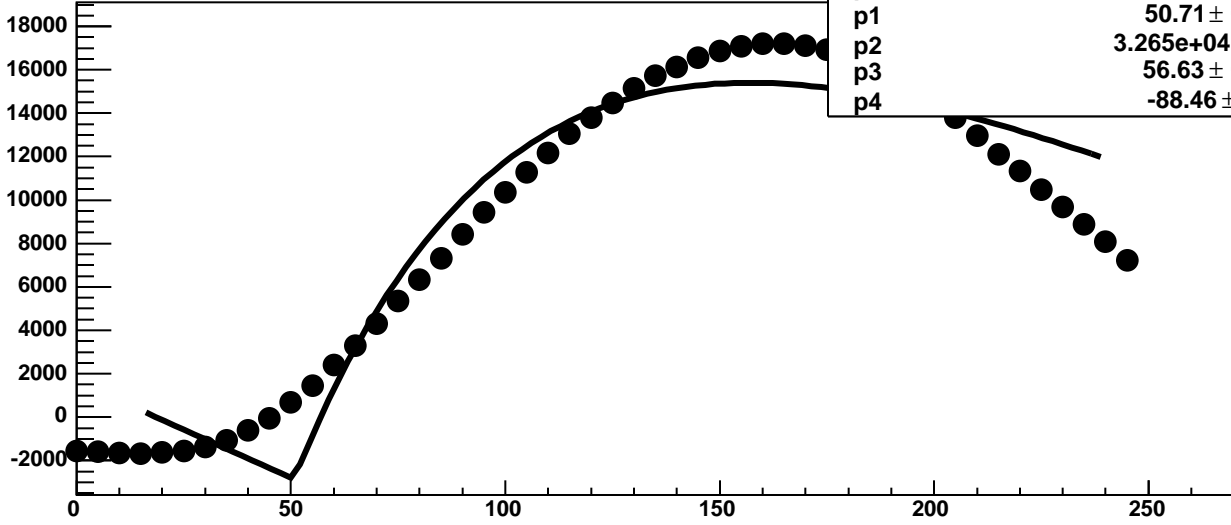
Chip 1, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



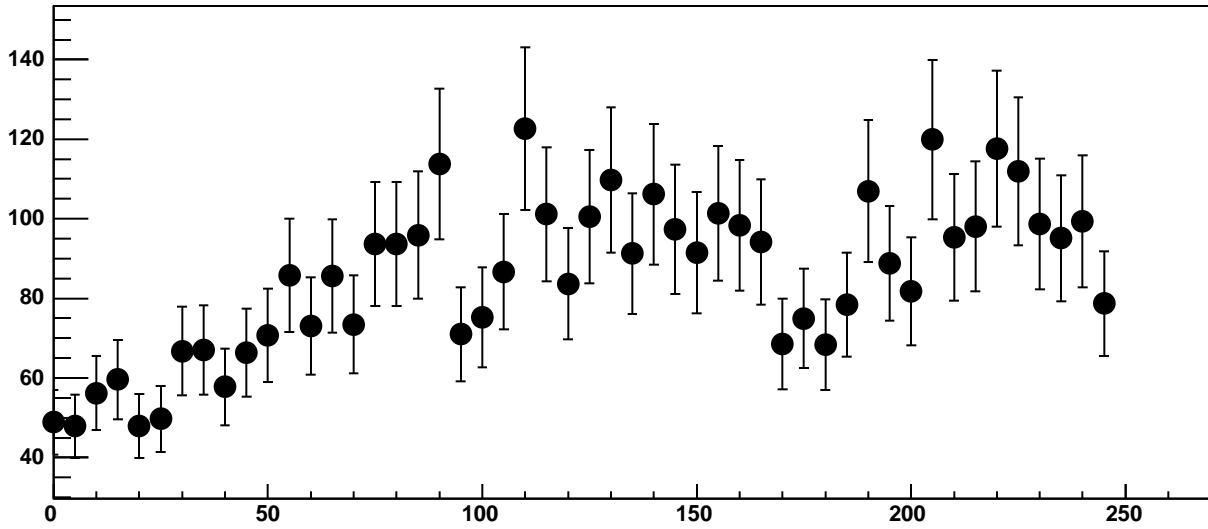
Chip 1, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



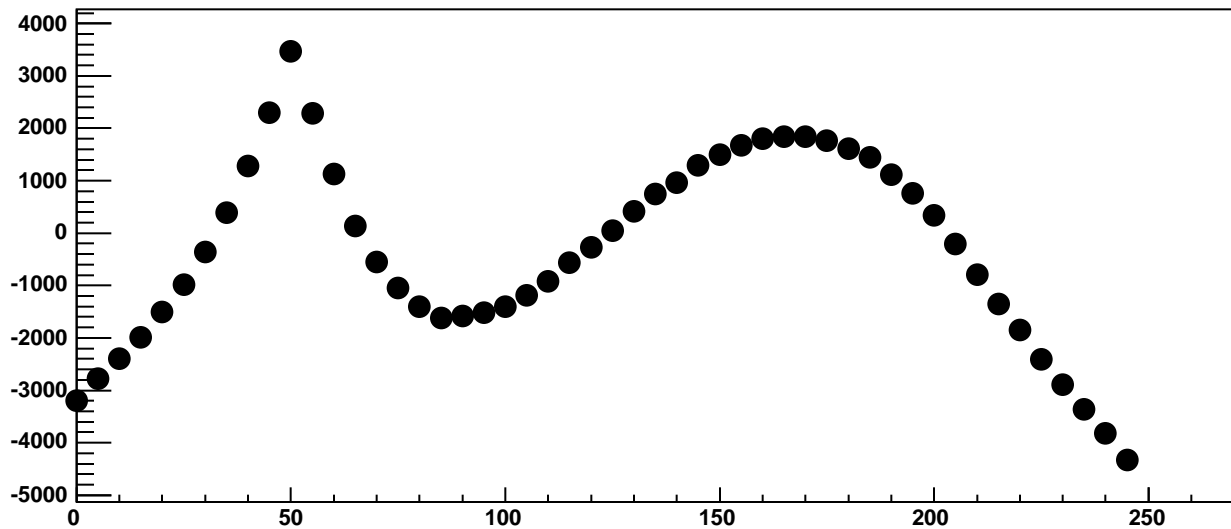
Chip 1, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



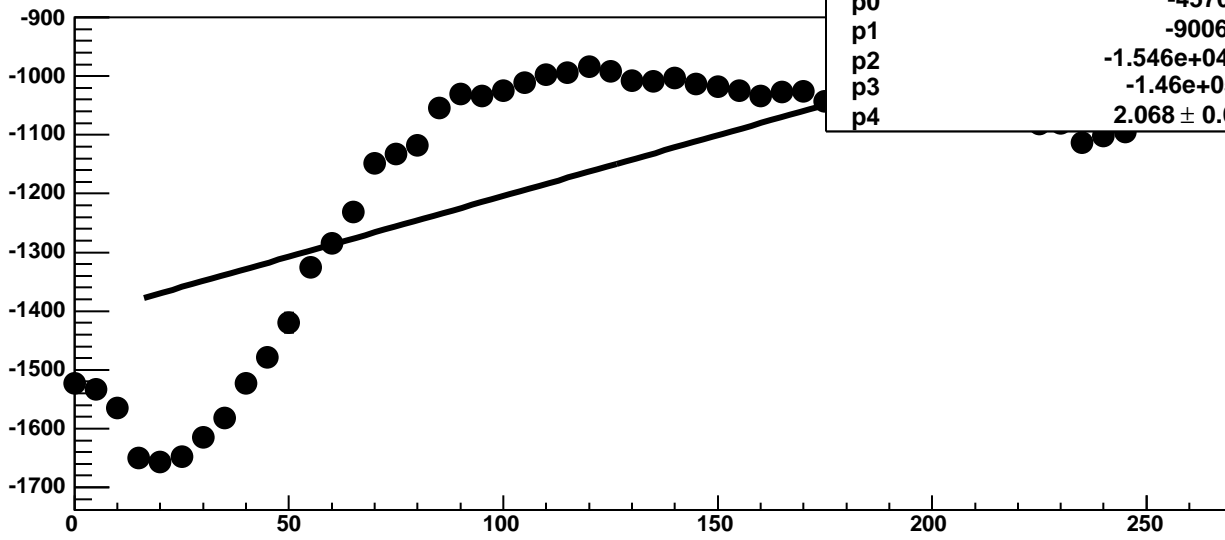
Chip 1, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



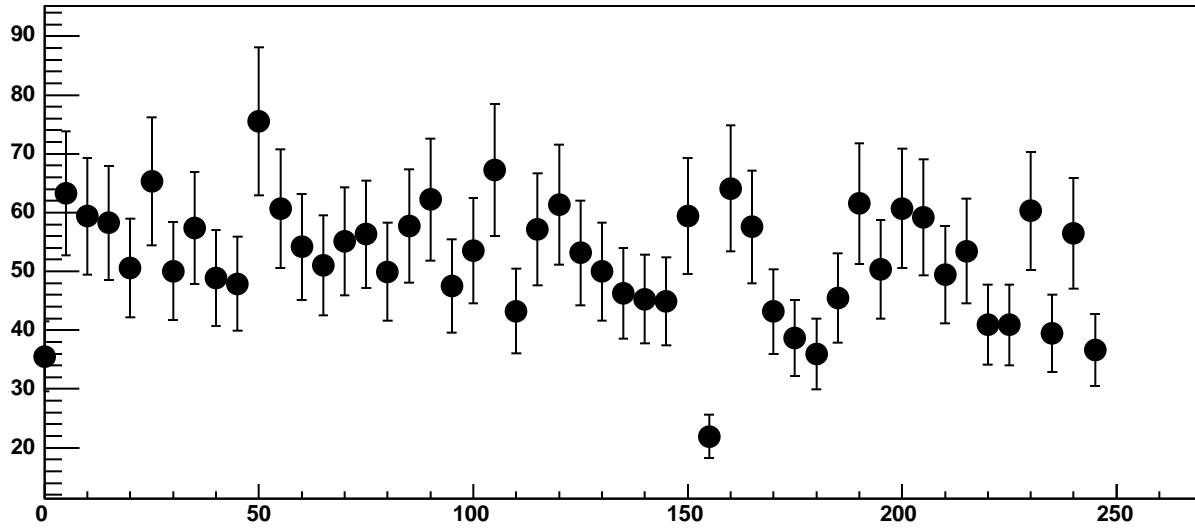
Chip 1, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold



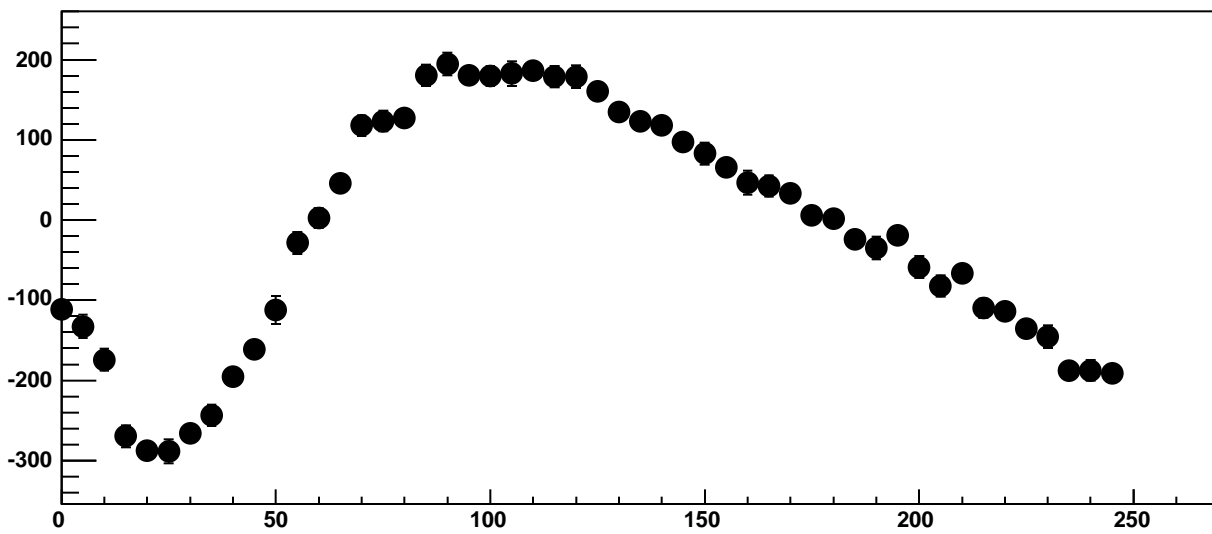
Chip 1, Channel 12, Enable 1, DAC=1600, ADC Mean vs Hold



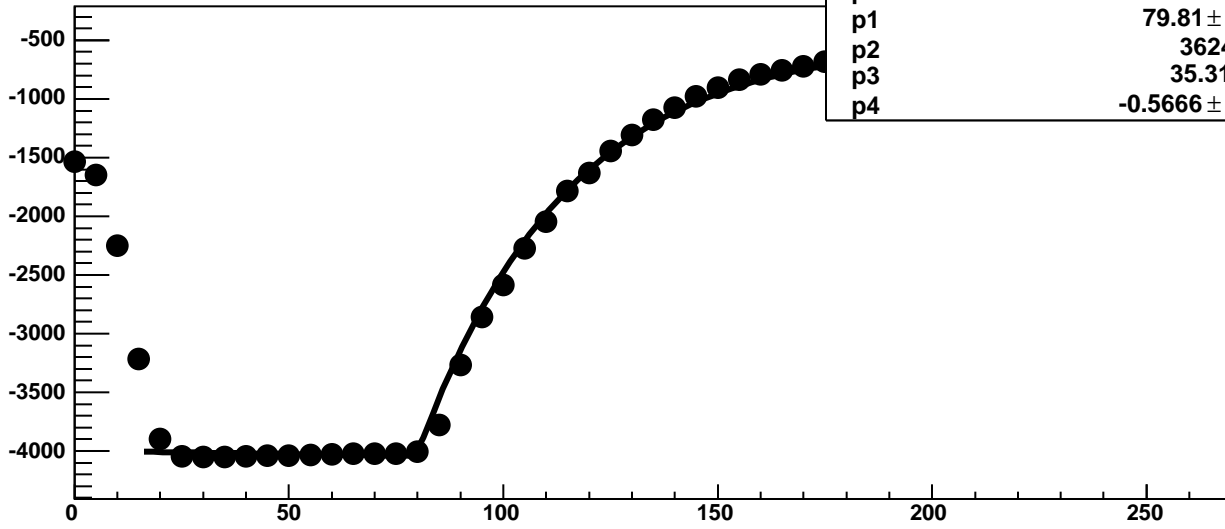
Chip 1, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold

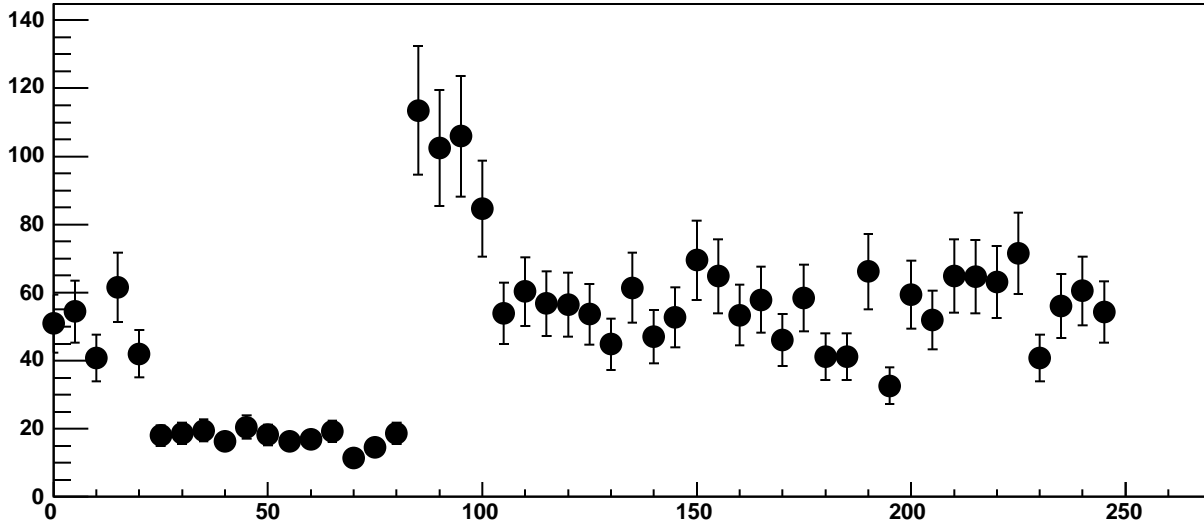


Chip 1, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

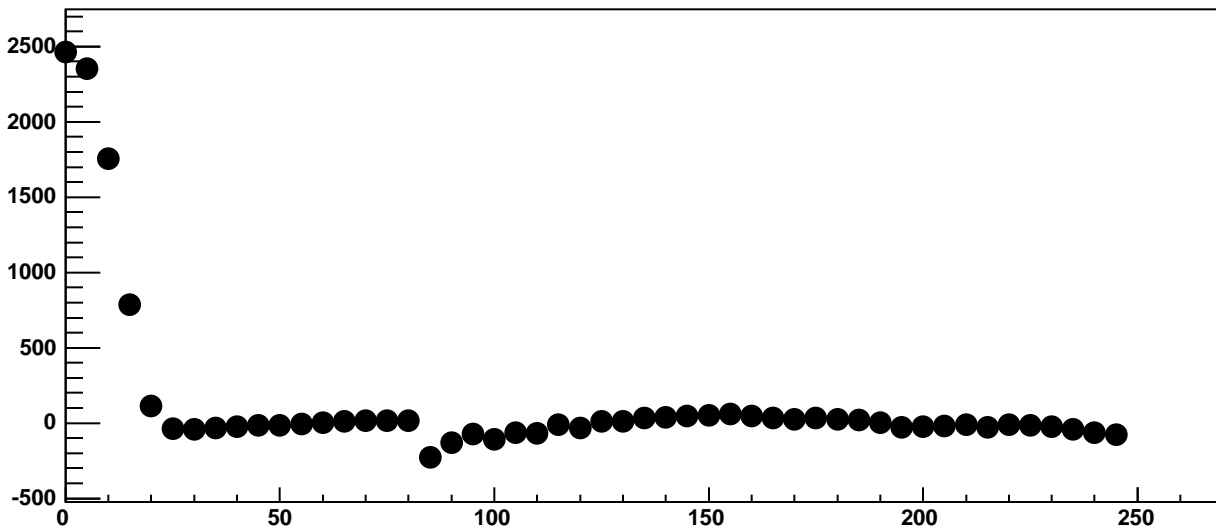


$\chi^2 / \text{ndf}$	3986 / 41
p0	$-4042 \pm 2.033$
p1	$79.81 \pm 0.04597$
p2	$3624 \pm 11.91$
p3	$35.31 \pm 0.198$
p4	$-0.5666 \pm 0.06352$

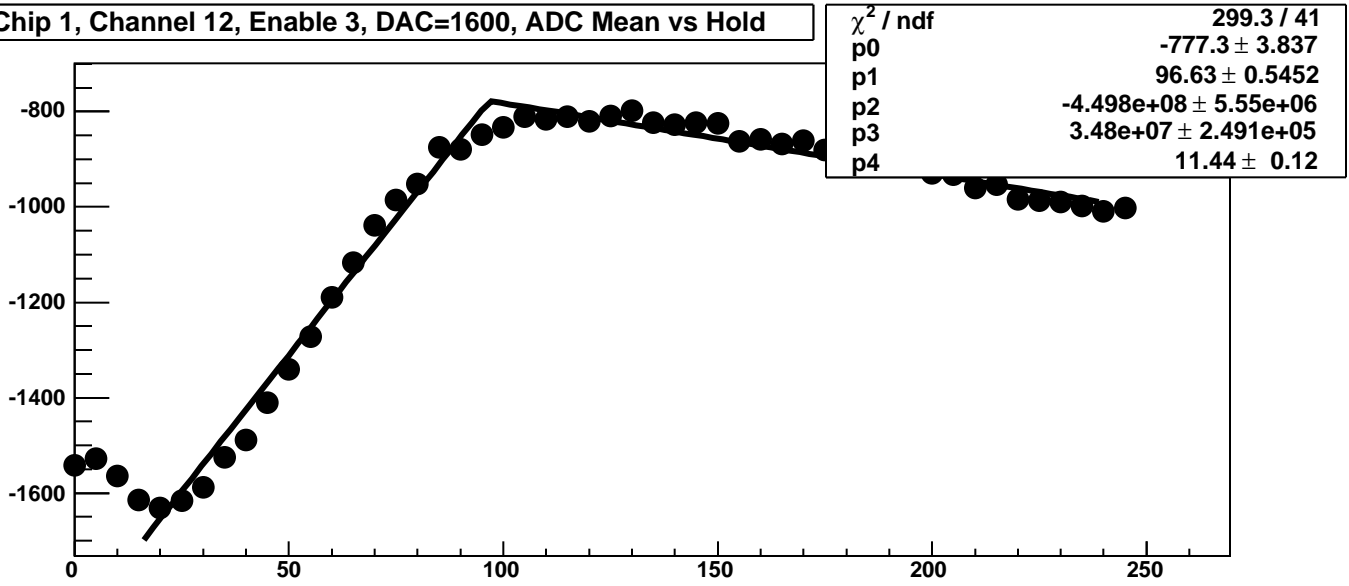
Chip 1, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



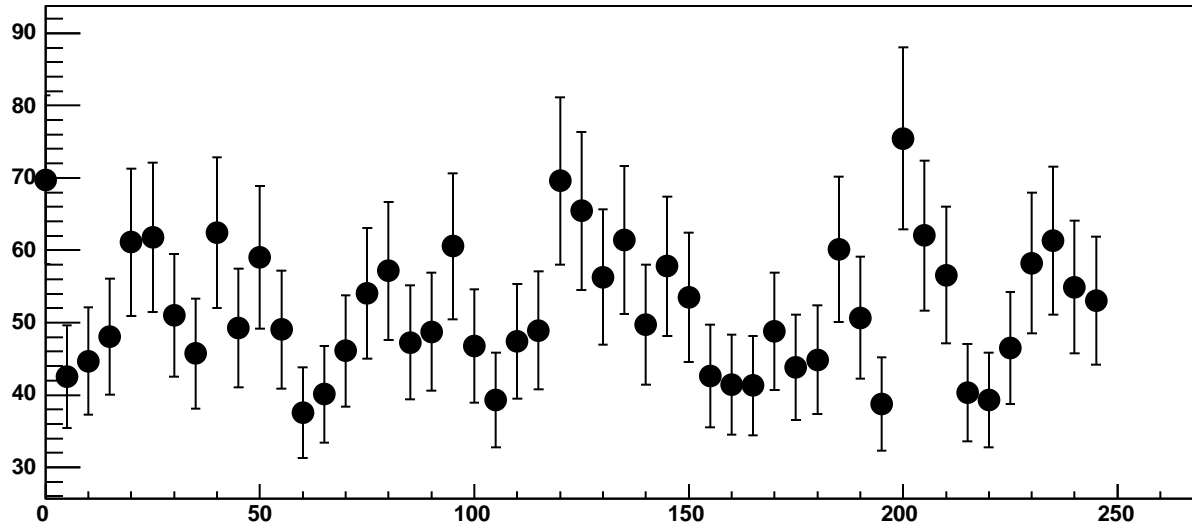
Chip 1, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold



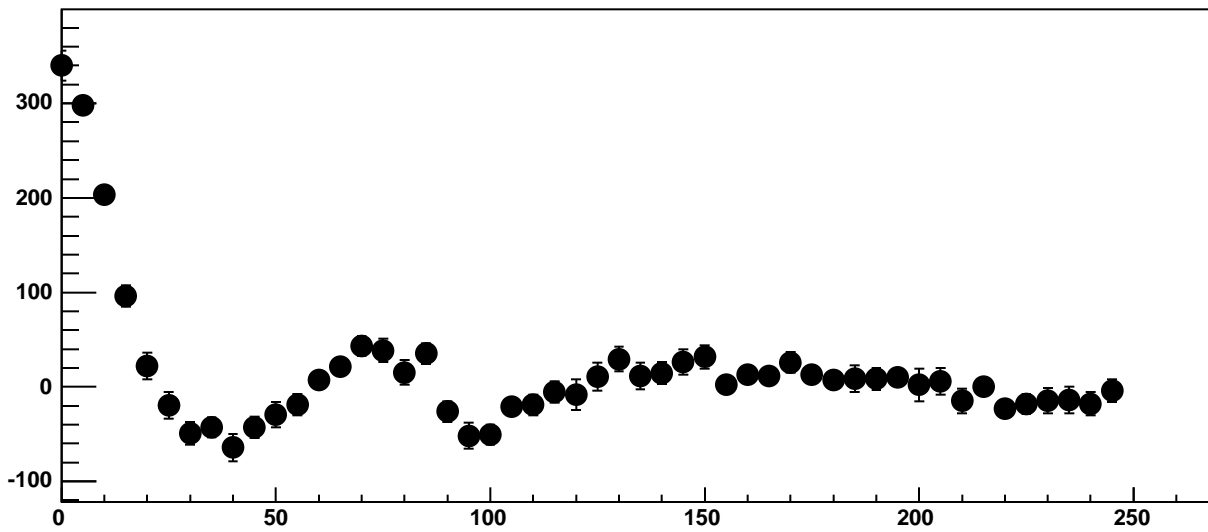
Chip 1, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold



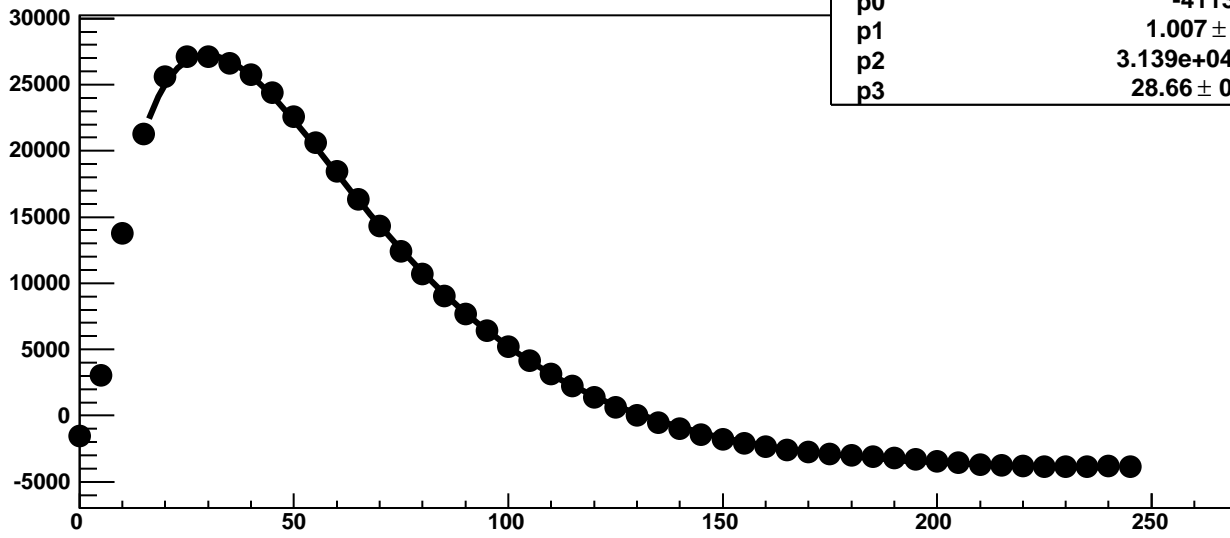
Chip 1, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

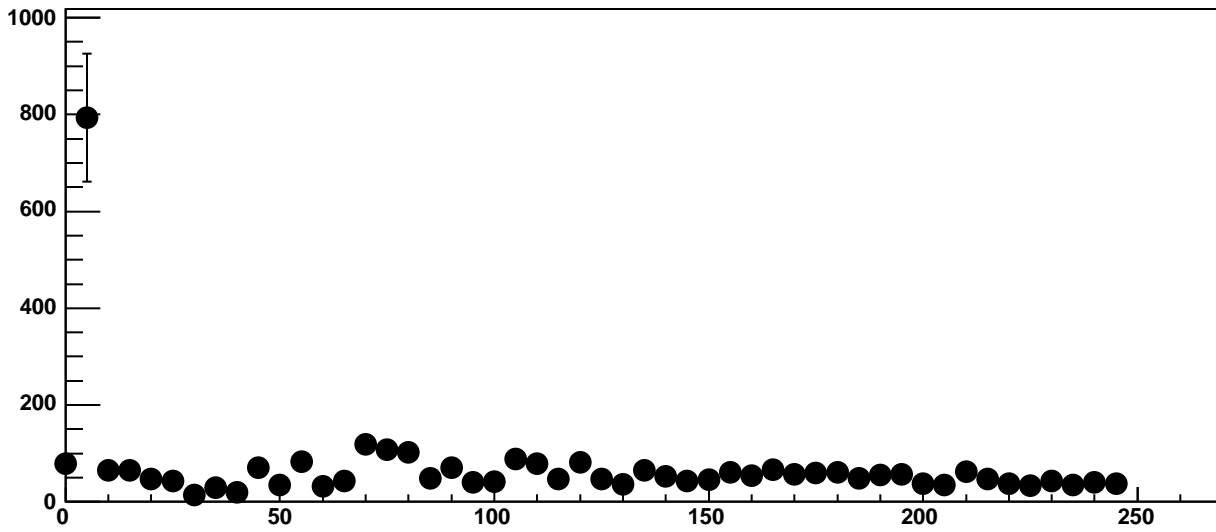


Chip 1, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold

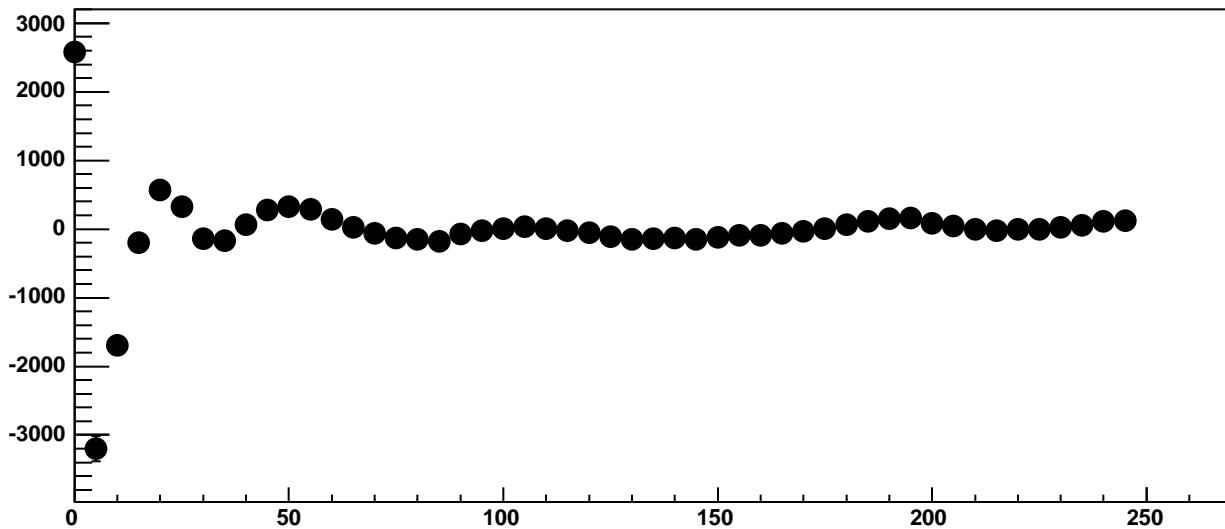


$\chi^2 / \text{ndf}$	1.129e+04 / 42
p0	-4113 ± 2.822
p1	1.007 ± 0.01399
p2	3.139e+04 ± 3.476
p3	28.66 ± 0.008413

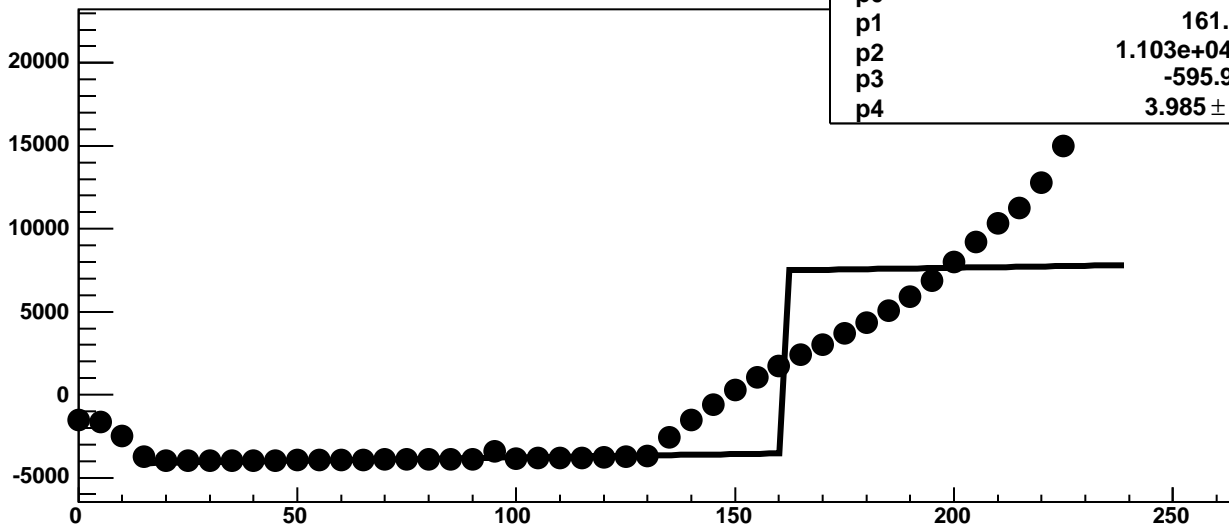
Chip 1, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold

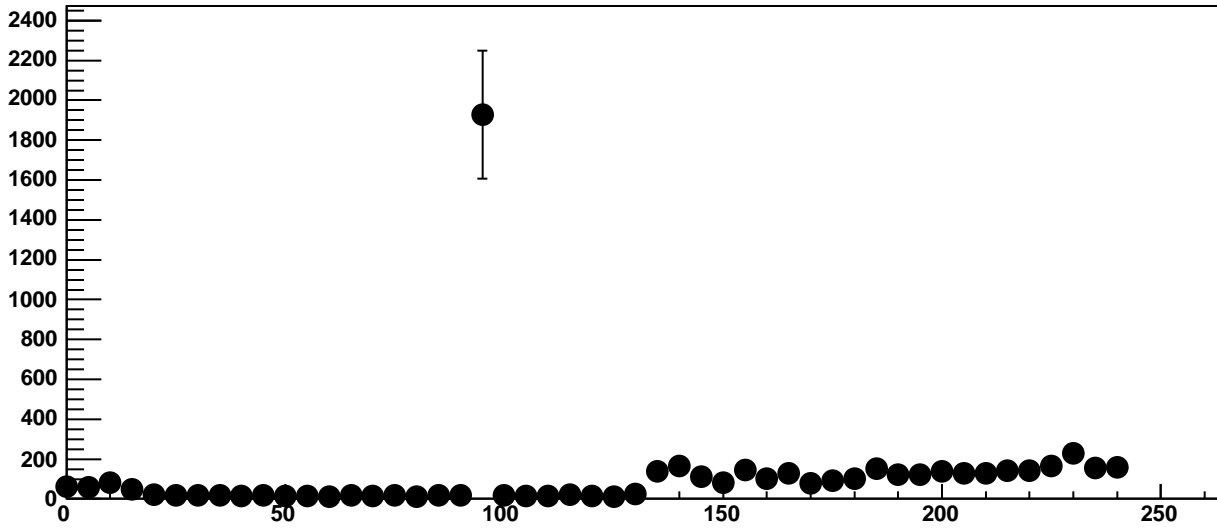


Chip 1, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

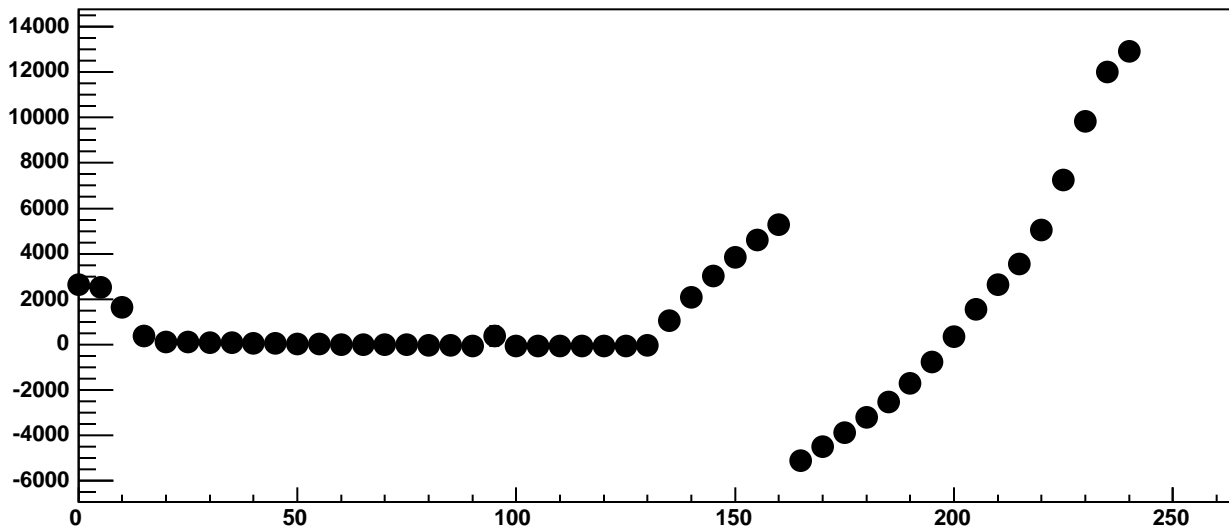


$\chi^2 / \text{ndf}$	6.48e+05 / 41
p0	-3536 ± 2.578
p1	161.1 ± 2.38
p2	1.103e+04 ± 6.285
p3	-595.9 ± 9.287
p4	3.985 ± 0.04072

Chip 1, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

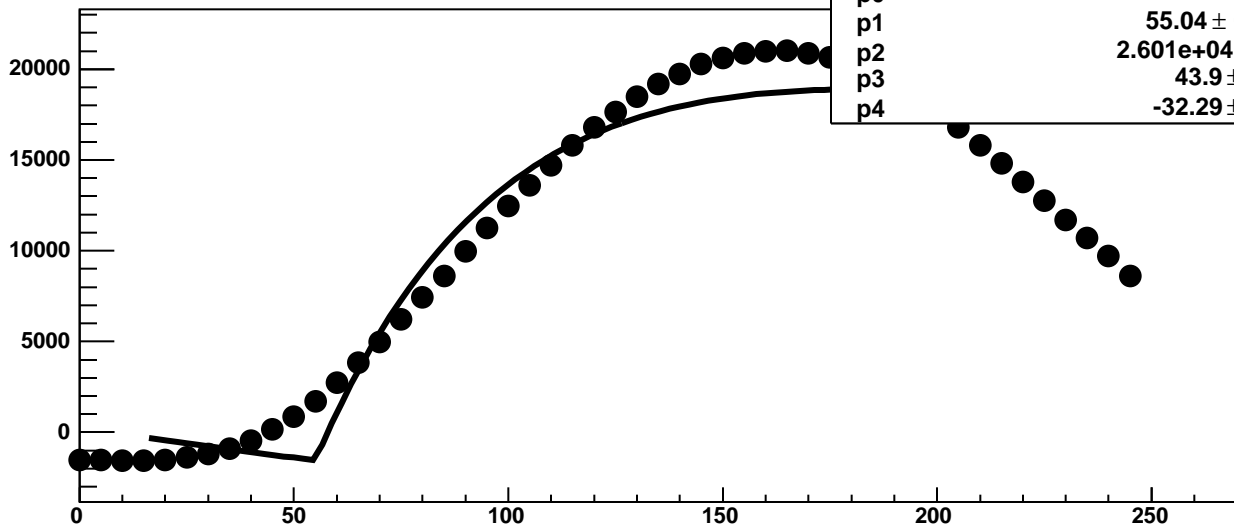


Chip 1, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold

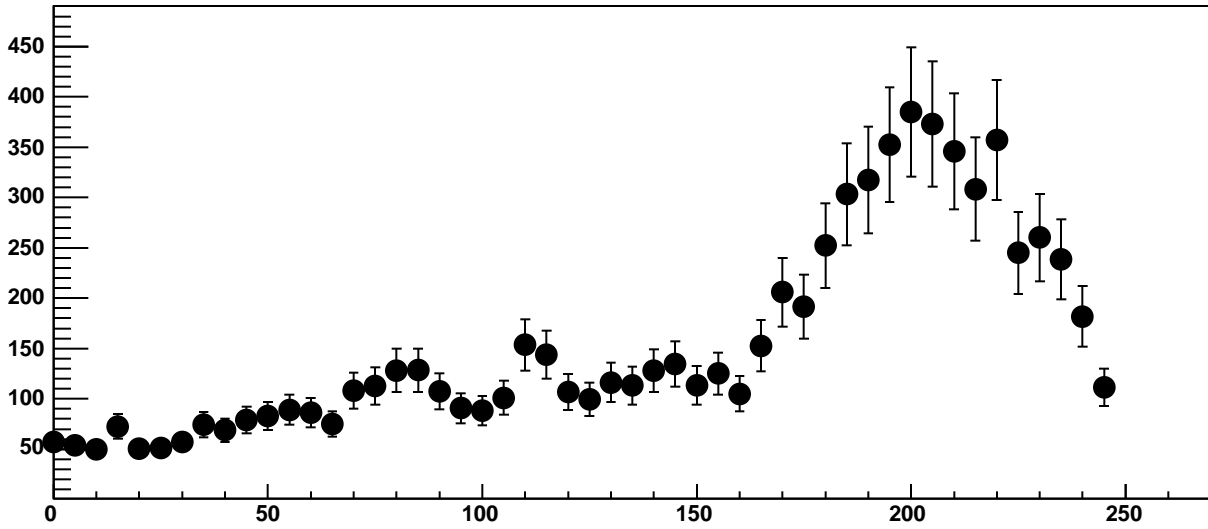




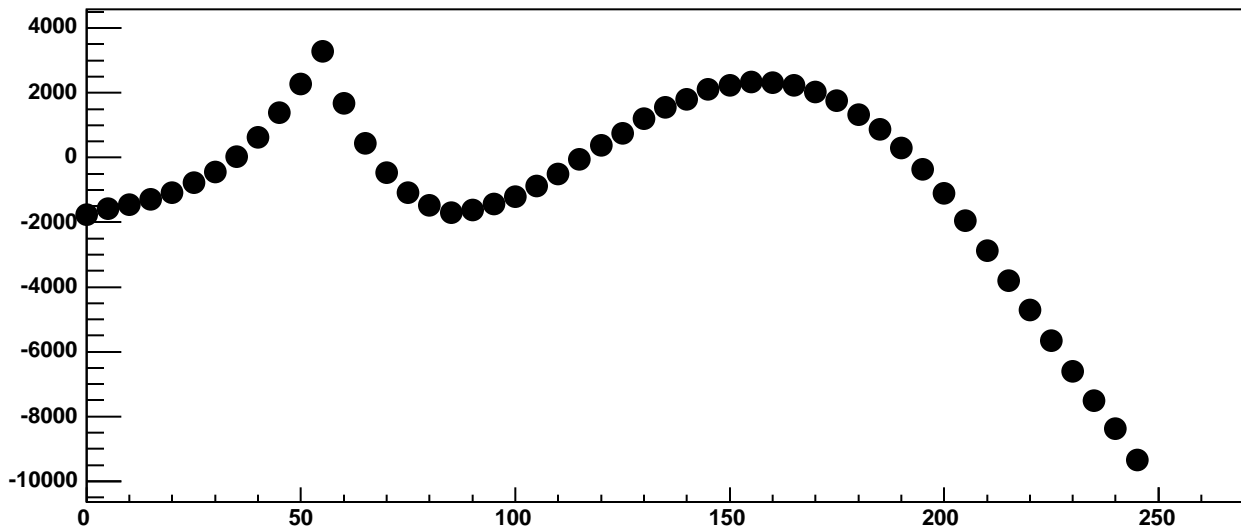
Chip 1, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold



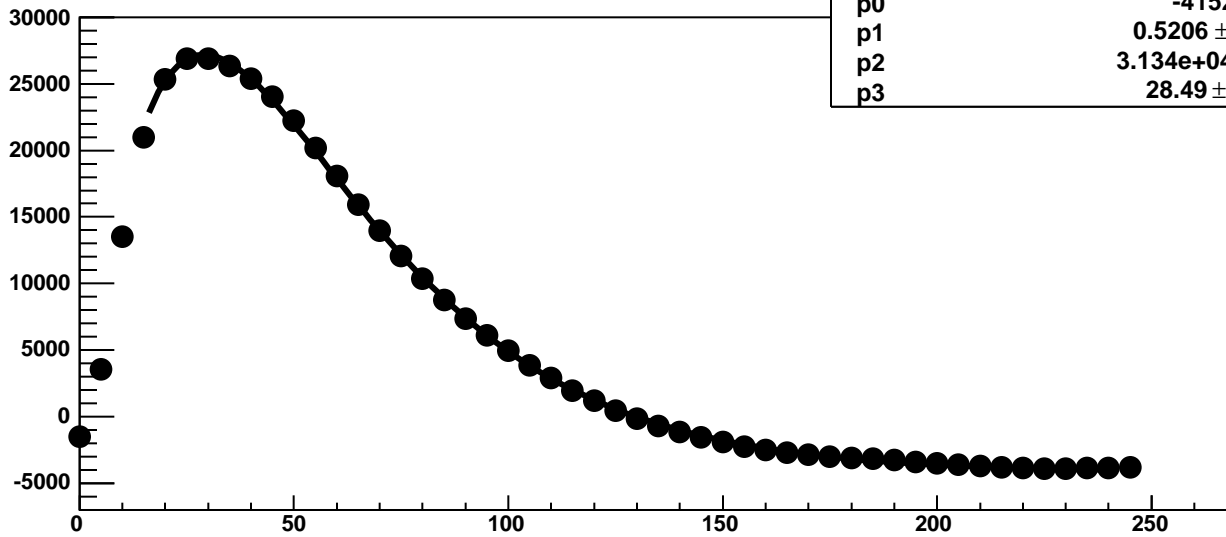
Chip 1, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

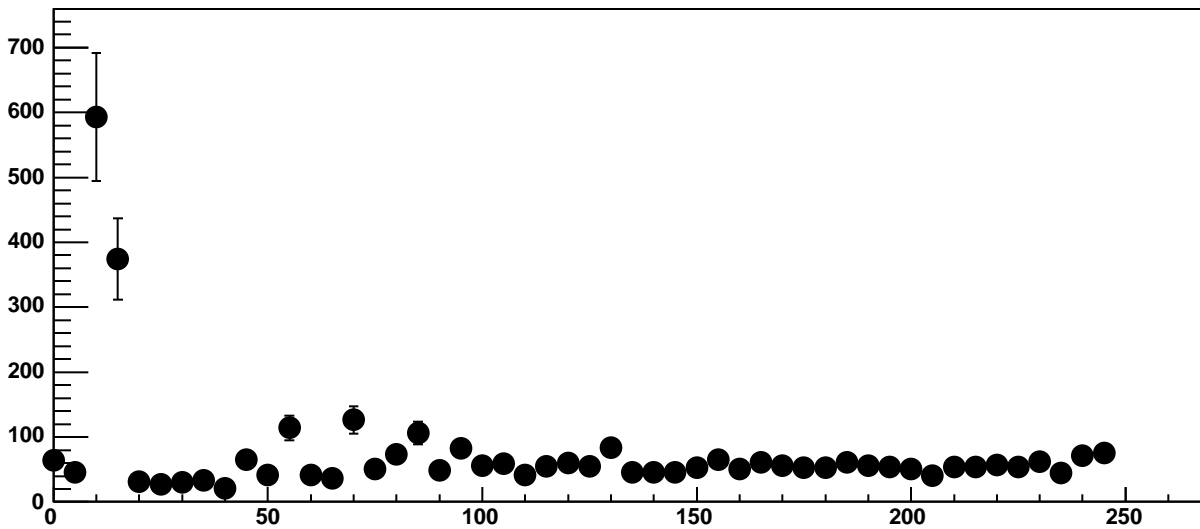


Chip 1, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold

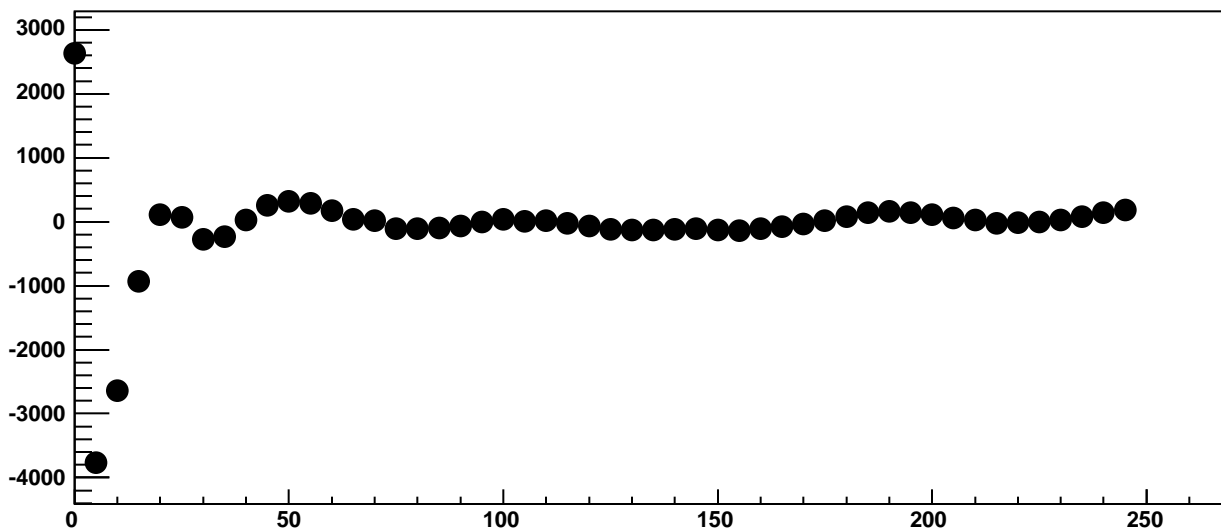


$\chi^2 / \text{ndf}$	6809 / 42
p0	-4152 ± 3.432
p1	0.5206 ± 0.01671
p2	3.134e+04 ± 4.062
p3	28.49 ± 0.01012

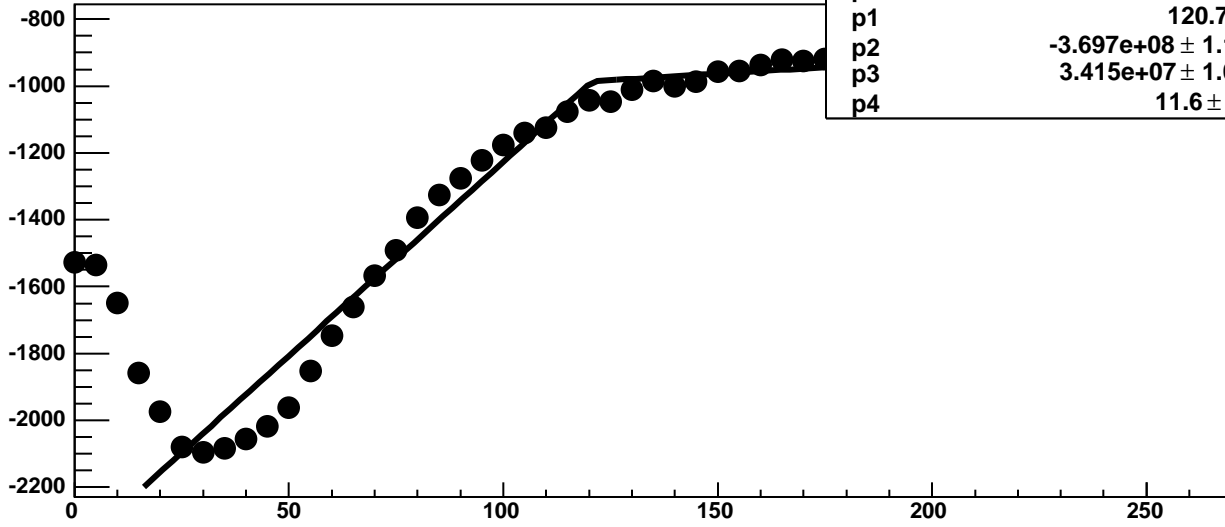
Chip 1, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

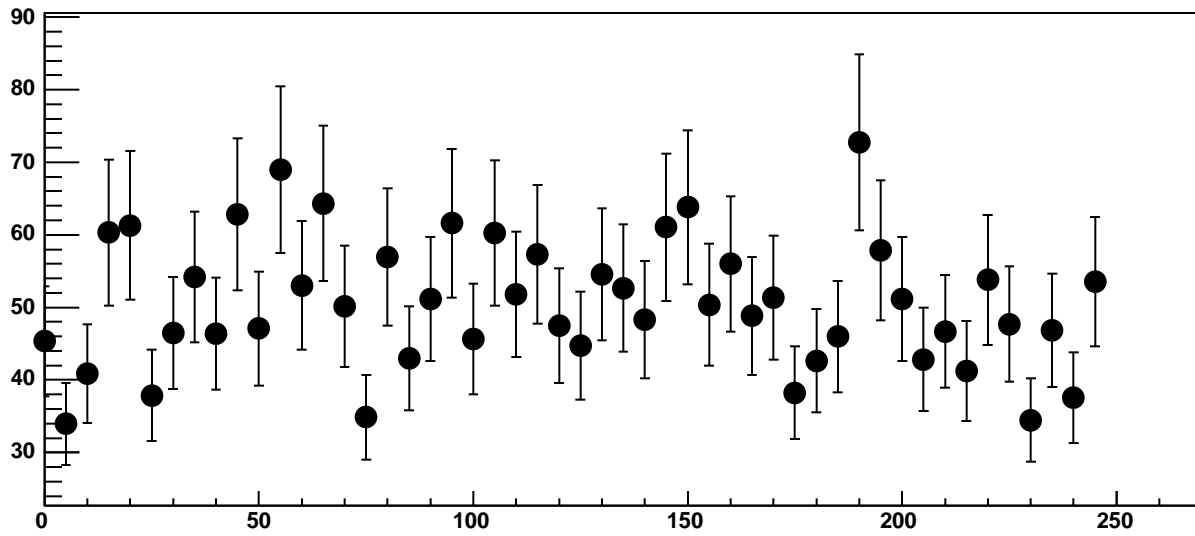


Chip 1, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

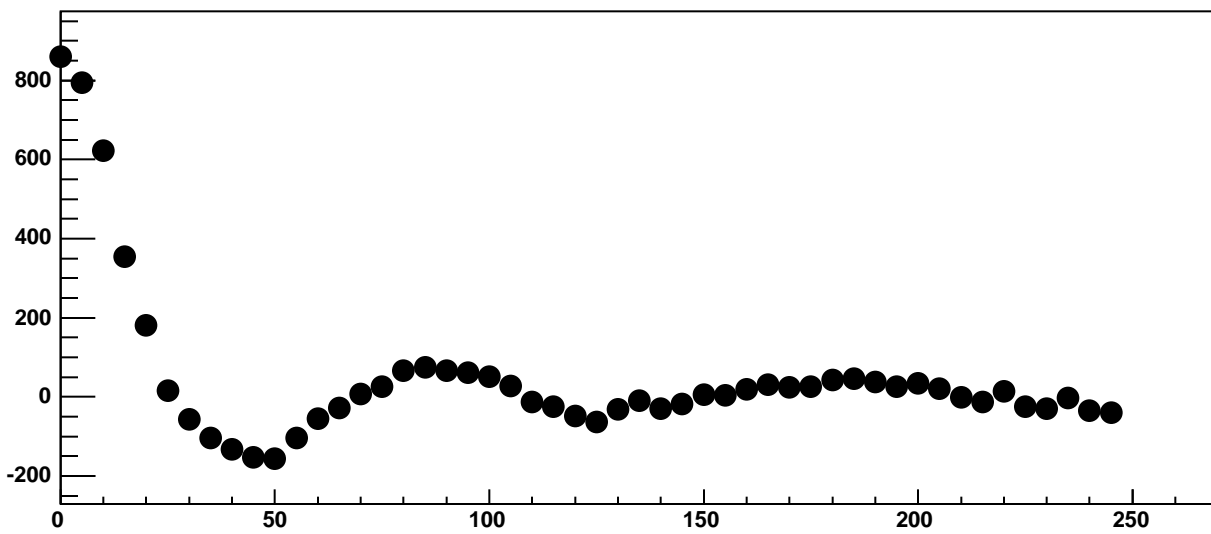


$\chi^2 / \text{ndf}$	1839 / 41
p0	-985.9 ± 5.127
p1	120.7 ± 0.632
p2	-3.697e+08 ± 1.172e+07
p3	3.415e+07 ± 1.096e+06
p4	11.6 ± 0.07884

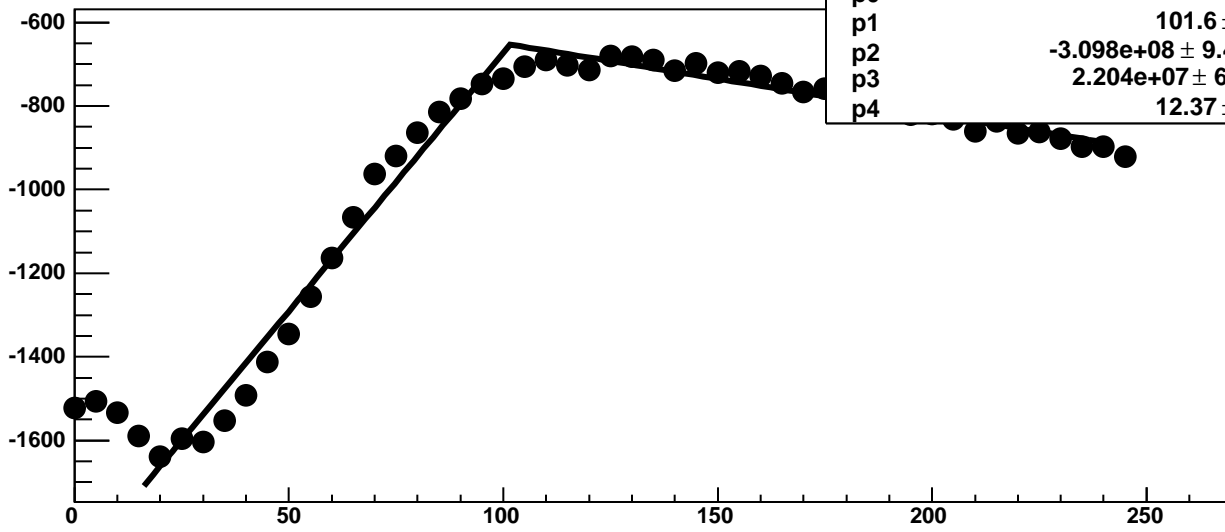
Chip 1, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

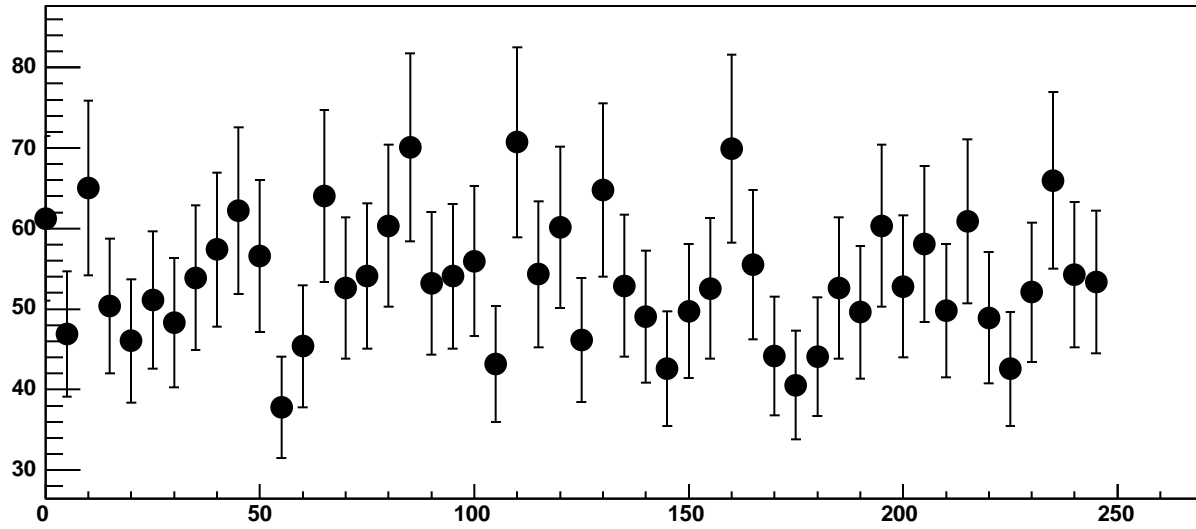


Chip 1, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

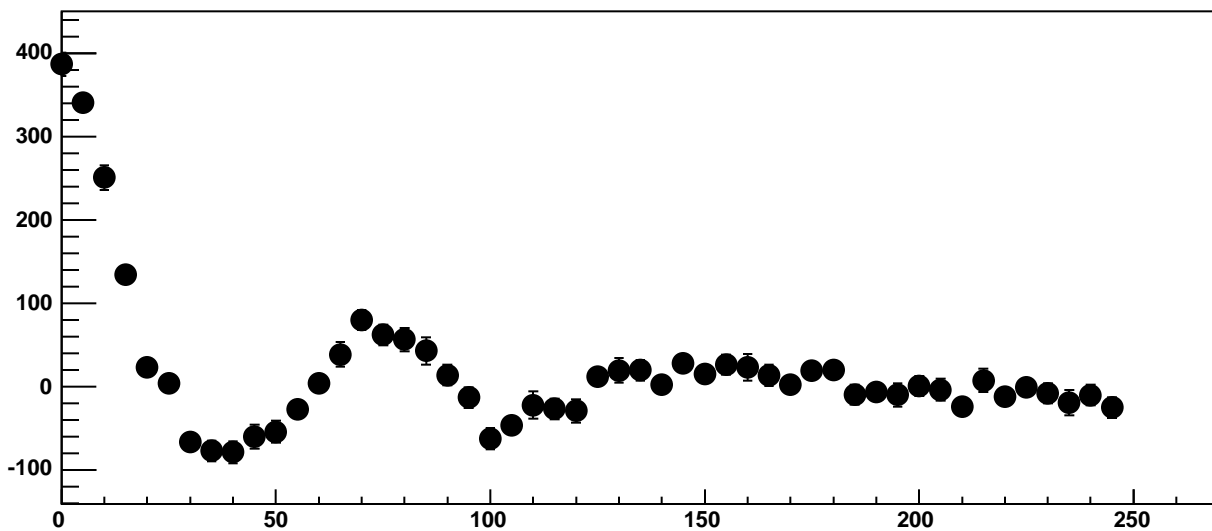


$\chi^2 / \text{ndf}$	495.9 / 41
p0	$-652.8 \pm 4.087$
p1	$101.6 \pm 0.5307$
p2	$-3.098\text{e}+08 \pm 9.413\text{e}+06$
p3	$2.204\text{e}+07 \pm 6.49\text{e}+05$
p4	$12.37 \pm 0.1106$

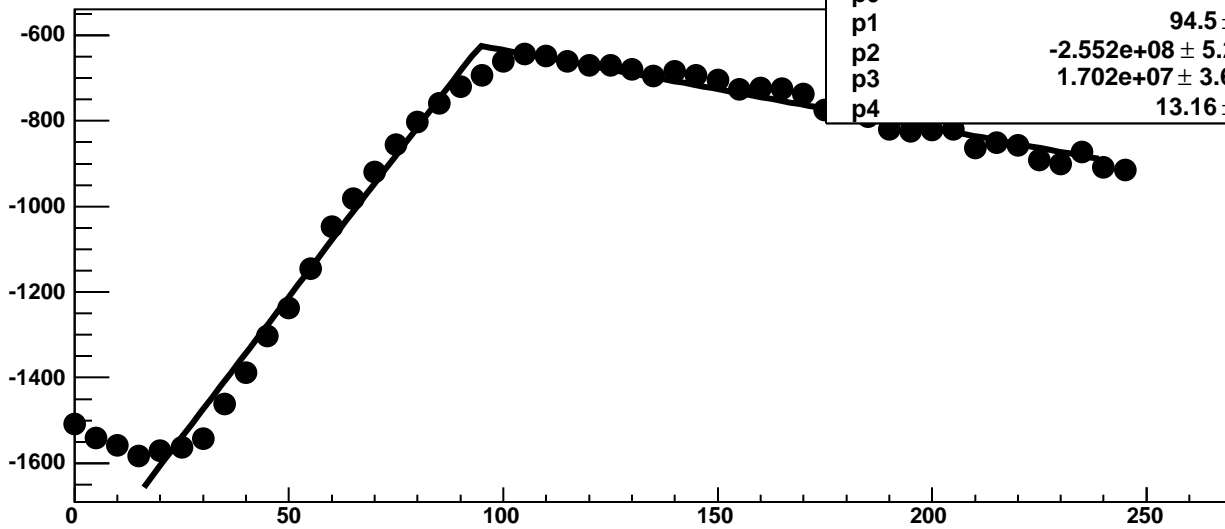
Chip 1, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

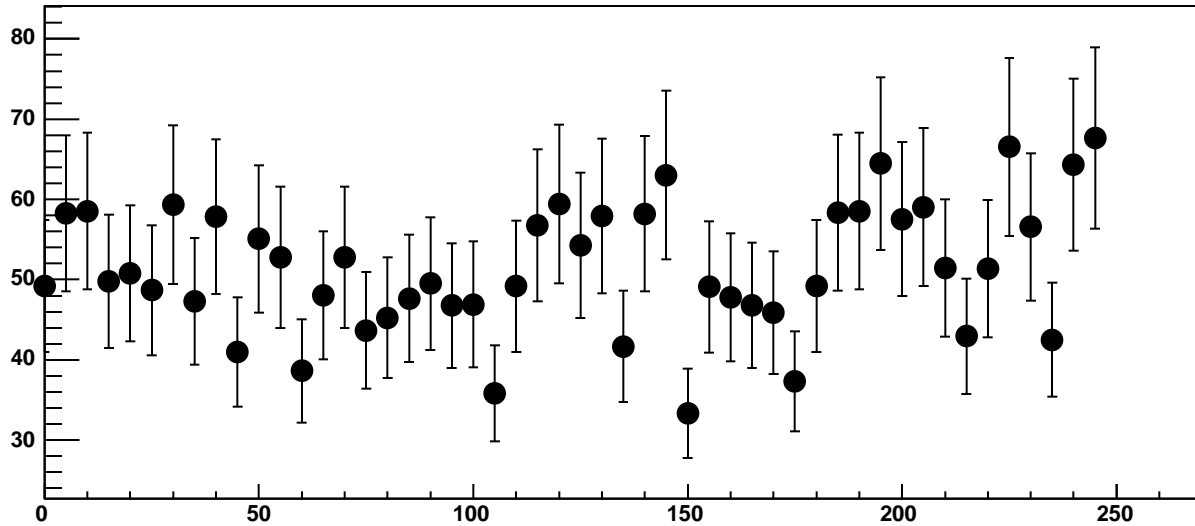


Chip 1, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold

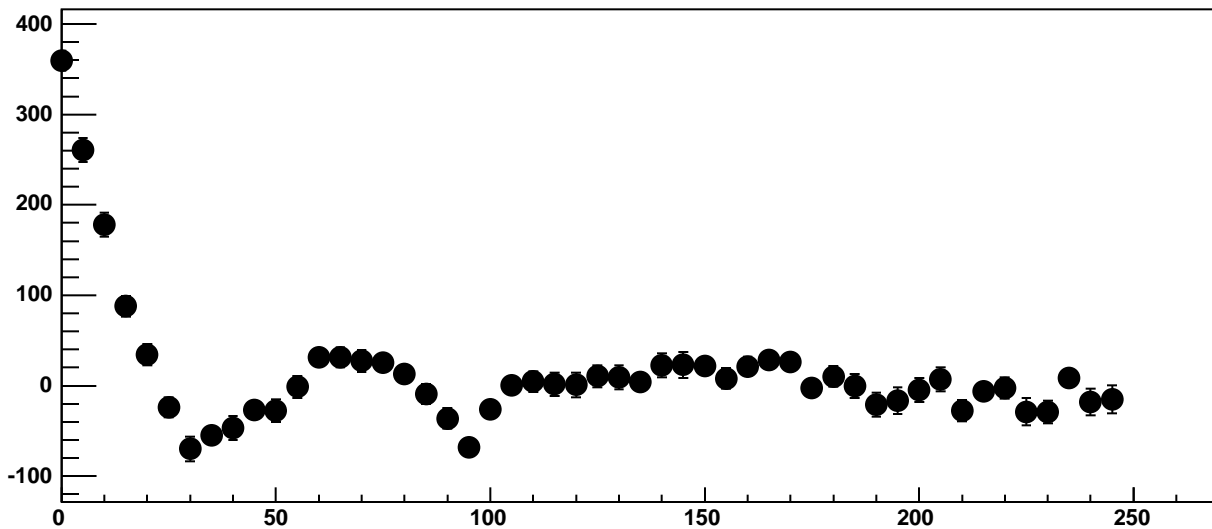


$\chi^2 / \text{ndf}$	293.7 / 41
p0	$-624.2 \pm 3.448$
p1	$94.5 \pm 0.4398$
p2	$-2.552\text{e}+08 \pm 5.282\text{e}+06$
p3	$1.702\text{e}+07 \pm 3.638\text{e}+05$
p4	$13.16 \pm 0.1129$

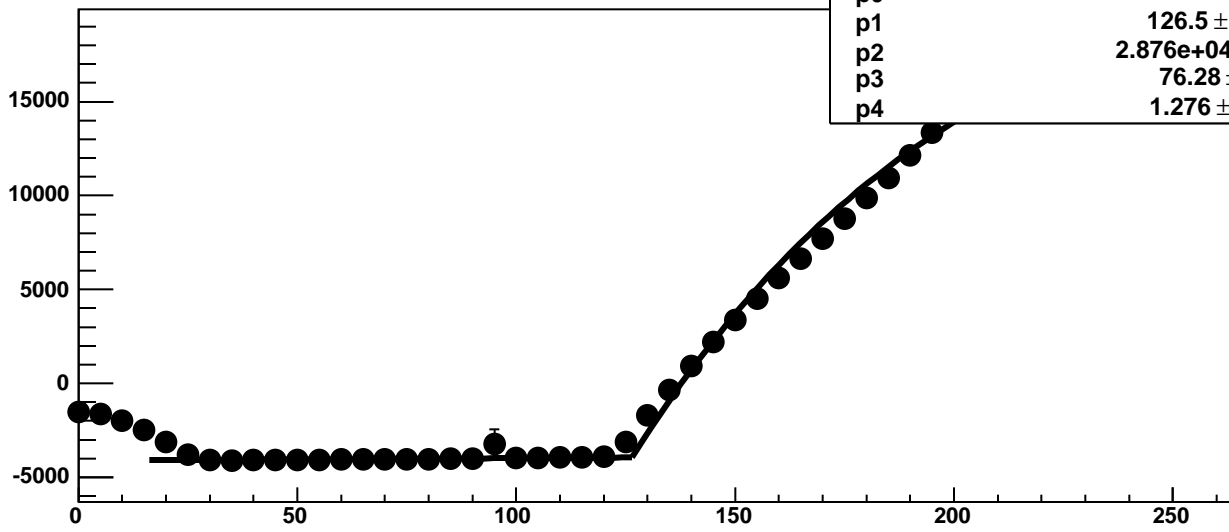
Chip 1, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

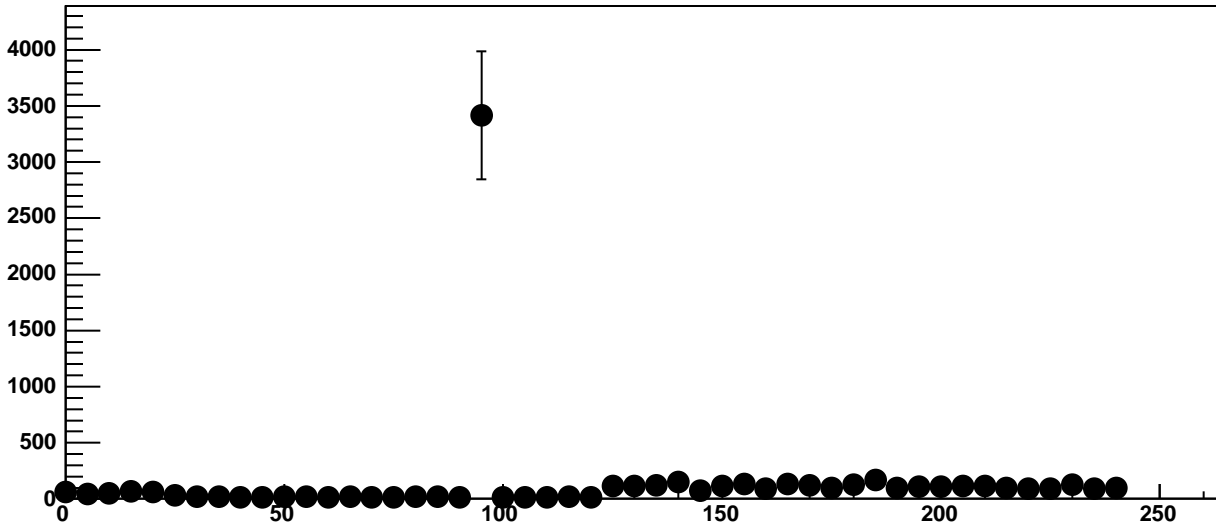


Chip 1, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

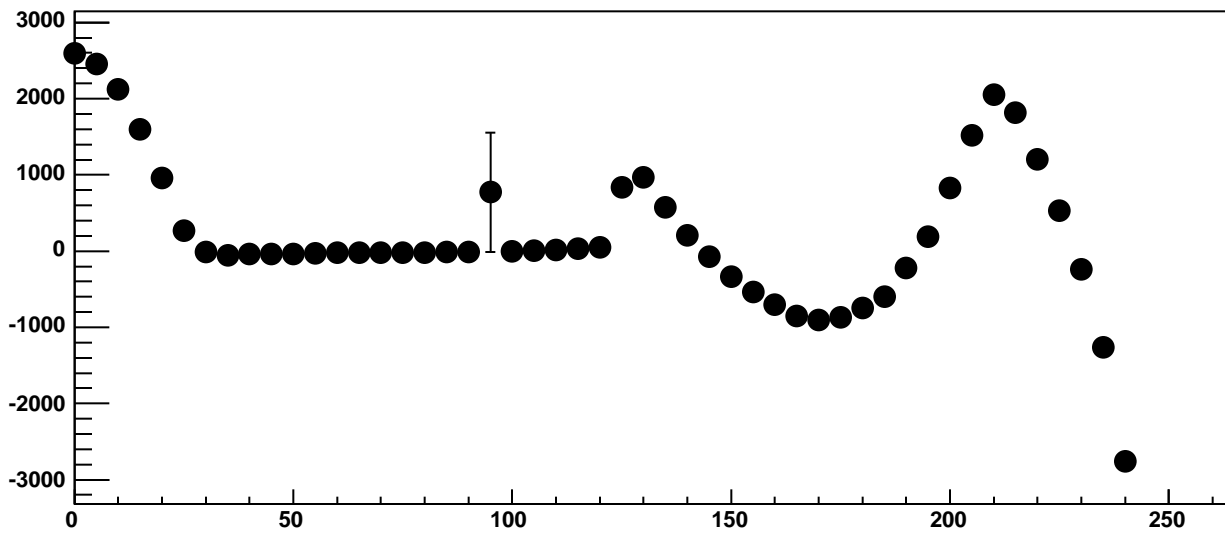


$\chi^2 / \text{ndf}$	6.411e+04 / 41
p0	-3951 ± 1.817
p1	126.5 ± 0.05181
p2	2.876e+04 ± 59.94
p3	76.28 ± 0.3218
p4	1.276 ± 0.03011

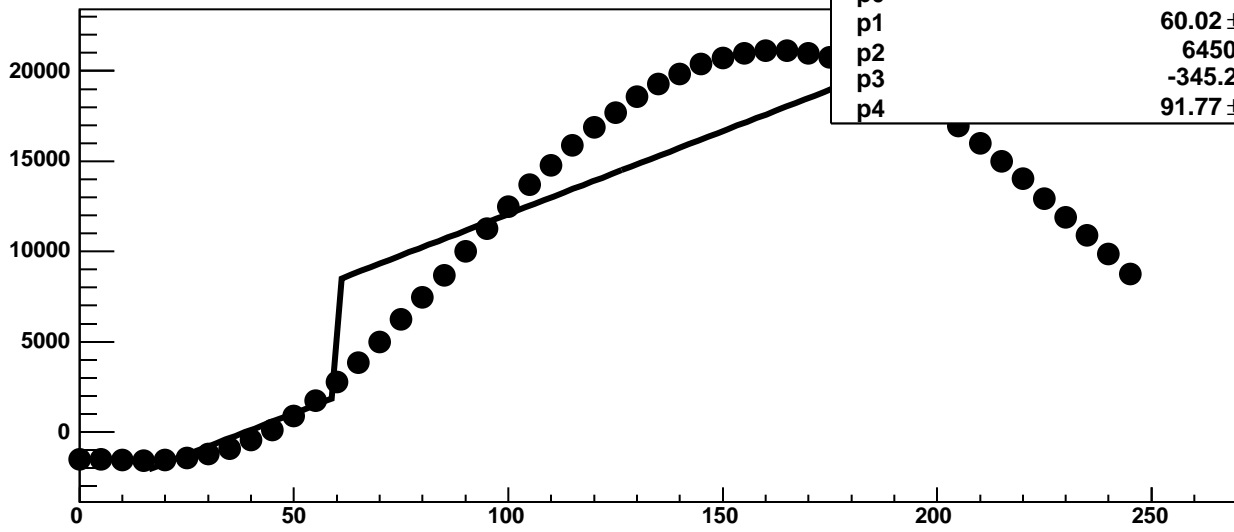
Chip 1, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

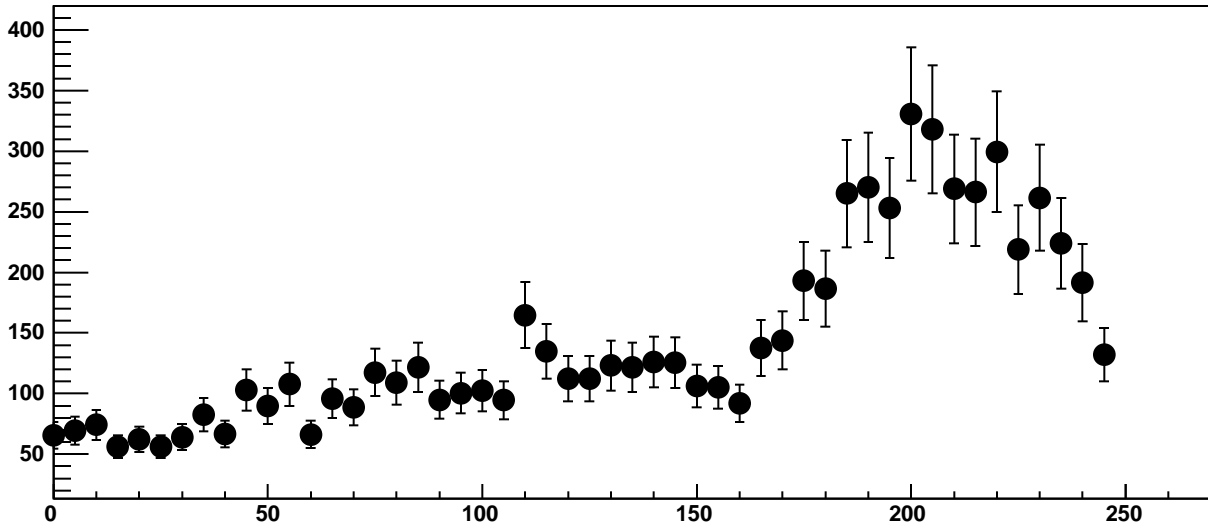


Chip 1, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

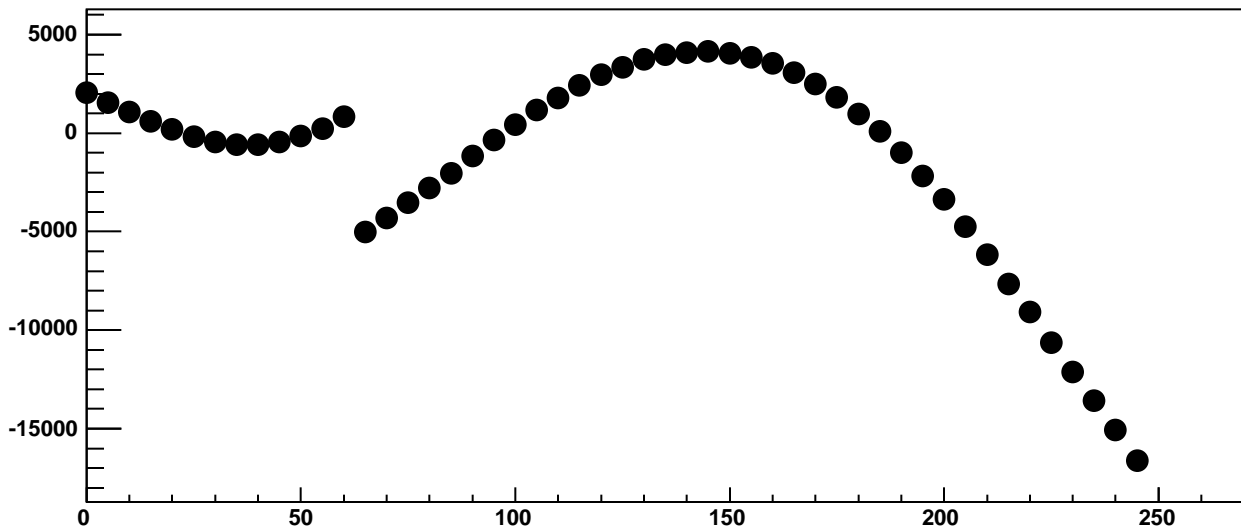


$\chi^2 / \text{ndf}$	6.873e+05 / 41
p0	1956 ± 15.1
p1	60.02 ± 0.2259
p2	6450 ± 34.41
p3	-345.2 ± 11.98
p4	91.77 ± 0.4618

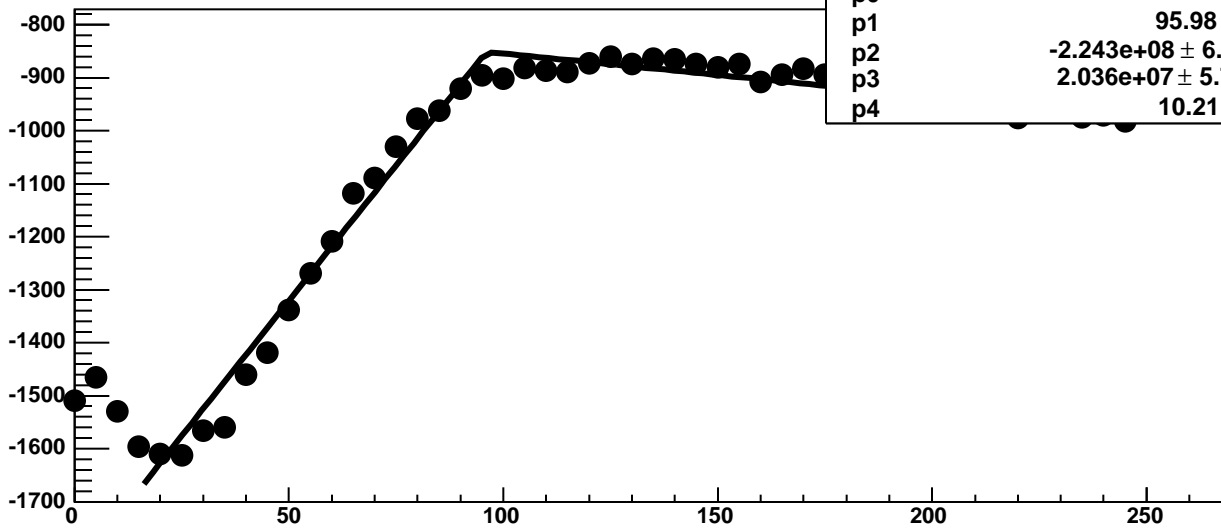
Chip 1, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

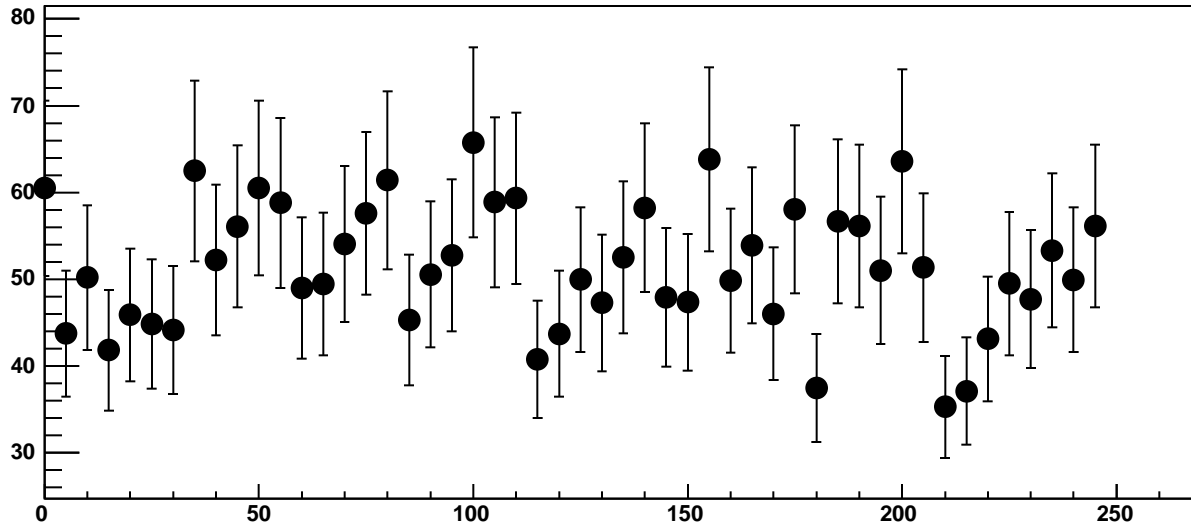


Chip 1, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold

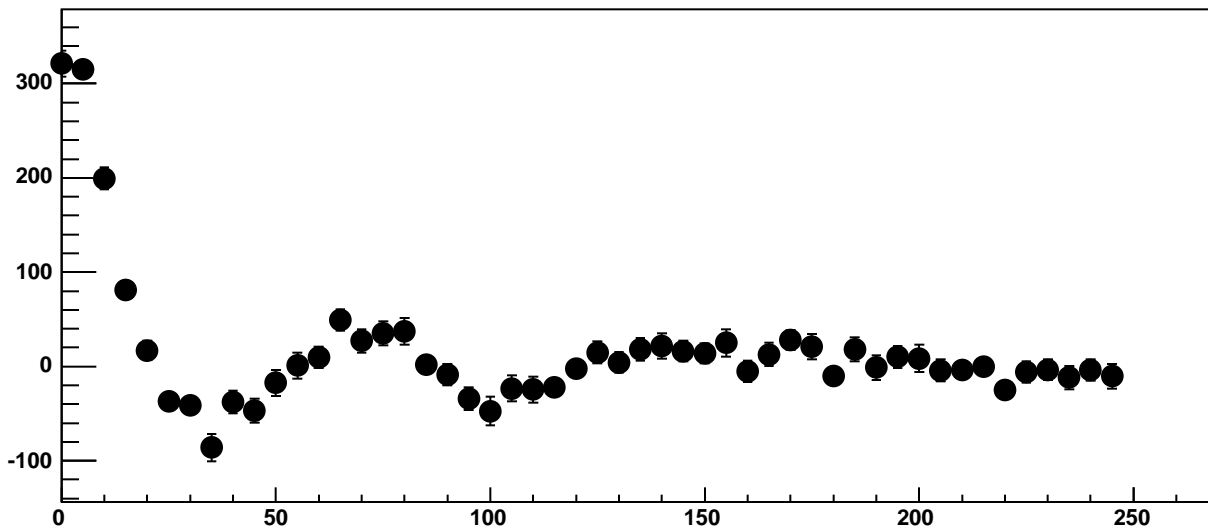


$\chi^2 / \text{ndf}$	270.6 / 41
p0	-851.2 ± 4.129
p1	95.98 ± 0.6442
p2	-2.243e+08 ± 6.781e+06
p3	2.036e+07 ± 5.757e+05
p4	10.21 ± 0.1098

Chip 1, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

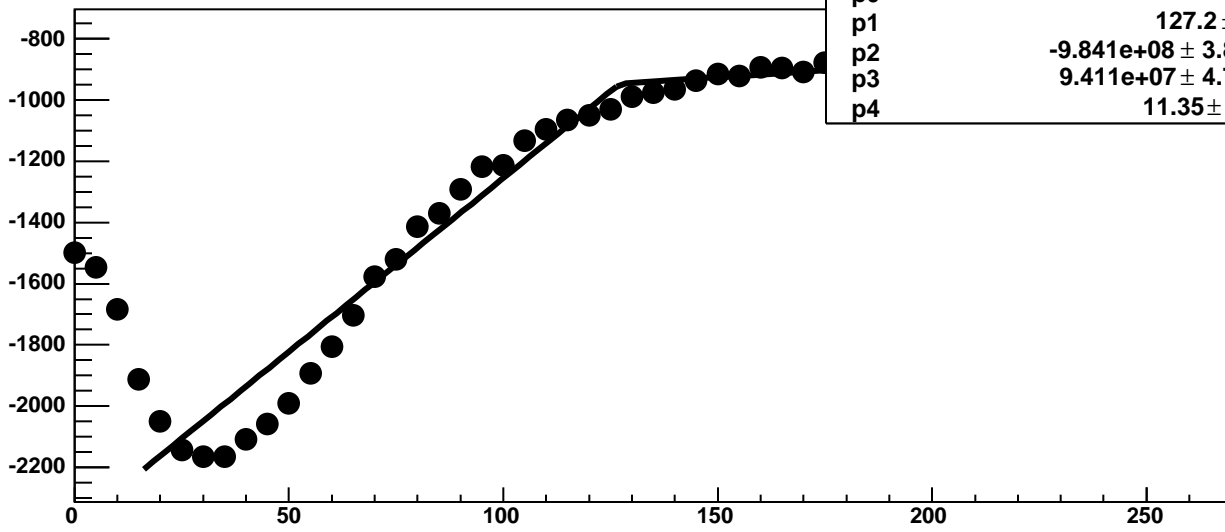


Chip 1, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold

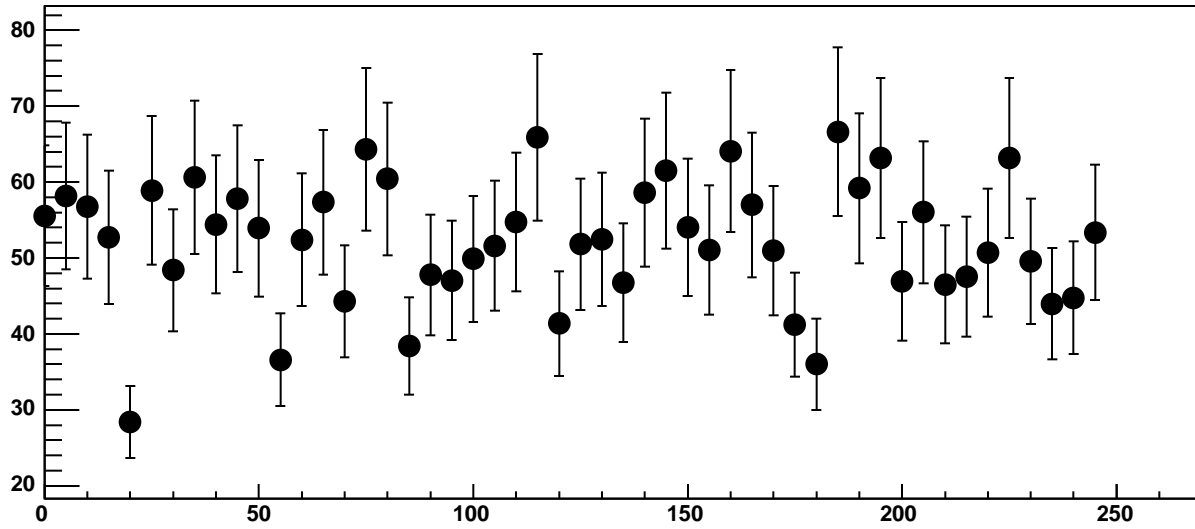




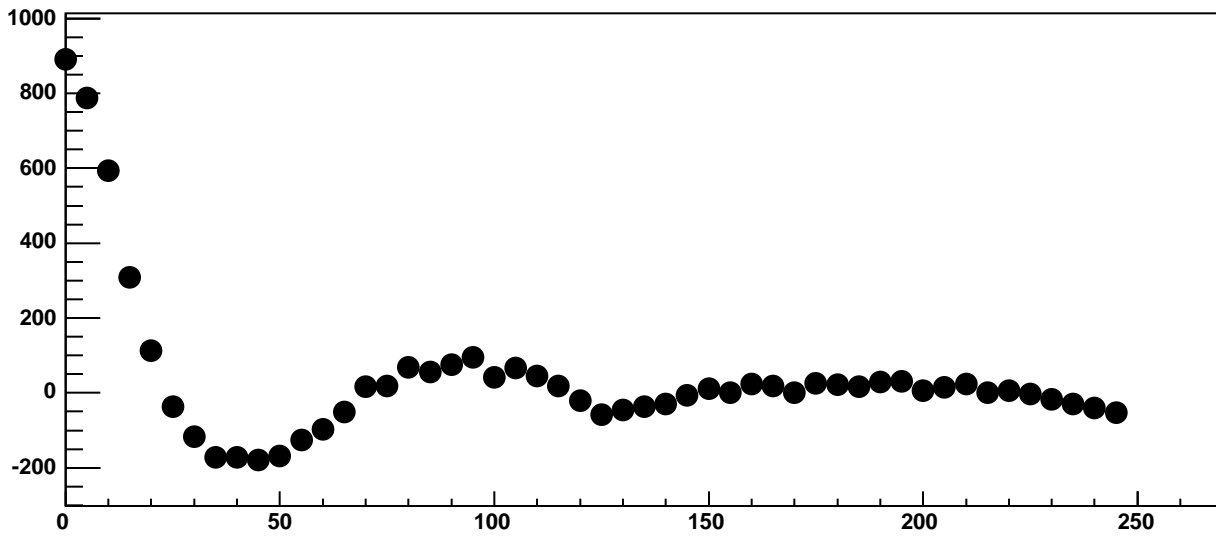
Chip 1, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold



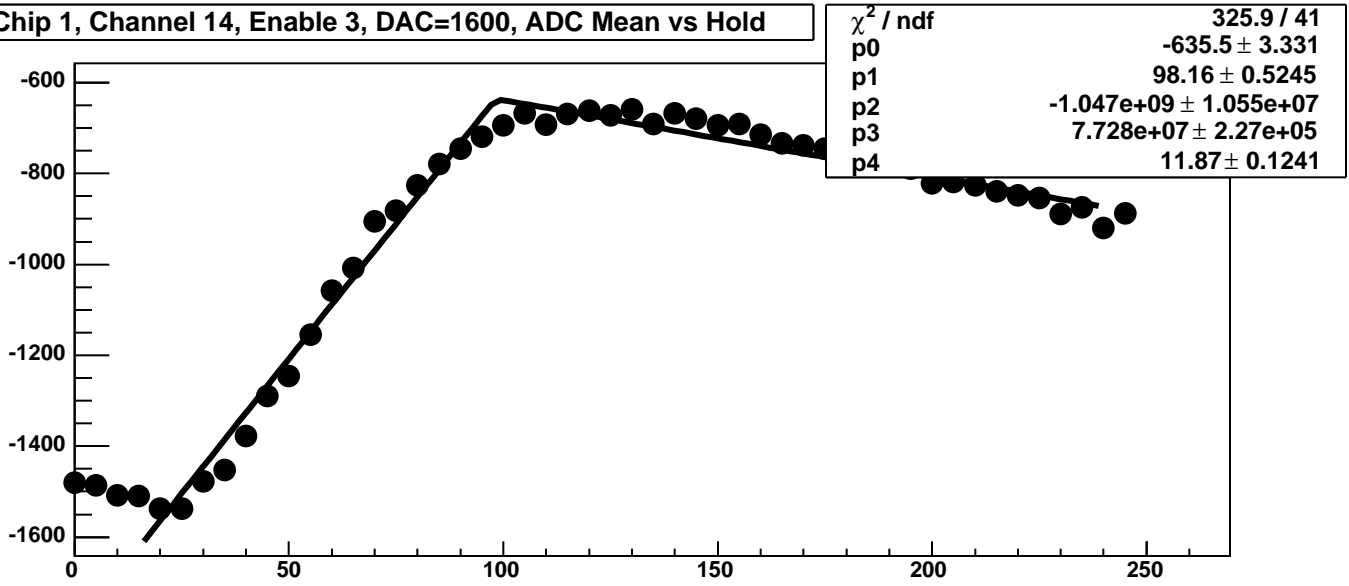
Chip 1, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



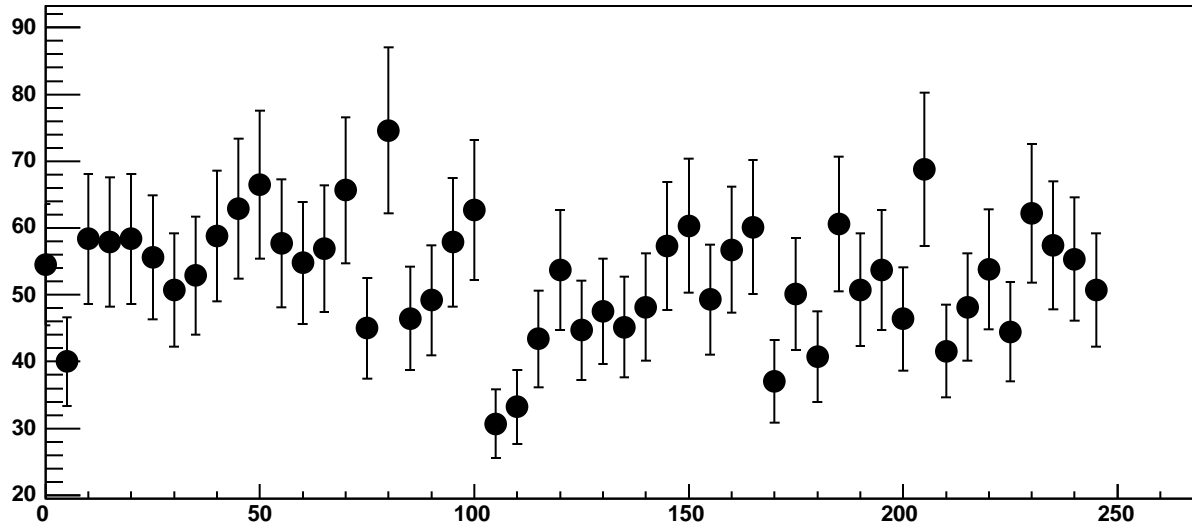
Chip 1, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold



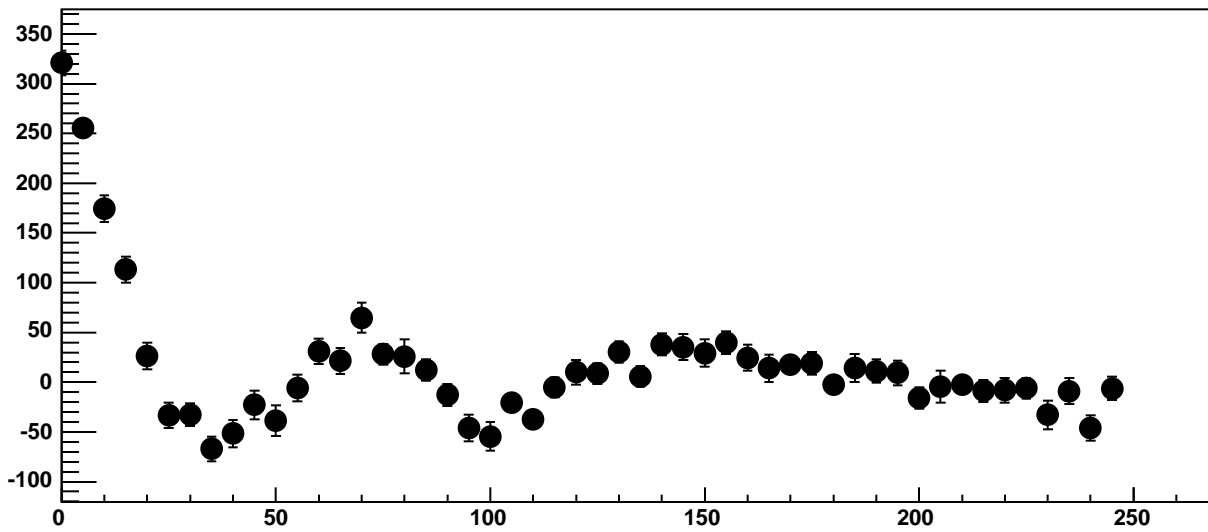
Chip 1, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold



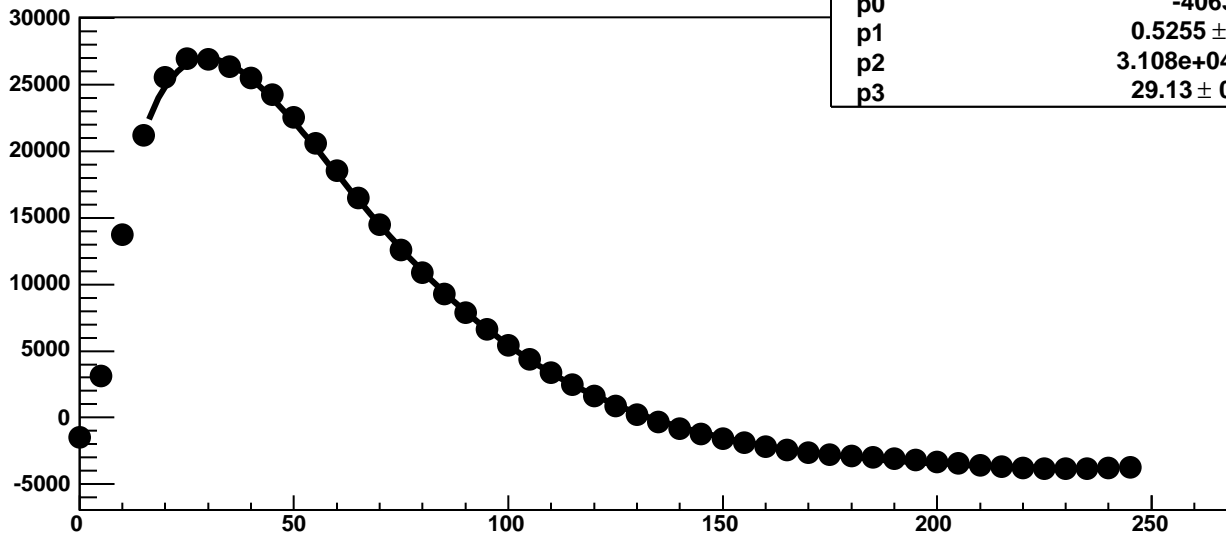
Chip 1, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



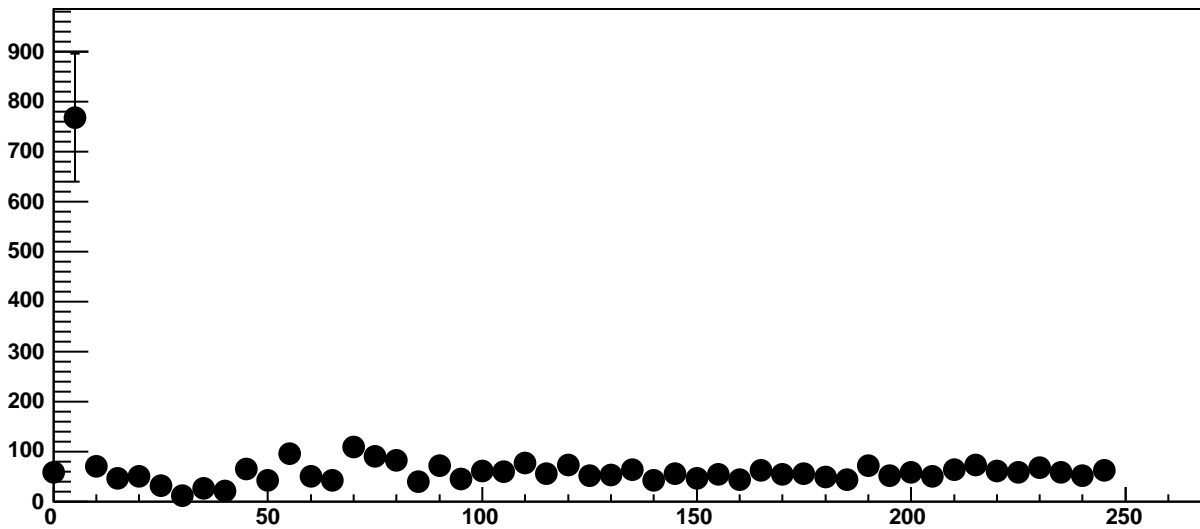
Chip 1, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold



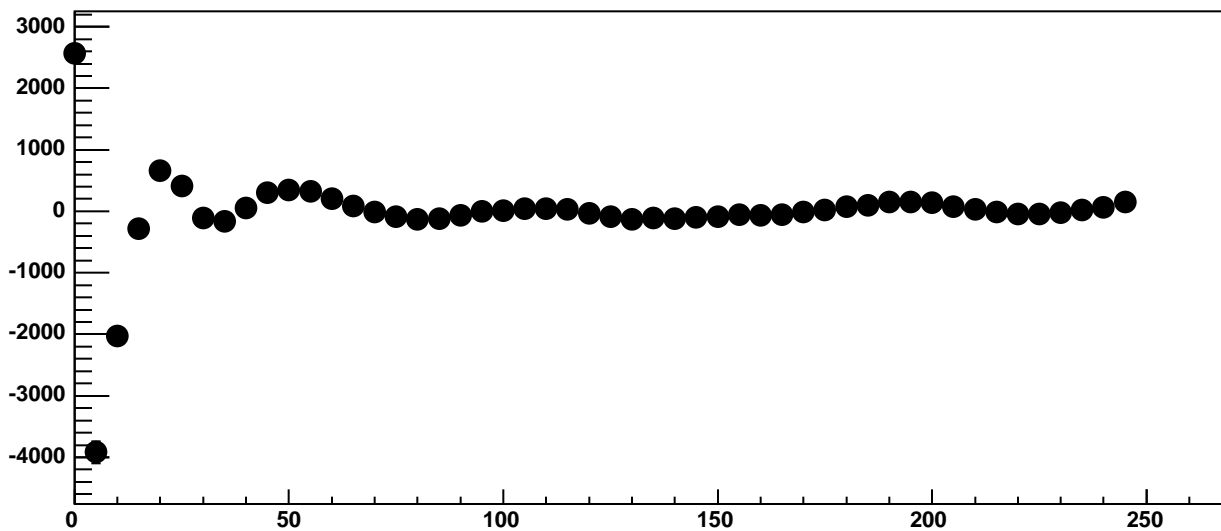
Chip 1, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold



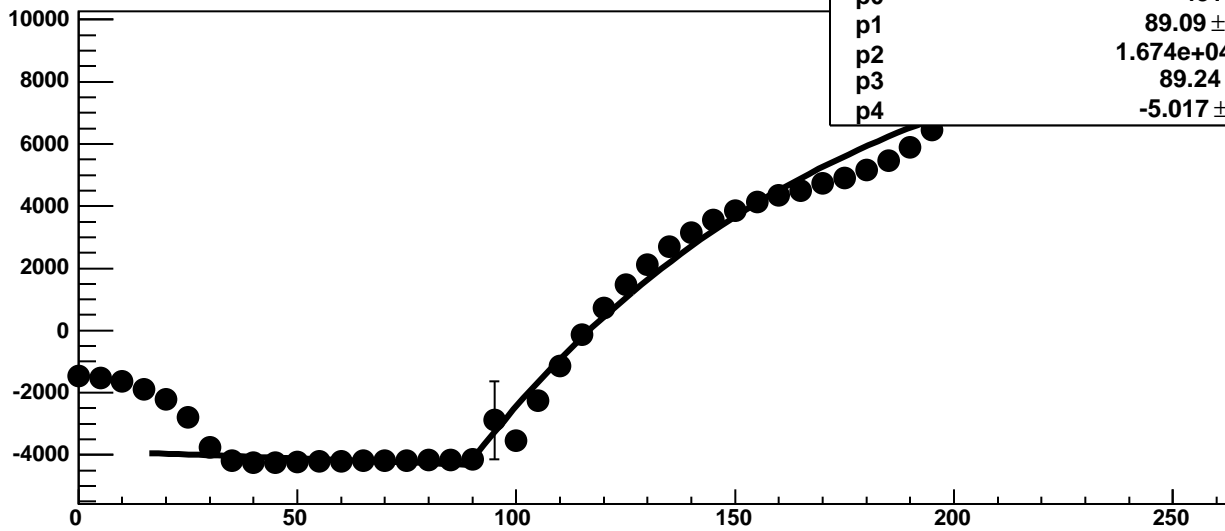
Chip 1, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold

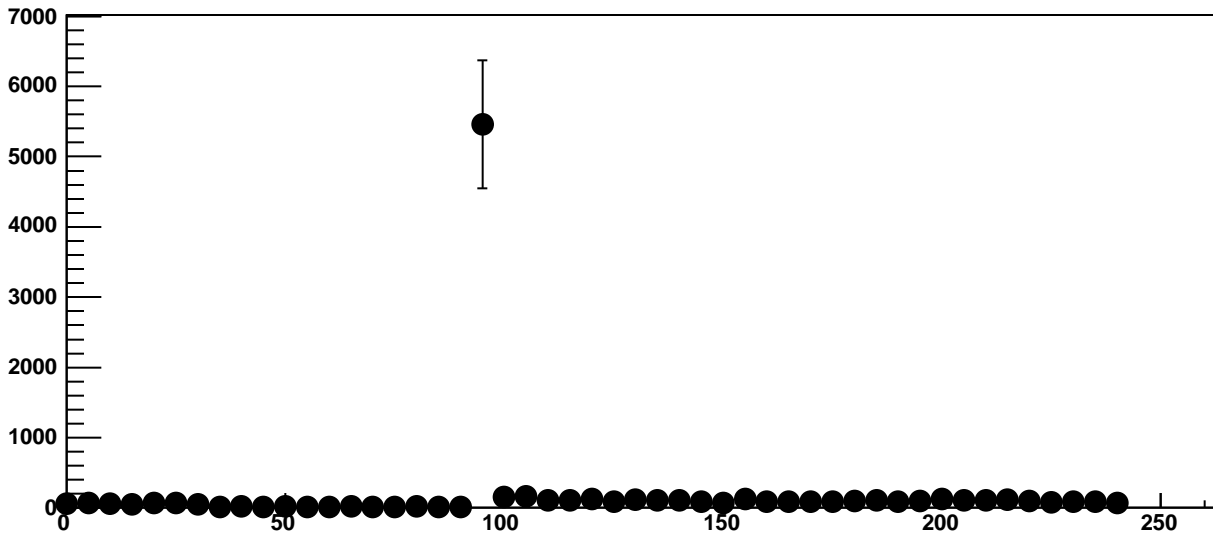


Chip 1, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

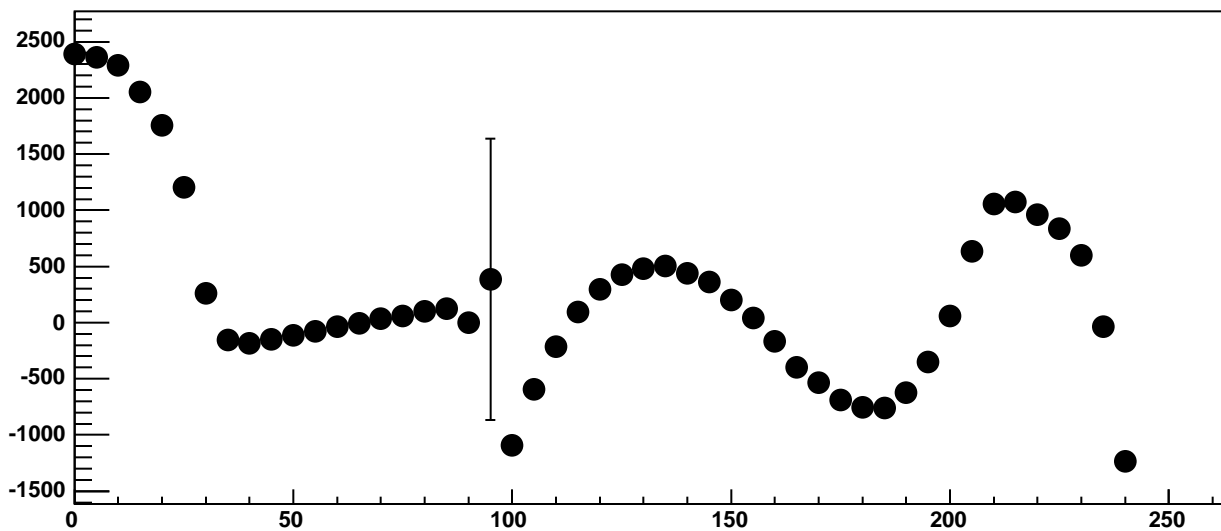


$\chi^2 / \text{ndf}$	7.526e+04 / 41
p0	-4311 ± 2.427
p1	89.09 ± 0.02447
p2	1.674e+04 ± 37.06
p3	89.24 ± 0.3228
p4	-5.017 ± 0.07221

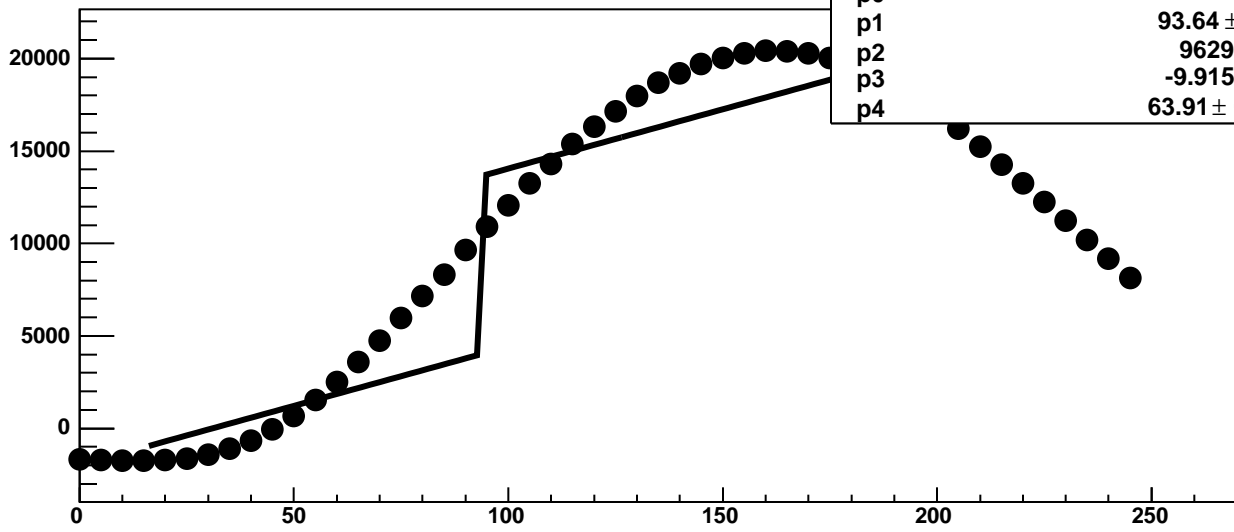
Chip 1, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

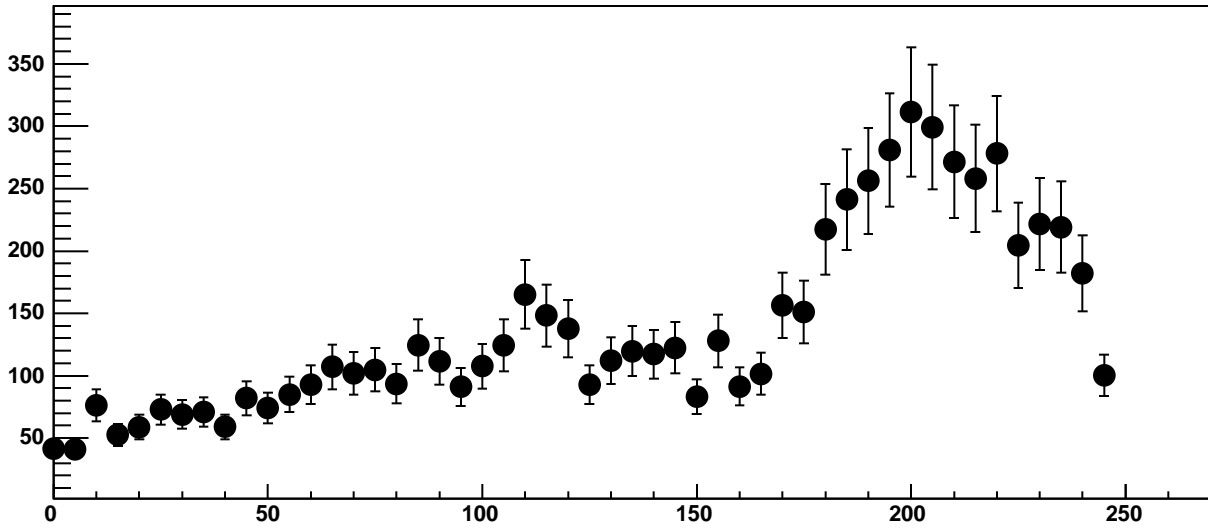


Chip 1, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

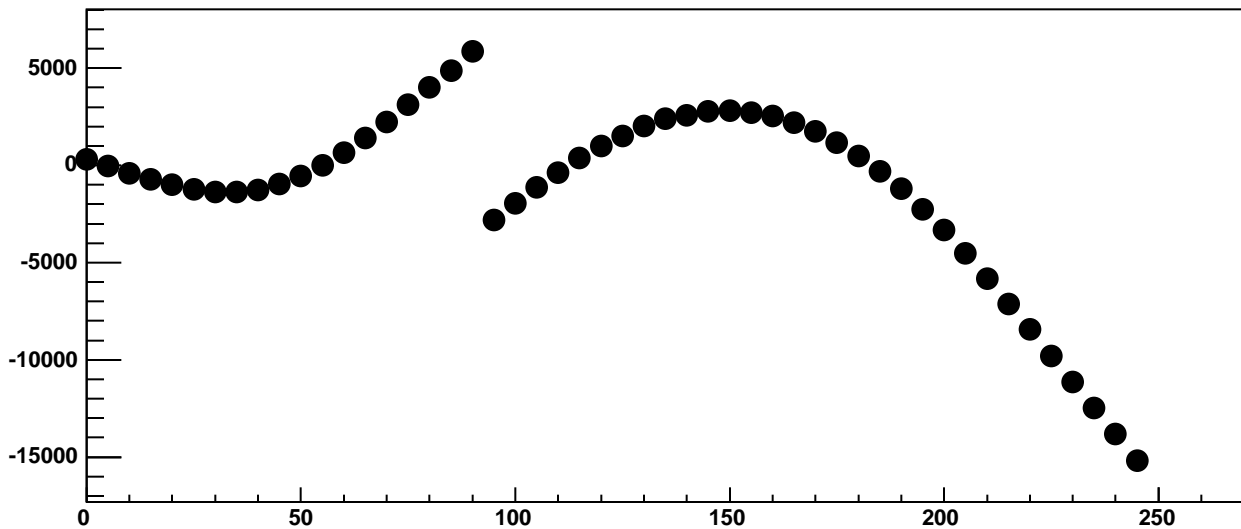


$\chi^2 / \text{ndf}$	6.217e+05 / 41
p0	4012 ± 4.835
p1	93.64 ± 0.5885
p2	9629 ± 4.279
p3	-9.915 ± 0.879
p4	63.91 ± 0.09452

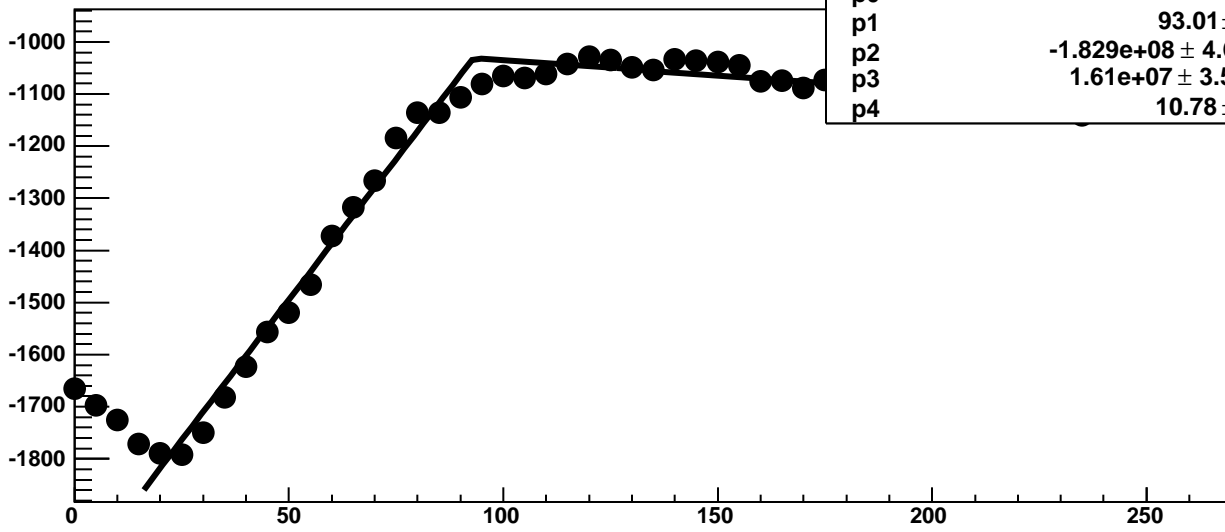
Chip 1, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

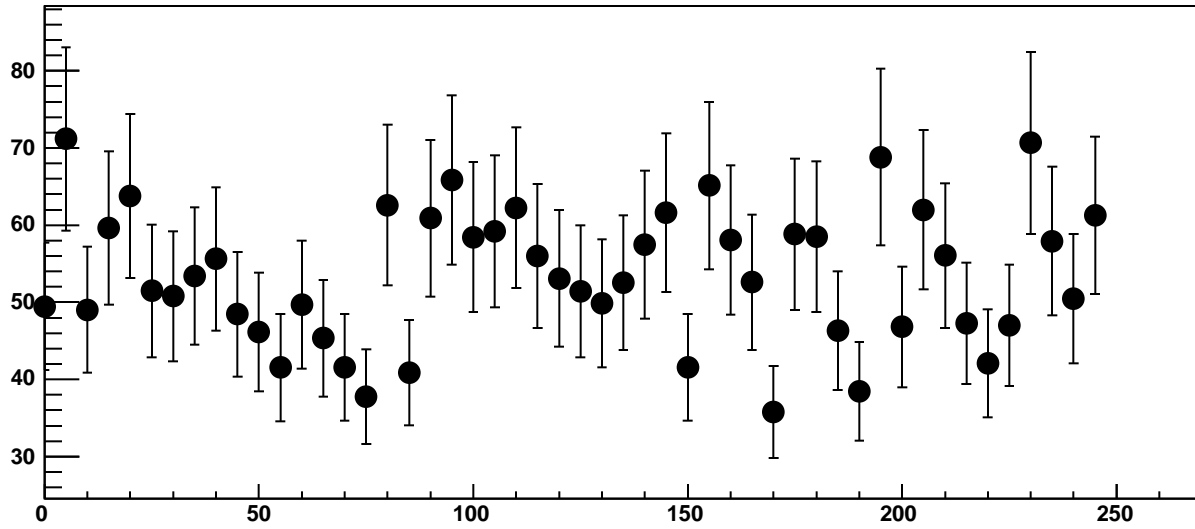


Chip 1, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

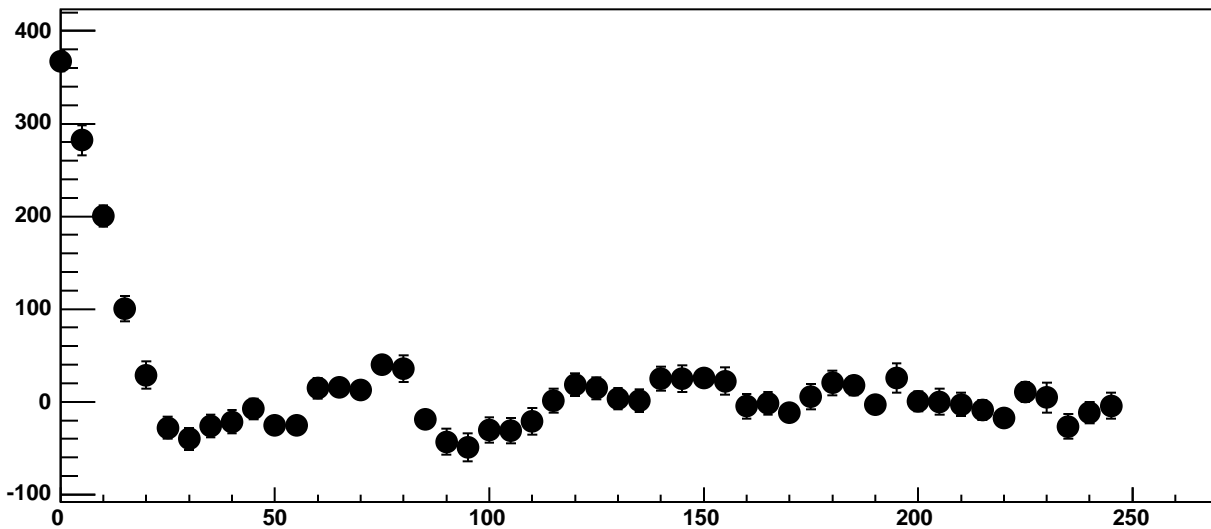


$\chi^2 / \text{ndf}$	207.3 / 41
p0	-1031 ± 4.443
p1	93.01 ± 0.6422
p2	-1.829e+08 ± 4.602e+06
p3	1.61e+07 ± 3.522e+05
p4	10.78 ± 0.1302

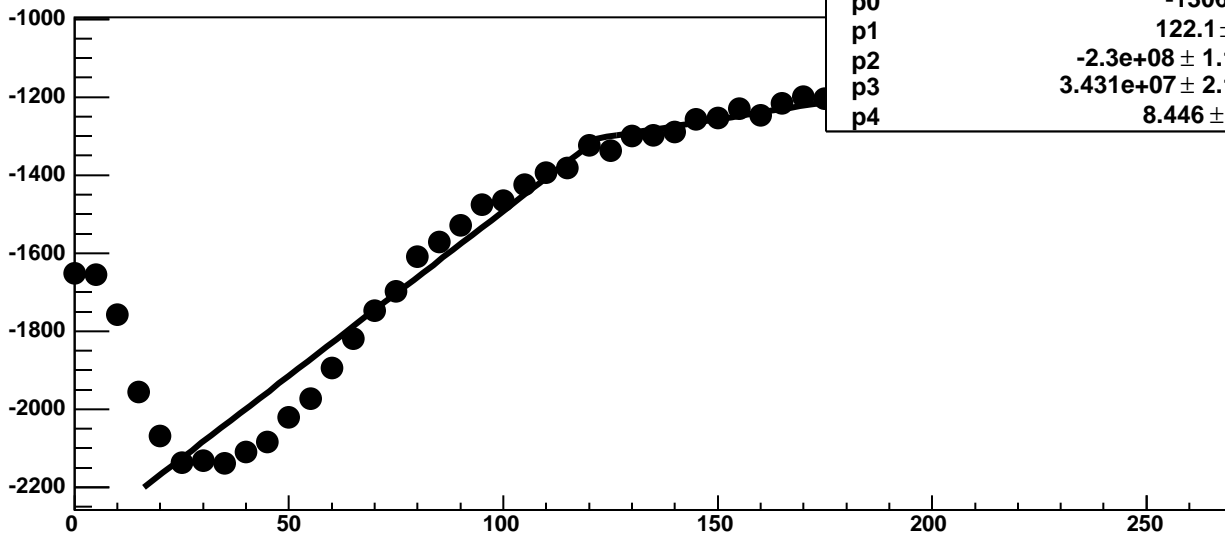
Chip 1, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

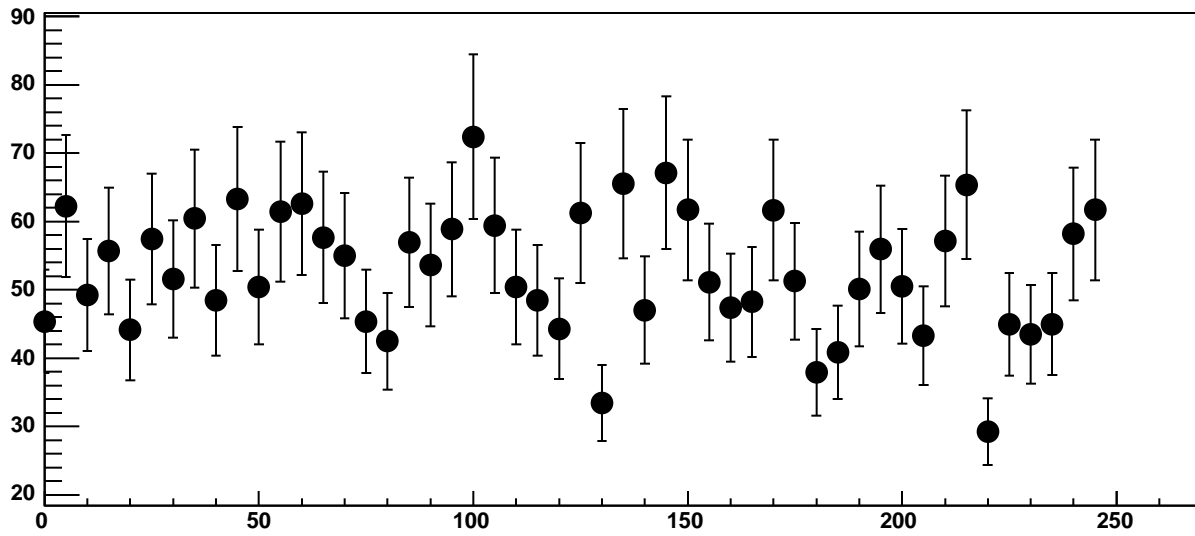


Chip 1, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

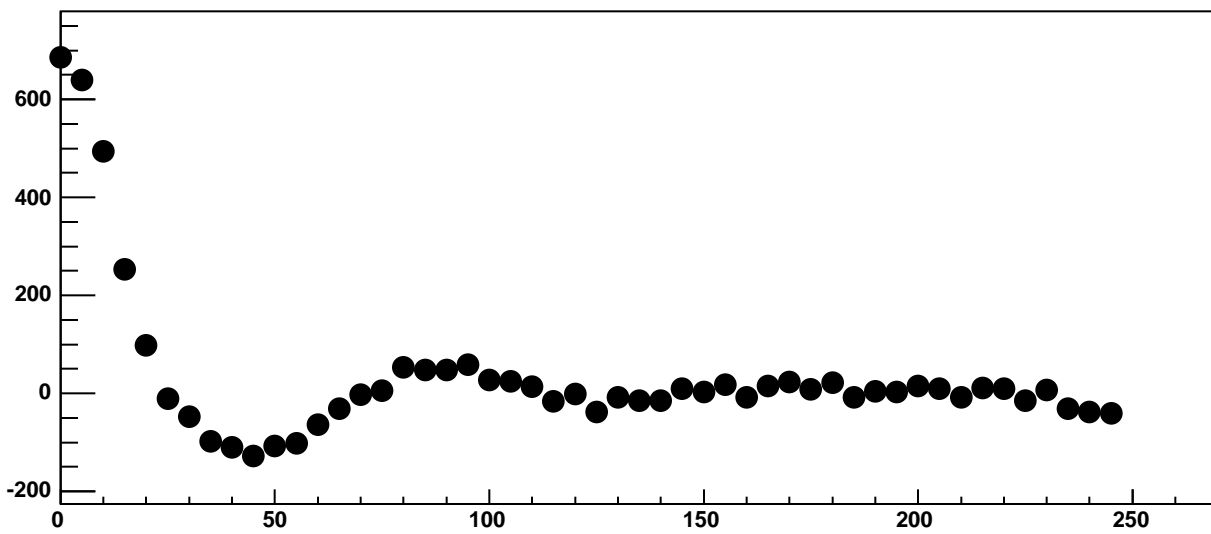


$\chi^2 / \text{ndf}$	1030 / 41
p0	$-1306 \pm 5.193$
p1	$122.1 \pm 0.7734$
p2	$-2.3\text{e}+08 \pm 1.182\text{e}+07$
p3	$3.431\text{e}+07 \pm 2.174\text{e}+06$
p4	$8.446 \pm 0.07941$

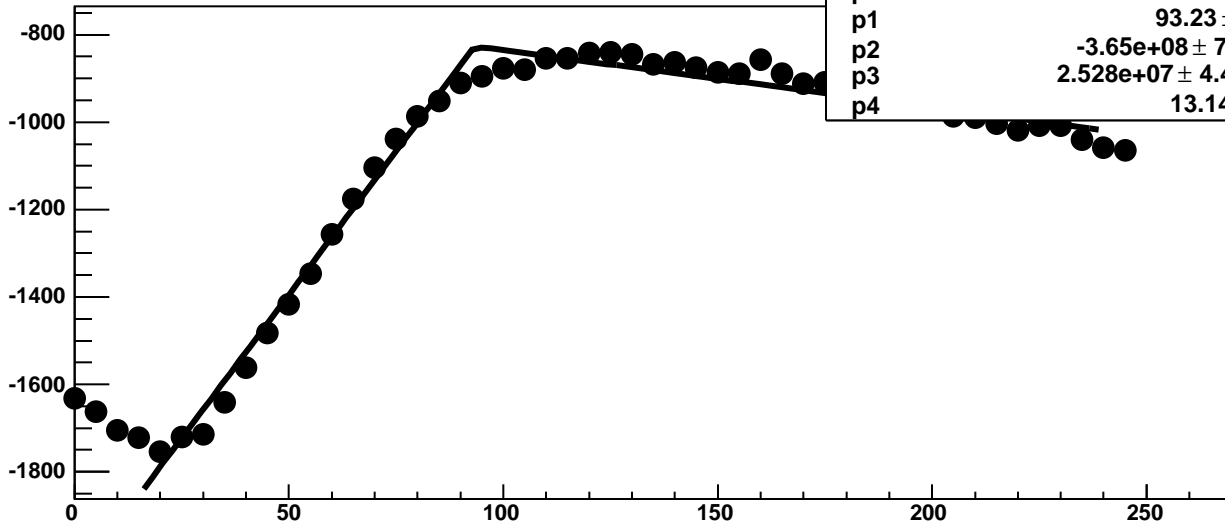
Chip 1, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold

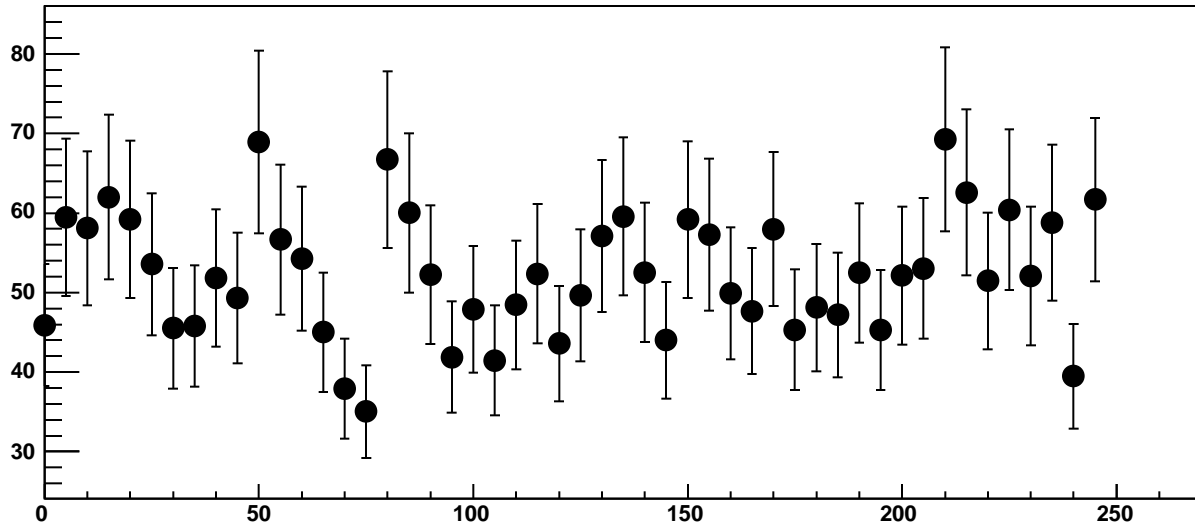


Chip 1, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

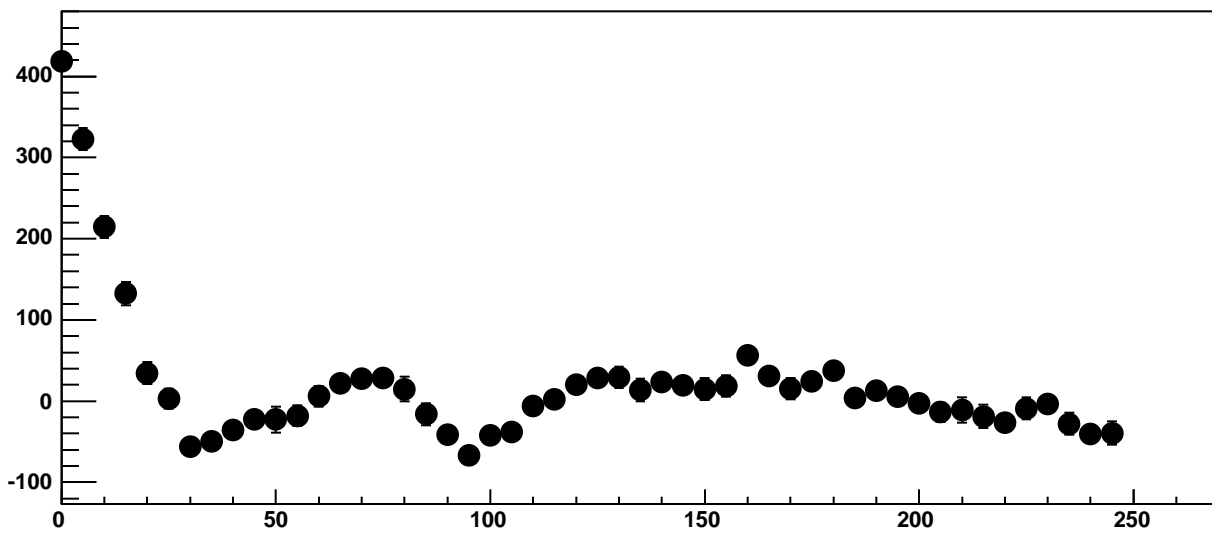


$\chi^2 / \text{ndf}$	395.4 / 41
p0	$-826.8 \pm 3.617$
p1	$93.23 \pm 0.4858$
p2	$-3.65\text{e}+08 \pm 7.77\text{e}+06$
p3	$2.528\text{e}+07 \pm 4.427\text{e}+05$
p4	$13.14 \pm 0.131$

Chip 1, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

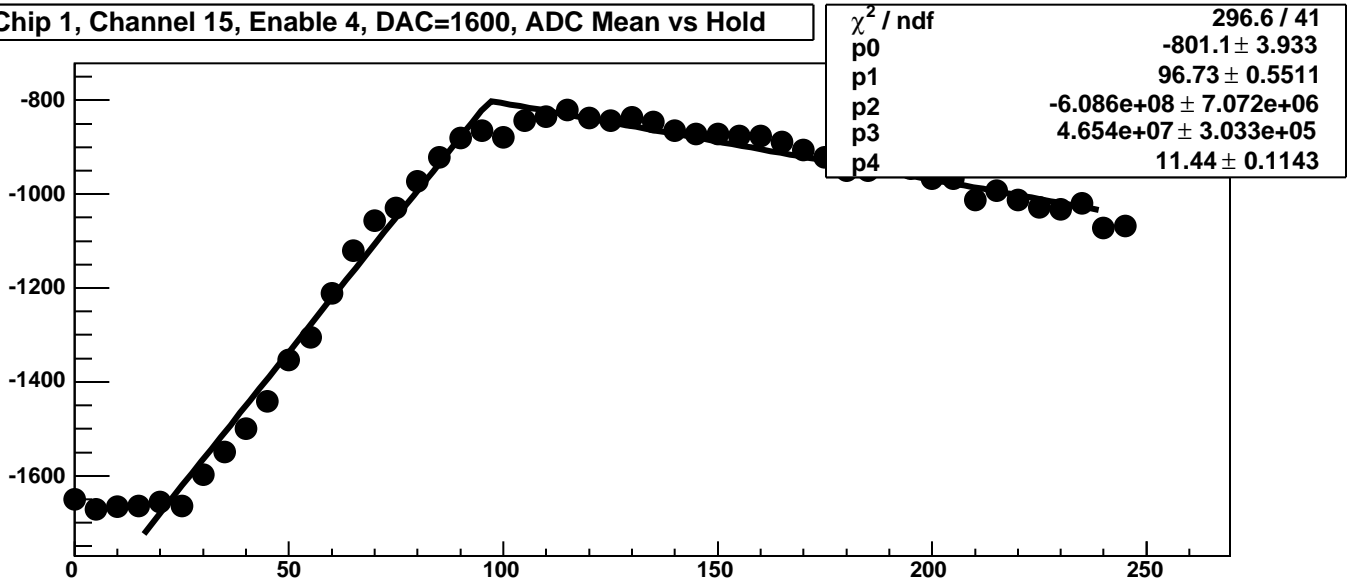


Chip 1, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

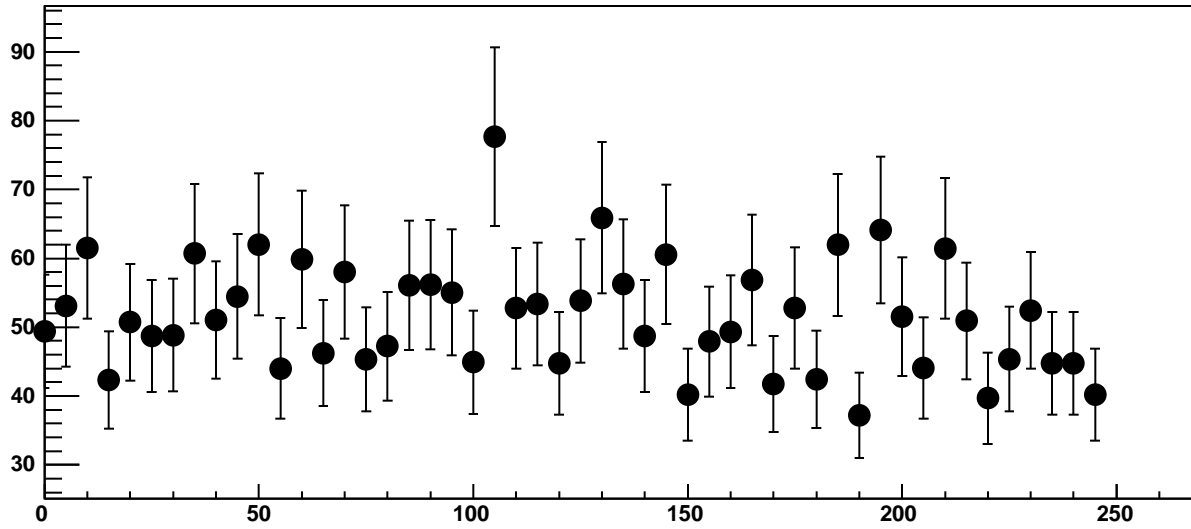




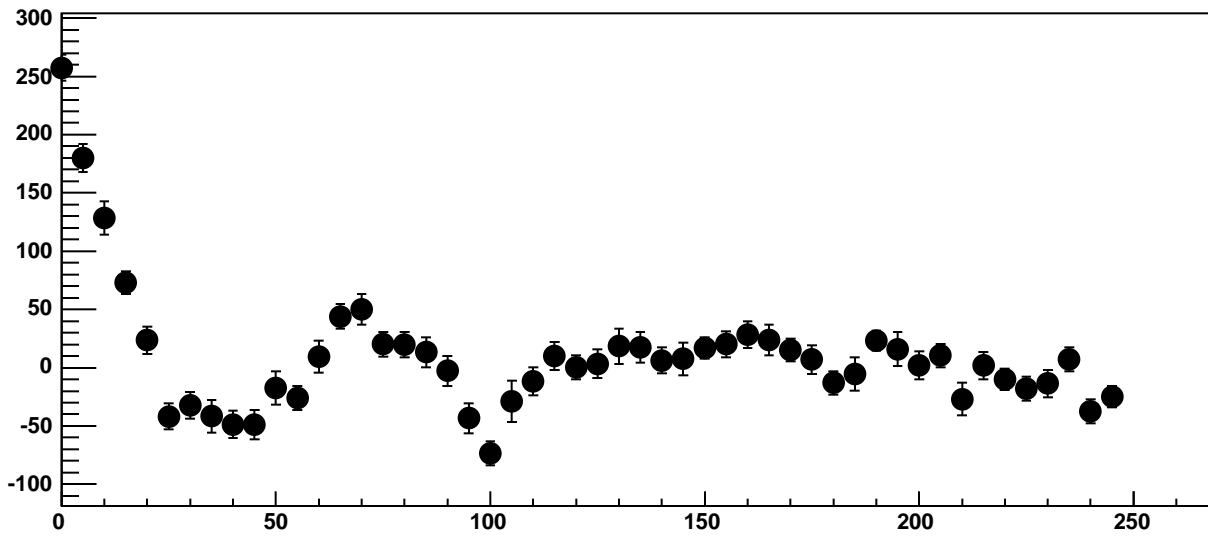
Chip 1, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold



Chip 1, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold

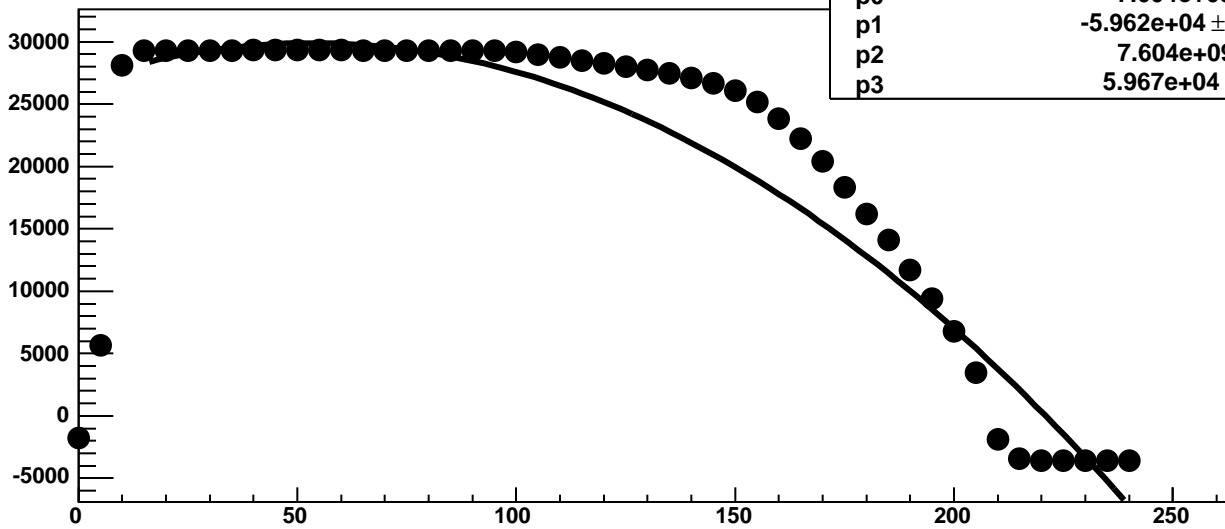


Chip 1, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

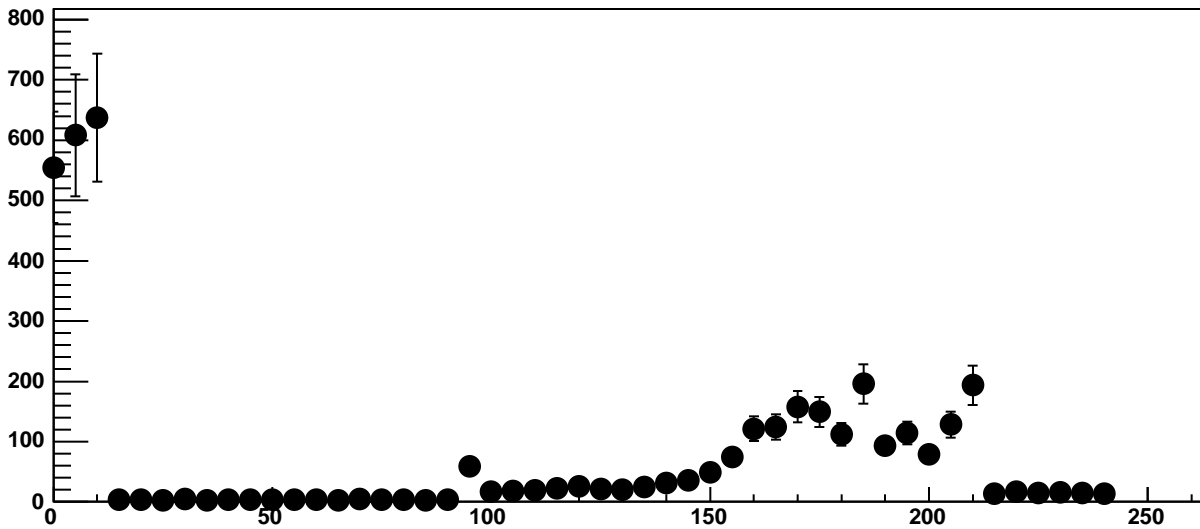


Chip 1, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold

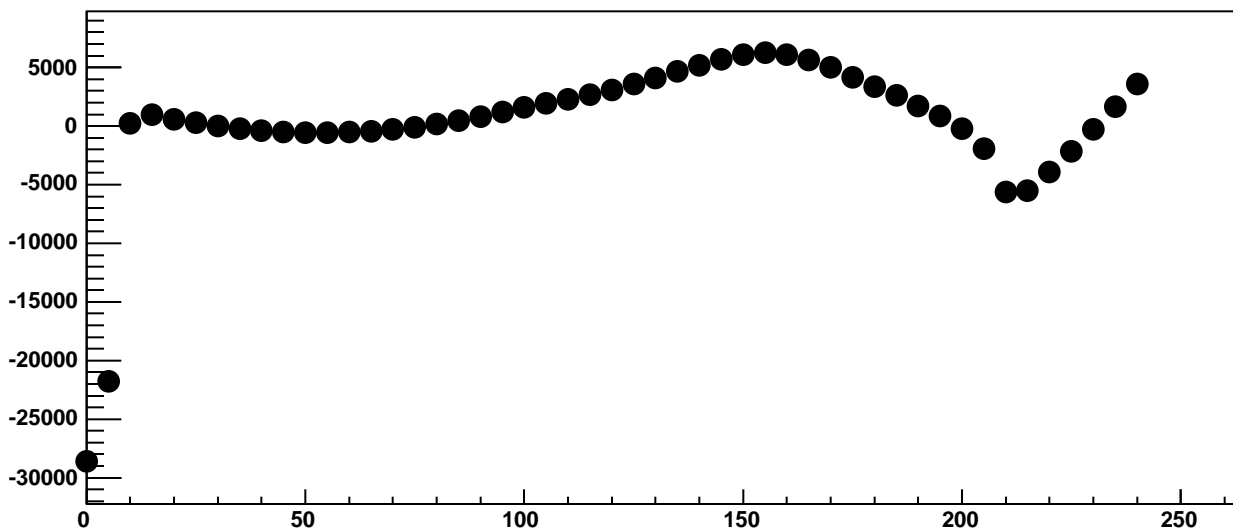
$\chi^2 / \text{ndf}$	1.639e+07 / 42
p0	-7.604e+09 $\pm$ 3.038
p1	-5.962e+04 $\pm$ 0.03786
p2	7.604e+09 $\pm$ 3.038
p3	5.967e+04 $\pm$ 0.0378



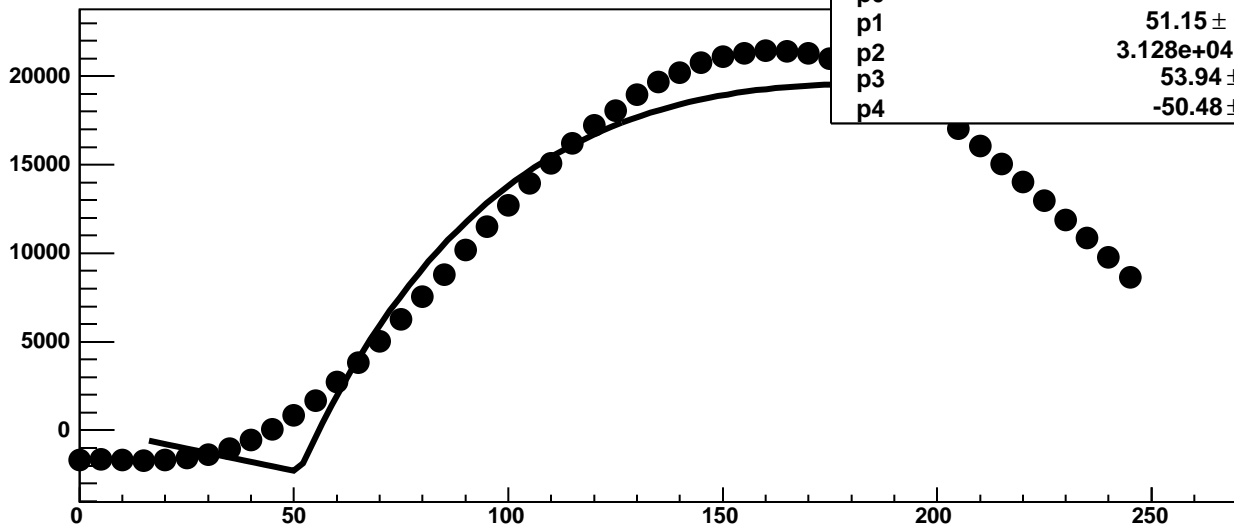
Chip 1, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

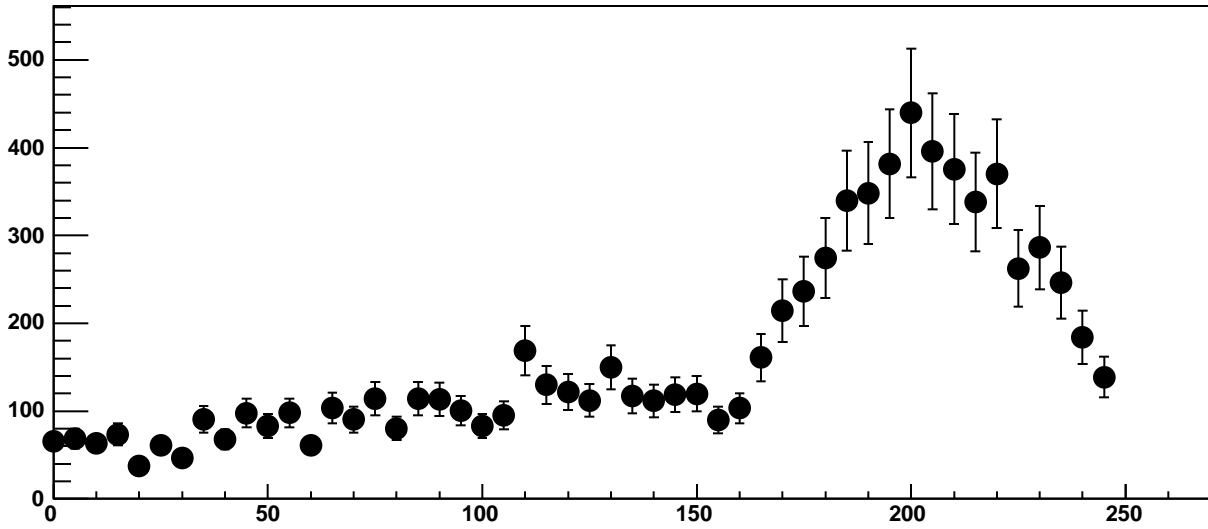


Chip 1, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

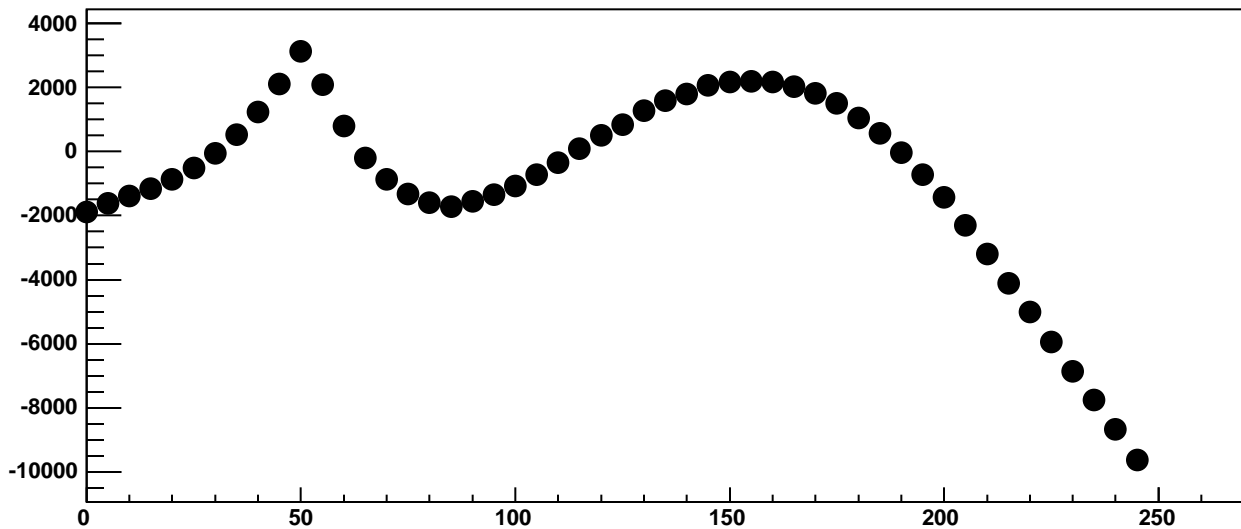


$\chi^2 / \text{ndf}$	2.371e+05 / 41
p0	-2364 ± 8.427
p1	51.15 ± 0.02922
p2	3.128e+04 ± 67.93
p3	53.94 ± 0.1164
p4	-50.48 ± 0.3362

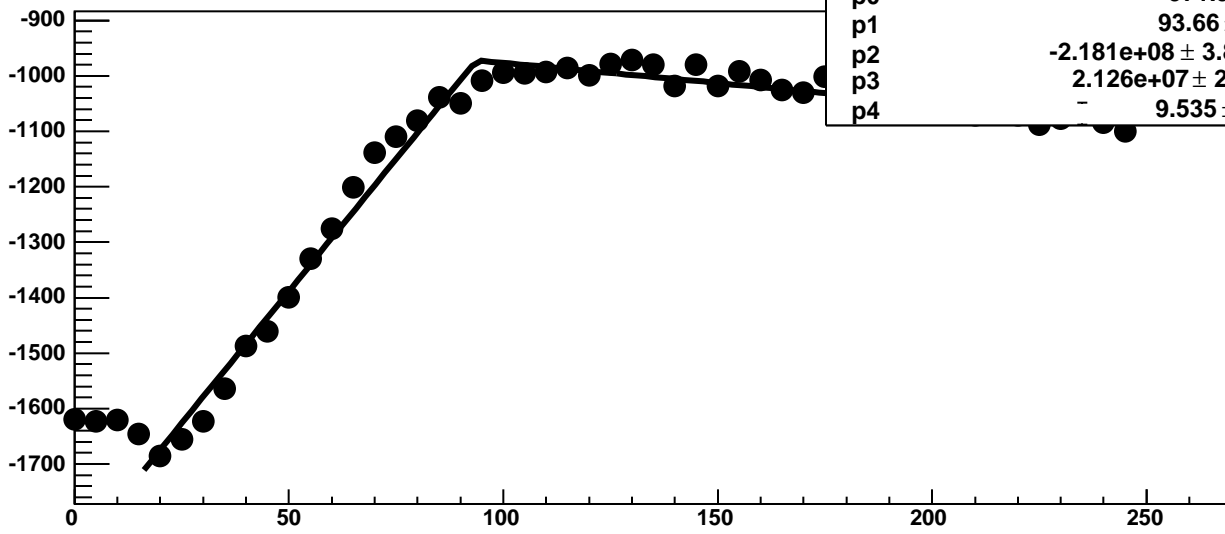
Chip 1, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

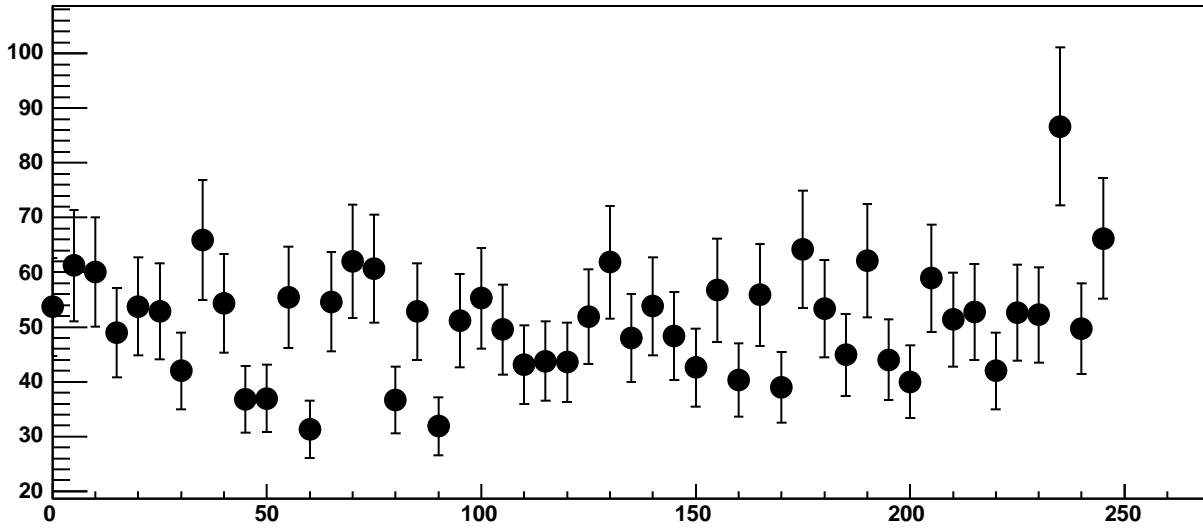


Chip 1, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

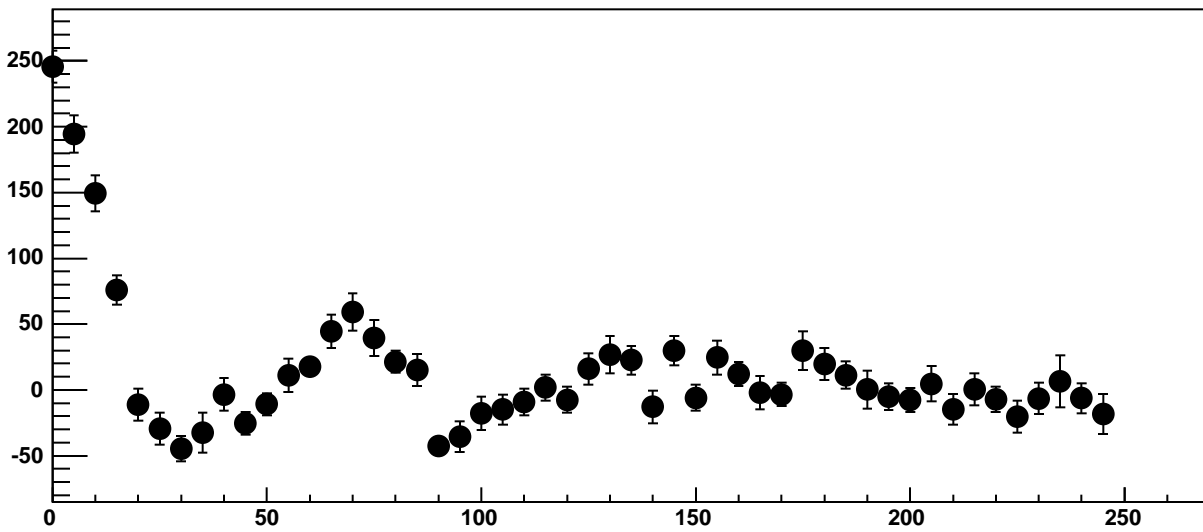


$\chi^2 / \text{ndf}$	228.6 / 41
p0	-971.9 ± 3.823
p1	93.66 ± 0.6241
p2	-2.181e+08 ± 3.894e+06
p3	2.126e+07 ± 2.79e+05
p4	- 9.535 ± 0.1114

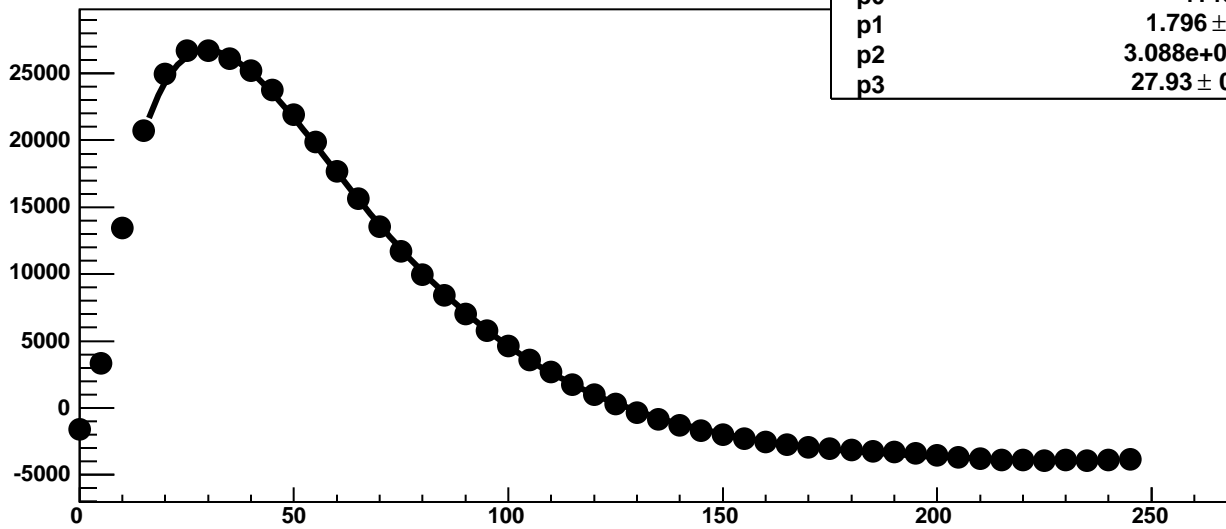
Chip 1, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold

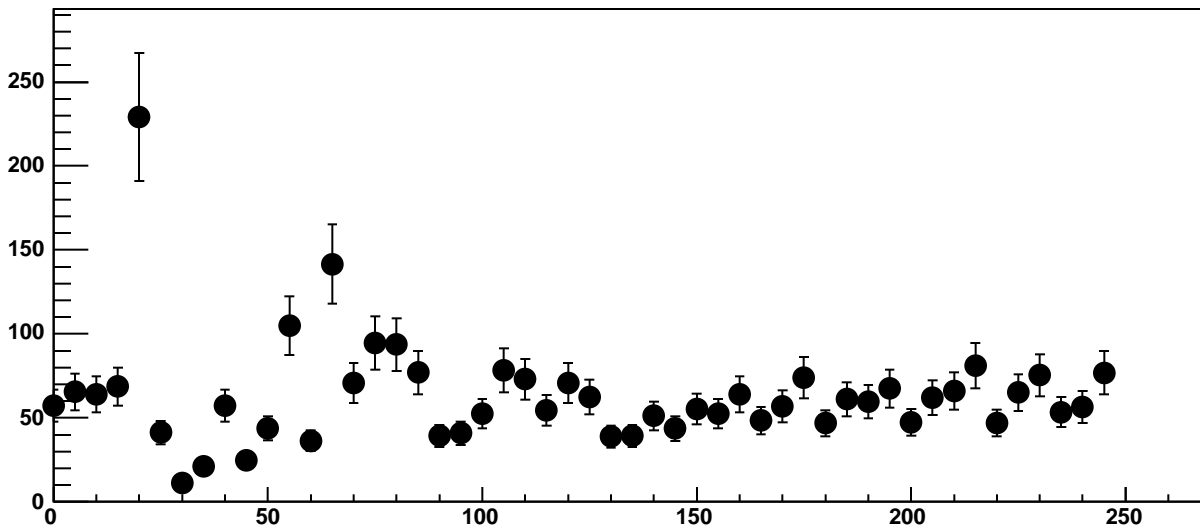


Chip 1, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold

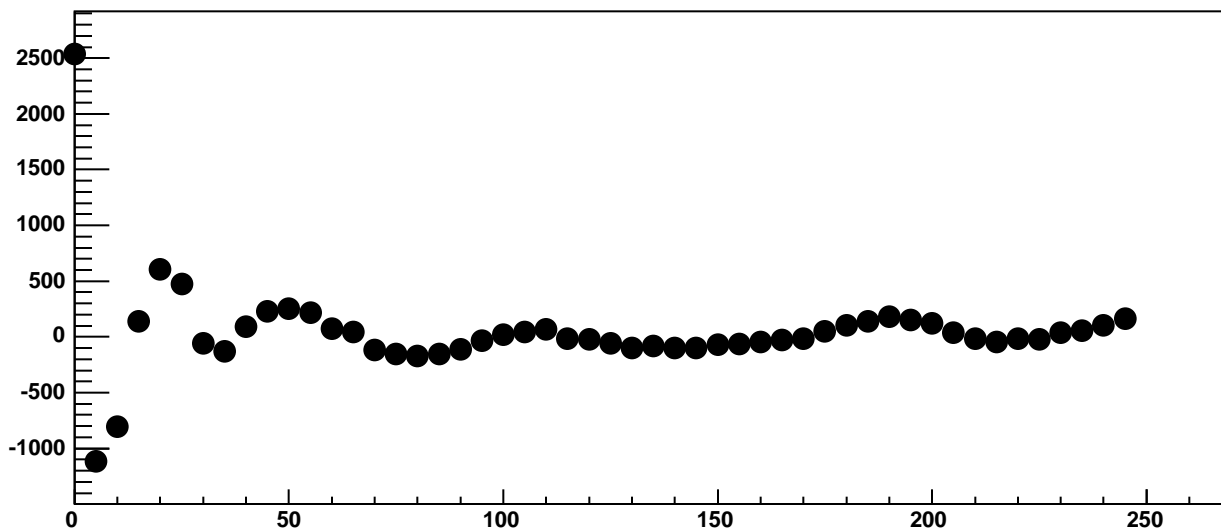


$\chi^2 / \text{ndf}$	8065 / 42
p0	-4140 ± 3.532
p1	1.796 ± 0.01586
p2	3.088e+04 ± 3.92
p3	27.93 ± 0.009308

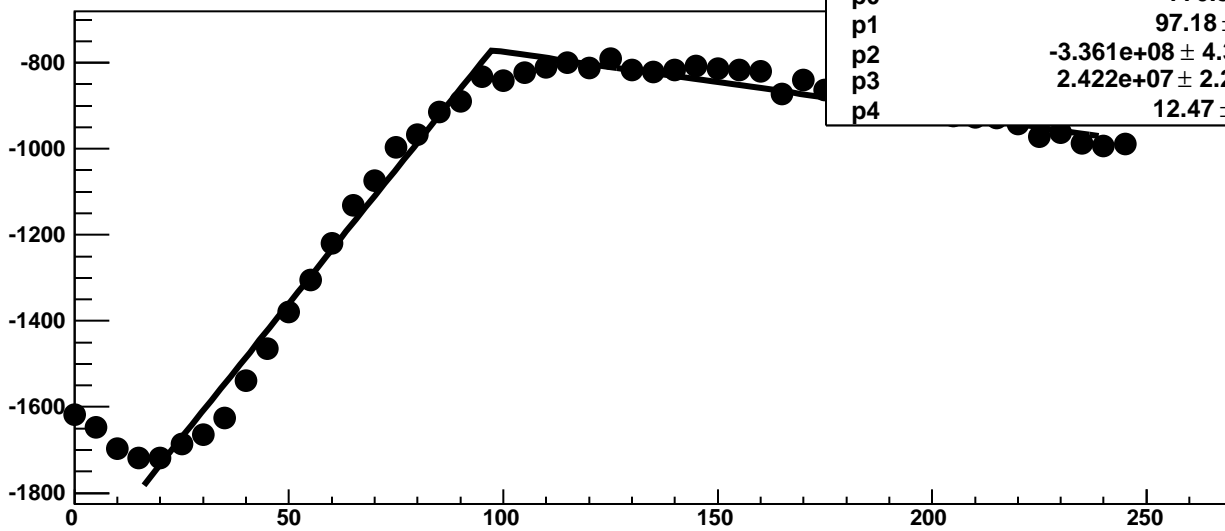
Chip 1, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold

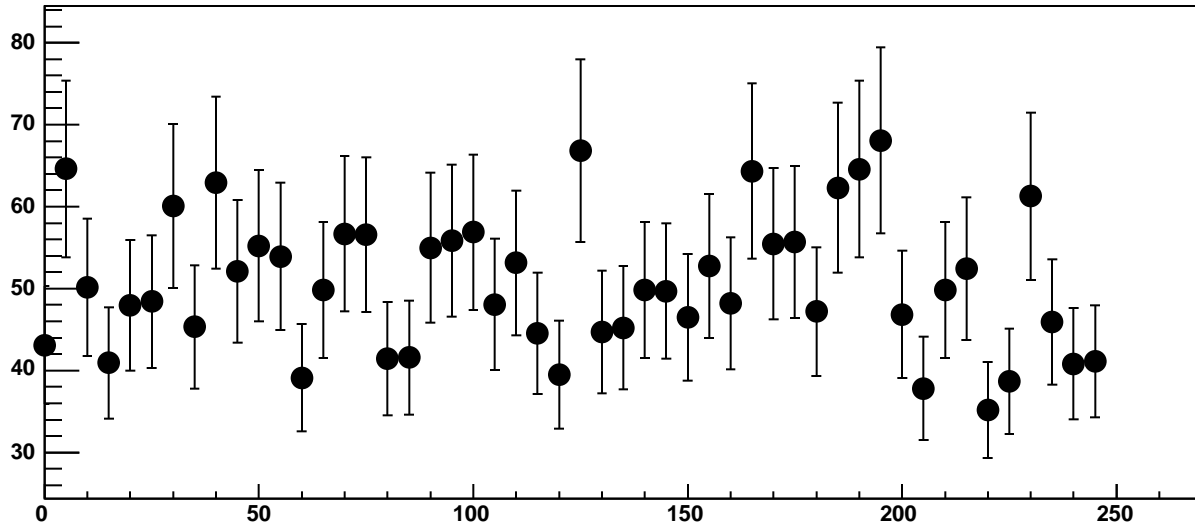


Chip 1, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

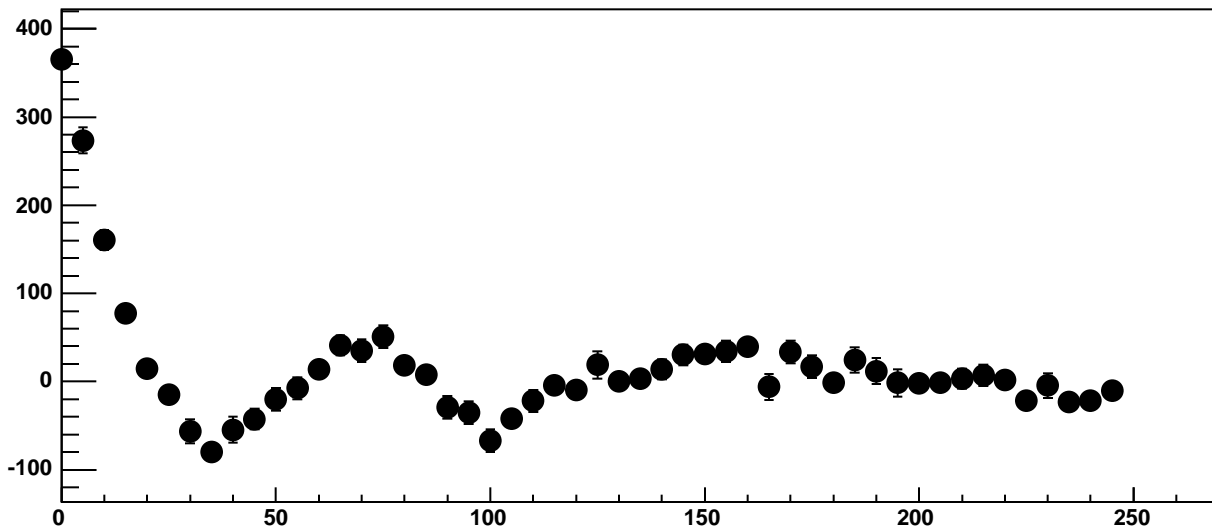


$\chi^2 / \text{ndf}$	345.6 / 41
p0	$-770.8 \pm 3.776$
p1	$97.18 \pm 0.4922$
p2	$-3.361\text{e}+08 \pm 4.308\text{e}+06$
p3	$2.422\text{e}+07 \pm 2.294\text{e}+05$
p4	$12.47 \pm 0.1095$

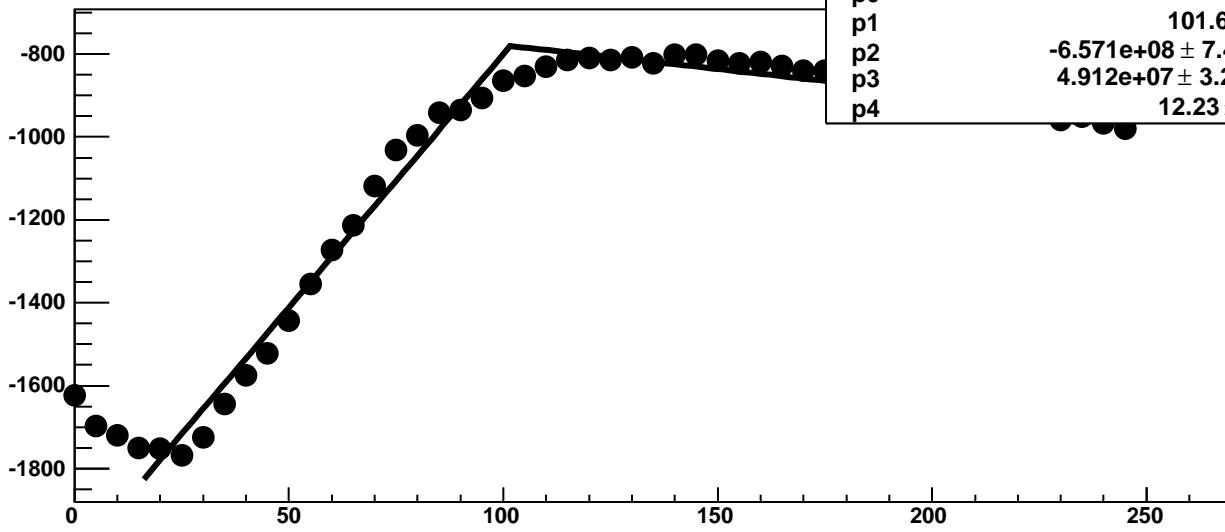
Chip 1, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

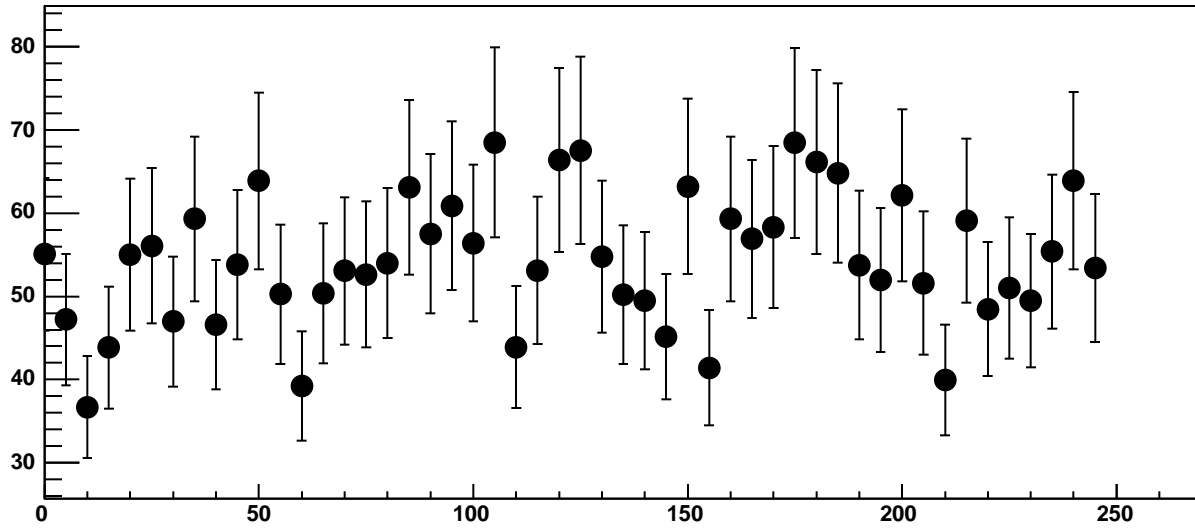


Chip 1, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

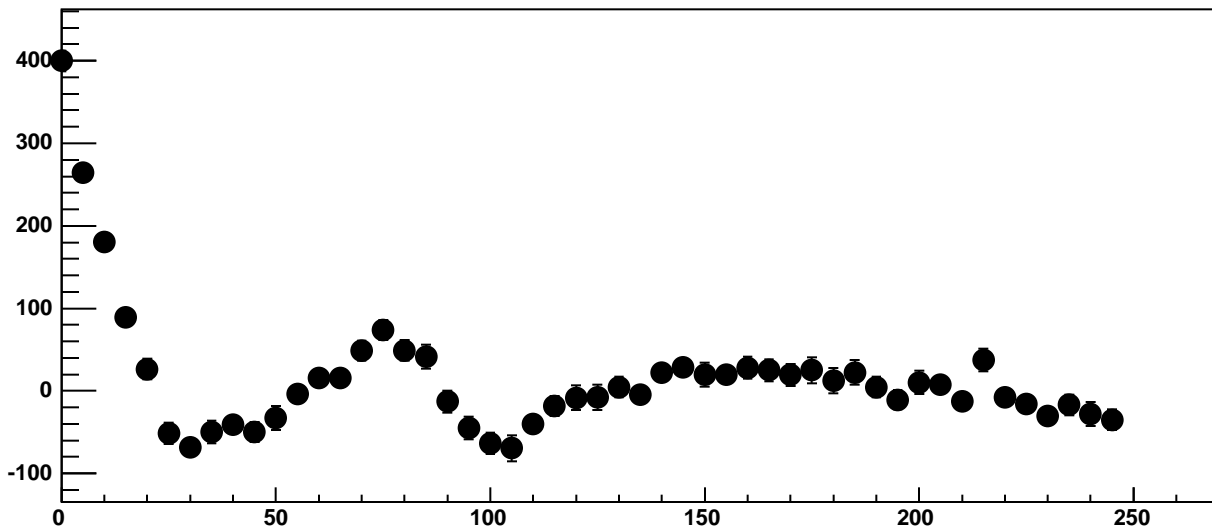


$\chi^2 / \text{ndf}$	404.8 / 41
p0	$-780.5 \pm 4.386$
p1	$101.6 \pm 0.569$
p2	$-6.571\text{e}+08 \pm 7.471\text{e}+06$
p3	$4.912\text{e}+07 \pm 3.246\text{e}+05$
p4	$12.23 \pm 0.1118$

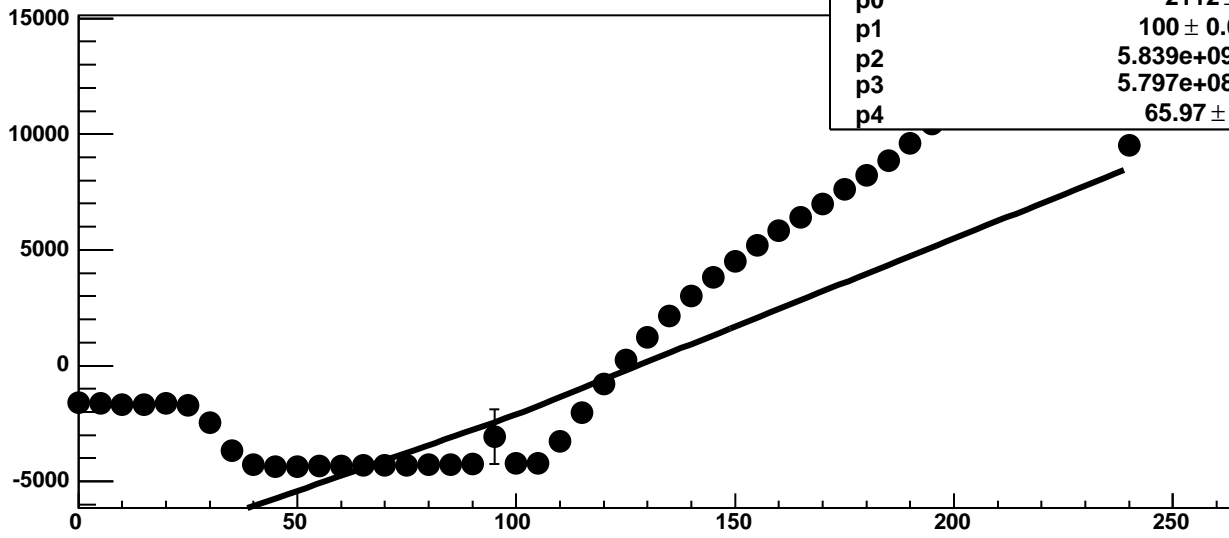
Chip 1, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

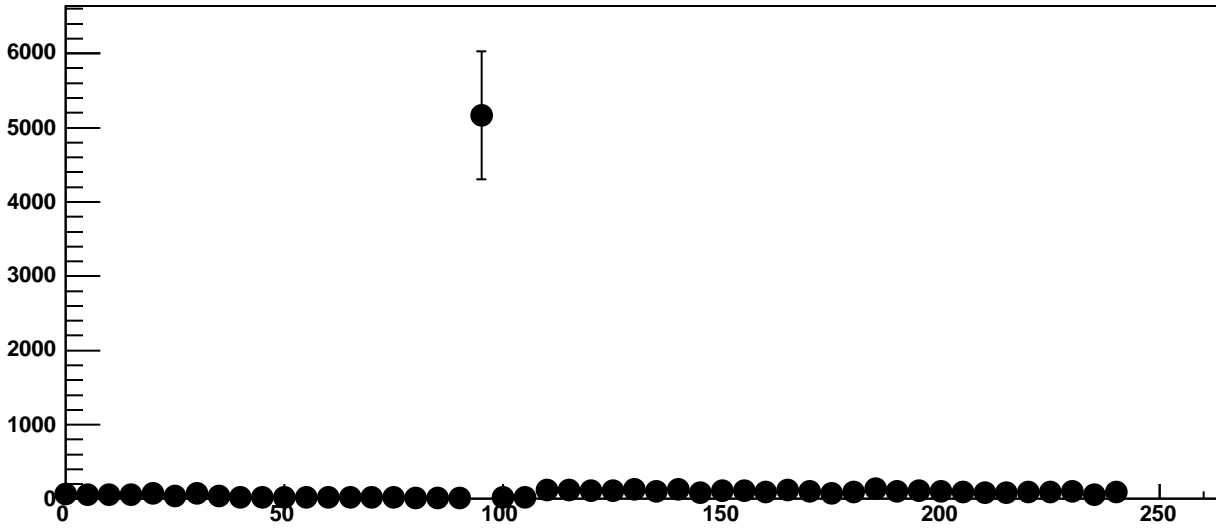


Chip 1, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold

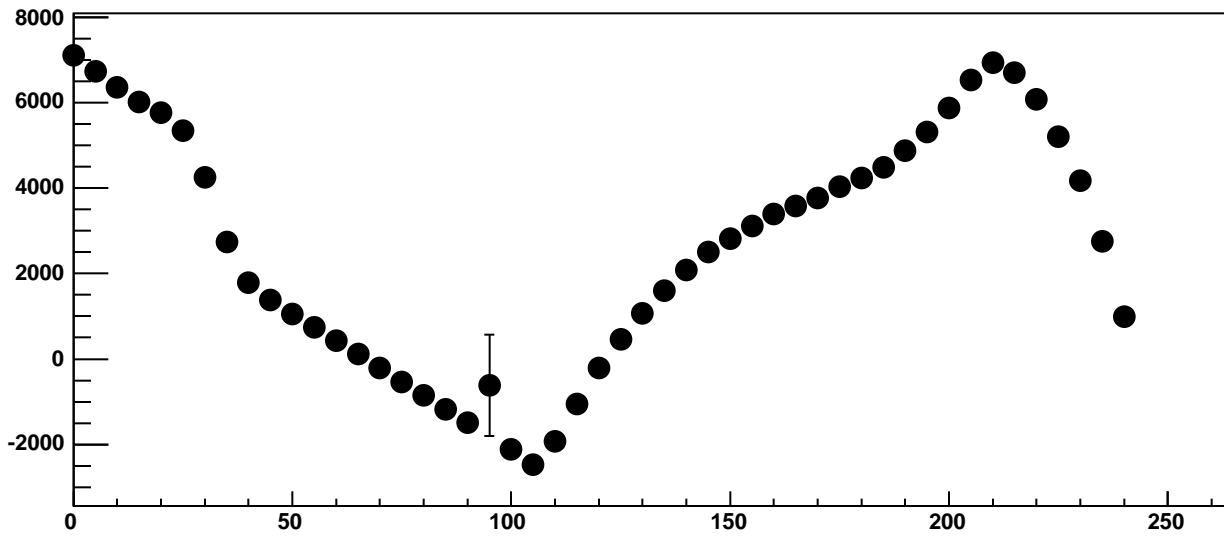


$\chi^2 / \text{ndf}$	2.816e+06 / 41
p0	-2112 ± 0.9664
p1	100 ± 0.0007223
p2	5.839e+09 ± 1.414
p3	5.797e+08 ± 1.414
p4	65.97 ± 0.03067

Chip 1, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold

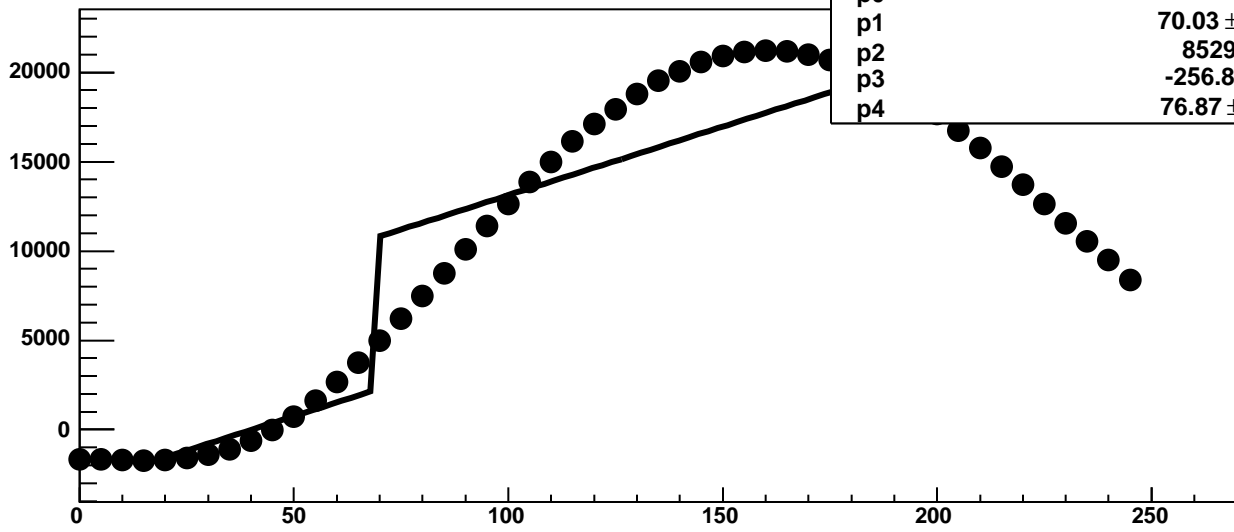


Chip 1, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold



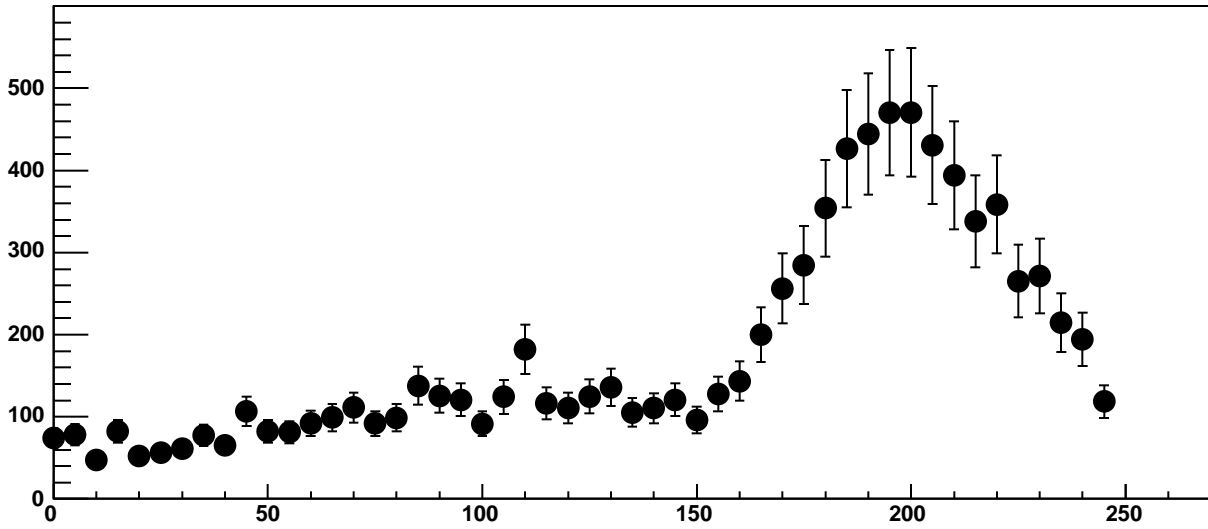


Chip 1, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

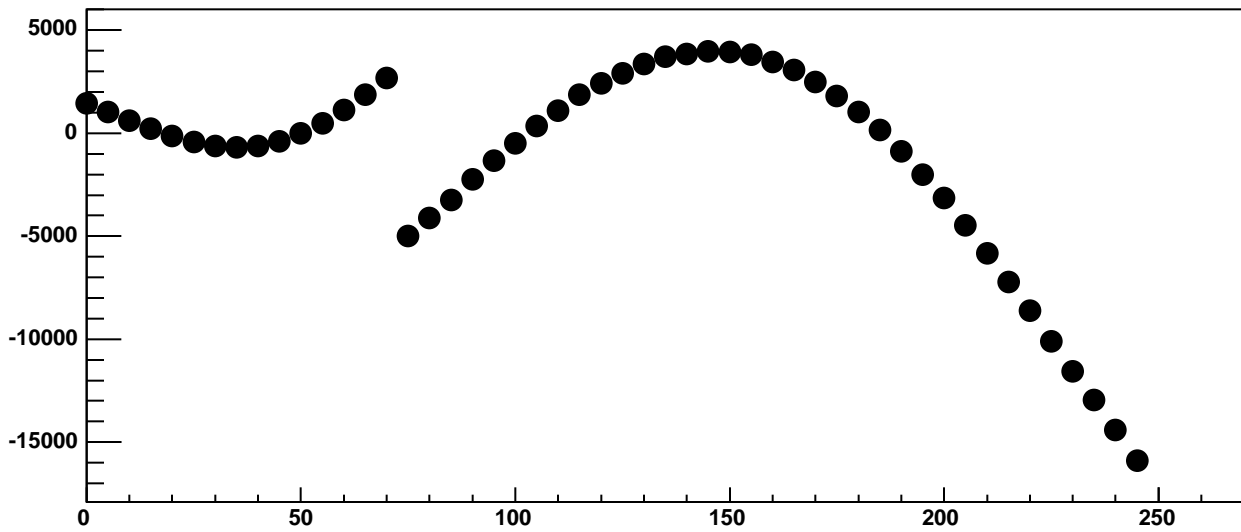


$\chi^2 / \text{ndf}$	5.7e+05 / 41
p0	2292 ± 14.89
p1	70.03 ± 0.3385
p2	8529 ± 38.81
p3	-256.8 ± 8.382
p4	76.87 ± 0.5803

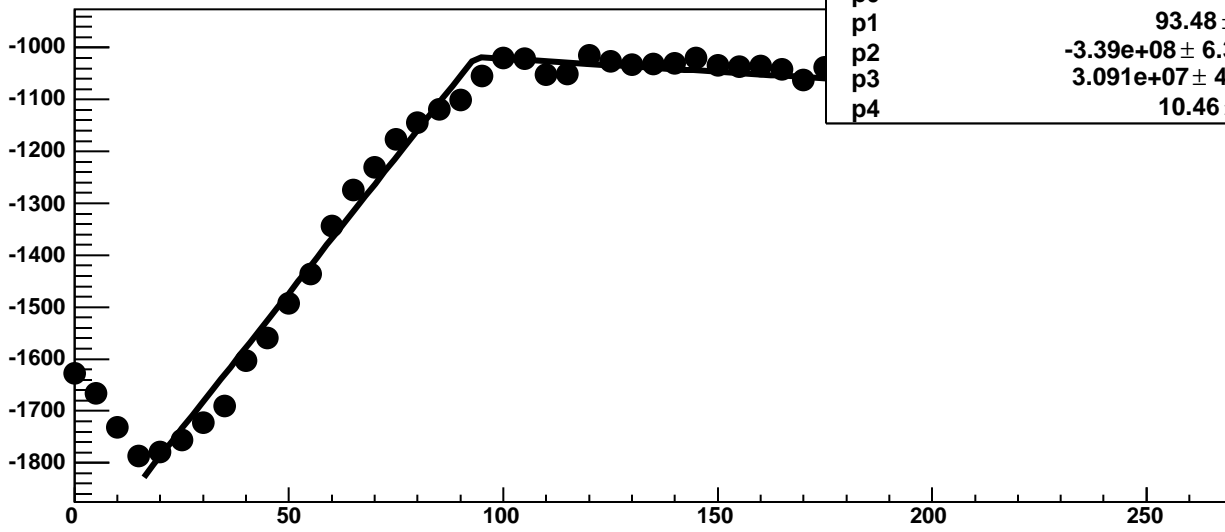
Chip 1, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

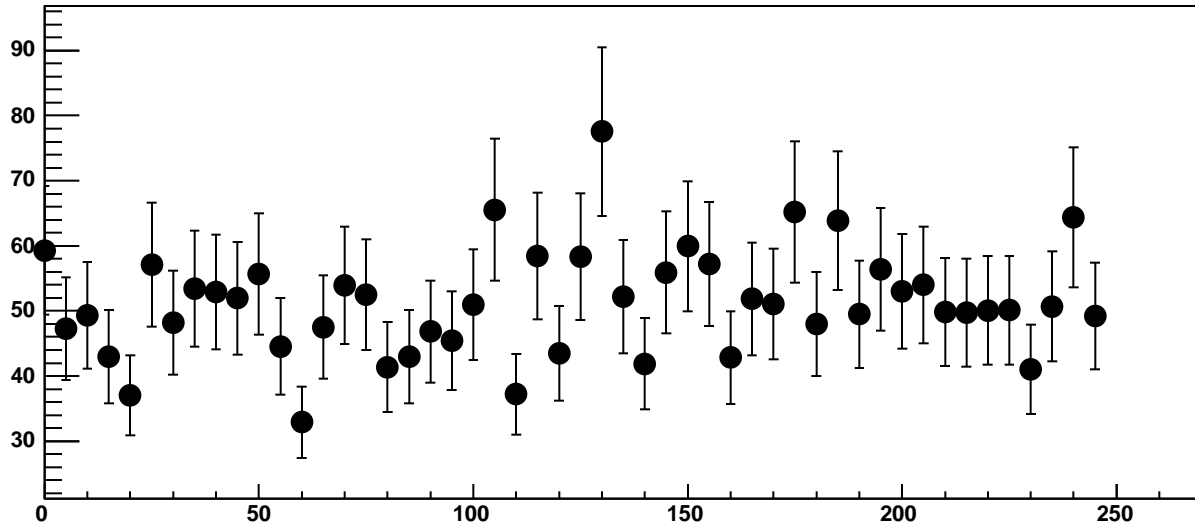


Chip 1, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

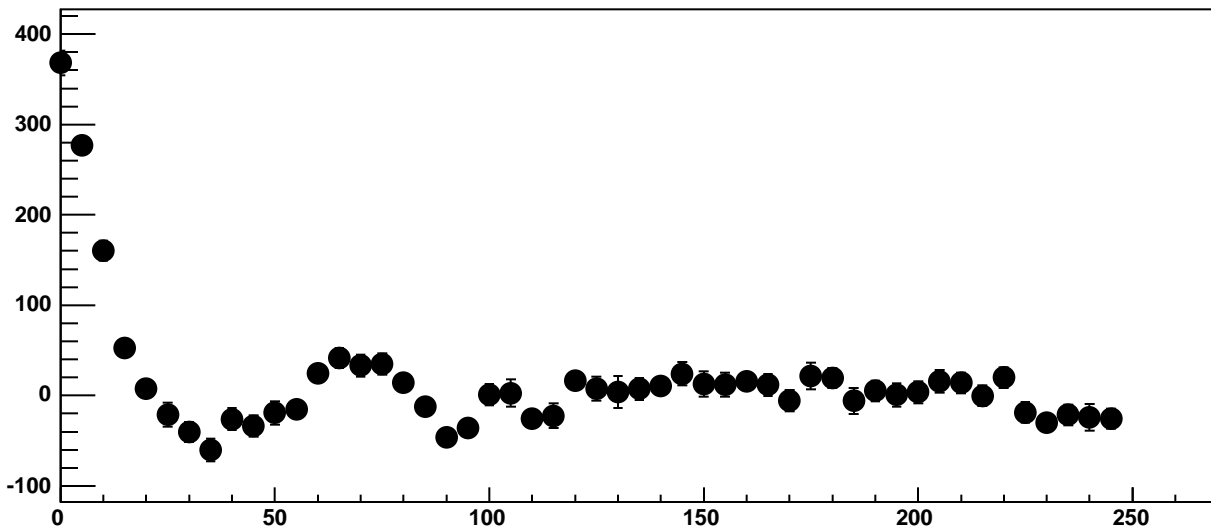


$\chi^2 / \text{ndf}$	218.4 / 41
p0	$-1018 \pm 3.975$
p1	$93.48 \pm 0.6088$
p2	$-3.39\text{e}+08 \pm 6.346\text{e}+06$
p3	$3.091\text{e}+07 \pm 4.18\text{e}+05$
p4	$10.46 \pm 0.1112$

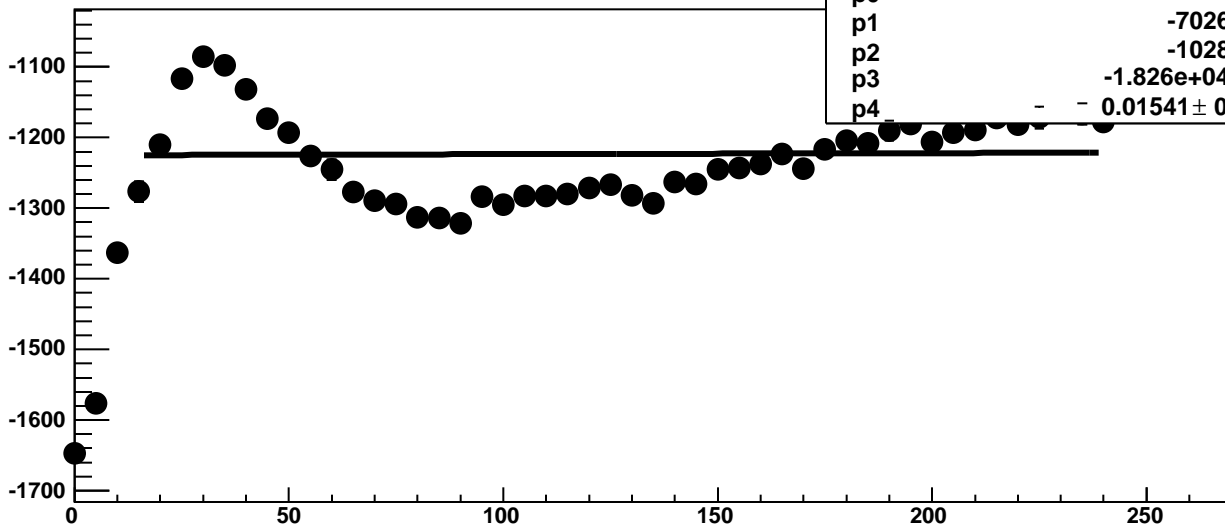
Chip 1, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



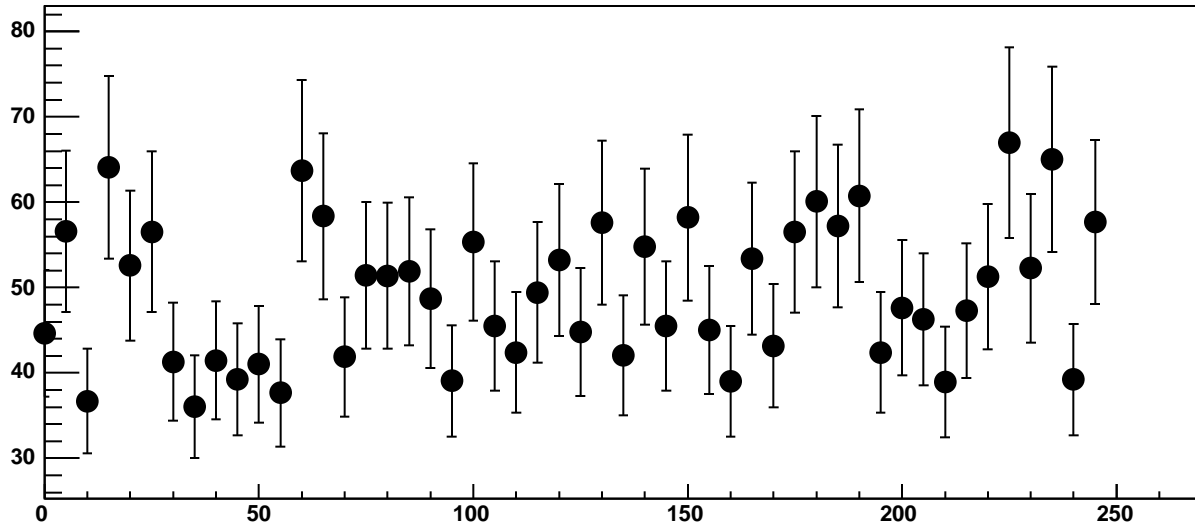
Chip 1, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold



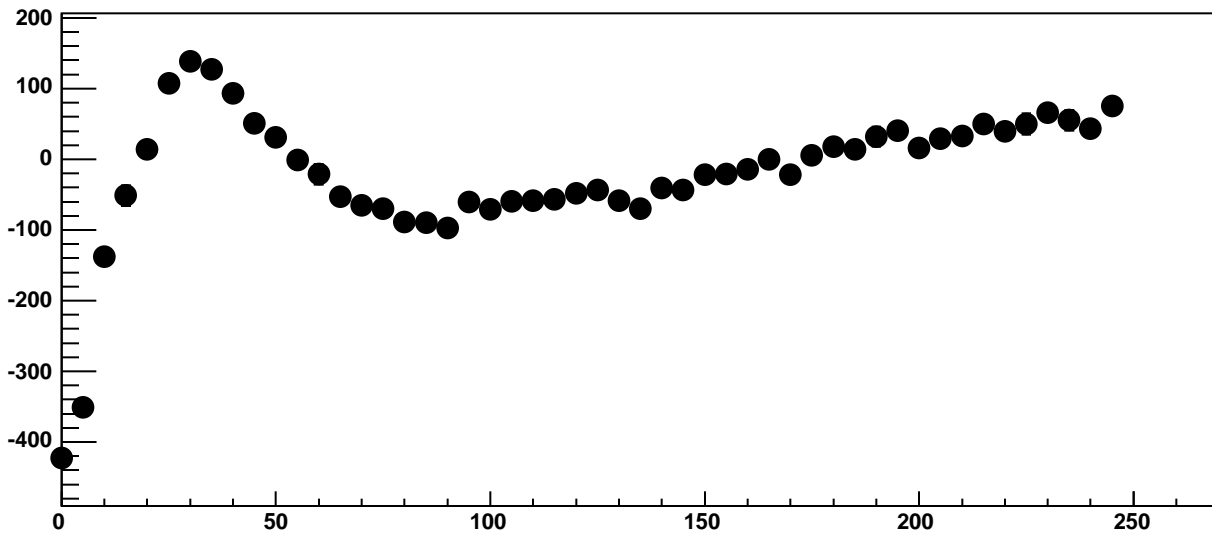
Chip 1, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold



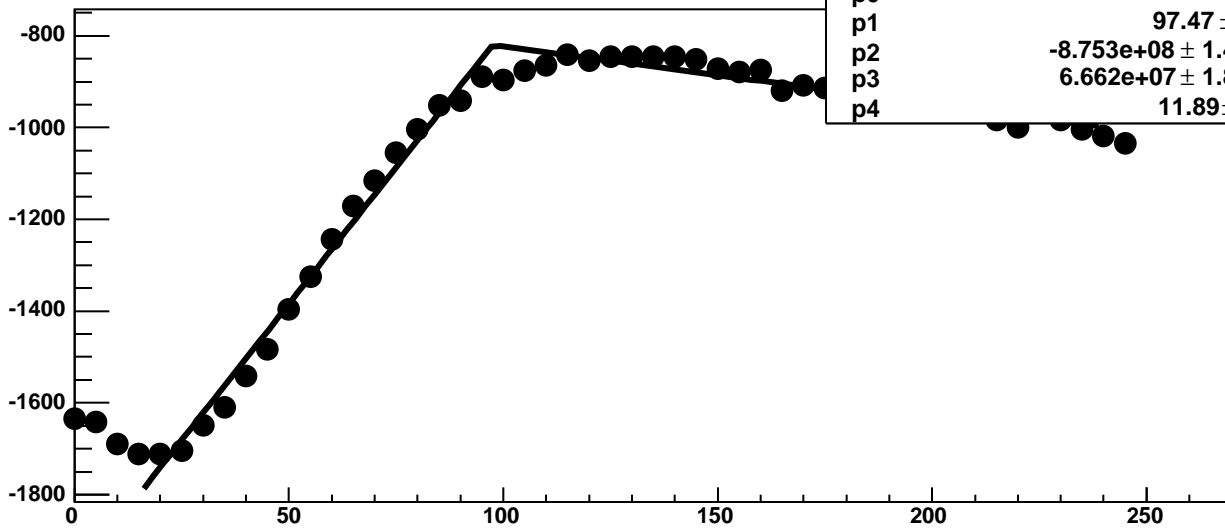
Chip 1, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

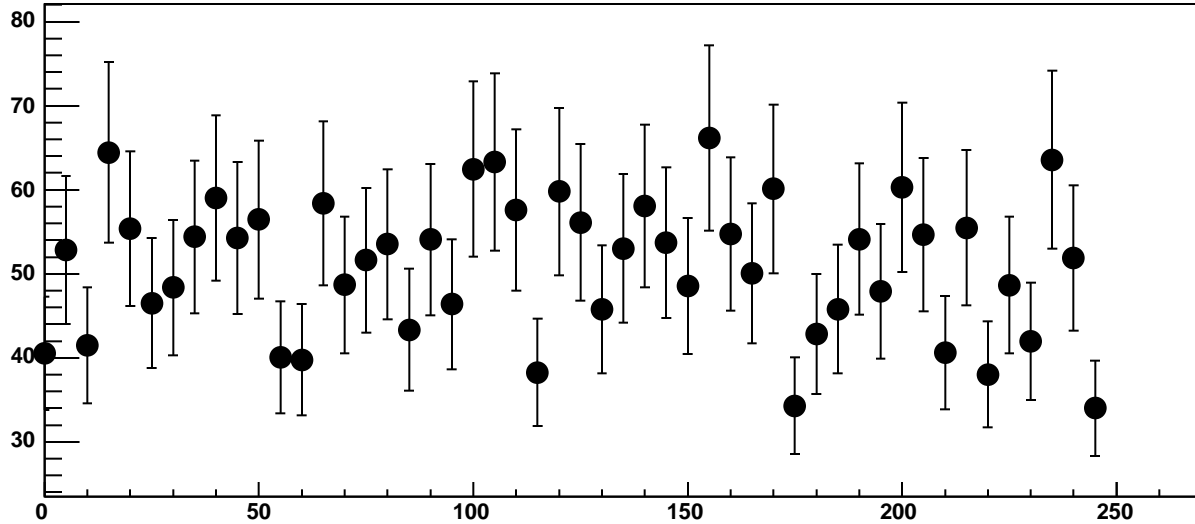


Chip 1, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

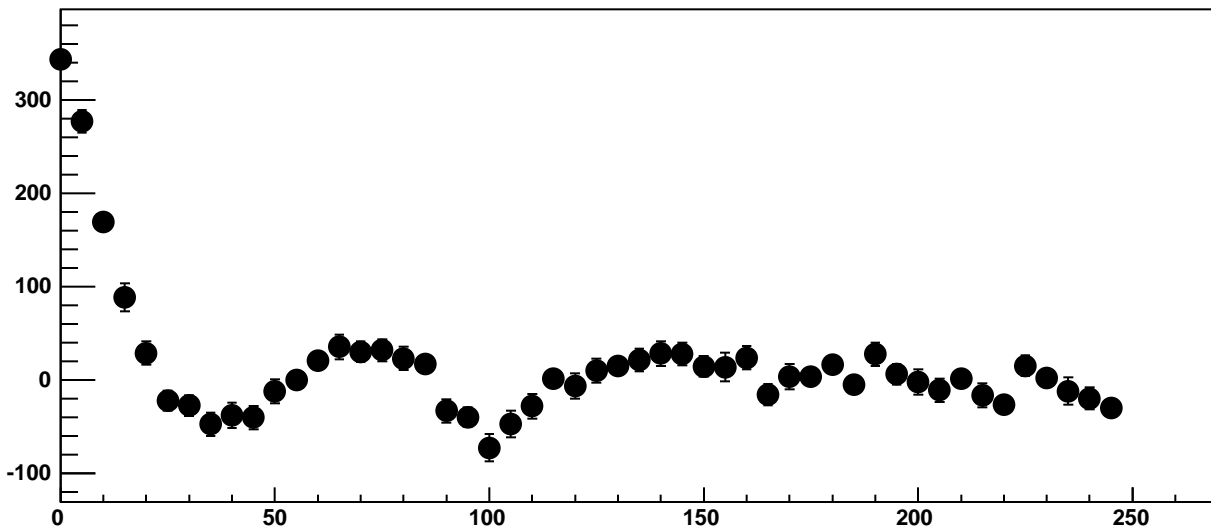


$\chi^2 / \text{ndf}$	229.6 / 41
p0	-819.9 ± 4.877
p1	97.47 ± 0.3865
p2	-8.753e+08 ± 1.425e+07
p3	6.662e+07 ± 1.816e+06
p4	11.89 ± 0.1172

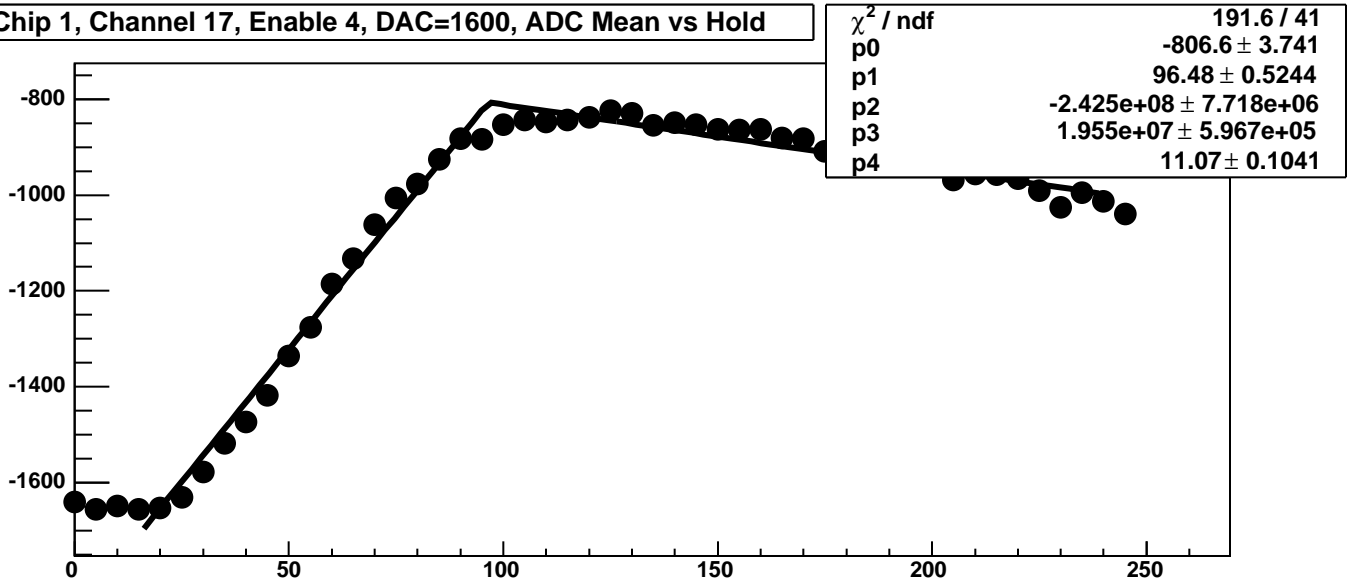
Chip 1, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



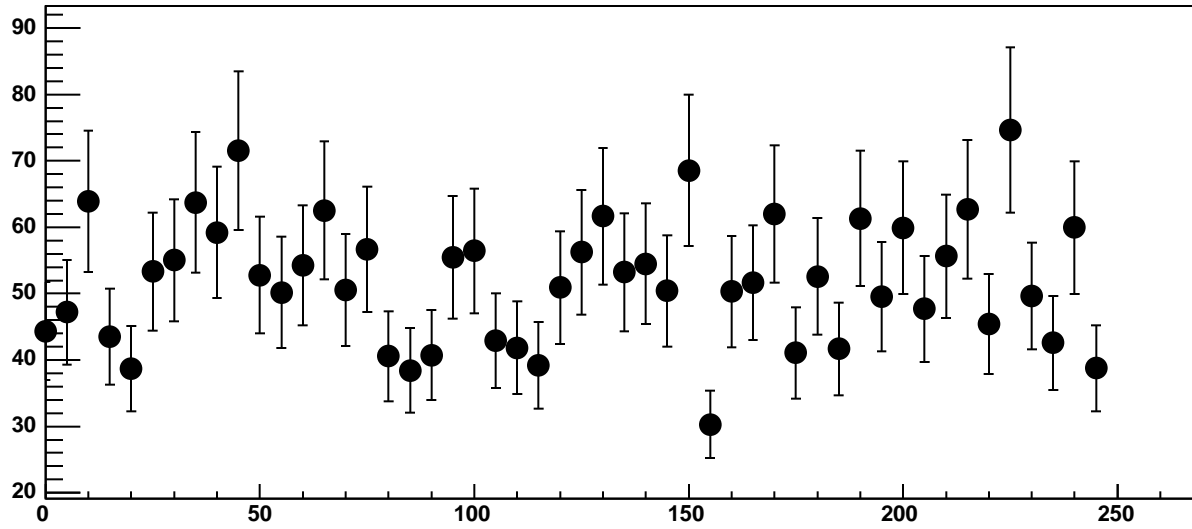
Chip 1, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



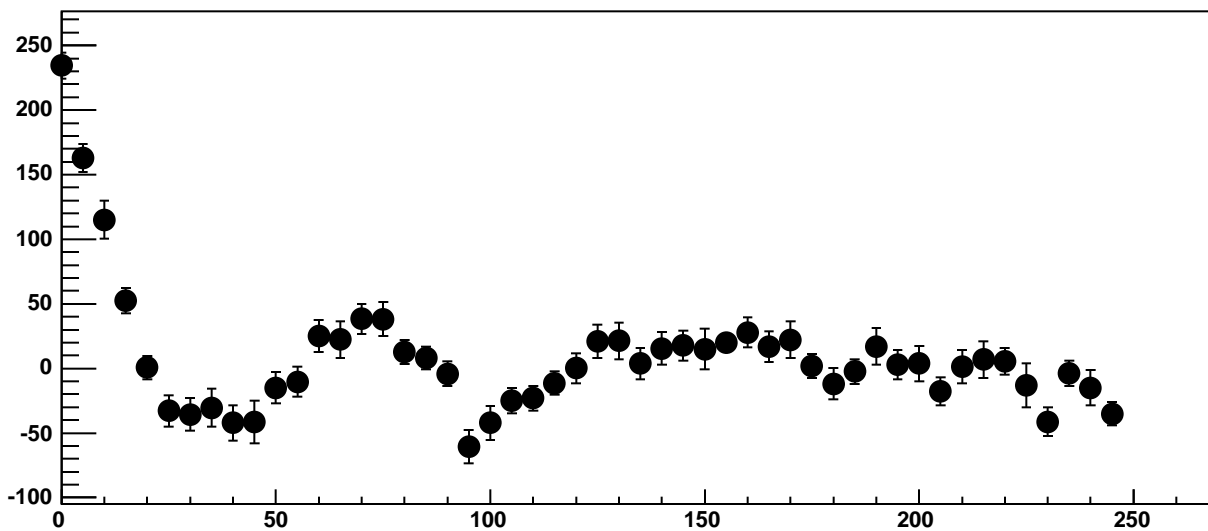
Chip 1, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold



Chip 1, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold

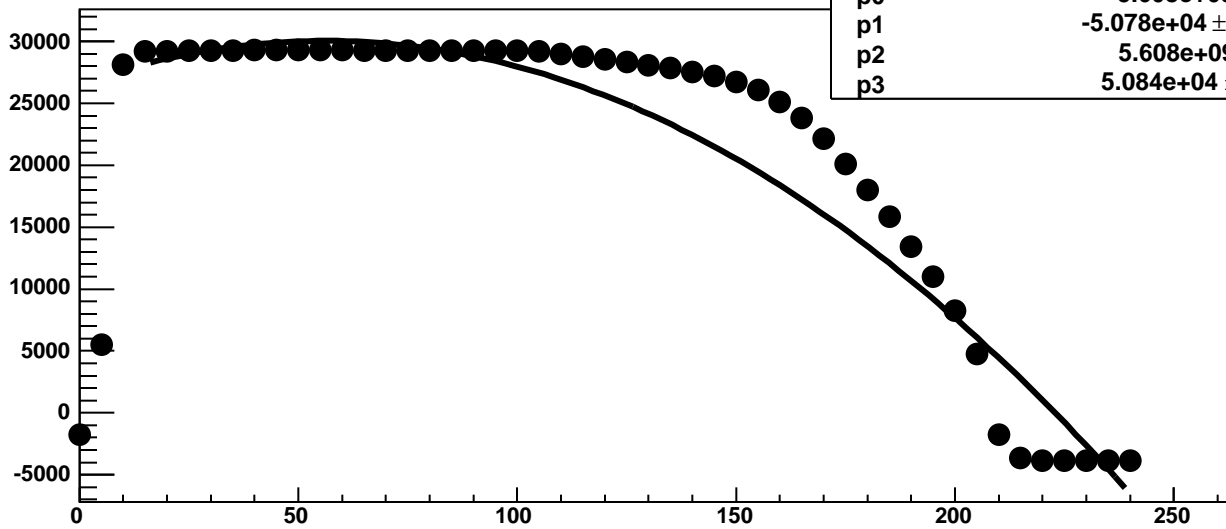


Chip 1, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

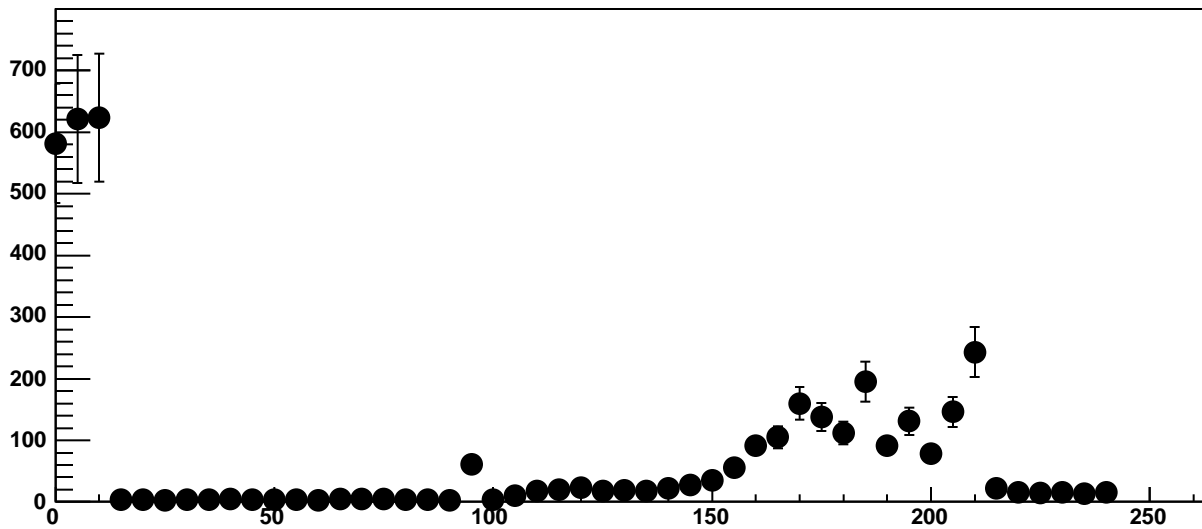


Chip 1, Channel 17, Enable 5!, DAC=1600, ADC Mean vs Hold

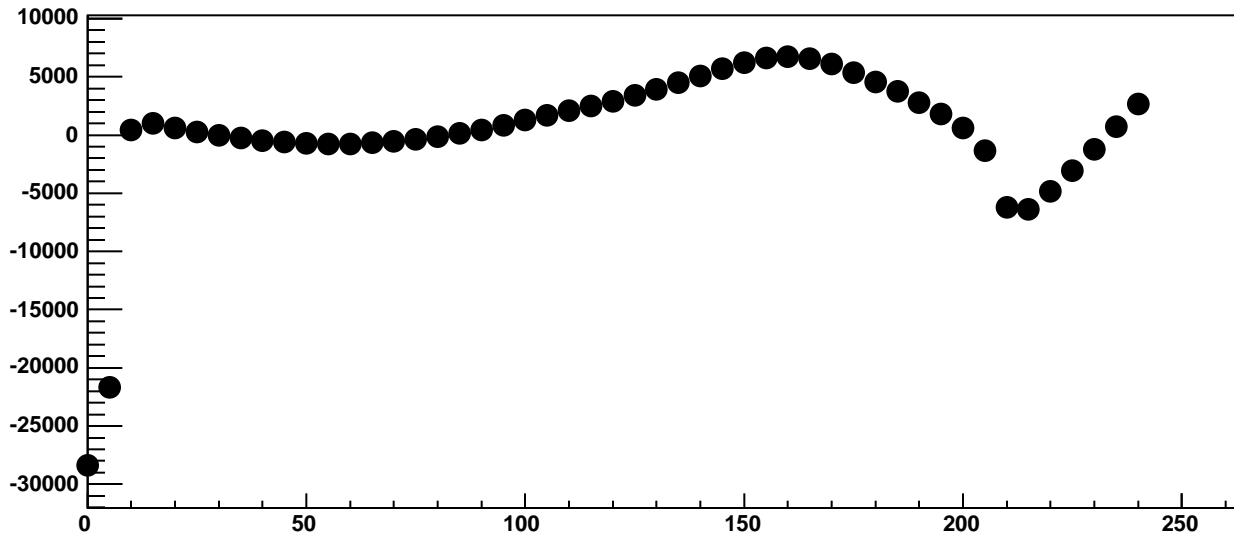
$\chi^2 / \text{ndf}$	2.073e+07 / 42
p0	-5.608e+09 $\pm$ 3.105
p1	-5.078e+04 $\pm$ 0.03746
p2	5.608e+09 $\pm$ 3.105
p3	5.084e+04 $\pm$ 0.0374



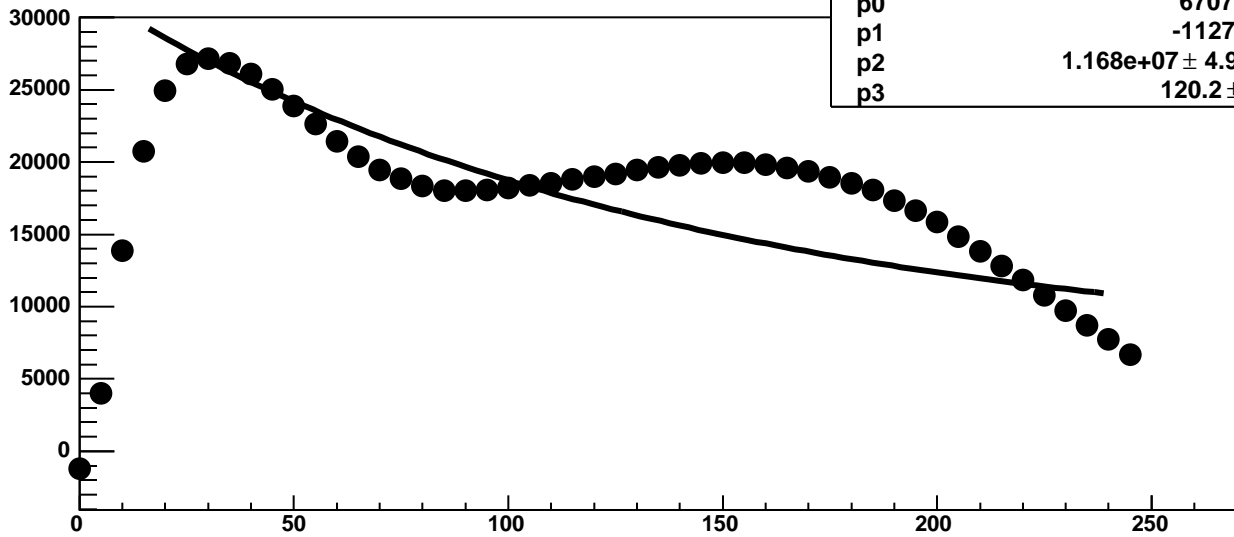
Chip 1, Channel 17, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 1, Channel 17, Enable 5!, DAC=1600, ADC Residuals vs Hold

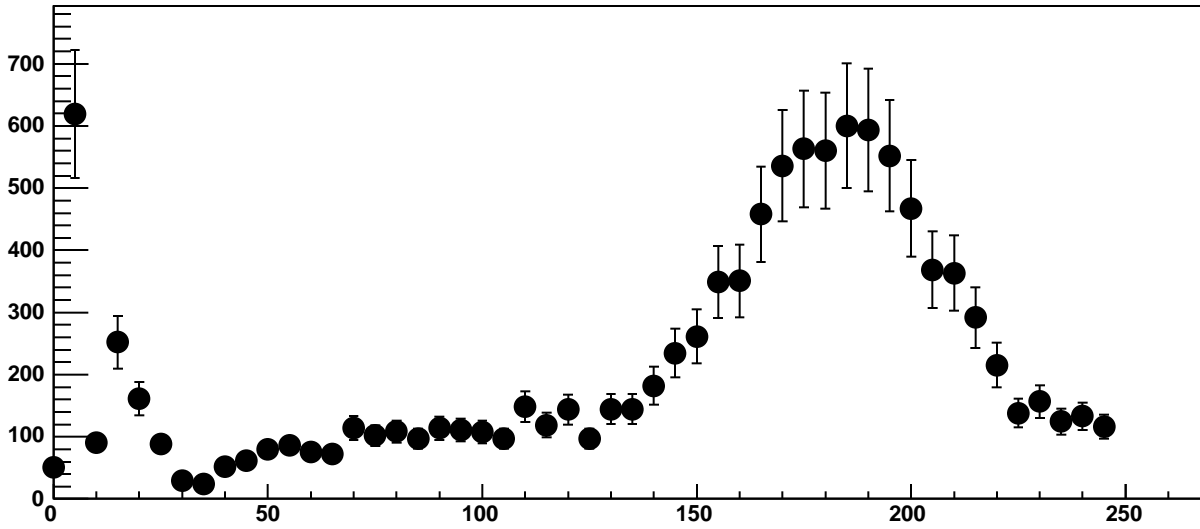


Chip 2, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold

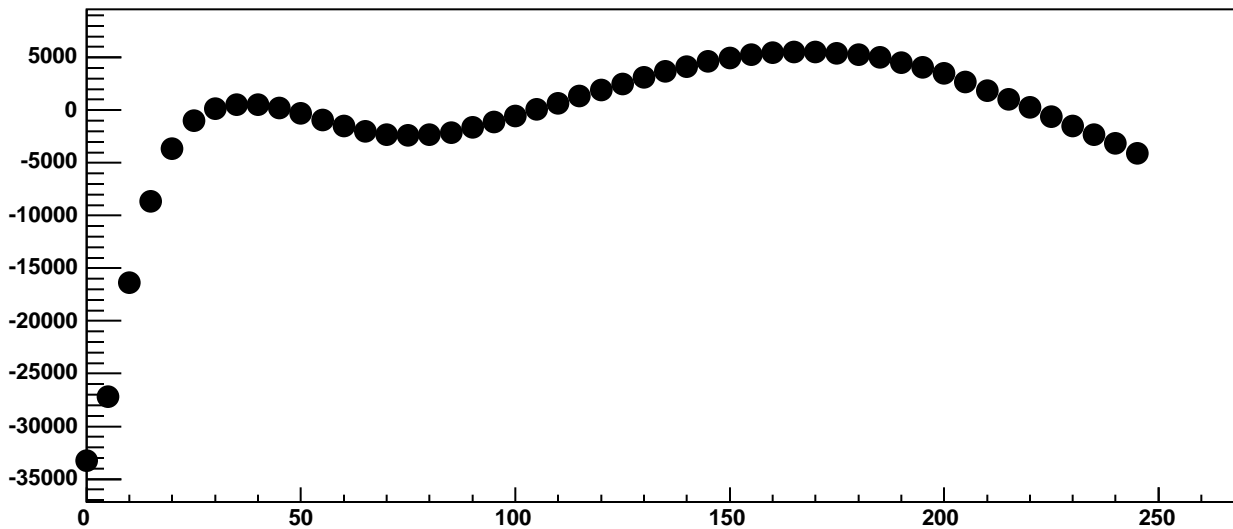


$\chi^2 / \text{ndf}$	2.204e+05 / 42
p0	6707 $\pm$ 49.56
p1	-1127 $\pm$ 8.444
p2	1.168e+07 $\pm$ 4.961e+05
p3	120.2 $\pm$ 0.4982

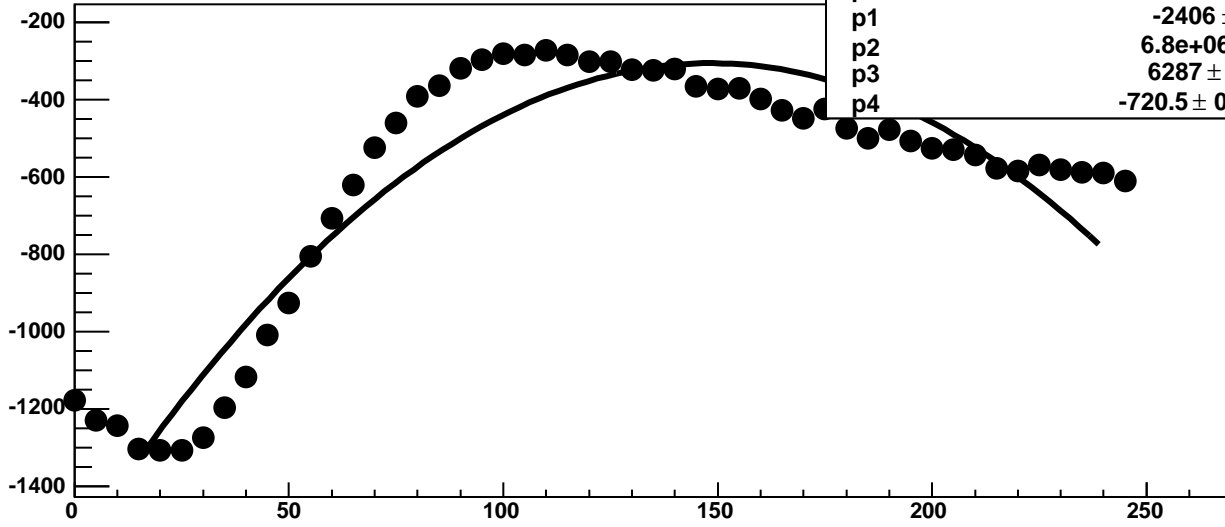
Chip 2, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold

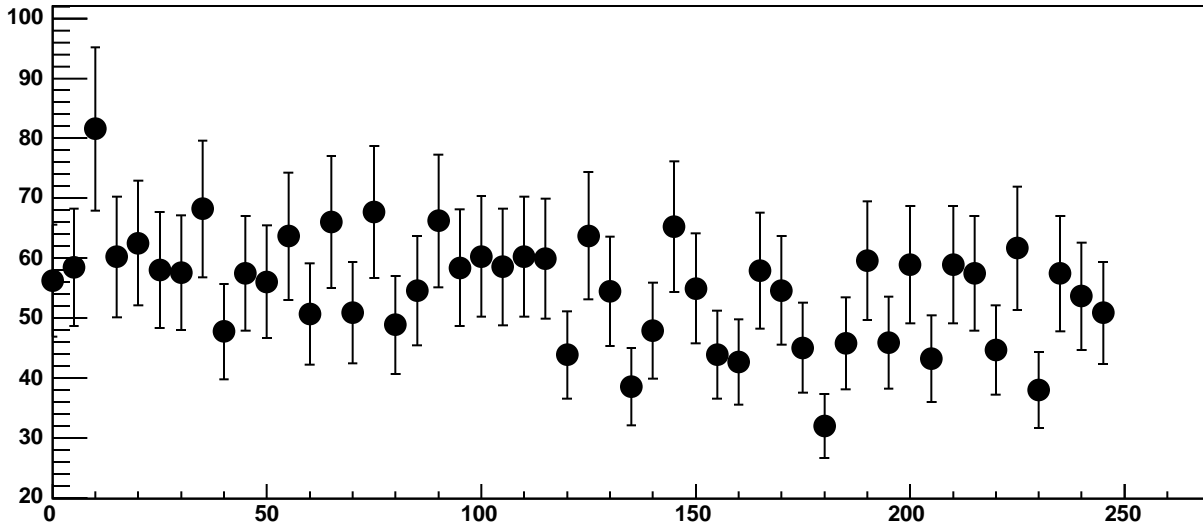


Chip 2, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

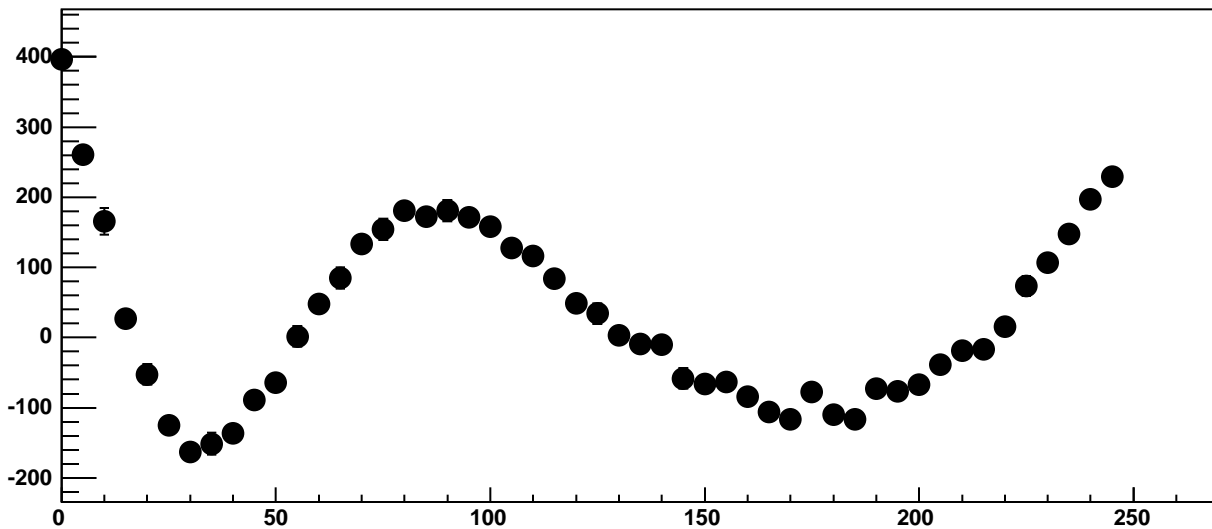


$\chi^2 / \text{ndf}$	3365 / 41
p0	$-4.303\text{e}+05 \pm 24.03$
p1	$-2406 \pm 0.2469$
p2	$6.8\text{e}+06 \pm 72.17$
p3	$6287 \pm 0.08228$
p4	$-720.5 \pm 0.009436$

Chip 2, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

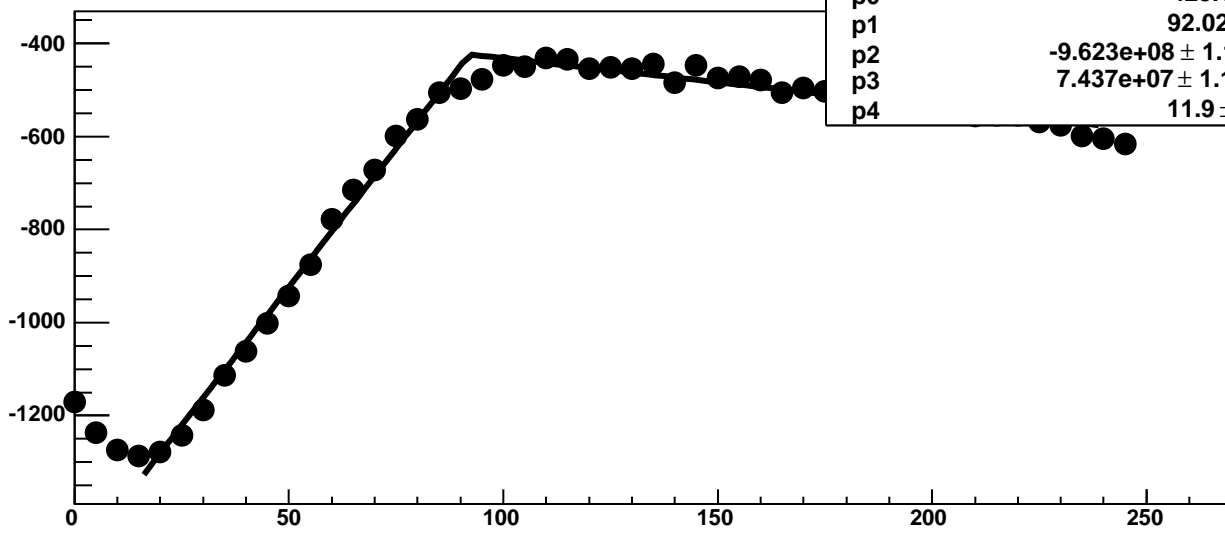


Chip 2, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



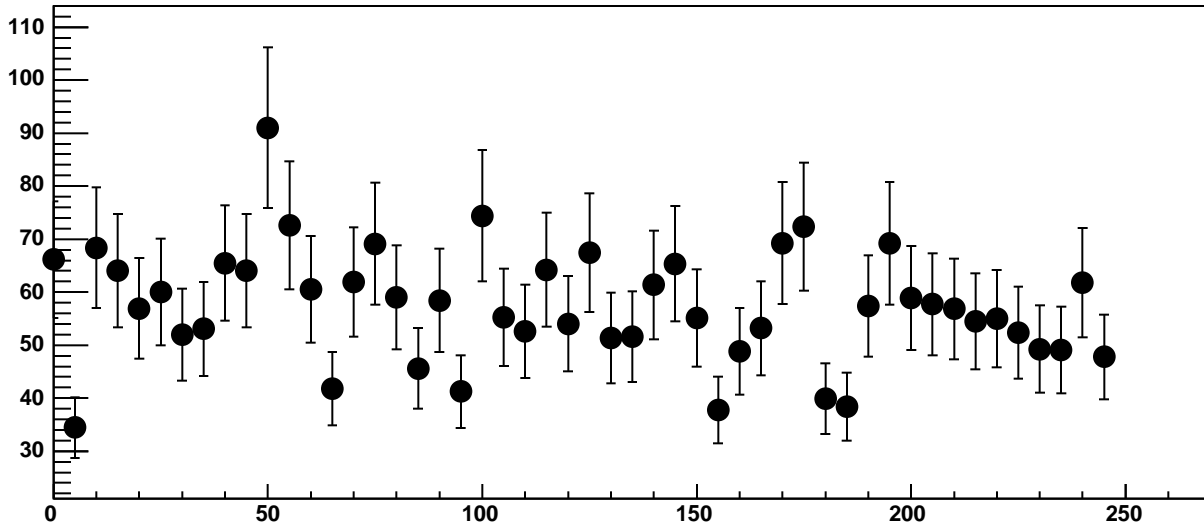


Chip 2, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

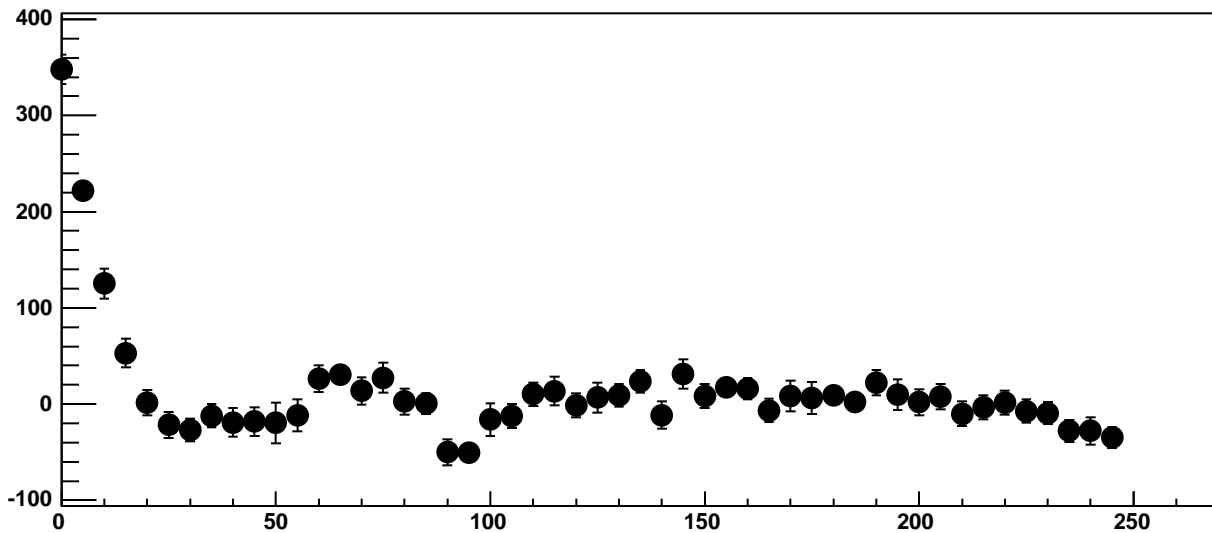


$\chi^2 / \text{ndf}$	123.2 / 41
p0	$-423.1 \pm 4.196$
p1	$92.02 \pm 0.596$
p2	$-9.623\text{e}+08 \pm 1.124\text{e}+07$
p3	$7.437\text{e}+07 \pm 1.165\text{e}+05$
p4	$11.9 \pm 0.1405$

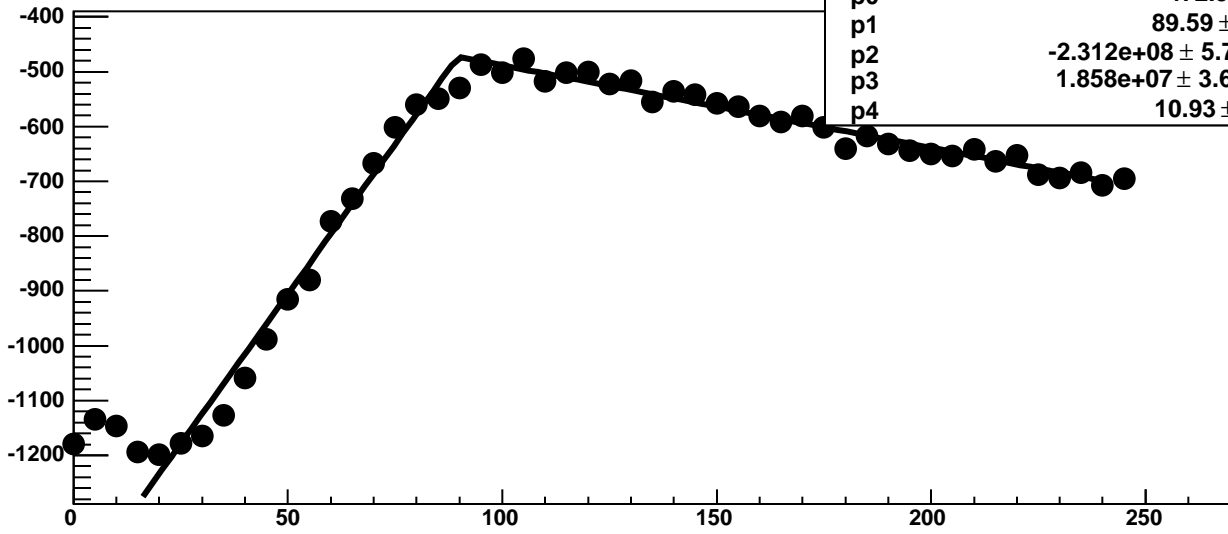
Chip 2, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



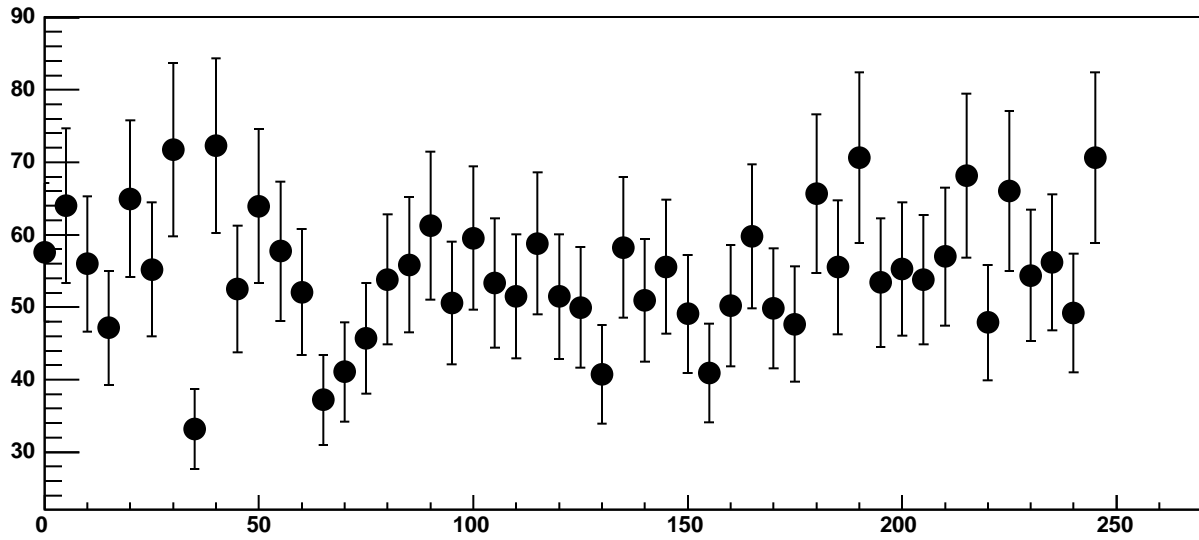
Chip 2, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



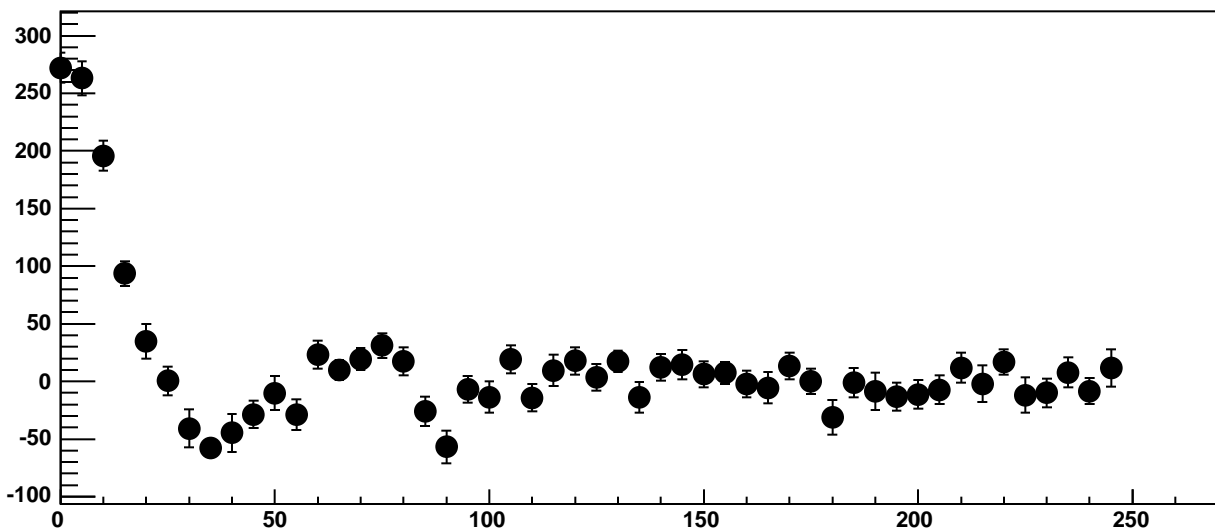
Chip 2, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold



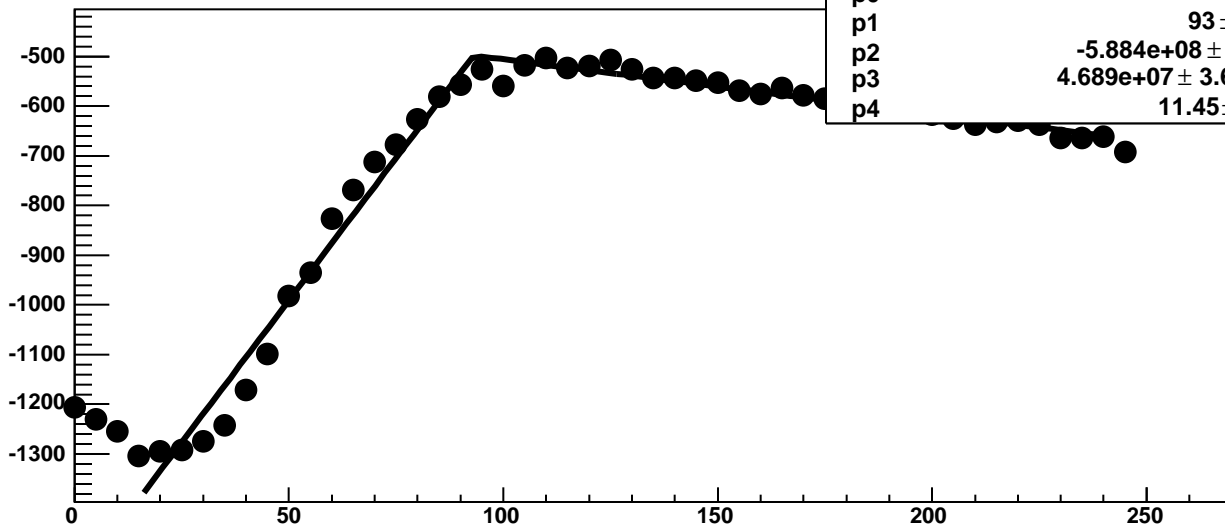
Chip 2, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold

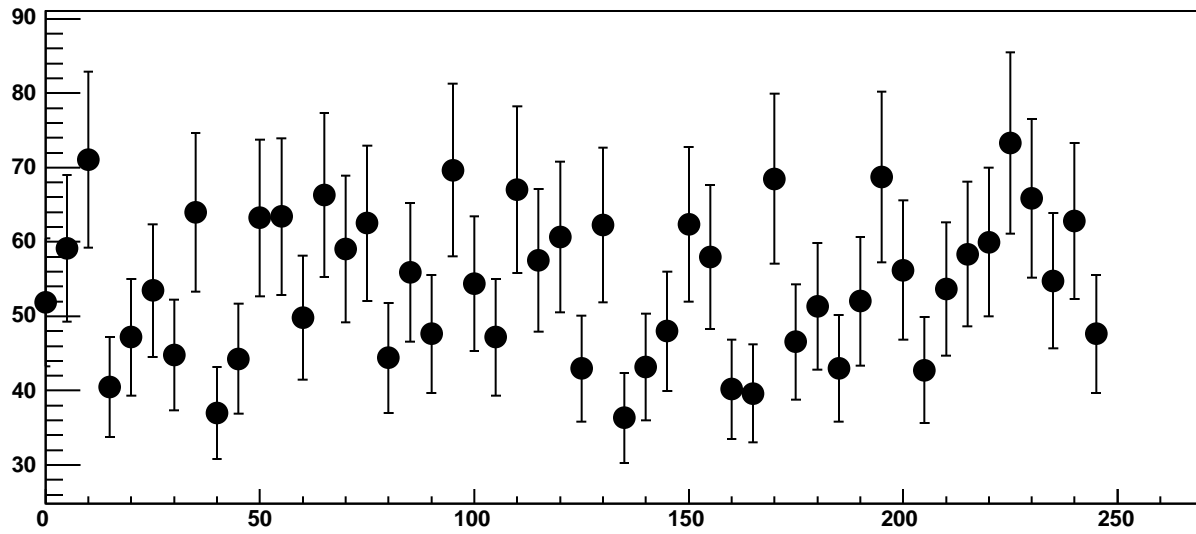


Chip 2, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

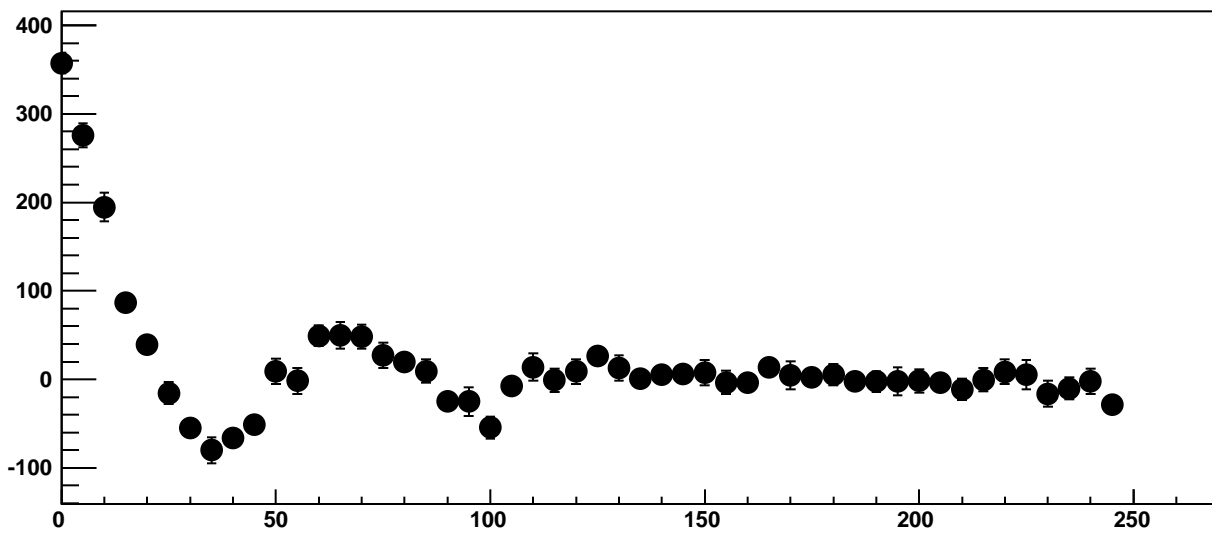


$\chi^2 / \text{ndf}$	341.1 / 41
p0	$-498 \pm 4.129$
p1	$93 \pm 0.5944$
p2	$-5.884\text{e}+08 \pm 7.7\text{e}+06$
p3	$4.689\text{e}+07 \pm 3.653\text{e}+05$
p4	$11.45 \pm 0.1203$

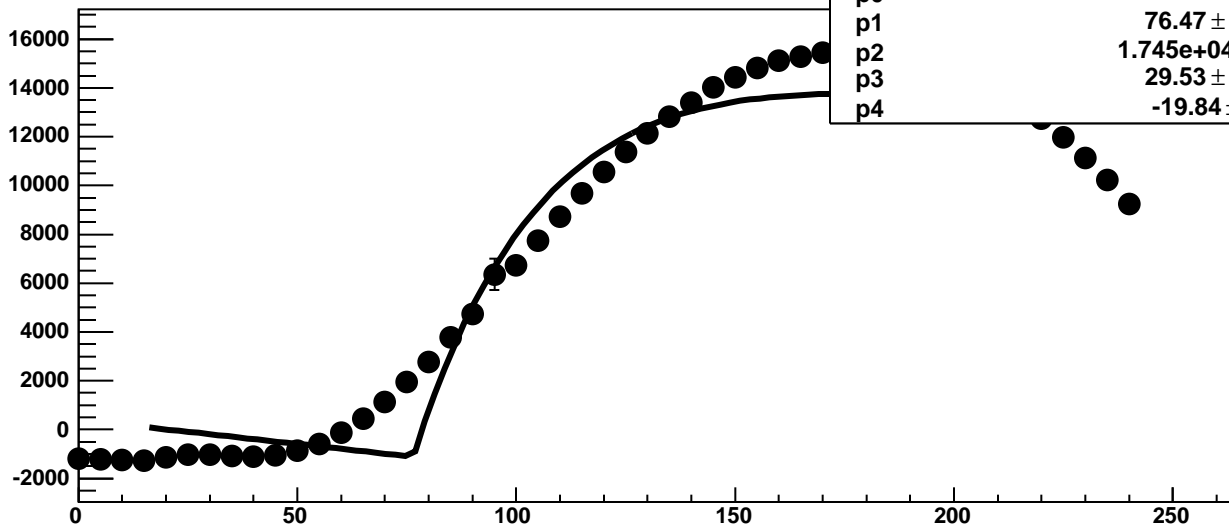
Chip 2, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

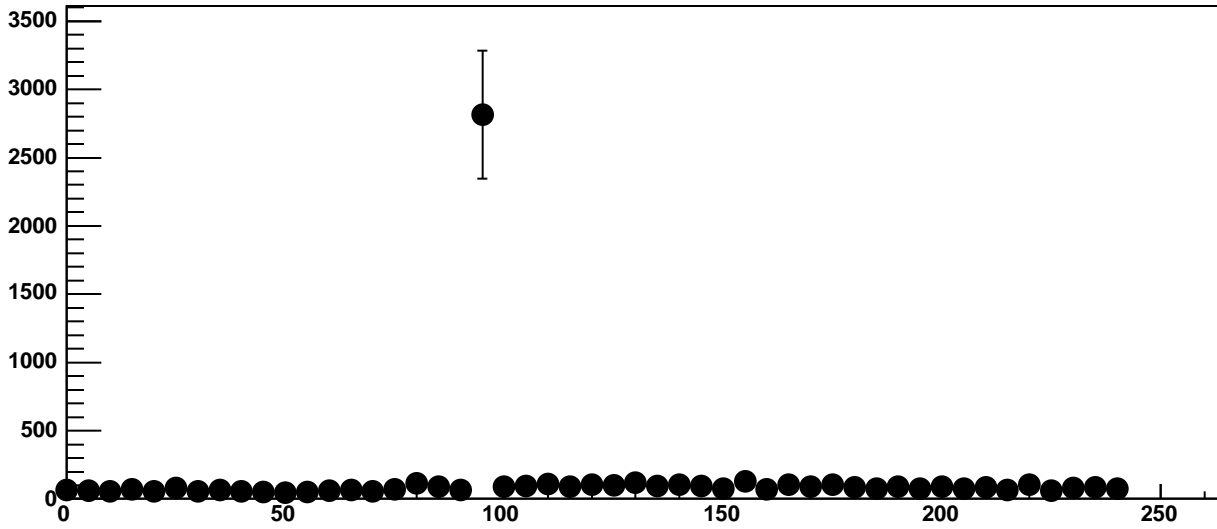


Chip 2, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

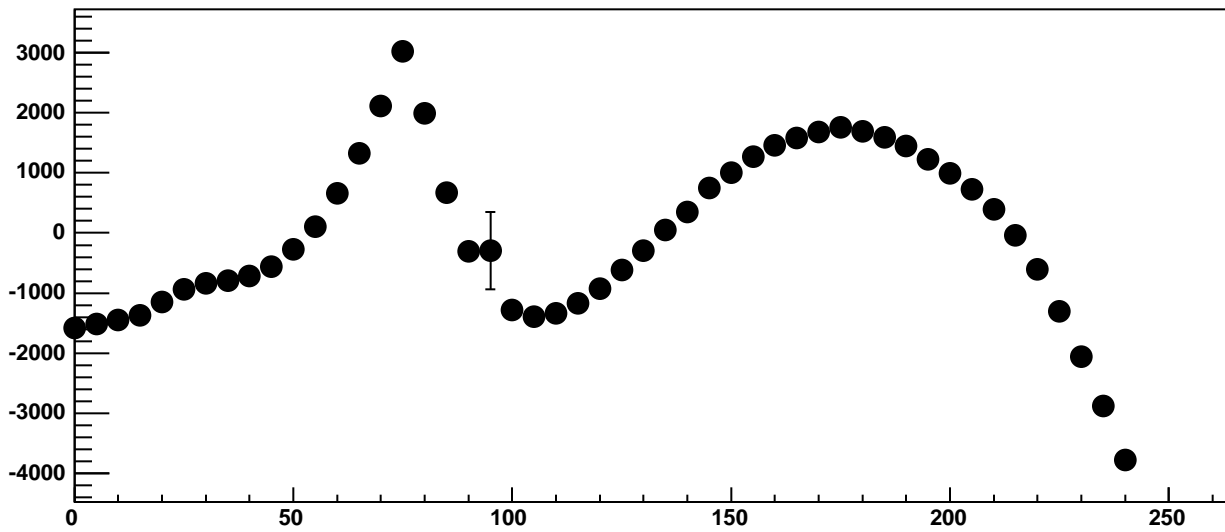


$\chi^2 / \text{ndf}$	2.801e+05 / 41
p0	-1112 ± 5.573
p1	76.47 ± 0.03403
p2	1.745e+04 ± 24.71
p3	29.53 ± 0.06445
p4	-19.84 ± 0.1429

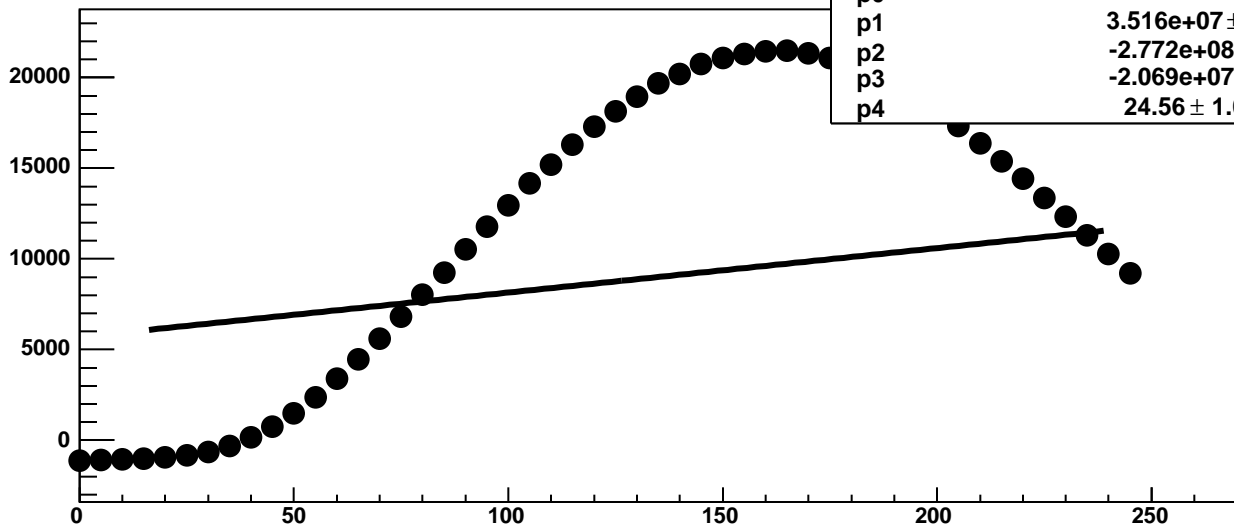
Chip 2, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

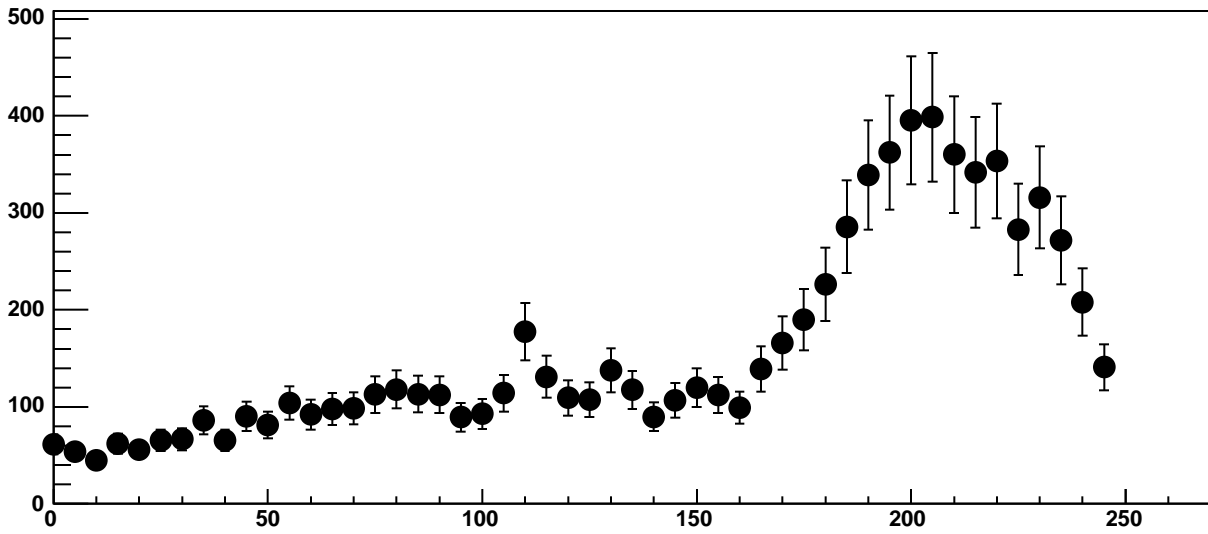


Chip 2, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

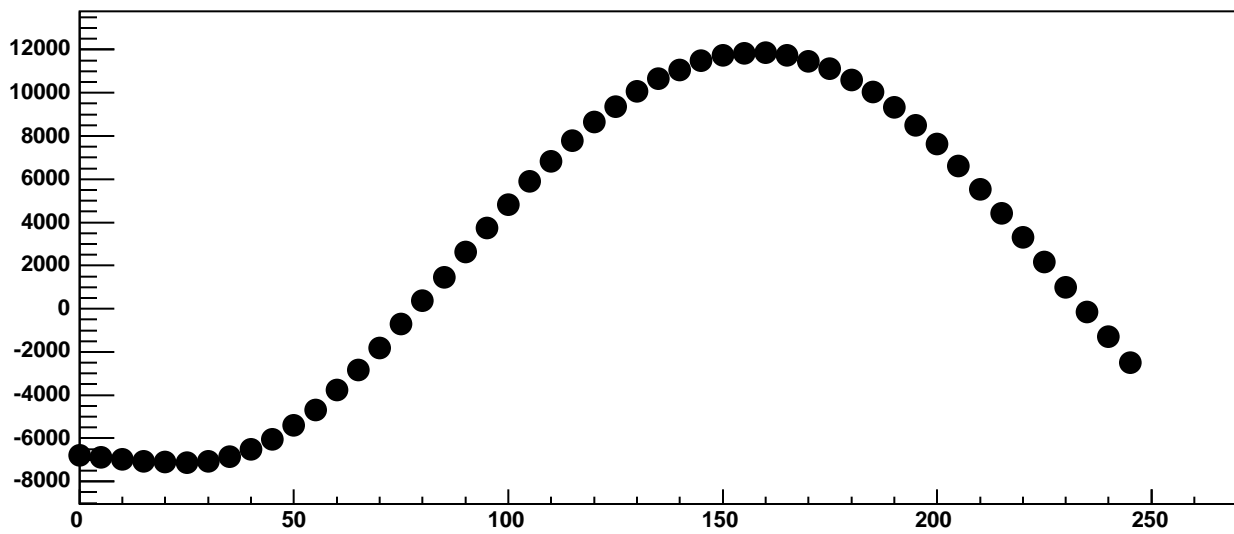


$\chi^2 / \text{ndf}$	3.891e+06 / 41
p0	8.638e+08 ± 3.713
p1	3.516e+07 ± 0.1512
p2	-2.772e+08 ± 33.94
p3	-2.069e+07 ± 1.414
p4	24.56 ± 1.056e-07

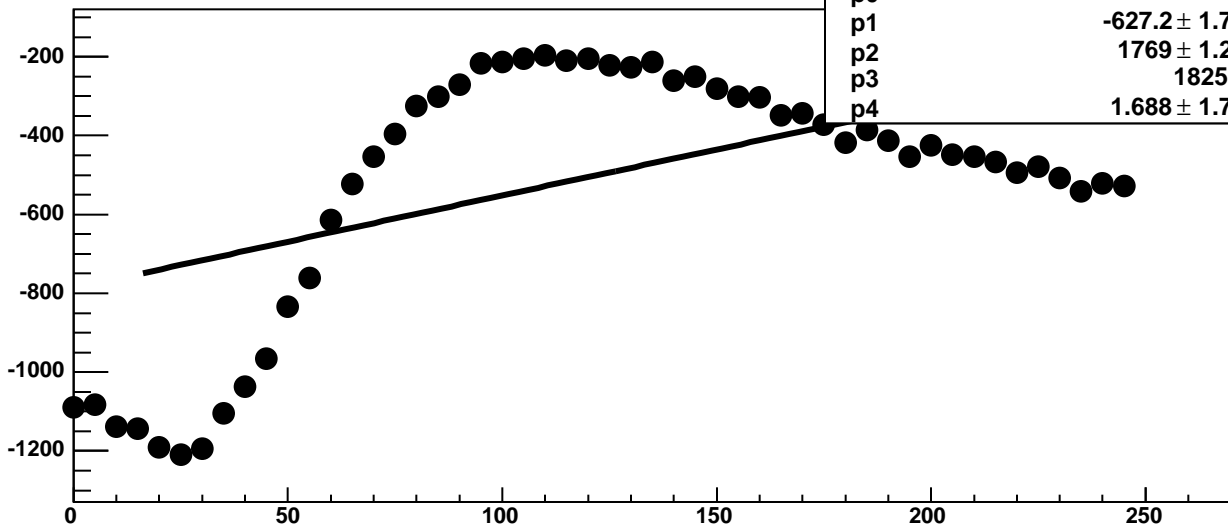
Chip 2, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



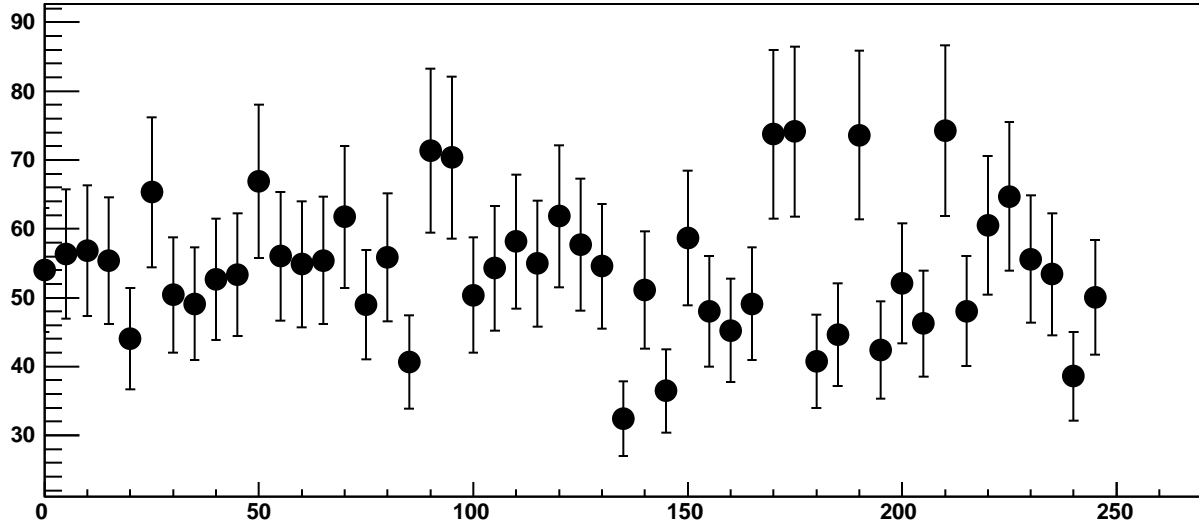
Chip 2, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold



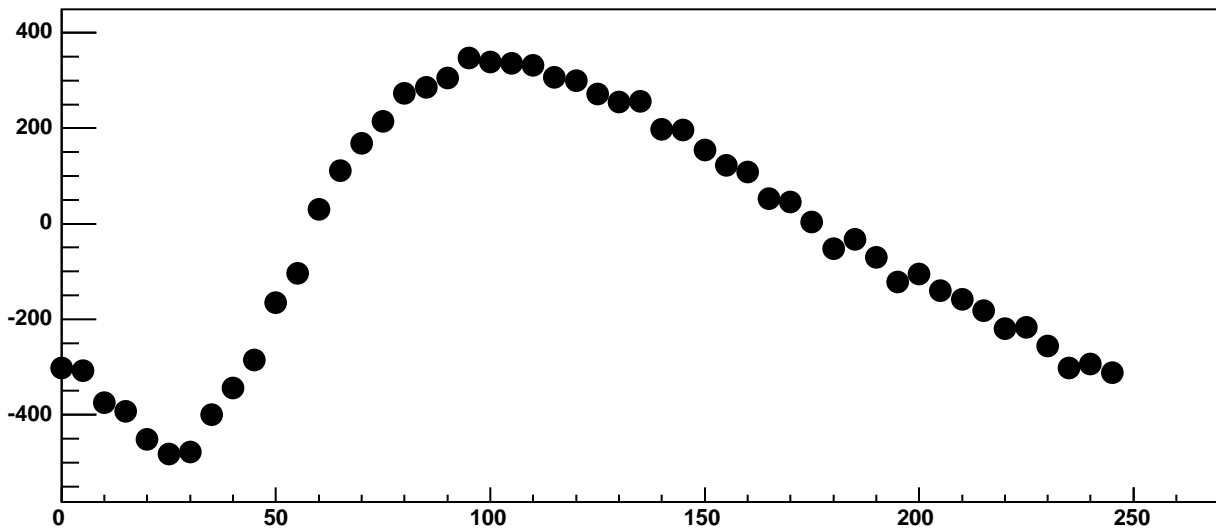
Chip 2, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold



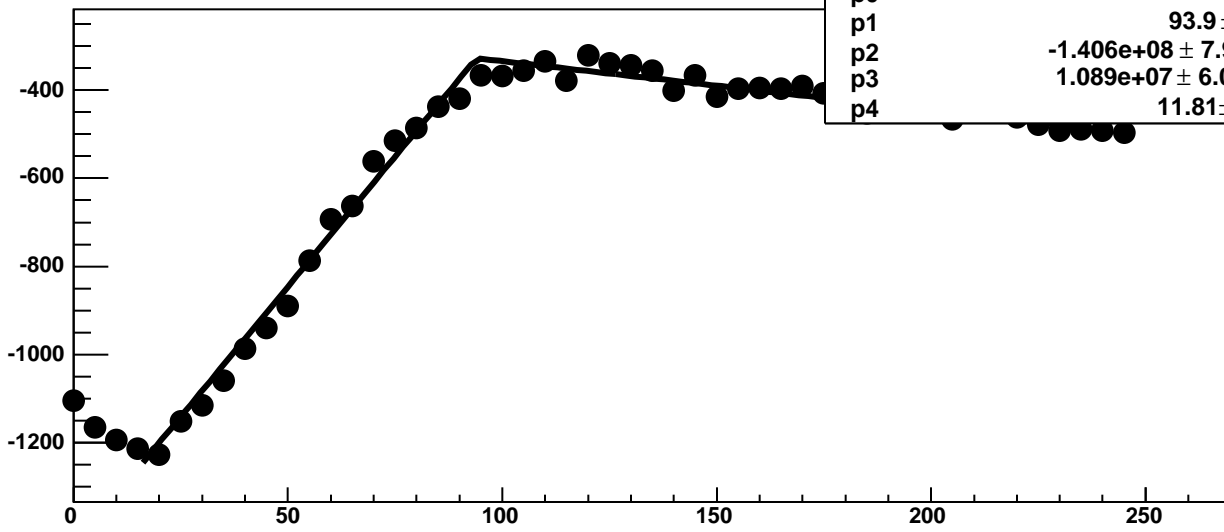
Chip 2, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



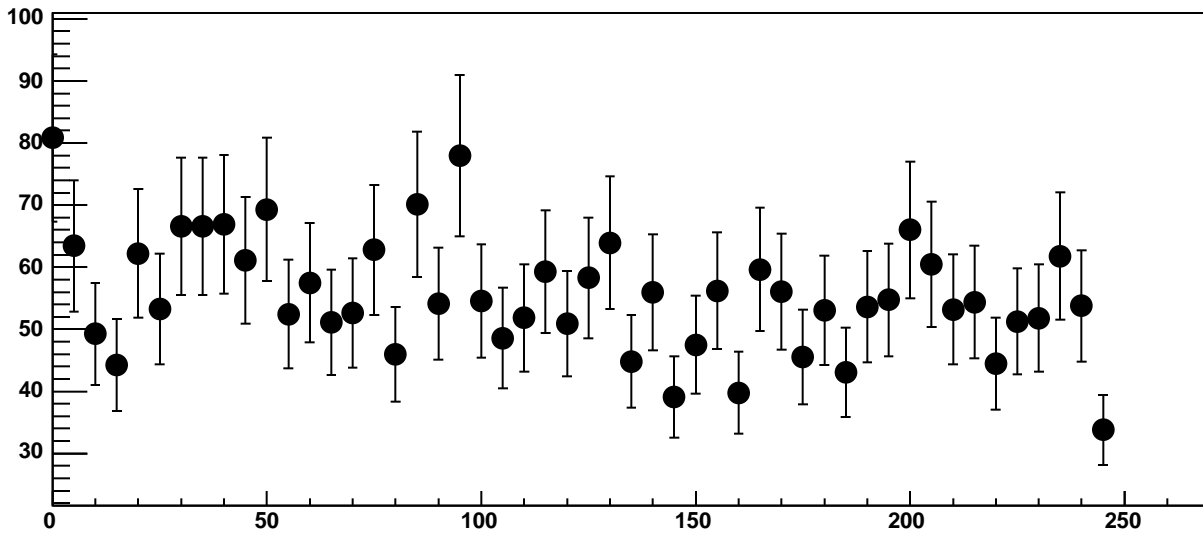
Chip 2, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold



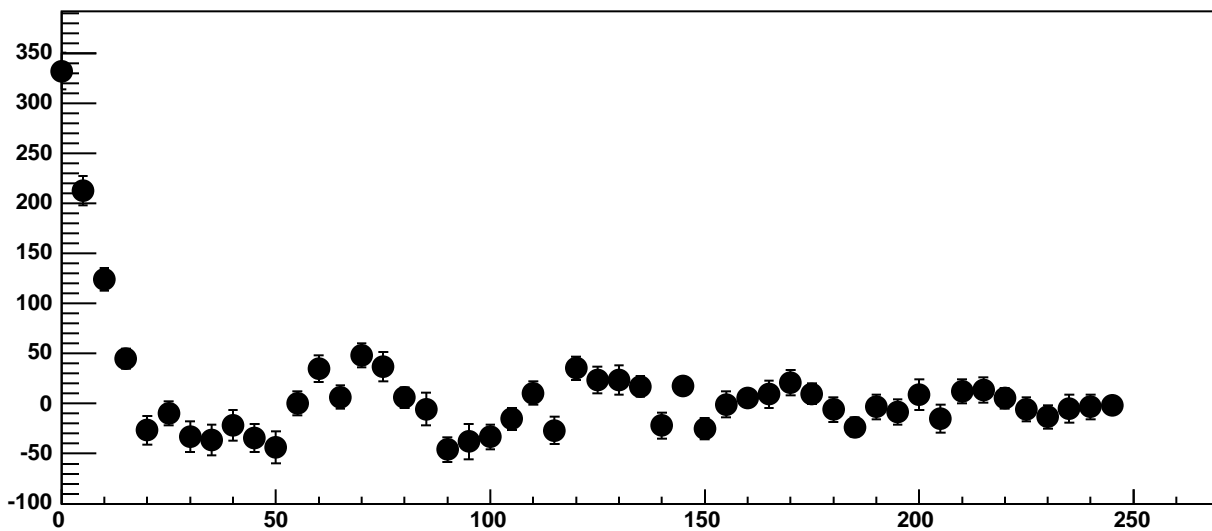
Chip 2, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold



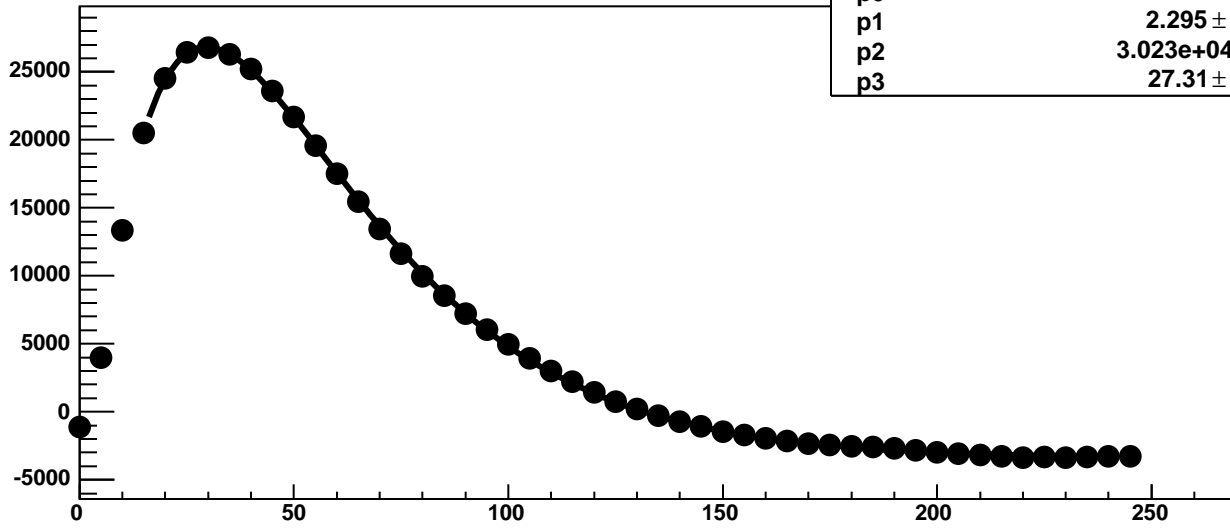
Chip 2, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

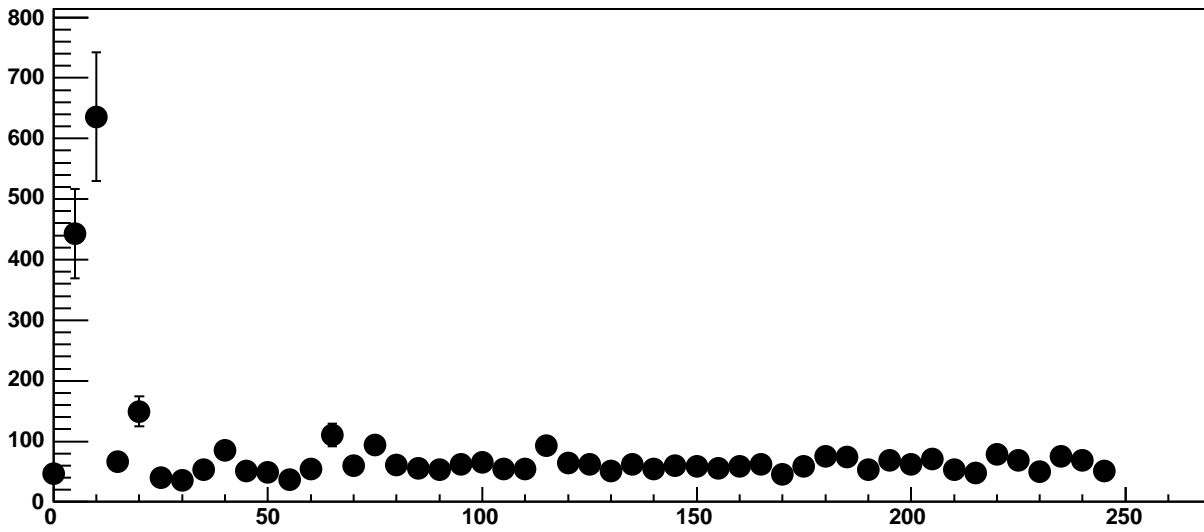


Chip 2, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

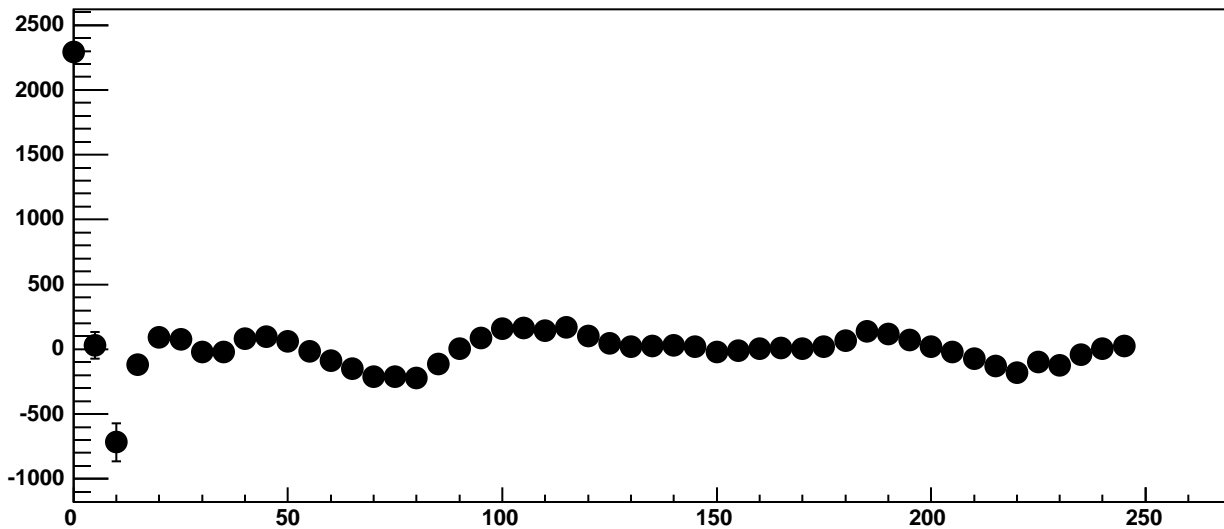


$\chi^2 / \text{ndf}$	2226 / 42
p0	-3407 ± 3.713
p1	2.295 ± 0.01697
p2	3.023e+04 ± 5.279
p3	27.31 ± 0.01067

Chip 2, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

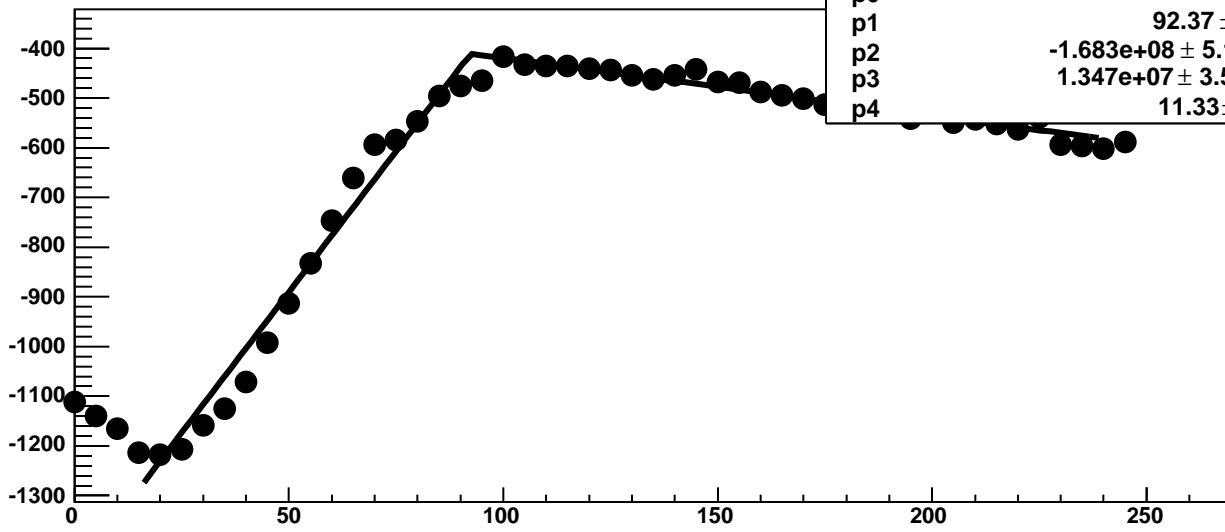


Chip 2, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold

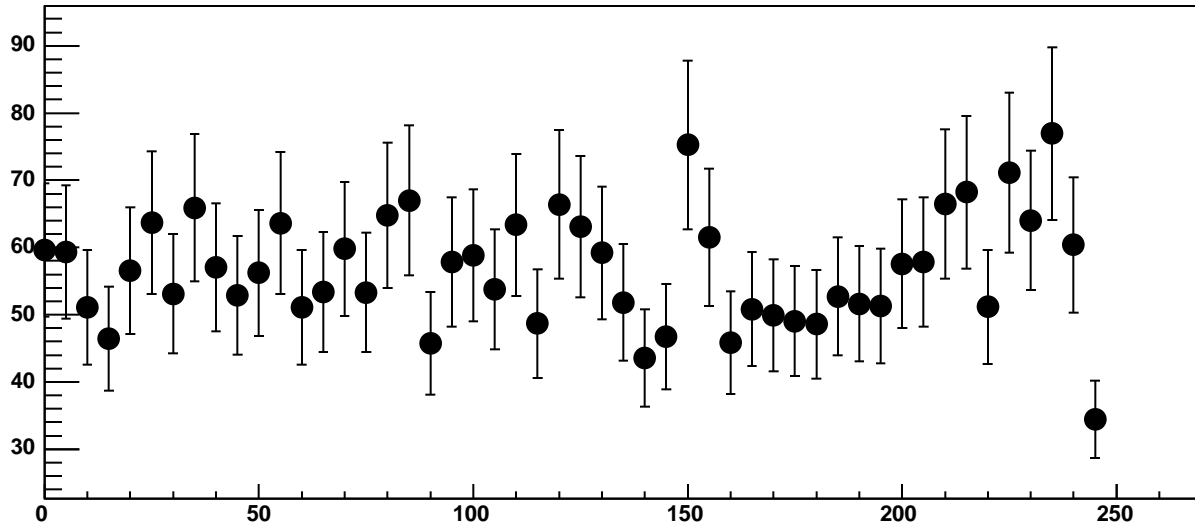




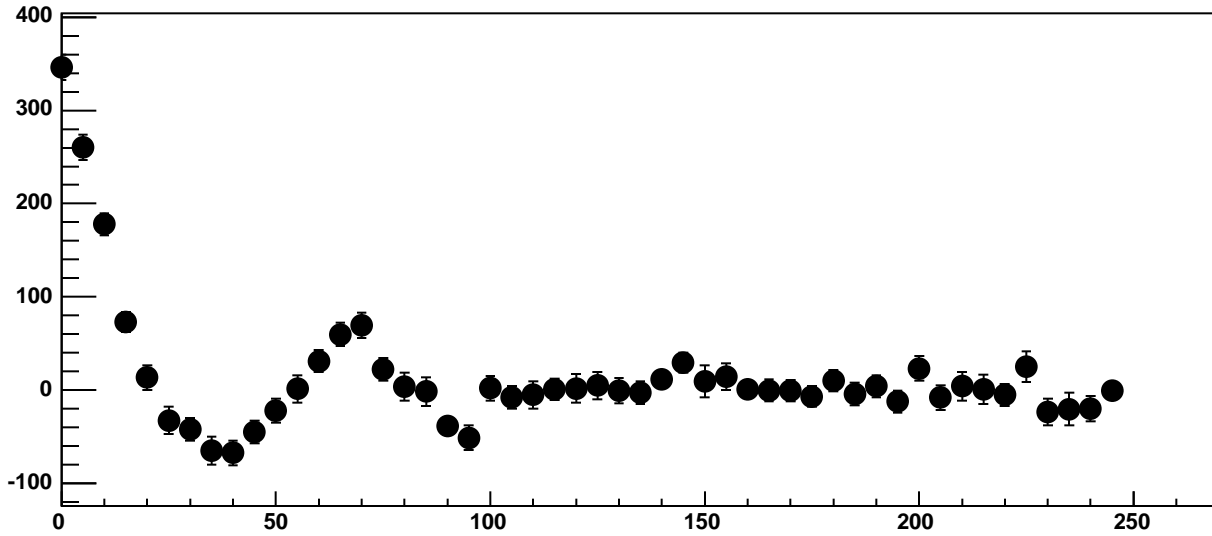
Chip 2, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold



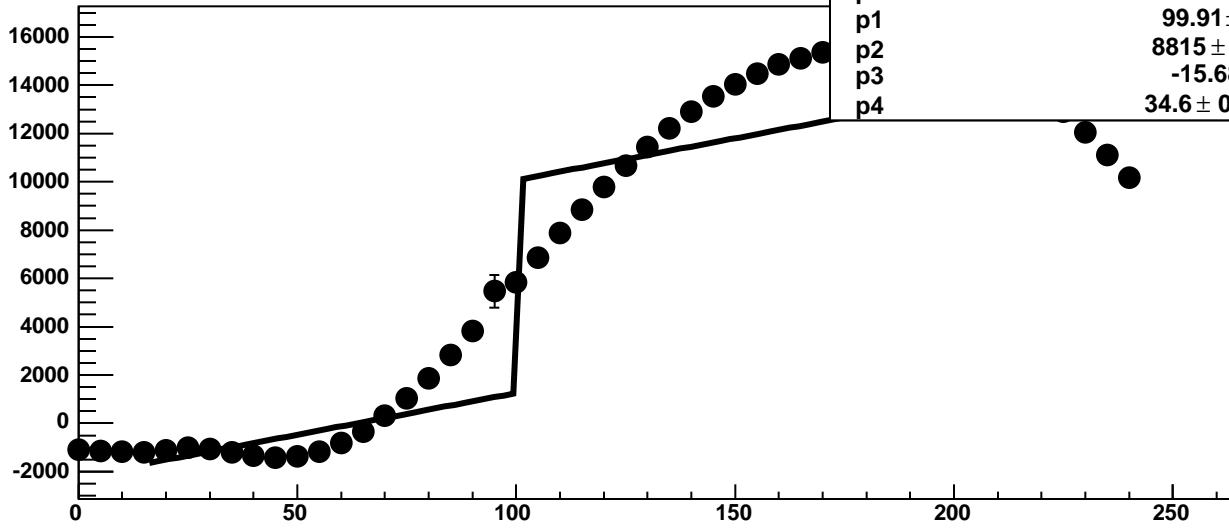
Chip 2, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

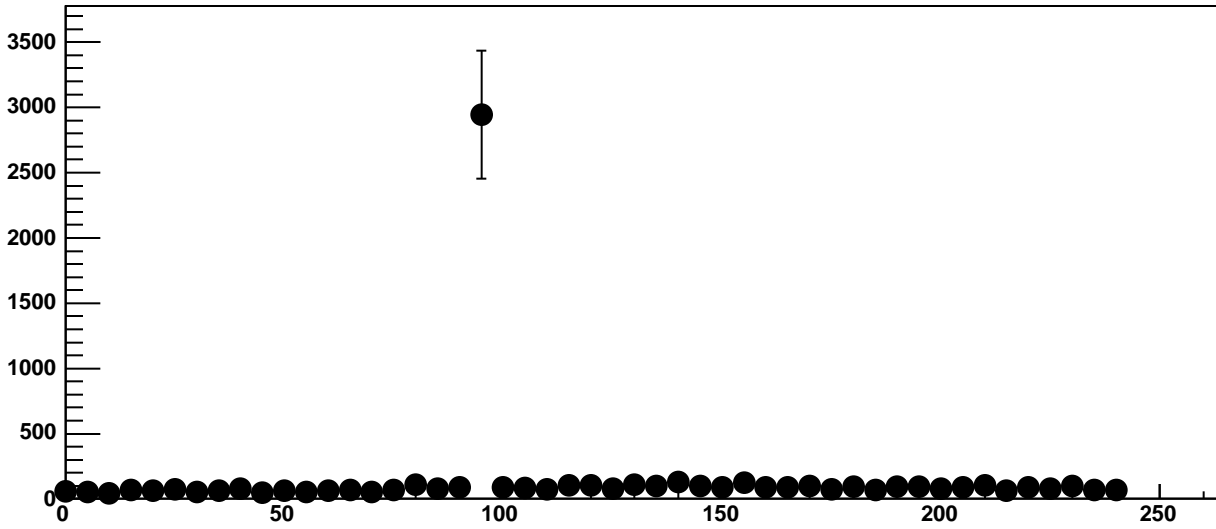


Chip 2, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

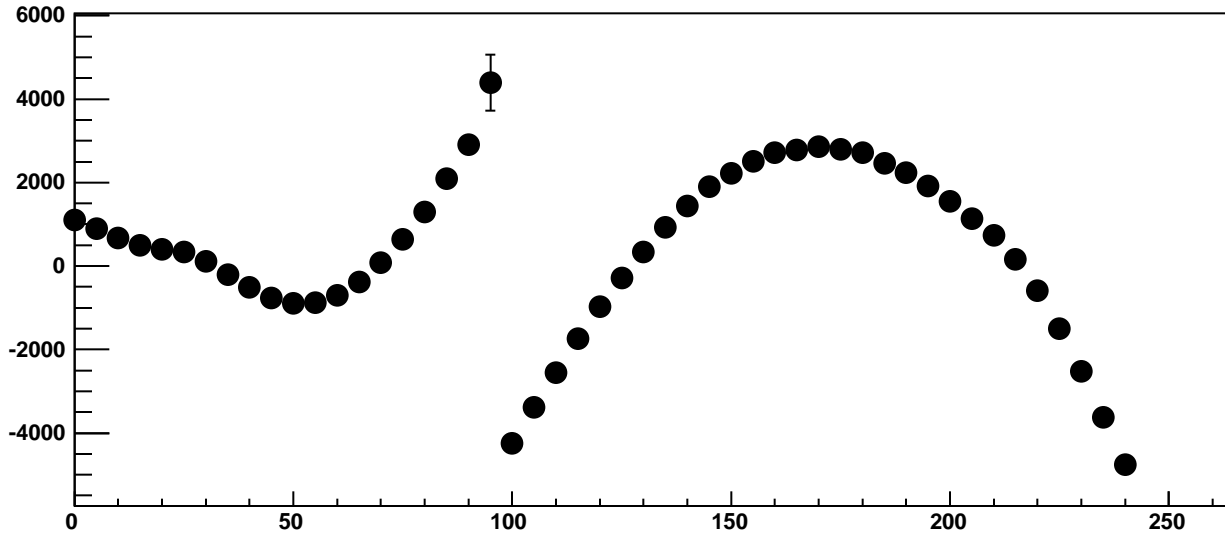


$\chi^2 / \text{ndf}$	4.997e+05 / 41
p0	1255 ± 0.0196
p1	99.91 ± 0.1912
p2	8815 ± 0.01954
p3	-15.68 ± 3.99
p4	34.6 ± 0.004526

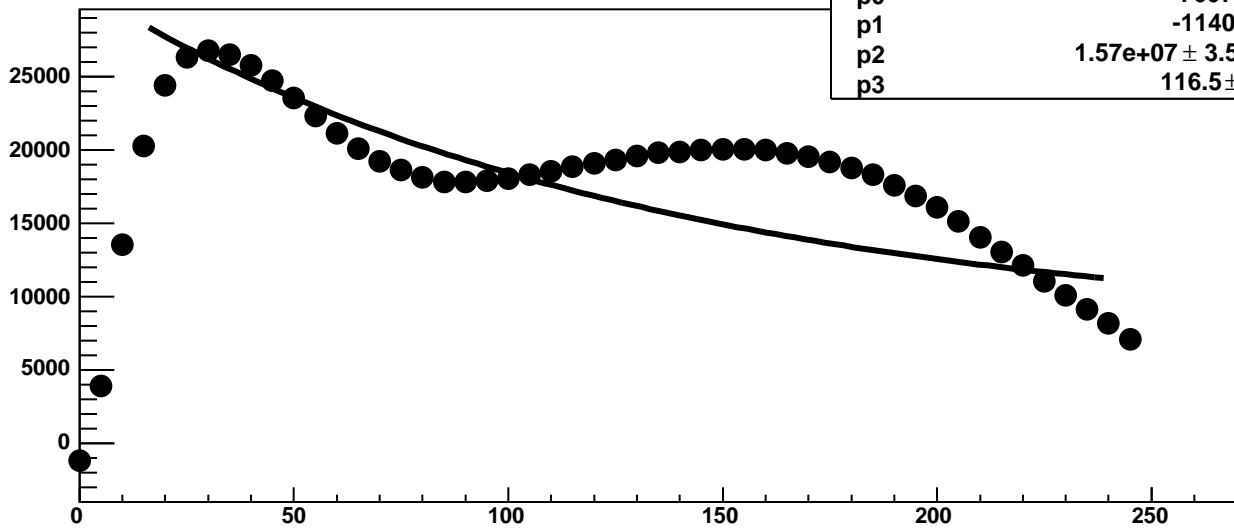
Chip 2, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

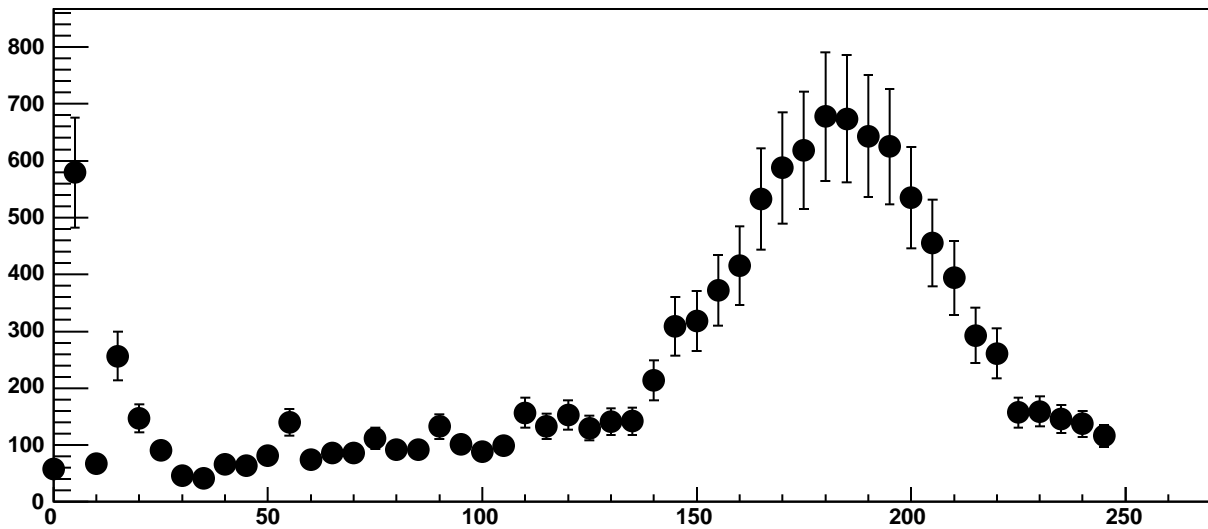


Chip 2, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold

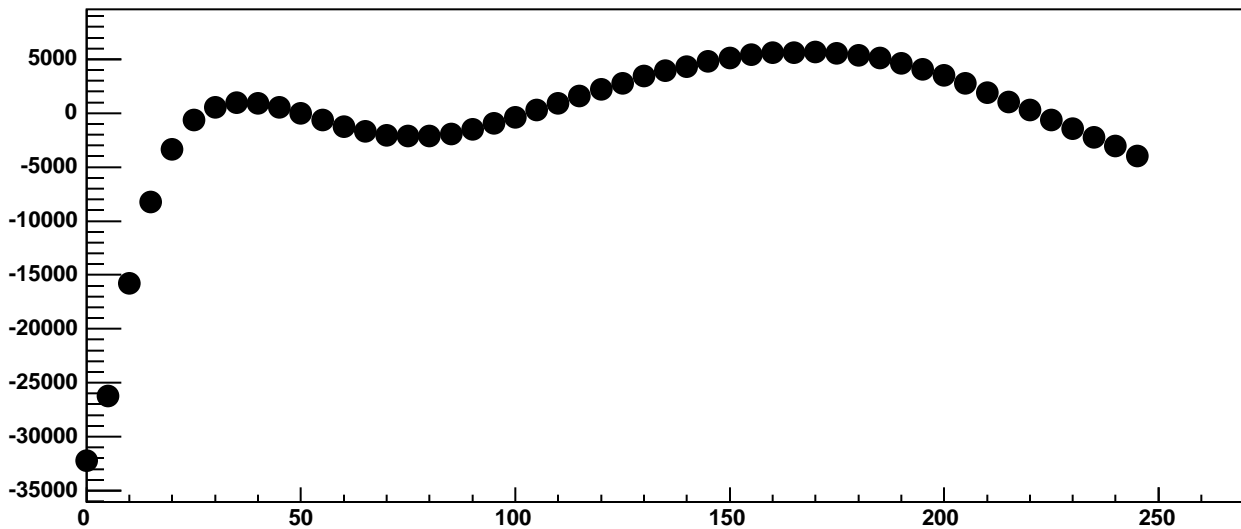


$\chi^2 / \text{ndf}$	1.955e+05 / 42
p0	7607 ± 51.55
p1	-1140 ± 6.493
p2	1.57e+07 ± 3.541e+05
p3	116.5 ± 0.5364

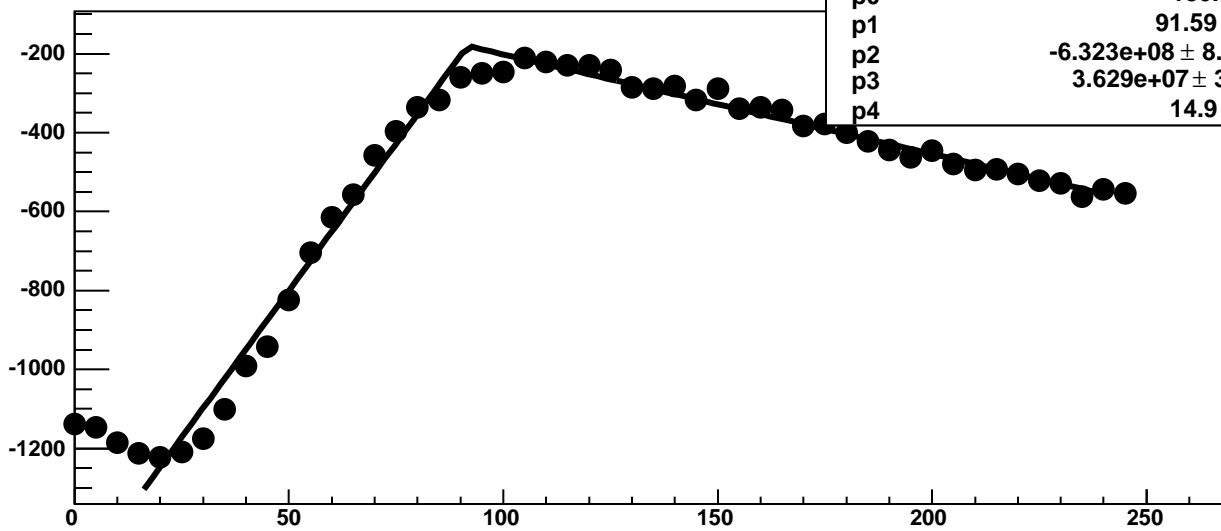
Chip 2, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold

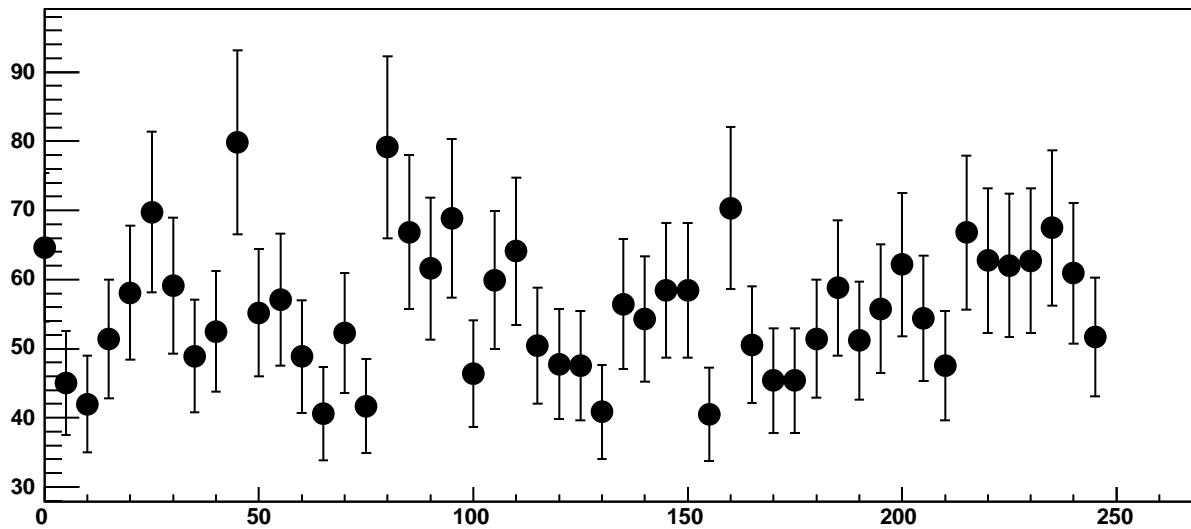


Chip 2, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

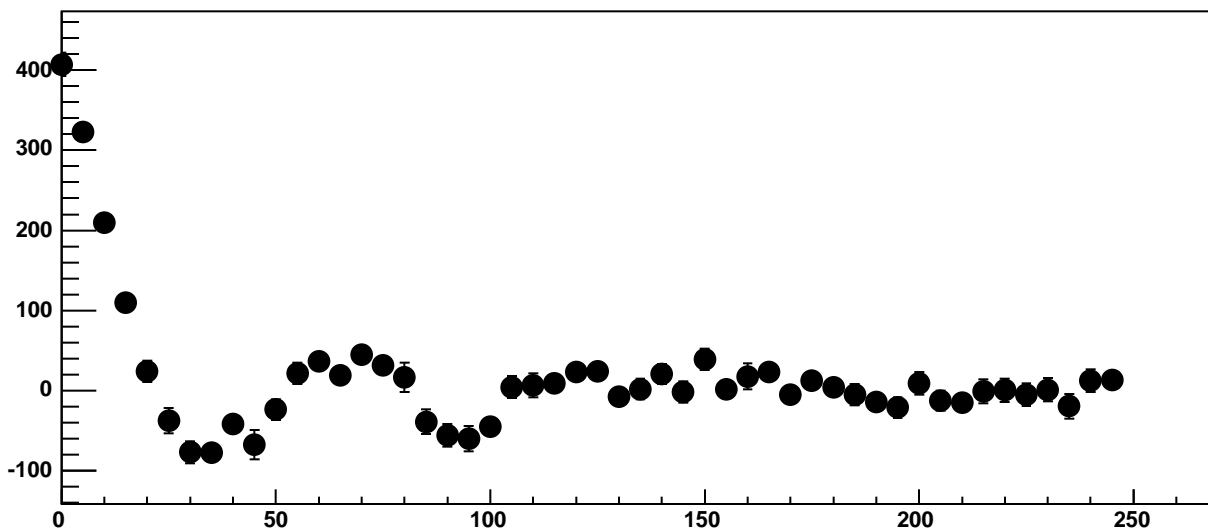


$\chi^2 / \text{ndf}$	341.8 / 41
p0	$-180.3 \pm 4.021$
p1	$91.59 \pm 0.4467$
p2	$-6.323\text{e}+08 \pm 8.296\text{e}+06$
p3	$3.629\text{e}+07 \pm 3.39\text{e}+05$
p4	$14.9 \pm 0.1423$

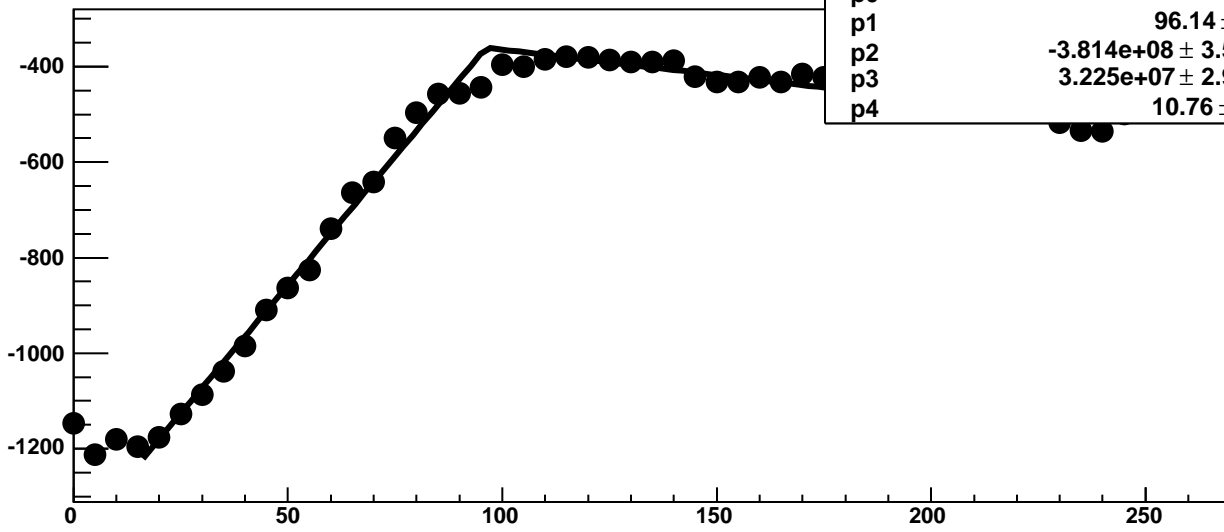
Chip 2, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold

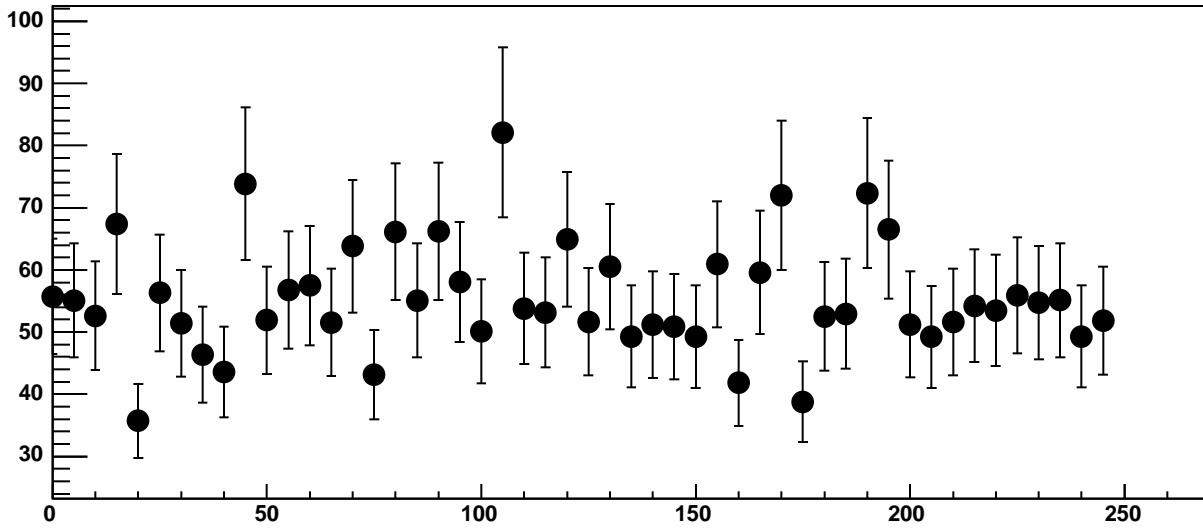


Chip 2, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

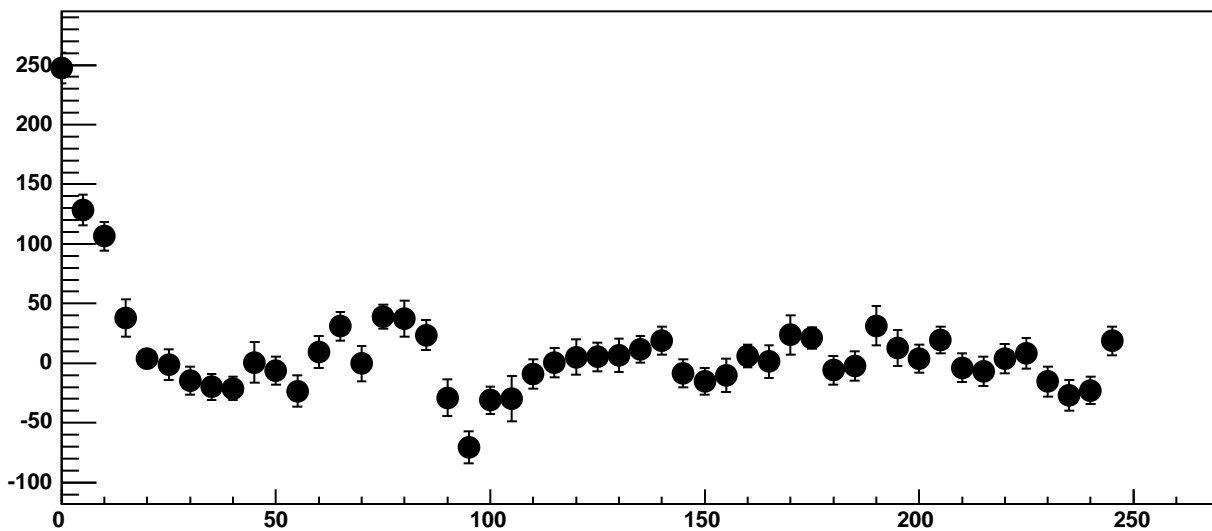


$\chi^2 / \text{ndf}$	127.2 / 41
p0	$-360.3 \pm 4.373$
p1	$96.14 \pm 0.6503$
p2	$-3.814\text{e}+08 \pm 3.563\text{e}+07$
p3	$3.225\text{e}+07 \pm 2.948\text{e}+06$
p4	$10.76 \pm 0.1206$

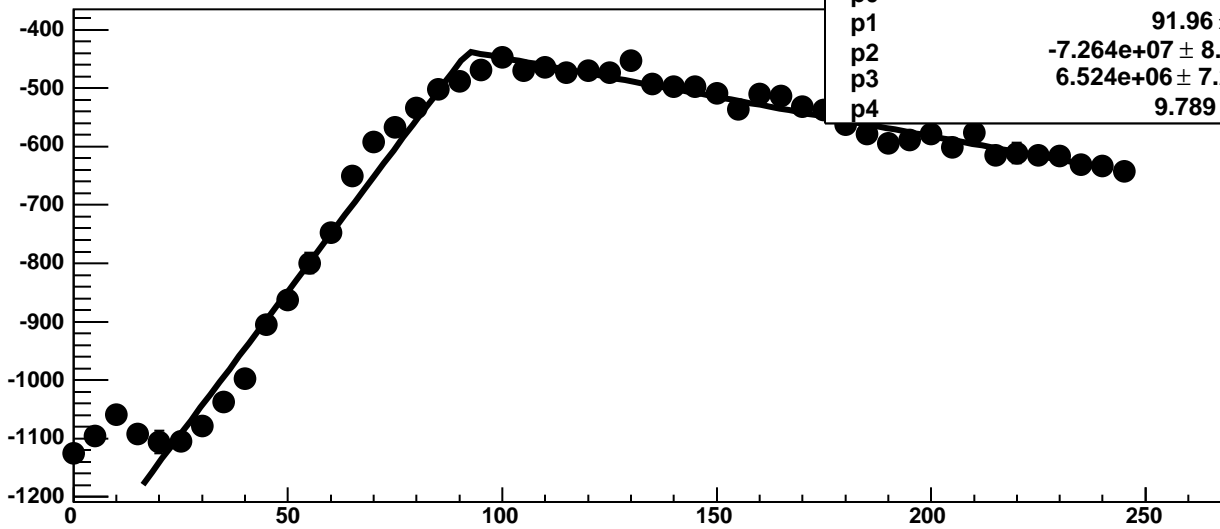
Chip 2, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

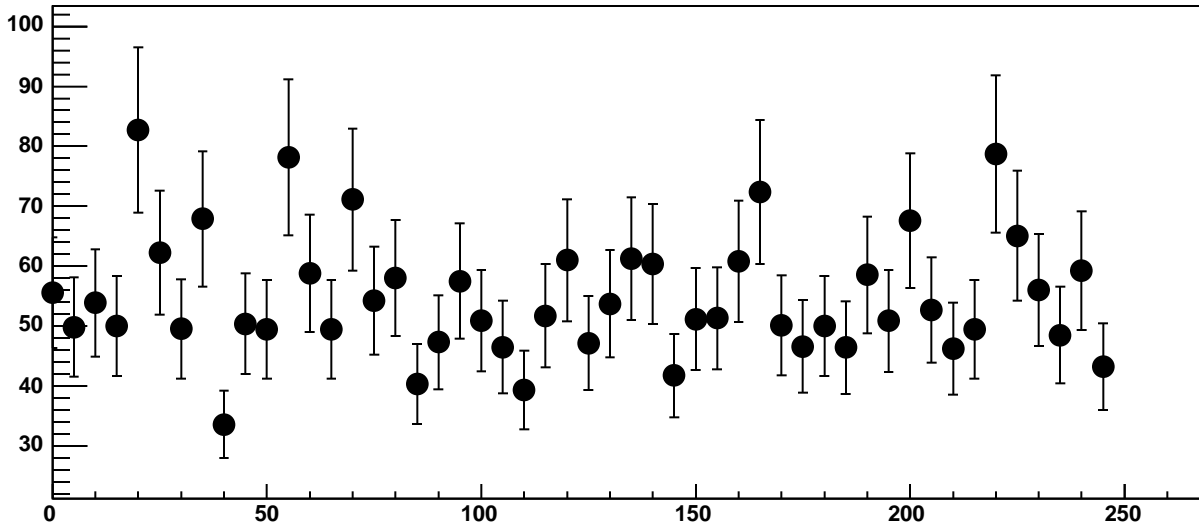


Chip 2, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

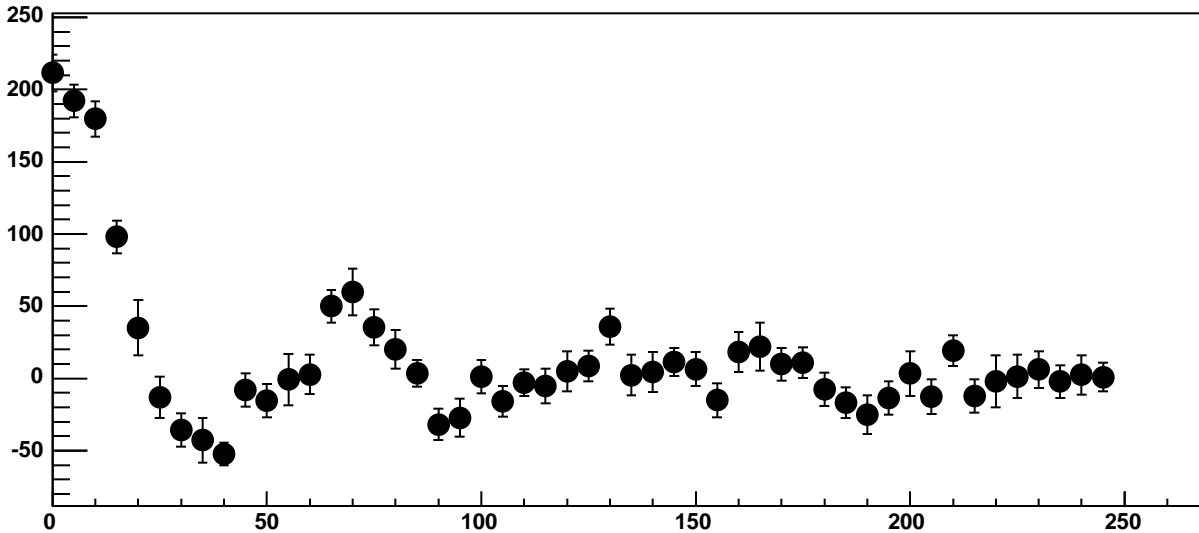


$\chi^2 / \text{ndf}$	233.7 / 41
p0	-436.9 ± 3.841
p1	91.96 ± 0.6446
p2	-7.264e+07 ± 8.108e+06
p3	6.524e+06 ± 7.257e+05
p4	9.789 ± 0.1293

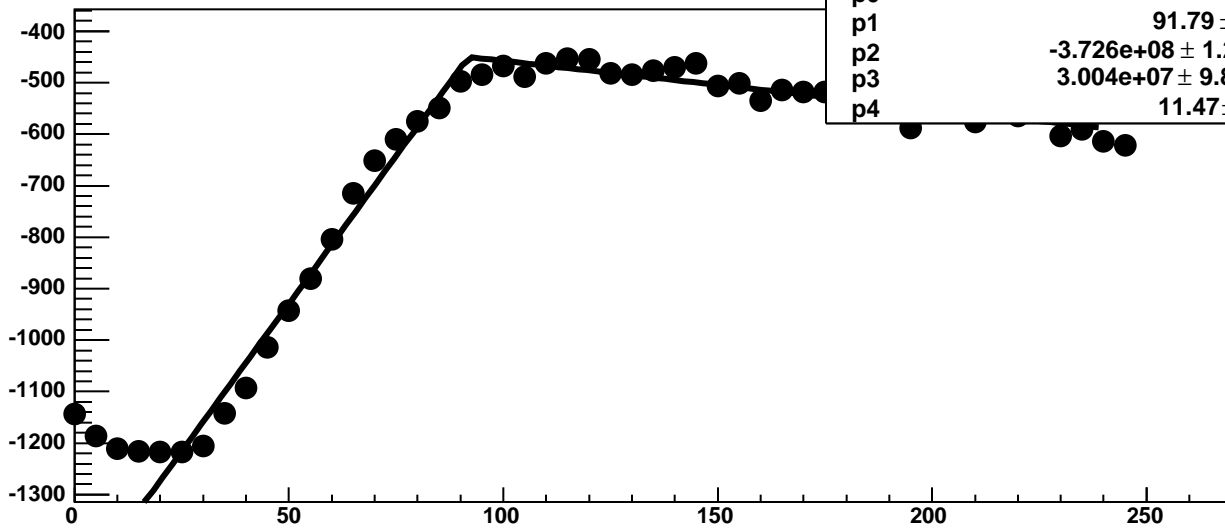
Chip 2, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold

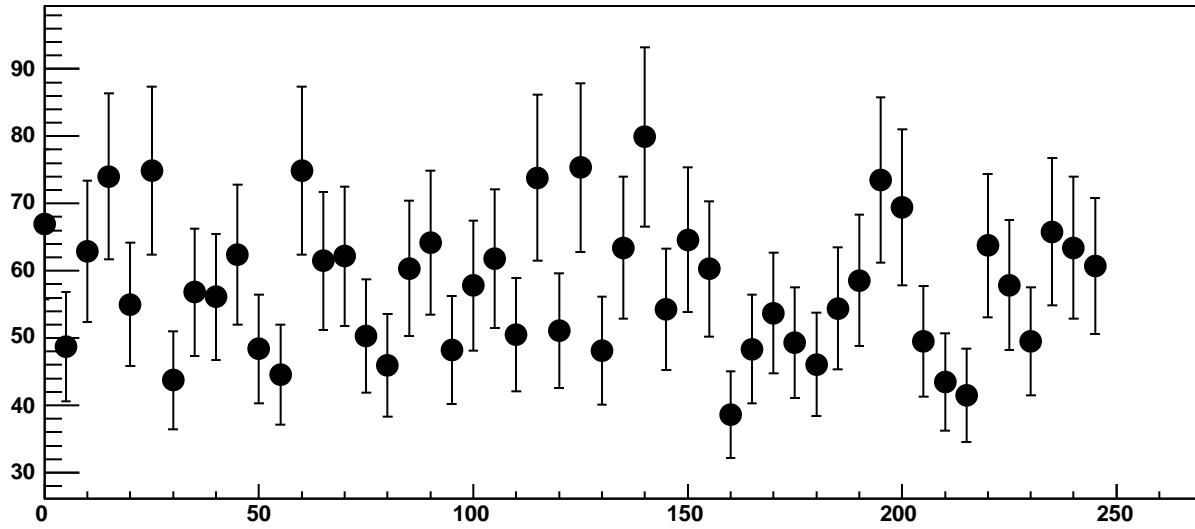


Chip 2, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

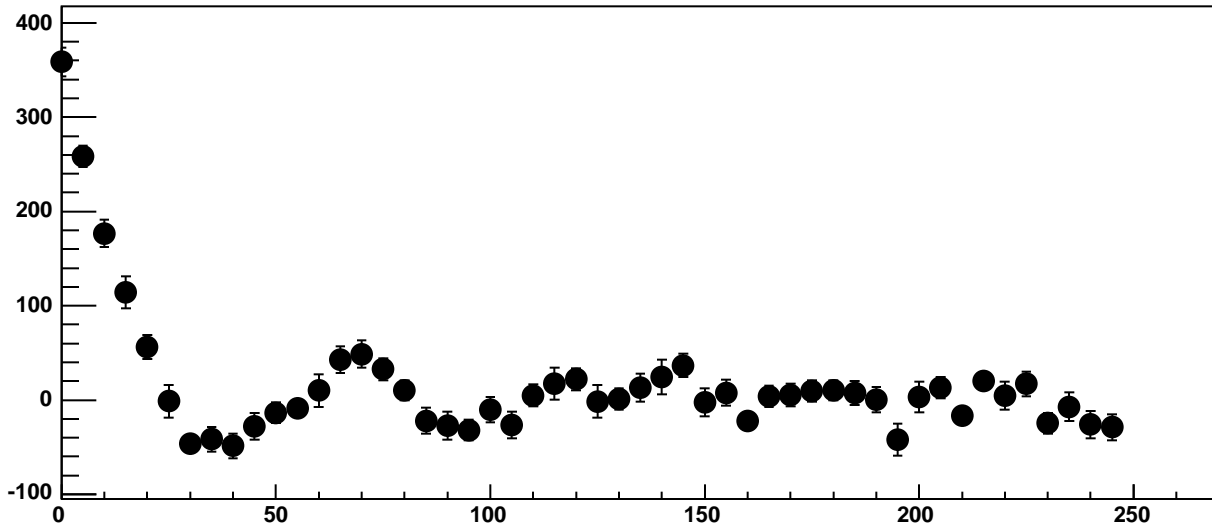


$\chi^2 / \text{ndf}$	215.1 / 41
p0	-449.8 ± 4.416
p1	91.79 ± 0.6416
p2	-3.726e+08 ± 1.298e+07
p3	3.004e+07 ± 9.854e+05
p4	11.47 ± 0.1449

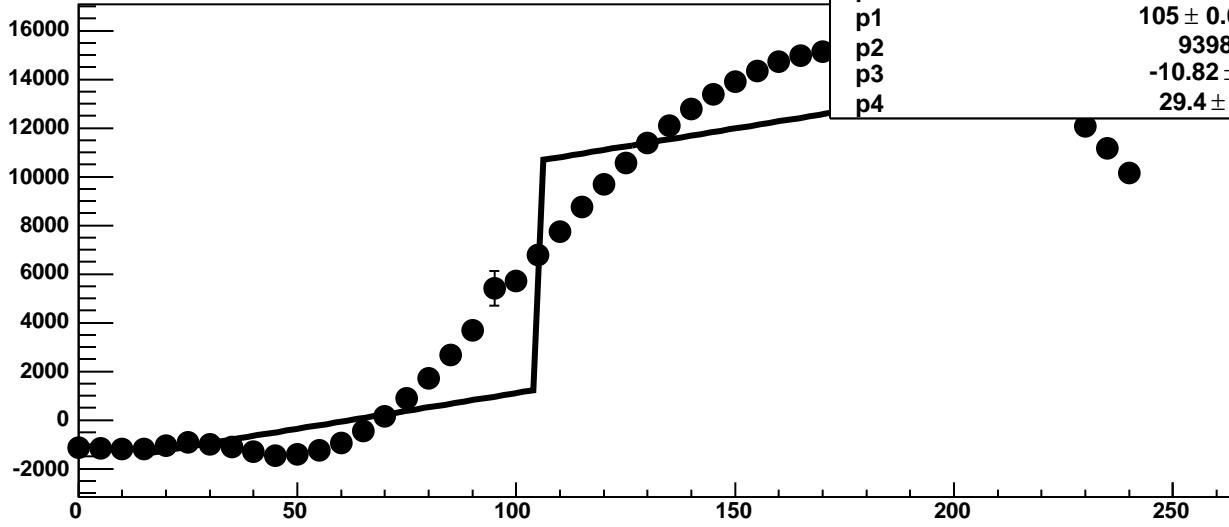
Chip 2, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

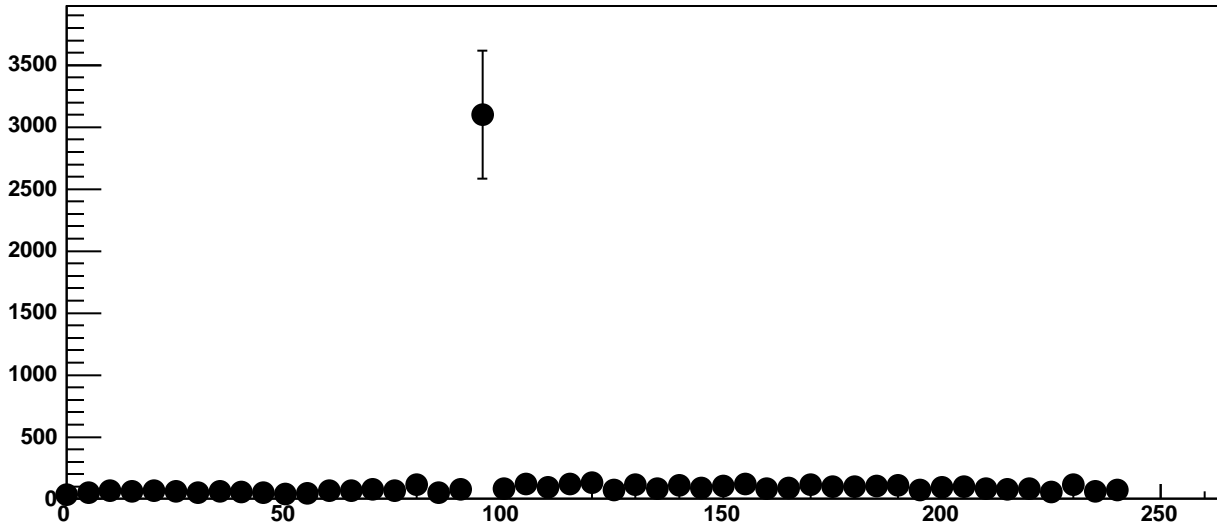


Chip 2, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

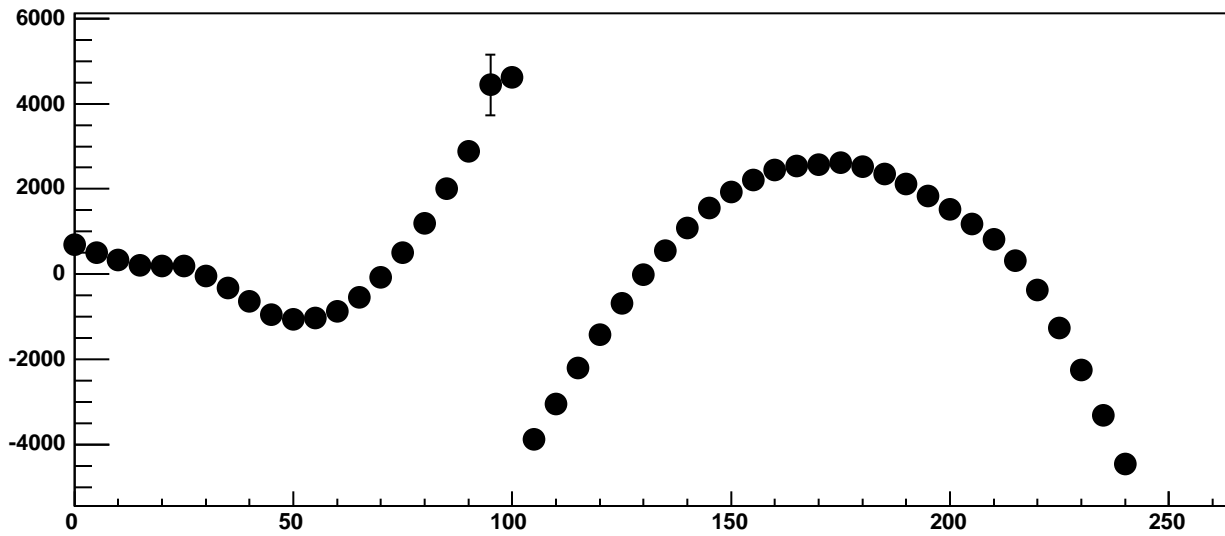


$\chi^2 / \text{ndf}$	4.715e+05 / 41
p0	1259 ± 5.869
p1	105 ± 0.0003365
p2	9398 ± 12.38
p3	-10.82 ± 0.1964
p4	29.4 ± 0.08078

Chip 2, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

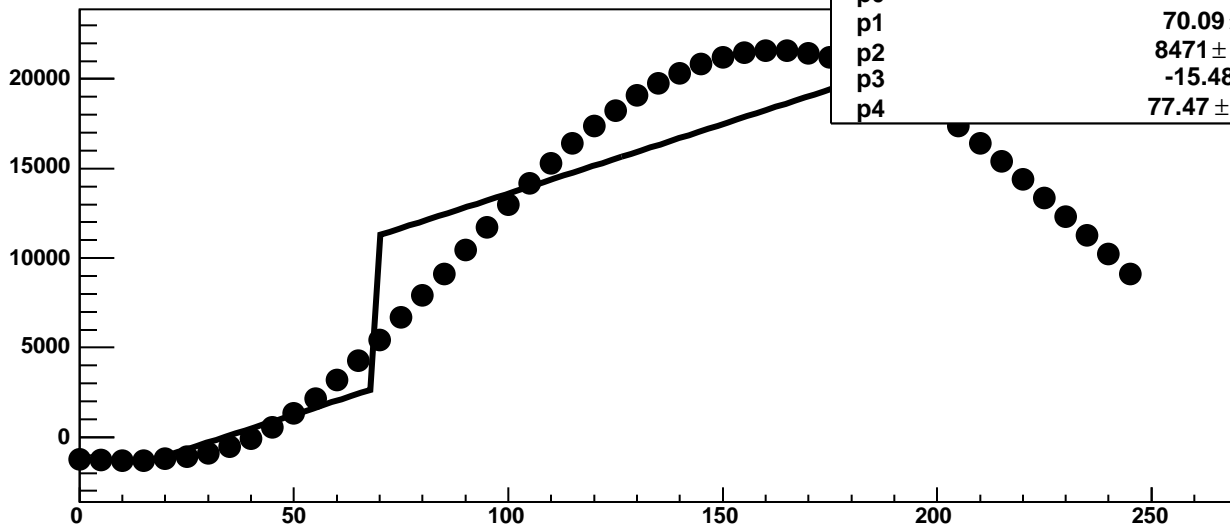


Chip 2, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



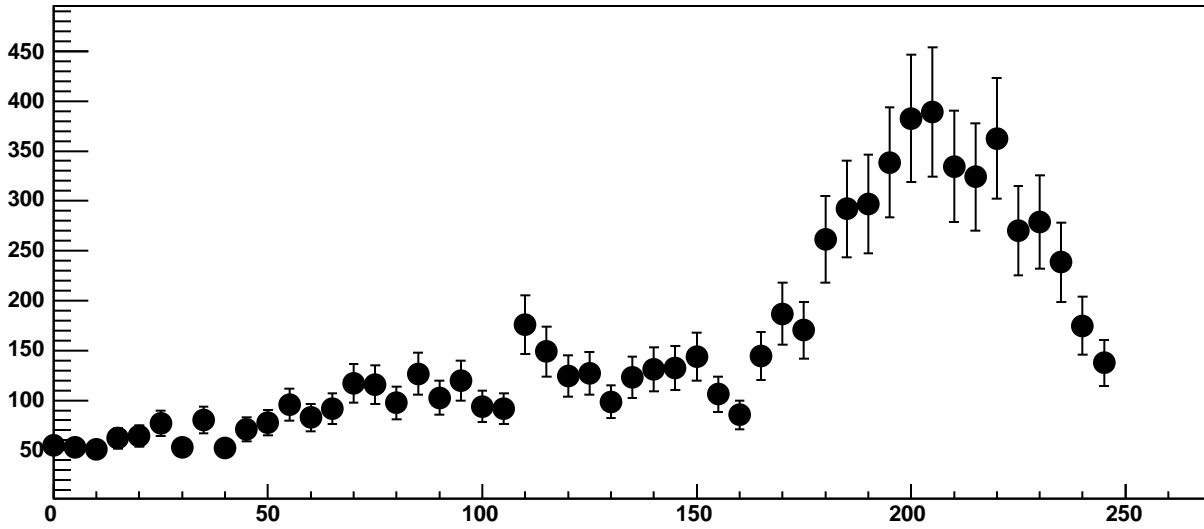


Chip 2, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

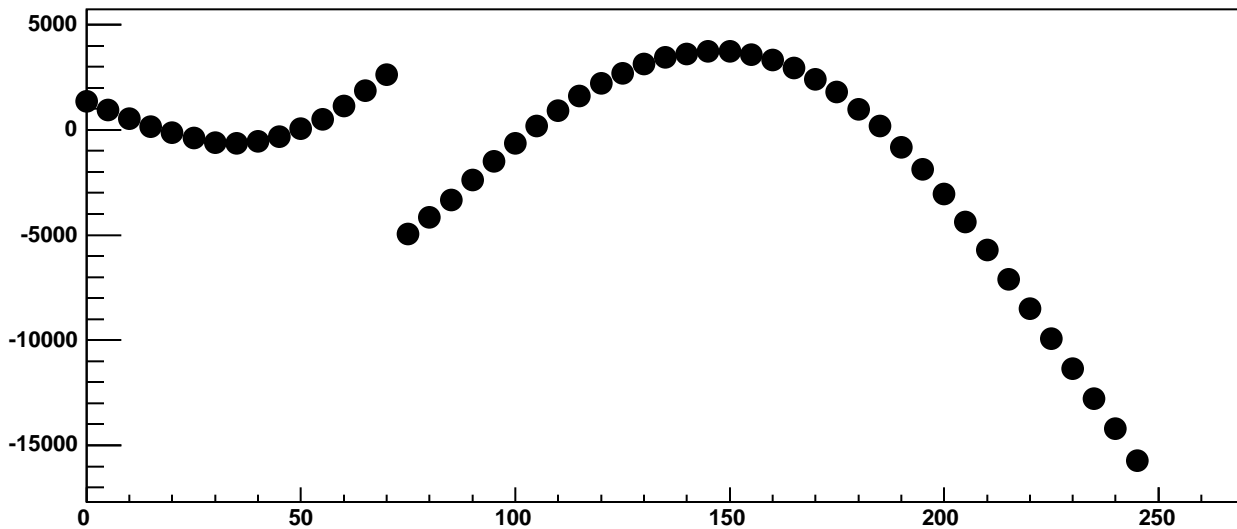


$\chi^2 / \text{ndf}$	5.495e+05 / 41
p0	2817 ± 0.1024
p1	70.09 ± 0.2611
p2	8471 ± 0.09736
p3	-15.48 ± 8.203
p4	77.47 ± 0.07601

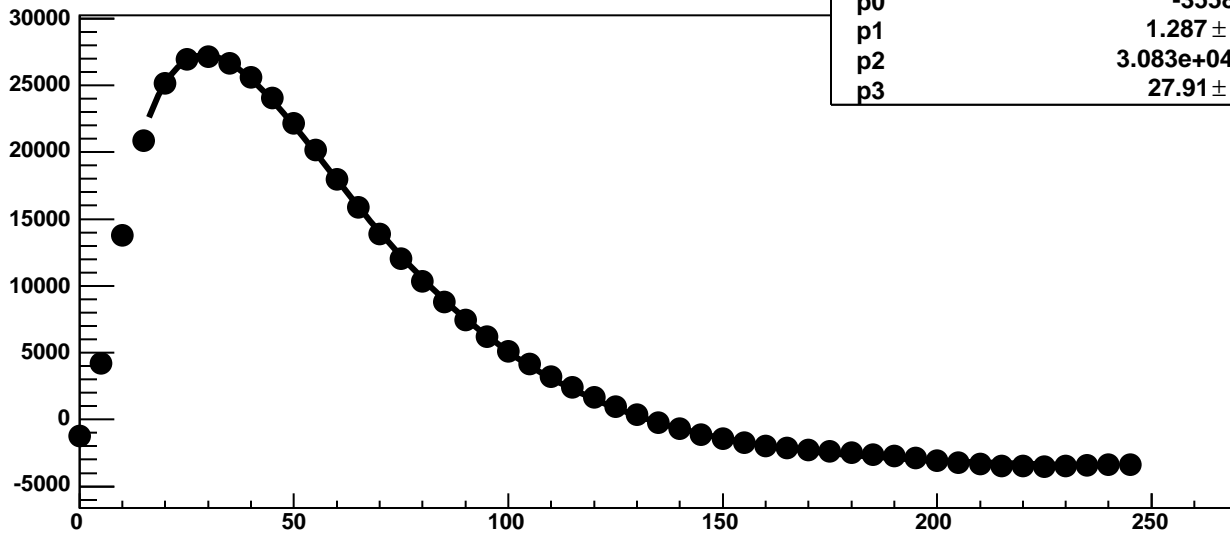
Chip 2, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

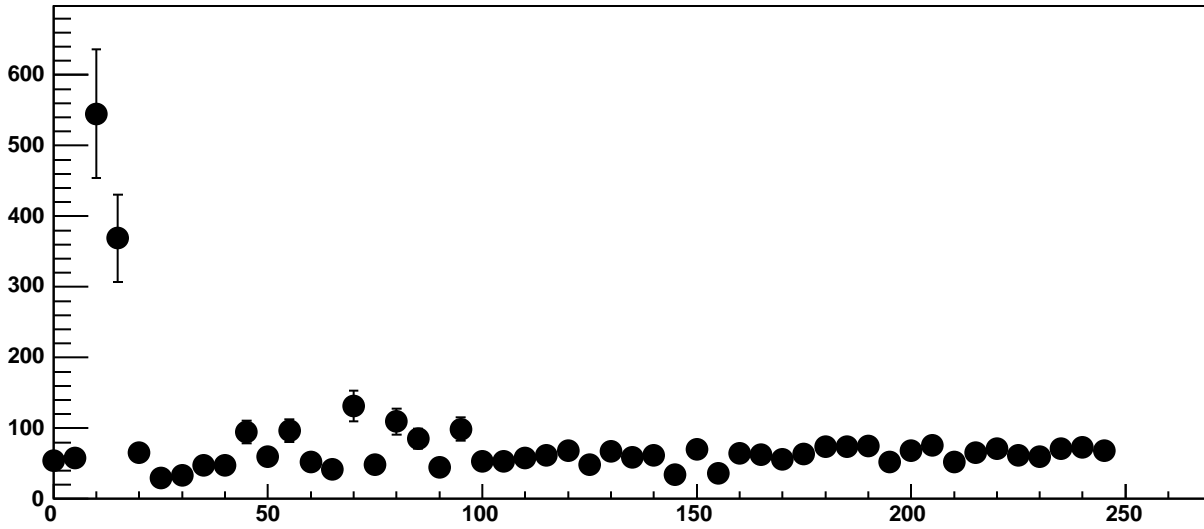


Chip 2, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold

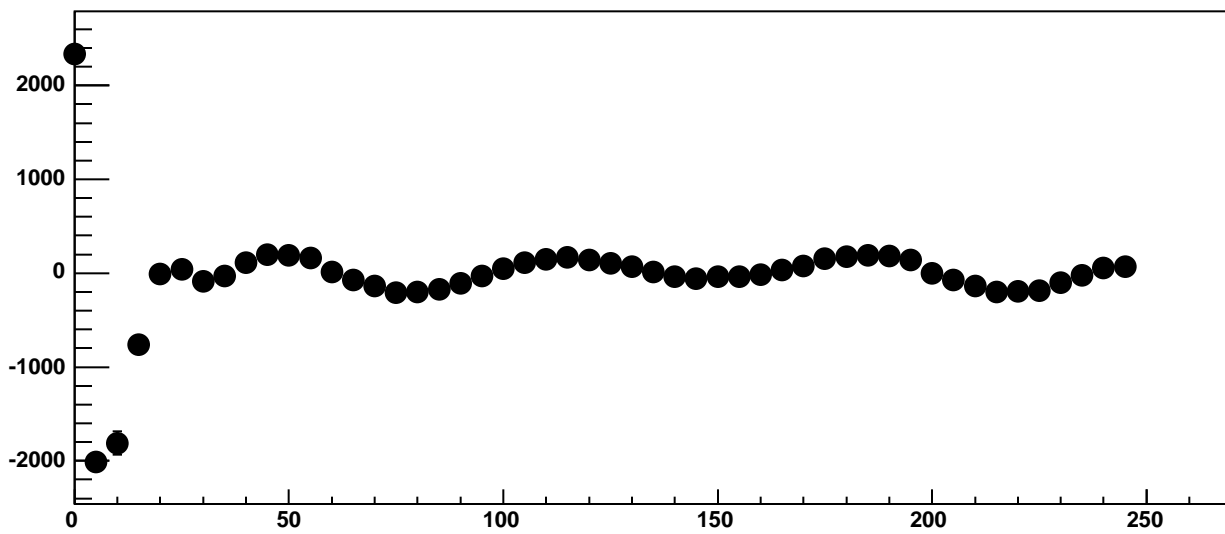


$\chi^2 / \text{ndf}$	3360 / 42
p0	-3558 $\pm$ 4.025
p1	1.287 $\pm$ 0.02529
p2	3.083e+04 $\pm$ 5.148
p3	27.91 $\pm$ 0.01313

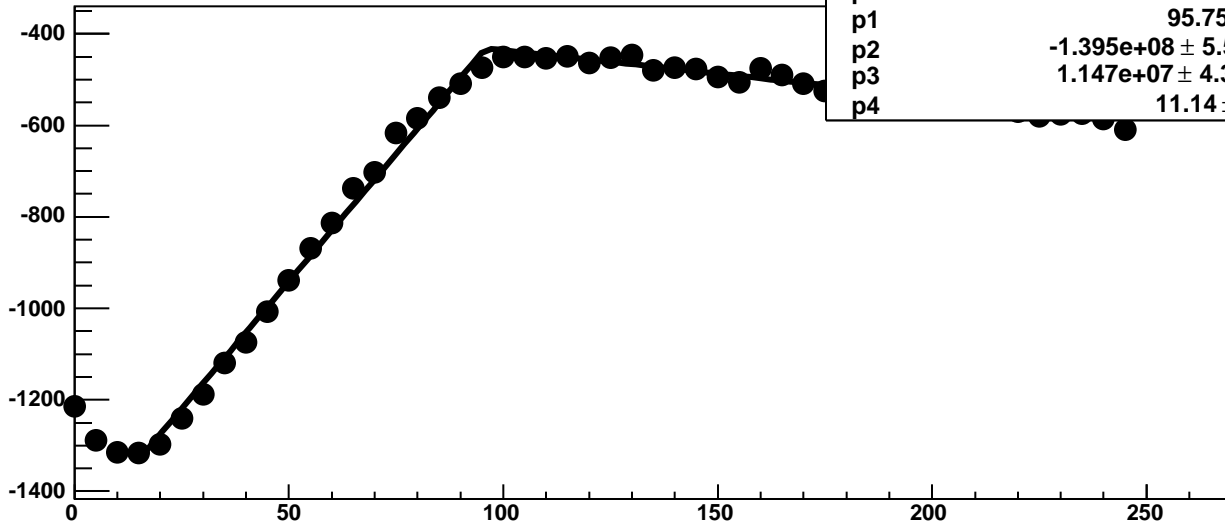
Chip 2, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold

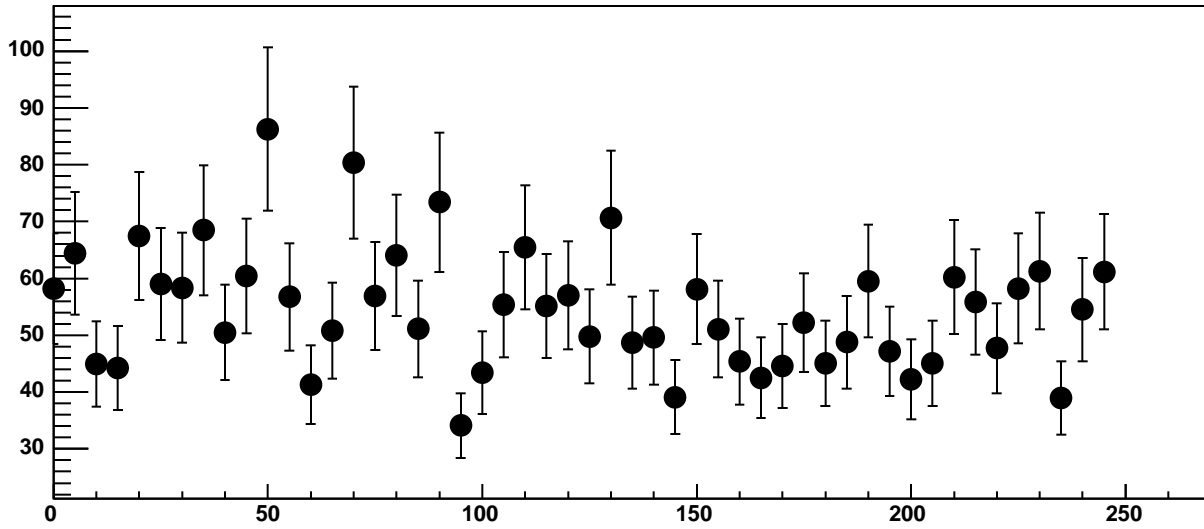


Chip 2, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

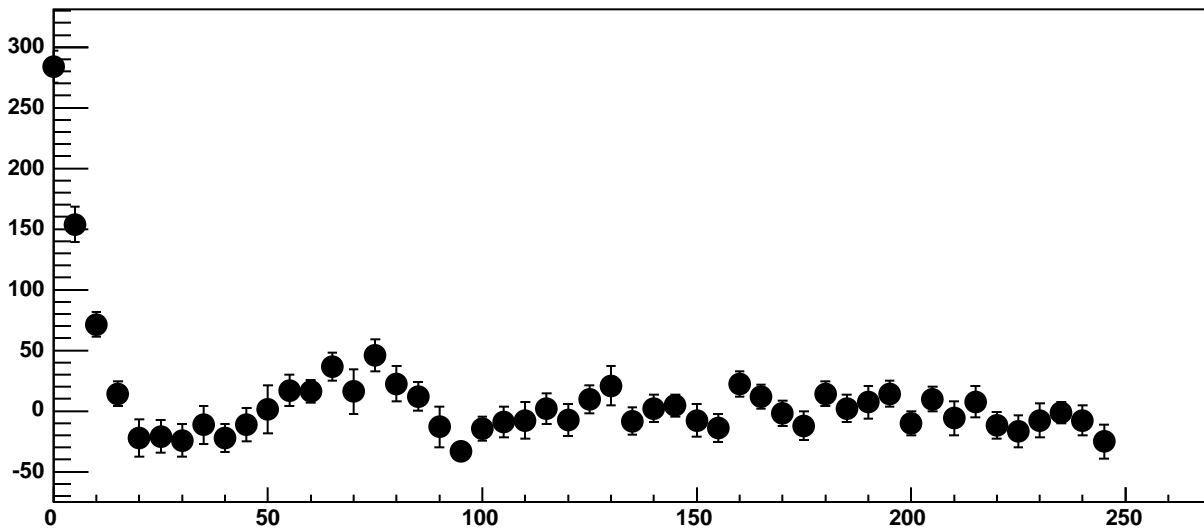


$\chi^2 / \text{ndf}$	89.52 / 41
p0	$-431.4 \pm 4.124$
p1	$95.75 \pm 0.569$
p2	$-1.395\text{e}+08 \pm 5.548\text{e}+06$
p3	$1.147\text{e}+07 \pm 4.375\text{e}+05$
p4	$11.14 \pm 0.1147$

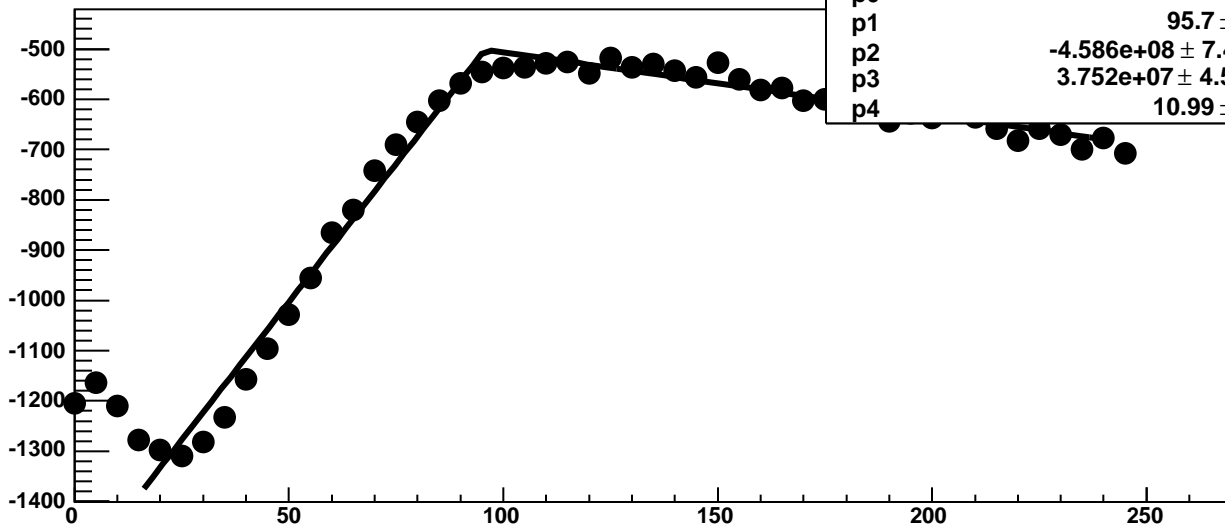
Chip 2, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

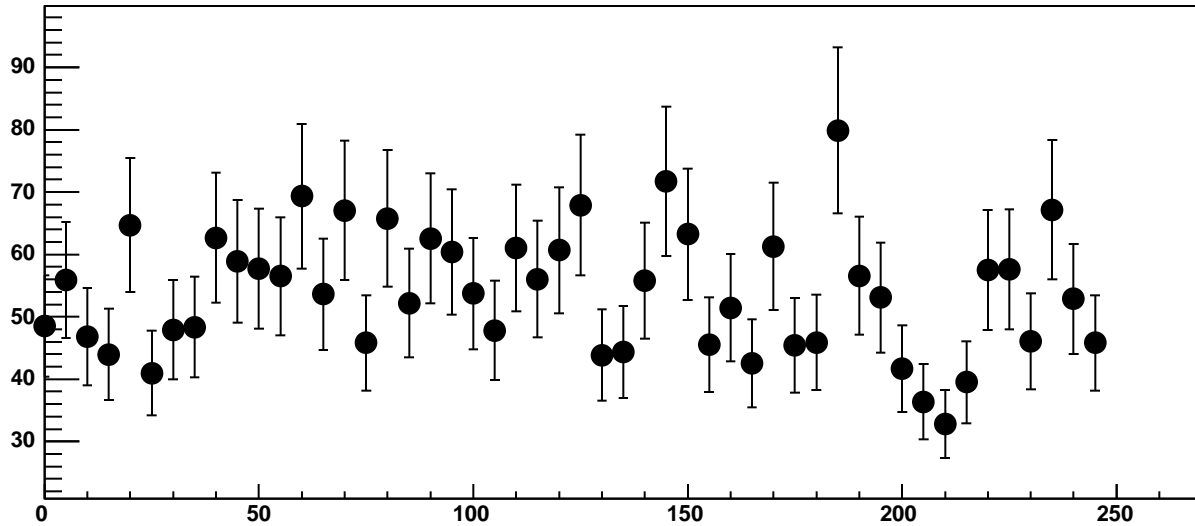


Chip 2, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

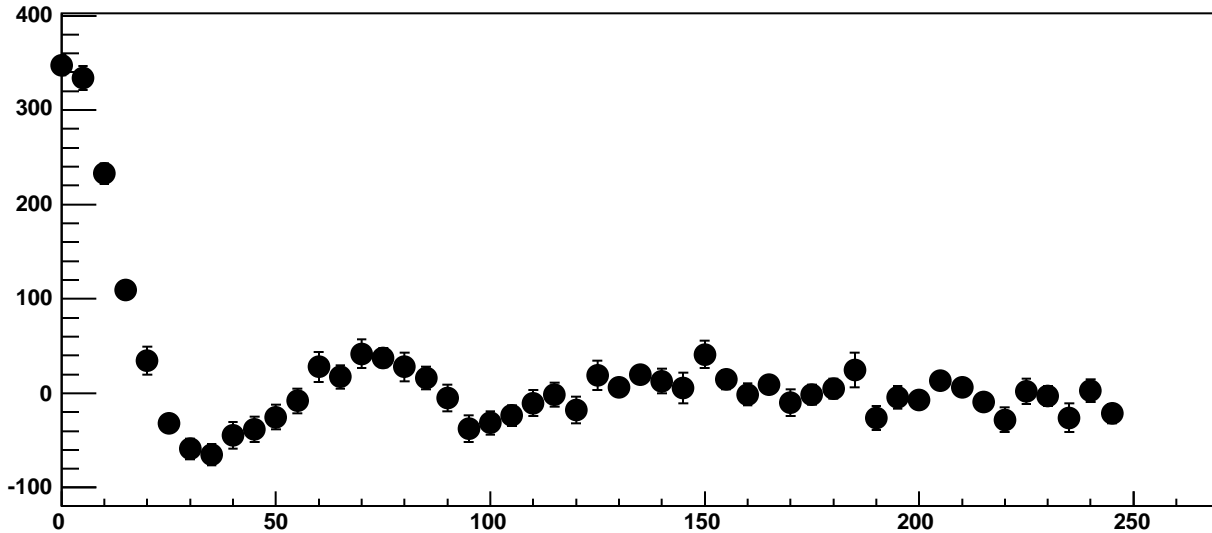


$\chi^2 / \text{ndf}$	307.8 / 41
p0	$-500.9 \pm 4.214$
p1	$95.7 \pm 0.6286$
p2	$-4.586\text{e}+08 \pm 7.401\text{e}+06$
p3	$3.752\text{e}+07 \pm 4.571\text{e}+05$
p4	$10.99 \pm 0.1204$

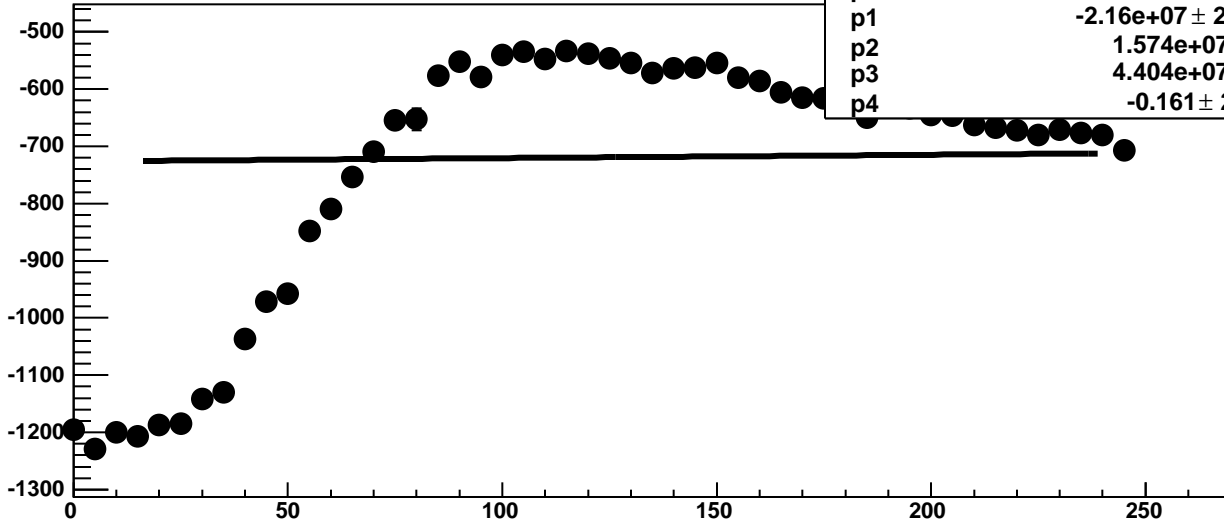
Chip 2, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

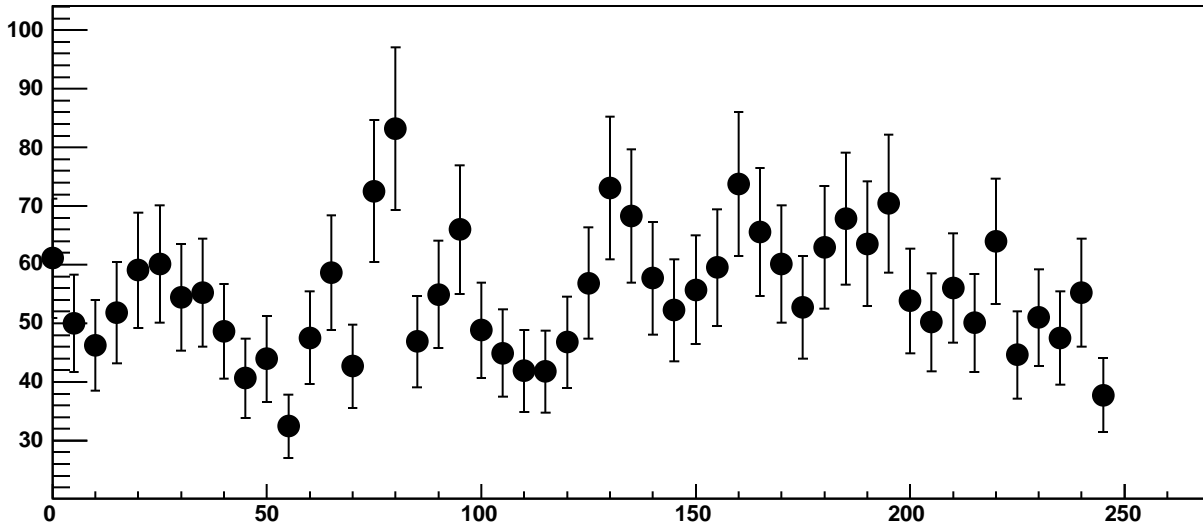


Chip 2, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold

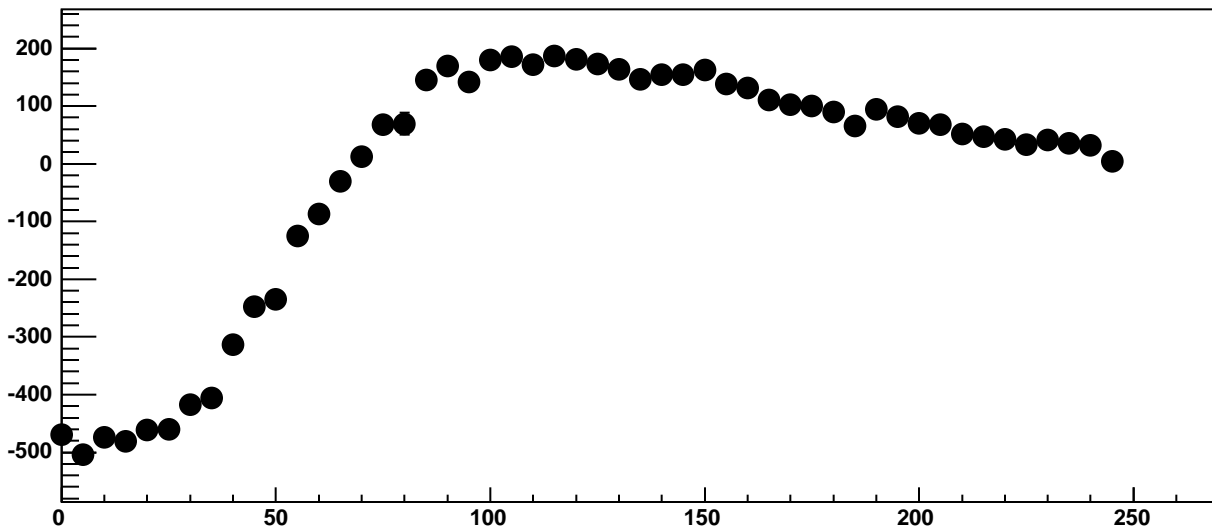


$\chi^2 / \text{ndf}$	1.193e+04 / 41
p0	-2.624e+06 $\pm$ 443.5
p1	-2.16e+07 $\pm$ 2.03e+04
p2	1.574e+07 $\pm$ 1312
p3	4.404e+07 $\pm$ 4442
p4	-0.161 $\pm$ 2.92e-05

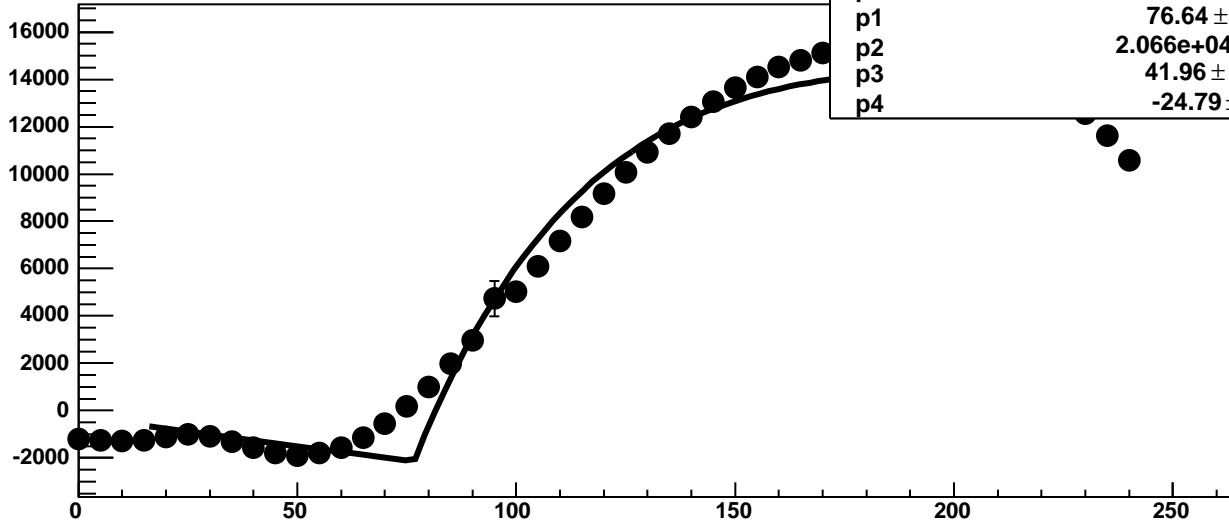
Chip 2, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold

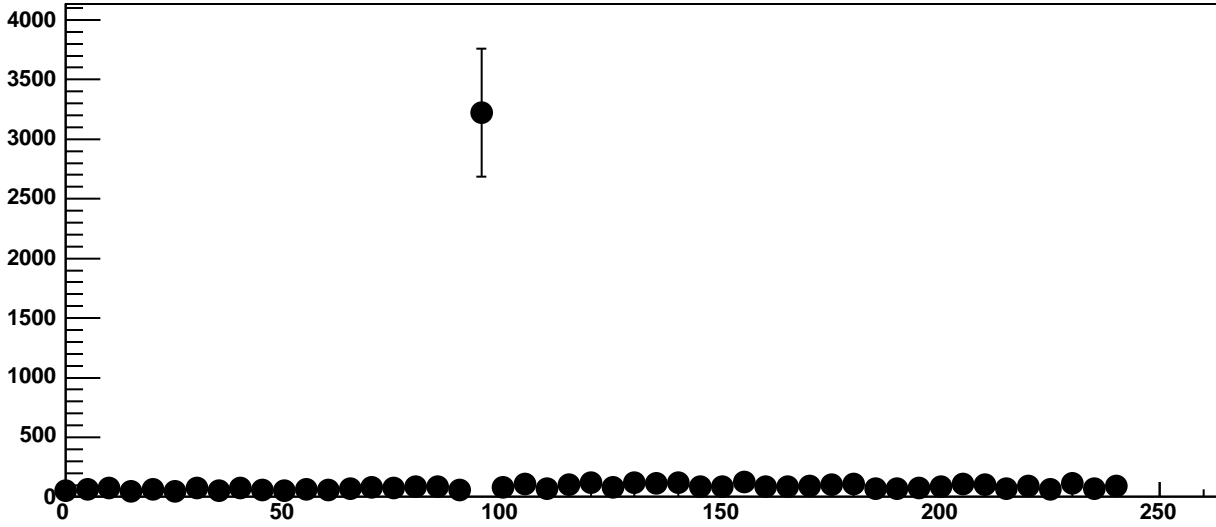


Chip 2, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

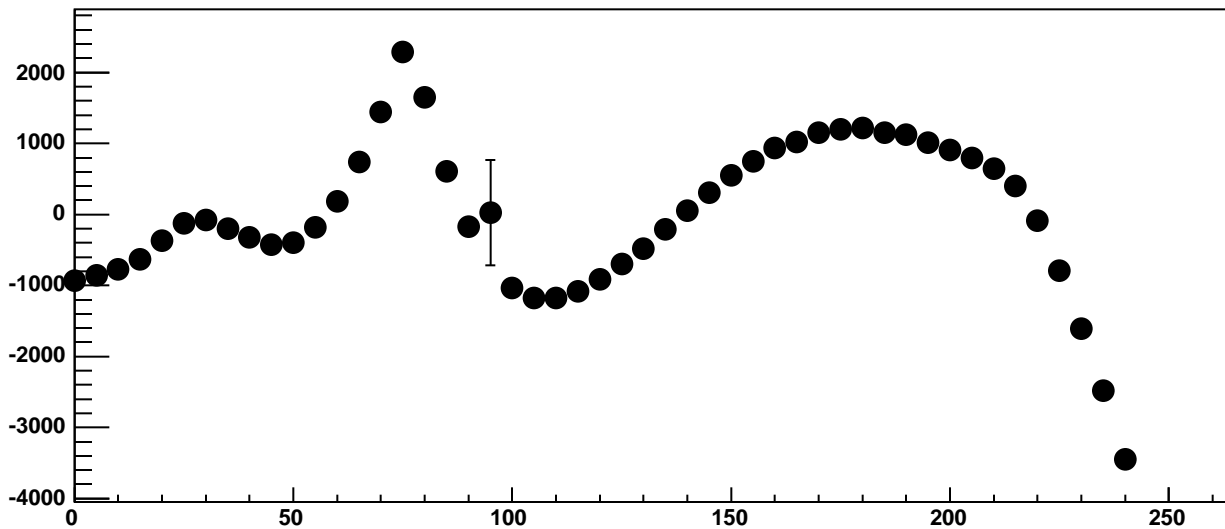


$\chi^2 / \text{ndf}$	1.467e+05 / 41
p0	-2160 ± 6.826
p1	76.64 ± 0.03401
p2	2.066e+04 ± 34.46
p3	41.96 ± 0.08793
p4	-24.79 ± 0.1722

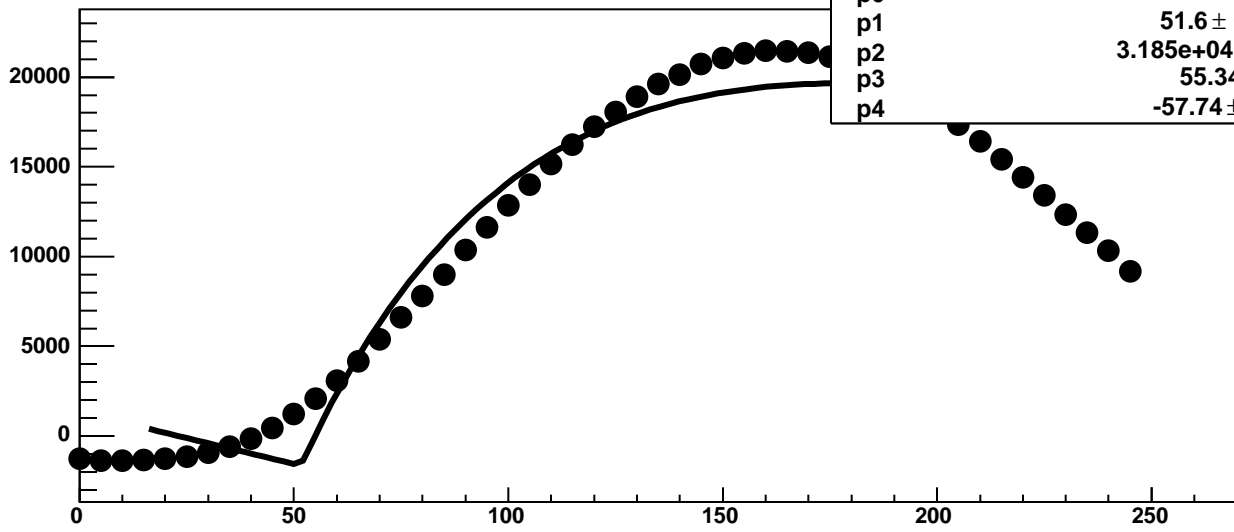
Chip 2, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

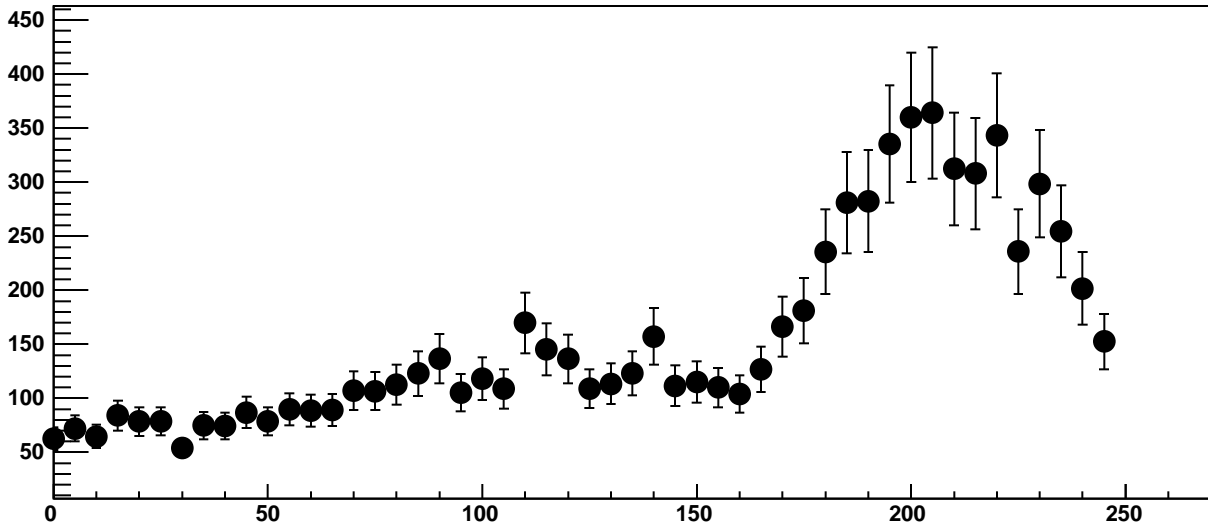


Chip 2, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

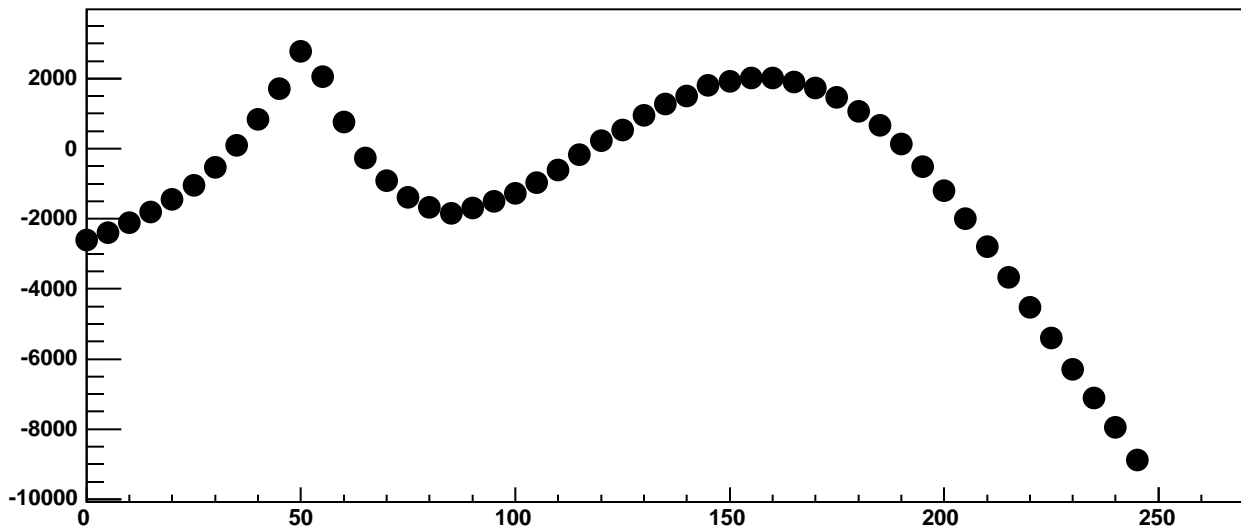


$\chi^2 / \text{ndf}$	1.983e+05 / 41
p0	-1651 ± 8.593
p1	51.6 ± 0.03098
p2	3.185e+04 ± 75.84
p3	55.34 ± 0.13
p4	-57.74 ± 0.3758

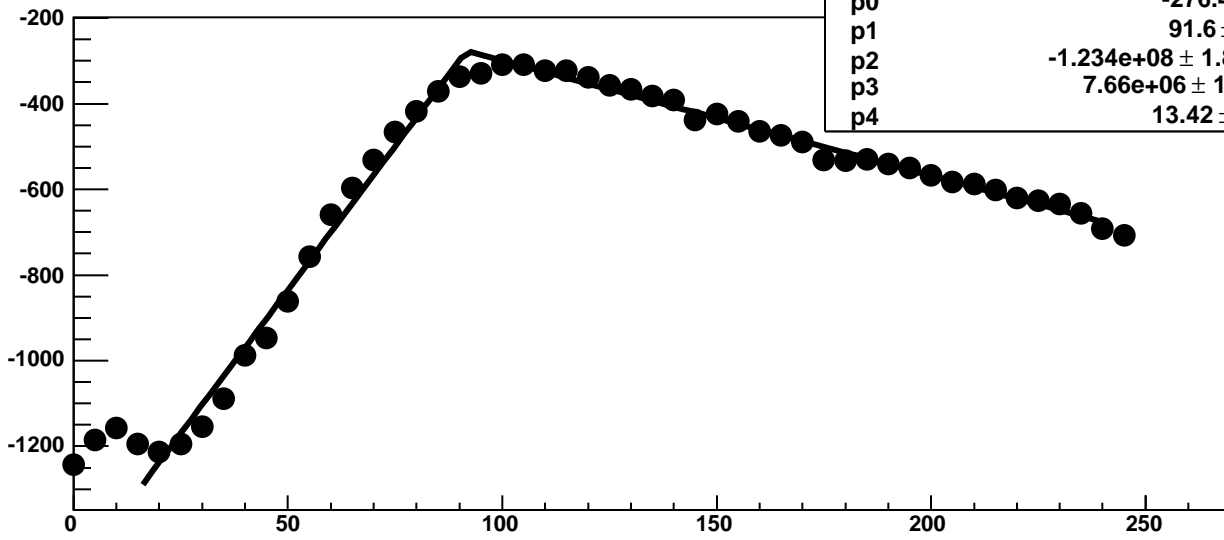
Chip 2, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



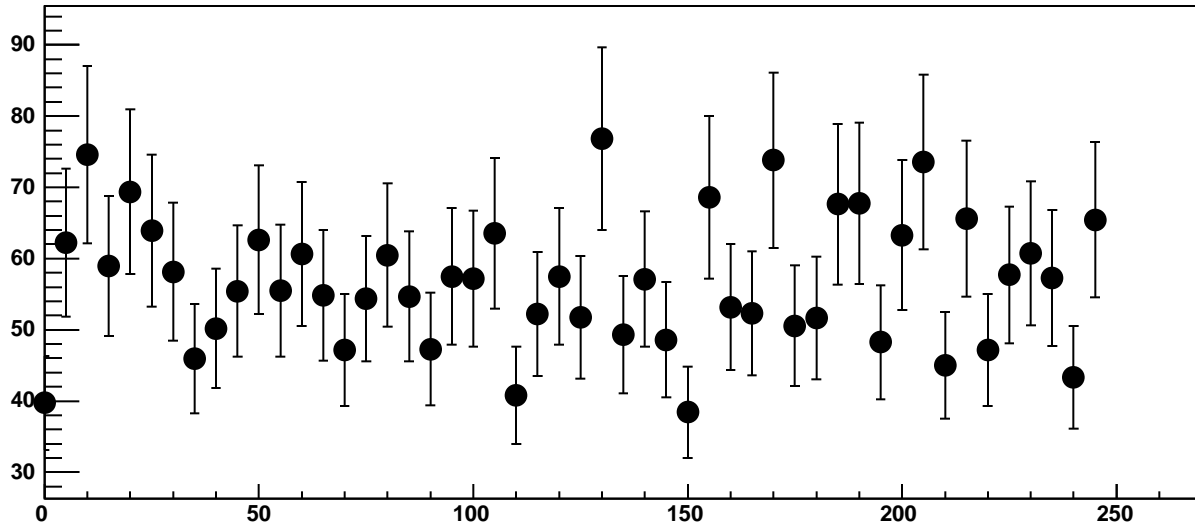
Chip 2, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



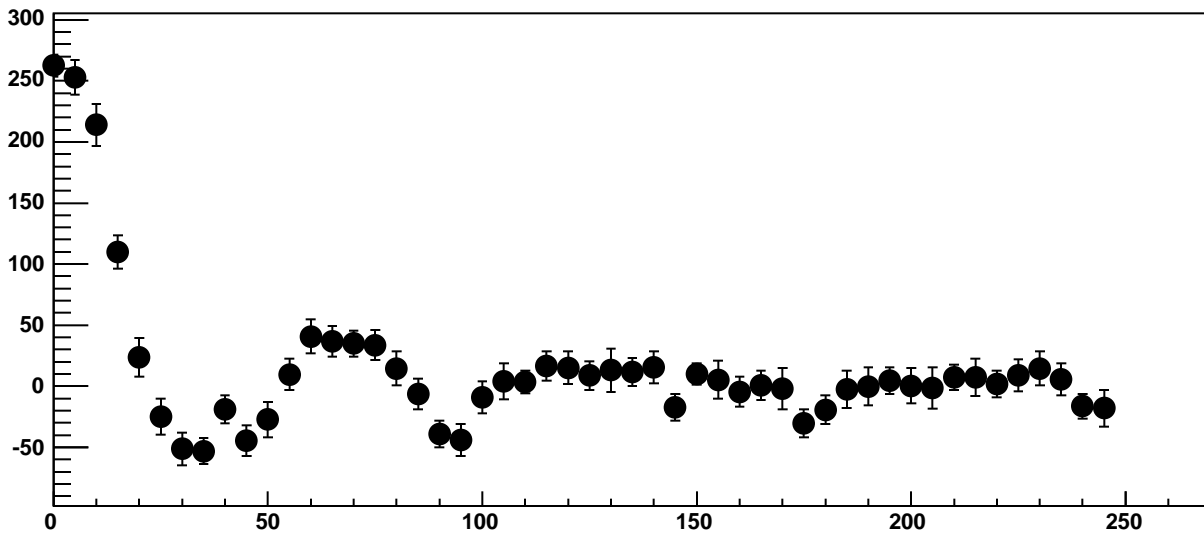
Chip 2, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 2, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

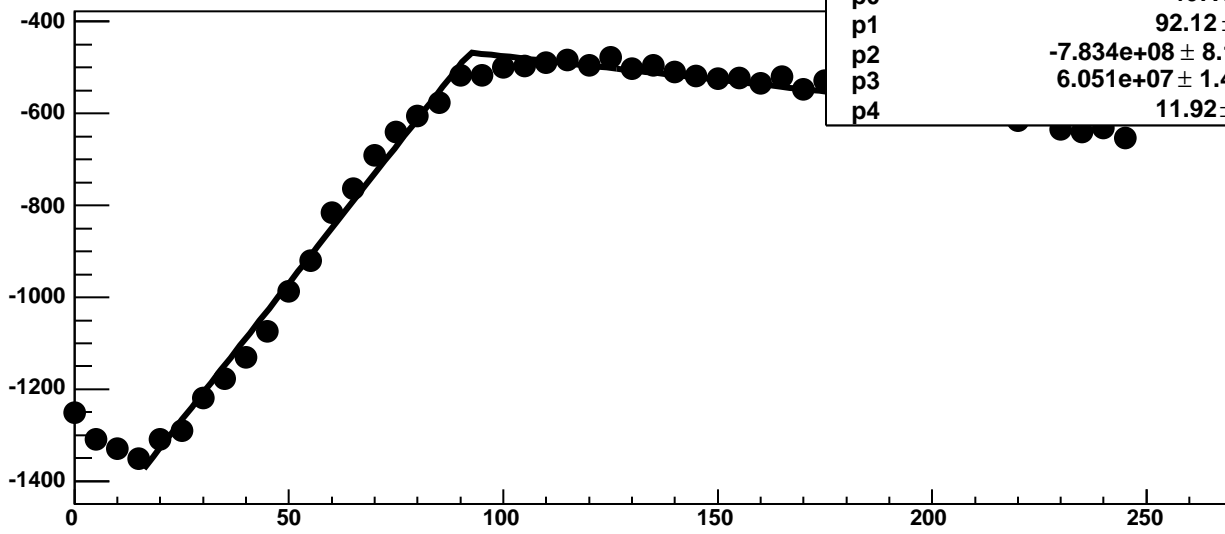


Chip 2, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold



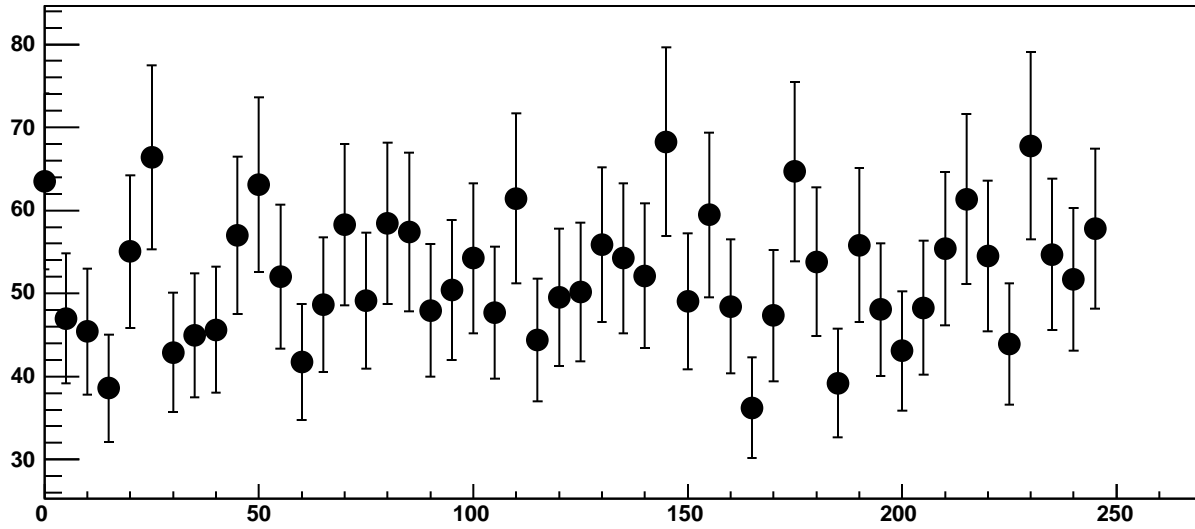


Chip 2, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

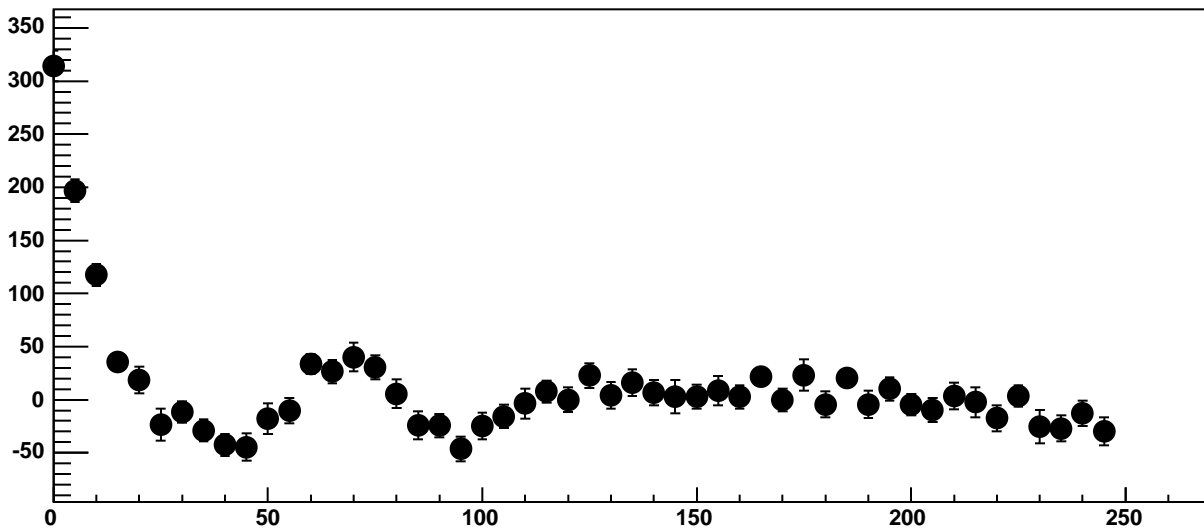


$\chi^2 / \text{ndf}$	159.1 / 41
p0	-467.1 ± 4.027
p1	92.12 ± 0.5639
p2	-7.834e+08 ± 8.162e+06
p3	6.051e+07 ± 1.425e+05
p4	11.92 ± 0.1226

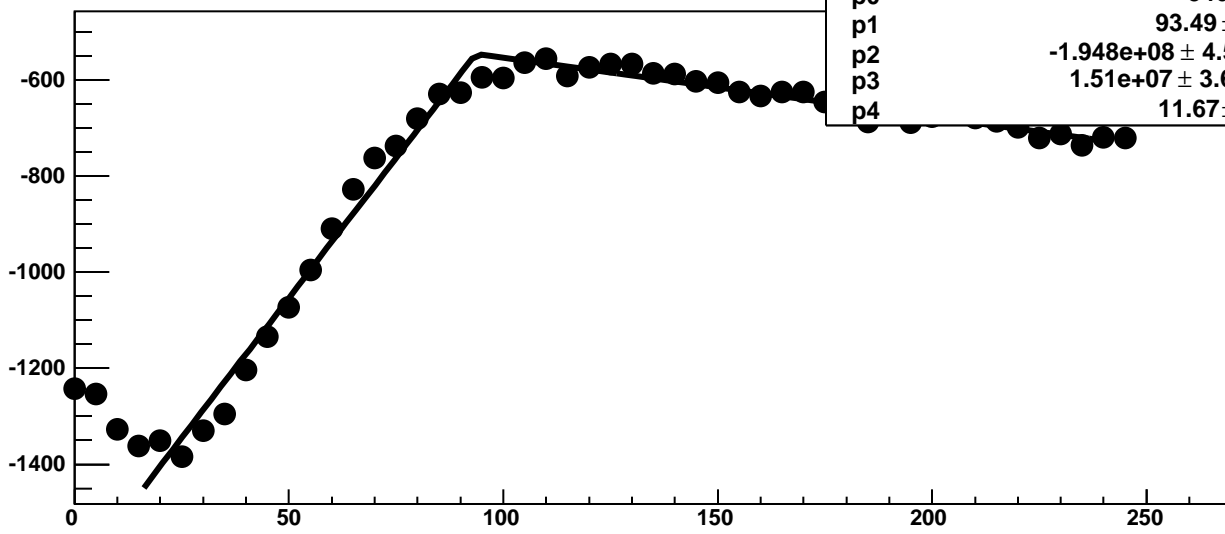
Chip 2, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

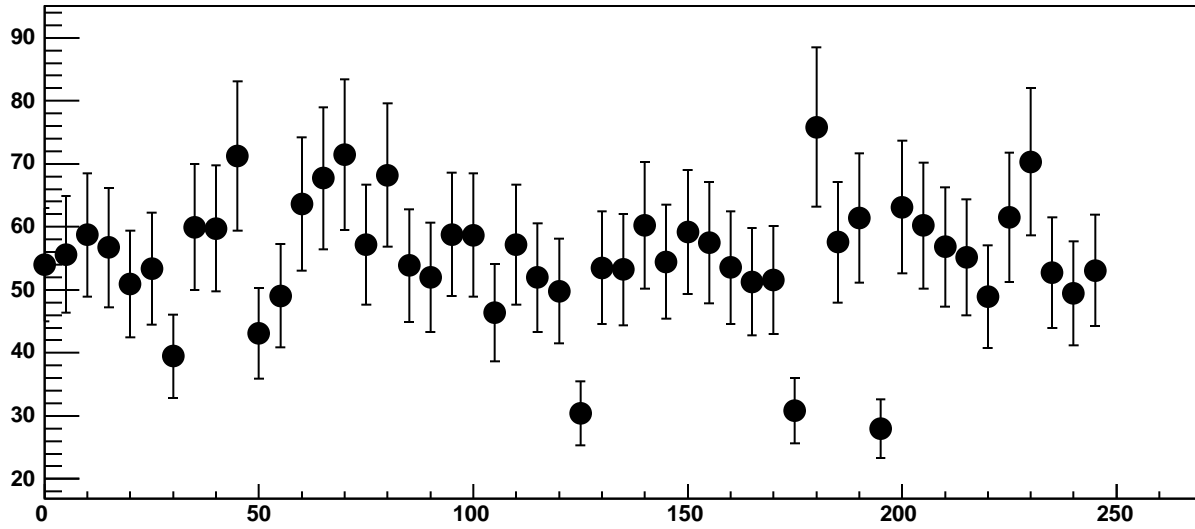


Chip 2, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

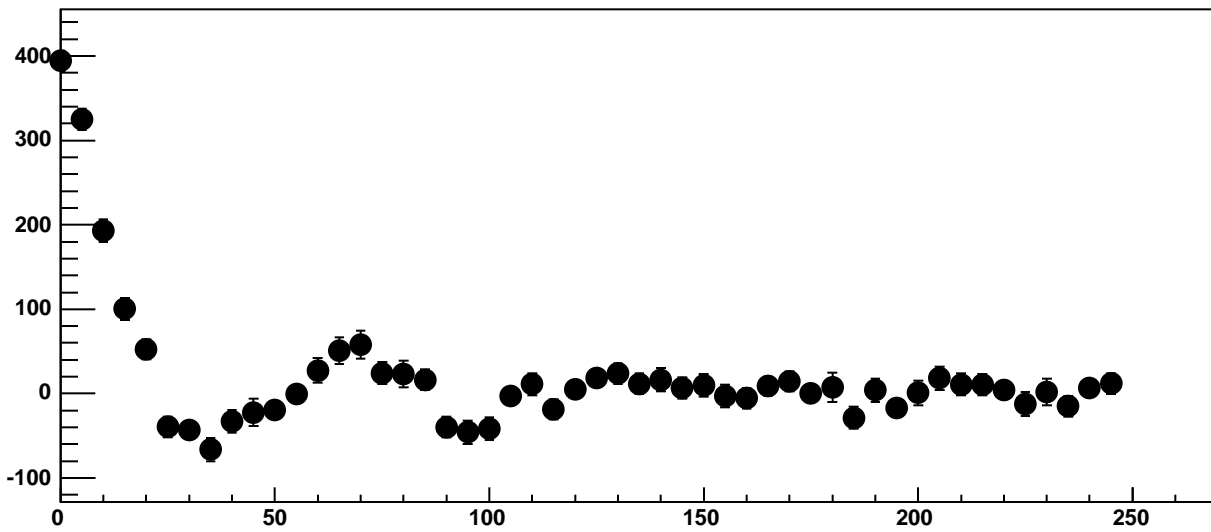


$\chi^2 / \text{ndf}$	251.3 / 41
p0	-546 ± 3.793
p1	93.49 ± 0.5789
p2	-1.948e+08 ± 4.584e+06
p3	1.51e+07 ± 3.637e+05
p4	11.67 ± 0.1233

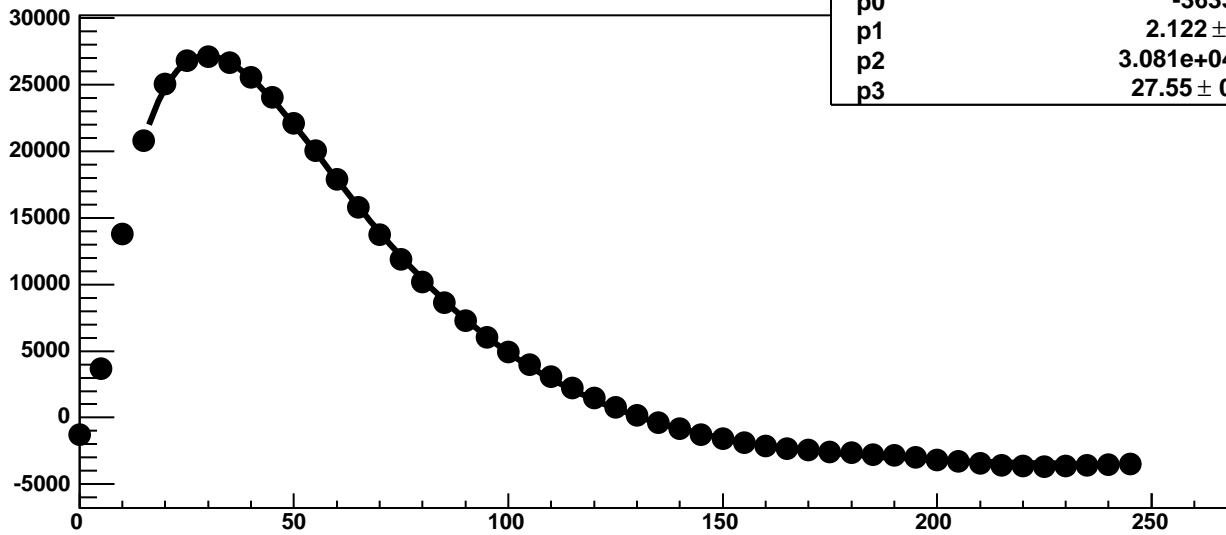
Chip 2, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

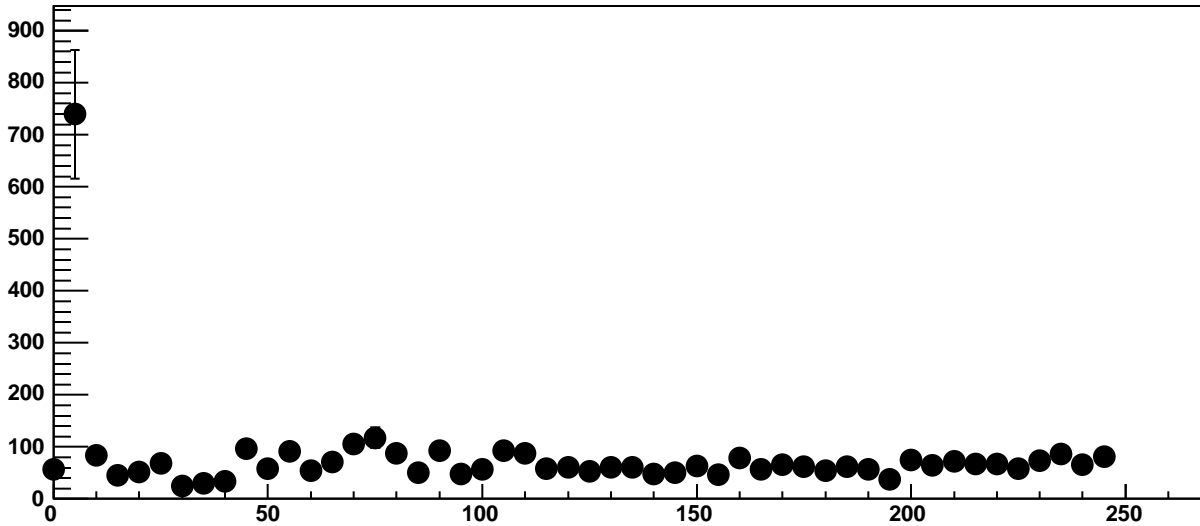


Chip 2, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

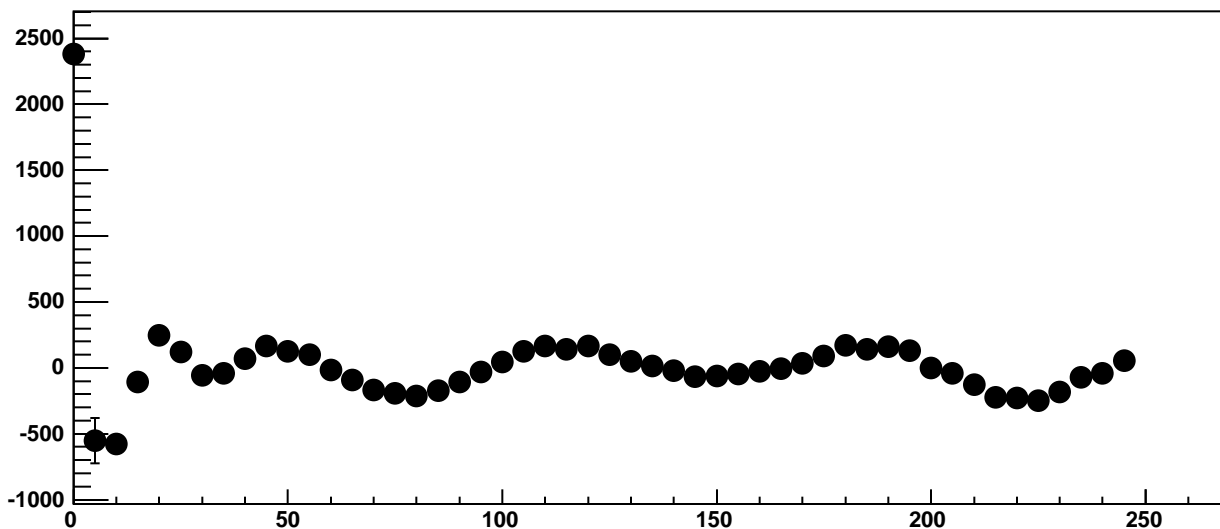


$\chi^2 / \text{ndf}$	3675 / 42
p0	-3635 ± 3.771
p1	2.122 ± 0.01246
p2	3.081e+04 ± 4.681
p3	27.55 ± 0.009666

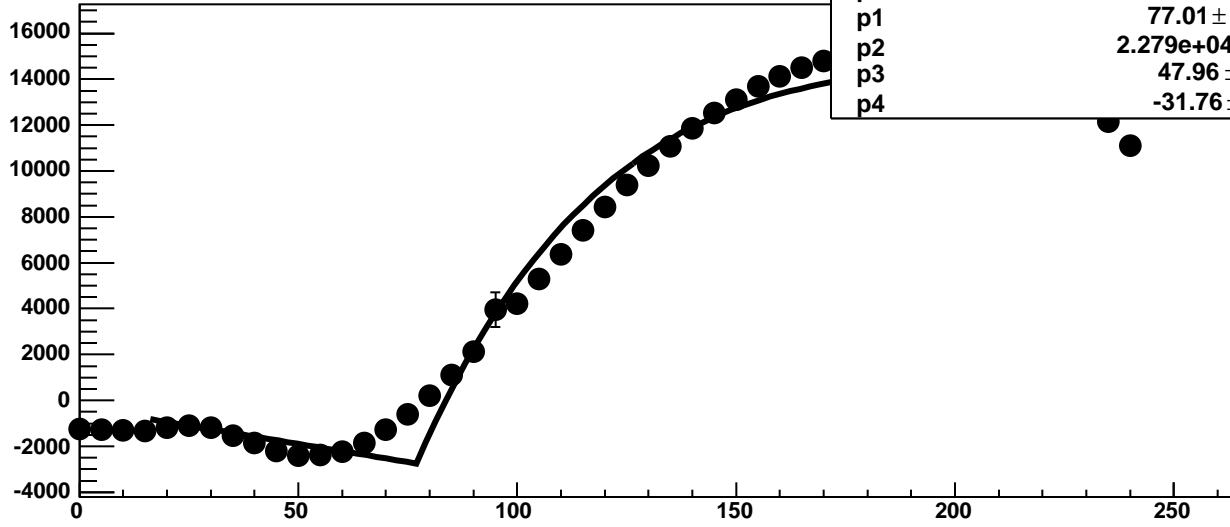
Chip 2, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

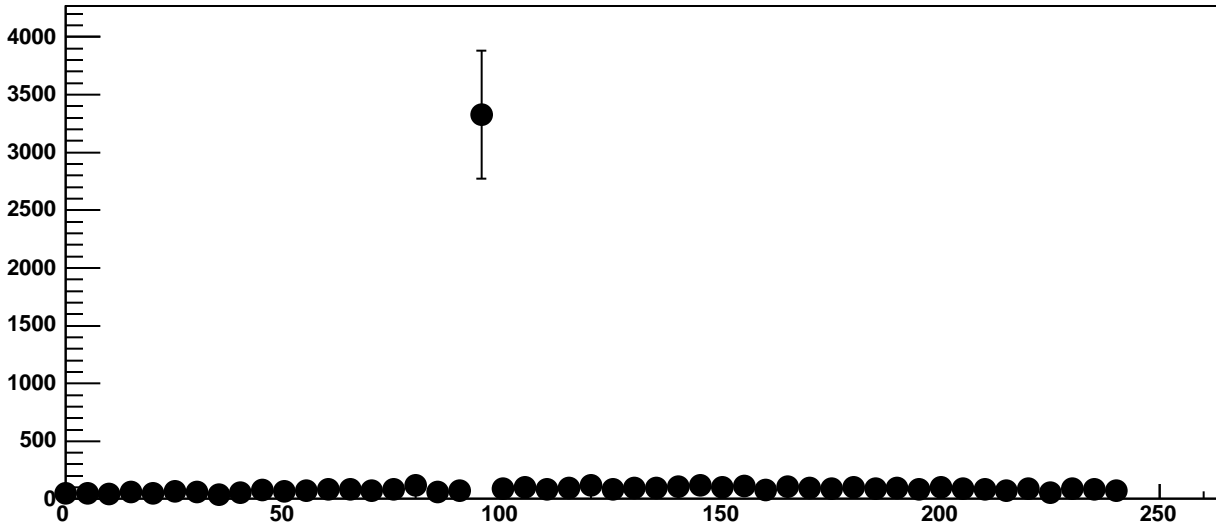


Chip 2, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

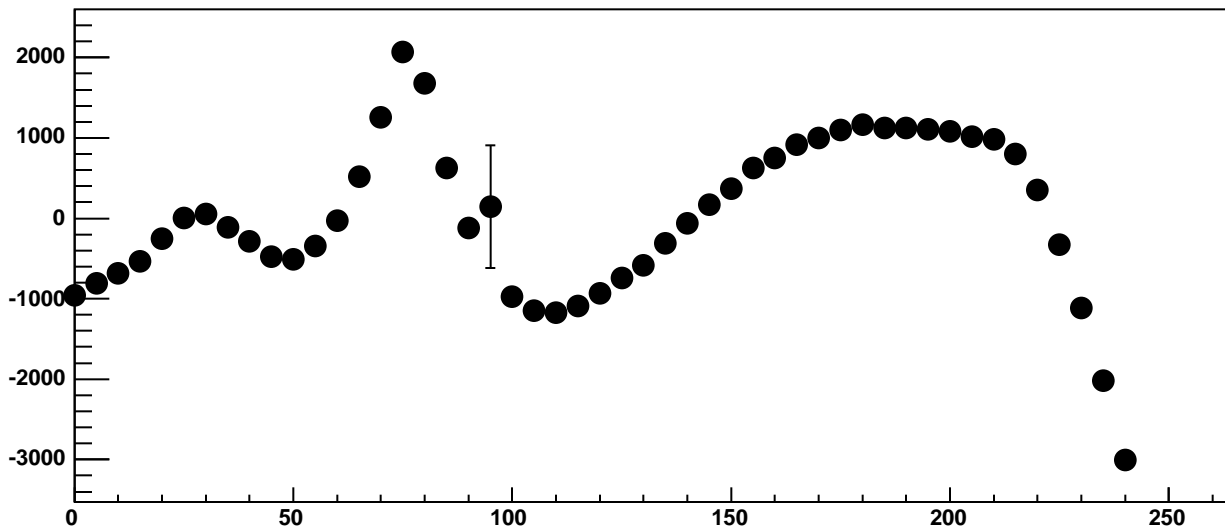


$\chi^2 / \text{ndf}$	1.232e+05 / 41
p0	-2751 ± 7.627
p1	77.01 ± 0.03529
p2	2.279e+04 ± 41.75
p3	47.96 ± 0.1015
p4	-31.76 ± 0.1933

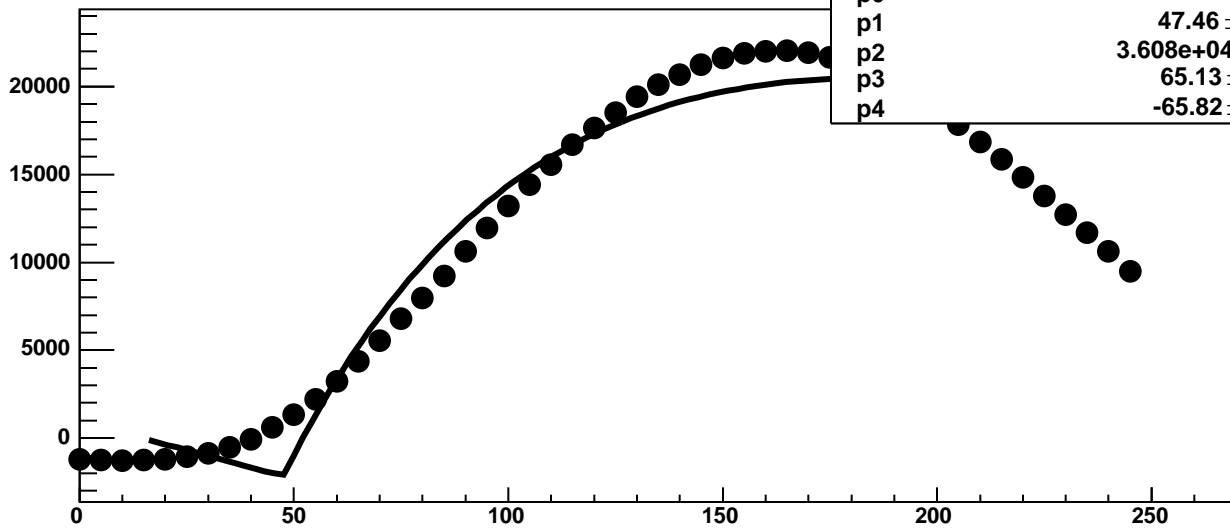
Chip 2, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold

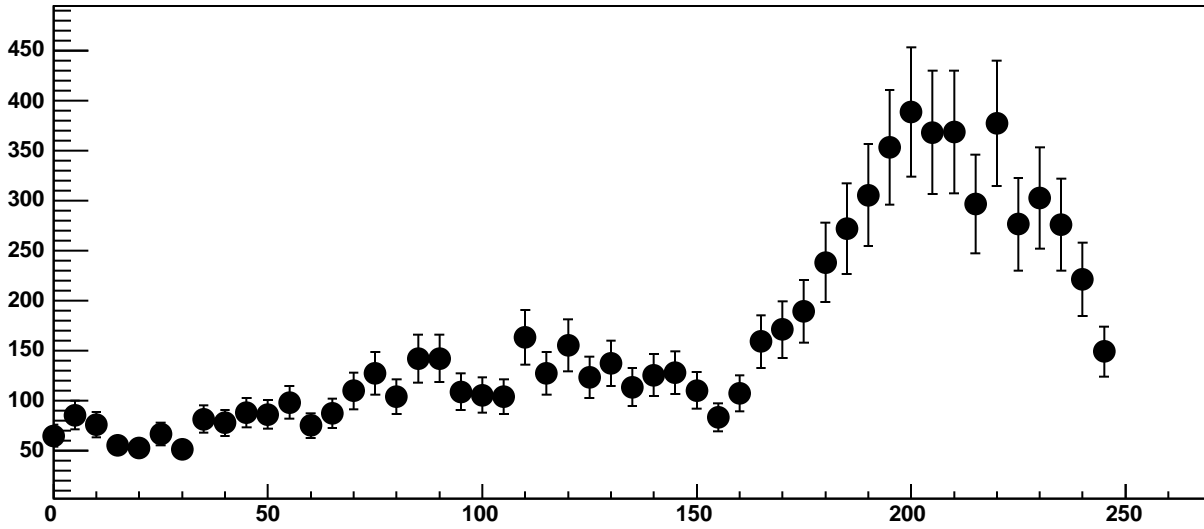


Chip 2, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

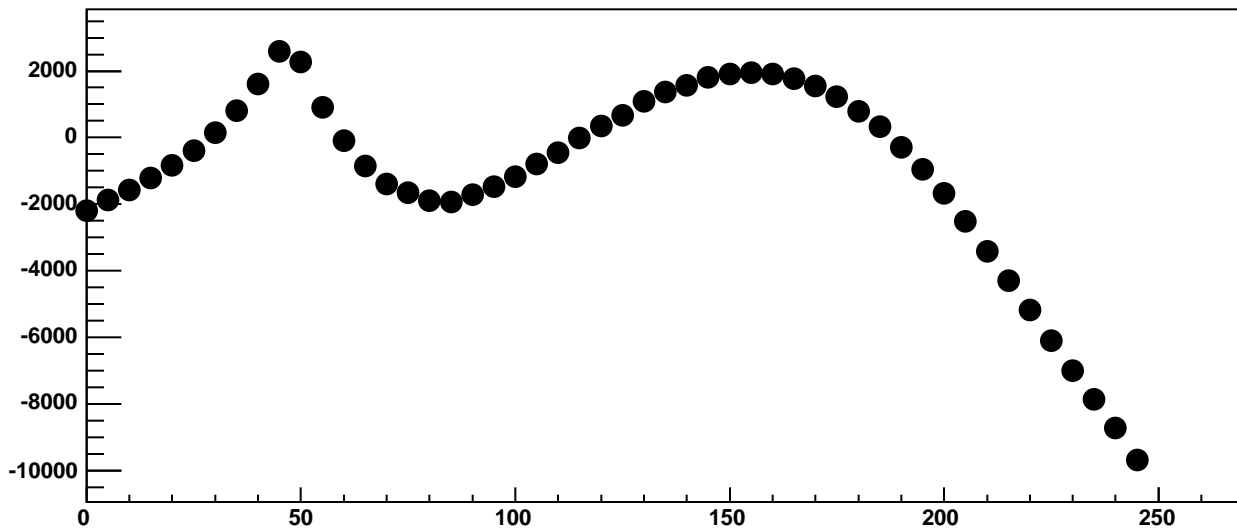


$\chi^2 / \text{ndf}$	1.973e+05 / 41
p0	-2156 ± 8.993
p1	47.46 ± 0.0304
p2	3.608e+04 ± 92.34
p3	65.13 ± 0.1513
p4	-65.82 ± 0.4153

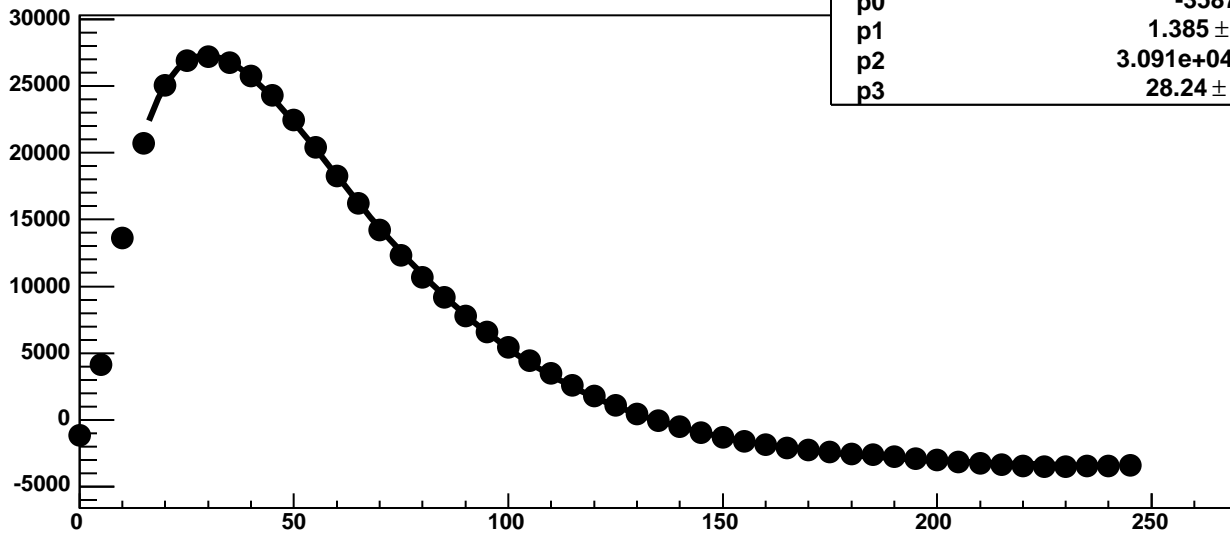
Chip 2, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

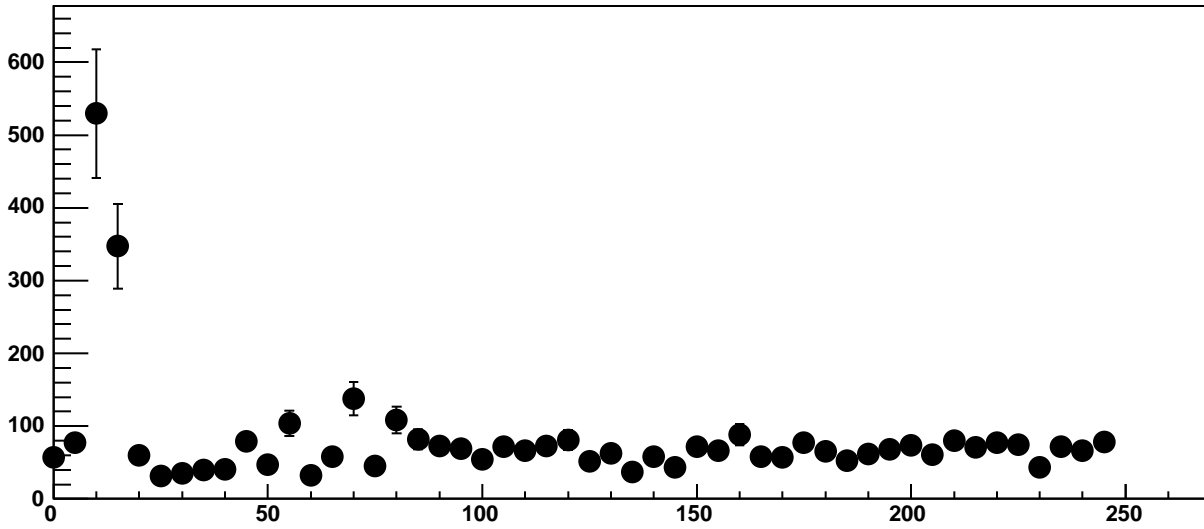


Chip 2, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold

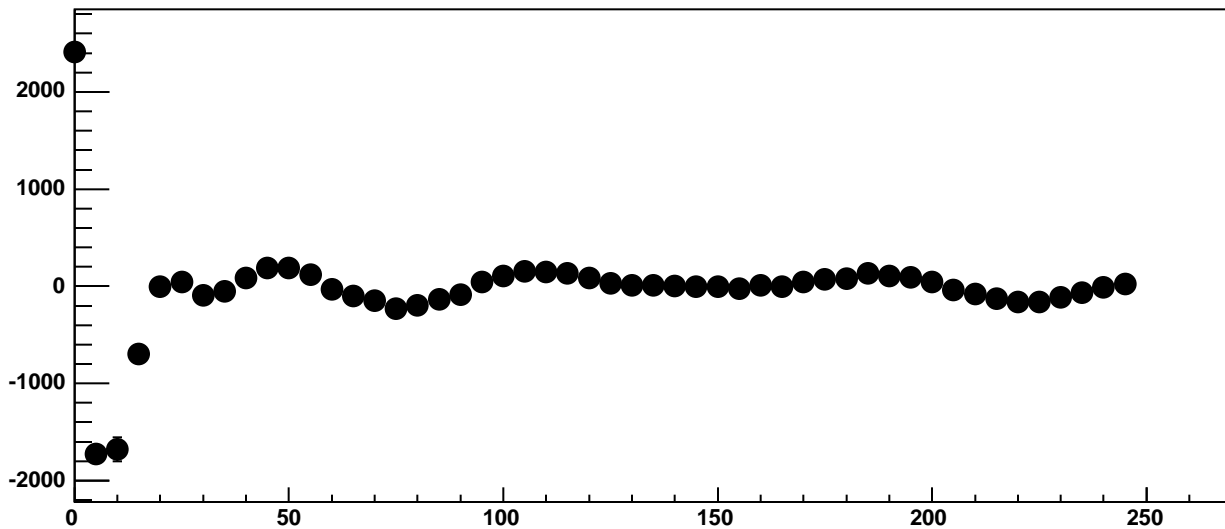


$\chi^2 / \text{ndf}$	2566 / 42
p0	$-3587 \pm 4.118$
p1	$1.385 \pm 0.02371$
p2	$3.091\text{e}+04 \pm 5.087$
p3	$28.24 \pm 0.01306$

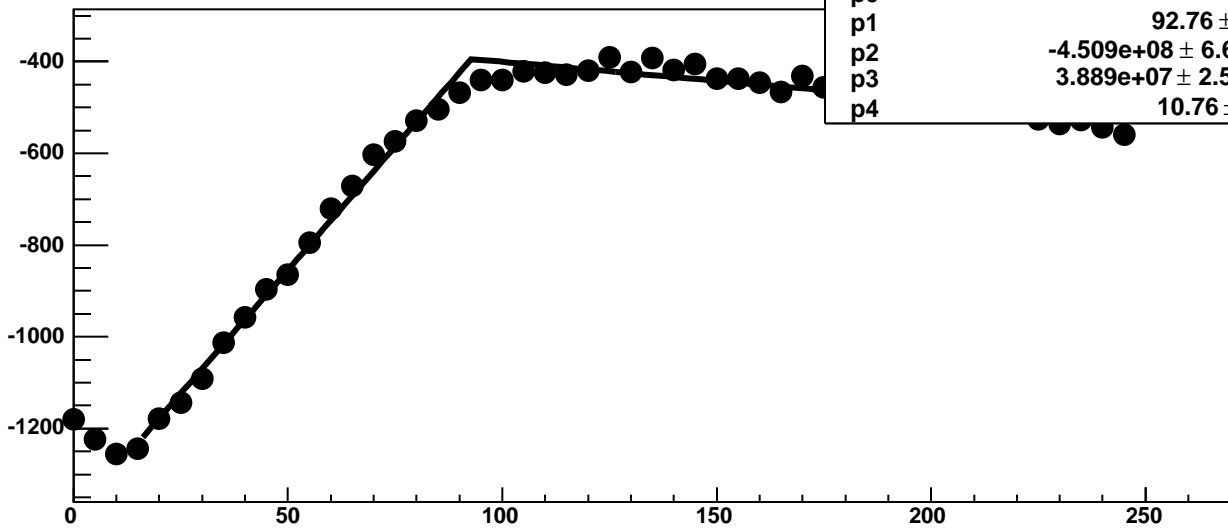
Chip 2, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

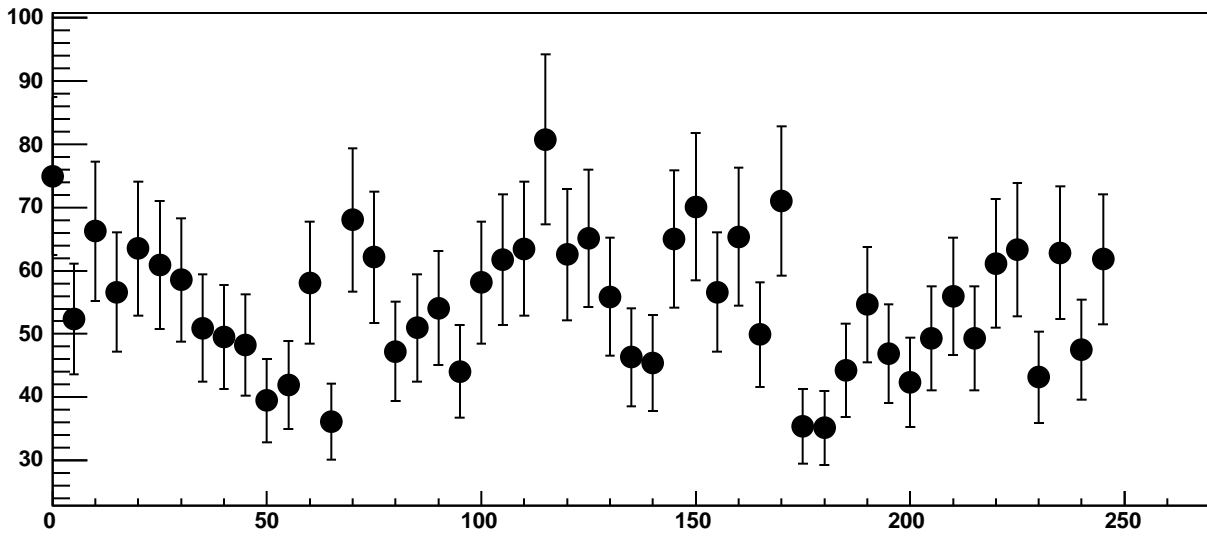


Chip 2, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

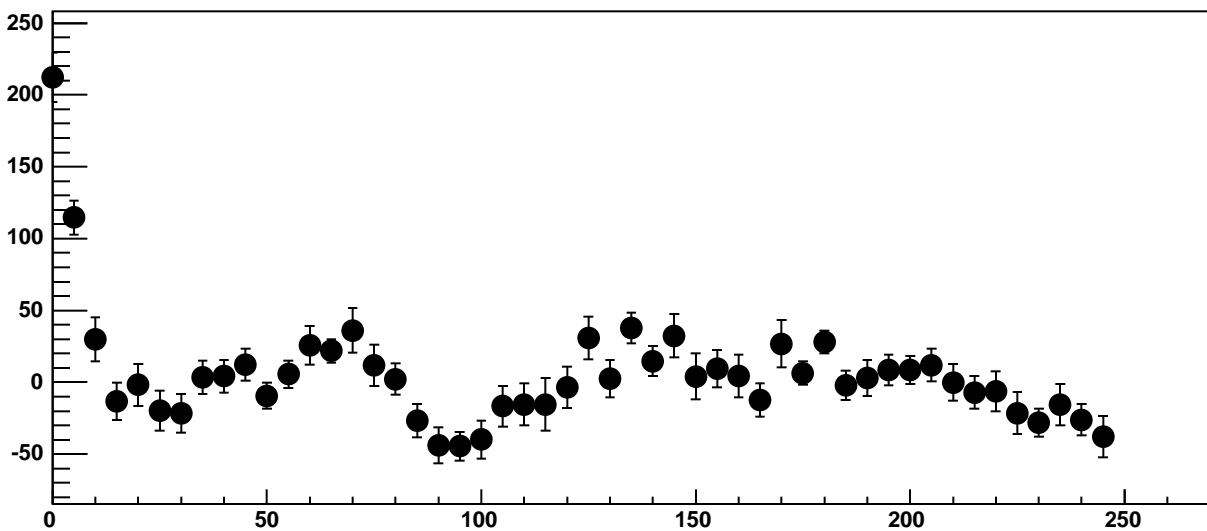


$\chi^2 / \text{ndf}$	135.7 / 41
p0	$-394.3 \pm 4.375$
p1	$92.76 \pm 0.6585$
p2	$-4.509\text{e}+08 \pm 6.616\text{e}+06$
p3	$3.889\text{e}+07 \pm 2.521\text{e}+05$
p4	$10.76 \pm 0.1371$

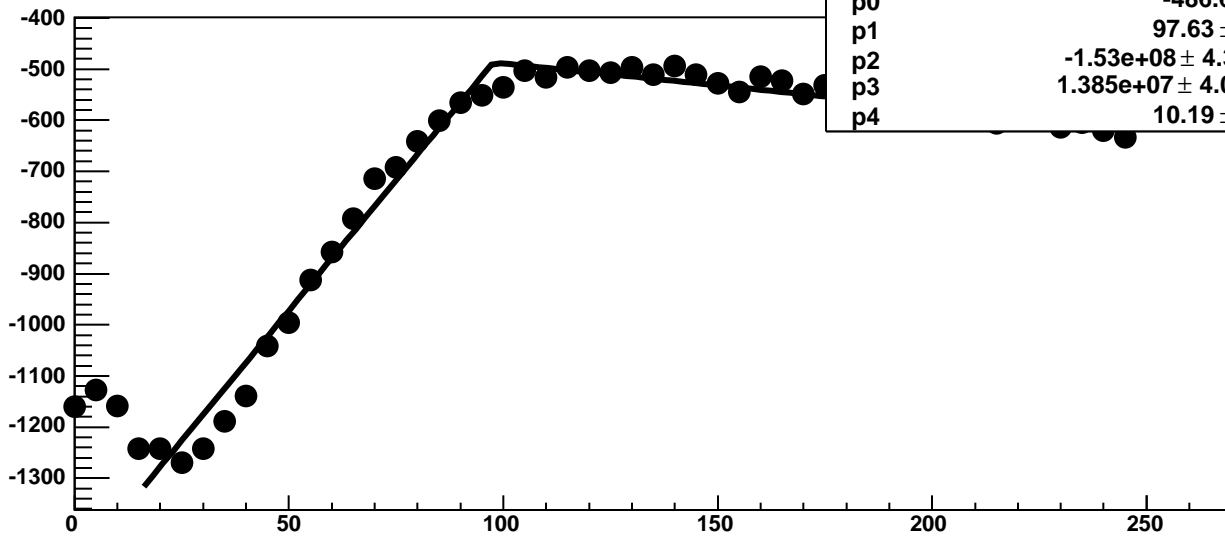
Chip 2, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

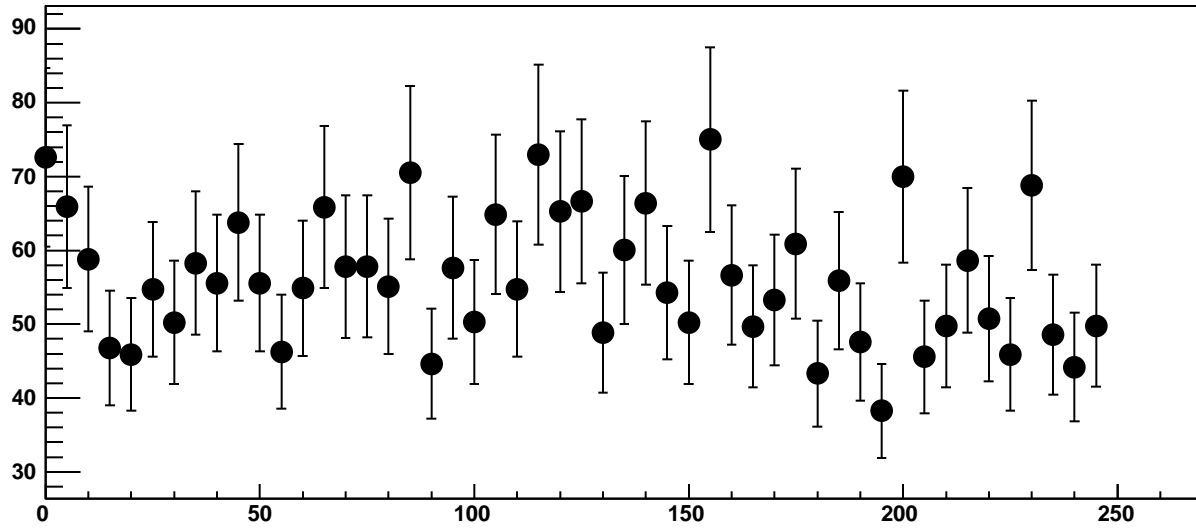


Chip 2, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

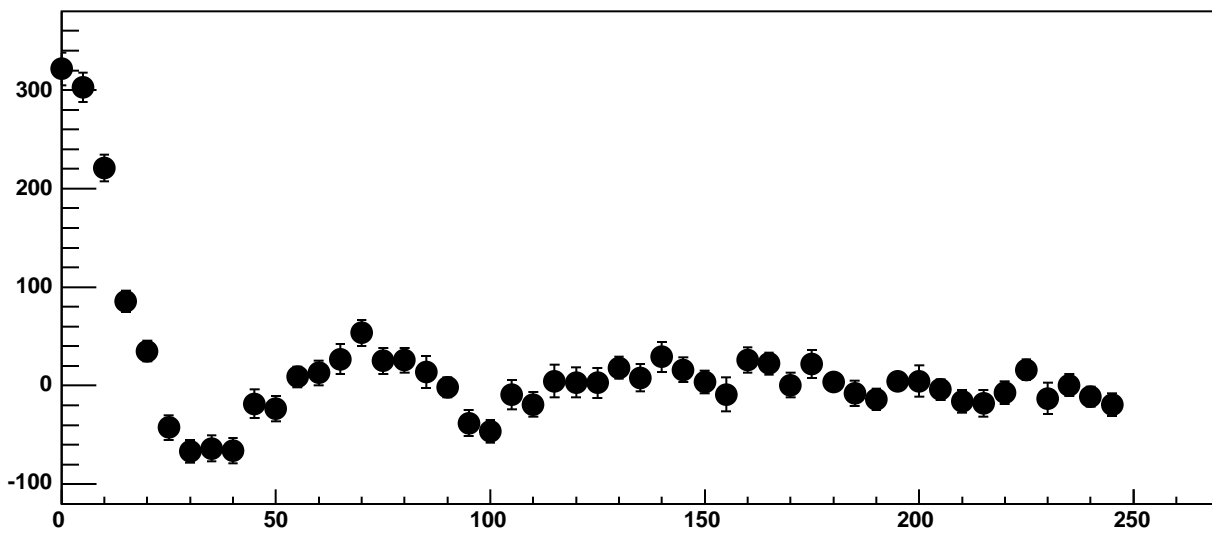


$\chi^2 / \text{ndf}$	261.2 / 41
p0	$-486.6 \pm 4.421$
p1	$97.63 \pm 0.6734$
p2	$-1.53\text{e}+08 \pm 4.353\text{e}+06$
p3	$1.385\text{e}+07 \pm 4.064\text{e}+05$
p4	$10.19 \pm 0.1095$

Chip 2, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

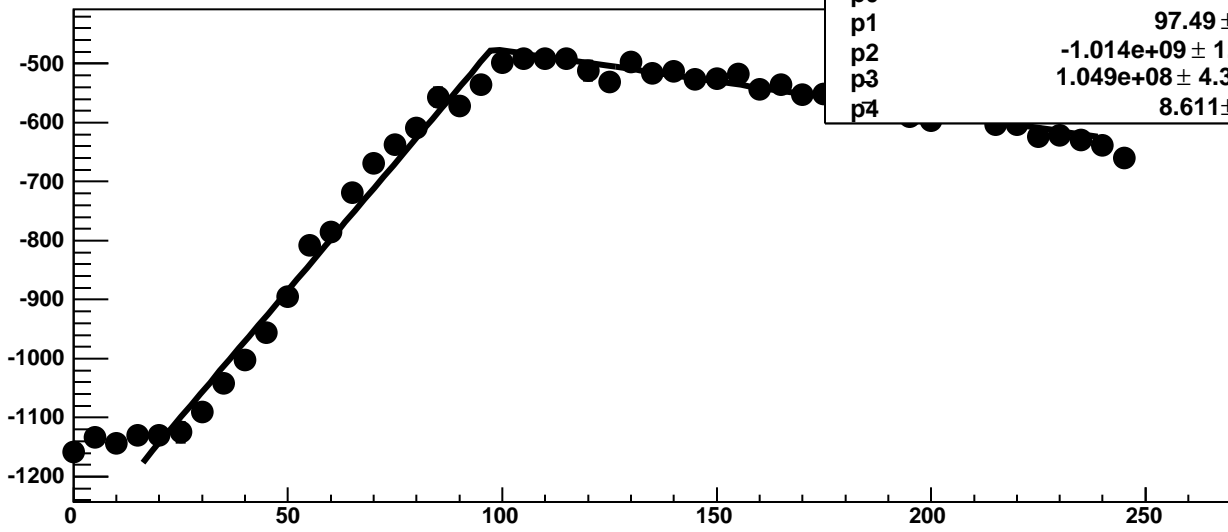


Chip 2, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold



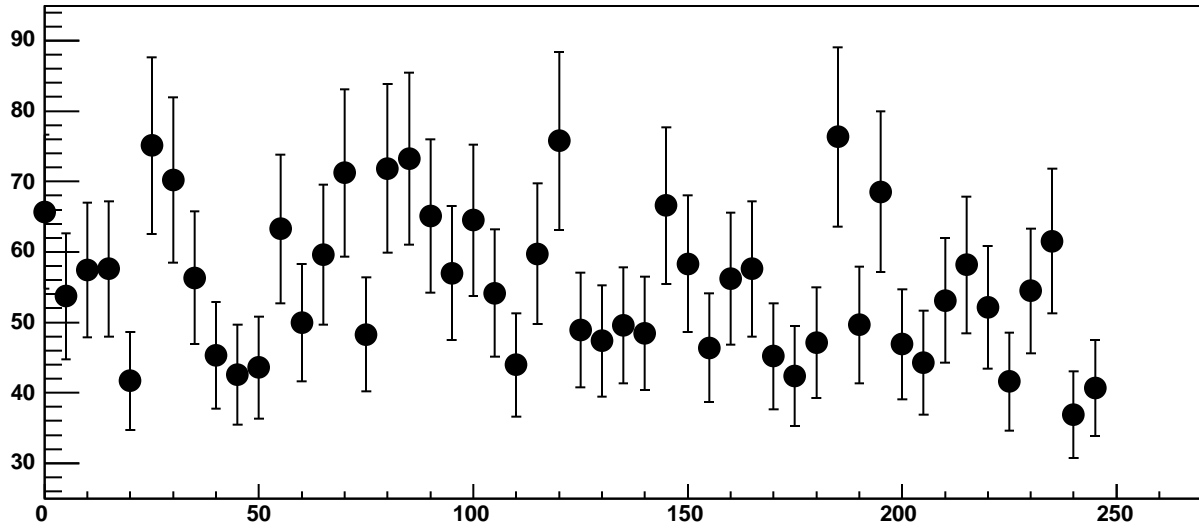


Chip 2, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold

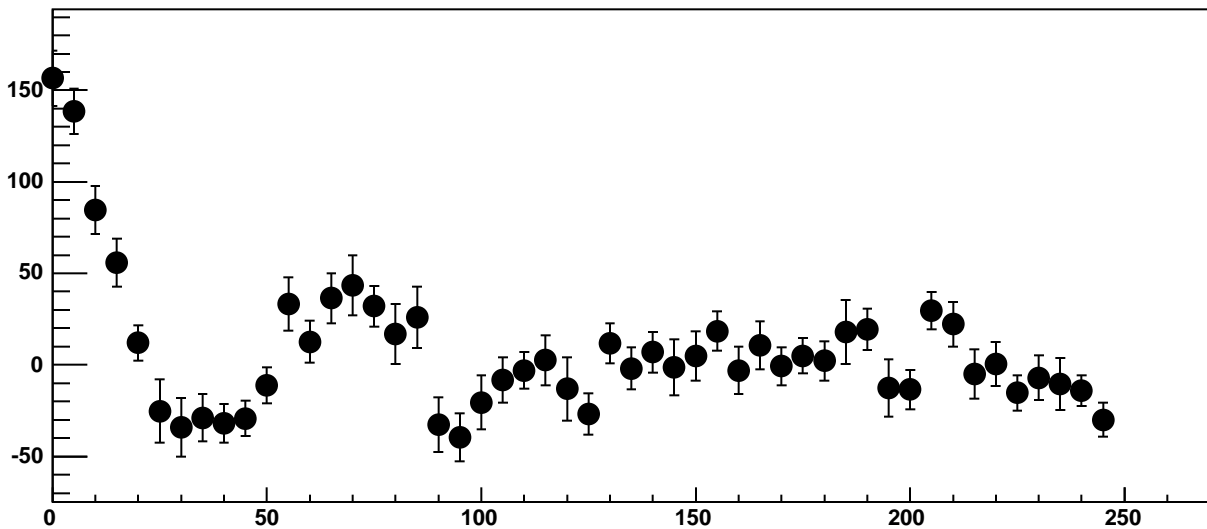


$\chi^2 / \text{ndf}$	135.9 / 41
p0	$-475.2 \pm 4.074$
p1	$97.49 \pm 0.8367$
p2	$-1.014\text{e}+09 \pm 1.54\text{e}+07$
p3	$1.049\text{e}+08 \pm 4.354\text{e}+05$
p4	$8.611 \pm 0.1312$

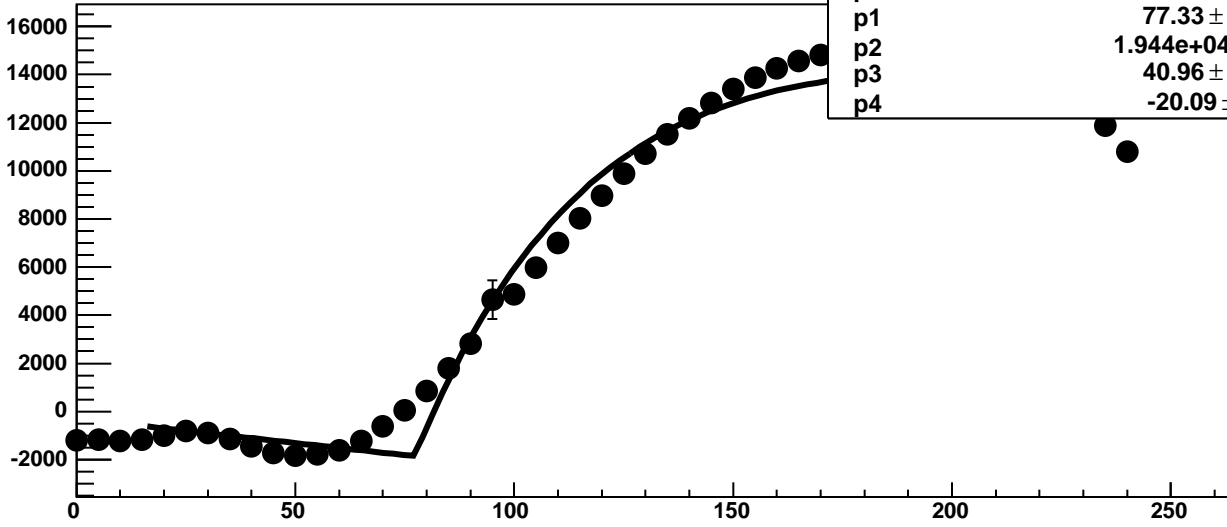
Chip 2, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold

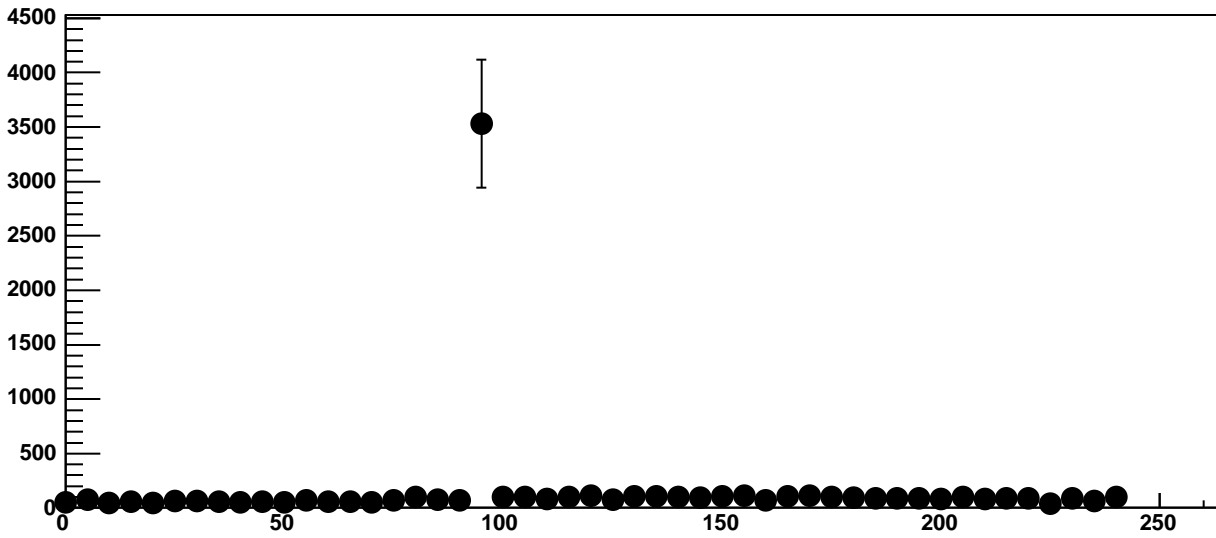


Chip 2, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

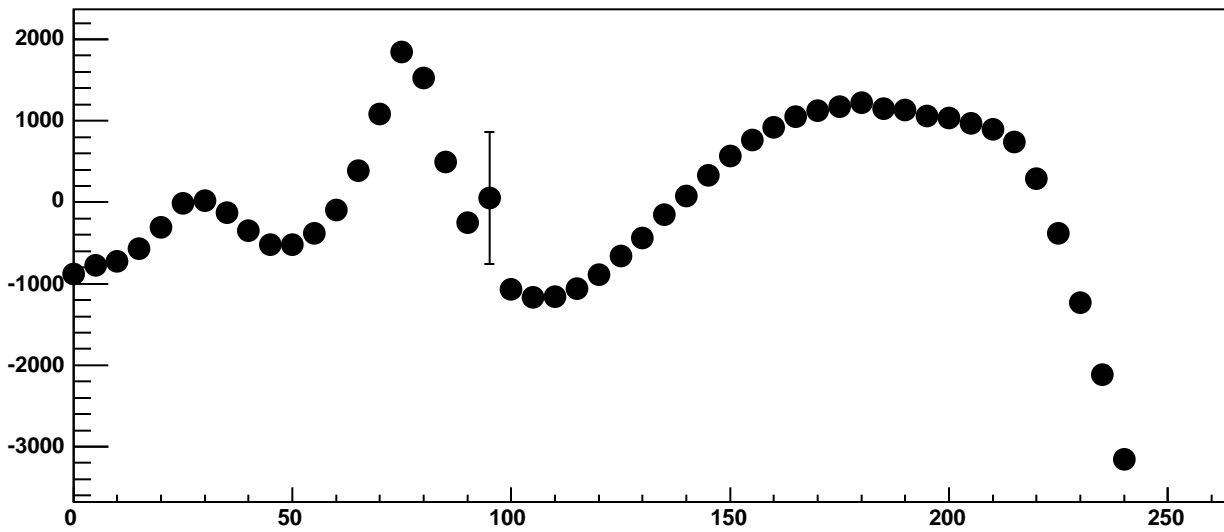


$\chi^2 / \text{ndf}$	1.266e+05 / 41
p0	-1861 ± 6.218
p1	77.33 ± 0.03466
p2	1.944e+04 ± 32.36
p3	40.96 ± 0.08824
p4	-20.09 ± 0.1626

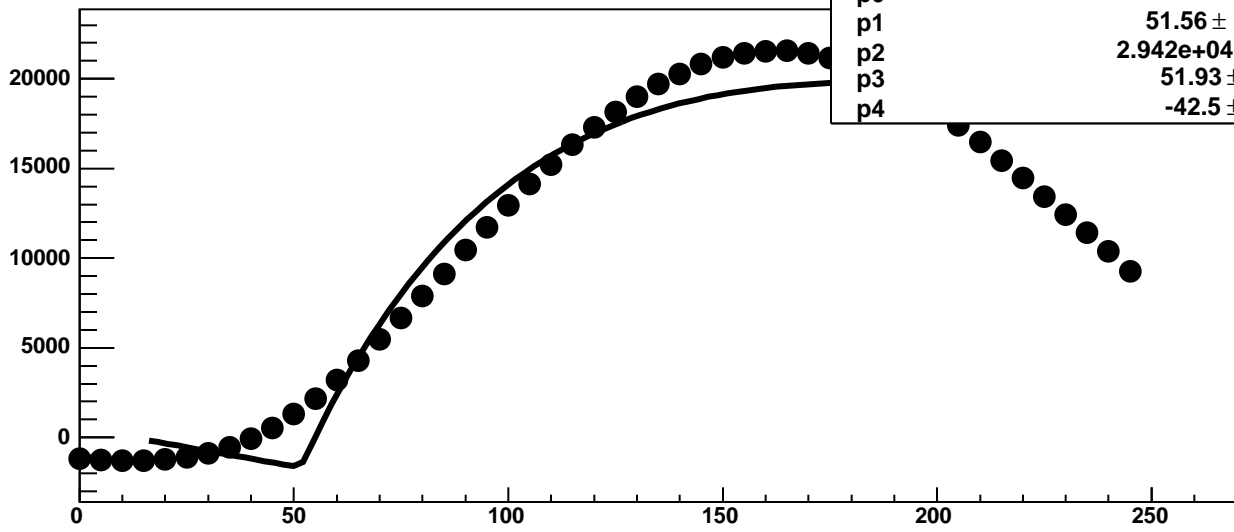
Chip 2, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



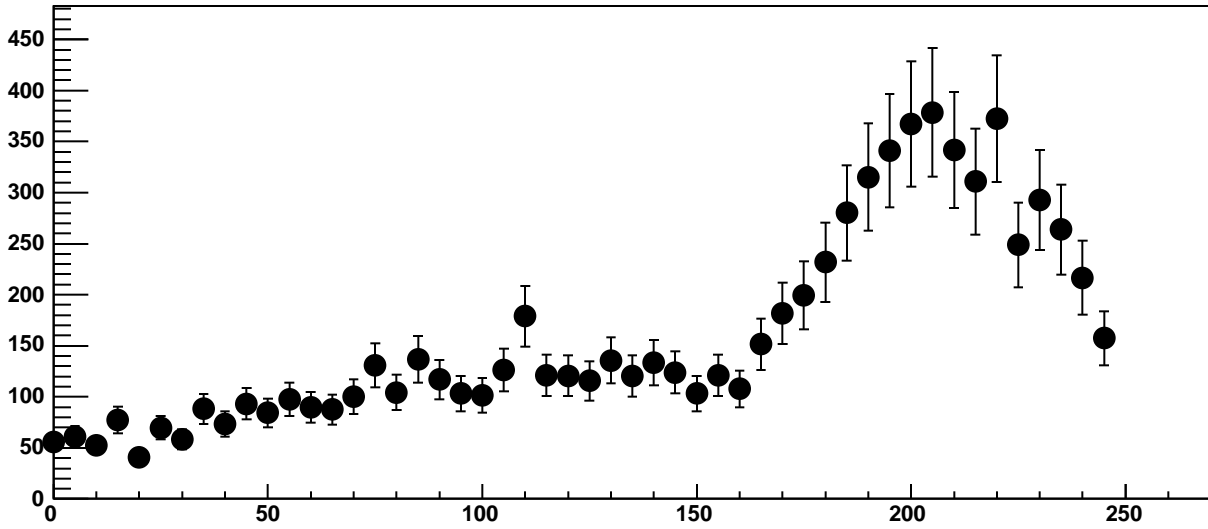
Chip 2, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold



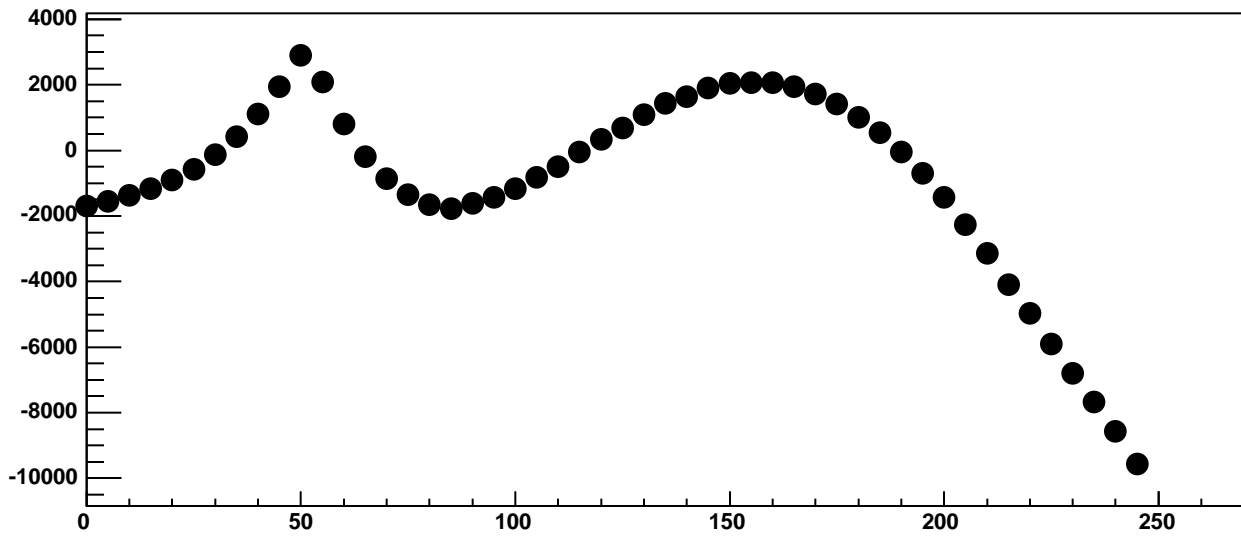
Chip 2, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold



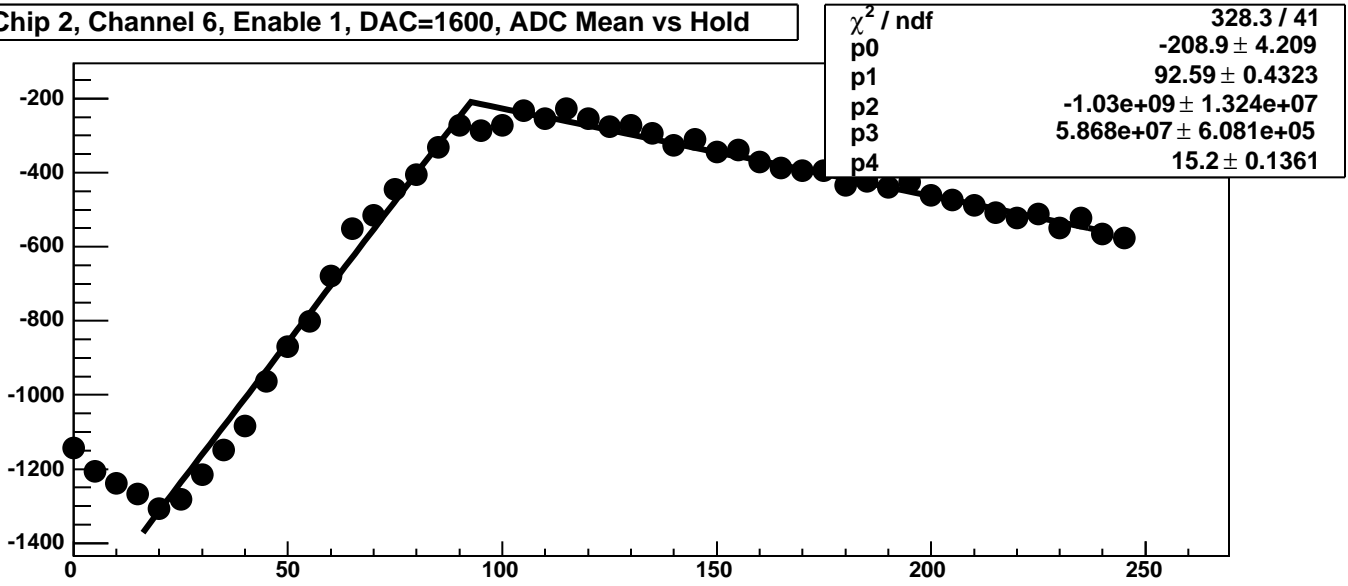
Chip 2, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



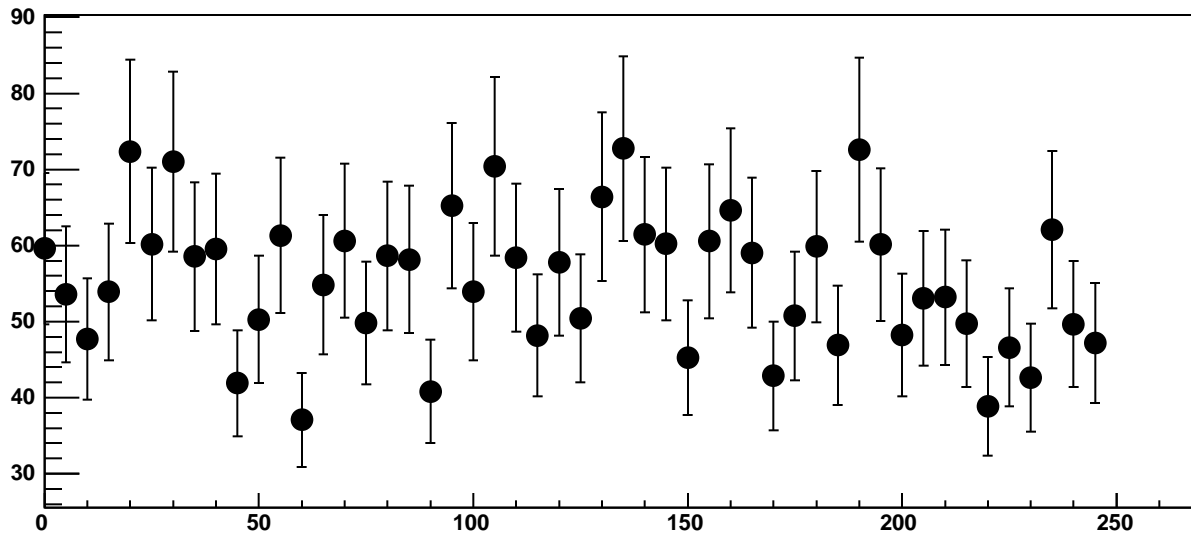
Chip 2, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



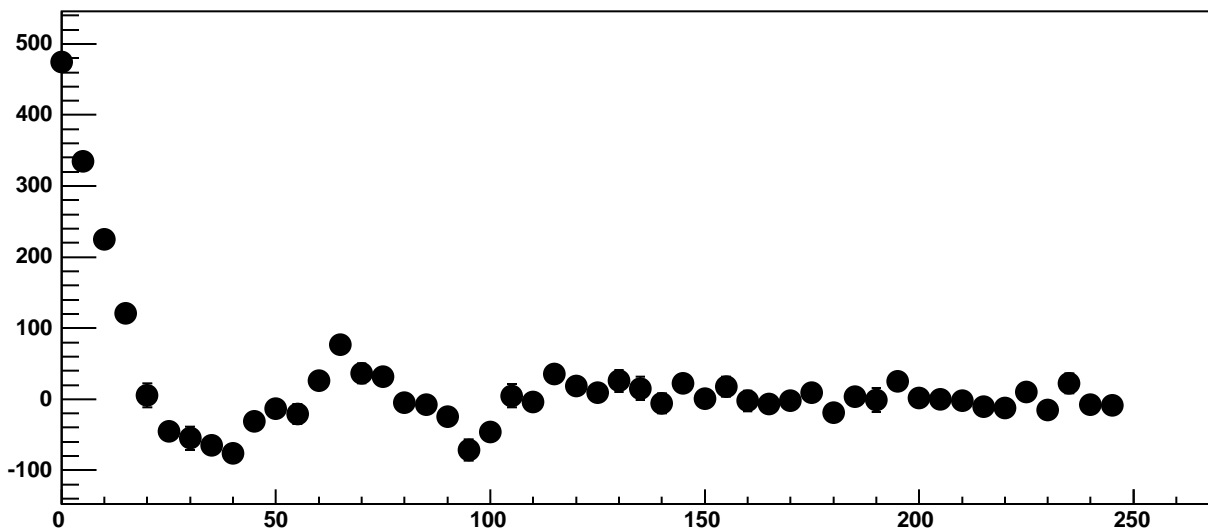
Chip 2, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



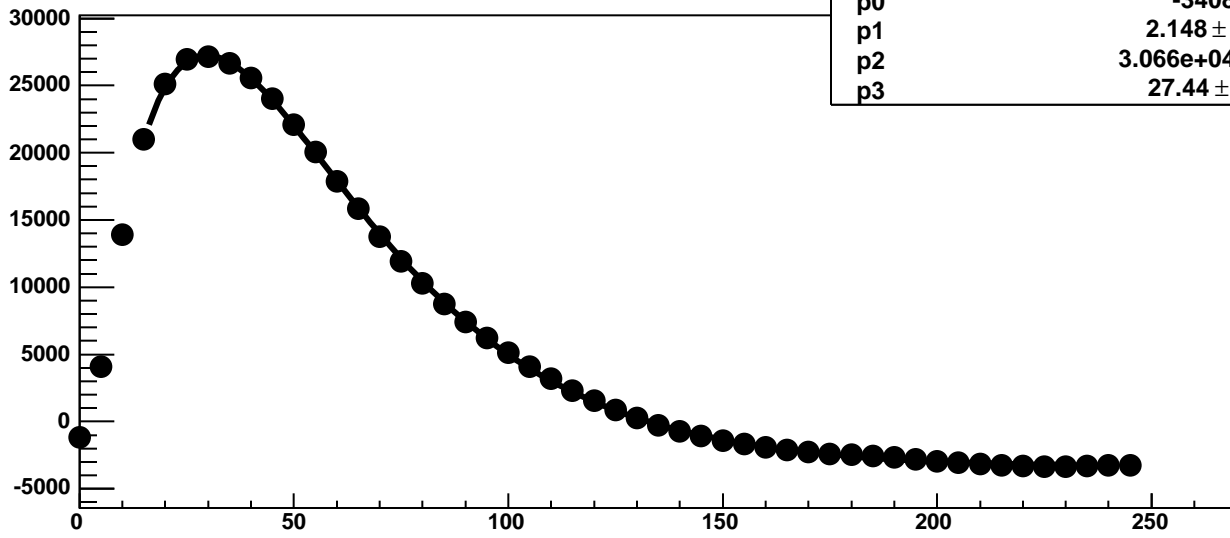
Chip 2, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

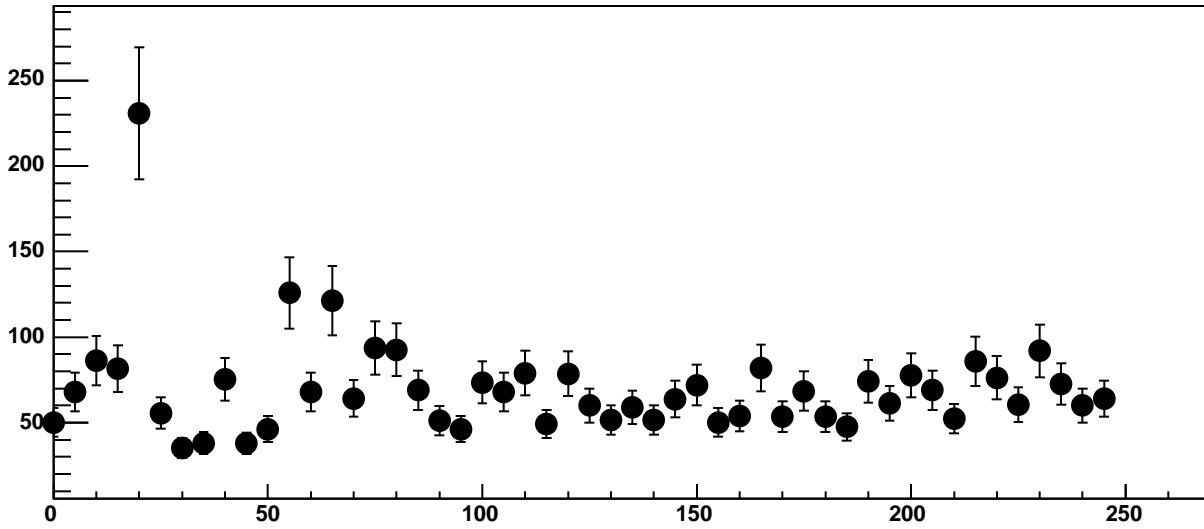


Chip 2, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold

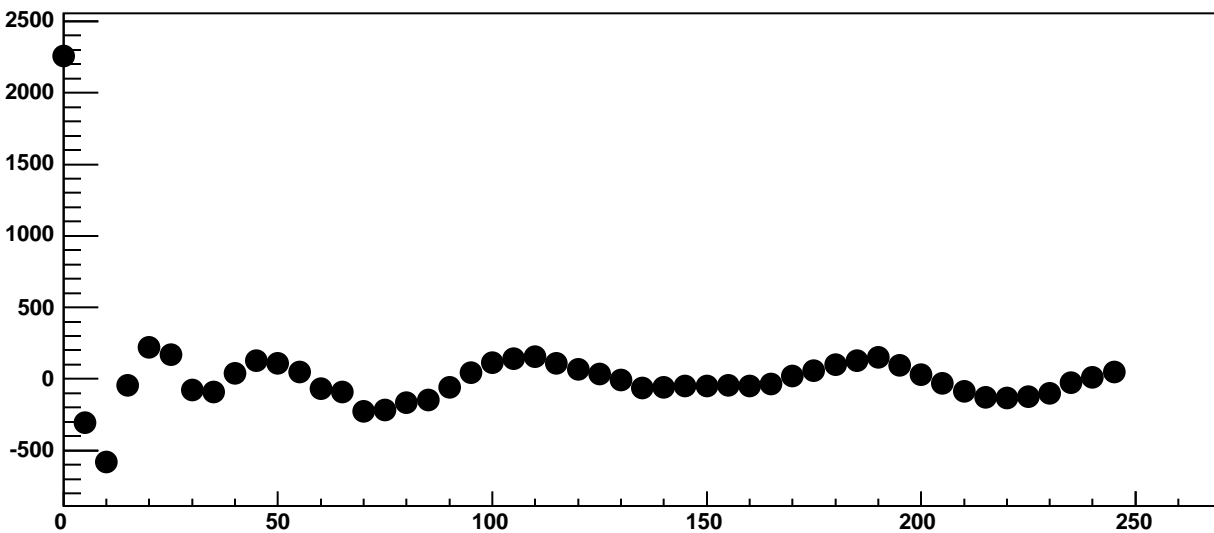


$\chi^2 / \text{ndf}$	2319 / 42
p0	-3408 ± 3.935
p1	2.148 ± 0.01907
p2	3.066e+04 ± 5.551
p3	27.44 ± 0.01117

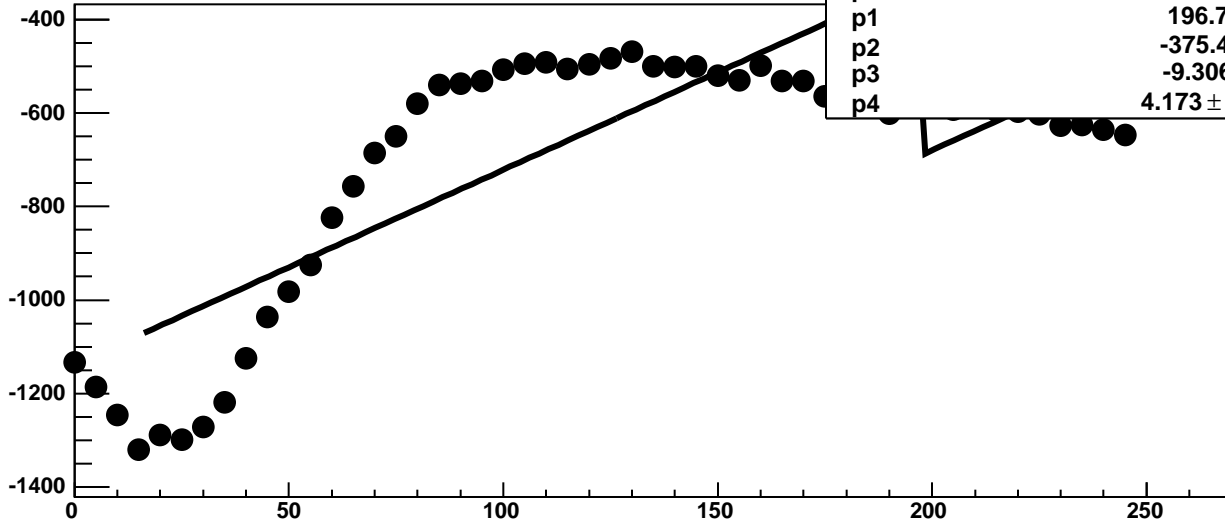
Chip 2, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



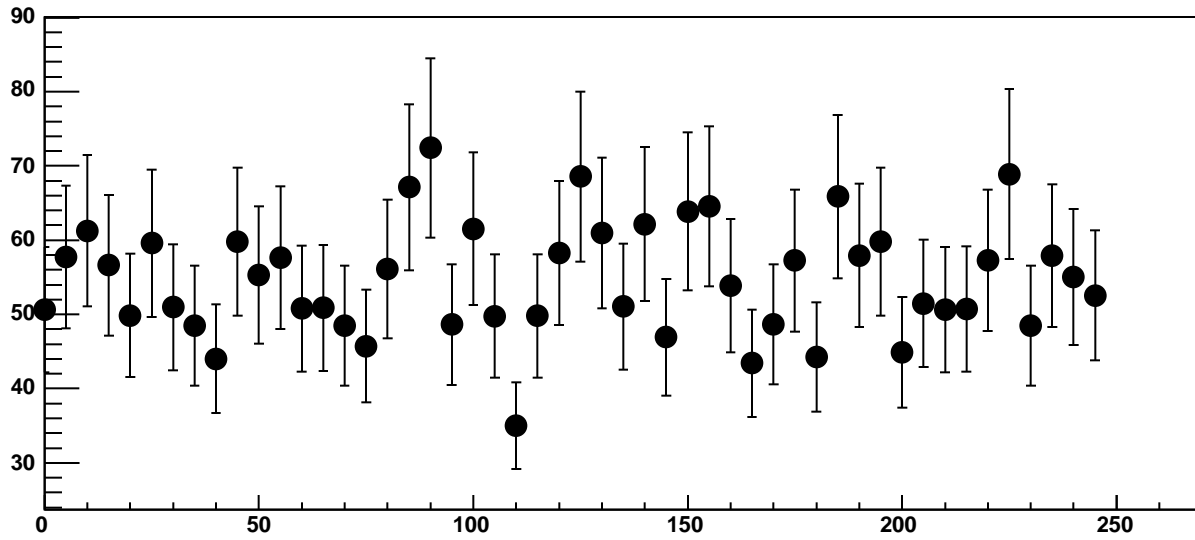
Chip 2, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold



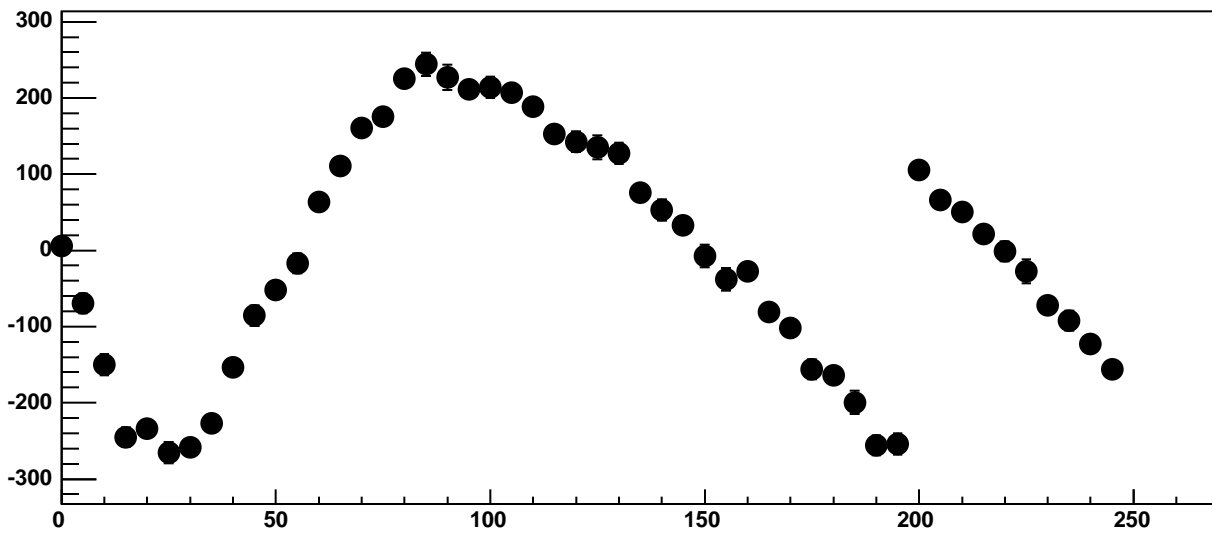
Chip 2, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold



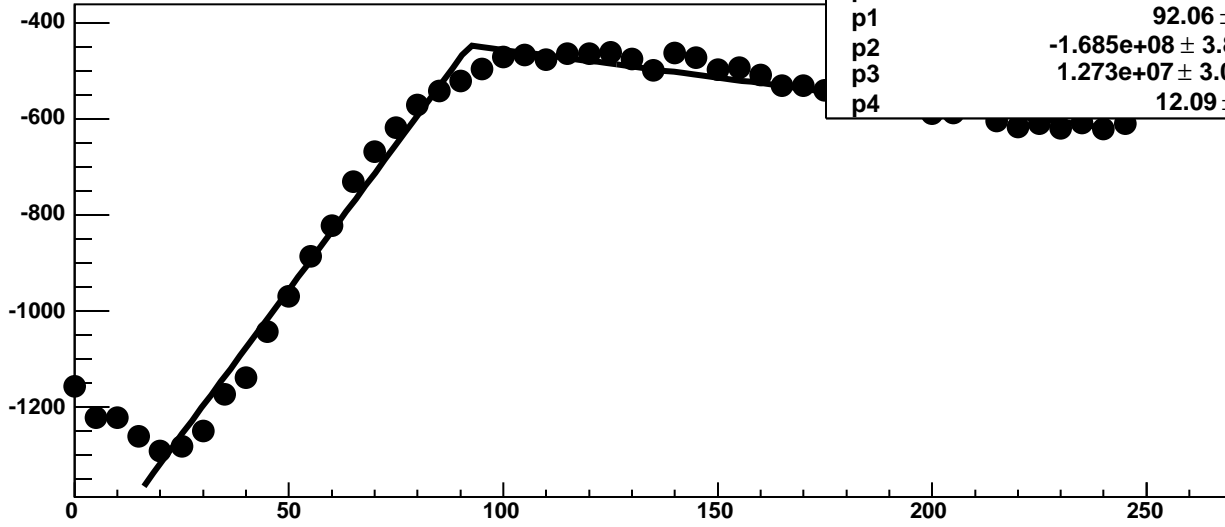
Chip 2, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

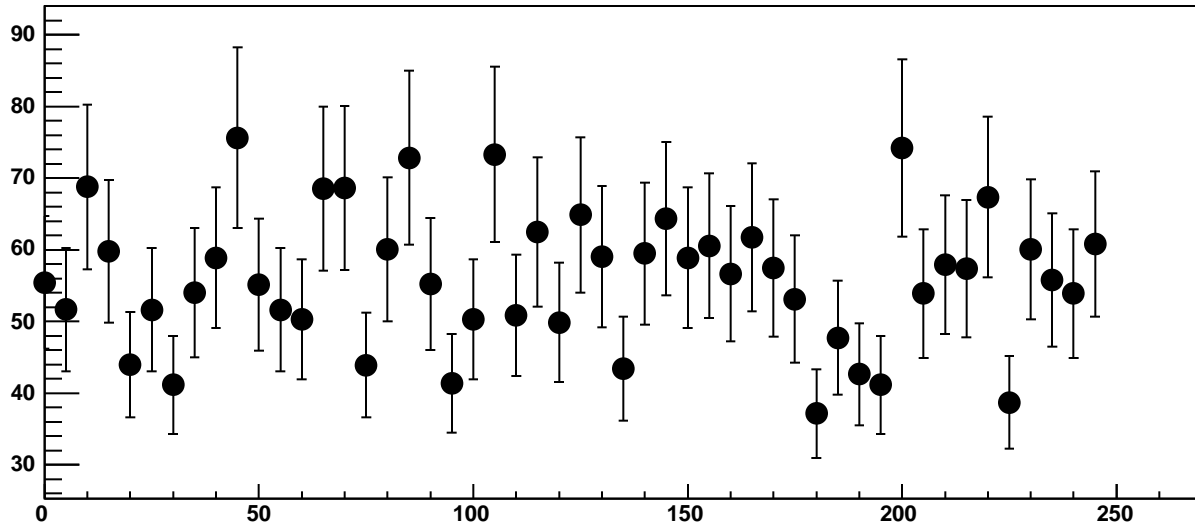


Chip 2, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

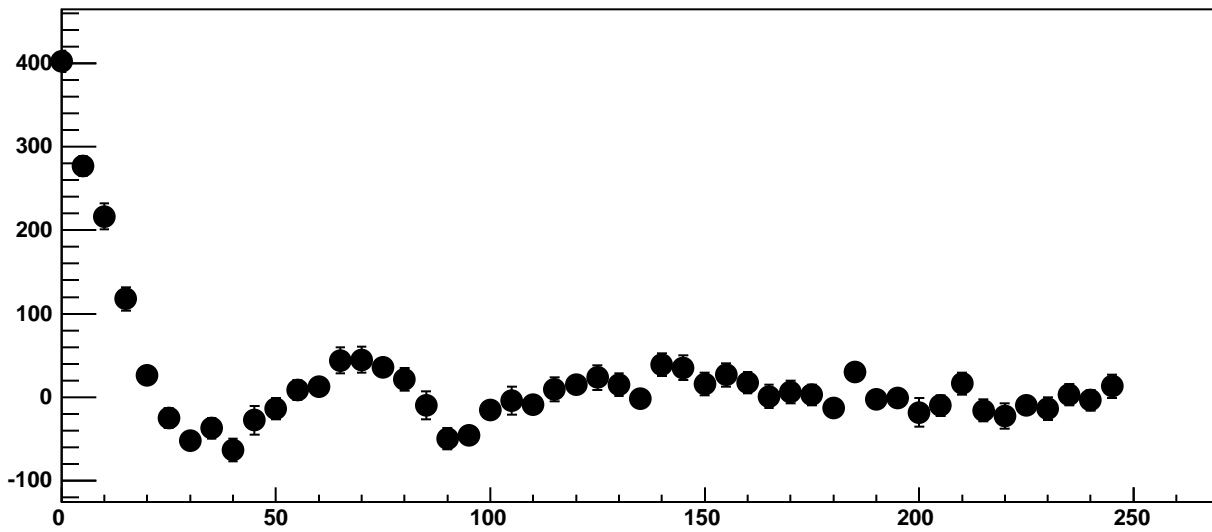


$\chi^2 / \text{ndf}$	269.9 / 41
p0	$-446.7 \pm 4.035$
p1	$92.06 \pm 0.5645$
p2	$-1.685\text{e}+08 \pm 3.896\text{e}+06$
p3	$1.273\text{e}+07 \pm 3.009\text{e}+05$
p4	$12.09 \pm 0.1227$

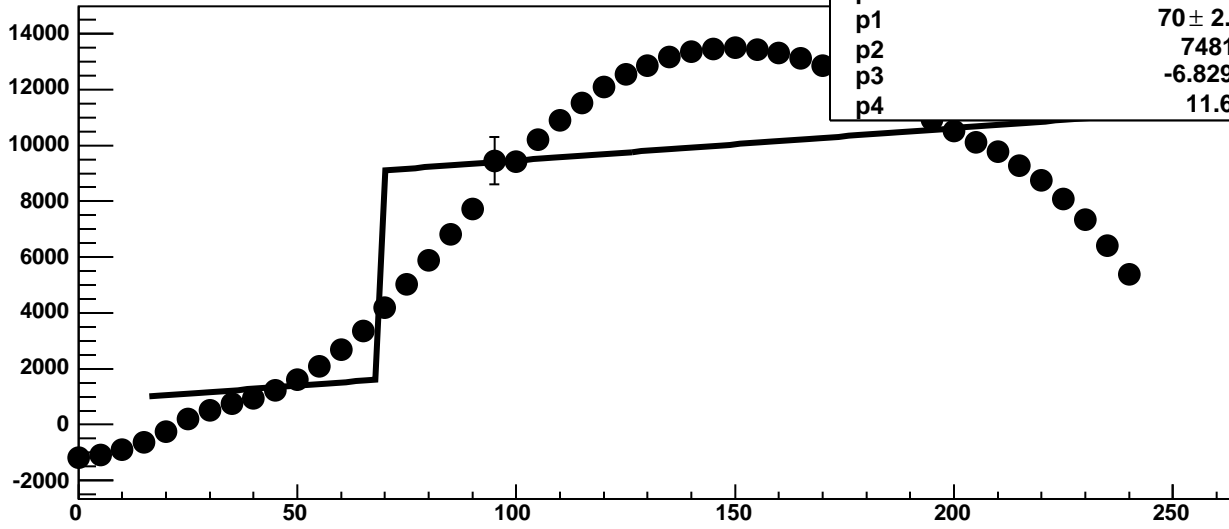
Chip 2, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

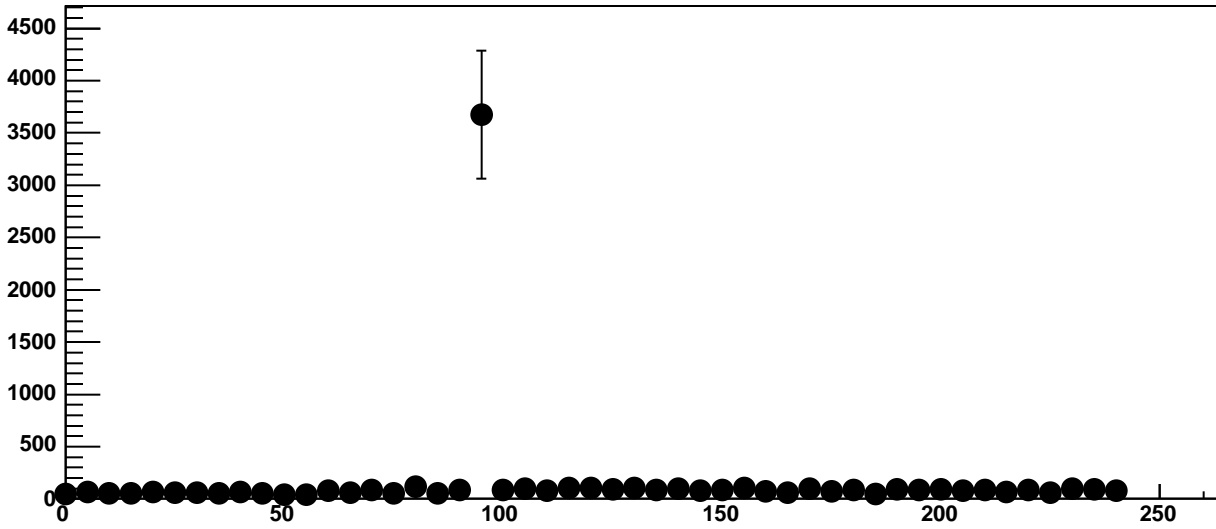


Chip 2, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold

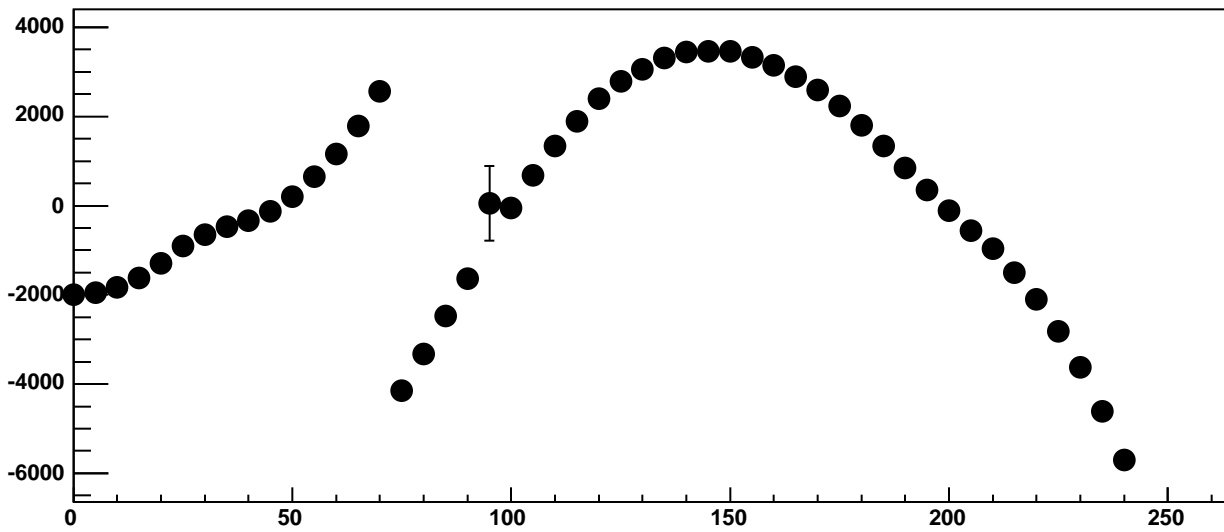


$\chi^2 / \text{ndf}$	8.335e+05 / 41
p0	1629 ± 2.019
p1	70 ± 2.081e-05
p2	7481 ± 1.465
p3	-6.829 ± 14.09
p4	11.6 ± 0.226

Chip 2, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

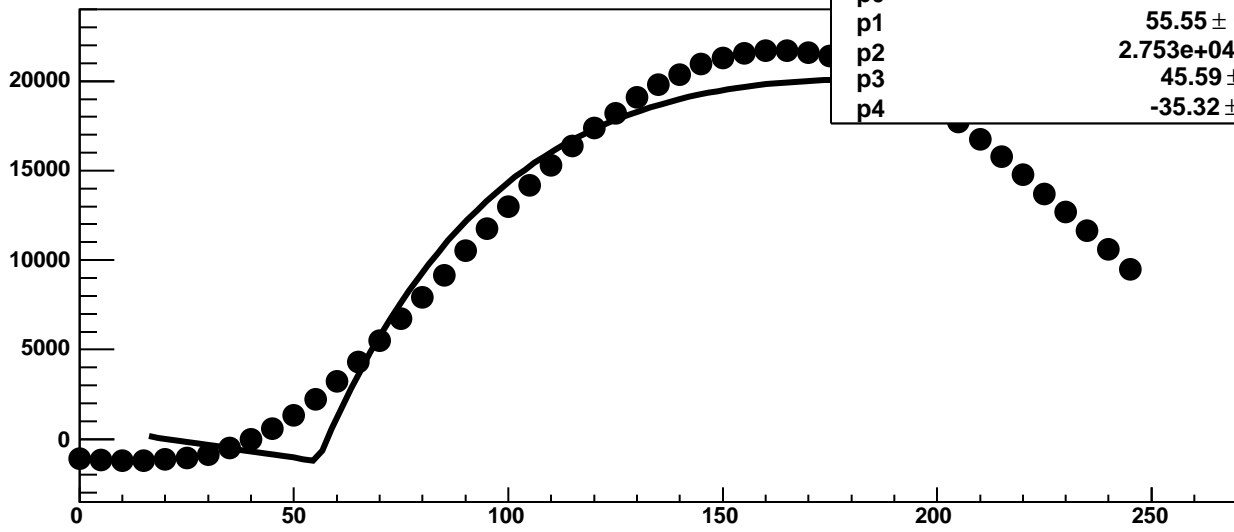


Chip 2, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold



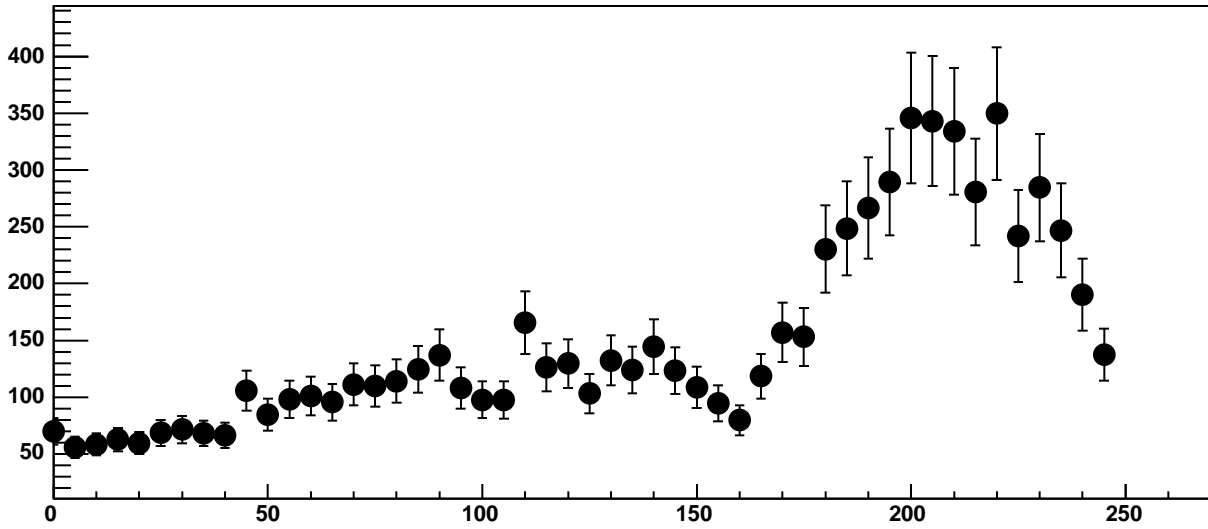


Chip 2, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

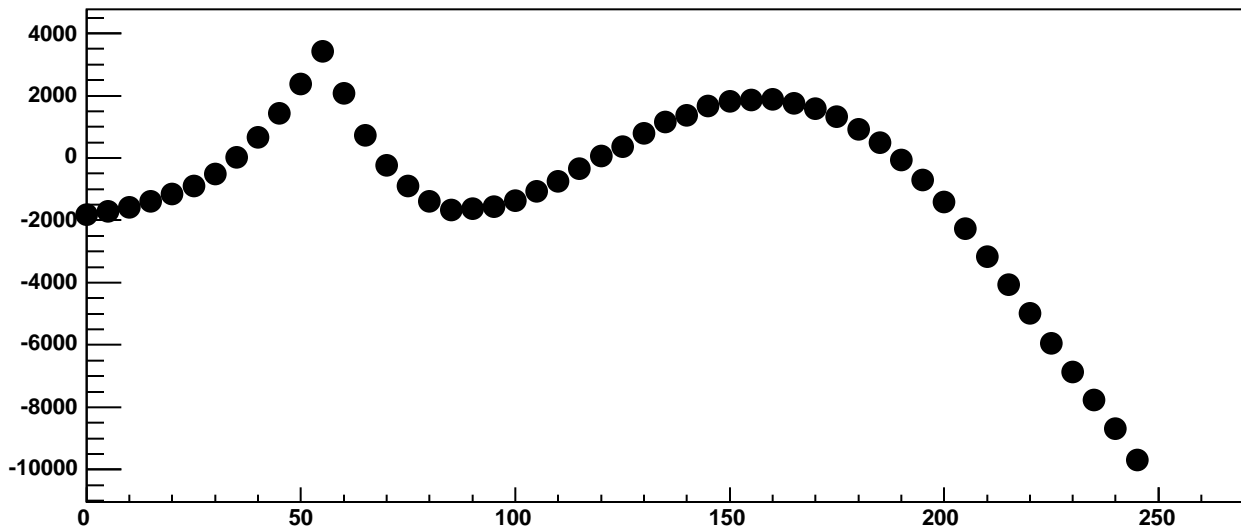


$\chi^2 / \text{ndf}$	2.251e+05 / 41
p0	-1236 ± 8.813
p1	55.55 ± 0.03428
p2	2.753e+04 ± 57.31
p3	45.59 ± 0.1047
p4	-35.32 ± 0.3074

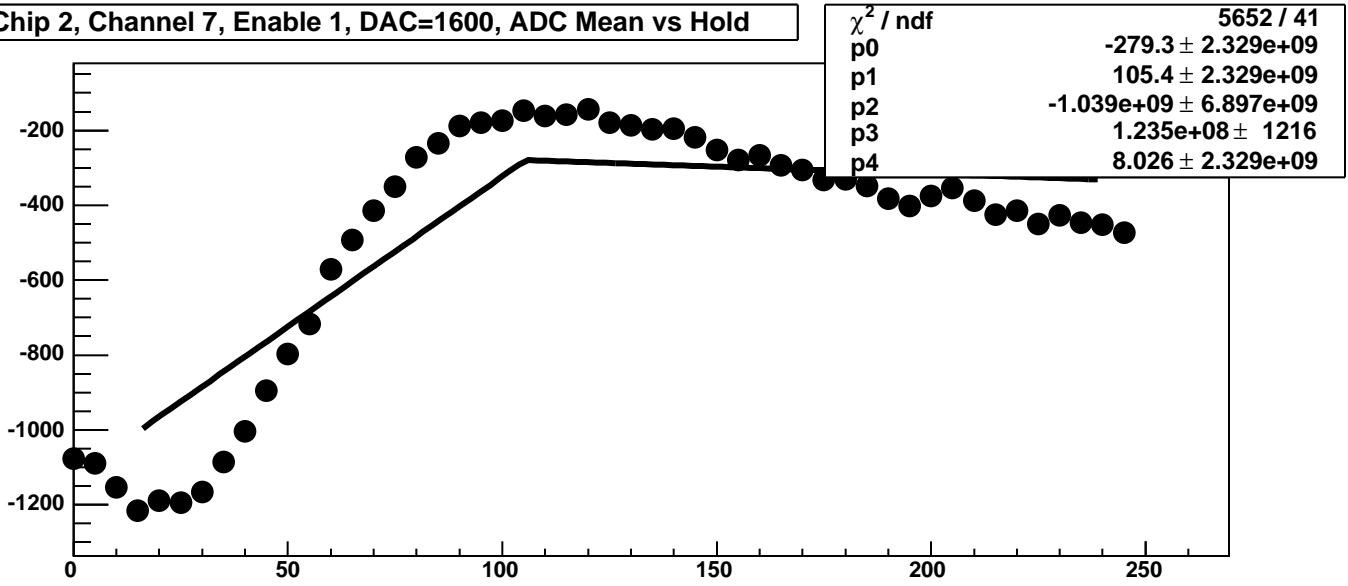
Chip 2, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



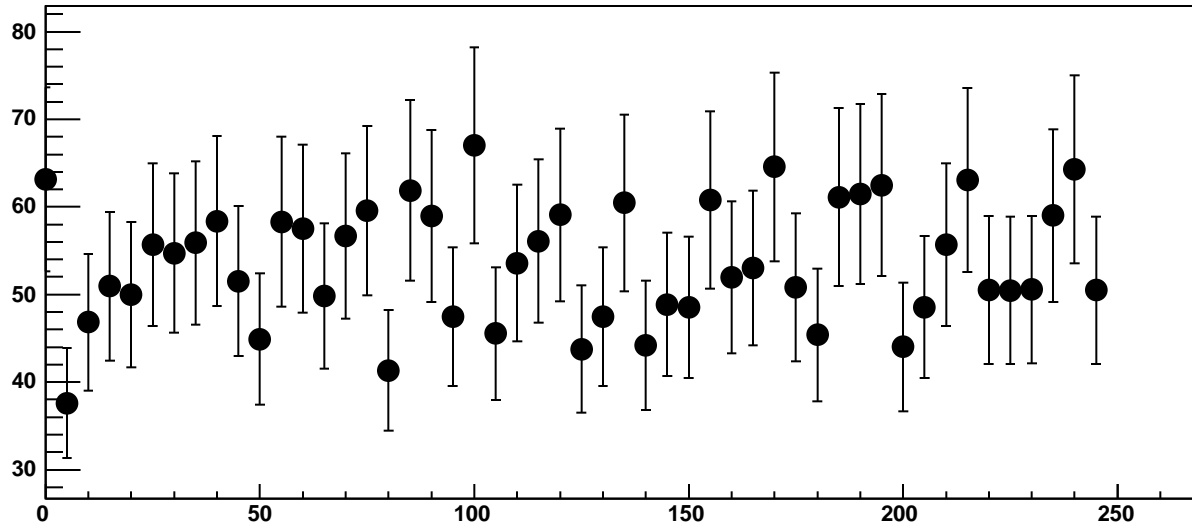
Chip 2, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold



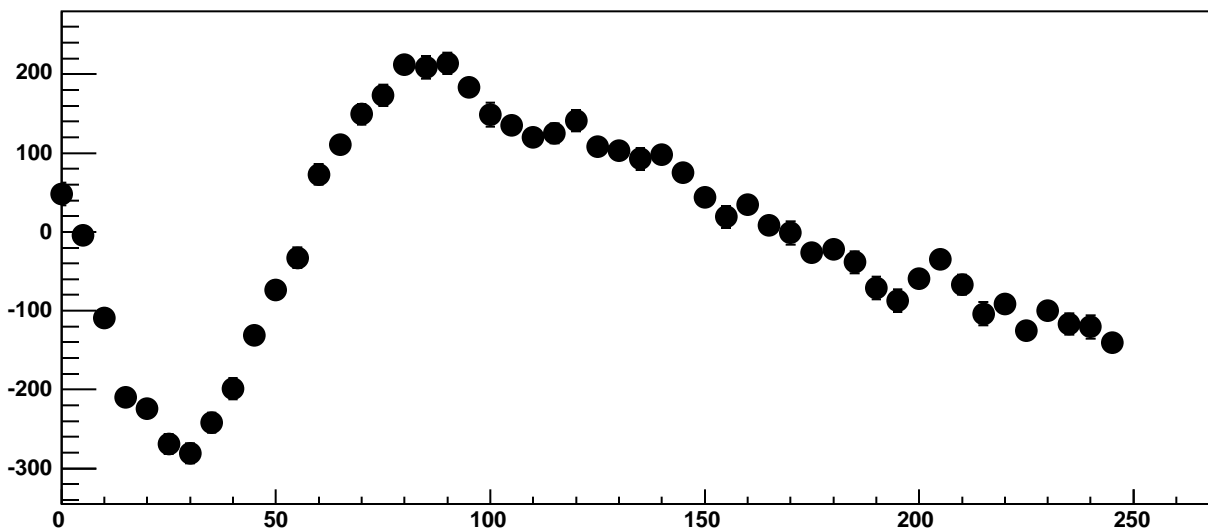
Chip 2, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold



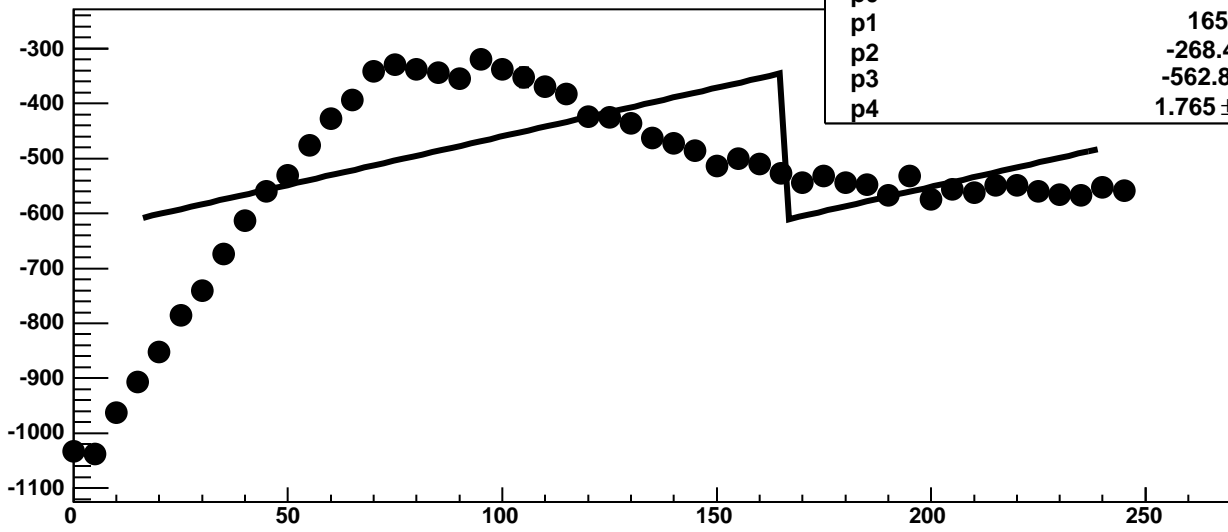
Chip 2, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



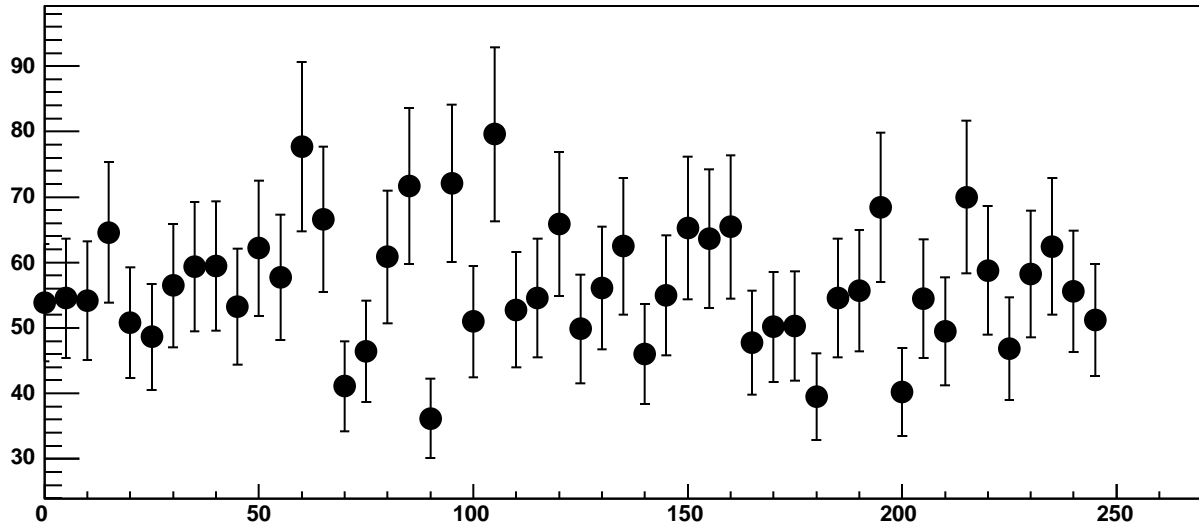
Chip 2, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold



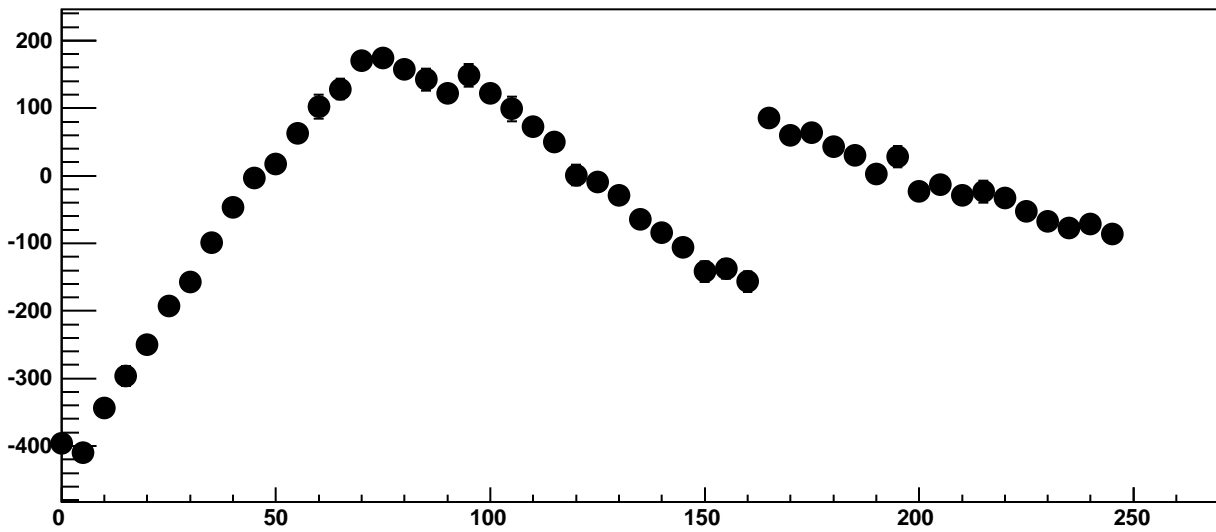
Chip 2, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold



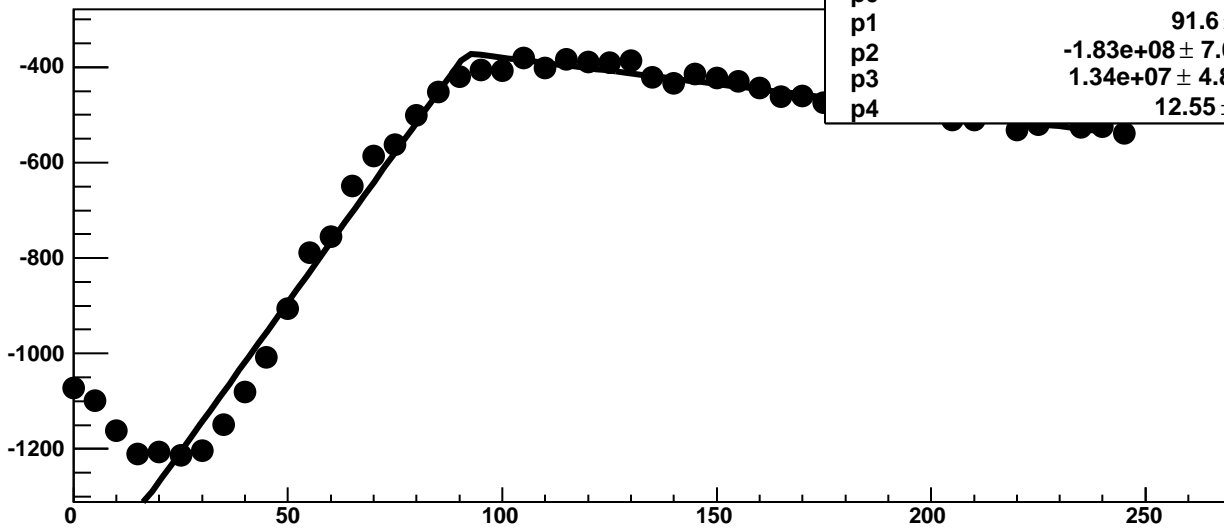
Chip 2, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



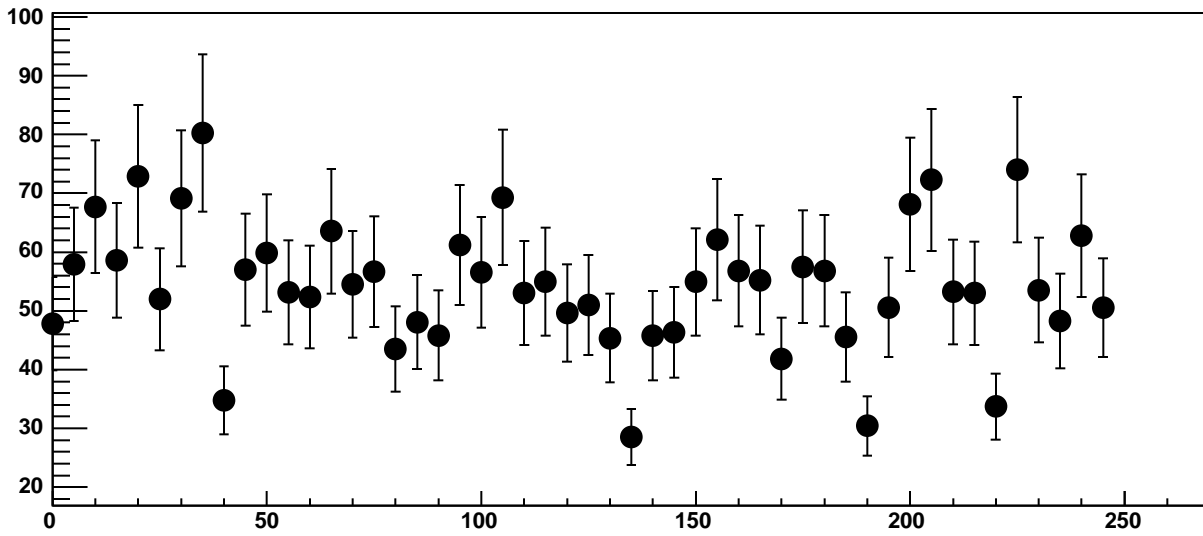
Chip 2, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold



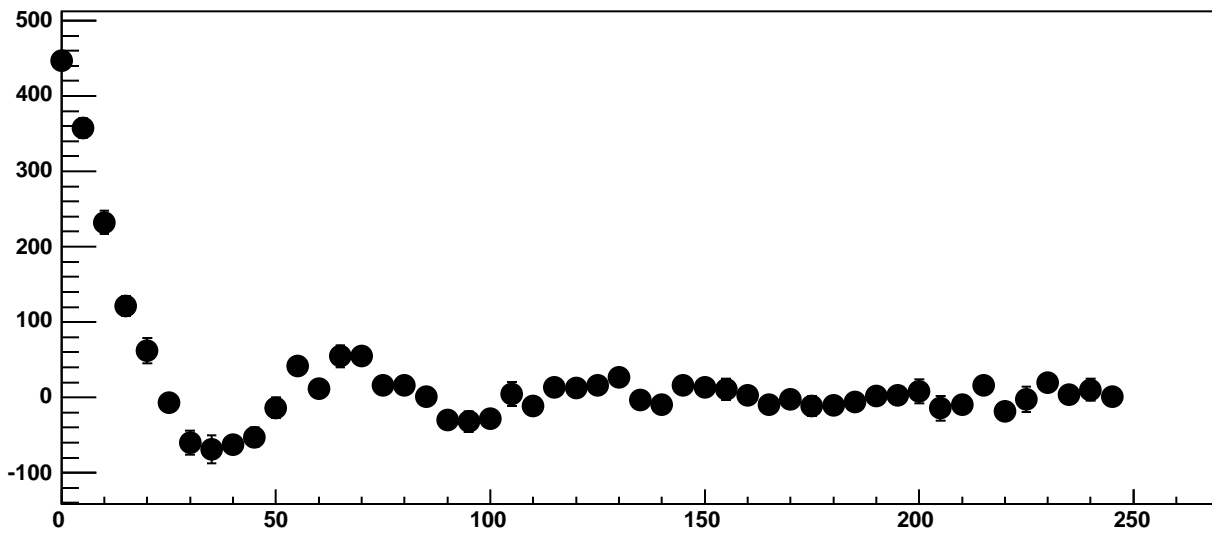
Chip 2, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold



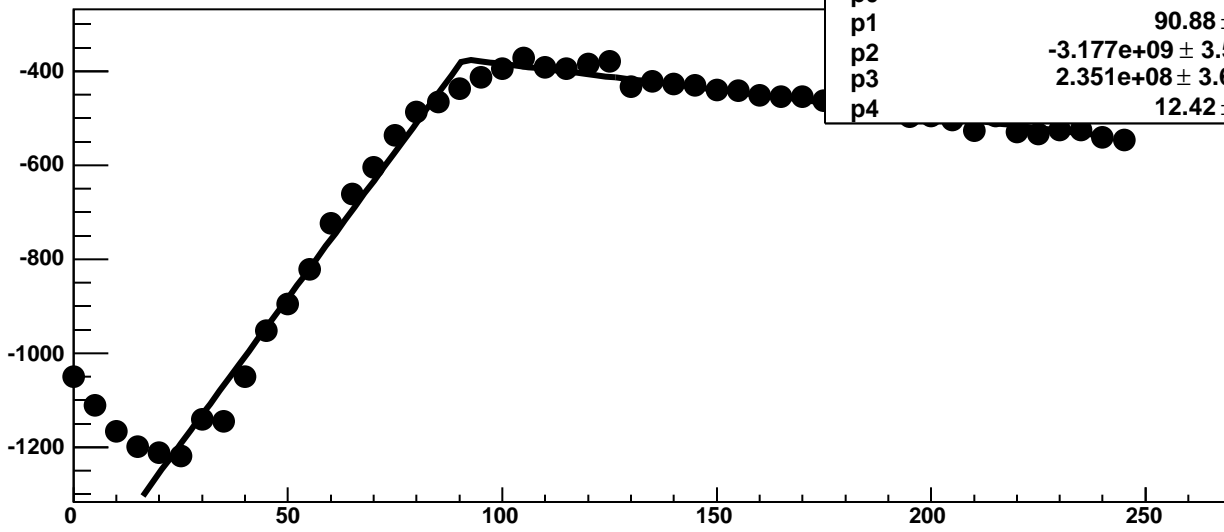
Chip 2, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

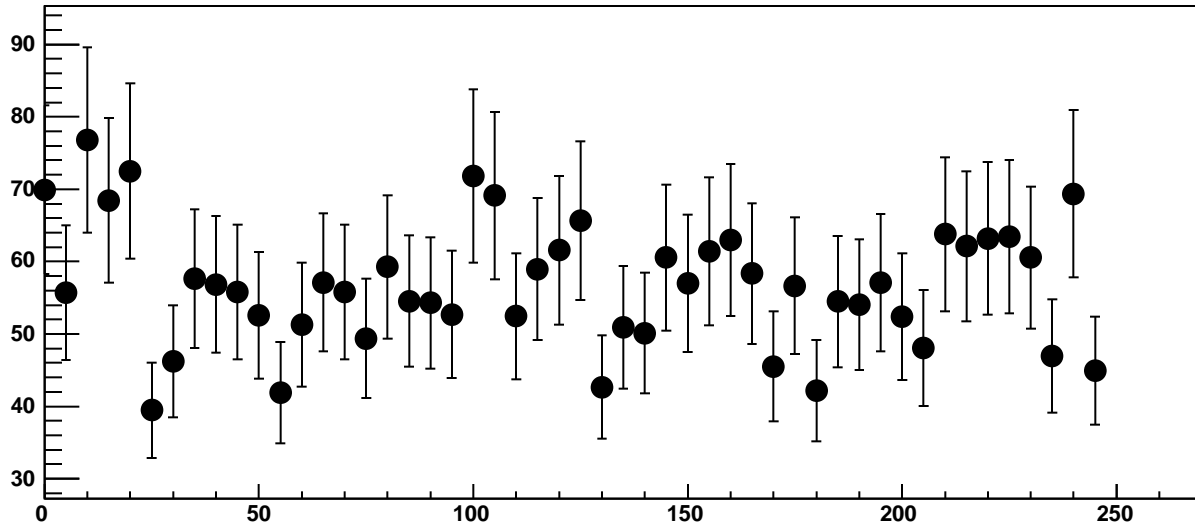


Chip 2, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

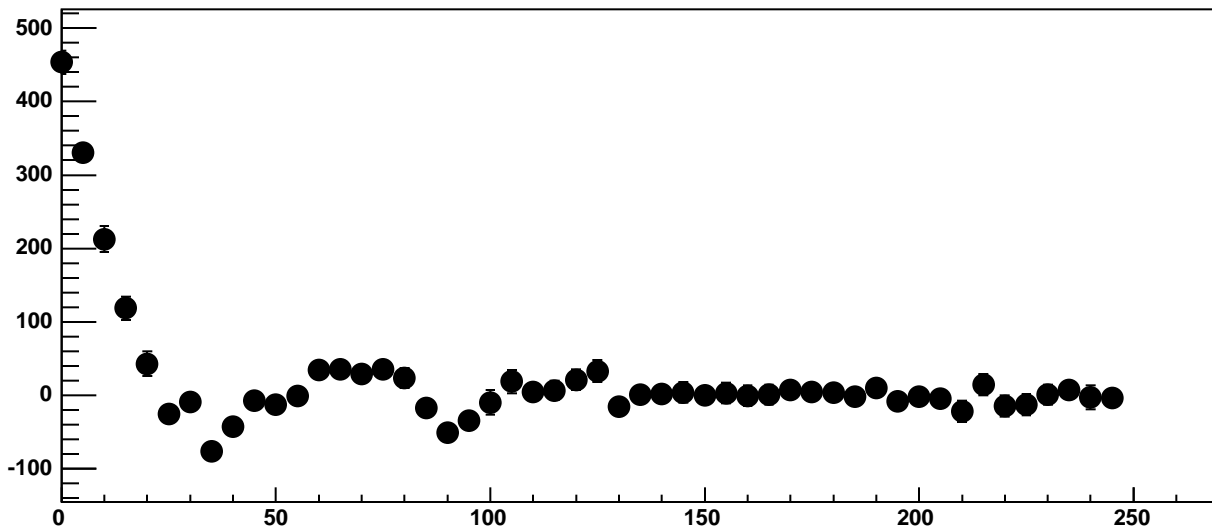


$\chi^2 / \text{ndf}$	197.6 / 41
p0	$-374.5 \pm 4.512$
p1	$90.88 \pm 0.5769$
p2	$-3.177\text{e}+09 \pm 3.507\text{e}+07$
p3	$2.351\text{e}+08 \pm 3.693\text{e}+05$
p4	$12.42 \pm 0.1367$

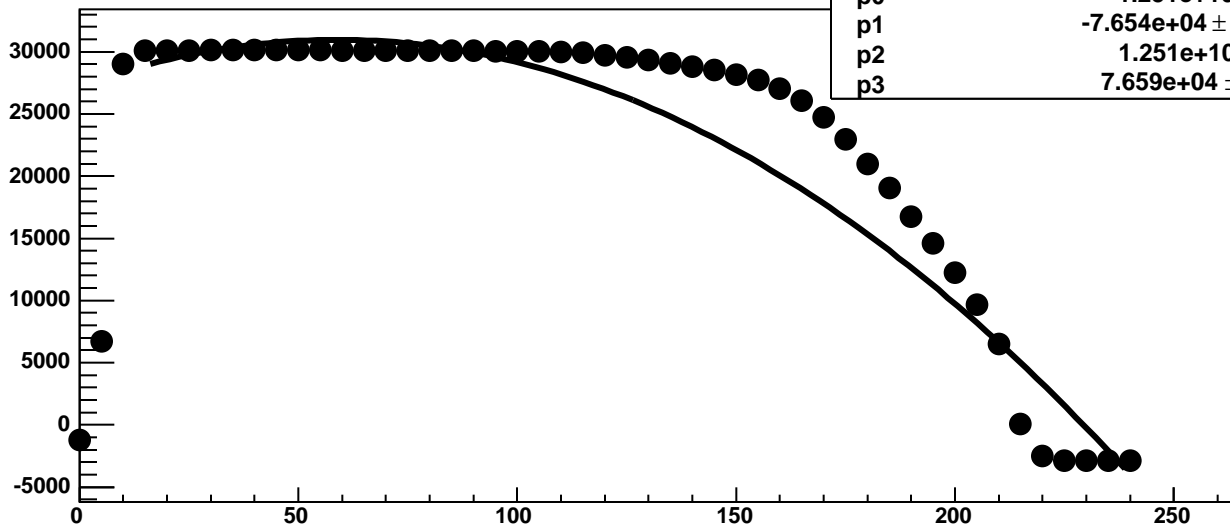
Chip 2, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

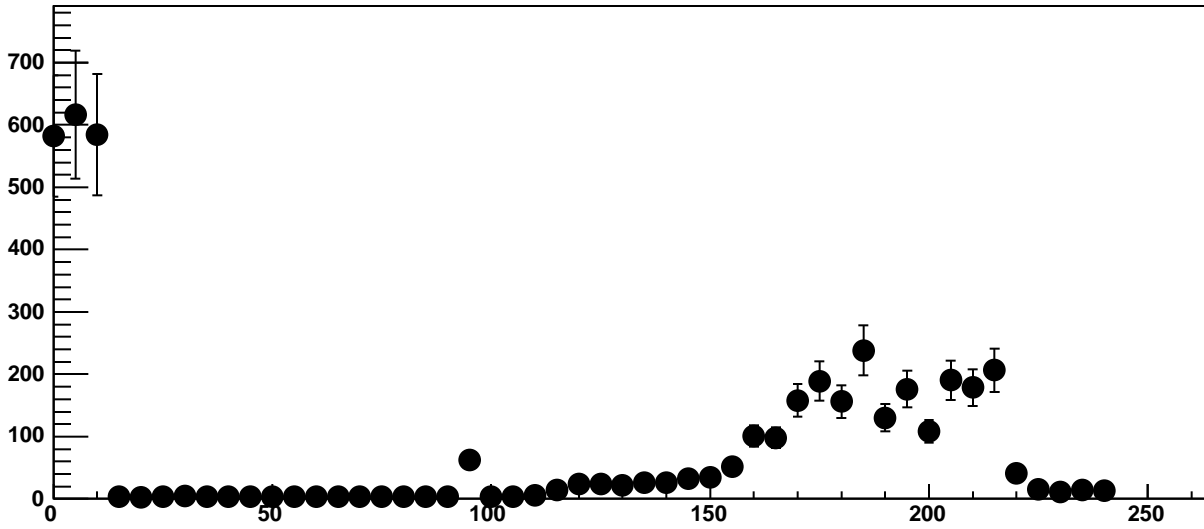


Chip 2, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold

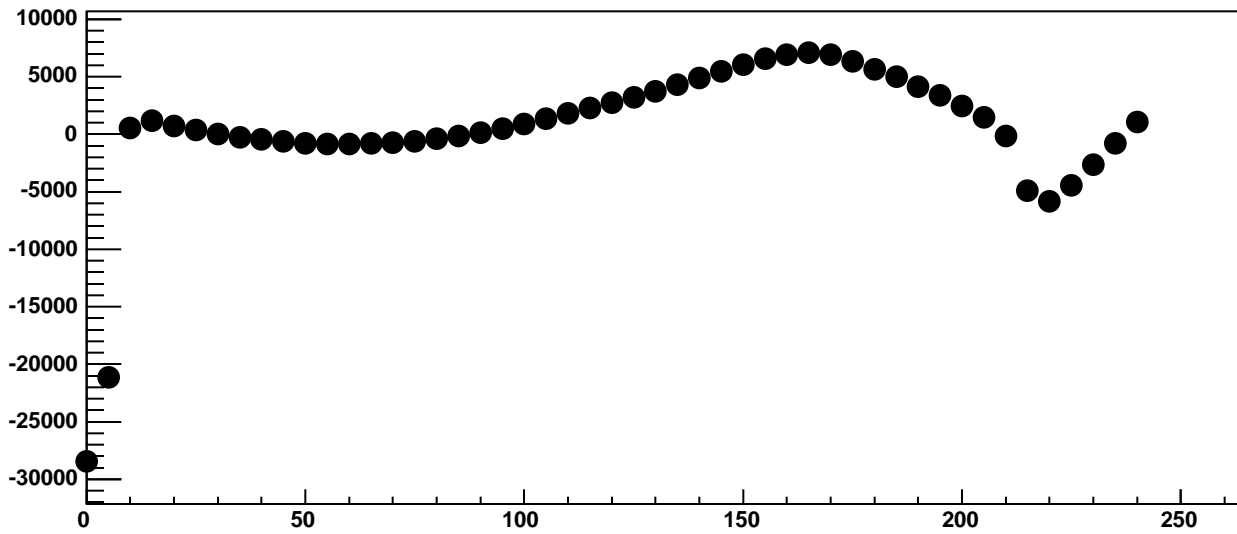


$\chi^2 / \text{ndf}$	2.31e+07 / 42
p0	-1.251e+10 $\pm$ 2.862
p1	-7.654e+04 $\pm$ 0.03463
p2	1.251e+10 $\pm$ 2.862
p3	7.659e+04 $\pm$ 0.0346

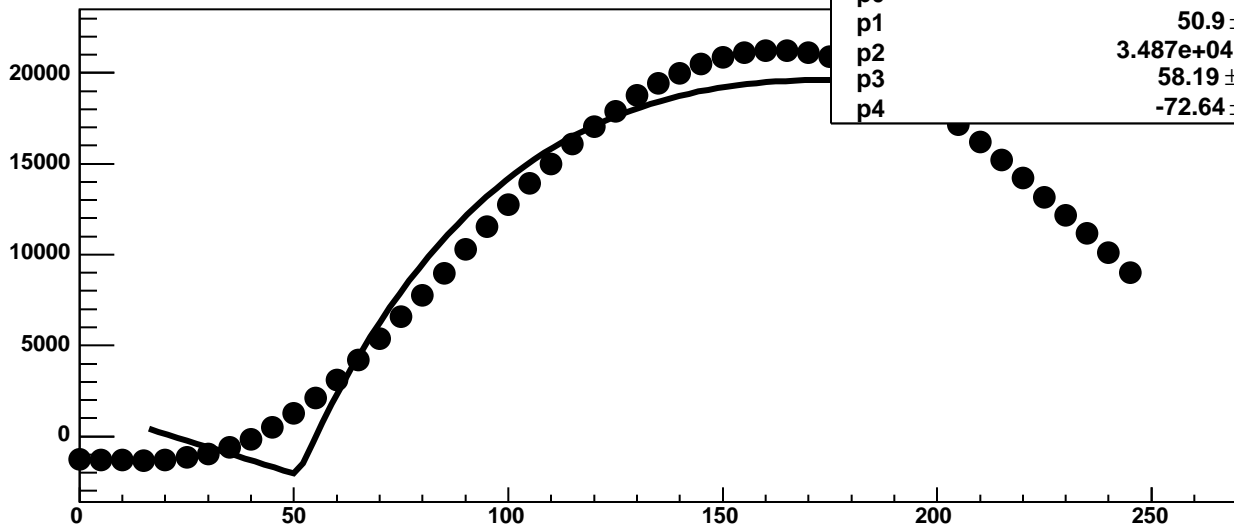
Chip 2, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold

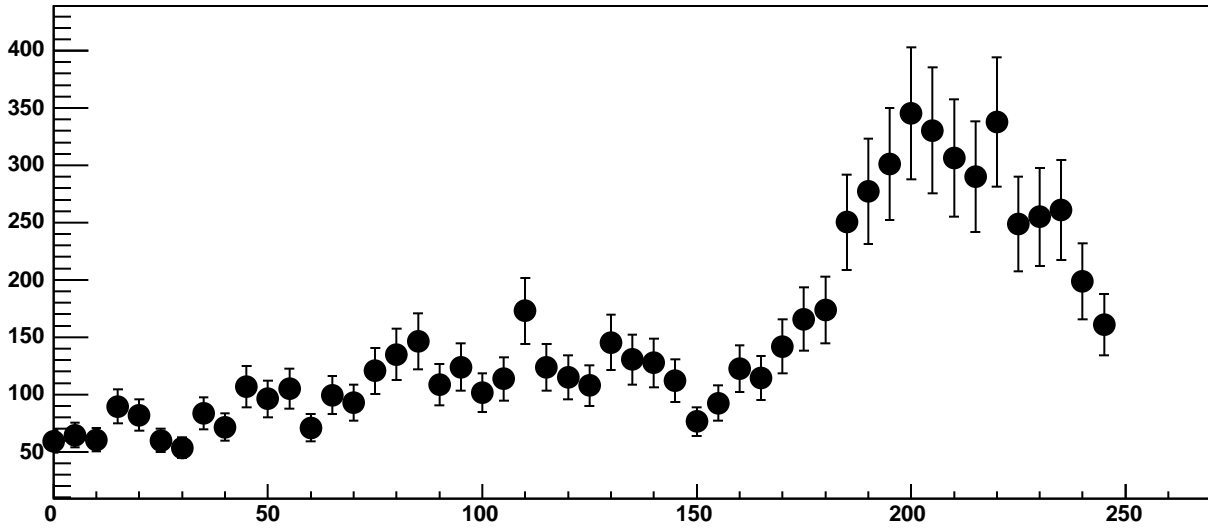


Chip 2, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

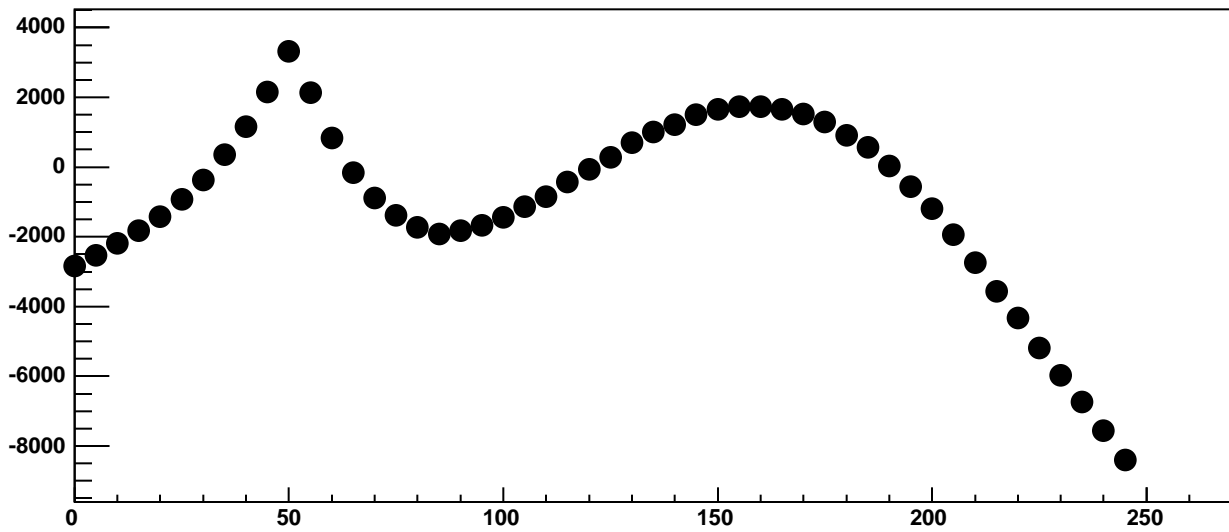


$\chi^2 / \text{ndf}$	1.929e+05 / 41
p0	-2112 ± 8.906
p1	50.9 ± 0.0311
p2	3.487e+04 ± 84.07
p3	58.19 ± 0.1364
p4	-72.64 ± 0.4021

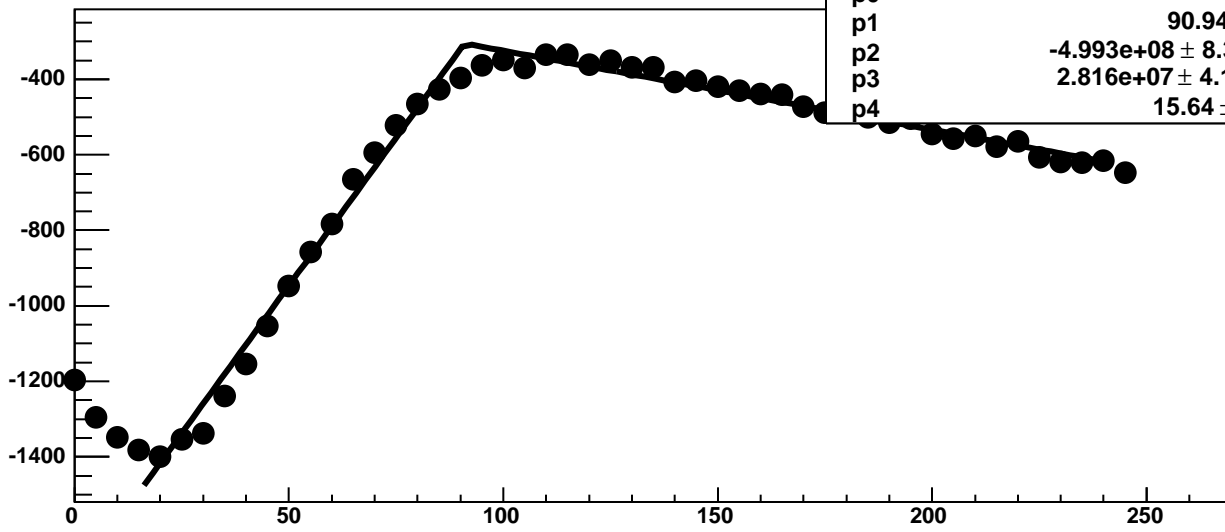
Chip 2, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

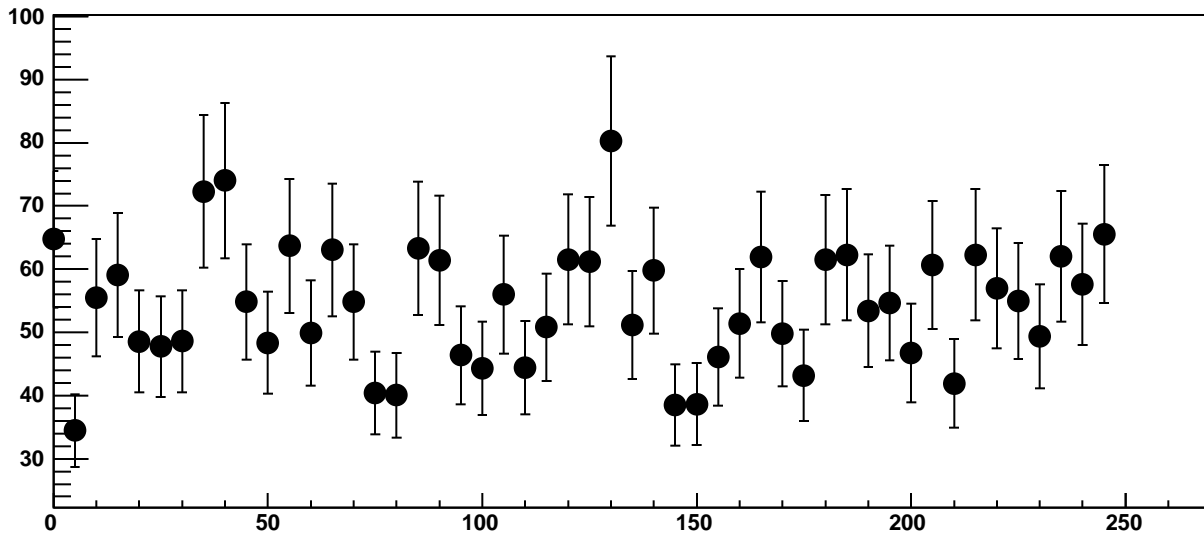


Chip 2, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

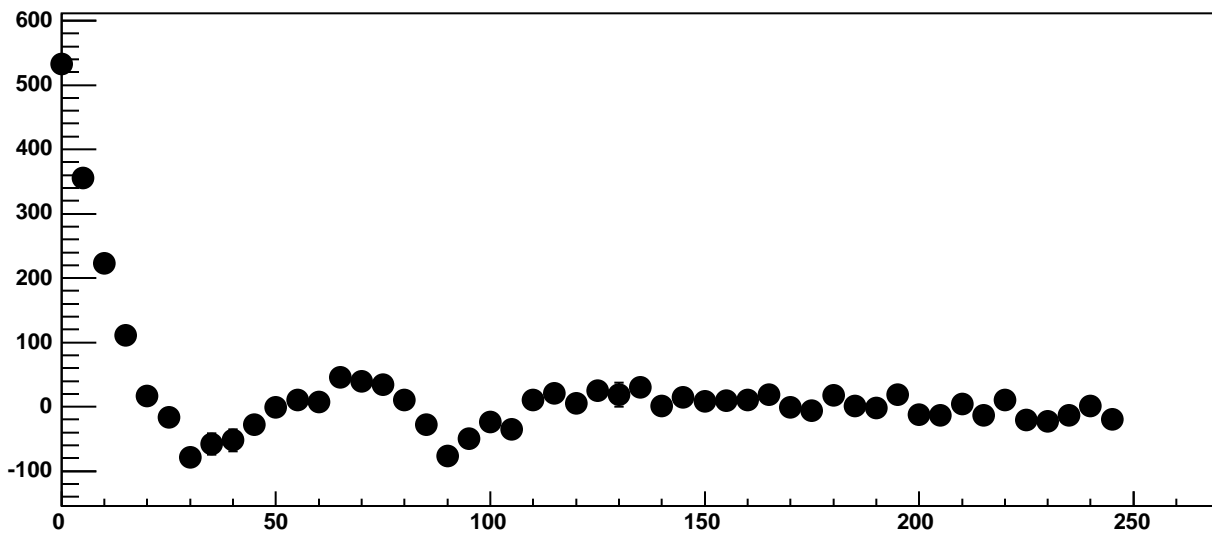


$\chi^2 / \text{ndf}$	290.5 / 41
p0	$-305.7 \pm 3.859$
p1	$90.94 \pm 0.404$
p2	$-4.993\text{e}+08 \pm 8.351\text{e}+06$
p3	$2.816\text{e}+07 \pm 4.121\text{e}+05$
p4	$15.64 \pm 0.1304$

Chip 2, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

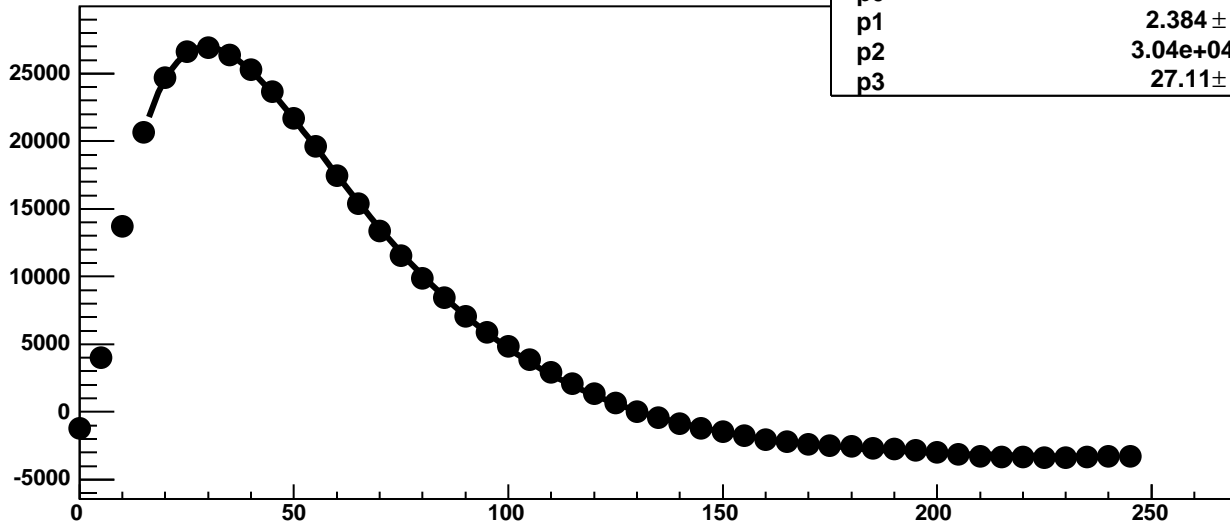


Chip 2, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



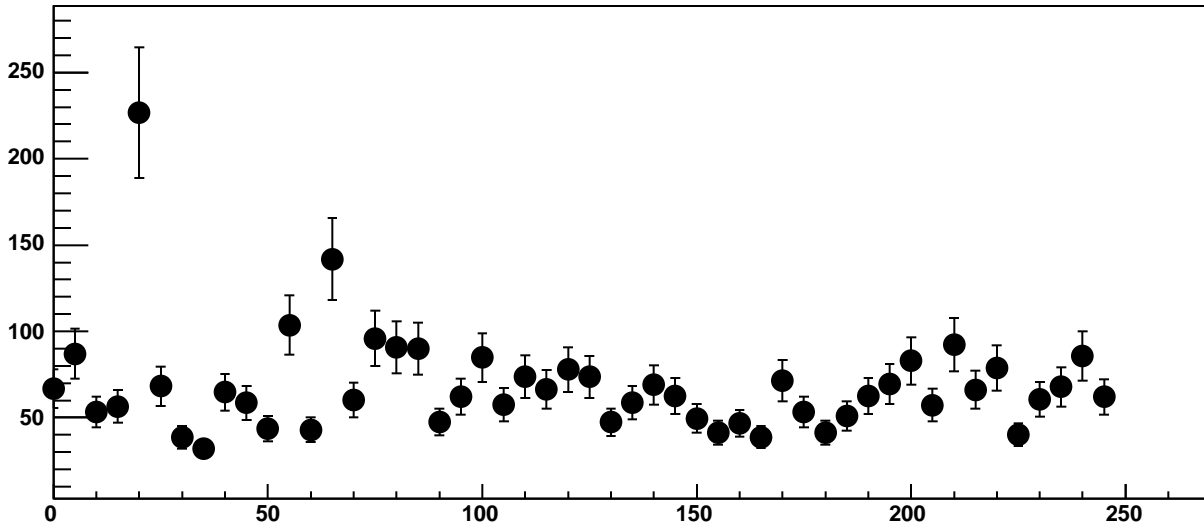


Chip 2, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold

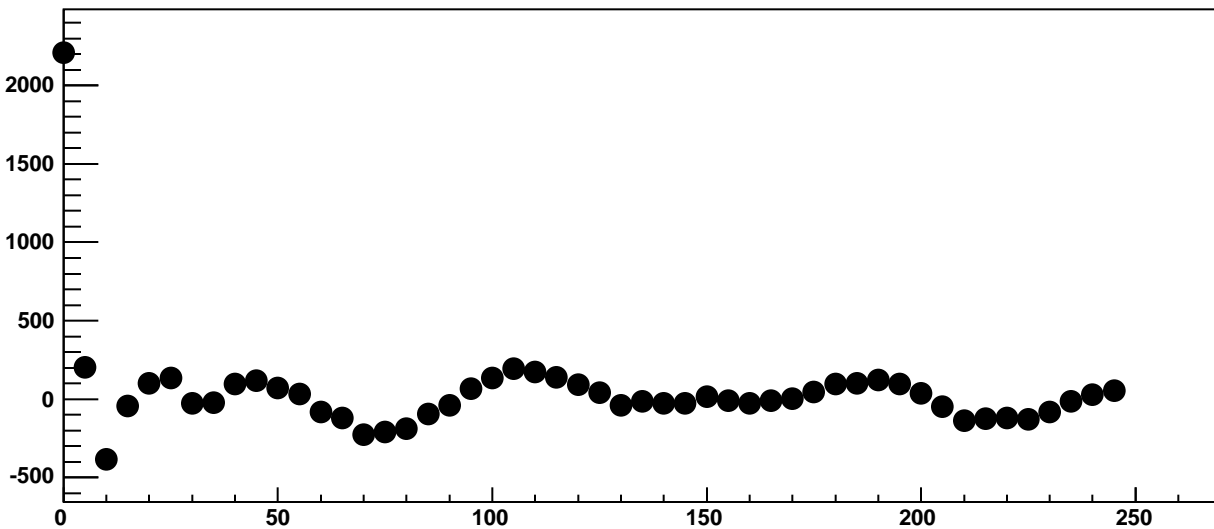


$\chi^2 / \text{ndf}$	2083 / 42
p0	-3434 ± 3.545
p1	2.384 ± 0.01514
p2	3.04e+04 ± 5.236
p3	27.11 ± 0.01033

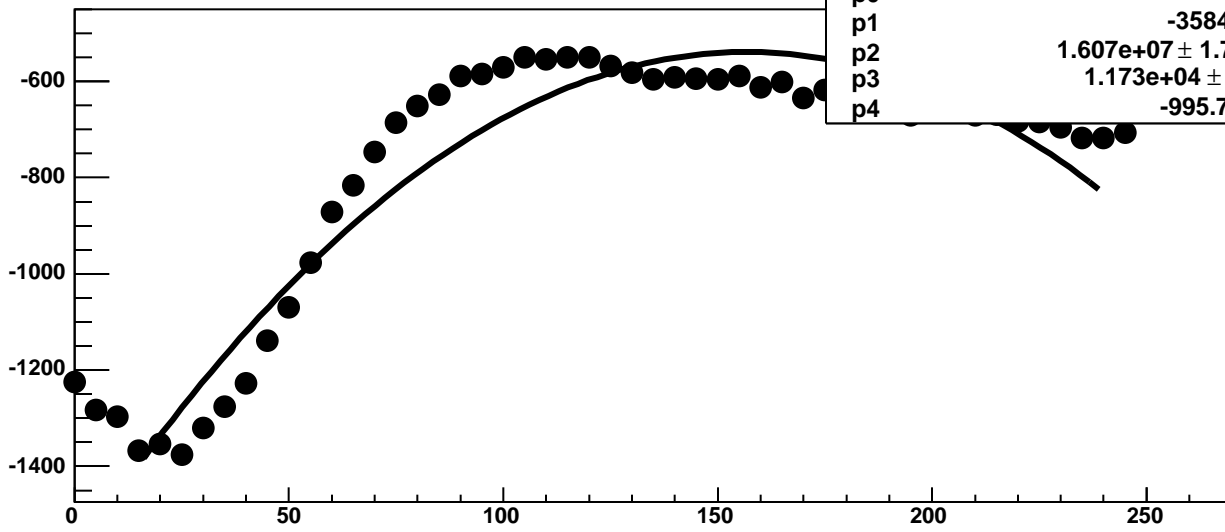
Chip 2, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold

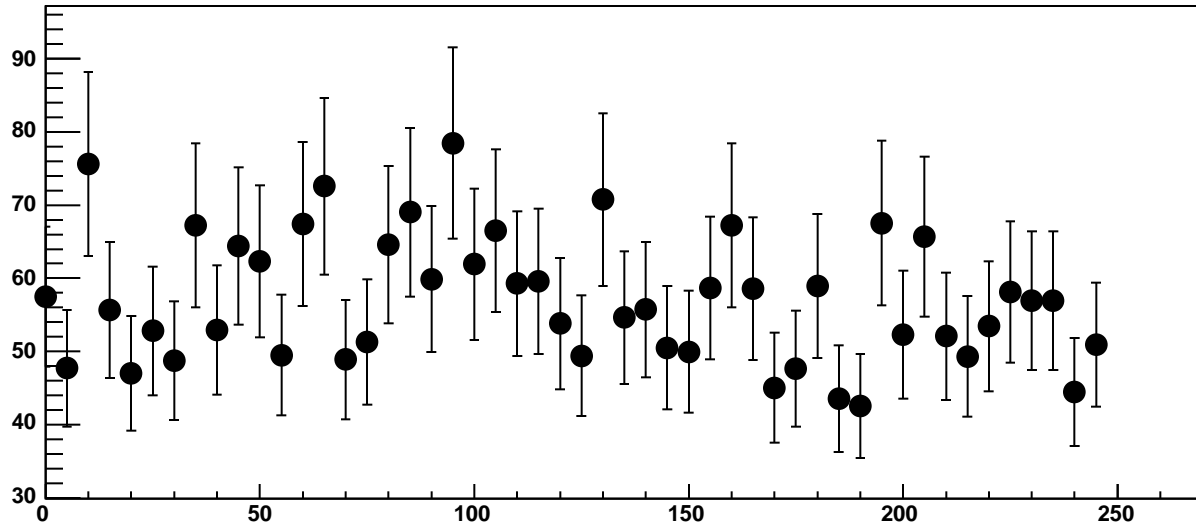


Chip 2, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

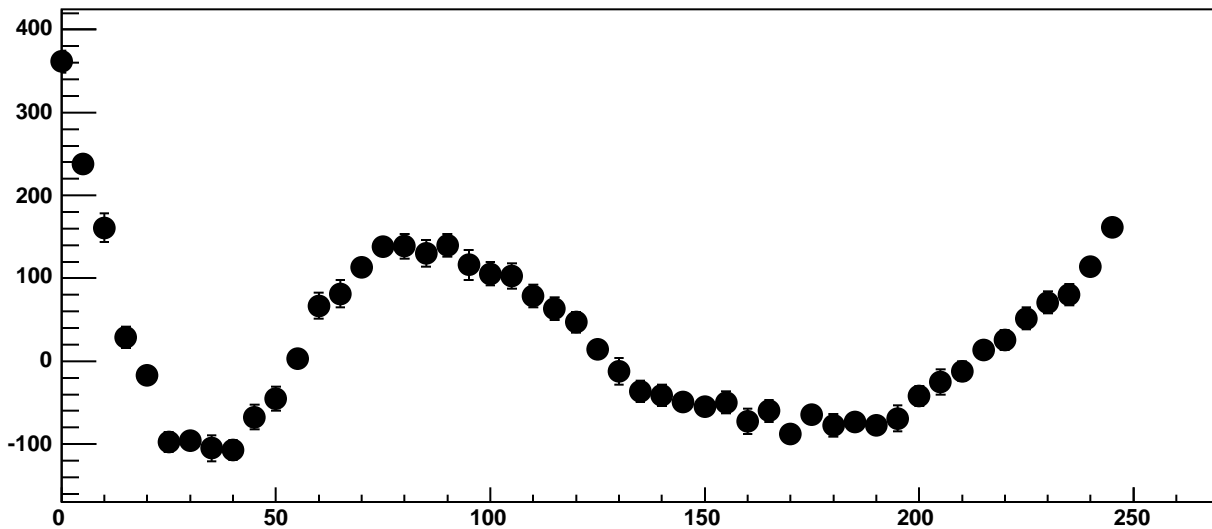


$\chi^2 / \text{ndf}$	1677 / 41
p0	$-6.629\text{e}+05 \pm 7181$
p1	$-3584 \pm 0.341$
p2	$1.607\text{e}+07 \pm 1.761\text{e}+05$
p3	$1.173\text{e}+04 \pm 0.02588$
p4	$-995.7 \pm 10.93$

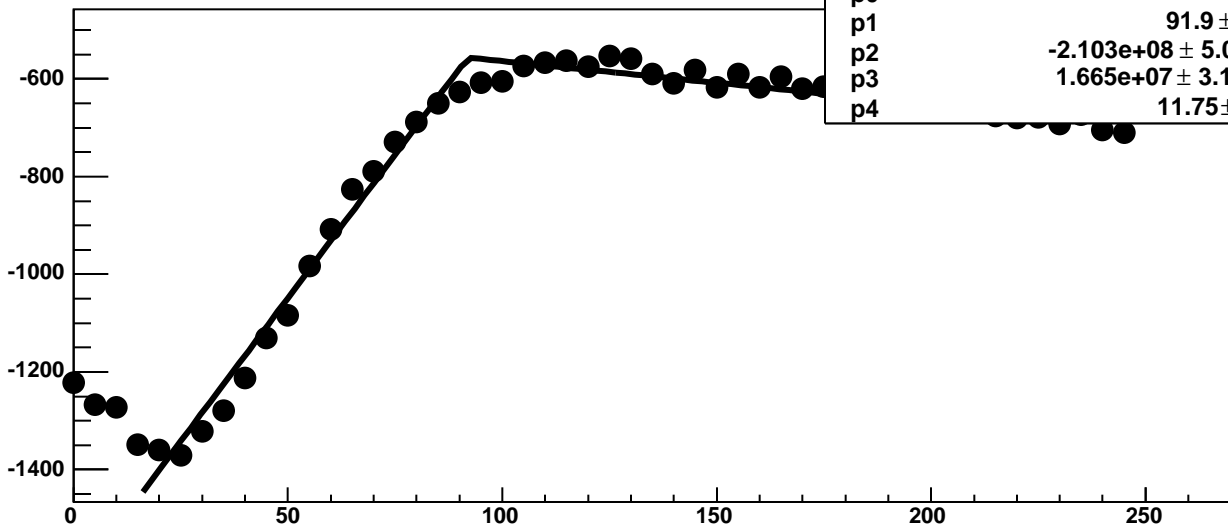
Chip 2, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

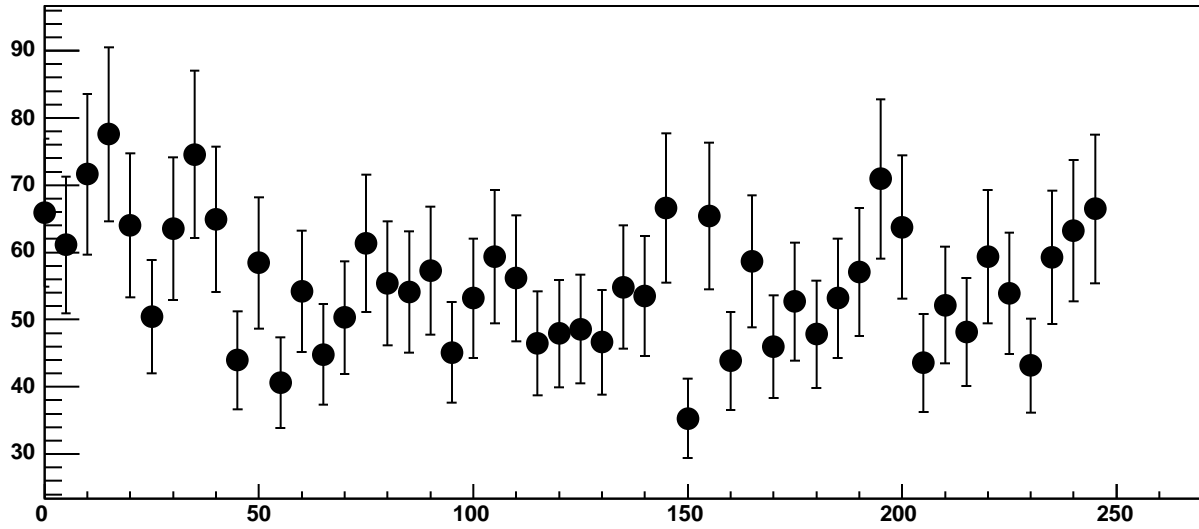


Chip 2, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

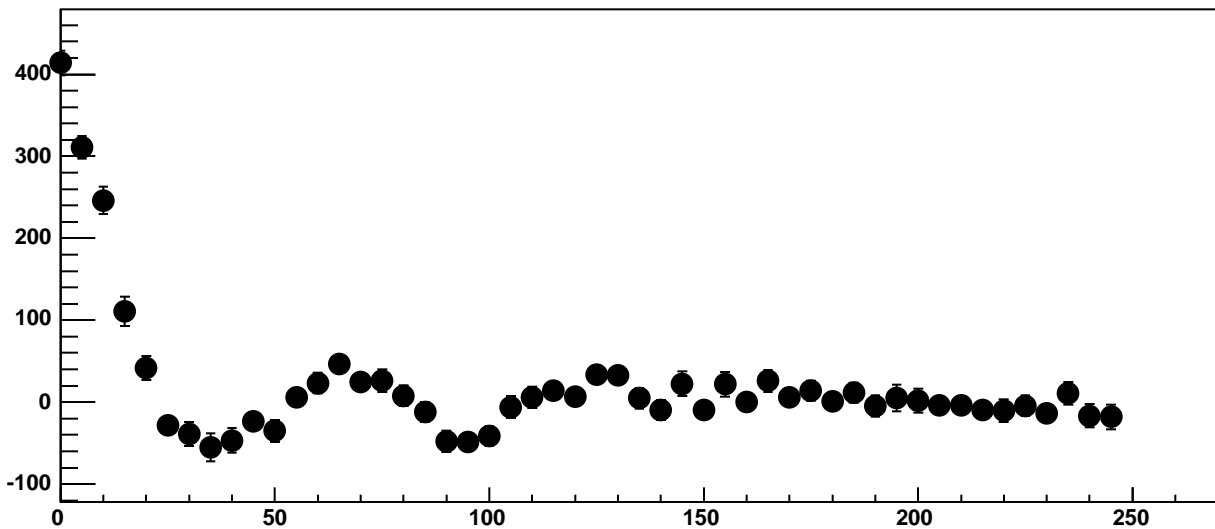


$\chi^2 / \text{ndf}$	211.6 / 41
p0	$-556.5 \pm 4.035$
p1	$91.9 \pm 0.6025$
p2	$-2.103\text{e}+08 \pm 5.082\text{e}+06$
p3	$1.665\text{e}+07 \pm 3.197\text{e}+05$
p4	$11.75 \pm 0.1487$

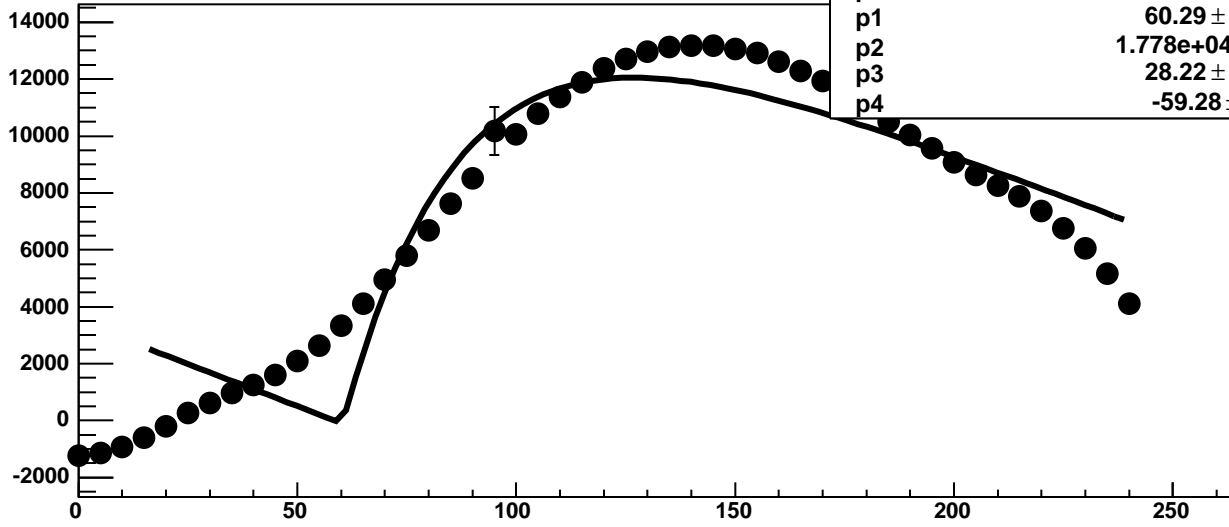
Chip 2, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

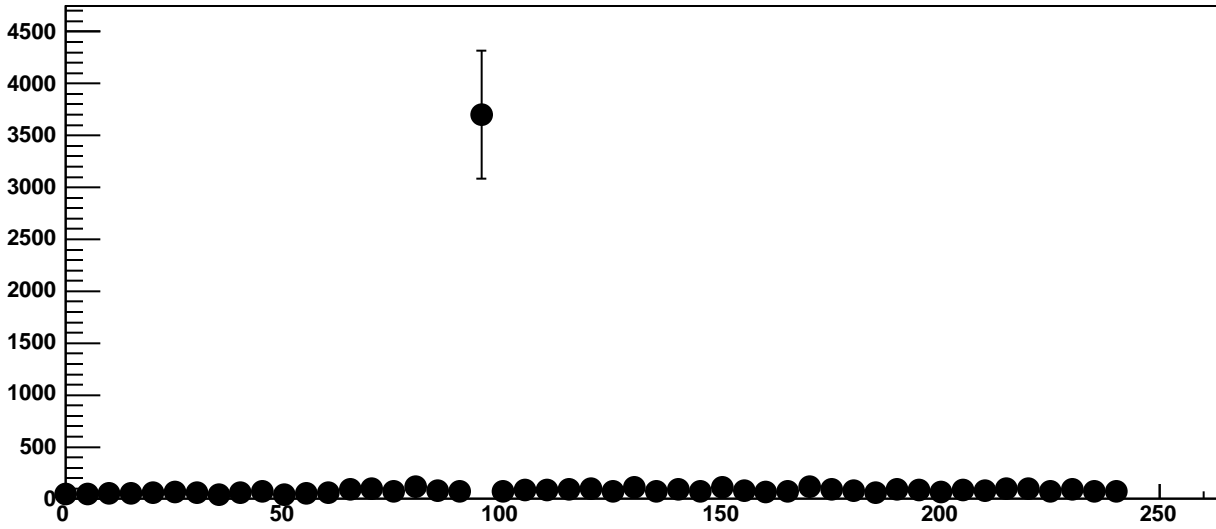


Chip 2, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold

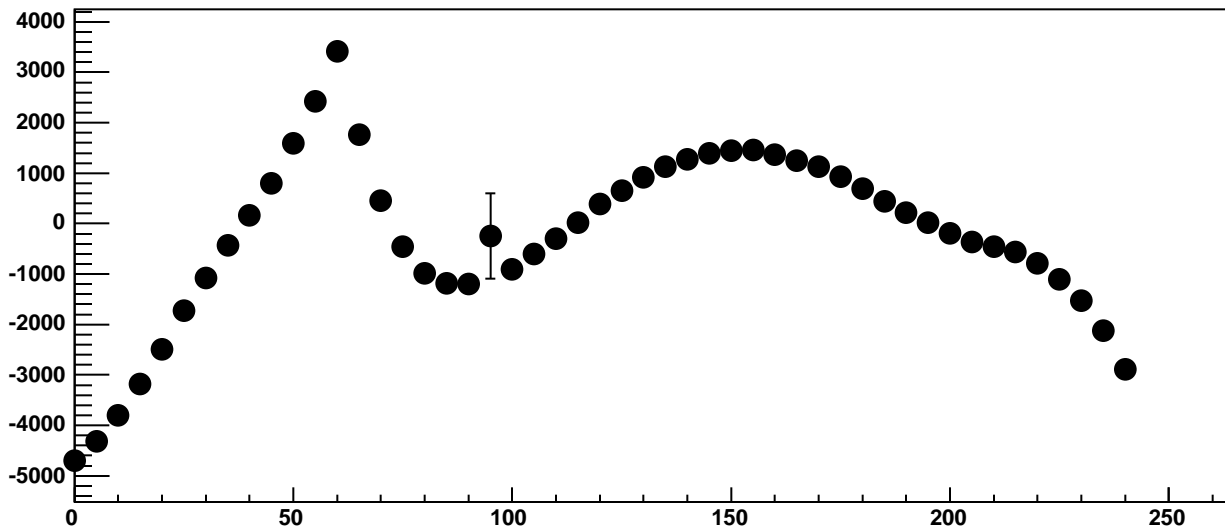


$\chi^2 / \text{ndf}$	3.71e+05 / 41
p0	-102.5 ± 4.768
p1	60.29 ± 0.03207
p2	1.778e+04 ± 21.97
p3	28.22 ± 0.05896
p4	-59.28 ± 0.1297

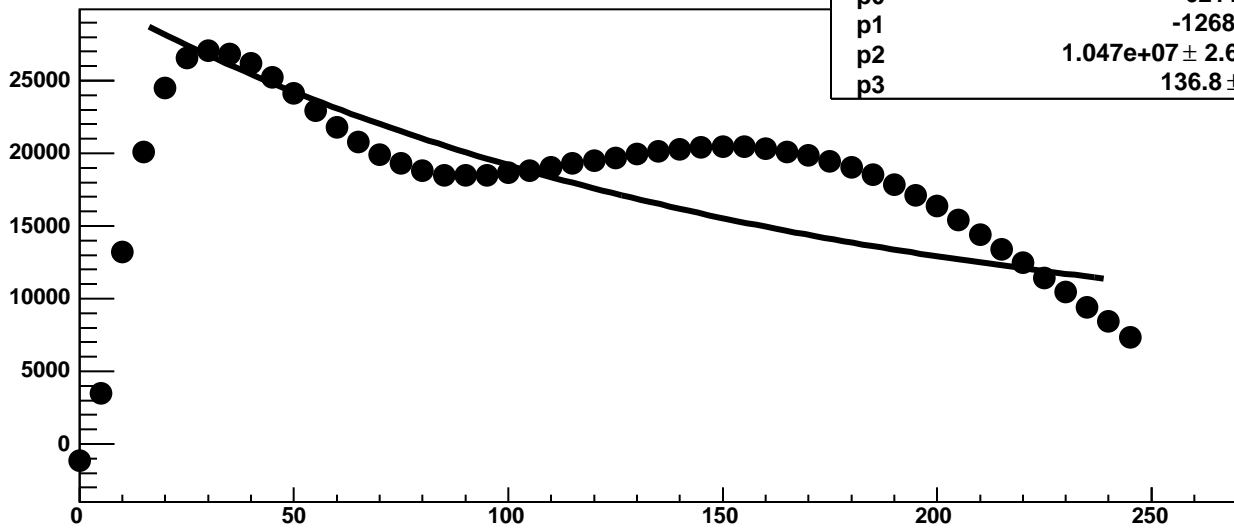
Chip 2, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold

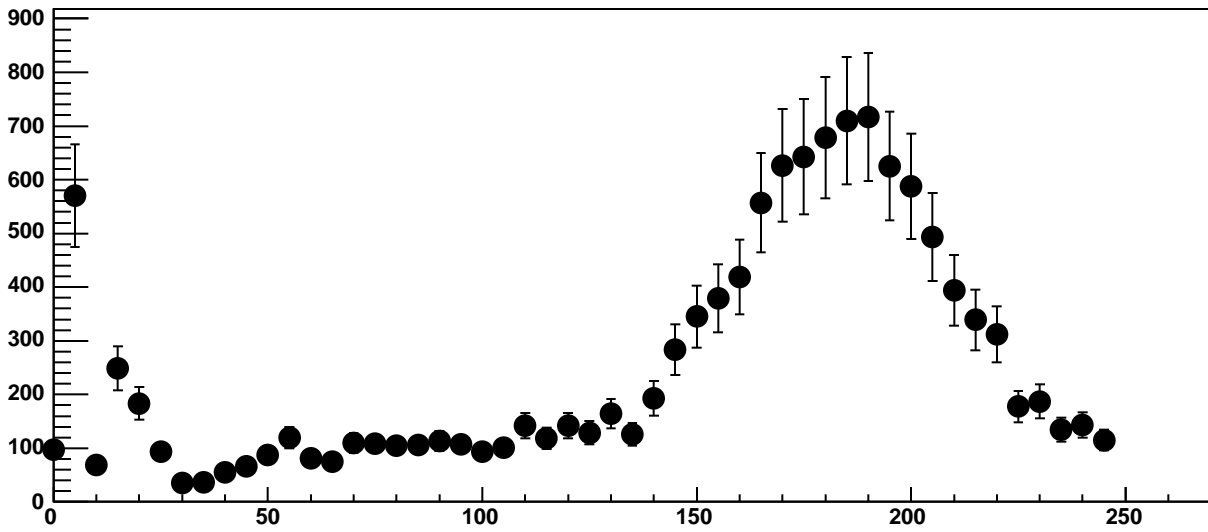


Chip 2, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold

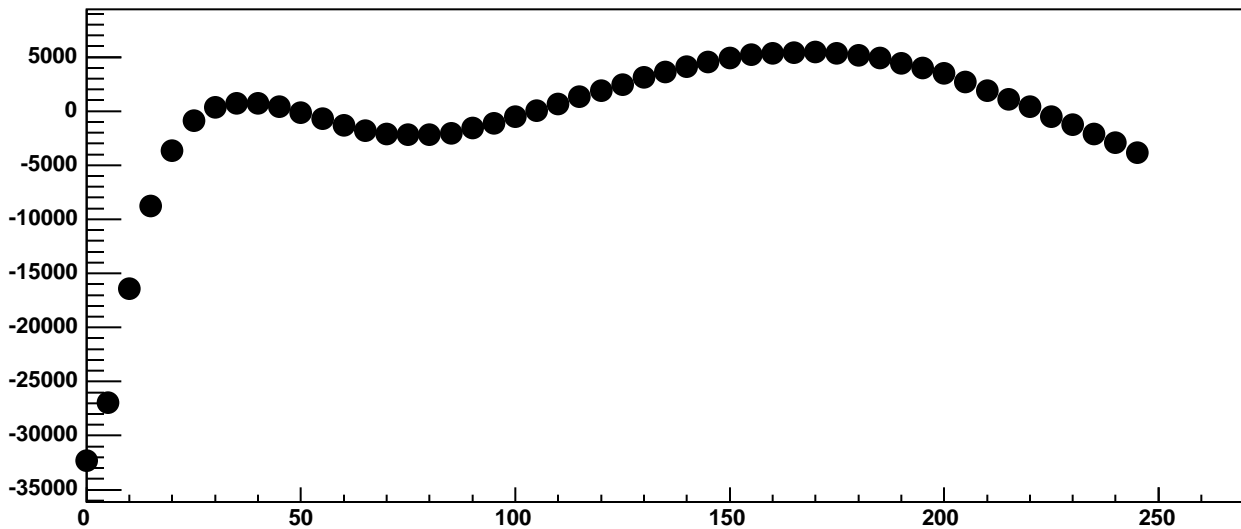


$\chi^2 / \text{ndf}$	1.815e+05 / 42
p0	6211 ± 69.45
p1	-1268 ± 8.374
p2	1.047e+07 ± 2.687e+05
p3	136.8 ± 0.7058

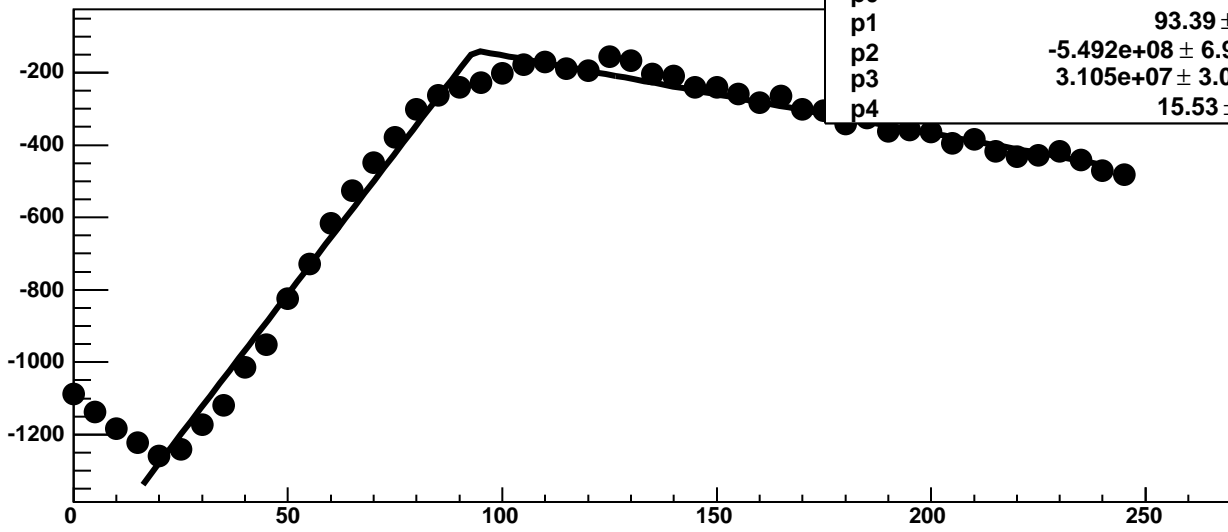
Chip 2, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold

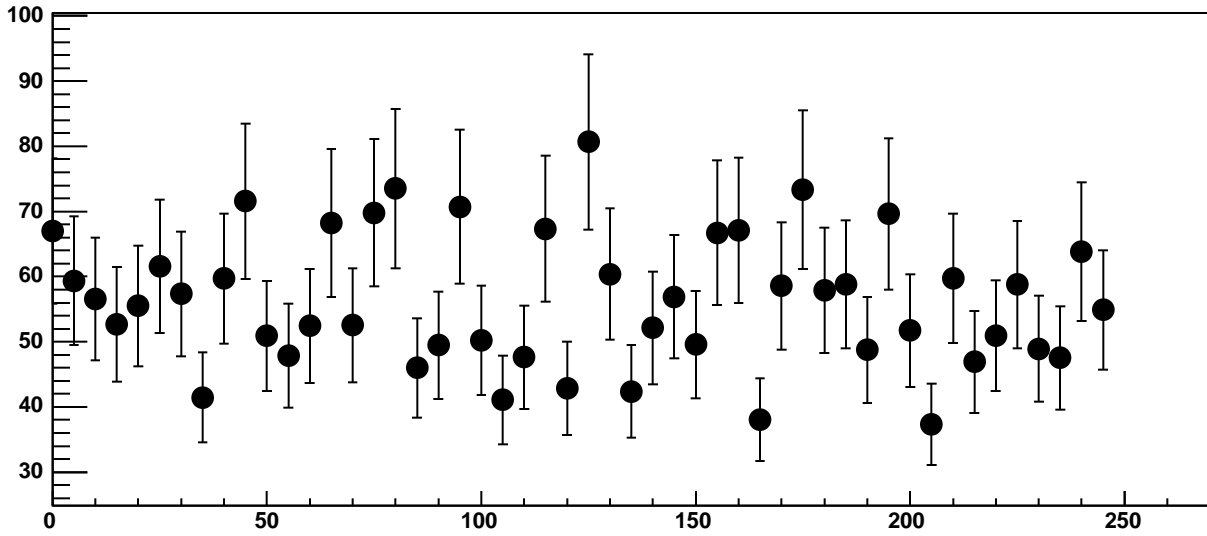


Chip 2, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

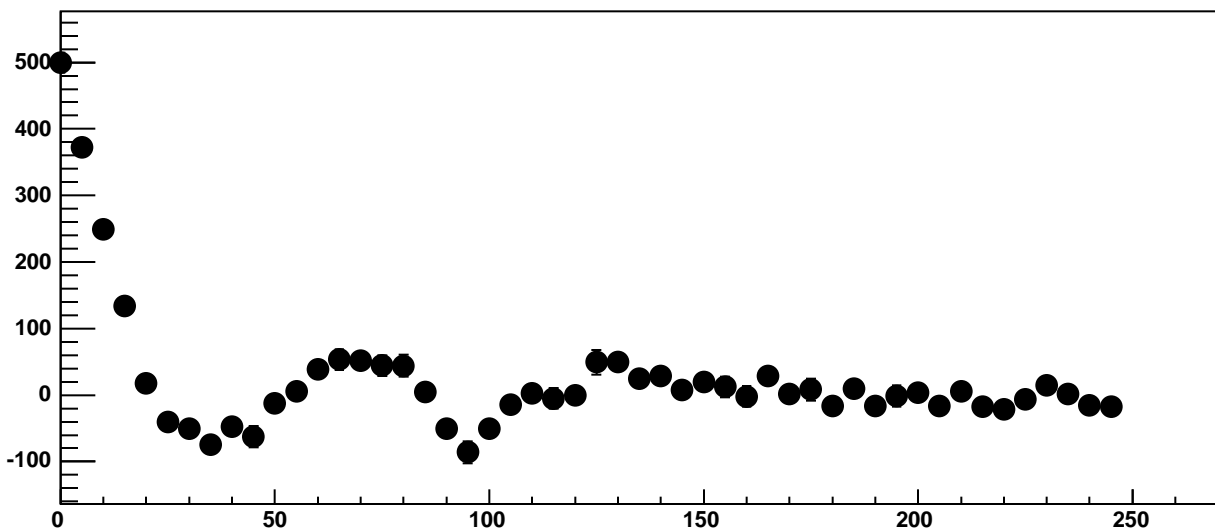


$\chi^2 / \text{ndf}$	426.4 / 41
p0	-137.7 $\pm$ 3.892
p1	93.39 $\pm$ 0.4343
p2	-5.492e+08 $\pm$ 6.916e+06
p3	3.105e+07 $\pm$ 3.042e+05
p4	15.53 $\pm$ 0.1341

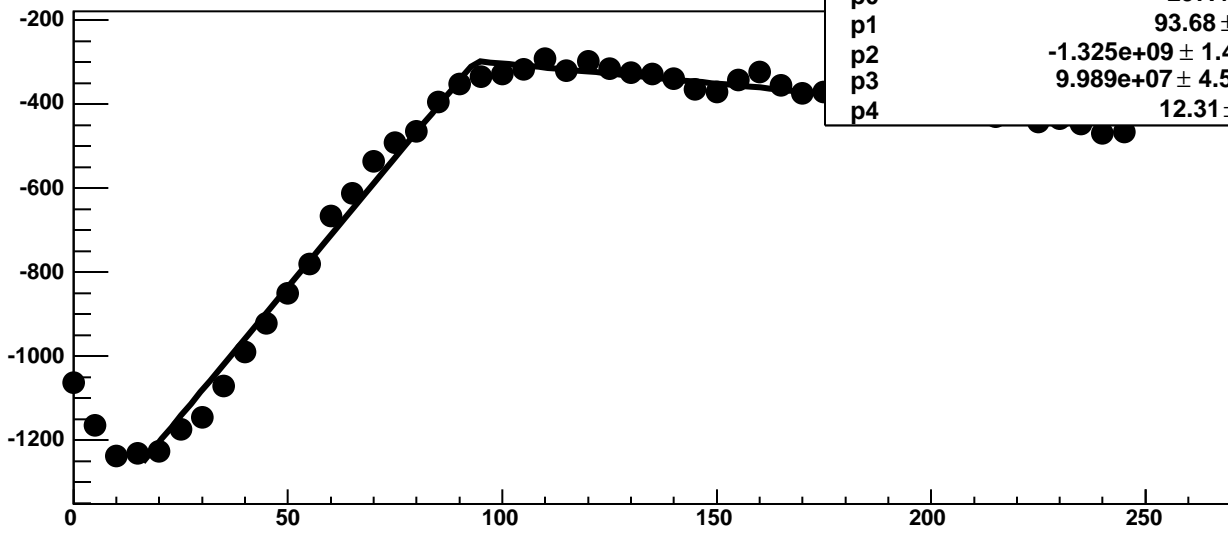
Chip 2, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

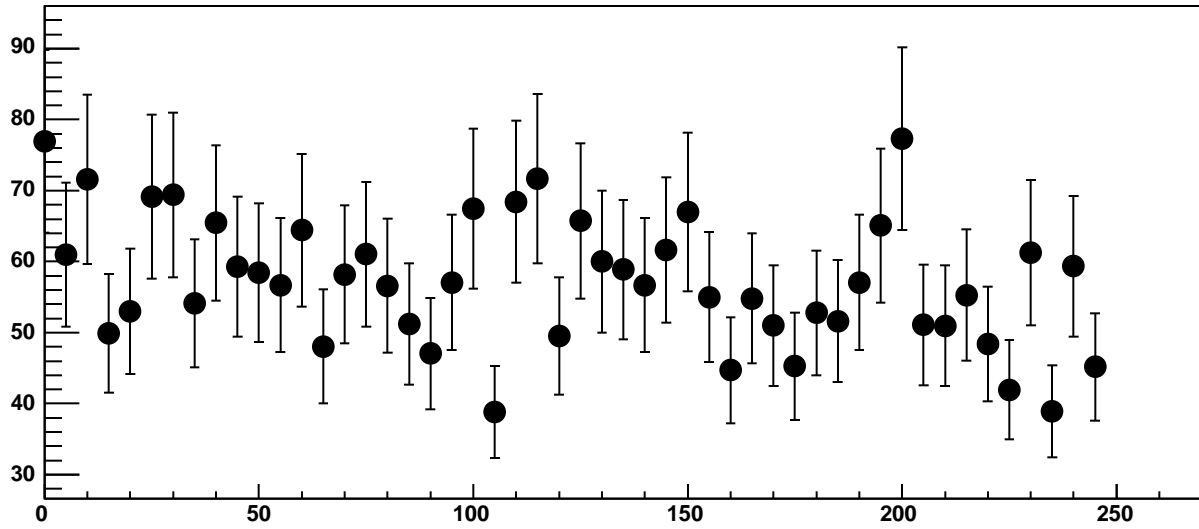


Chip 2, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

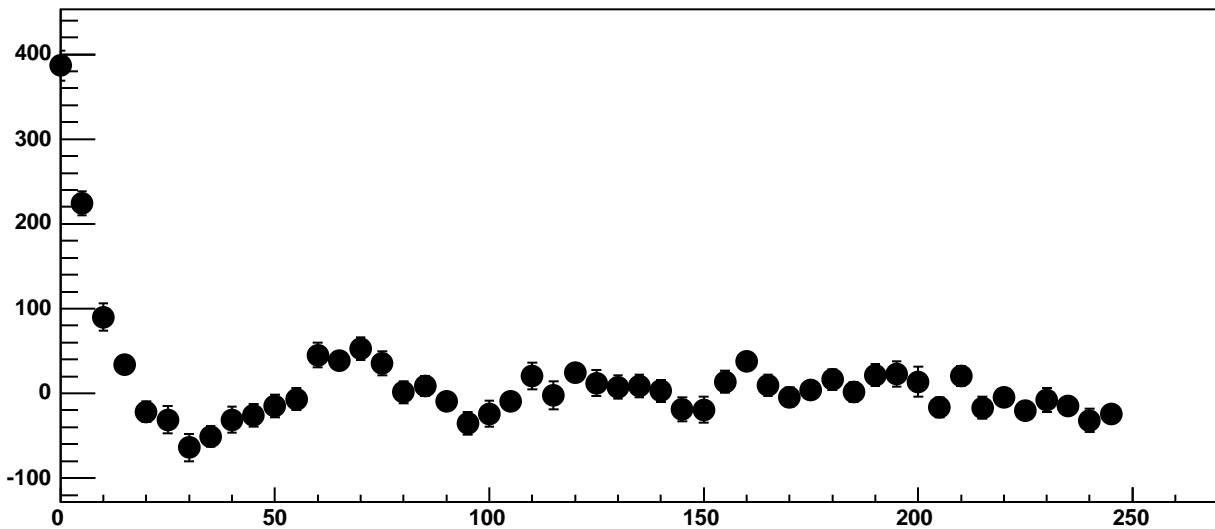


$\chi^2 / \text{ndf}$	168.2 / 41
p0	-297.4 ± 4.306
p1	93.68 ± 0.6069
p2	-1.325e+09 ± 1.482e+07
p3	9.989e+07 ± 4.555e+05
p4	12.31 ± 0.1371

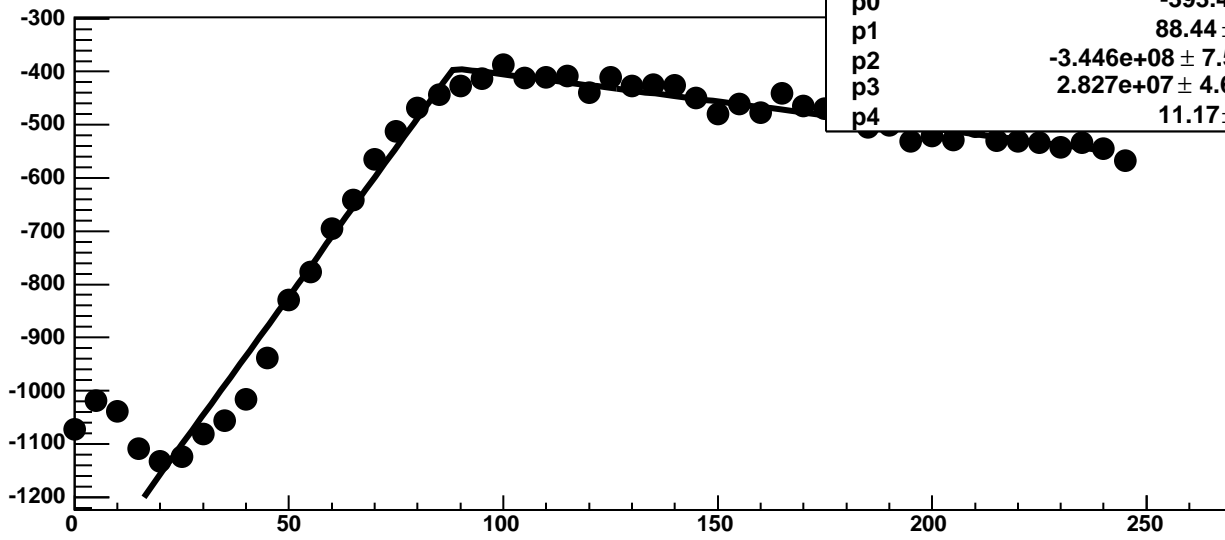
Chip 2, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

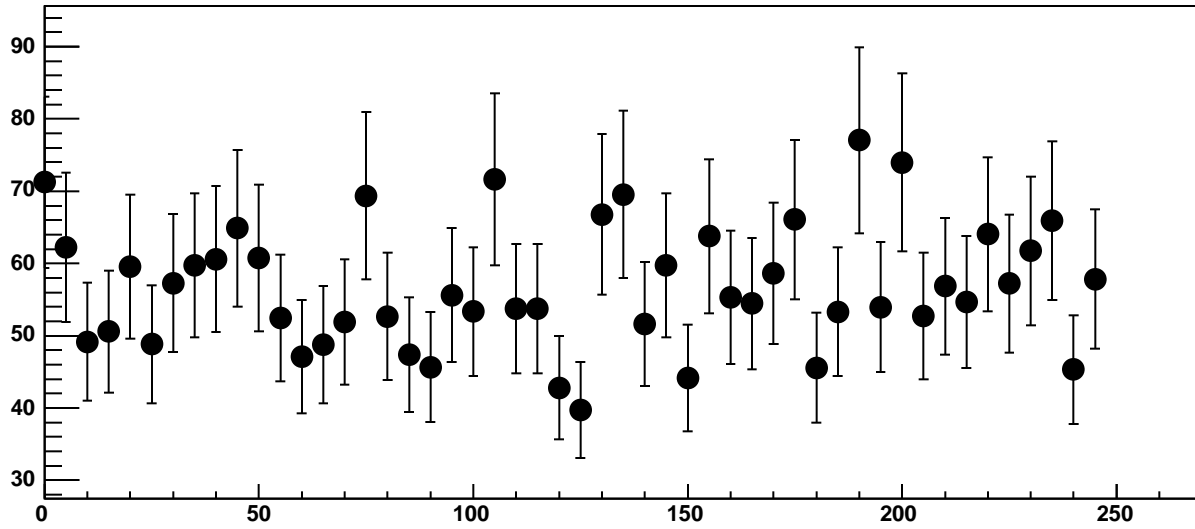


Chip 2, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold

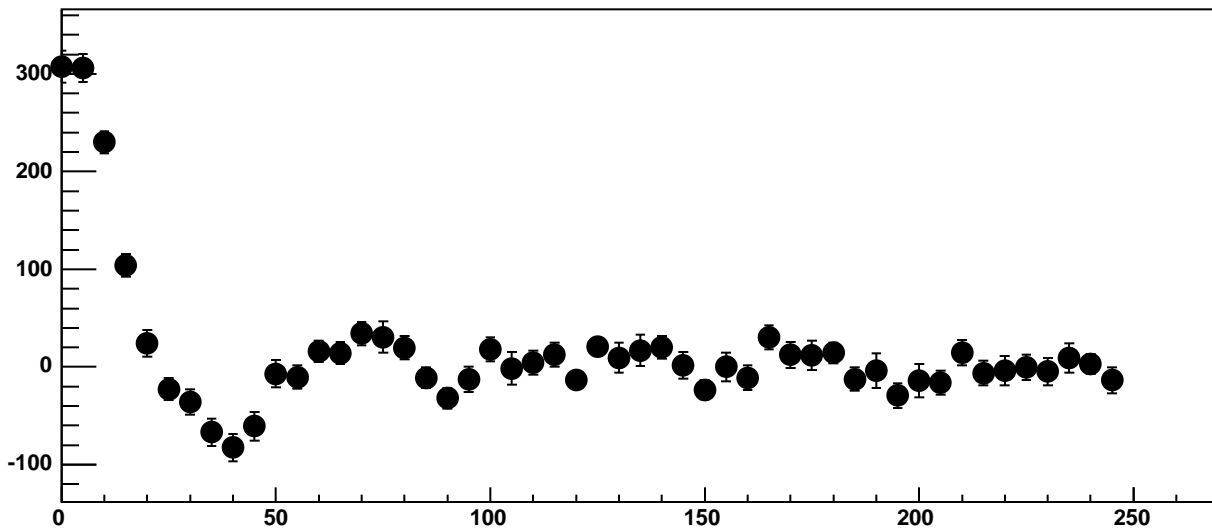


$\chi^2 / \text{ndf}$	243 / 41
p0	$-393.4 \pm 3.972$
p1	$88.44 \pm 0.6263$
p2	$-3.446\text{e}+08 \pm 7.596\text{e}+06$
p3	$2.827\text{e}+07 \pm 4.647\text{e}+05$
p4	$11.17 \pm 0.1449$

Chip 2, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

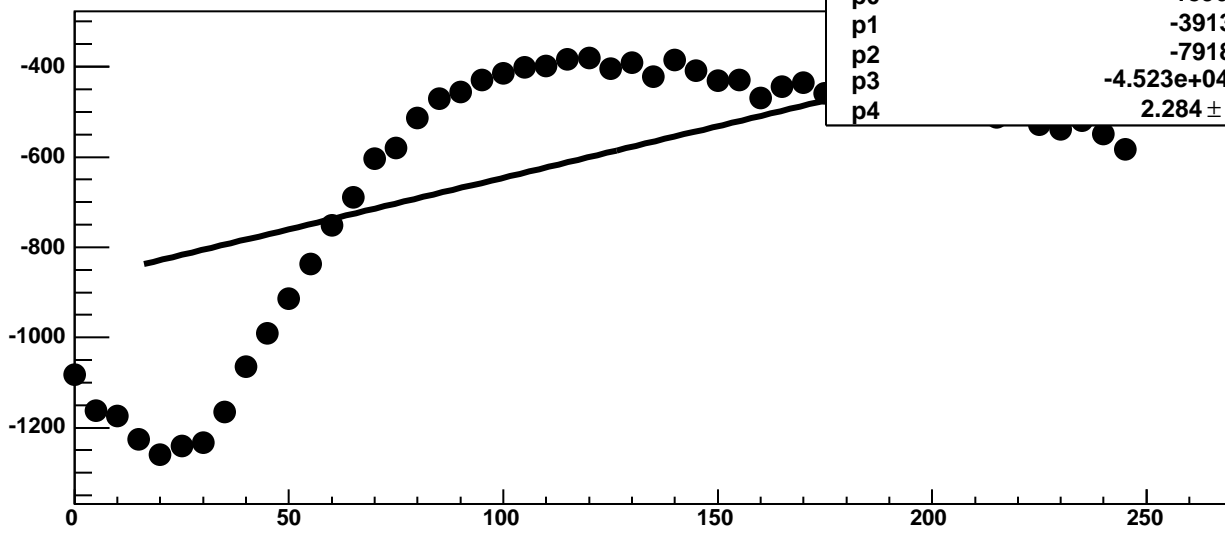


Chip 2, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold



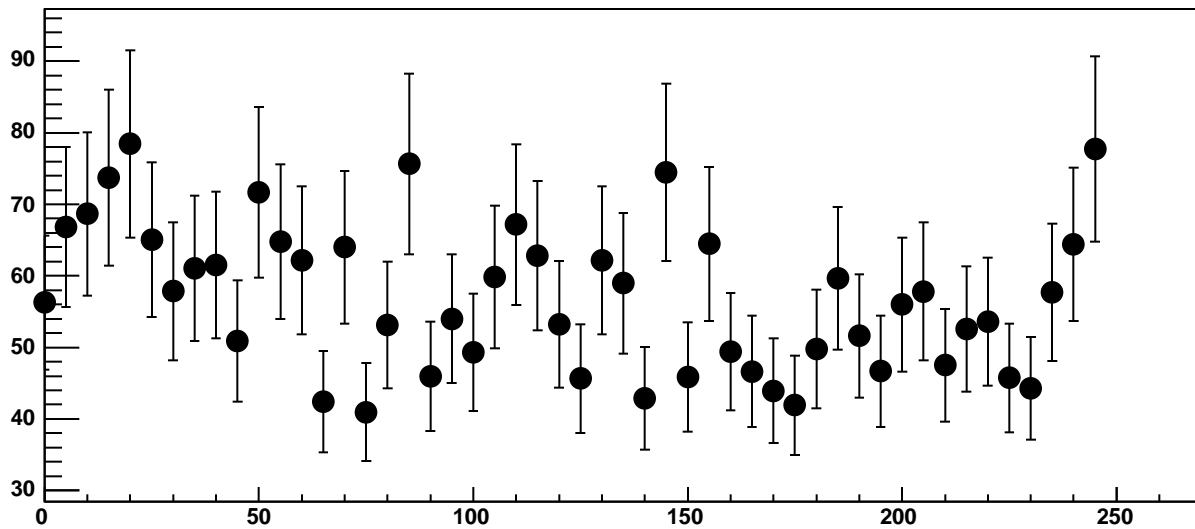


Chip 2, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

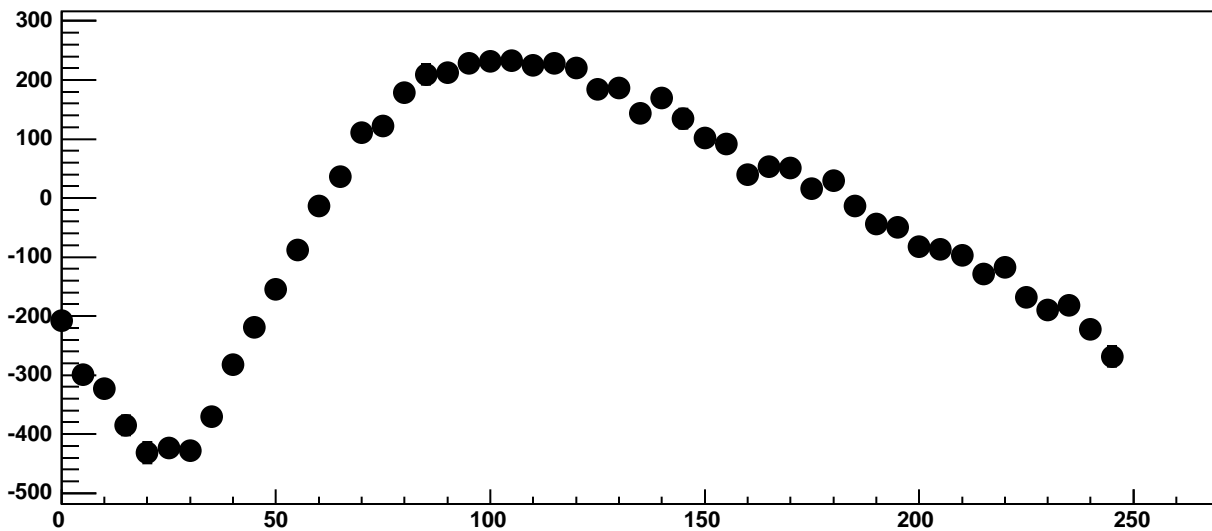


$\chi^2 / \text{ndf}$	9951 / 41
p0	-1896 ± 8.747
p1	-3913 ± 3.701
p2	-7918 ± 11.83
p3	-4.523e+04 ± 857.8
p4	2.284 ± 0.00216

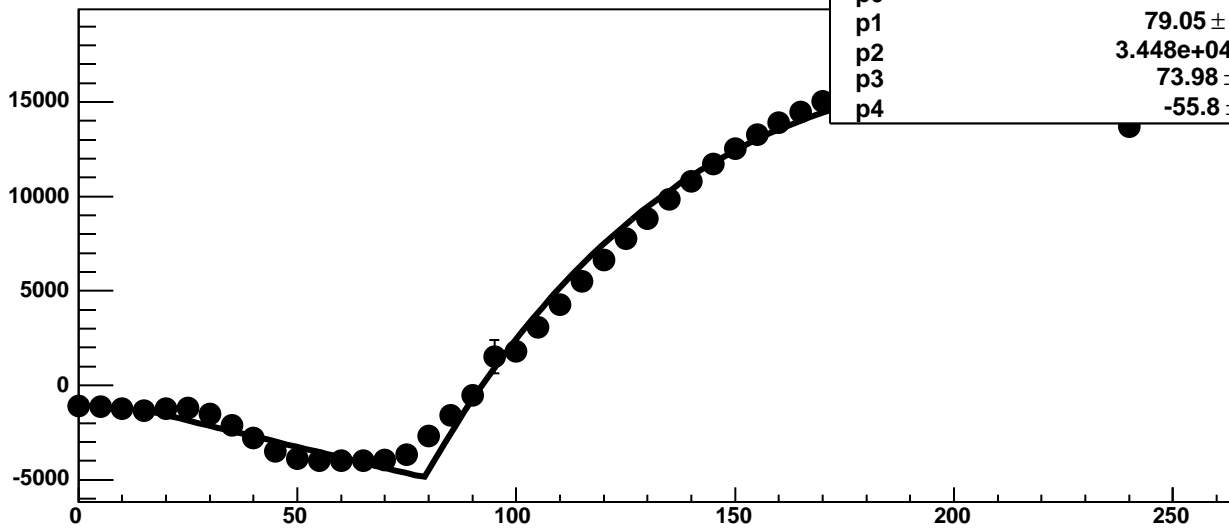
Chip 2, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



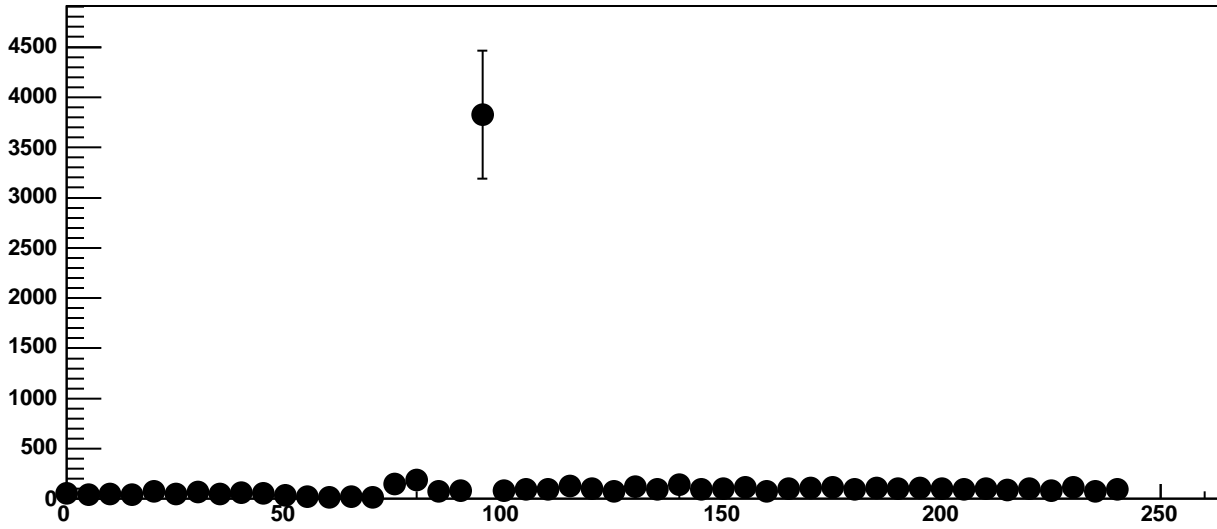
Chip 2, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold



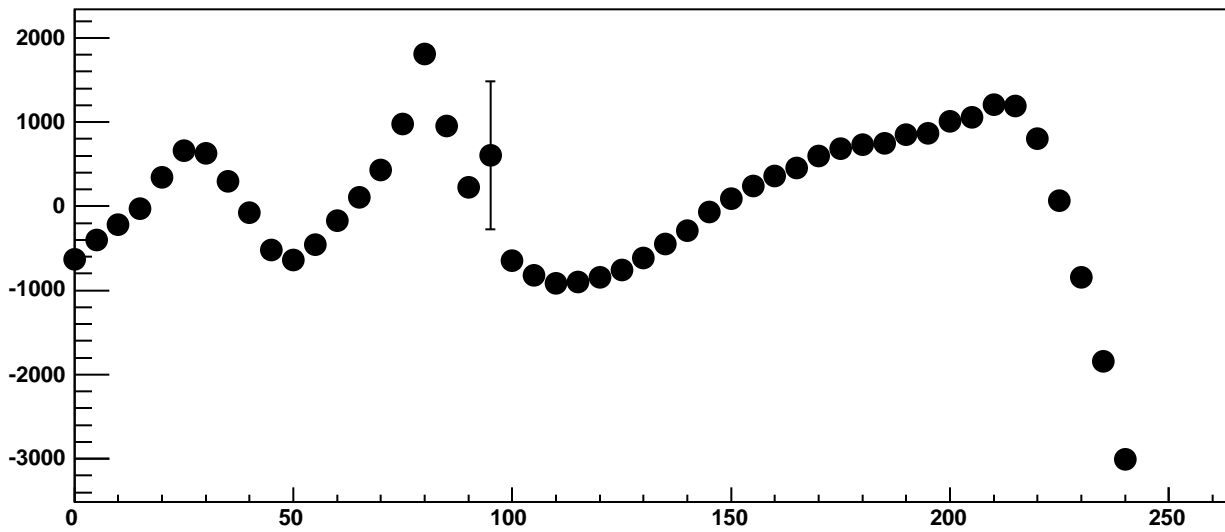
Chip 2, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold



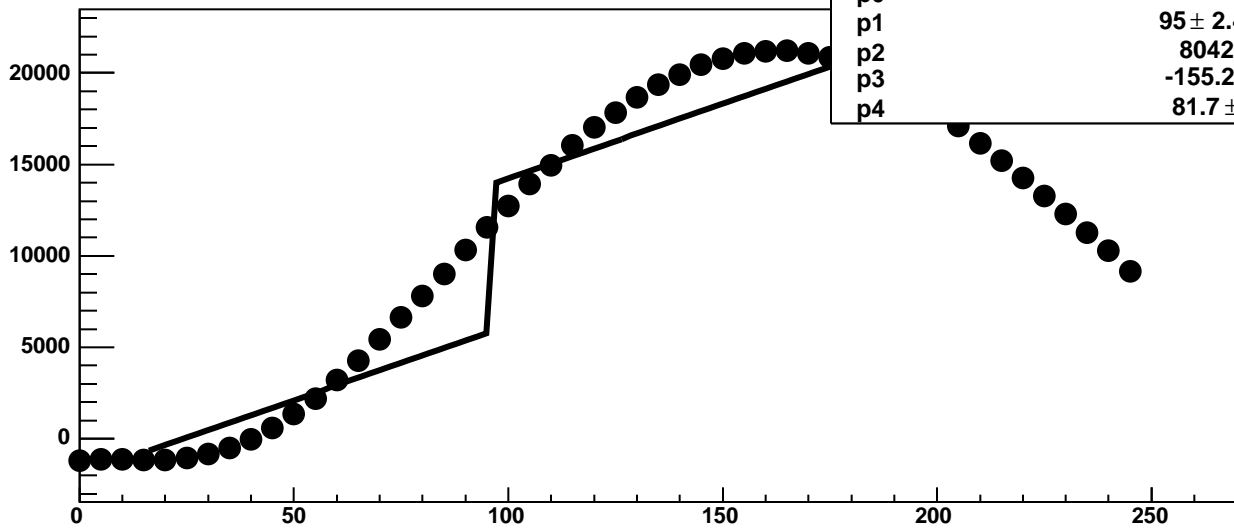
Chip 2, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

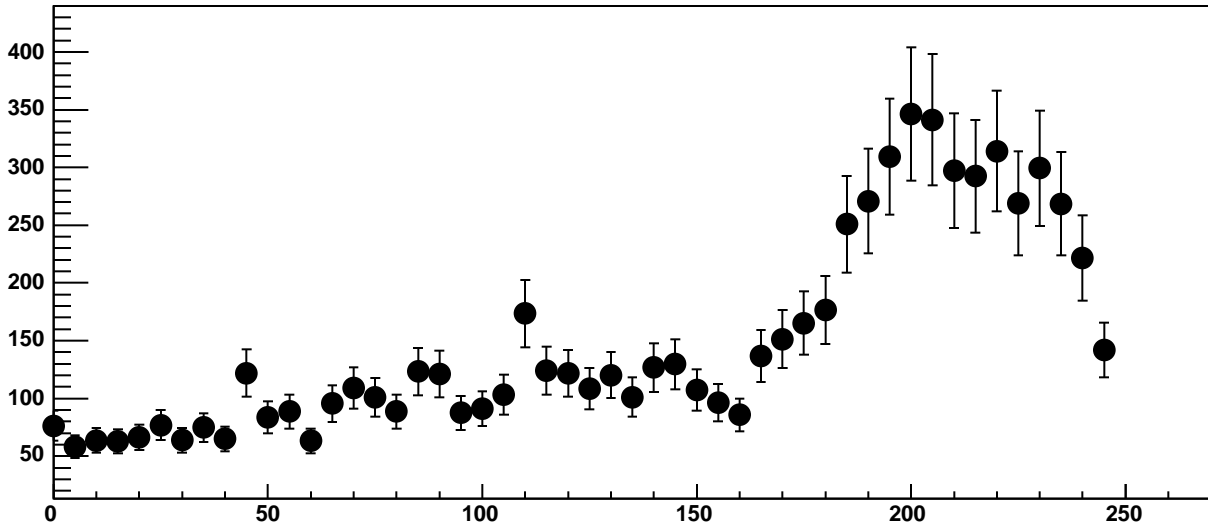


Chip 2, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold

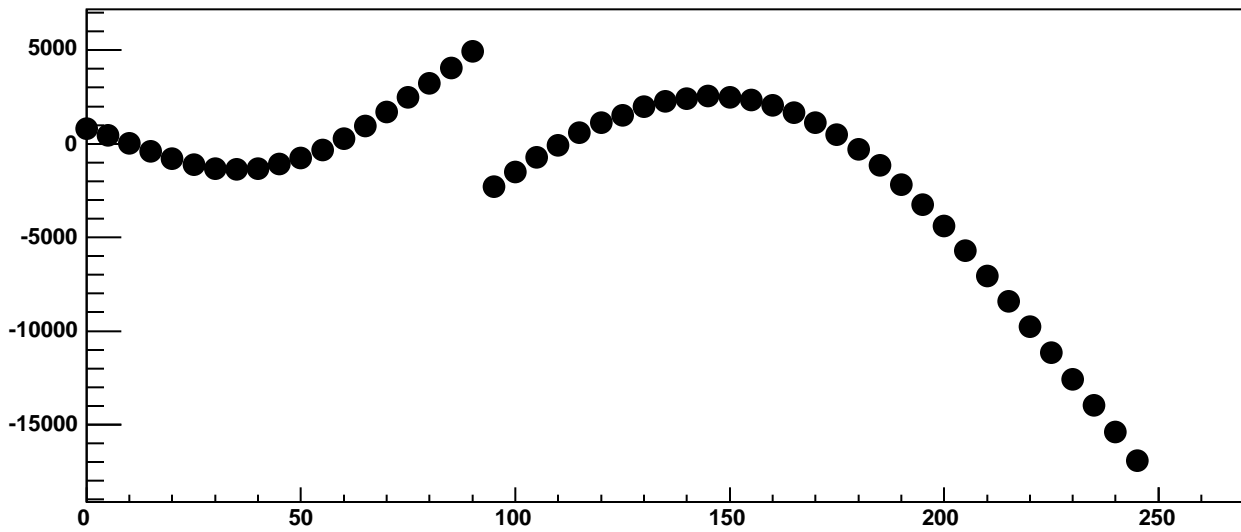


$\chi^2 / \text{ndf}$	4.861e+05 / 41
p0	5785 ± 43.38
p1	95 ± 2.415e-05
p2	8042 ± 42.85
p3	-155.2 ± 16.72
p4	81.7 ± 0.6246

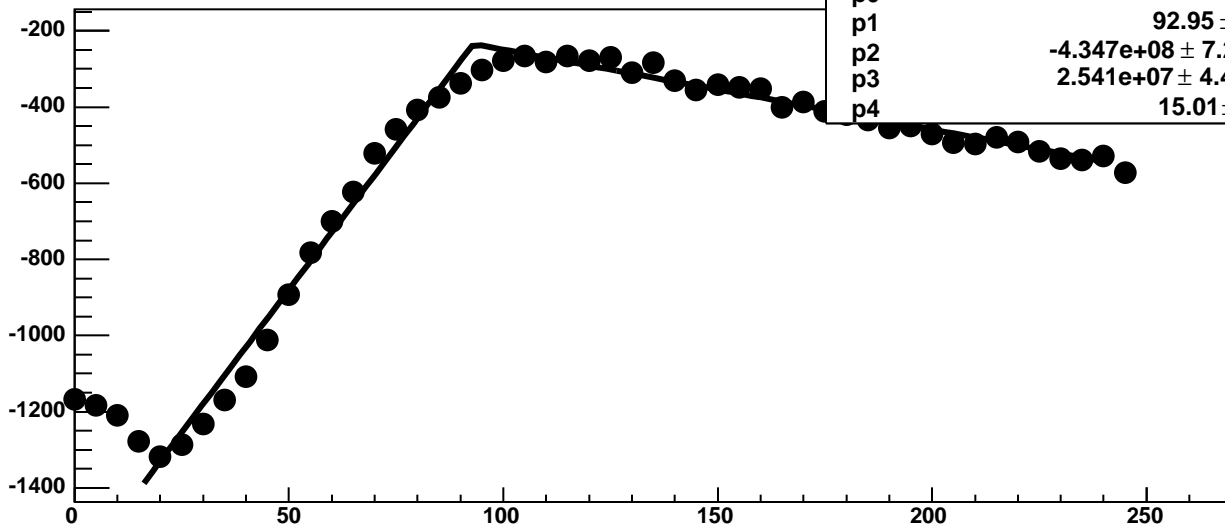
Chip 2, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold

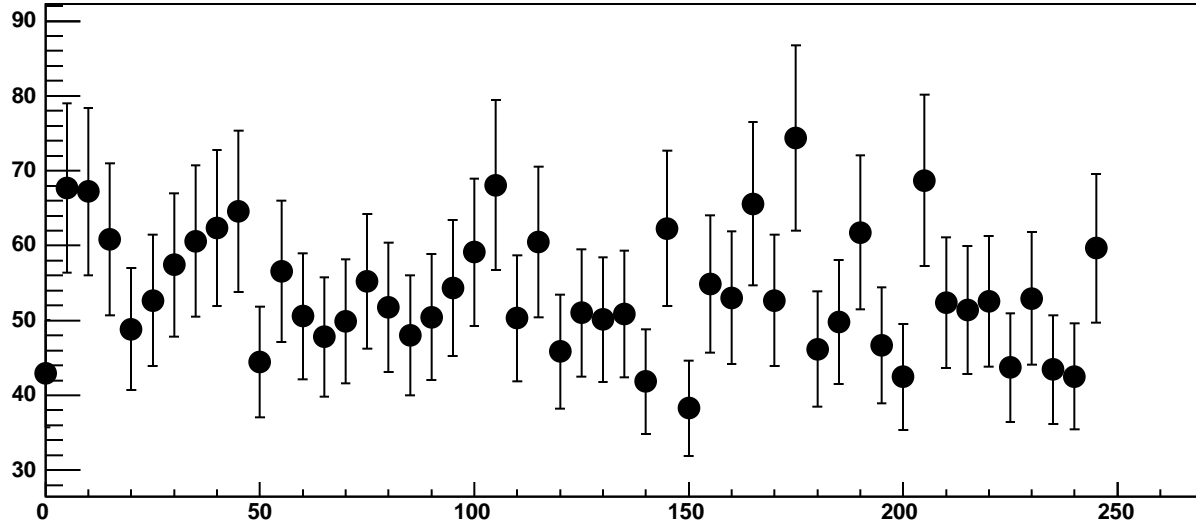


Chip 2, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

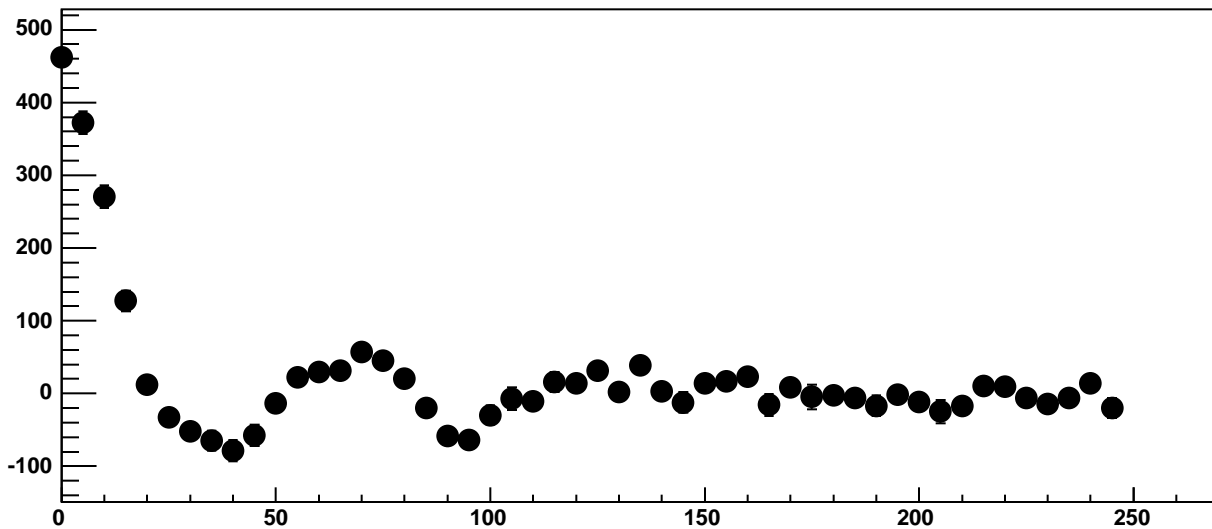


$\chi^2 / \text{ndf}$	340.1 / 41
p0	-234.6 ± 3.819
p1	92.95 ± 0.4044
p2	-4.347e+08 ± 7.249e+06
p3	2.541e+07 ± 4.492e+05
p4	15.01 ± 0.1178

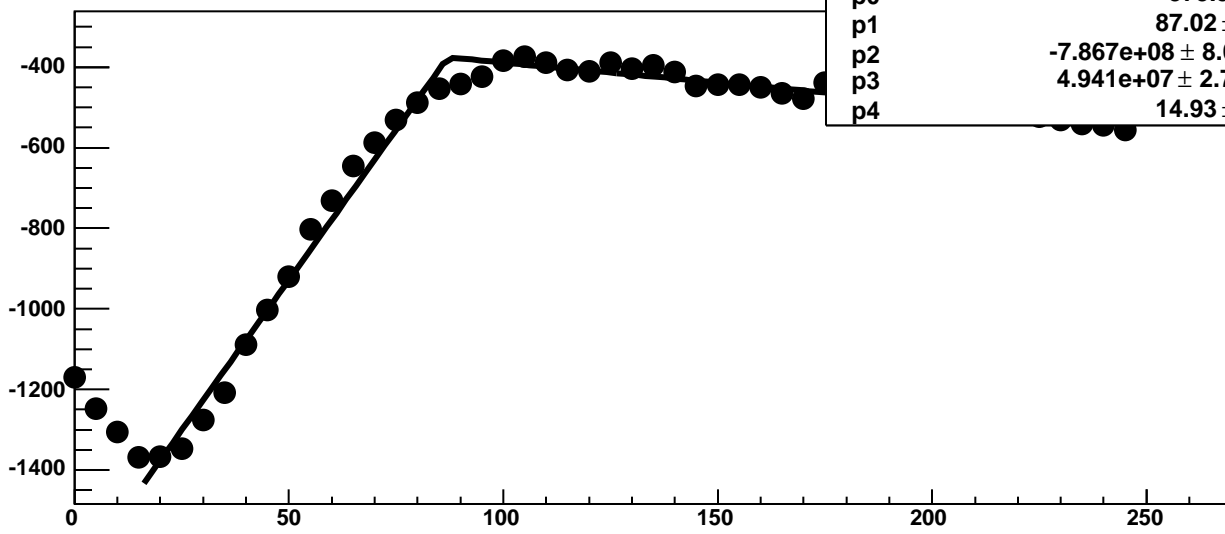
Chip 2, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

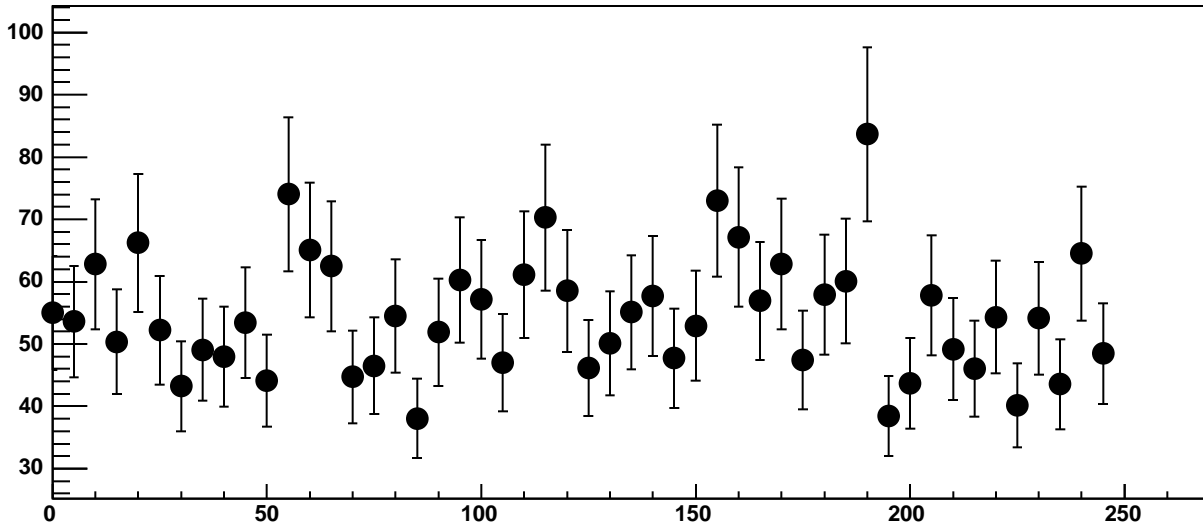


Chip 2, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

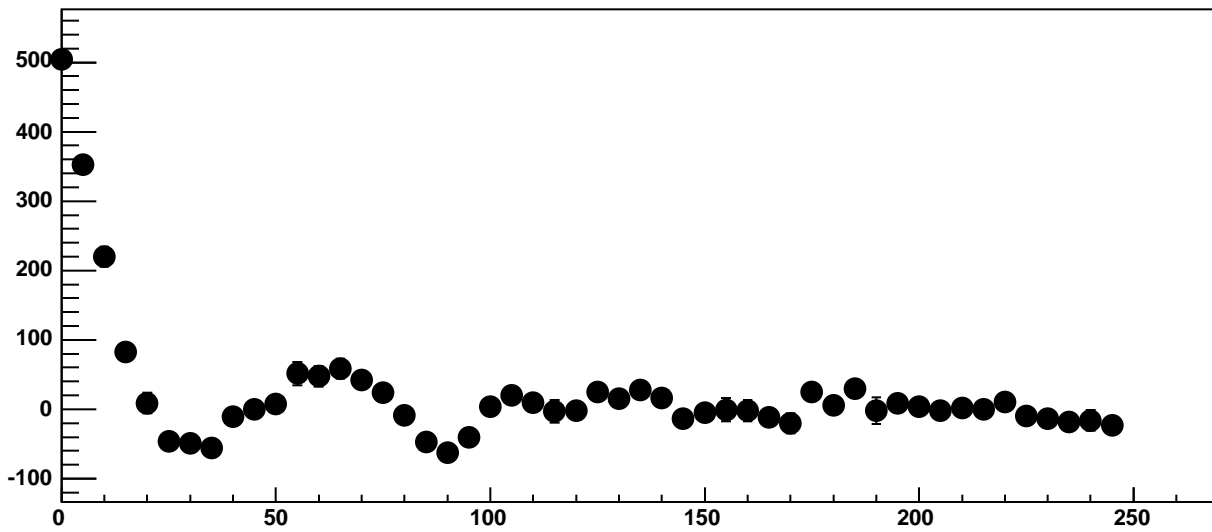


$\chi^2 / \text{ndf}$	283.1 / 41
p0	$-375.5 \pm 4.244$
p1	$87.02 \pm 0.4503$
p2	$-7.867\text{e}+08 \pm 8.095\text{e}+06$
p3	$4.941\text{e}+07 \pm 2.738\text{e}+05$
p4	$14.93 \pm 0.1329$

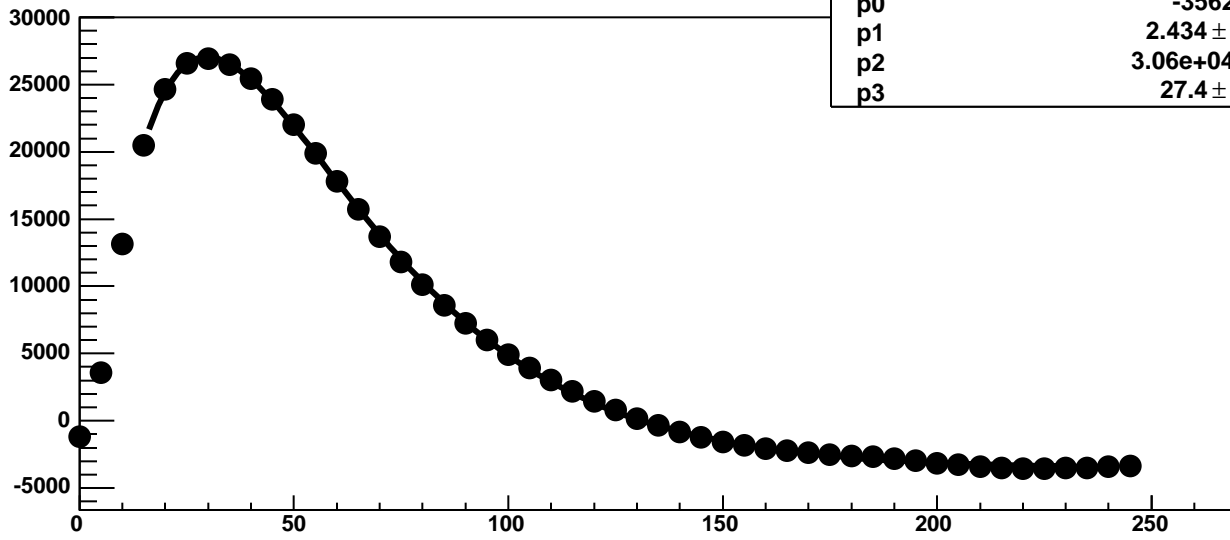
Chip 2, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

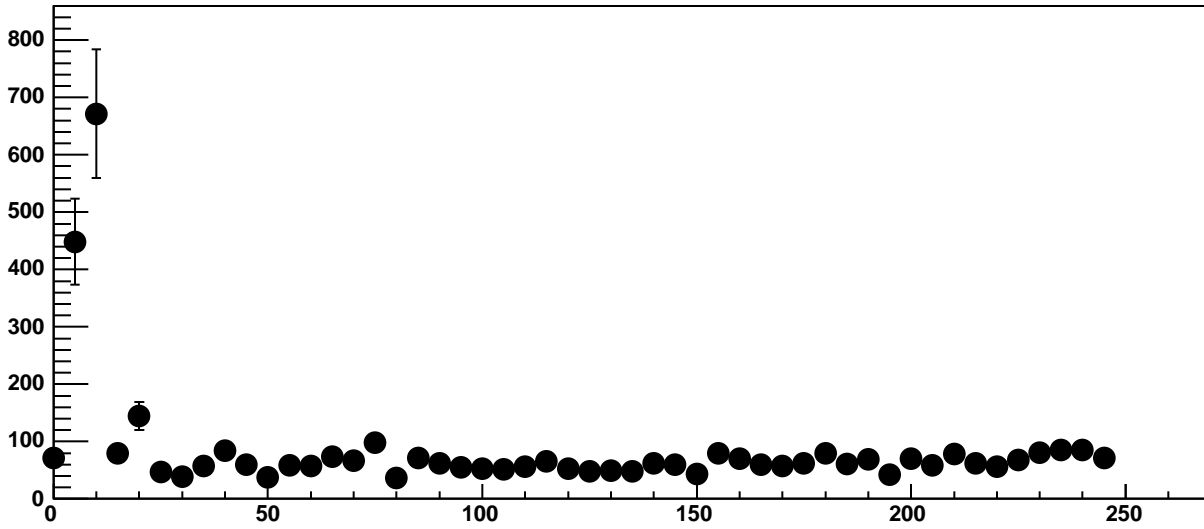


Chip 2, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold

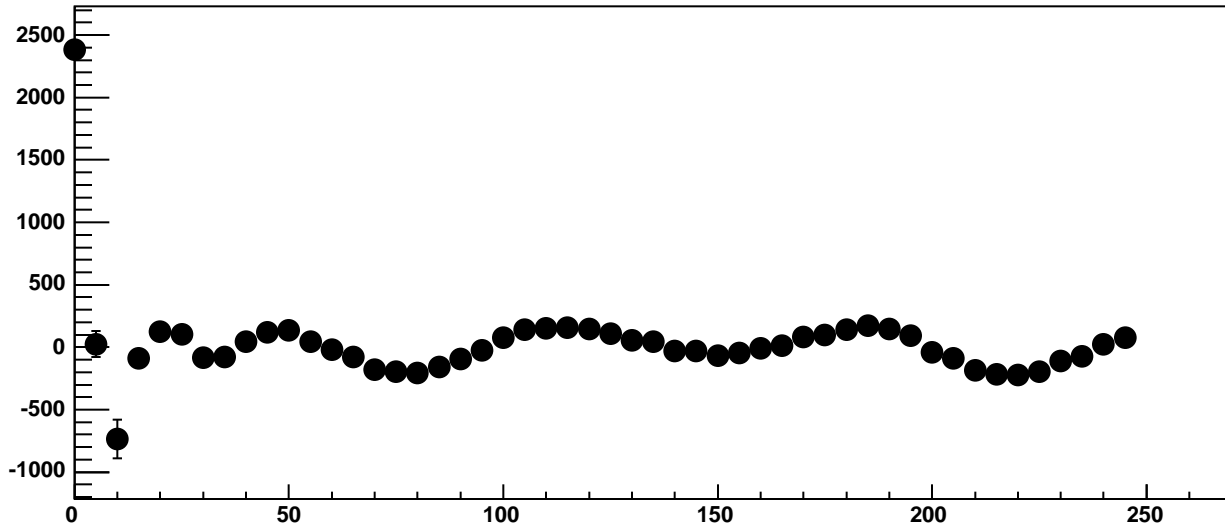


$\chi^2 / \text{ndf}$	3662 / 42
p0	-3562 ± 3.907
p1	2.434 ± 0.01836
p2	3.06e+04 ± 5.639
p3	27.4 ± 0.01082

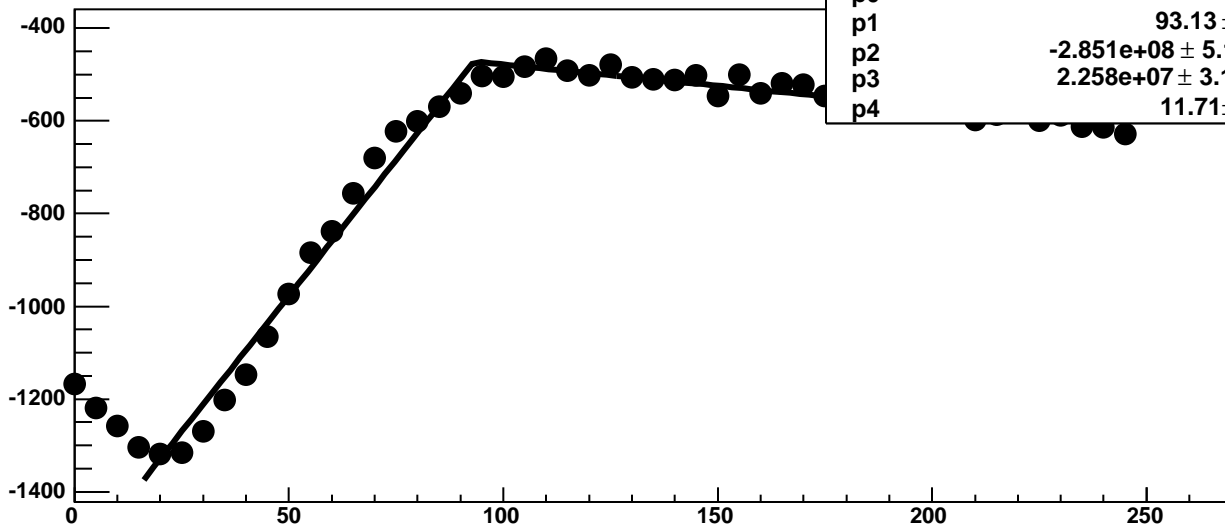
Chip 2, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold

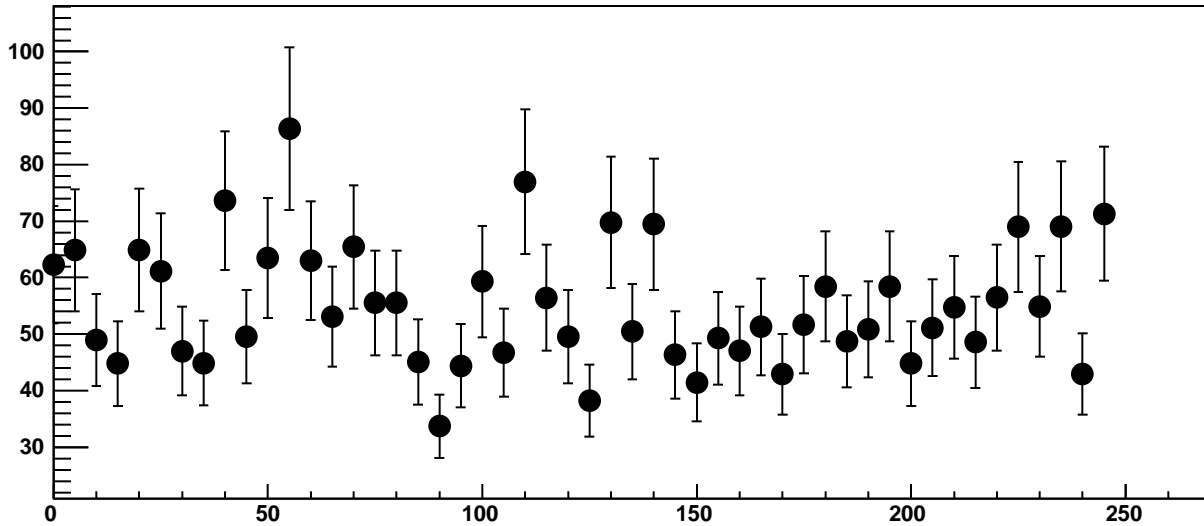


Chip 2, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

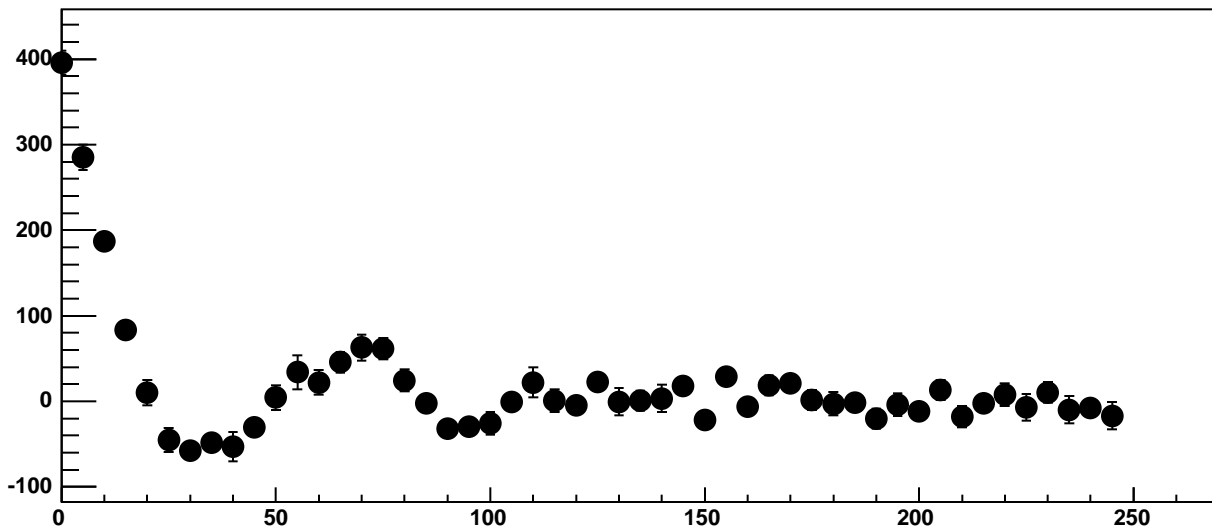


$\chi^2 / \text{ndf}$	278.4 / 41
p0	-472.1 ± 3.991
p1	93.13 ± 0.5409
p2	-2.851e+08 ± 5.141e+06
p3	2.258e+07 ± 3.126e+05
p4	11.71 ± 0.1174

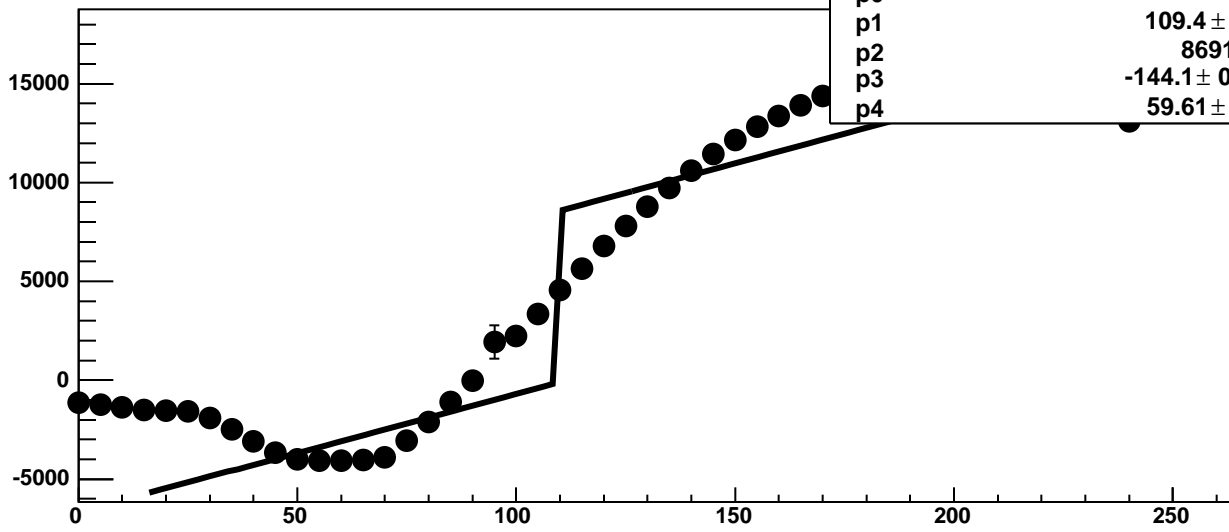
Chip 2, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



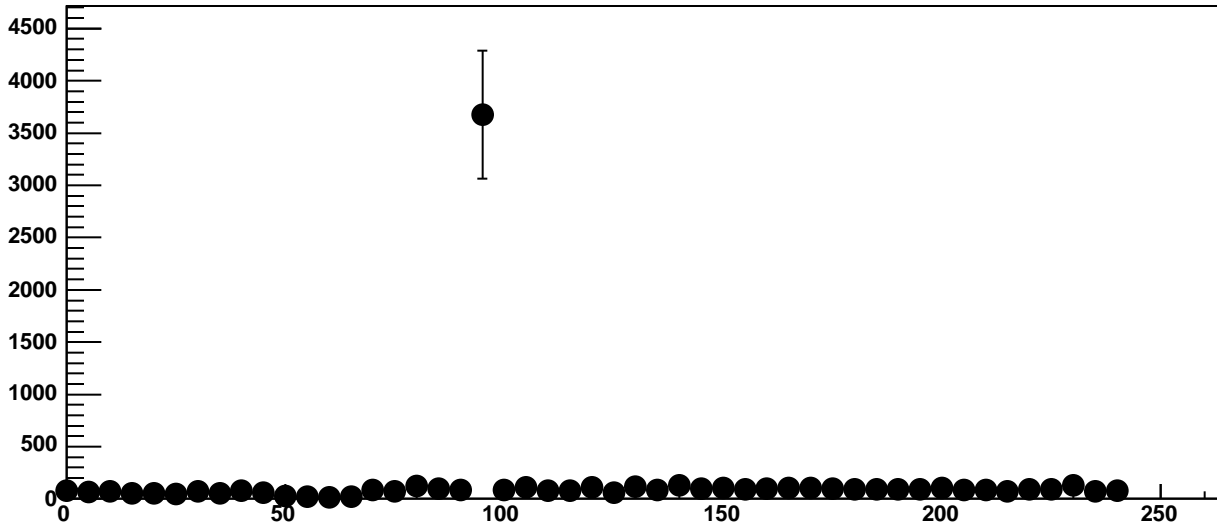
Chip 2, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold



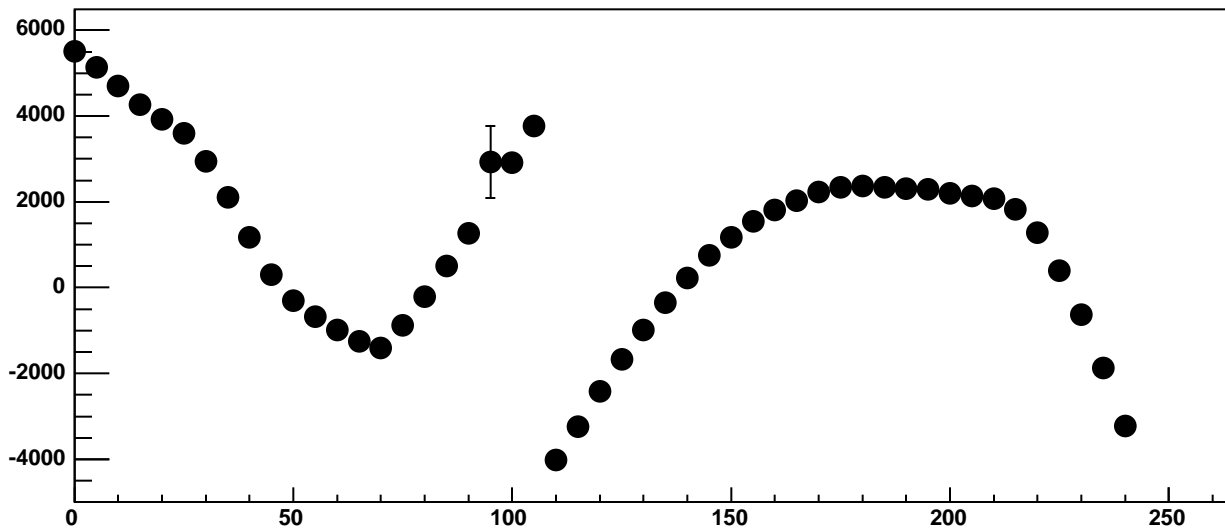
Chip 2, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 2, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold

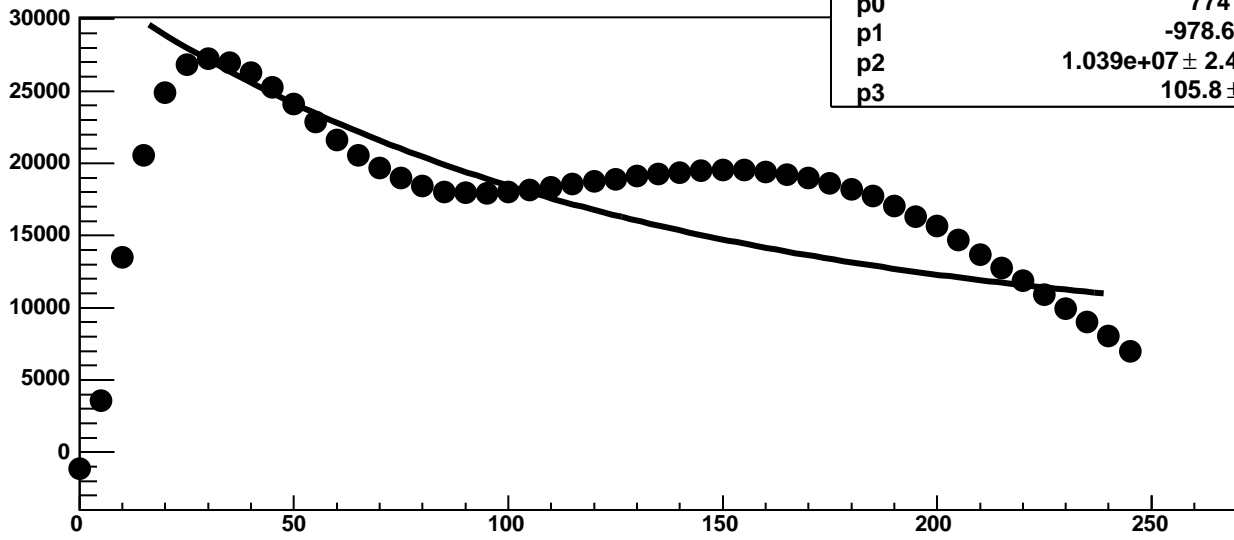


Chip 2, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



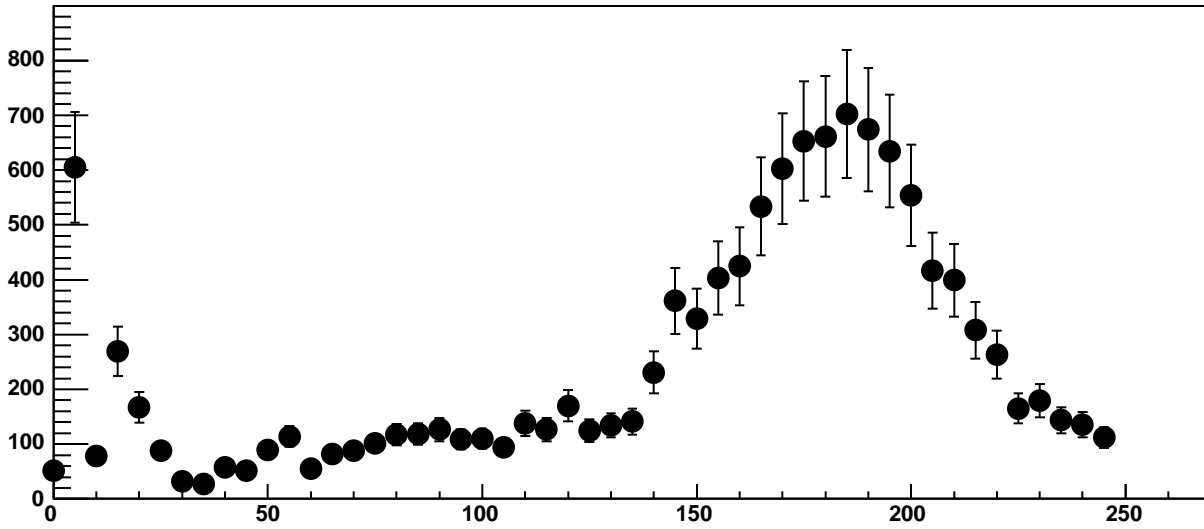


Chip 2, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold

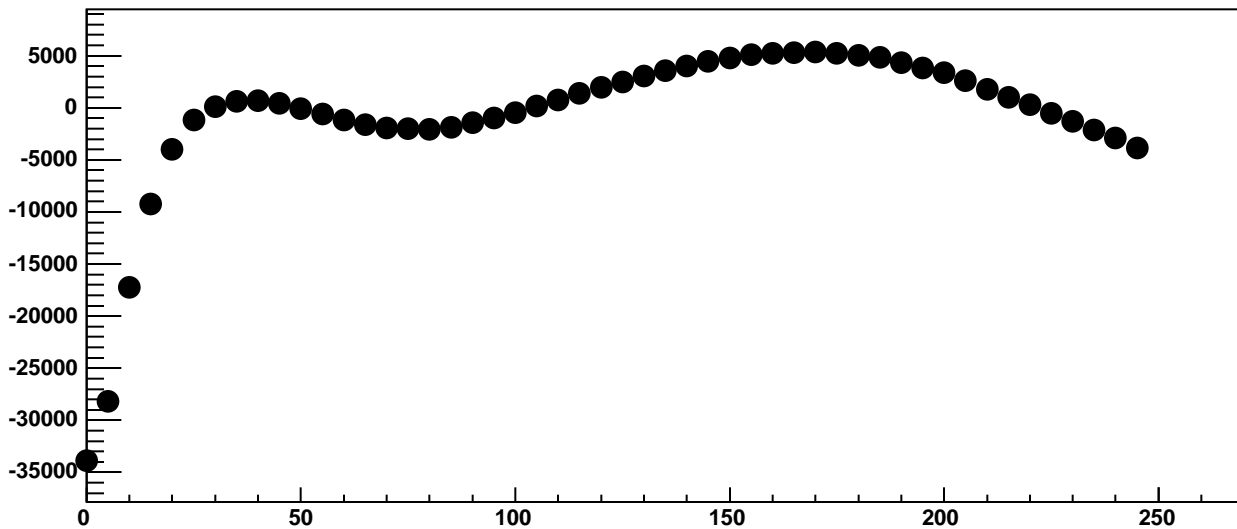


$\chi^2 / \text{ndf}$	1.757e+05 / 42
p0	7741 ± 43.8
p1	-978.6 ± 5.009
p2	1.039e+07 ± 2.439e+05
p3	105.8 ± 0.4018

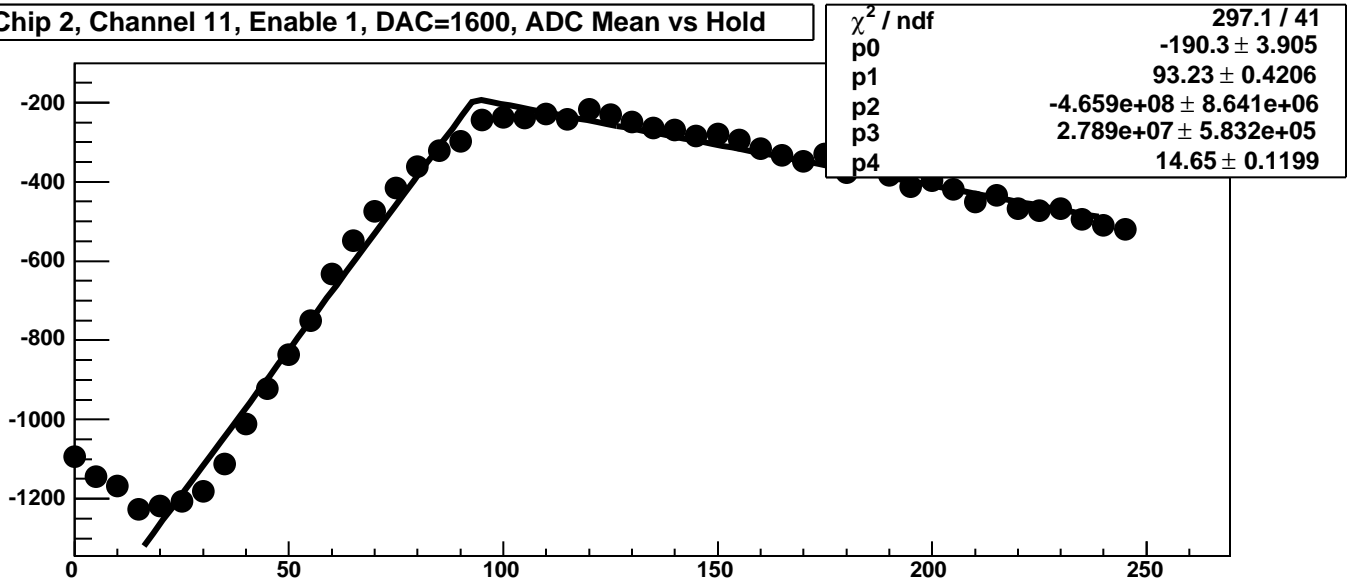
Chip 2, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



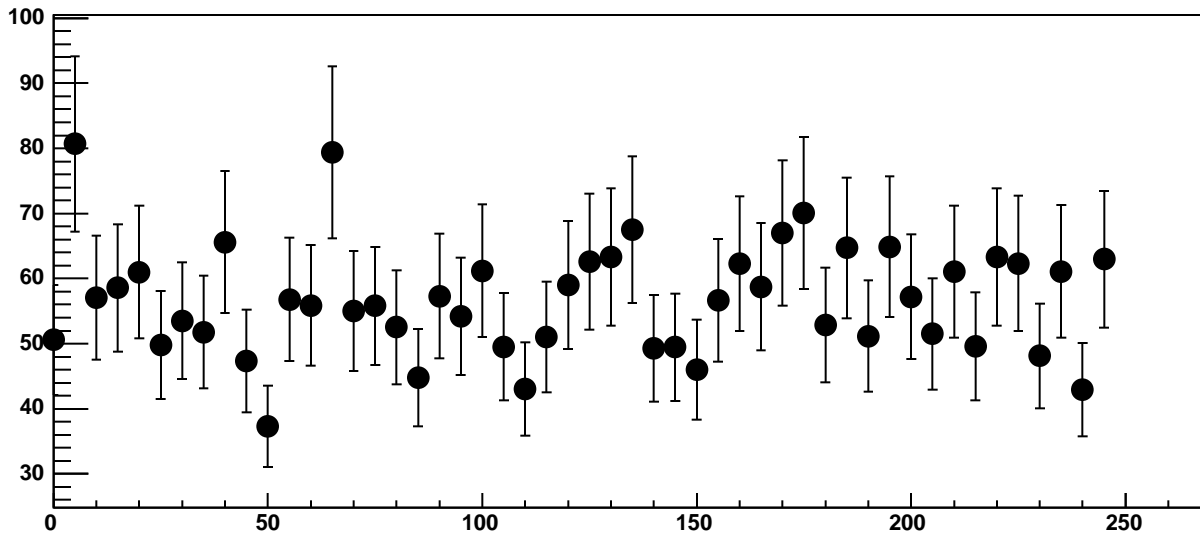
Chip 2, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold



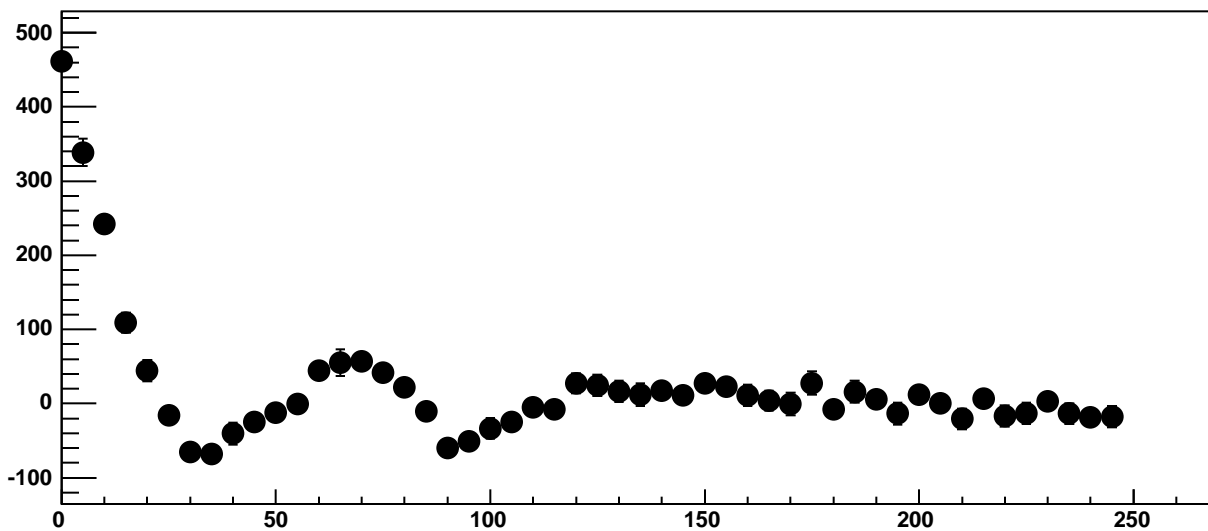
Chip 2, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold



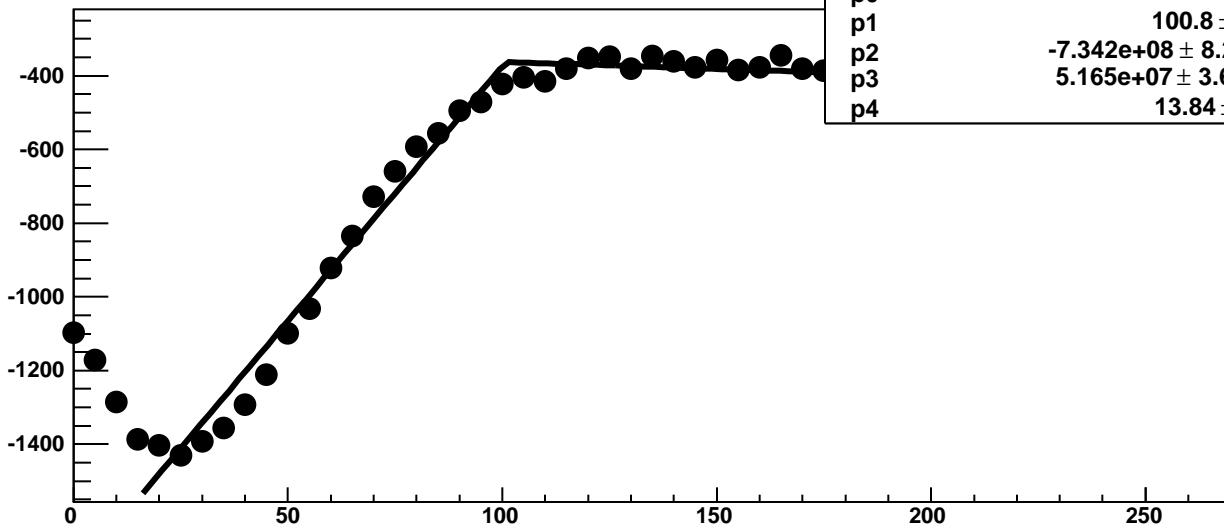
Chip 2, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

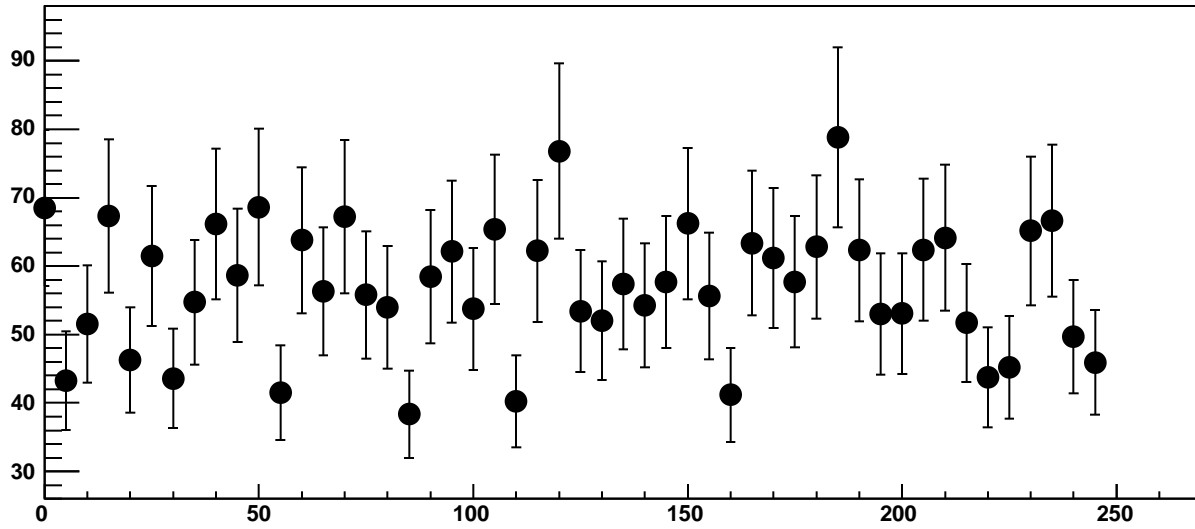


Chip 2, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

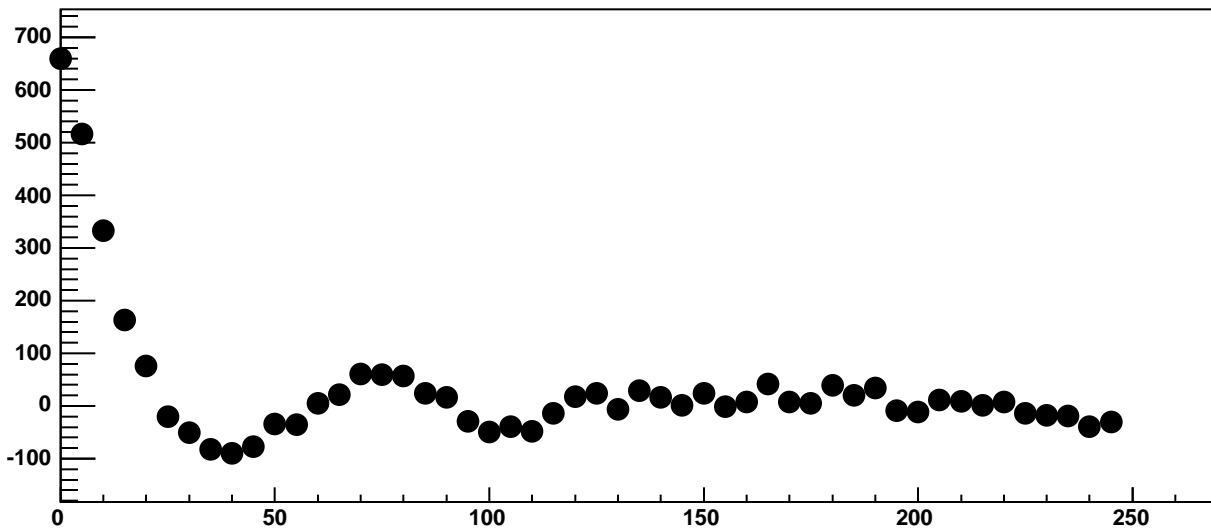


$\chi^2 / \text{ndf}$	503.6 / 41
p0	-362.8 ± 4.718
p1	100.8 ± 0.5225
p2	-7.342e+08 ± 8.251e+06
p3	5.165e+07 ± 3.647e+05
p4	13.84 ± 0.1122

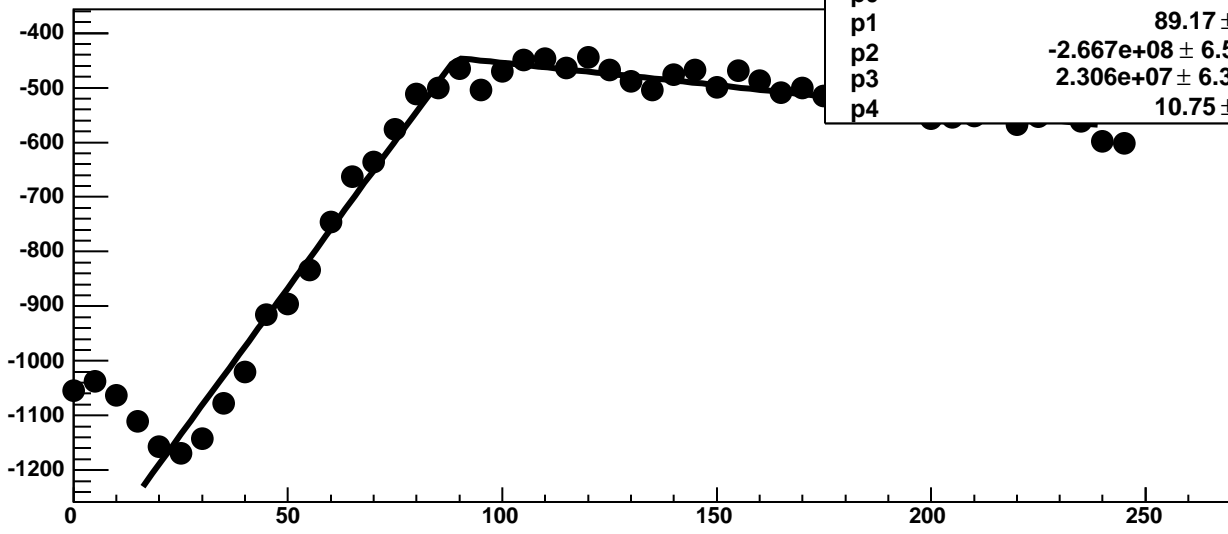
Chip 2, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

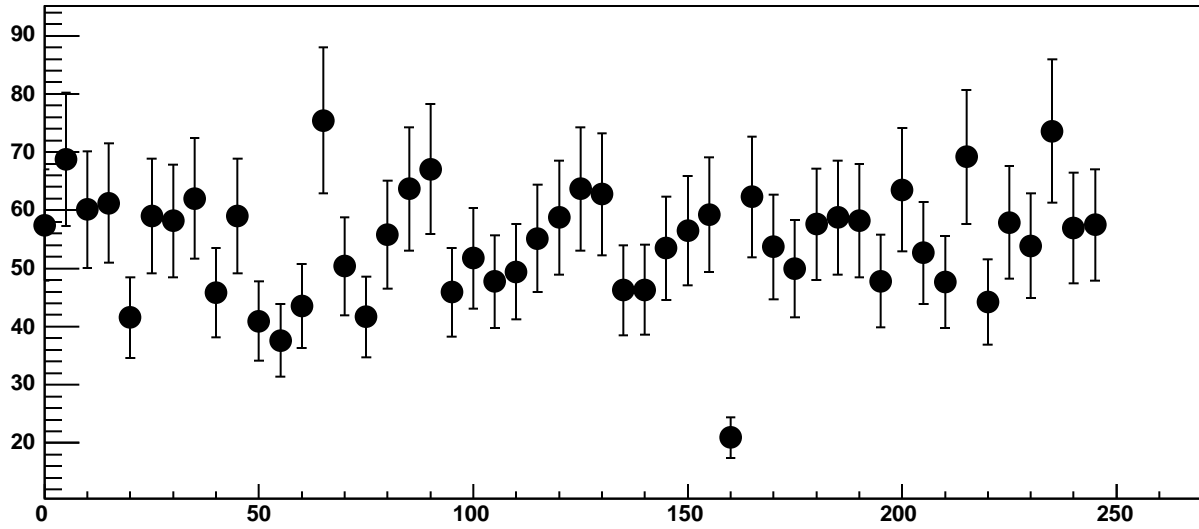


Chip 2, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold

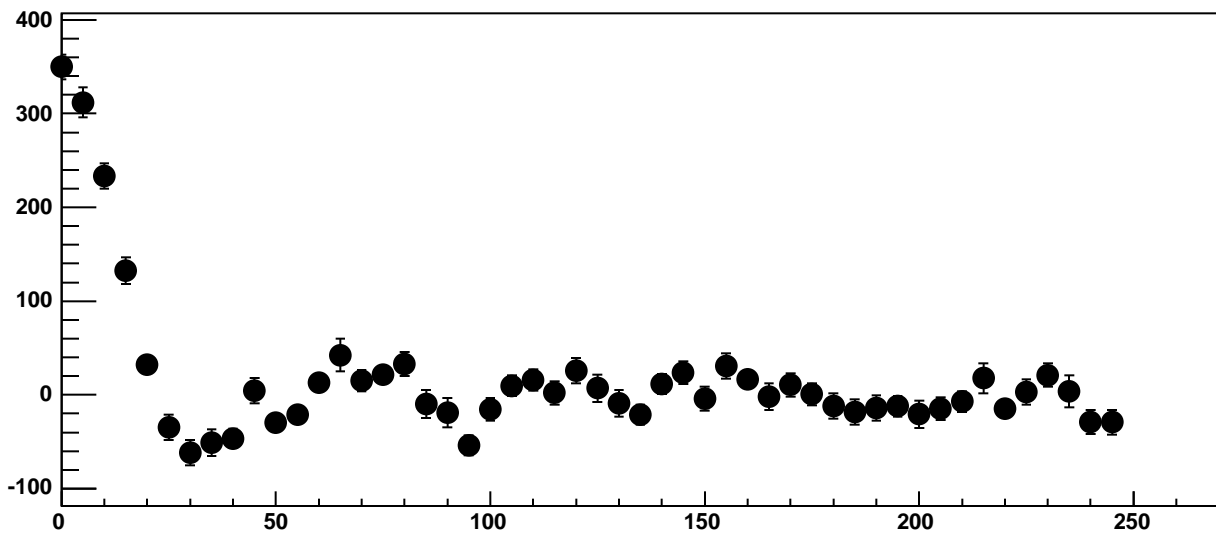


$\chi^2 / \text{ndf}$	280.1 / 41
p0	-445.4 ± 3.844
p1	89.17 ± 0.6072
p2	-2.667e+08 ± 6.505e+06
p3	2.306e+07 ± 6.352e+05
p4	10.75 ± 0.1277

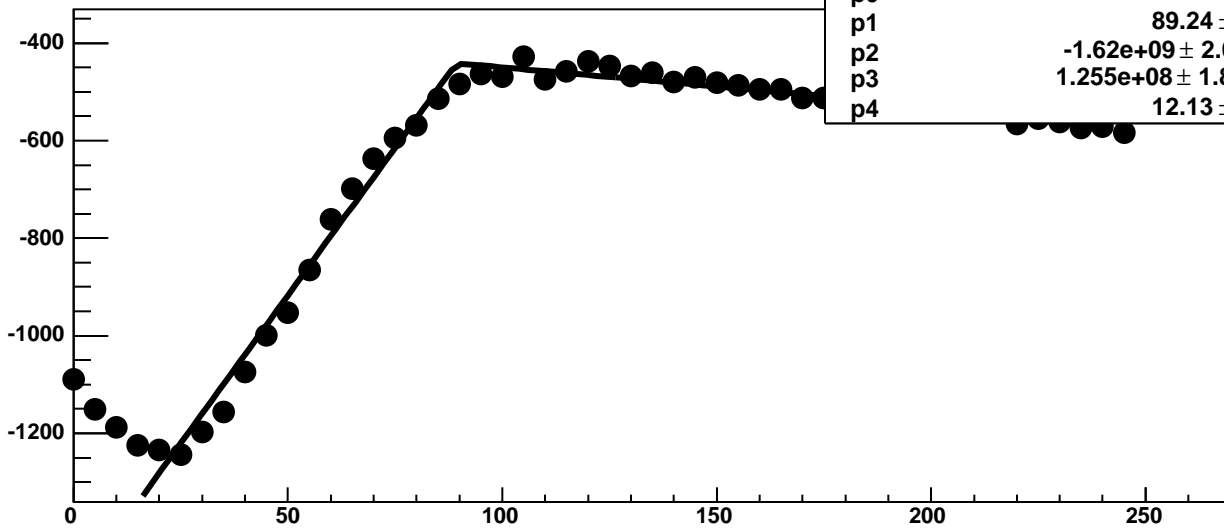
Chip 2, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

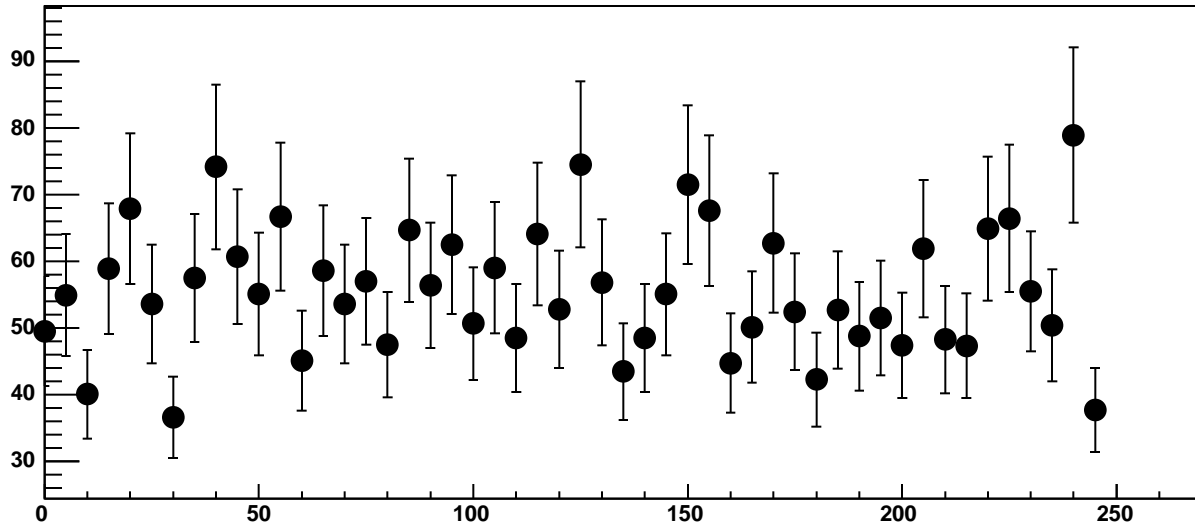


Chip 2, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

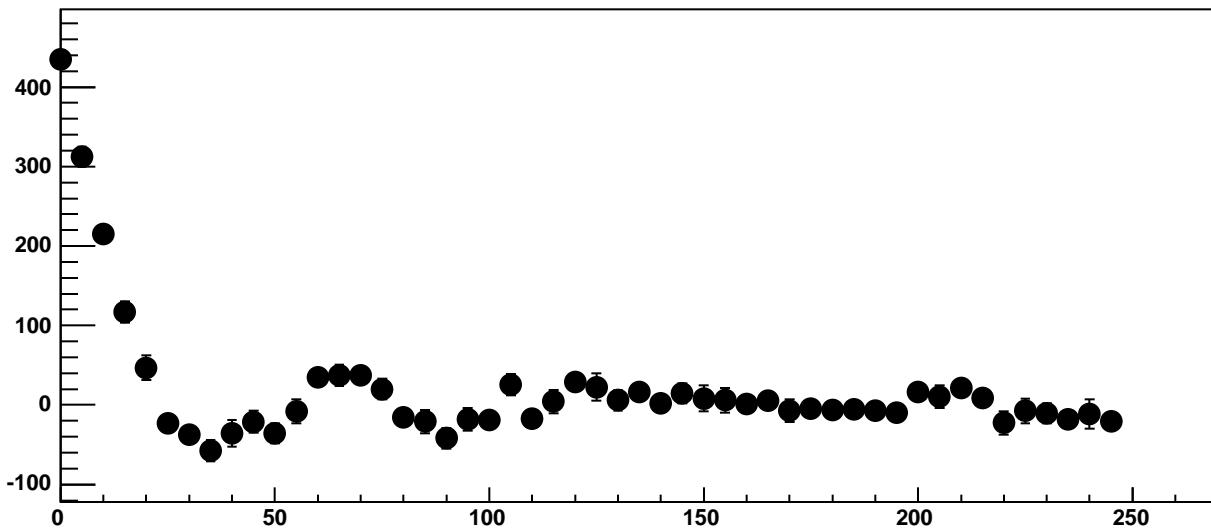


$\chi^2 / \text{ndf}$	225.5 / 41
p0	-441.3 ± 4.285
p1	89.24 ± 0.6345
p2	-1.62e+09 ± 2.015e+07
p3	1.255e+08 ± 1.806e+05
p4	12.13 ± 0.1515

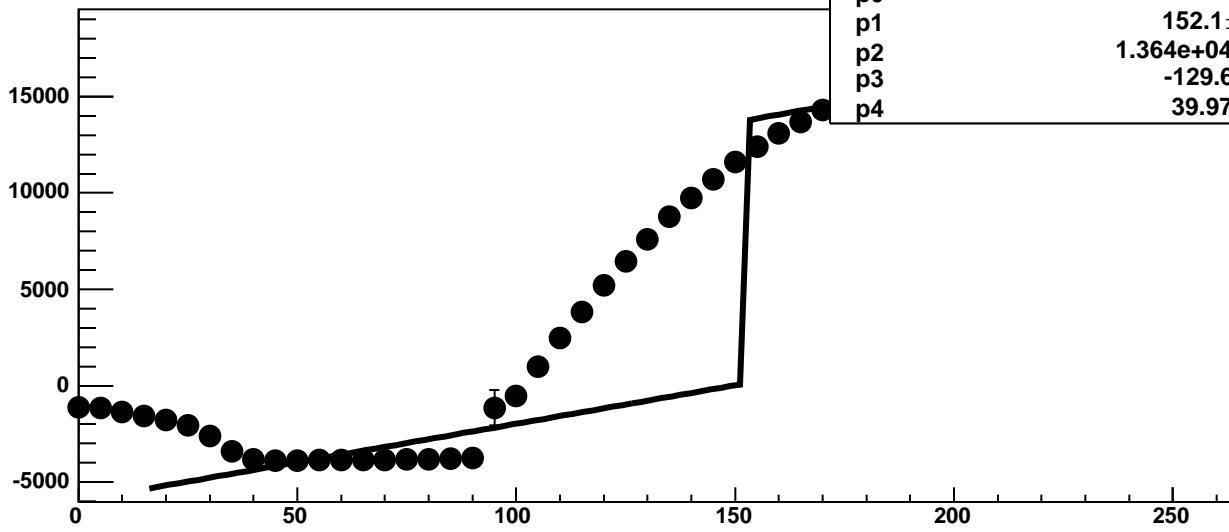
Chip 2, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

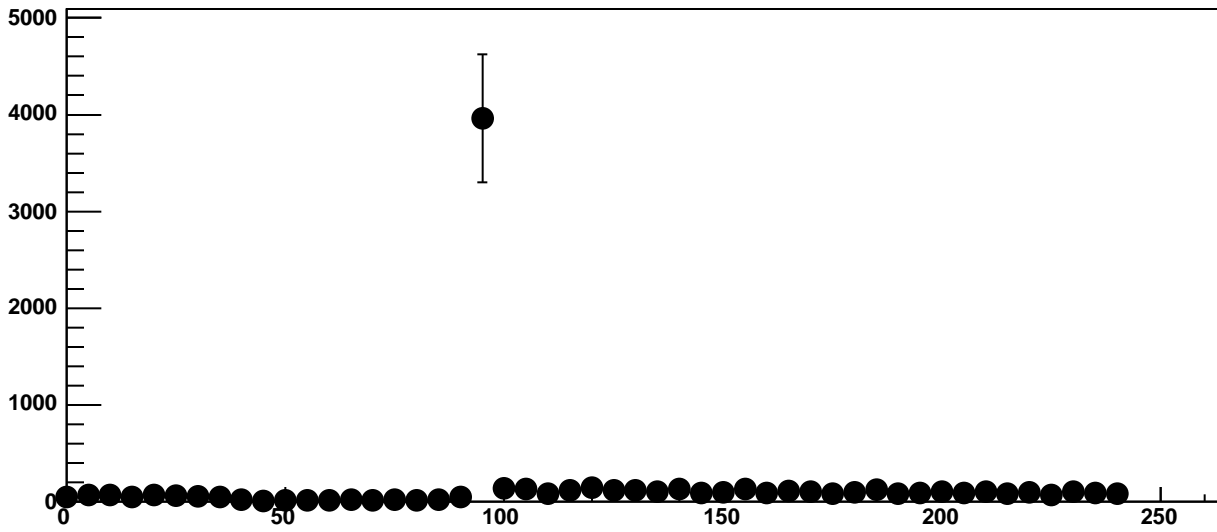


Chip 2, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

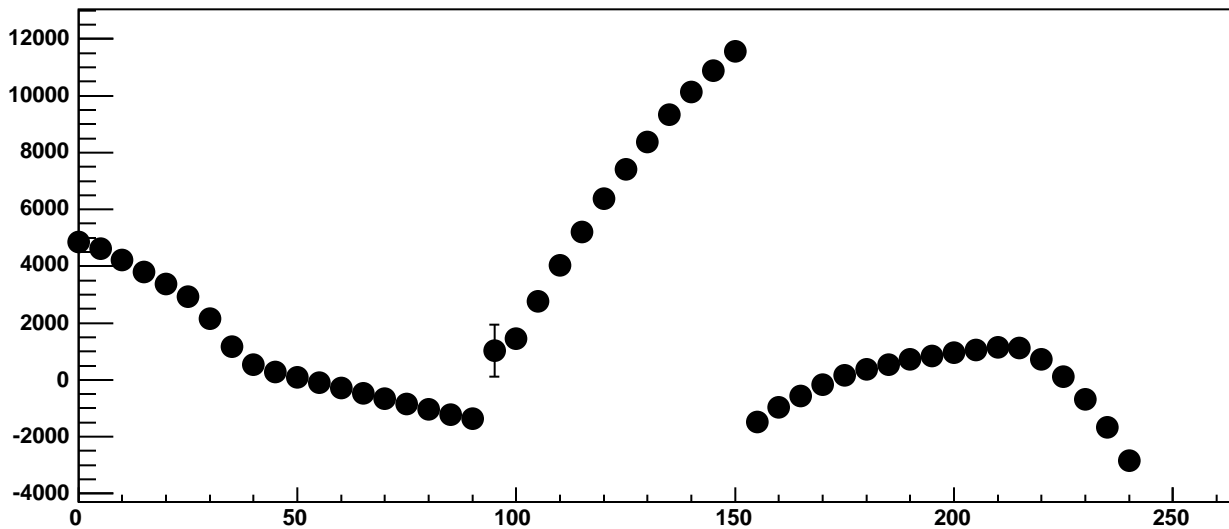


$\chi^2 / \text{ndf}$	1.533e+06 / 41
p0	110.4 ± 3.508
p1	152.1 ± 0.3509
p2	1.364e+04 ± 16.57
p3	-129.6 ± 2.548
p4	39.97 ± 0.159

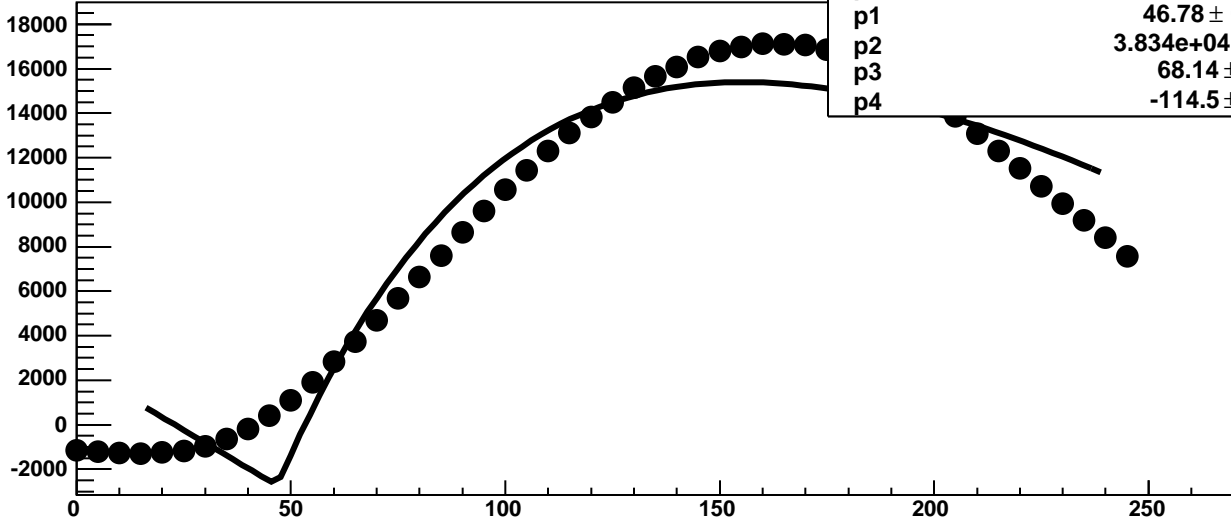
Chip 2, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



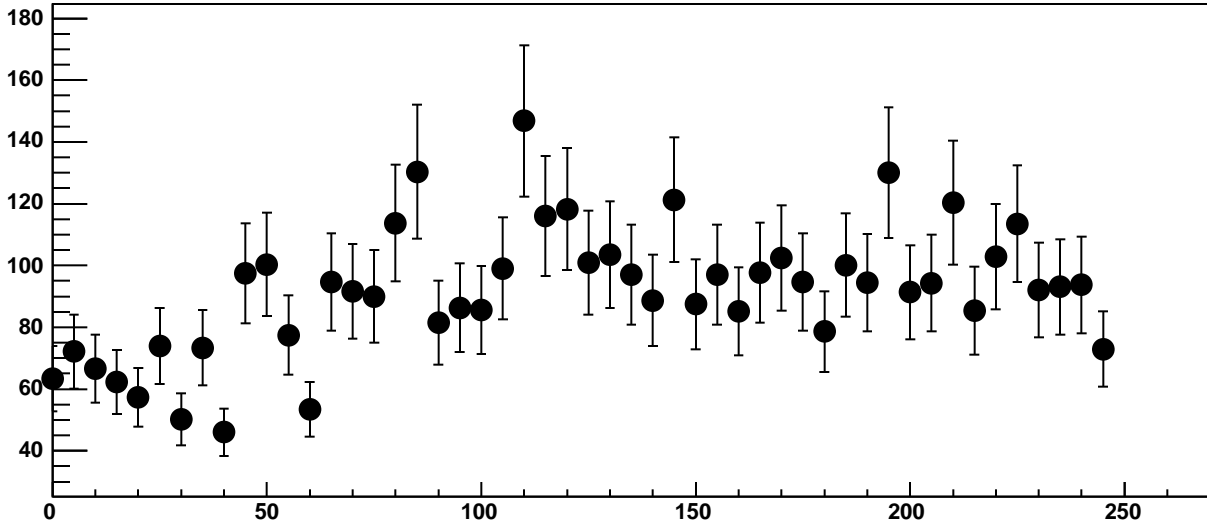
Chip 2, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



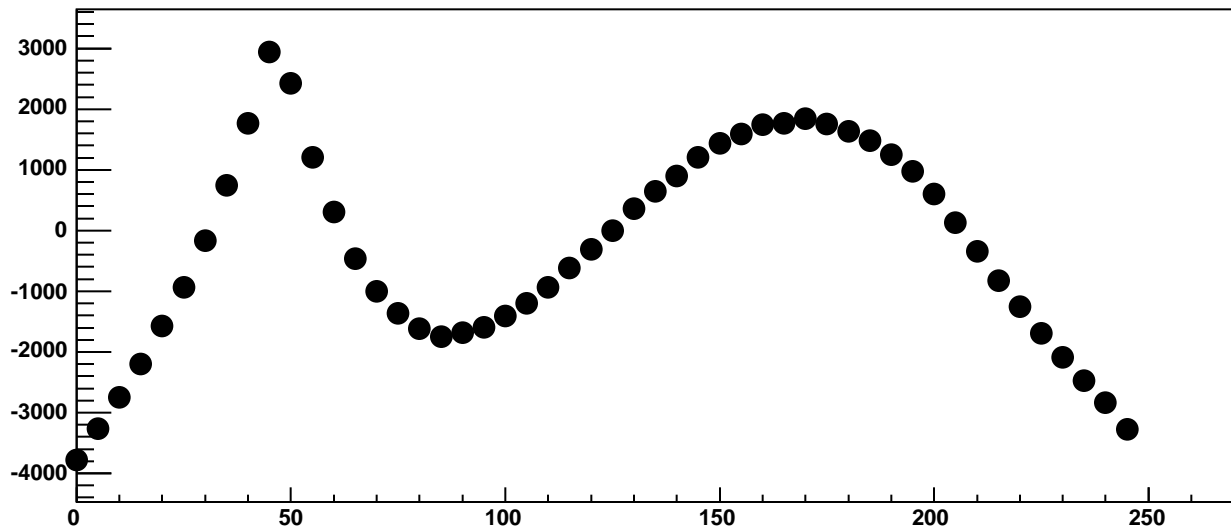
Chip 2, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



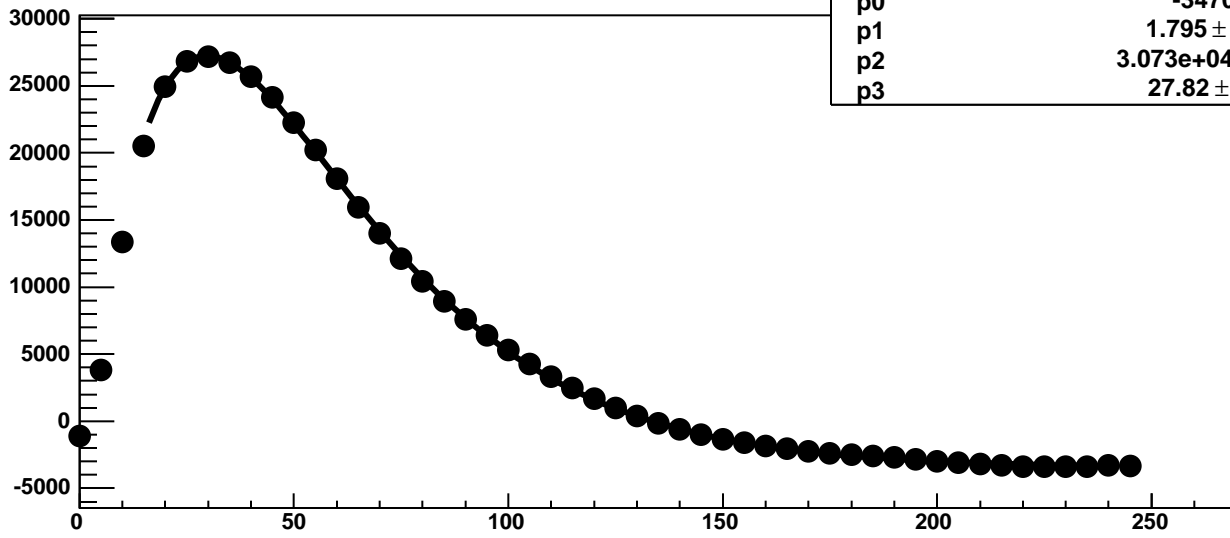
Chip 2, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

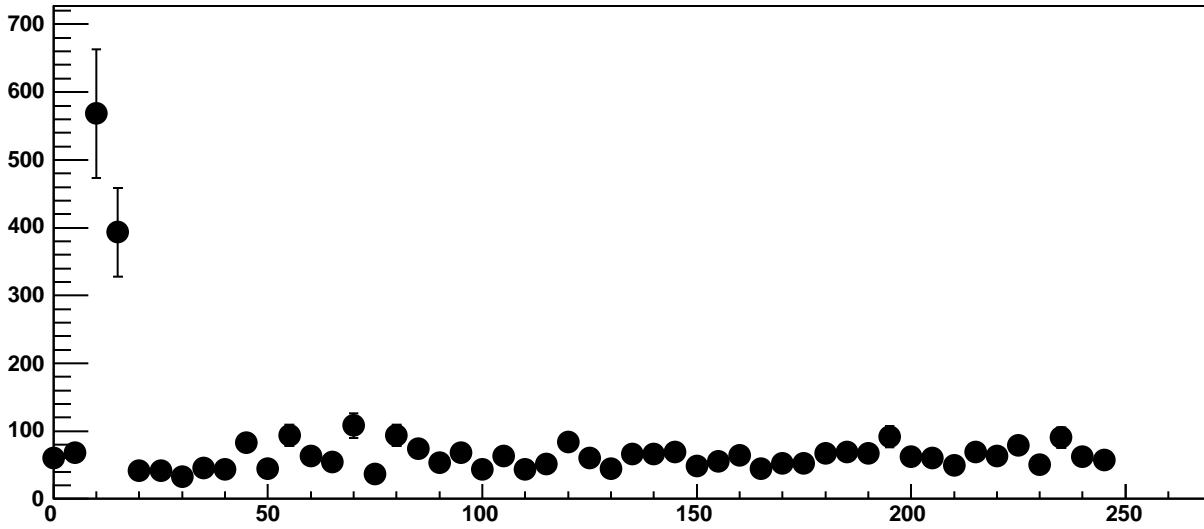


Chip 2, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

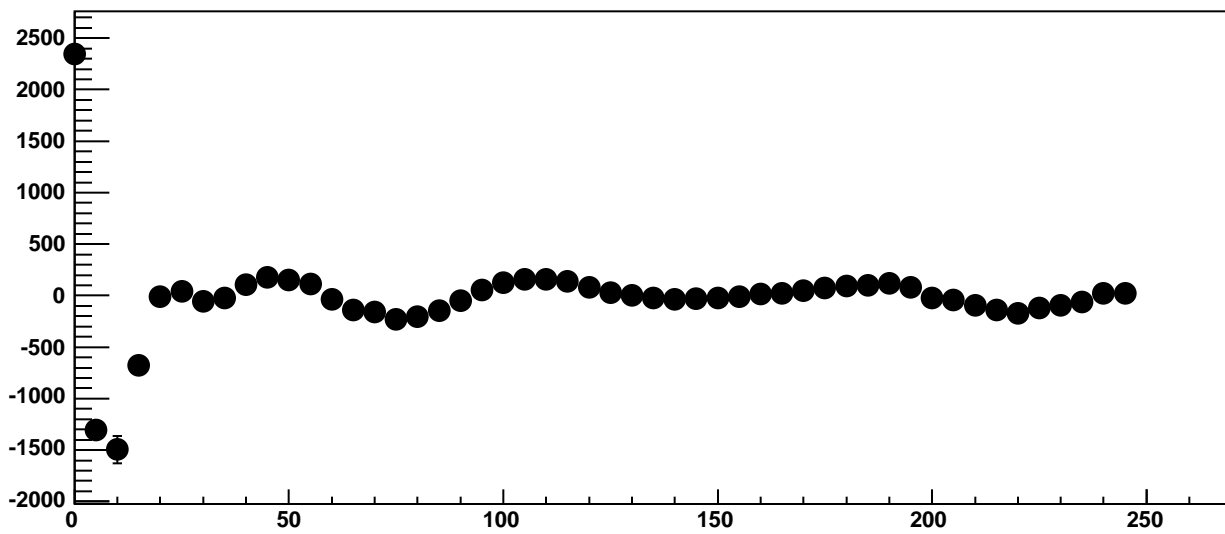


$\chi^2 / \text{ndf}$	3100 / 42
p0	-3470 ± 3.864
p1	1.795 ± 0.02046
p2	3.073e+04 ± 5.035
p3	27.82 ± 0.01147

Chip 2, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

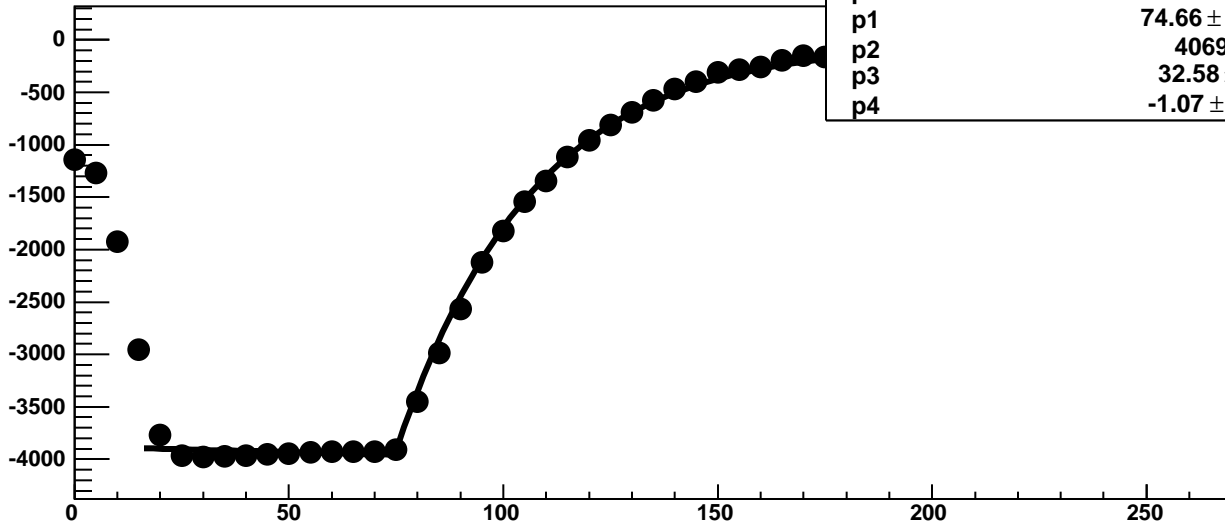


Chip 2, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



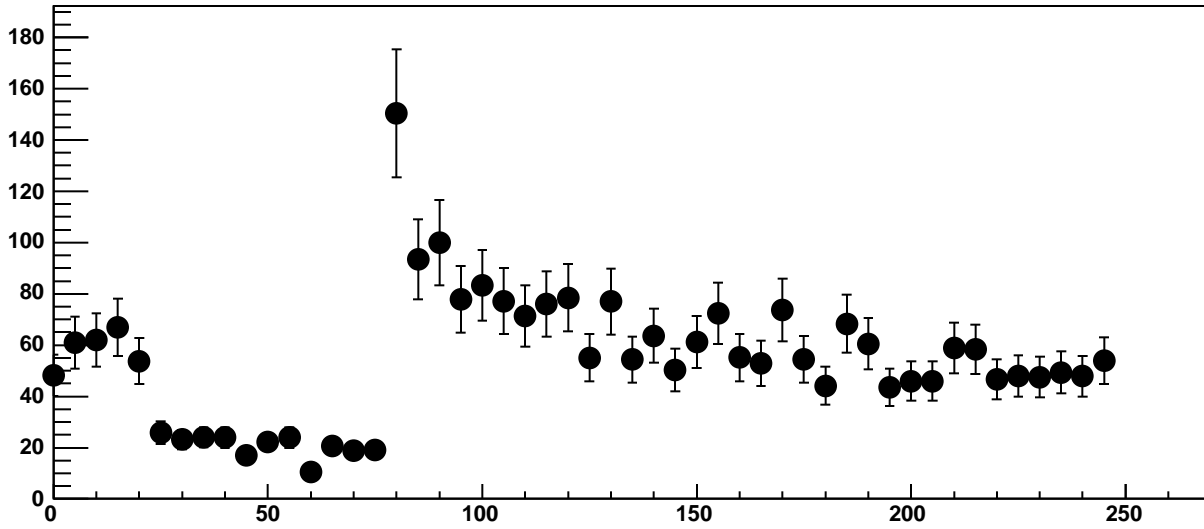


Chip 2, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

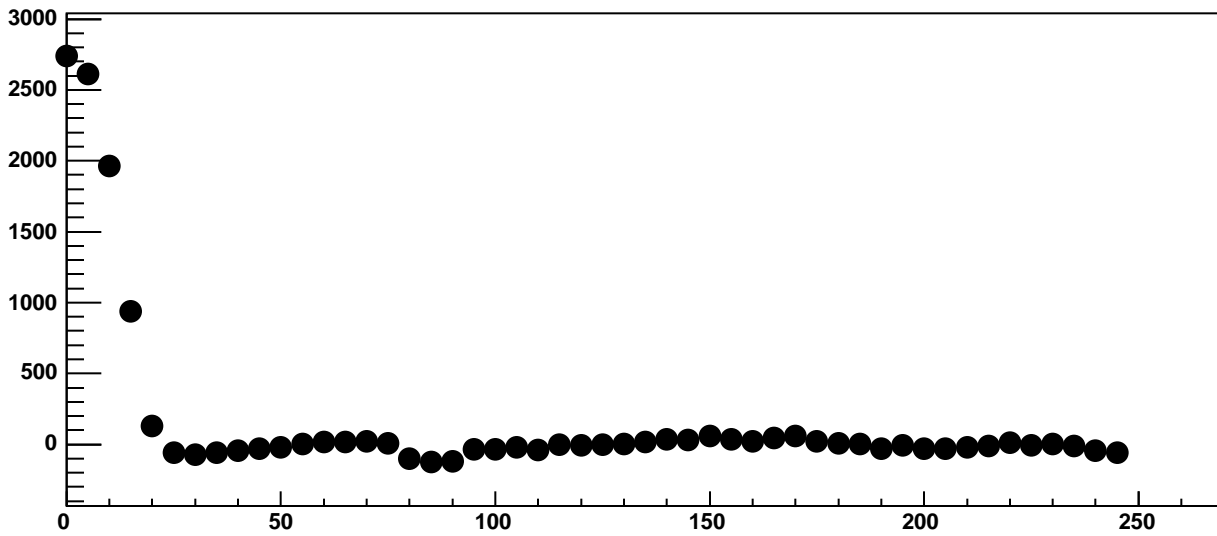


$\chi^2 / \text{ndf}$	4631 / 41
p0	$-3958 \pm 2.31$
p1	$74.66 \pm 0.04015$
p2	$4069 \pm 15.24$
p3	$32.58 \pm 0.2061$
p4	$-1.07 \pm 0.08491$

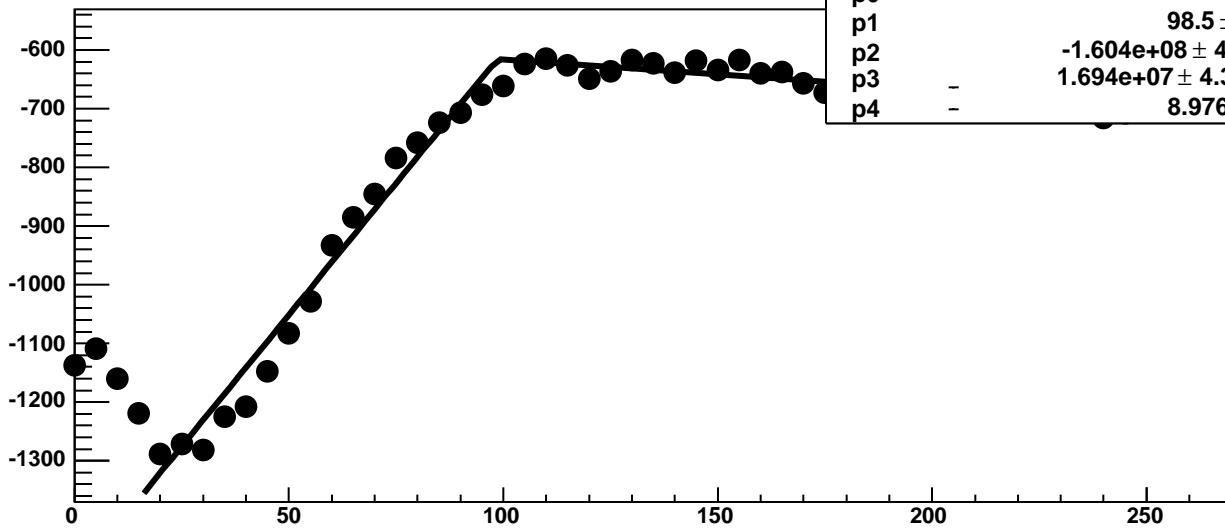
Chip 2, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

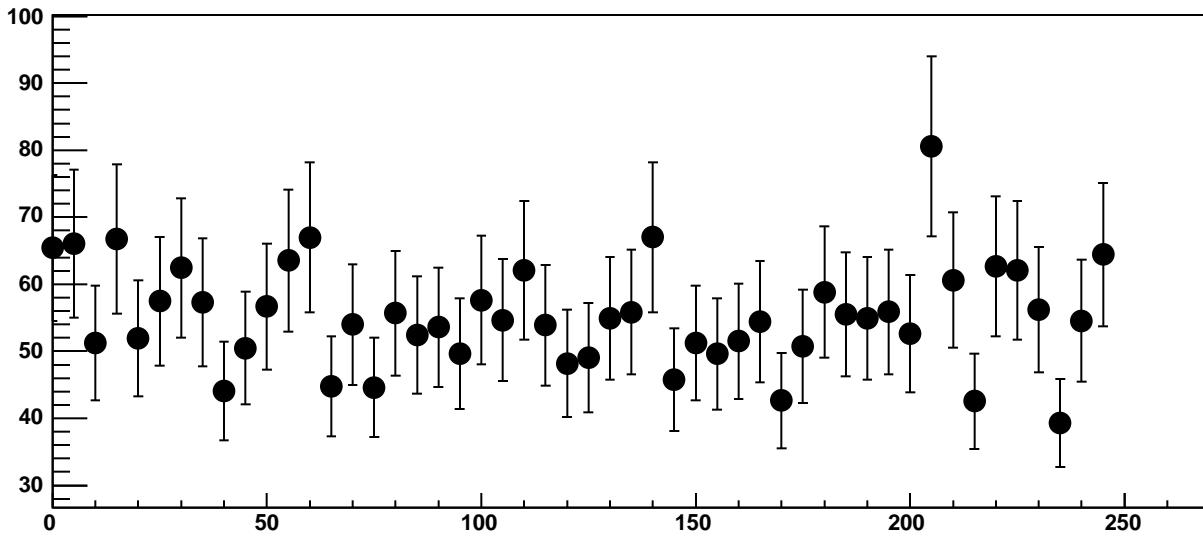


Chip 2, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

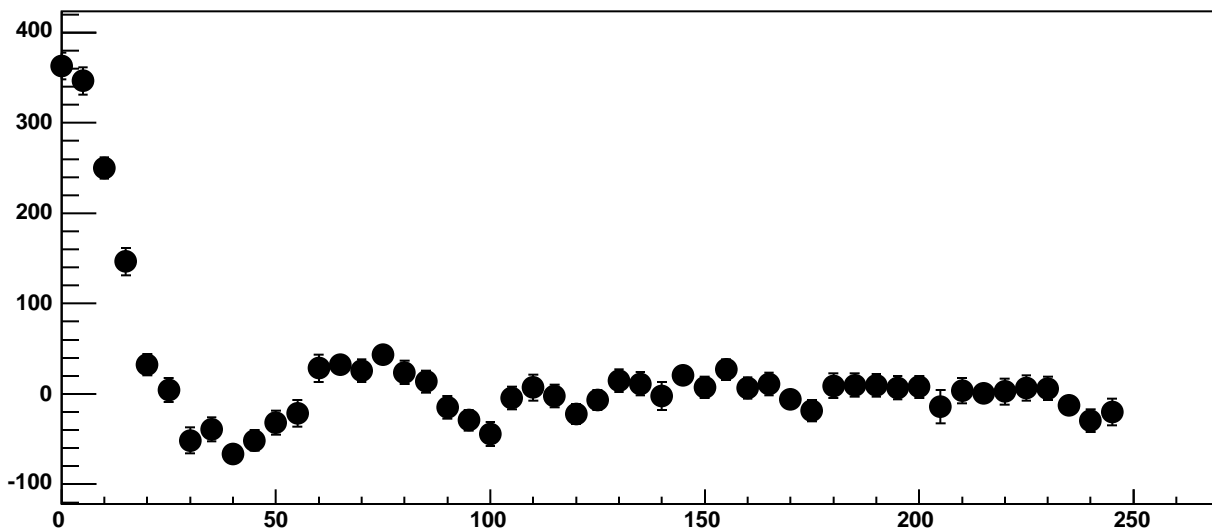


$\chi^2 / \text{ndf}$	282.5 / 41
p0	$-615.9 \pm 4.335$
p1	$98.5 \pm 0.7915$
p2	$-1.604\text{e}+08 \pm 4.93\text{e}+06$
p3	$1.694\text{e}+07 \pm 4.381\text{e}+05$
p4	$8.976 \pm 0.124$

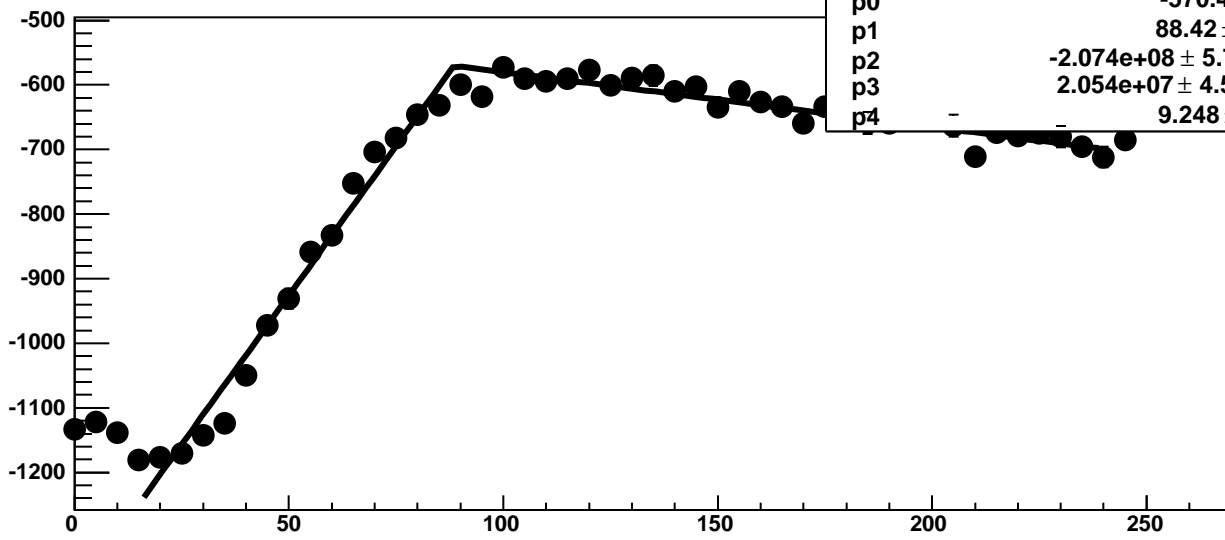
Chip 2, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

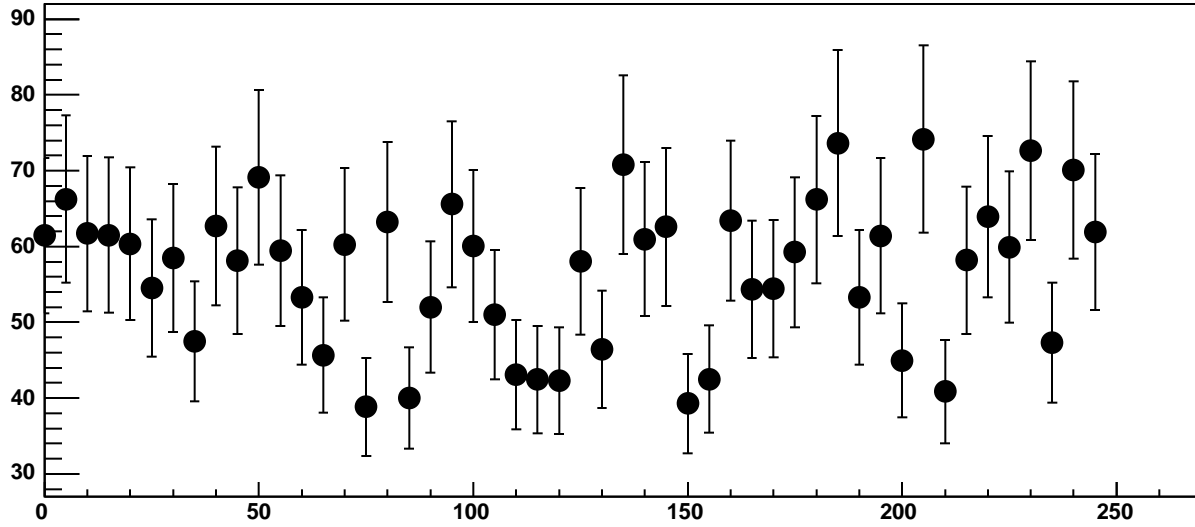


Chip 2, Channel 12, Enable 4, DAC=1600, ADC Mean vs Hold

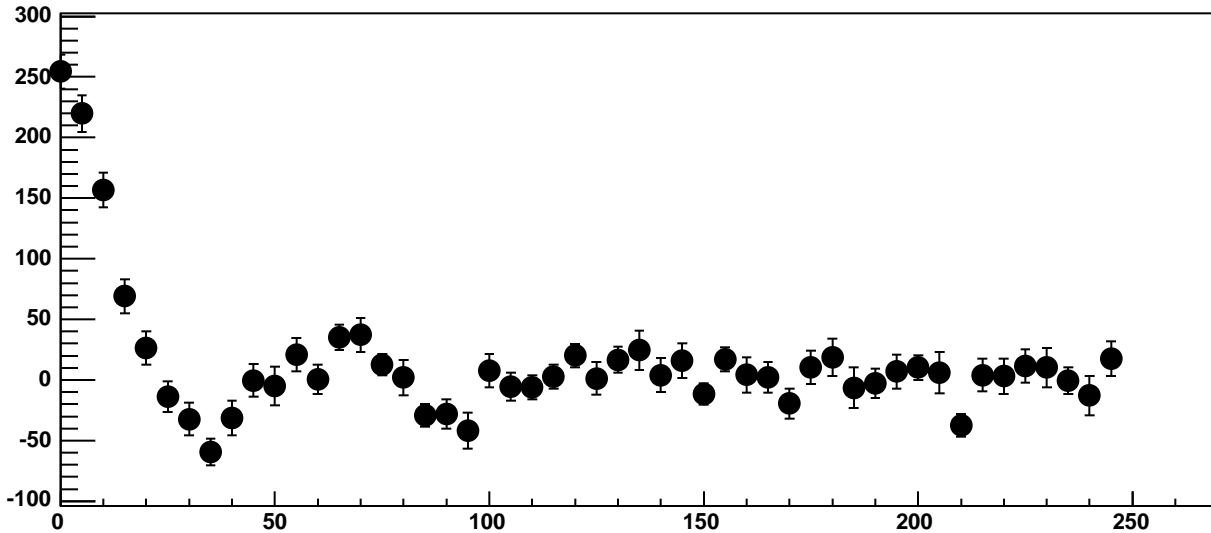


$\chi^2 / \text{ndf}$	155 / 41
p0	$-570.4 \pm 3.957$
p1	$88.42 \pm 0.7158$
p2	$-2.074\text{e}+08 \pm 5.767\text{e}+06$
p3	$2.054\text{e}+07 \pm 4.592\text{e}+05$
p4	$9.248 \pm 0.1421$

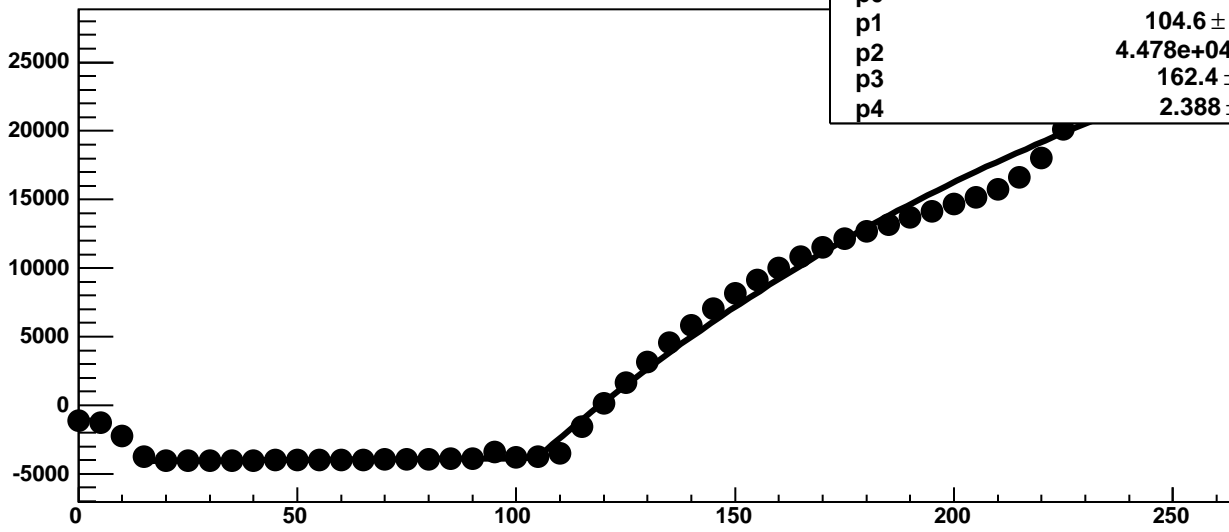
Chip 2, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold

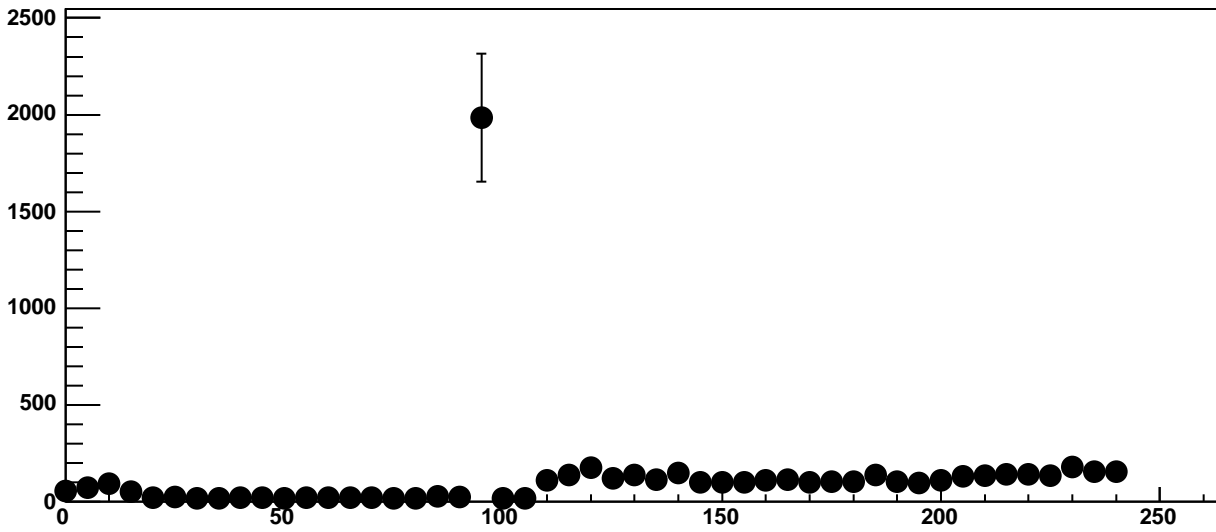


Chip 2, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

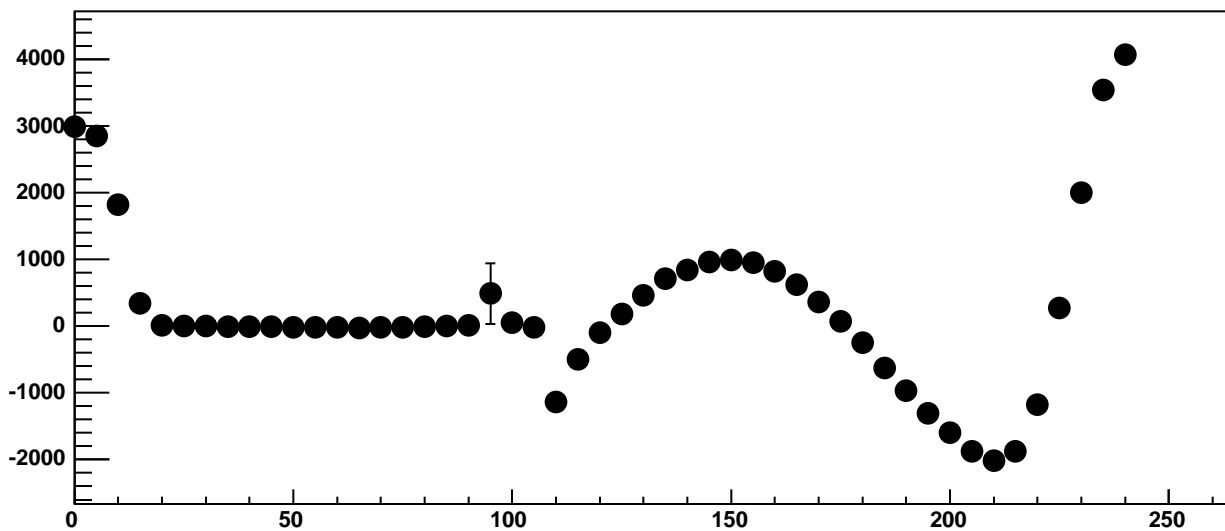


$\chi^2 / \text{ndf}$	5.864e+04 / 41
p0	-3857 ± 2.748
p1	104.6 ± 0.01795
p2	4.478e+04 ± 175.6
p3	162.4 ± 0.8524
p4	2.388 ± 0.0512

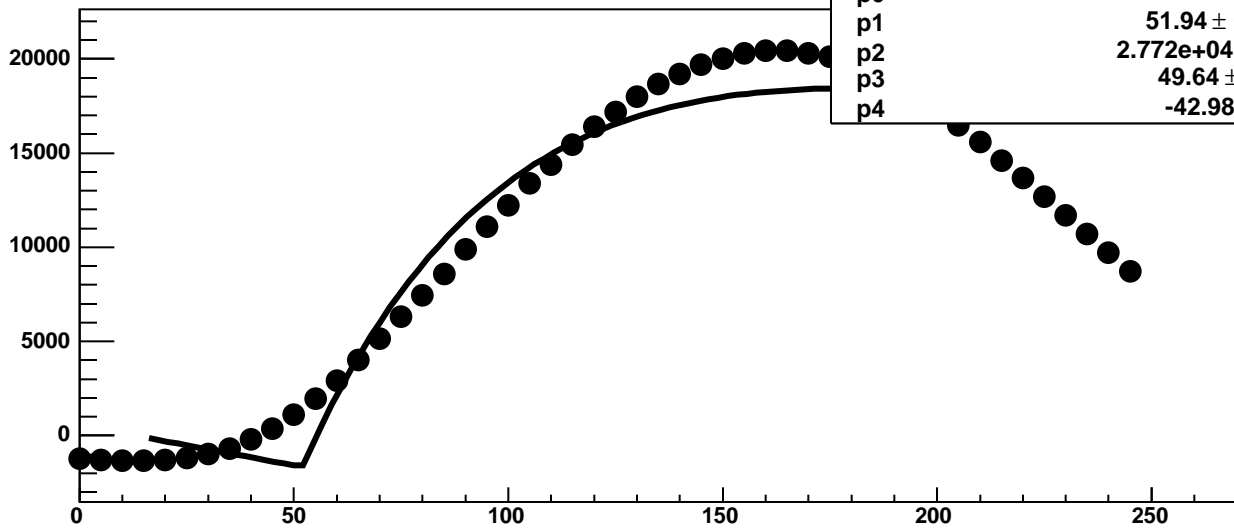
Chip 2, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold



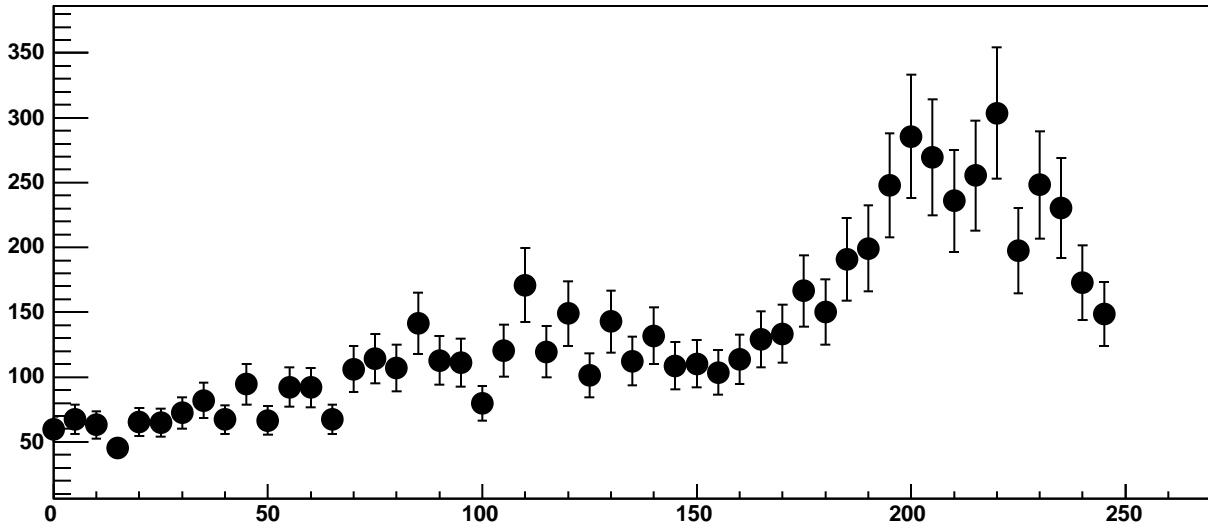
Chip 2, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



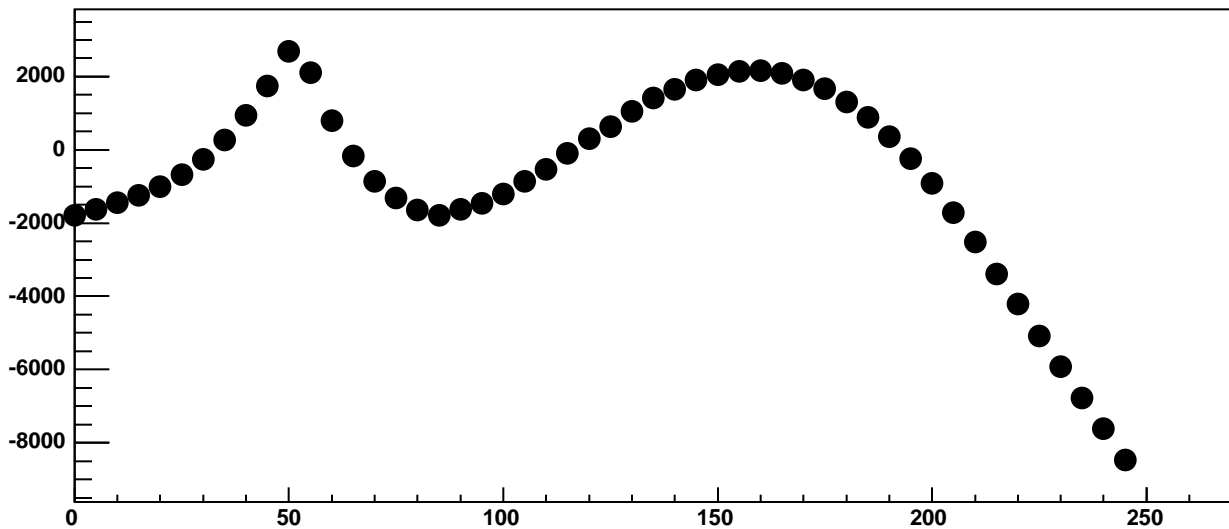
Chip 2, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold



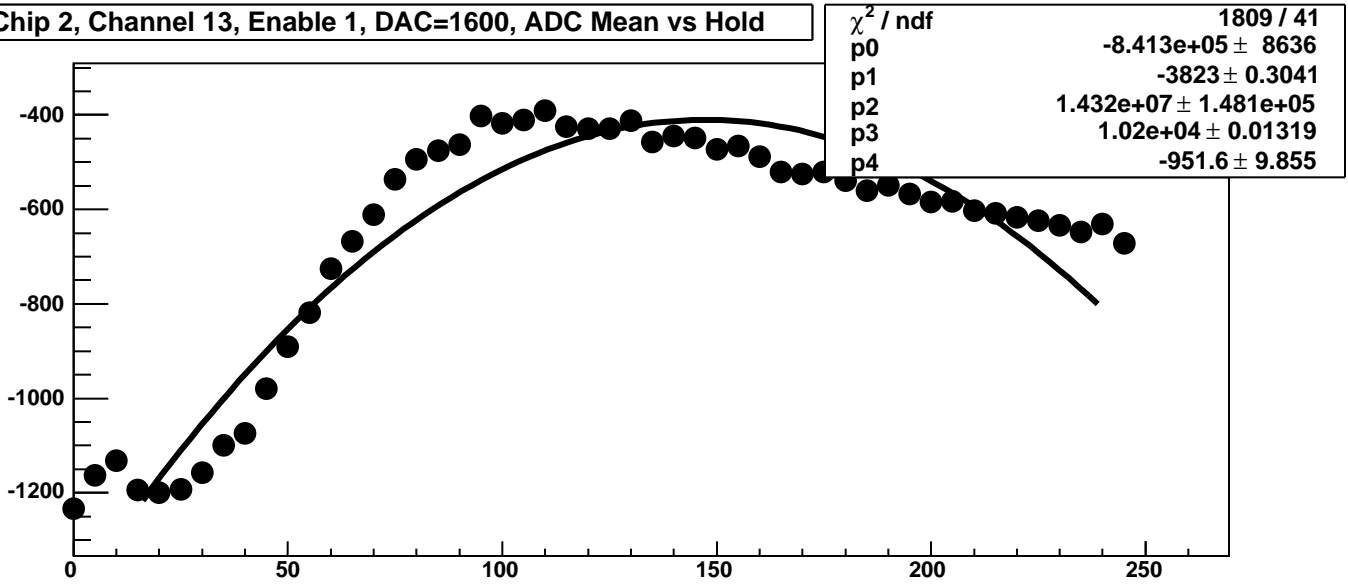
Chip 2, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



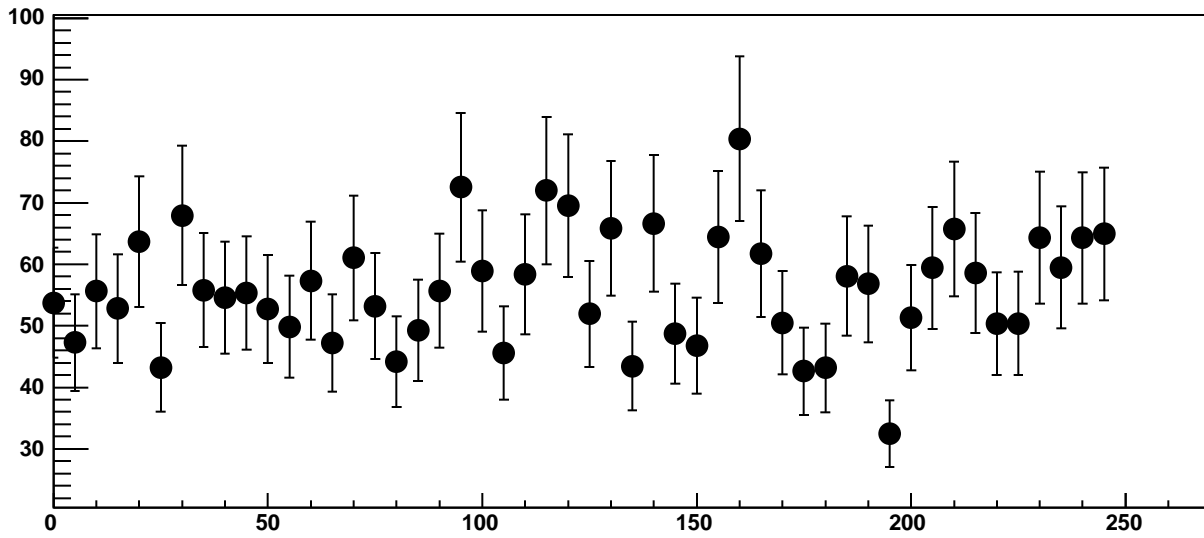
Chip 2, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold



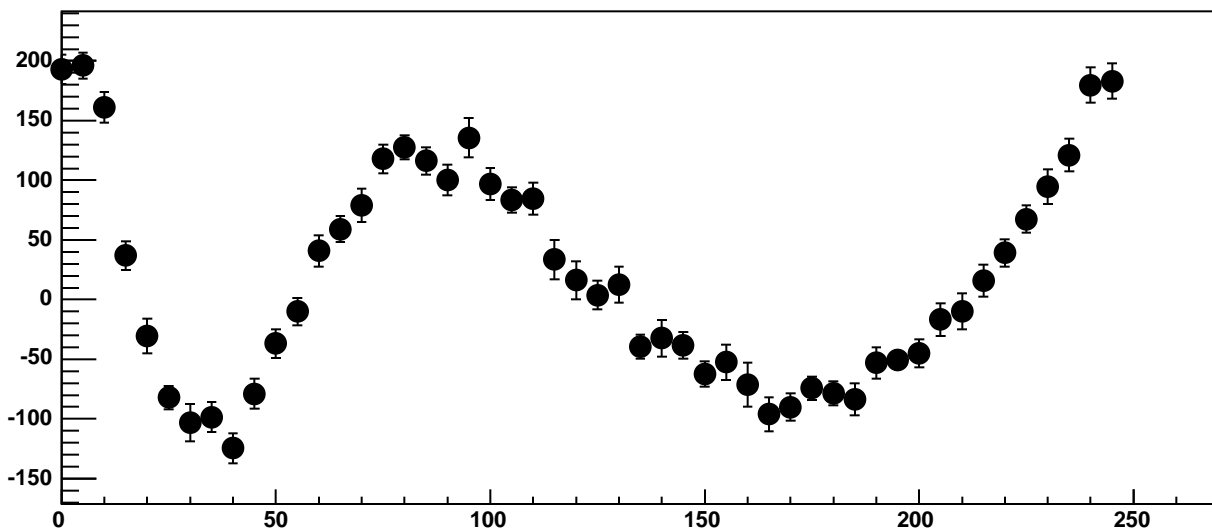
Chip 2, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold



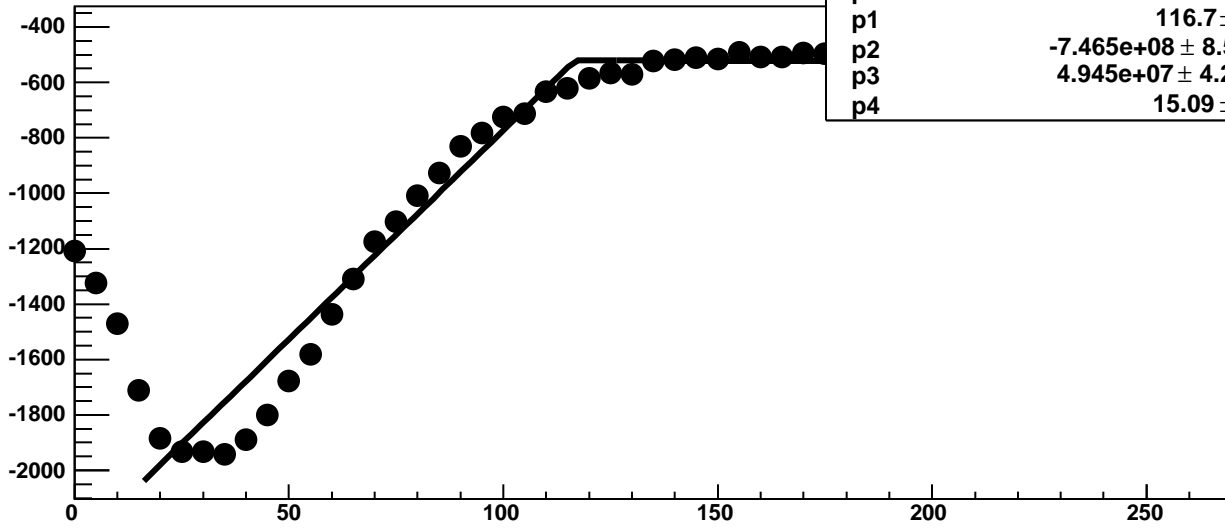
Chip 2, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold

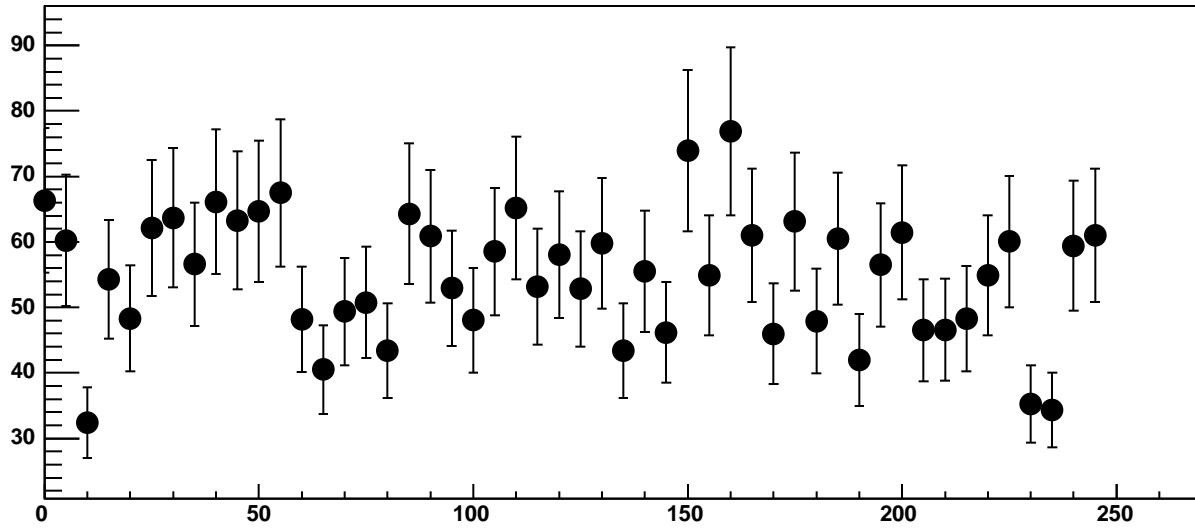


Chip 2, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

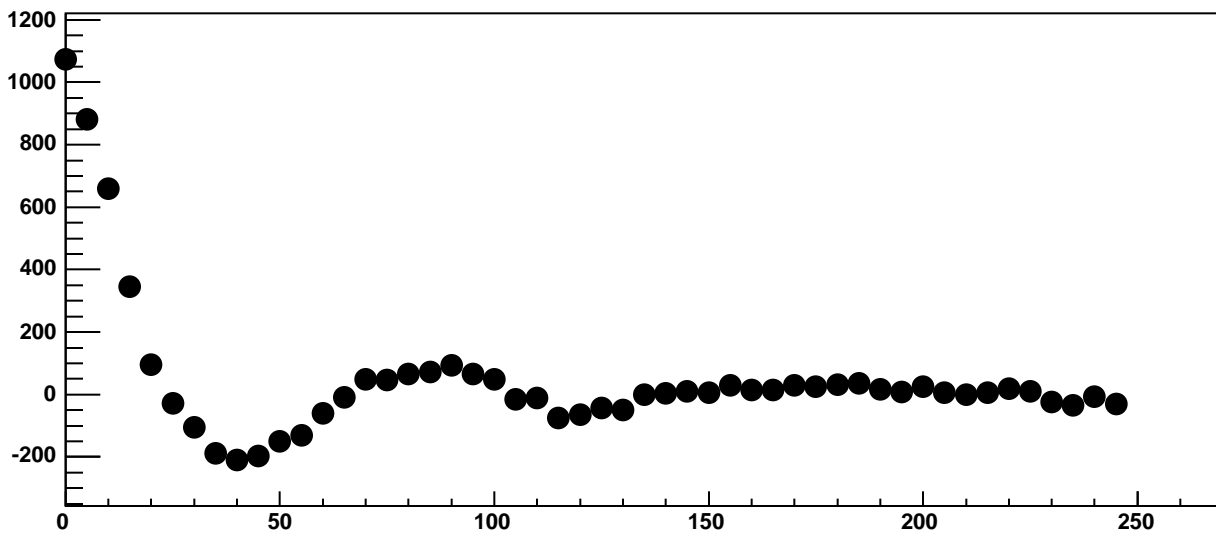


$\chi^2 / \text{ndf}$	2052 / 41
p0	$-521.2 \pm 4.916$
p1	$116.7 \pm 0.4846$
p2	$-7.465\text{e}+08 \pm 8.529\text{e}+06$
p3	$4.945\text{e}+07 \pm 4.239\text{e}+05$
p4	$15.09 \pm 0.0925$

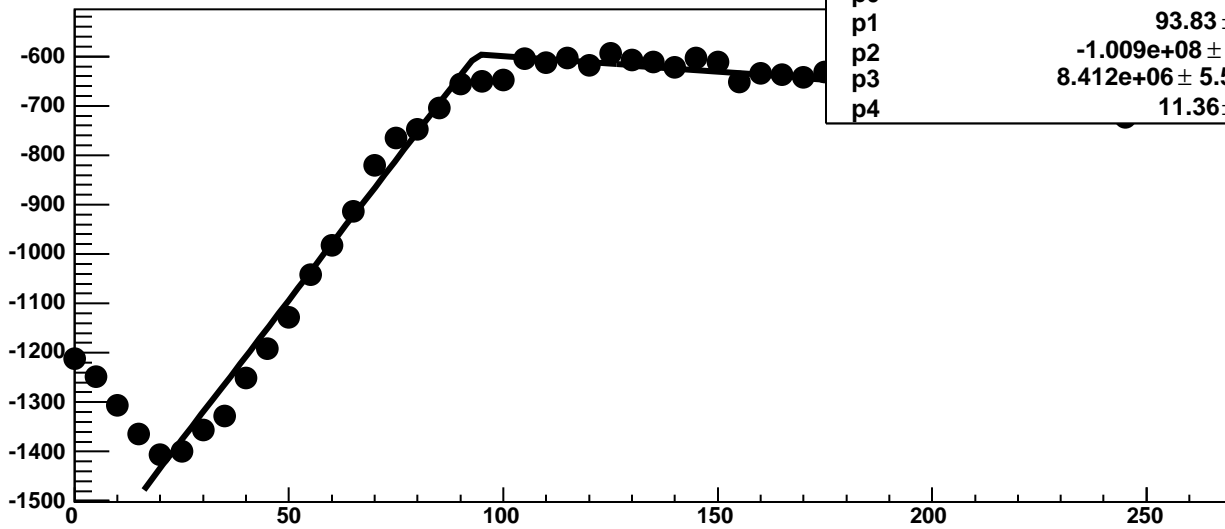
Chip 2, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

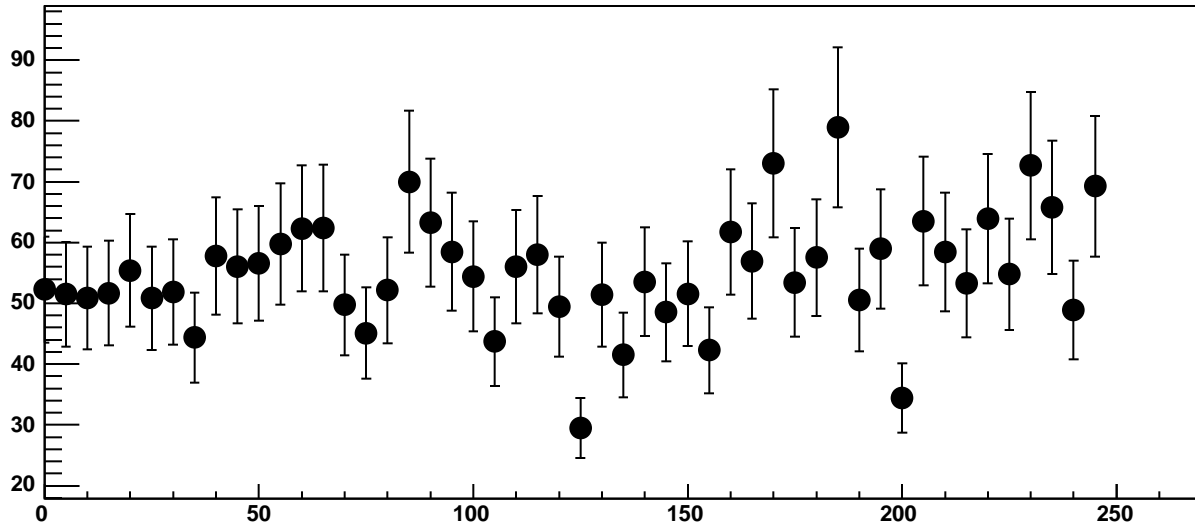


Chip 2, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

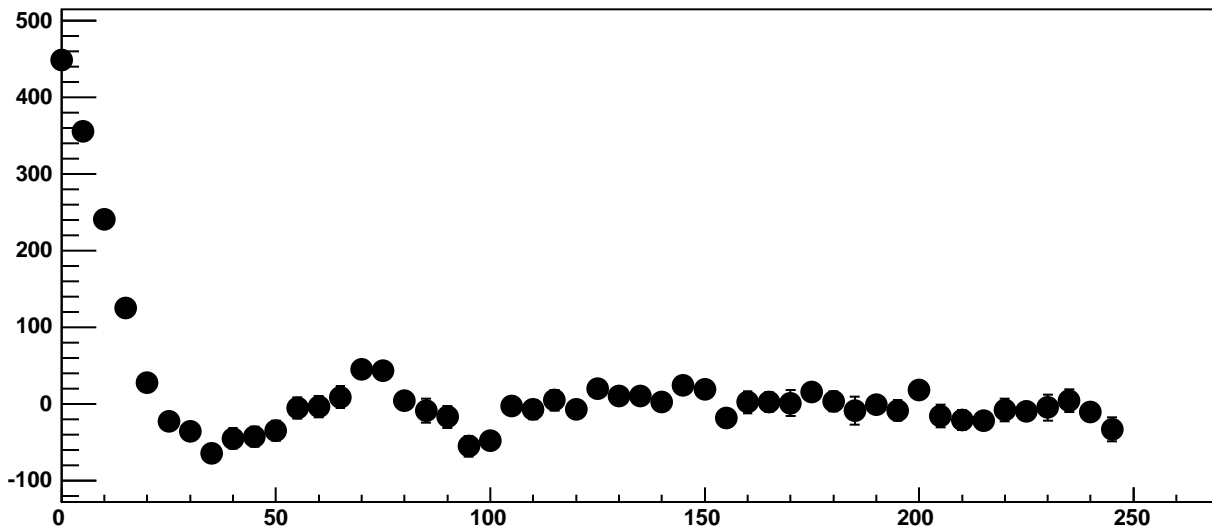


$\chi^2 / \text{ndf}$	305.4 / 41
p0	$-595.2 \pm 3.871$
p1	$93.83 \pm 0.6499$
p2	$-1.009\text{e}+08 \pm 6.8\text{e}+06$
p3	$8.412\text{e}+06 \pm 5.586\text{e}+05$
p4	$11.36 \pm 0.1363$

Chip 2, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

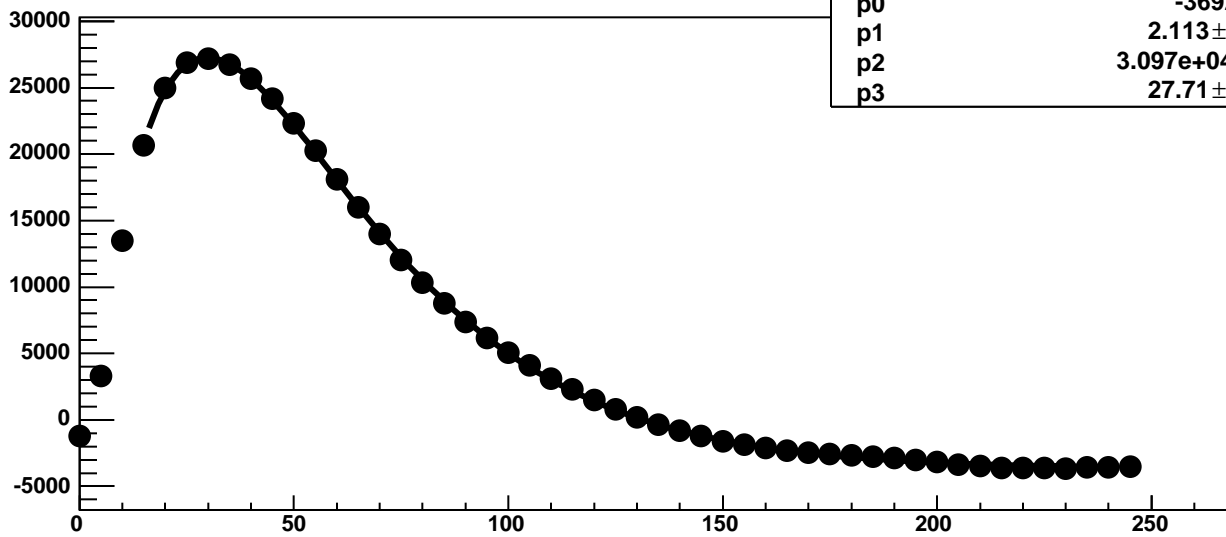


Chip 2, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

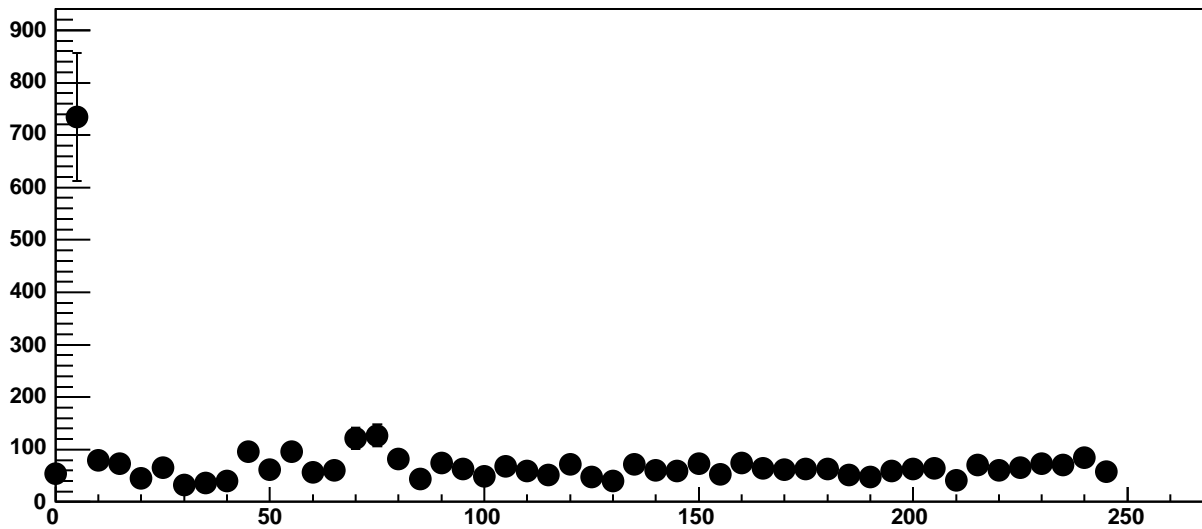




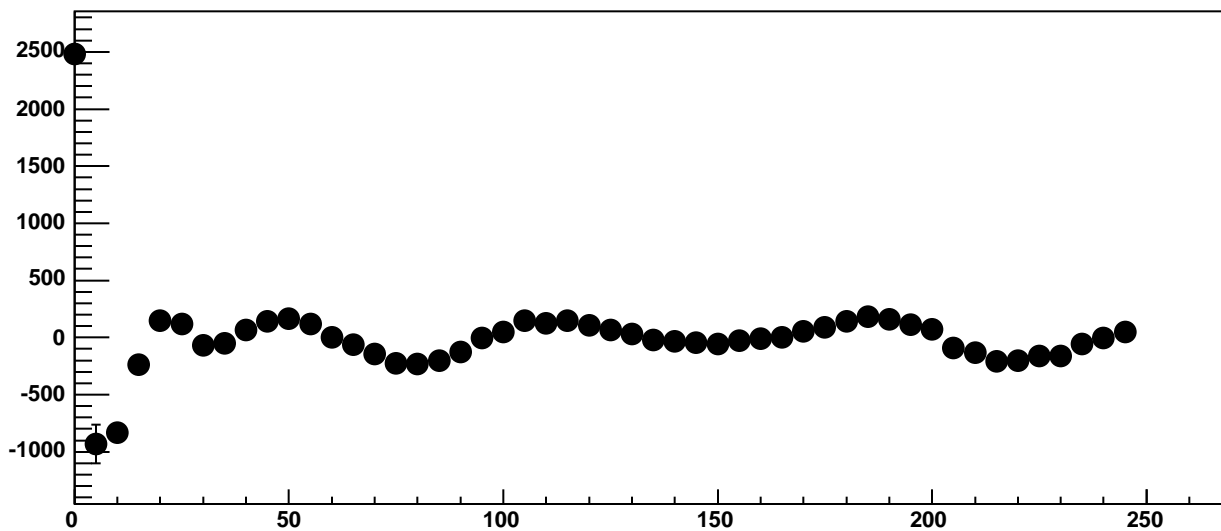
Chip 2, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold



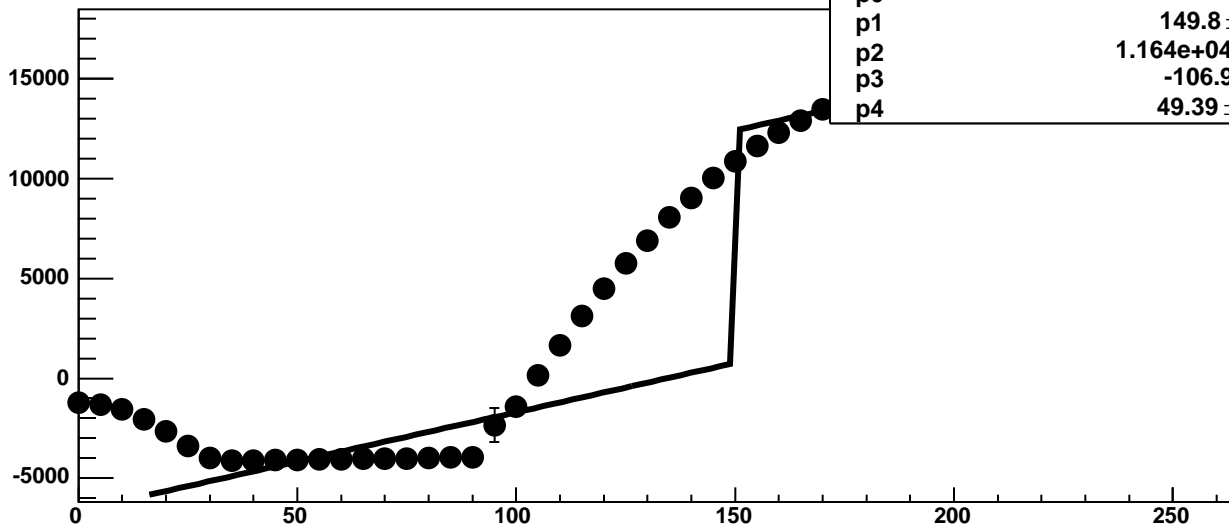
Chip 2, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold

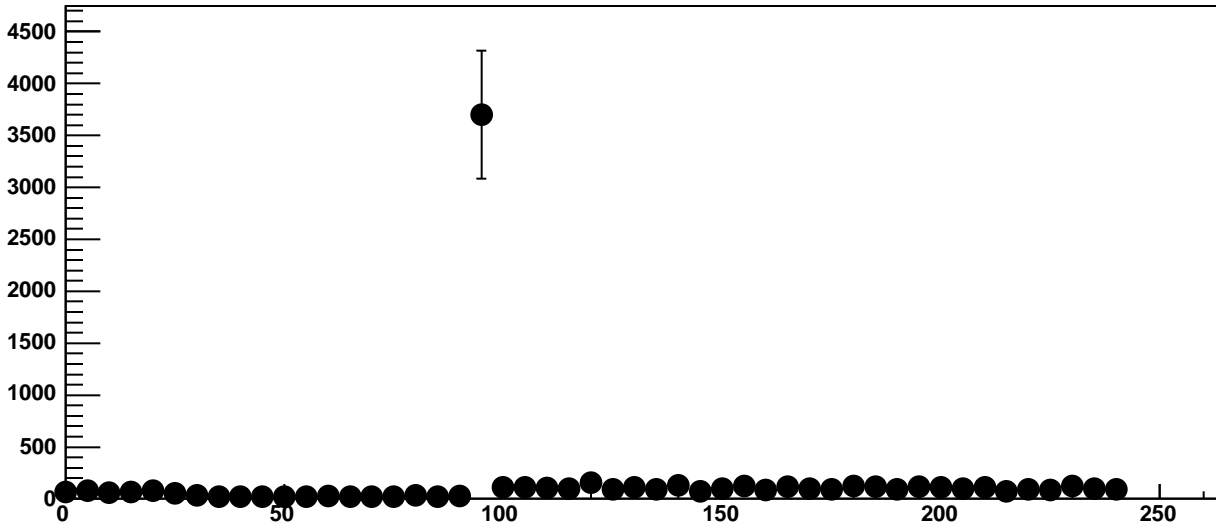


Chip 2, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

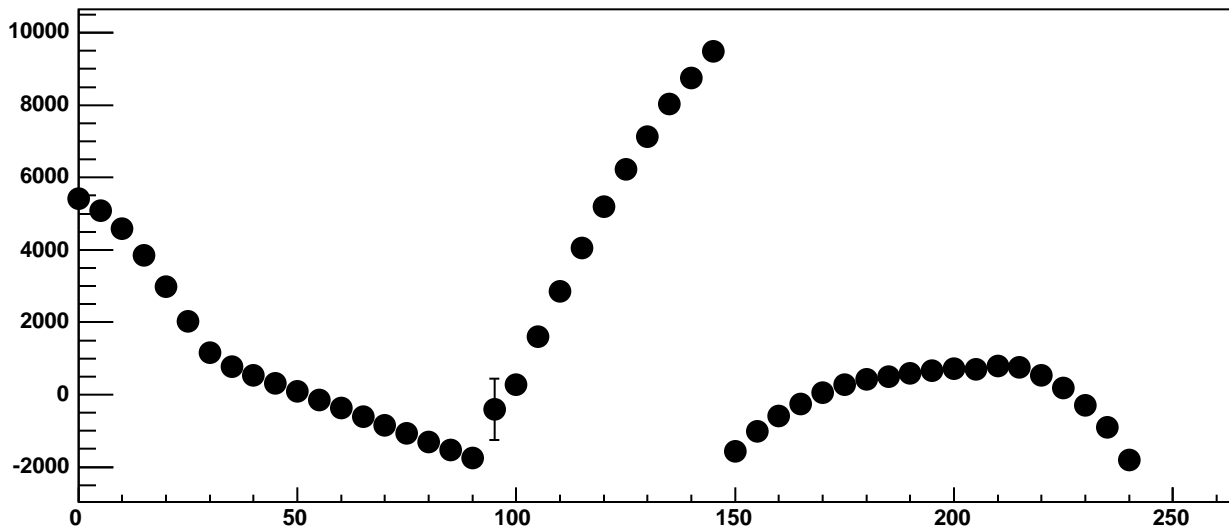


$\chi^2 / \text{ndf}$	1.224e+06 / 41
p0	766.2 ± 3.735
p1	149.8 ± 0.3389
p2	1.164e+04 ± 16.89
p3	-106.9 ± 2.415
p4	49.39 ± 0.1825

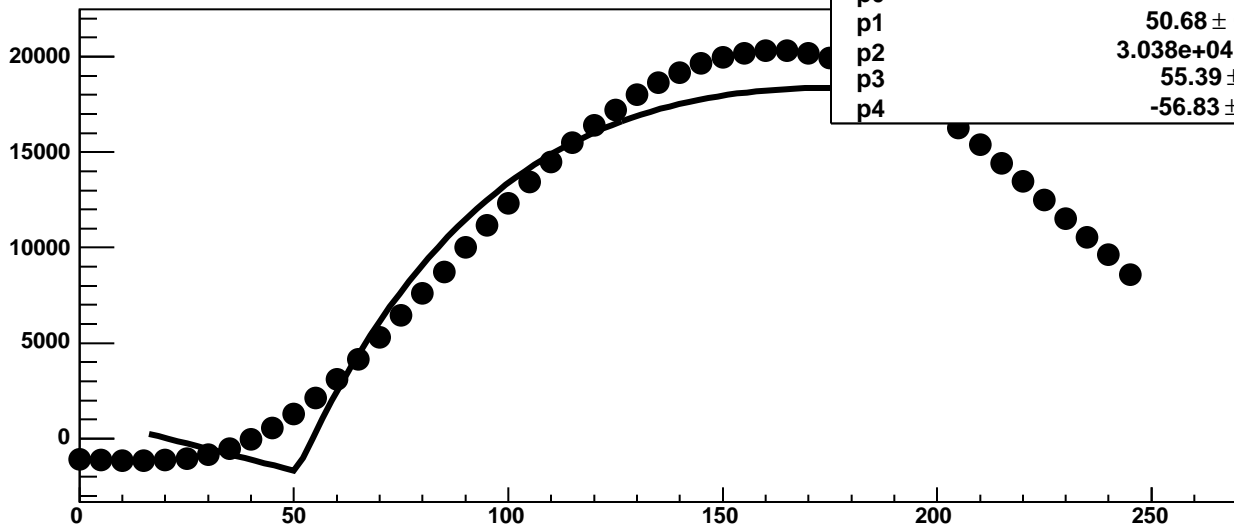
Chip 2, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



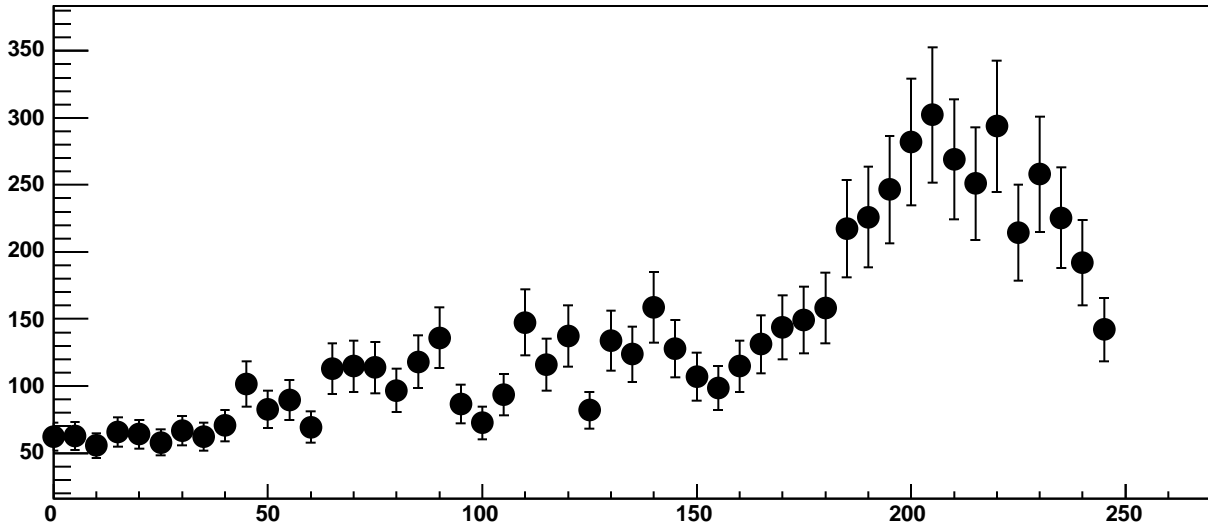
Chip 2, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold



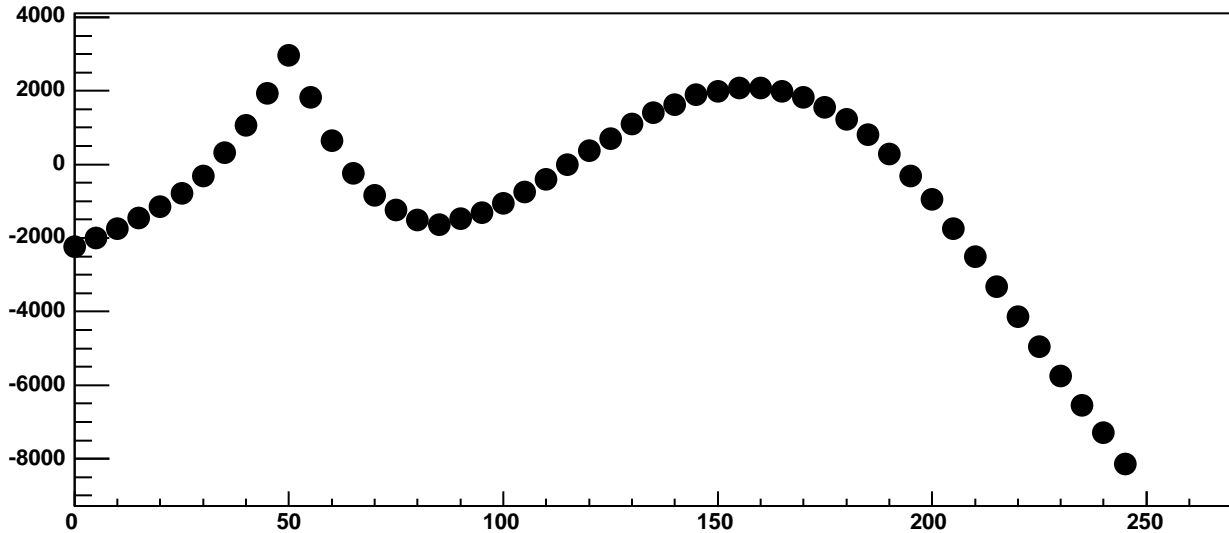
Chip 2, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold



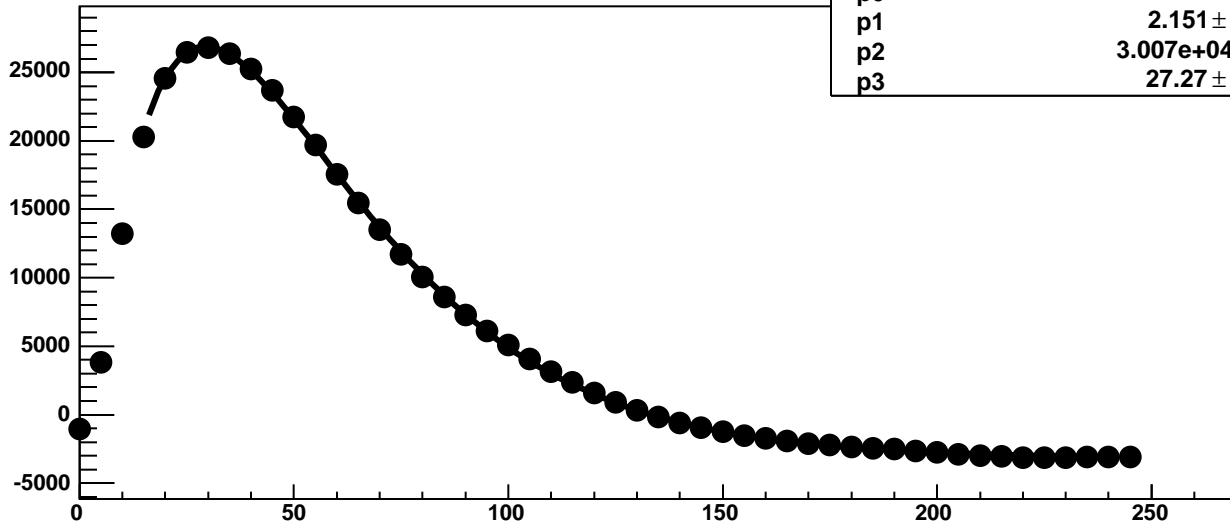
Chip 2, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

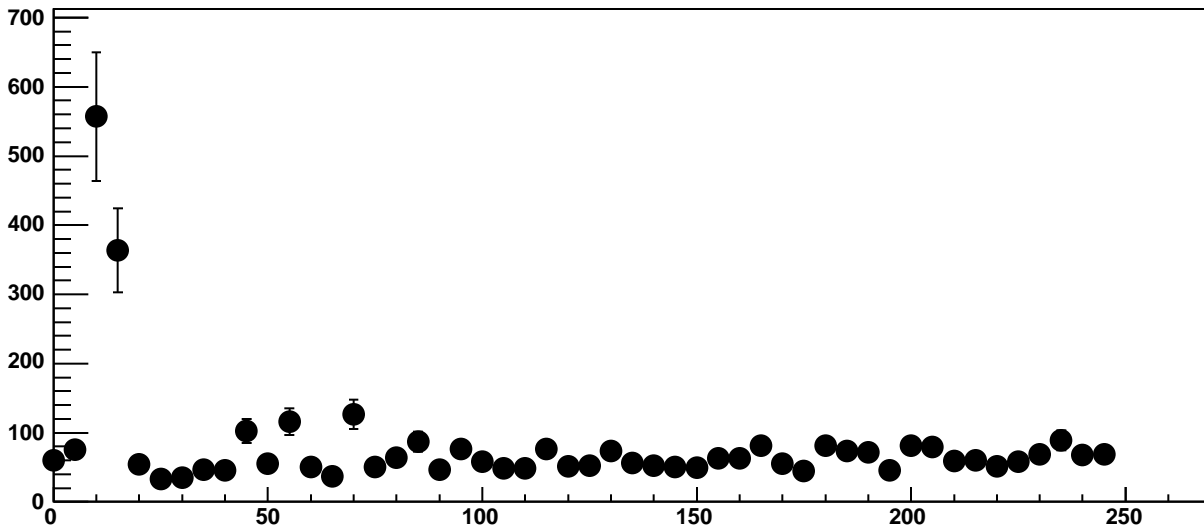


Chip 2, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold

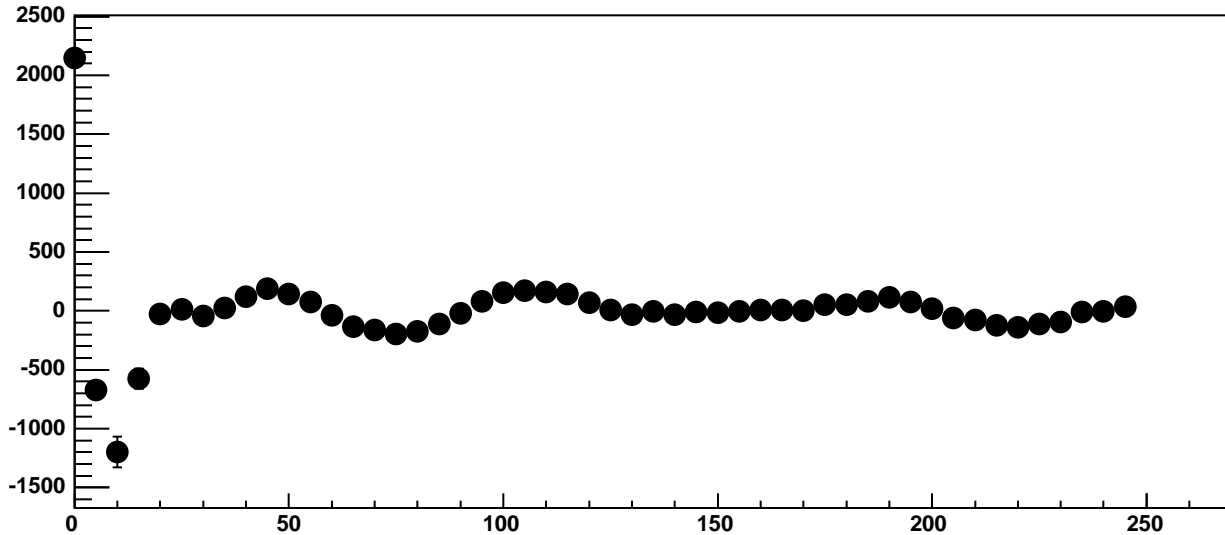


$\chi^2 / \text{ndf}$	2414 / 42
p0	-3197 ± 3.877
p1	2.151 ± 0.02302
p2	3.007e+04 ± 5.148
p3	27.27 ± 0.01229

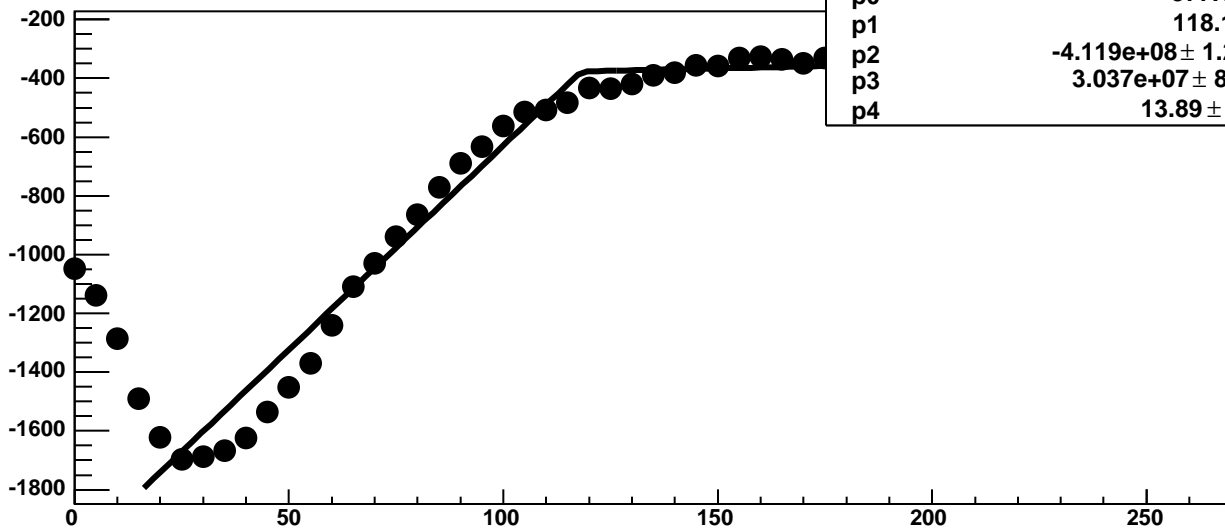
Chip 2, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

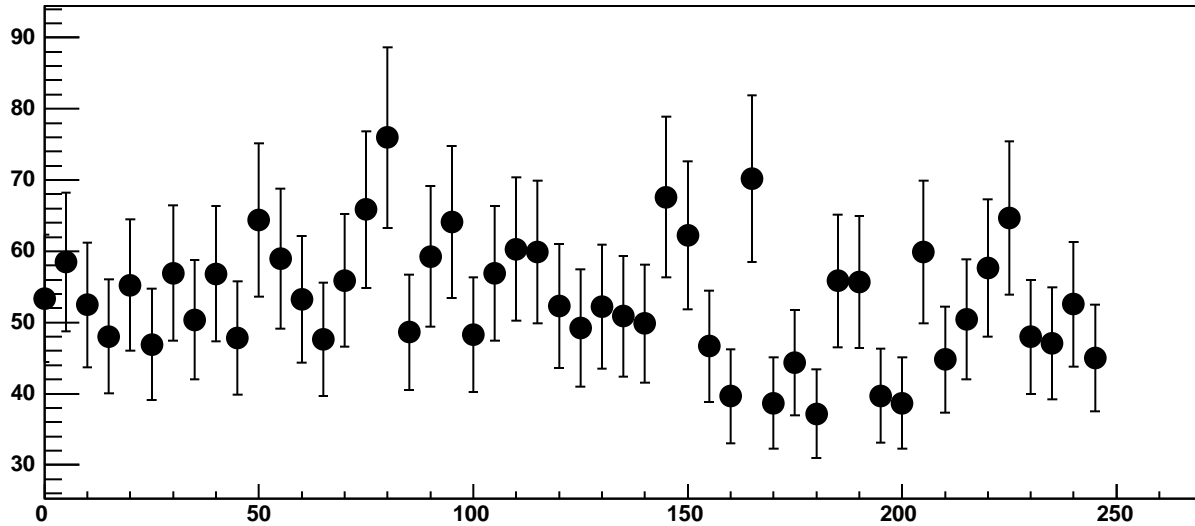


Chip 2, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

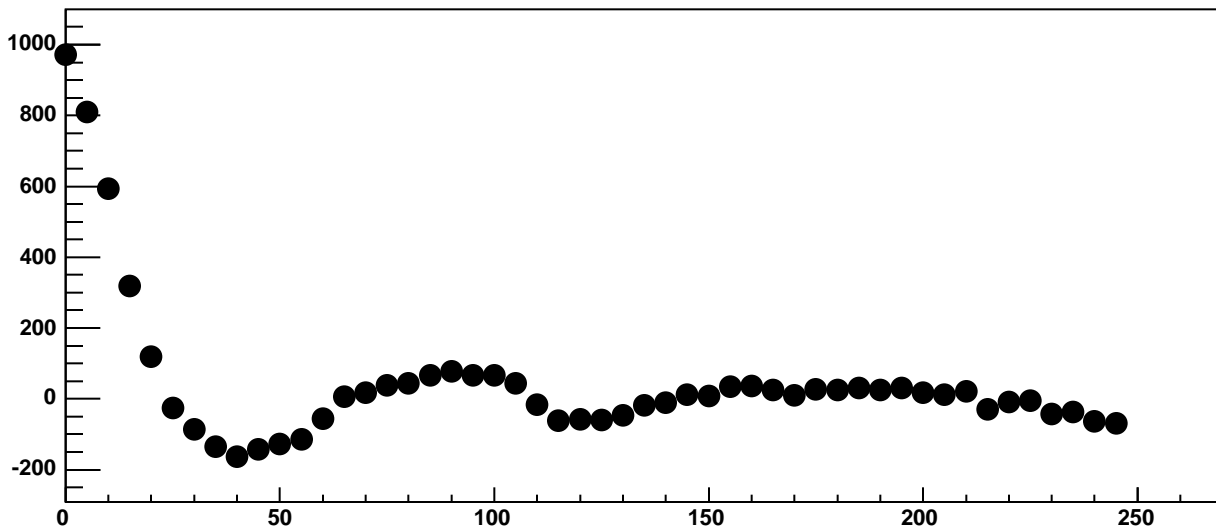


$\chi^2 / \text{ndf}$	1978 / 41
p0	-377.1 ± 4.767
p1	118.1 ± 0.543
p2	-4.119e+08 ± 1.209e+07
p3	3.037e+07 ± 8.52e+05
p4	13.89 ± 0.08984

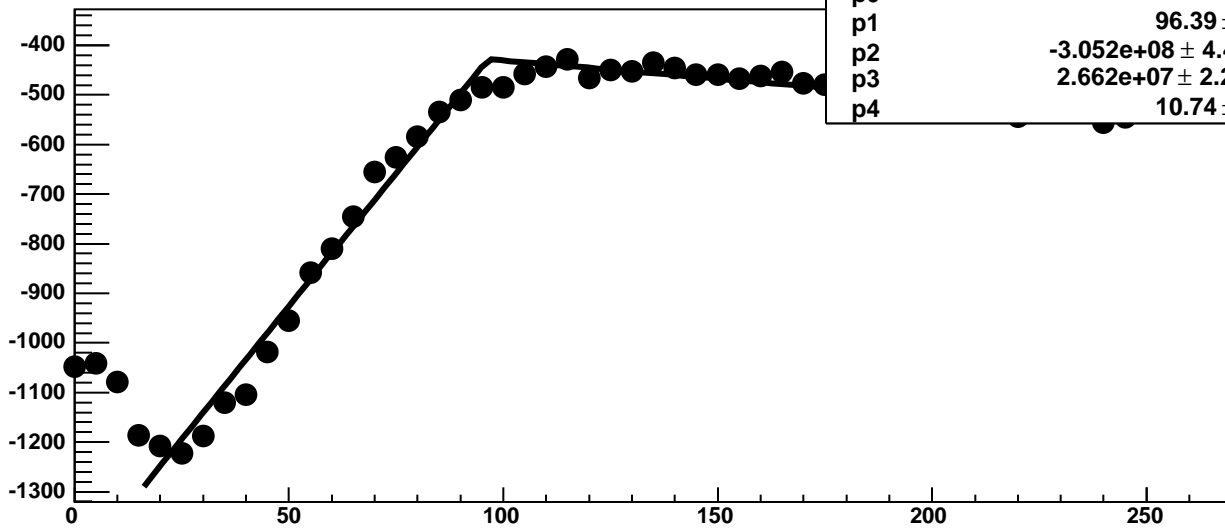
Chip 2, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

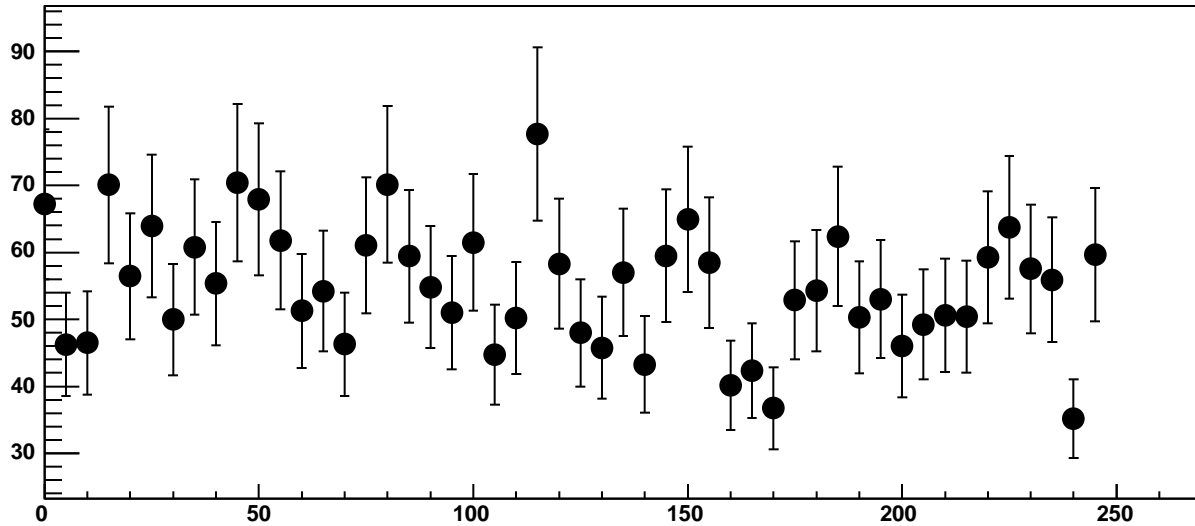


Chip 2, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

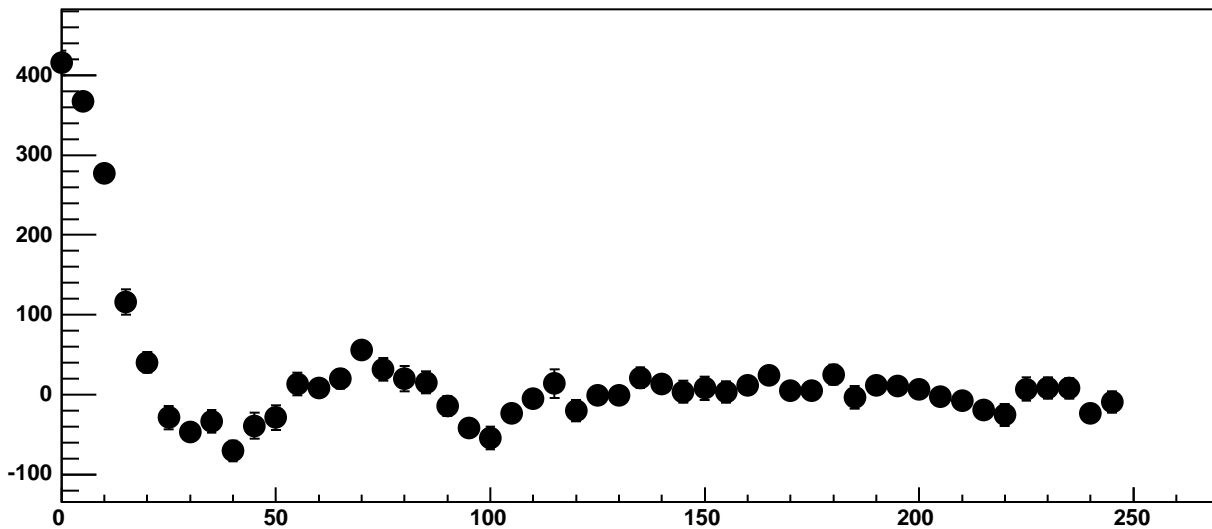


$\chi^2 / \text{ndf}$	240 / 41
p0	-428 ± 4.183
p1	96.39 ± 0.6622
p2	-3.052e+08 ± 4.459e+06
p3	2.662e+07 ± 2.214e+05
p4	10.74 ± 0.1317

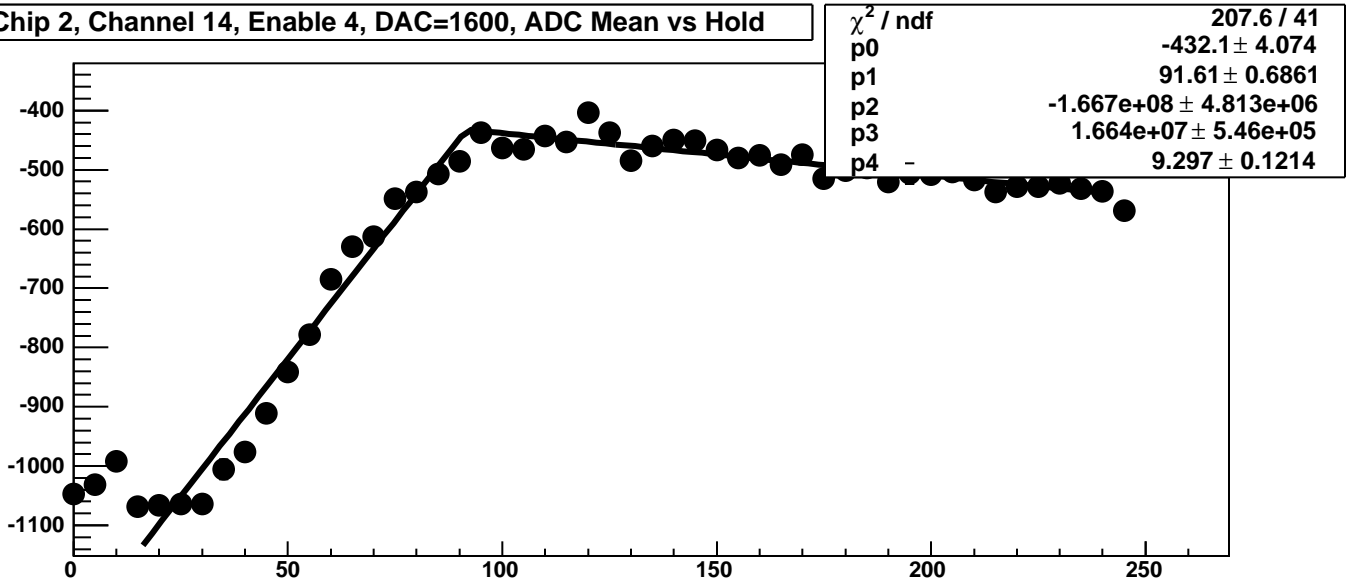
Chip 2, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



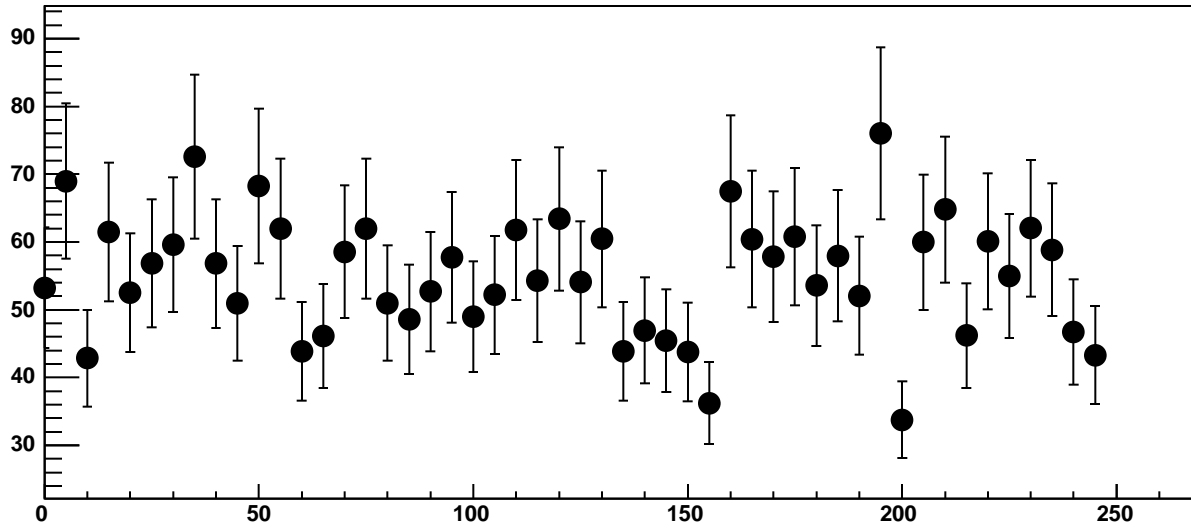
Chip 2, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold



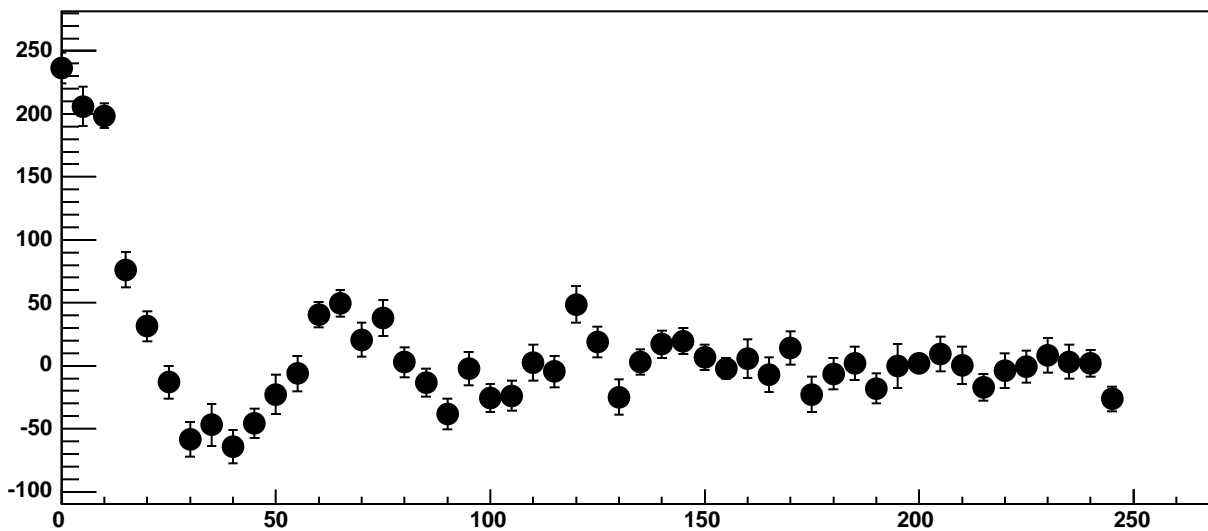
Chip 2, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold



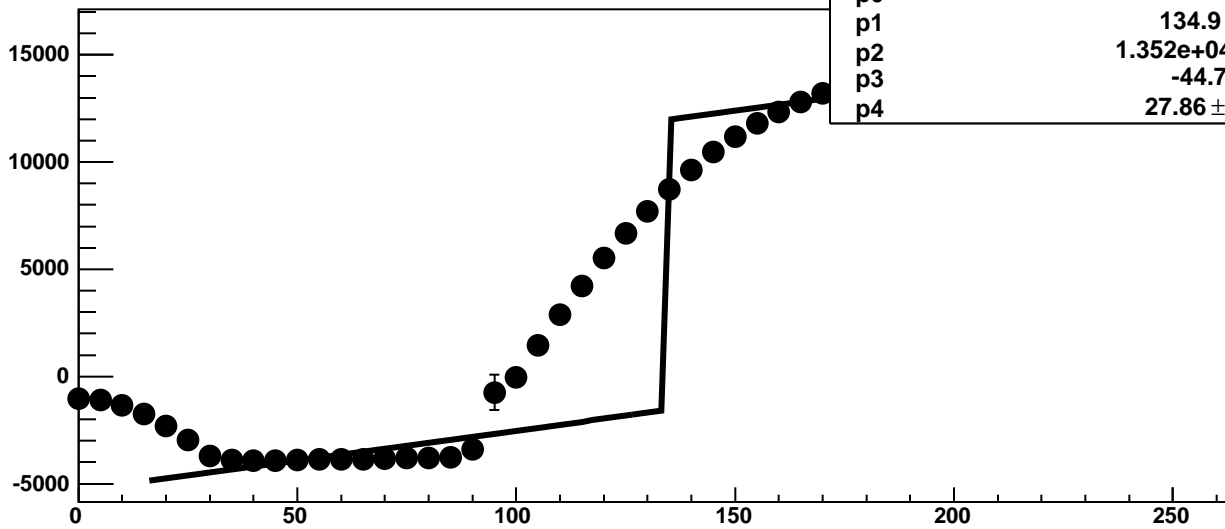
Chip 2, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

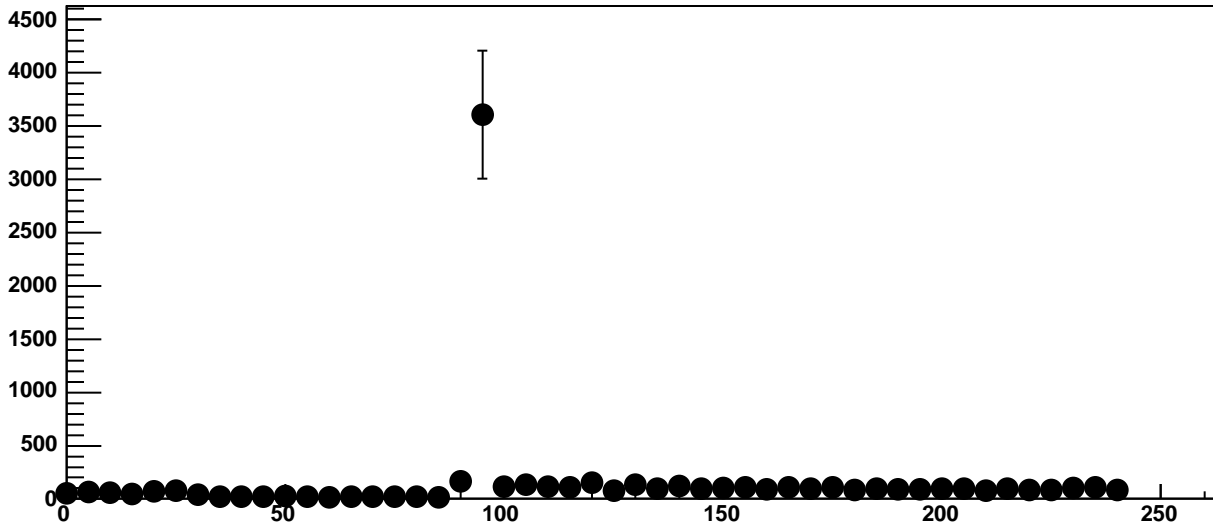


Chip 2, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

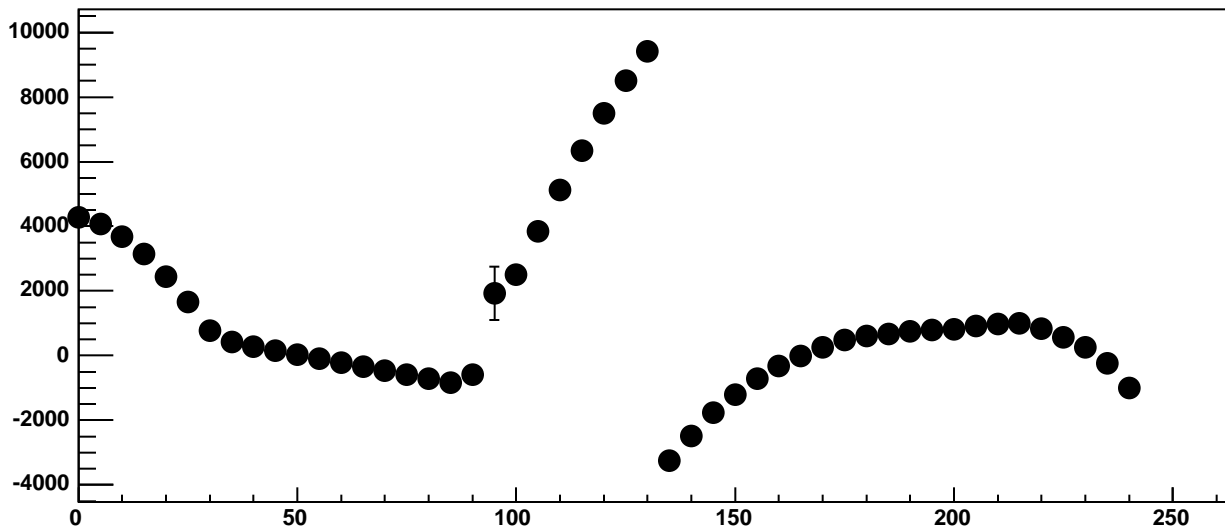


$\chi^2 / \text{ndf}$	7.775e+05 / 41
p0	-1555 ± 1.135
p1	134.9 ± 0.3812
p2	1.352e+04 ± 1.746
p3	-44.72 ± 1.22
p4	27.86 ± 0.01606

Chip 2, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

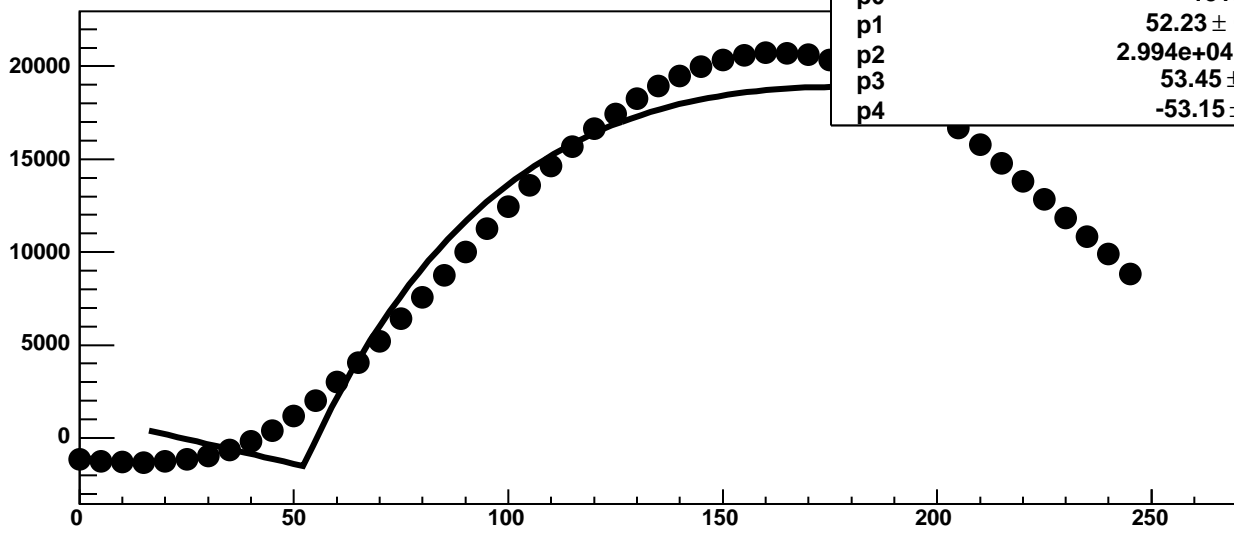


Chip 2, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold



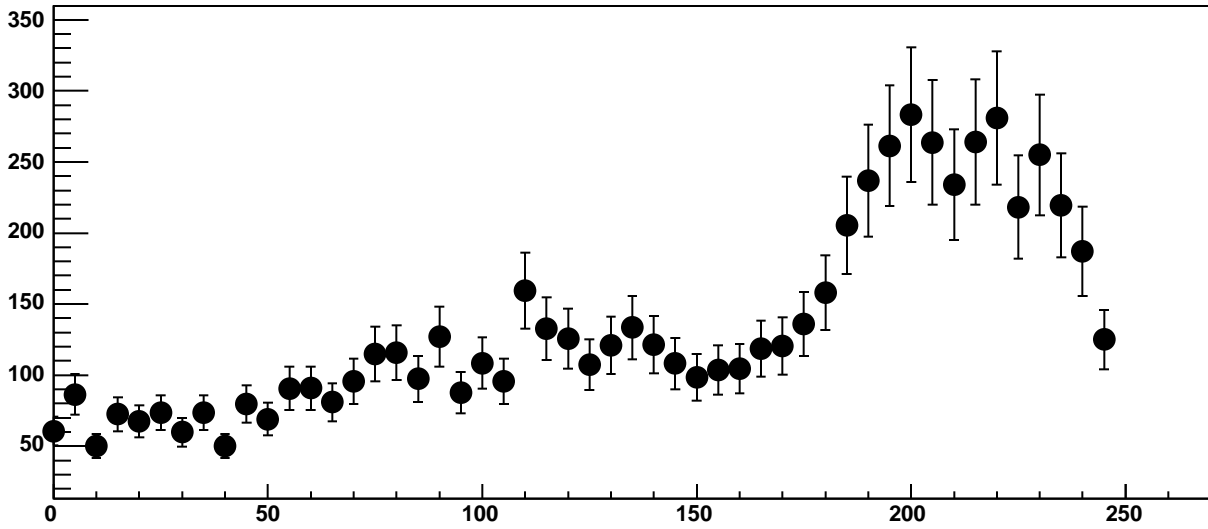


Chip 2, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

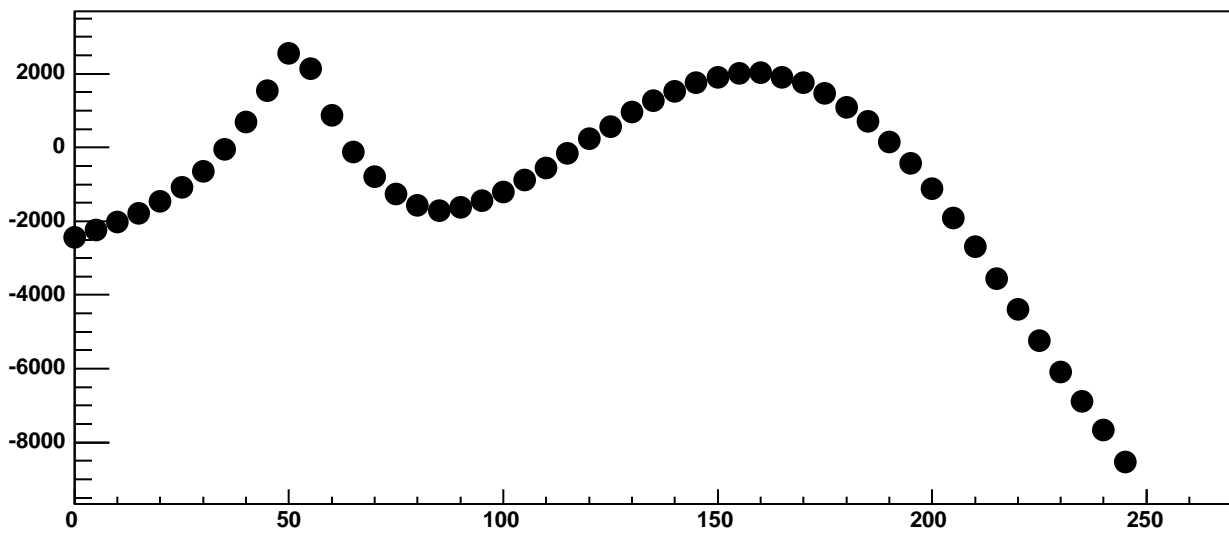


$\chi^2 / \text{ndf}$	2.305e+05 / 41
p0	-1513 ± 7.61
p1	52.23 ± 0.02952
p2	2.994e+04 ± 64.88
p3	53.45 ± 0.1165
p4	-53.15 ± 0.3271

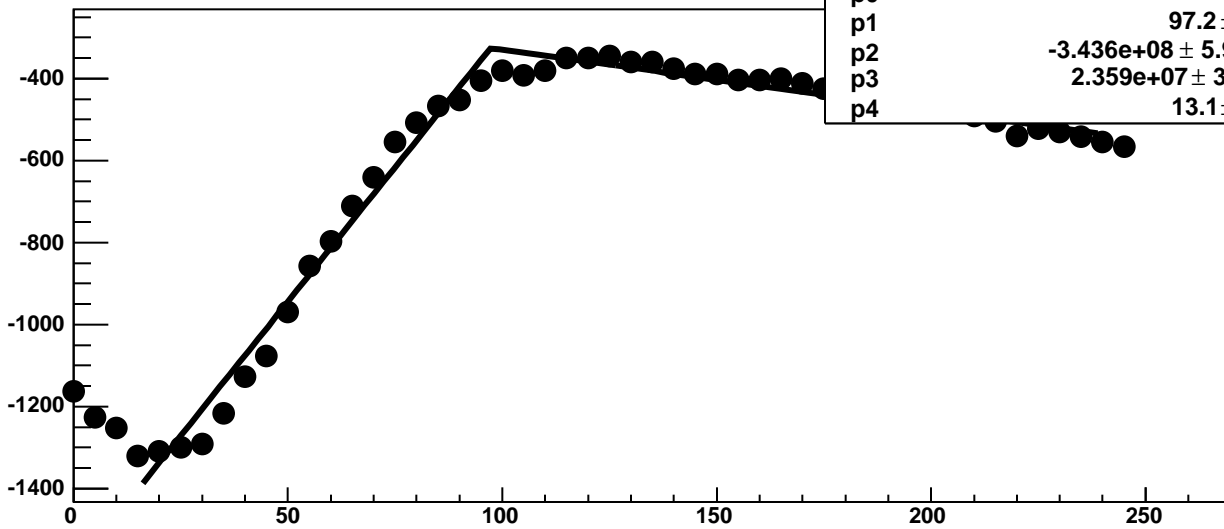
Chip 2, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

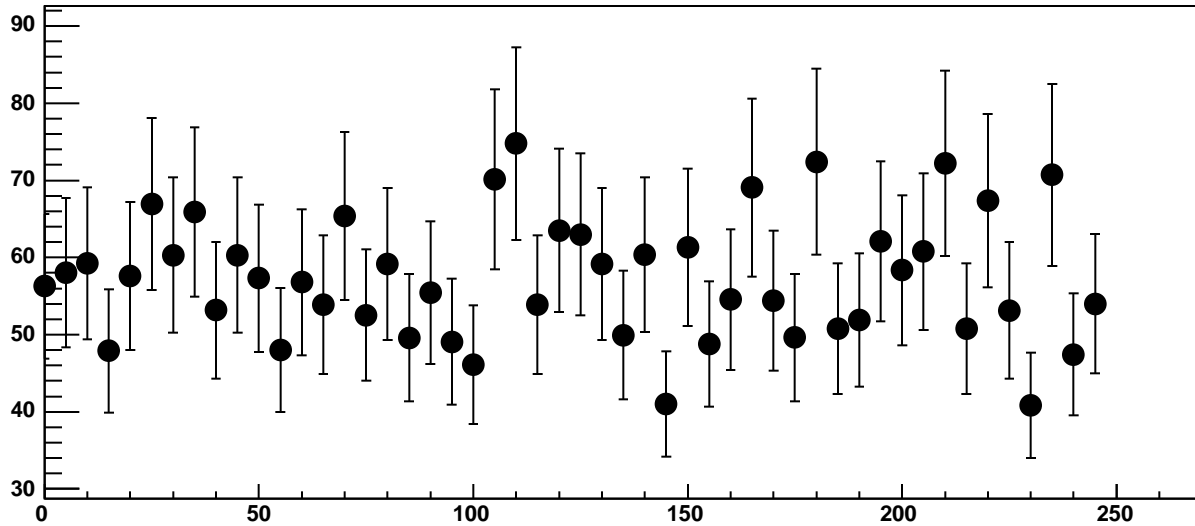


Chip 2, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

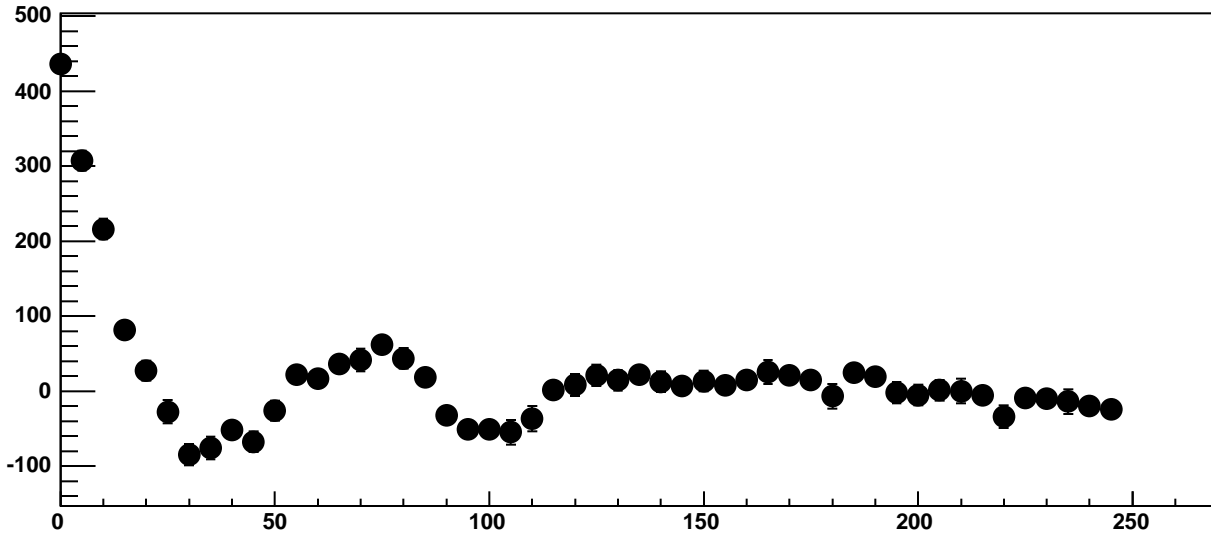


$\chi^2 / \text{ndf}$	336.4 / 41
p0	$-325.6 \pm 4.347$
p1	$97.2 \pm 0.5203$
p2	$-3.436\text{e}+08 \pm 5.929\text{e}+06$
p3	$2.359\text{e}+07 \pm 3.48\text{e}+05$
p4	$13.1 \pm 0.1227$

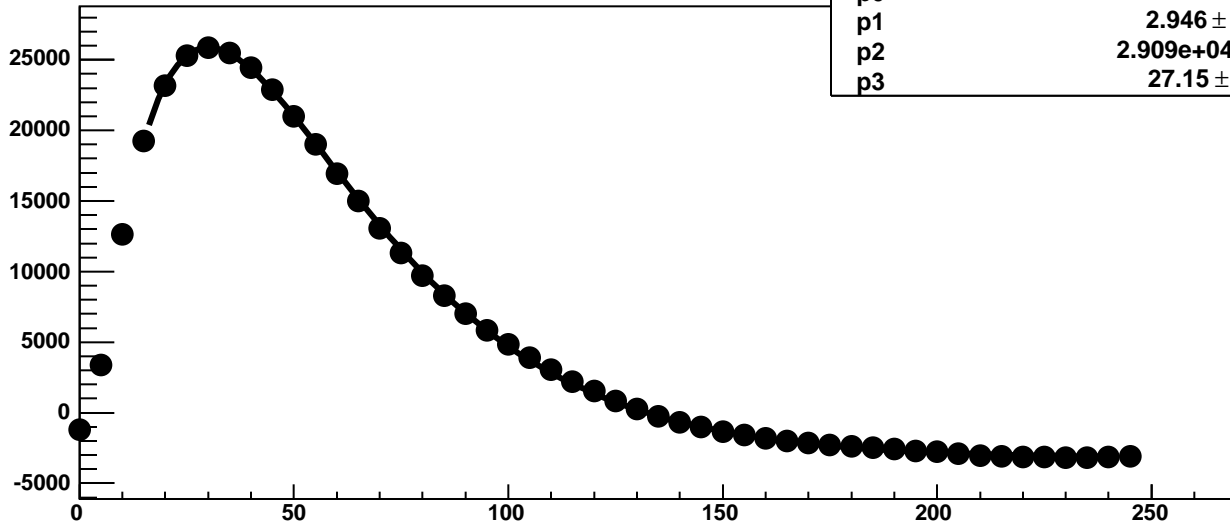
Chip 2, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

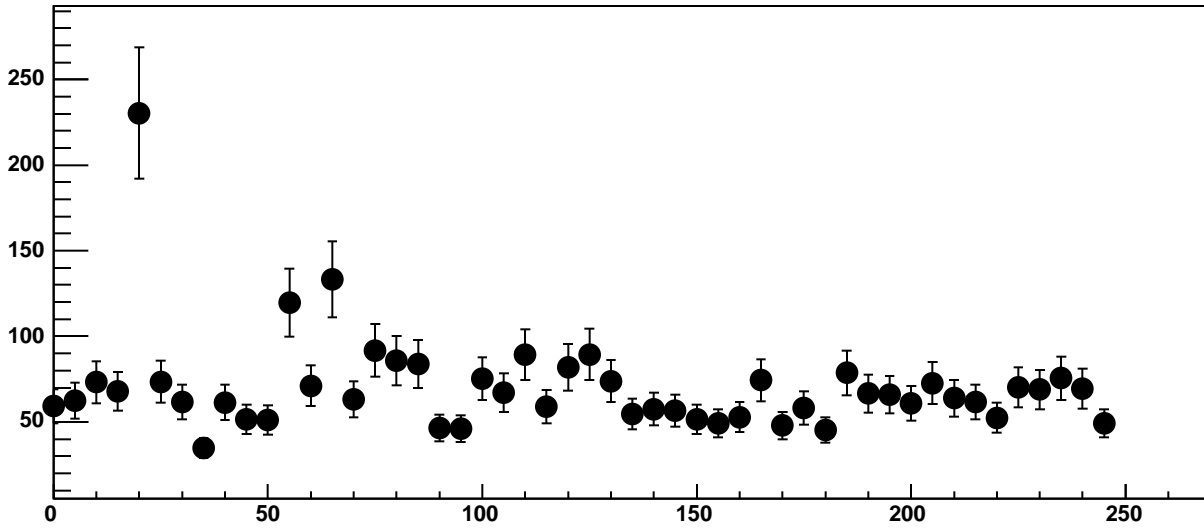


Chip 2, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold

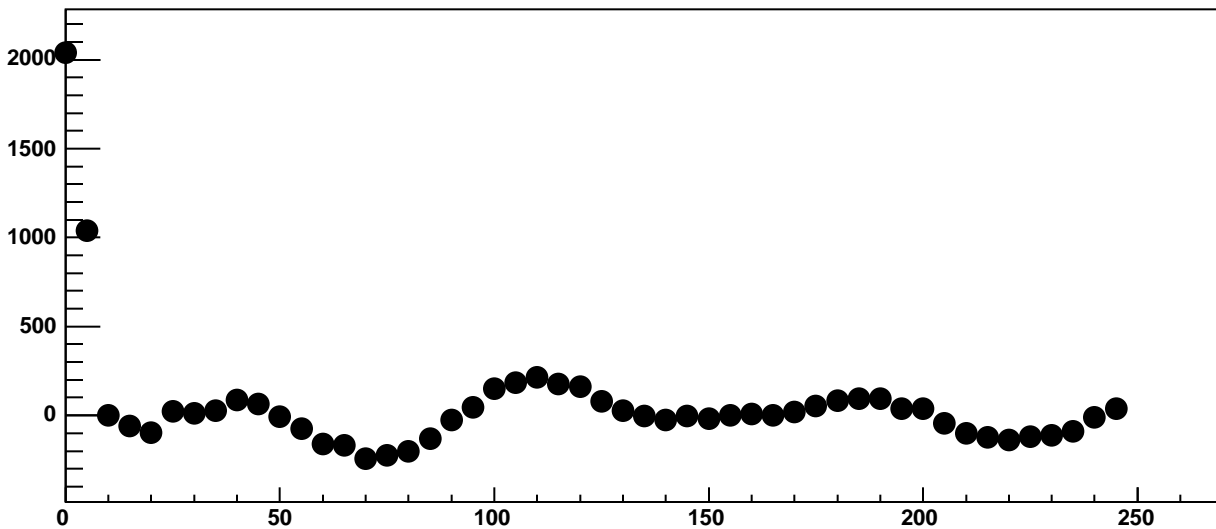


$\chi^2 / \text{ndf}$	1959 / 42
p0	$-3221 \pm 3.816$
p1	$2.946 \pm 0.01712$
p2	$2.909\text{e}+04 \pm 5.936$
p3	$27.15 \pm 0.01128$

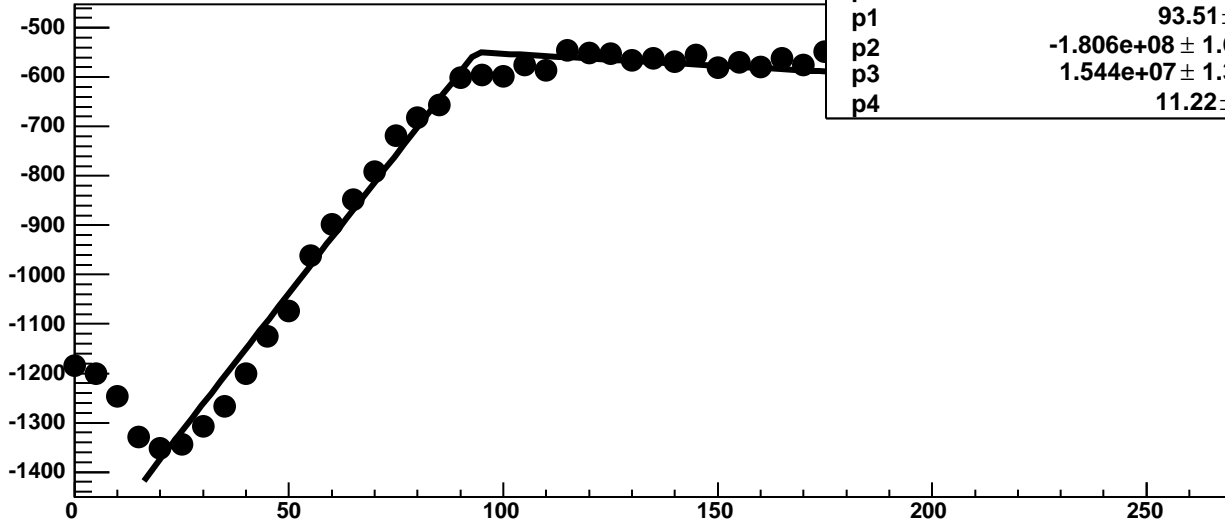
Chip 2, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

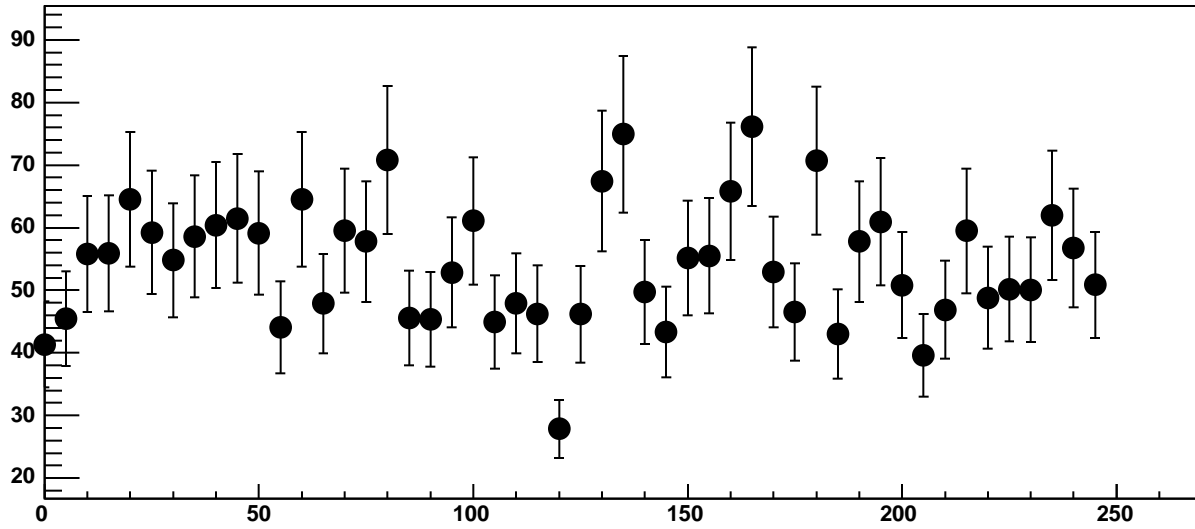


Chip 2, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

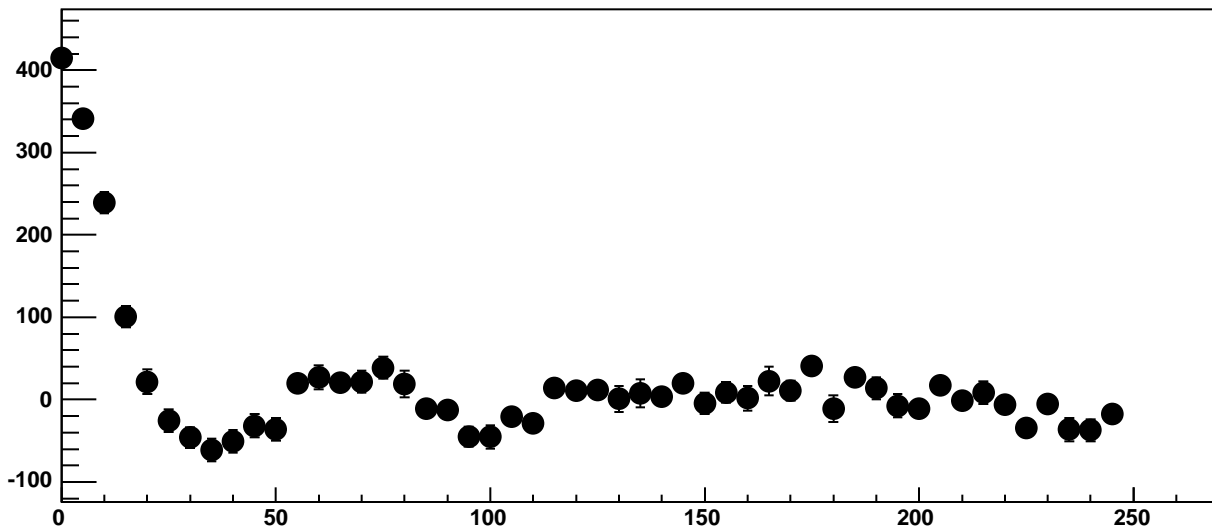


$\chi^2 / \text{ndf}$	253.5 / 41
p0	-549.4 ± 3.822
p1	93.51 ± 0.6227
p2	-1.806e+08 ± 1.647e+07
p3	1.544e+07 ± 1.395e+06
p4	11.22 ± 0.1355

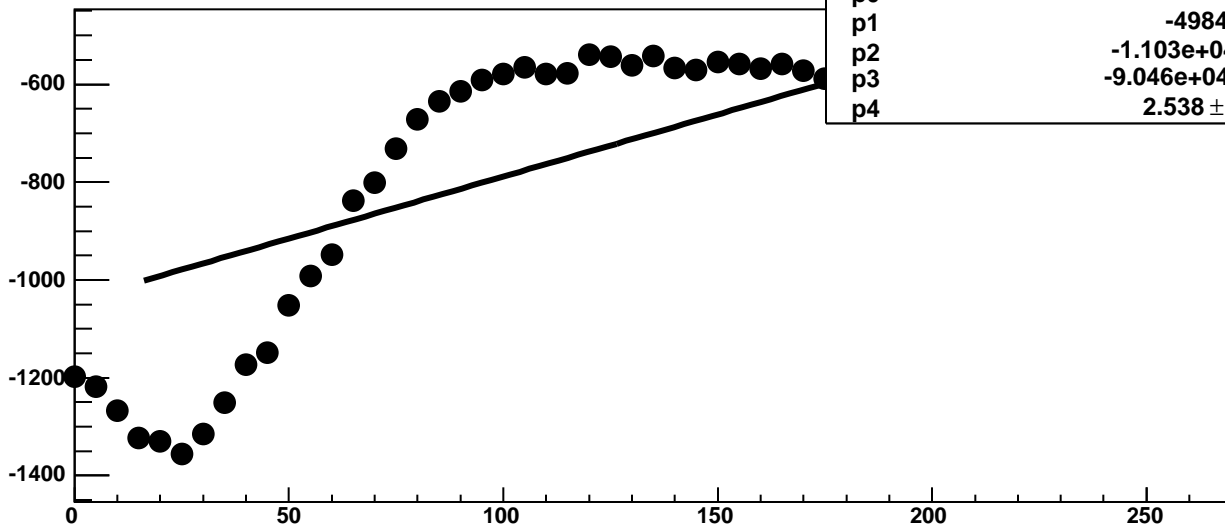
Chip 2, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

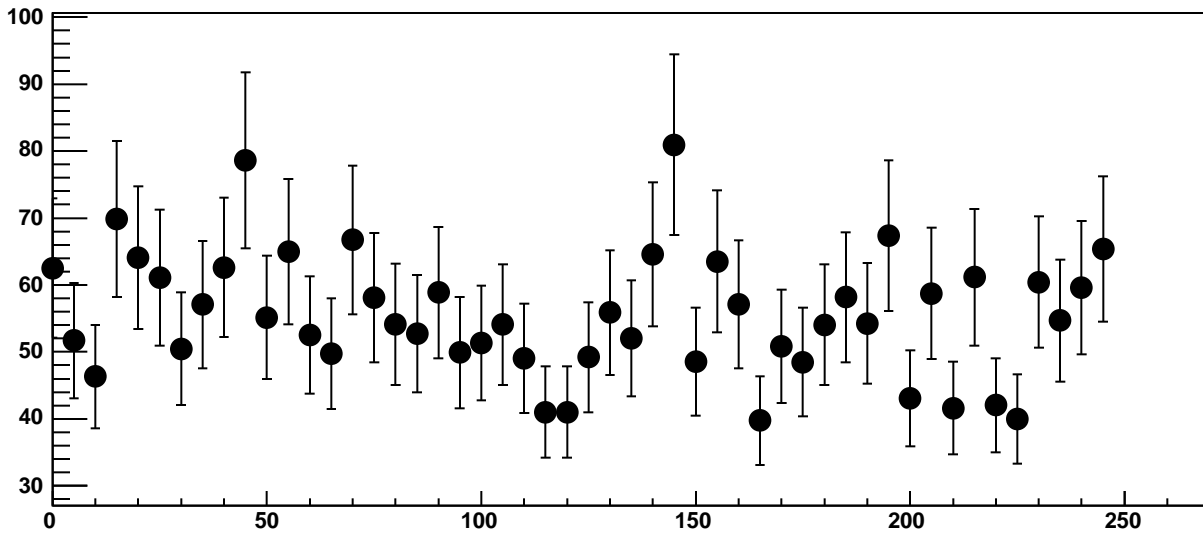


Chip 2, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

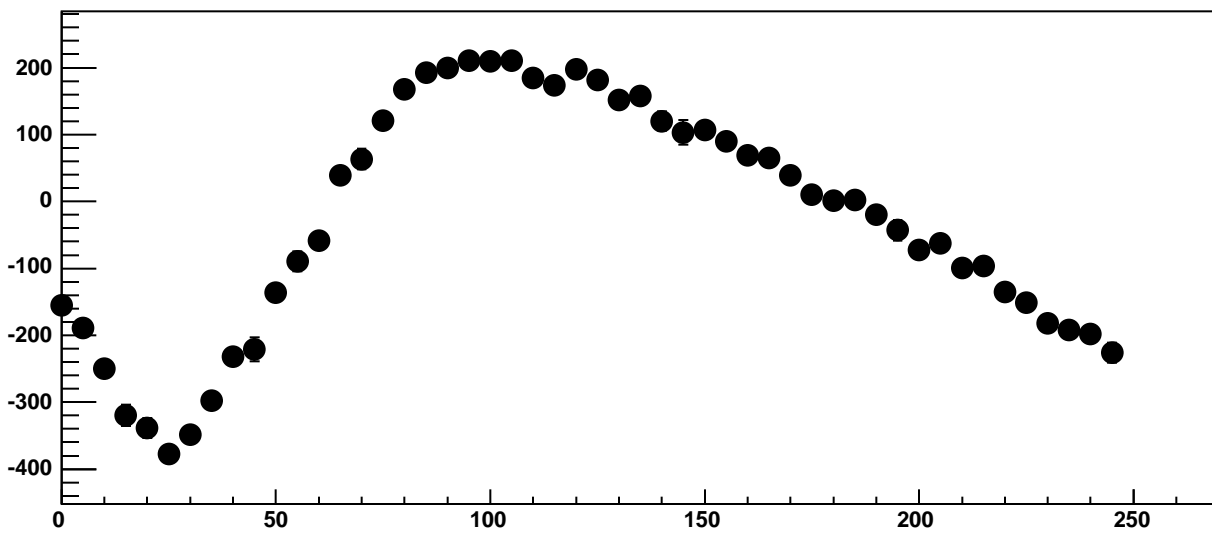


$\chi^2 / \text{ndf}$	8646 / 41
p0	$-2657 \pm 8.757$
p1	$-4984 \pm 3.253$
p2	$-1.103\text{e}+04 \pm 11.7$
p3	$-9.046\text{e}+04 \pm 576.4$
p4	$2.538 \pm 0.00171$

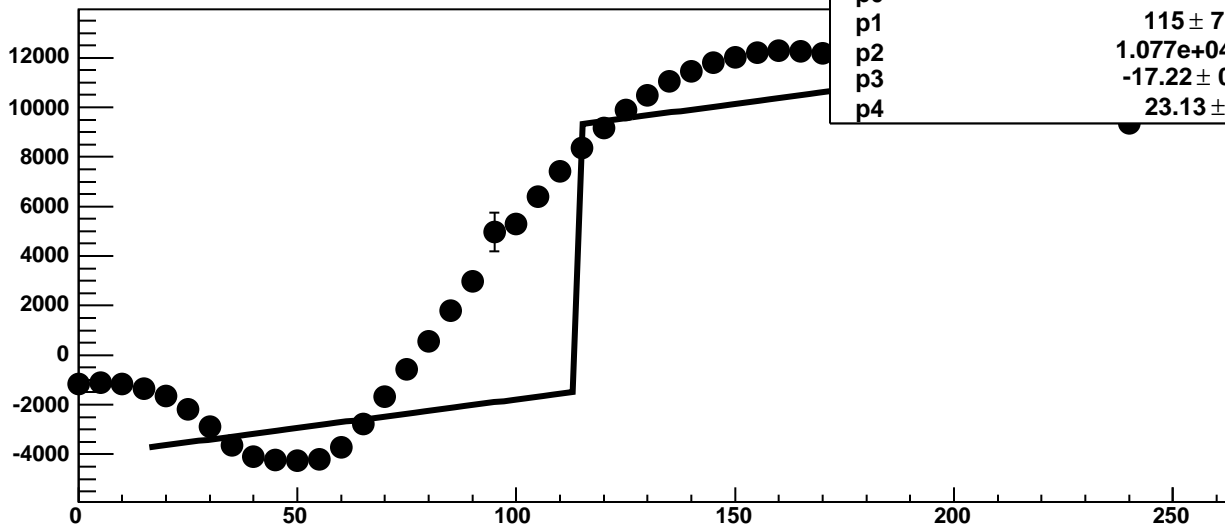
Chip 2, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

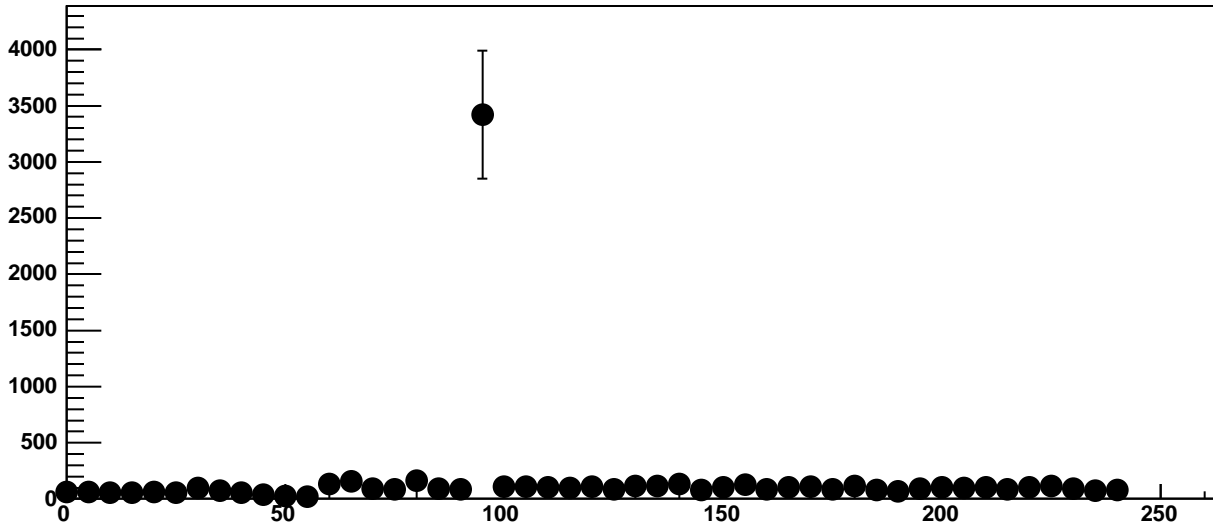


Chip 2, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

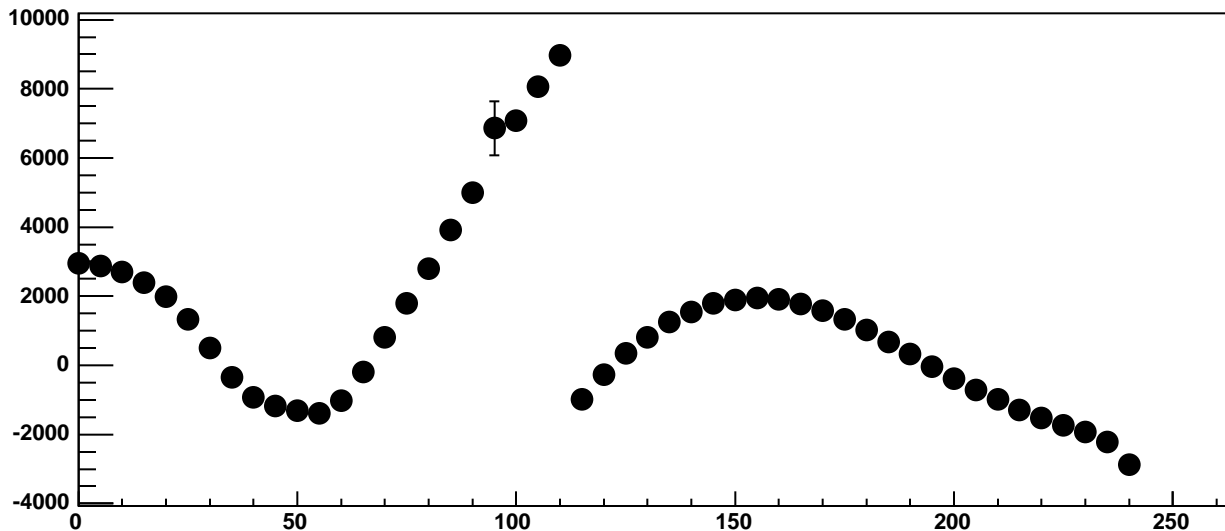


$\chi^2 / \text{ndf}$	7.707e+05 / 41
p0	-1437 ± 1.24
p1	115 ± 7.742e-06
p2	1.077e+04 ± 3.087
p3	-17.22 ± 0.002498
p4	23.13 ± 0.01708

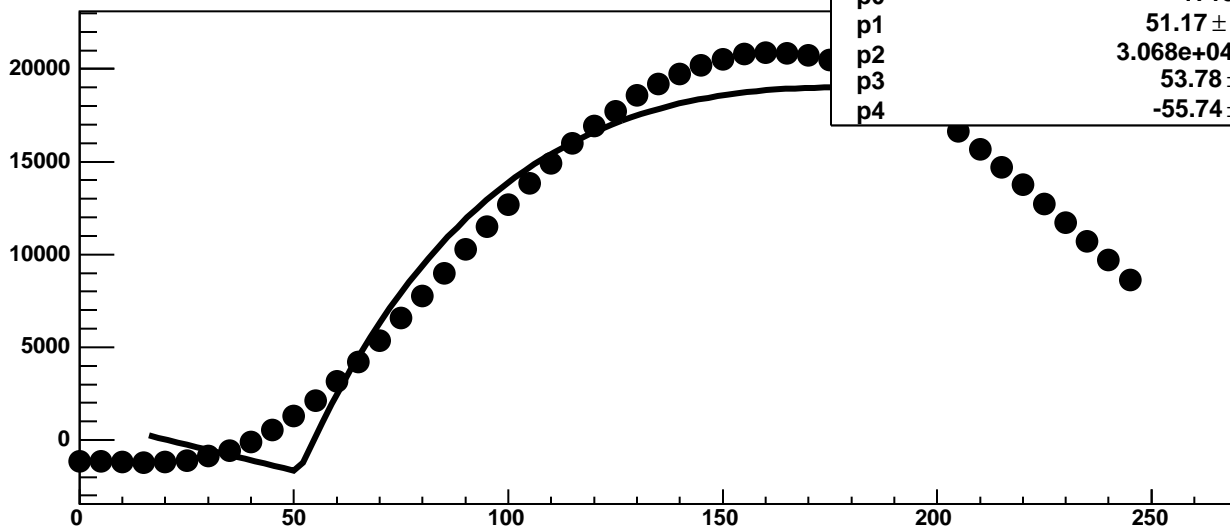
Chip 2, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold

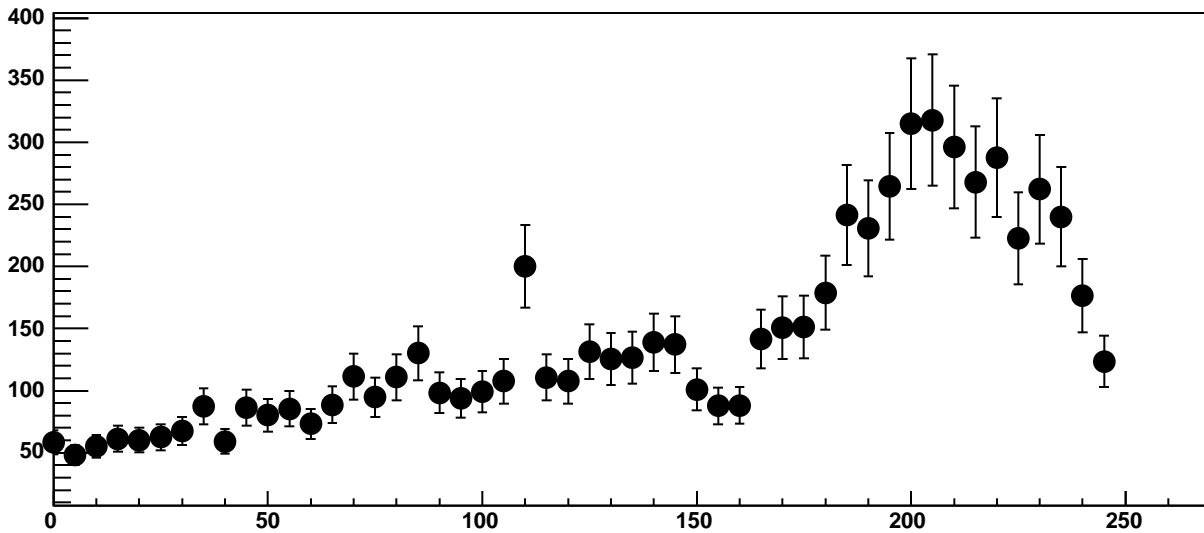


Chip 2, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

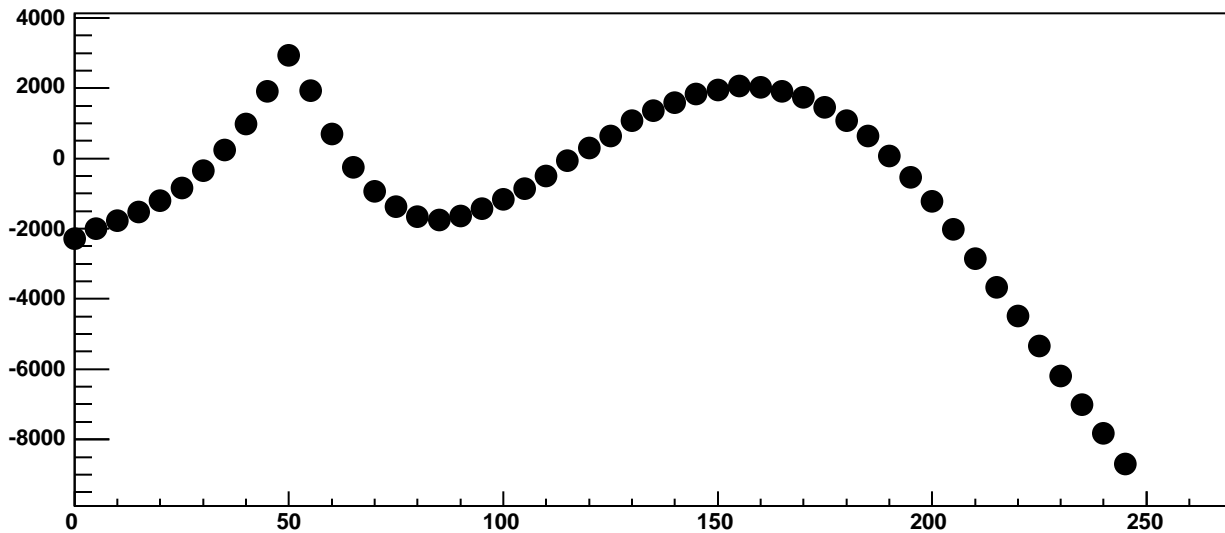


$\chi^2 / \text{ndf}$	2.341e+05 / 41
p0	-1713 ± 8.056
p1	51.17 ± 0.02956
p2	3.068e+04 ± 66.18
p3	53.78 ± 0.1164
p4	-55.74 ± 0.3283

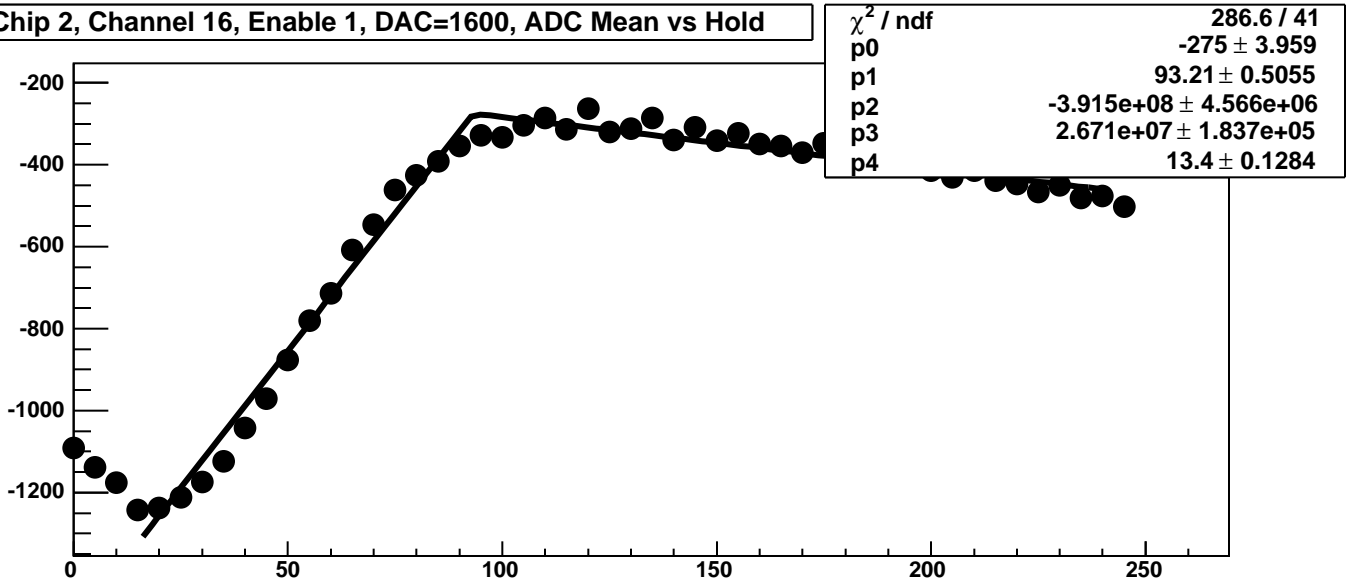
Chip 2, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



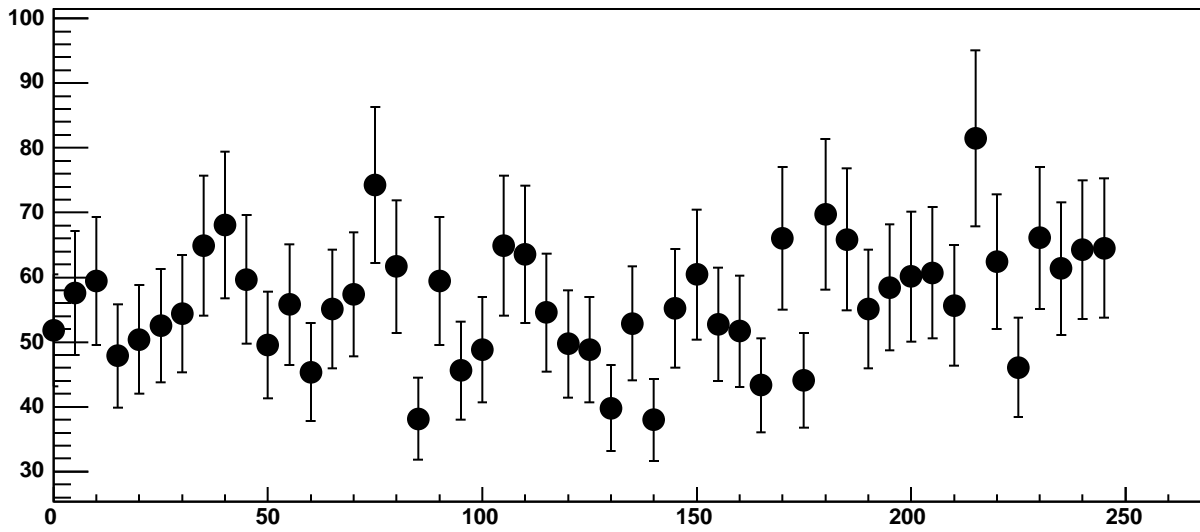
Chip 2, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold



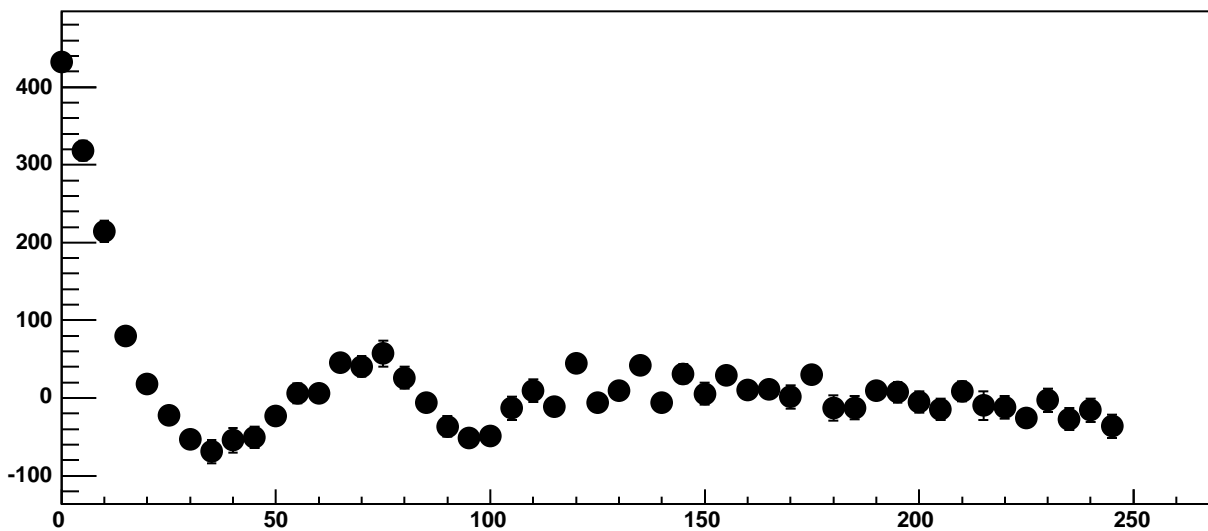
Chip 2, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 2, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

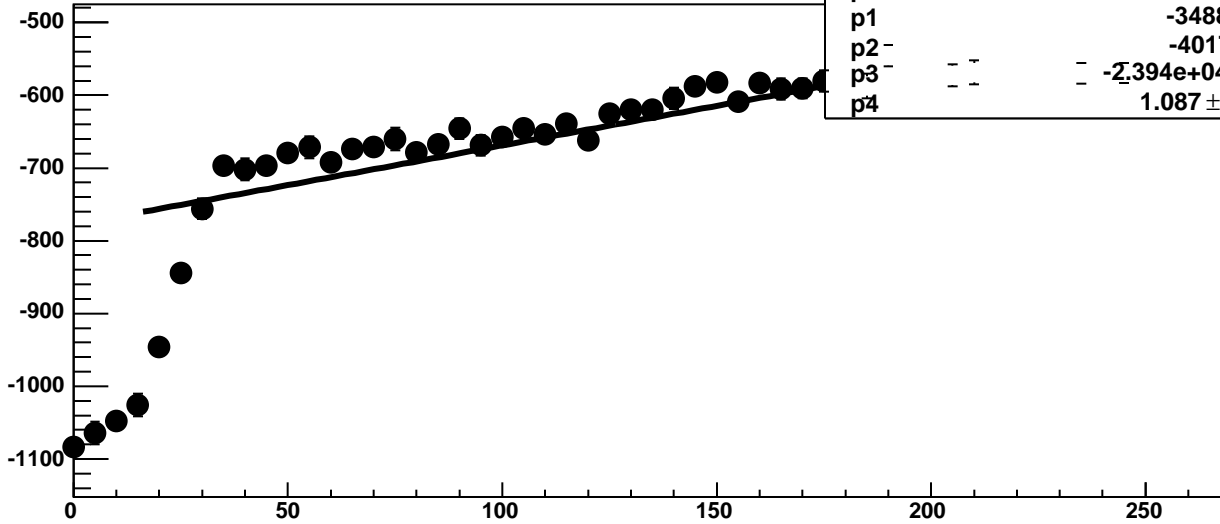


Chip 2, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



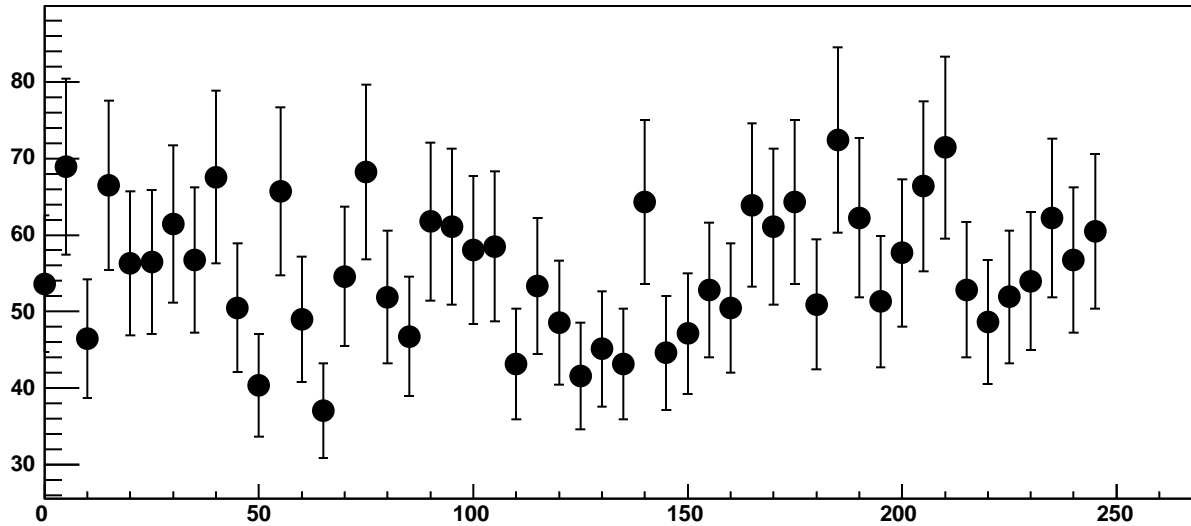


Chip 2, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold

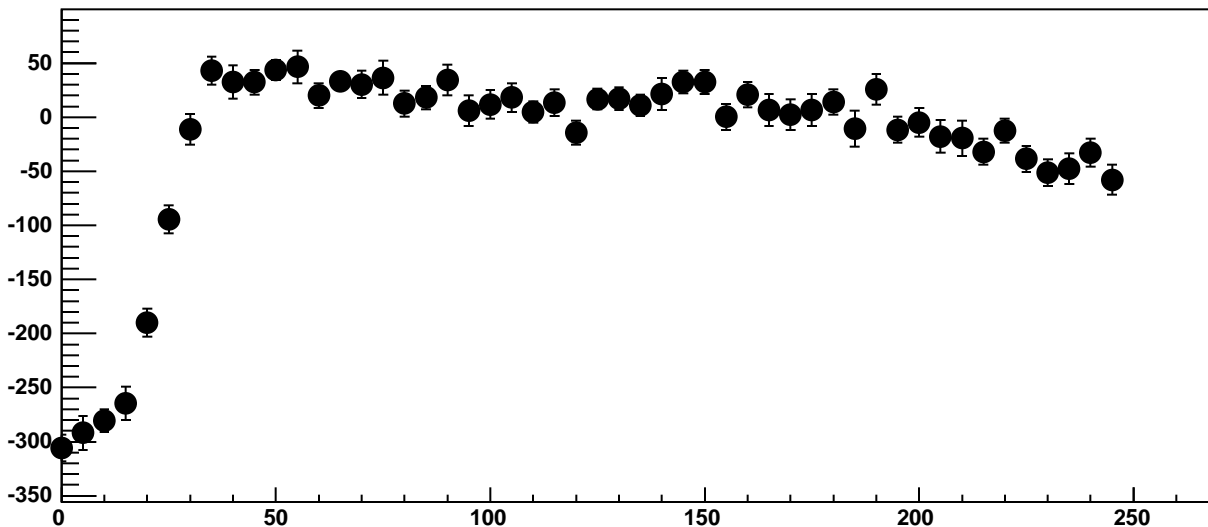


$\chi^2 / \text{ndf}$	765 / 41
p0	$-552 \pm 19.11$
p1	$-3488 \pm 2.953$
p2	$-4017 \pm 86.01$
p3	$-2.394e+04 \pm 523.9$
p4	$1.087 \pm 0.02842$

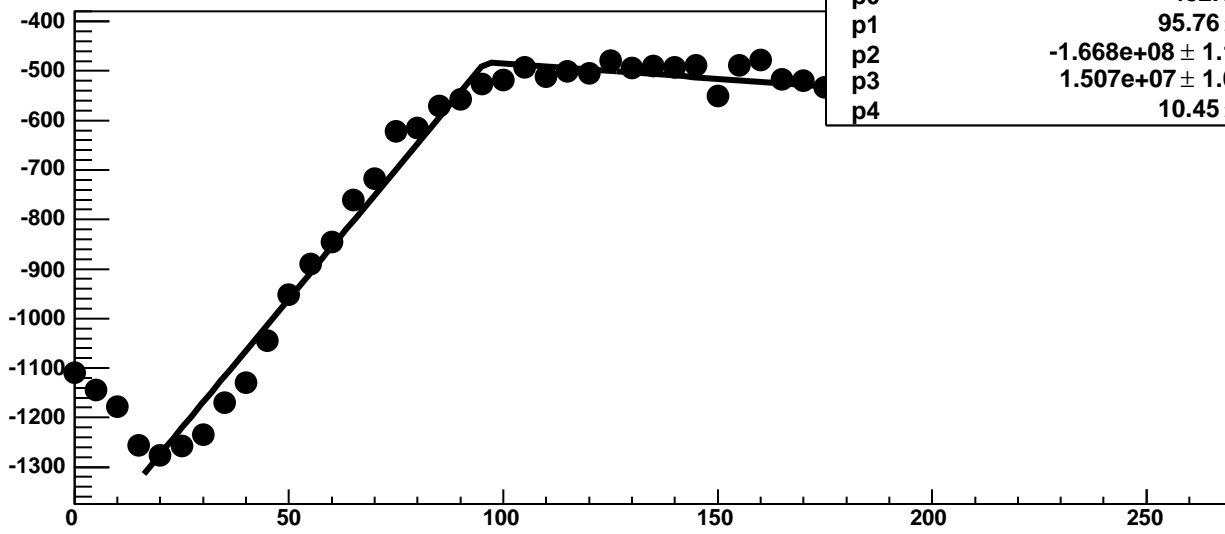
Chip 2, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

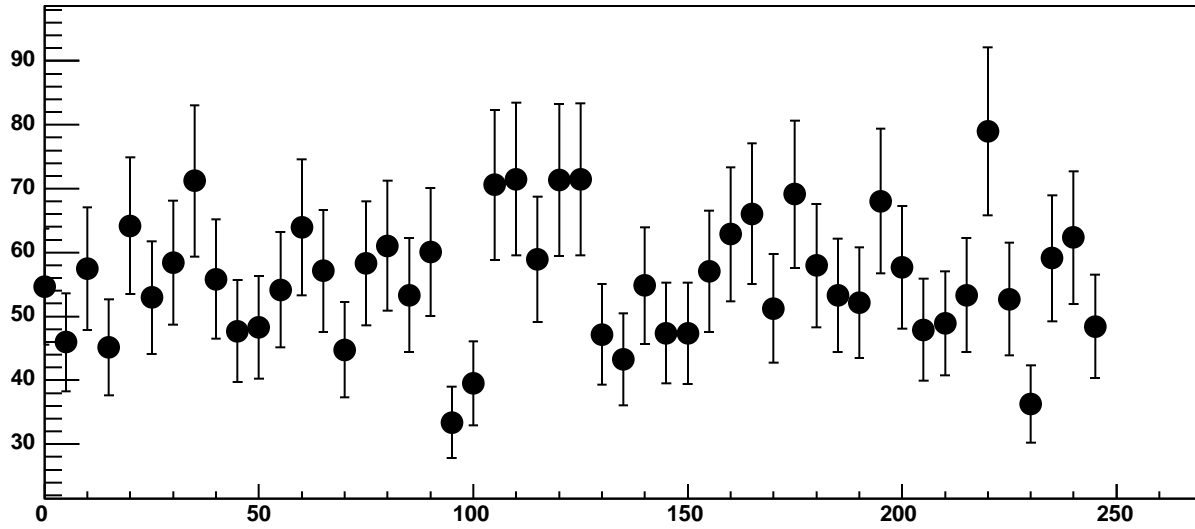


Chip 2, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

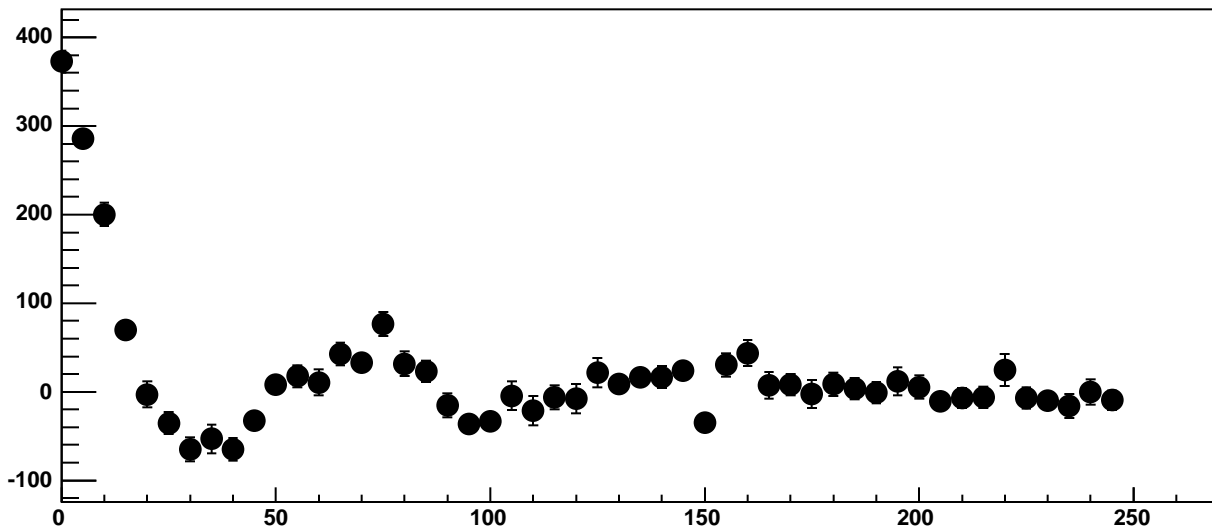


$\chi^2 / \text{ndf}$	272.4 / 41
p0	-482.1 ± 4.432
p1	95.76 ± 0.6261
p2	-1.668e+08 ± 1.185e+07
p3	1.507e+07 ± 1.059e+06
p4	10.45 ± 0.1113

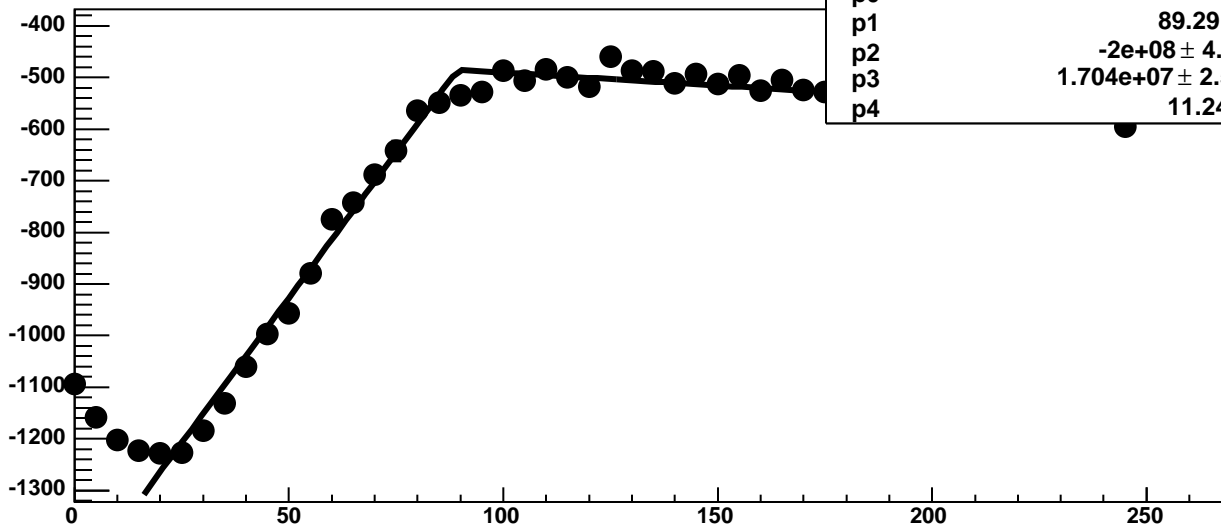
Chip 2, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

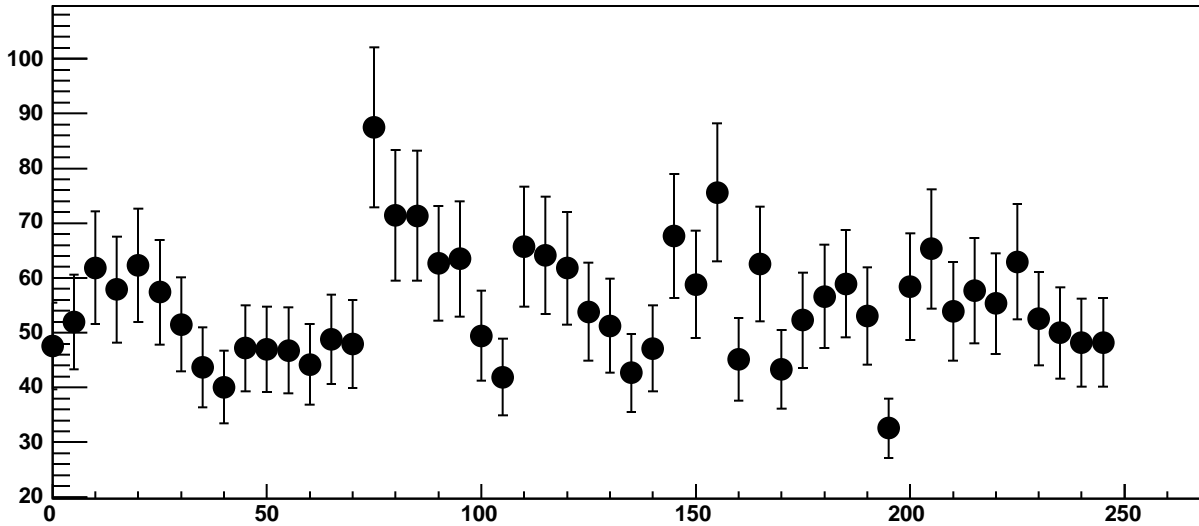


Chip 2, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

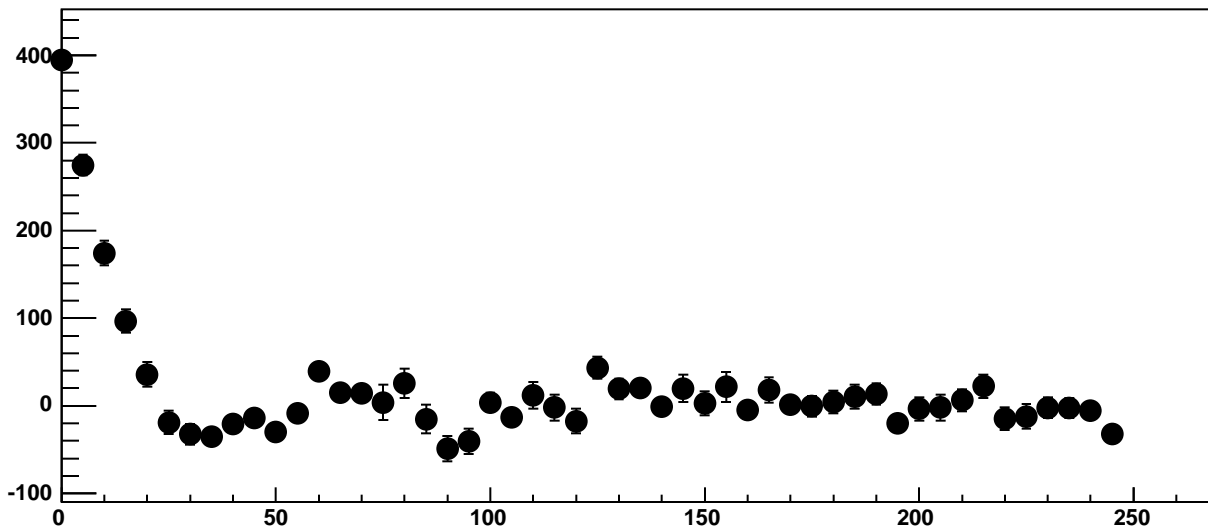


$\chi^2 / \text{ndf}$	180.7 / 41
p0	$-485.2 \pm 4.239$
p1	$89.29 \pm 0.7371$
p2	$-2e+08 \pm 4.395e+06$
p3	$1.704e+07 \pm 2.539e+05$
p4	$11.24 \pm 0.165$

Chip 2, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold

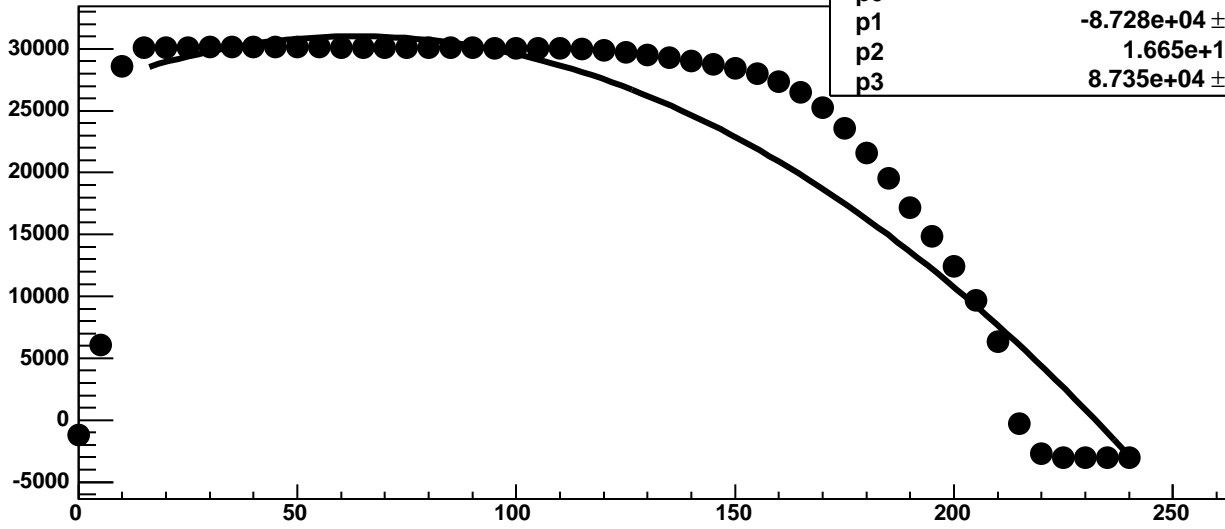


Chip 2, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

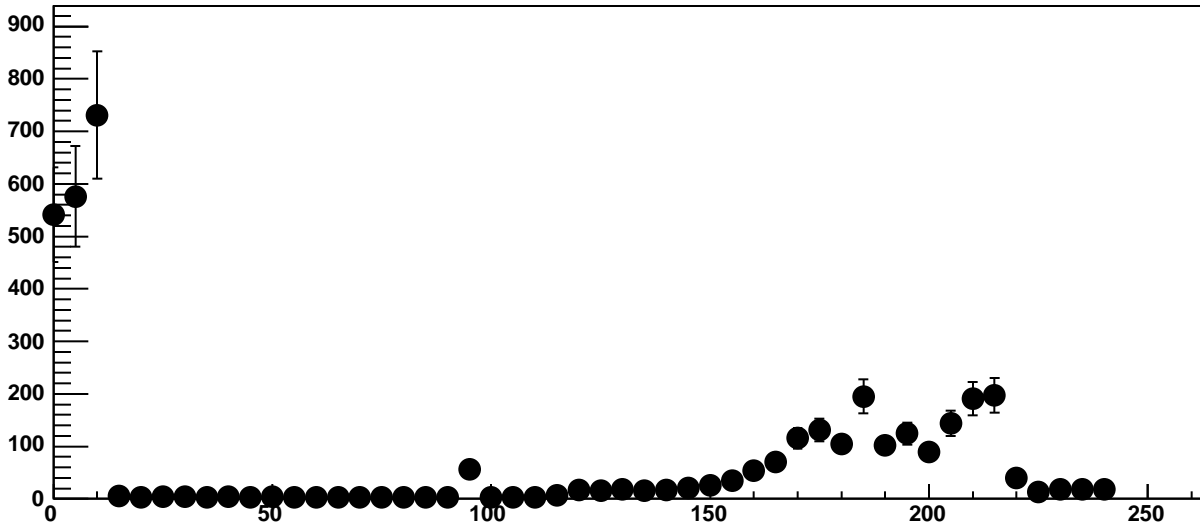


Chip 2, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

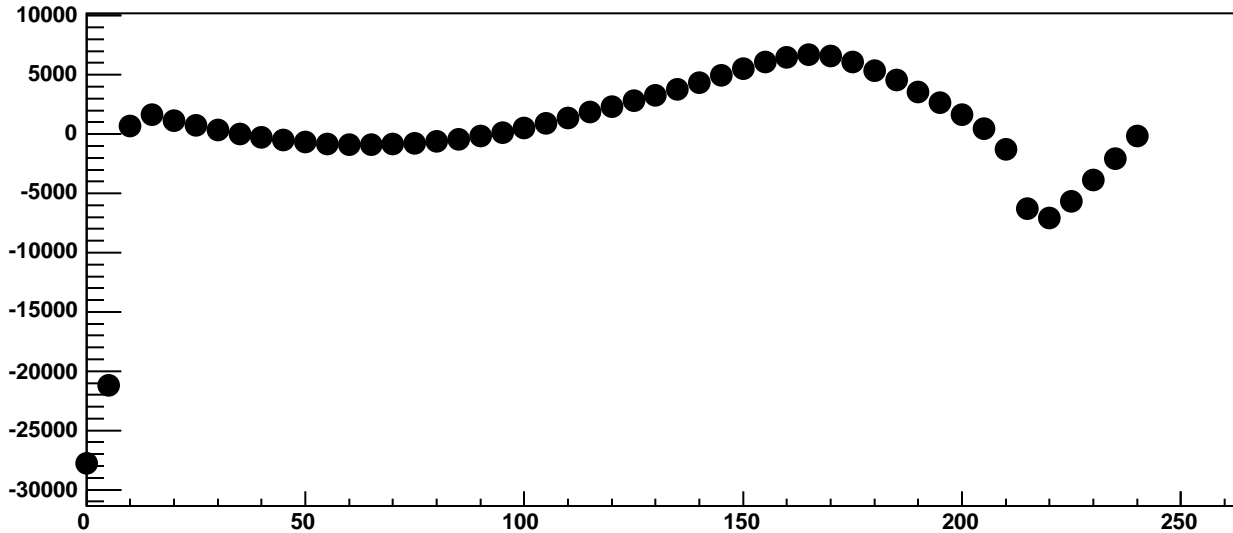
$\chi^2 / \text{ndf}$	3.167e+07 / 42
p0	-1.665e+10 $\pm$ 2.711
p1	-8.728e+04 $\pm$ 0.03279
p2	1.665e+10 $\pm$ 2.711
p3	8.735e+04 $\pm$ 0.03277



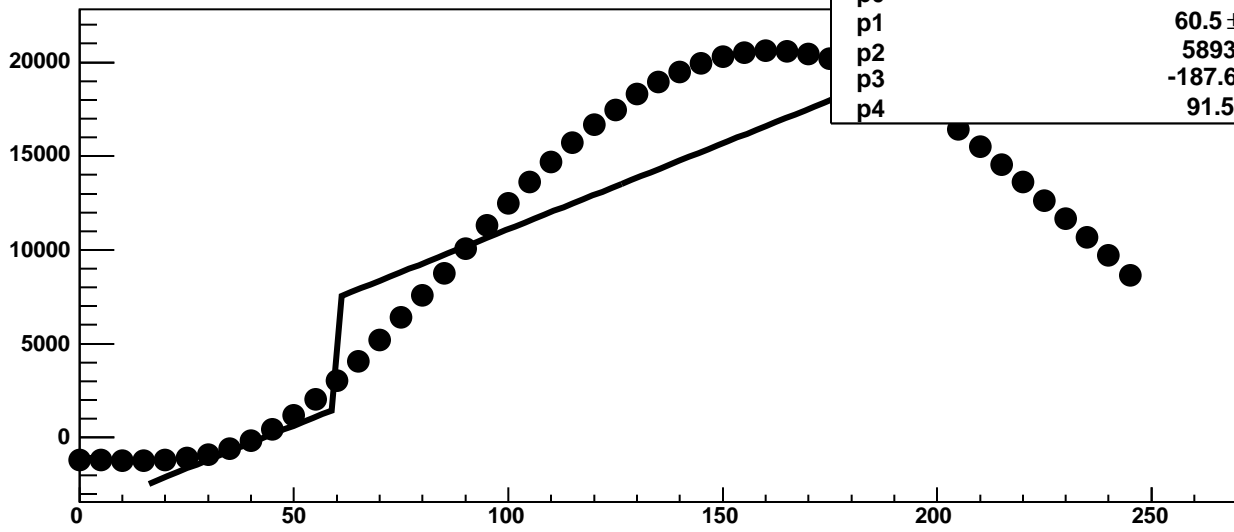
Chip 2, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

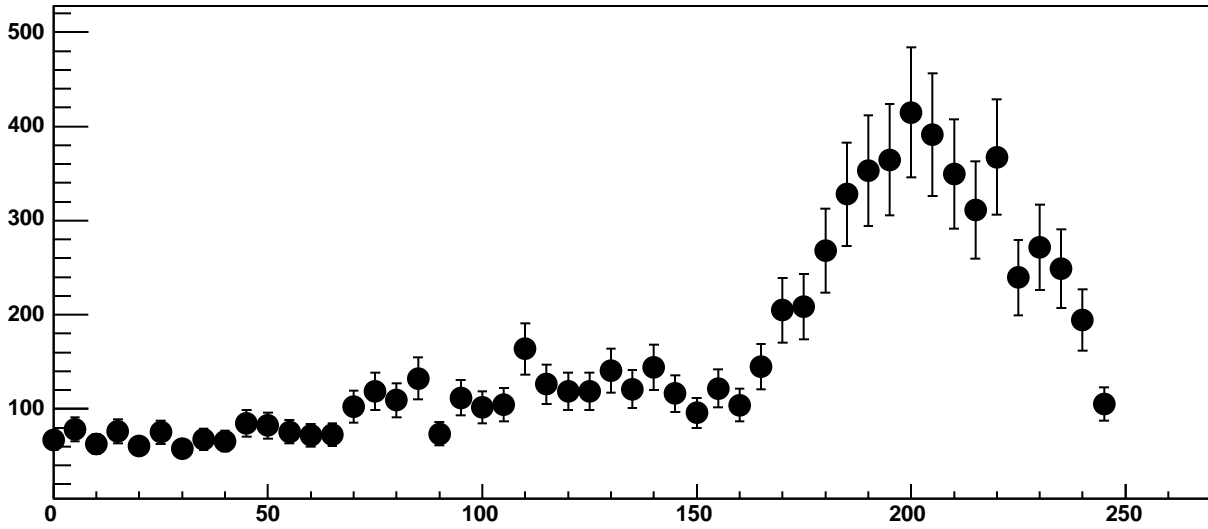


Chip 2, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

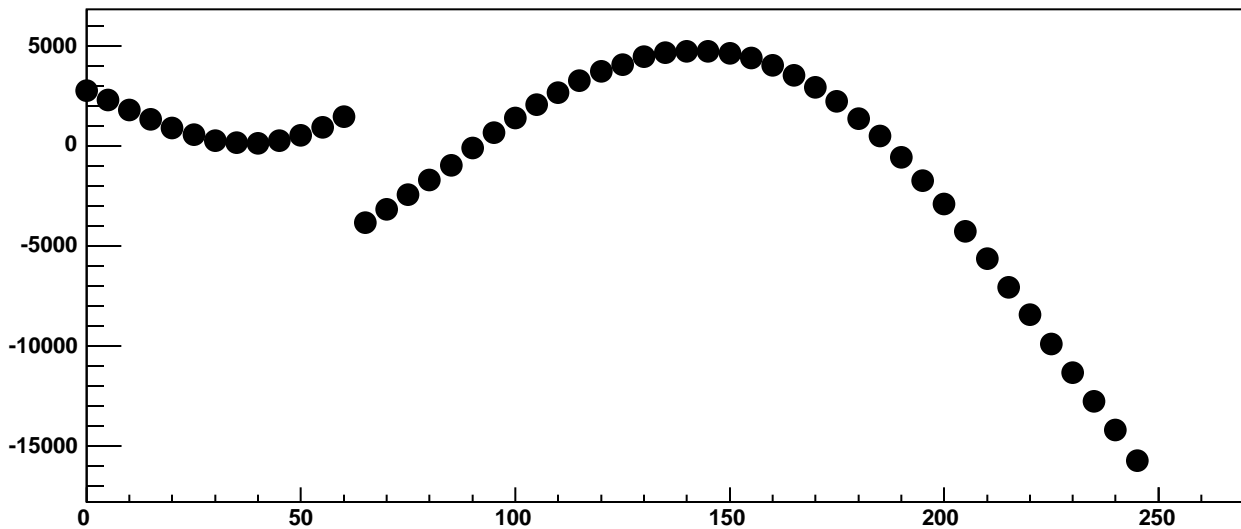


$\chi^2 / \text{ndf}$	6.383e+05 / 41
p0	1598 ± 10.26
p1	60.5 ± 0.3033
p2	5893 ± 38.31
p3	-187.6 ± 6.161
p4	91.5 ± 0.498

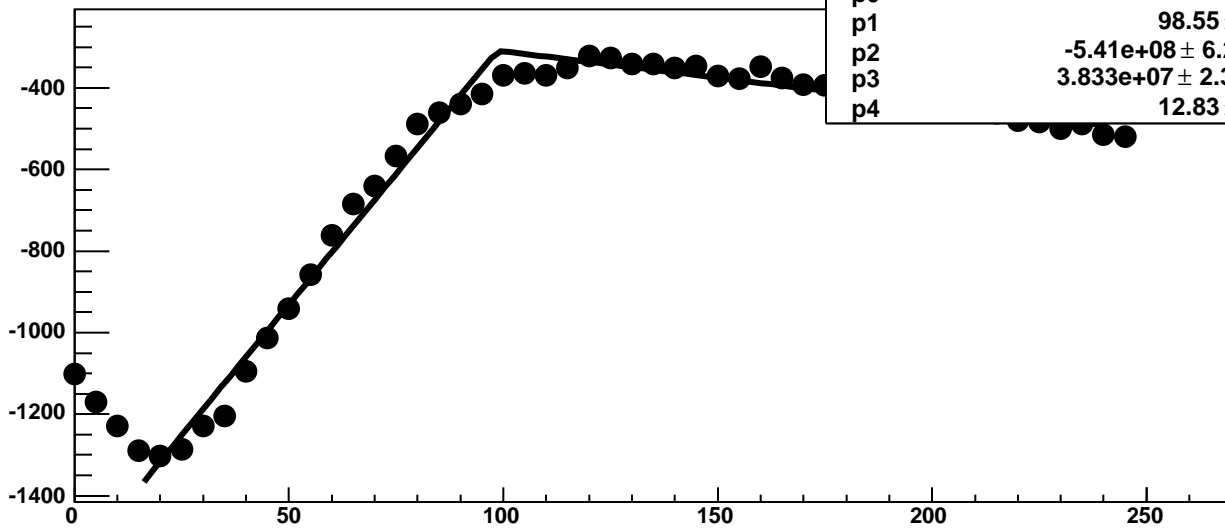
Chip 2, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

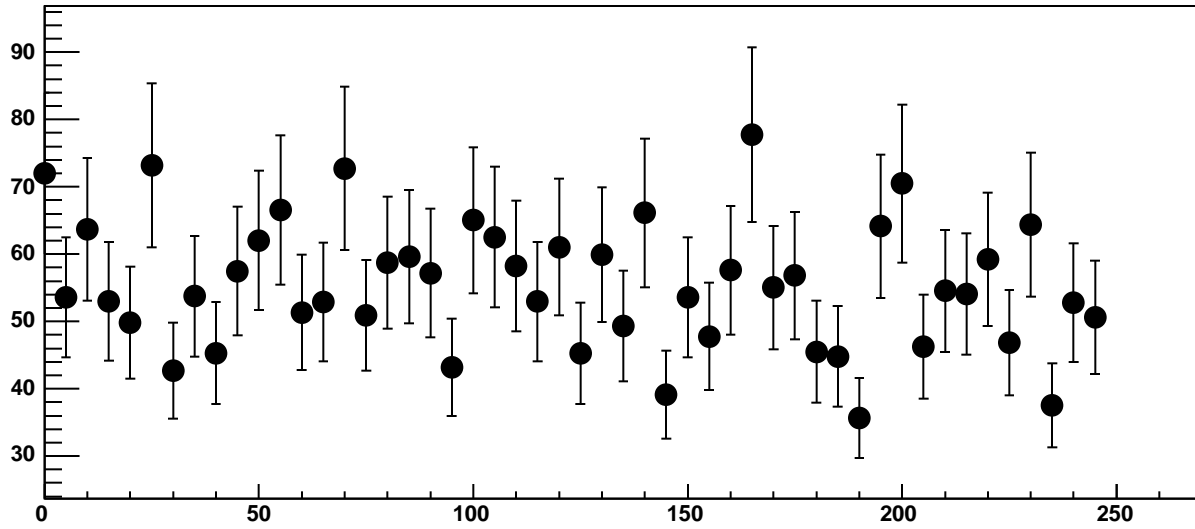


Chip 2, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

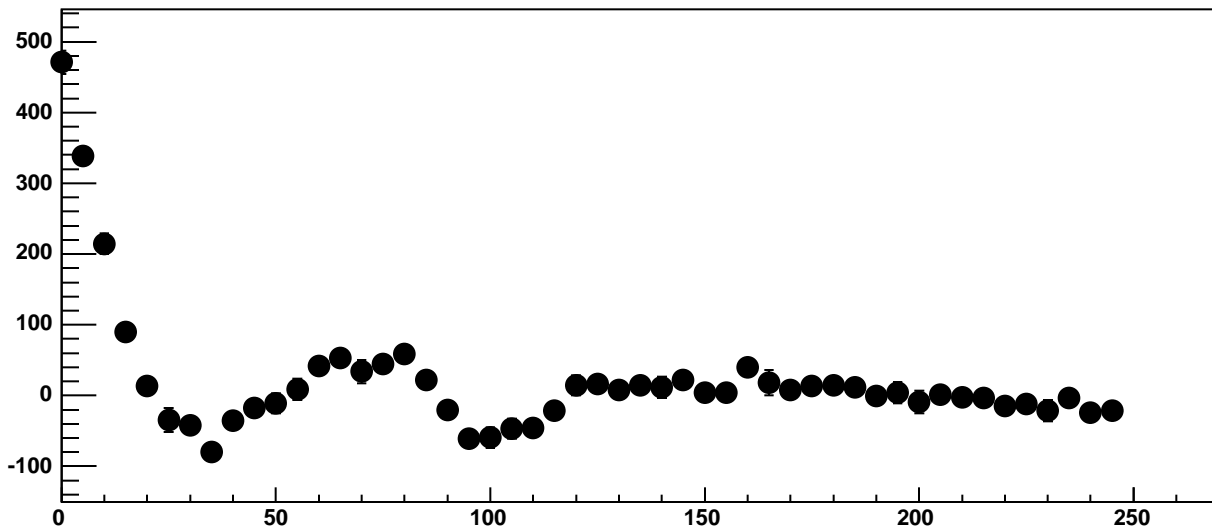


$\chi^2 / \text{ndf}$	326.4 / 41
p0	$-308.6 \pm 4.252$
p1	$98.55 \pm 0.5361$
p2	$-5.41\text{e}+08 \pm 6.253\text{e}+06$
p3	$3.833\text{e}+07 \pm 2.331\text{e}+05$
p4	$12.83 \pm 0.1181$

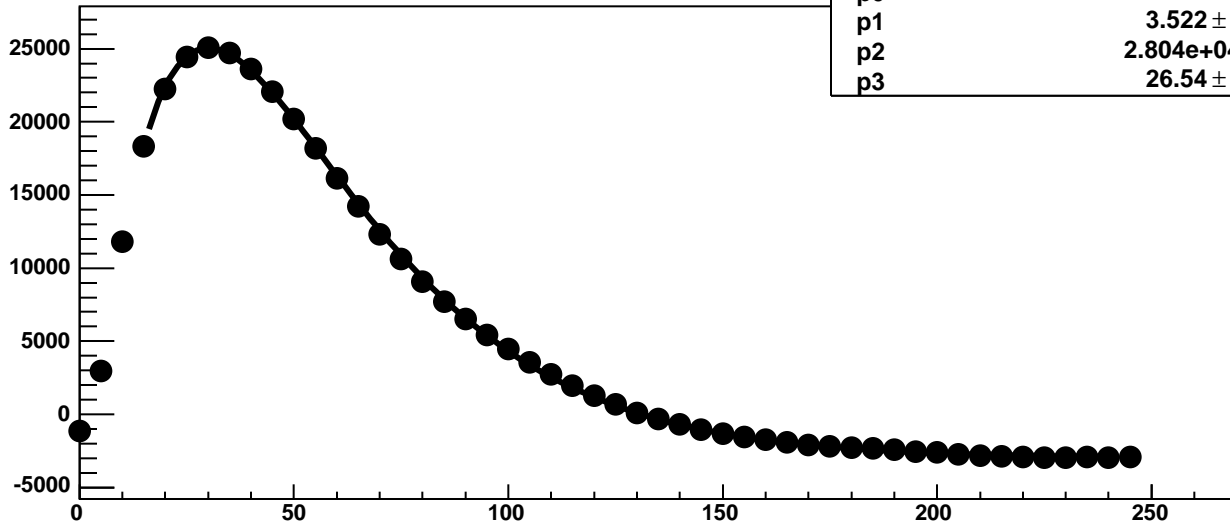
Chip 2, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

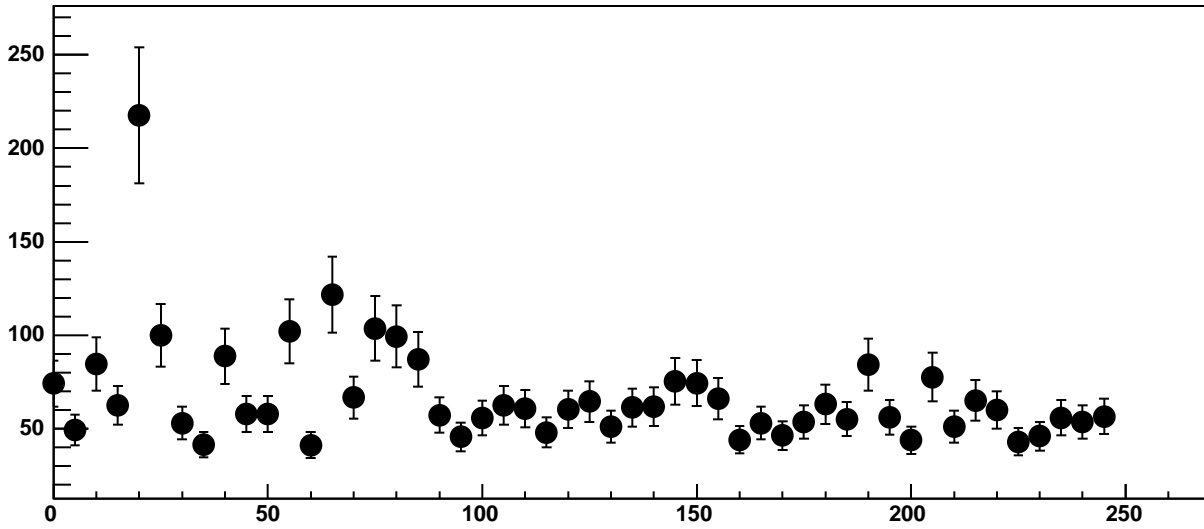


Chip 2, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

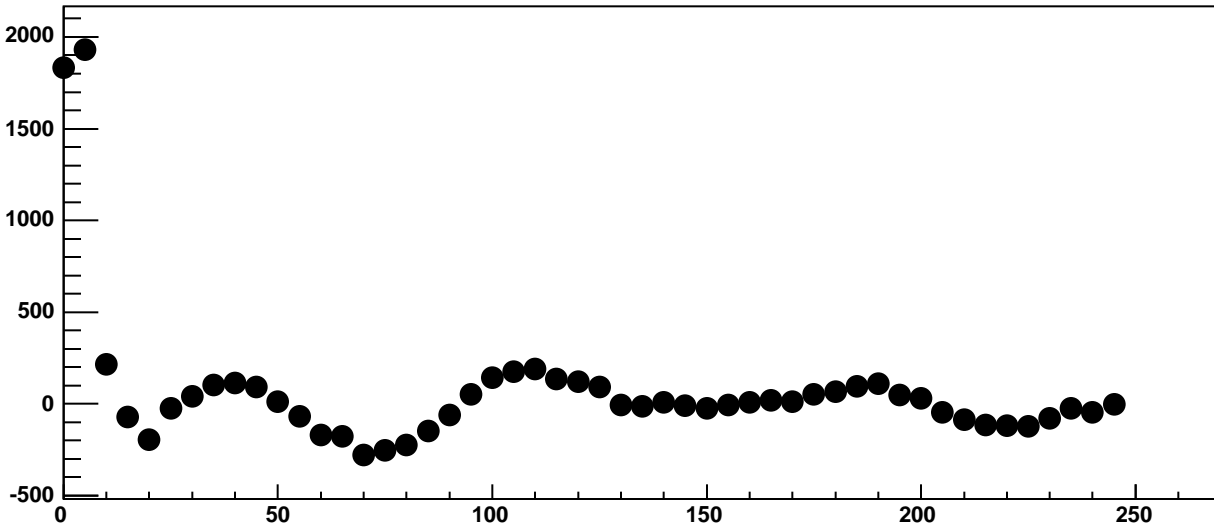


$\chi^2 / \text{ndf}$	2565 / 42
p0	$-2987 \pm 3.286$
p1	$3.522 \pm 0.01594$
p2	$2.804\text{e}+04 \pm 6.12$
p3	$26.54 \pm 0.01074$

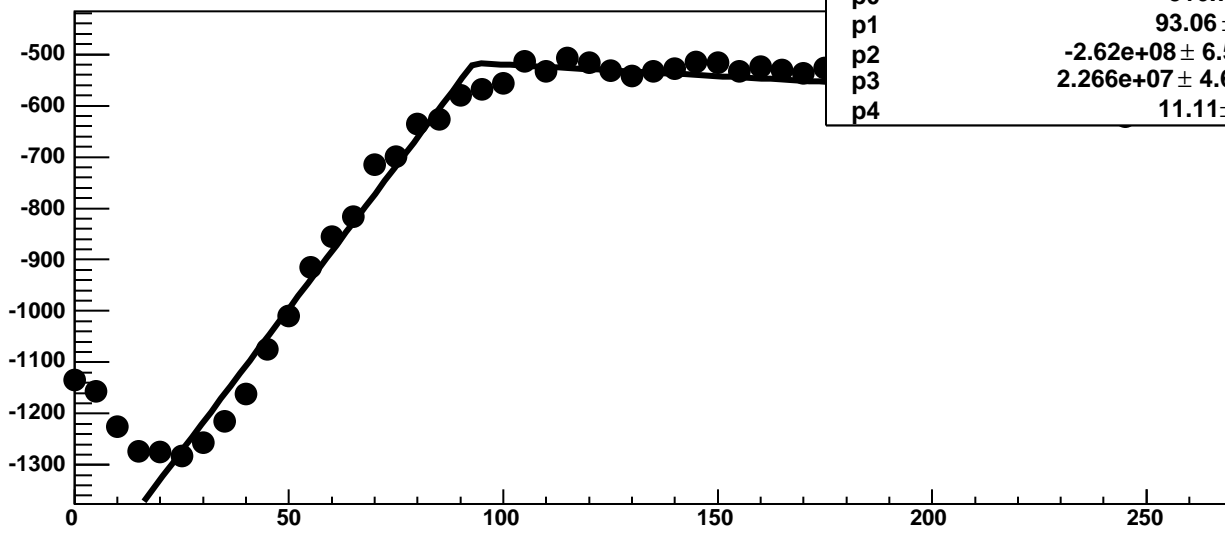
Chip 2, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

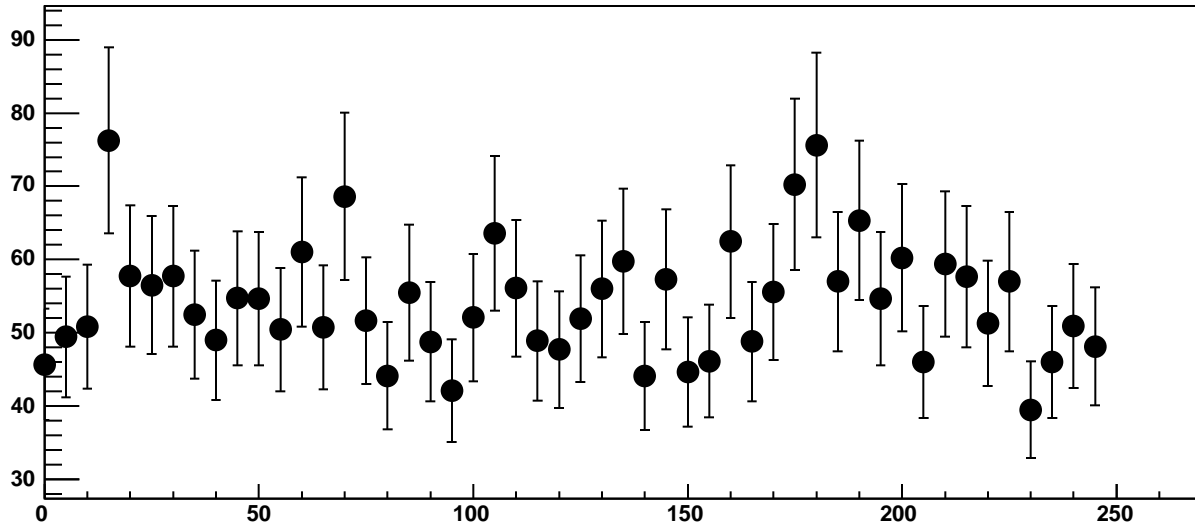


Chip 2, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

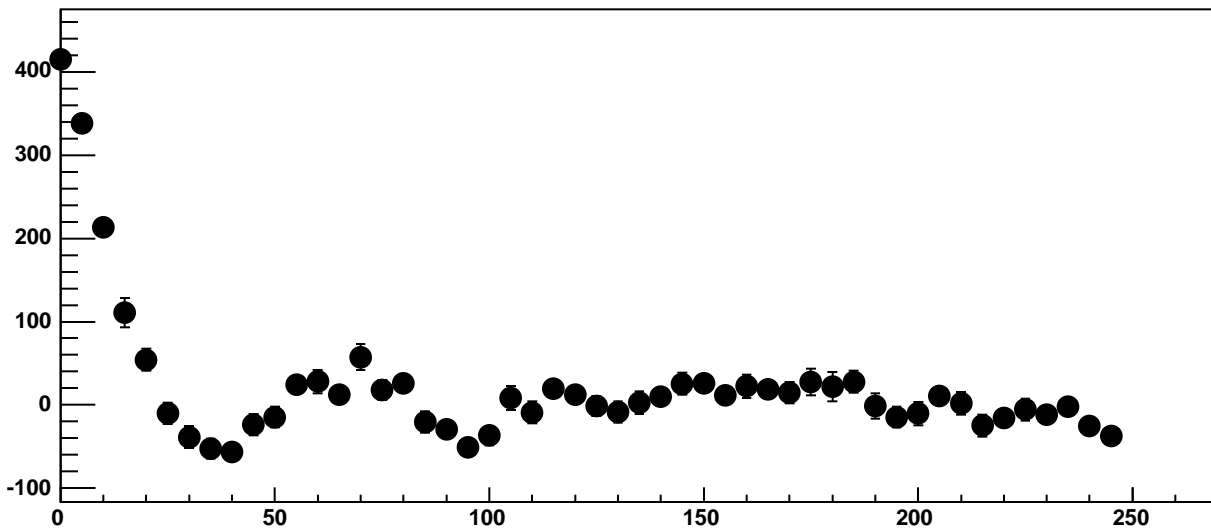


$\chi^2 / \text{ndf}$	242 / 41
p0	$-516.7 \pm 4.086$
p1	$93.06 \pm 0.6407$
p2	$-2.62\text{e}+08 \pm 6.583\text{e}+06$
p3	$2.266\text{e}+07 \pm 4.603\text{e}+05$
p4	$11.11 \pm 0.1384$

Chip 2, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold

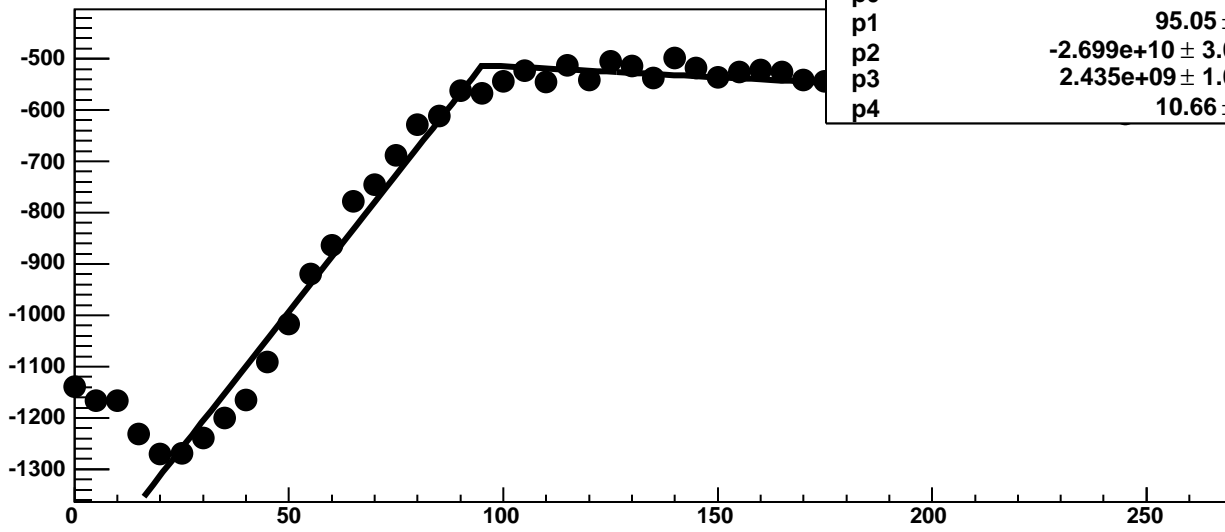


Chip 2, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



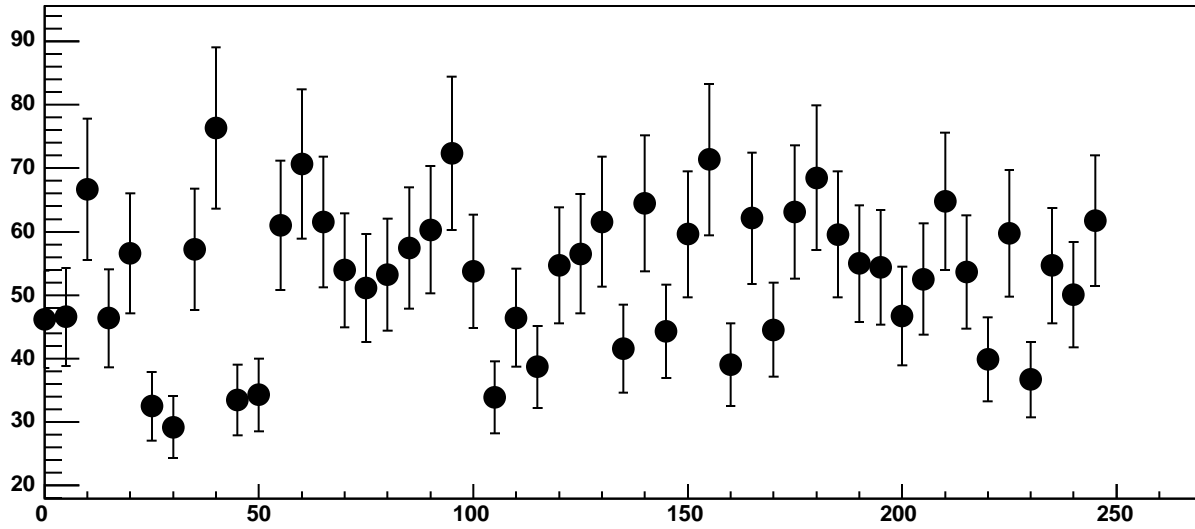


Chip 2, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

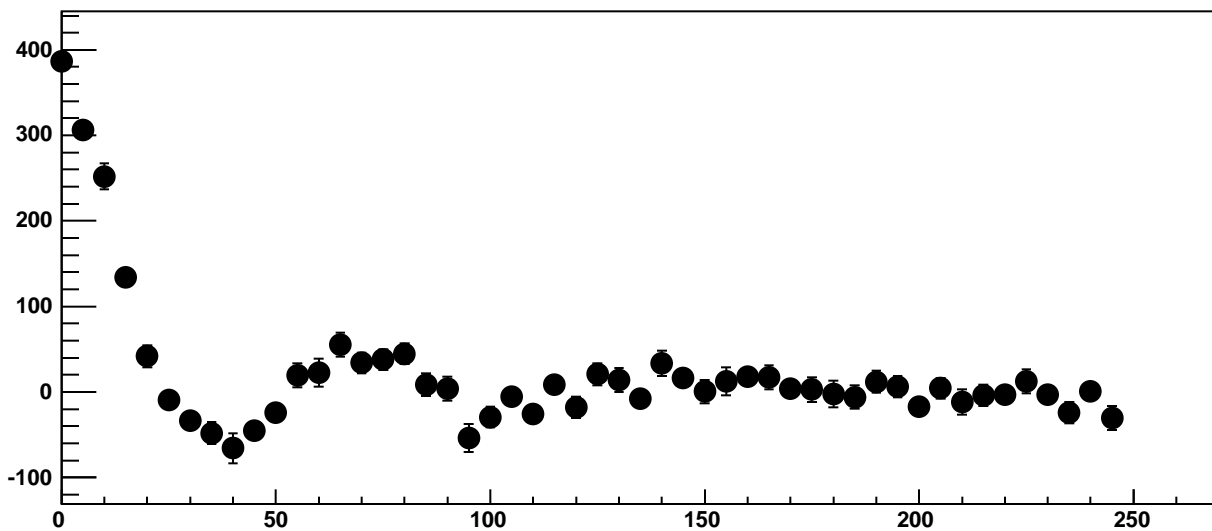


$\chi^2 / \text{ndf}$	370.7 / 41
p0	-512.7 ± 3.968
p1	95.05 ± 0.6879
p2	-2.699e+10 ± 3.034e+08
p3	2.435e+09 ± 1.033e+06
p4	10.66 ± 0.1158

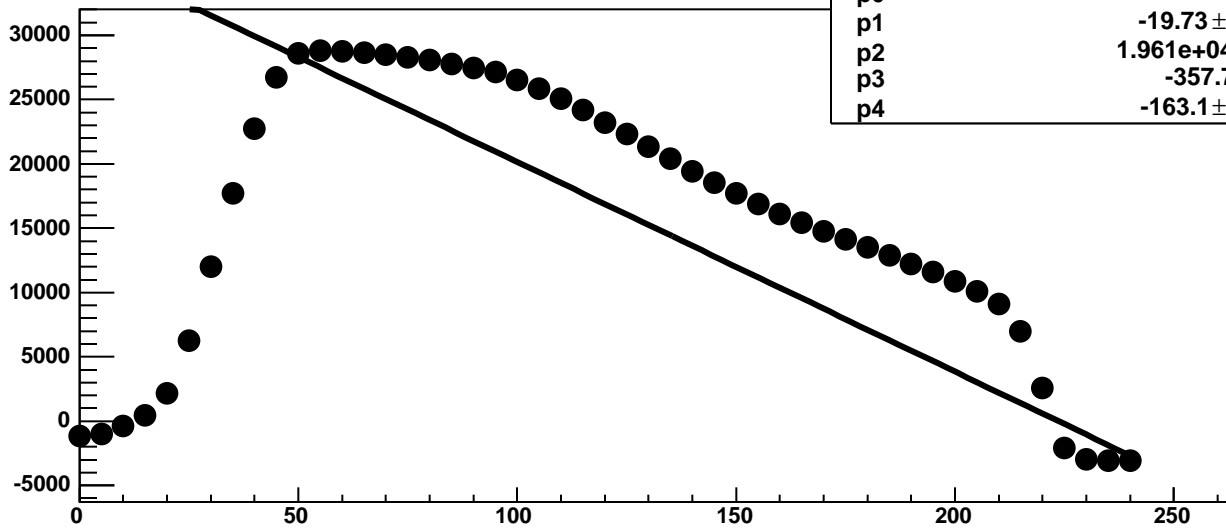
Chip 2, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 2, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

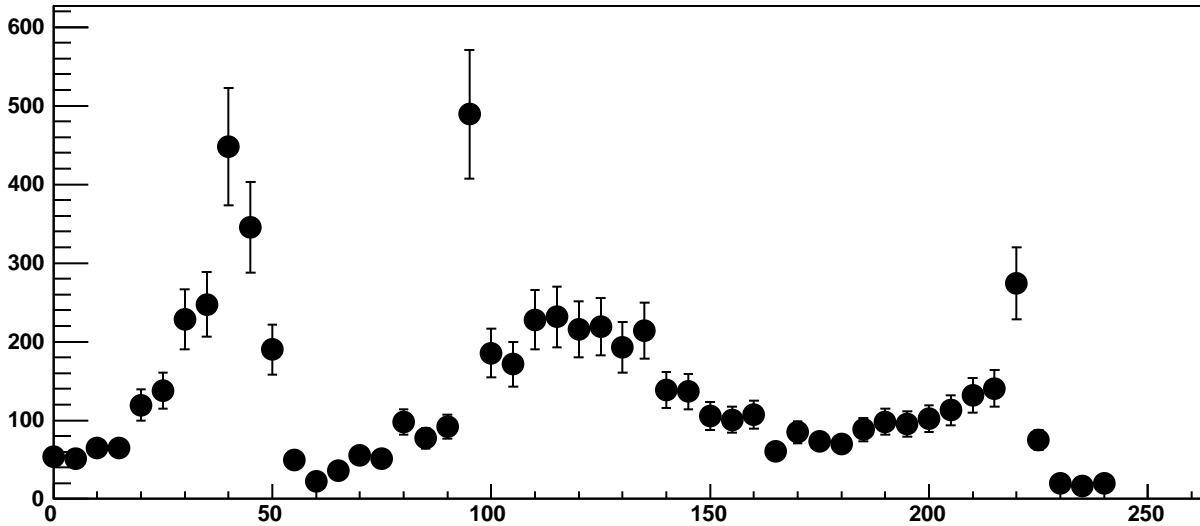


Chip 2, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold

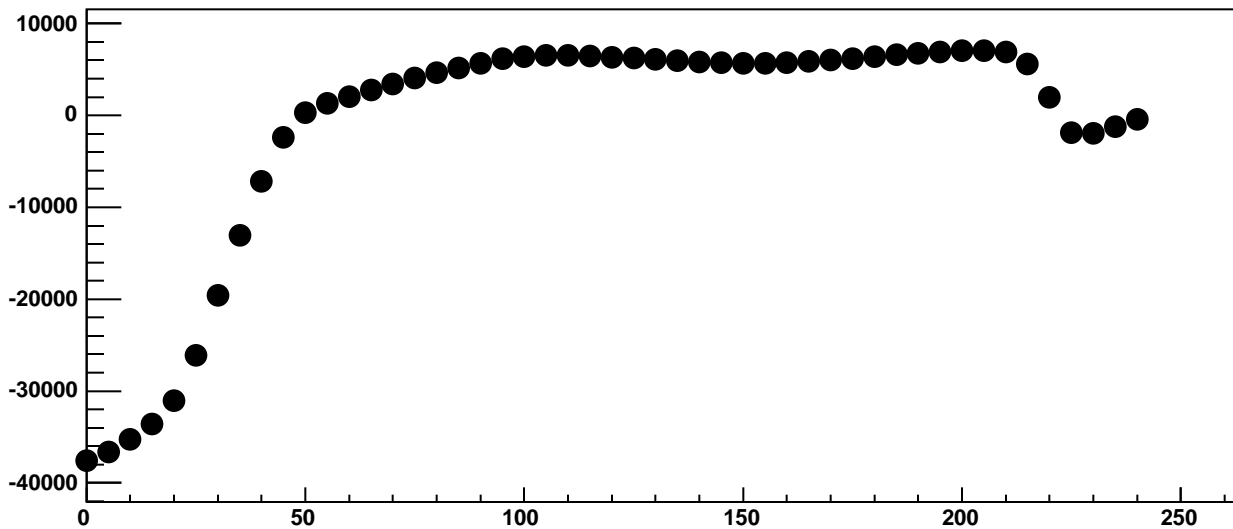


$\chi^2 / \text{ndf}$	9.754e+06 / 41
p0	2.007e+04 ± 15.49
p1	-19.73 ± 0.02623
p2	1.961e+04 ± 10.03
p3	-357.7 ± 1.464
p4	-163.1 ± 0.03362

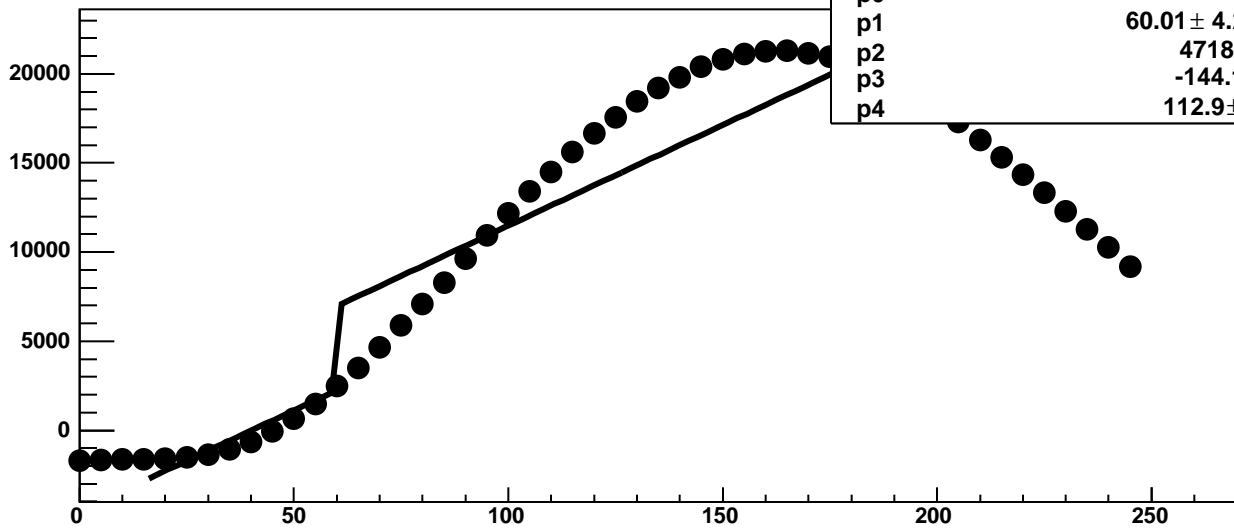
Chip 2, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



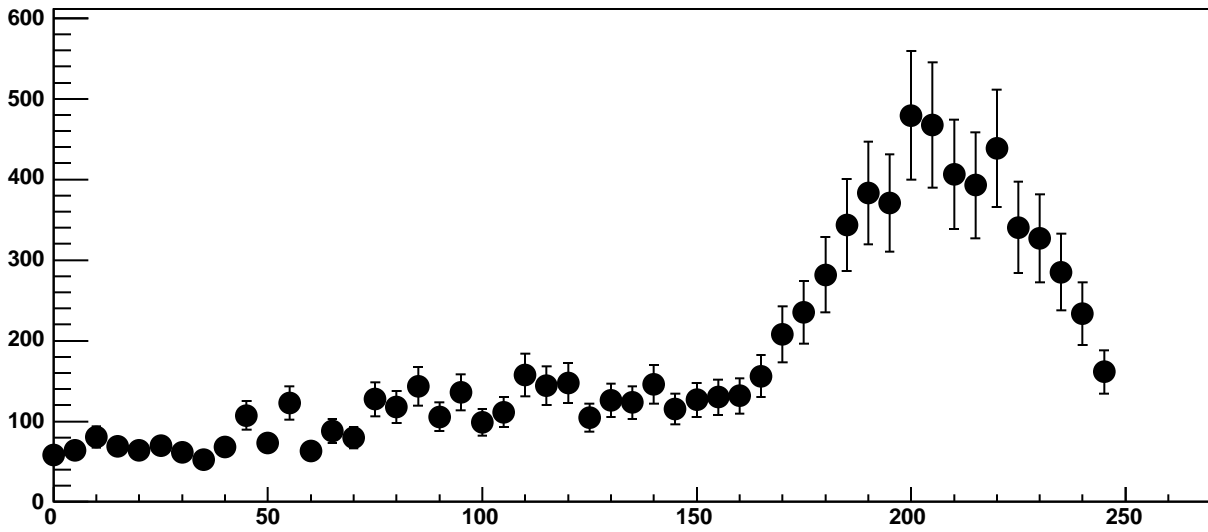
Chip 2, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold



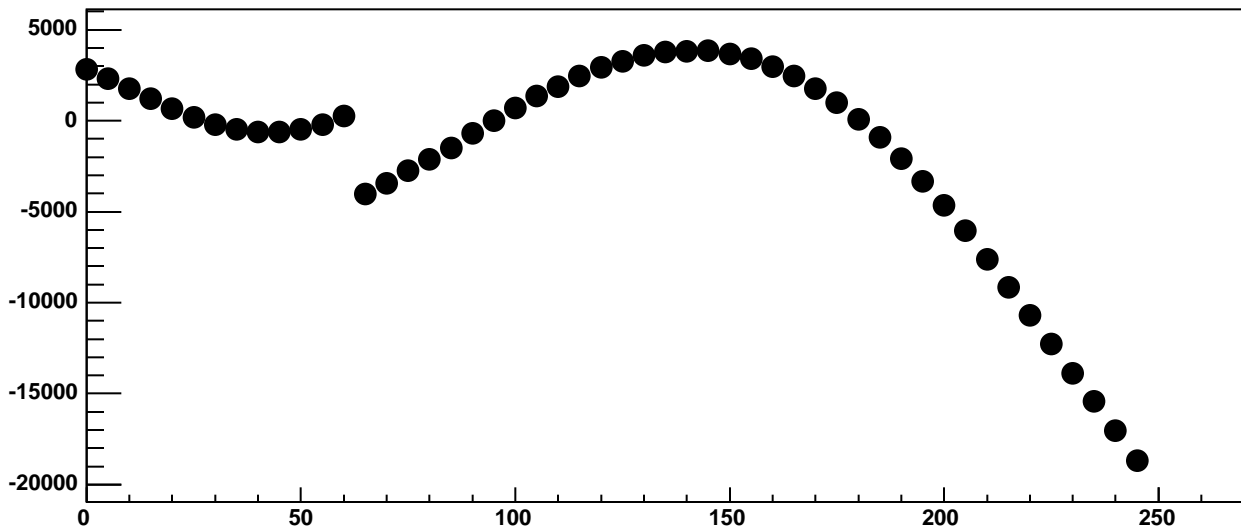
Chip 3, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold



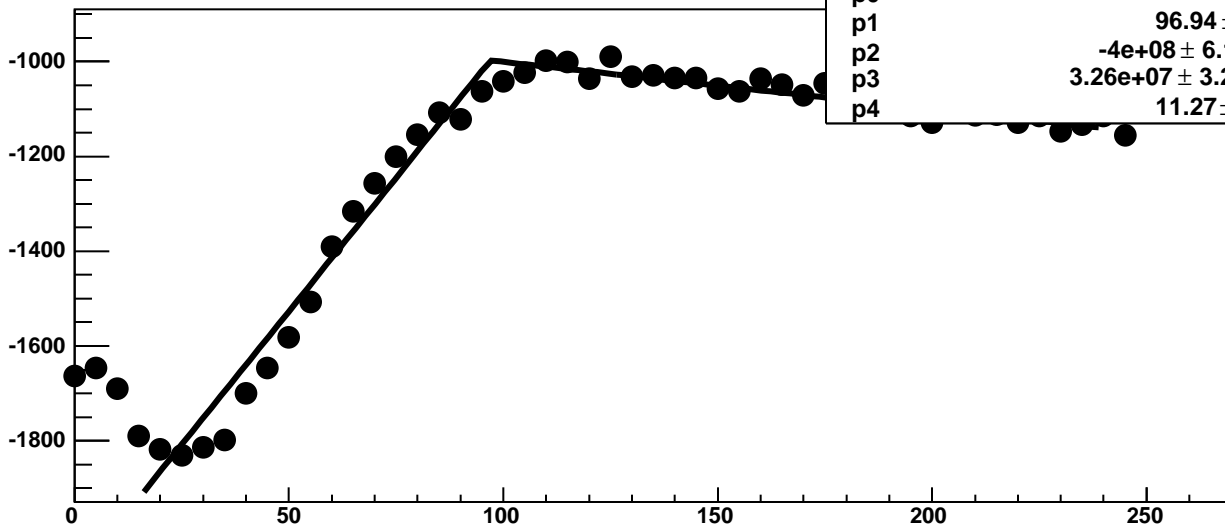
Chip 3, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold

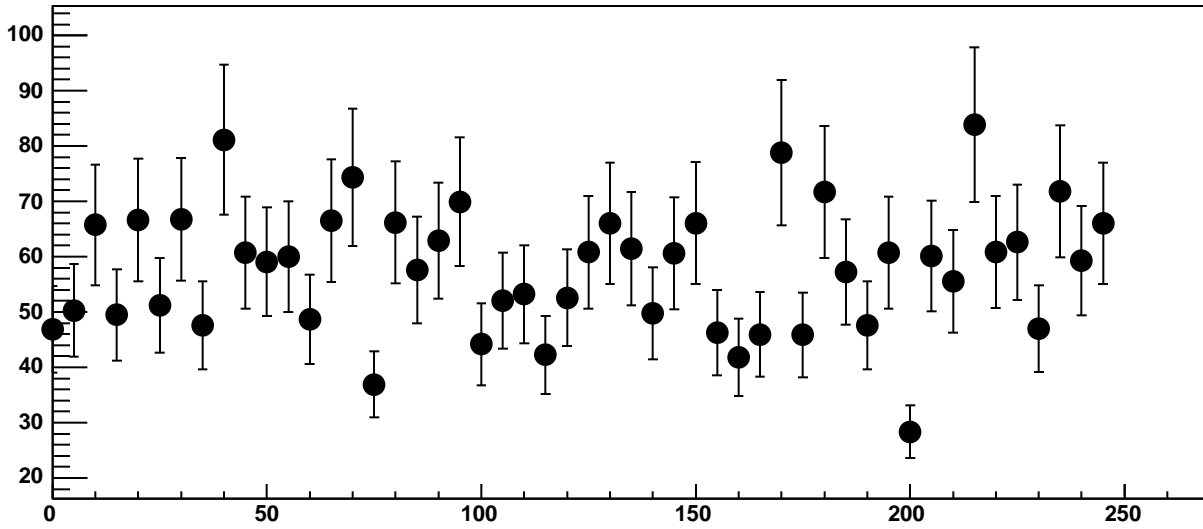


Chip 3, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

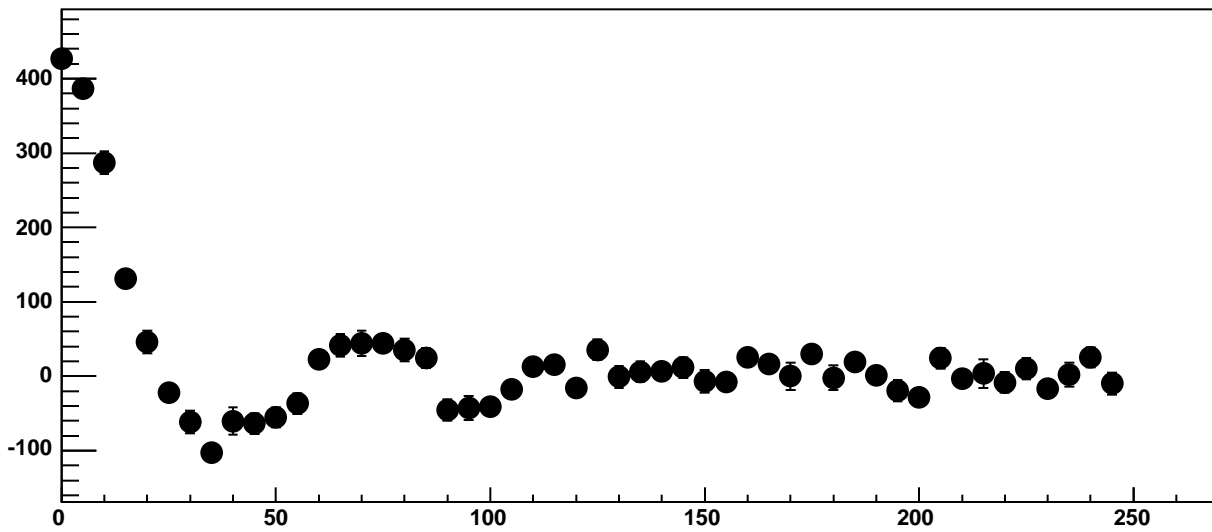


$\chi^2 / \text{ndf}$	461.2 / 41
p0	$-997.5 \pm 4.117$
p1	$96.94 \pm 0.6323$
p2	$-4e+08 \pm 6.103e+06$
p3	$3.26e+07 \pm 3.284e+05$
p4	$11.27 \pm 0.1304$

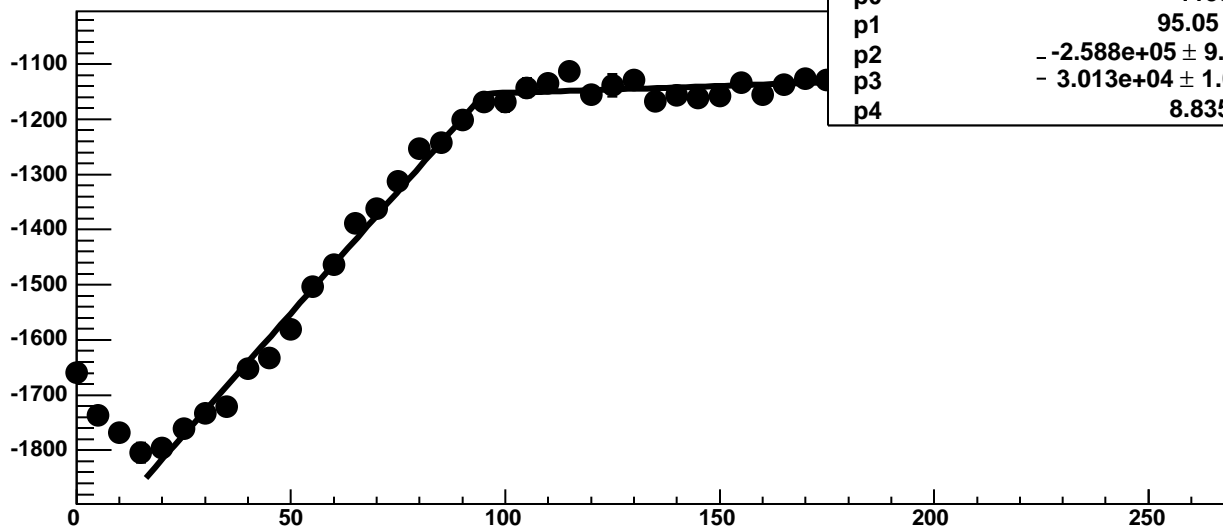
Chip 3, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold

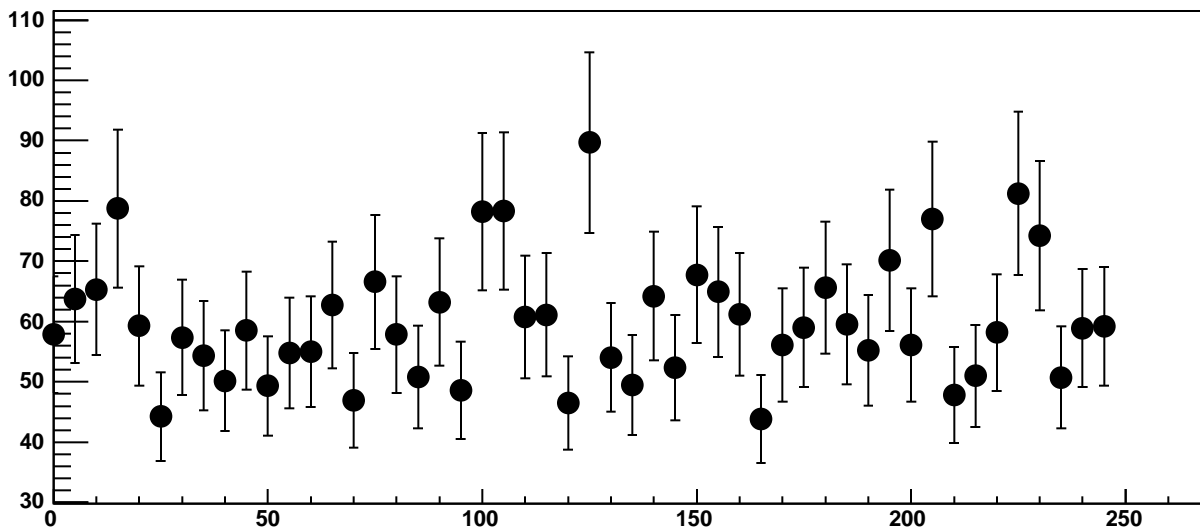


Chip 3, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

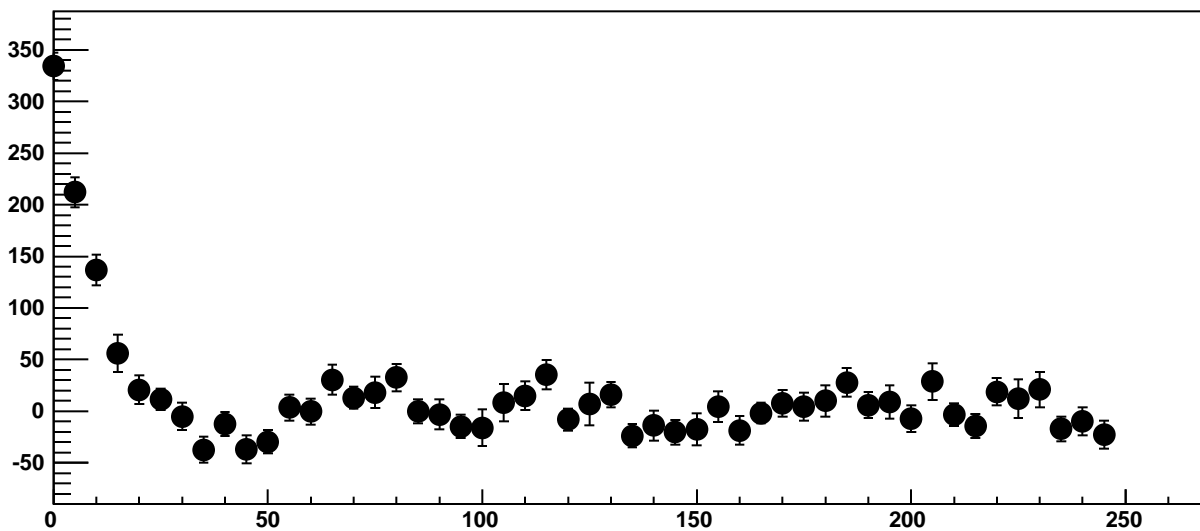


$\chi^2 / \text{ndf}$	92.3 / 41
p0	-1153 ± 5.533
p1	95.05 ± 0.9259
p2	-2.588e+05 ± 9.011e+04
p3	-3.013e+04 ± 1.051e+04
p4	8.835 ± 0.127

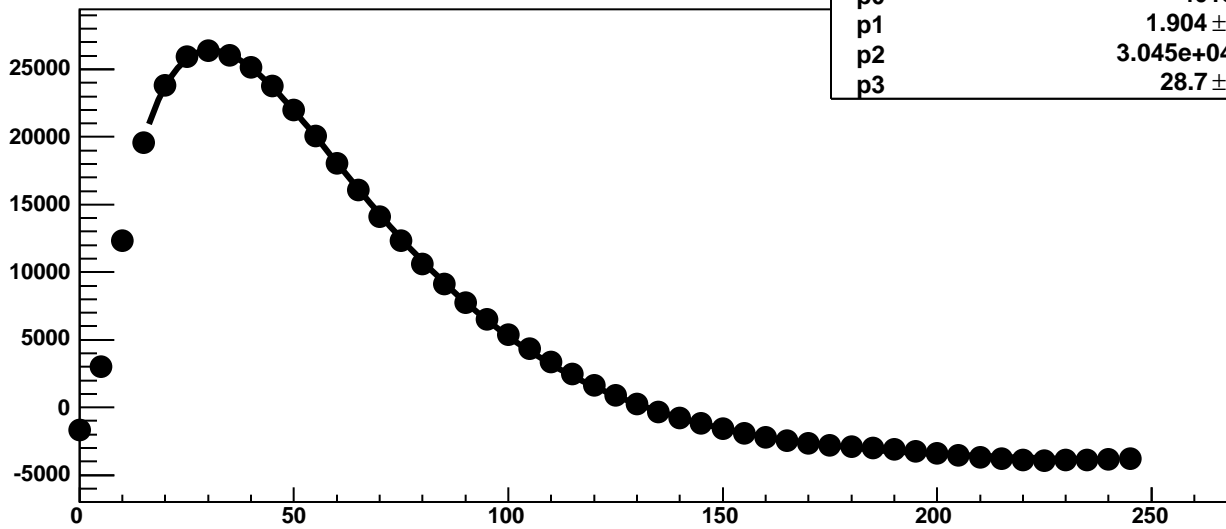
Chip 3, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



Chip 3, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

3087 / 42

p0

$-4018 \pm 4.046$

p1

$1.904 \pm 0.01999$

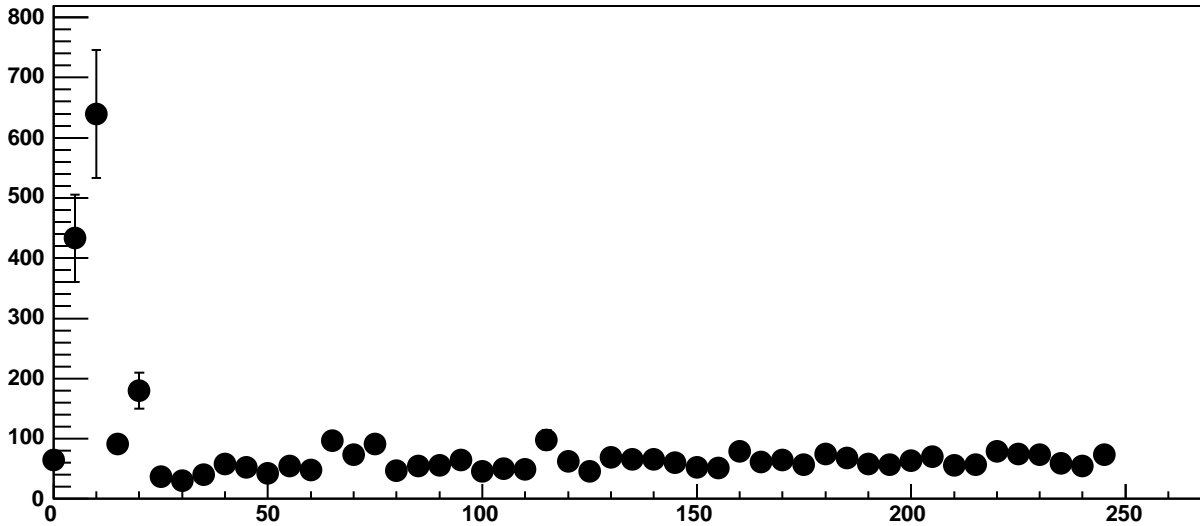
p2

$3.045\text{e}+04 \pm 5.082$

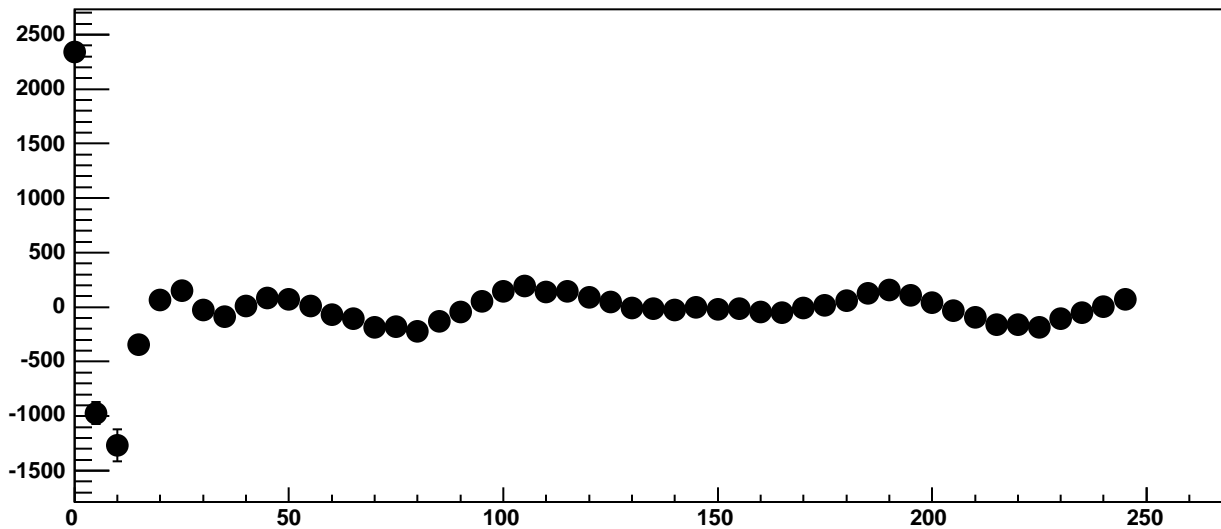
p3

$28.7 \pm 0.01124$

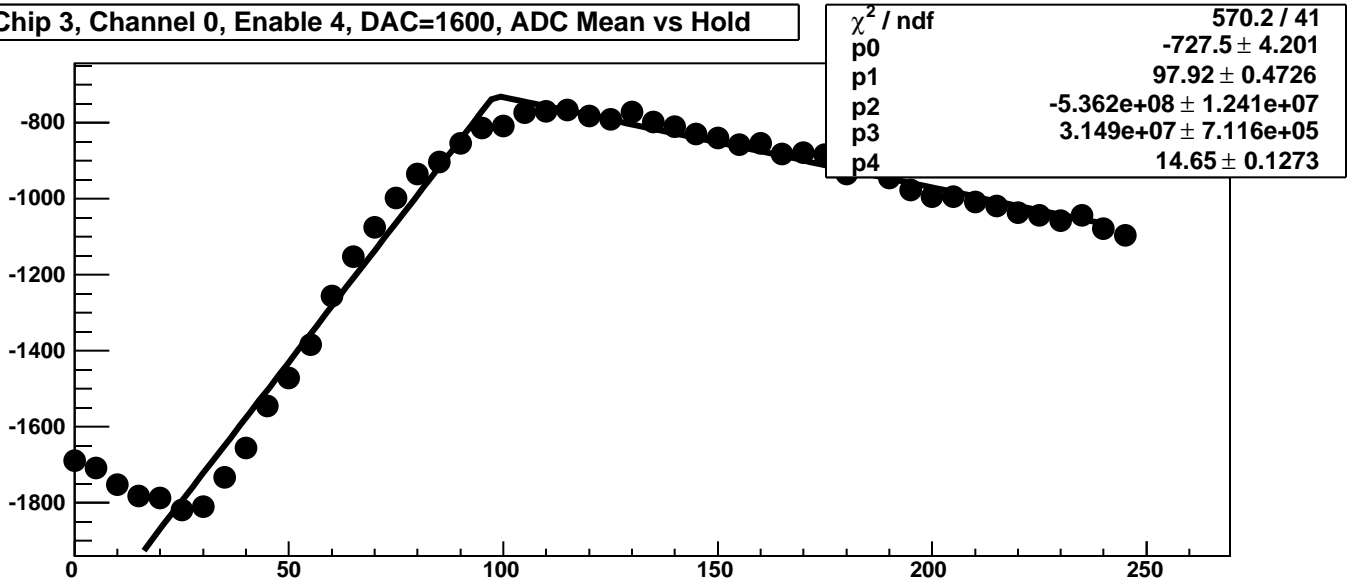
Chip 3, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



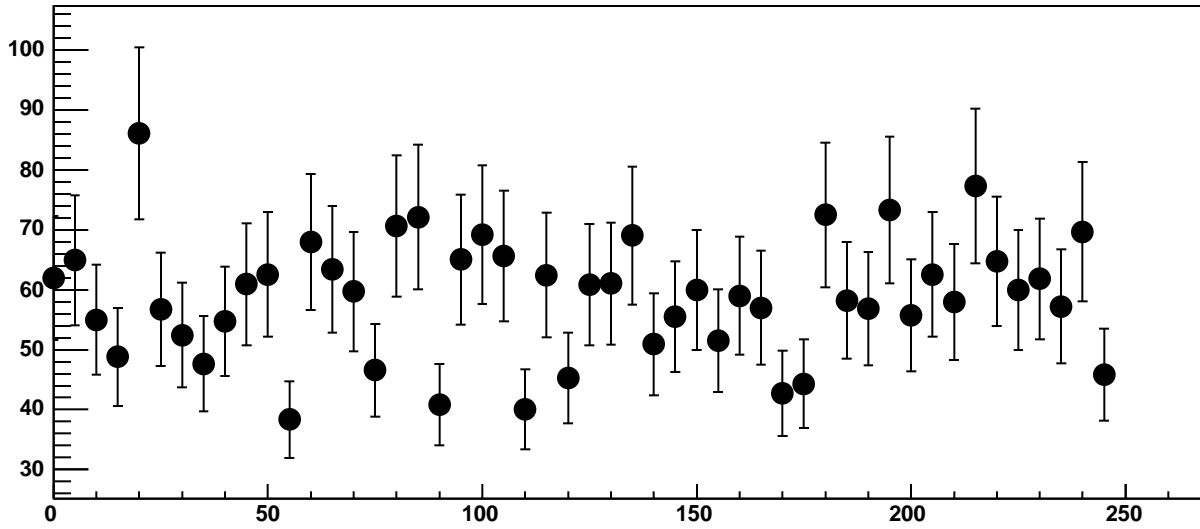
Chip 3, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold



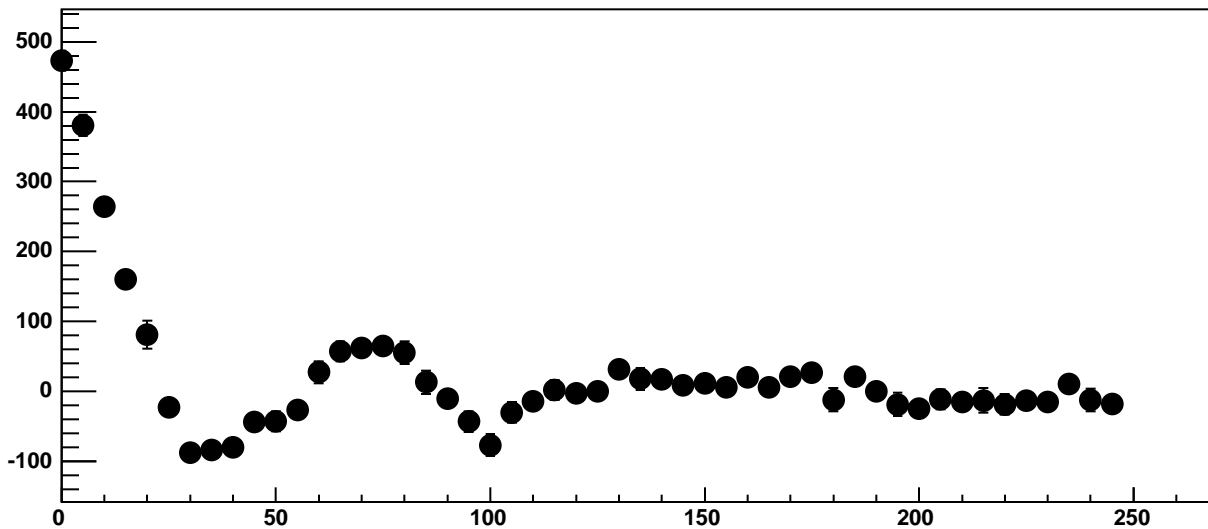
Chip 3, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold



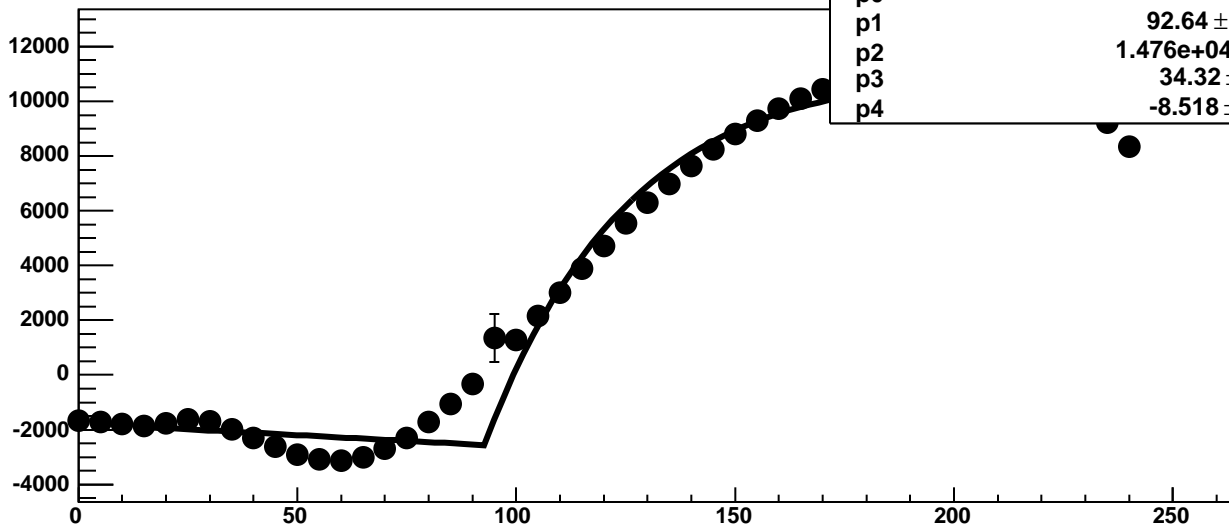
Chip 3, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

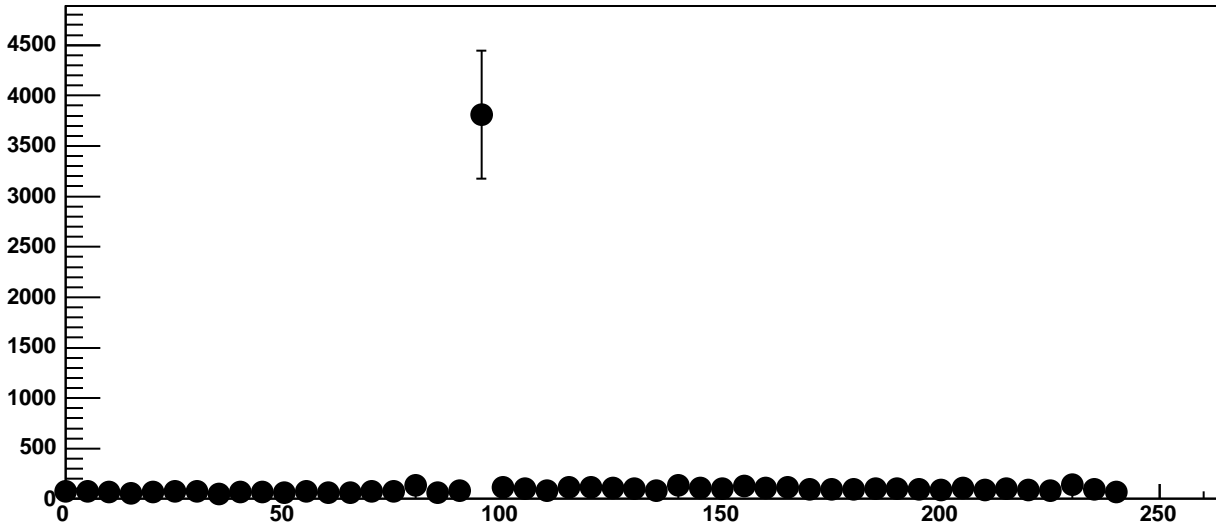


Chip 3, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

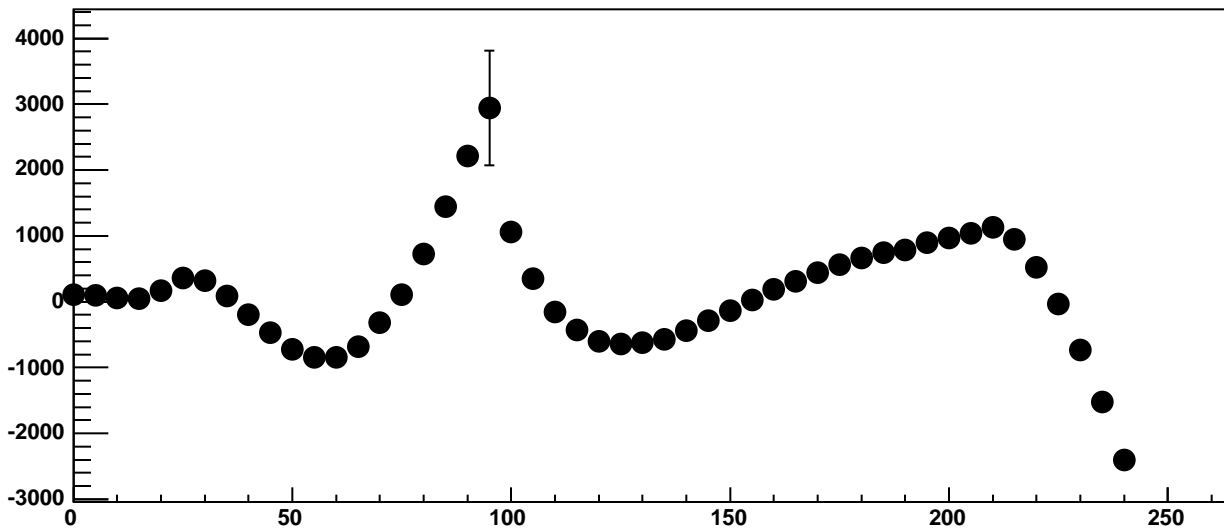


$\chi^2 / \text{ndf}$	8.656e+04 / 41
p0	-2560 ± 7.394
p1	92.64 ± 0.06361
p2	1.476e+04 ± 28.38
p3	34.32 ± 0.1168
p4	-8.518 ± 0.1454

Chip 3, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

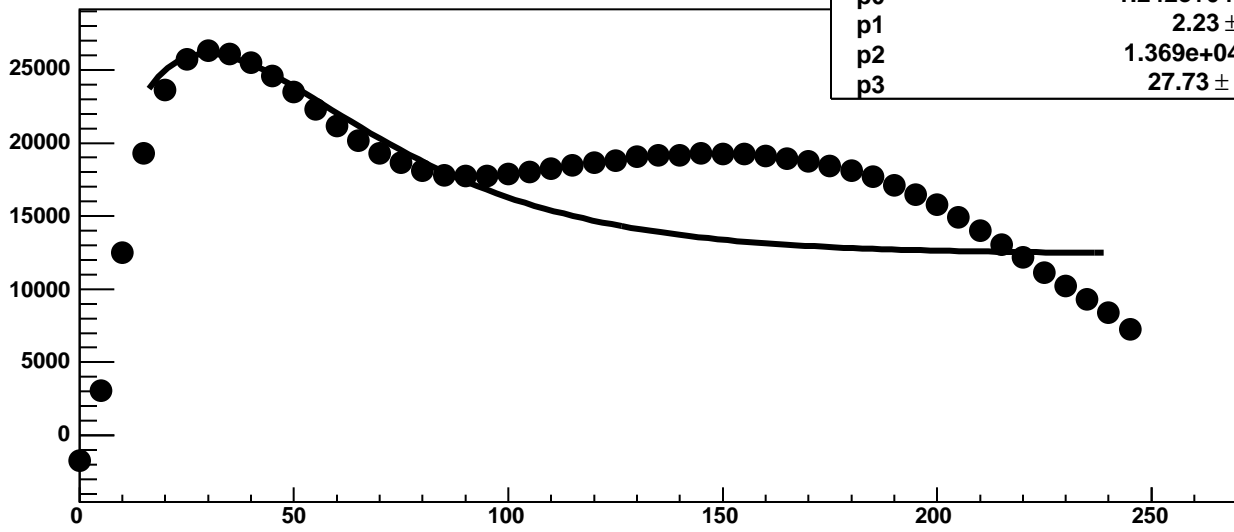


Chip 3, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold



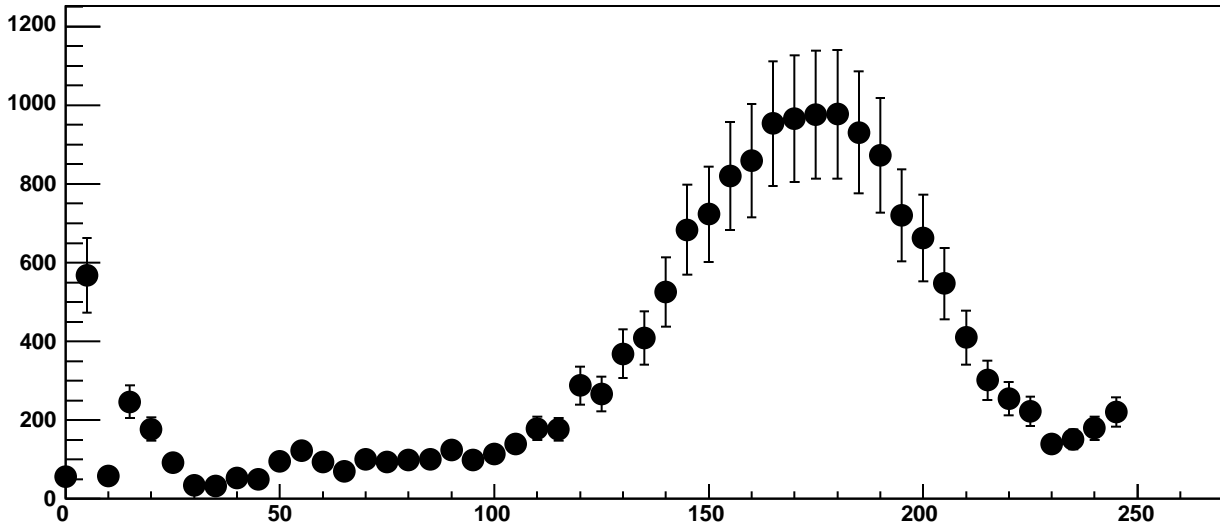


Chip 3, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold

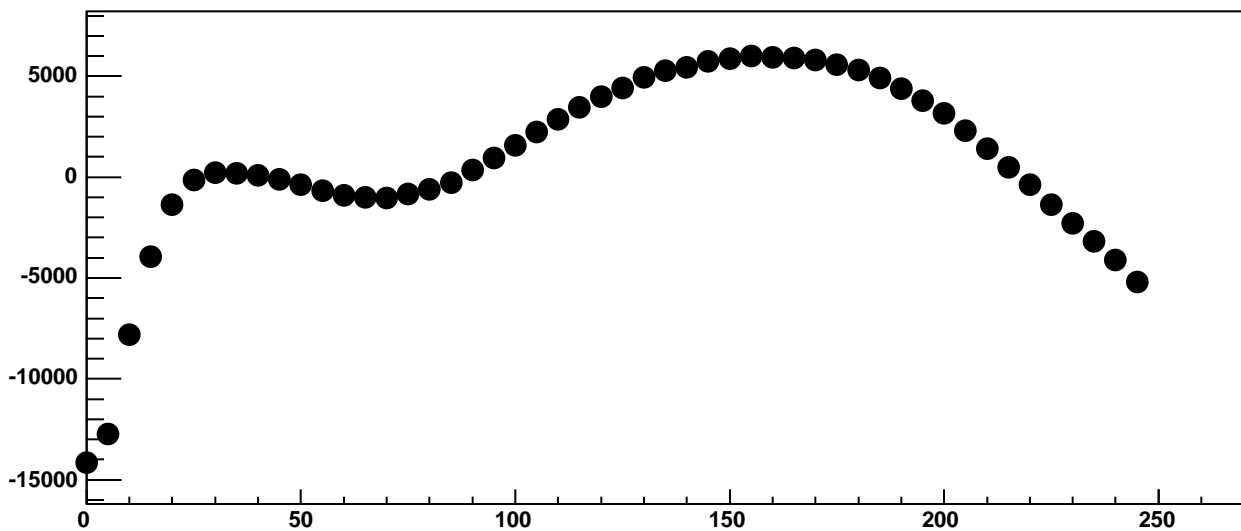


$\chi^2 / \text{ndf}$	9.228e+04 / 42
p0	1.242e+04 $\pm$ 21.07
p1	2.23 $\pm$ 0.1346
p2	1.369e+04 $\pm$ 21.2
p3	27.73 $\pm$ 0.08671

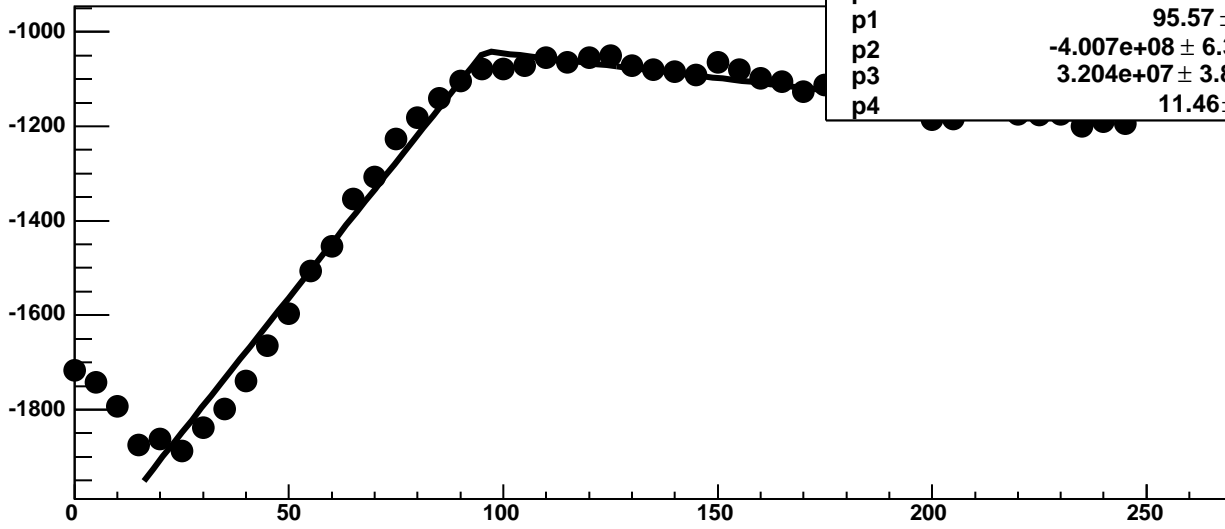
Chip 3, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold

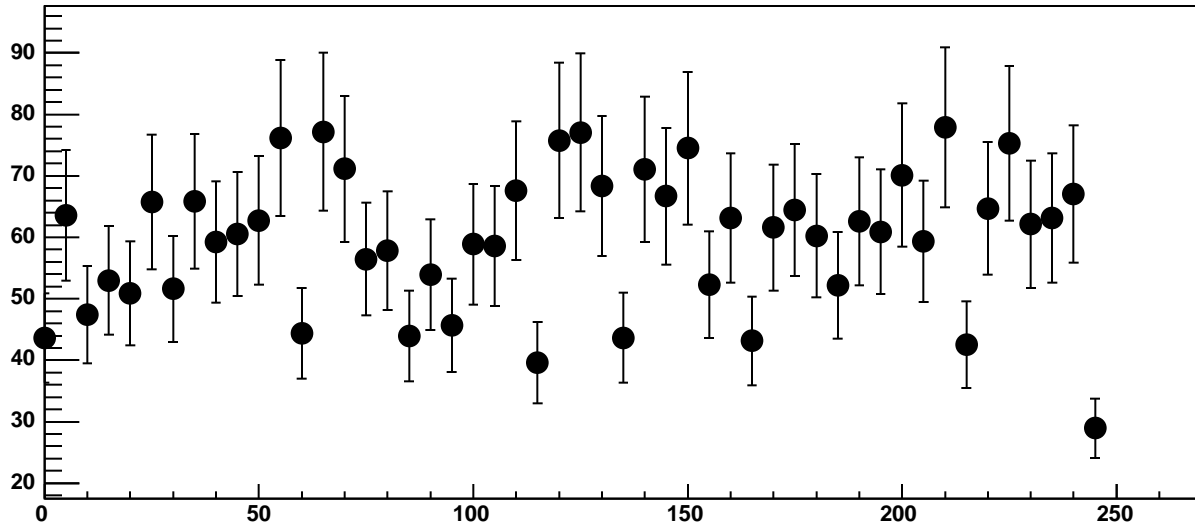


Chip 3, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

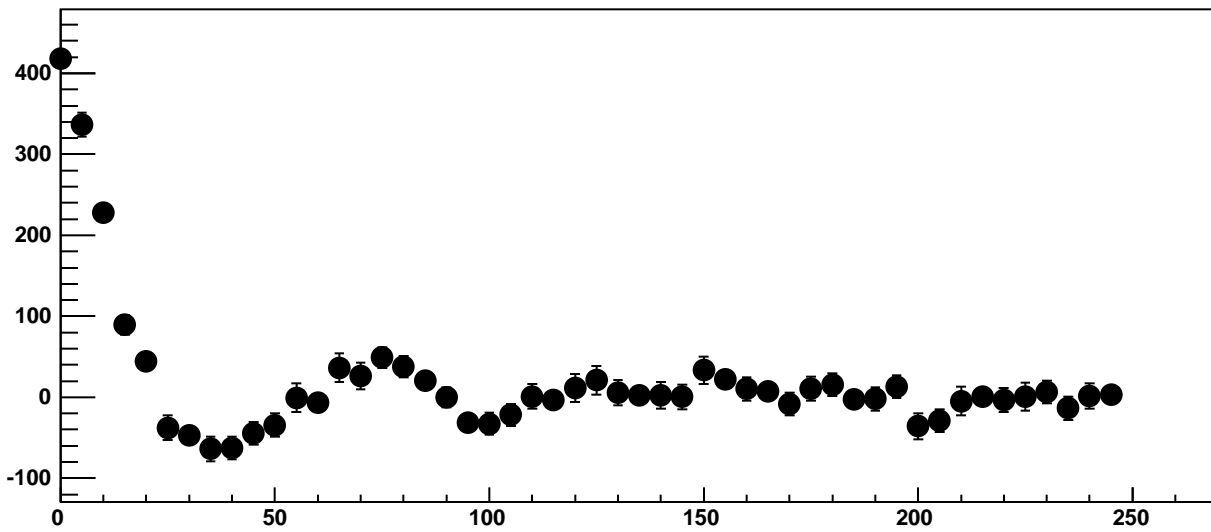


$\chi^2 / \text{ndf}$	222.4 / 41
p0	-1041 ± 4.673
p1	95.57 ± 0.6024
p2	-4.007e+08 ± 6.322e+06
p3	3.204e+07 ± 3.845e+05
p4	11.46 ± 0.1193

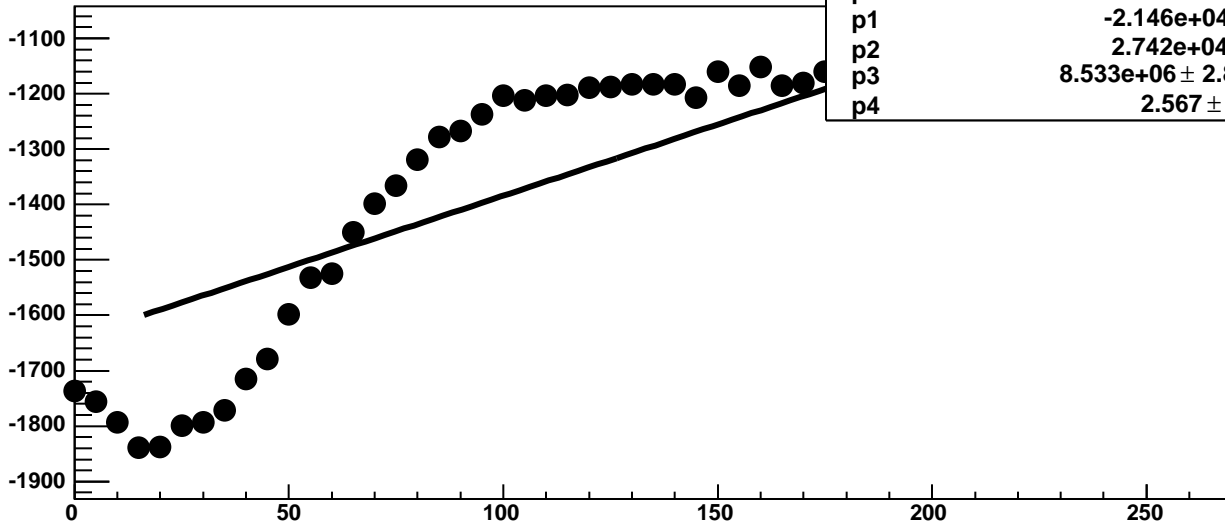
Chip 3, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

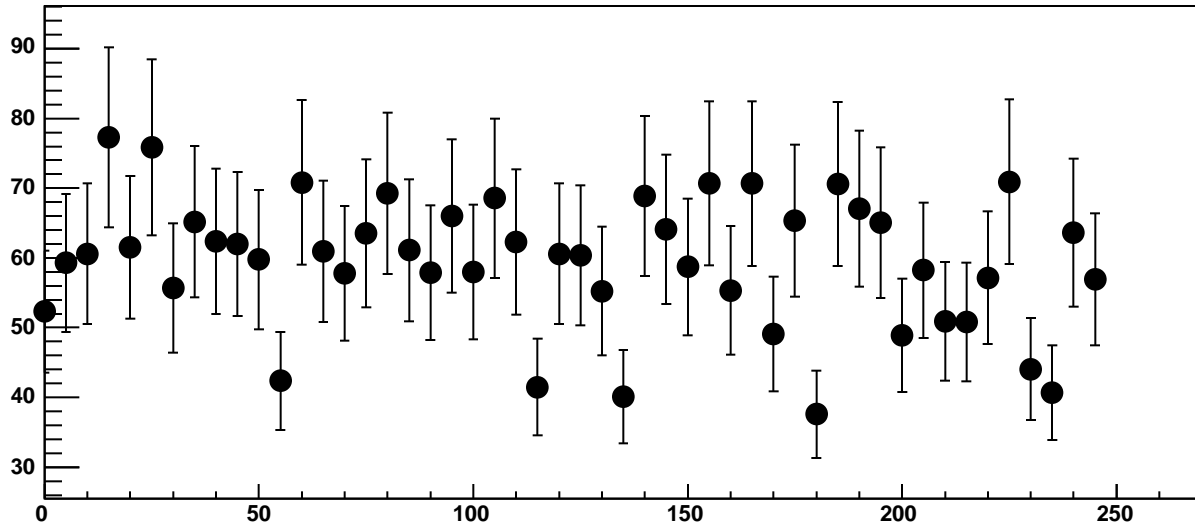


Chip 3, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

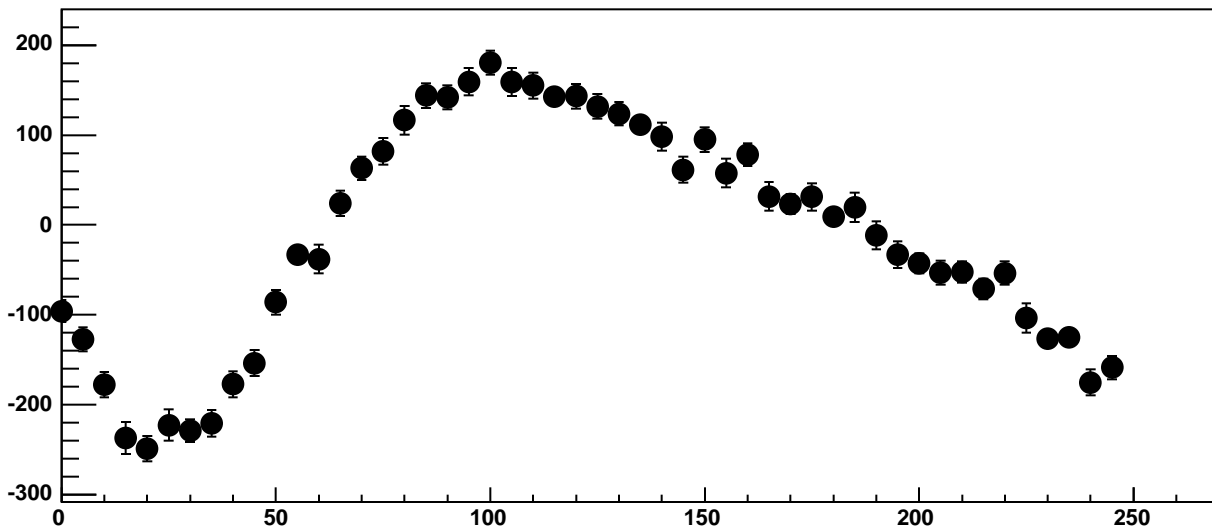


$\chi^2 / \text{ndf}$	3830 / 41
p0	-5.679e+04 ± 22.45
p1	-2.146e+04 ± 8.736
p2	2.742e+04 ± 9262
p3	8.533e+06 ± 2.877e+06
p4	2.567 ± 0.00104

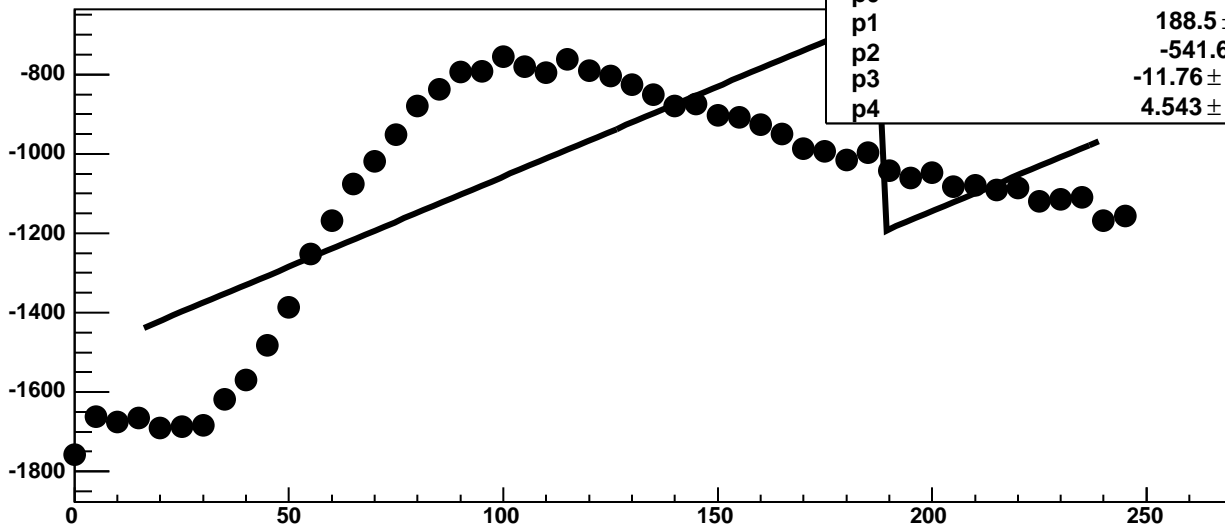
Chip 3, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



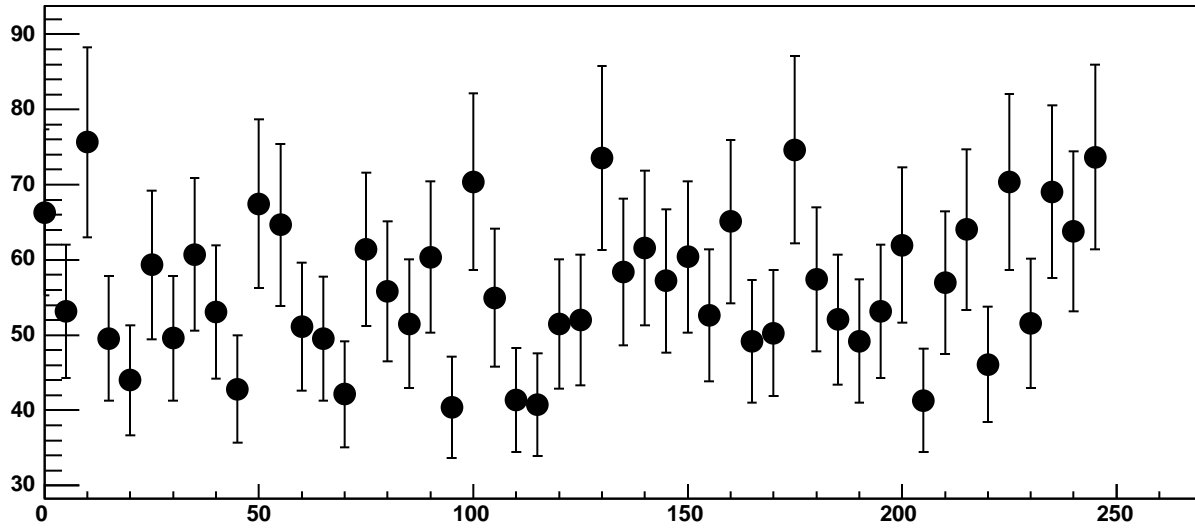
Chip 3, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold



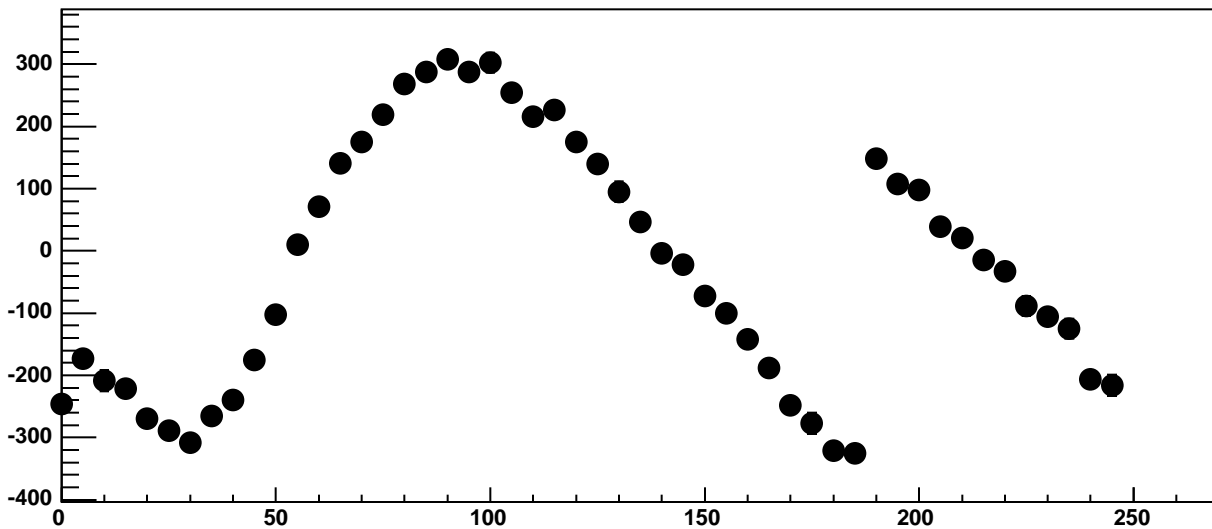
Chip 3, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold



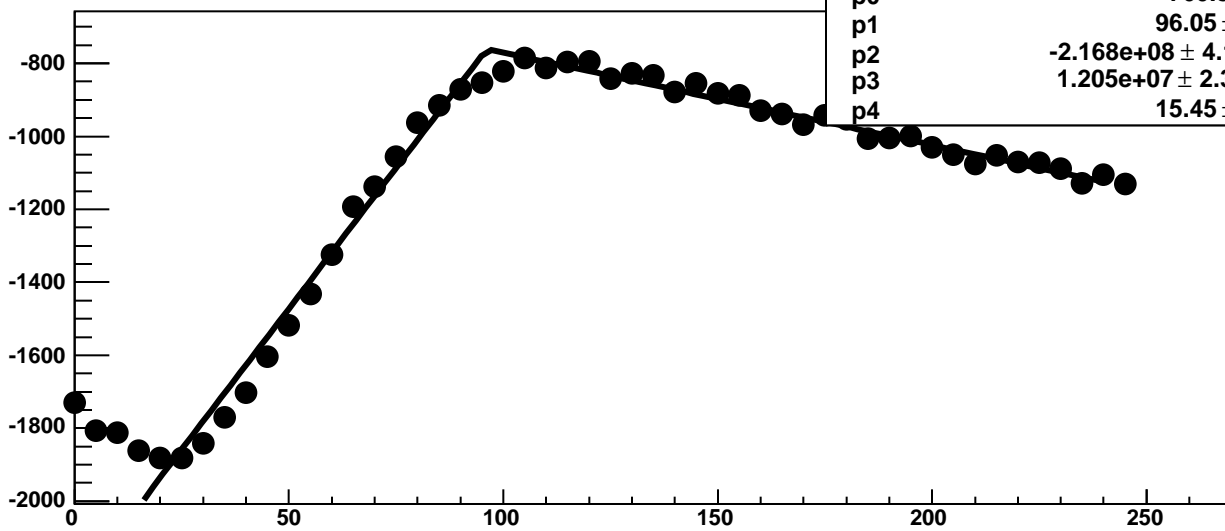
Chip 3, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold

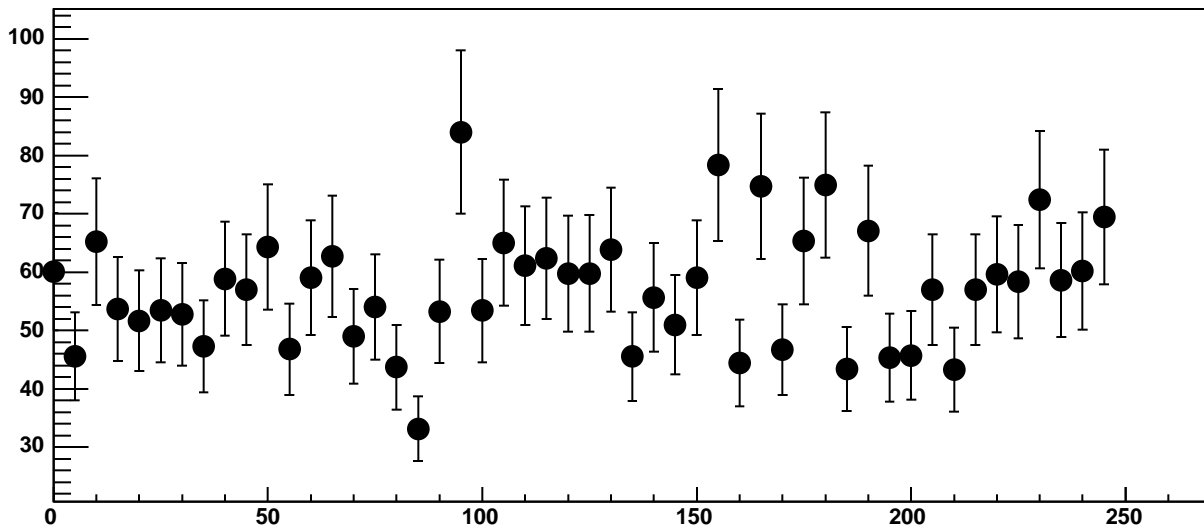


Chip 3, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

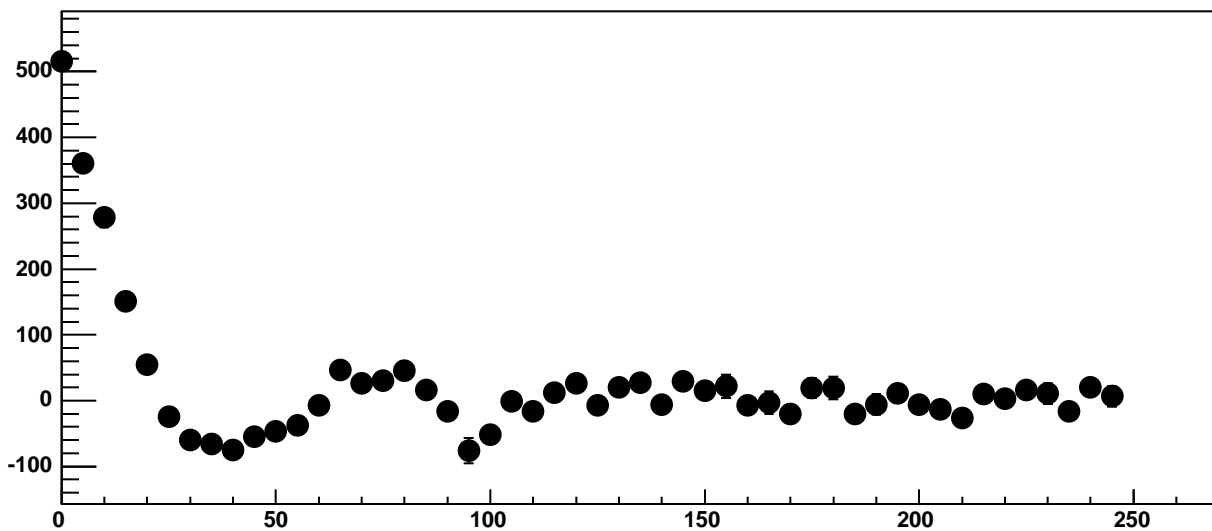


$\chi^2 / \text{ndf}$	439.9 / 41
p0	-760.8 ± 4.303
p1	96.05 ± 0.3988
p2	-2.168e+08 ± 4.146e+06
p3	1.205e+07 ± 2.326e+05
p4	15.45 ± 0.1102

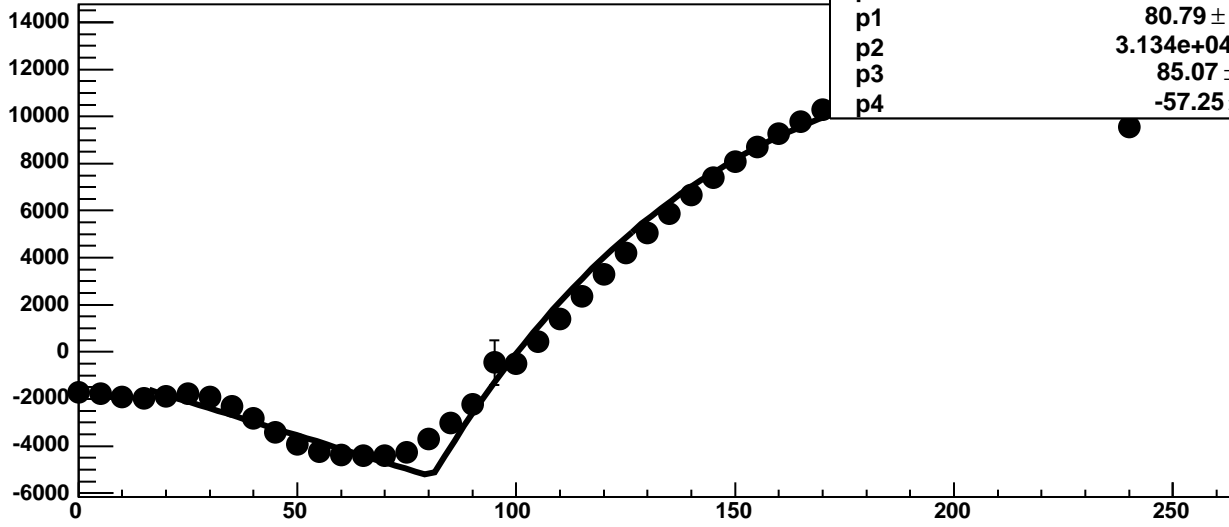
Chip 3, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

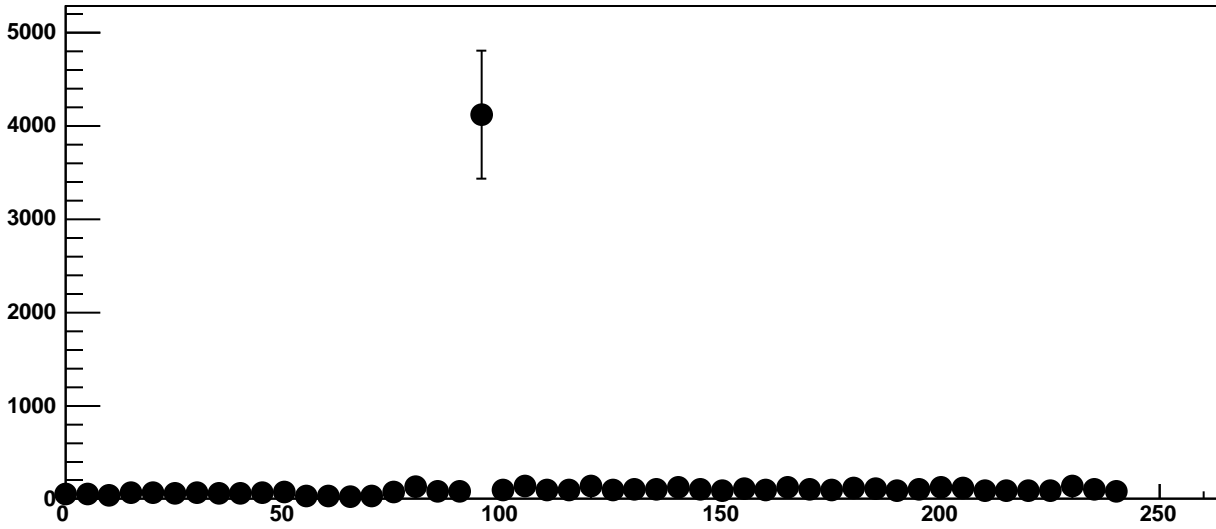


Chip 3, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

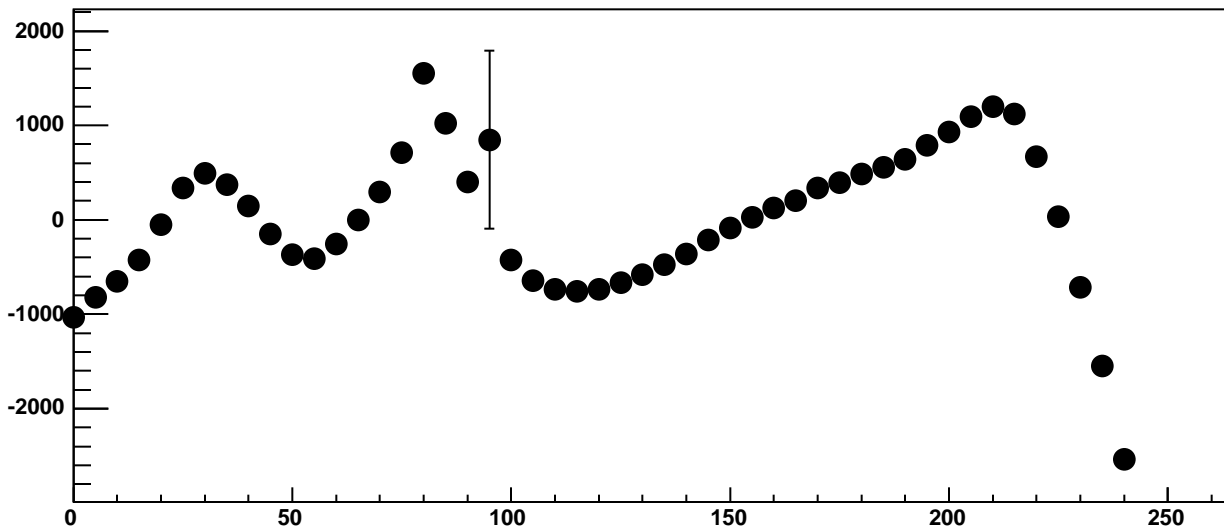


$\chi^2 / \text{ndf}$	5.887e+04 / 41
p0	-5306 ± 5.271
p1	80.79 ± 0.04292
p2	3.134e+04 ± 56.29
p3	85.07 ± 0.2094
p4	-57.25 ± 0.1761

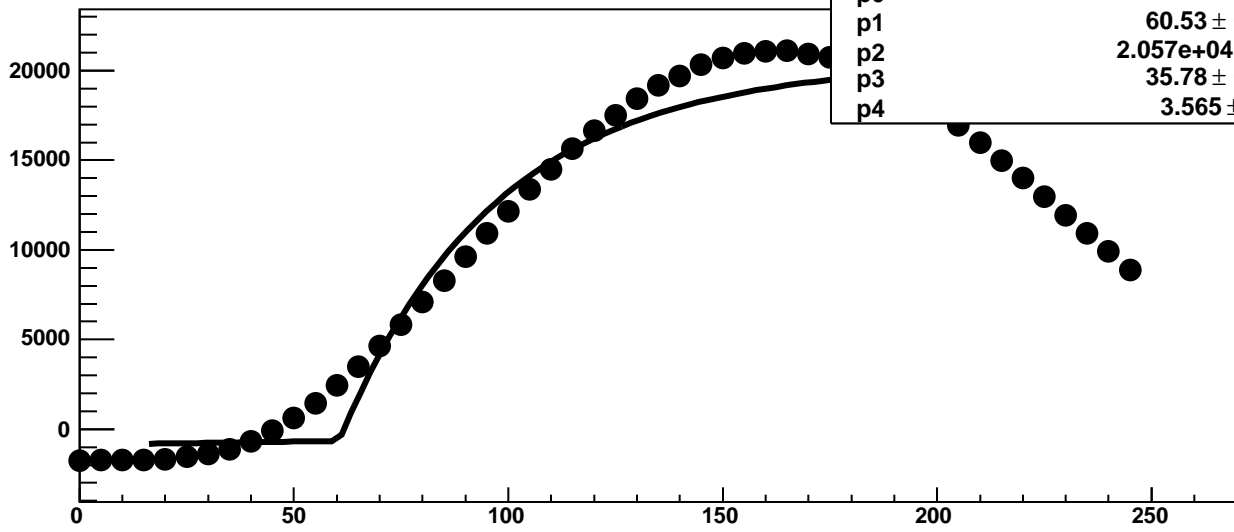
Chip 3, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

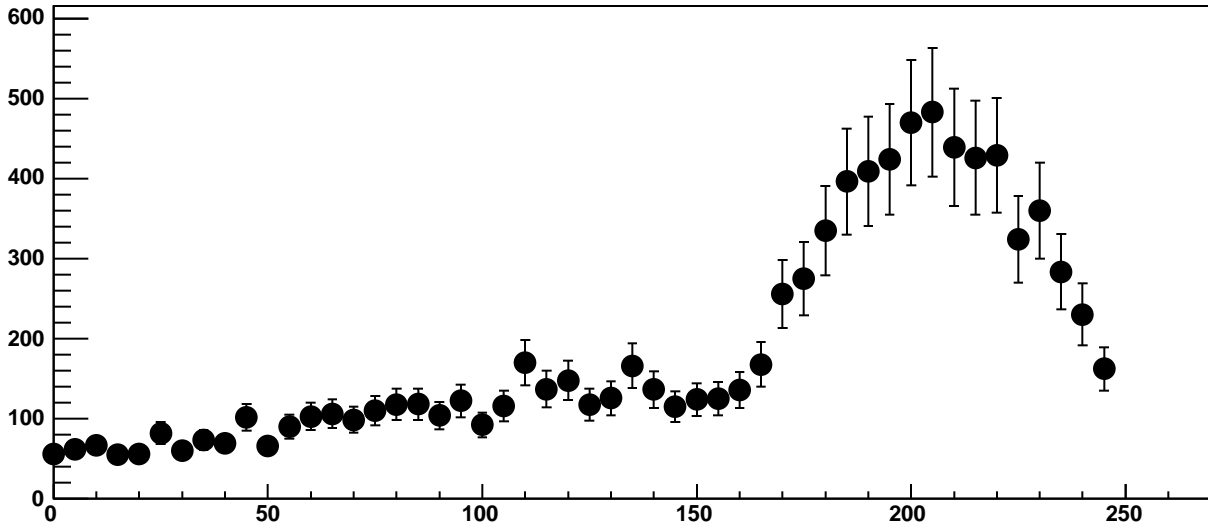


Chip 3, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold

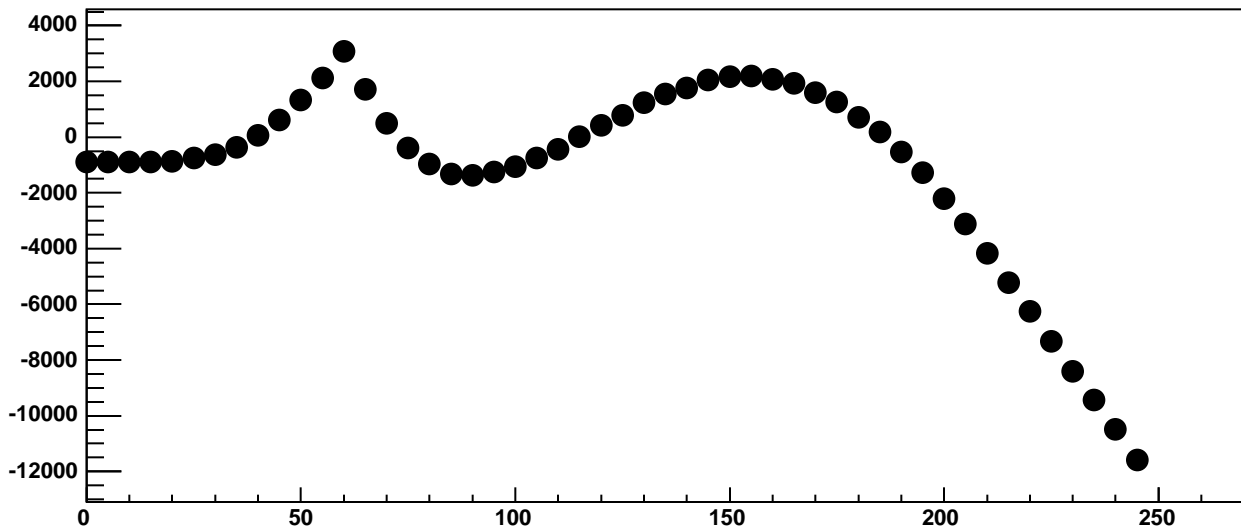


$\chi^2 / \text{ndf}$	1.91e+05 / 41
p0	-654.2 ± 9.149
p1	60.53 ± 0.04032
p2	2.057e+04 ± 45.22
p3	35.78 ± 0.09919
p4	3.565 ± 0.2733

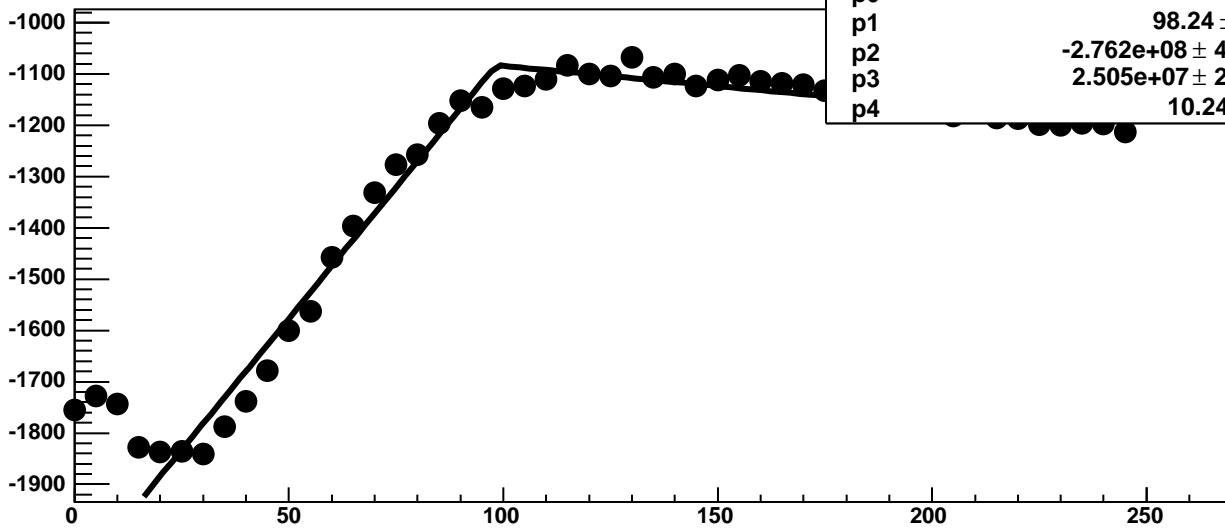
Chip 3, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

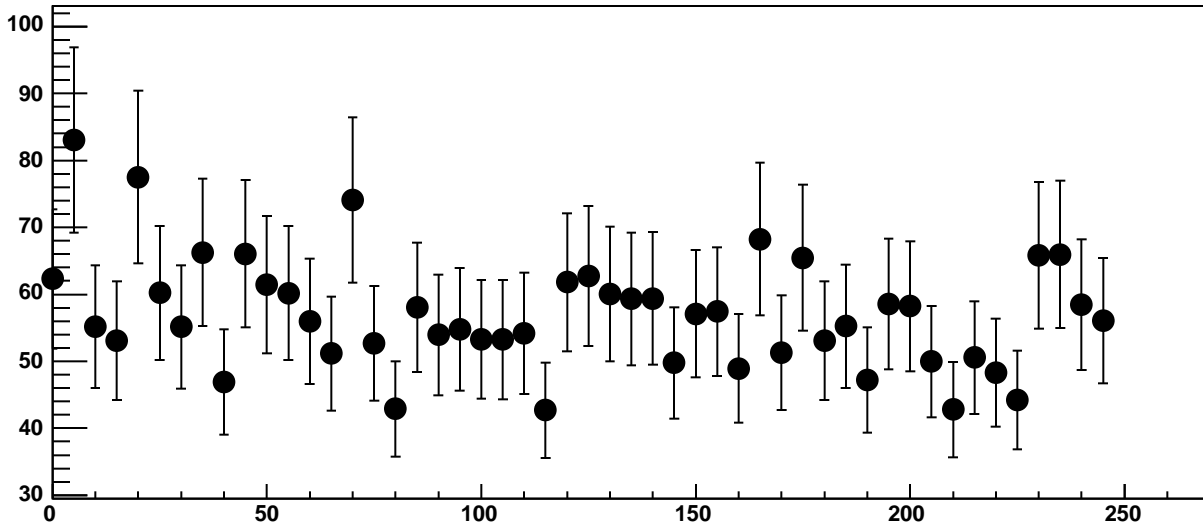


Chip 3, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

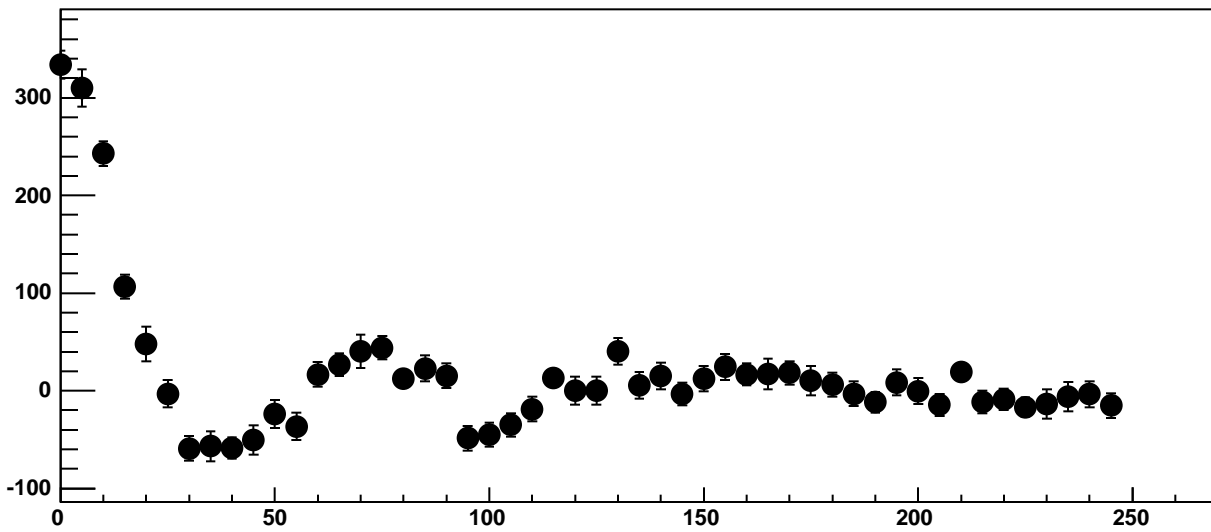


$\chi^2 / \text{ndf}$	276.8 / 41
p0	-1083 ± 4.292
p1	98.24 ± 0.6935
p2	-2.762e+08 ± 4.36e+06
p3	2.505e+07 ± 2.37e+05
p4	10.24 ± 0.128

Chip 3, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

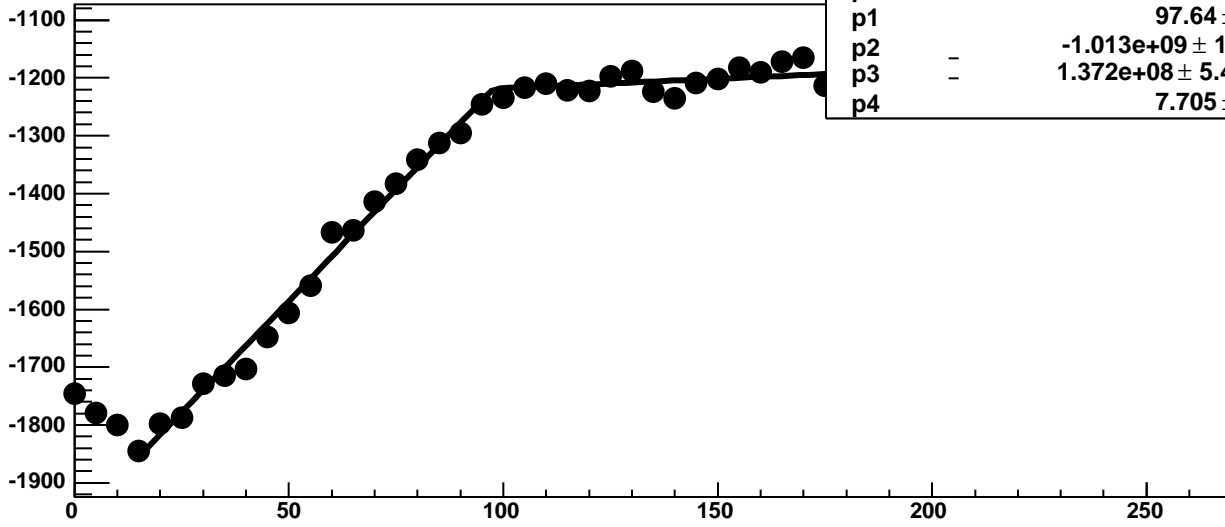


Chip 3, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



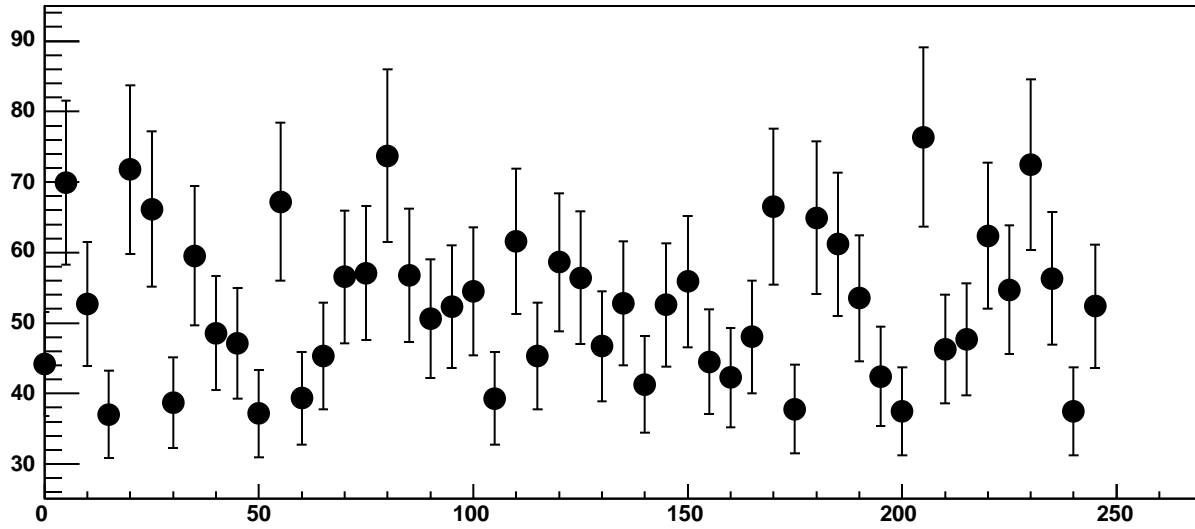


Chip 3, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

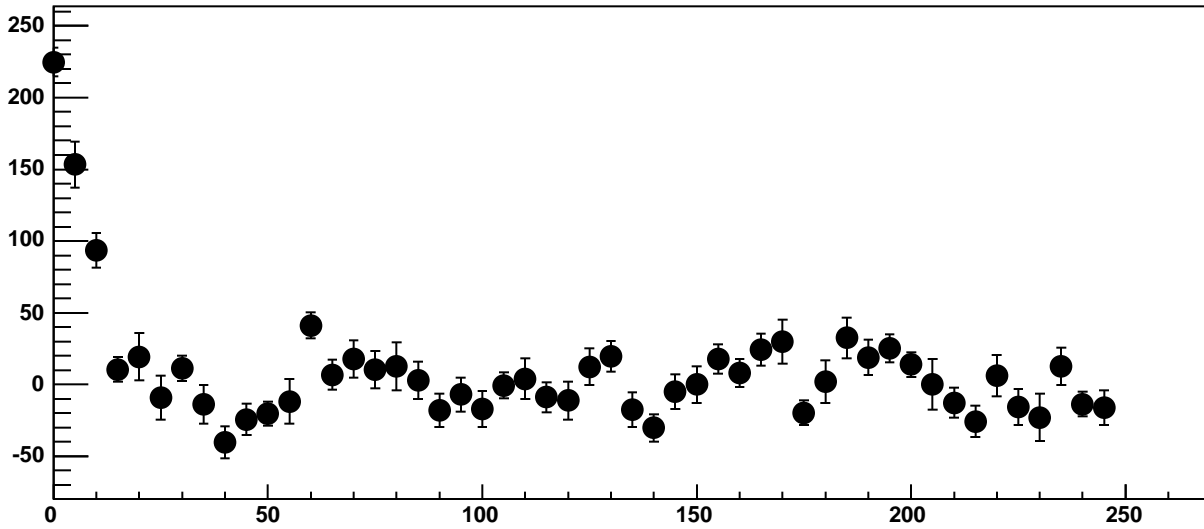


$\chi^2 / \text{ndf}$	126.2 / 41	
p0	-1218 ± 4.396	
p1	97.64 ± 0.9818	
p2	-1.013e+09 ± 1.78e+07	
p3	-	1.372e+08 ± 5.448e+05
p4	-	7.705 ± 0.1152

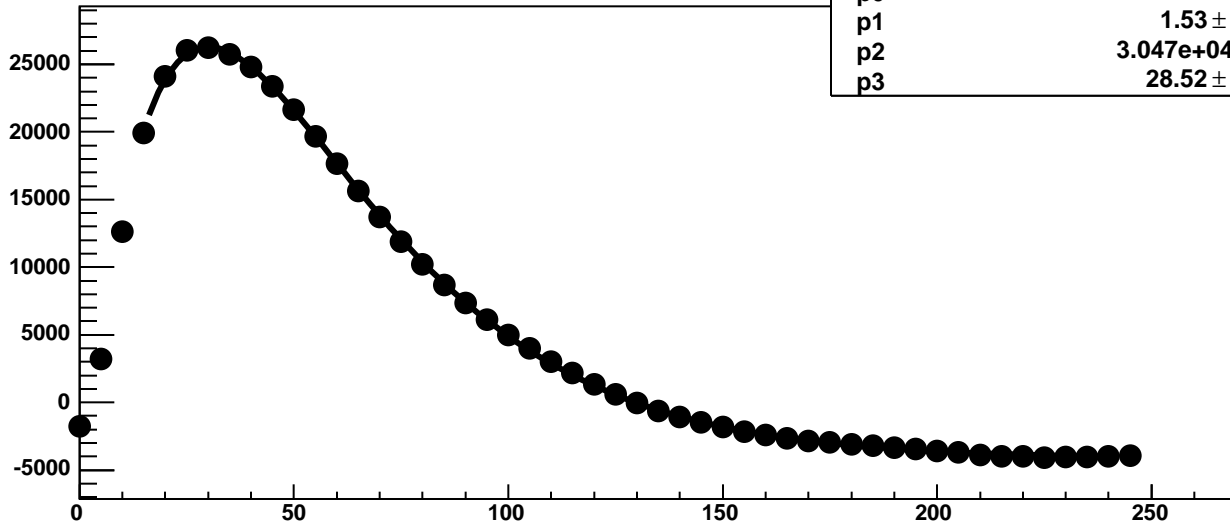
Chip 3, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

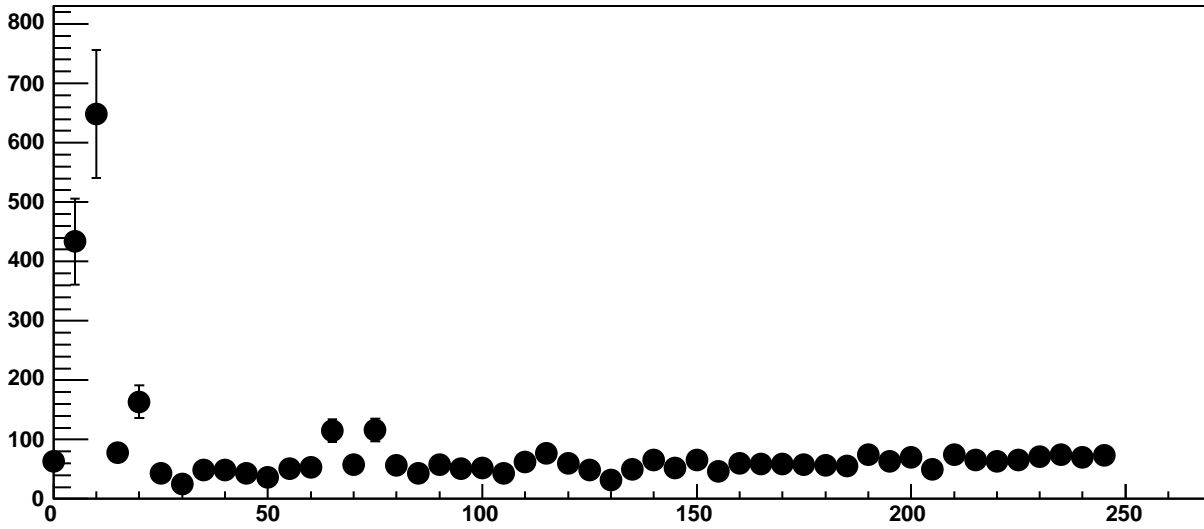


Chip 3, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

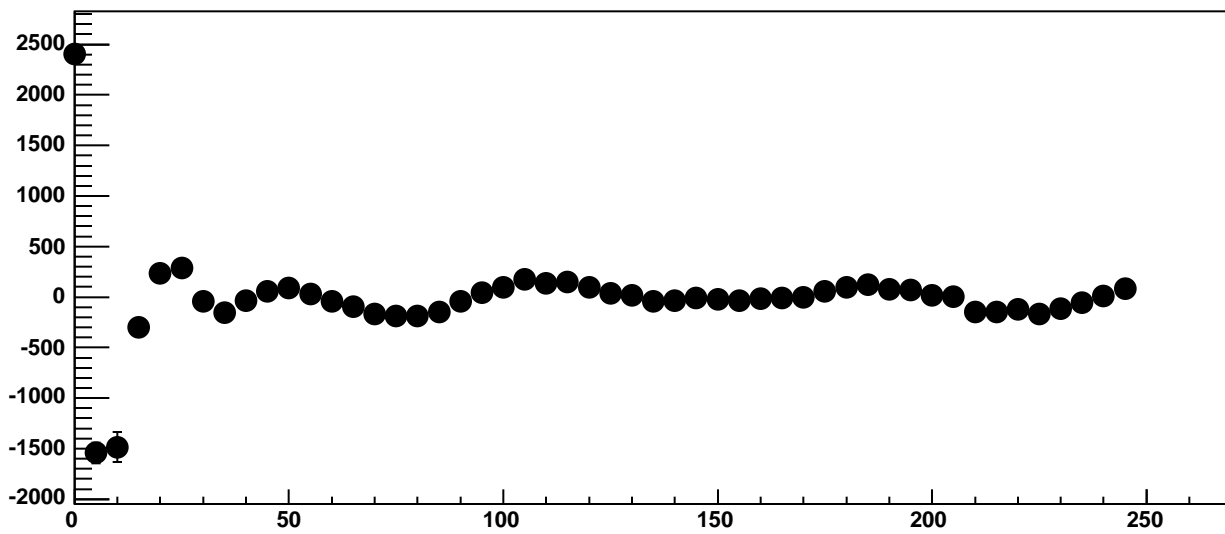


$\chi^2 / \text{ndf}$	3561 / 42
p0	$-4168 \pm 3.982$
p1	$1.53 \pm 0.01879$
p2	$3.047\text{e}+04 \pm 4.978$
p3	$28.52 \pm 0.01078$

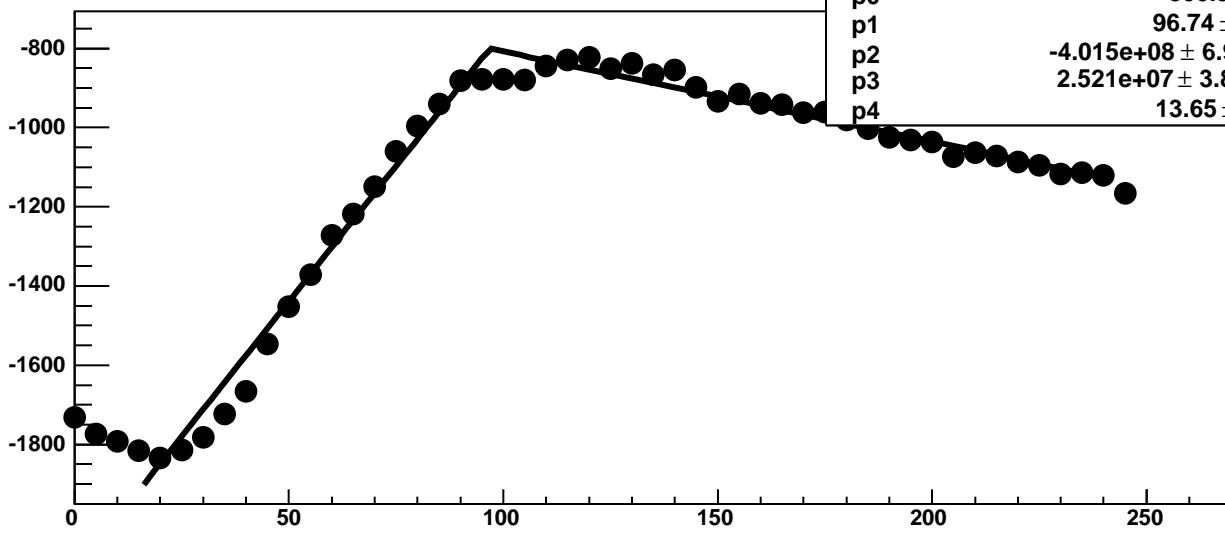
Chip 3, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold

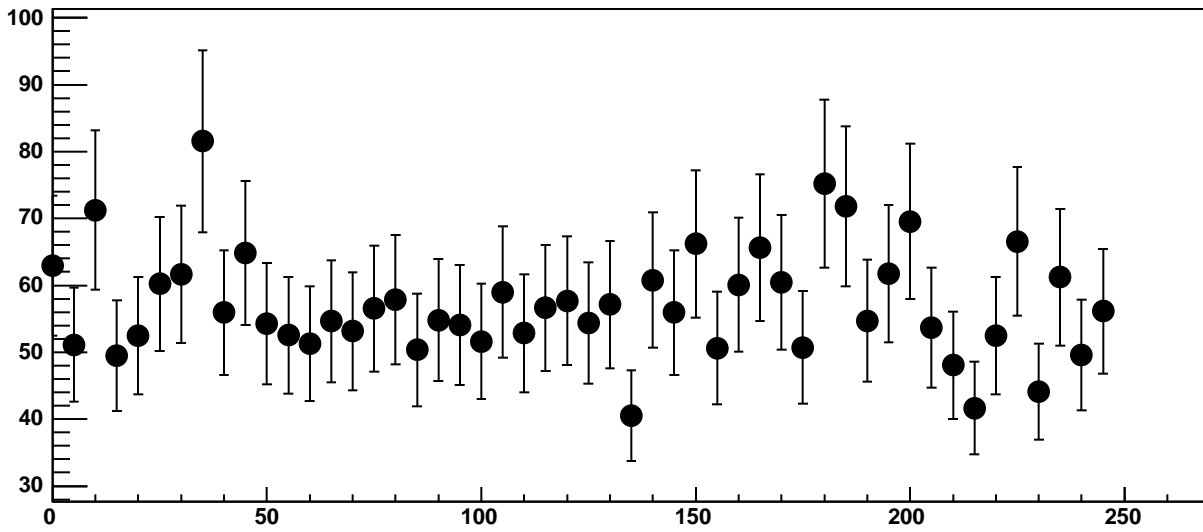


Chip 3, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

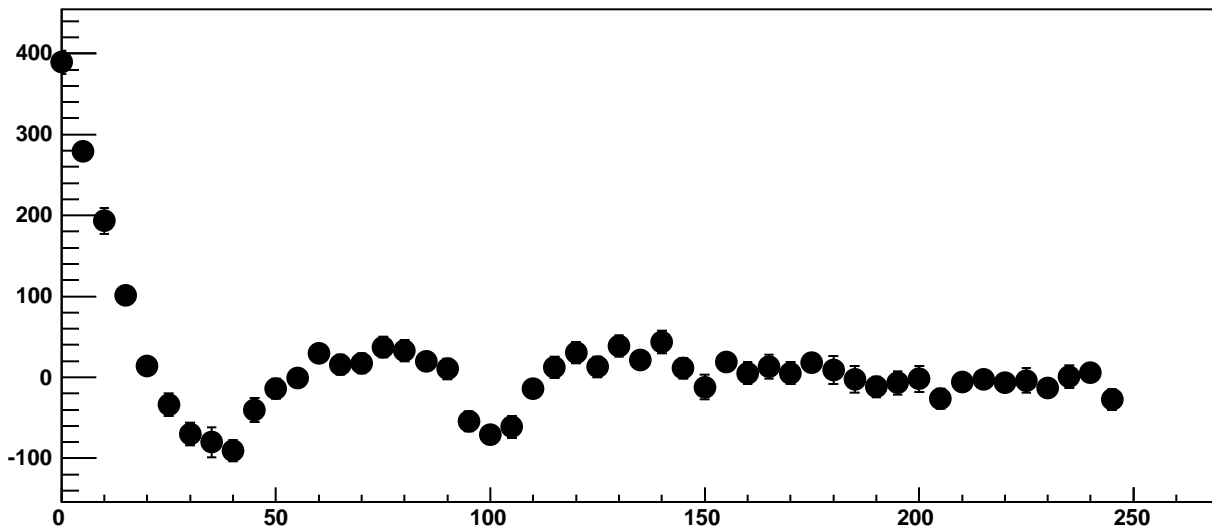


$\chi^2 / \text{ndf}$	340.2 / 41
p0	$-800.5 \pm 4.077$
p1	$96.74 \pm 0.4734$
p2	$-4.015\text{e}+08 \pm 6.927\text{e}+06$
p3	$2.521\text{e}+07 \pm 3.812\text{e}+05$
p4	$13.65 \pm 0.1242$

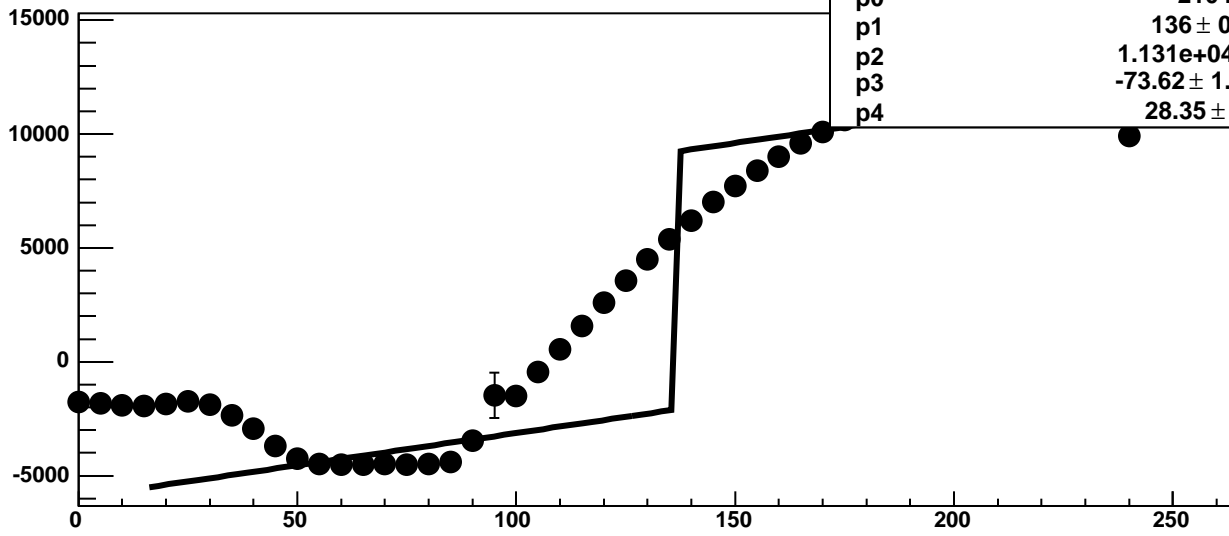
Chip 3, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

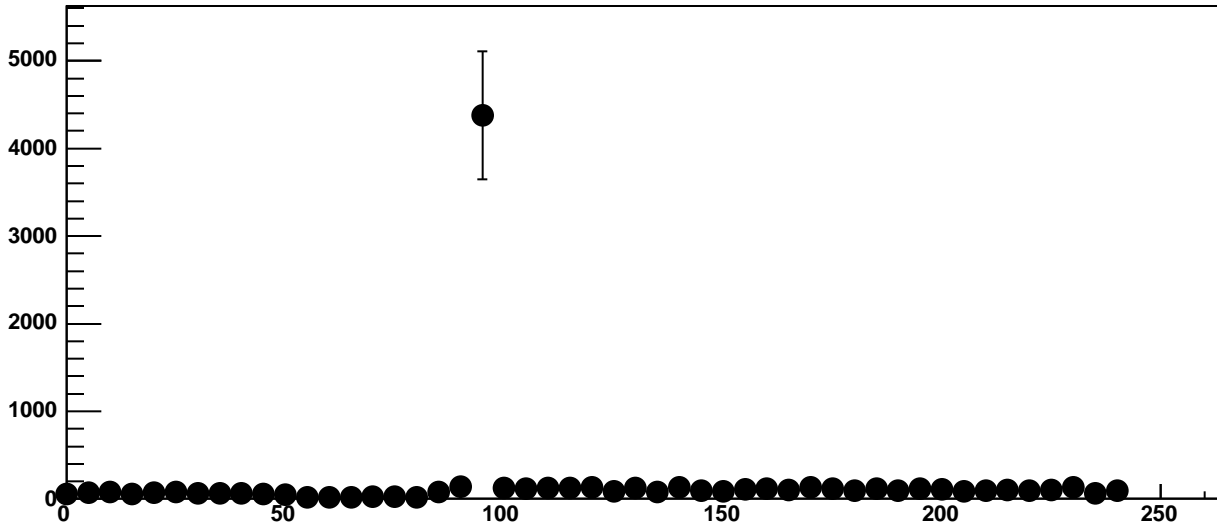


Chip 3, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

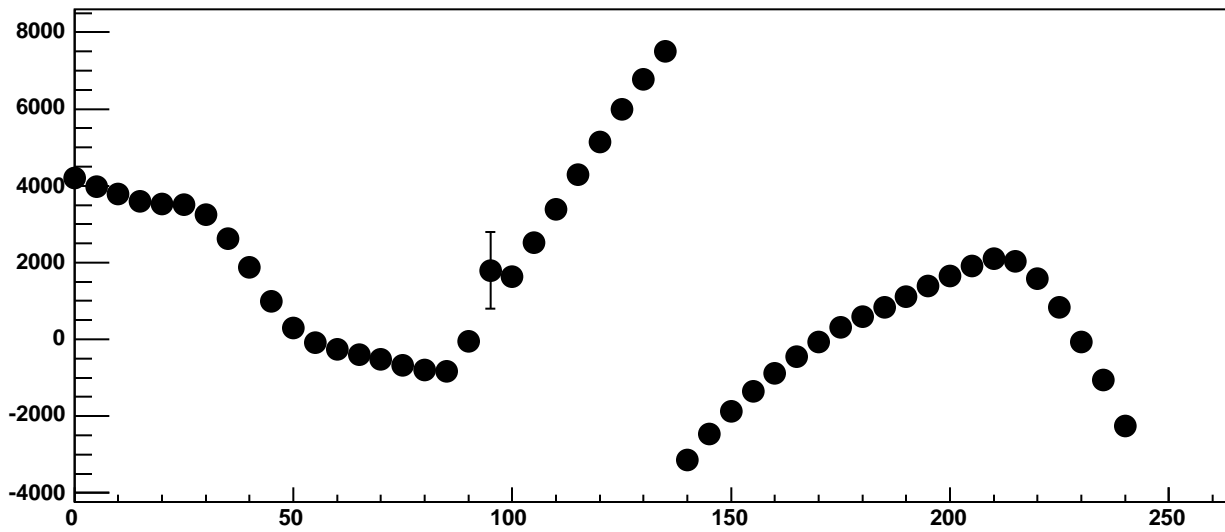


$\chi^2 / \text{ndf}$	8.196e+05 / 41
p0	-2104 ± 5.699
p1	136 ± 0.002379
p2	1.131e+04 ± 11.06
p3	-73.62 ± 1.313e-05
p4	28.35 ± 0.07793

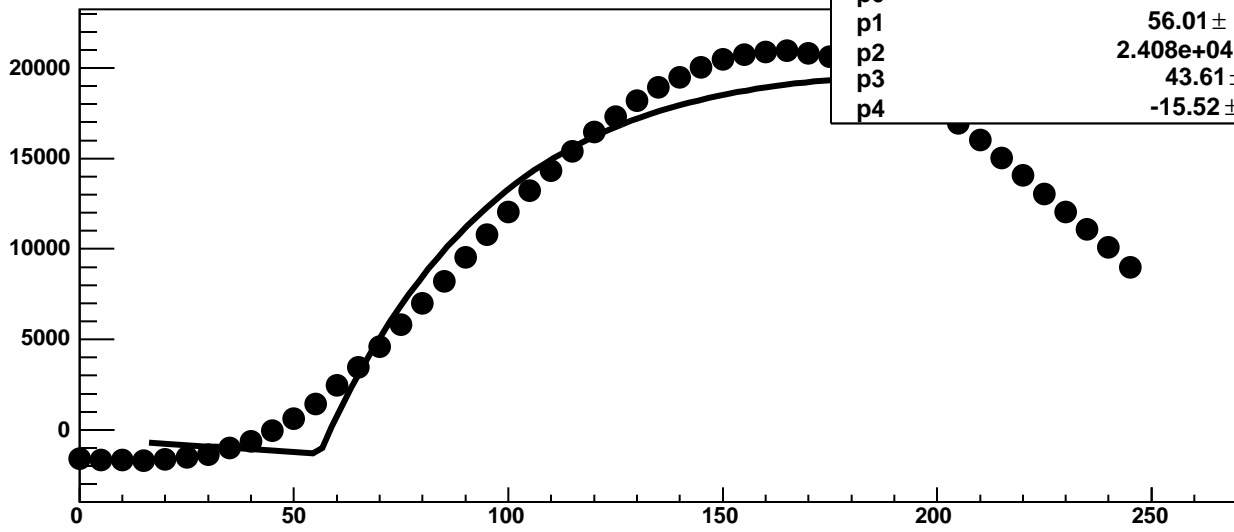
Chip 3, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

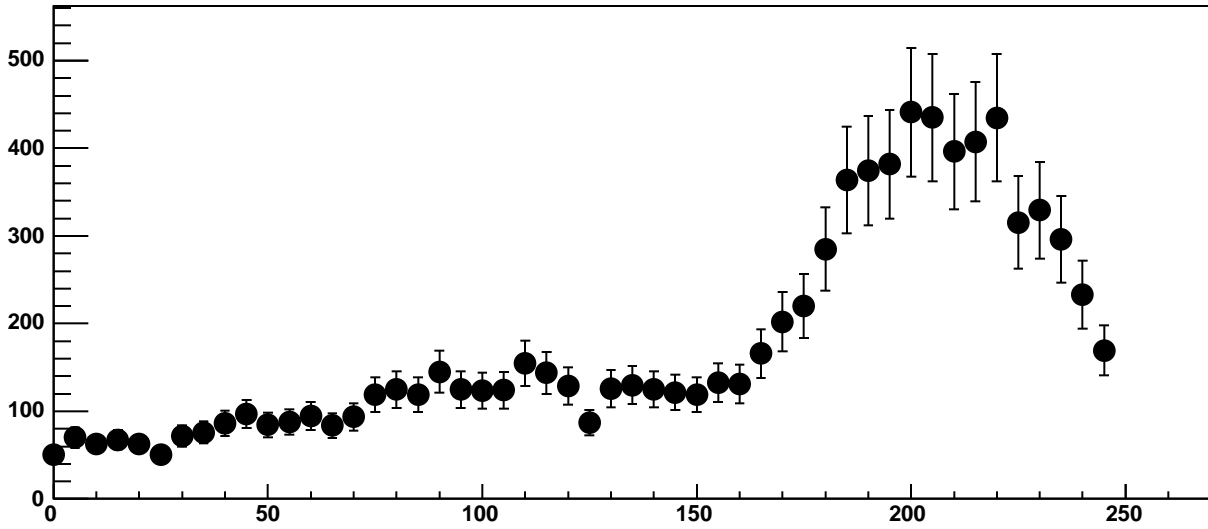


Chip 3, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

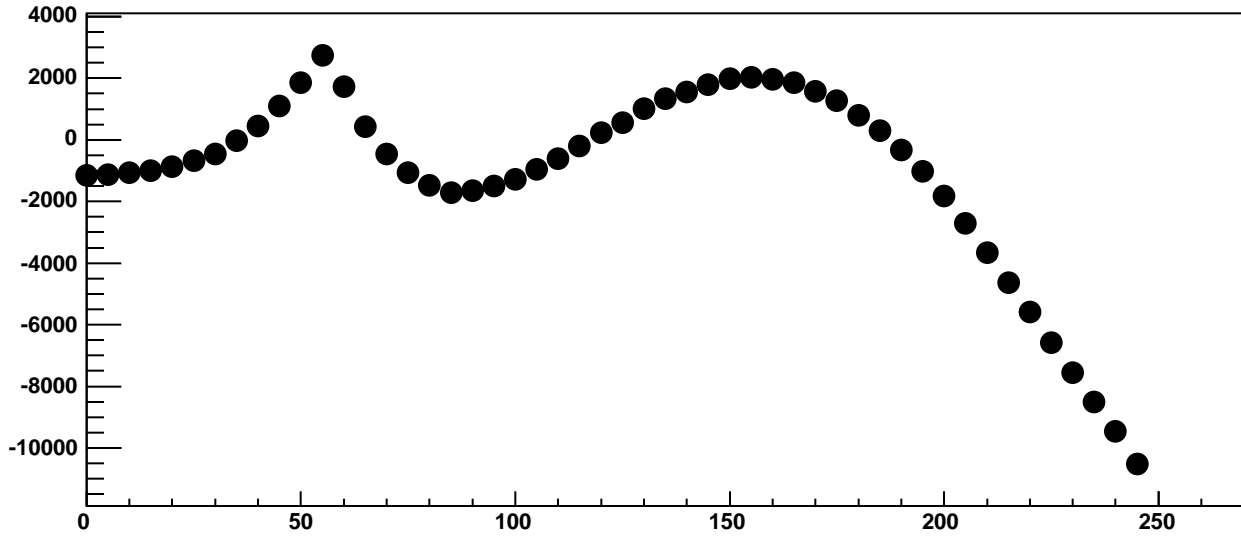


$\chi^2 / \text{ndf}$	1.701e+05 / 41
p0	-1317 ± 9.278
p1	56.01 ± 0.03324
p2	2.408e+04 ± 55.16
p3	43.61 ± 0.1091
p4	-15.52 ± 0.3126

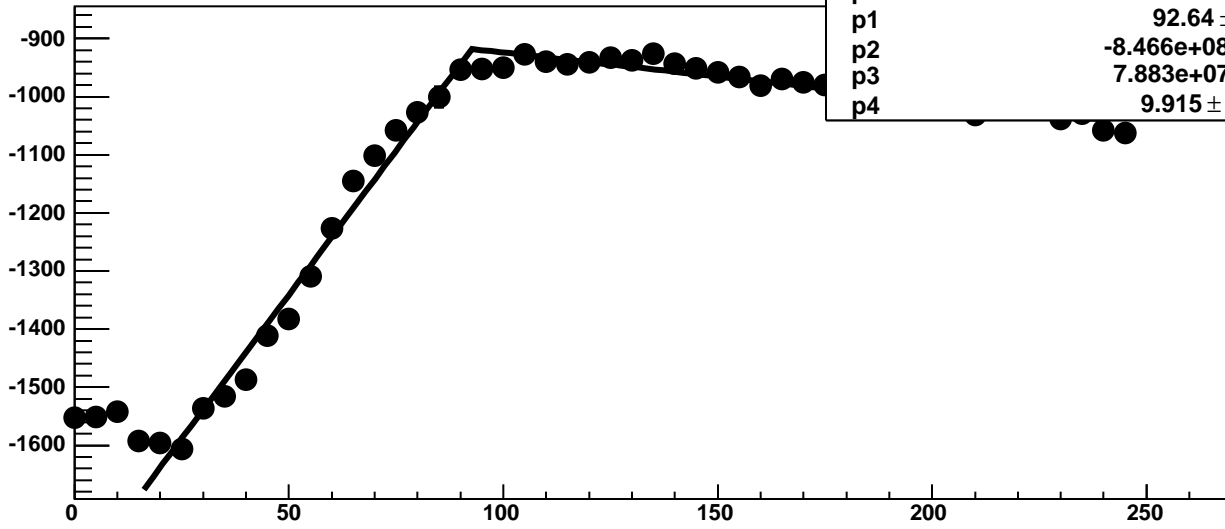
Chip 3, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

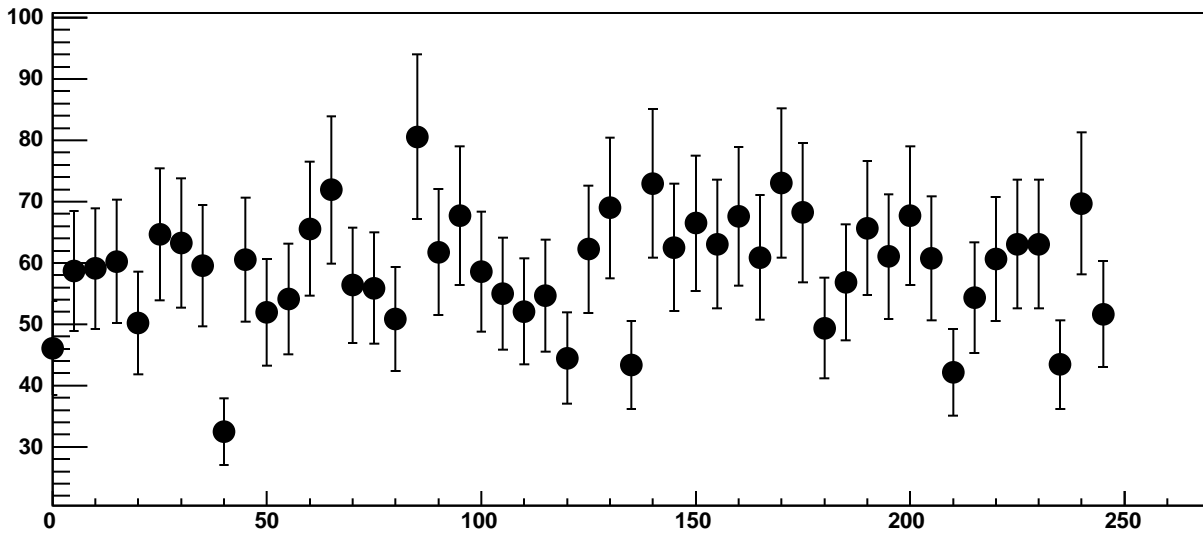


Chip 3, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

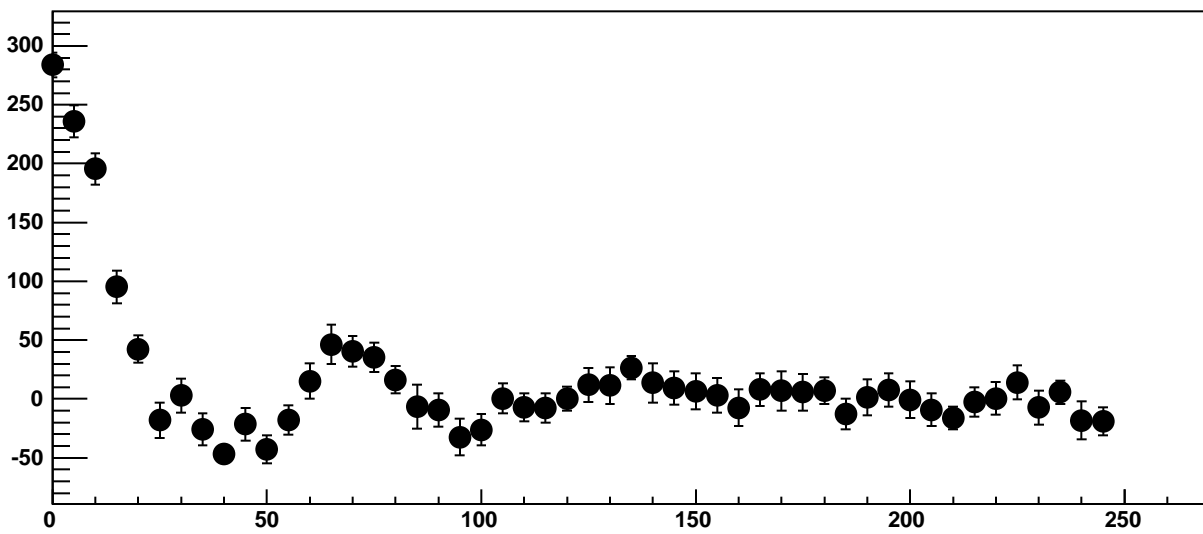


$\chi^2 / \text{ndf}$	179.4 / 41
p0	$-917.9 \pm 1.324$
p1	$92.64 \pm 0.3834$
p2	$-8.466\text{e}+08 \pm 1.414$
p3	$7.883\text{e}+07 \pm 1.414$
p4	$9.915 \pm 0.03123$

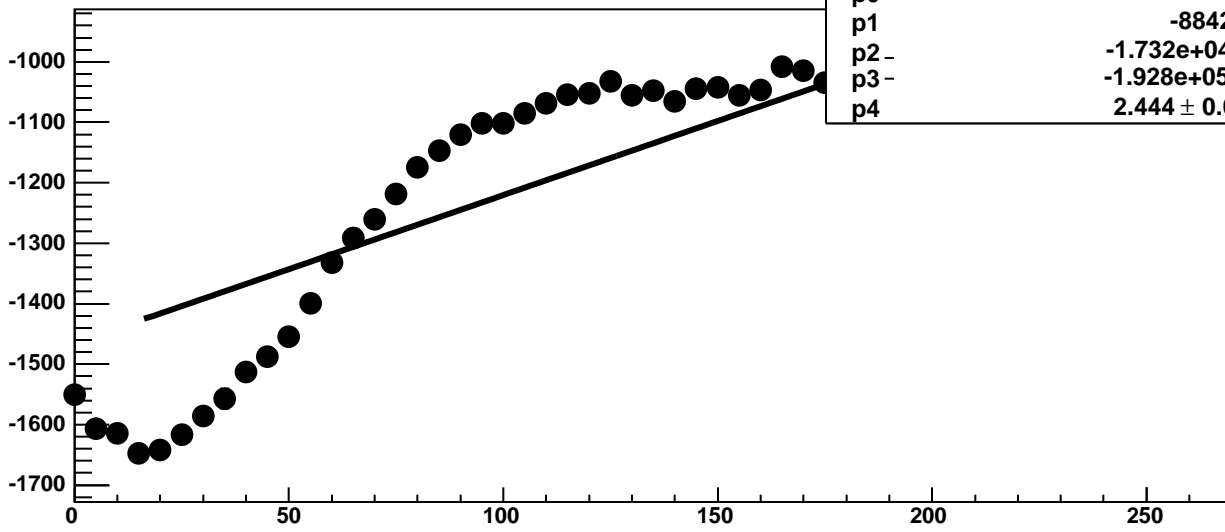
Chip 3, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



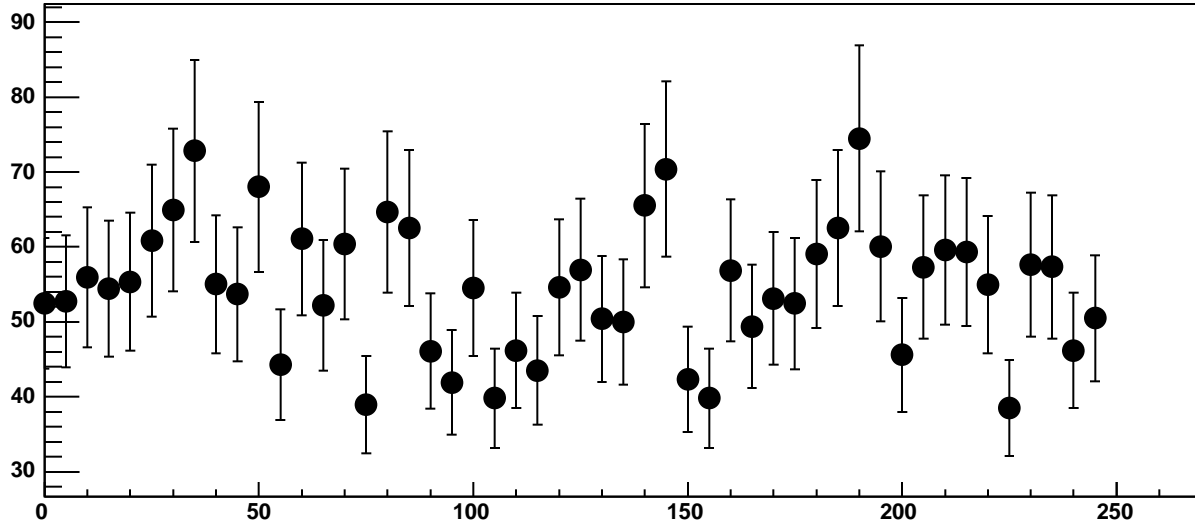
Chip 3, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold



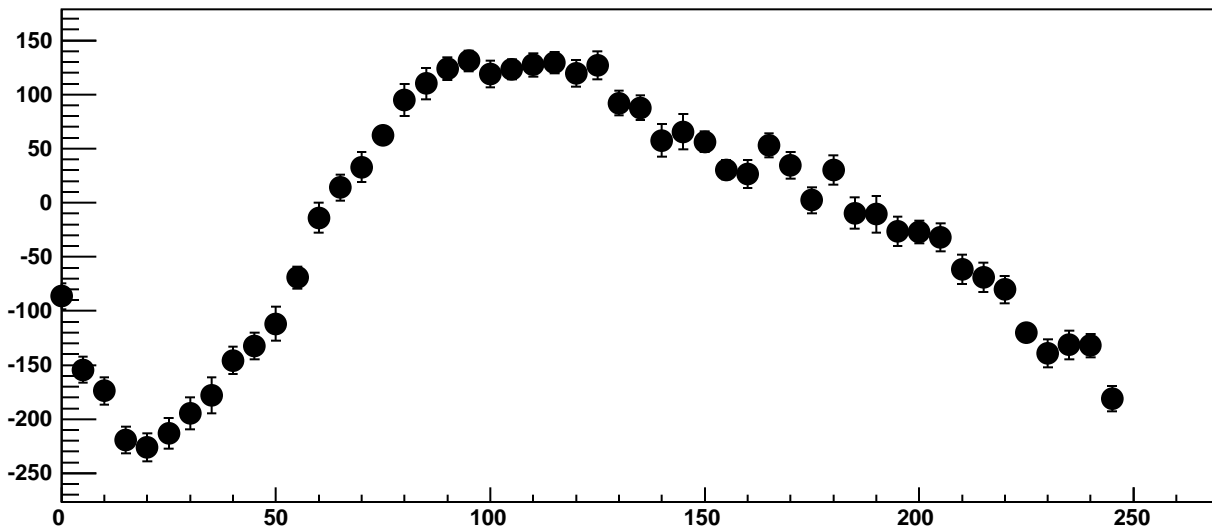
Chip 3, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold



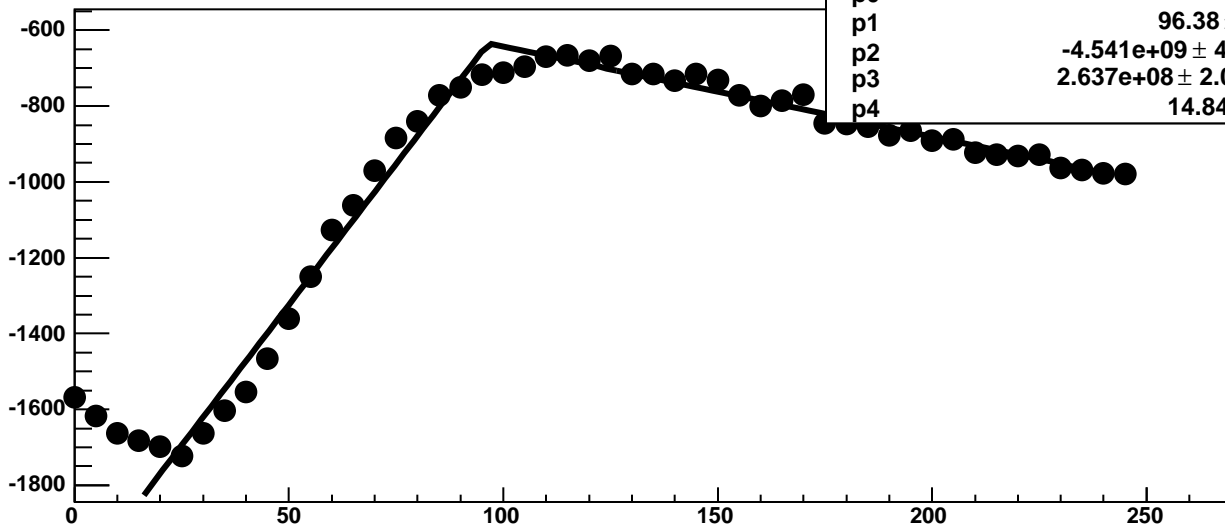
Chip 3, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

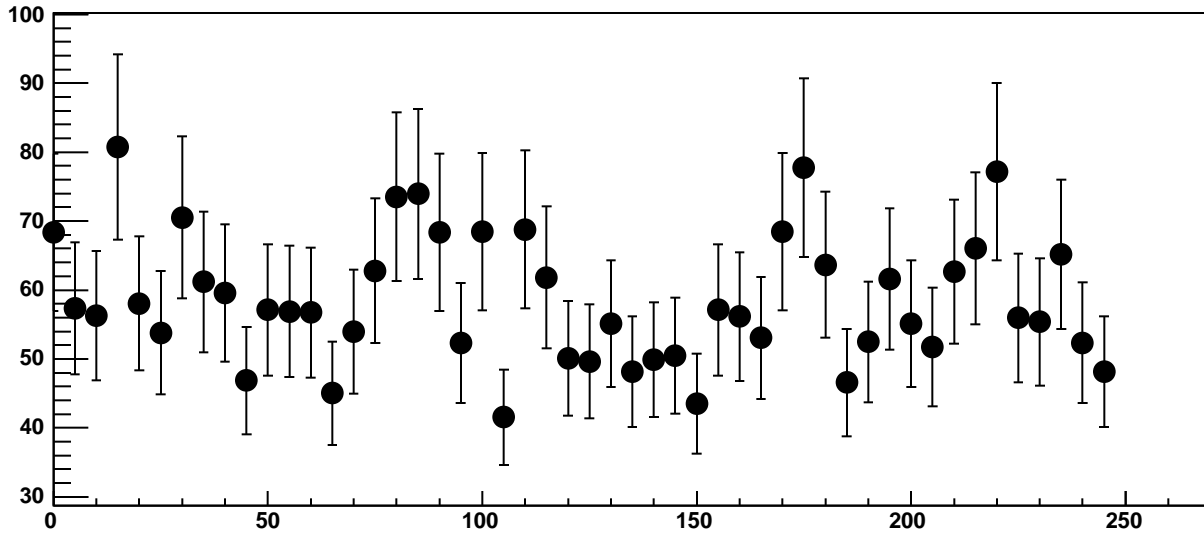


Chip 3, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

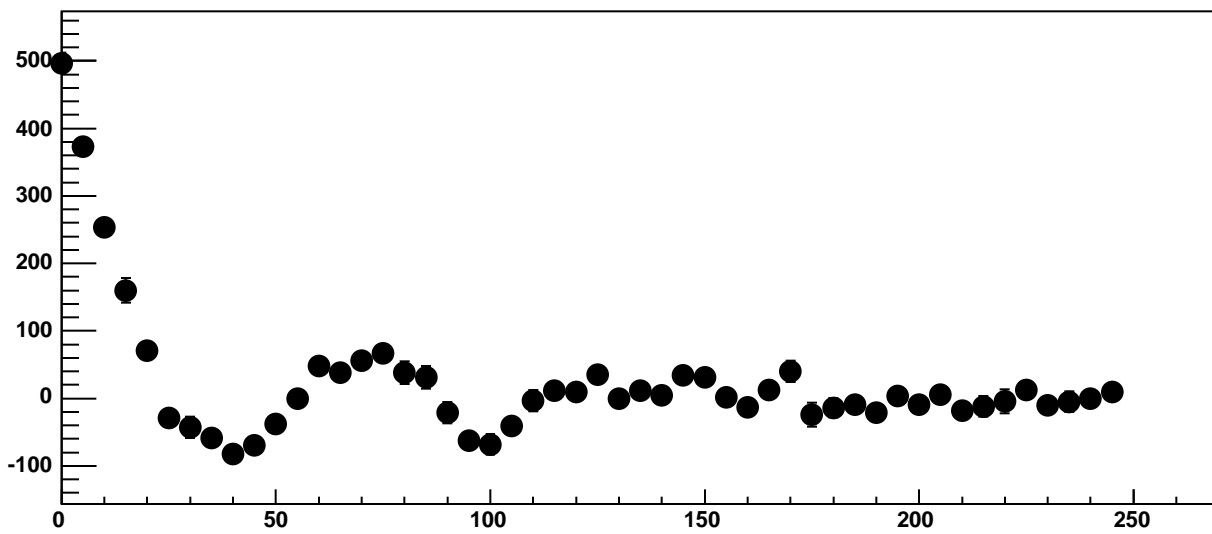


$\chi^2 / \text{ndf}$	414.4 / 41
p0	$-634.5 \pm 4.136$
p1	$96.38 \pm 0.4751$
p2	$-4.541\text{e}+09 \pm 4.03\text{e}+07$
p3	$2.637\text{e}+08 \pm 2.094\text{e}+05$
p4	$14.84 \pm 0.142$

Chip 3, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

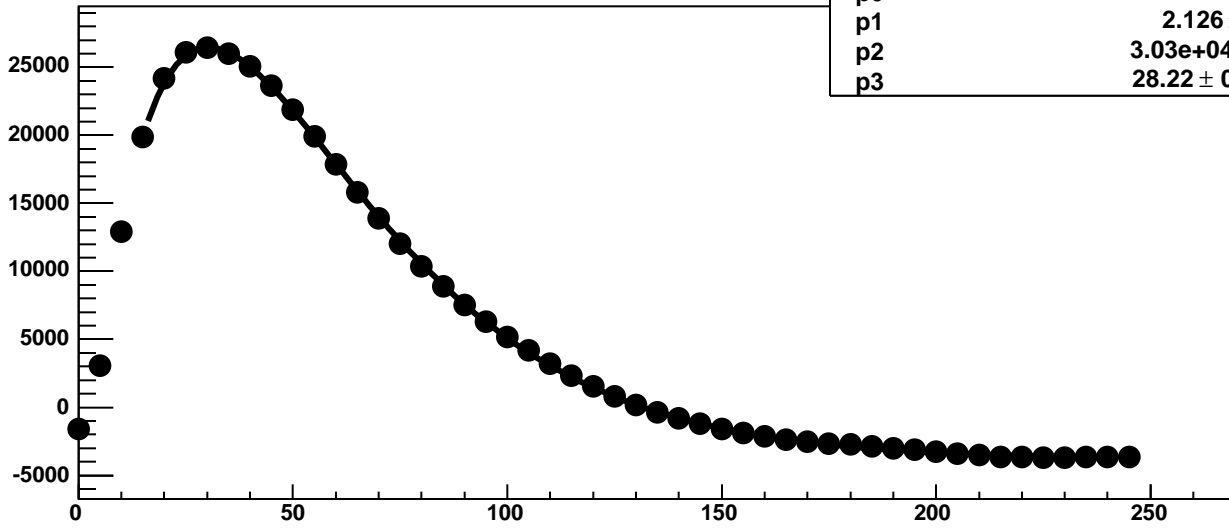


Chip 3, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



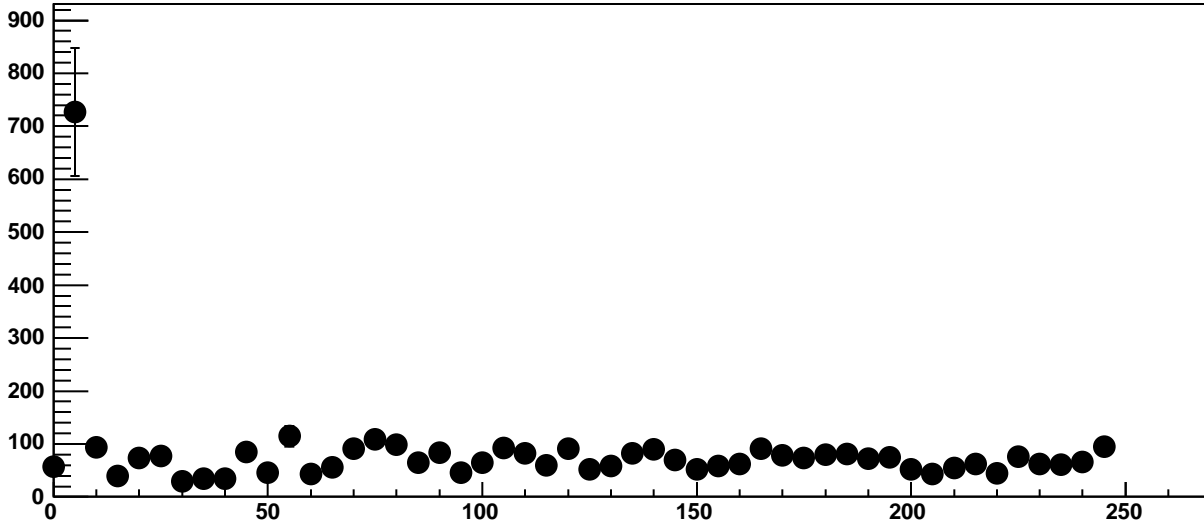


Chip 3, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold

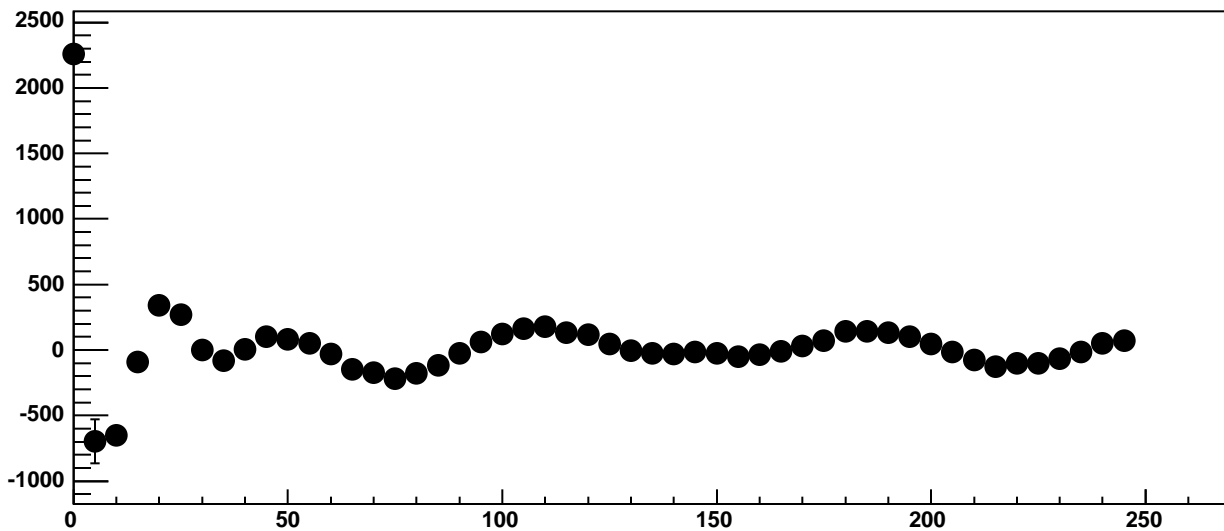


$\chi^2 / \text{ndf}$	2313 / 42
p0	-3833 ± 3.814
p1	2.126 ± 0.0121
p2	3.03e+04 ± 4.924
p3	28.22 ± 0.009952

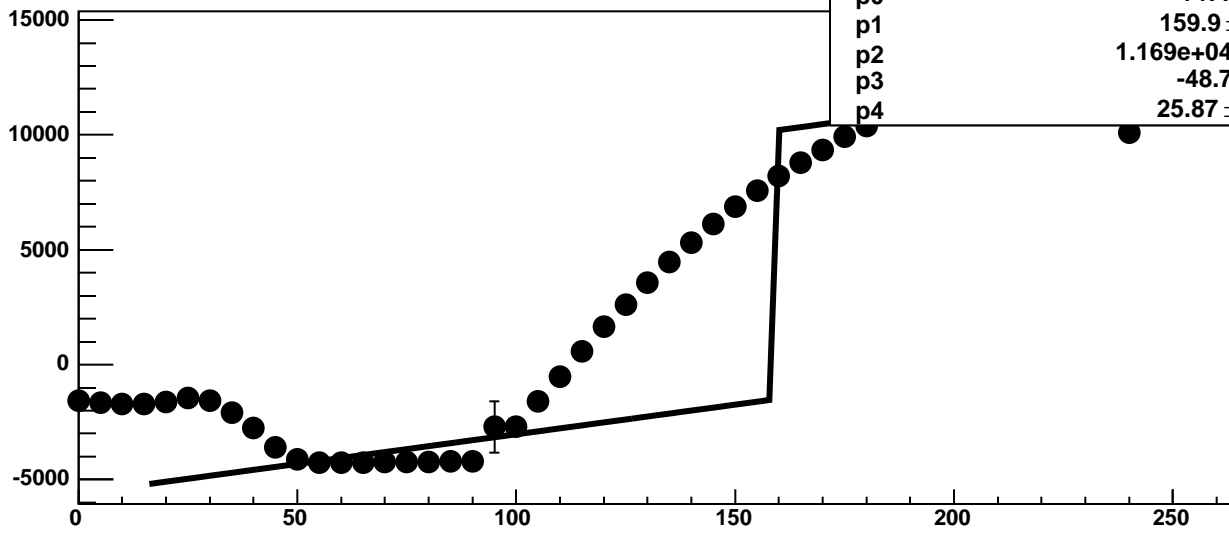
Chip 3, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



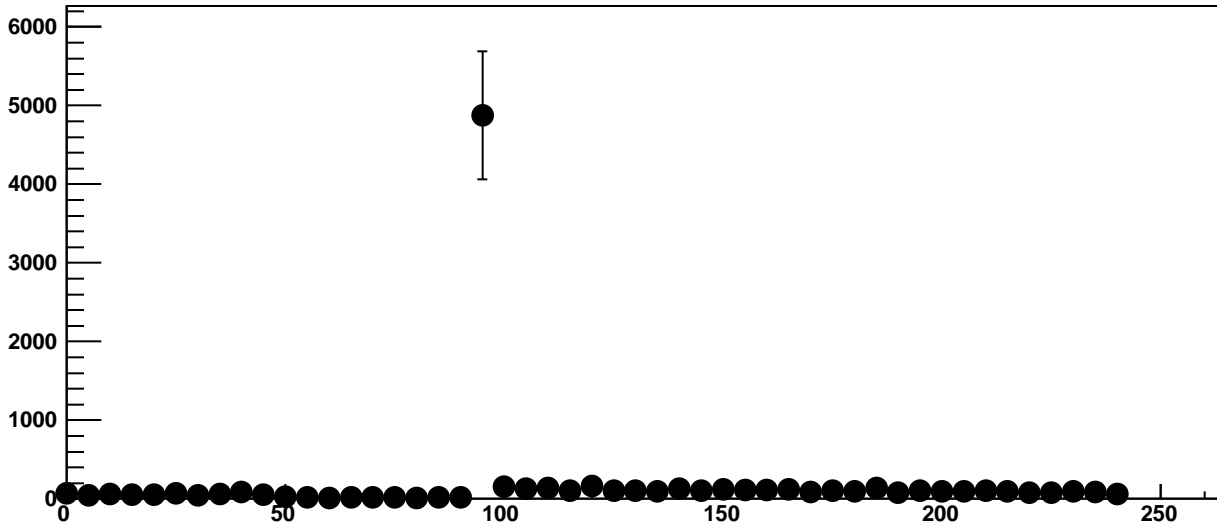
Chip 3, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold



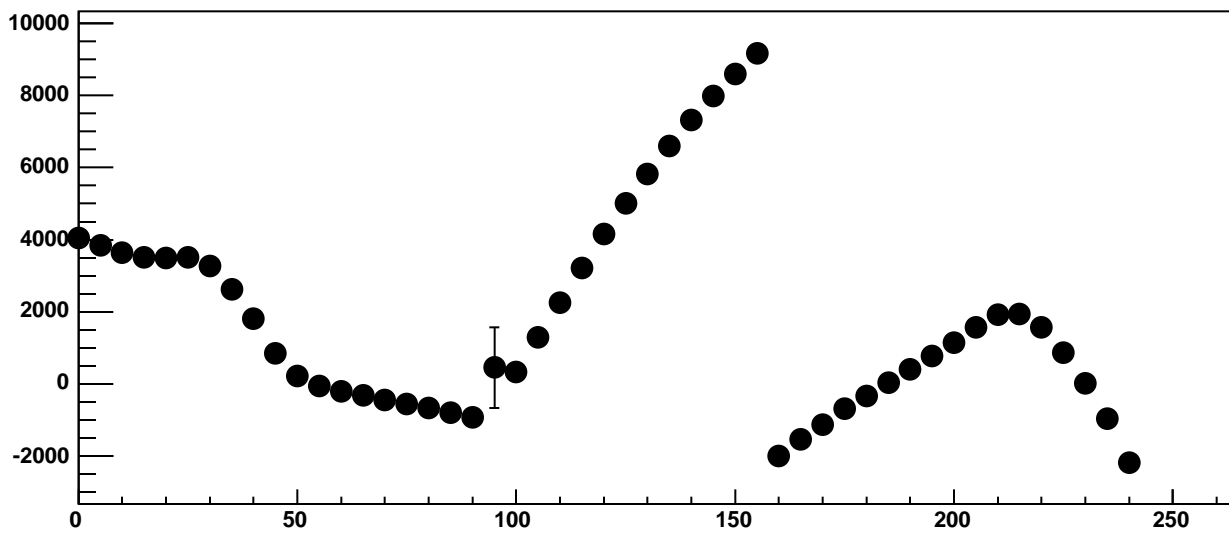
Chip 3, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold



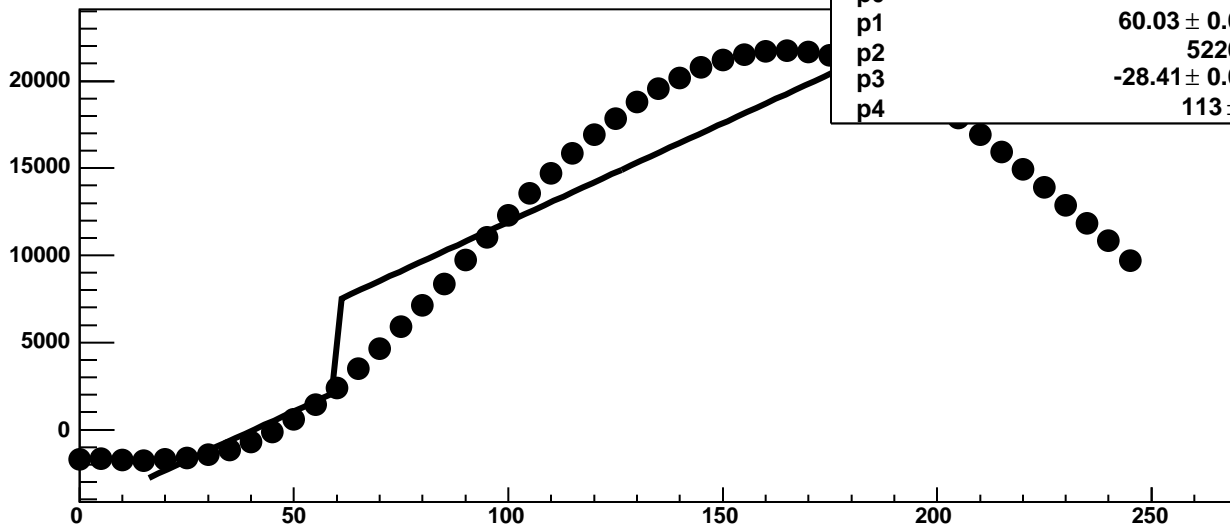
Chip 3, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

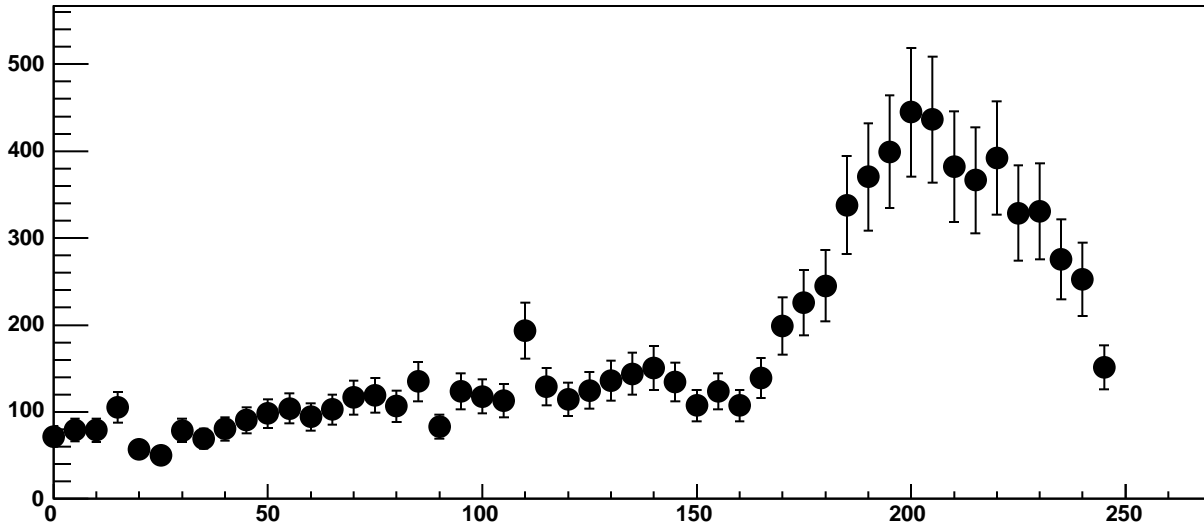


Chip 3, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

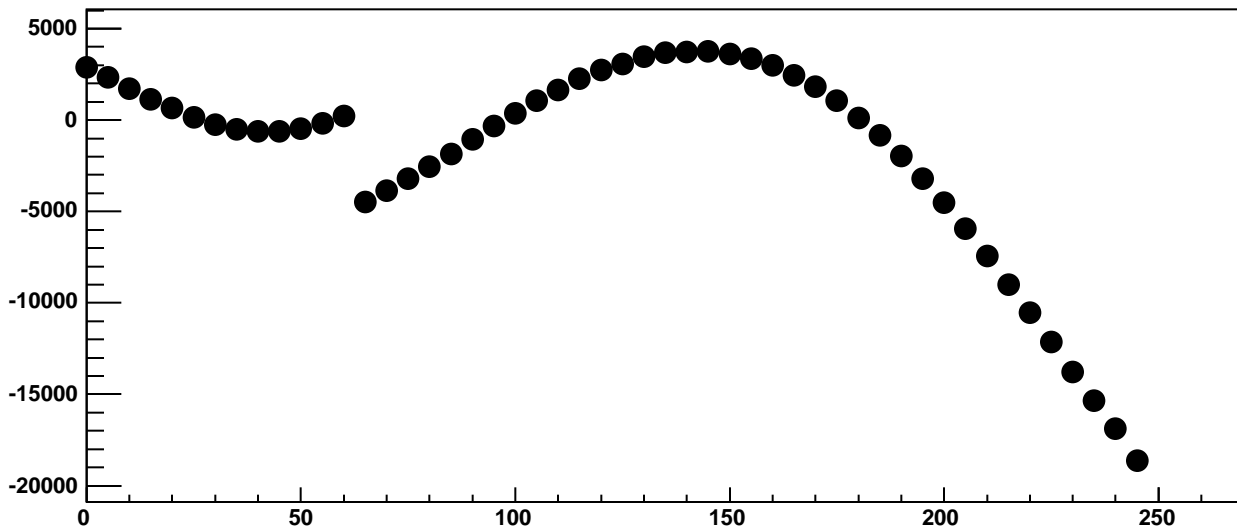


$\chi^2 / \text{ndf}$	4.803e+05 / 41
p0	2189 ± 7.496
p1	60.03 ± 0.0001002
p2	5220 ± 14.6
p3	-28.41 ± 0.0001315
p4	113 ± 0.1193

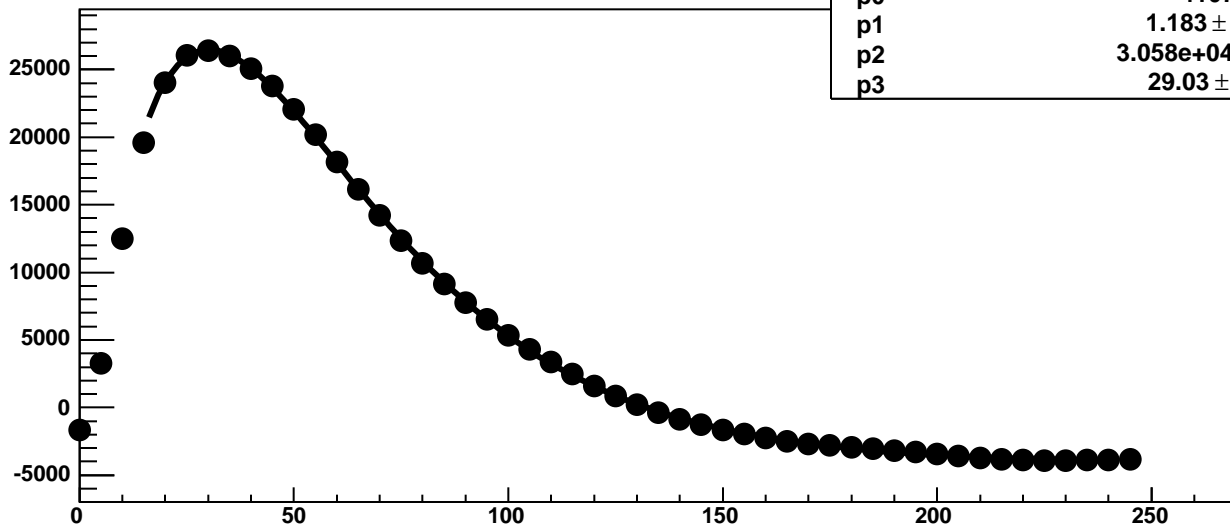
Chip 3, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

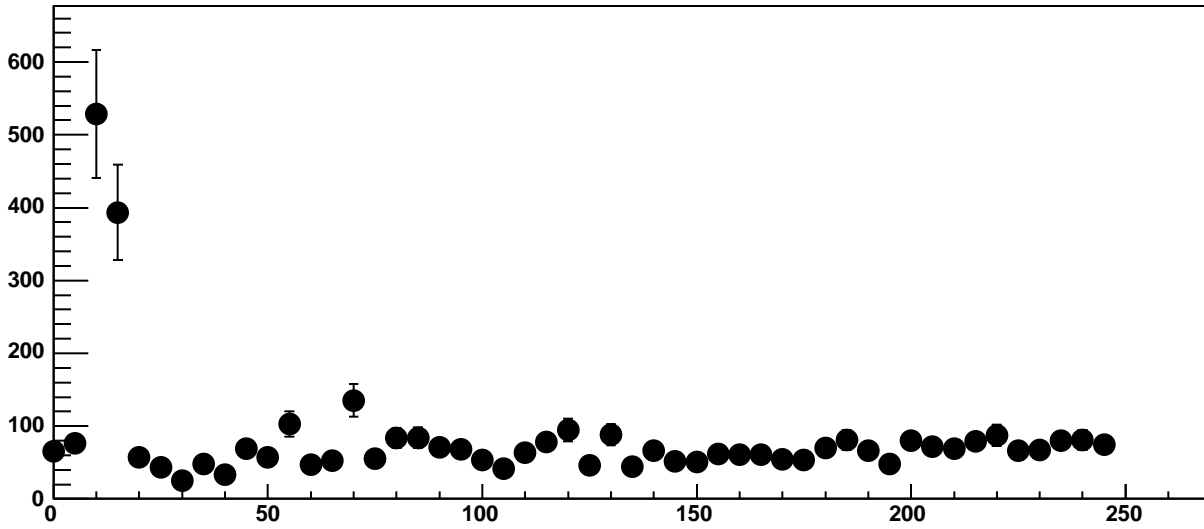


Chip 3, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold

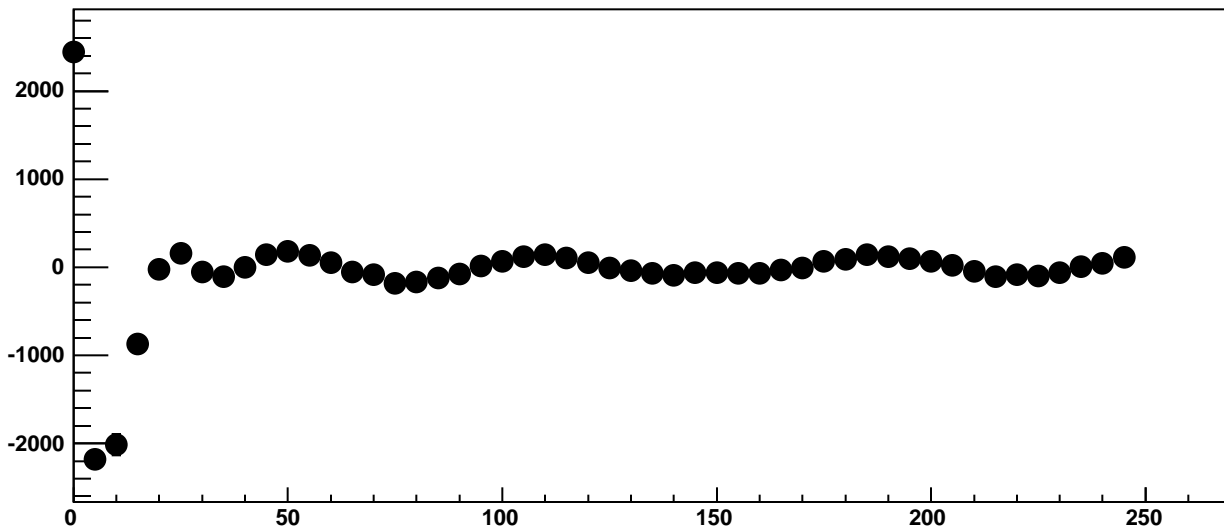


$\chi^2 / \text{ndf}$	2162 / 42
p0	-4107 ± 4.447
p1	1.183 ± 0.02403
p2	3.058e+04 ± 5.296
p3	29.03 ± 0.01321

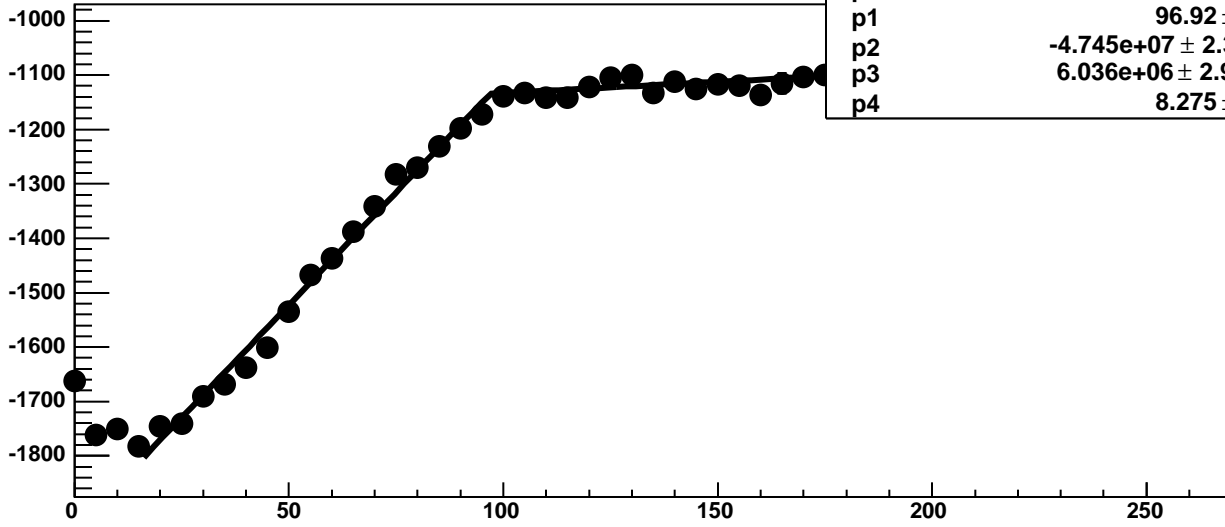
Chip 3, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold

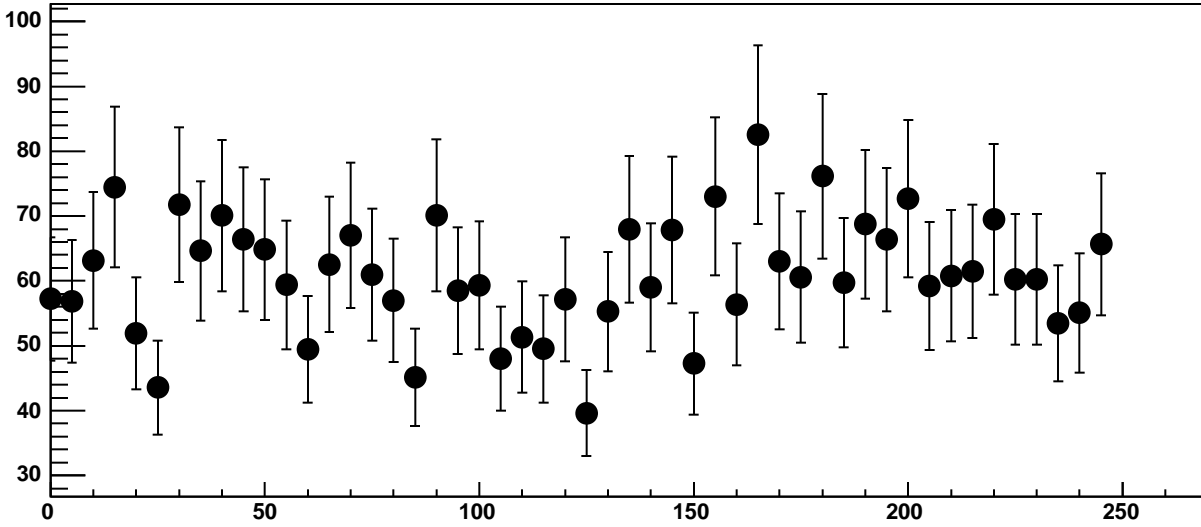


Chip 3, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

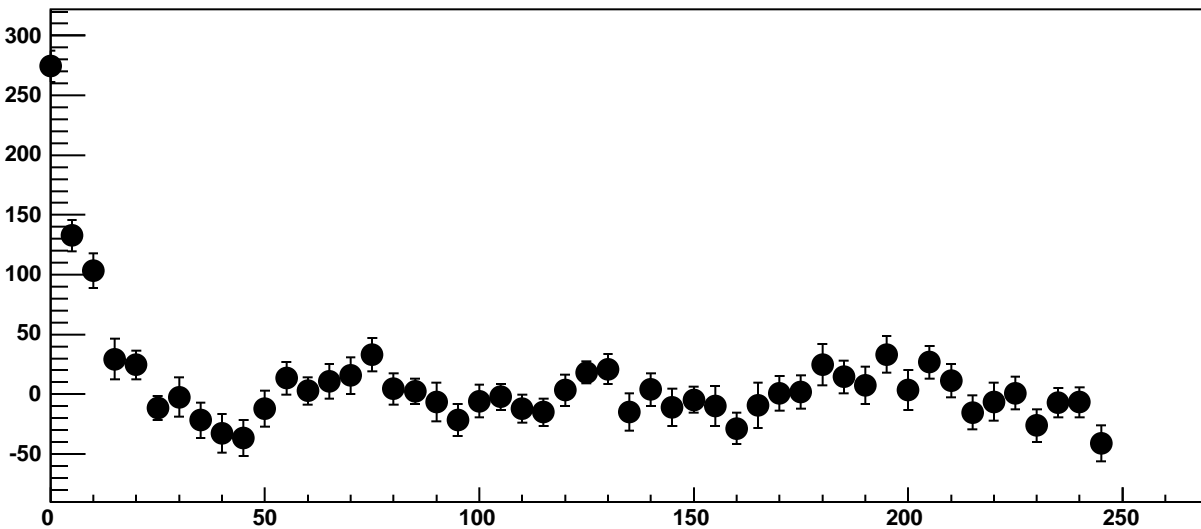


$\chi^2 / \text{ndf}$	67.6 / 41
p0	-1134 ± 4.766
p1	96.92 ± 0.9623
p2	-4.745e+07 ± 2.317e+06
p3	6.036e+06 ± 2.956e+05
p4	8.275 ± 0.1242

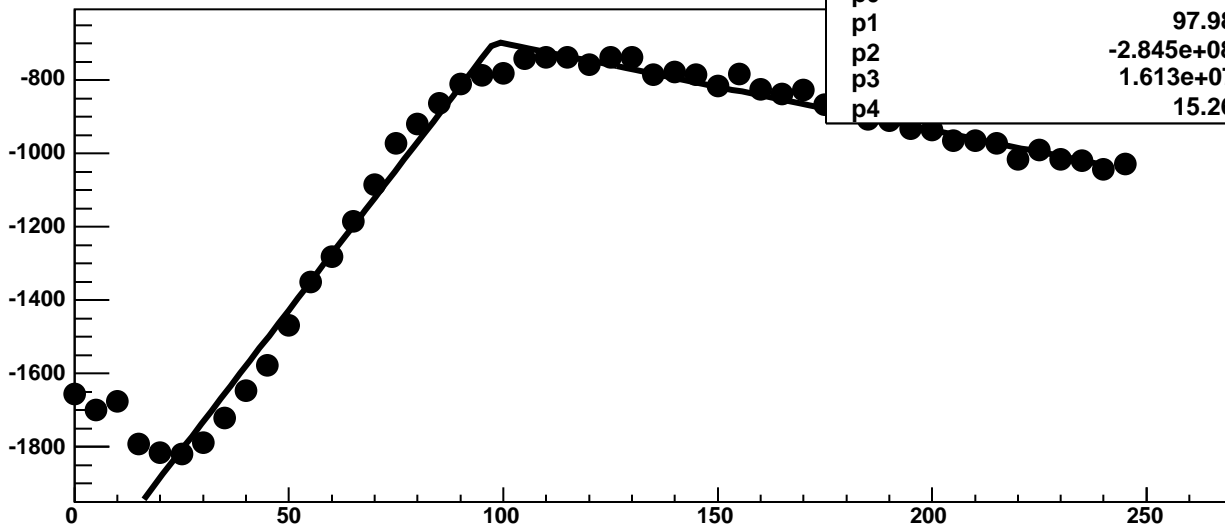
Chip 3, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

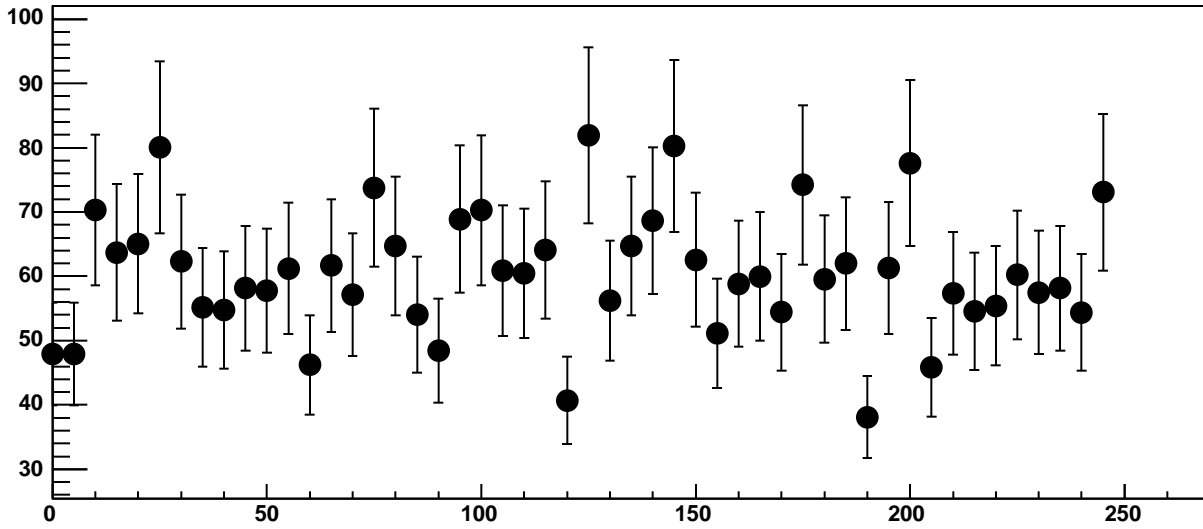


Chip 3, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

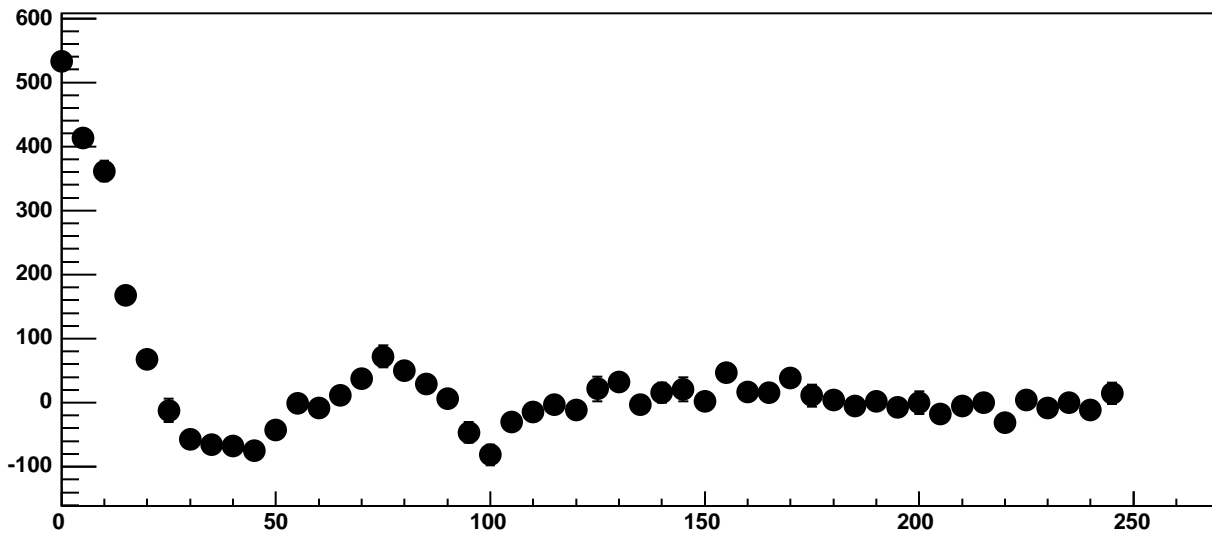


$\chi^2 / \text{ndf}$	403.4 / 41
p0	-694.2 ± nan
p1	97.98 ± nan
p2	-2.845e+08 ± nan
p3	1.613e+07 ± nan
p4	15.26 ± nan

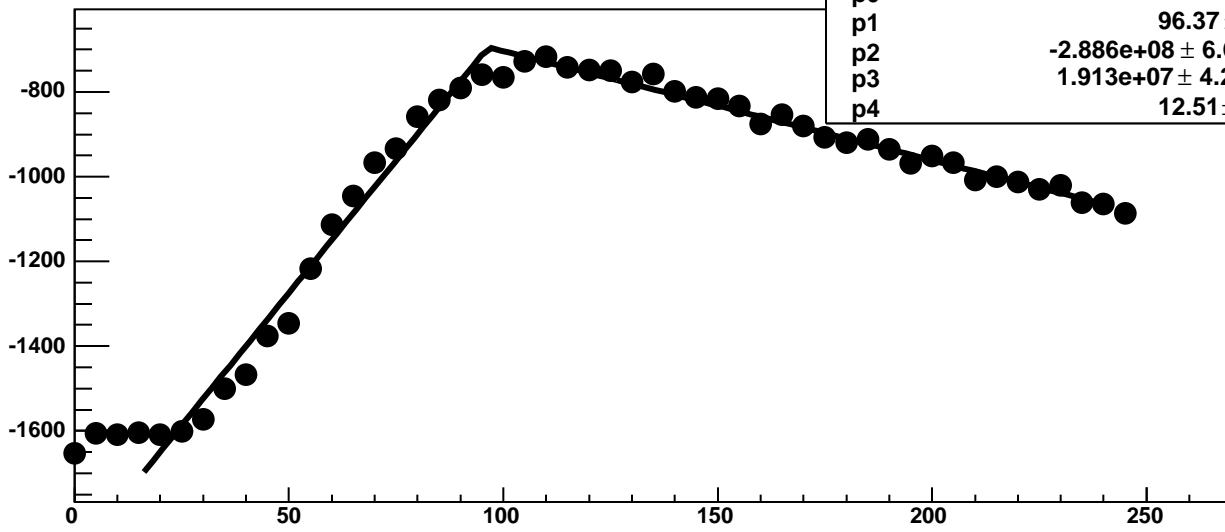
Chip 3, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



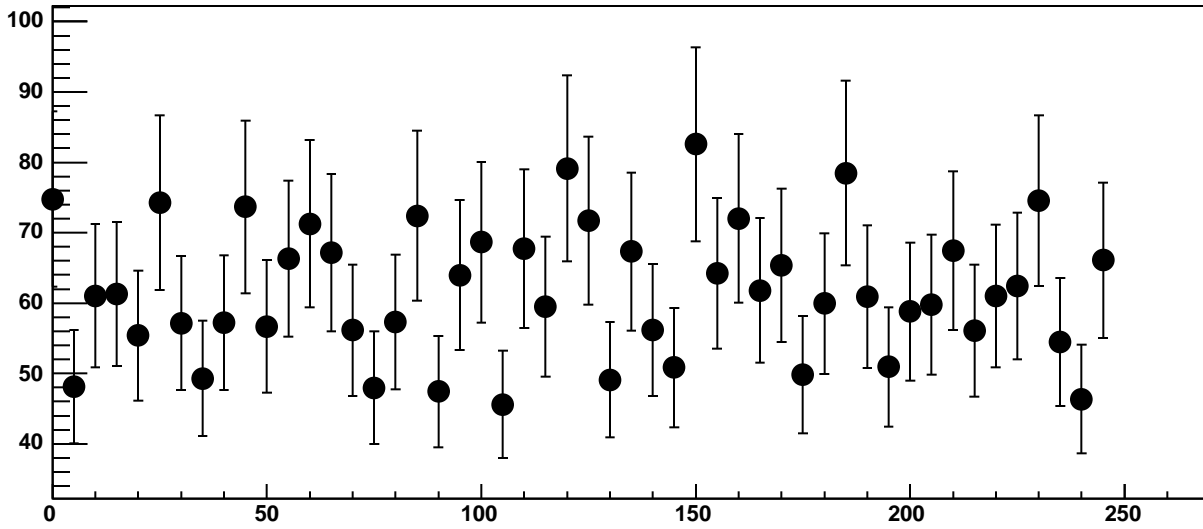
Chip 3, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold



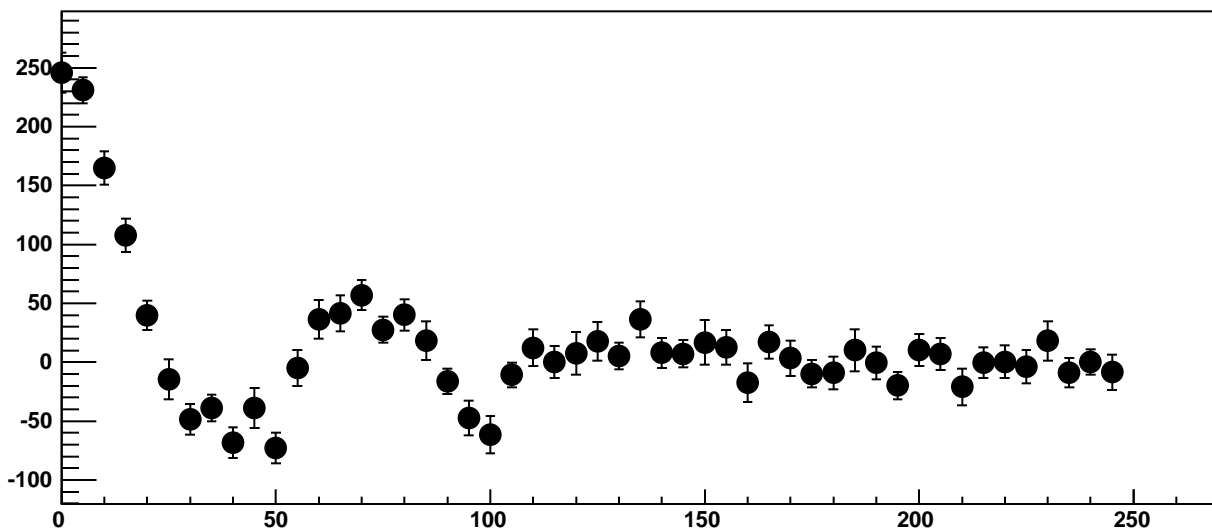
Chip 3, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold



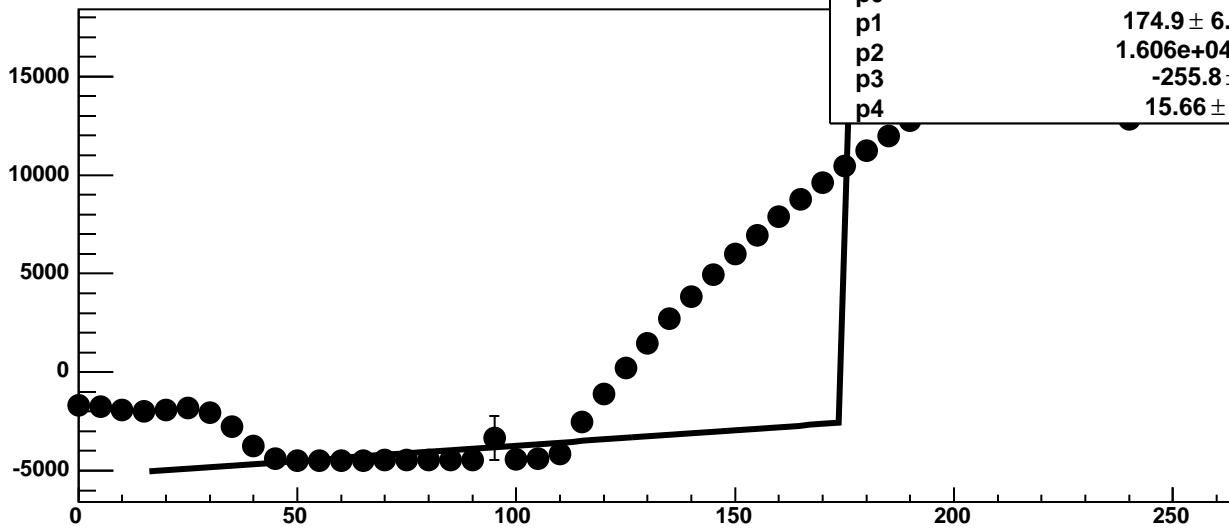
Chip 3, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold

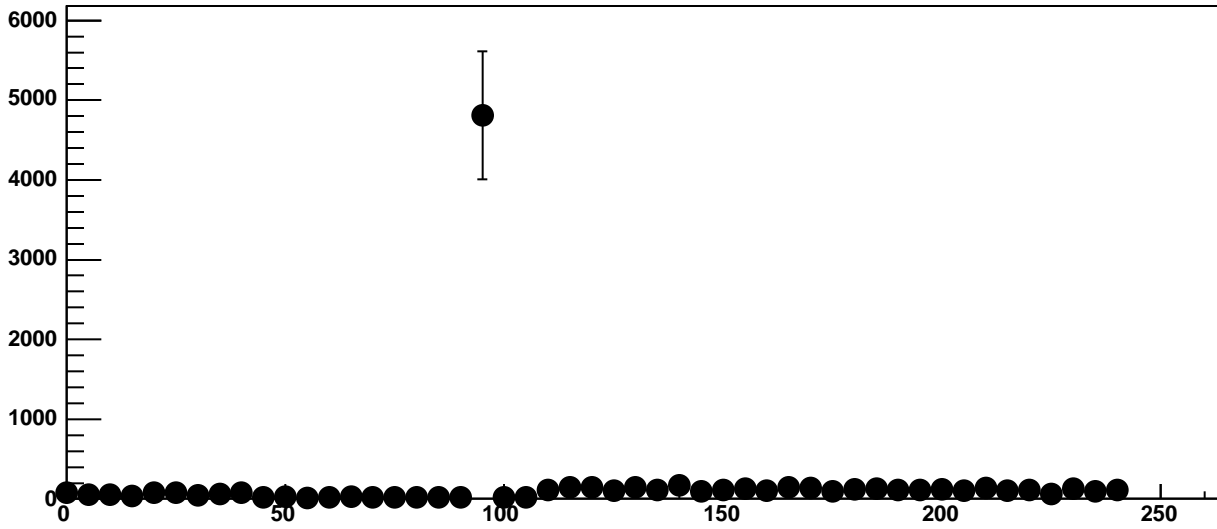


Chip 3, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

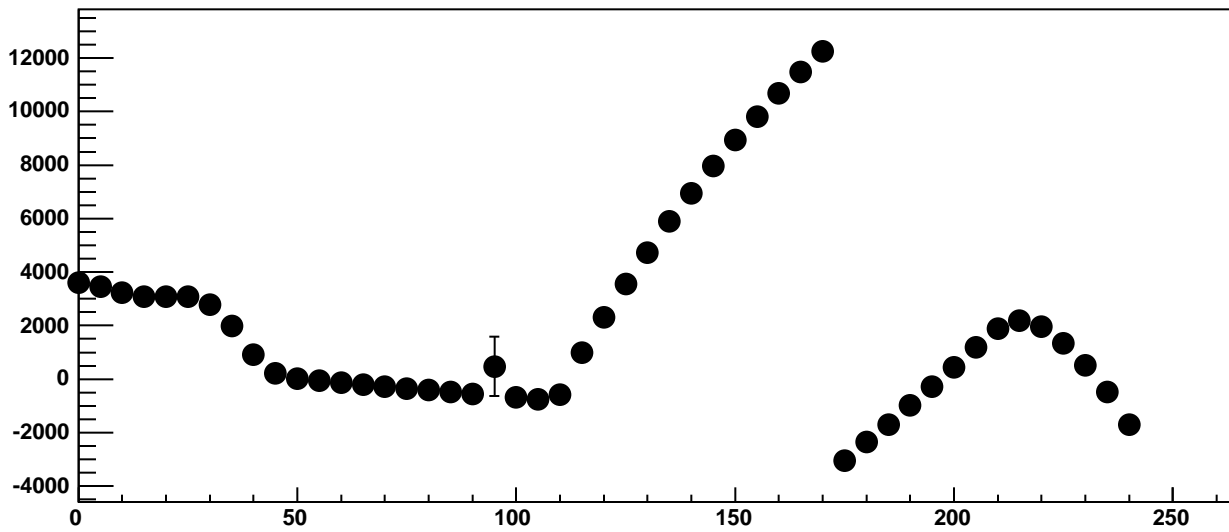


$\chi^2 / \text{ndf}$	1.379e+06 / 41
p0	-2556 ± 4.517
p1	174.9 ± 6.904e-05
p2	1.606e+04 ± 10.37
p3	-255.8 ± 0.1898
p4	15.66 ± 0.04326

Chip 3, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

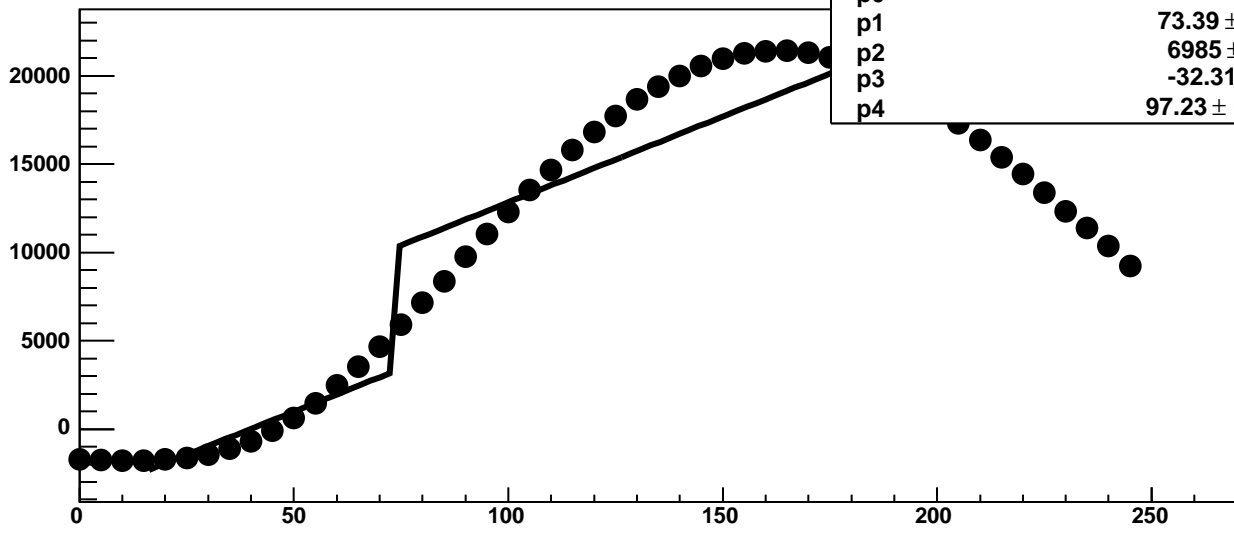


Chip 3, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold

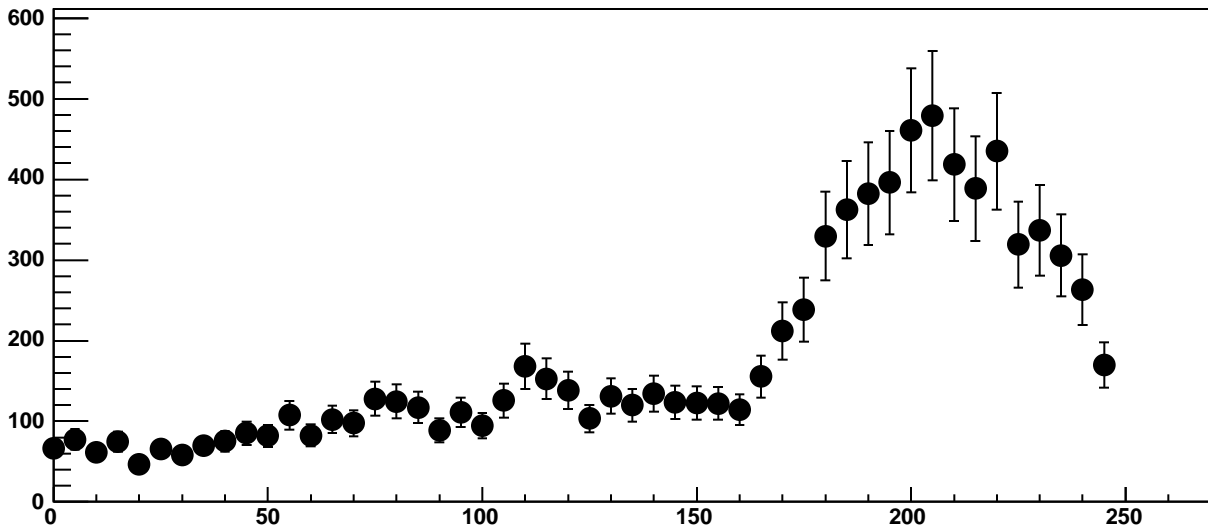




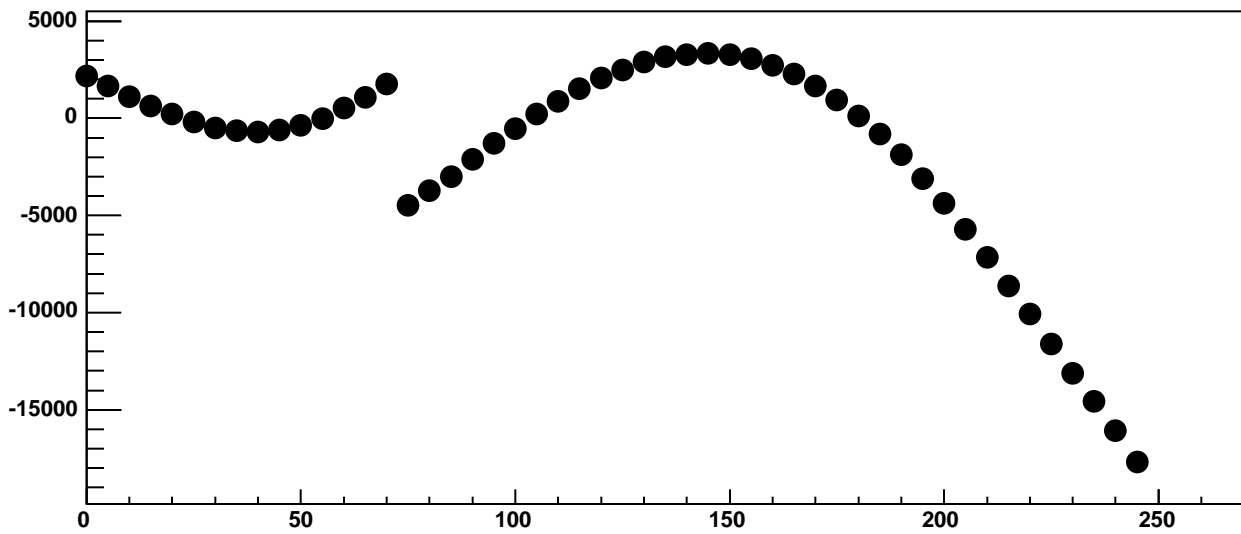
Chip 3, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold



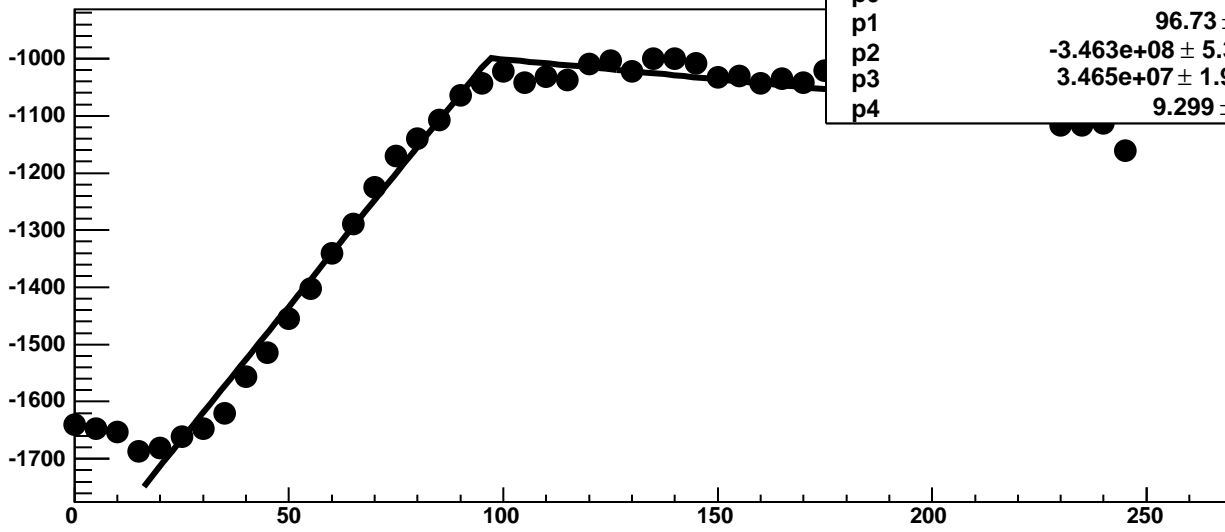
Chip 3, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

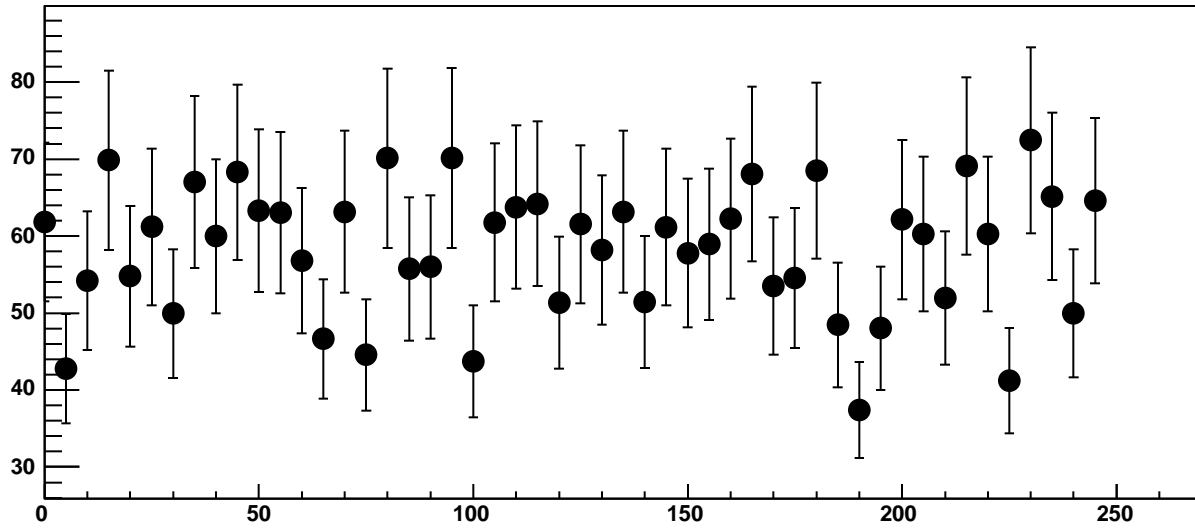


Chip 3, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

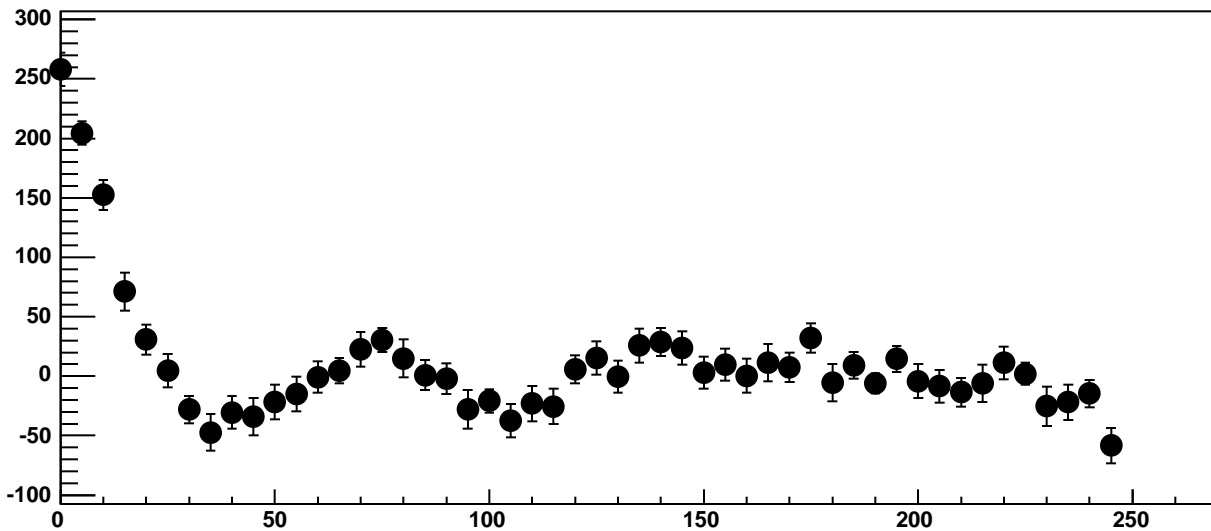


$\chi^2 / \text{ndf}$	120.1 / 41
p0	-998.8 ± 4.498
p1	96.73 ± 0.8019
p2	-3.463e+08 ± 5.323e+06
p3	3.465e+07 ± 1.983e+05
p4	9.299 ± 0.1355

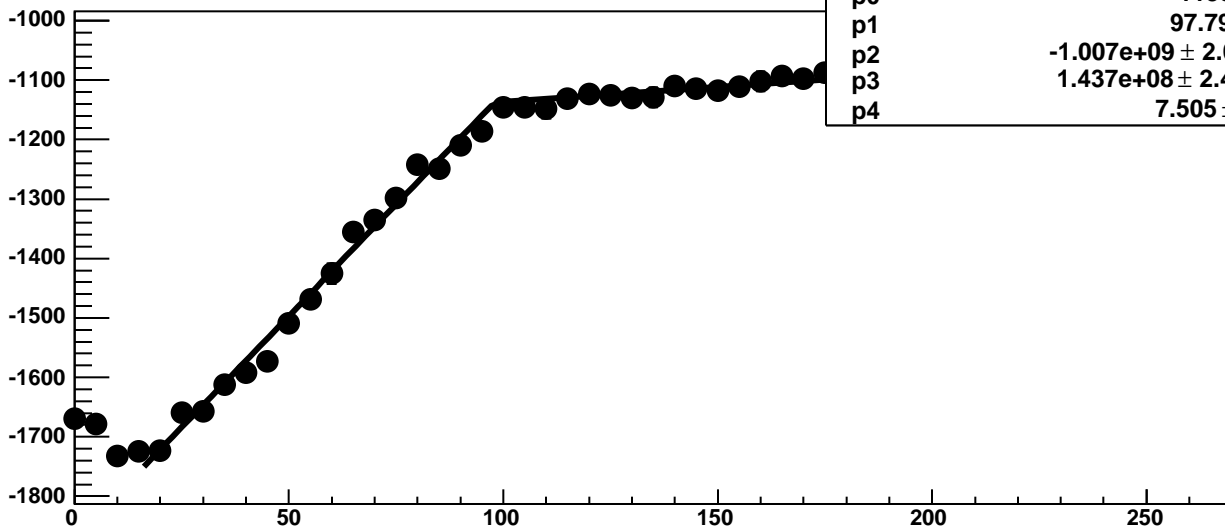
Chip 3, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold

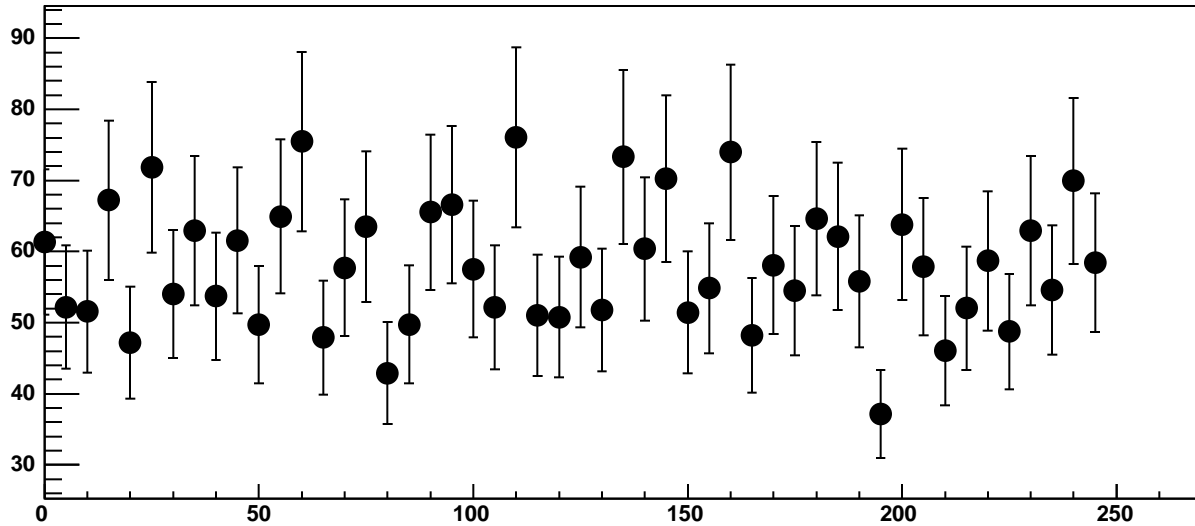


Chip 3, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

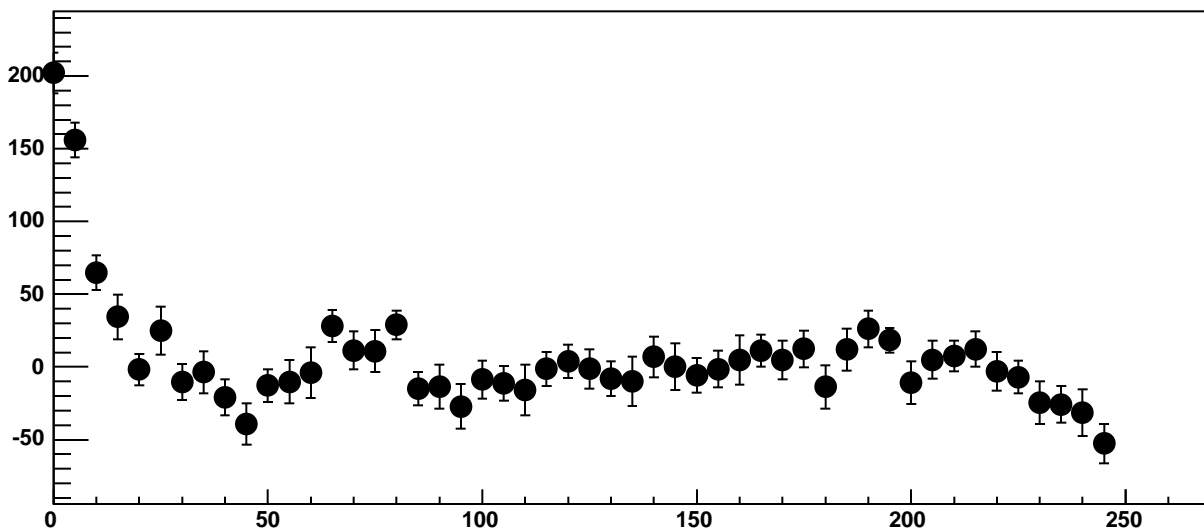


$\chi^2 / \text{ndf}$	72.4 / 41
p0	-1138 ± 5.231
p1	97.79 ± 1.141
p2	-1.007e+09 ± 2.061e+07
p3	1.437e+08 ± 2.472e+05
p4	7.505 ± 0.1309

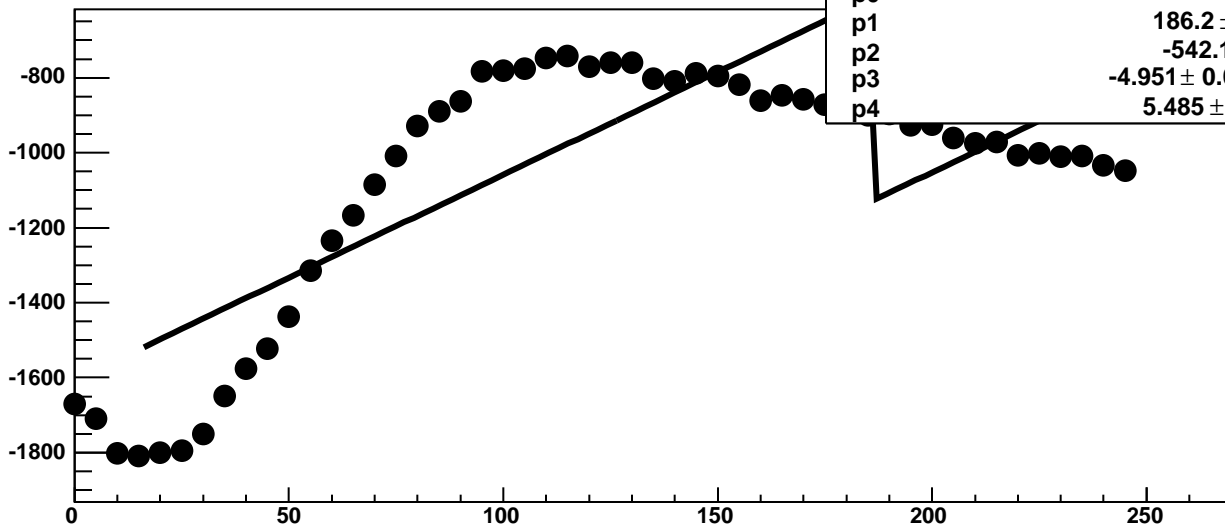
Chip 3, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

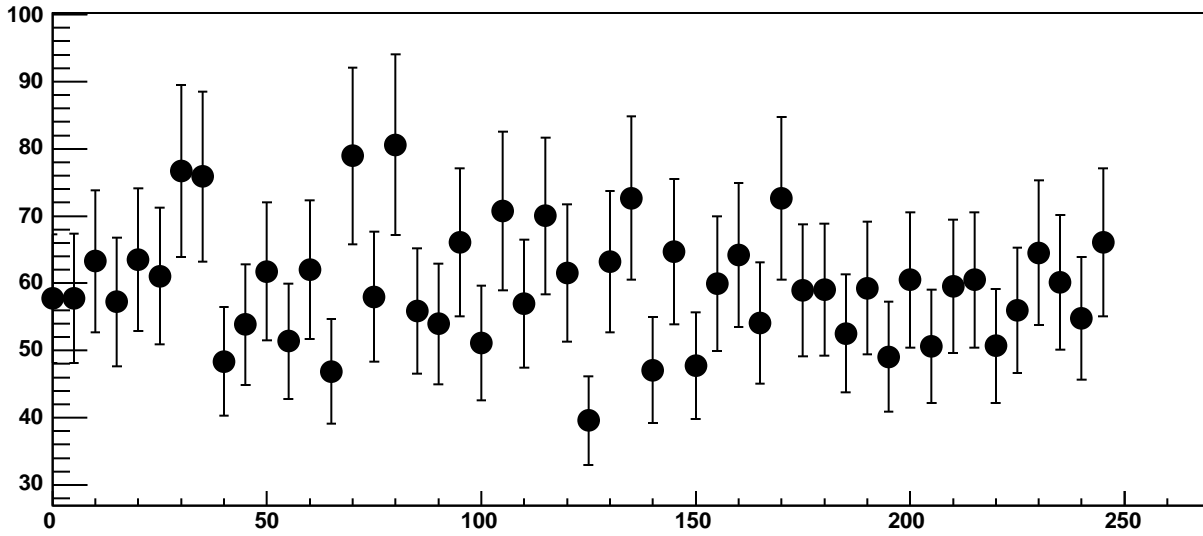


Chip 3, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

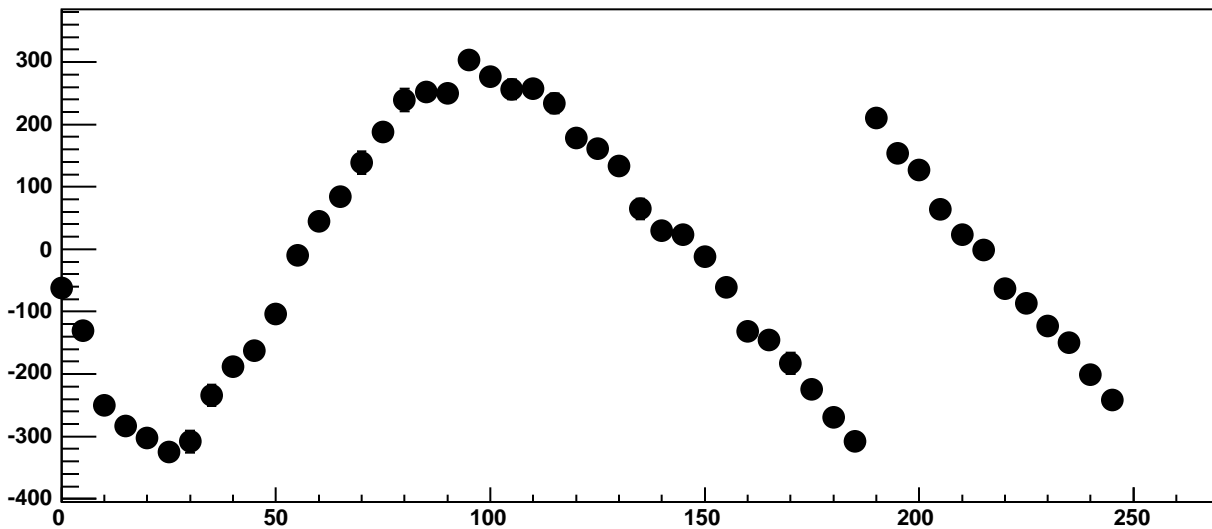


$\chi^2 / \text{ndf}$	8859 / 41
p0	$-586 \pm 4.53$
p1	$186.2 \pm 0.1565$
p2	$-542.1 \pm 6.786$
p3	$-4.951 \pm 0.0004324$
p4	$5.485 \pm 0.04891$

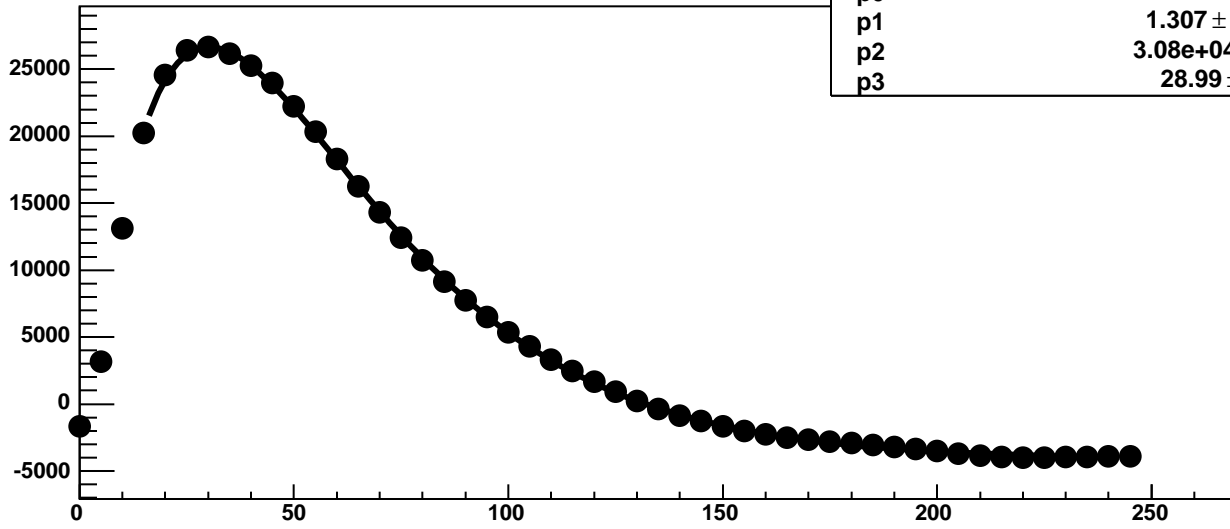
Chip 3, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

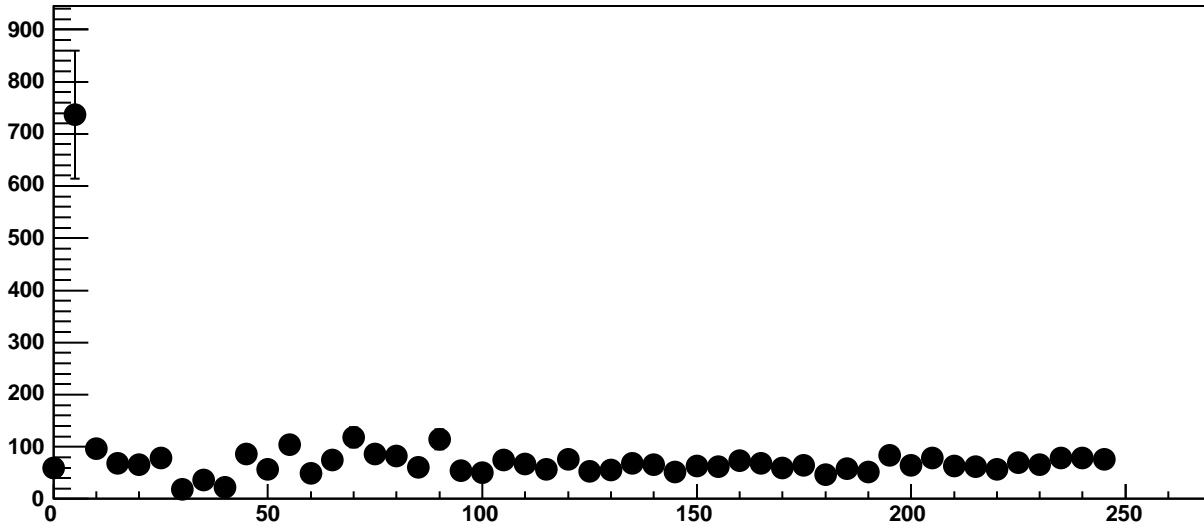


Chip 3, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

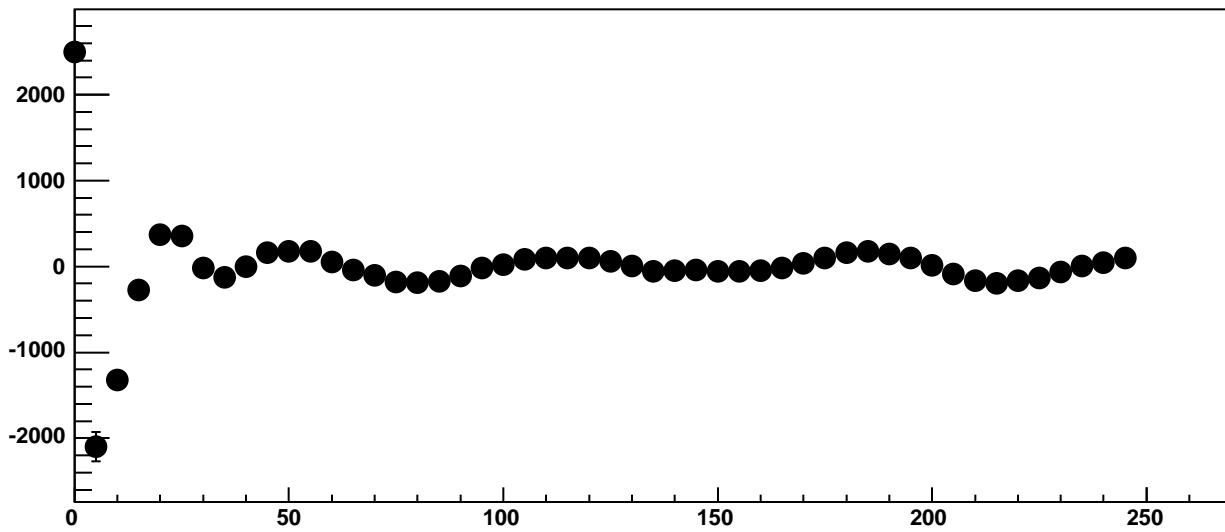


$\chi^2 / \text{ndf}$	3690 / 42
p0	$-4152 \pm 4.142$
p1	$1.307 \pm 0.01668$
p2	$3.08\text{e}+04 \pm 4.721$
p3	$28.99 \pm 0.0109$

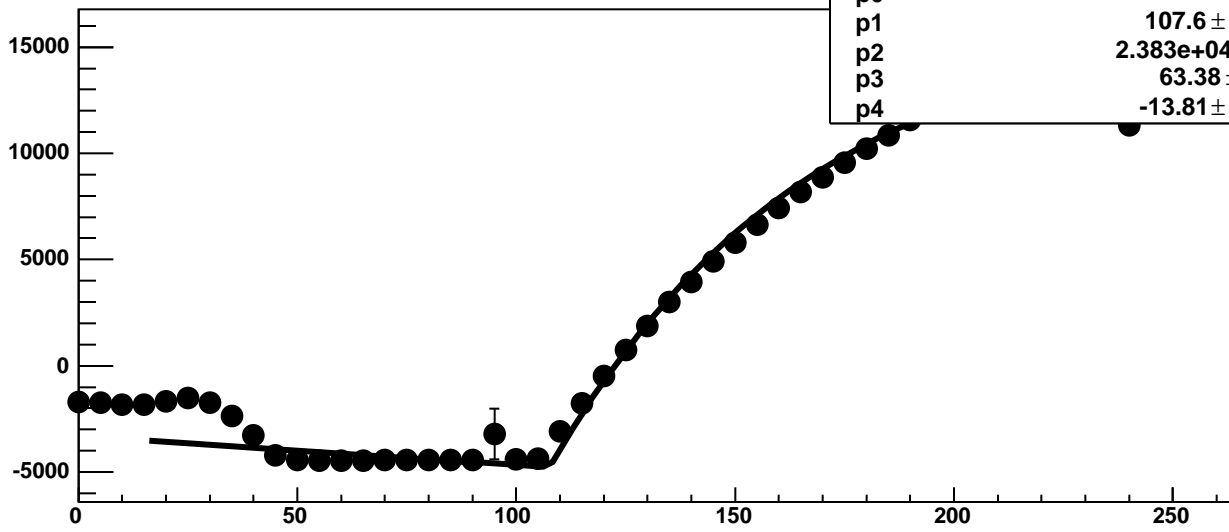
Chip 3, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



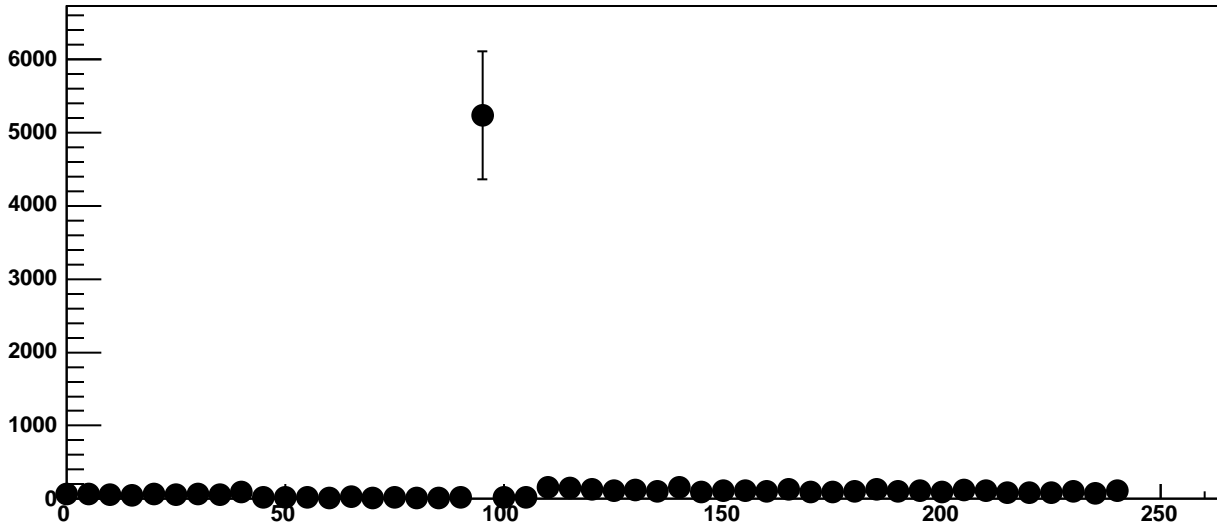
Chip 3, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold



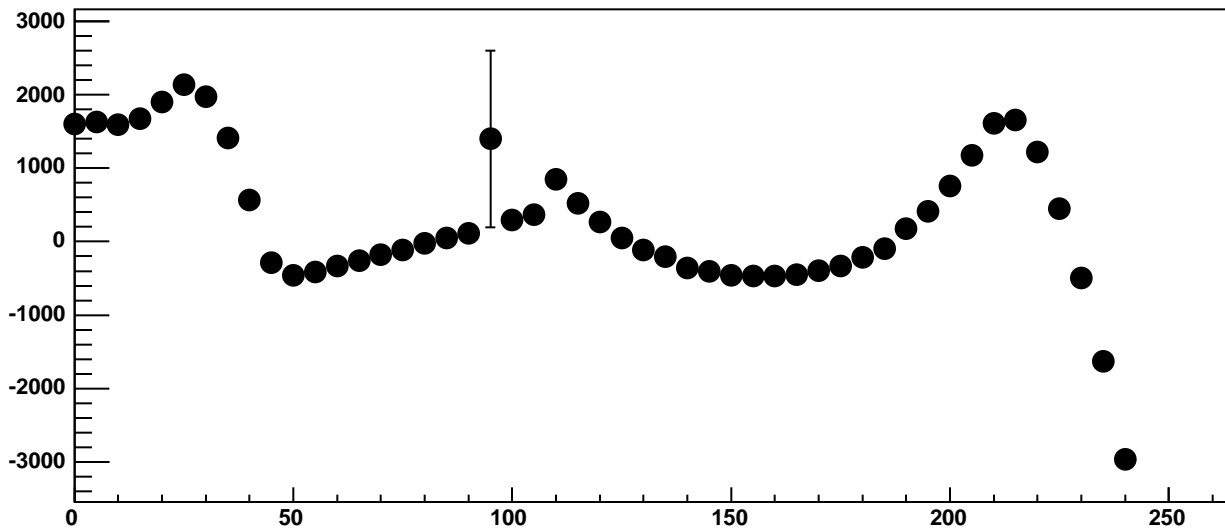
Chip 3, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold



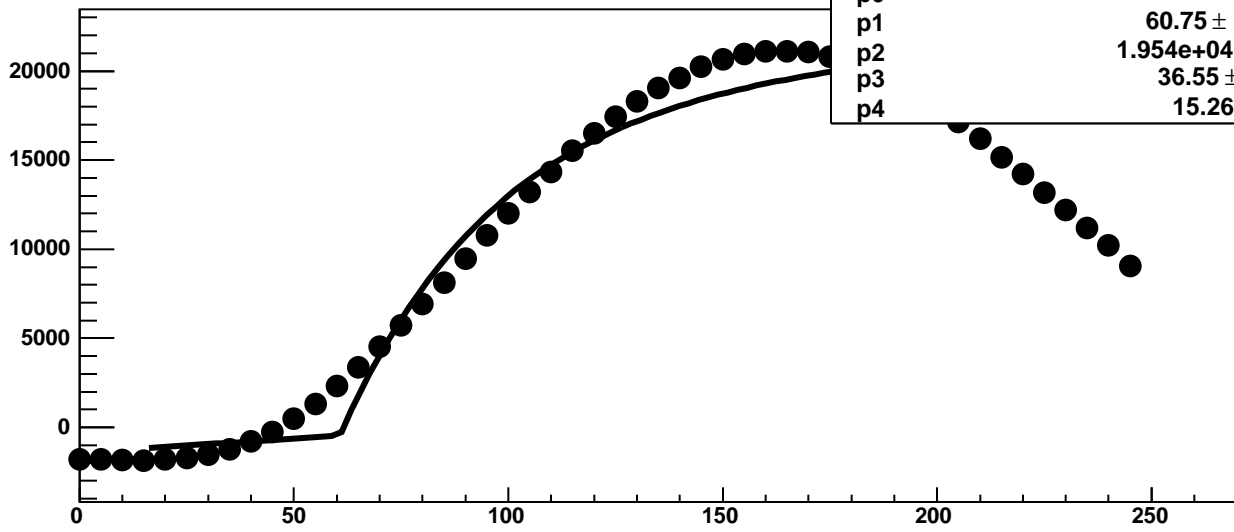
Chip 3, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

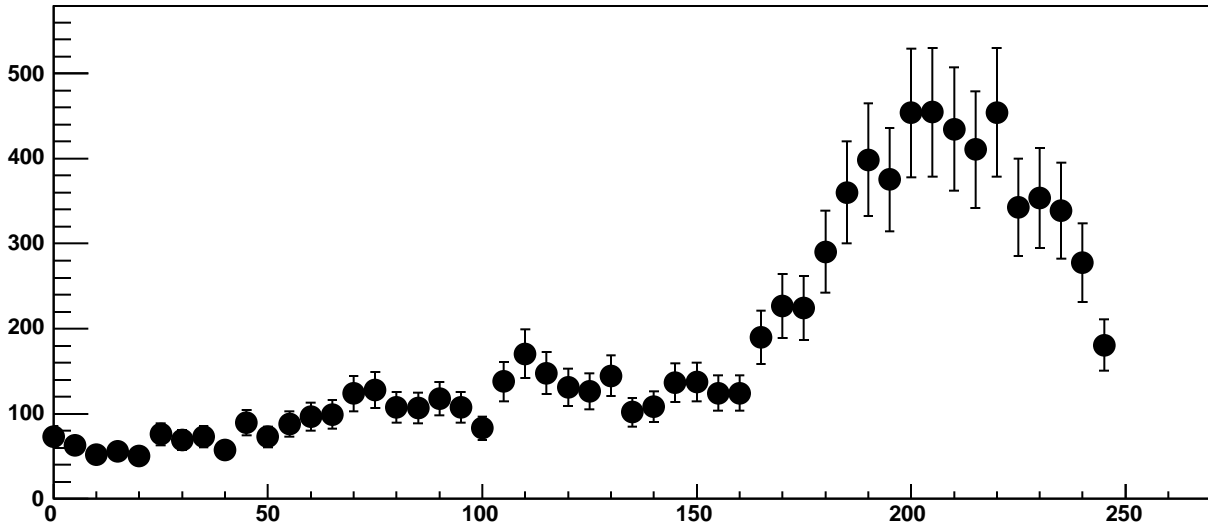


Chip 3, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

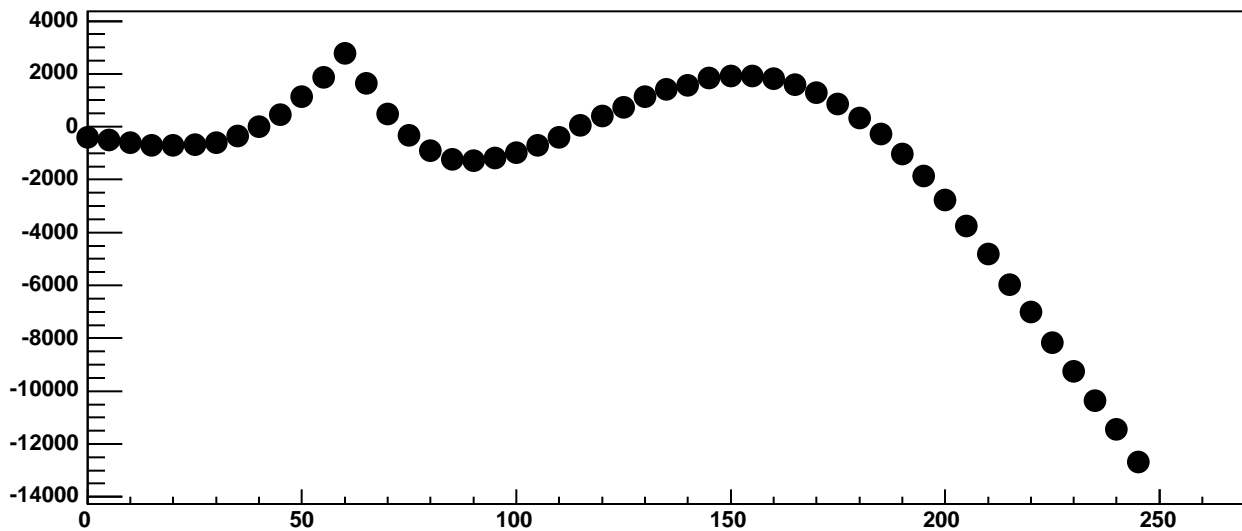


$\chi^2 / \text{ndf}$	1.718e+05 / 41
p0	-471.8 ± 9.374
p1	60.75 ± 0.04258
p2	1.954e+04 ± 45.43
p3	36.55 ± 0.1046
p4	15.26 ± 0.276

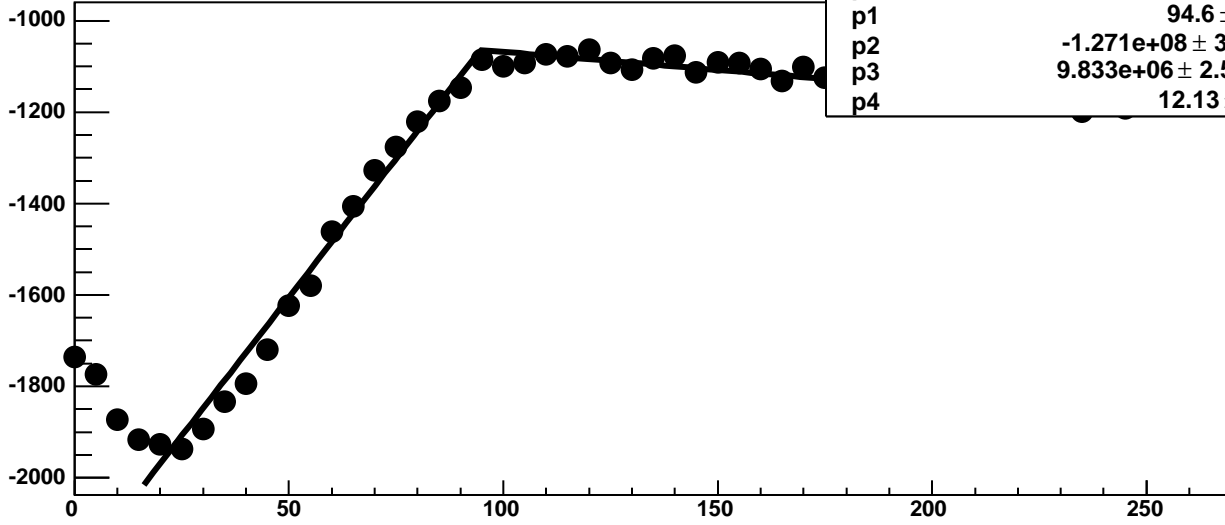
Chip 3, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

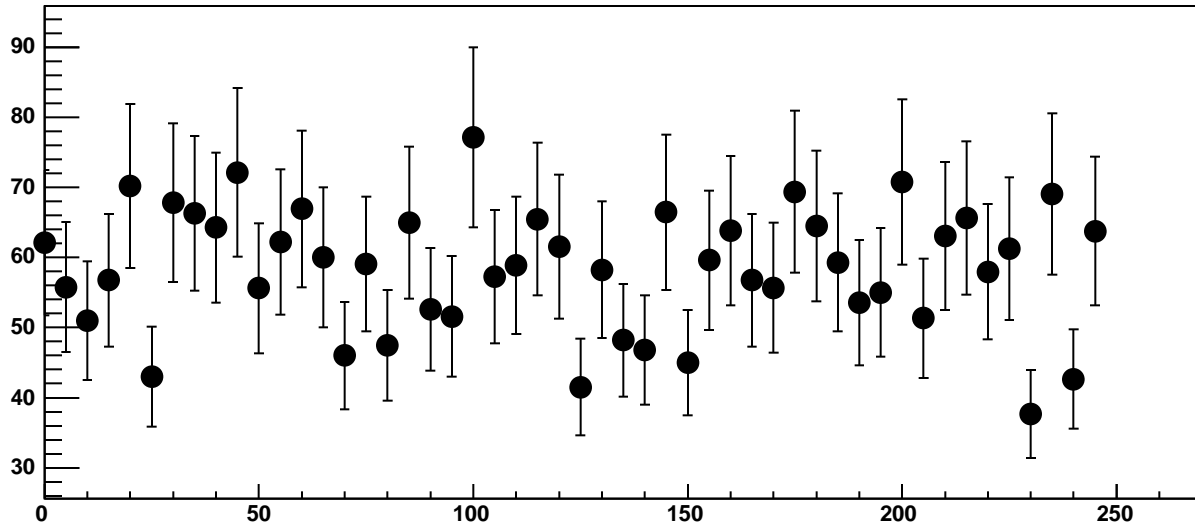


Chip 3, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

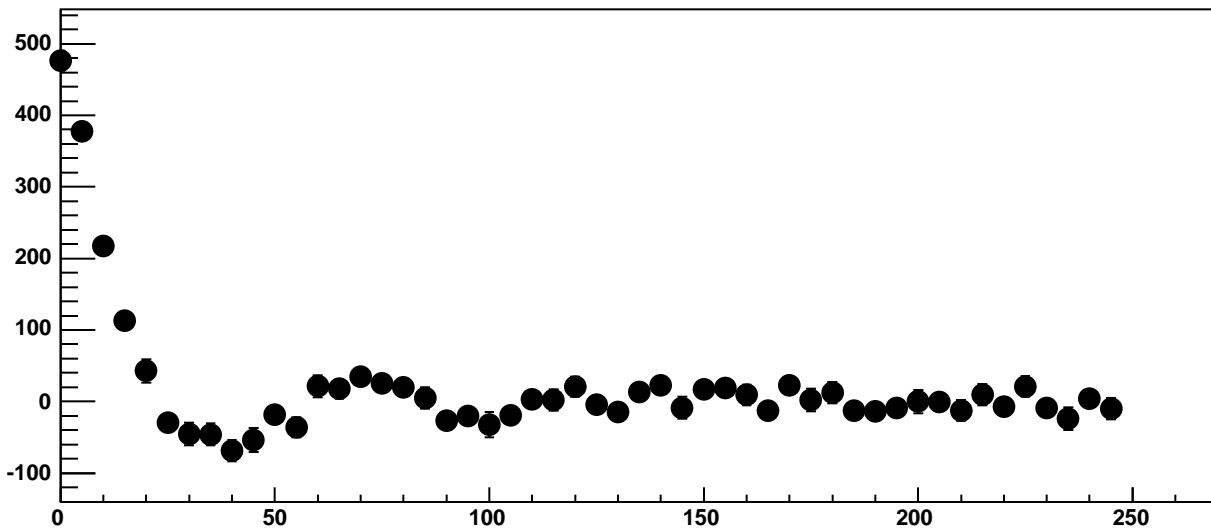


$\chi^2 / \text{ndf}$	214.7 / 41
p0	-1064 ± 4.216
p1	94.6 ± 0.5895
p2	-1.271e+08 ± 3.23e+06
p3	9.833e+06 ± 2.531e+05
p4	12.13 ± 0.1281

Chip 3, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

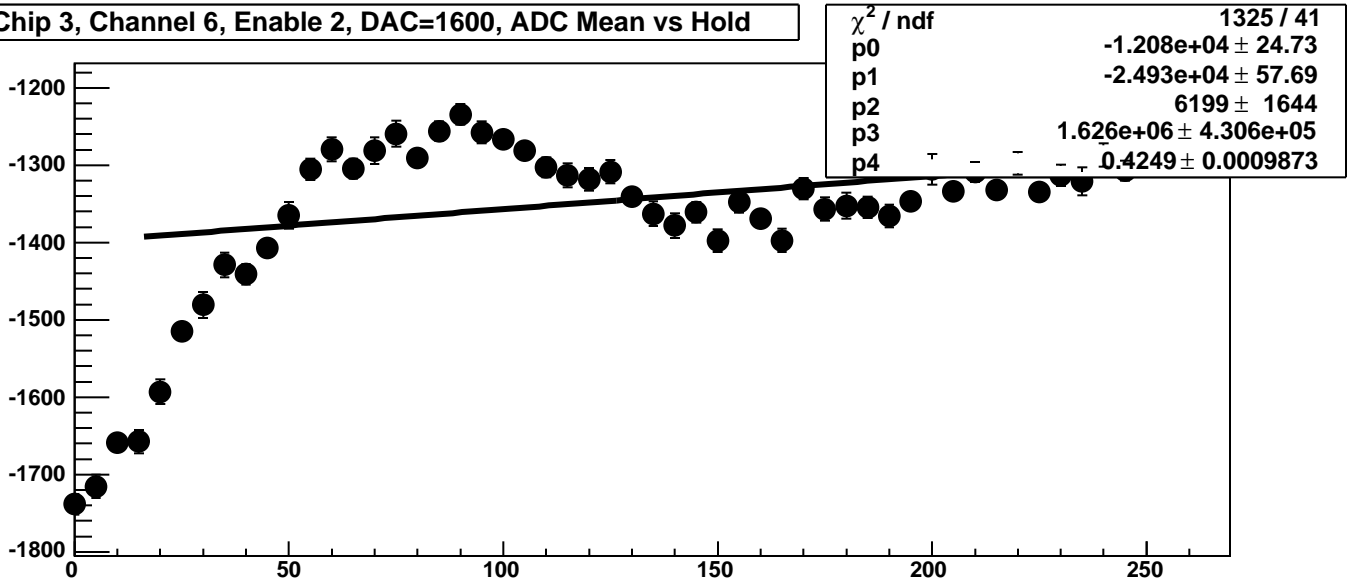


Chip 3, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

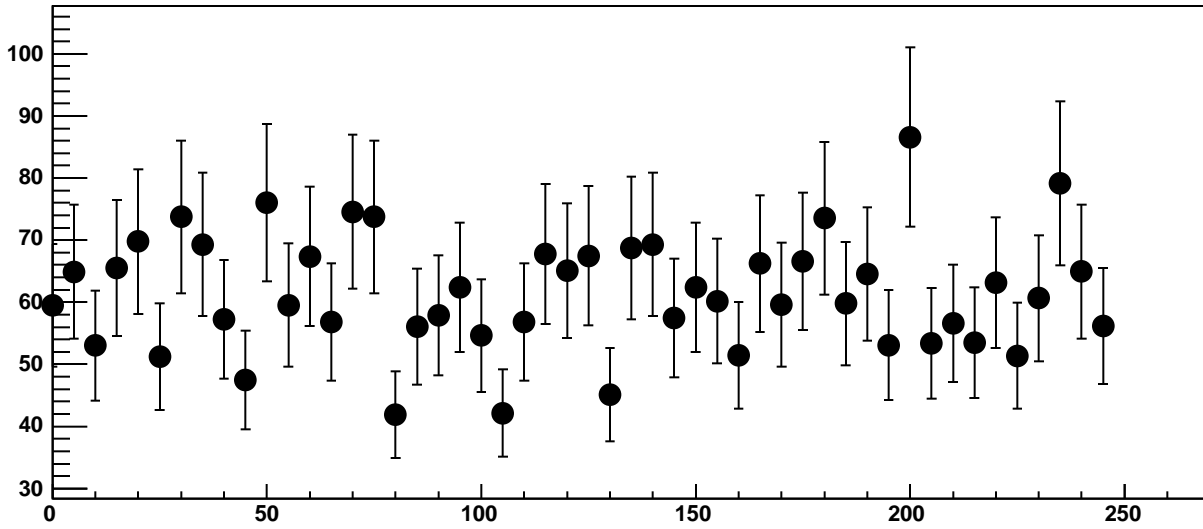




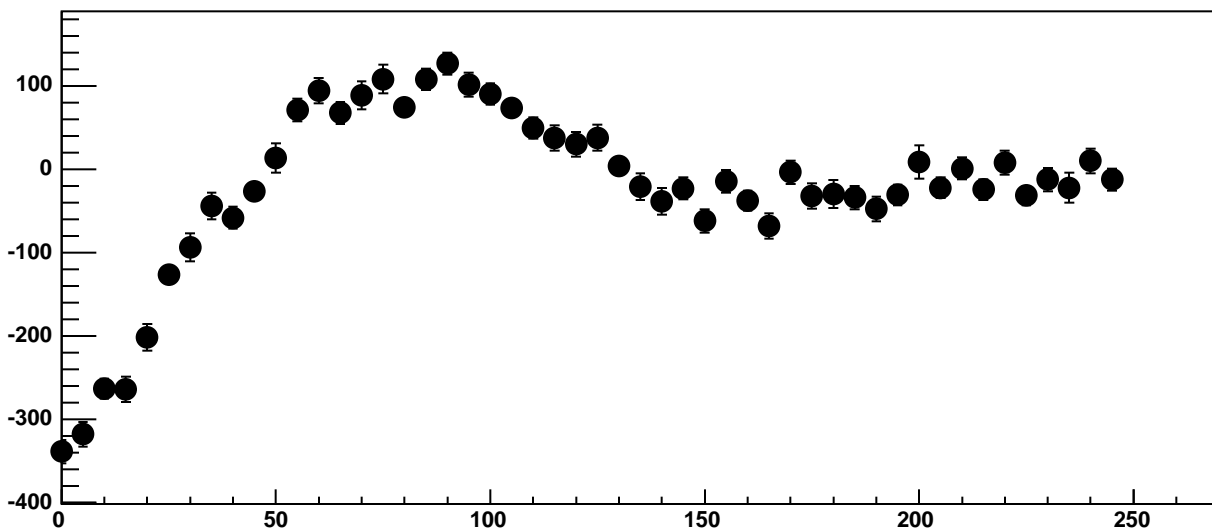
Chip 3, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold



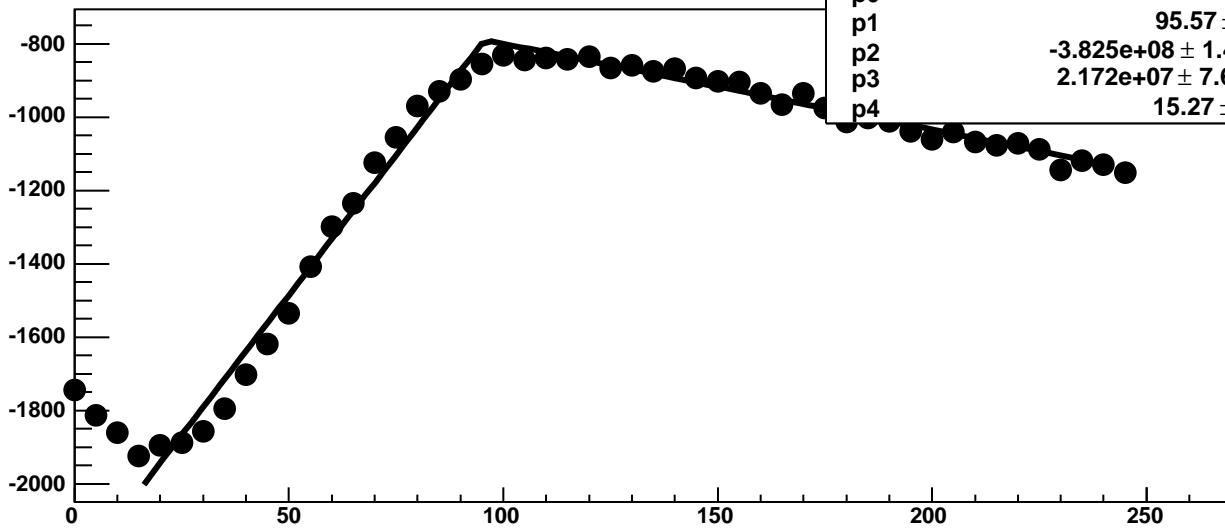
Chip 3, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold

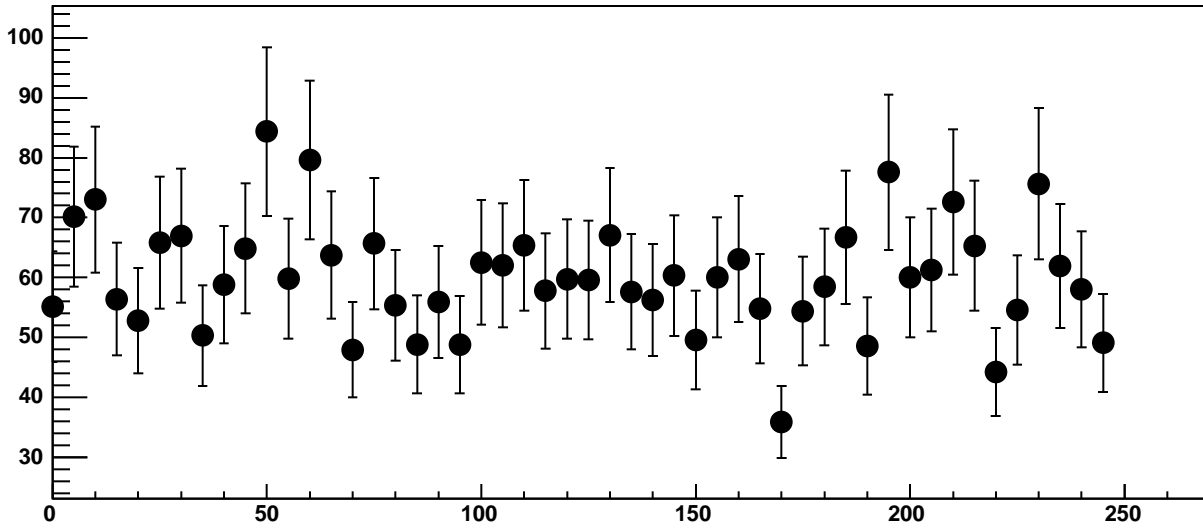


Chip 3, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

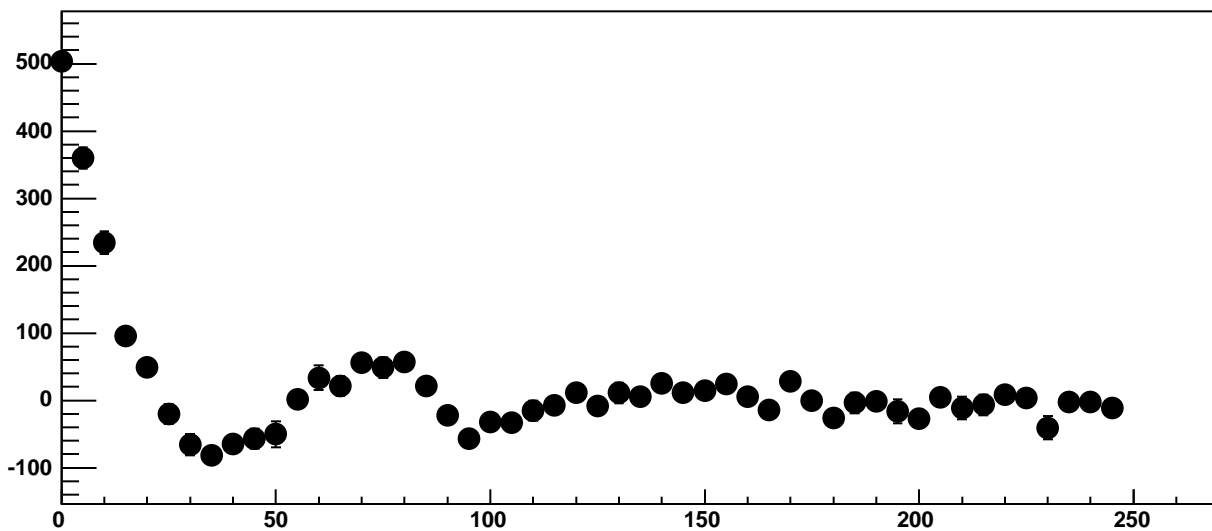


$\chi^2 / \text{ndf}$	331.8 / 41
p0	$-789.5 \pm 4.586$
p1	$95.57 \pm 0.4392$
p2	$-3.825\text{e}+08 \pm 1.403\text{e}+07$
p3	$2.172\text{e}+07 \pm 7.657\text{e}+05$
p4	$15.27 \pm 0.1245$

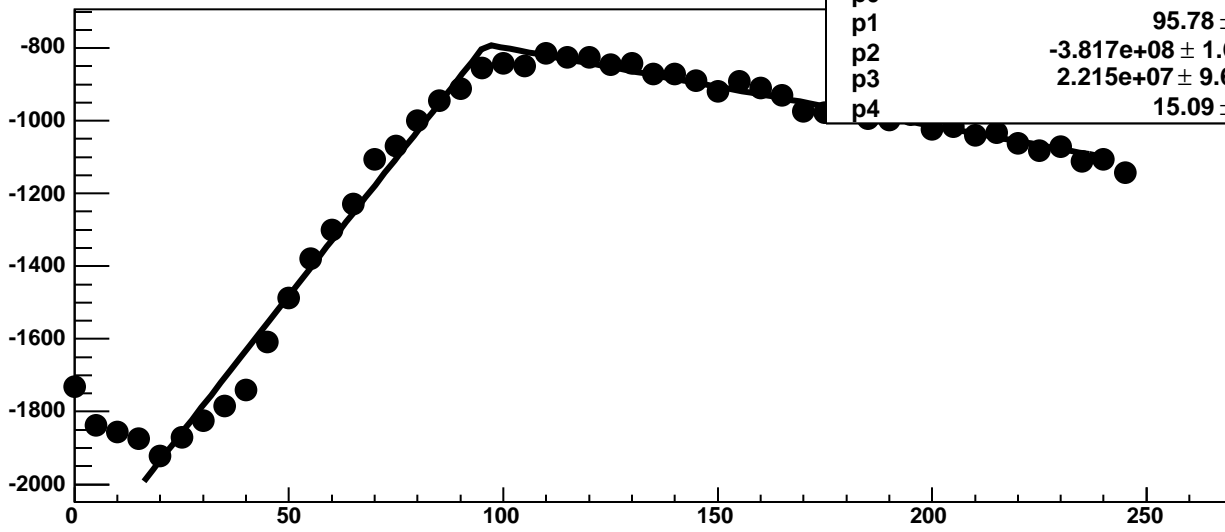
Chip 3, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

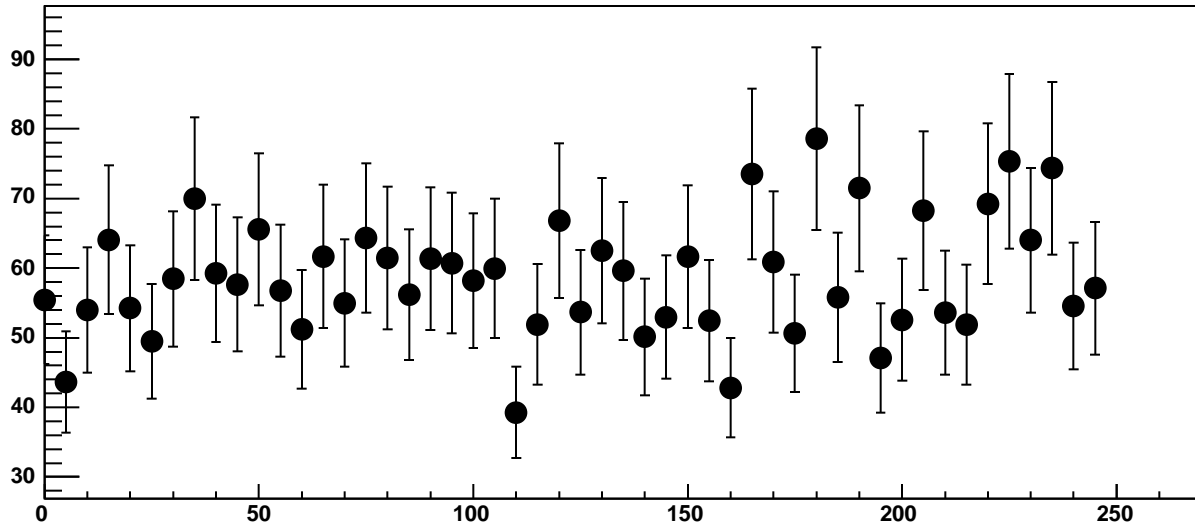


Chip 3, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

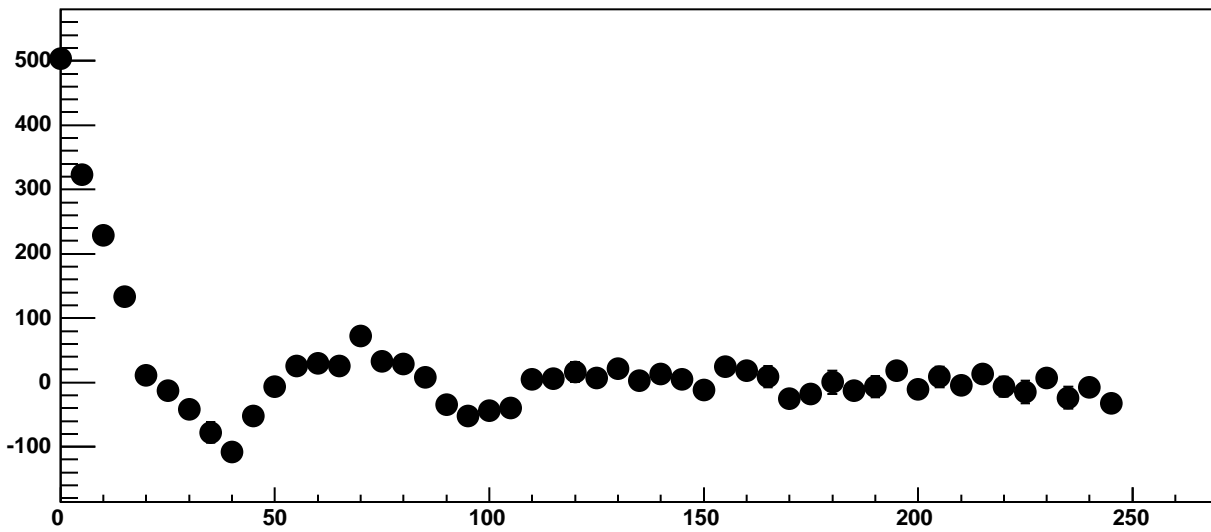


$\chi^2 / \text{ndf}$	323.3 / 41
p0	-790 ± 4.206
p1	95.78 ± 0.4616
p2	-3.817e+08 ± 1.656e+07
p3	2.215e+07 ± 9.674e+05
p4	15.09 ± 0.1335

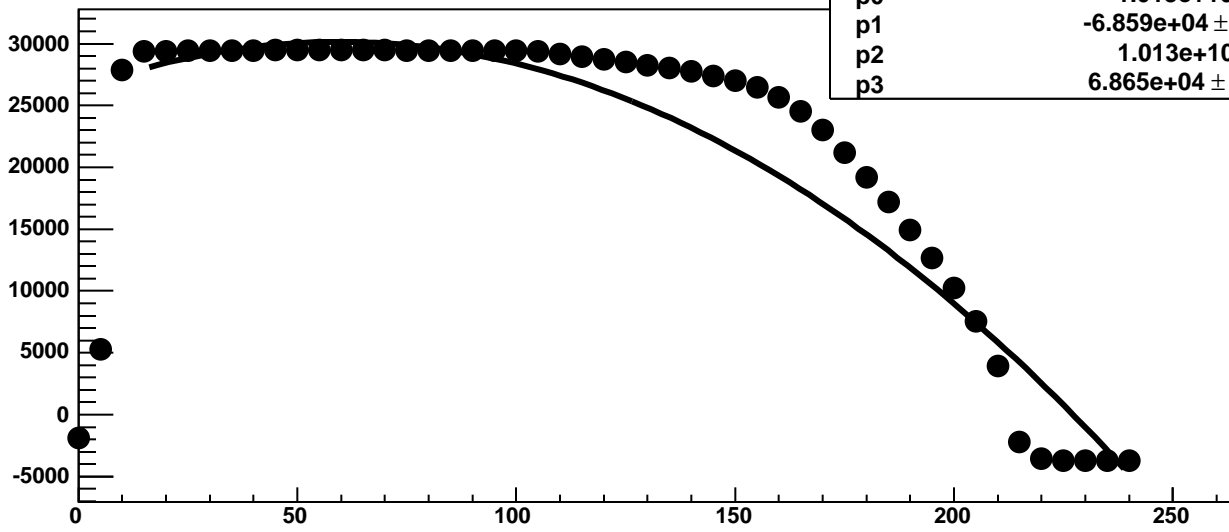
Chip 3, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

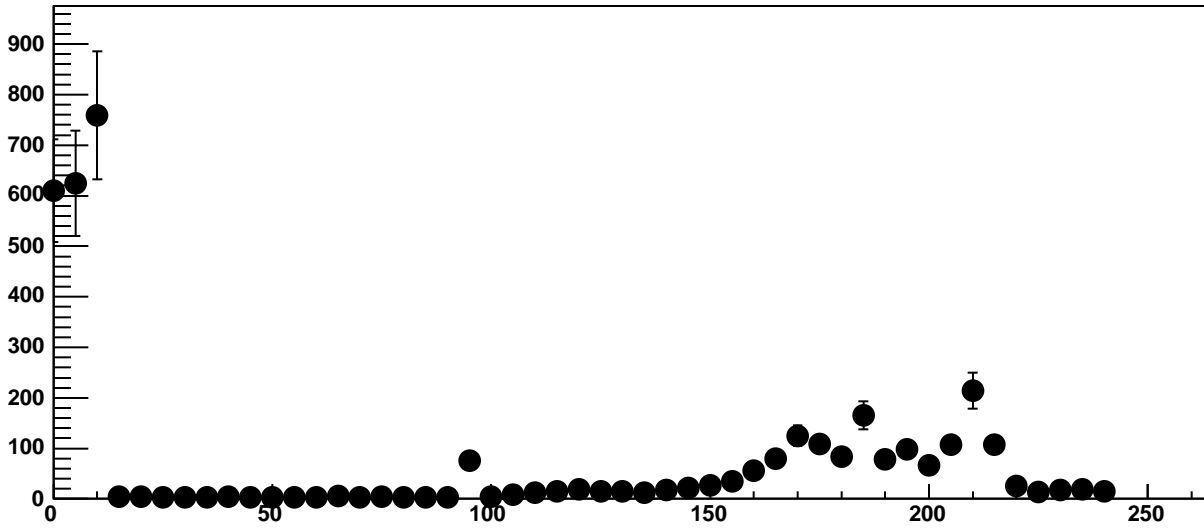


Chip 3, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

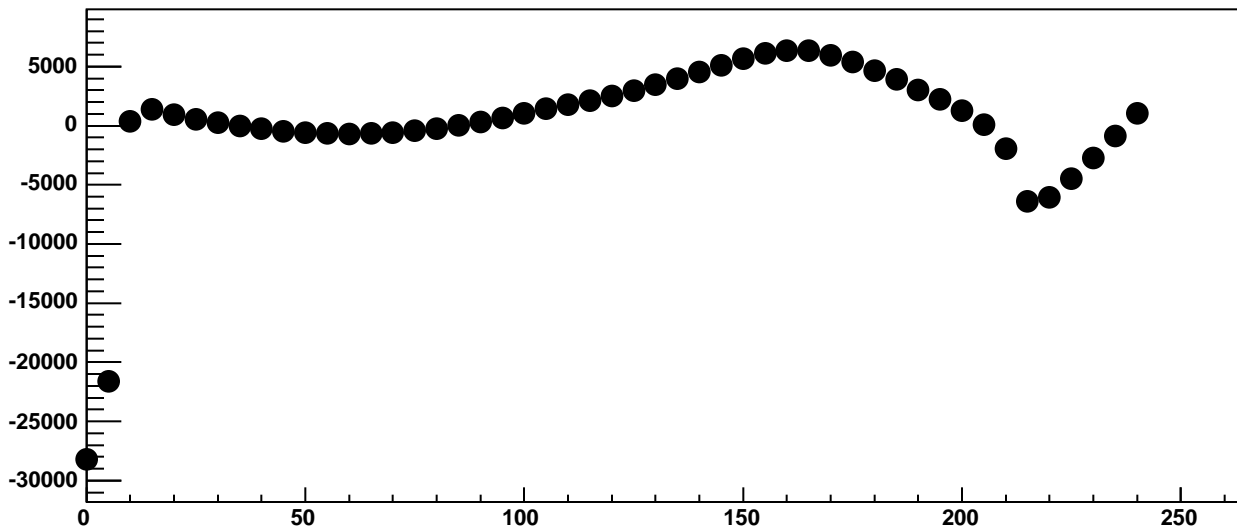


$\chi^2 / \text{ndf}$	2.141e+07 / 42
p0	-1.013e+10 $\pm$ 3.022
p1	-6.859e+04 $\pm$ 0.04051
p2	1.013e+10 $\pm$ 3.022
p3	6.865e+04 $\pm$ 0.04047

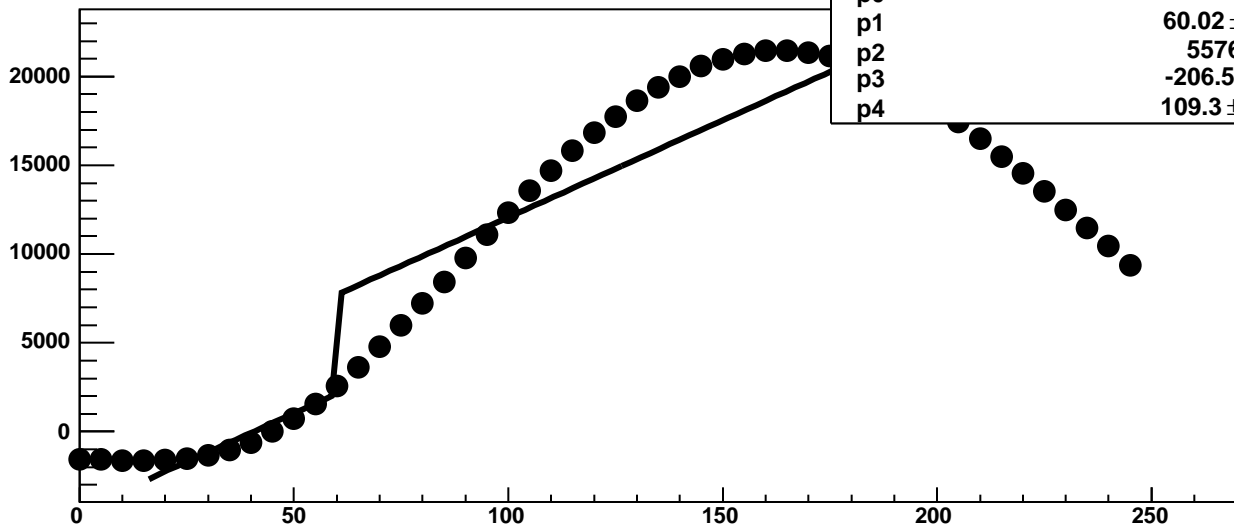
Chip 3, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold

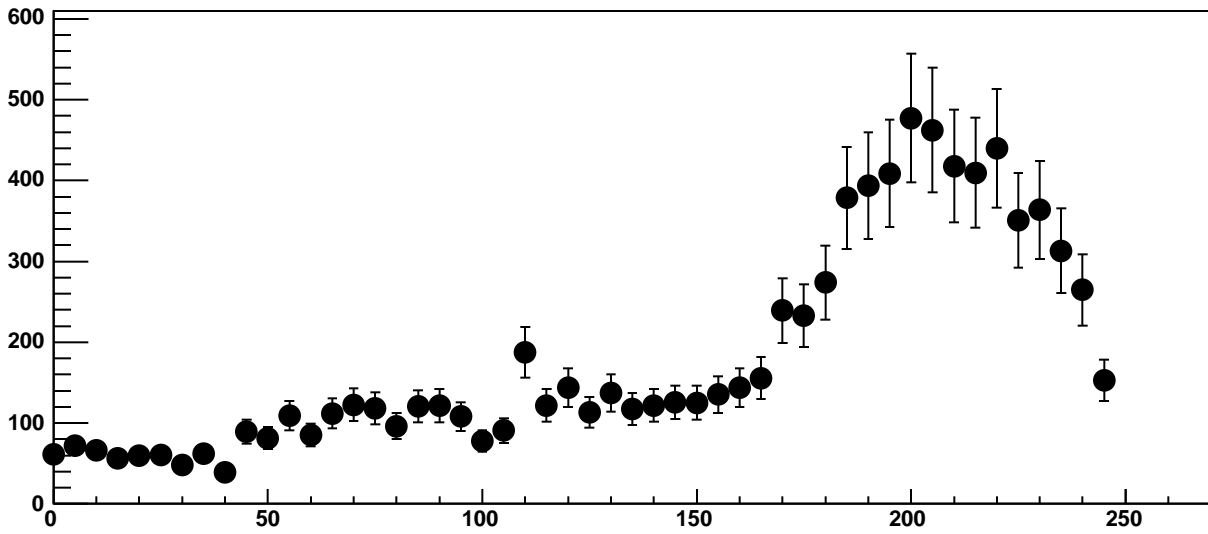


Chip 3, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

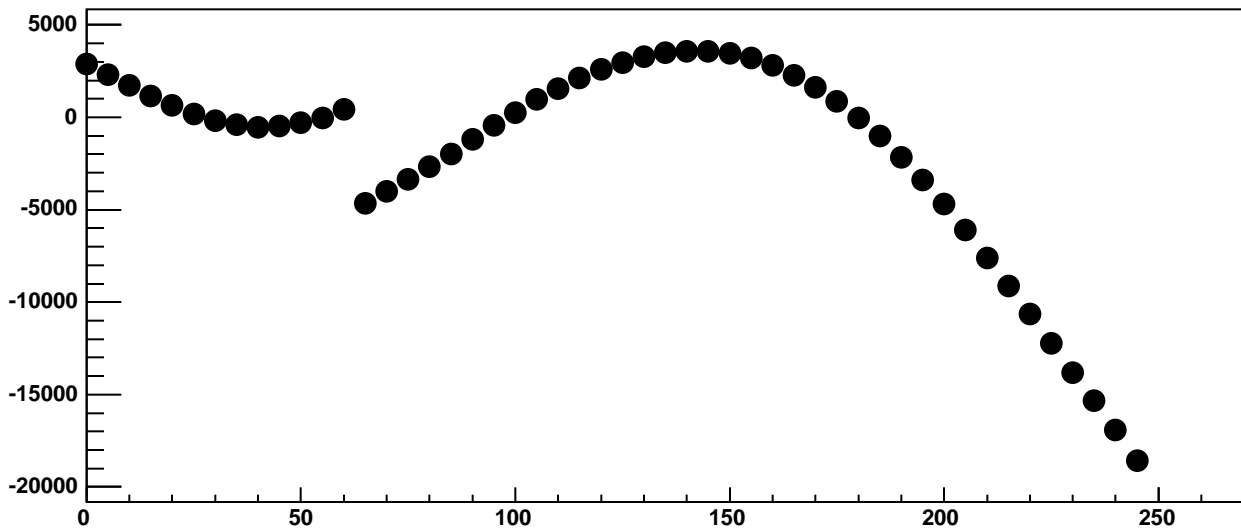


$\chi^2 / \text{ndf}$	4.399e+05 / 41
p0	2126 ± 15.06
p1	60.02 ± 0.1791
p2	5576 ± 38.9
p3	-206.5 ± 12.09
p4	109.3 ± 0.6437

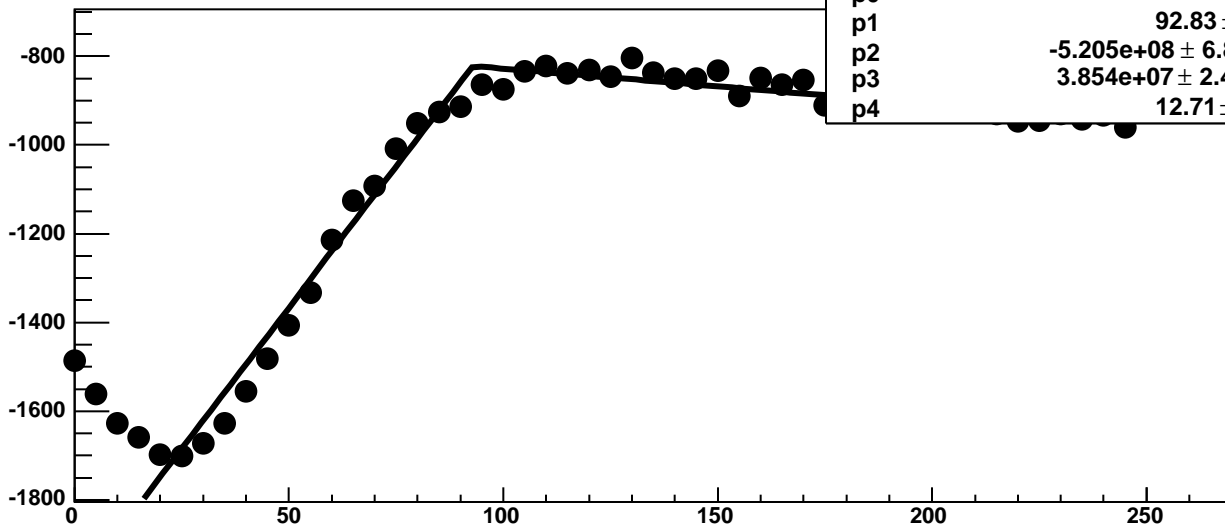
Chip 3, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

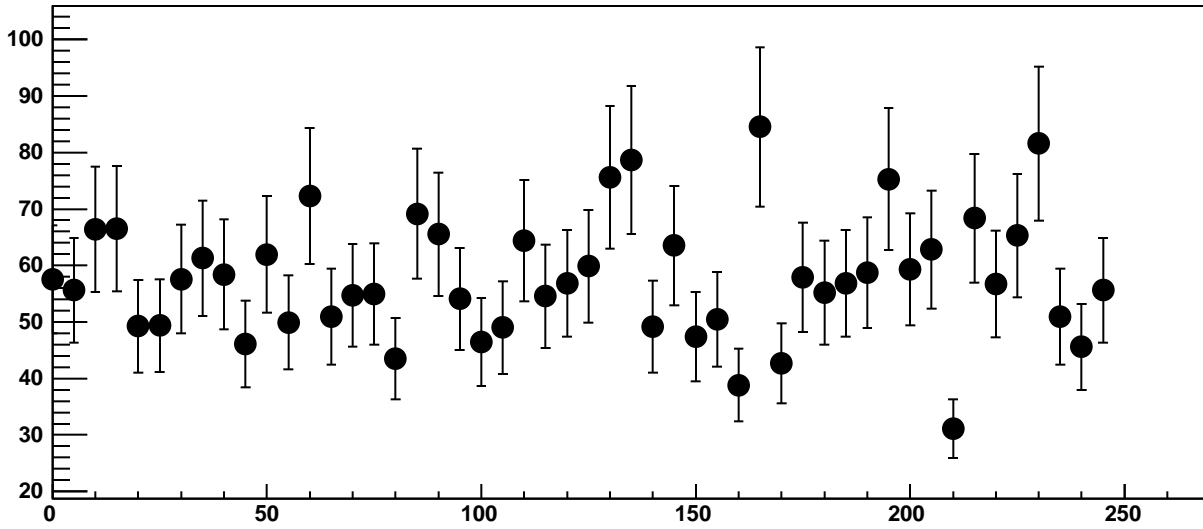


Chip 3, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

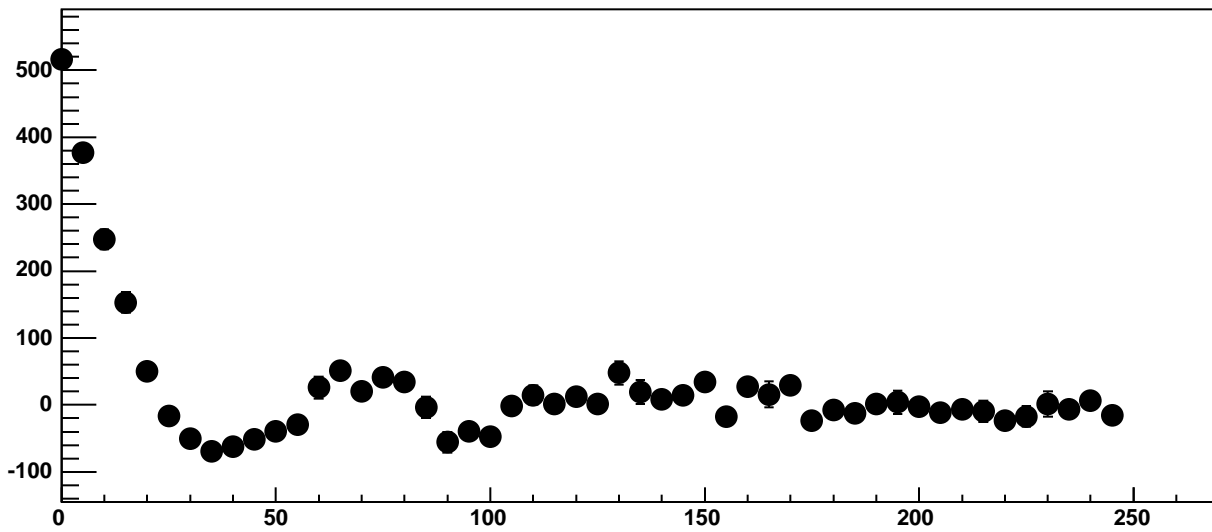


$\chi^2 / \text{ndf}$	367.7 / 41
p0	$-822.3 \pm 4.305$
p1	$92.83 \pm 0.5888$
p2	$-5.205\text{e}+08 \pm 6.837\text{e}+06$
p3	$3.854\text{e}+07 \pm 2.436\text{e}+05$
p4	$12.71 \pm 0.1405$

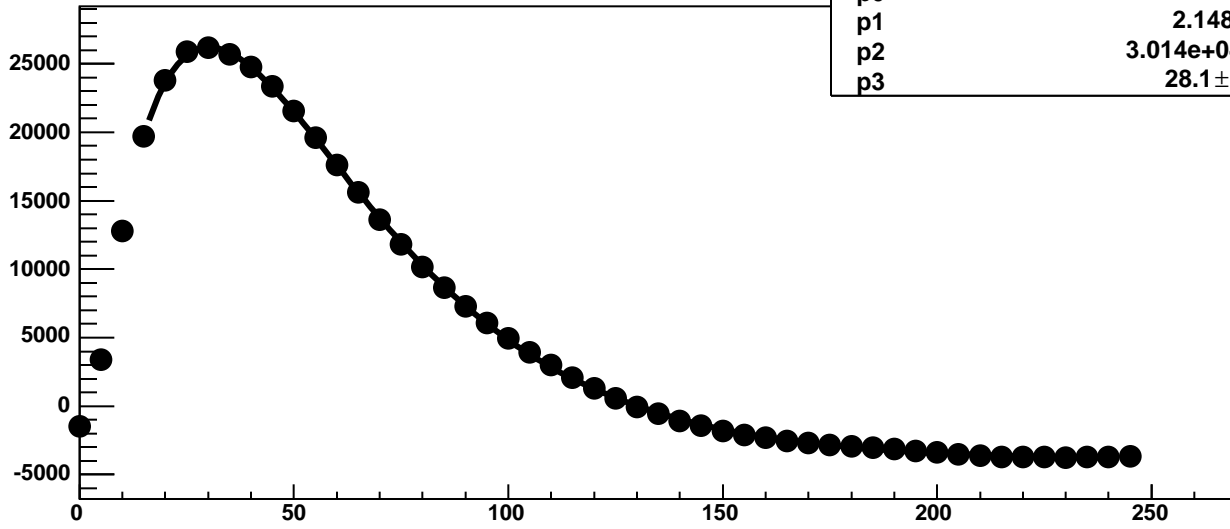
Chip 3, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

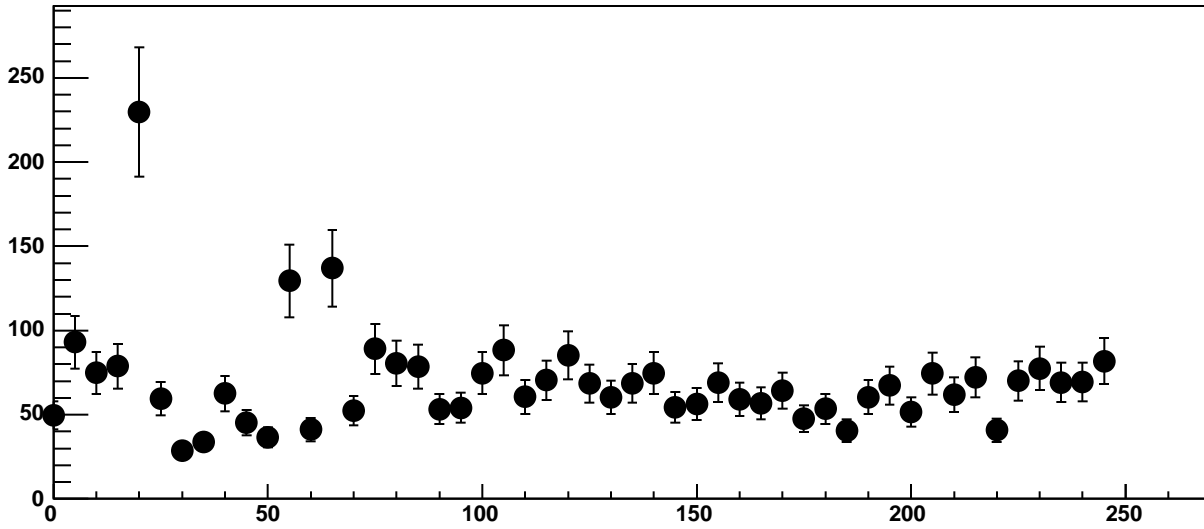


Chip 3, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold

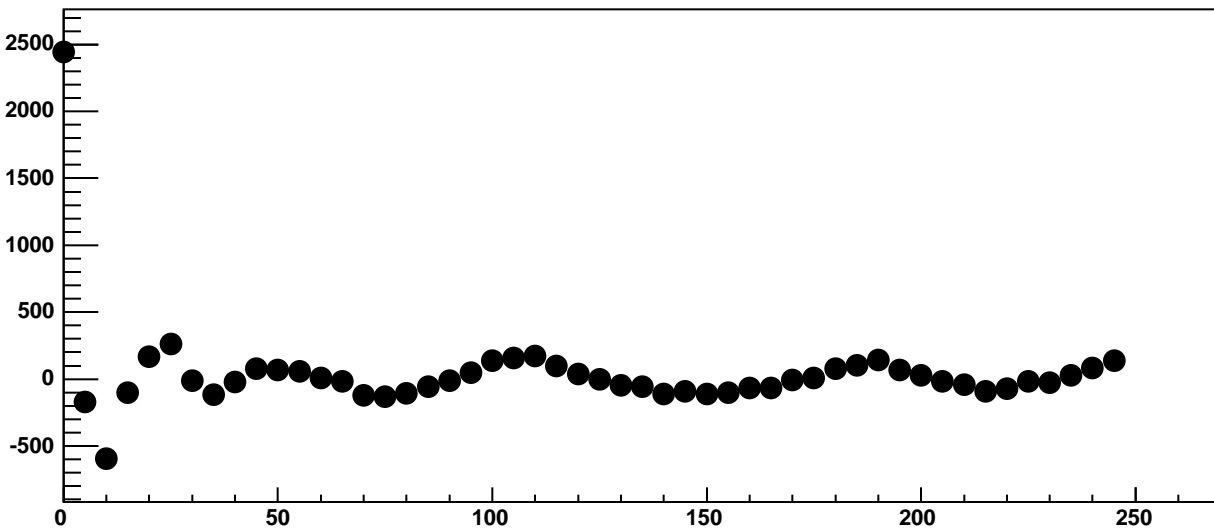


$\chi^2 / \text{ndf}$	1989 / 42
p0	$-3928 \pm 3.702$
p1	$2.148 \pm 0.019$
p2	$3.014\text{e}+04 \pm 5.01$
p3	$28.1 \pm 0.01127$

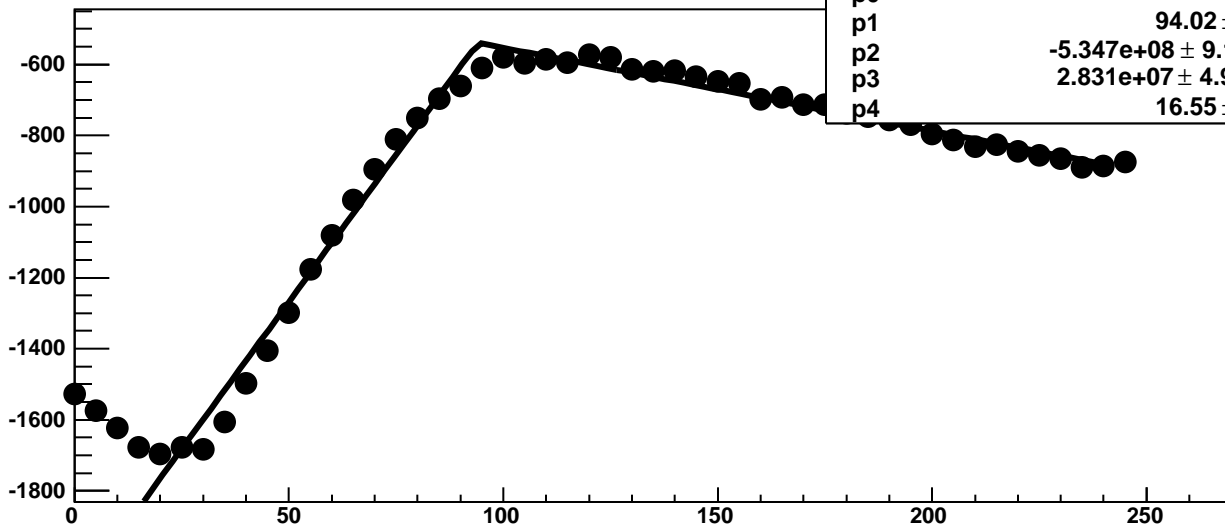
Chip 3, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold

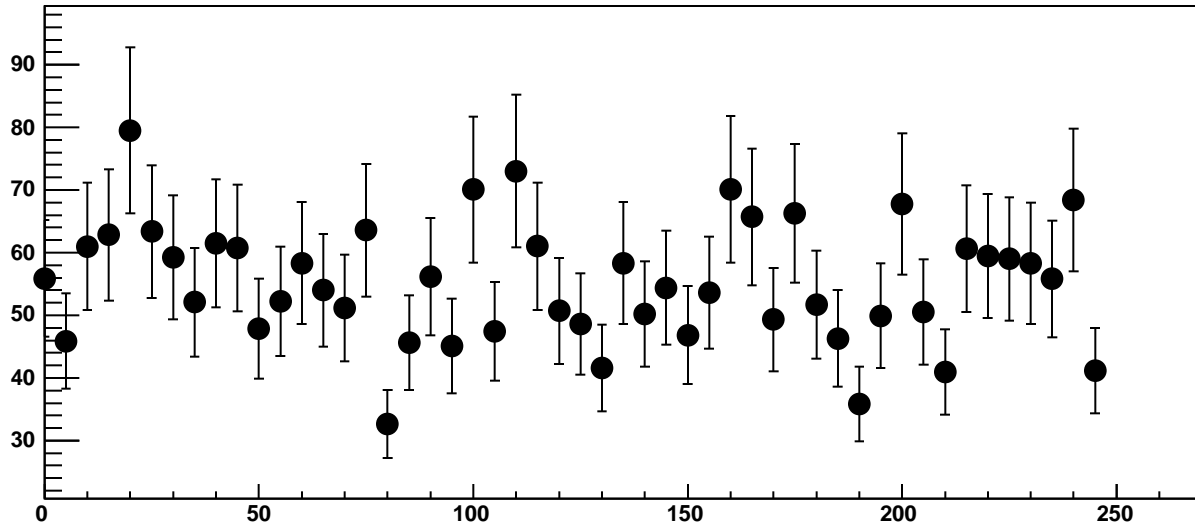


Chip 3, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

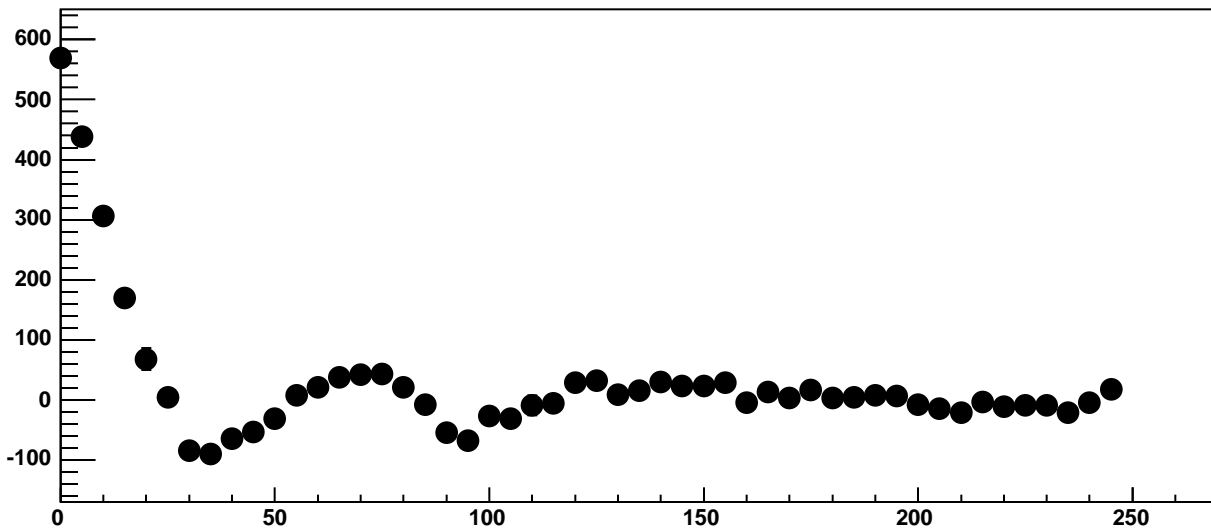


$\chi^2 / \text{ndf}$	456.5 / 41
p0	$-539.4 \pm 3.862$
p1	$94.02 \pm 0.3679$
p2	$-5.347\text{e}+08 \pm 9.108\text{e}+06$
p3	$2.831\text{e}+07 \pm 4.938\text{e}+05$
p4	$16.55 \pm 0.1252$

Chip 3, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

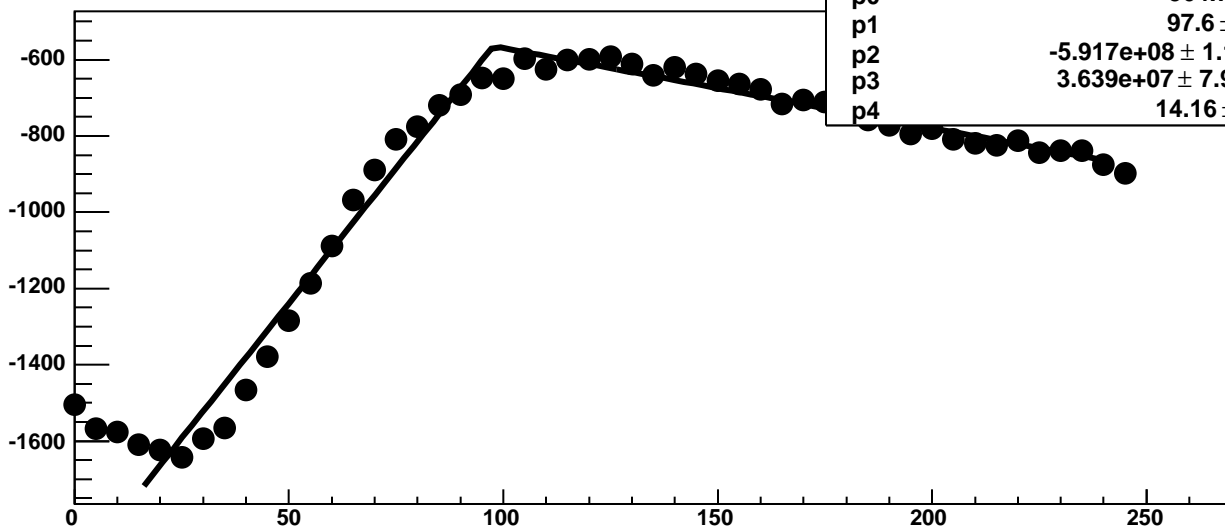


Chip 3, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold



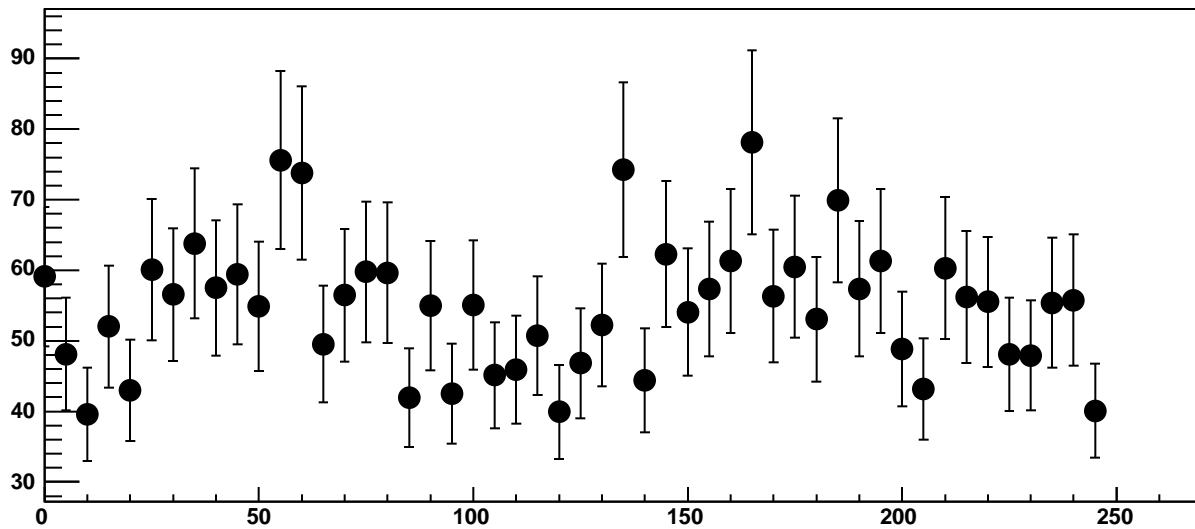


Chip 3, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

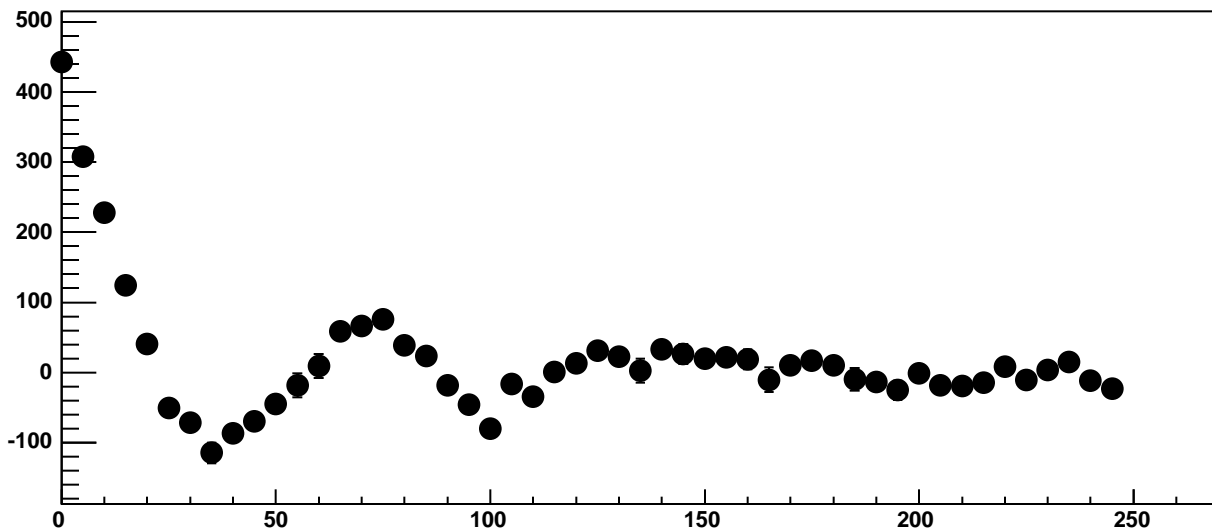


$\chi^2 / \text{ndf}$	540.6 / 41
p0	$-564.7 \pm 3.719$
p1	$97.6 \pm 0.4034$
p2	$-5.917\text{e}+08 \pm 1.176\text{e}+07$
p3	$3.639\text{e}+07 \pm 7.914\text{e}+05$
p4	$14.16 \pm 0.1038$

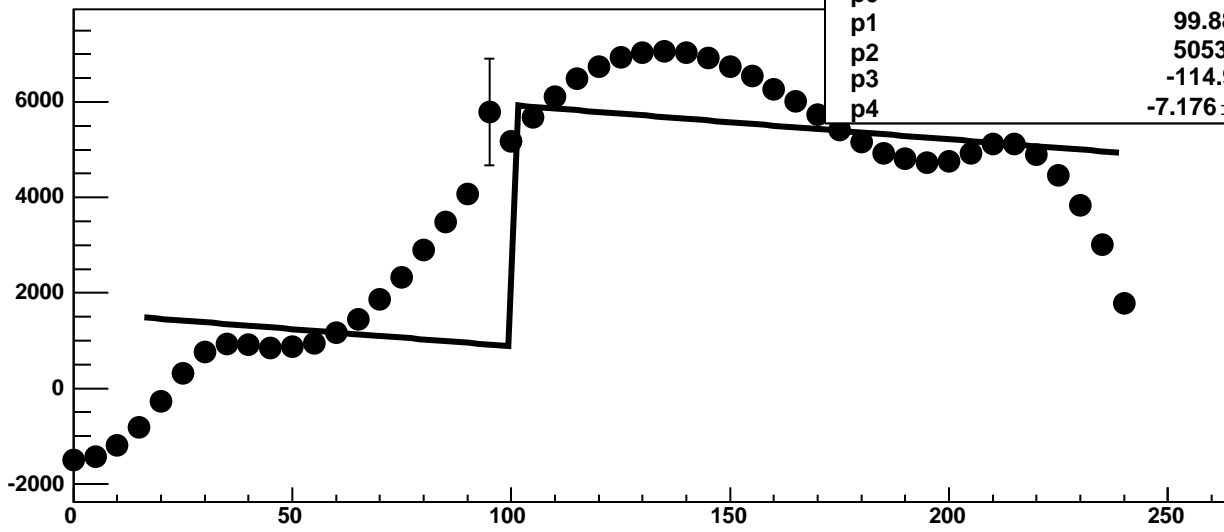
Chip 3, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



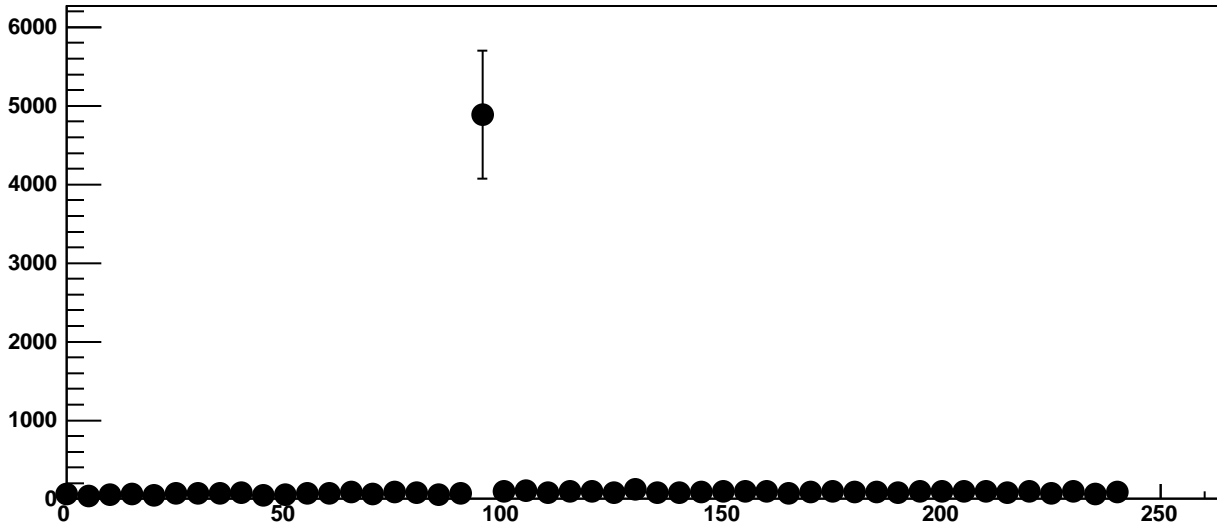
Chip 3, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold



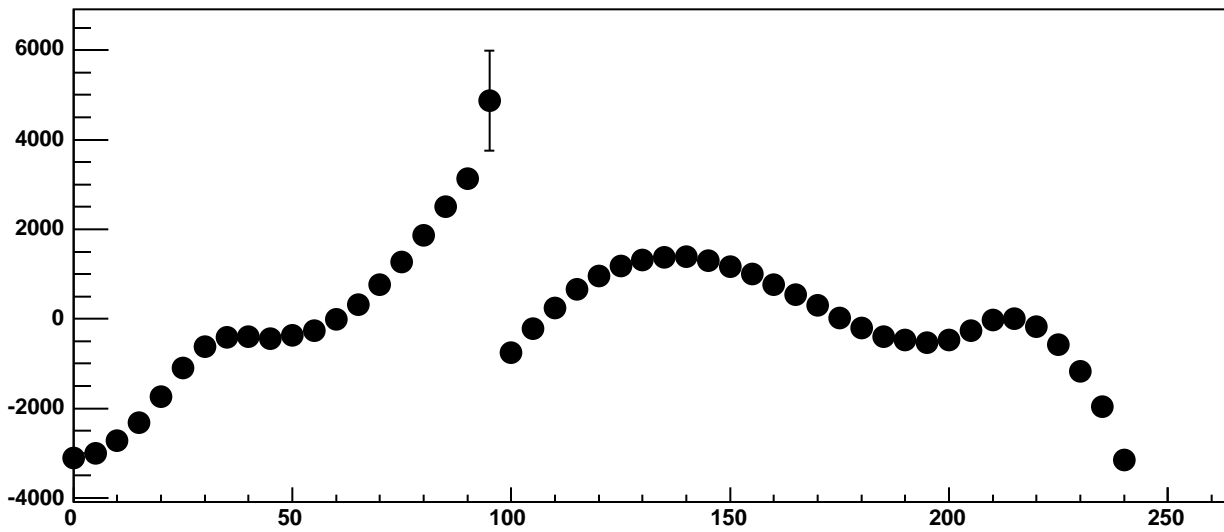
Chip 3, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold



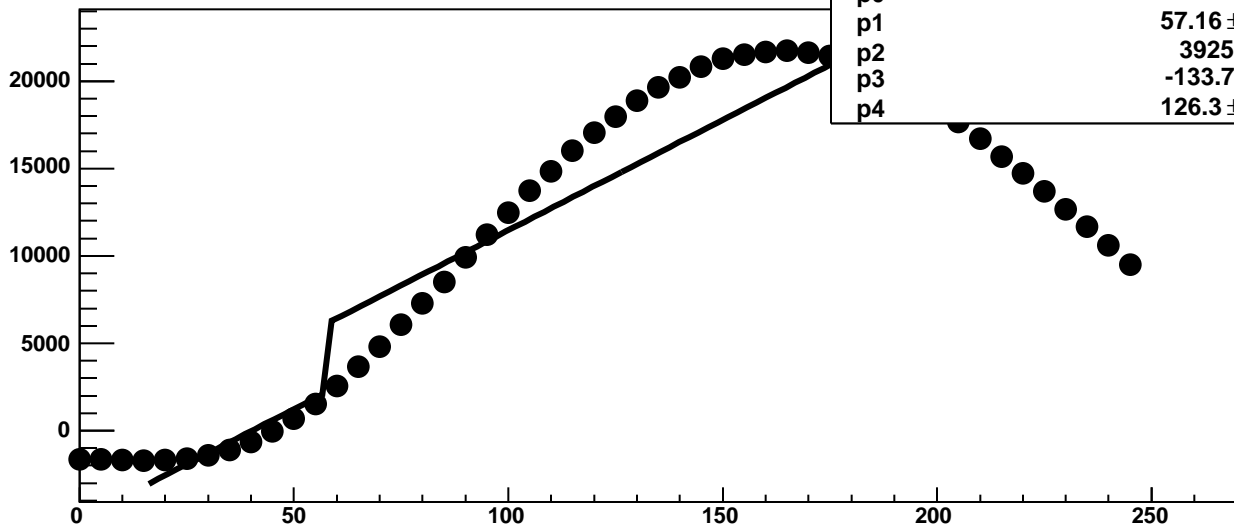
Chip 3, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



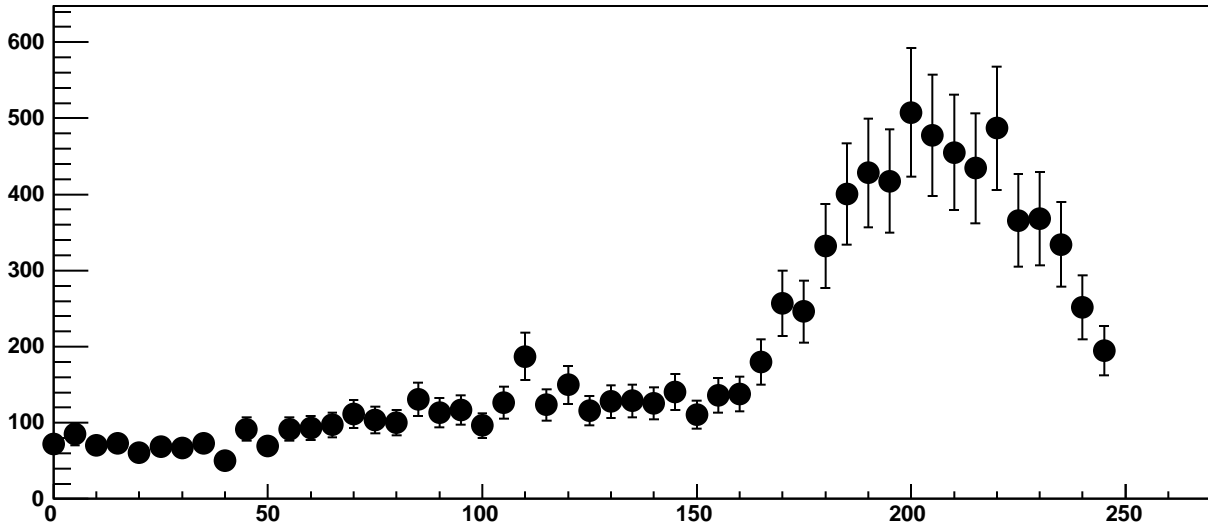
Chip 3, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold



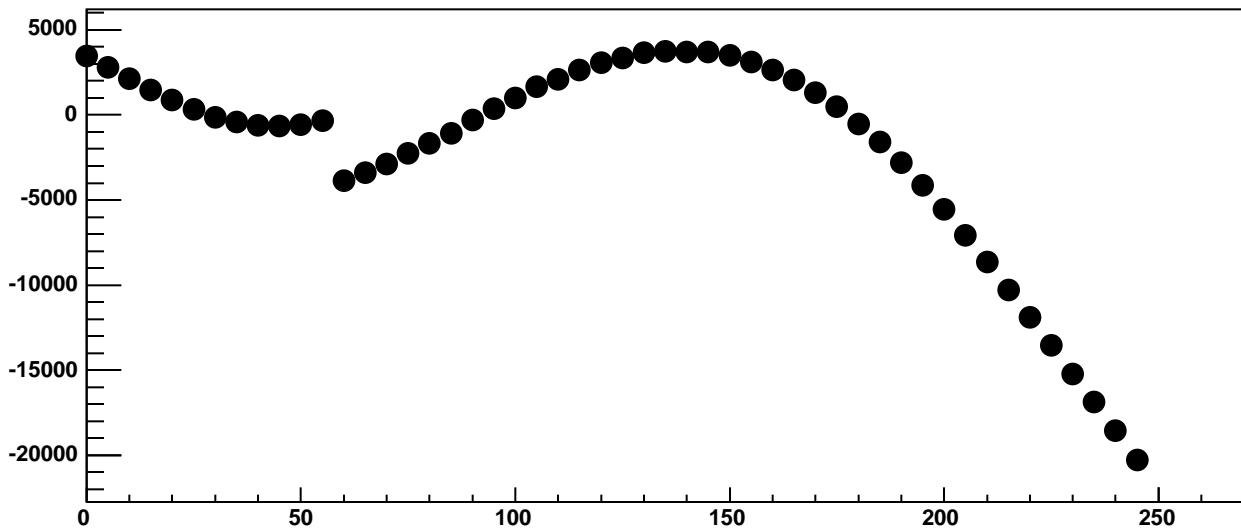
Chip 3, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold



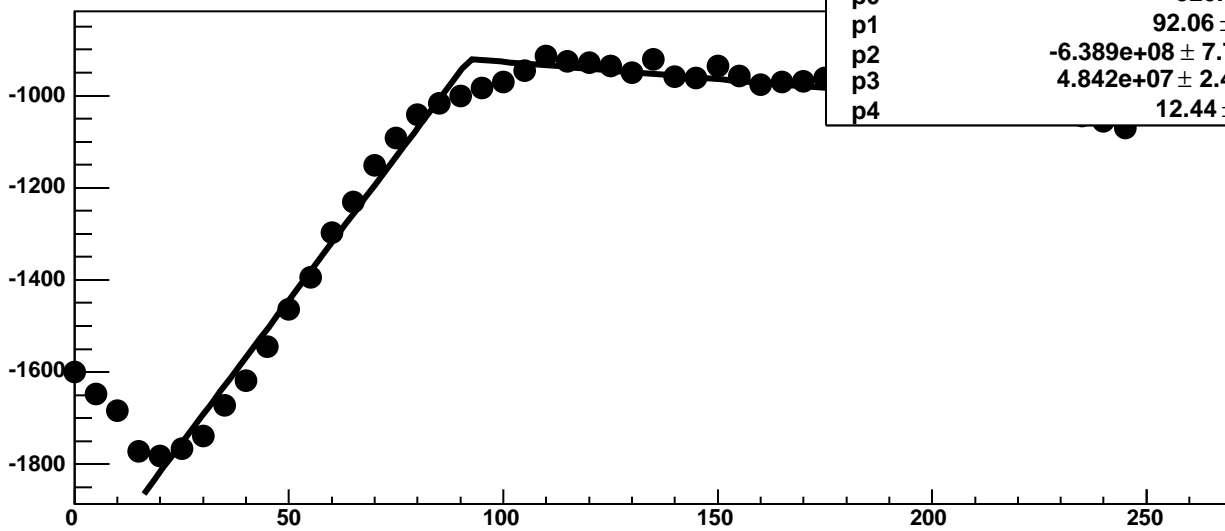
Chip 3, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

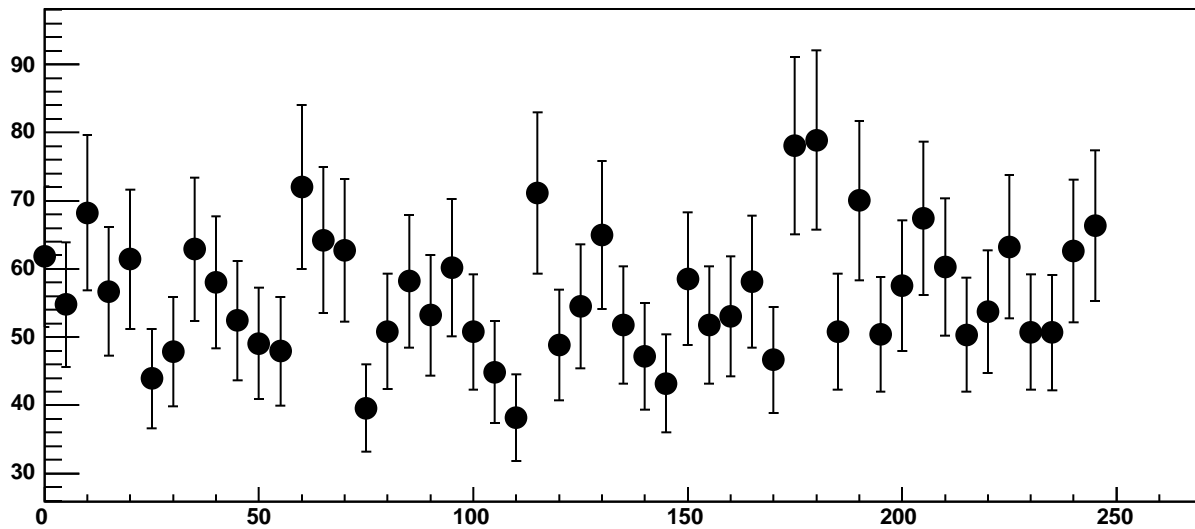


Chip 3, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

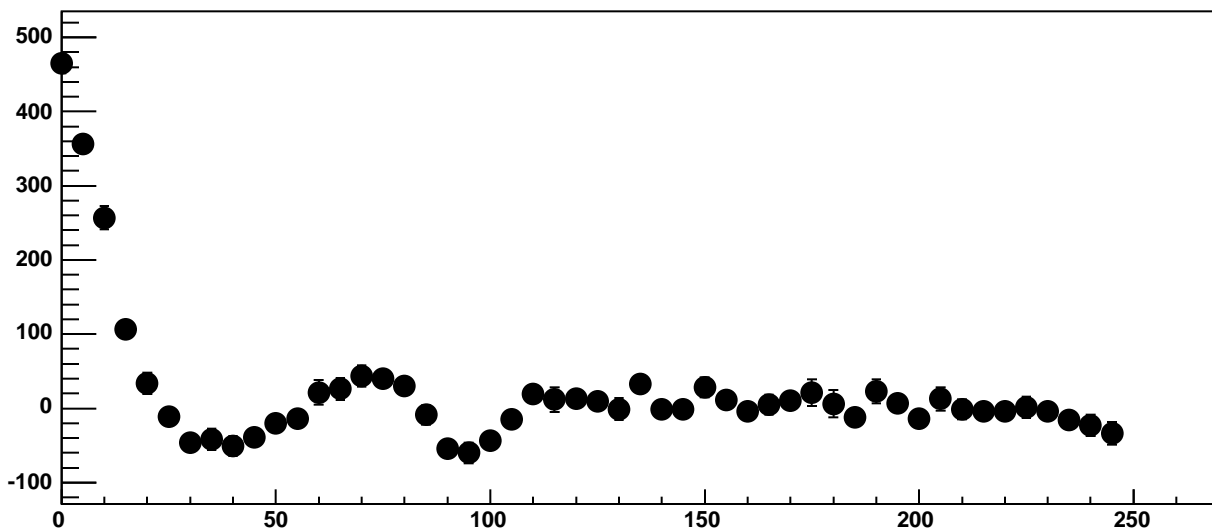


$\chi^2 / \text{ndf}$	259.2 / 41
p0	$-920.4 \pm 4.09$
p1	$92.06 \pm 0.5584$
p2	$-6.389\text{e}+08 \pm 7.725\text{e}+06$
p3	$4.842\text{e}+07 \pm 2.447\text{e}+05$
p4	$12.44 \pm 0.1317$

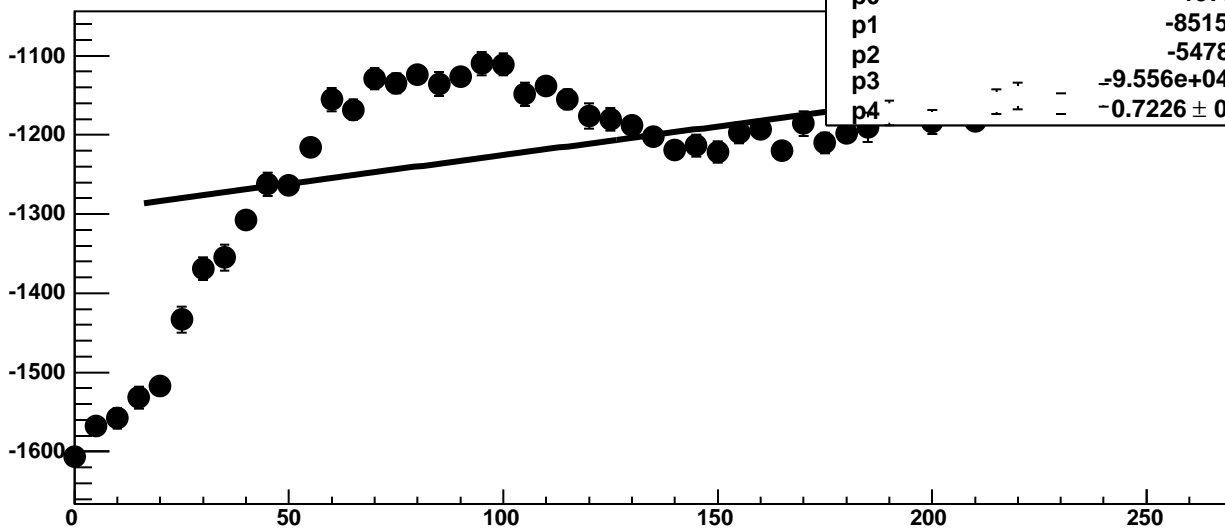
Chip 3, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



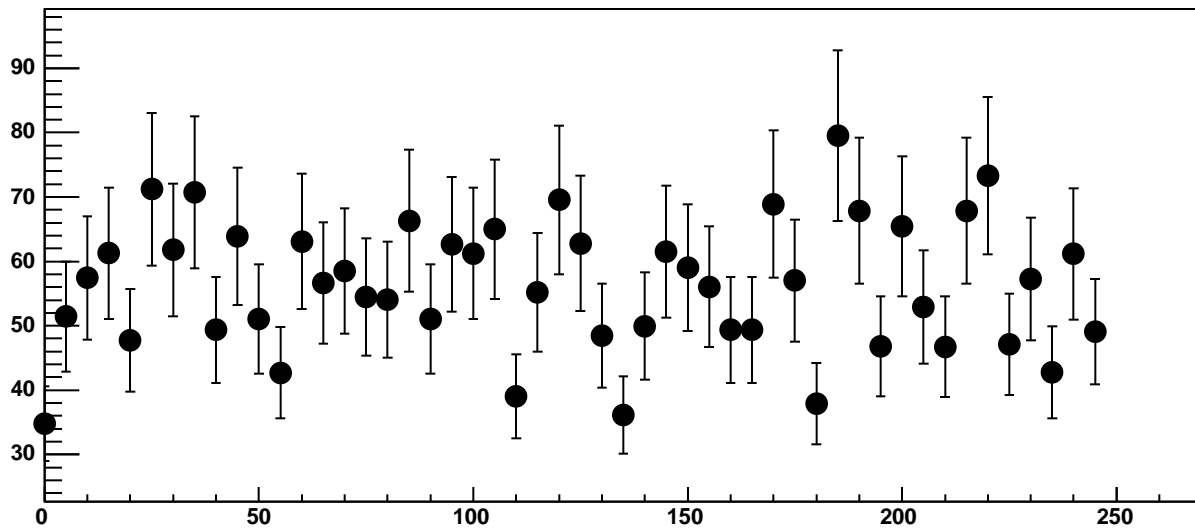
Chip 3, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



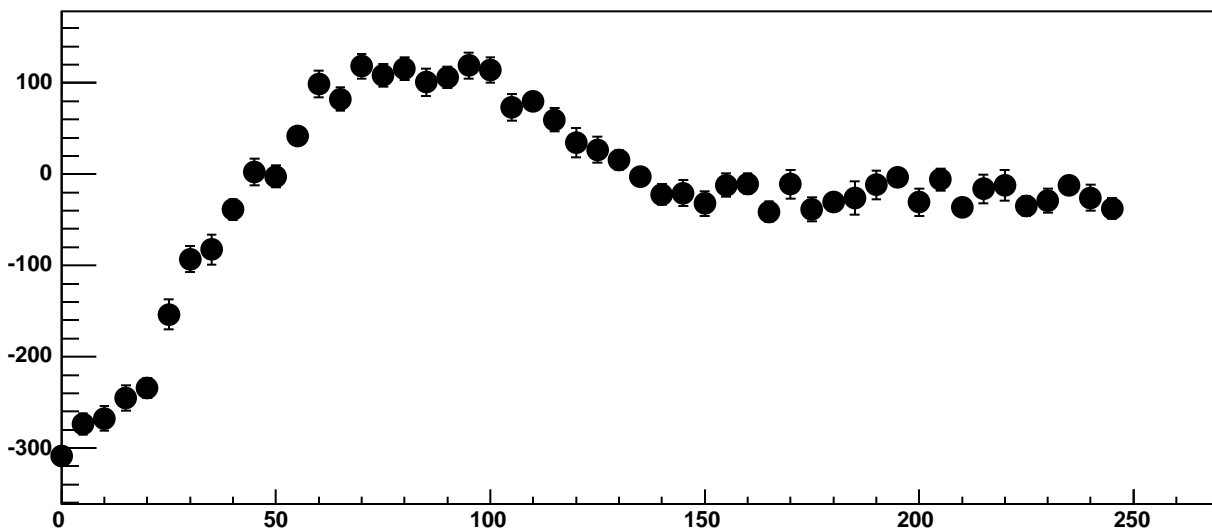
Chip 3, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold



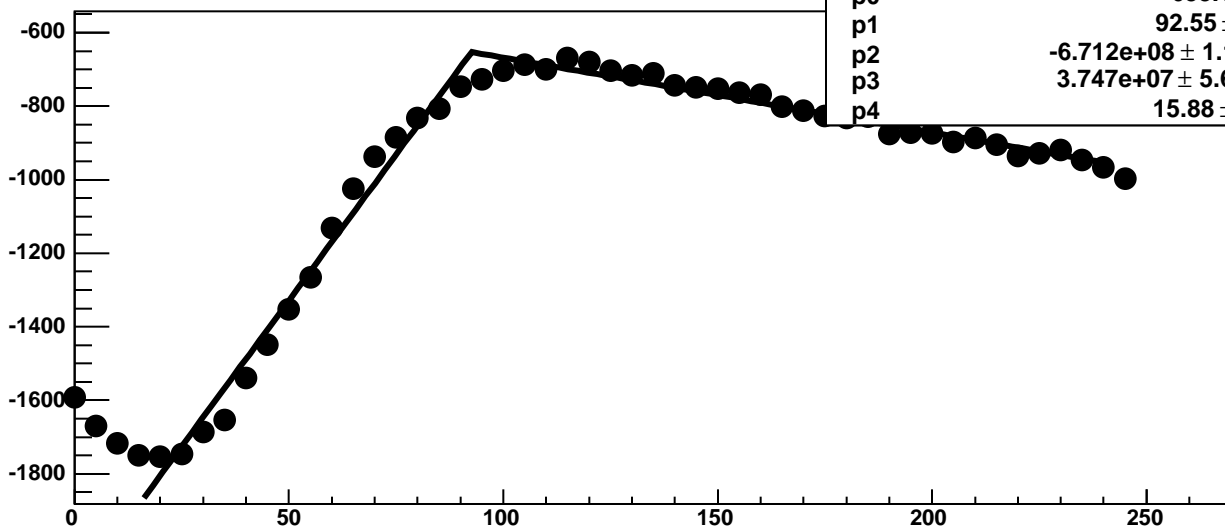
Chip 3, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold

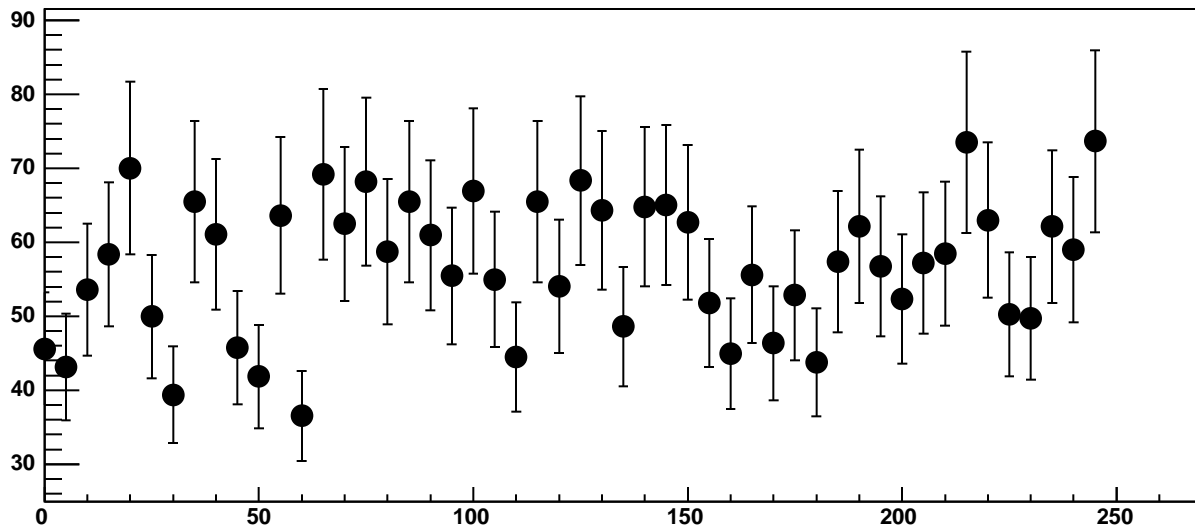


Chip 3, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

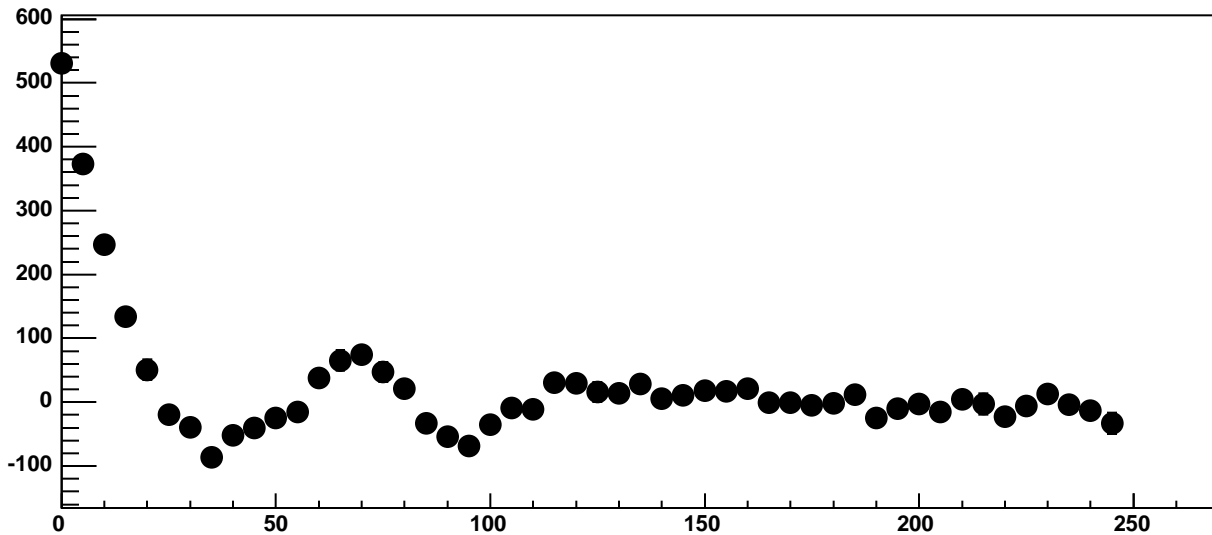


$\chi^2 / \text{ndf}$	370.4 / 41
p0	-653.1 ± 4.272
p1	92.55 ± 0.4658
p2	-6.712e+08 ± 1.172e+07
p3	3.747e+07 ± 5.664e+05
p4	15.88 ± 0.1456

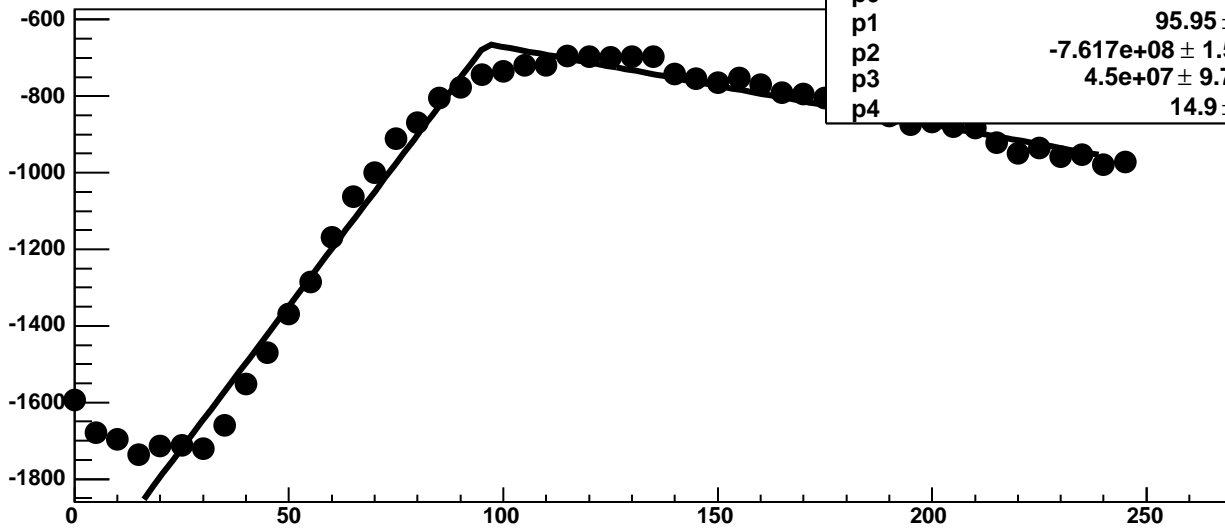
Chip 3, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

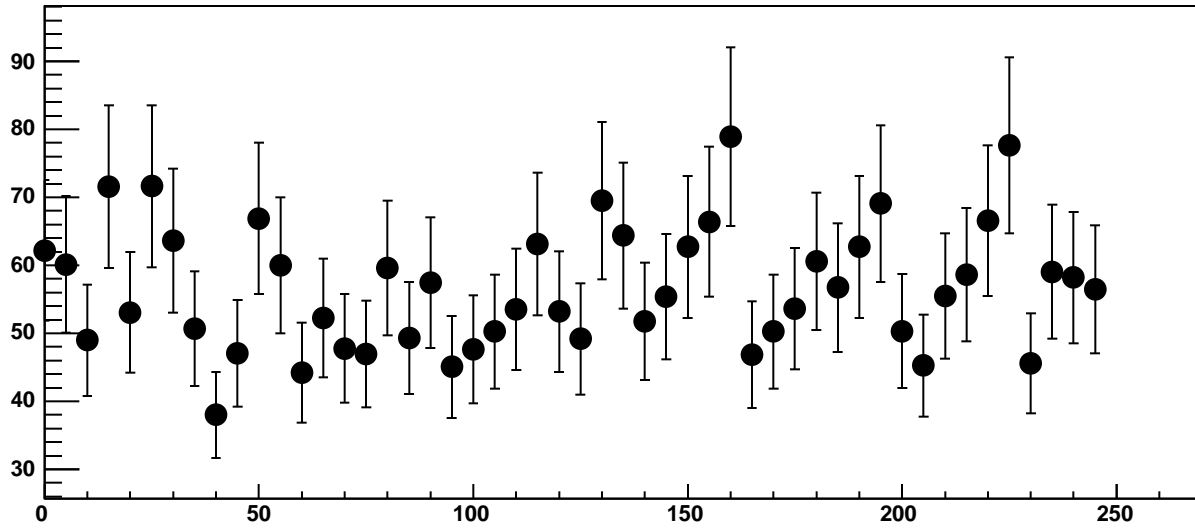


Chip 3, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

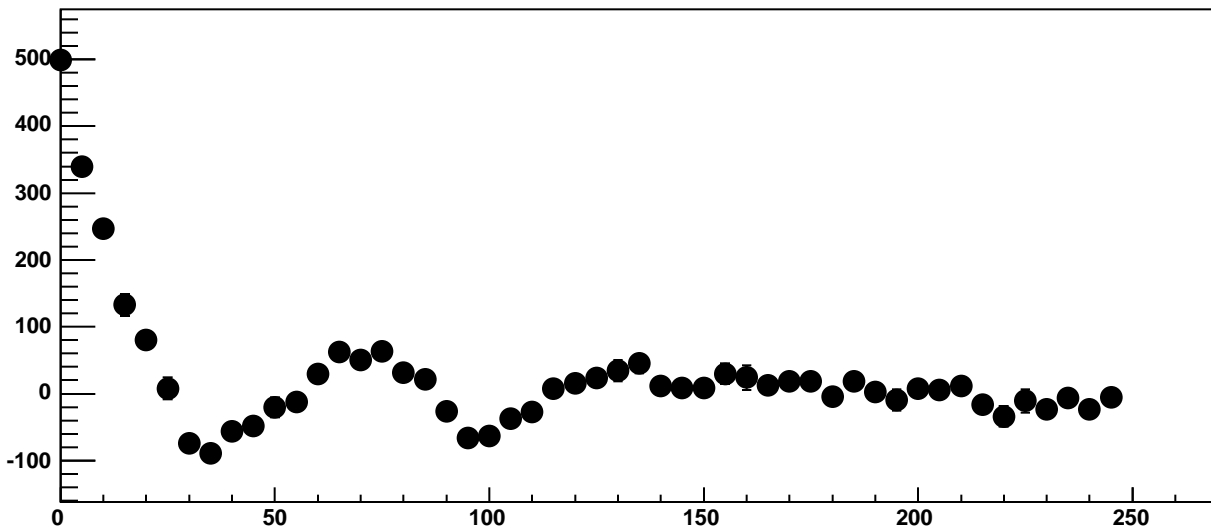


$\chi^2 / \text{ndf}$	505.3 / 41
p0	-663.1 ± 4.076
p1	95.95 ± 0.4142
p2	-7.617e+08 ± 1.518e+07
p3	4.5e+07 ± 9.723e+05
p4	14.9 ± 0.1162

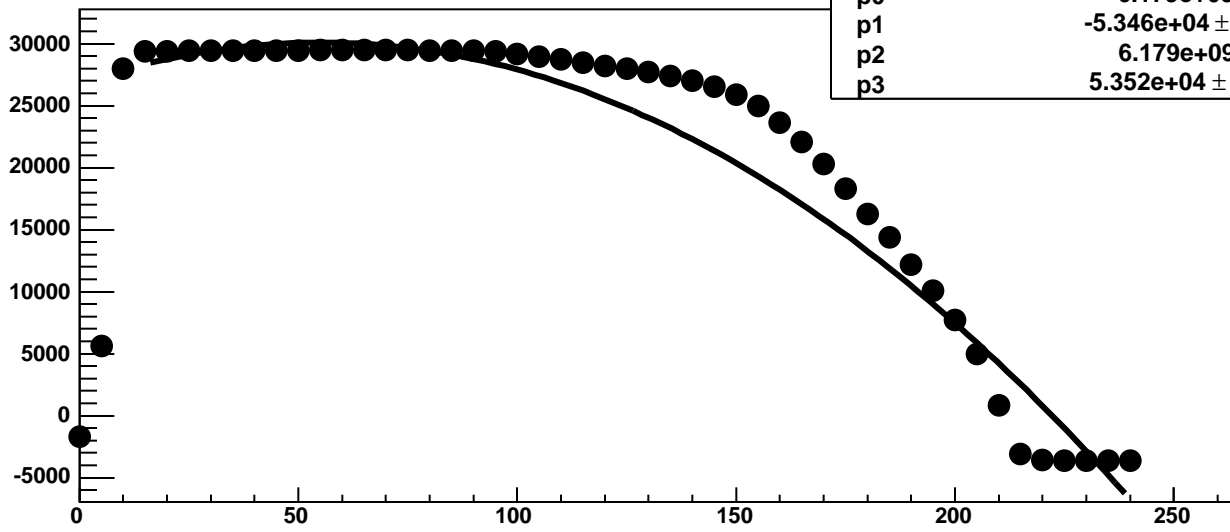
Chip 3, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

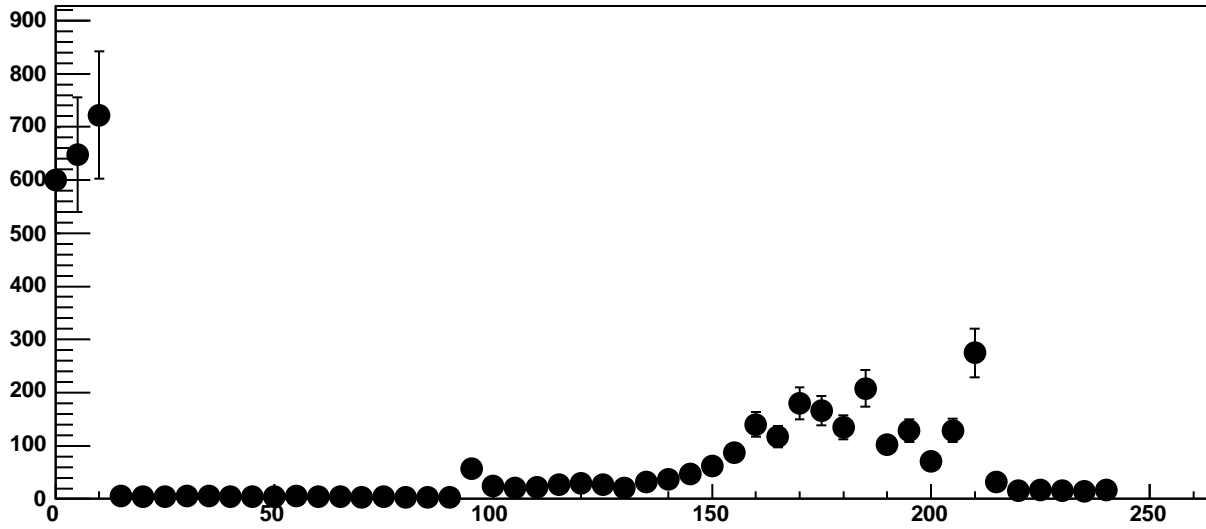


Chip 3, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold

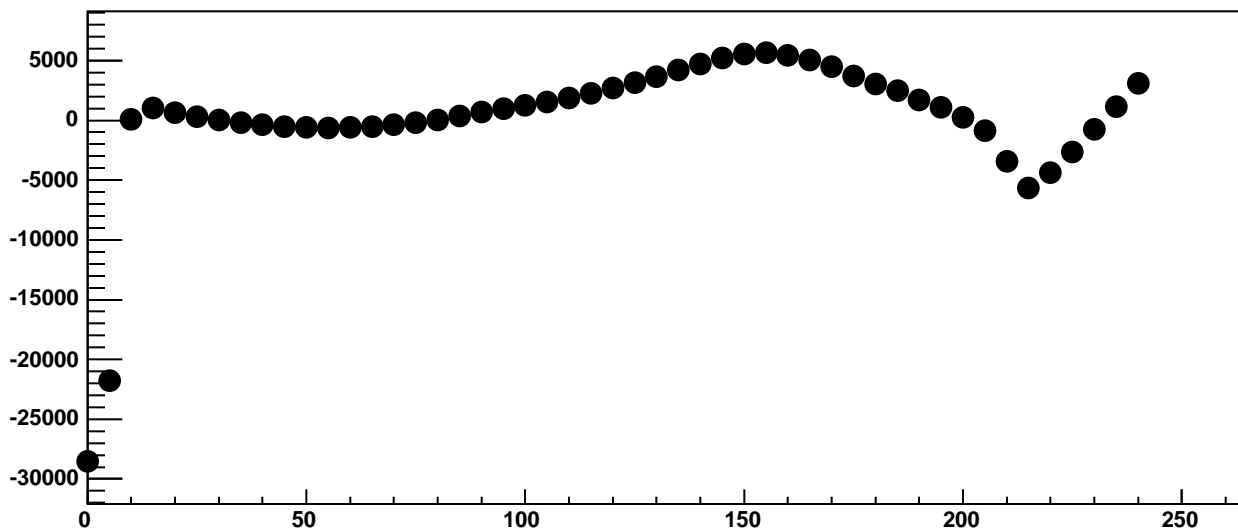


$\chi^2 / \text{ndf}$	1.022e+07 / 42
p0	-6.179e+09 $\pm$ 3.149
p1	-5.346e+04 $\pm$ 0.03781
p2	6.179e+09 $\pm$ 3.149
p3	5.352e+04 $\pm$ 0.03774

Chip 3, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

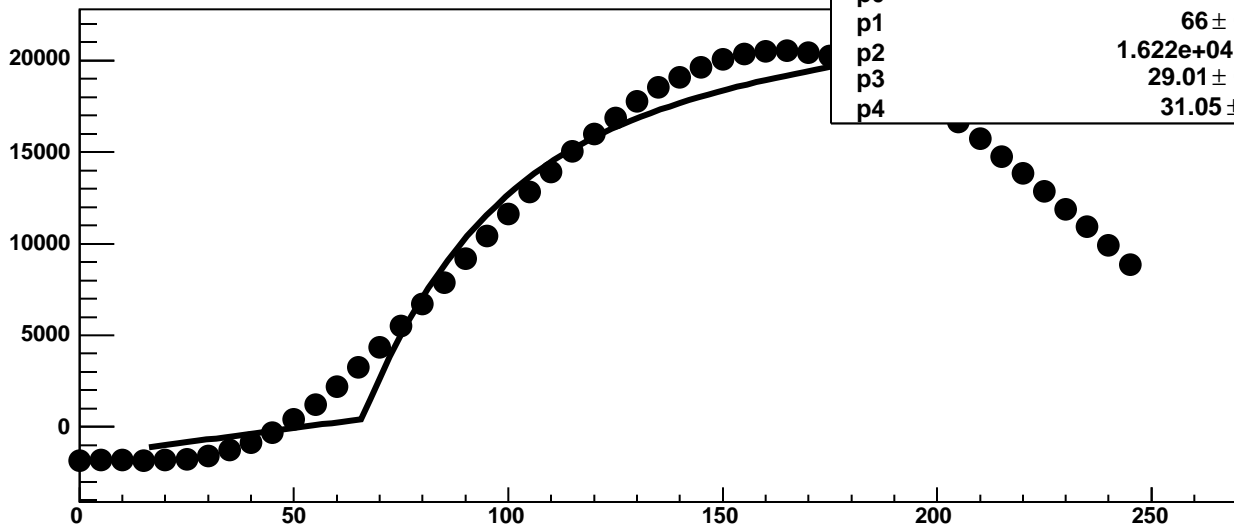


Chip 3, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold



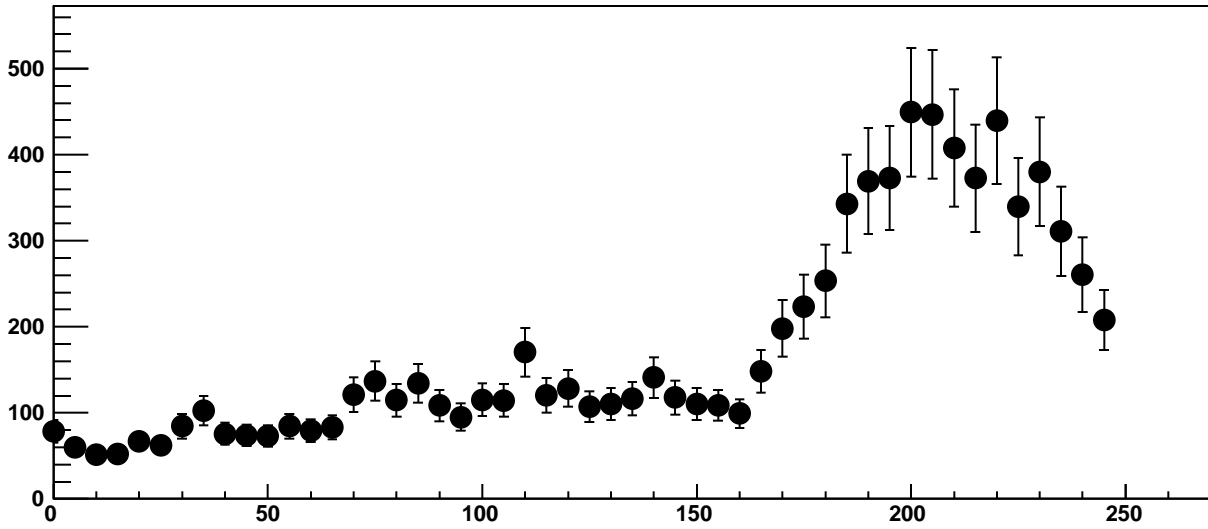


Chip 3, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold

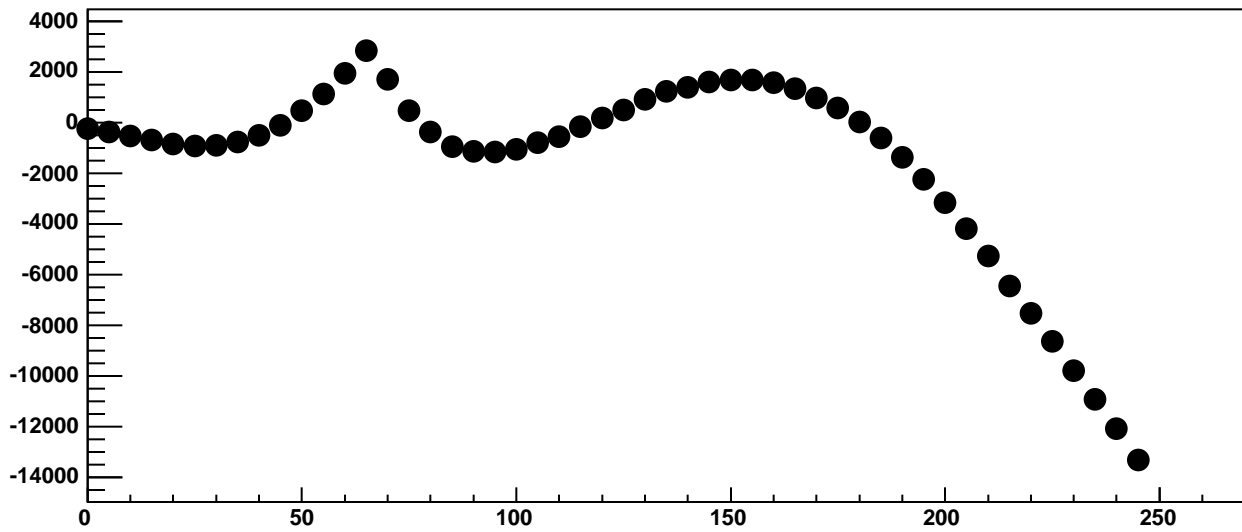


$\chi^2 / \text{ndf}$	1.972e+05 / 41
p0	434.4 ± 9.145
p1	66 ± 0.04744
p2	1.622e+04 ± 35.25
p3	29.01 ± 0.08984
p4	31.05 ± 0.2353

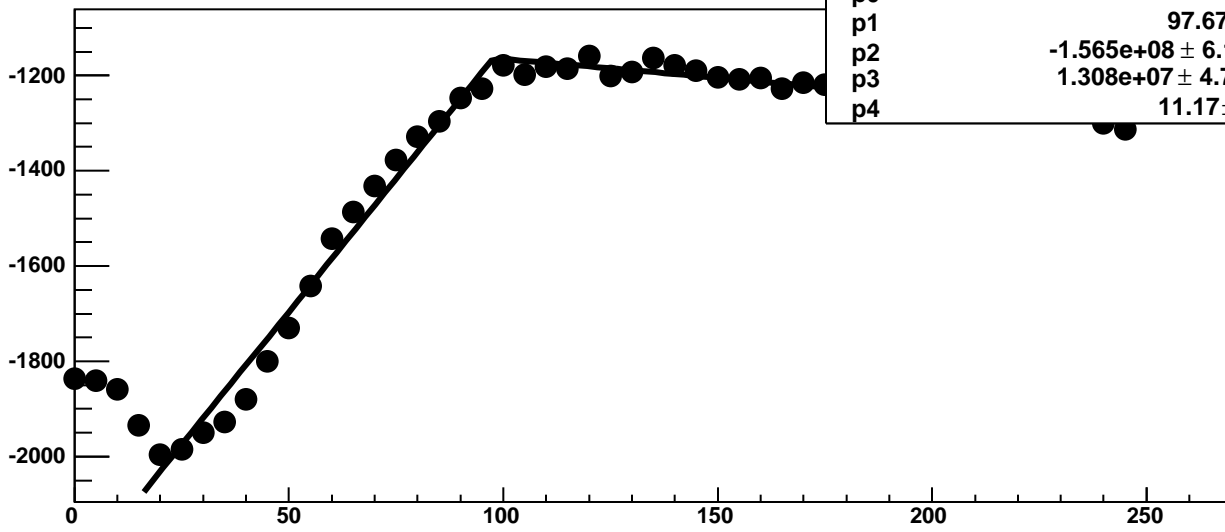
Chip 3, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold

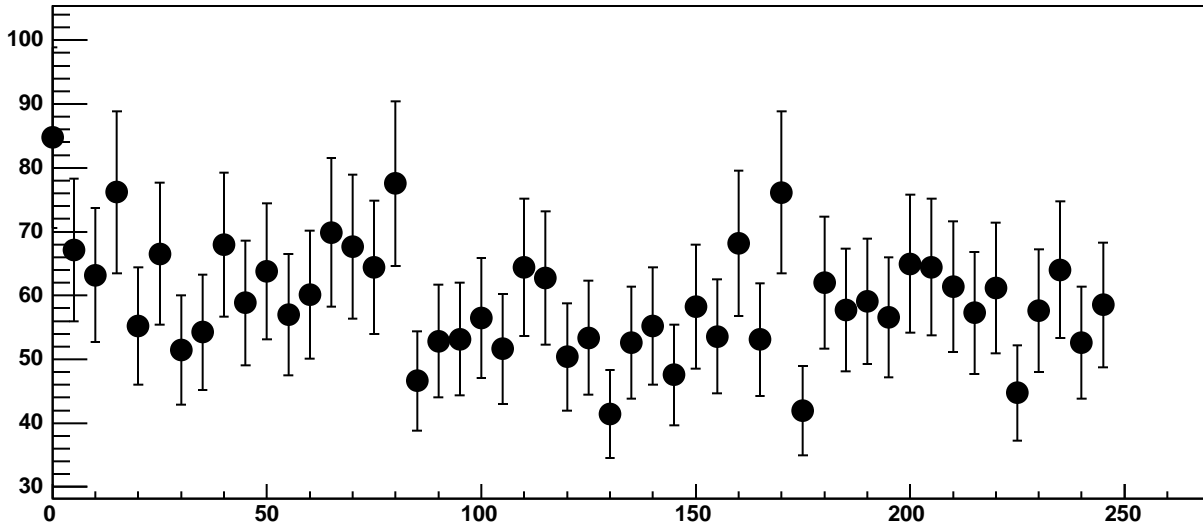


Chip 3, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

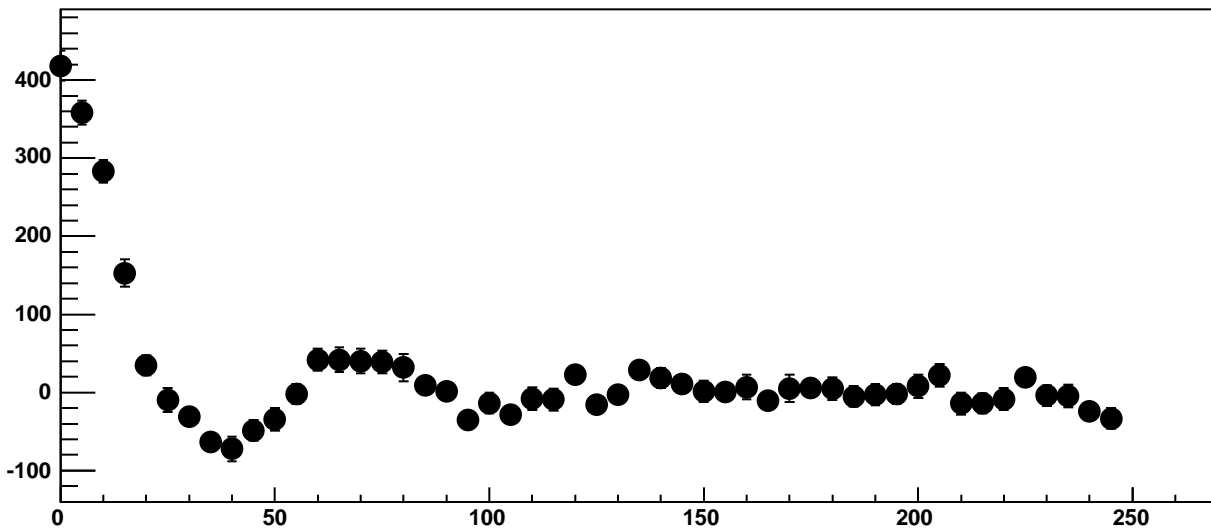


$\chi^2 / \text{ndf}$	236.2 / 41
p0	-1163 ± 4.354
p1	97.67 ± 0.659
p2	-1.565e+08 ± 6.141e+06
p3	1.308e+07 ± 4.743e+05
p4	11.17 ± 0.1327

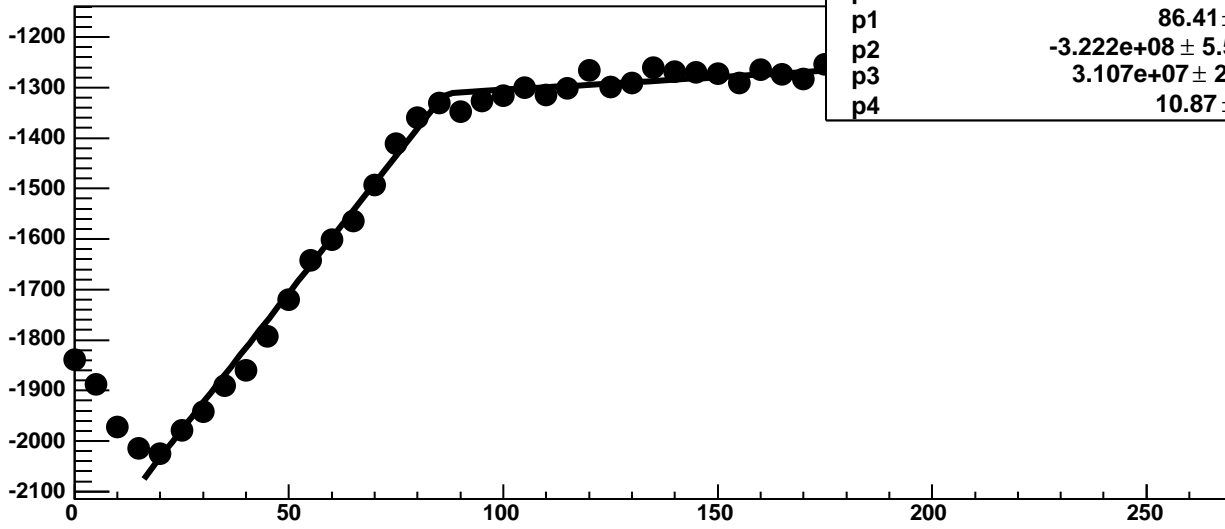
Chip 3, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

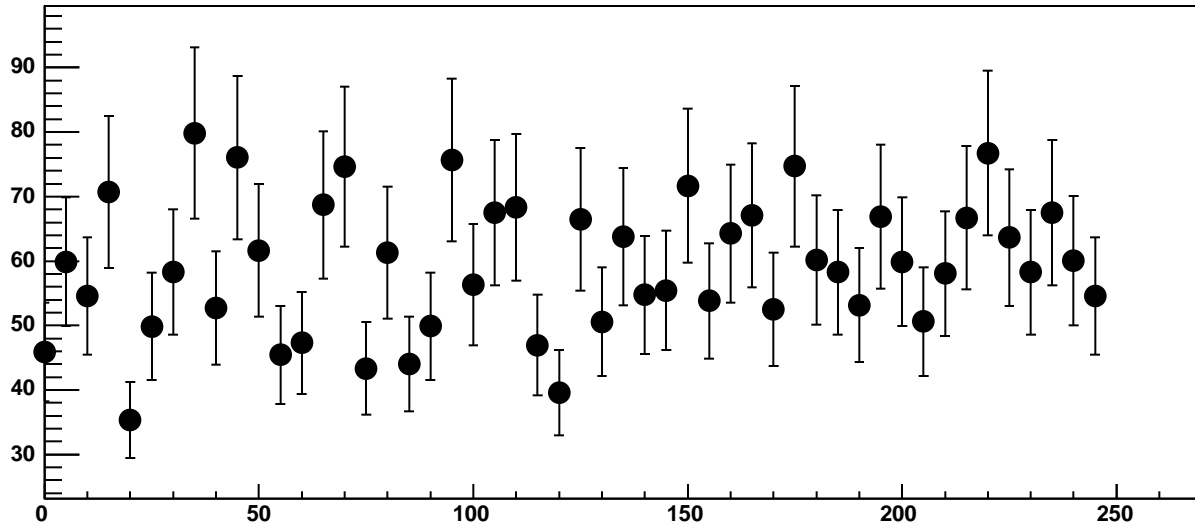


Chip 3, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

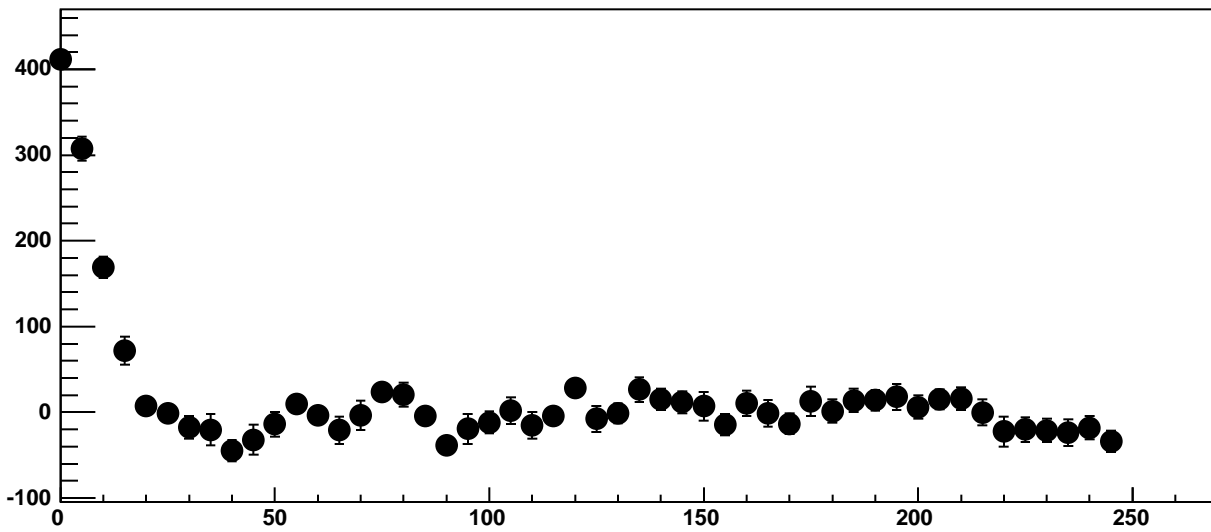


$\chi^2 / \text{ndf}$	103.4 / 41
p0	-1311 ± 4.978
p1	86.41 ± 0.7318
p2	-3.222e+08 ± 5.514e+06
p3	3.107e+07 ± 2.87e+05
p4	10.87 ± 0.1373

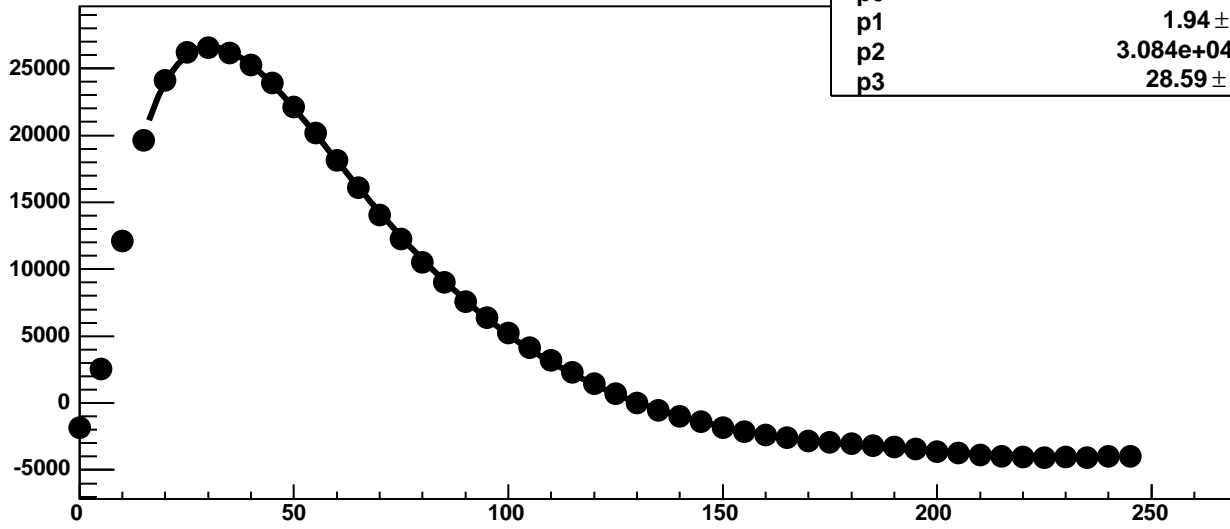
Chip 3, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



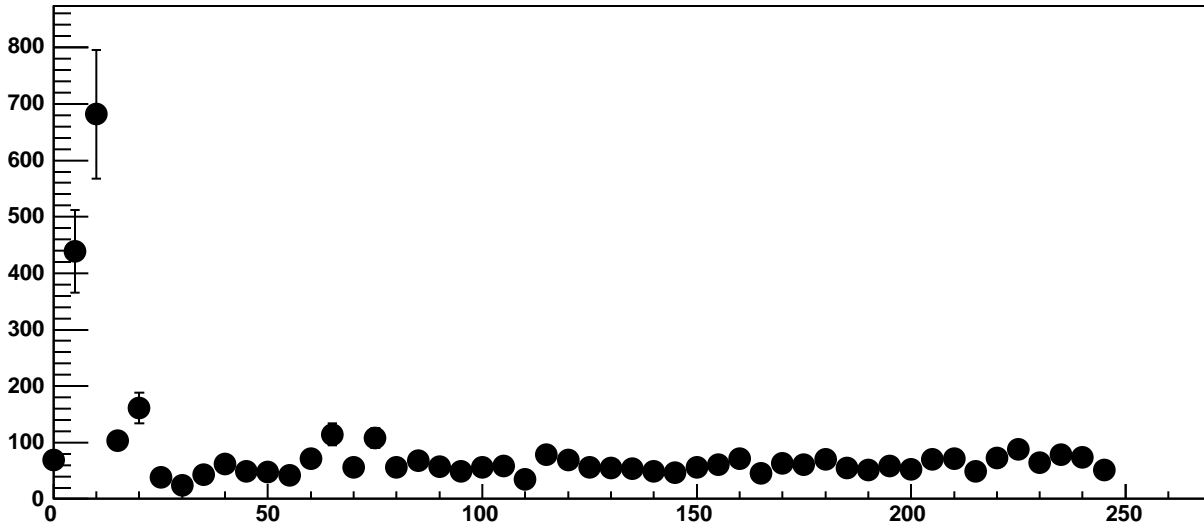
Chip 3, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold



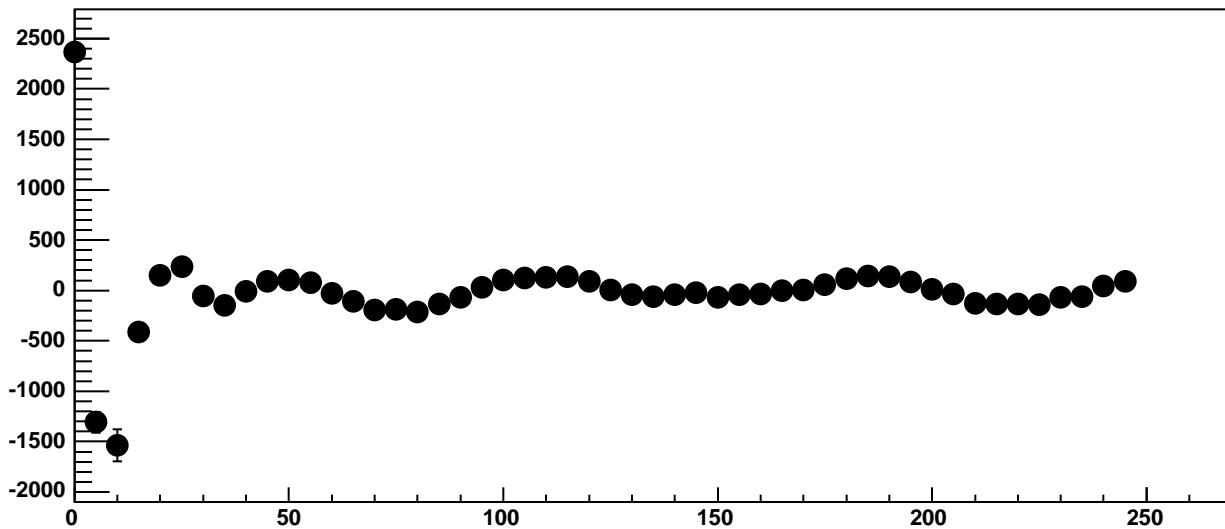
Chip 3, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold



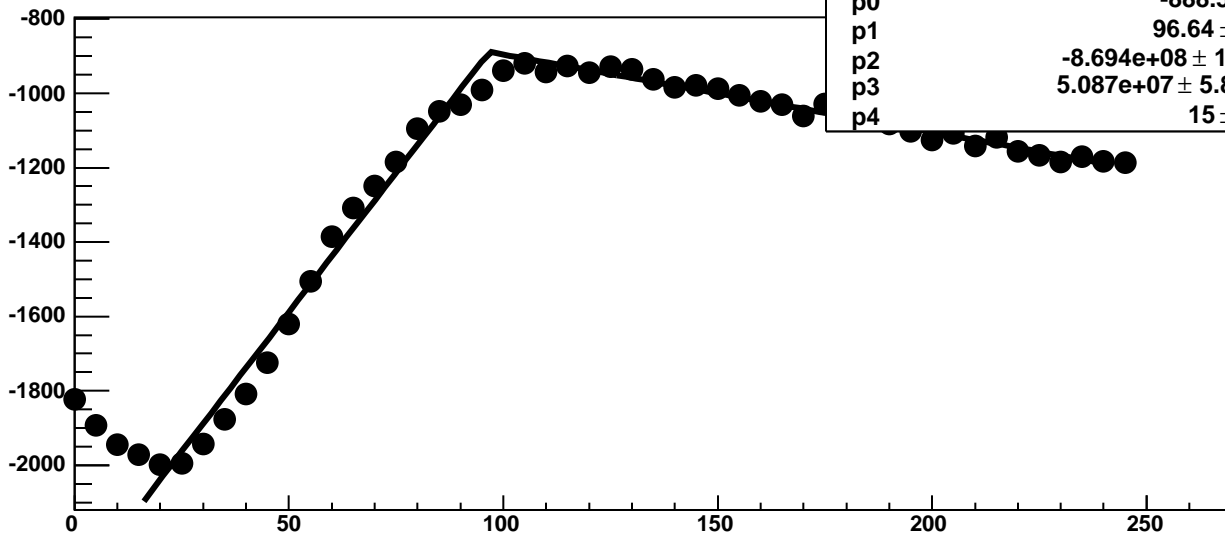
Chip 3, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold

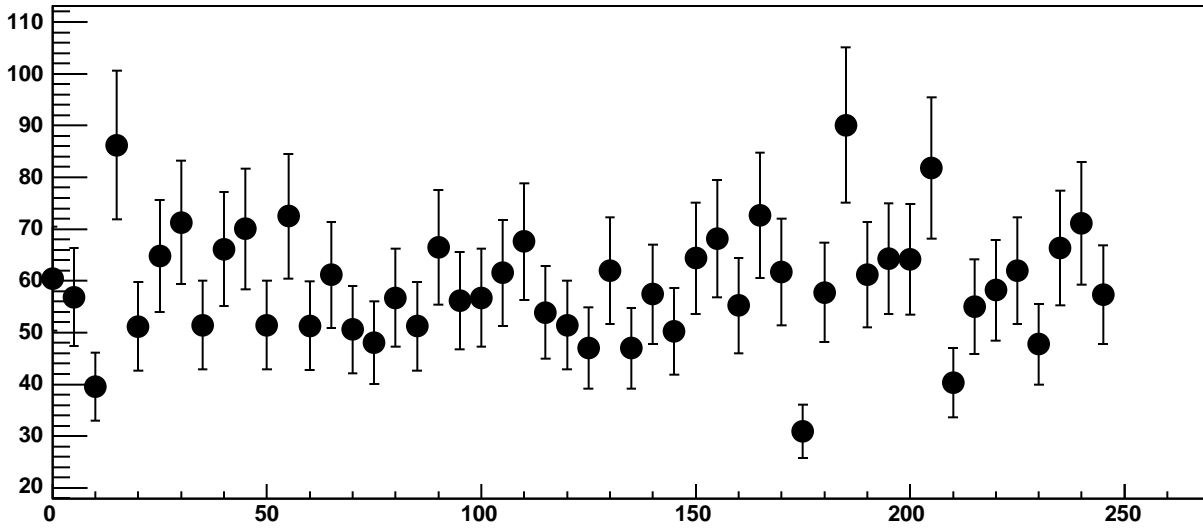


Chip 3, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

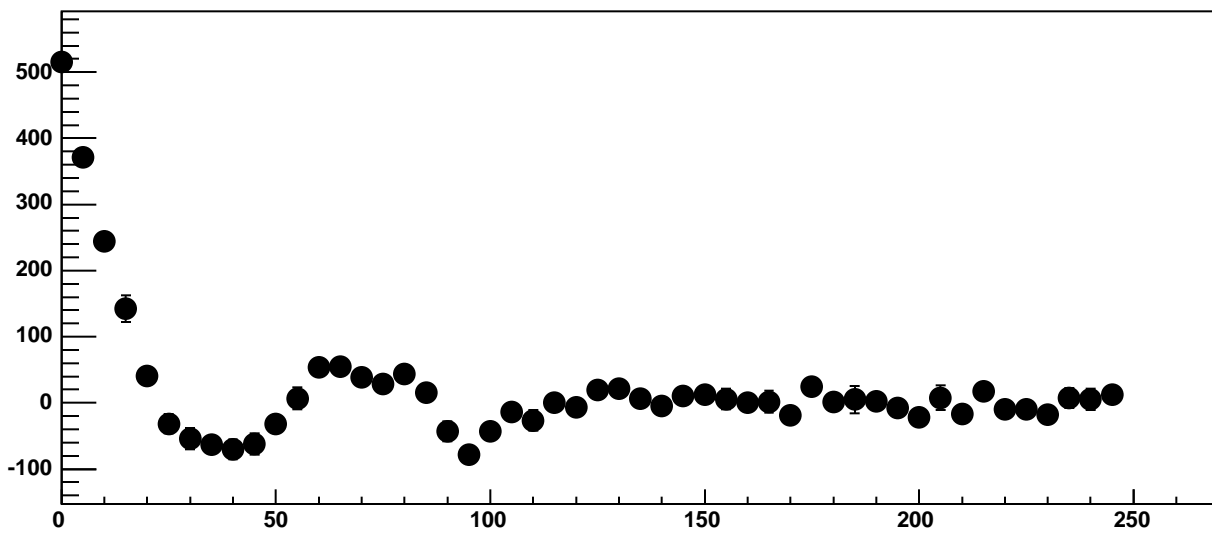


$\chi^2 / \text{ndf}$	311.2 / 41
p0	-888.5 ± 4.316
p1	96.64 ± 0.4625
p2	-8.694e+08 ± 1.22e+07
p3	5.087e+07 ± 5.807e+05
p4	15 ± 0.1364

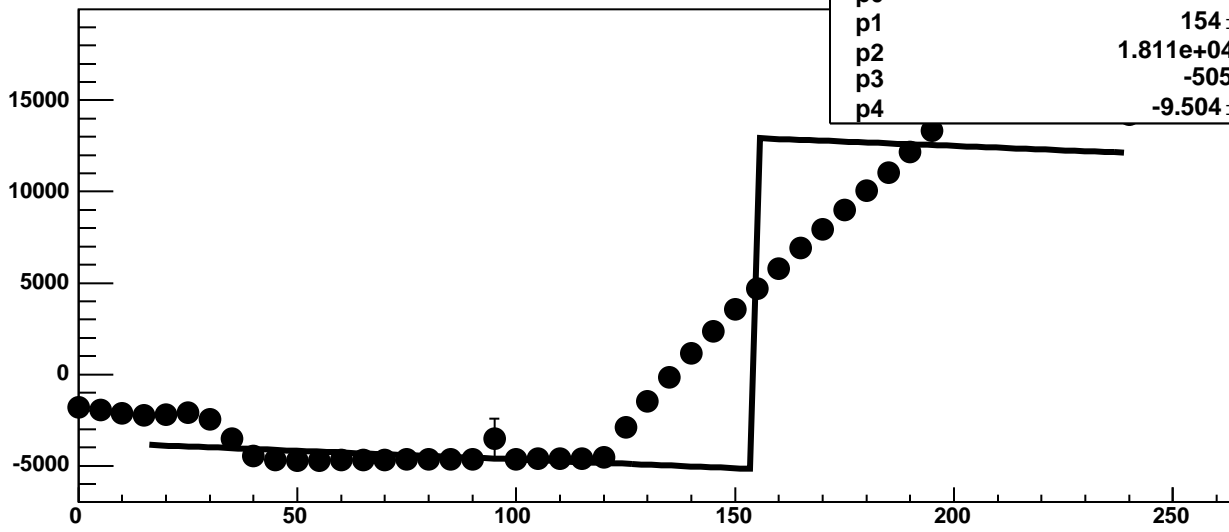
Chip 3, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



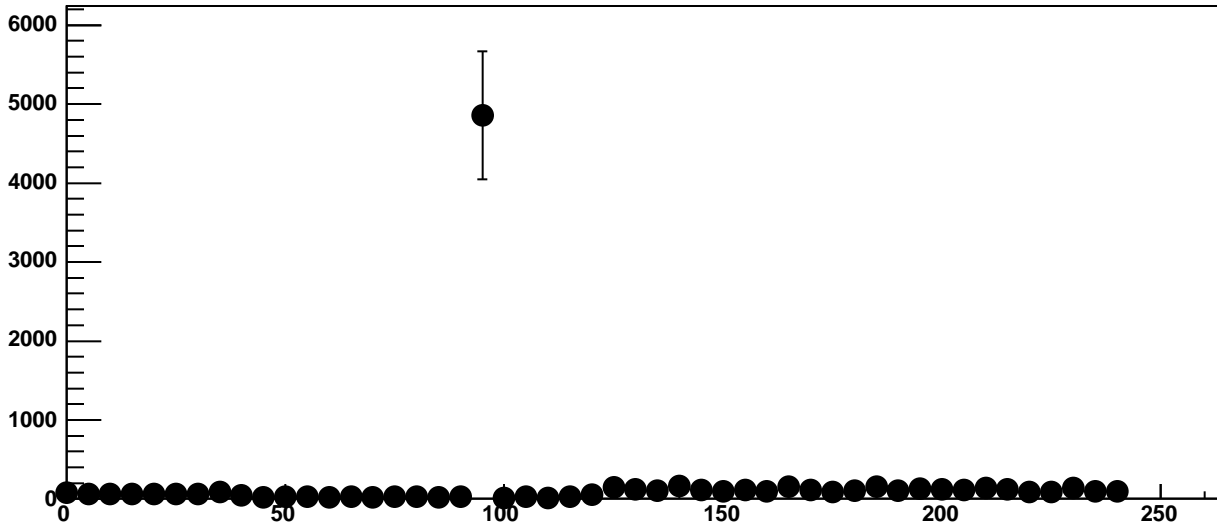
Chip 3, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold



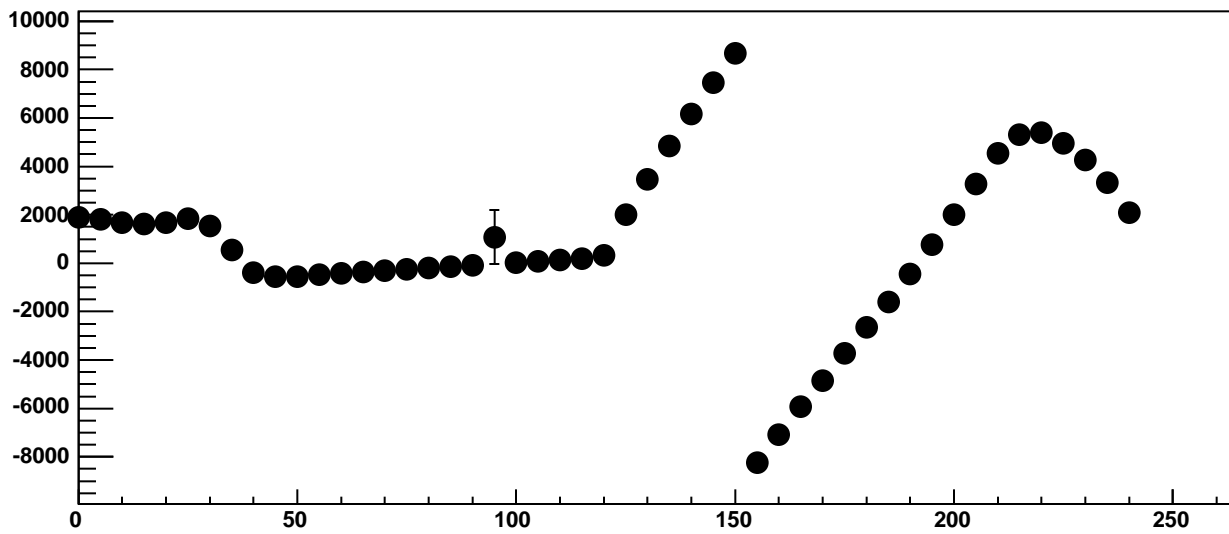
Chip 3, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 3, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold

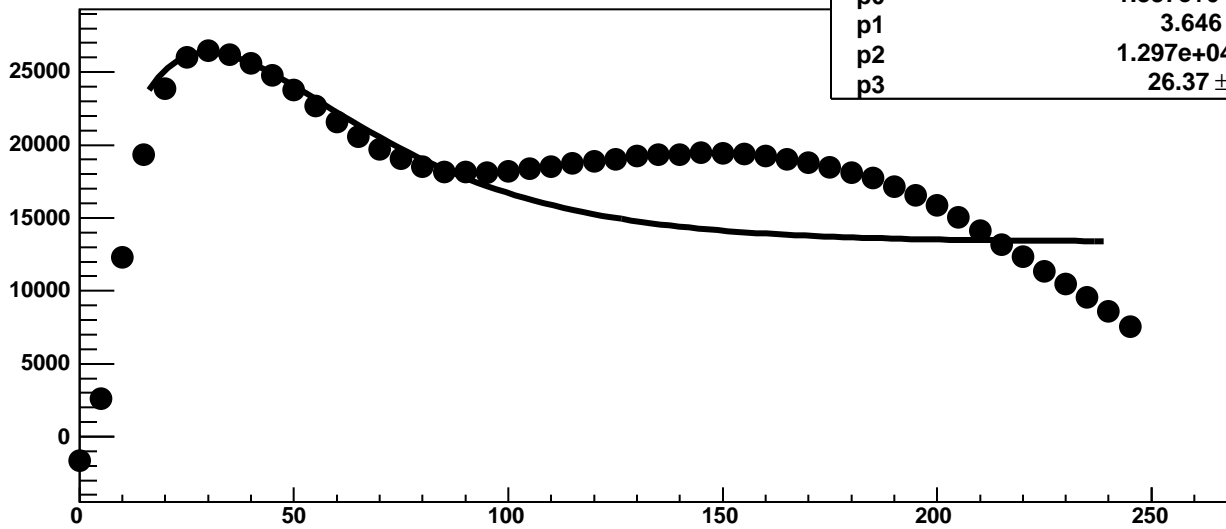


Chip 3, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

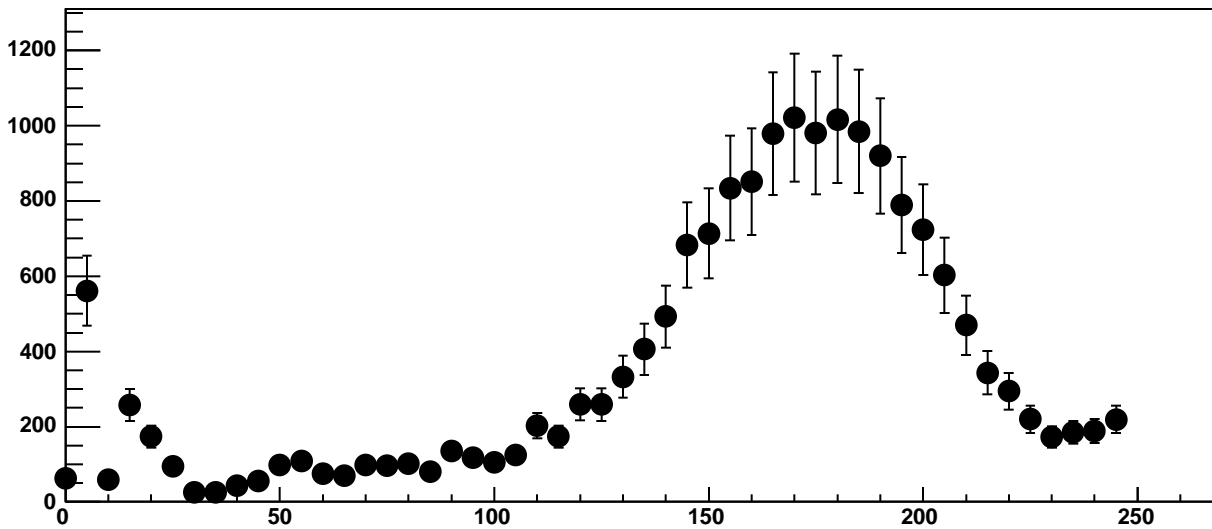


Chip 3, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

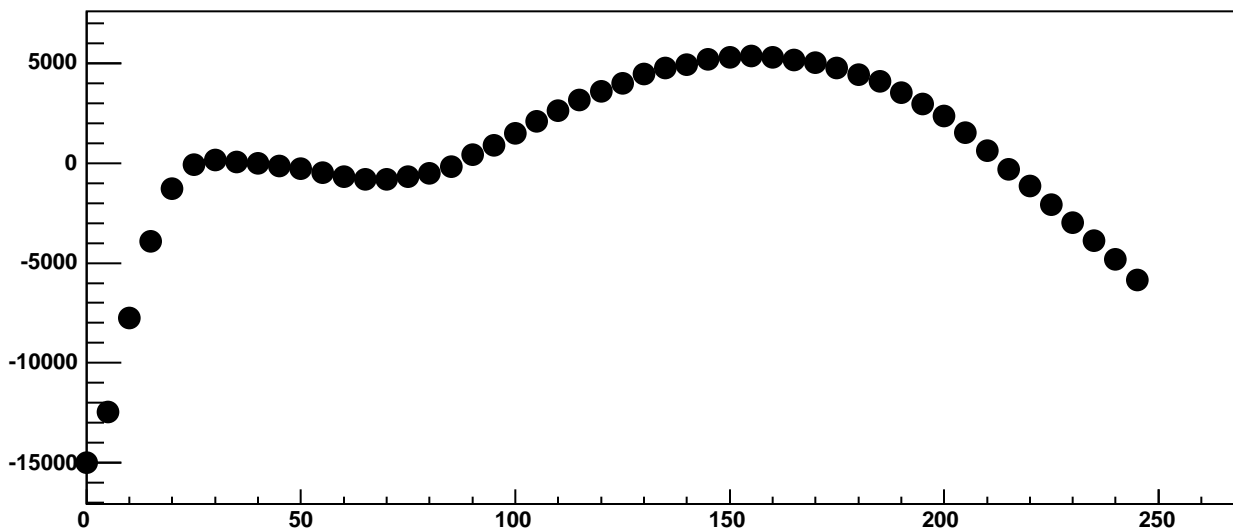
$\chi^2 / \text{ndf}$	8.502e+04 / 42
p0	1.337e+04 $\pm$ 23.05
p1	3.646 $\pm$ 0.1303
p2	1.297e+04 $\pm$ 23.04
p3	26.37 $\pm$ 0.08701



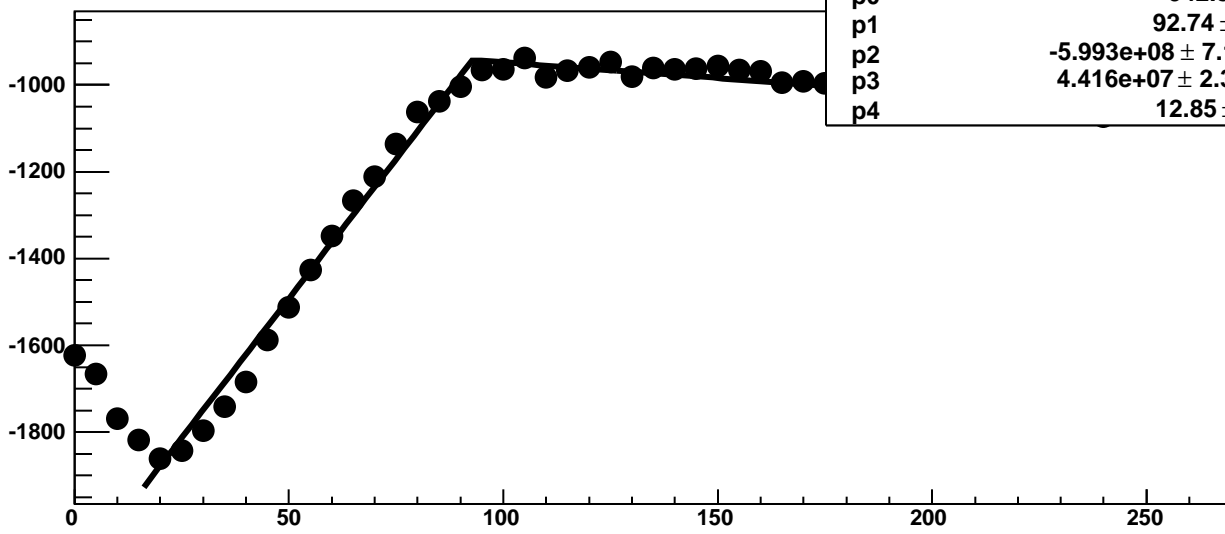
Chip 3, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

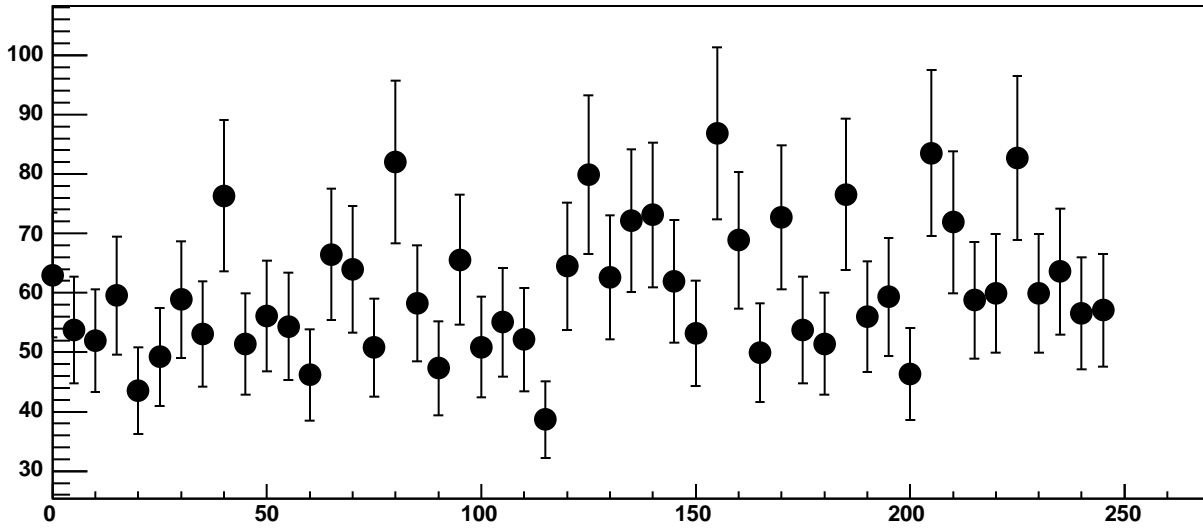


Chip 3, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

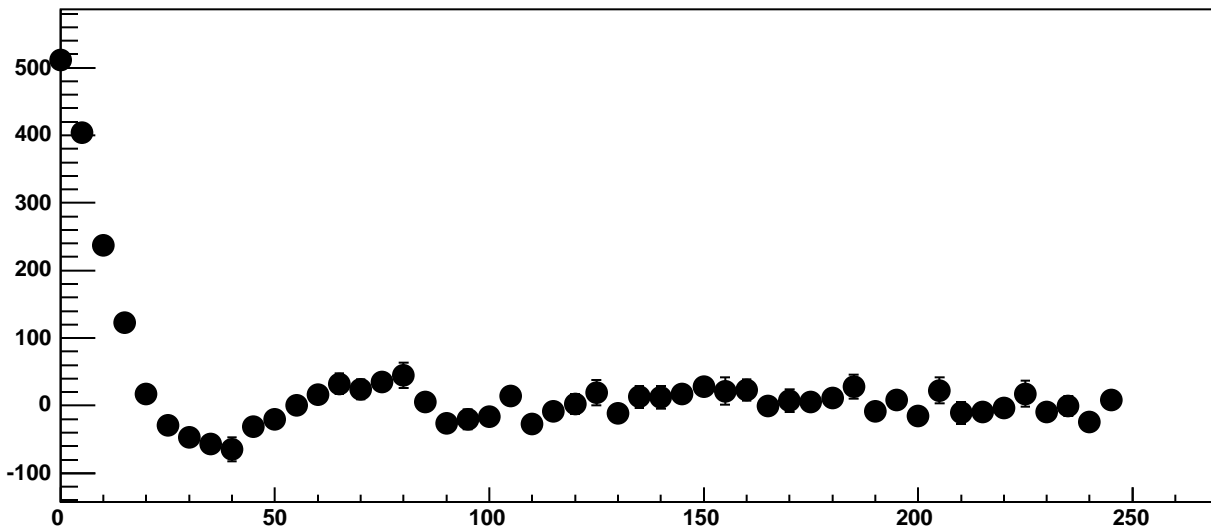


$\chi^2 / \text{ndf}$	216.5 / 41
p0	-942.8 ± 4.526
p1	92.74 ± 0.5855
p2	-5.993e+08 ± 7.103e+06
p3	4.416e+07 ± 2.396e+05
p4	12.85 ± 0.1333

Chip 3, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold

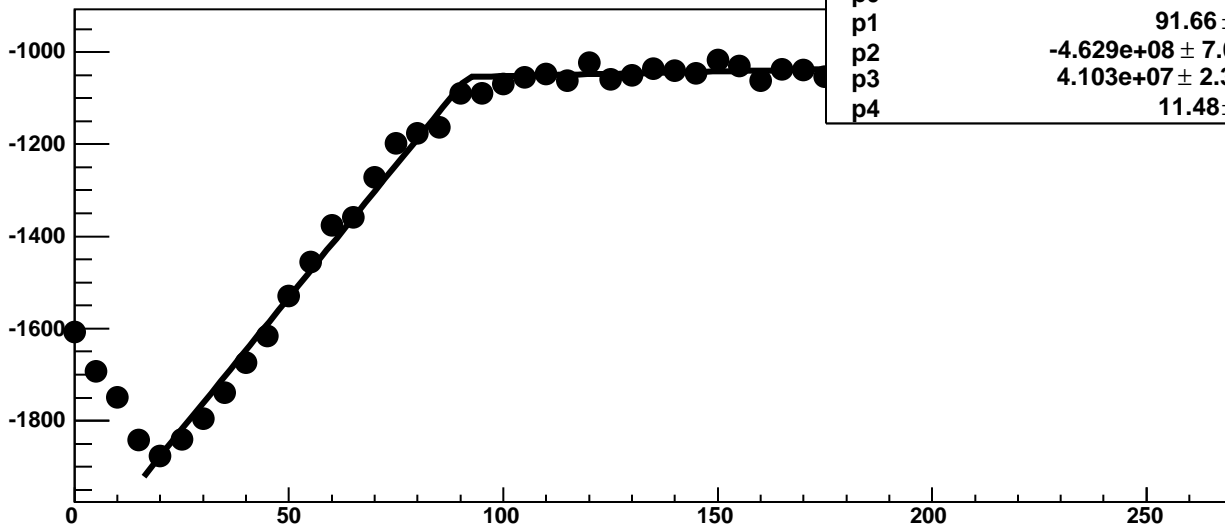


Chip 3, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold



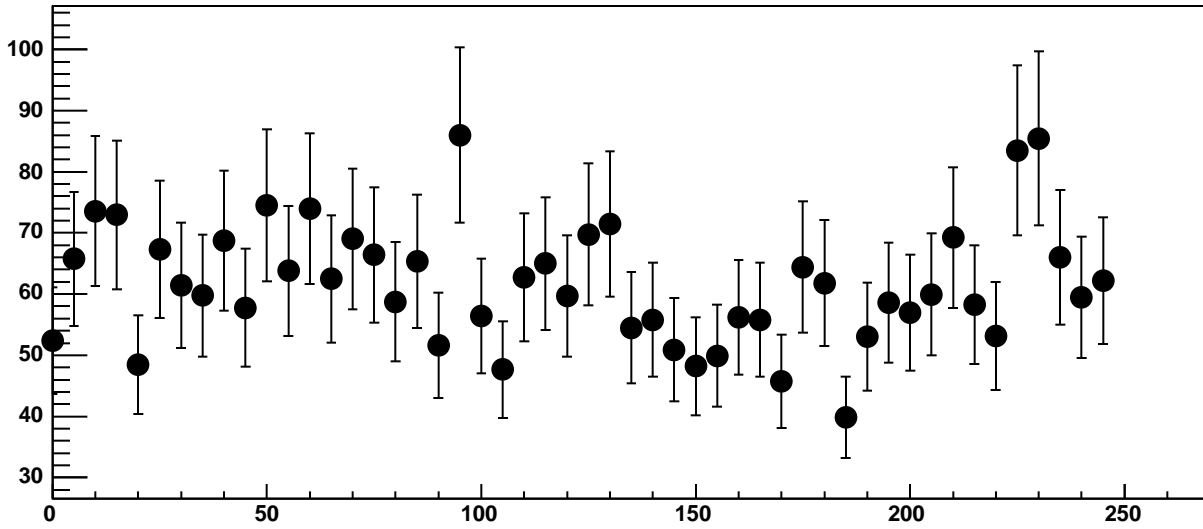


Chip 3, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

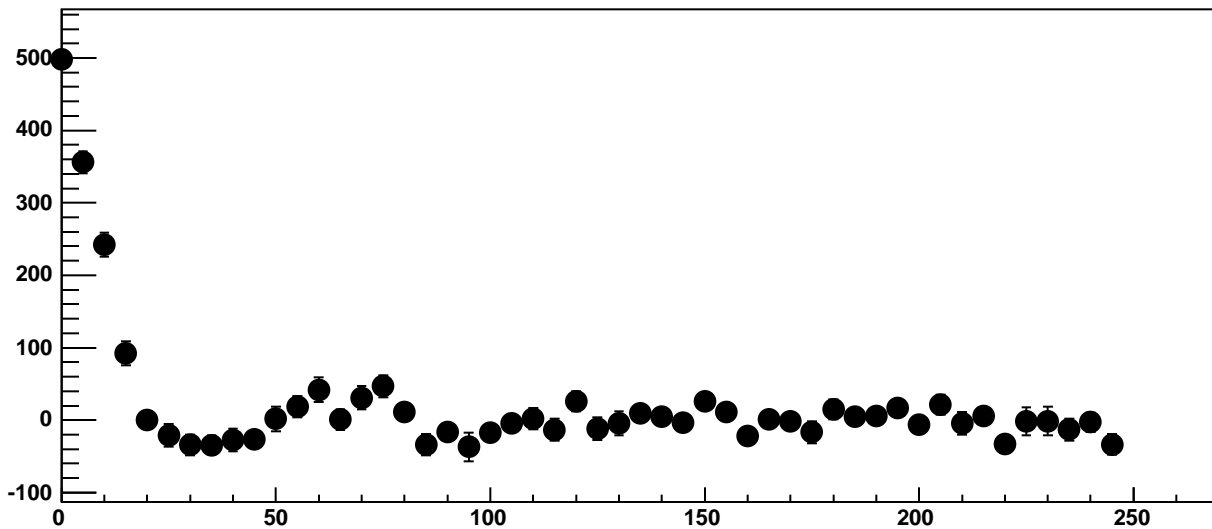


$\chi^2 / \text{ndf}$	115.9 / 41
p0	-1054 ± 5.183
p1	91.66 ± 0.7549
p2	-4.629e+08 ± 7.012e+06
p3	4.103e+07 ± 2.322e+05
p4	11.48 ± 0.1488

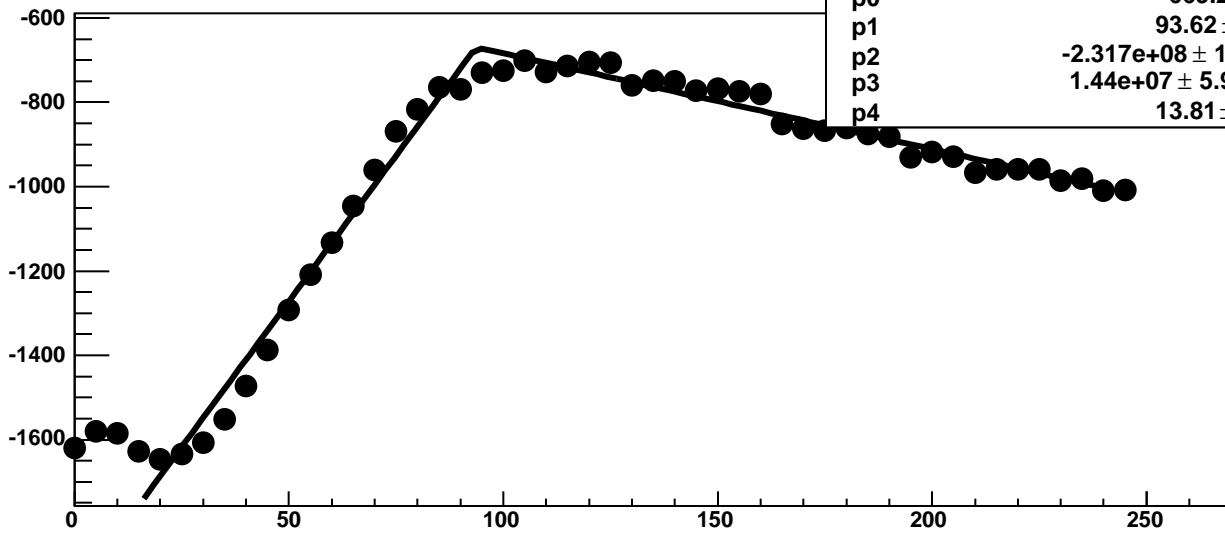
Chip 3, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

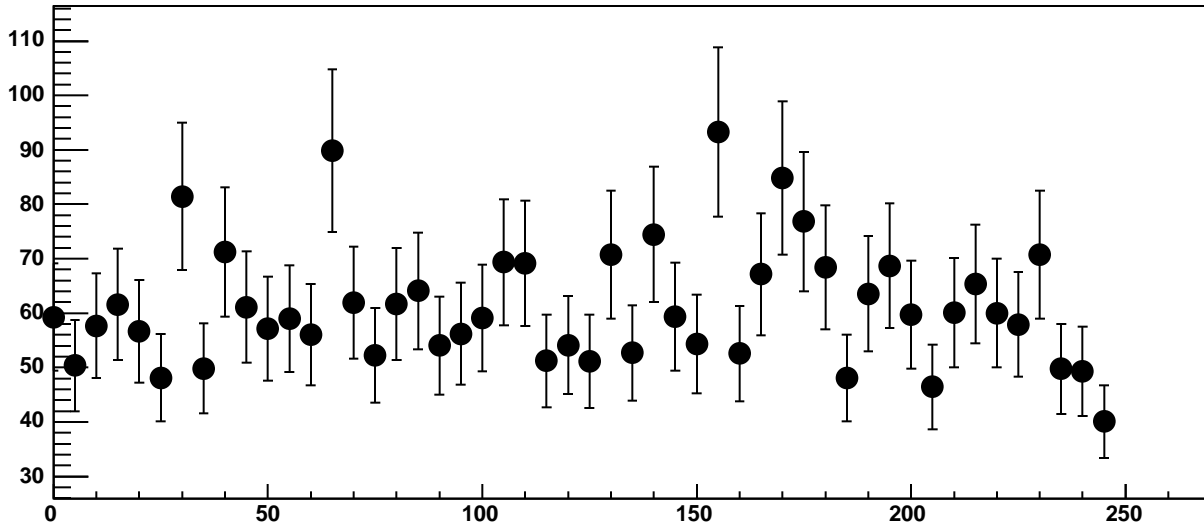


Chip 3, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold

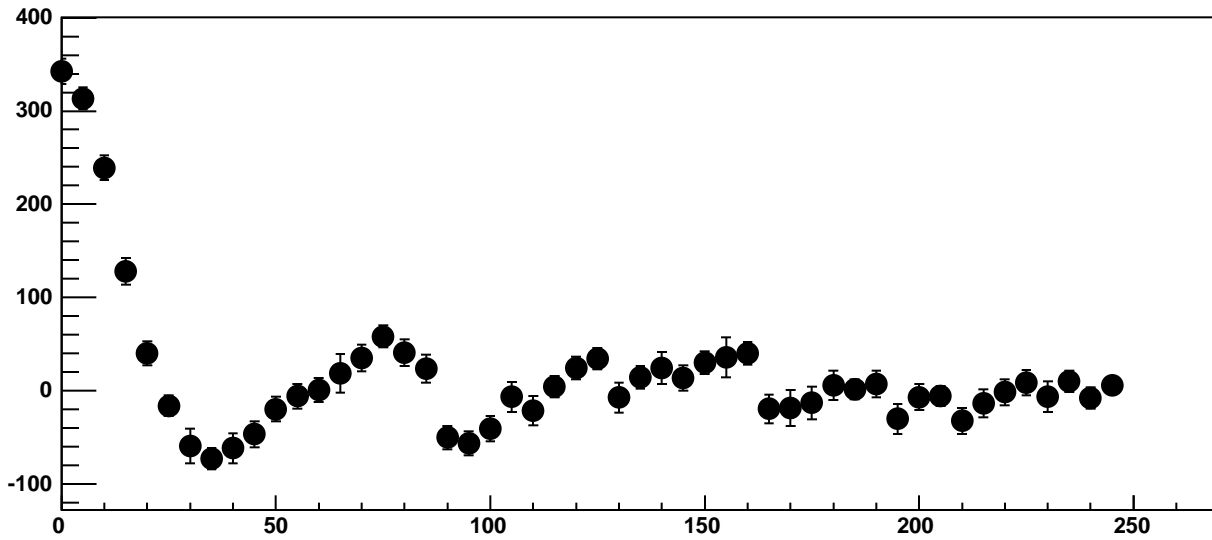


$\chi^2 / \text{ndf}$	313.2 / 41
p0	$-669.2 \pm 4.328$
p1	$93.62 \pm 0.5263$
p2	$-2.317\text{e}+08 \pm 1.01\text{e}+07$
p3	$1.44\text{e}+07 \pm 5.965\text{e}+05$
p4	$13.81 \pm 0.1445$

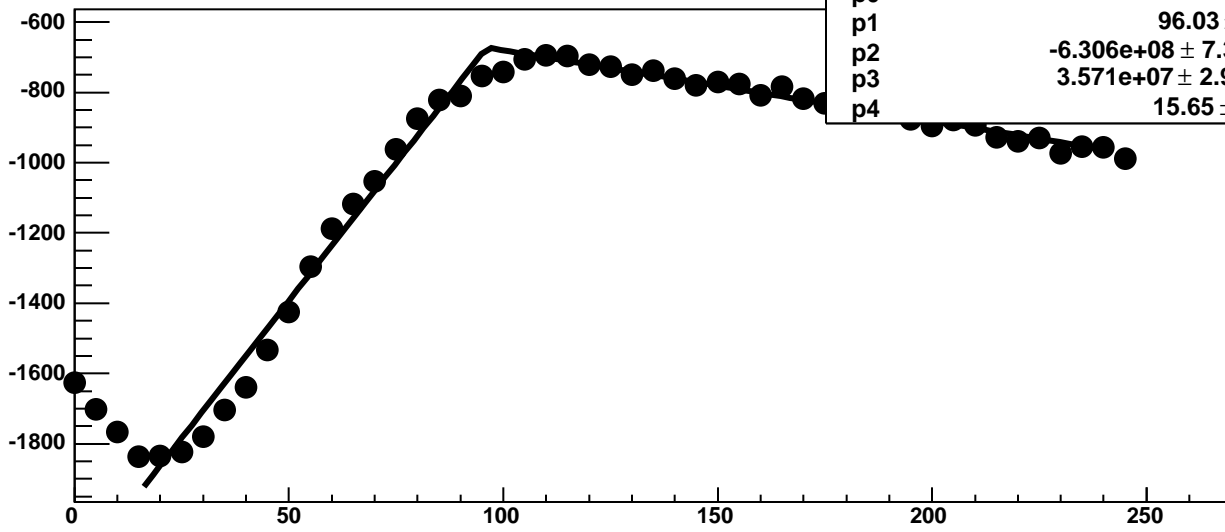
Chip 3, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



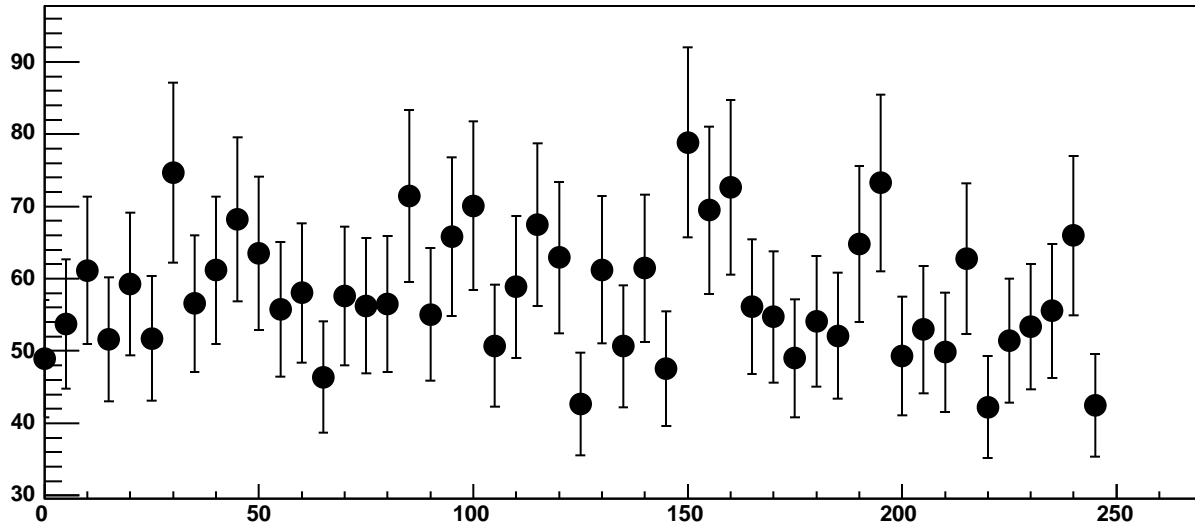
Chip 3, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold



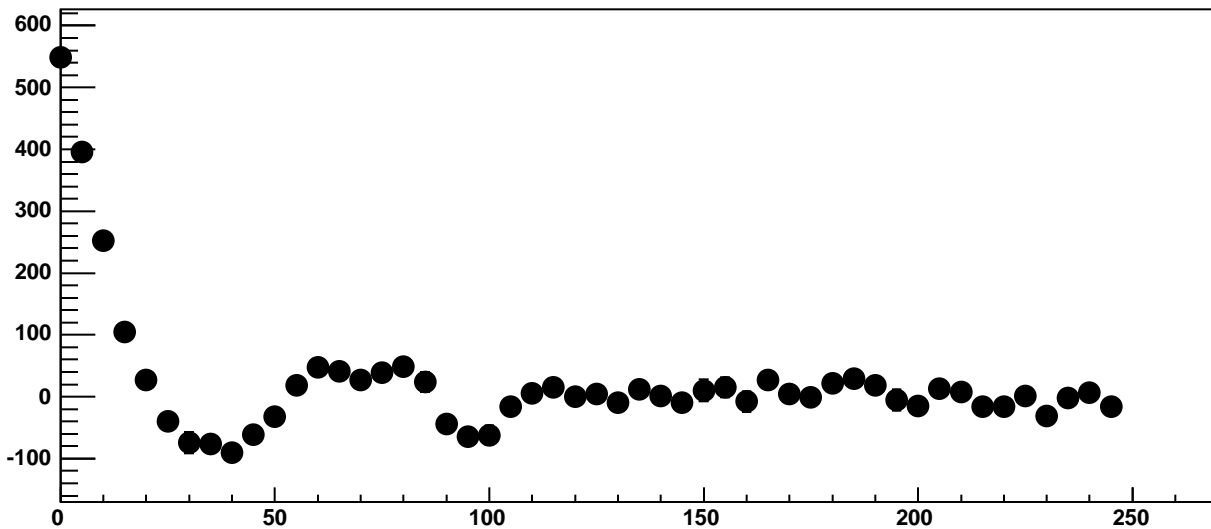
Chip 3, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold



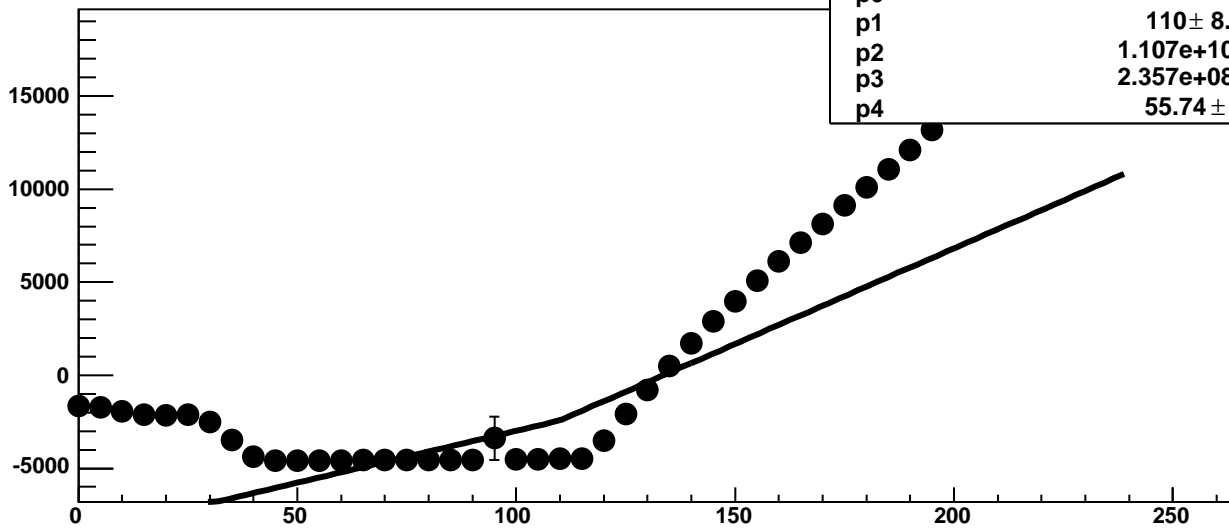
Chip 3, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

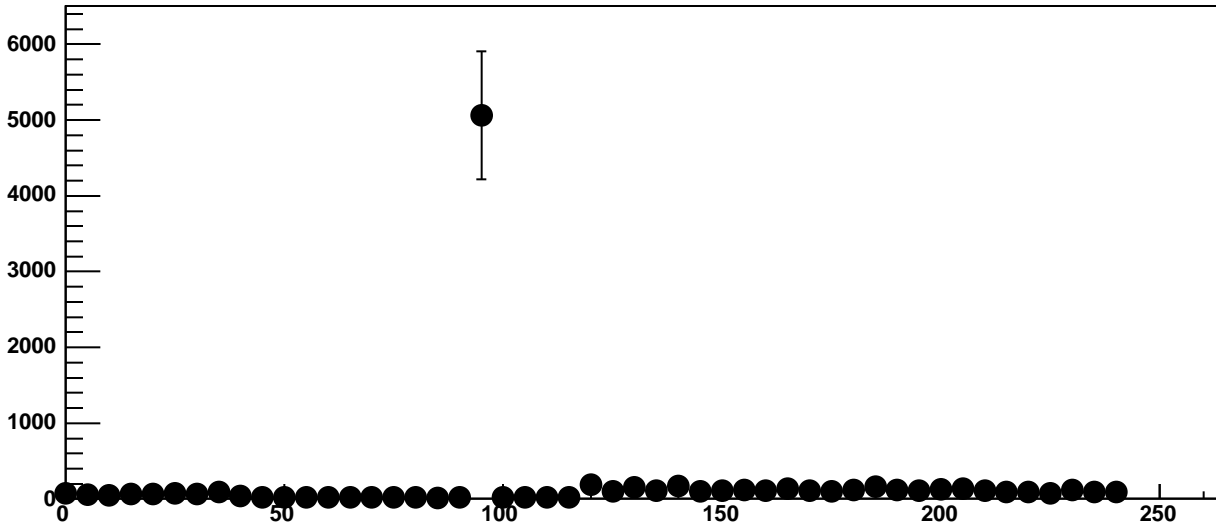


Chip 3, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

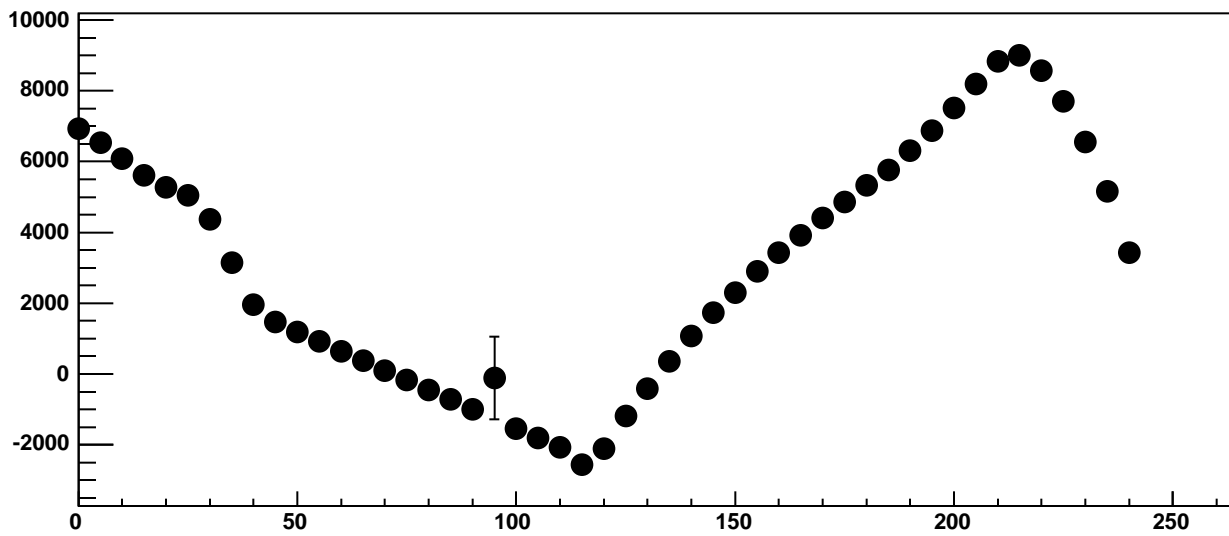


$\chi^2 / \text{ndf}$	2.87e+06 / 41
p0	-2425 ± 1.449
p1	110 ± 8.484e-05
p2	1.107e+10 ± 1.414
p3	2.357e+08 ± 1.418
p4	55.74 ± 0.03356

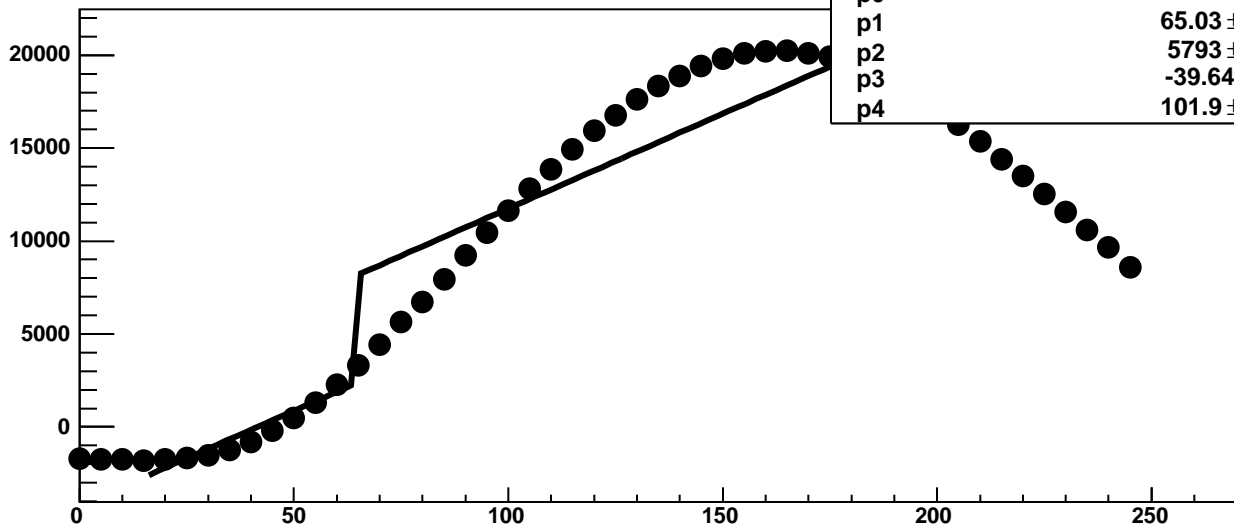
Chip 3, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold

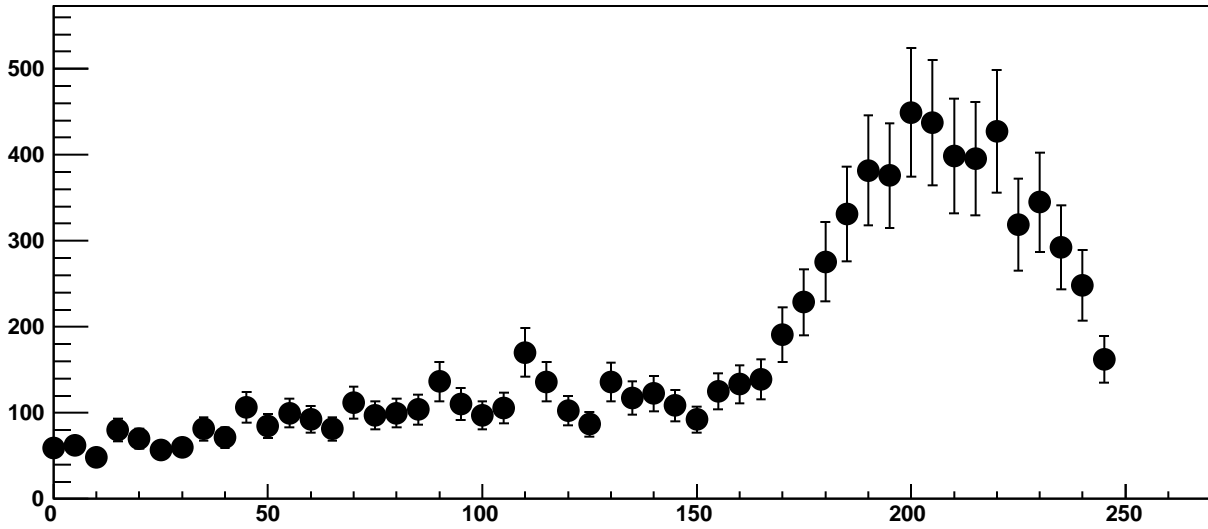


Chip 3, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold

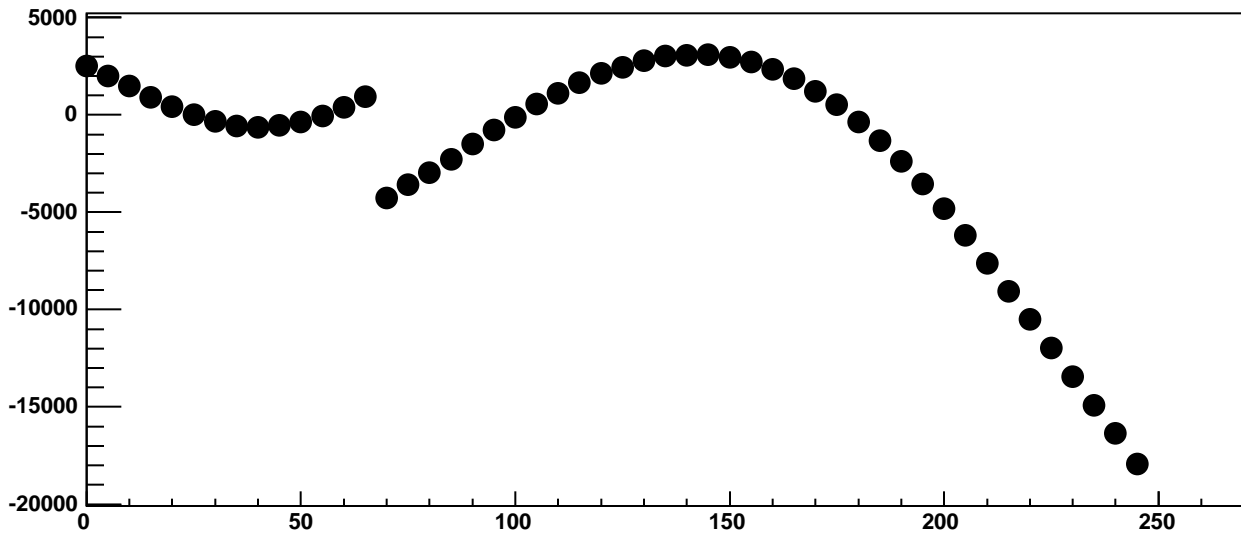


$\chi^2 / \text{ndf}$	4.313e+05 / 41
p0	2395 ± 0.8354
p1	65.03 ± 0.4838
p2	5793 ± 0.5959
p3	-39.64 ± 18.16
p4	101.9 ± 0.1258

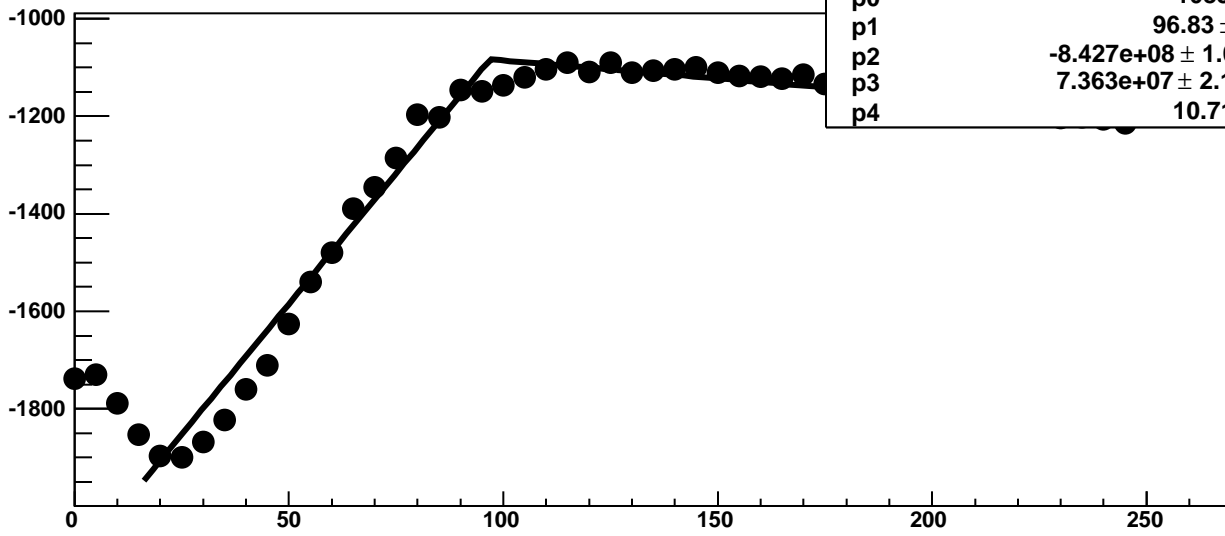
Chip 3, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold

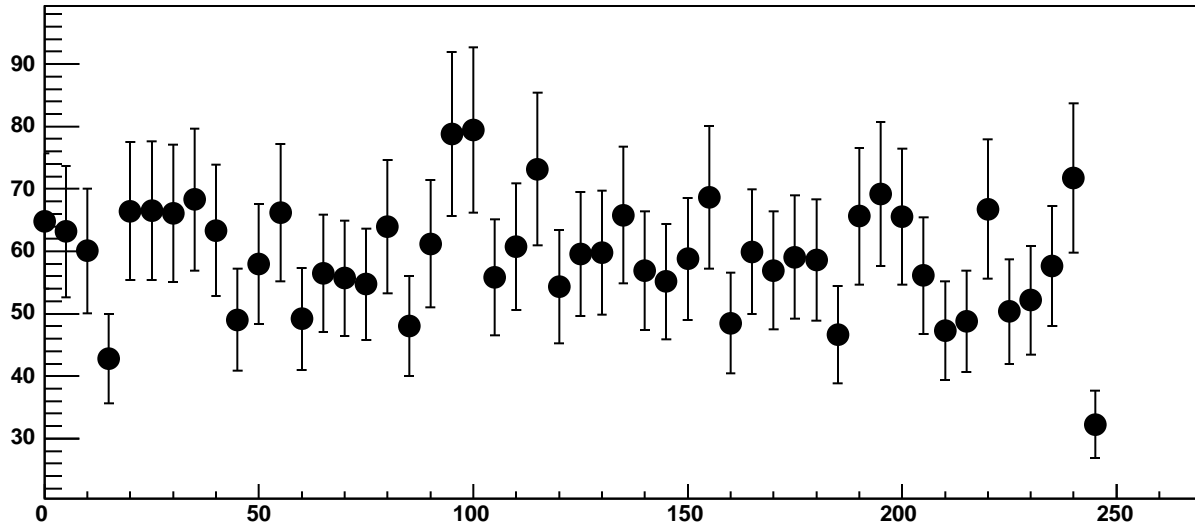


Chip 3, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

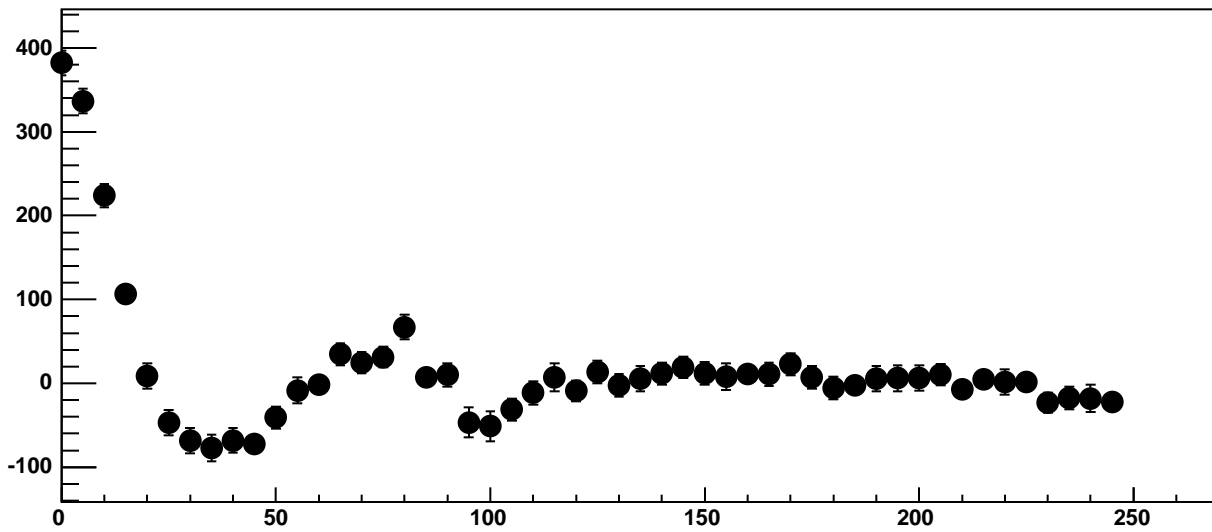


$\chi^2 / \text{ndf}$	325.9 / 41
p0	$-1083 \pm 4.924$
p1	$96.83 \pm 0.7256$
p2	$-8.427\text{e}+08 \pm 1.087\text{e}+07$
p3	$7.363\text{e}+07 \pm 2.135\text{e}+05$
p4	$10.71 \pm 0.131$

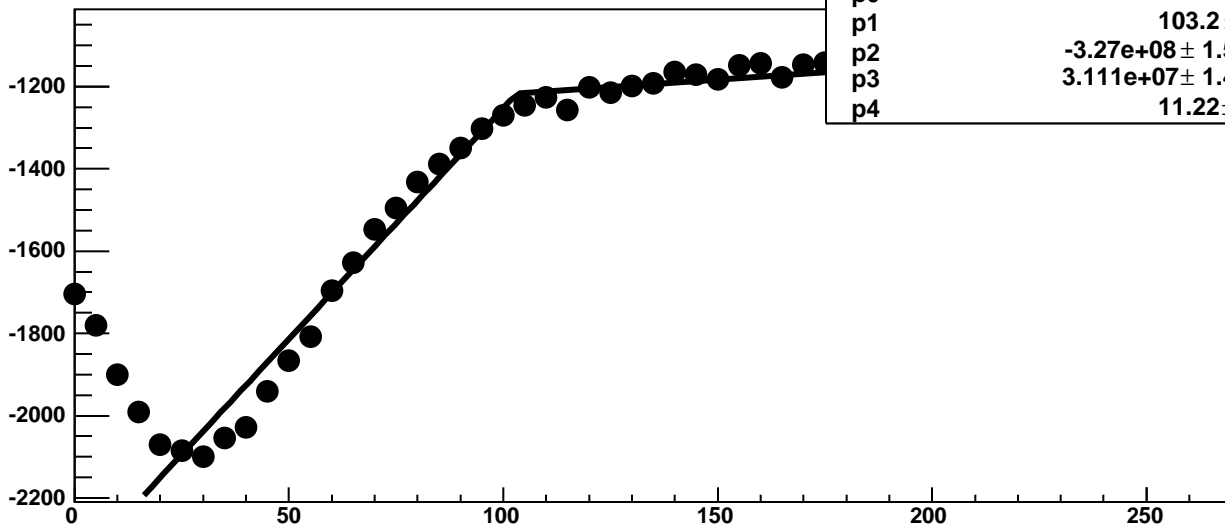
Chip 3, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

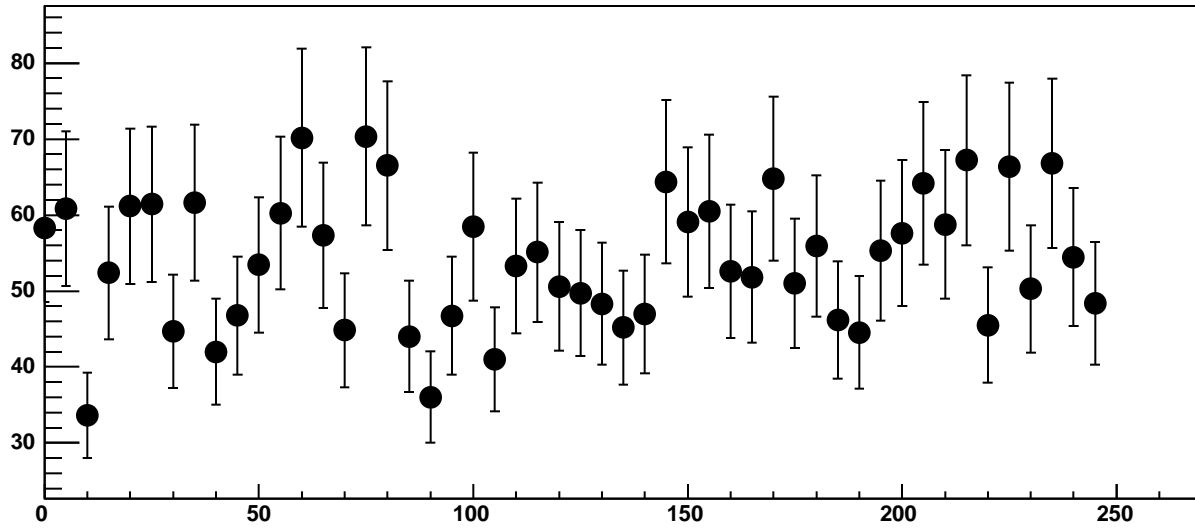


Chip 3, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

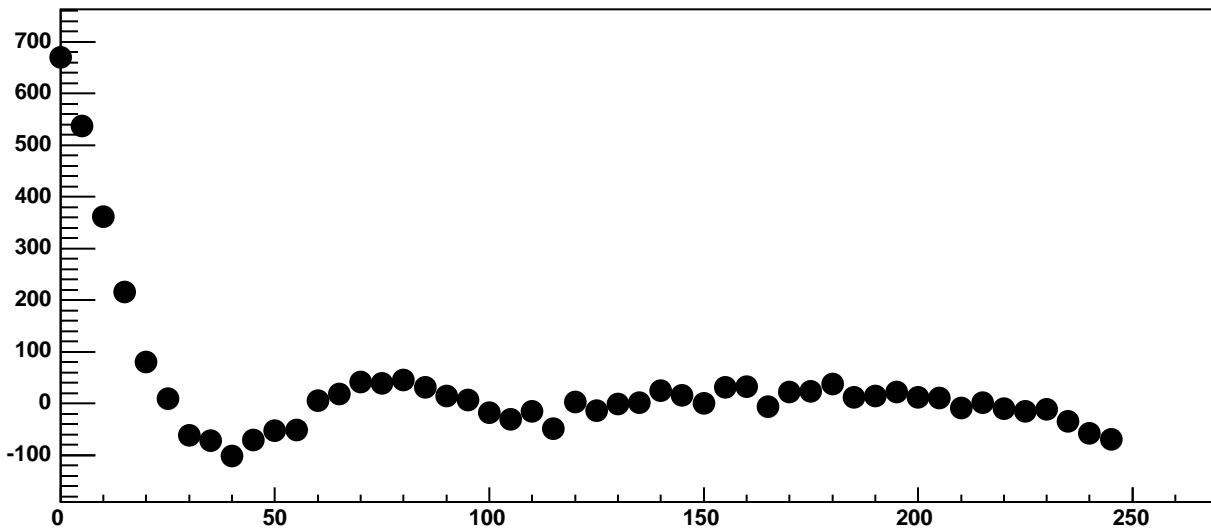


$\chi^2 / \text{ndf}$	752 / 41
p0	$-1217 \pm 4.642$
p1	$103.2 \pm 0.6581$
p2	$-3.27\text{e}+08 \pm 1.547\text{e}+07$
p3	$3.111\text{e}+07 \pm 1.427\text{e}+06$
p4	$11.22 \pm 0.1057$

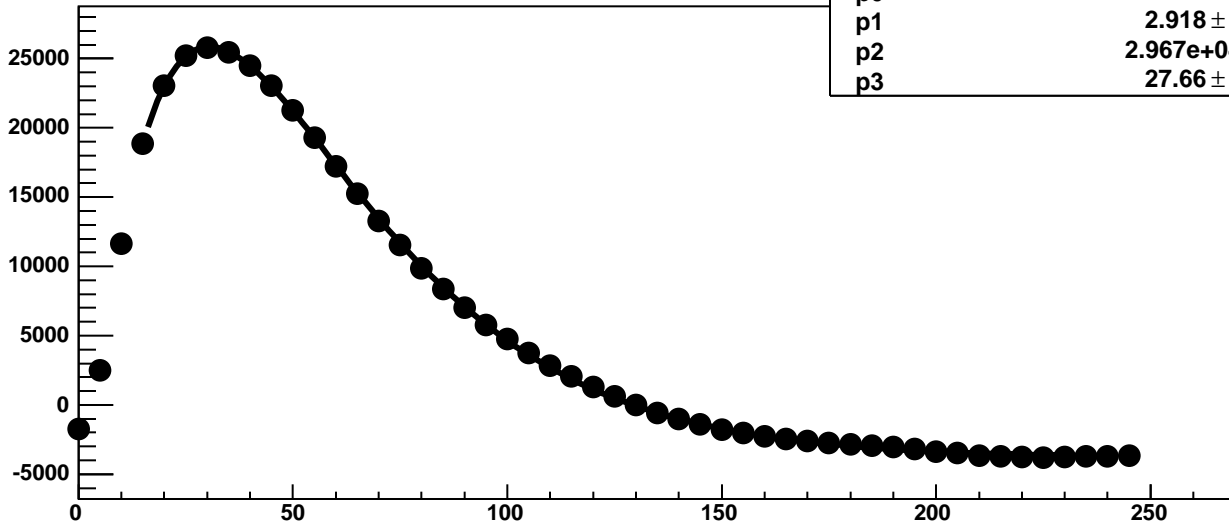
Chip 3, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

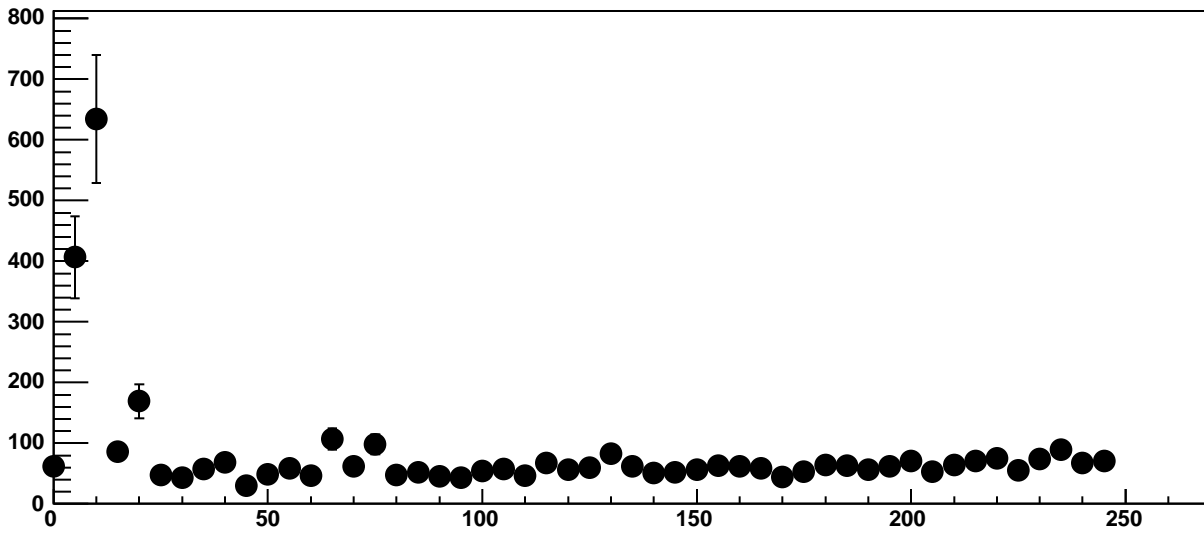


Chip 3, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

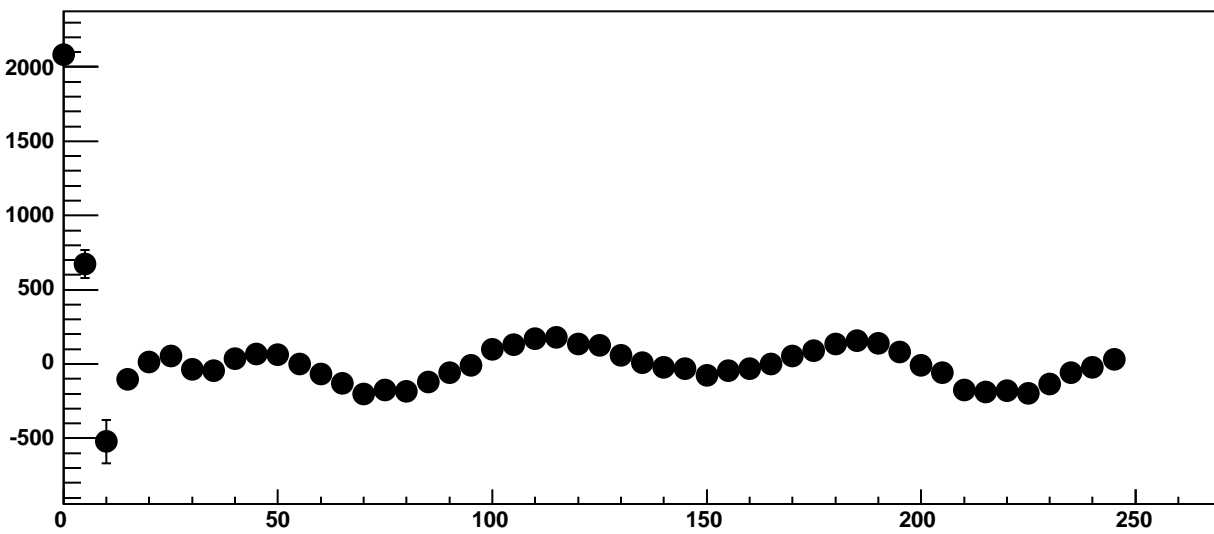


$\chi^2 / \text{ndf}$	2916 / 42
p0	-3817 ± 3.828
p1	2.918 ± 0.01805
p2	2.967e+04 ± 5.51
p3	27.66 ± 0.01066

Chip 3, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

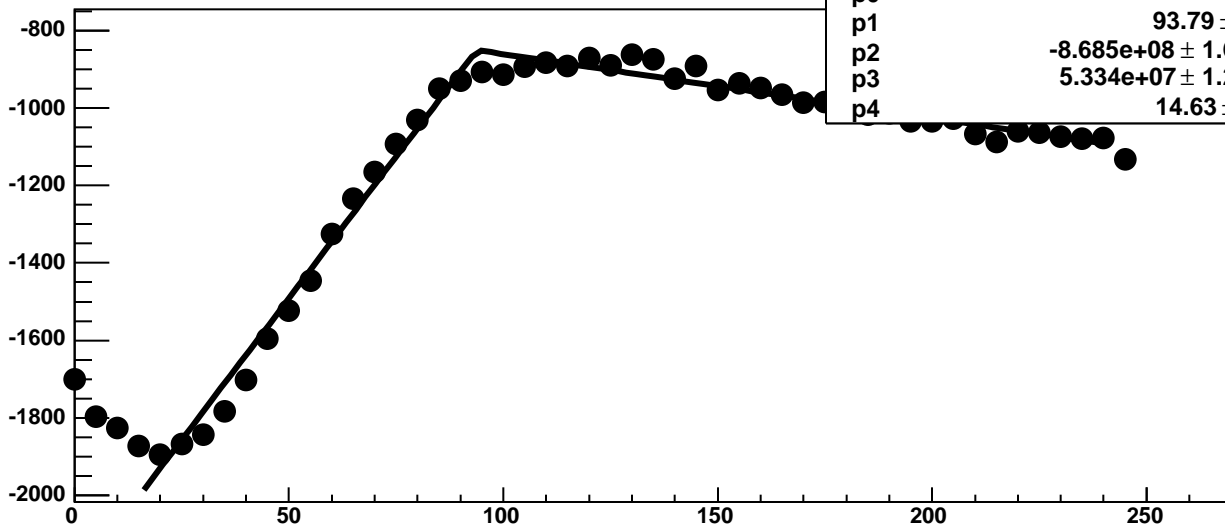


Chip 3, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold



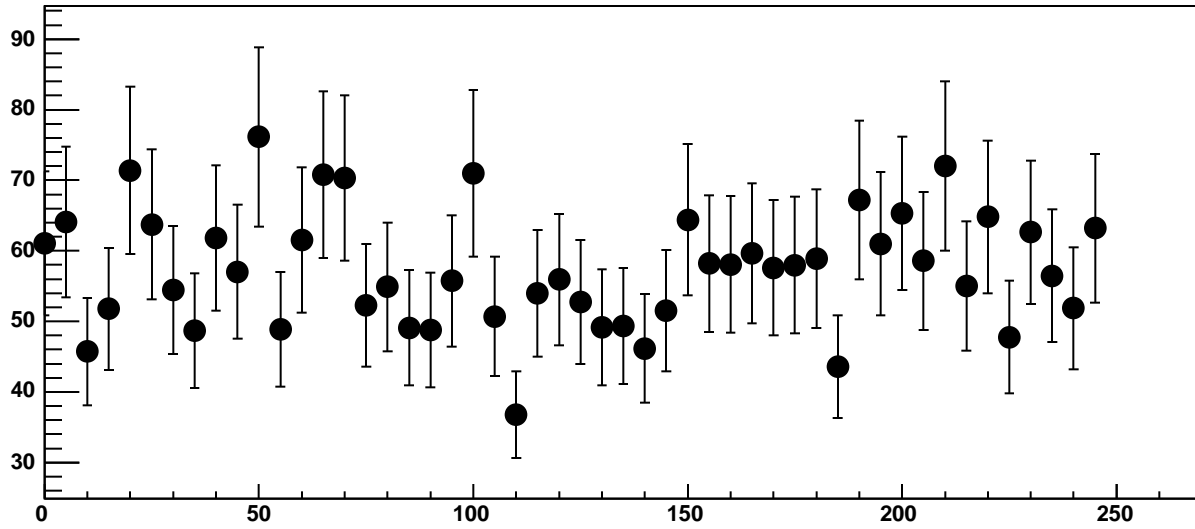


Chip 3, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

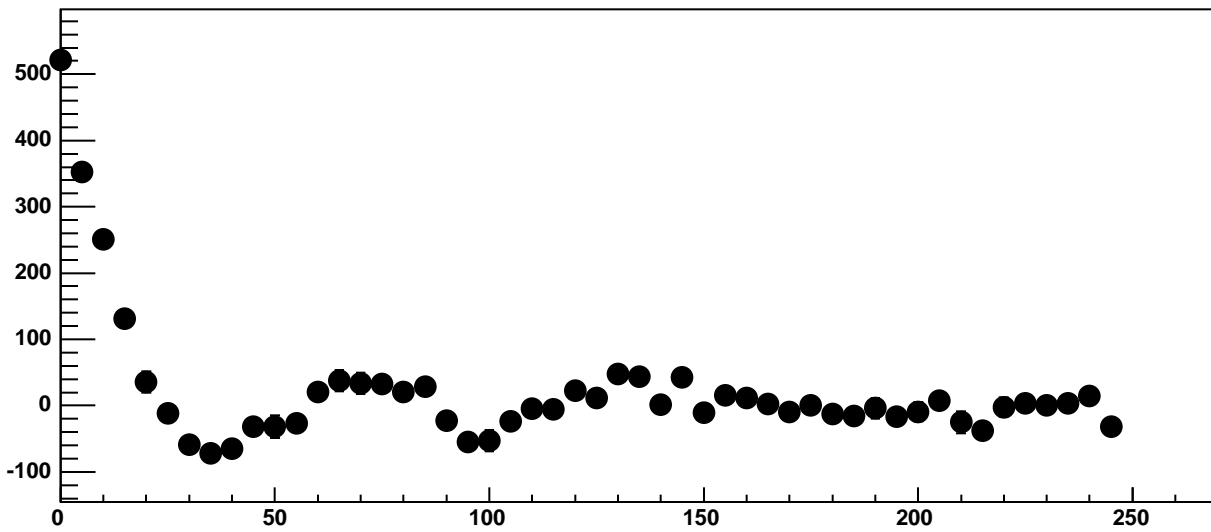


$\chi^2 / \text{ndf}$	366 / 41
p0	$-850.5 \pm 3.963$
p1	$93.79 \pm 0.4145$
p2	$-8.685\text{e}+08 \pm 1.651\text{e}+07$
p3	$5.334\text{e}+07 \pm 1.214\text{e}+06$
p4	$14.63 \pm 0.1186$

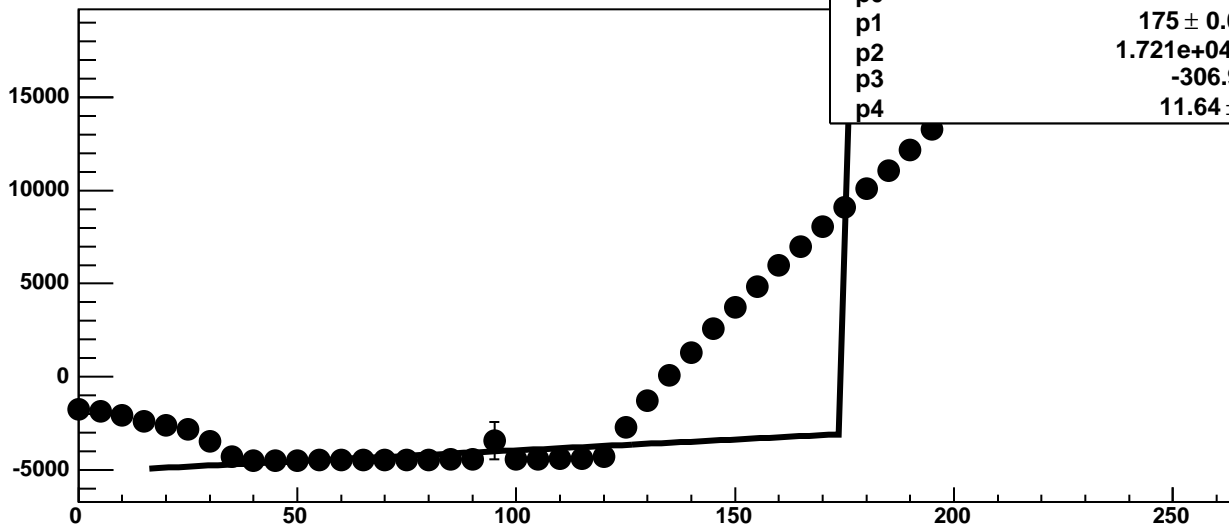
Chip 3, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

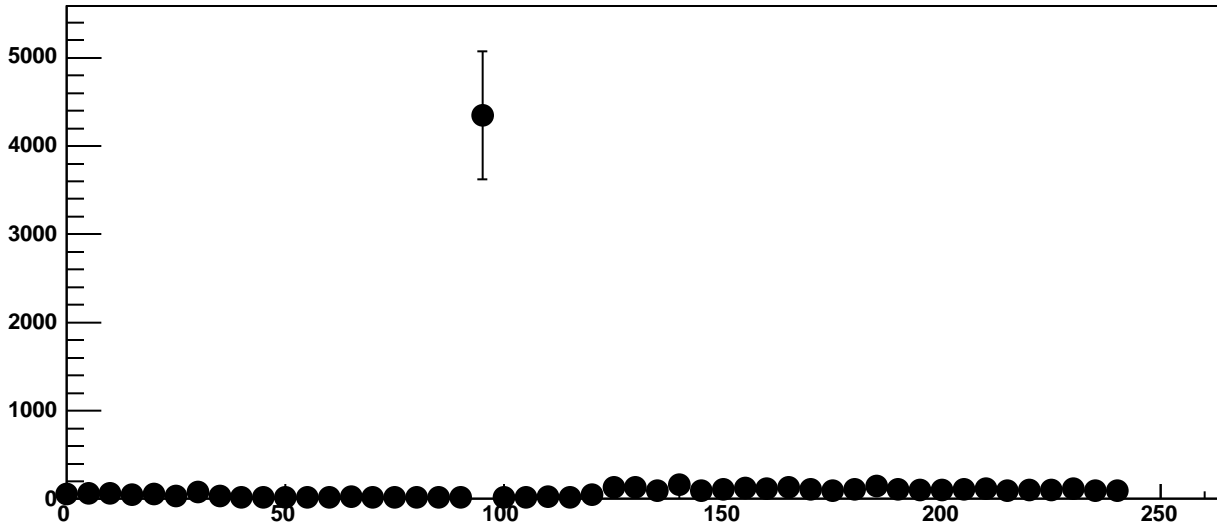


Chip 3, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

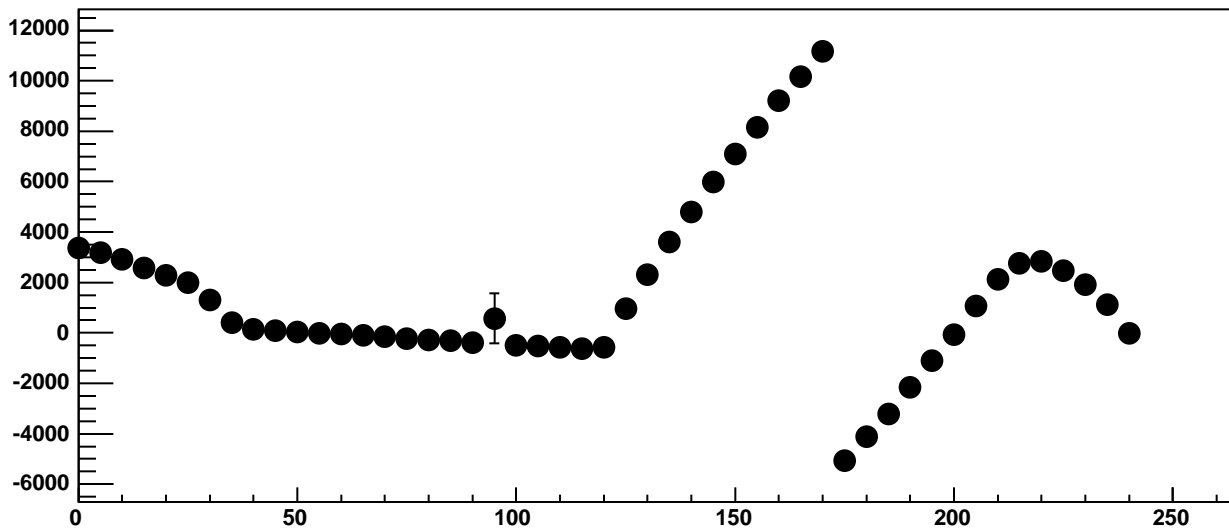


$\chi^2 / \text{ndf}$	1.129e+06 / 41
p0	-3067 ± 16.93
p1	175 ± 0.0003224
p2	1.721e+04 ± 12.49
p3	-306.9 ± 1.53
p4	11.64 ± 0.1569

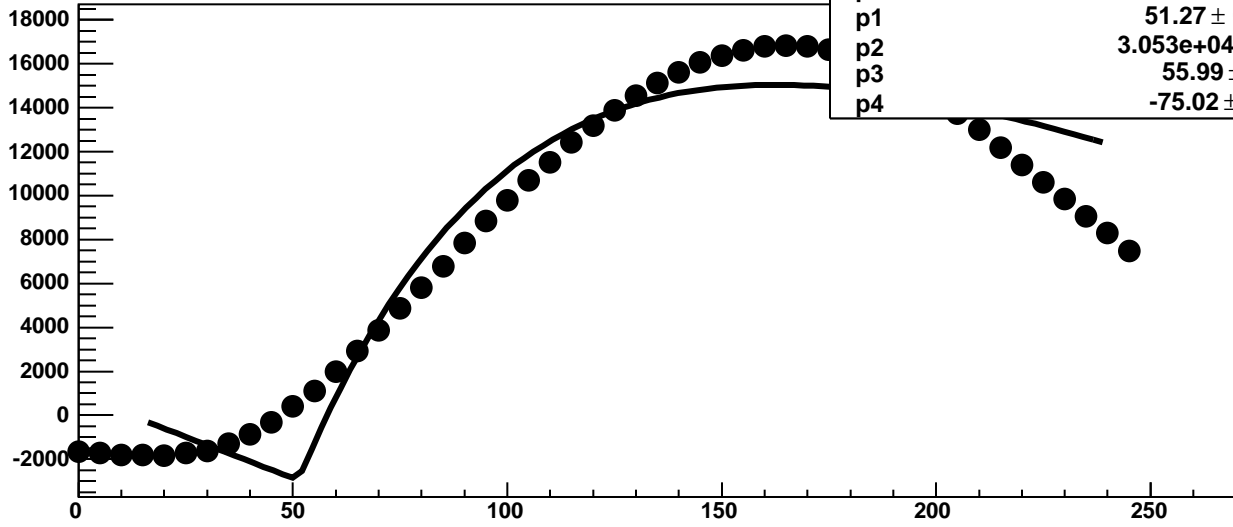
Chip 3, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

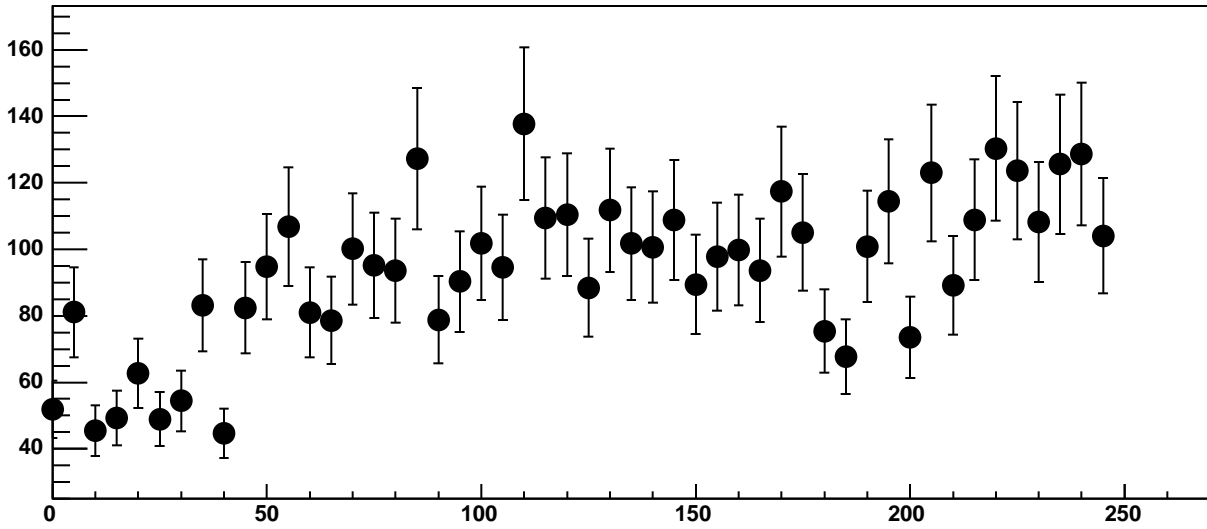


Chip 3, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold

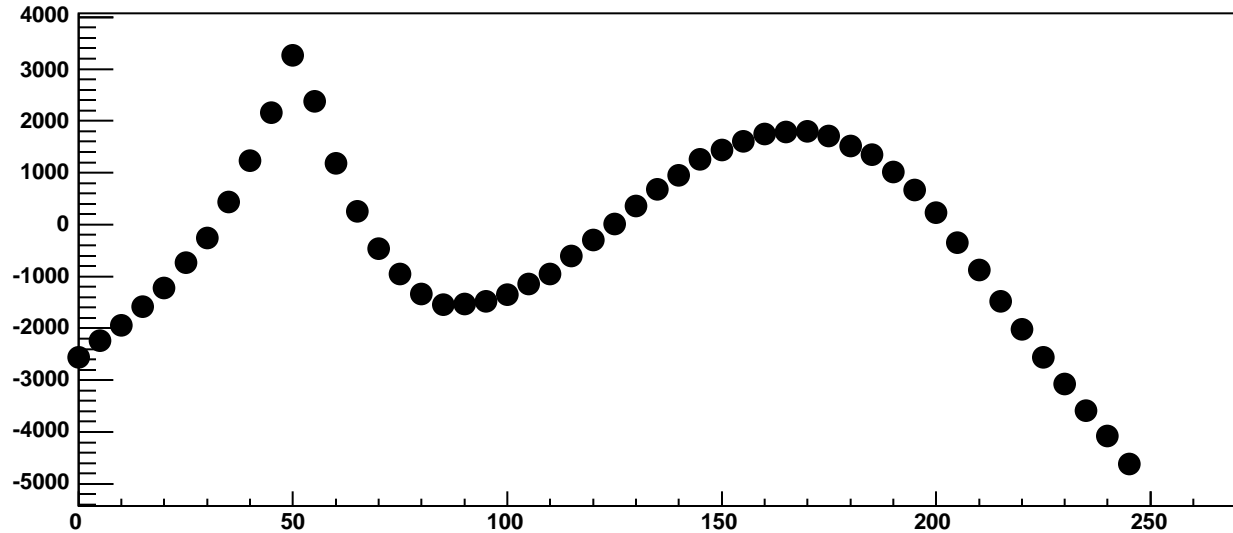


$\chi^2 / \text{ndf}$	2.486e+05 / 41
p0	-2950 ± 6.723
p1	51.27 ± 0.03063
p2	3.053e+04 ± 59.41
p3	55.99 ± 0.1121
p4	-75.02 ± 0.2726

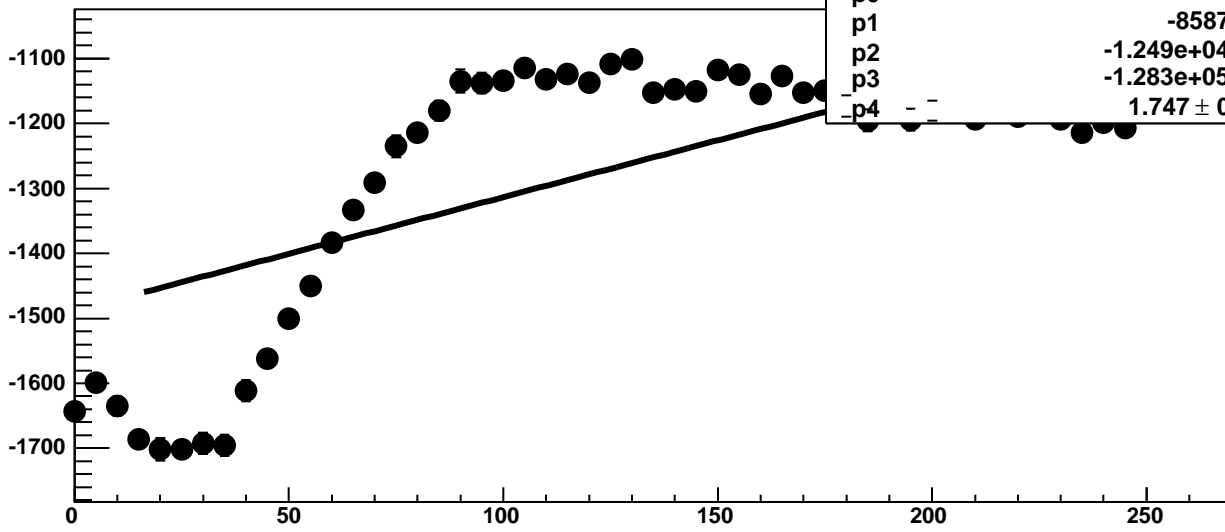
Chip 3, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

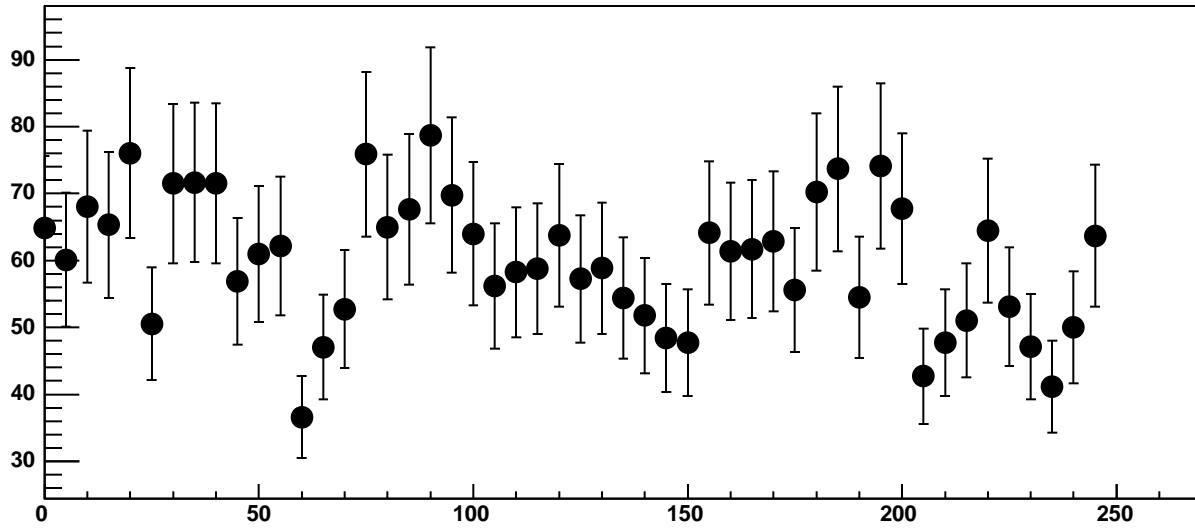


Chip 3, Channel 12, Enable 1, DAC=1600, ADC Mean vs Hold

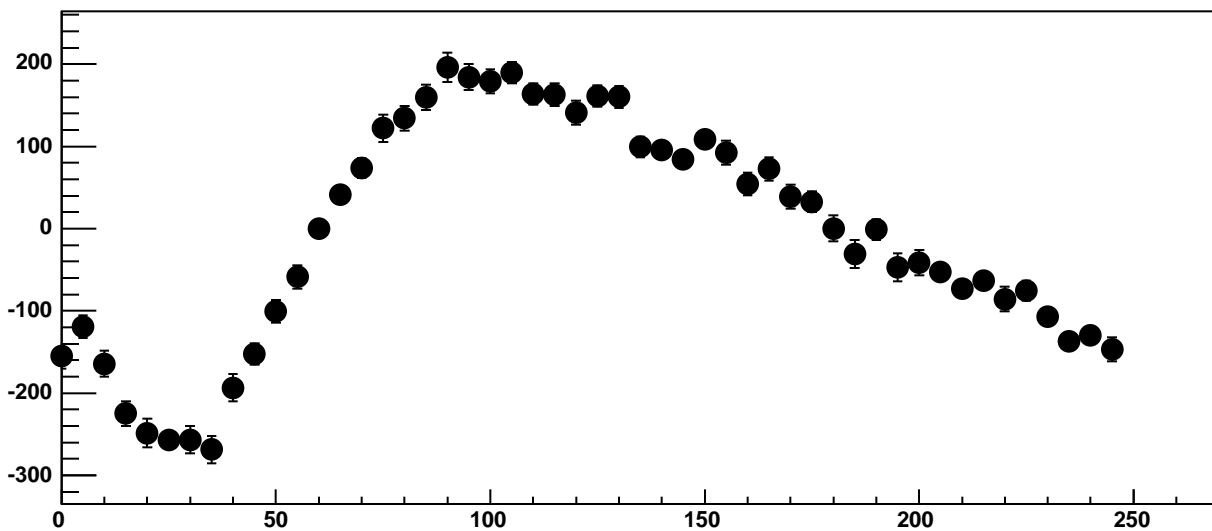


$\chi^2 / \text{ndf}$	4371 / 41
p0	$-3996 \pm 10.15$
p1	$-8587 \pm 4.308$
p2	$-1.249\text{e}+04 \pm 12.12$
p3	$-1.283\text{e}+05 \pm 437.8$
p4	$1.747 \pm 0.001164$

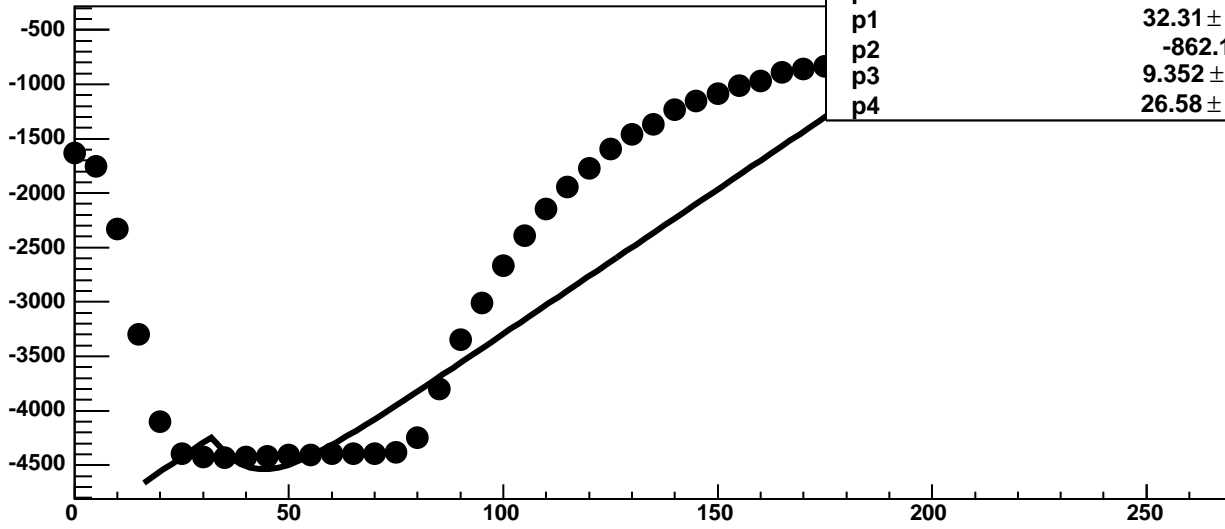
Chip 3, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold

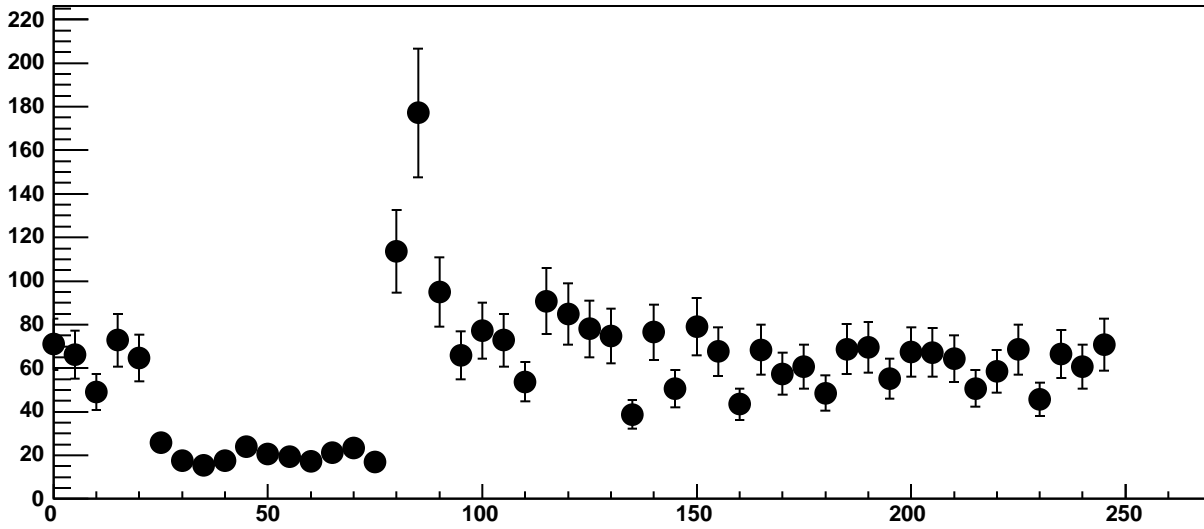


Chip 3, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

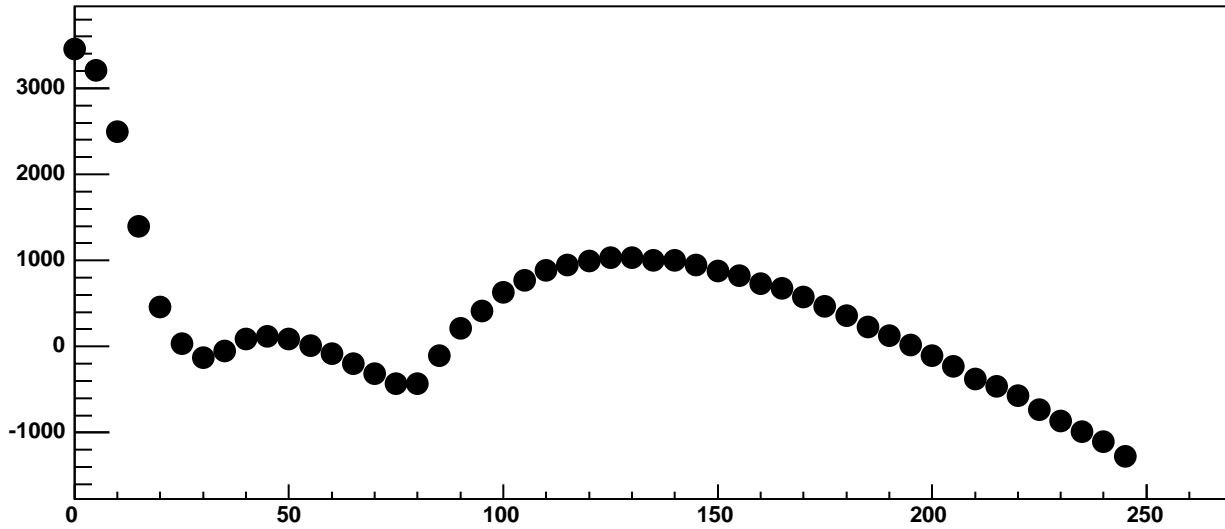


$\chi^2 / \text{ndf}$	1.123e+05 / 41
p0	-4232 ± 2.73
p1	32.31 ± 0.06735
p2	-862.1 ± 4.383
p3	9.352 ± 0.09341
p4	26.58 ± 0.02874

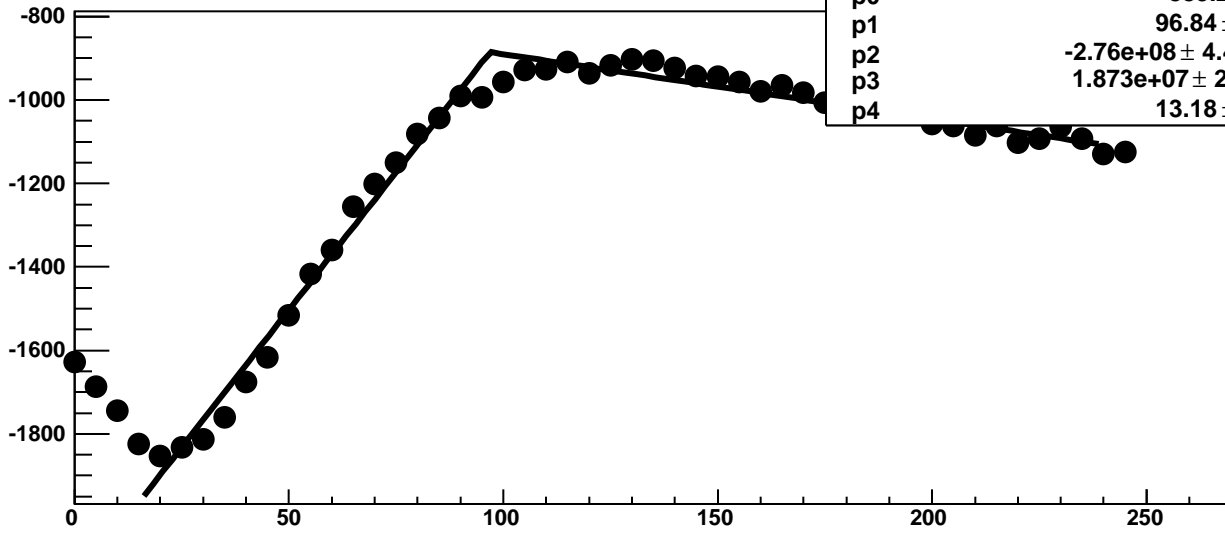
Chip 3, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

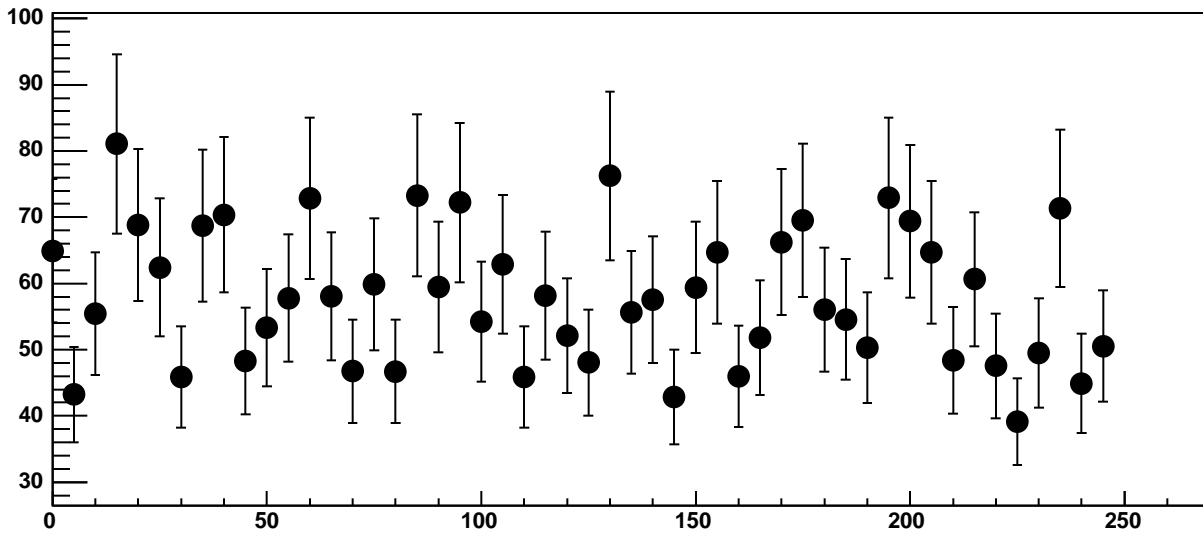


Chip 3, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

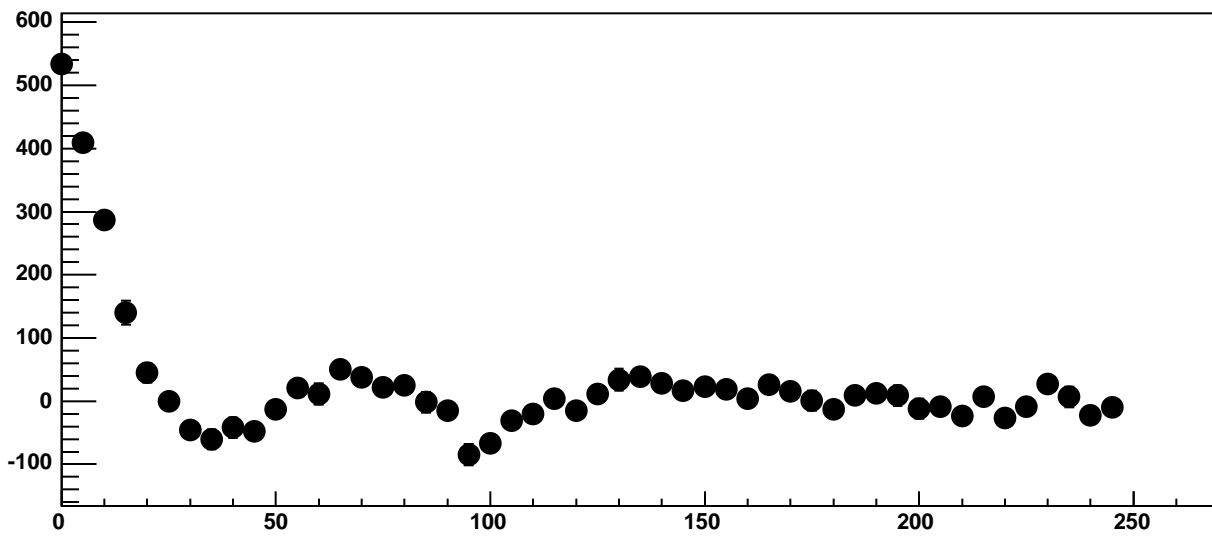


$\chi^2 / \text{ndf}$	286.9 / 41
p0	$-885.2 \pm 4.175$
p1	$96.84 \pm 0.5527$
p2	$-2.76\text{e}+08 \pm 4.486\text{e}+06$
p3	$1.873\text{e}+07 \pm 2.47\text{e}+05$
p4	$13.18 \pm 0.1433$

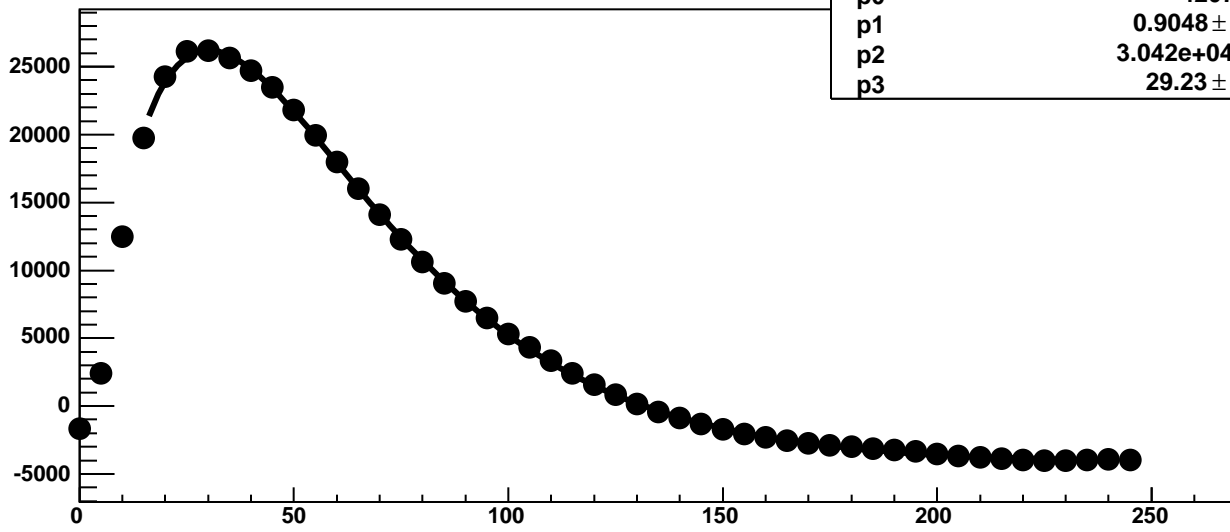
Chip 3, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

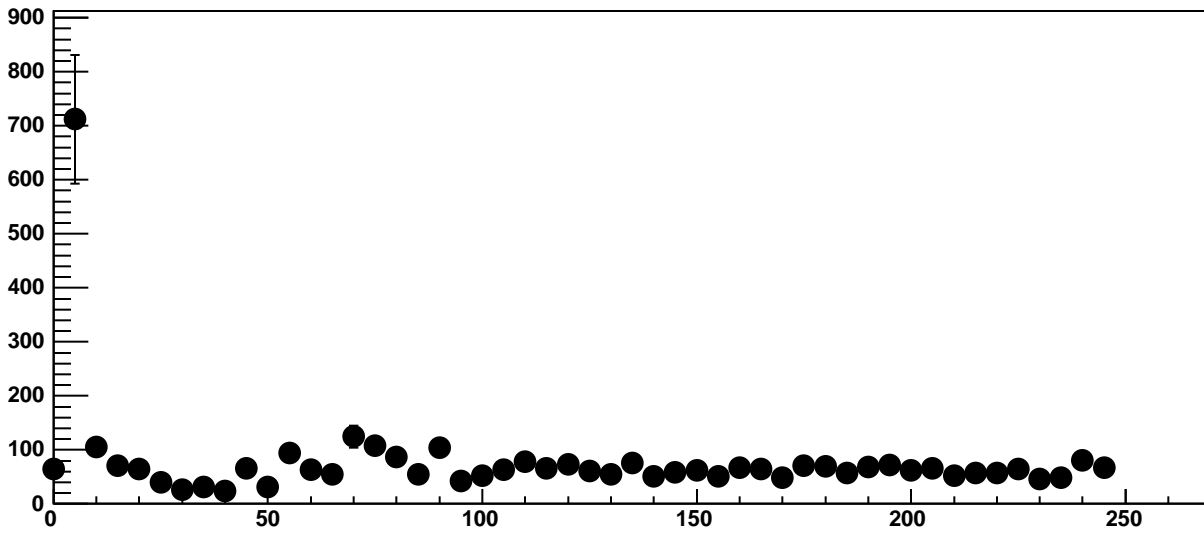


Chip 3, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold

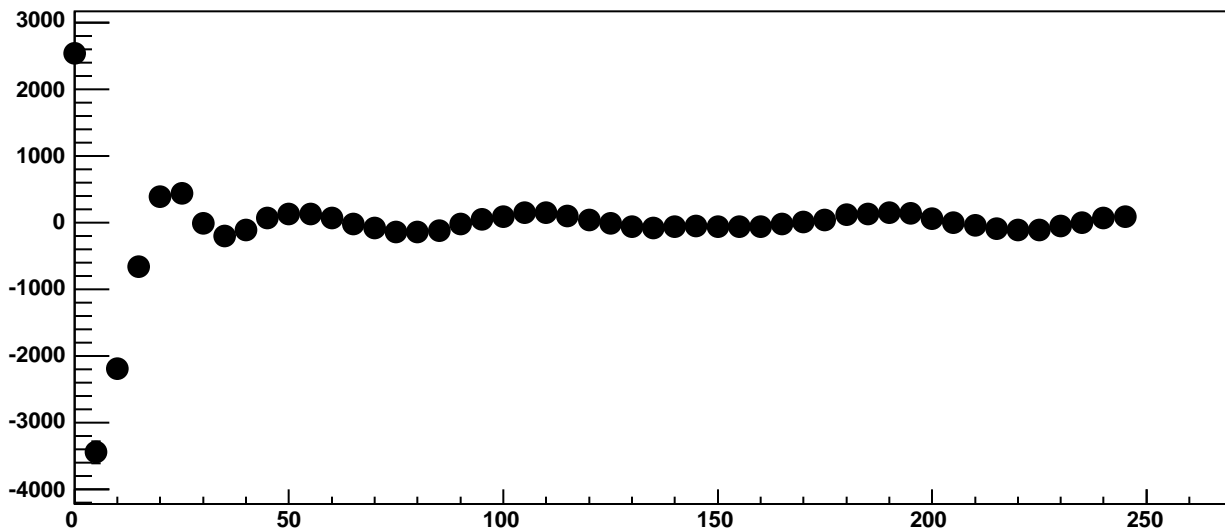


$\chi^2 / \text{ndf}$	7352 / 42
p0	$-4207 \pm 3.857$
p1	$0.9048 \pm 0.01698$
p2	$3.042e+04 \pm 4.576$
p3	$29.23 \pm 0.01092$

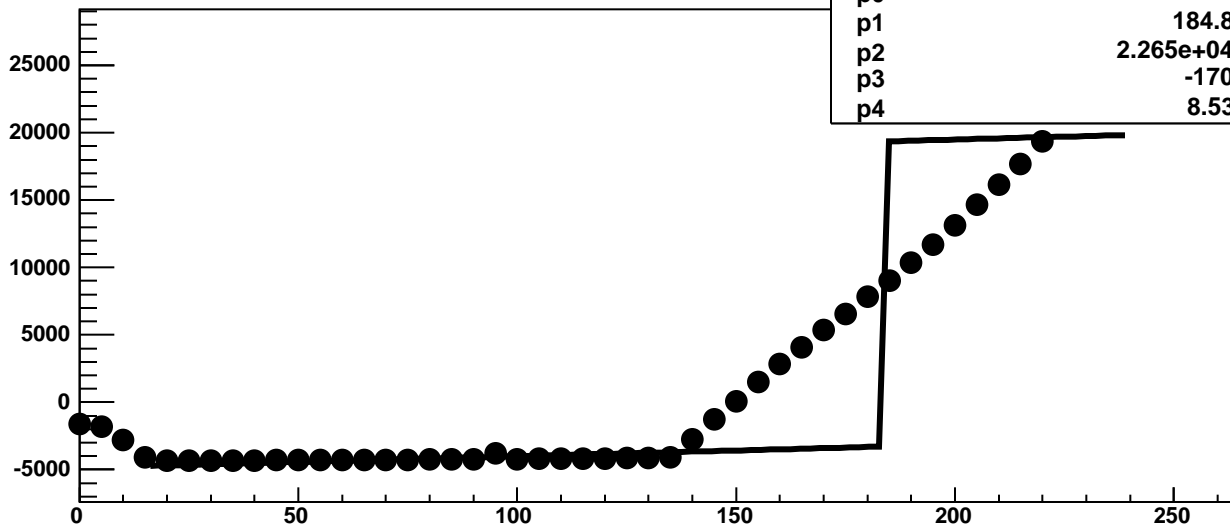
Chip 3, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold

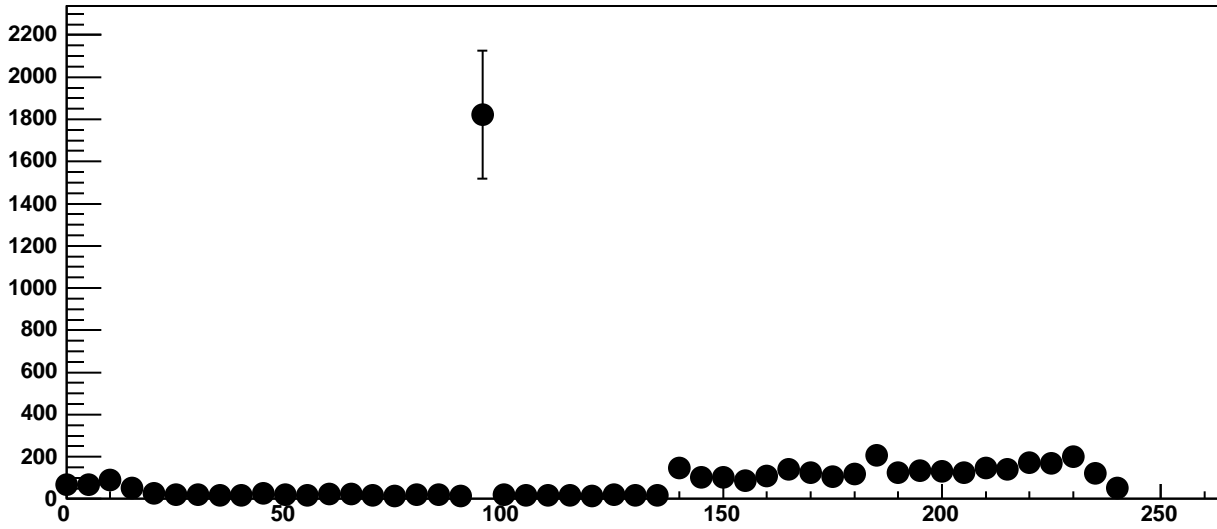


Chip 3, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

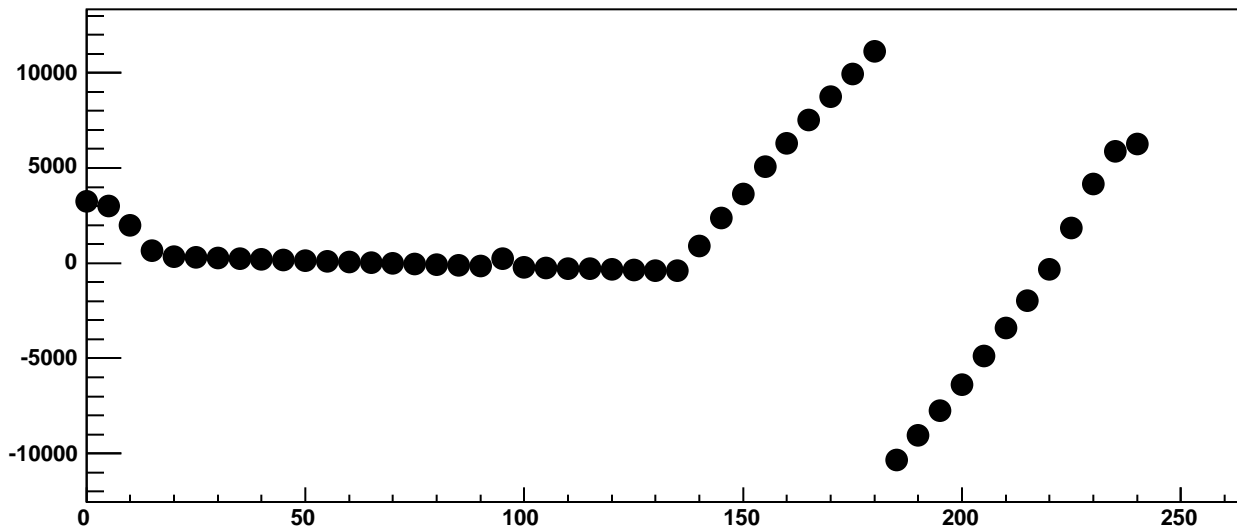


$\chi^2 / \text{ndf}$	1.339e+06 / 41
p0	-3280 ± 366.1
p1	184.8 ± 365.9
p2	2.265e+04 ± 2.932
p3	-170 ± 1.428
p4	8.536 ± 28

Chip 3, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

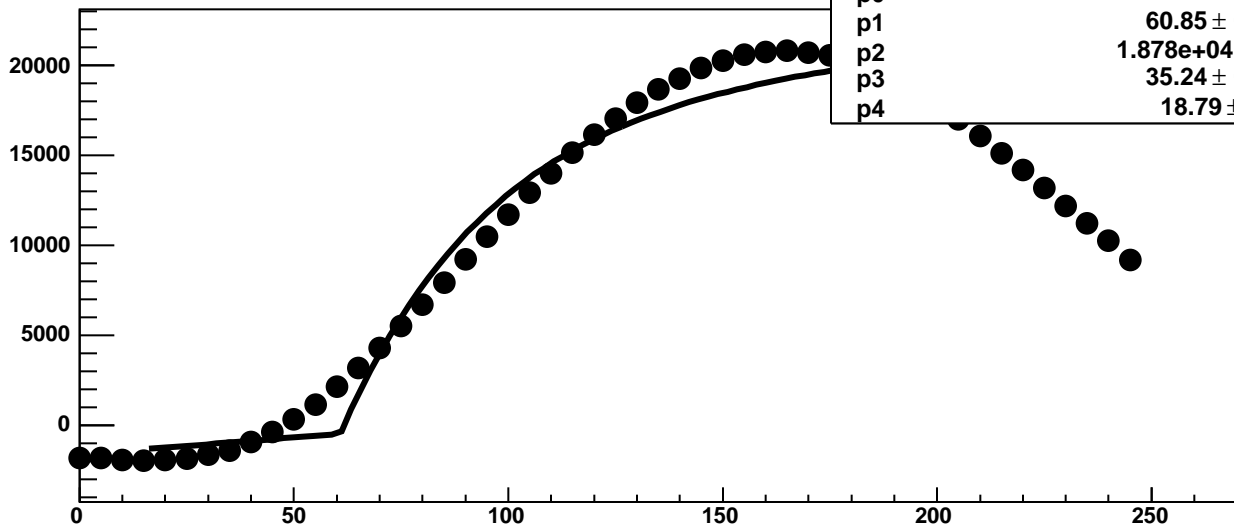


Chip 3, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



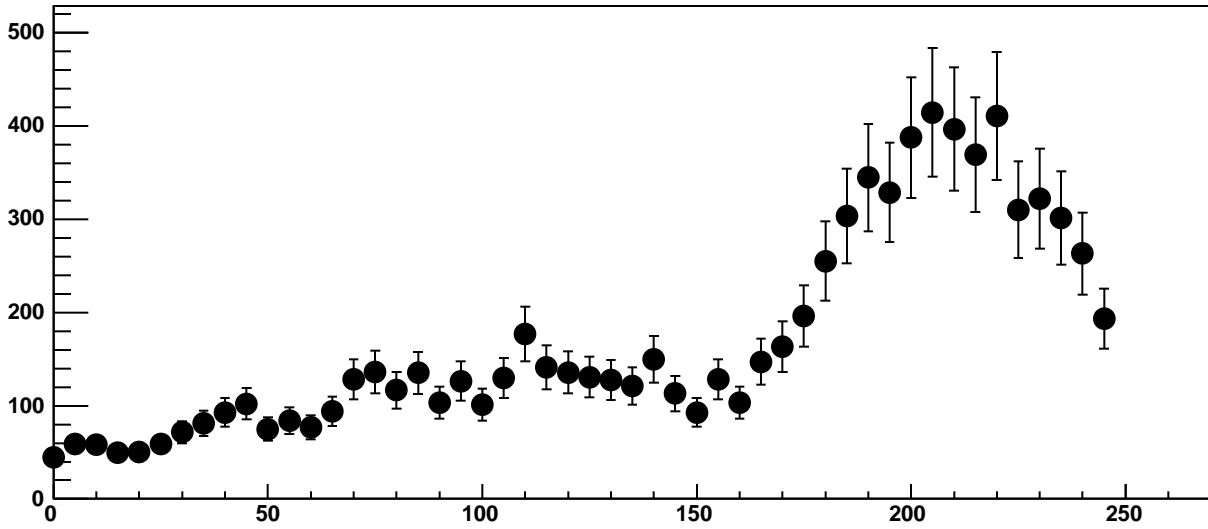


Chip 3, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

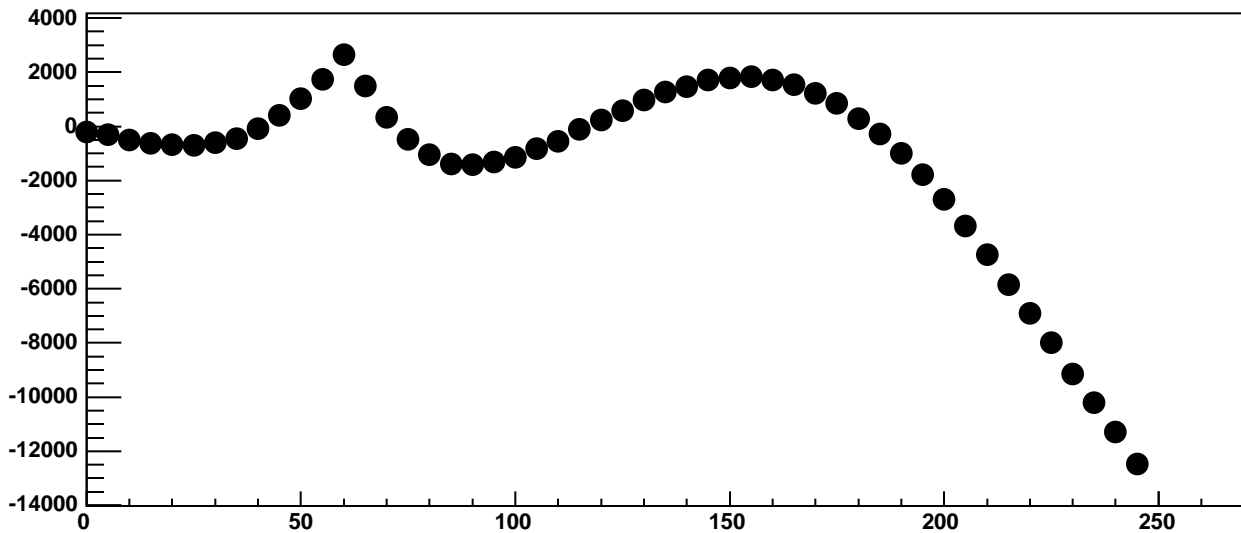


$\chi^2 / \text{ndf}$	1.934e+05 / 41
p0	-470.7 ± 9.118
p1	60.85 ± 0.04145
p2	1.878e+04 ± 41.55
p3	35.24 ± 0.09867
p4	18.79 ± 0.2538

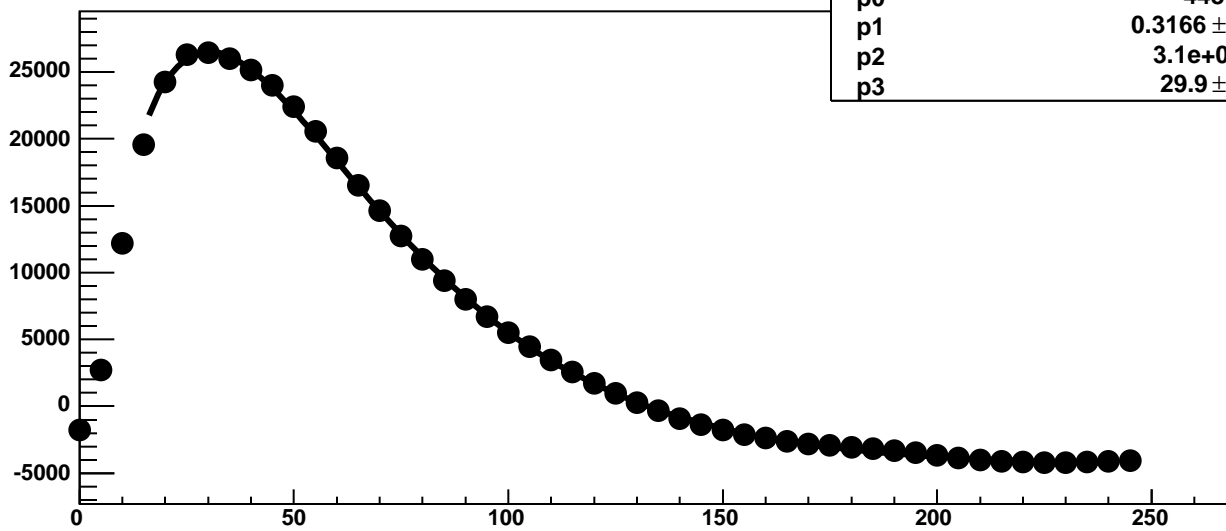
Chip 3, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

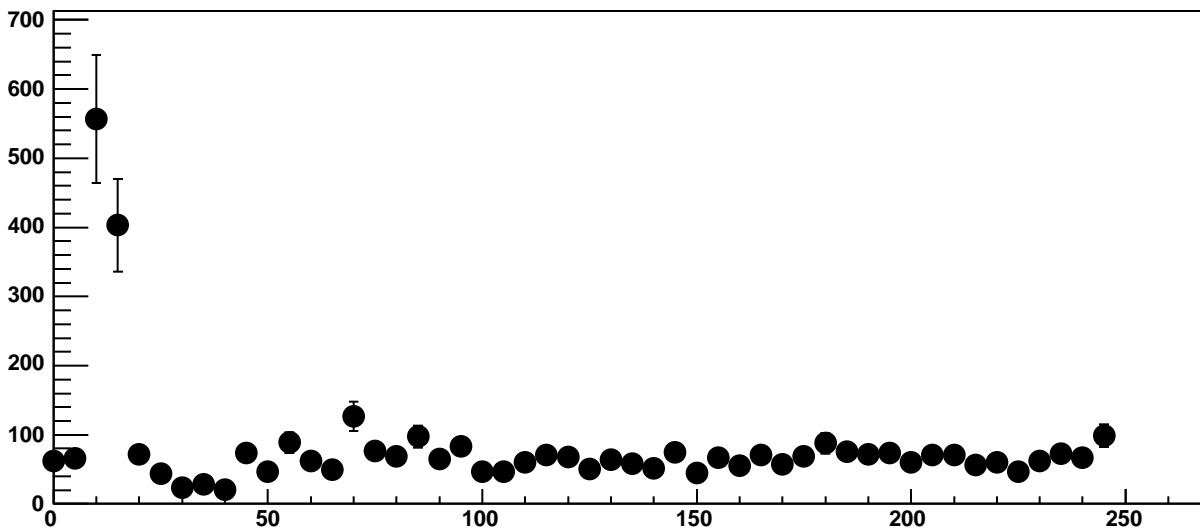


Chip 3, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold

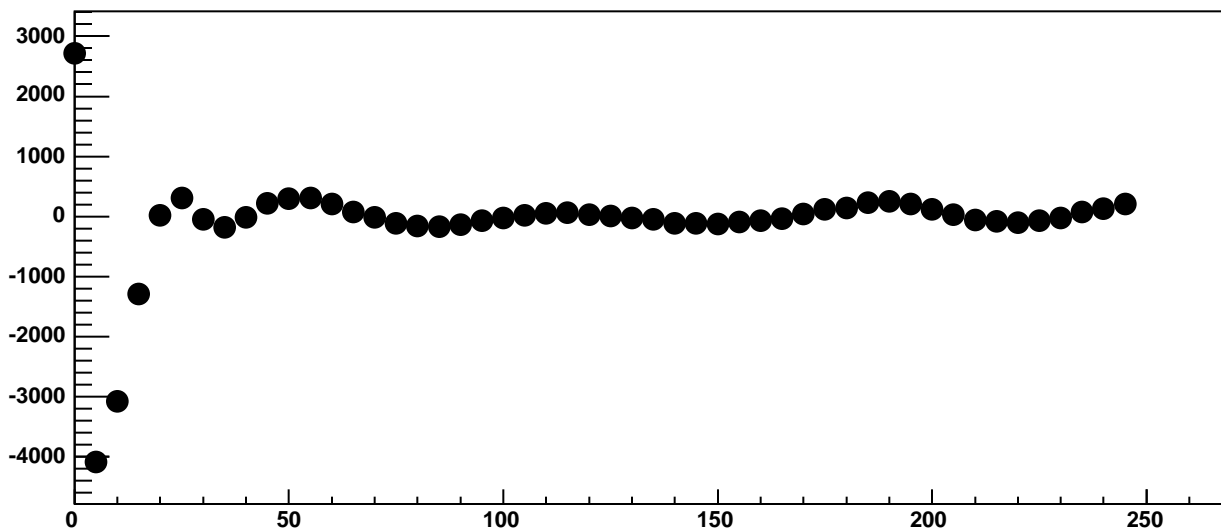


$\chi^2 / \text{ndf}$	5116 / 42
p0	-4481 ± 4.325
p1	0.3166 ± 0.02458
p2	3.1e+04 ± 5.18
p3	29.9 ± 0.01292

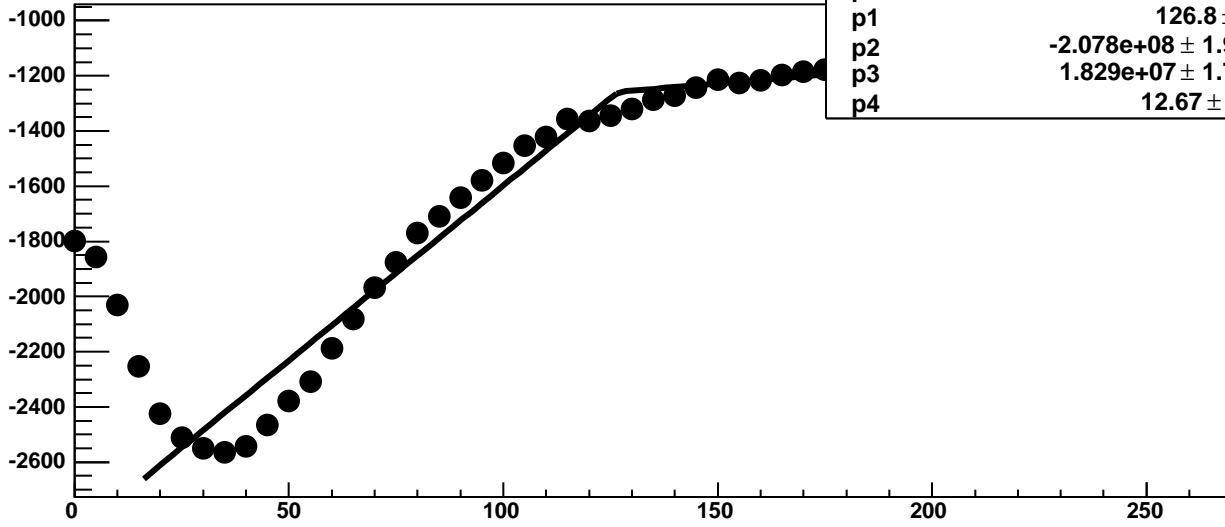
Chip 3, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

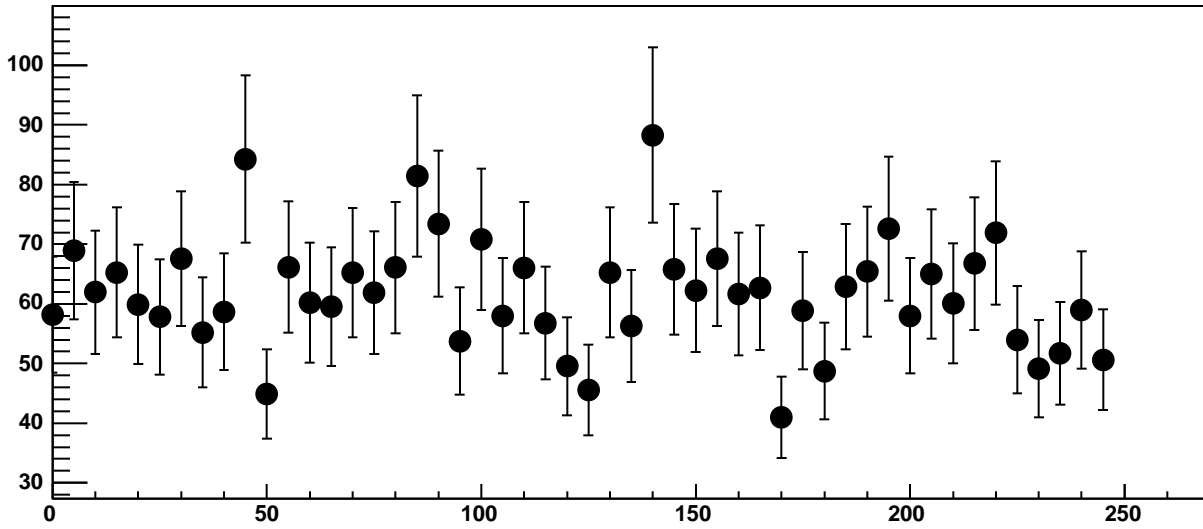


Chip 3, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

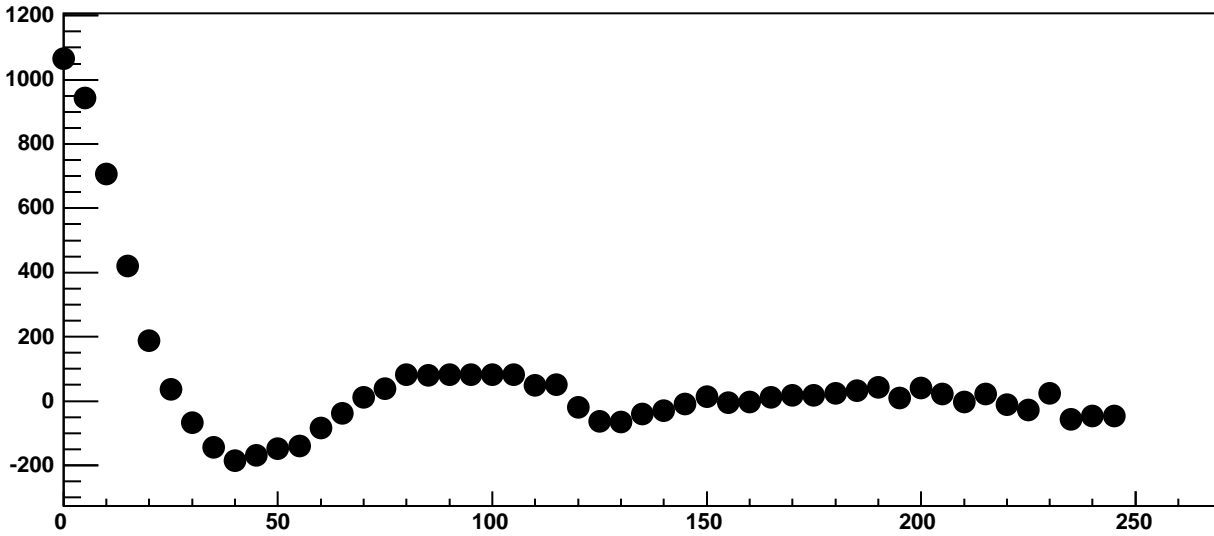


$\chi^2 / \text{ndf}$	2098 / 41
p0	$-1258 \pm 6.658$
p1	$126.8 \pm 0.7037$
p2	$-2.078\text{e}+08 \pm 1.964\text{e}+07$
p3	$1.829\text{e}+07 \pm 1.718\text{e}+06$
p4	$12.67 \pm 0.08252$

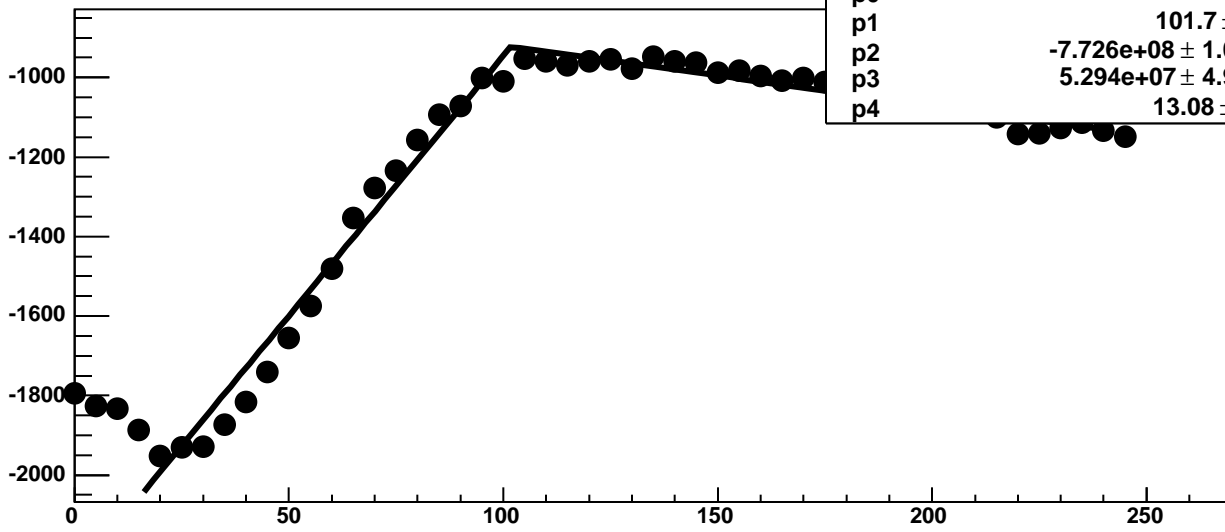
Chip 3, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

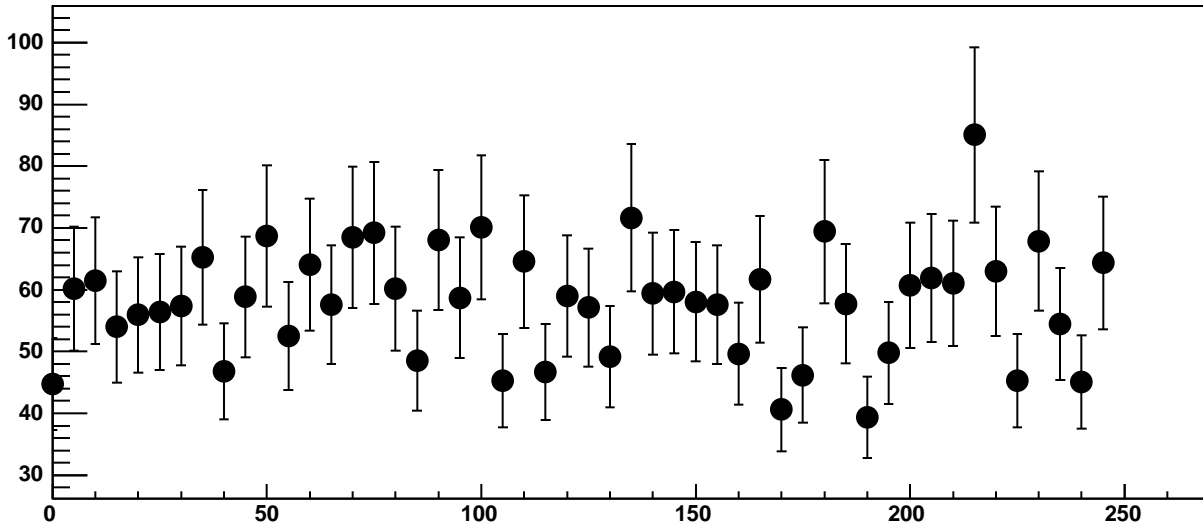


Chip 3, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

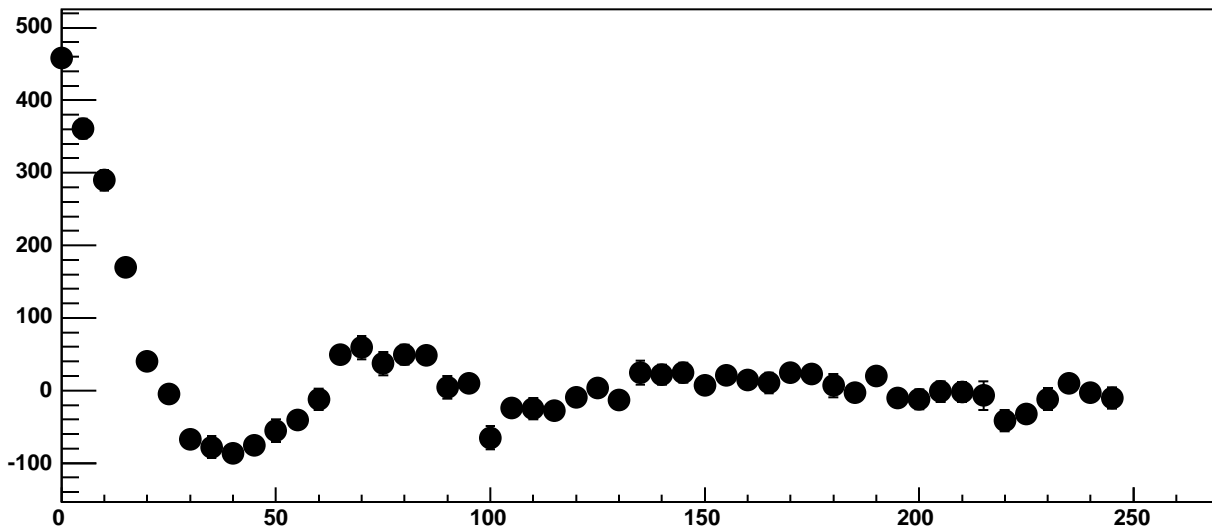


$\chi^2 / \text{ndf}$	521.4 / 41
p0	-922.4 ± 4.246
p1	101.7 ± 0.5497
p2	-7.726e+08 ± 1.065e+07
p3	5.294e+07 ± 4.911e+05
p4	13.08 ± 0.1224

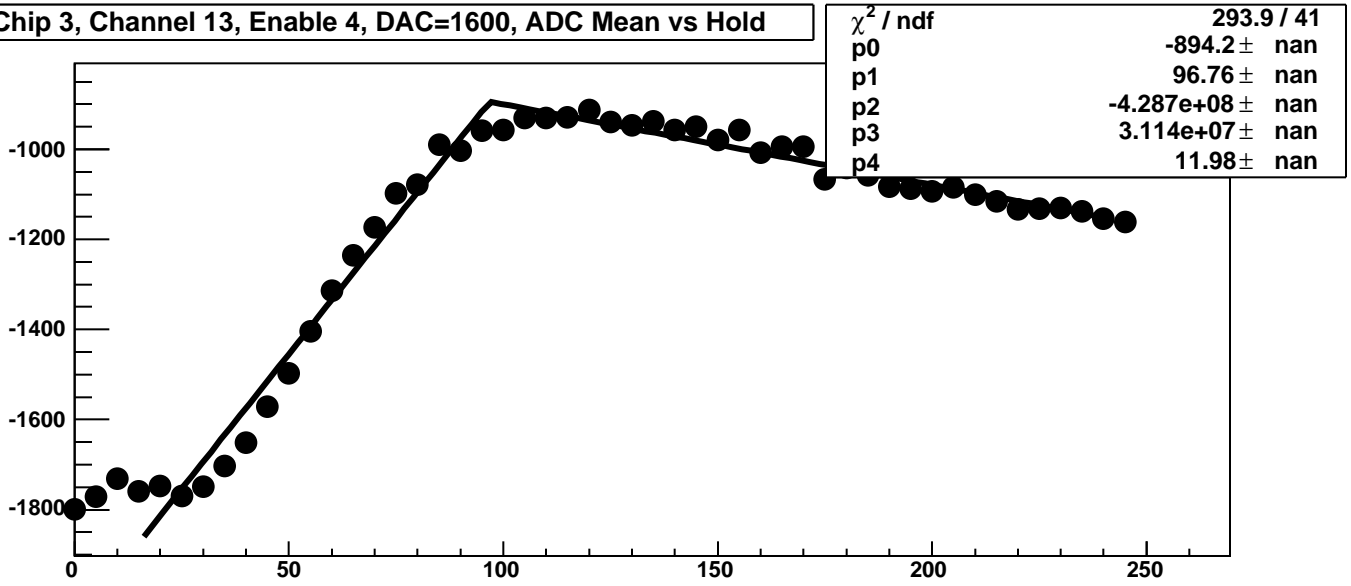
Chip 3, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



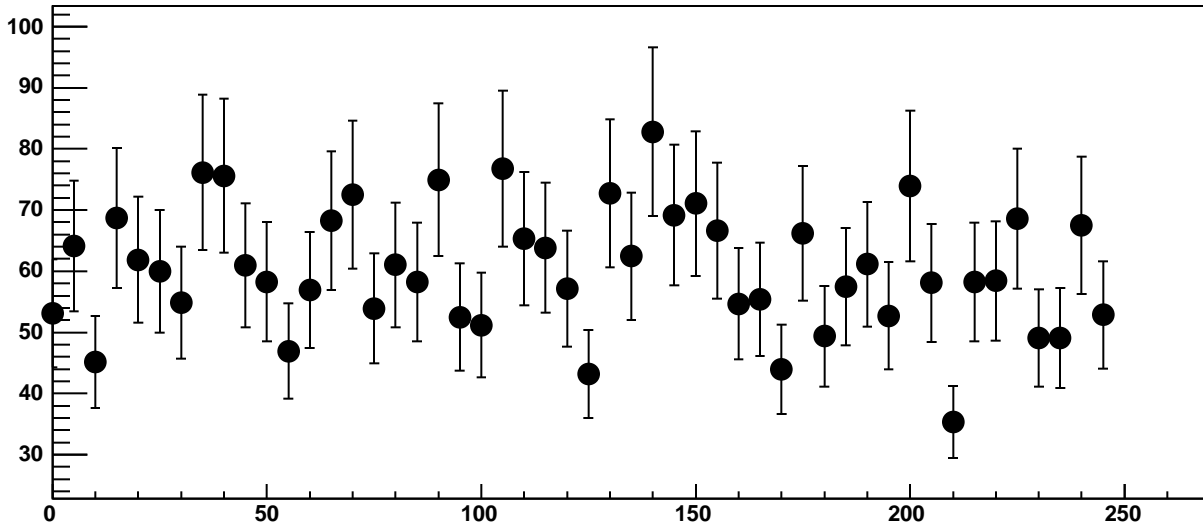
Chip 3, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold



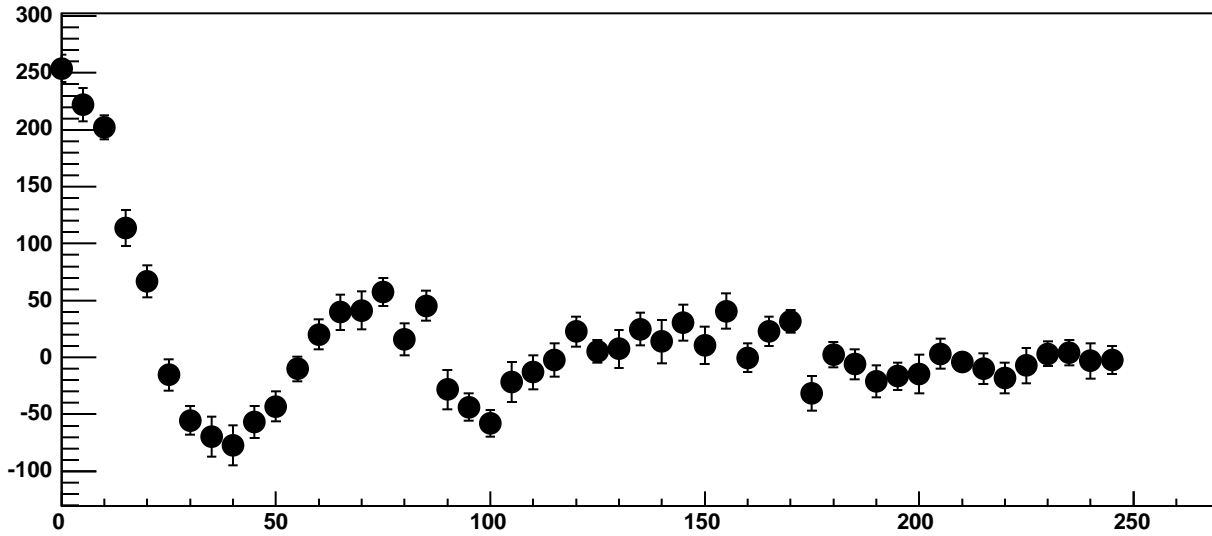
Chip 3, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold



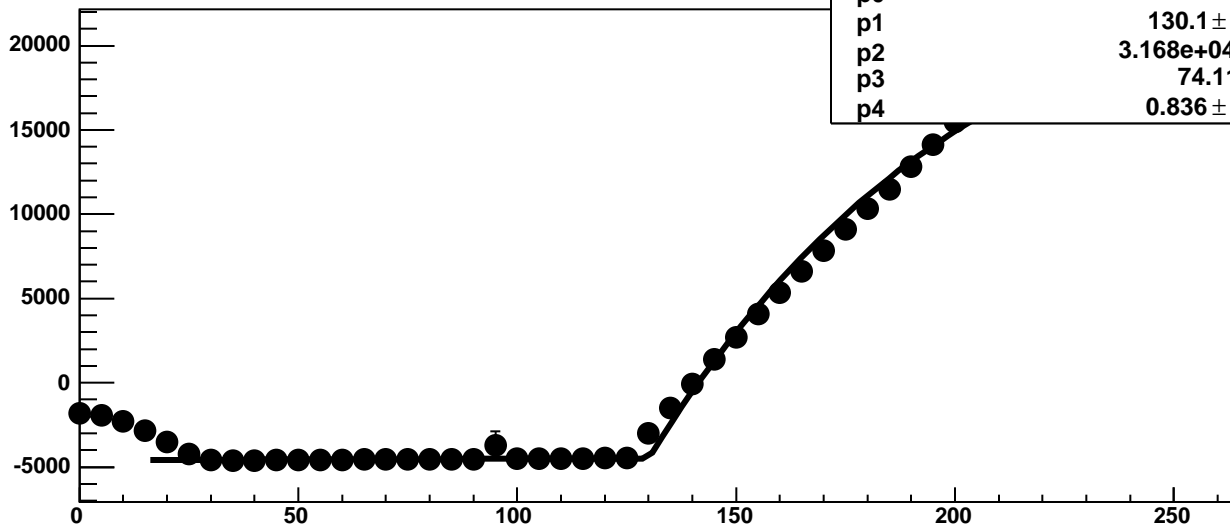
Chip 3, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

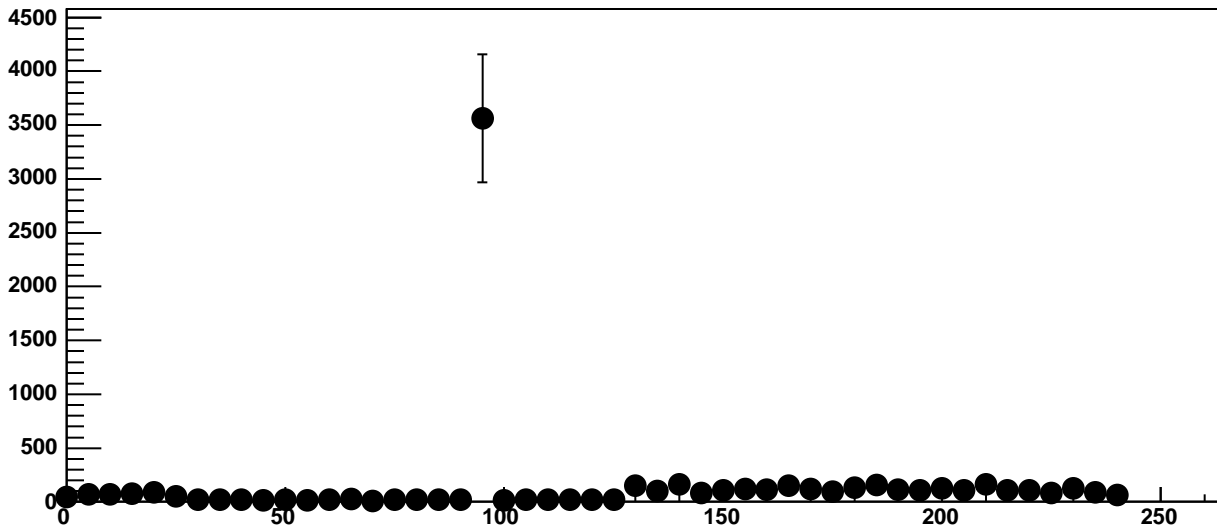


Chip 3, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

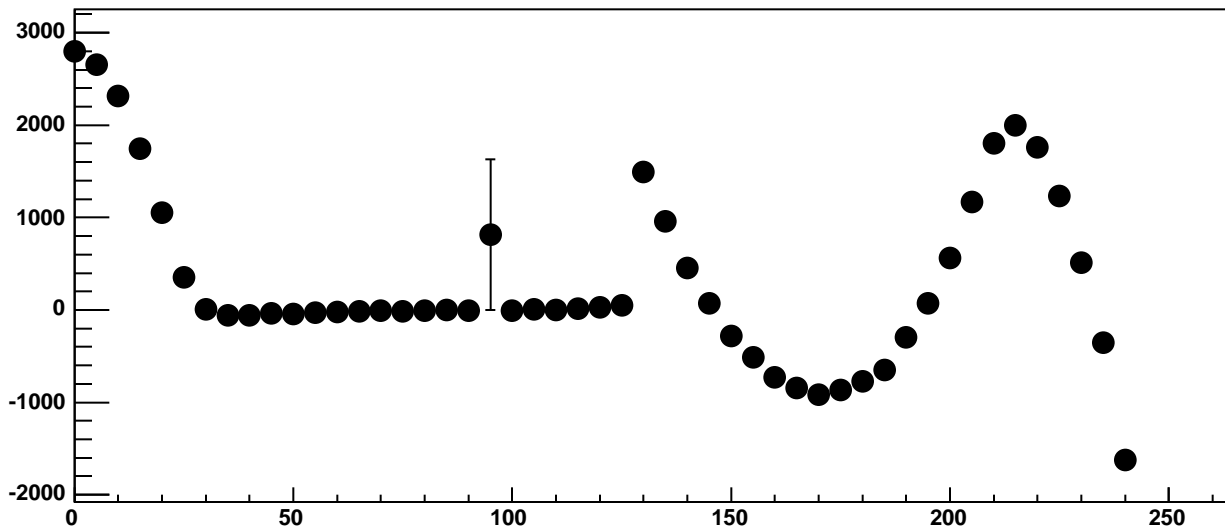


$\chi^2 / \text{ndf}$	5.778e+04 / 41
p0	-4489 ± 2.157
p1	130.1 ± 0.04713
p2	3.168e+04 ± 56.51
p3	74.11 ± 0.278
p4	0.836 ± 0.03493

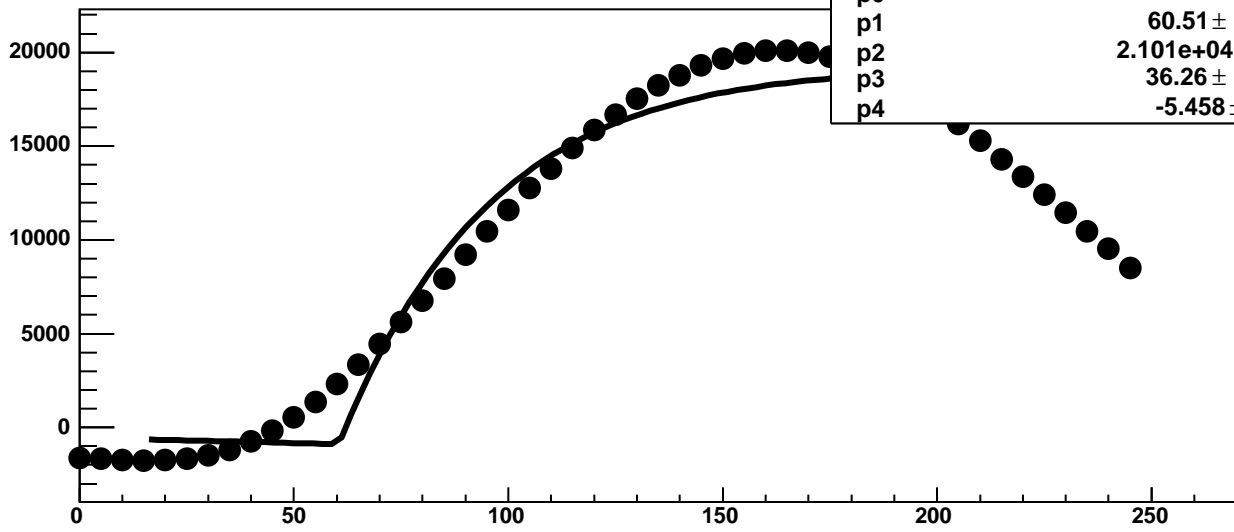
Chip 3, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

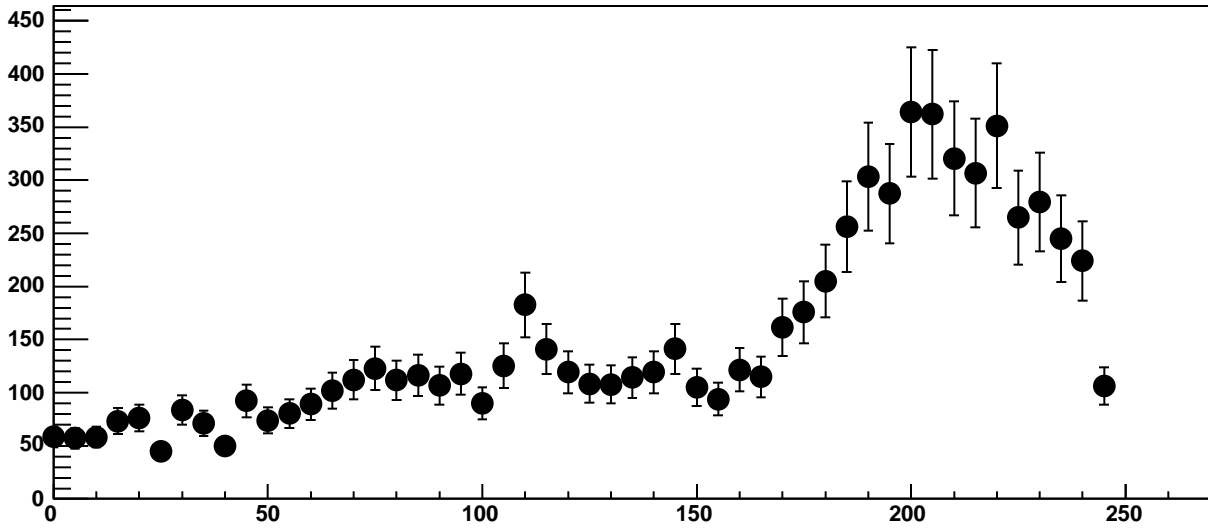


Chip 3, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

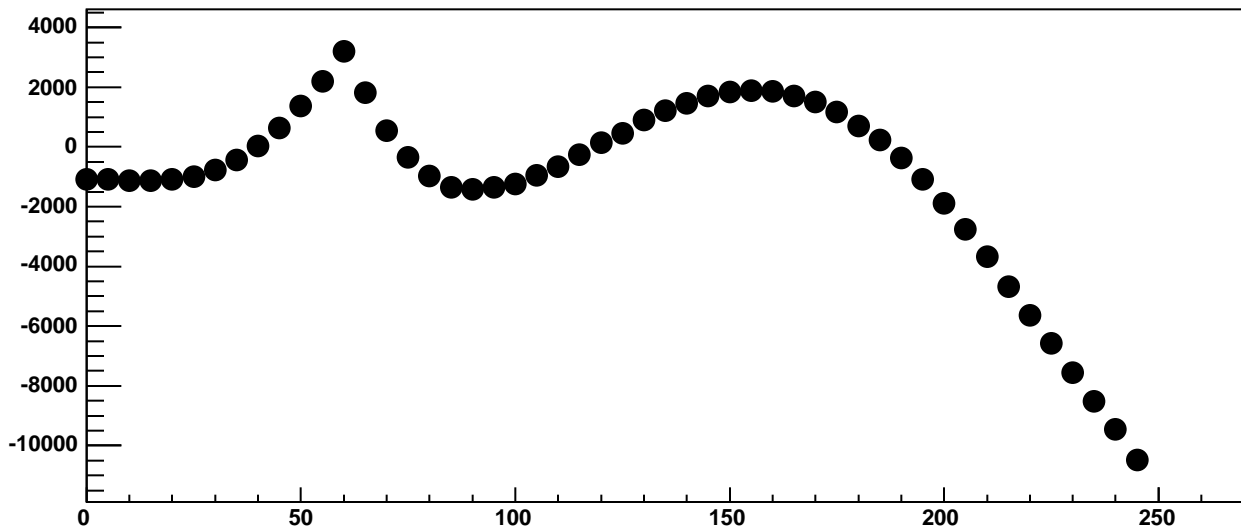


$\chi^2 / \text{ndf}$	2.181e+05 / 41
p0	-888.4 ± 8.227
p1	60.51 ± 0.03875
p2	2.101e+04 ± 43.24
p3	36.26 ± 0.09305
p4	-5.458 ± 0.2601

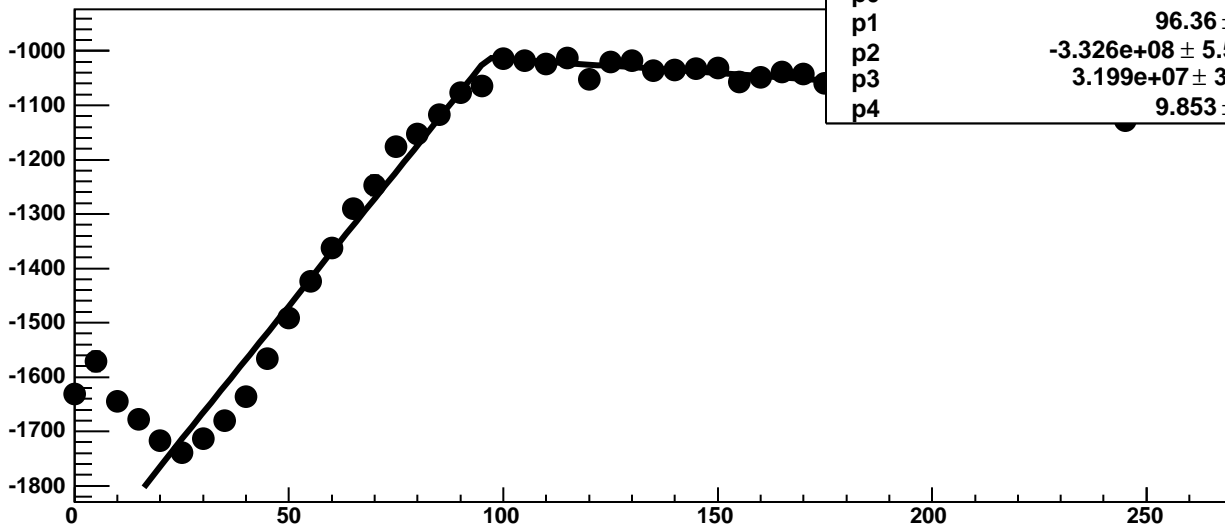
Chip 3, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

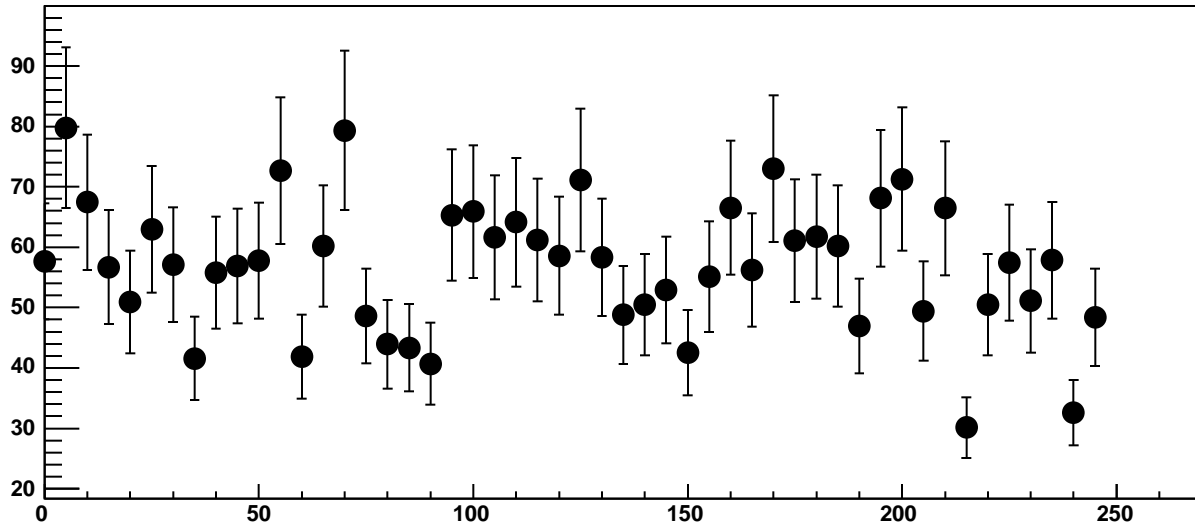


Chip 3, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold

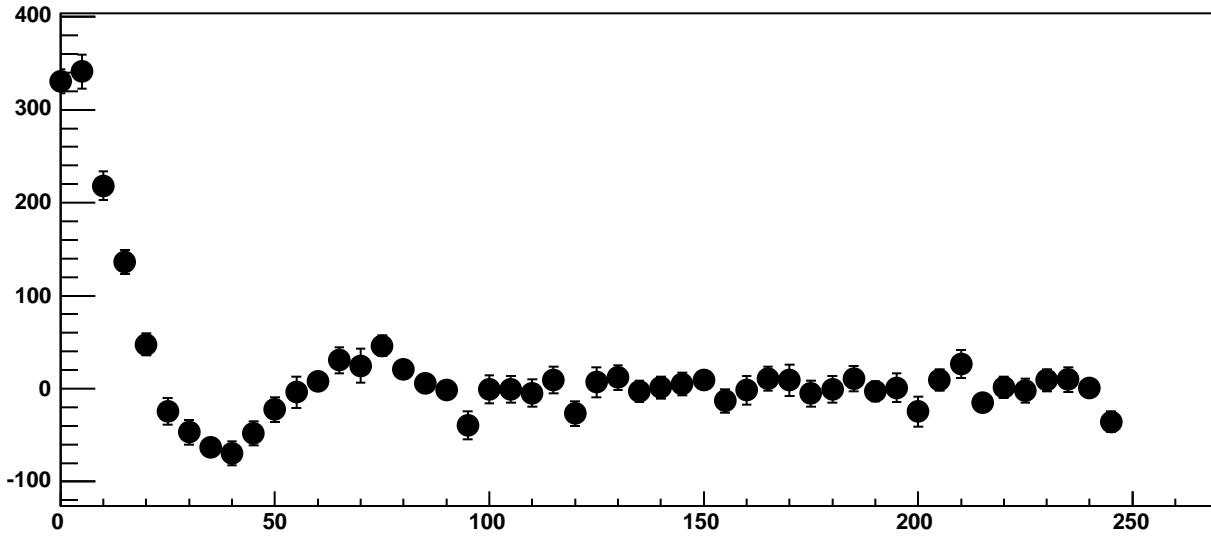


$\chi^2 / \text{ndf}$	290.4 / 41
p0	-1012 ± 4.662
p1	96.36 ± 0.7017
p2	-3.326e+08 ± 5.543e+06
p3	3.199e+07 ± 3.59e+05
p4	9.853 ± 0.1166

Chip 3, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

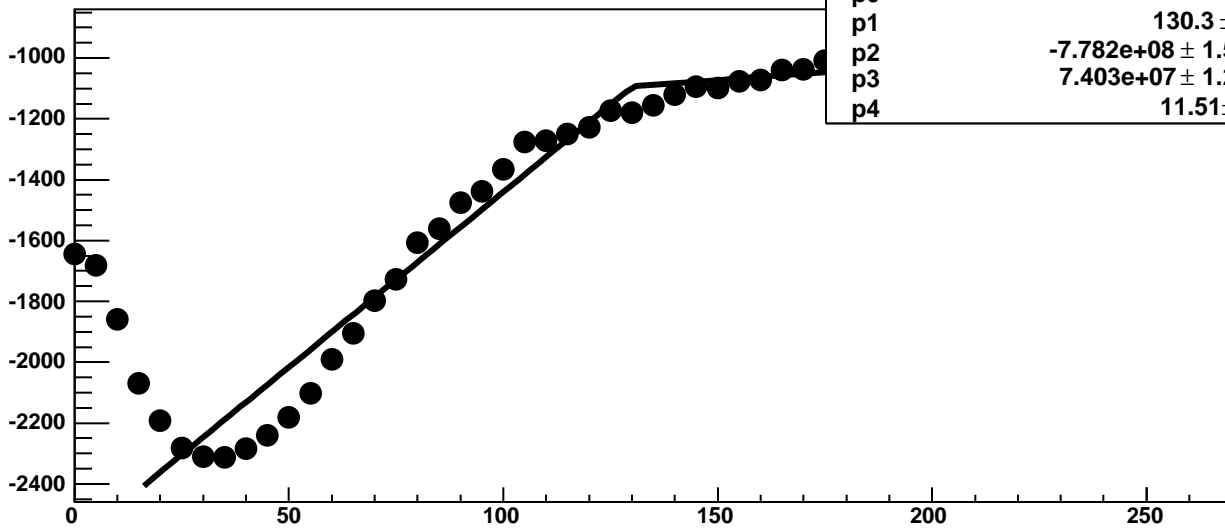


Chip 3, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold



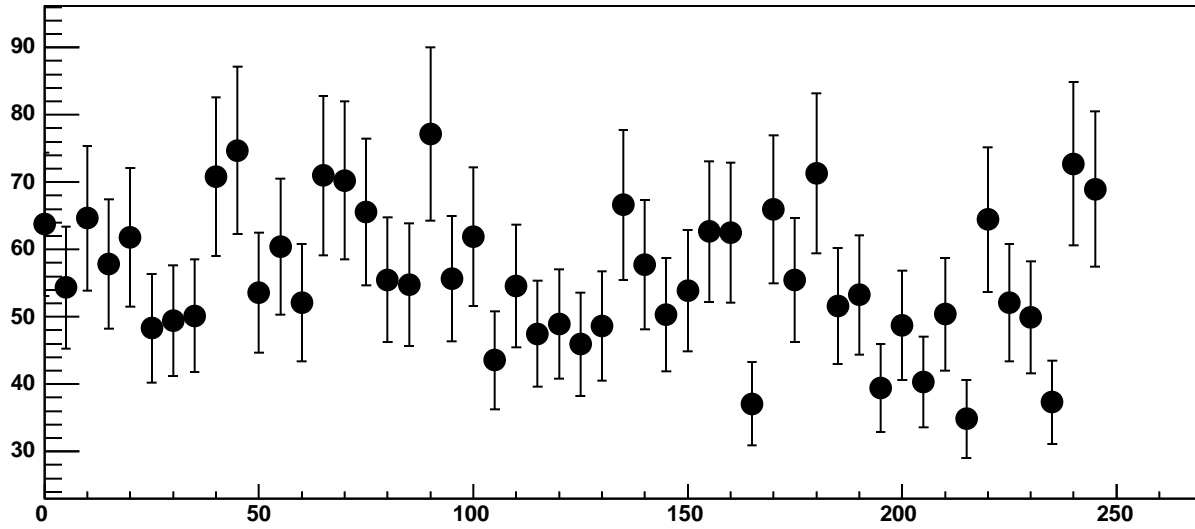


Chip 3, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

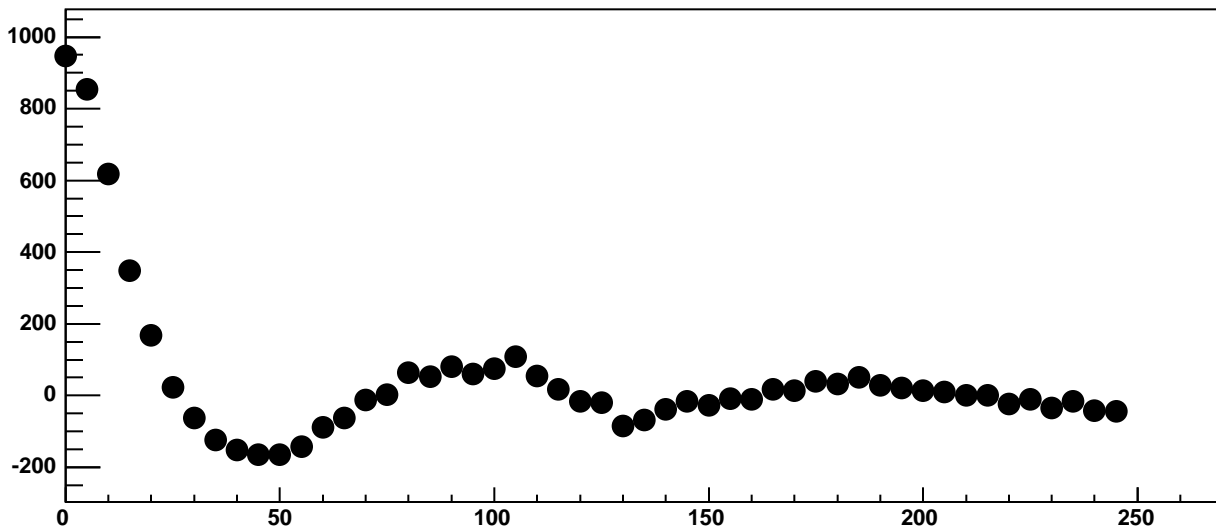


$\chi^2 / \text{ndf}$	1947 / 41
p0	-1092 ± 6.088
p1	130.3 ± 0.6884
p2	-7.782e+08 ± 1.538e+07
p3	7.403e+07 ± 1.212e+06
p4	11.51 ± 0.0712

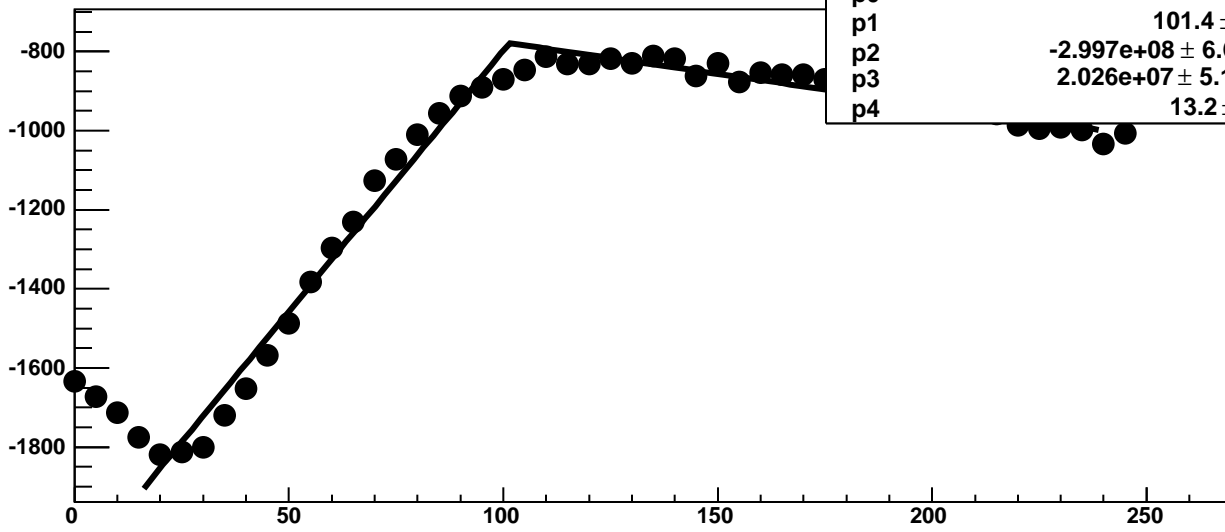
Chip 3, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

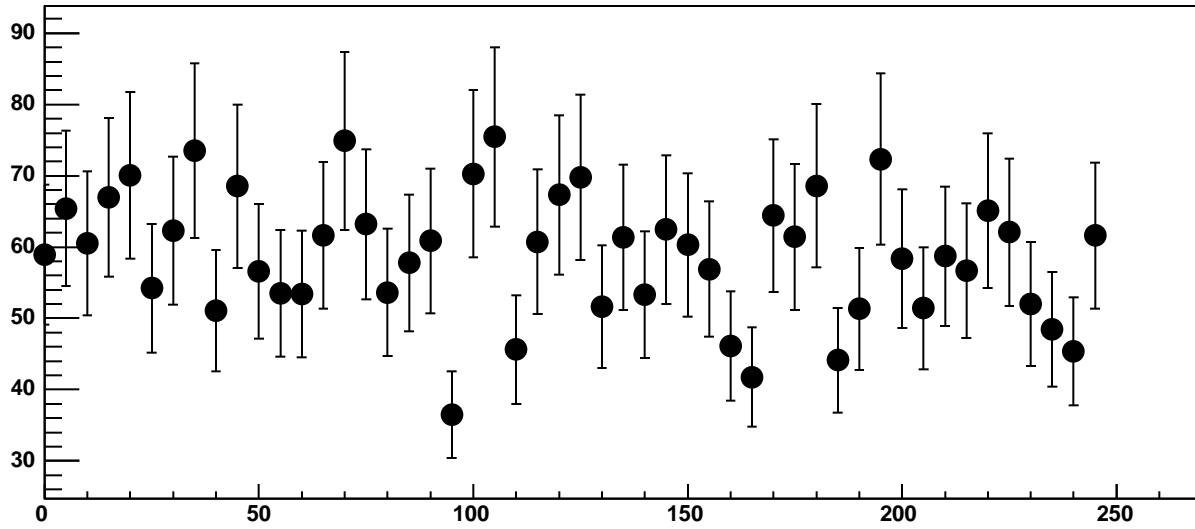


Chip 3, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

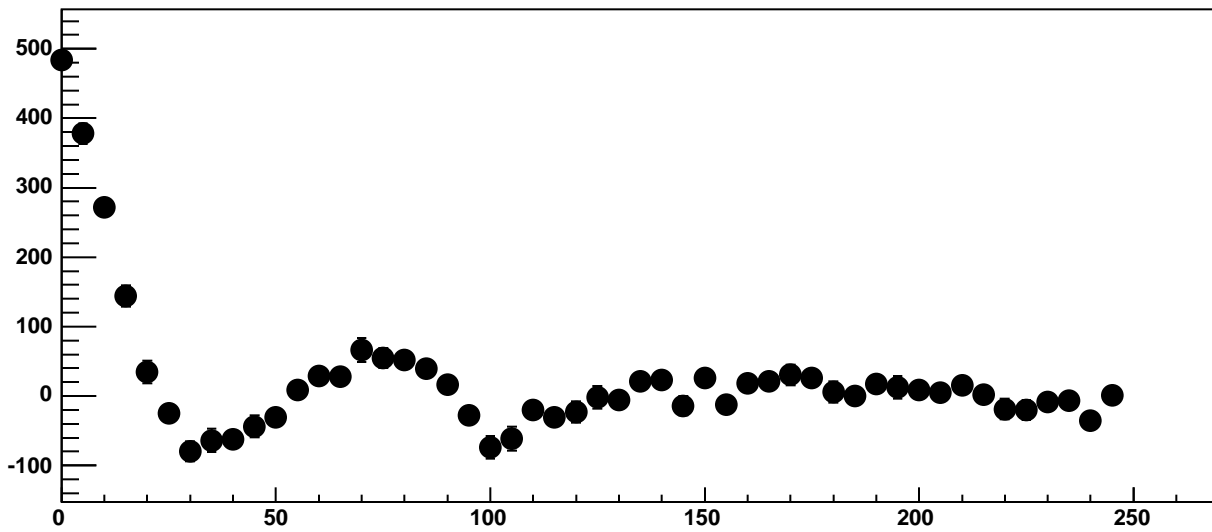


$\chi^2 / \text{ndf}$	353.3 / 41
p0	$-778.8 \pm 4.423$
p1	$101.4 \pm 0.4756$
p2	$-2.997\text{e}+08 \pm 6.607\text{e}+06$
p3	$2.026\text{e}+07 \pm 5.171\text{e}+05$
p4	$13.2 \pm 0.1108$

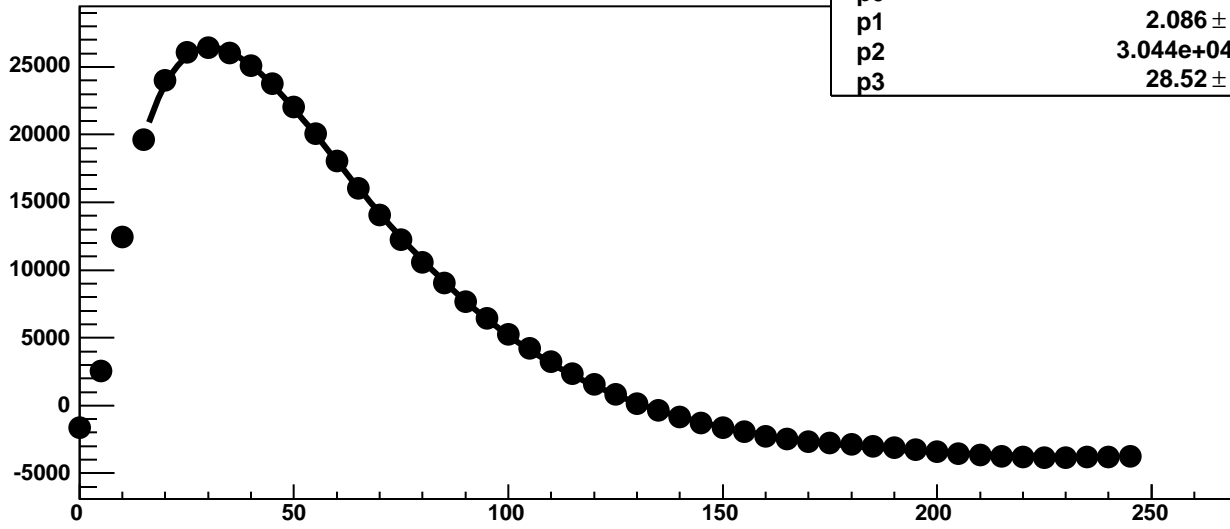
Chip 3, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

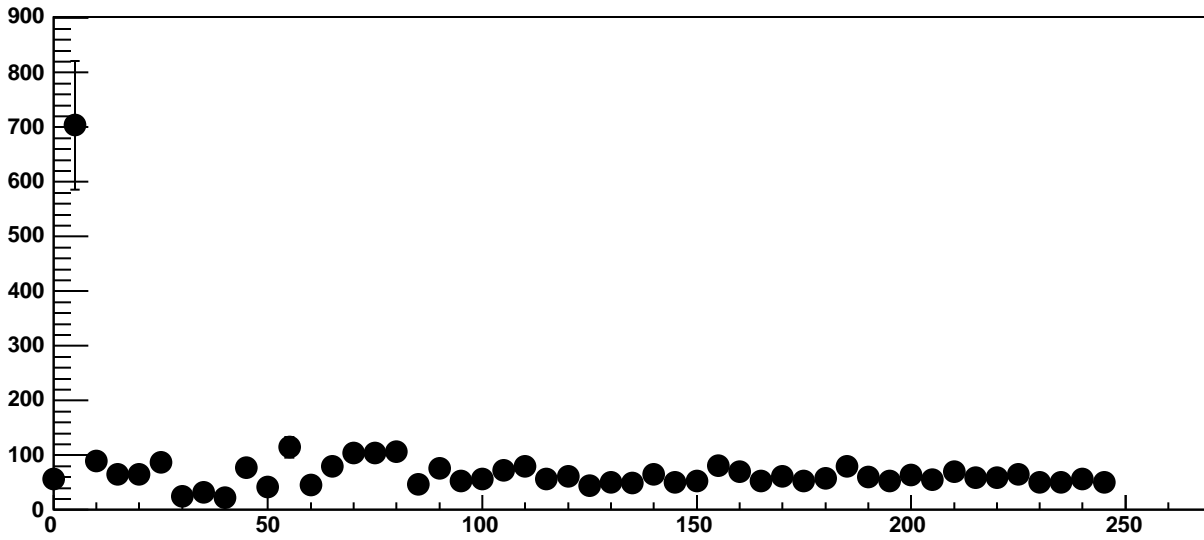


Chip 3, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold

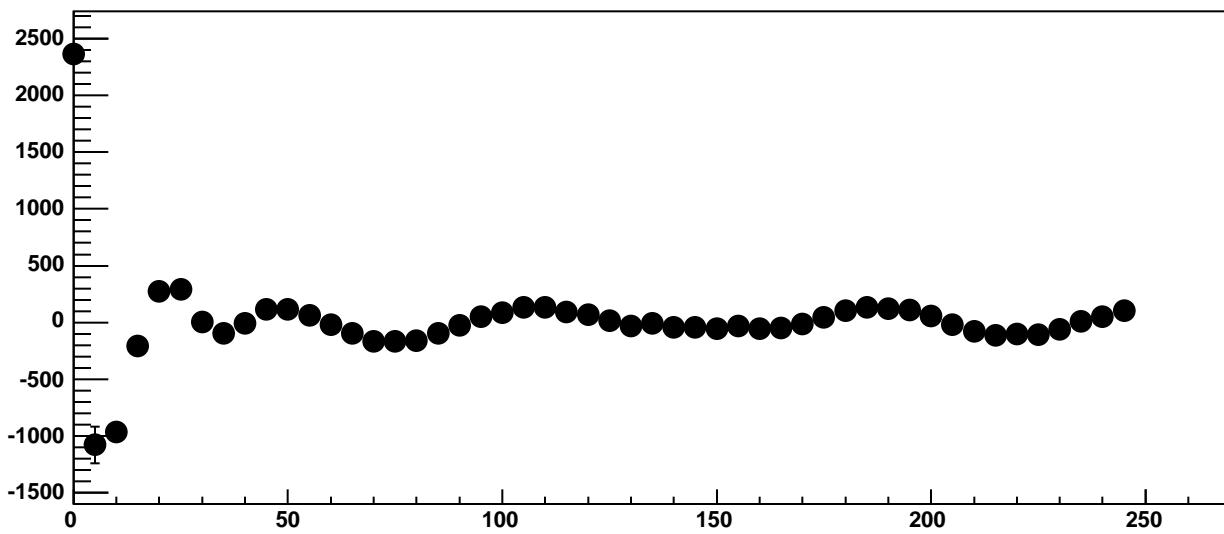


$\chi^2 / \text{ndf}$	2263 / 42
p0	-3995 ± 3.725
p1	2.086 ± 0.01509
p2	3.044e+04 ± 4.558
p3	28.52 ± 0.01008

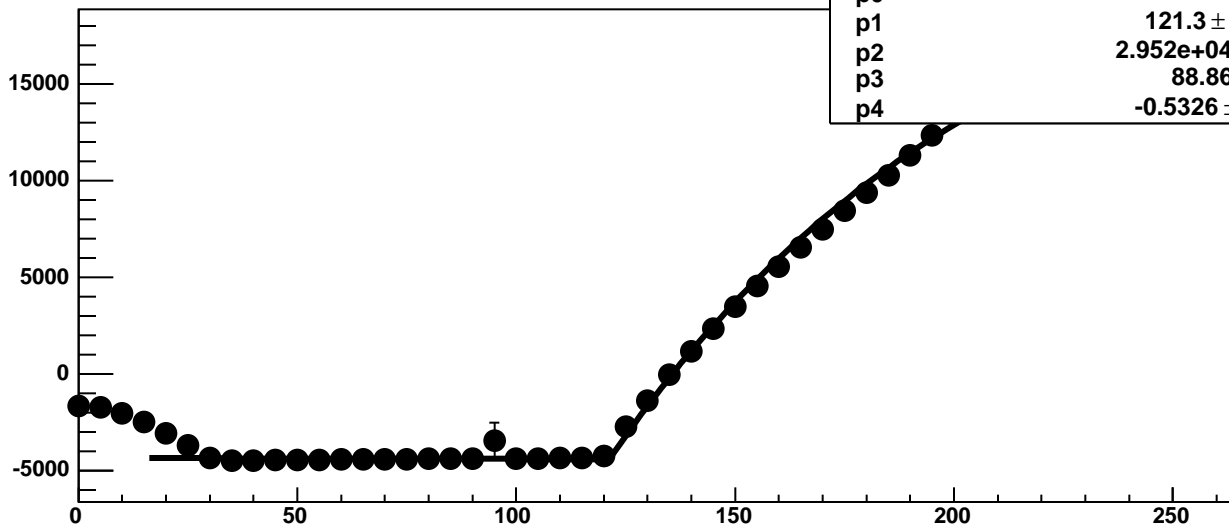
Chip 3, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



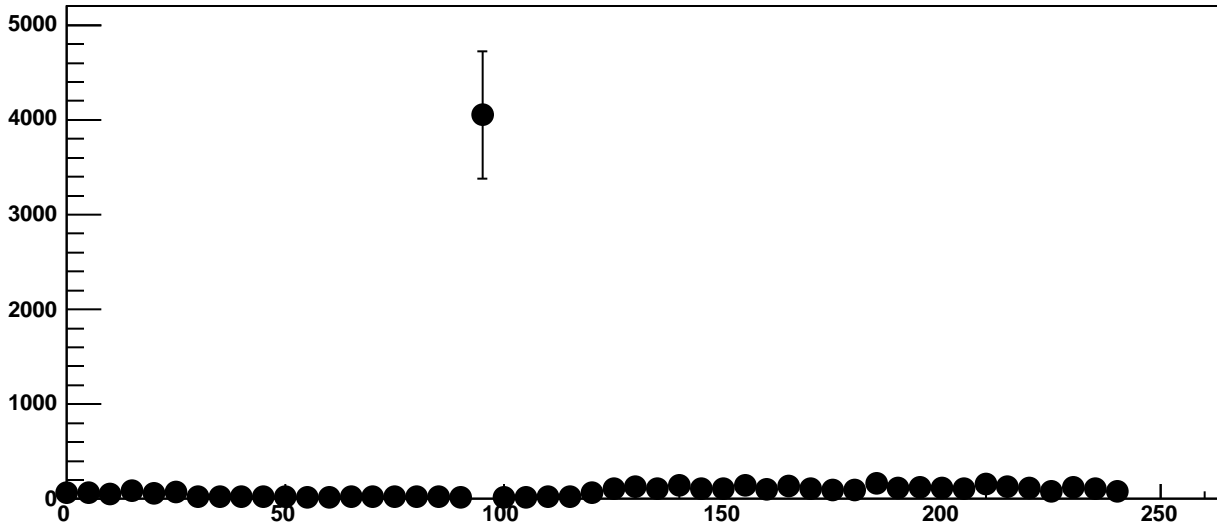
Chip 3, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold



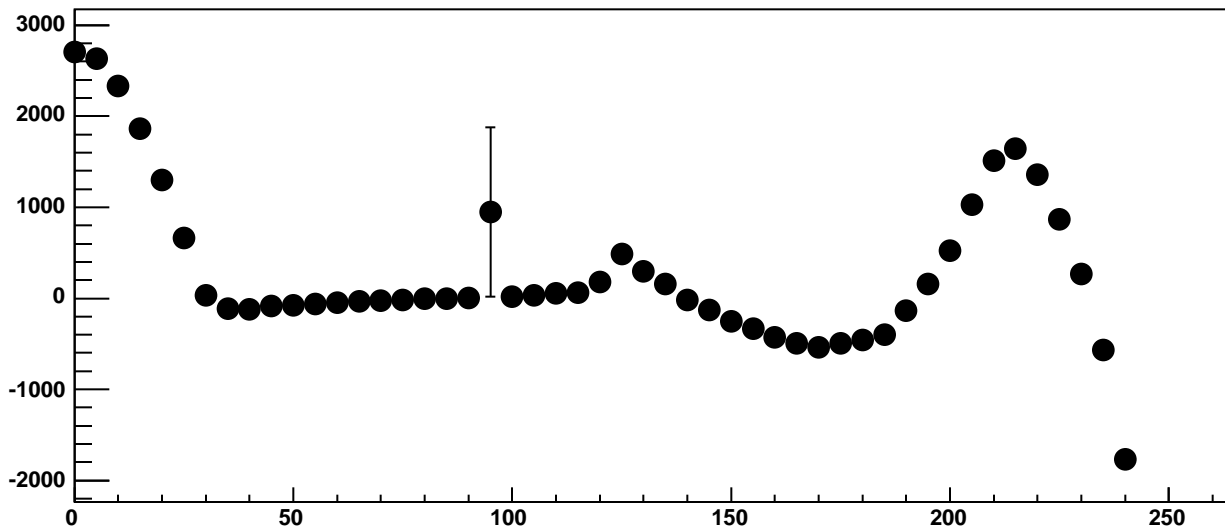
Chip 3, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold



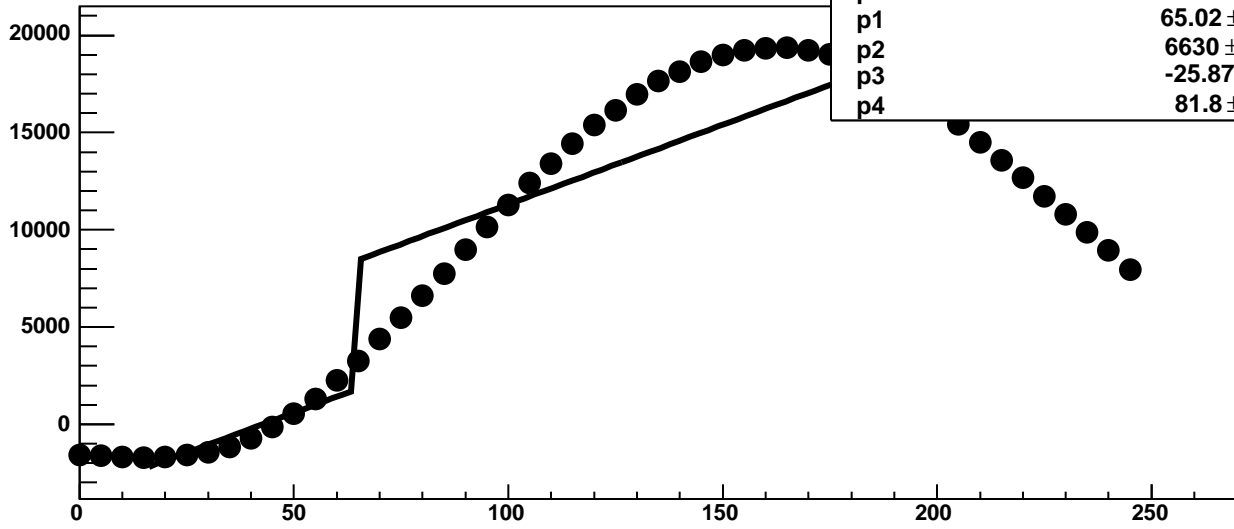
Chip 3, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

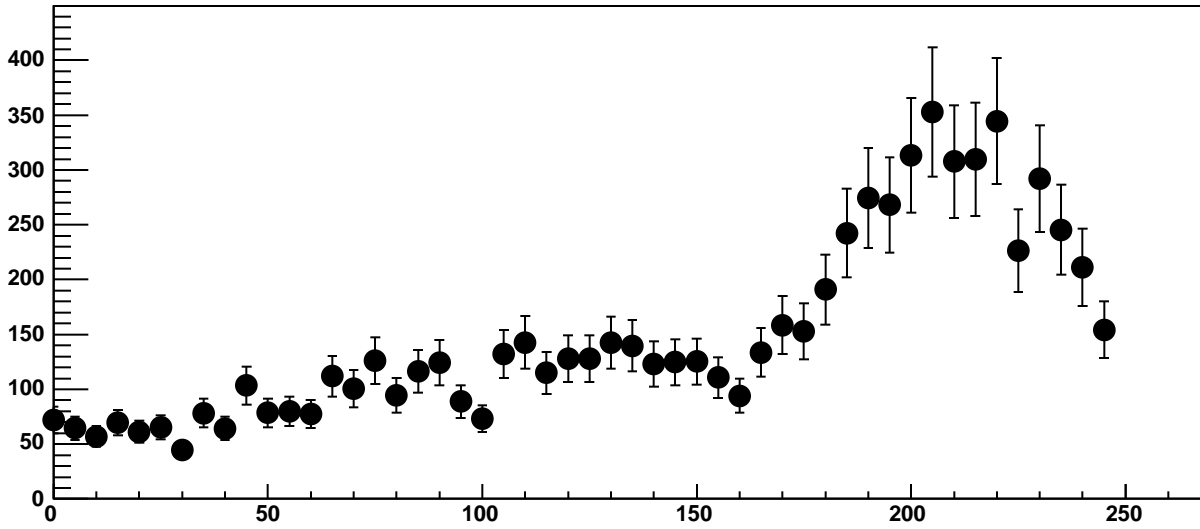


Chip 3, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

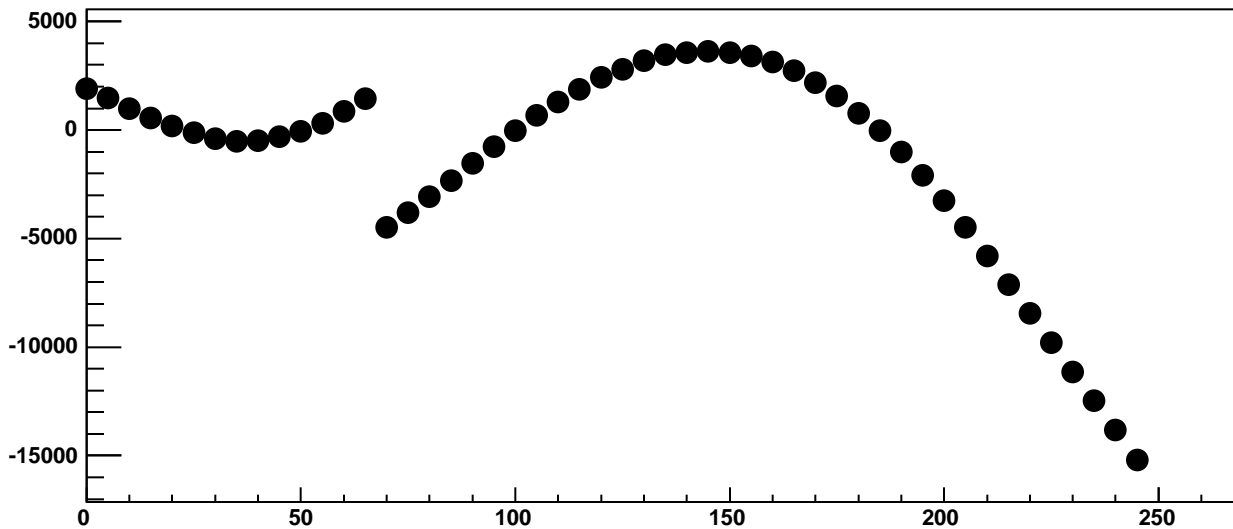


$\chi^2 / \text{ndf}$	4.715e+05 / 41
p0	1822 ± 0.1268
p1	65.02 ± 0.3627
p2	6630 ± 0.1294
p3	-25.87 ± 12.38
p4	81.8 ± 0.1243

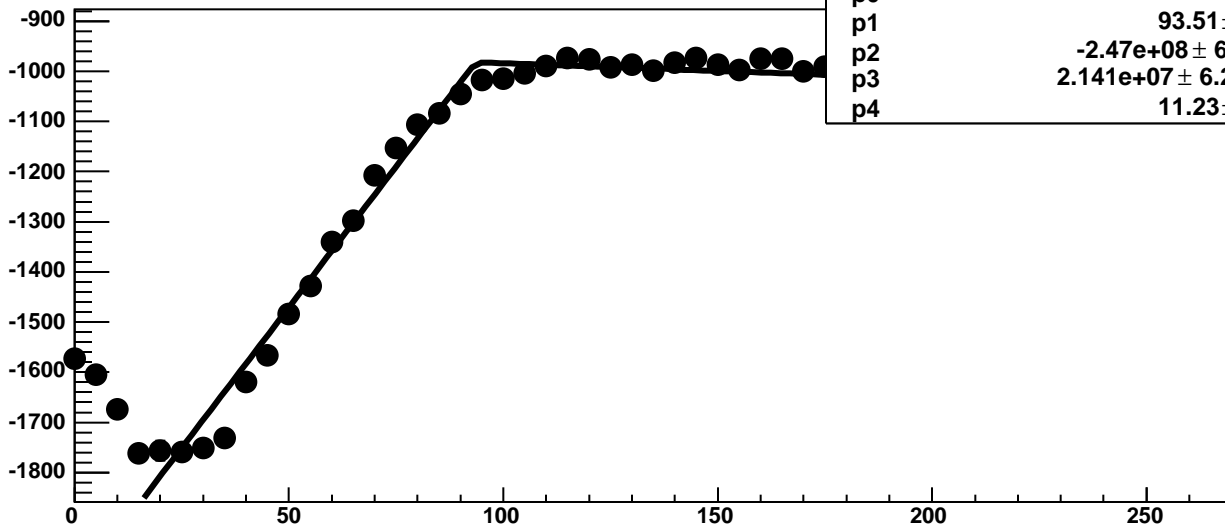
Chip 3, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

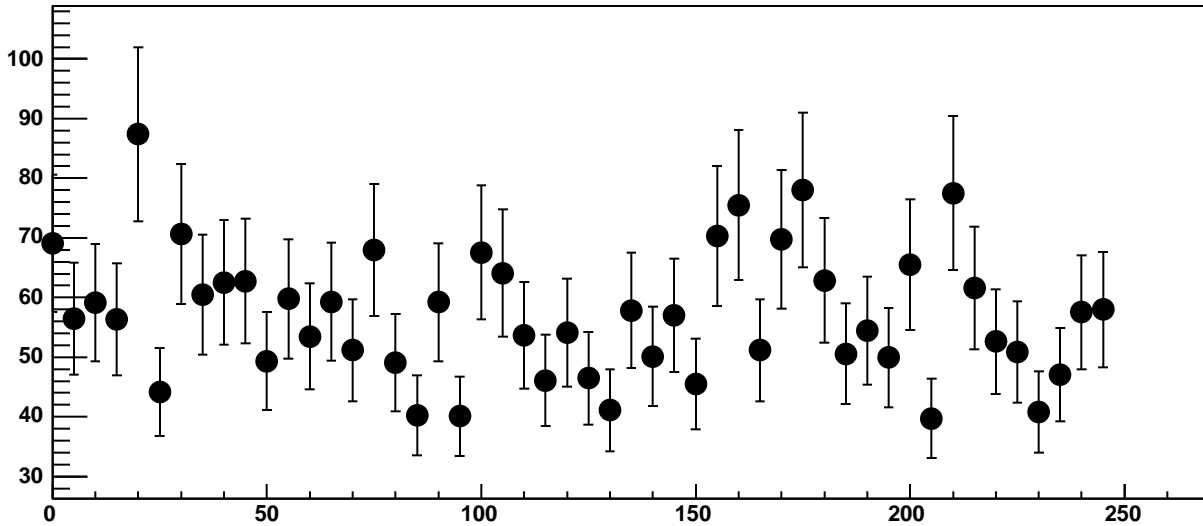


Chip 3, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

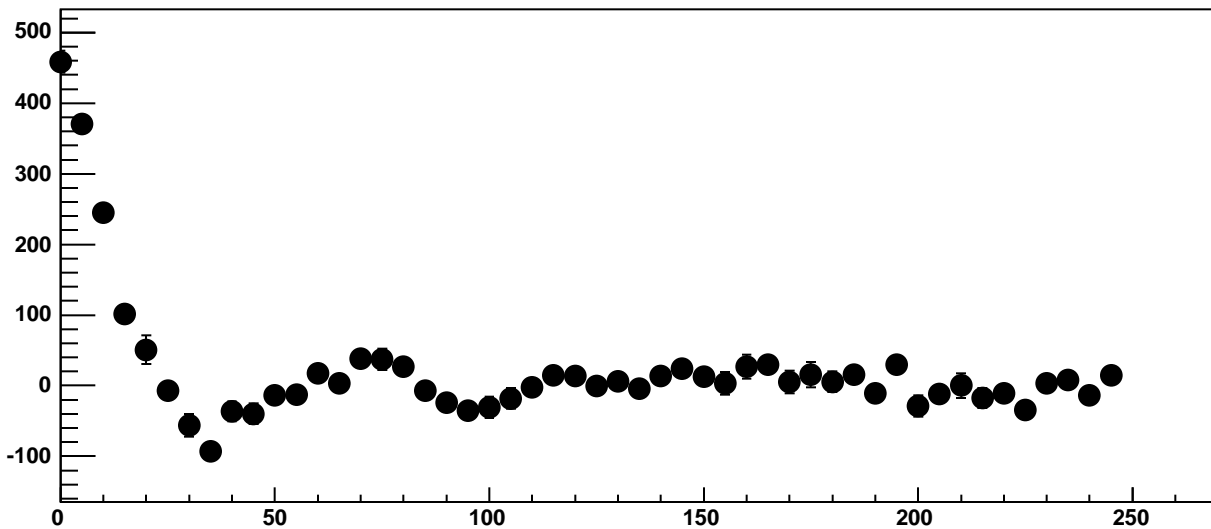


$\chi^2 / \text{ndf}$	237.8 / 41
p0	-981.8 ± 4.034
p1	93.51 ± 0.5812
p2	-2.47e+08 ± 6.31e+06
p3	2.141e+07 ± 6.247e+05
p4	11.23 ± 0.1193

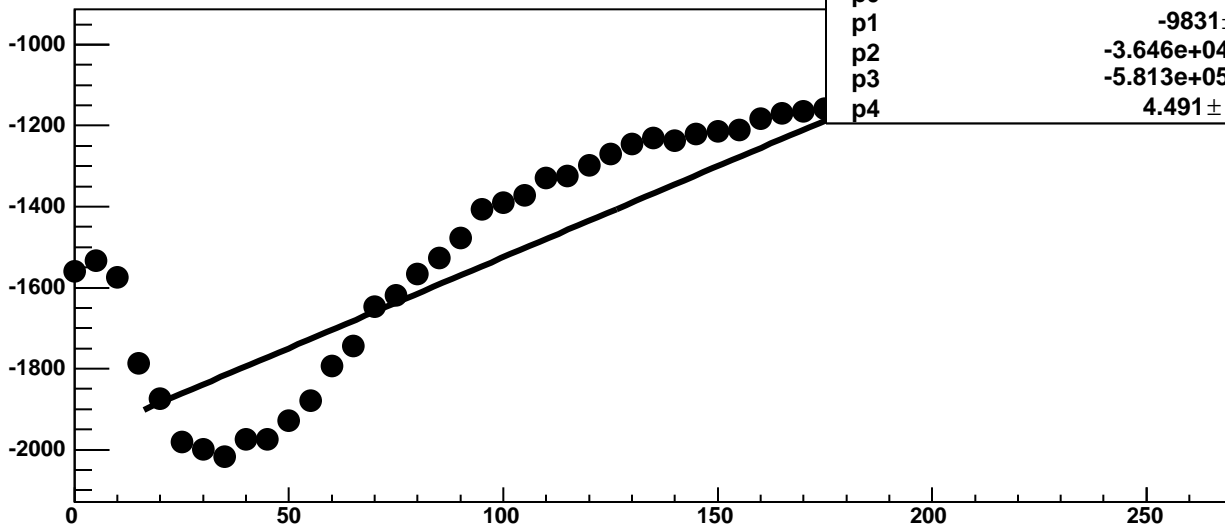
Chip 3, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

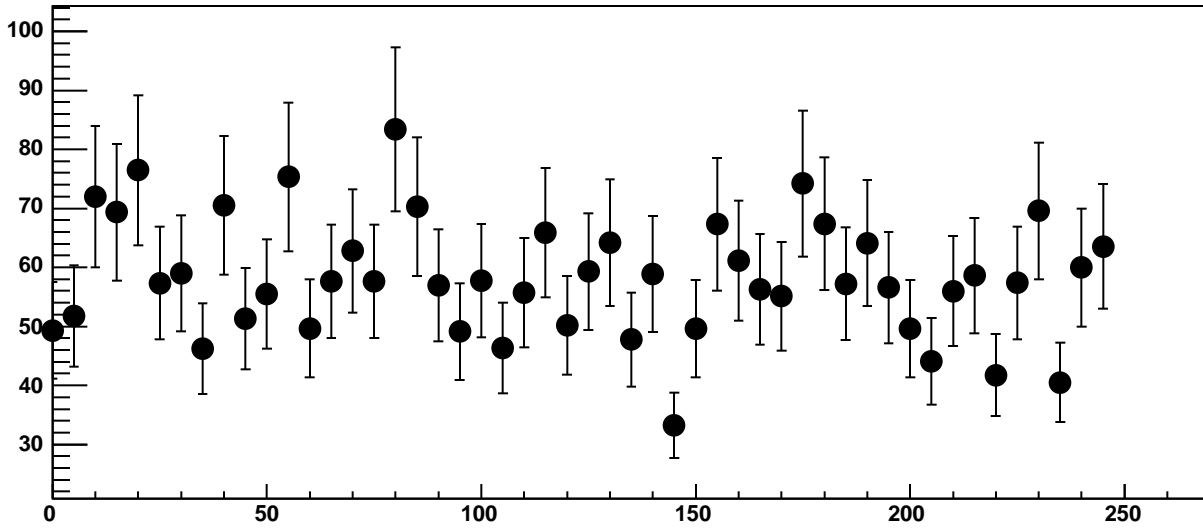


Chip 3, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

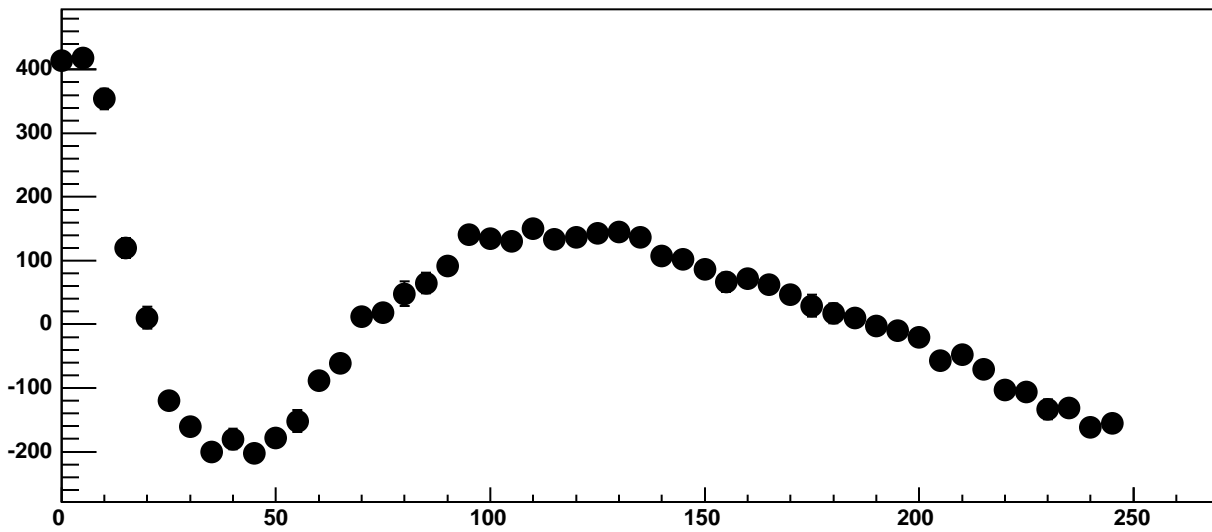


$\chi^2 / \text{ndf}$	3668 / 41
p0	-9660 ± 61.12
p1	-9831 ± 0.7217
p2	-3.646e+04 ± 225.5
p3	-5.813e+05 ± 3533
p4	4.491 ± 0.02857

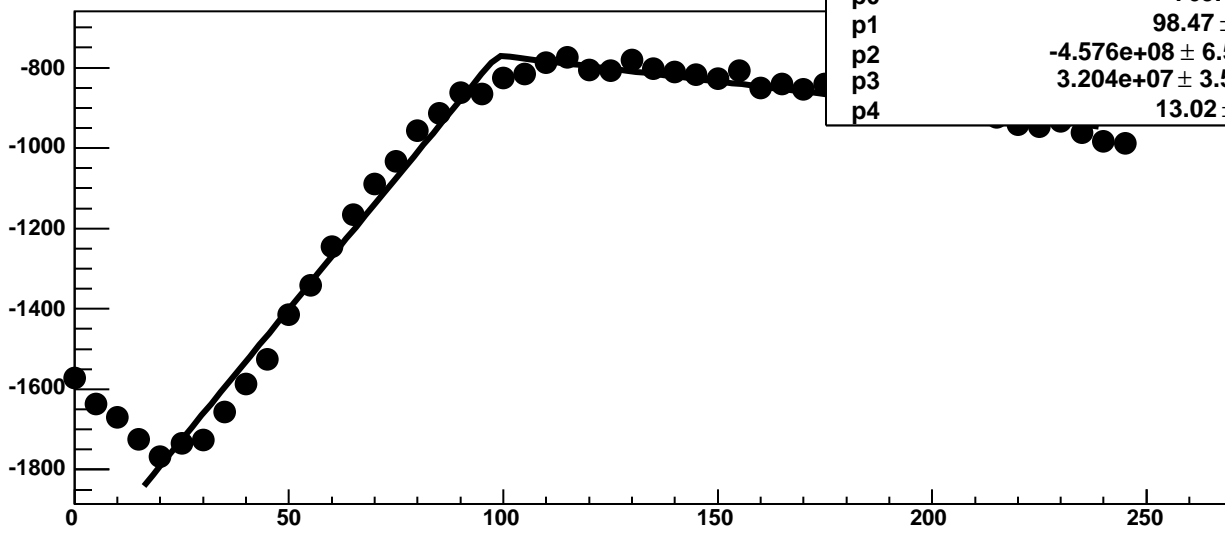
Chip 3, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold

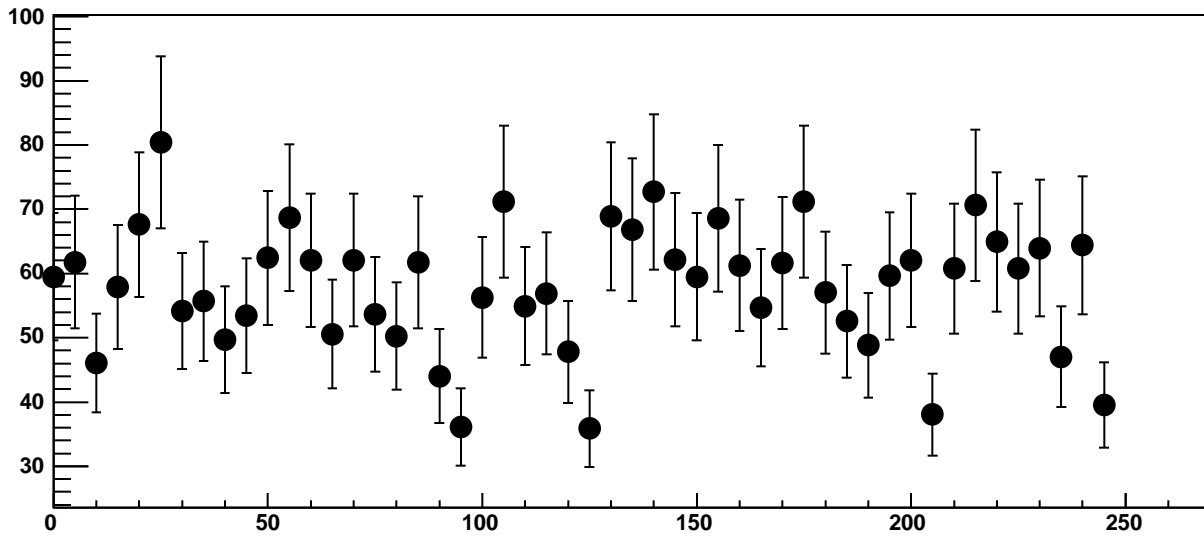


Chip 3, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

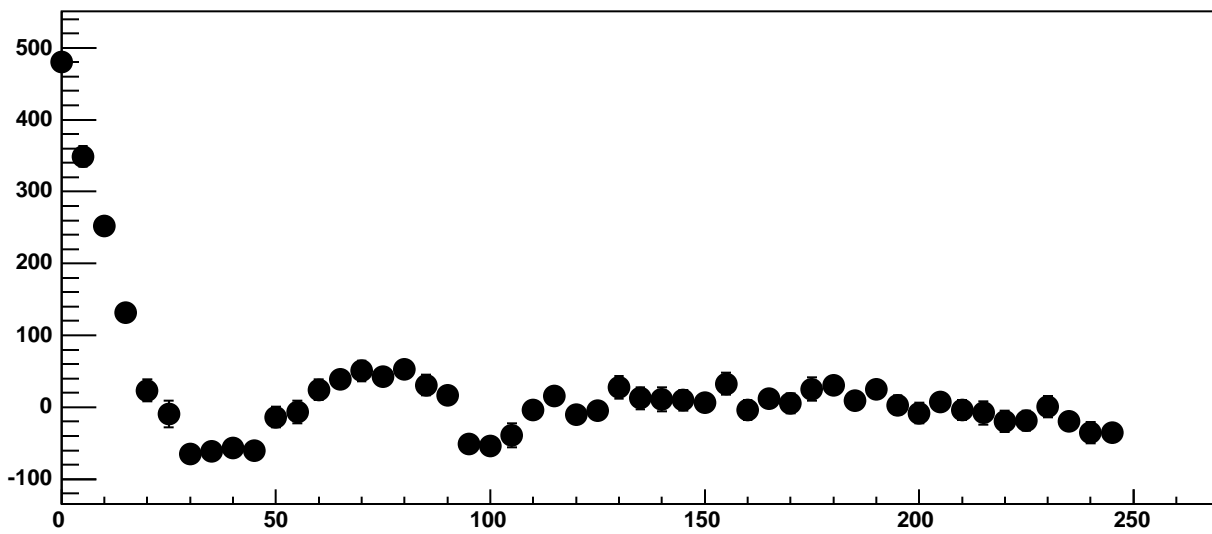


$\chi^2 / \text{ndf}$	371.5 / 41
p0	-769.1 ± 4.331
p1	98.47 ± 0.5024
p2	-4.576e+08 ± 6.576e+06
p3	3.204e+07 ± 3.584e+05
p4	13.02 ± 0.1183

Chip 3, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

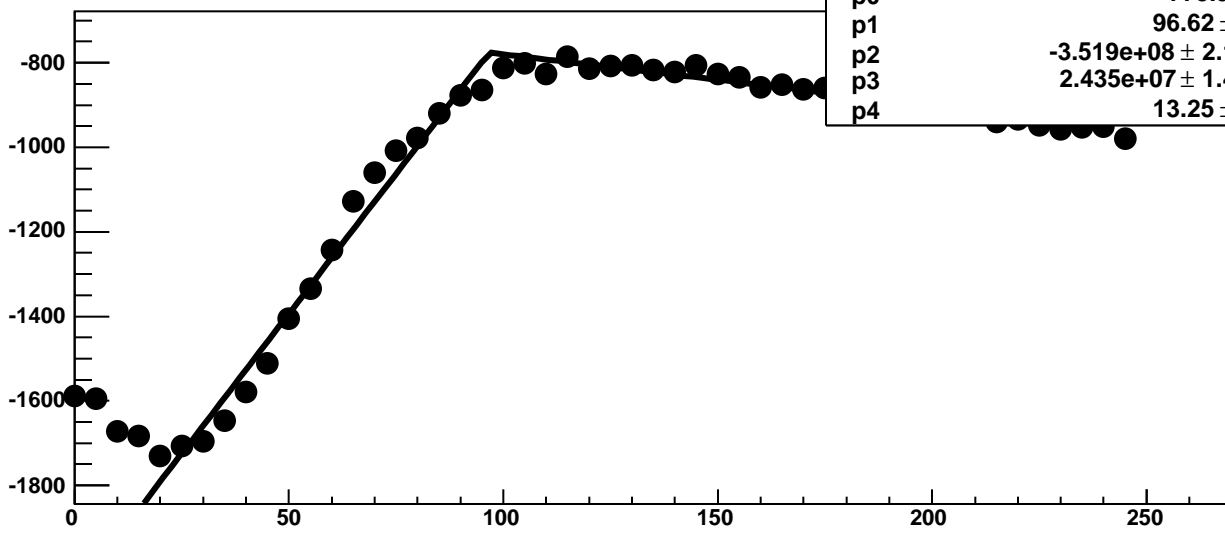


Chip 3, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold



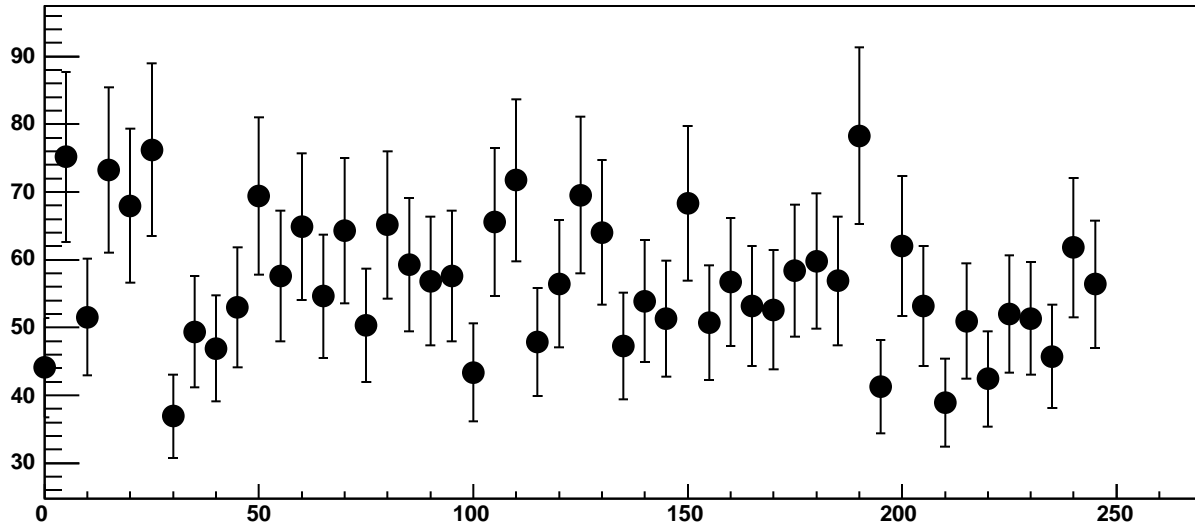


Chip 3, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

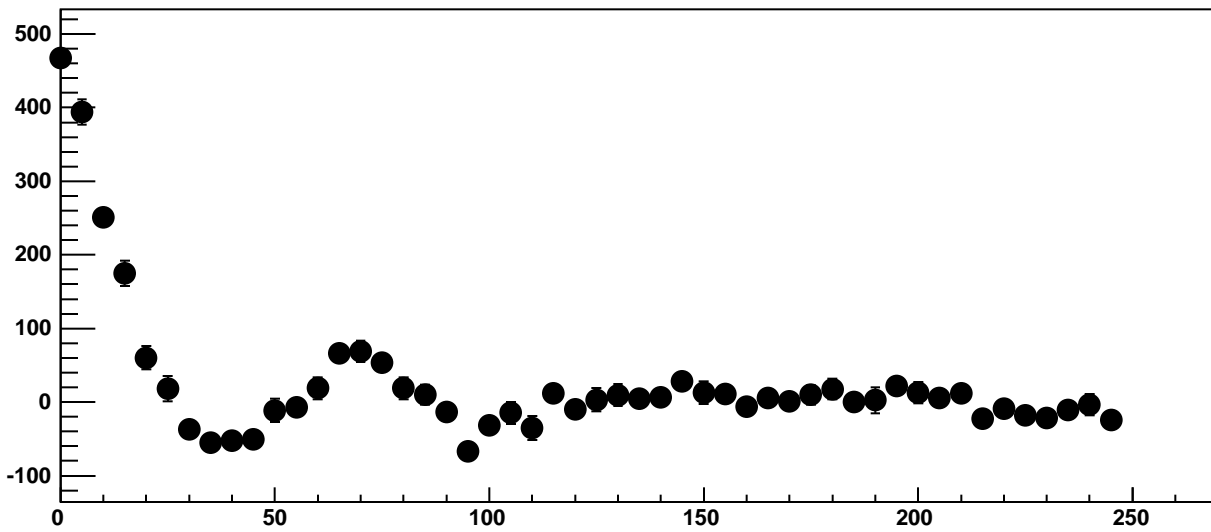


$\chi^2 / \text{ndf}$	359.4 / 41
p0	$-775.9 \pm 4.344$
p1	$96.62 \pm 0.5526$
p2	$-3.519\text{e}+08 \pm 2.168\text{e}+07$
p3	$2.435\text{e}+07 \pm 1.451\text{e}+06$
p4	$13.25 \pm 0.1325$

Chip 3, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold

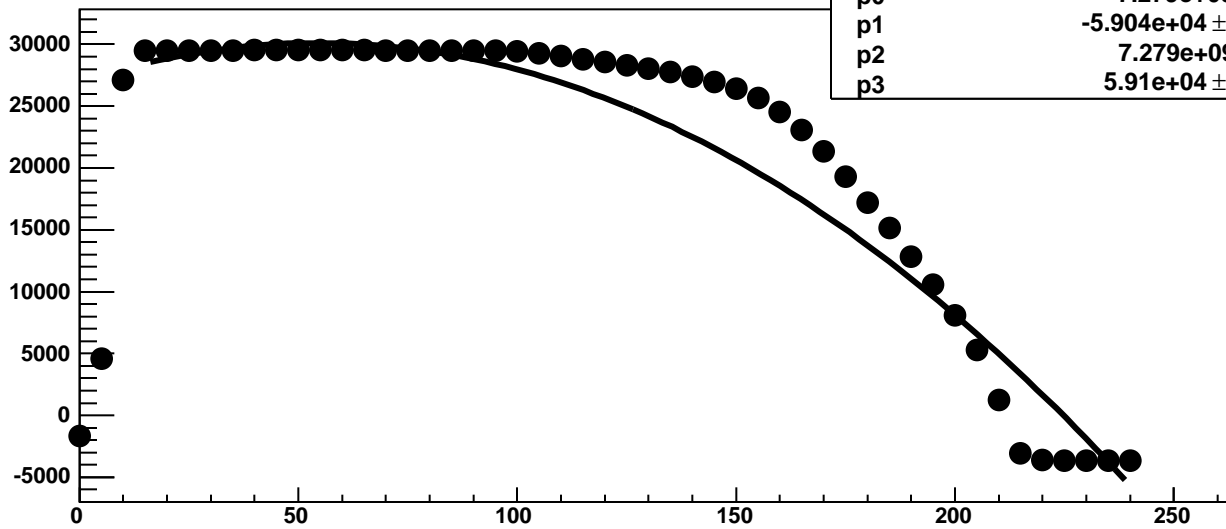


Chip 3, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

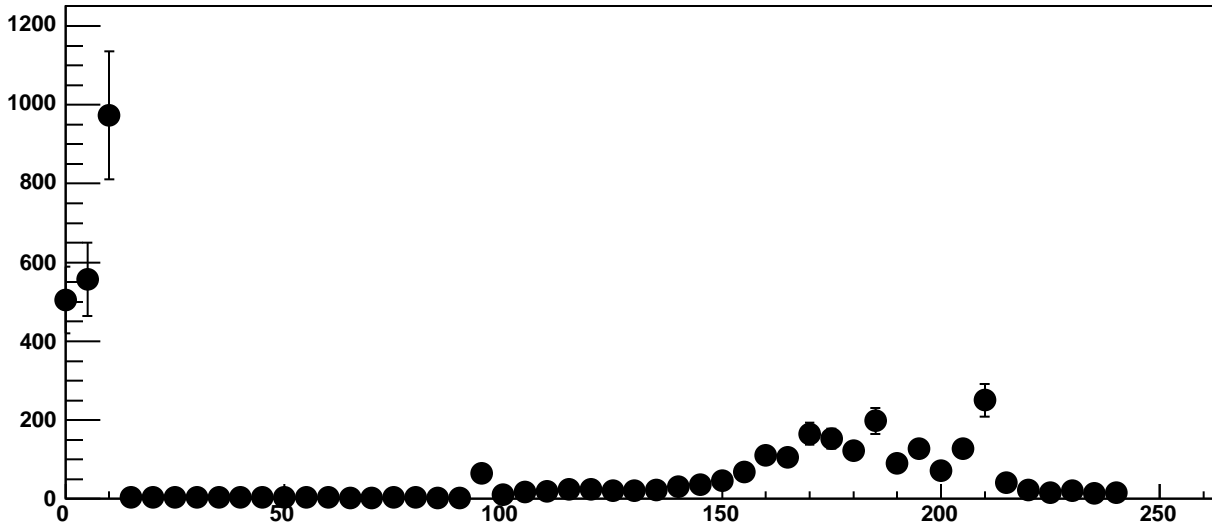


Chip 3, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold

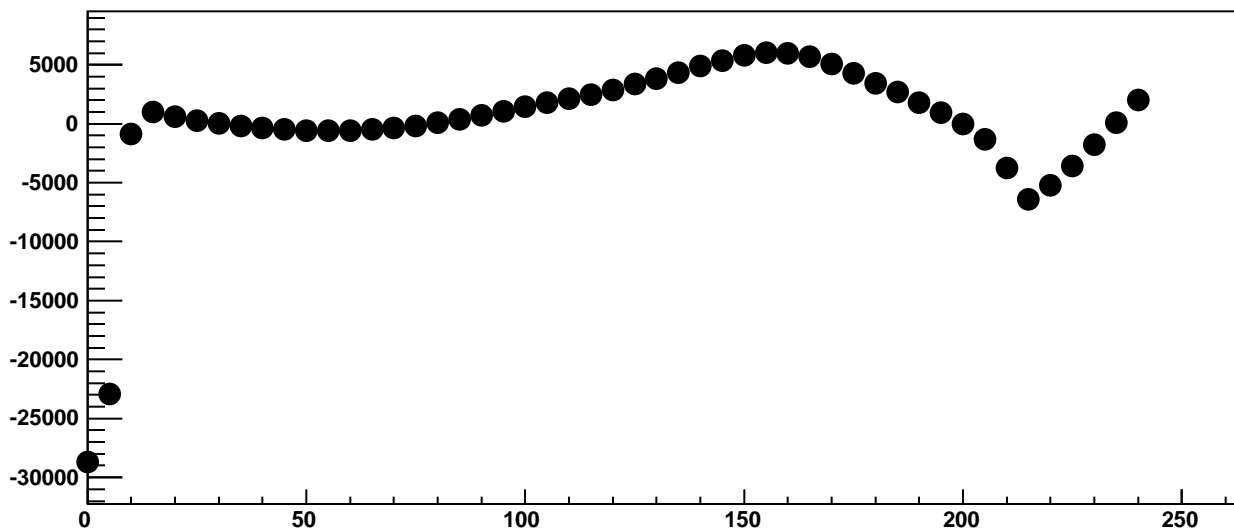
$\chi^2 / \text{ndf}$	1.283e+07 / 42
p0	-7.279e+09 $\pm$ 2.968
p1	-5.904e+04 $\pm$ 0.04038
p2	7.279e+09 $\pm$ 2.968
p3	5.91e+04 $\pm$ 0.04033



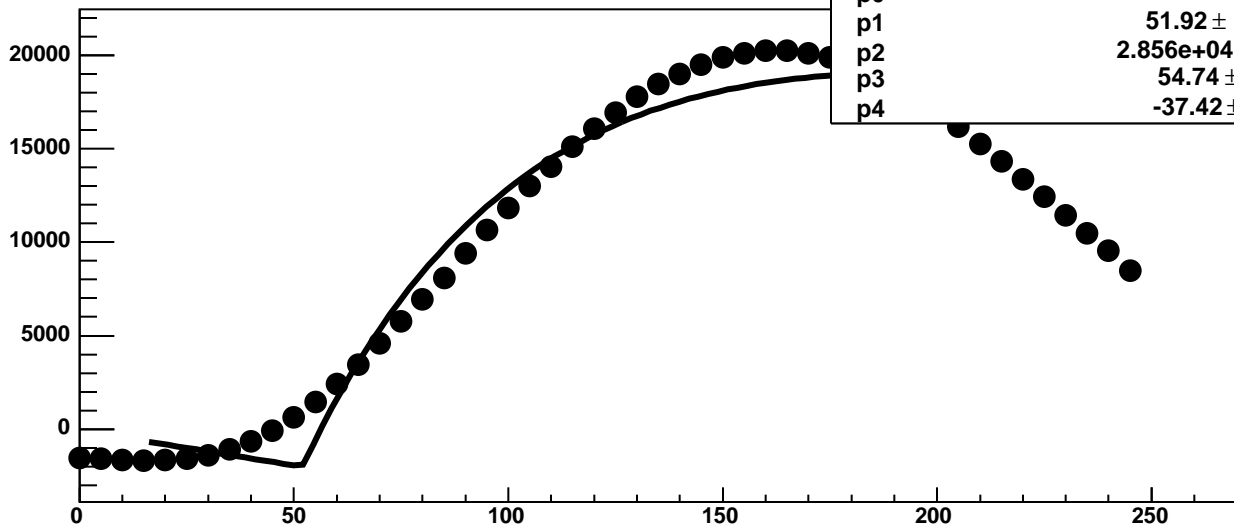
Chip 3, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

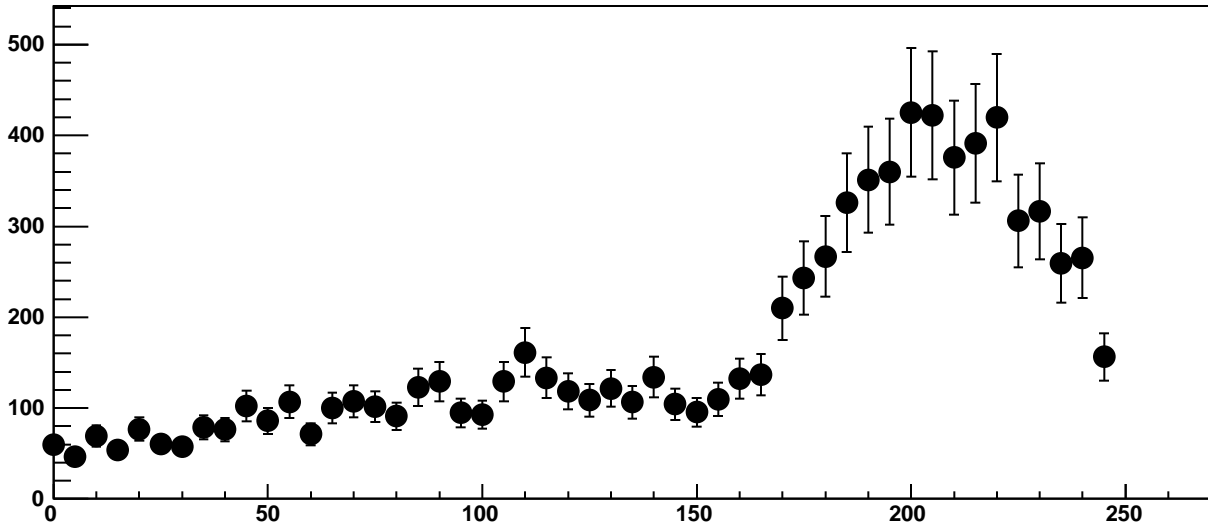


Chip 3, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

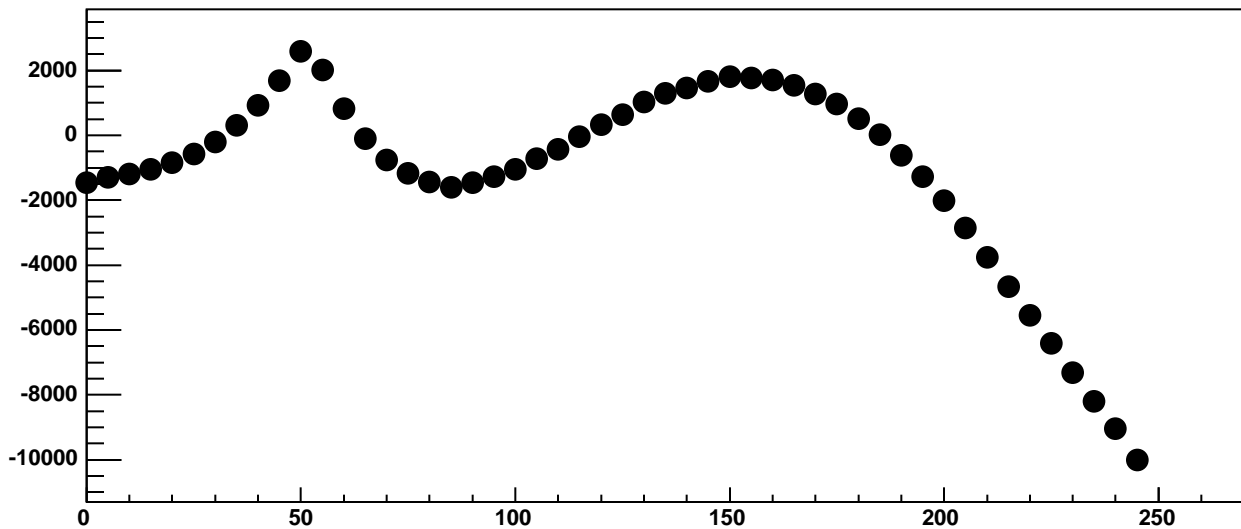


$\chi^2 / \text{ndf}$	1.66e+05 / 41
p0	-2018 ± 9.51
p1	51.92 ± 0.03476
p2	2.856e+04 ± 74.12
p3	54.74 ± 0.1396
p4	-37.42 ± 0.3699

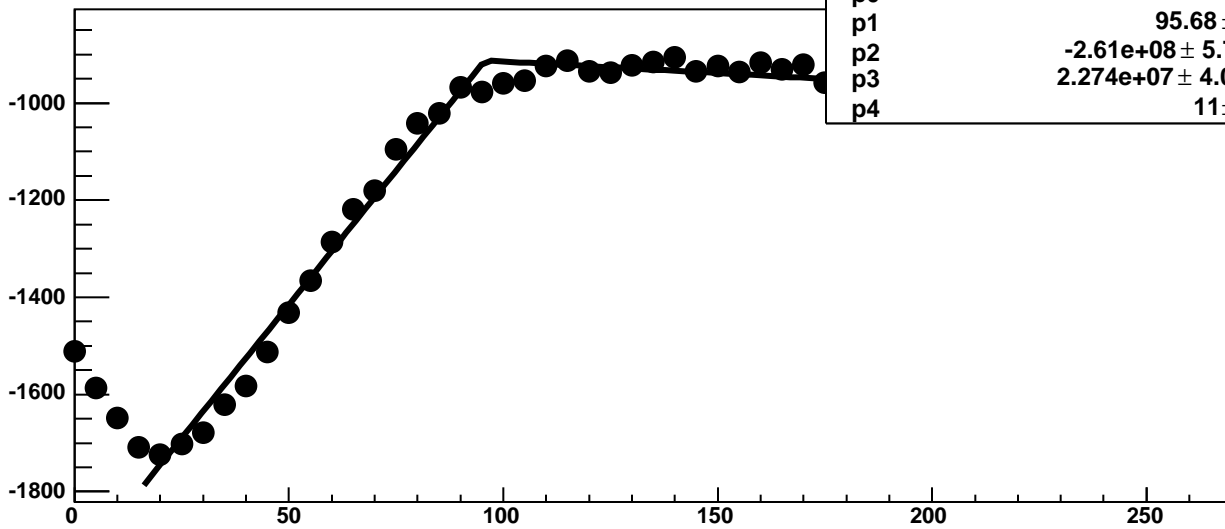
Chip 3, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

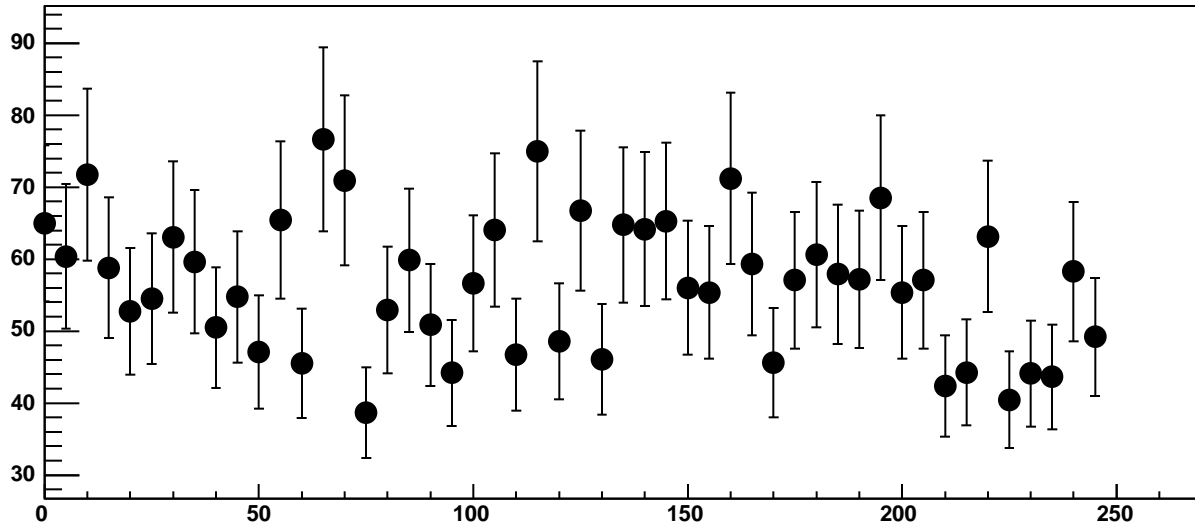


Chip 3, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

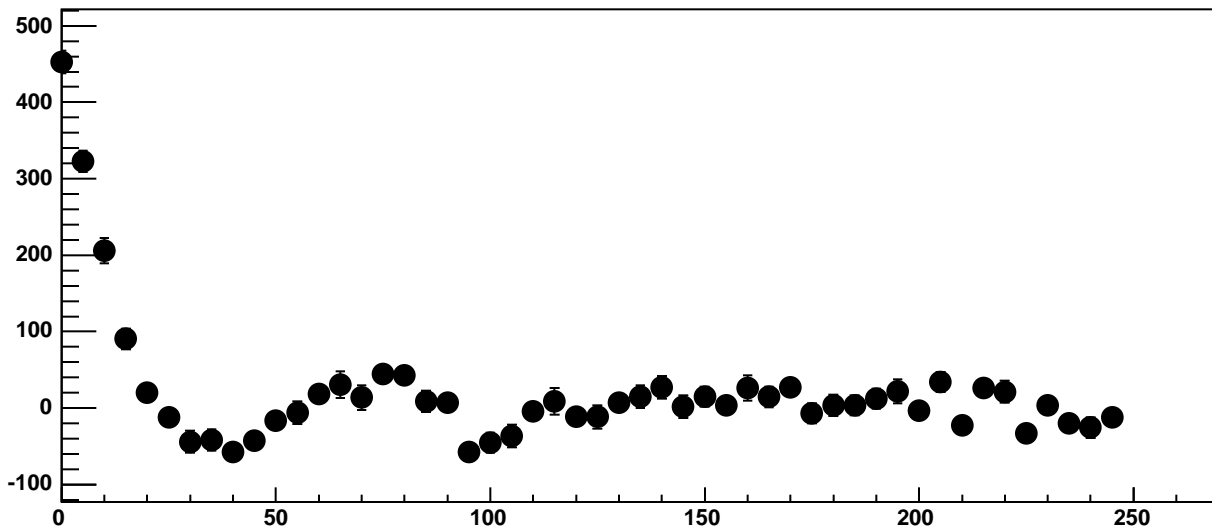


$\chi^2 / \text{ndf}$	266.9 / 41
p0	-912.3 ± 4.695
p1	95.68 ± 0.6382
p2	-2.61e+08 ± 5.779e+06
p3	2.274e+07 ± 4.096e+05
p4	11 ± 0.1196

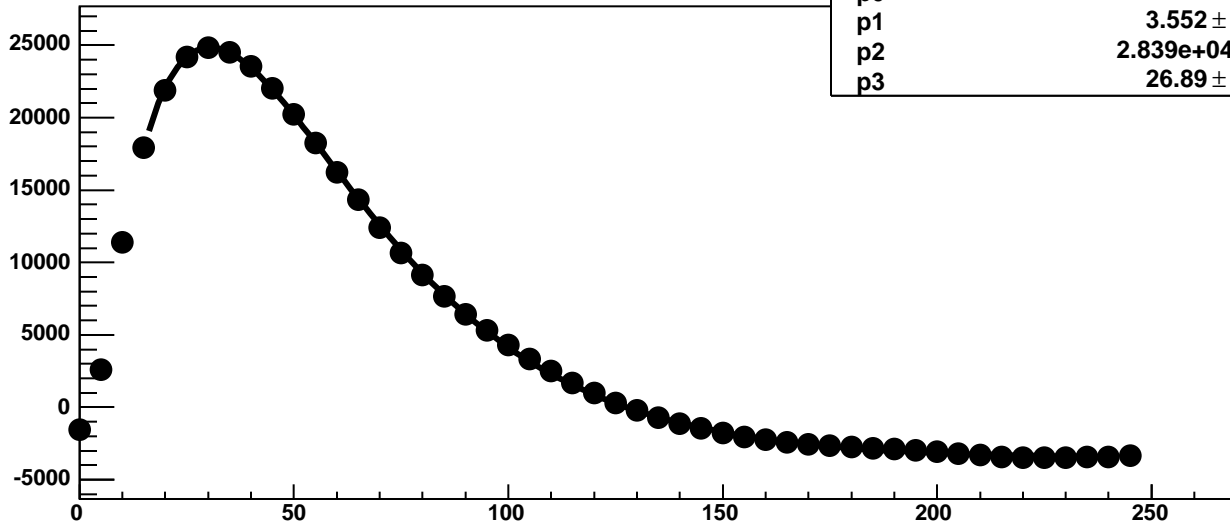
Chip 3, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold

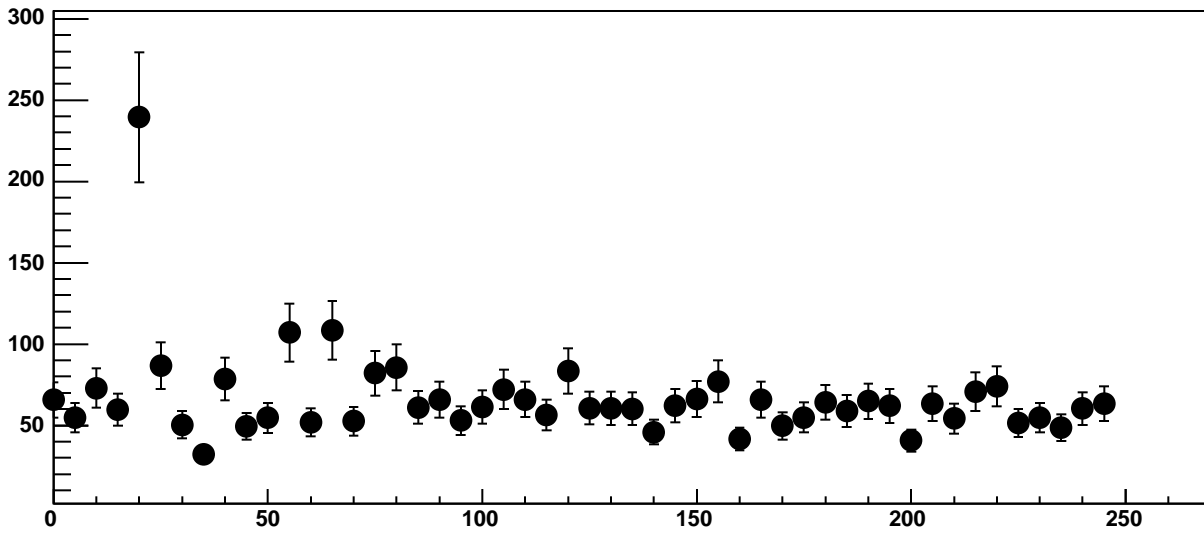


Chip 3, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold

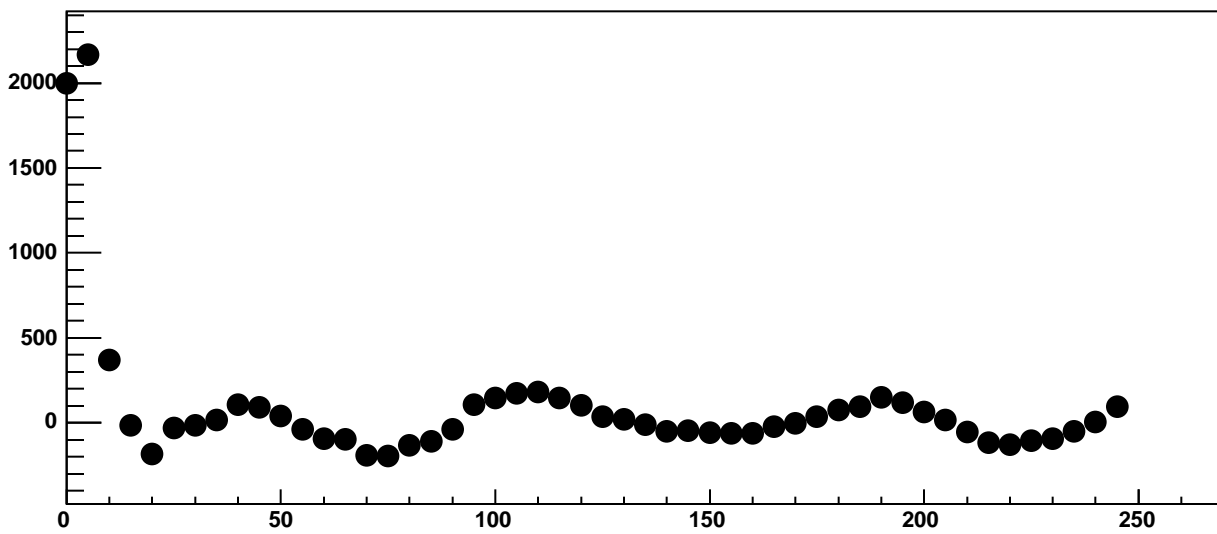


$\chi^2 / \text{ndf}$	1982 / 42
p0	-3524 ± 3.457
p1	3.552 ± 0.01502
p2	2.839e+04 ± 5.628
p3	26.89 ± 0.01046

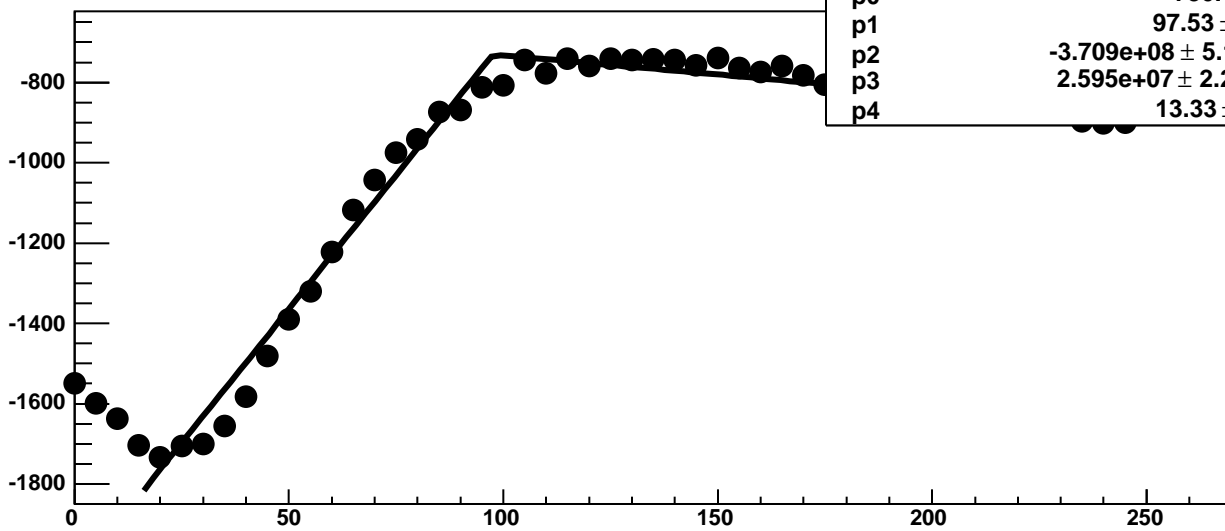
Chip 3, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold

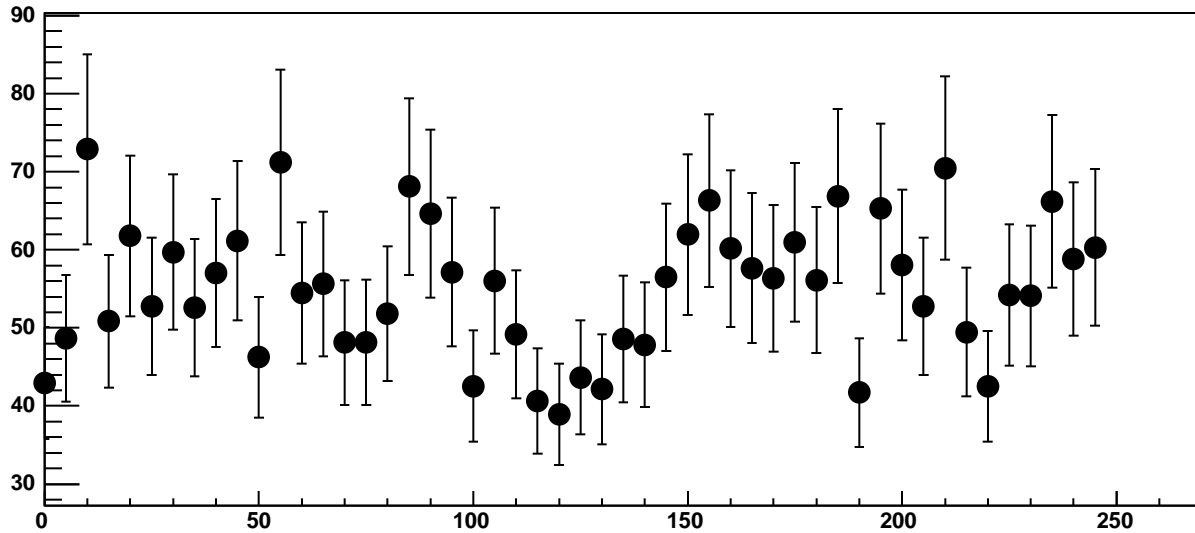


Chip 3, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

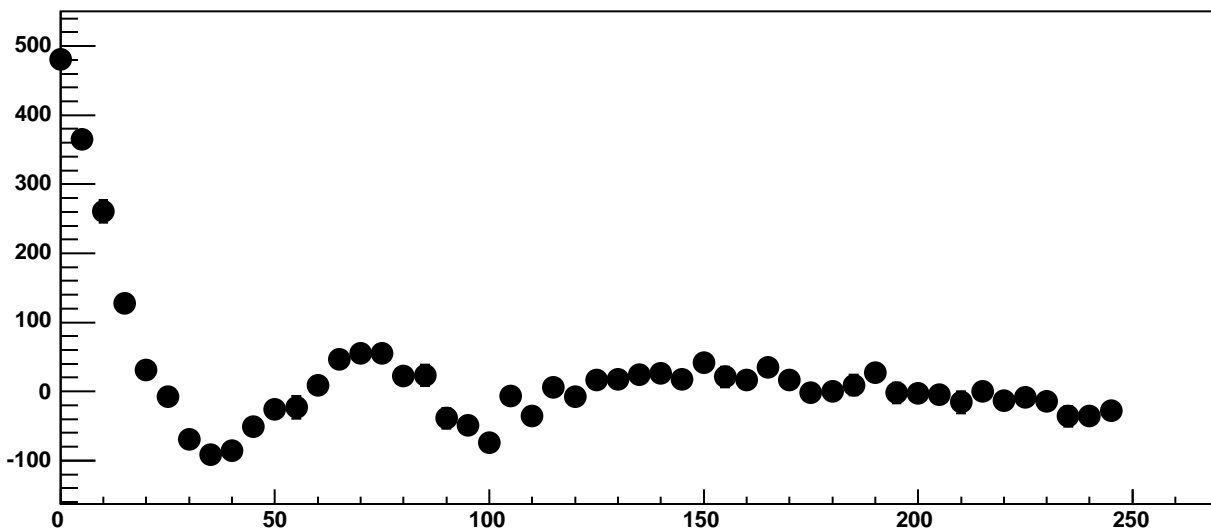


$\chi^2 / \text{ndf}$	494.7 / 41
p0	$-730.1 \pm 3.781$
p1	$97.53 \pm 0.5216$
p2	$-3.709\text{e}+08 \pm 5.137\text{e}+06$
p3	$2.595\text{e}+07 \pm 2.259\text{e}+05$
p4	$13.33 \pm 0.1272$

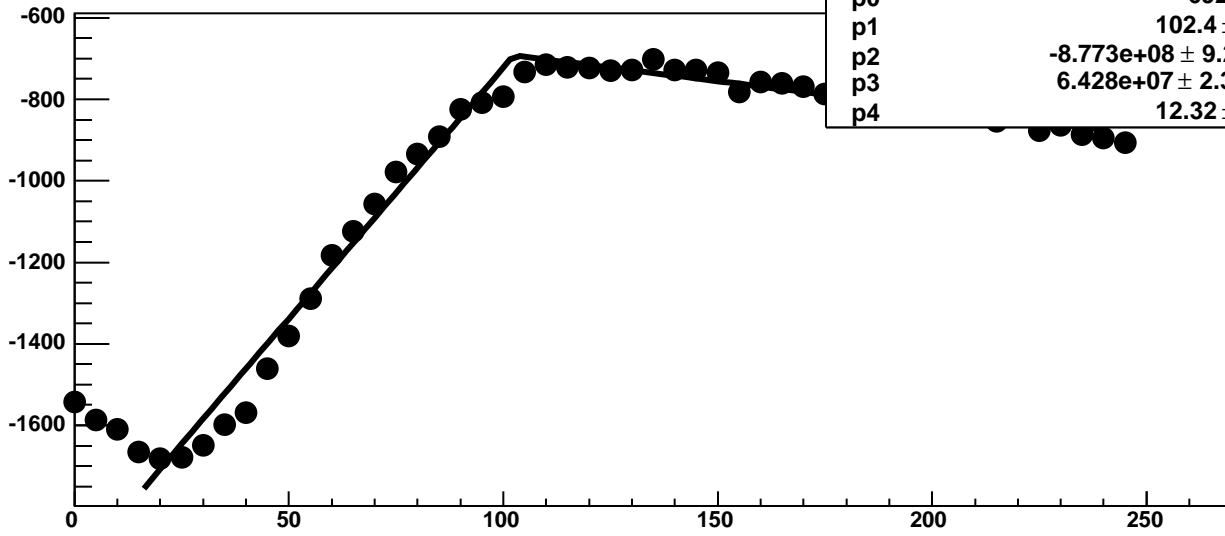
Chip 3, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

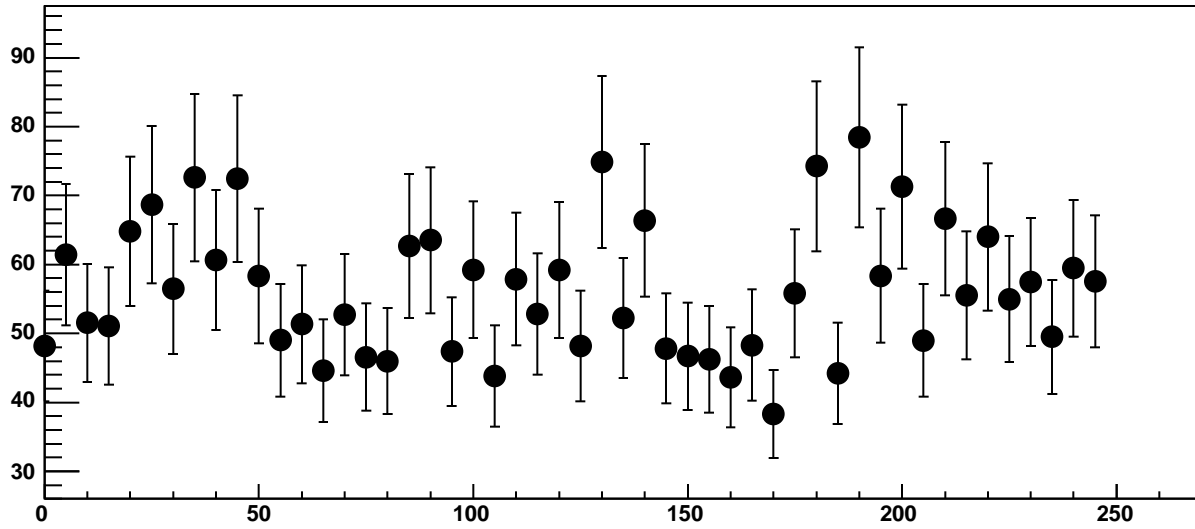


Chip 3, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

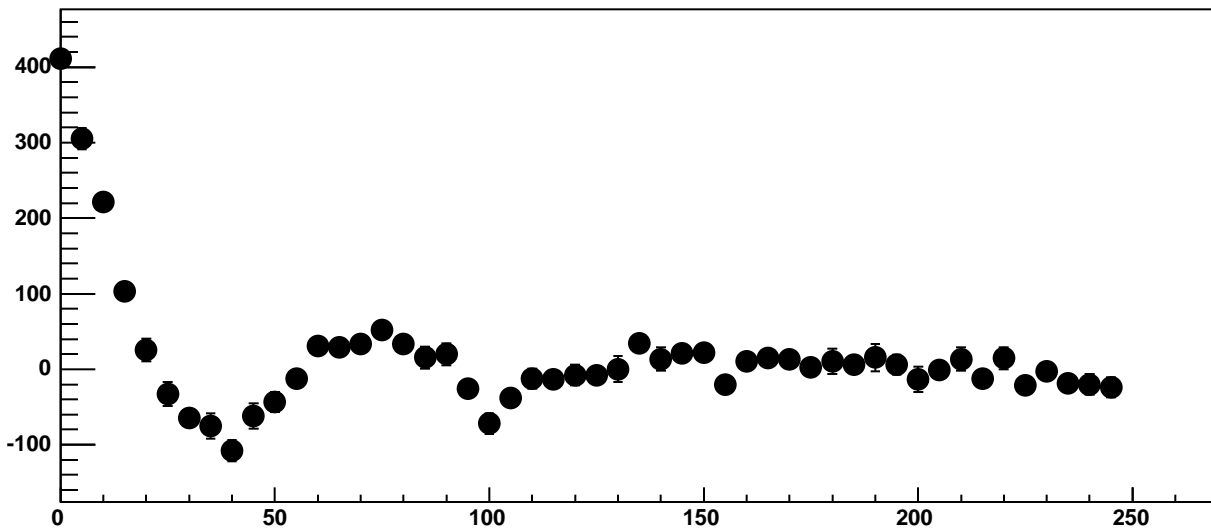


$\chi^2 / \text{ndf}$	364.1 / 41
p0	-692 ± 4.152
p1	102.4 ± 0.5412
p2	-8.773e+08 ± 9.212e+06
p3	6.428e+07 ± 2.324e+05
p4	12.32 ± 0.1189

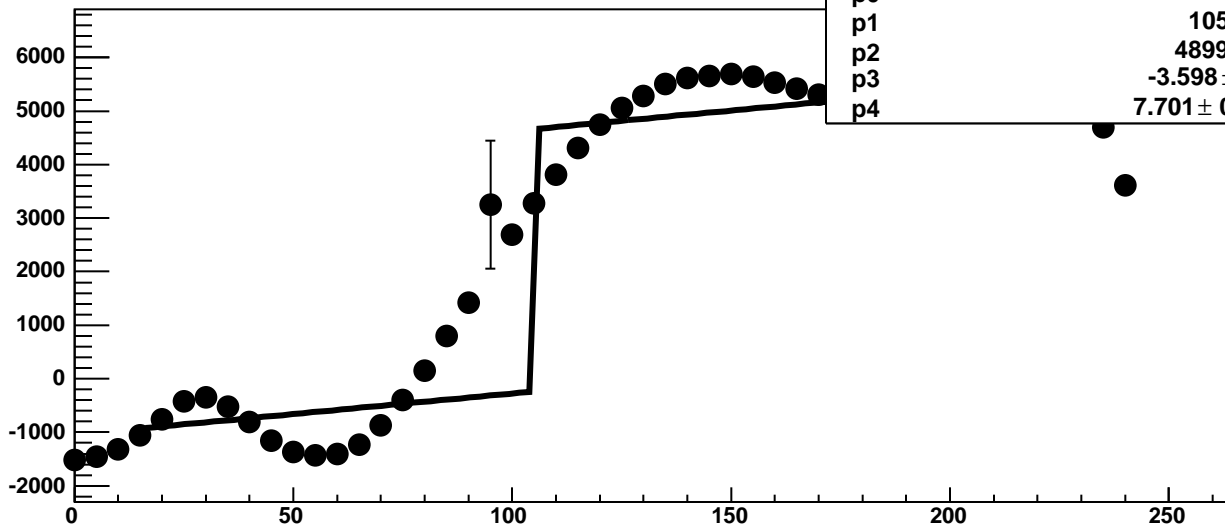
Chip 3, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

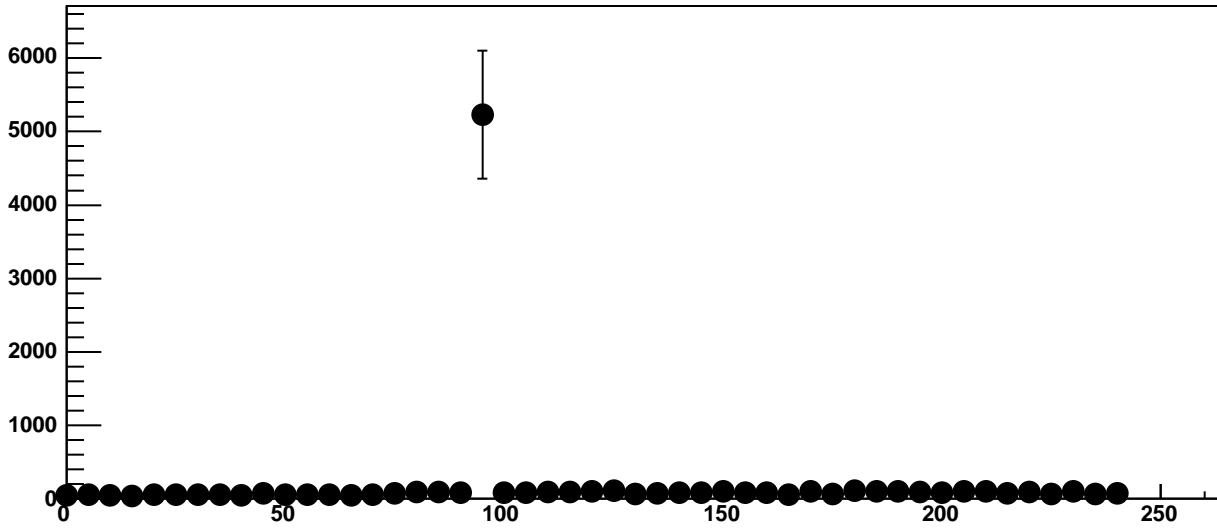


Chip 3, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold

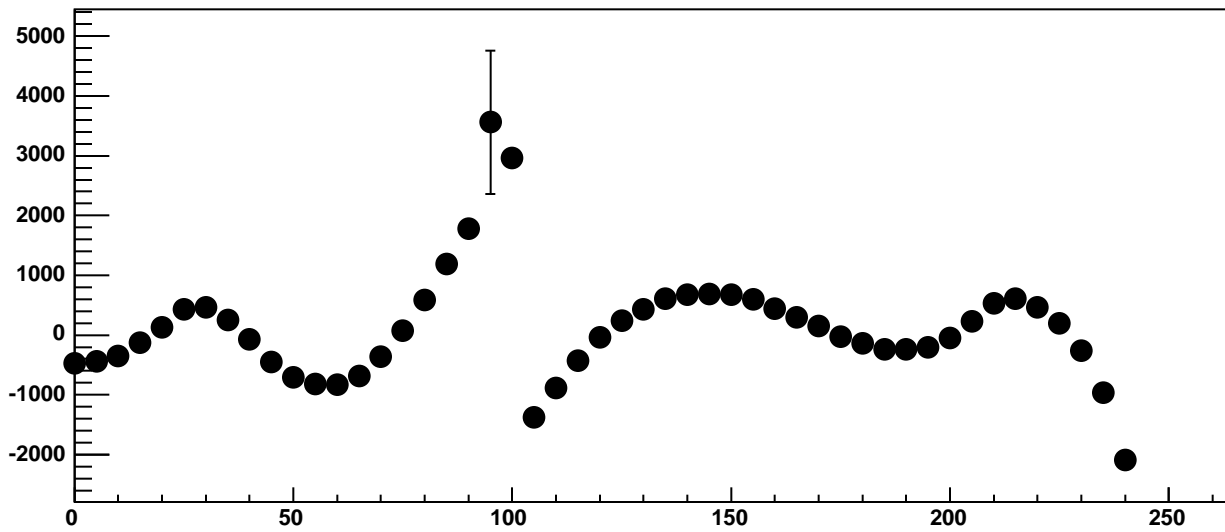


$\chi^2 / \text{ndf}$	8.968e+04 / 41
p0	-236.8 ± 0.5336
p1	105 ± 1.369
p2	4899 ± 0.754
p3	-3.598 ± 0.3148
p4	7.701 ± 0.006811

Chip 3, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold

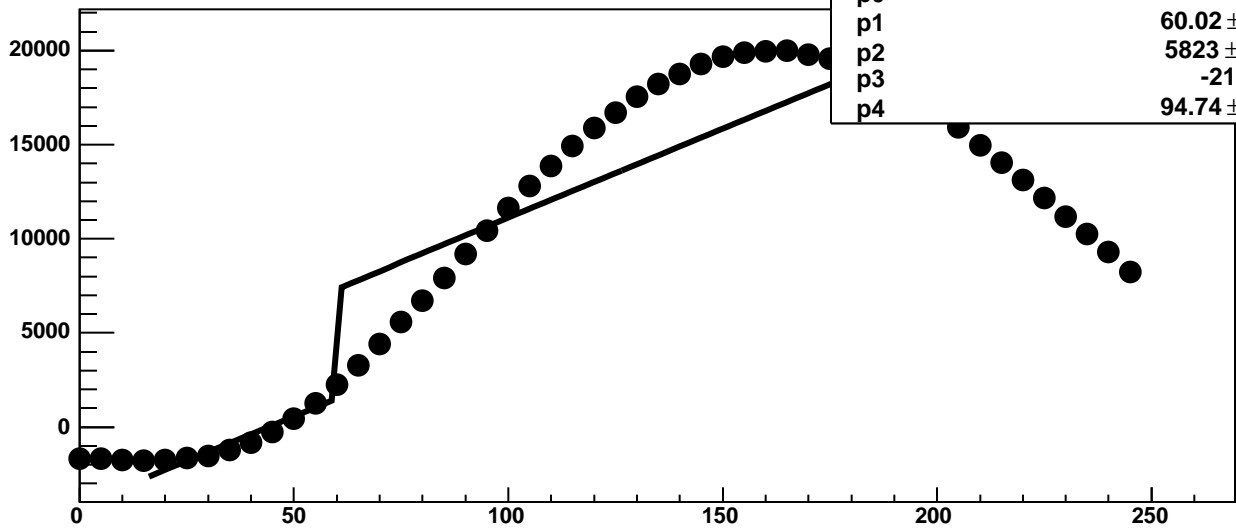


Chip 3, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold

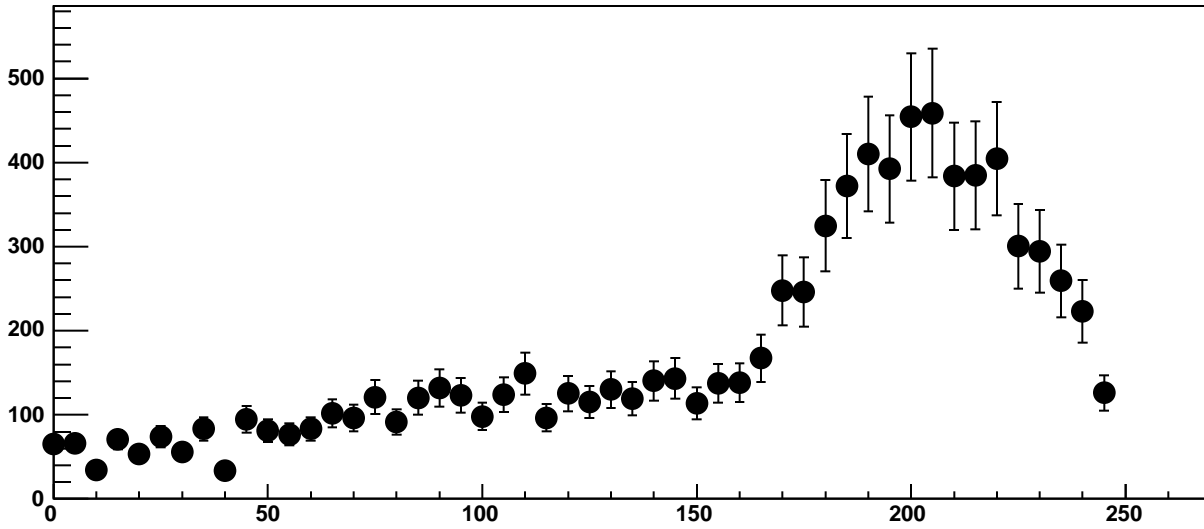




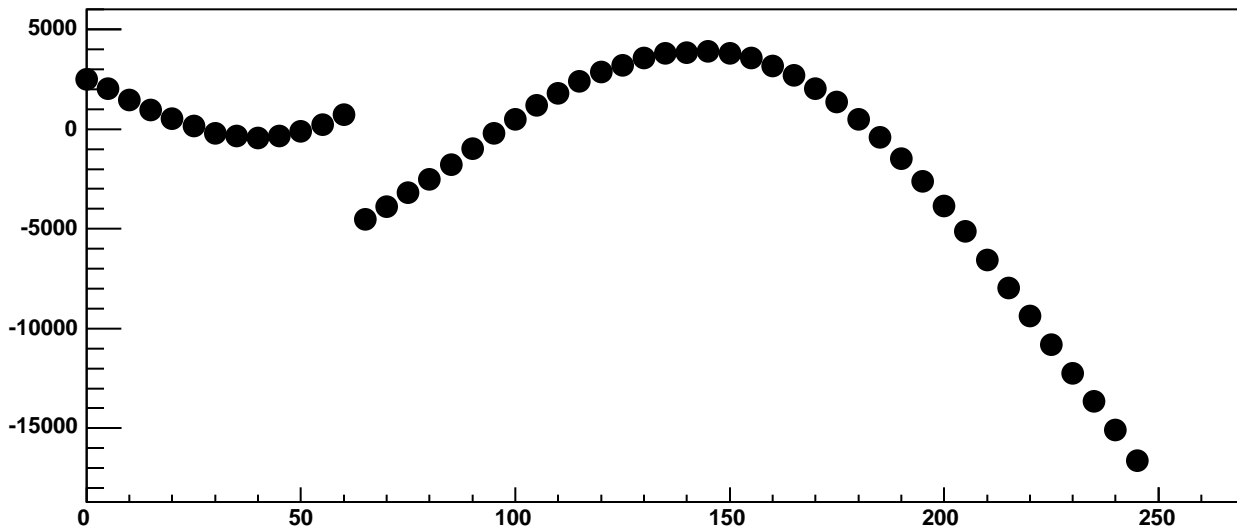
Chip 3, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold



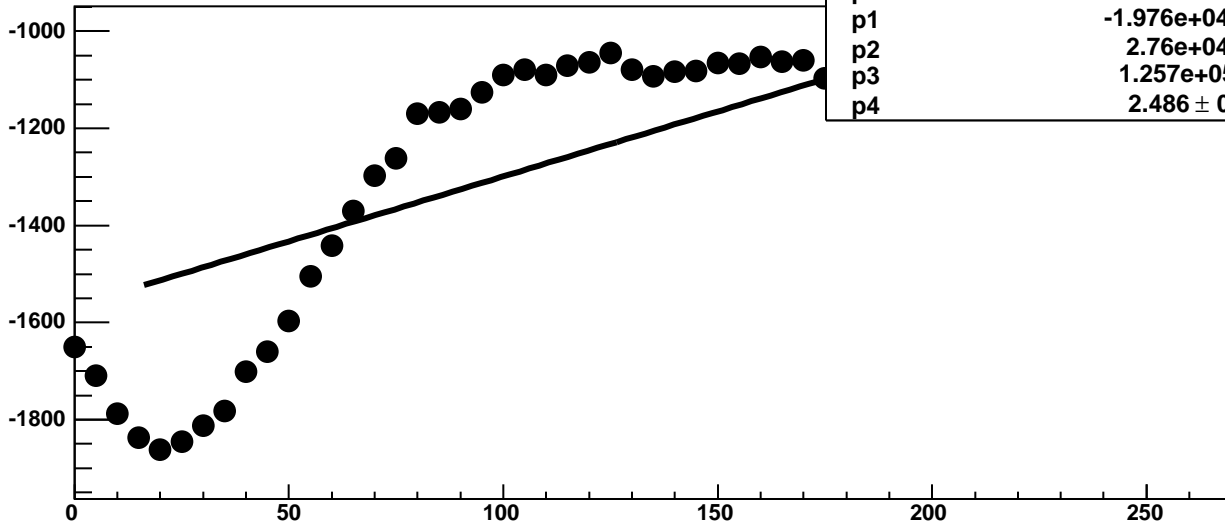
Chip 3, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

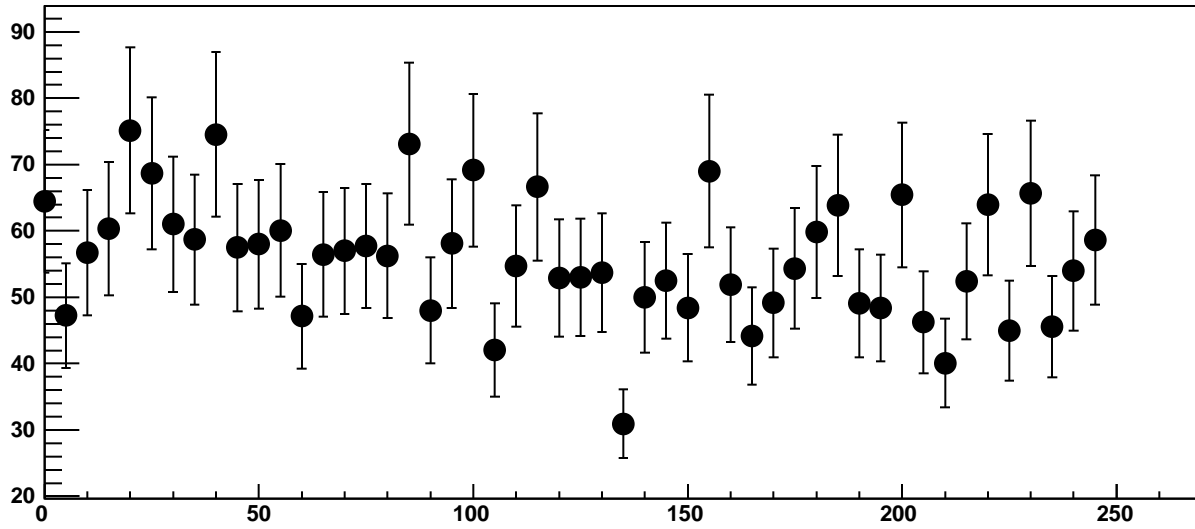


Chip 3, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

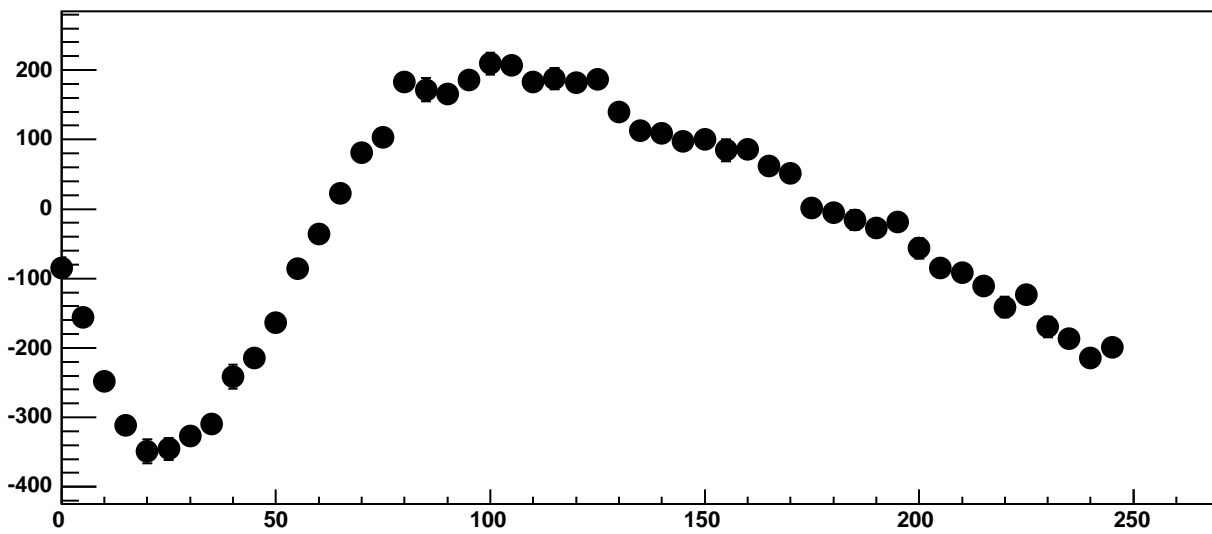


$\chi^2 / \text{ndf}$	7433 / 41
p0	-5.471e+04 ± 22.77
p1	-1.976e+04 ± 8.516
p2	2.76e+04 ± 155.6
p3	1.257e+05 ± 766
p4	2.486 ± 0.001145

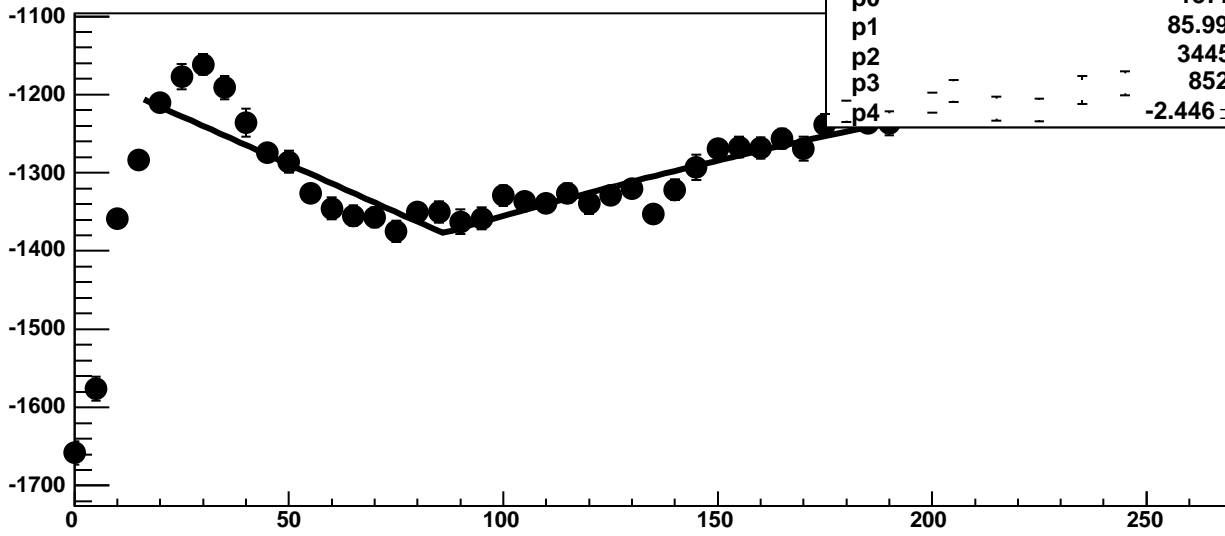
Chip 3, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

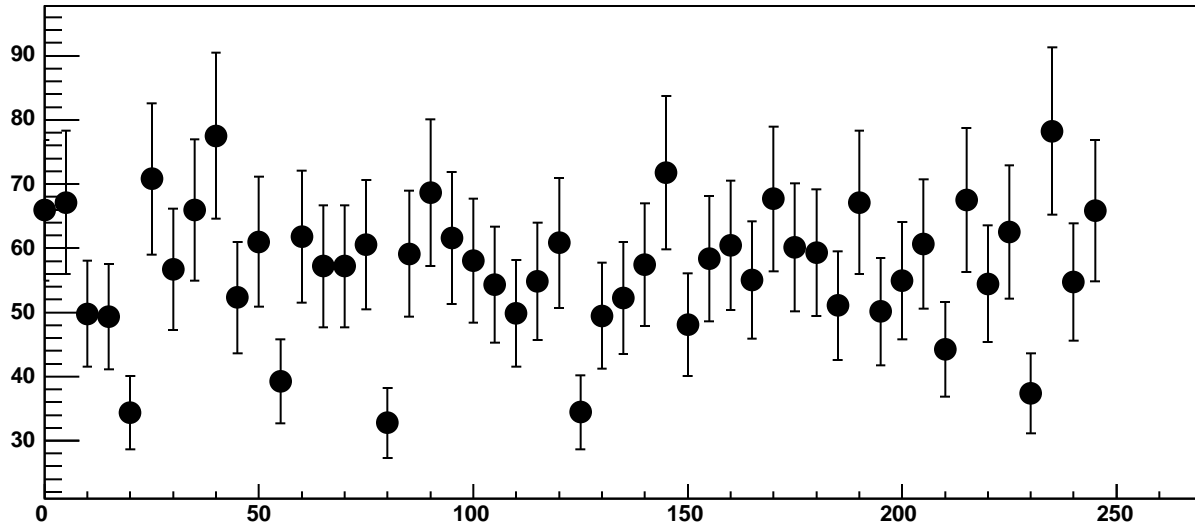


Chip 3, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold

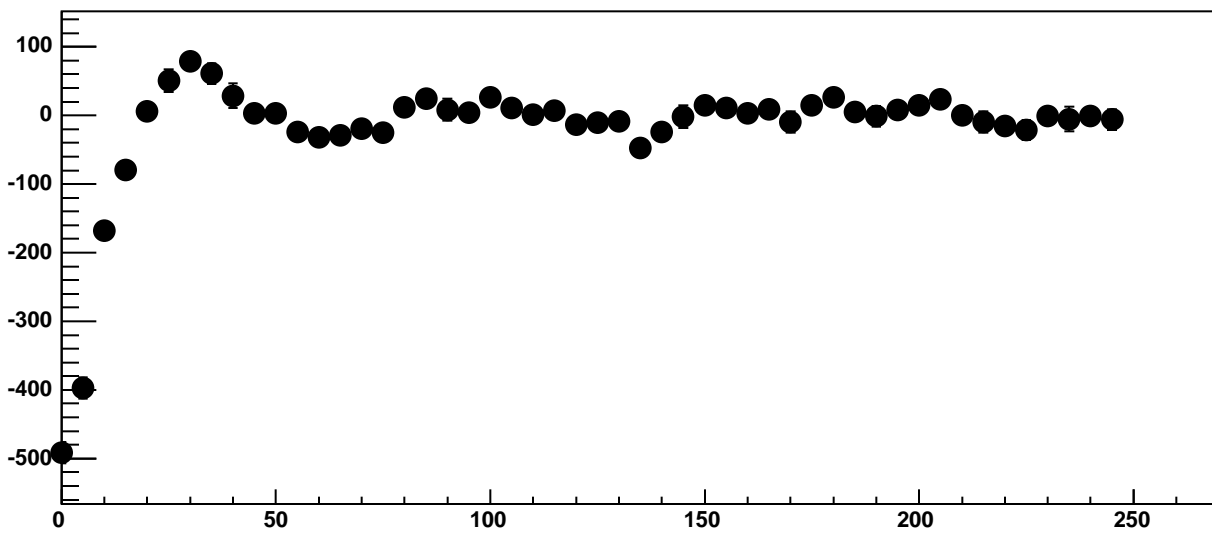


$\chi^2 / \text{ndf}$	189.8 / 41
p0	$-1377 \pm 4.561$
p1	$85.99 \pm 2.082$
p2	$3445 \pm 1461$
p3	$852 \pm 394.2$
p4	$-2.446 \pm 0.1284$

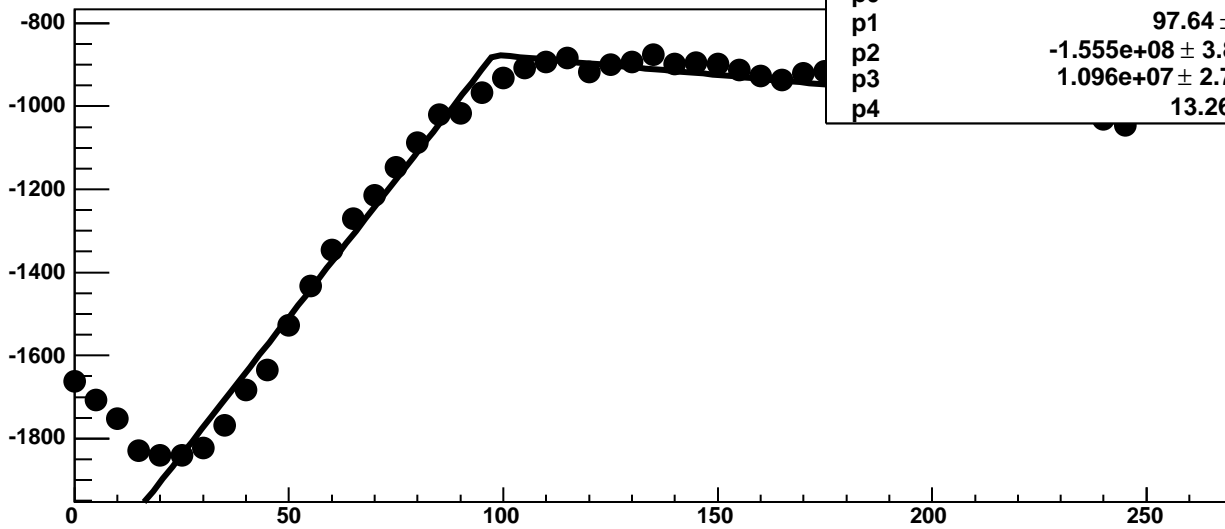
Chip 3, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

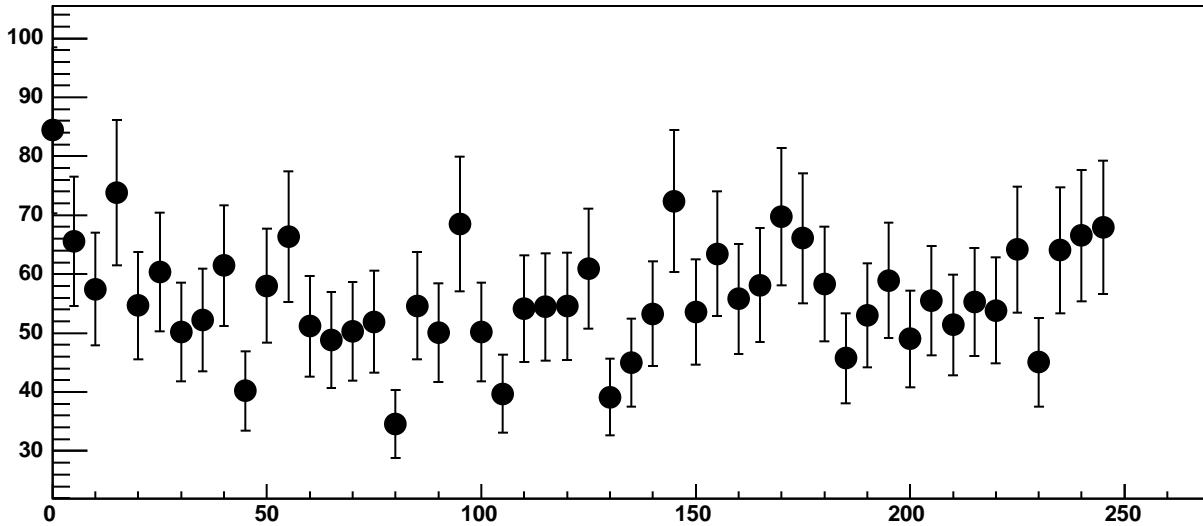


Chip 3, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

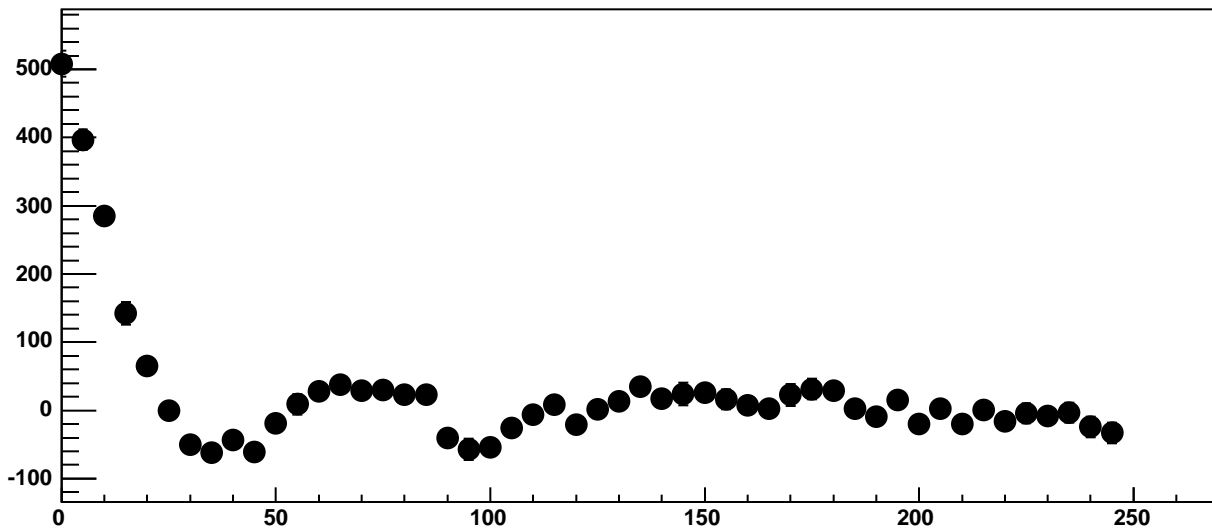


$\chi^2 / \text{ndf}$	347.9 / 41
p0	-875.9 ± 3.989
p1	97.64 ± 0.4914
p2	-1.555e+08 ± 3.879e+06
p3	1.096e+07 ± 2.735e+05
p4	13.26 ± 0.118

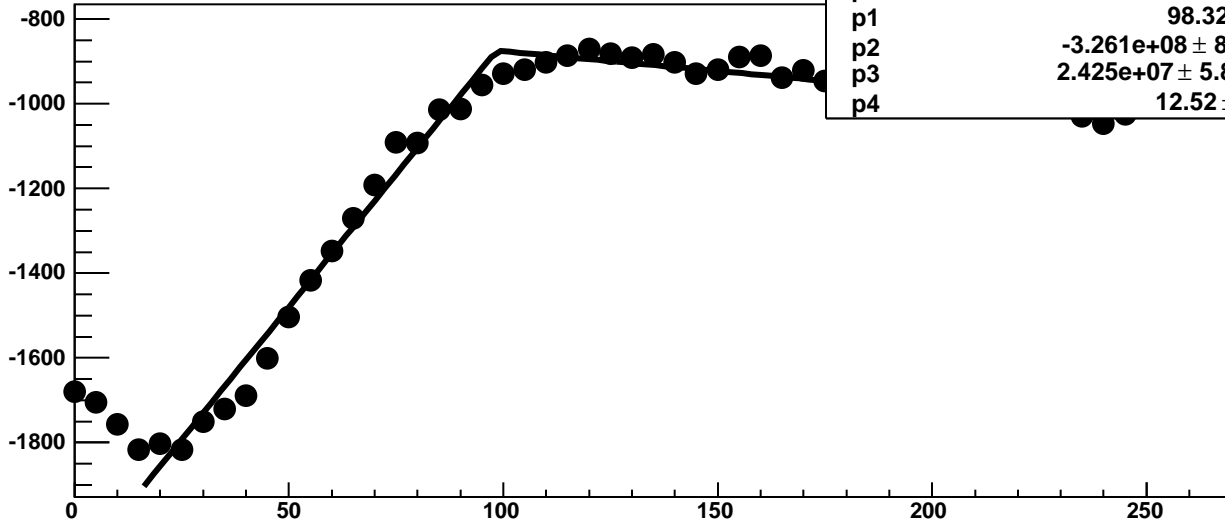
Chip 3, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold

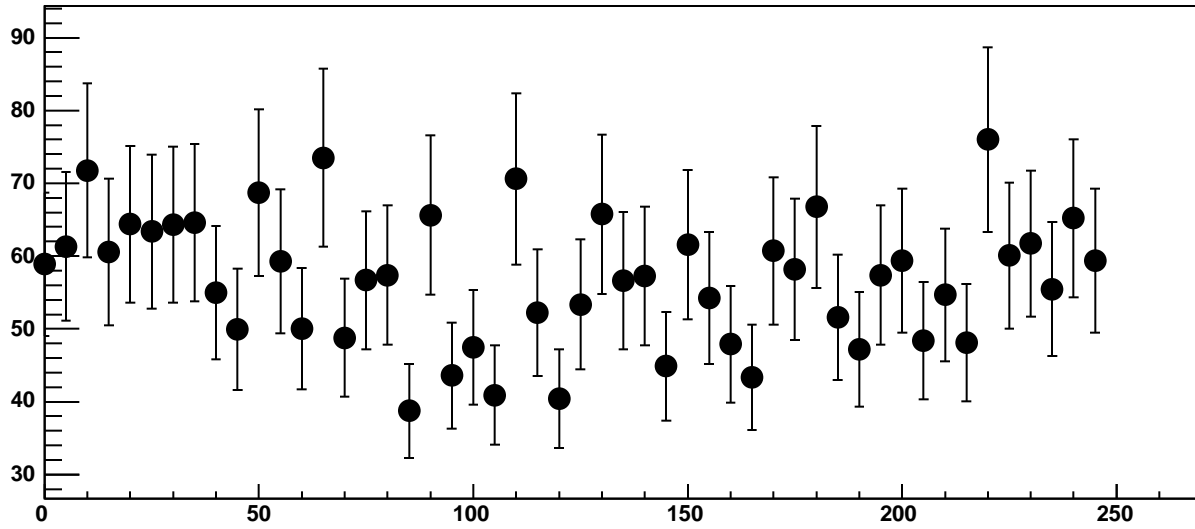


Chip 3, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

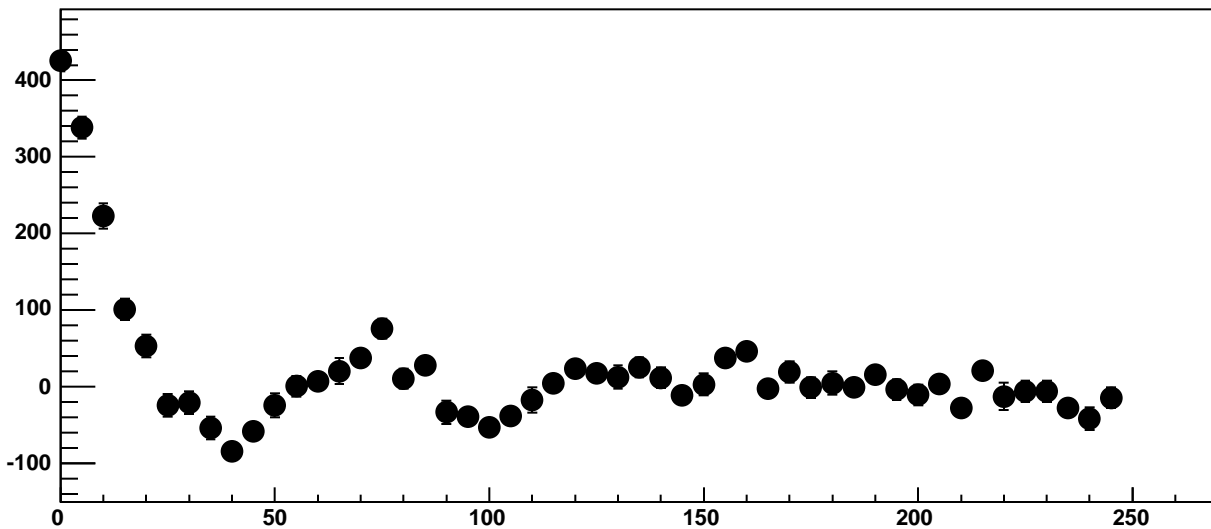


$\chi^2 / \text{ndf}$	344.2 / 41
p0	-874.7 ± 4.047
p1	98.32 ± 0.533
p2	-3.261e+08 ± 8.74e+06
p3	2.425e+07 ± 5.859e+05
p4	12.52 ± 0.1247

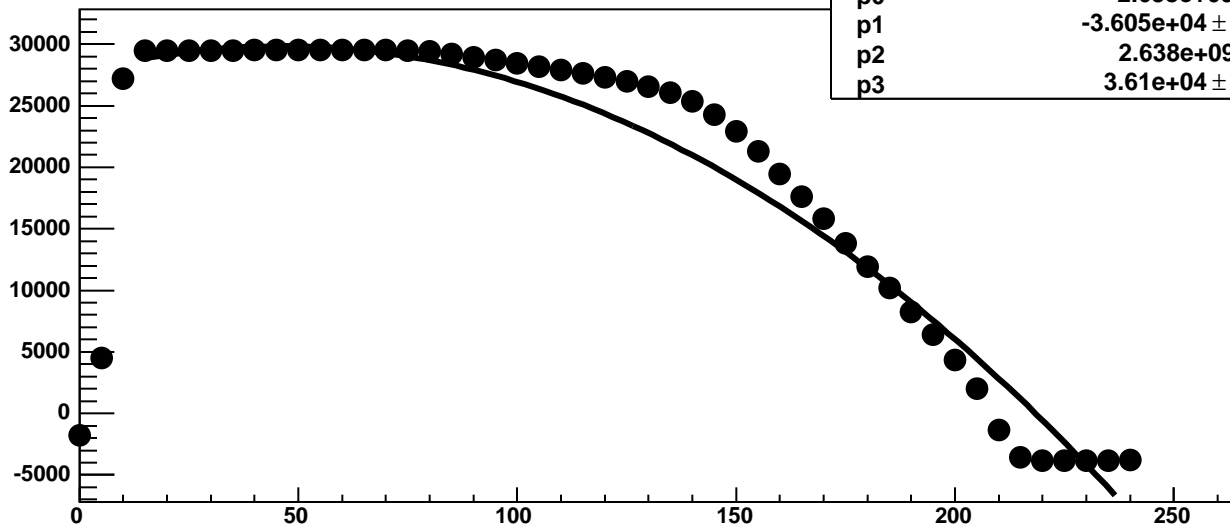
Chip 3, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

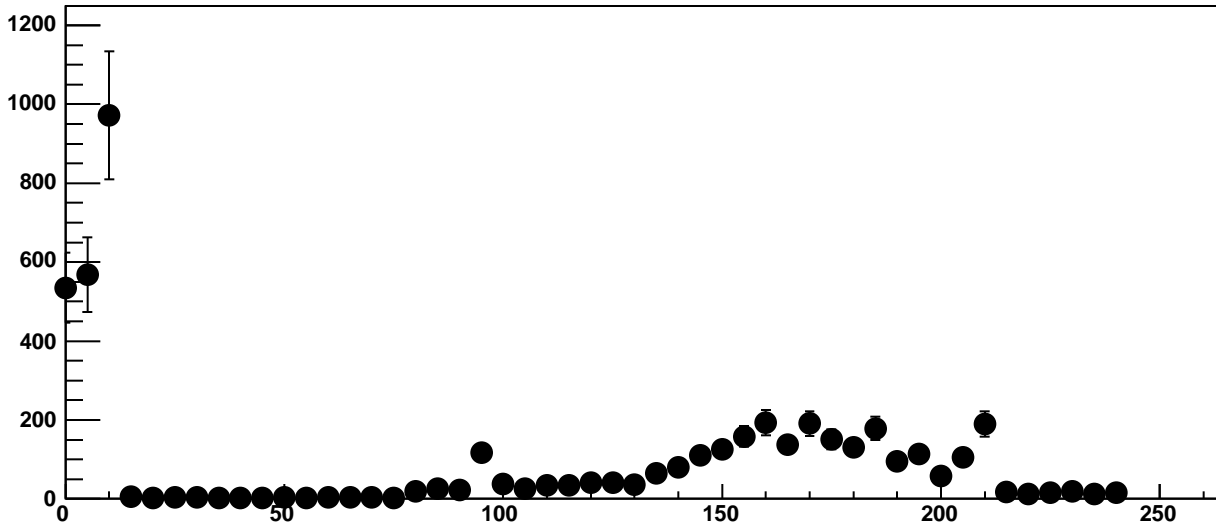


Chip 3, Channel 17, Enable 5!, DAC=1600, ADC Mean vs Hold

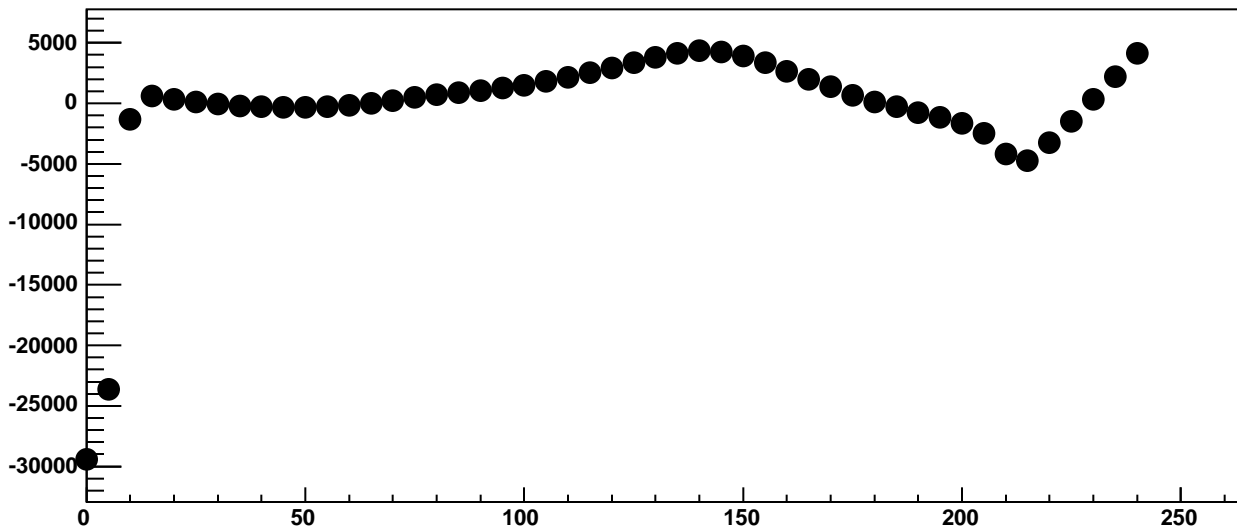


$\chi^2 / \text{ndf}$	7.765e+06 / 42
p0	-2.638e+09 $\pm$ 3.224
p1	-3.605e+04 $\pm$ 0.04418
p2	2.638e+09 $\pm$ 3.224
p3	3.61e+04 $\pm$ 0.04403

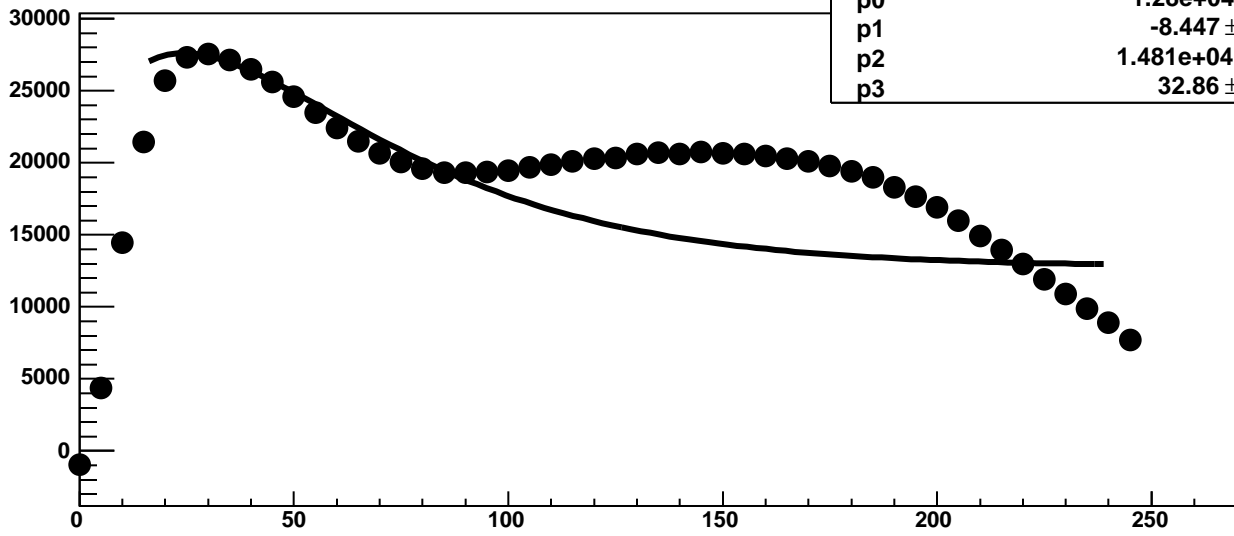
Chip 3, Channel 17, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 3, Channel 17, Enable 5!, DAC=1600, ADC Residuals vs Hold

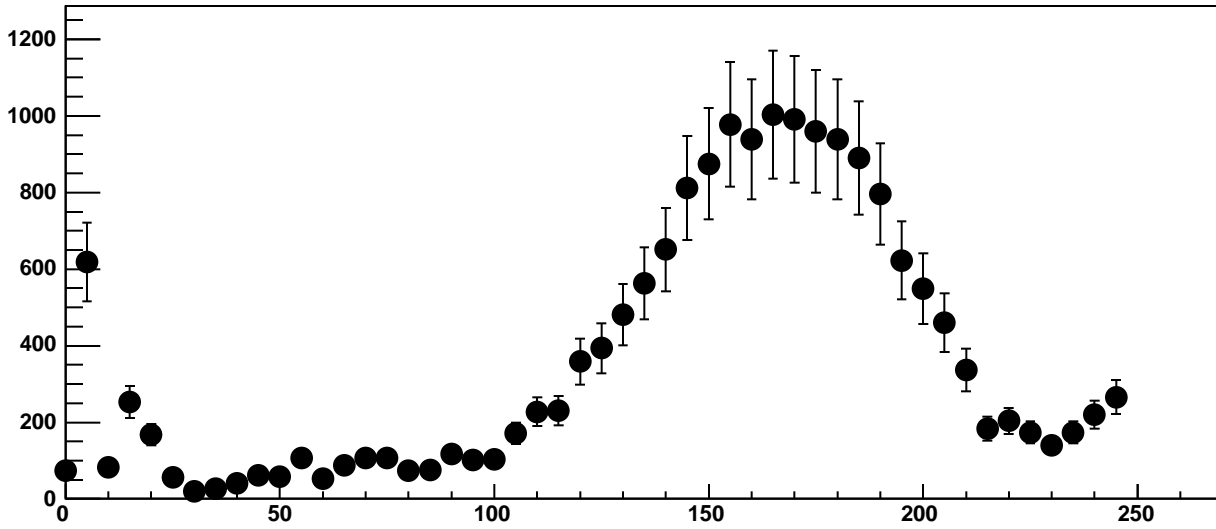


Chip 4, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold

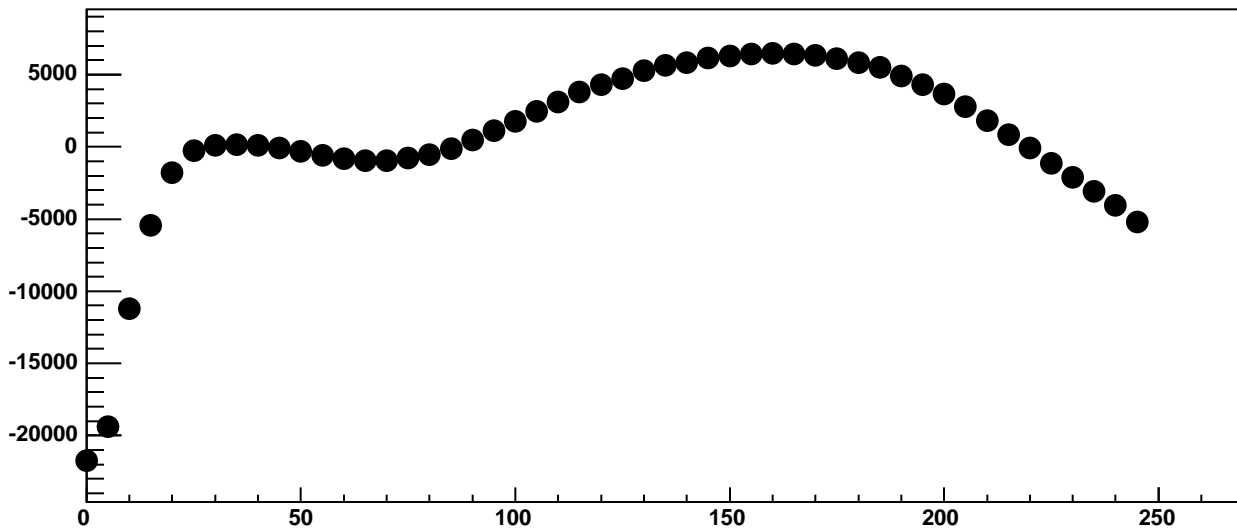


$\chi^2 / \text{ndf}$	8.525e+04 / 42
p0	1.28e+04 $\pm$ 20.88
p1	-8.447 $\pm$ 0.2174
p2	1.481e+04 $\pm$ 25.33
p3	32.86 $\pm$ 0.1084

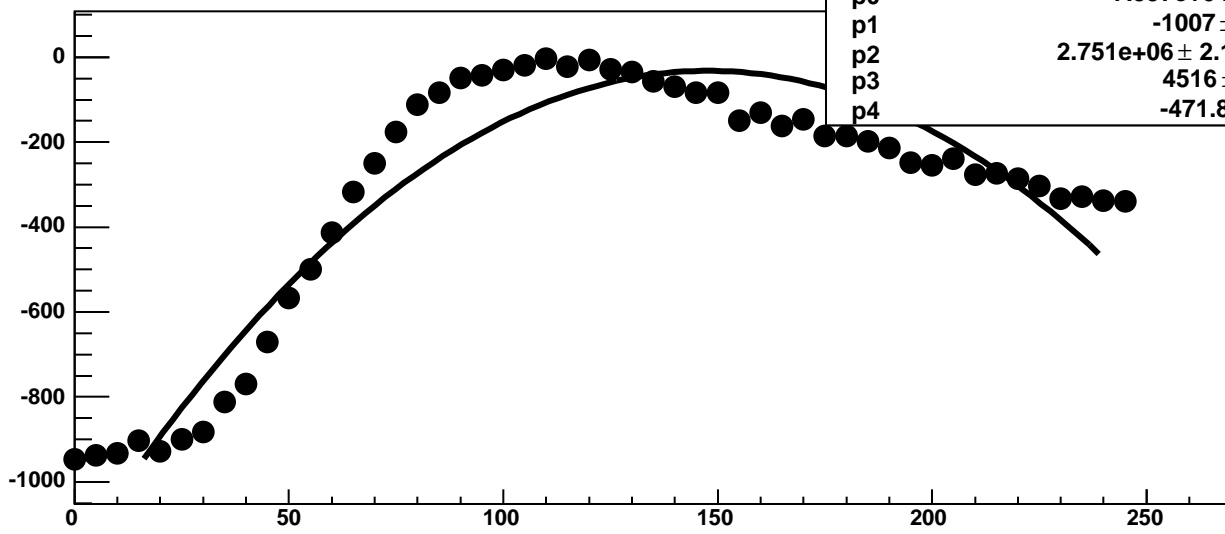
Chip 4, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



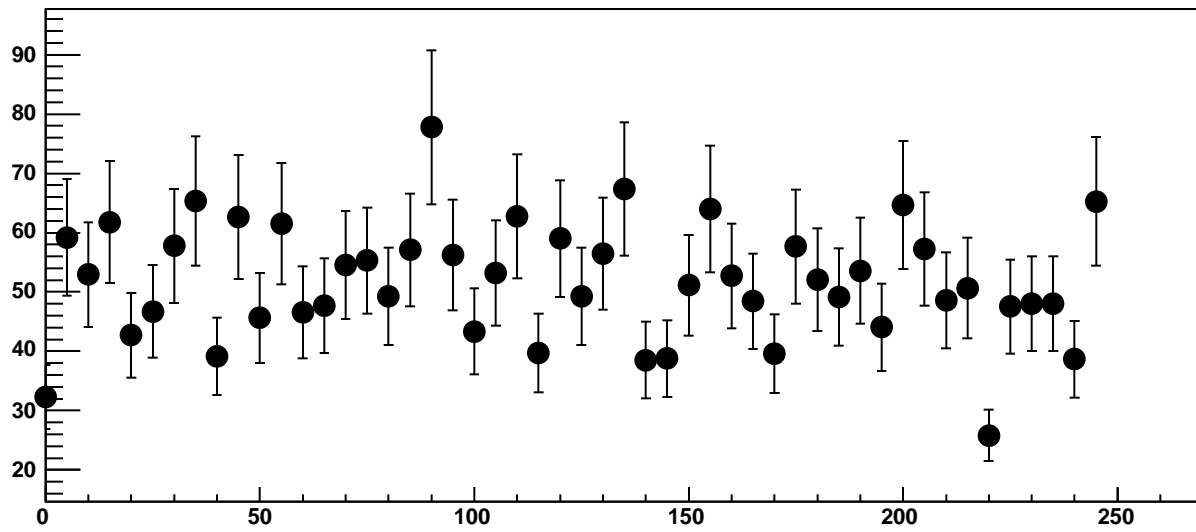
Chip 4, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold



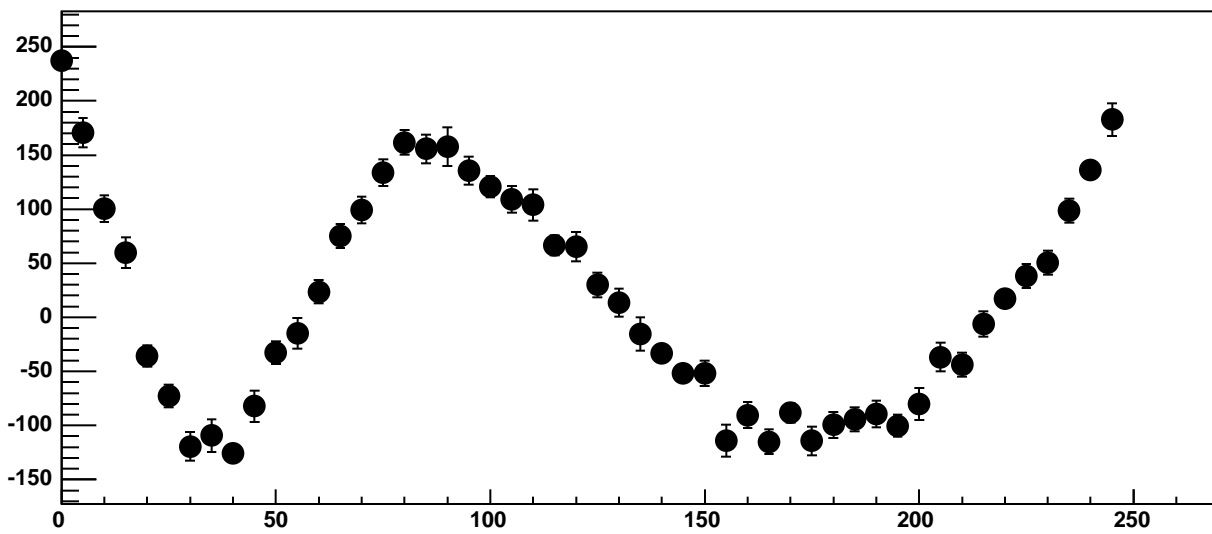
Chip 4, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 4, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

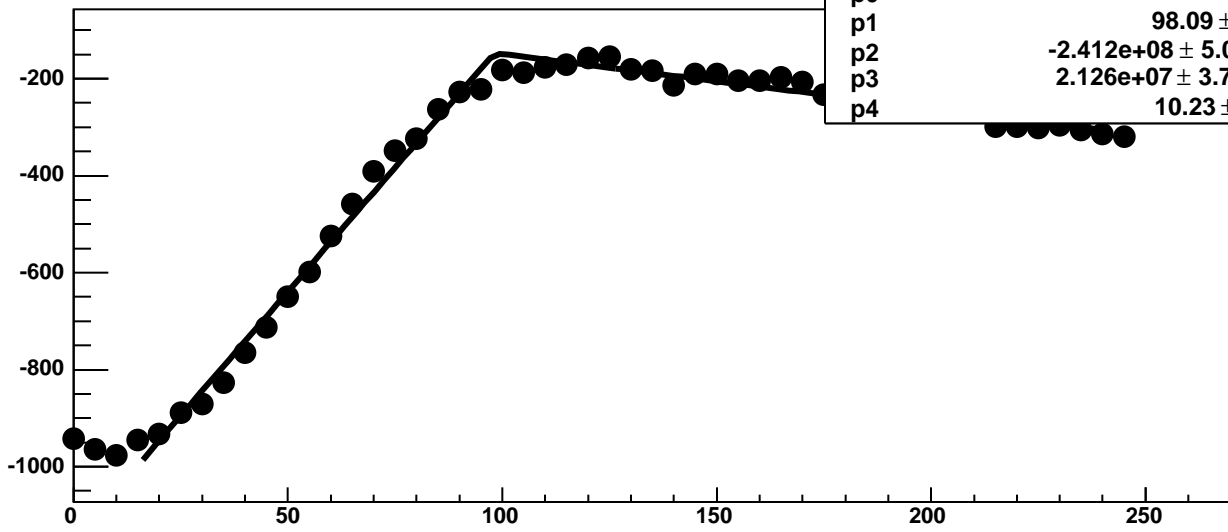


Chip 4, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



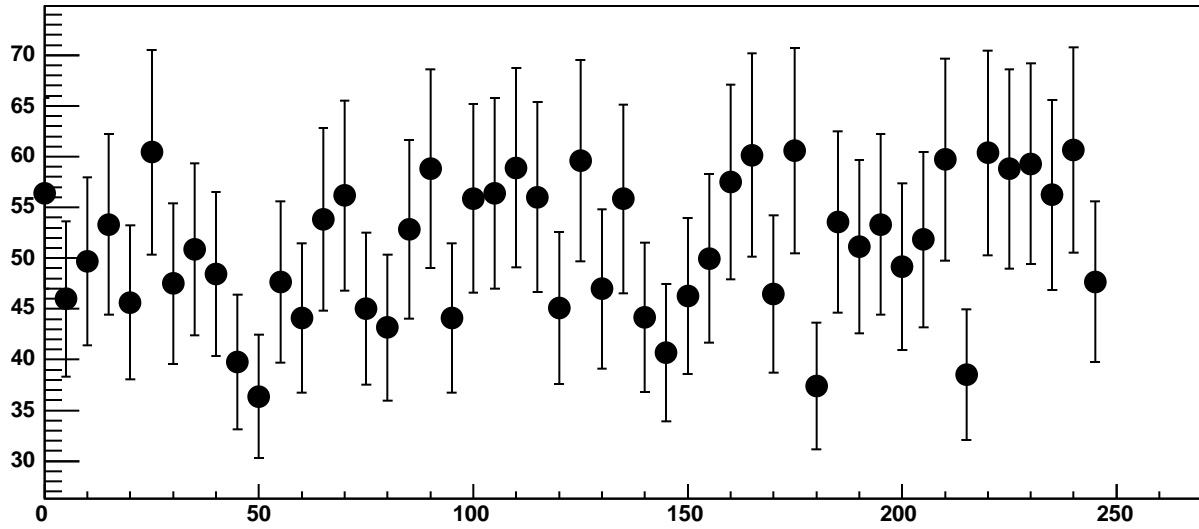


Chip 4, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

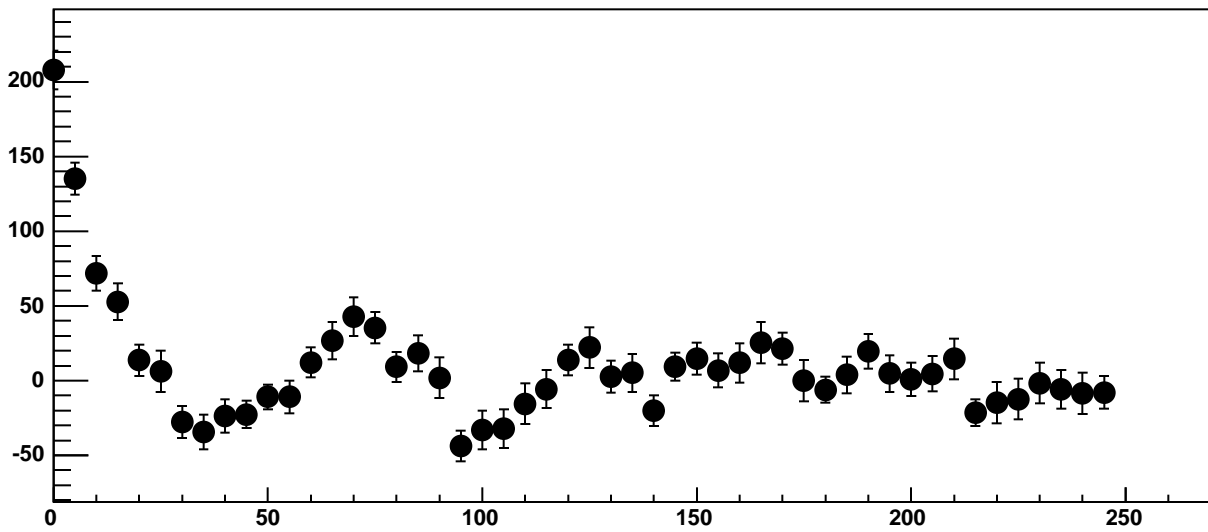


$\chi^2 / \text{ndf}$	147.4 / 41
p0	$-147.2 \pm 4.077$
p1	$98.09 \pm 0.6264$
p2	$-2.412\text{e}+08 \pm 5.018\text{e}+06$
p3	$2.126\text{e}+07 \pm 3.707\text{e}+05$
p4	$10.23 \pm 0.1126$

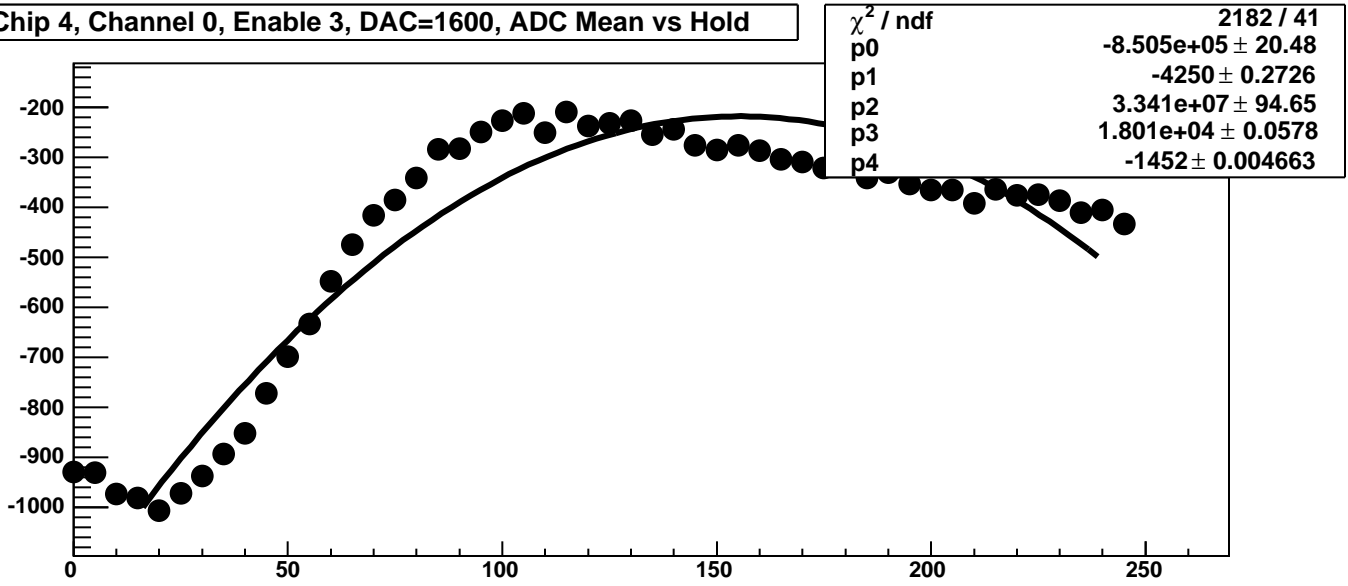
Chip 4, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



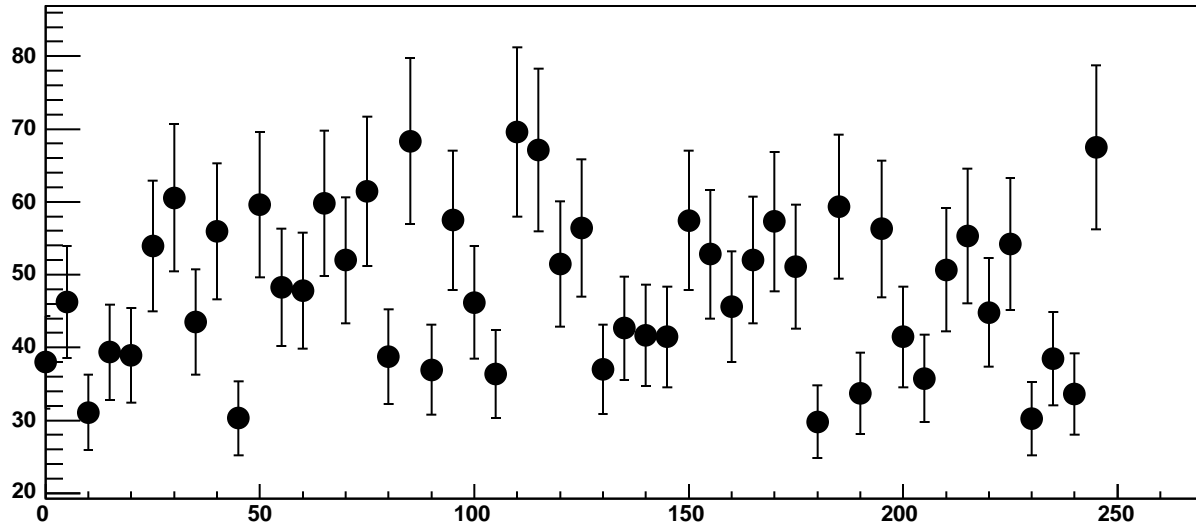
Chip 4, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



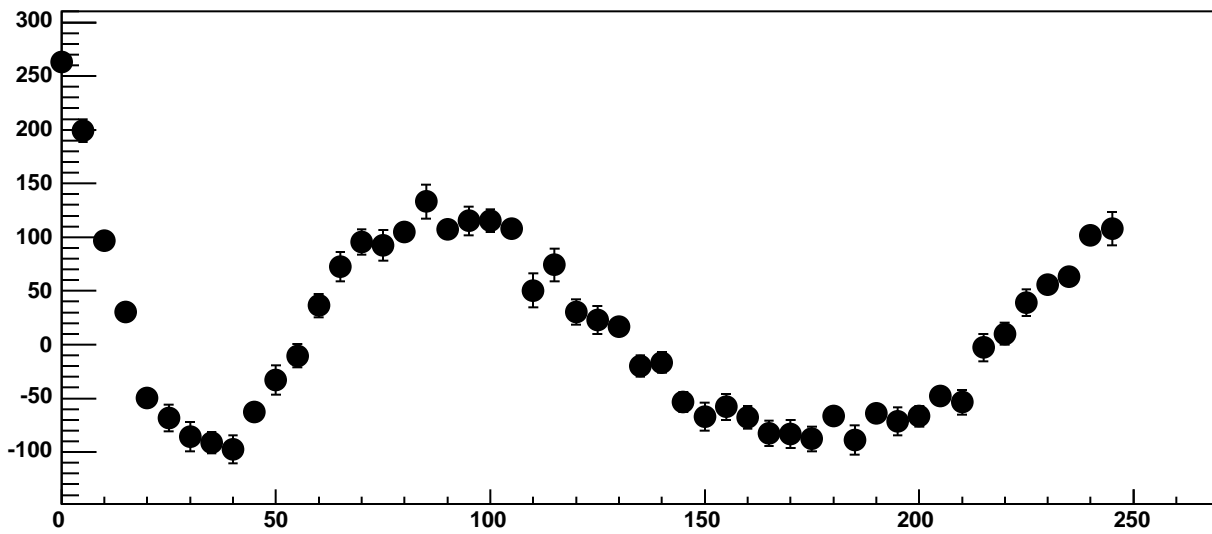
Chip 4, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold



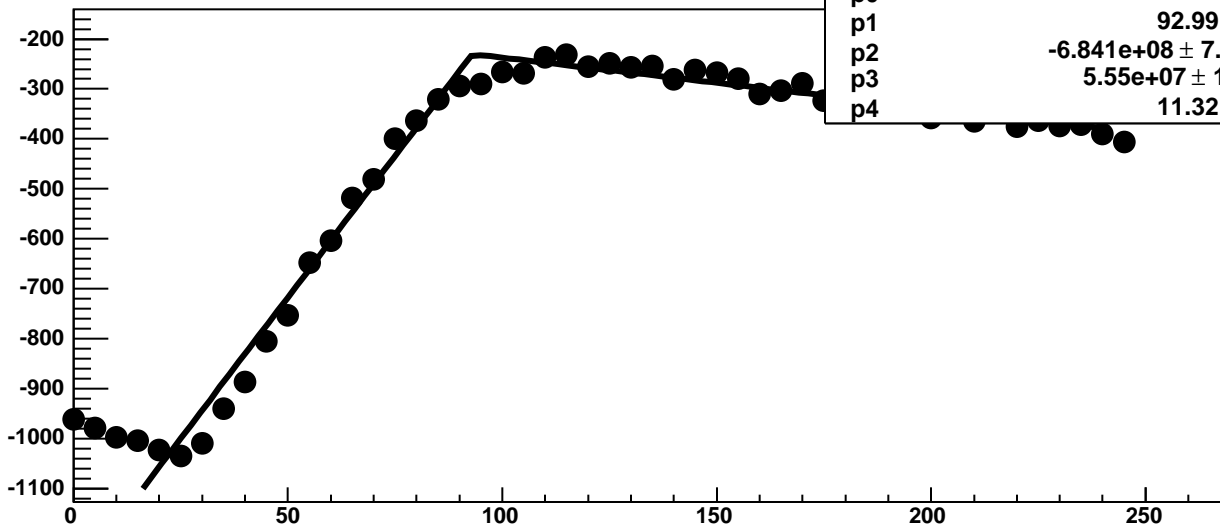
Chip 4, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold

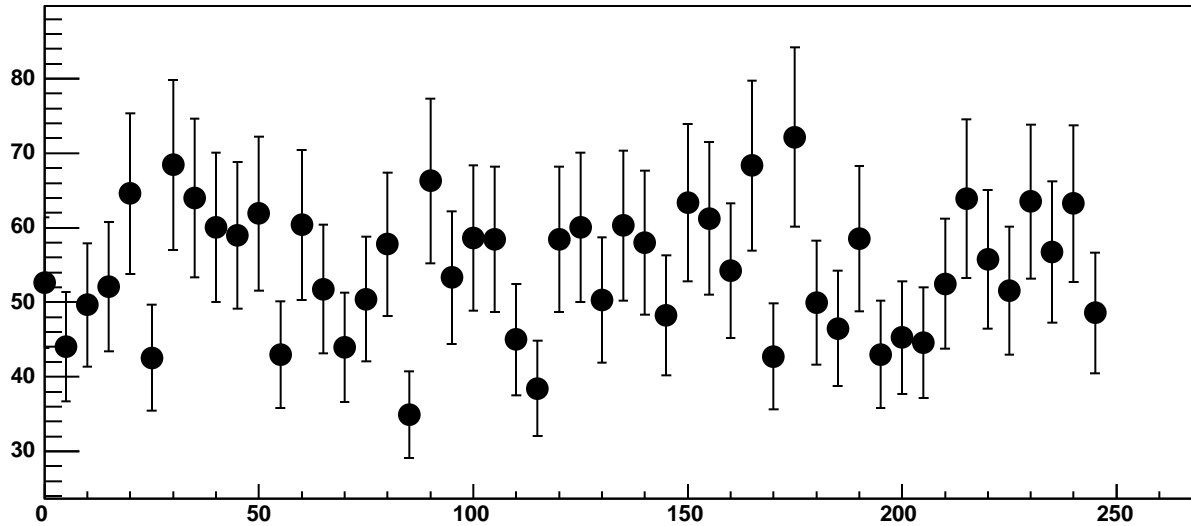


Chip 4, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

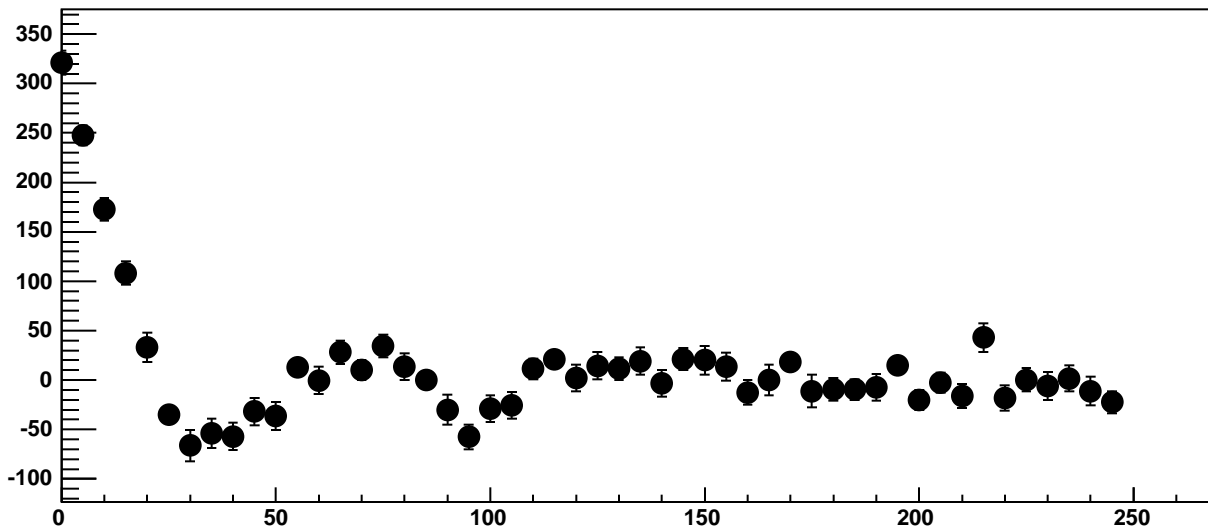


$\chi^2 / \text{ndf}$	256.2 / 41
p0	$-230.2 \pm 4.077$
p1	$92.99 \pm 0.5821$
p2	$-6.841\text{e}+08 \pm 7.938\text{e}+06$
p3	$5.55\text{e}+07 \pm 1.91\text{e}+05$
p4	$11.32 \pm 0.1277$

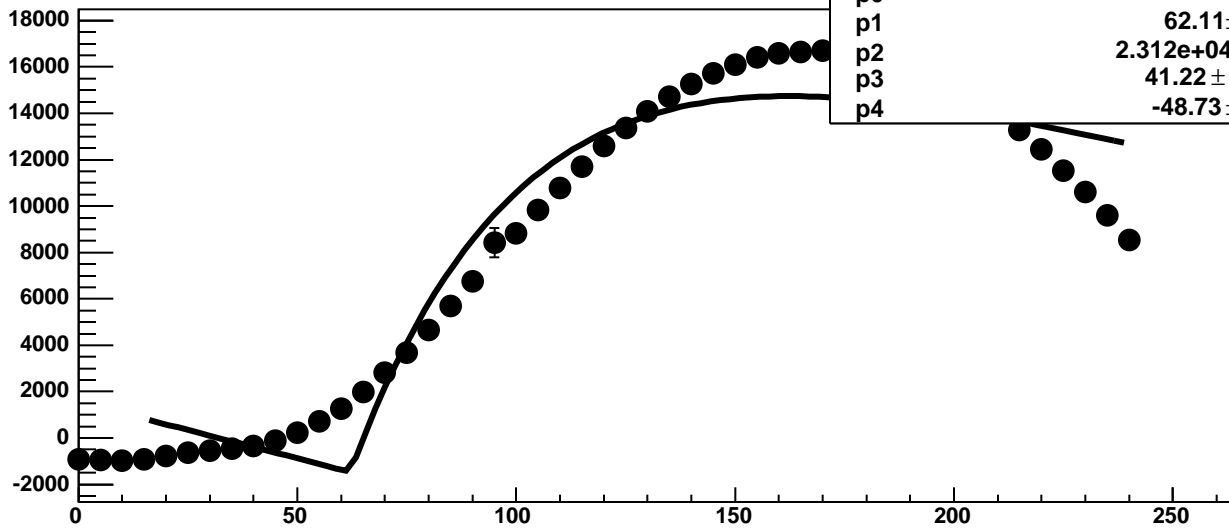
Chip 4, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



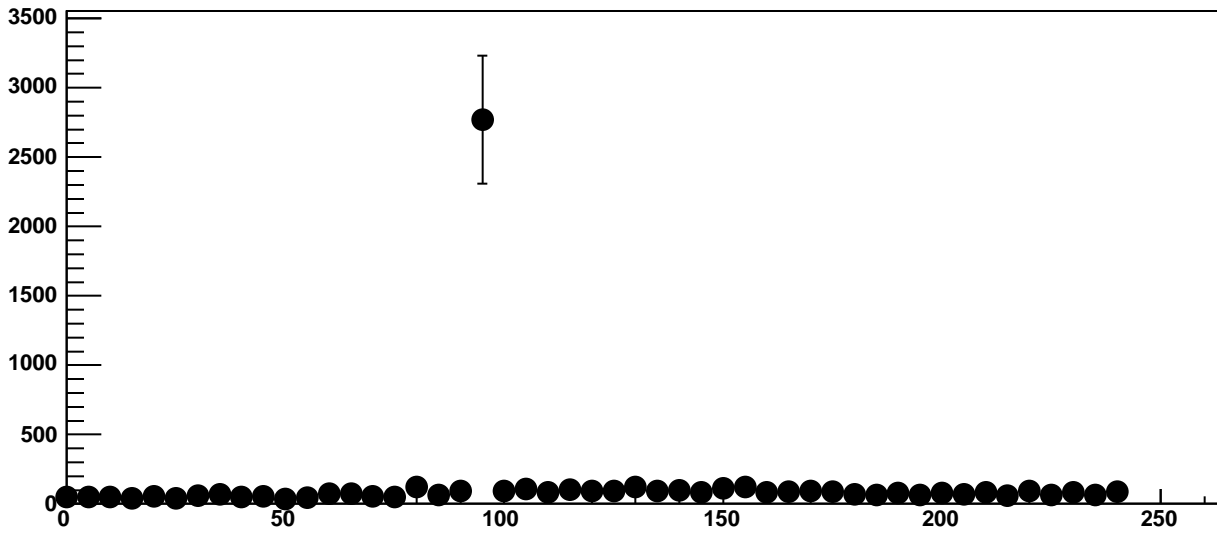
Chip 4, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold



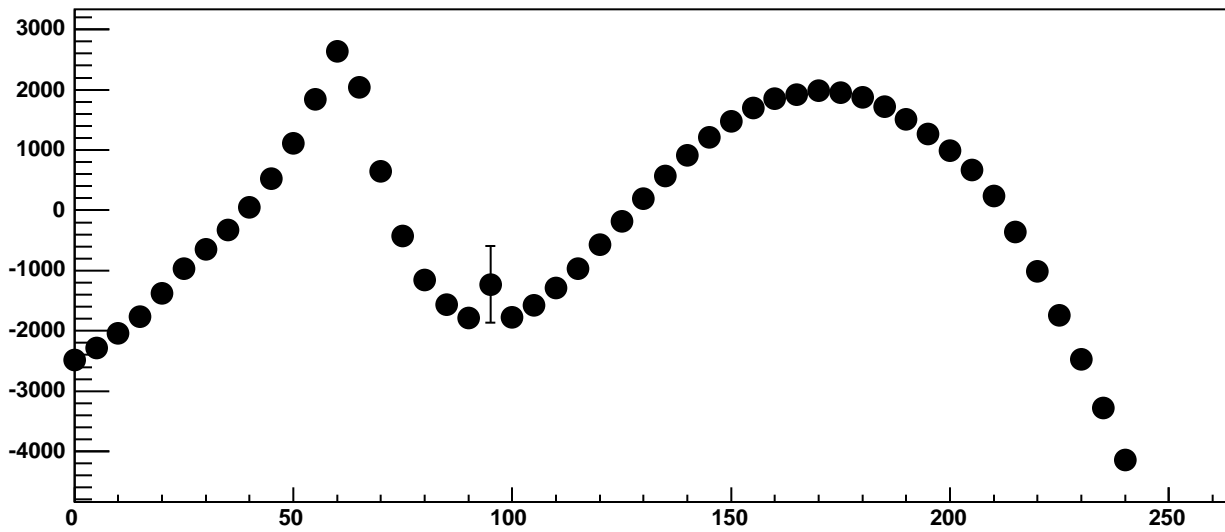
Chip 4, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold



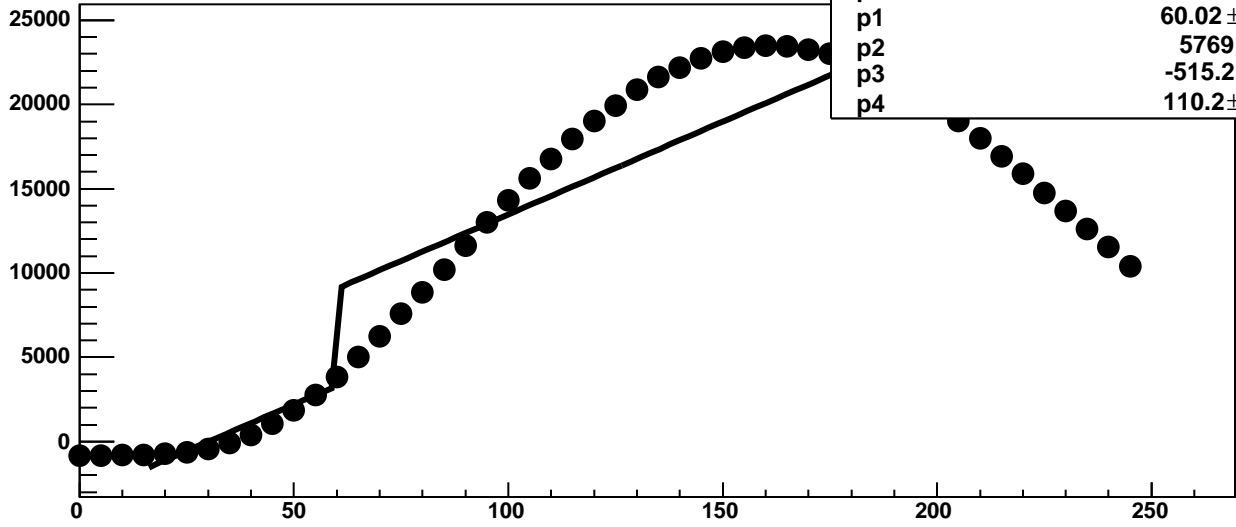
Chip 4, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

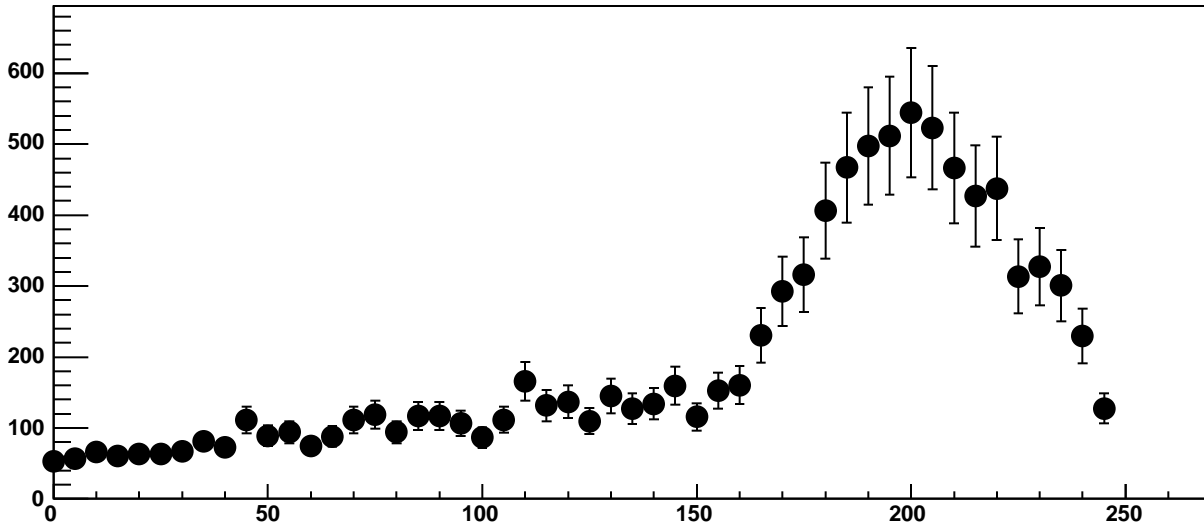


Chip 4, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

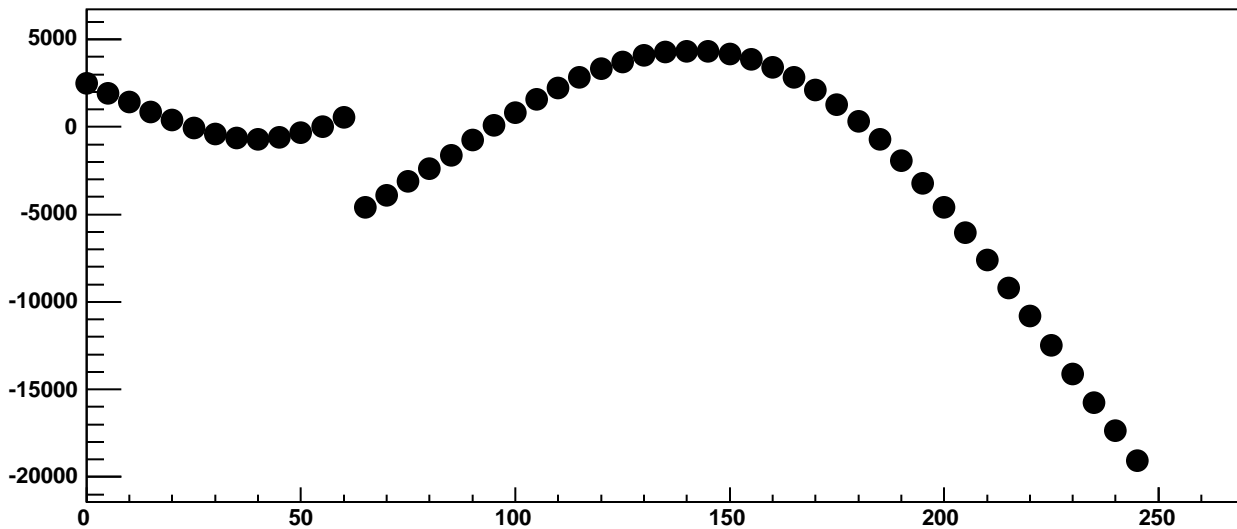


$\chi^2 / \text{ndf}$	5.423e+05 / 41
p0	3298 ± 17.69
p1	60.02 ± 0.2103
p2	5769 ± 39.94
p3	-515.2 ± 16.96
p4	110.2 ± 0.6213

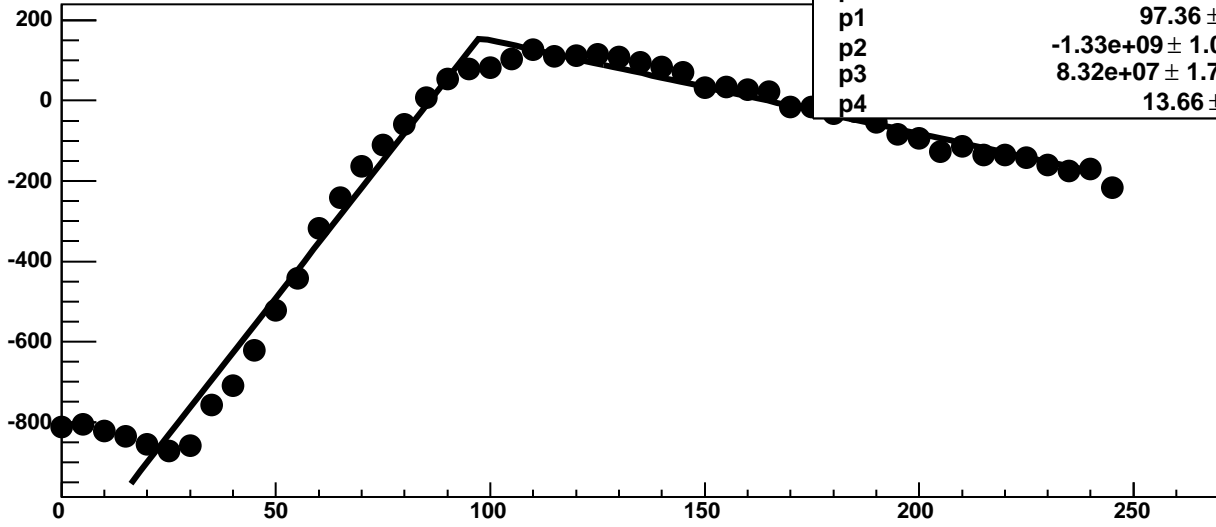
Chip 4, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



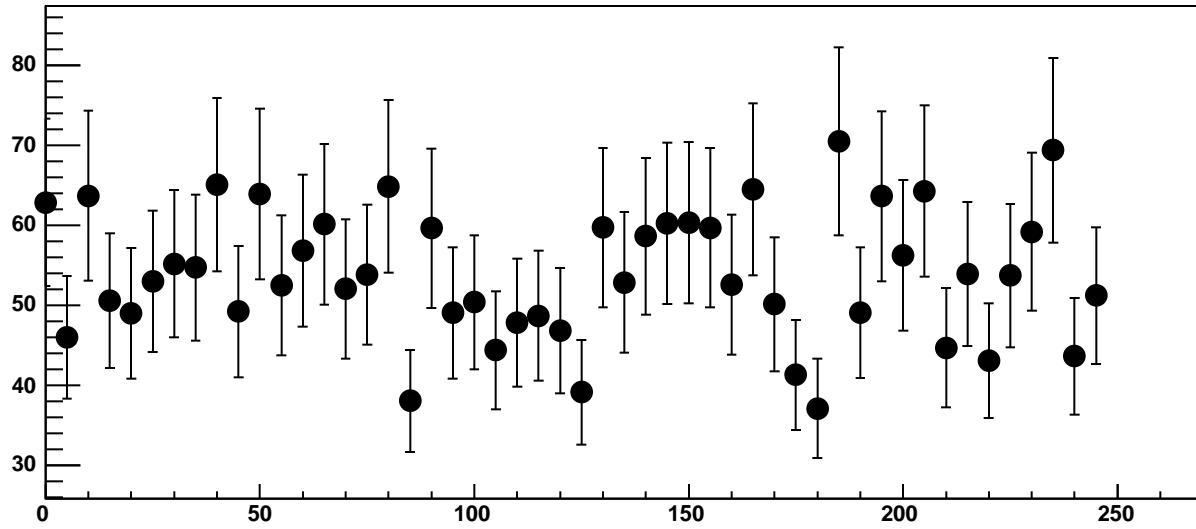
Chip 4, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold



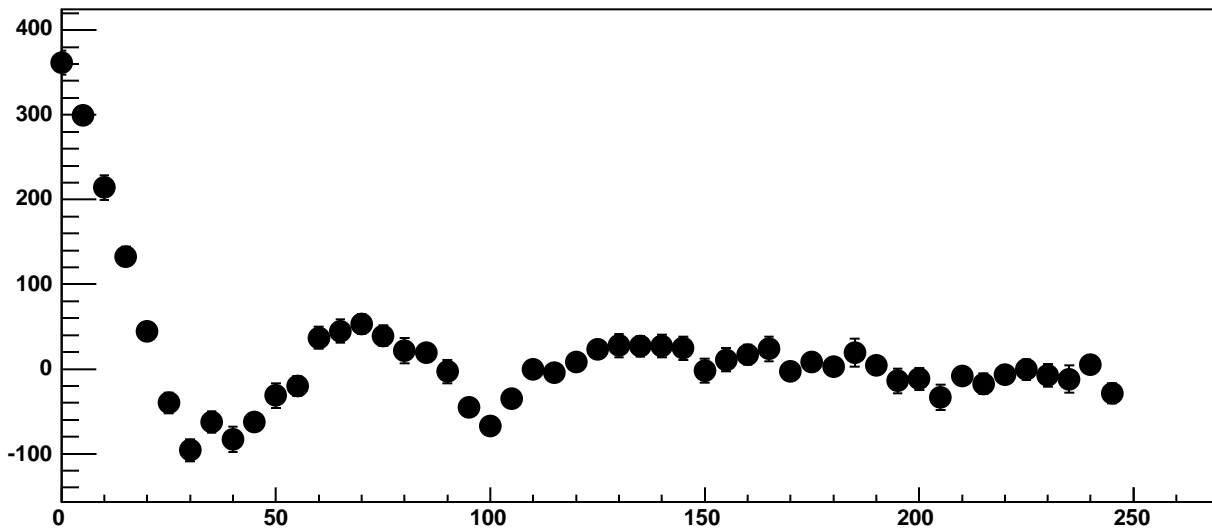
Chip 4, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold



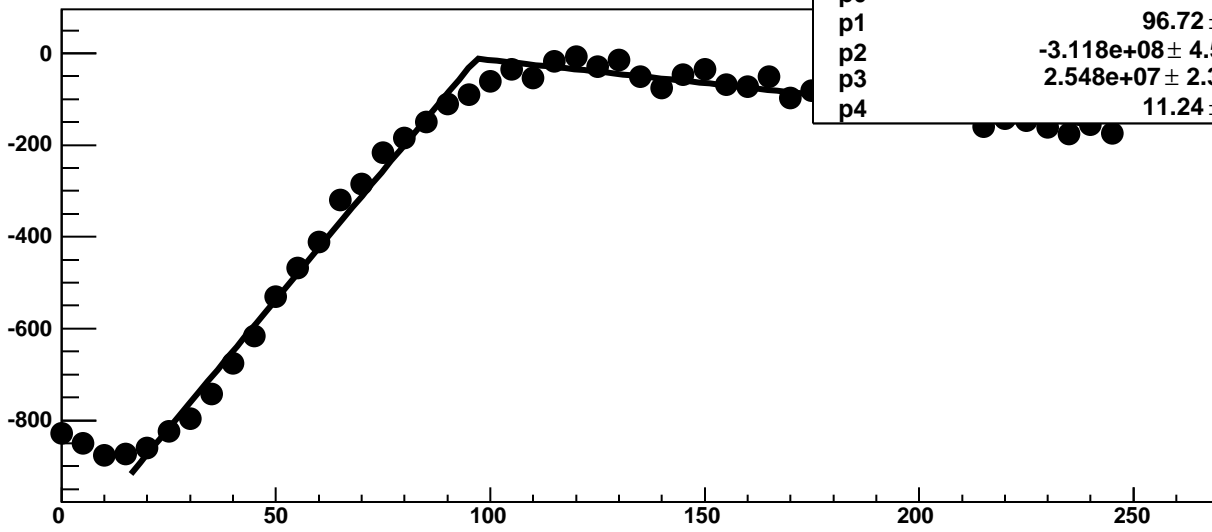
Chip 4, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

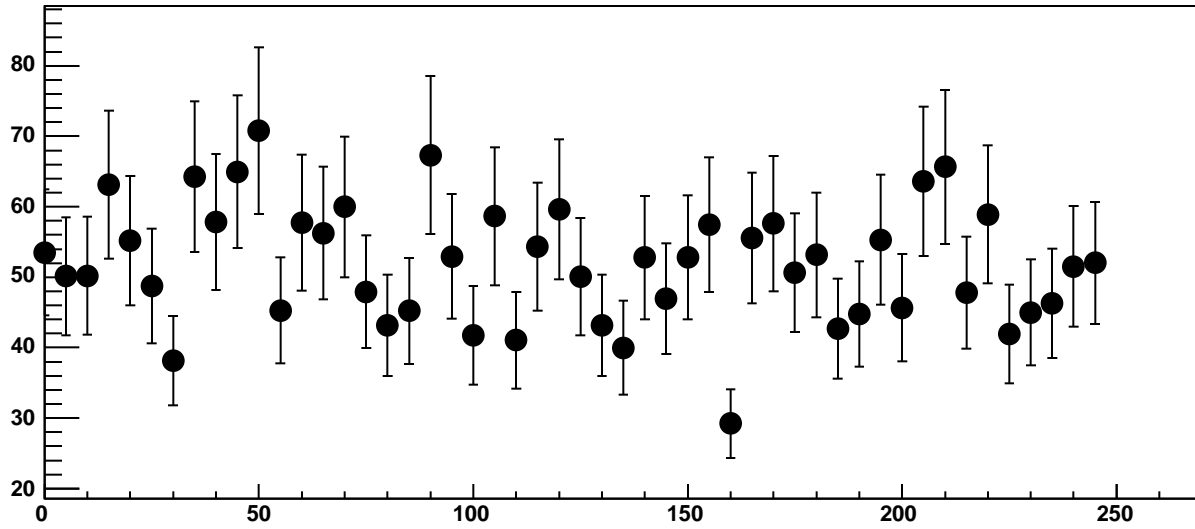


Chip 4, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

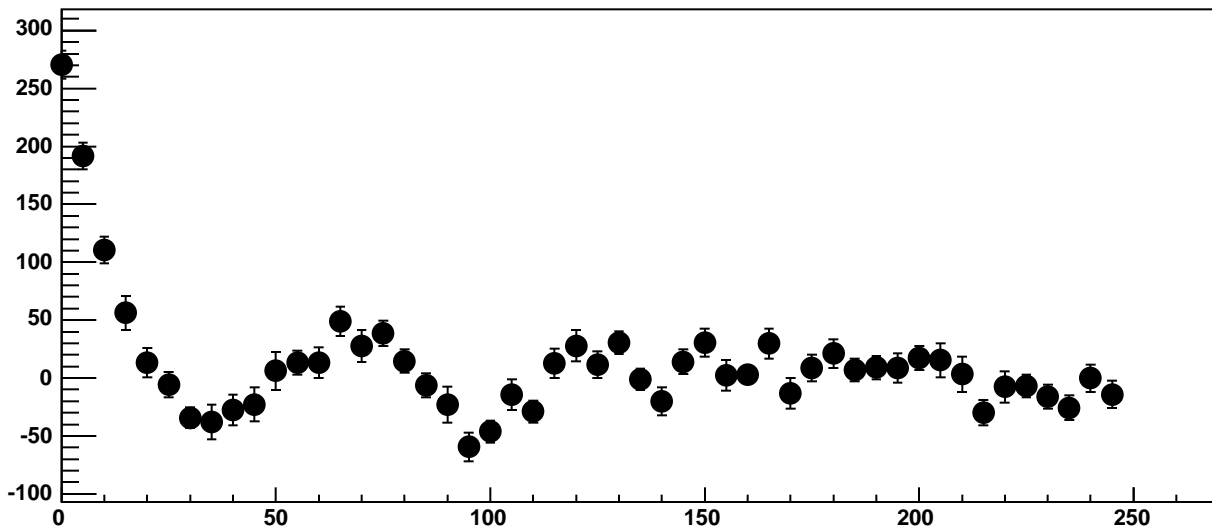


$\chi^2 / \text{ndf}$	200 / 41
p0	$-11.67 \pm 3.779$
p1	$96.72 \pm 0.5752$
p2	$-3.118\text{e}+08 \pm 4.591\text{e}+06$
p3	$2.548\text{e}+07 \pm 2.344\text{e}+05$
p4	$11.24 \pm 0.1195$

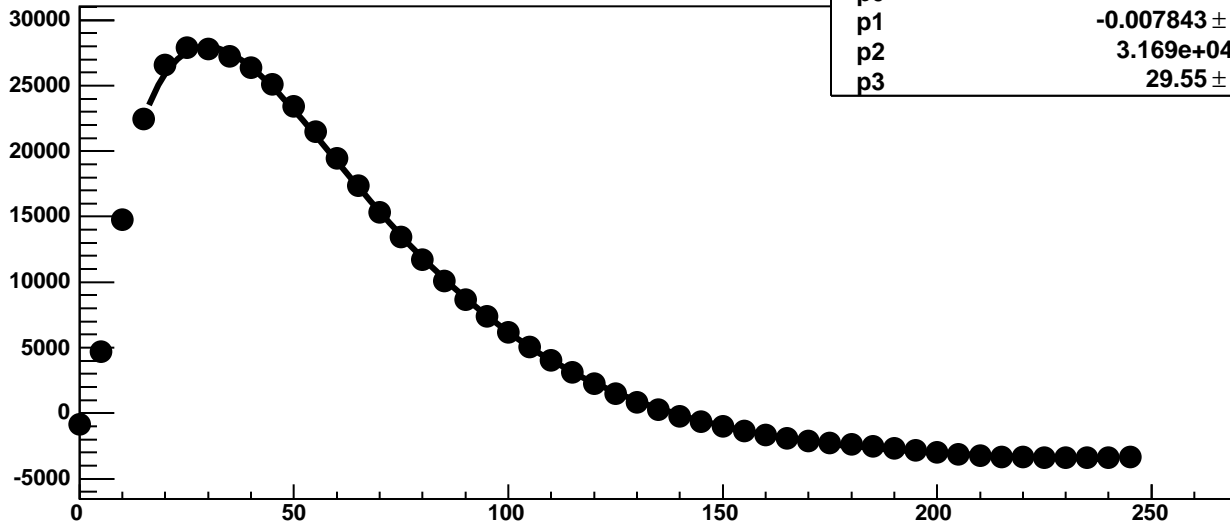
Chip 4, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

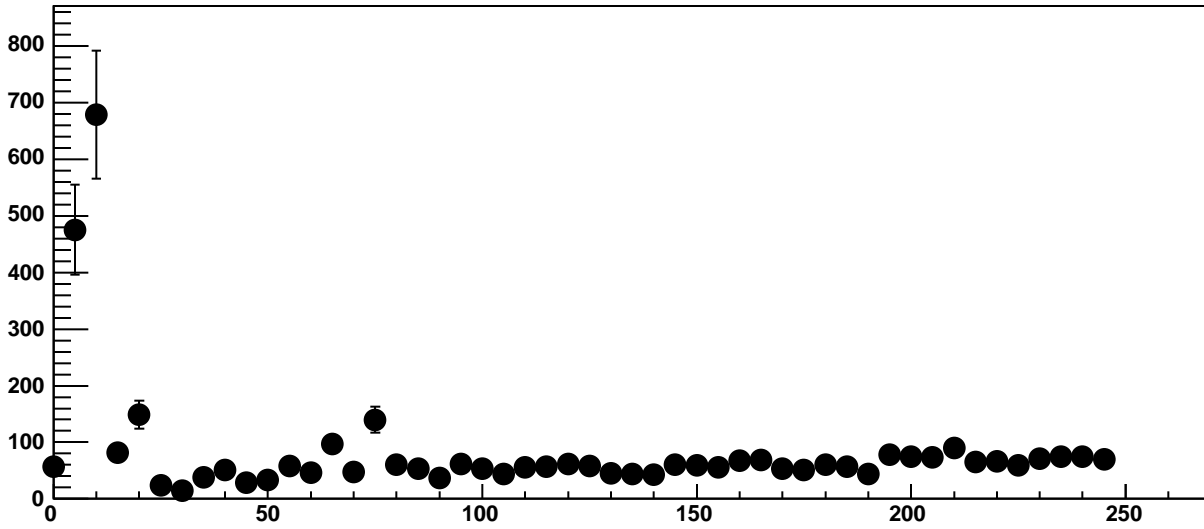


Chip 4, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

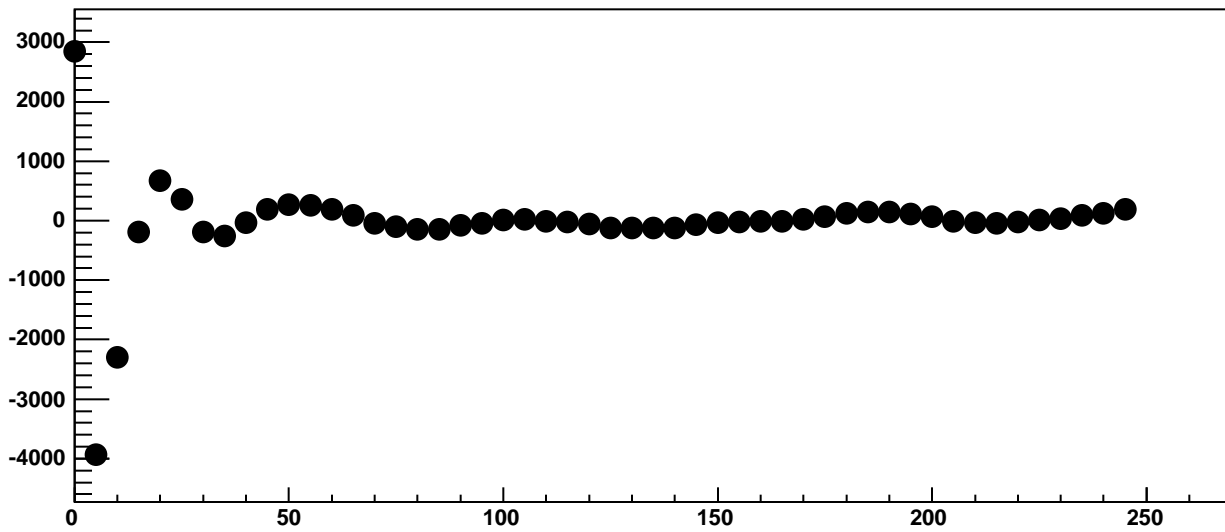


$\chi^2 / \text{ndf}$	1.31e+04 / 42
p0	-3705 ± 4.08
p1	-0.007843 ± 0.01884
p2	3.169e+04 ± 4.419
p3	29.55 ± 0.01068

Chip 4, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

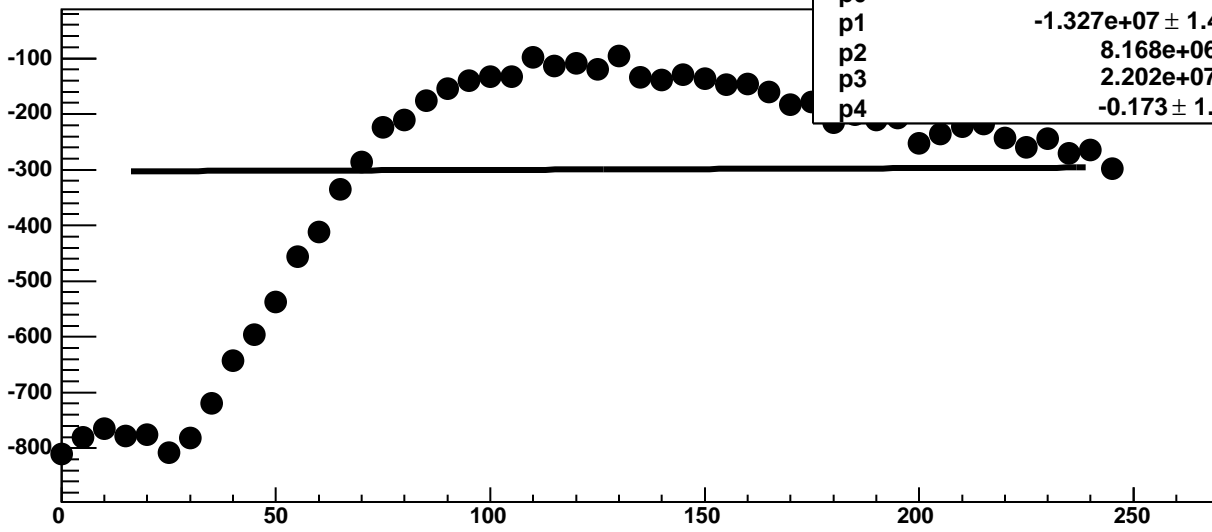


Chip 4, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold

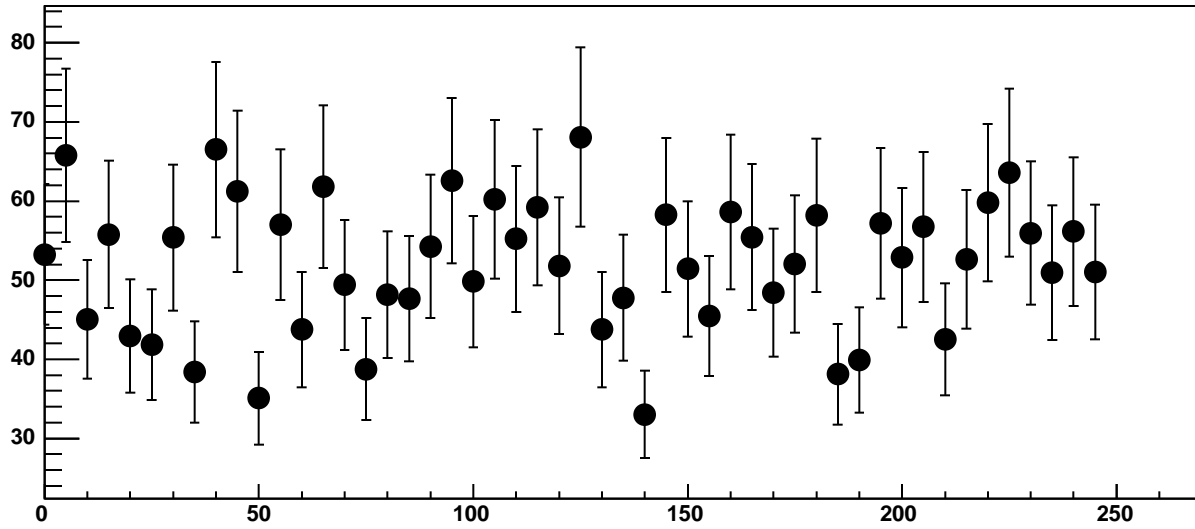




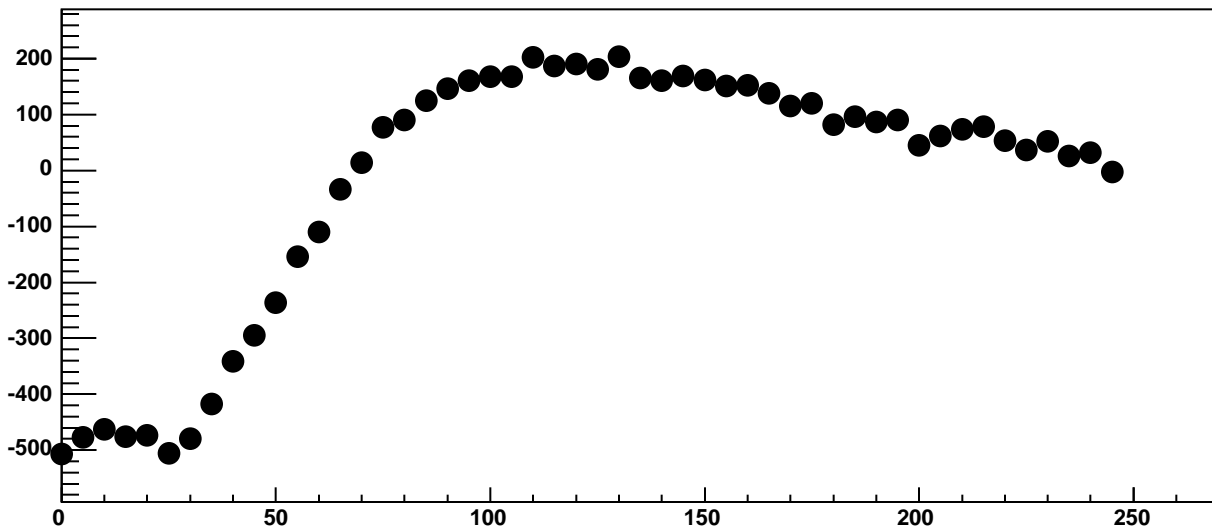
Chip 4, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold



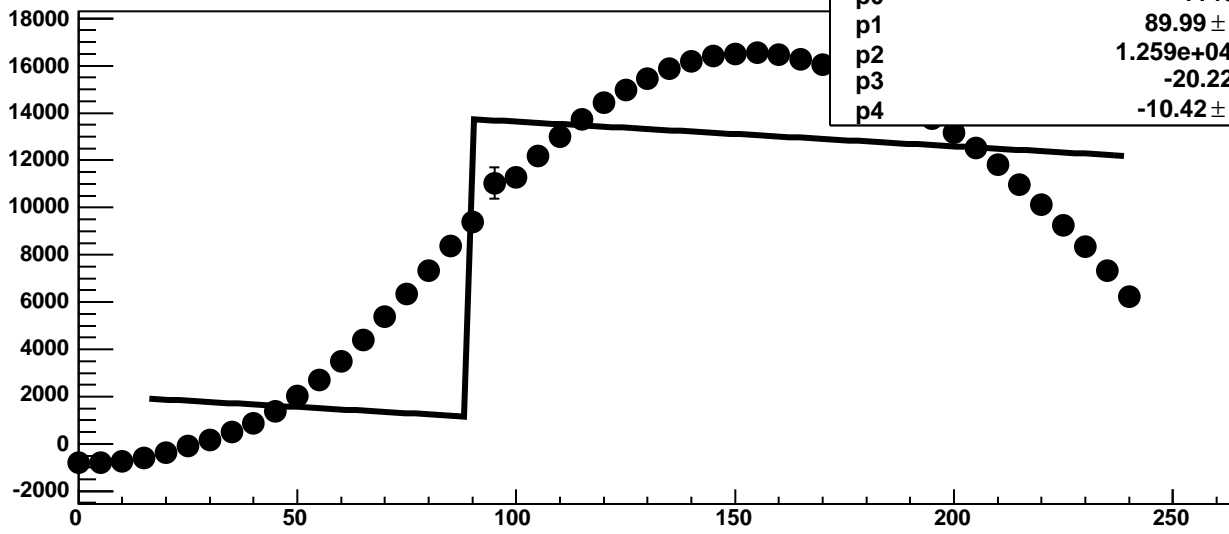
Chip 4, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



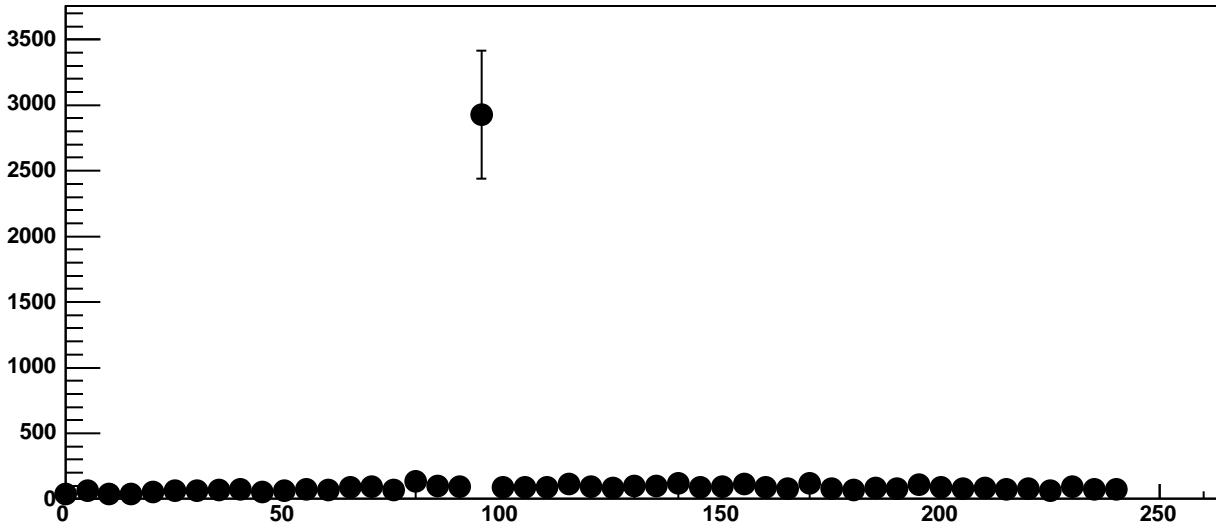
Chip 4, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold



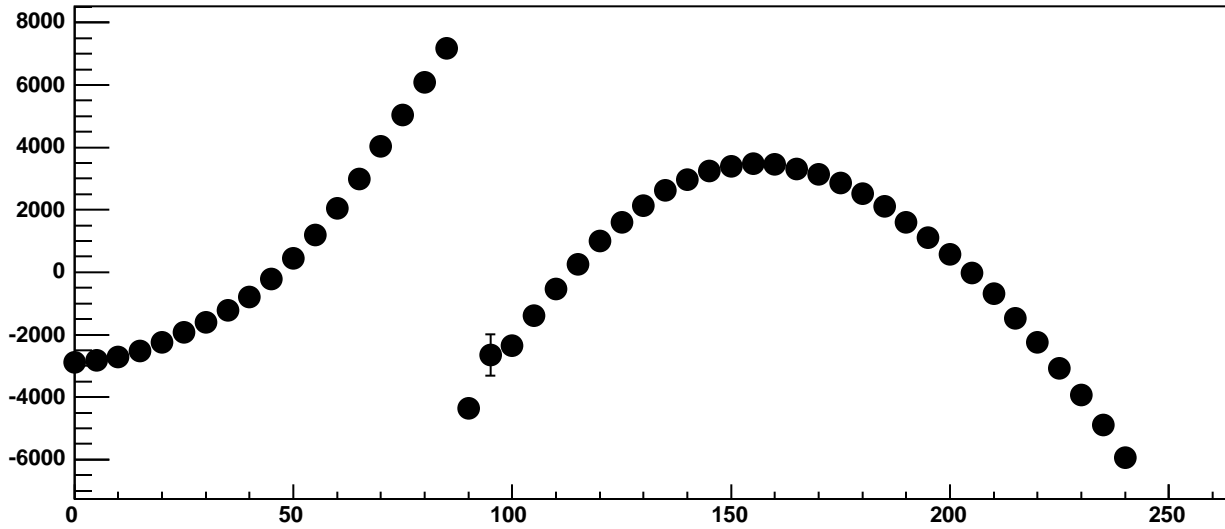
Chip 4, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold



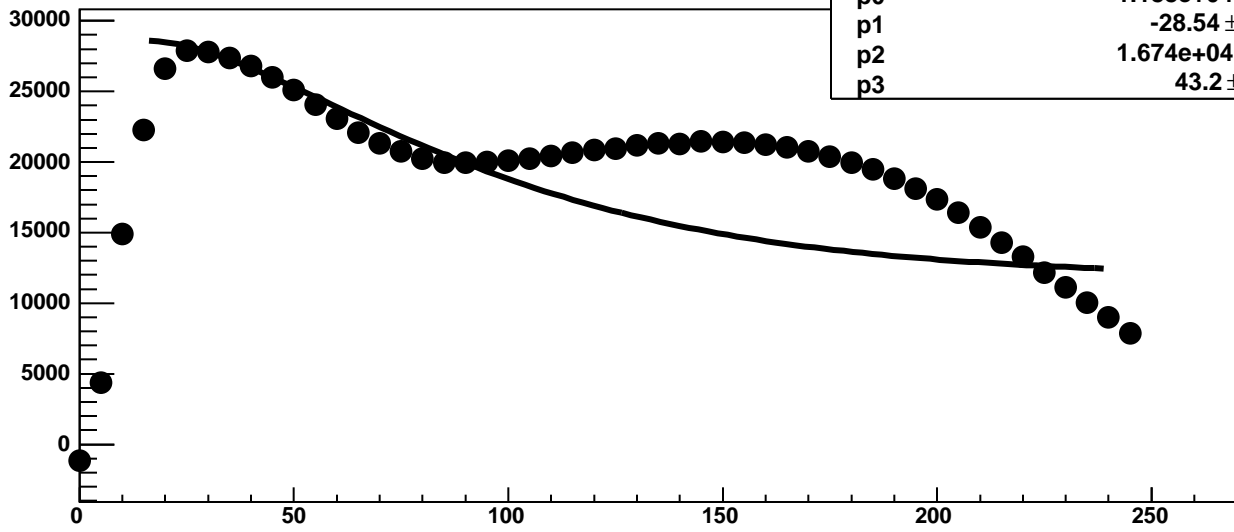
Chip 4, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

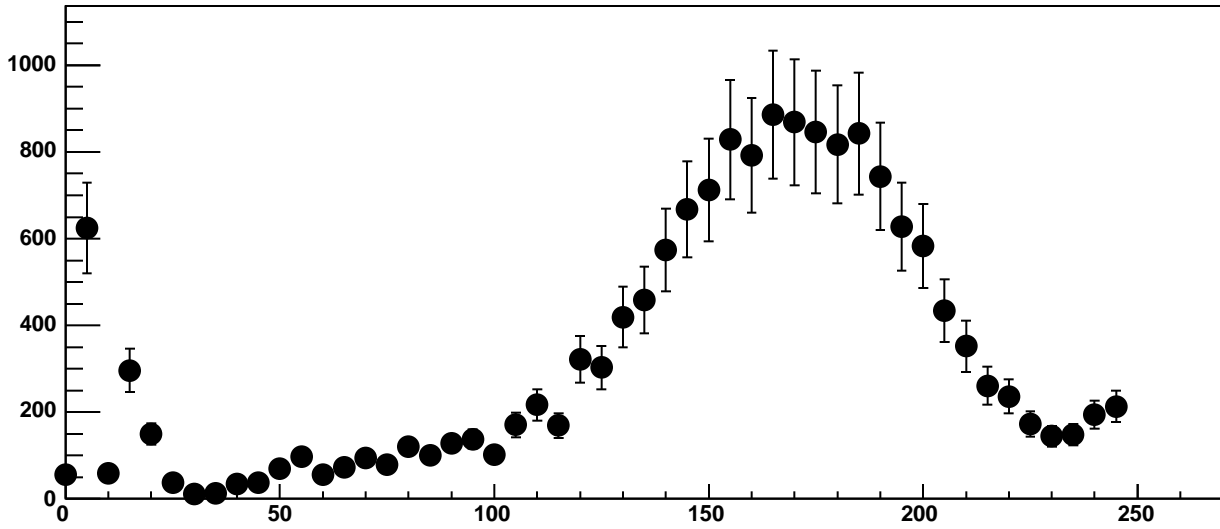


Chip 4, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold

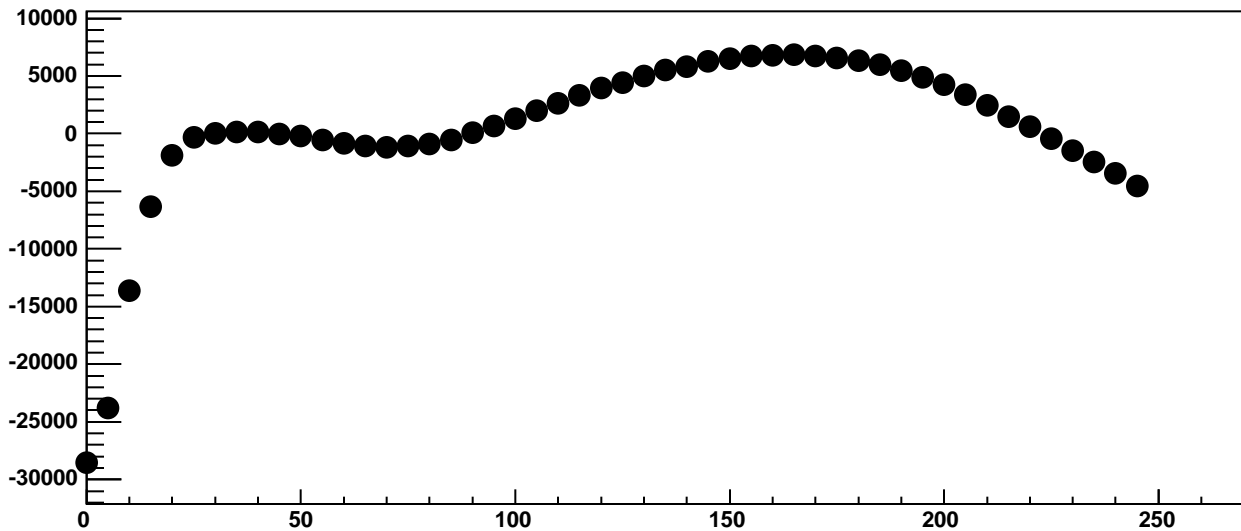


$\chi^2 / \text{ndf}$	9.349e+04 / 42
p0	1.188e+04 $\pm$ 26.63
p1	-28.54 $\pm$ 0.4175
p2	1.674e+04 $\pm$ 42.33
p3	43.2 $\pm$ 0.1817

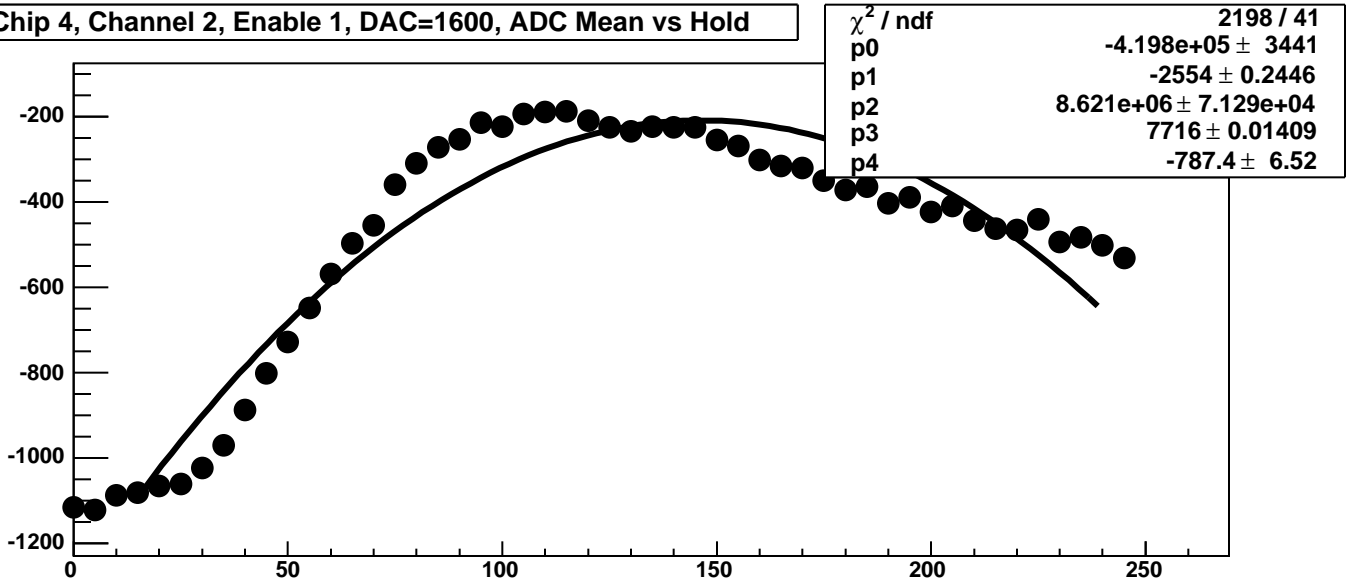
Chip 4, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



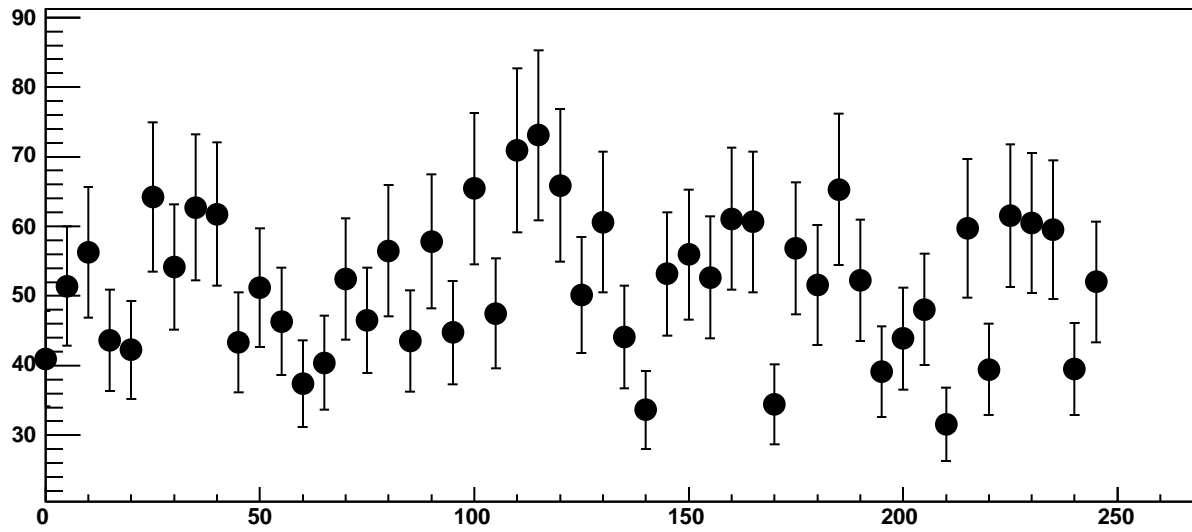
Chip 4, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold



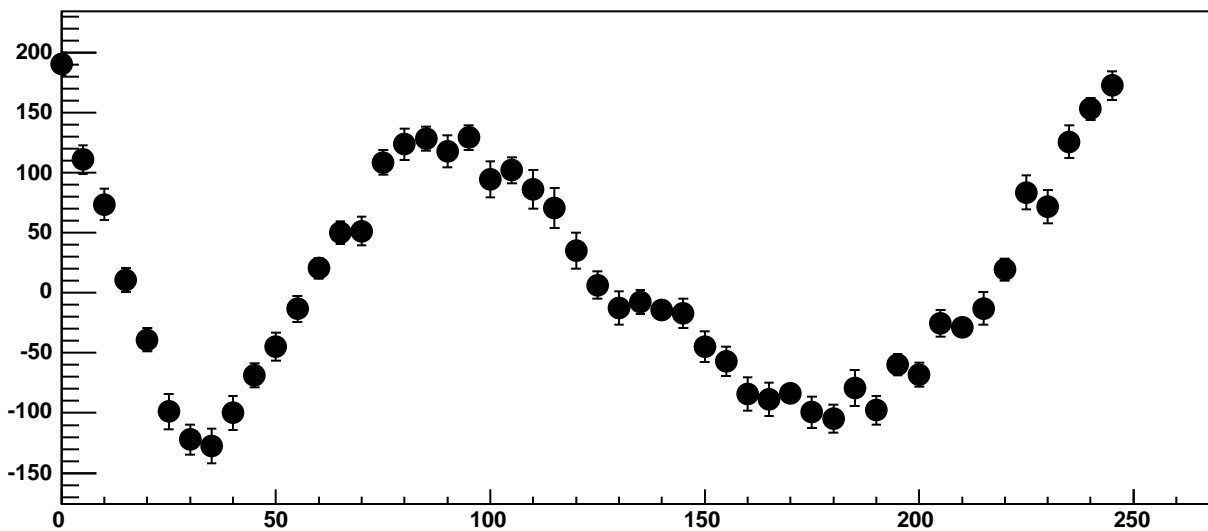
Chip 4, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold



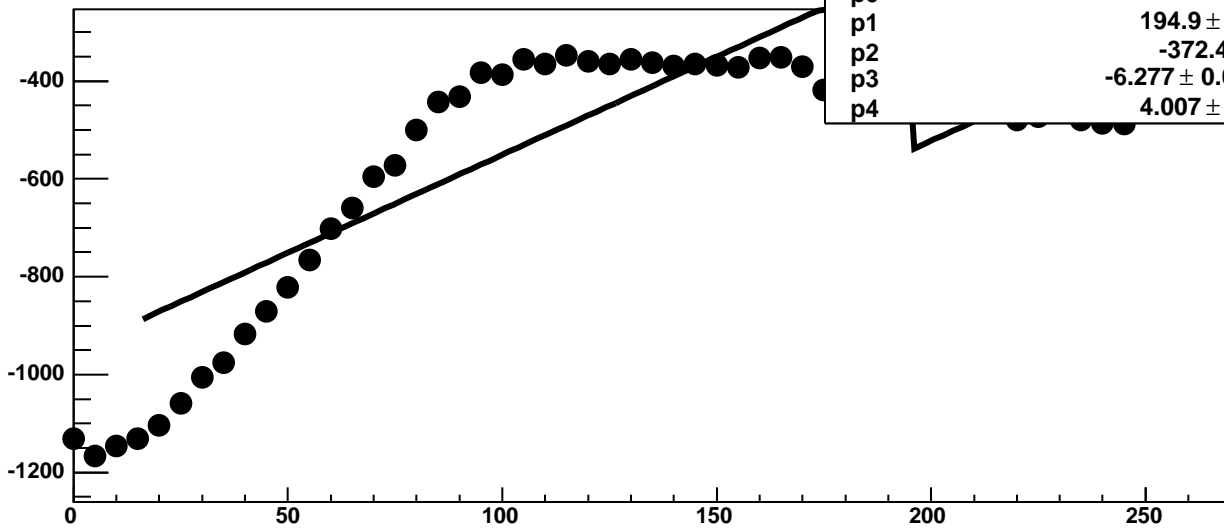
Chip 4, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold

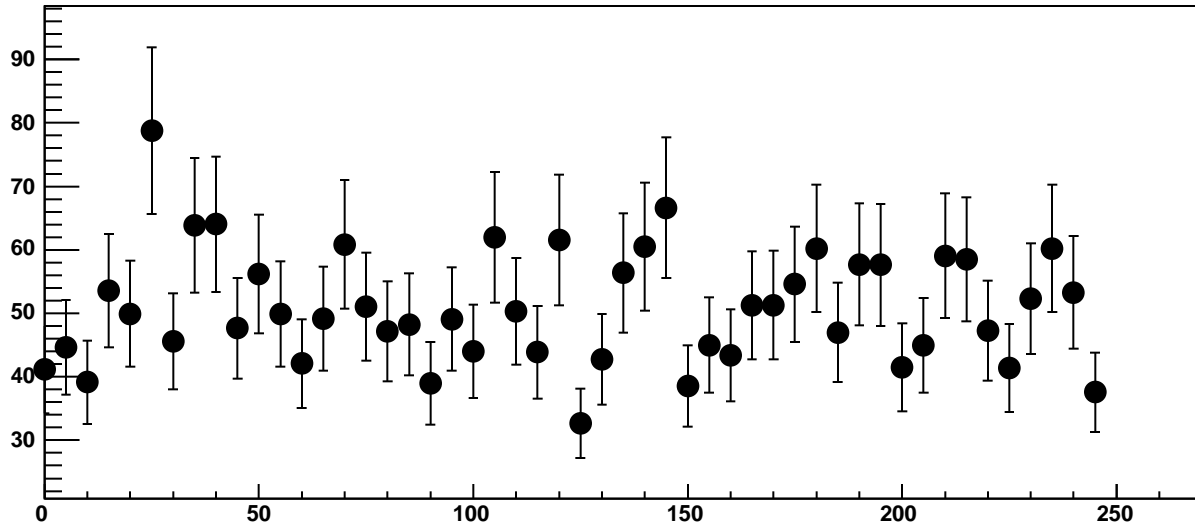


Chip 4, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

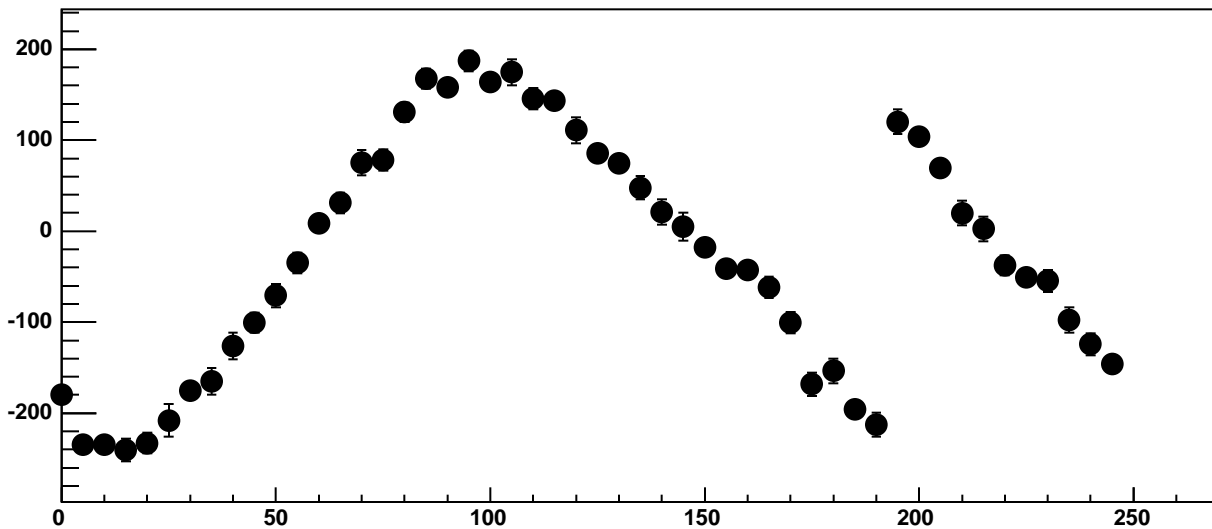


$\chi^2 / \text{ndf}$	5118 / 41
p0	$-170.2 \pm 4.095$
p1	$194.9 \pm 0.06789$
p2	$-372.4 \pm 5.753$
p3	$-6.277 \pm 0.0002282$
p4	$4.007 \pm 0.04229$

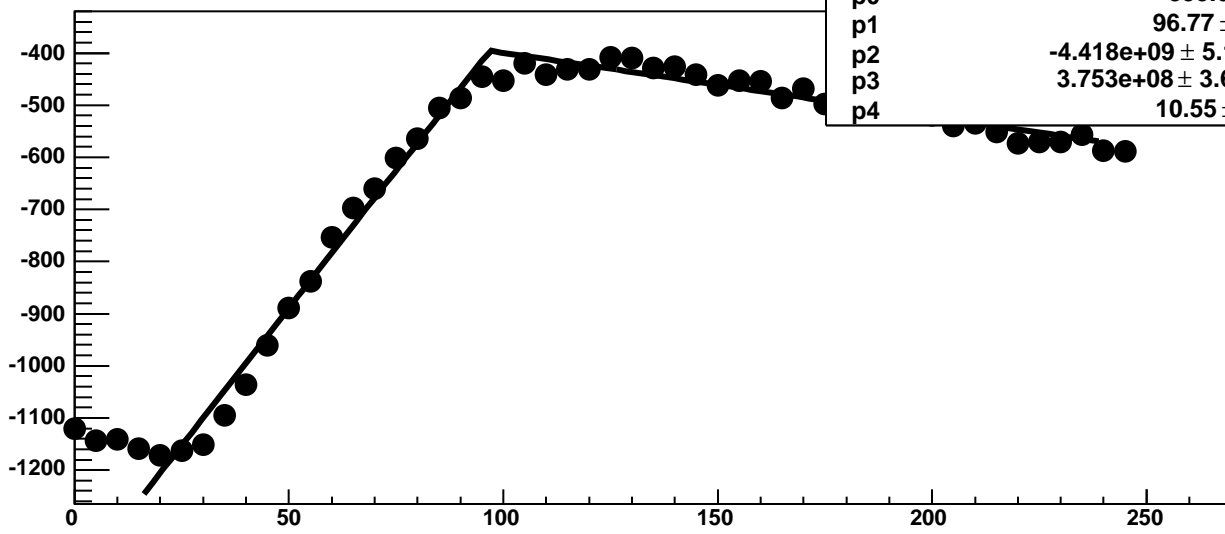
Chip 4, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

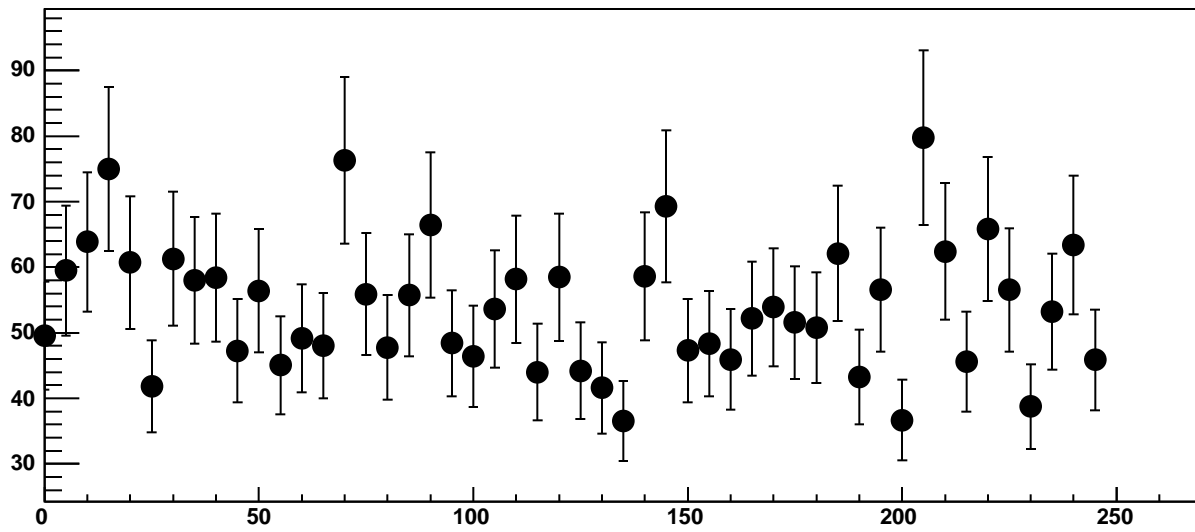


Chip 4, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

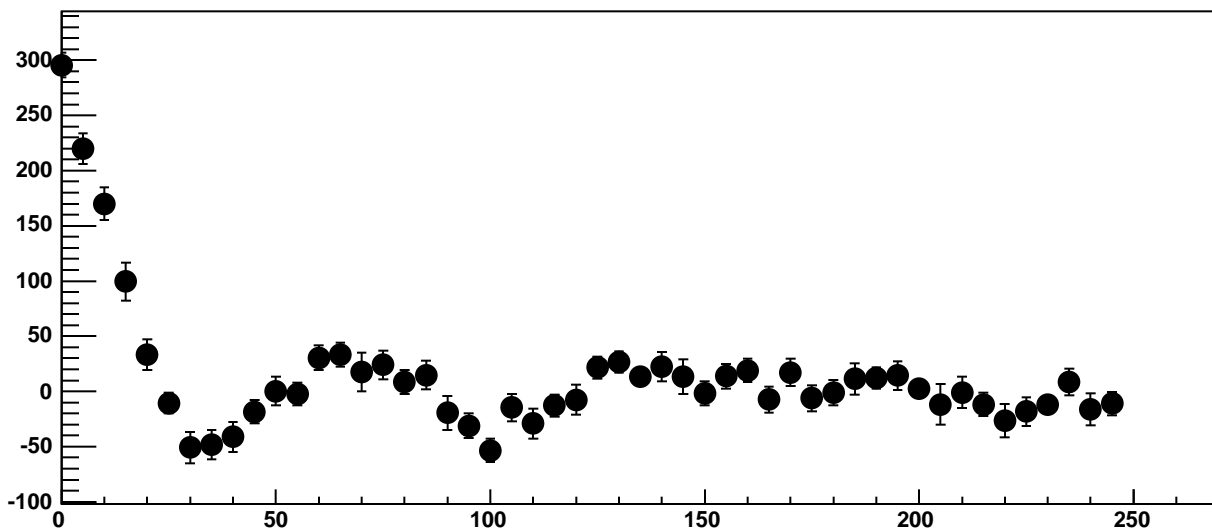


$\chi^2 / \text{ndf}$	184.2 / 41
p0	$-395.6 \pm 3.833$
p1	$96.77 \pm 0.6156$
p2	$-4.418\text{e}+09 \pm 5.156\text{e}+07$
p3	$3.753\text{e}+08 \pm 3.628\text{e}+05$
p4	$10.55 \pm 0.1259$

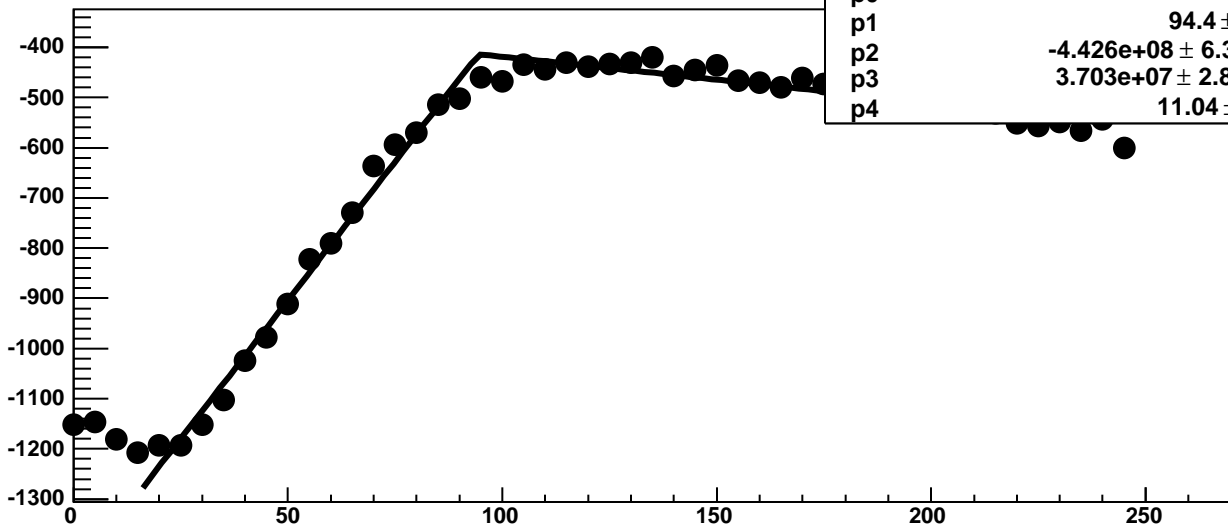
Chip 4, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold

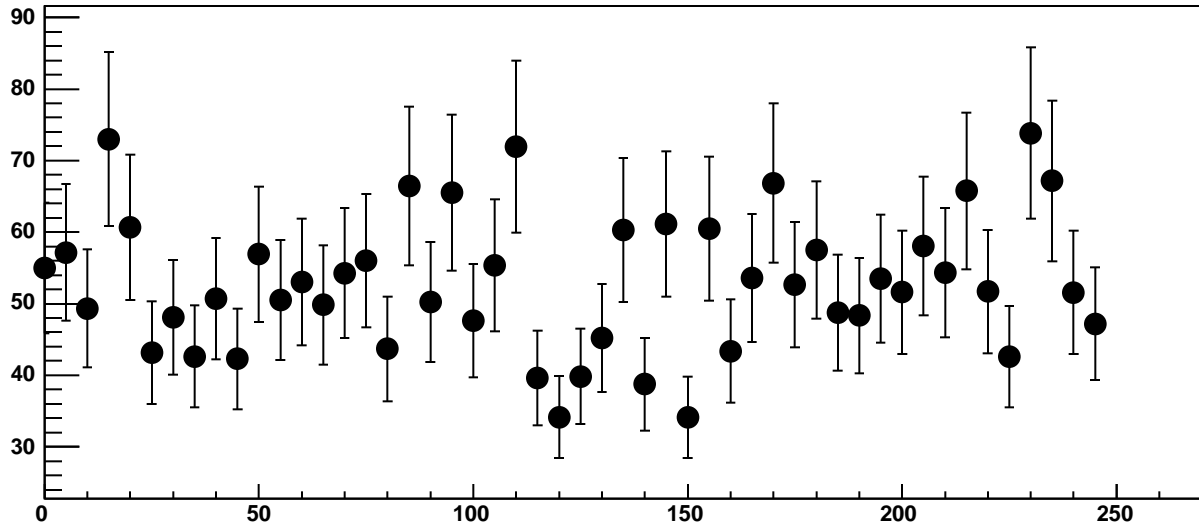


Chip 4, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

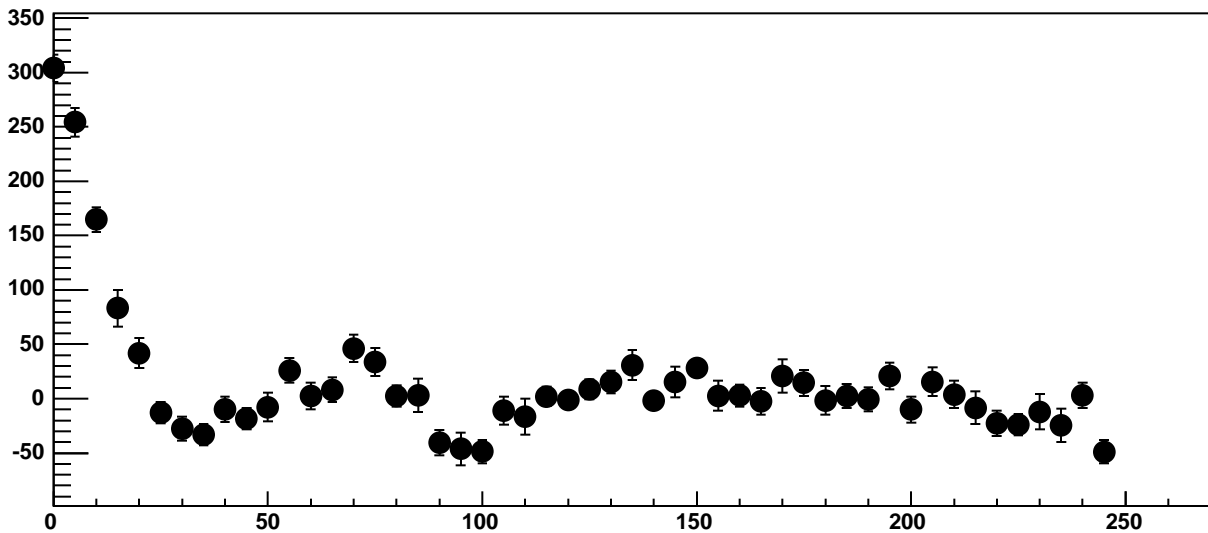


$\chi^2 / \text{ndf}$	171.4 / 41
p0	$-413.6 \pm 3.735$
p1	$94.4 \pm 0.6248$
p2	$-4.426\text{e}+08 \pm 6.385\text{e}+06$
p3	$3.703\text{e}+07 \pm 2.833\text{e}+05$
p4	$11.04 \pm 0.1331$

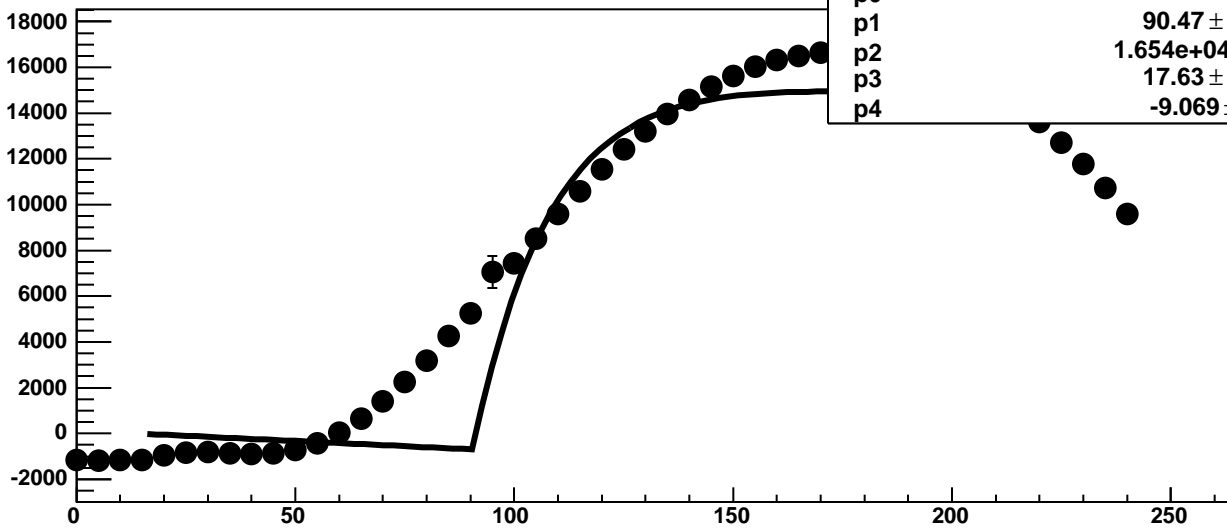
Chip 4, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

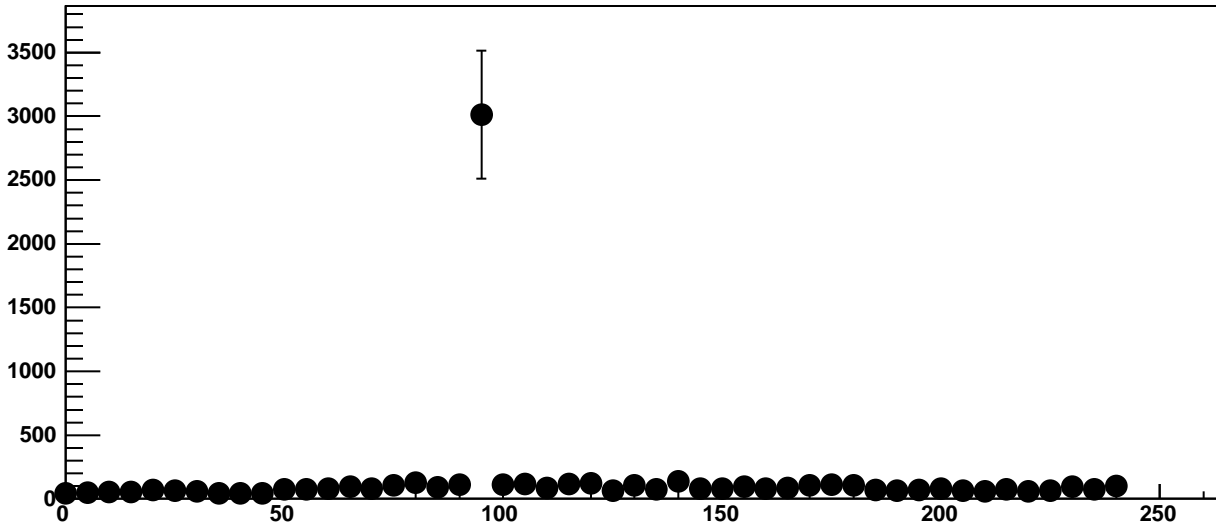


Chip 4, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

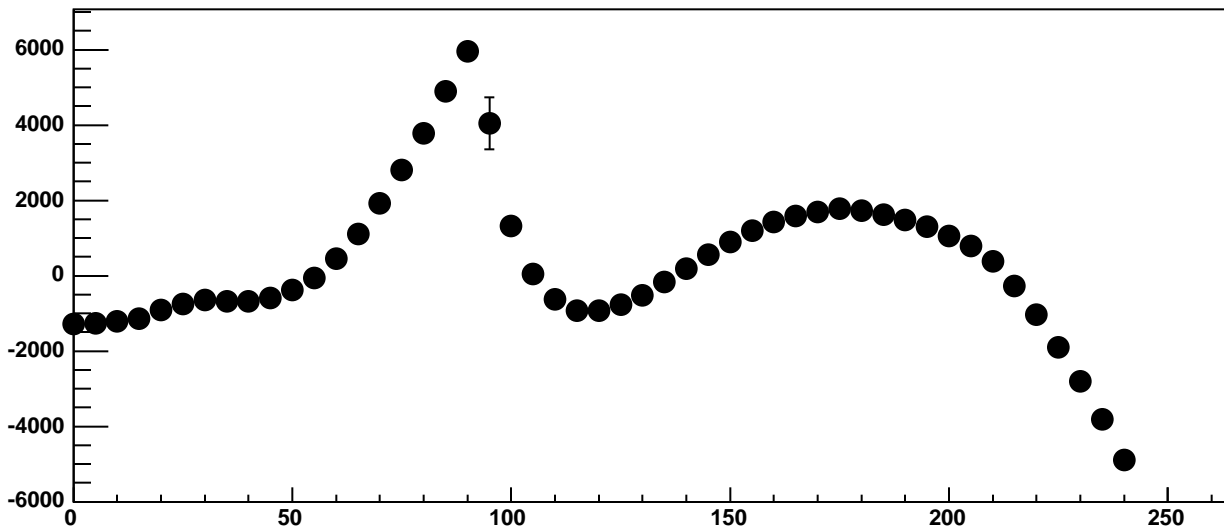


$\chi^2 / \text{ndf}$	3.84e+05 / 41
p0	-695 ± 7
p1	90.47 ± 0.05292
p2	1.654e+04 ± 20.85
p3	17.63 ± 0.05356
p4	-9.069 ± 0.1267

Chip 4, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

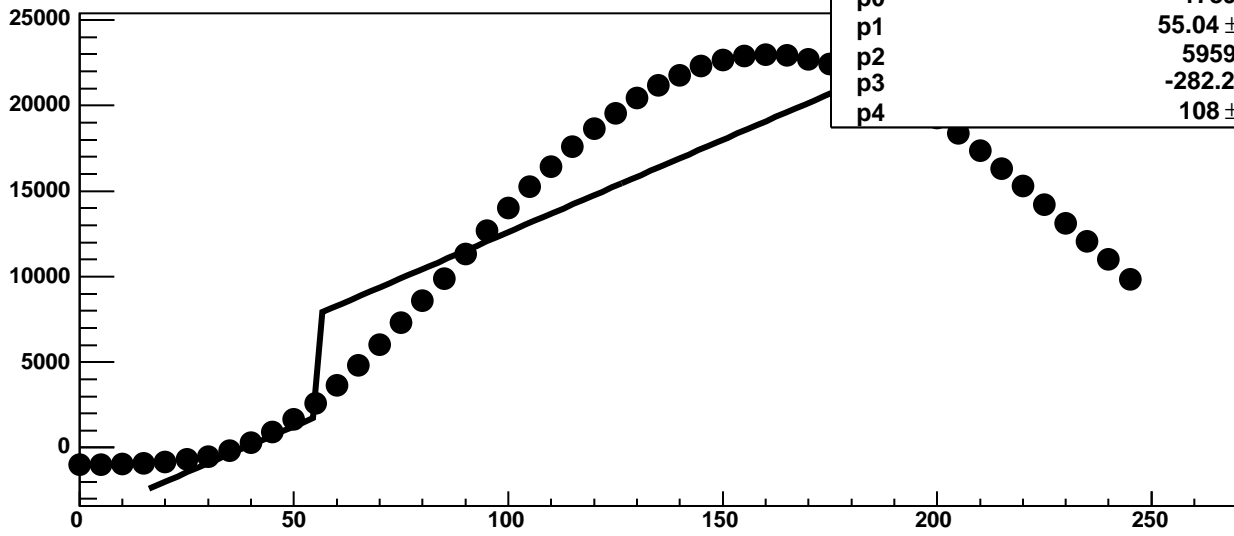


Chip 4, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



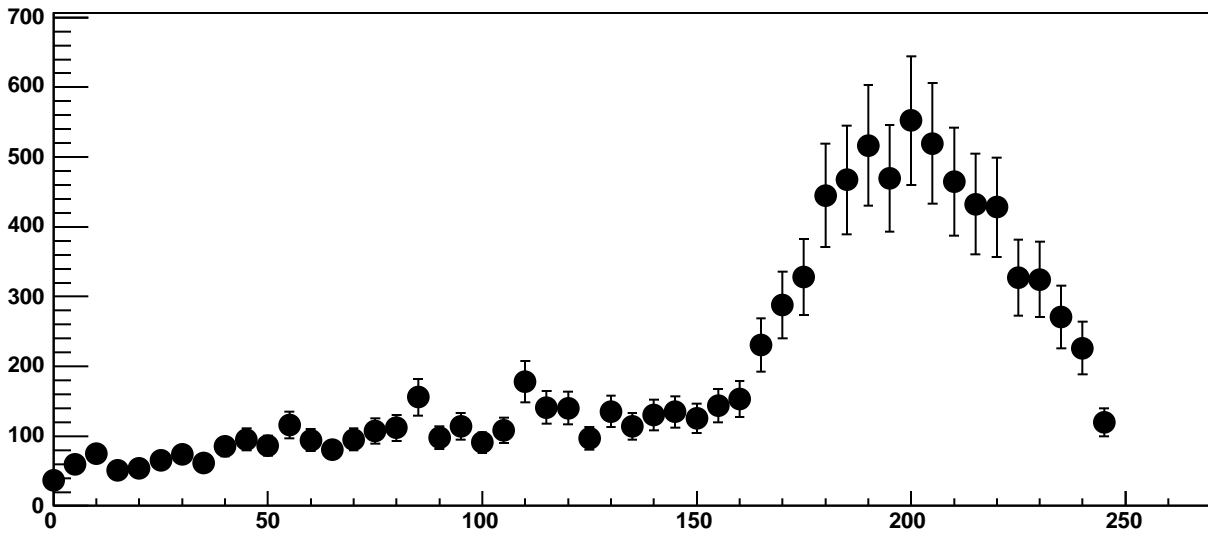


Chip 4, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

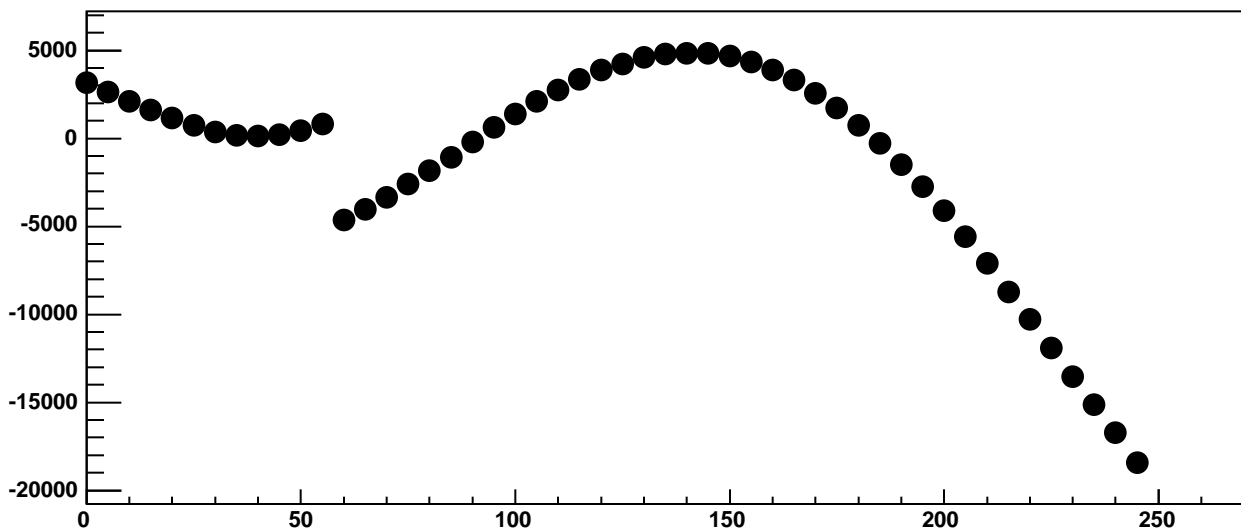


$\chi^2 / \text{ndf}$	6.615e+05 / 41
p0	1789 ± 11.07
p1	55.04 ± 0.2825
p2	5959 ± 31.81
p3	-282.2 ± 8.136
p4	108 ± 0.5216

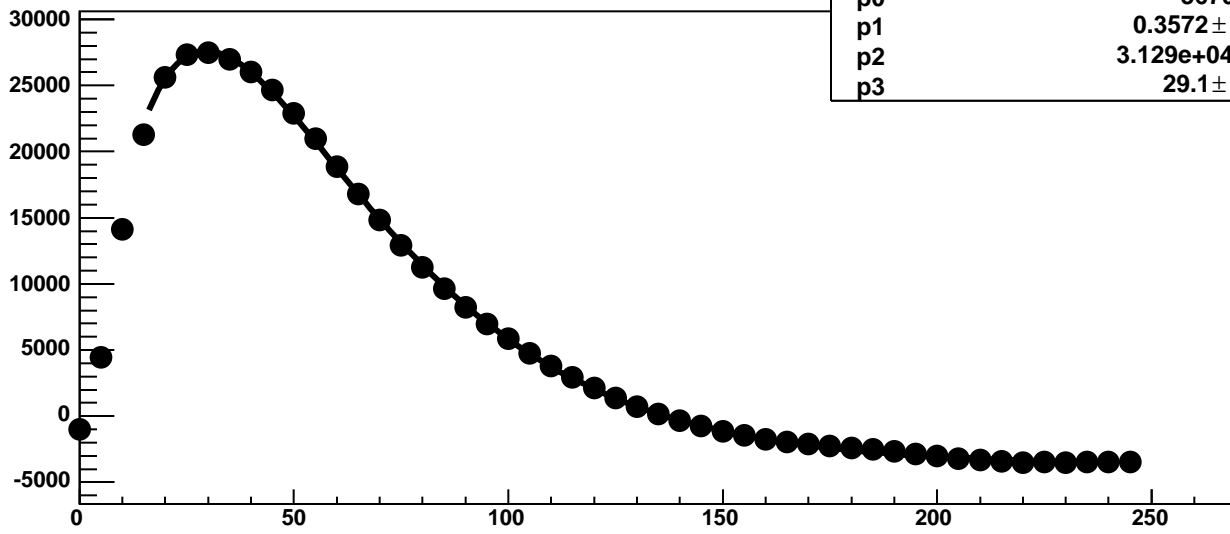
Chip 4, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

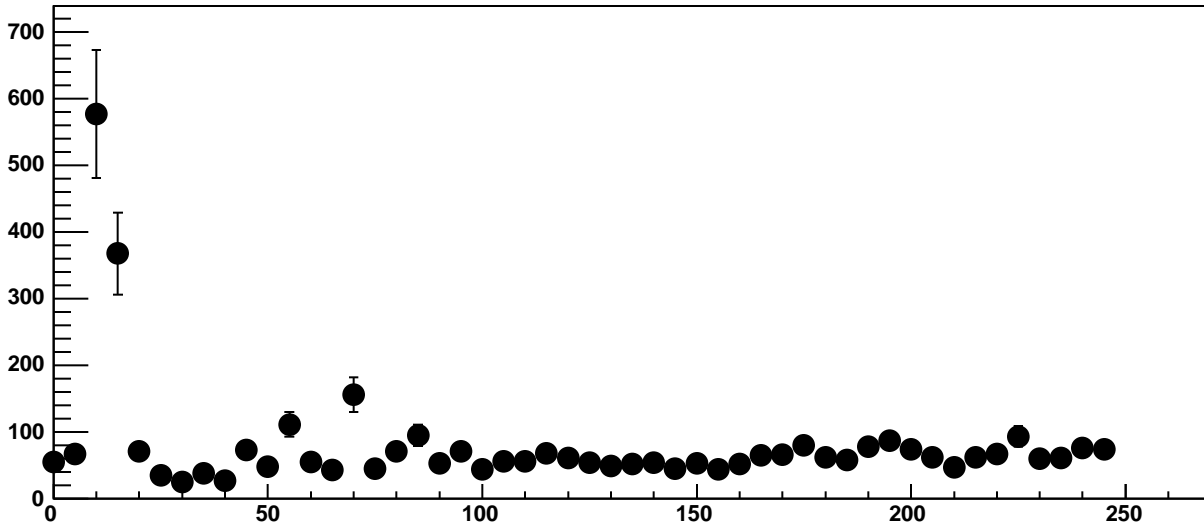


Chip 4, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold

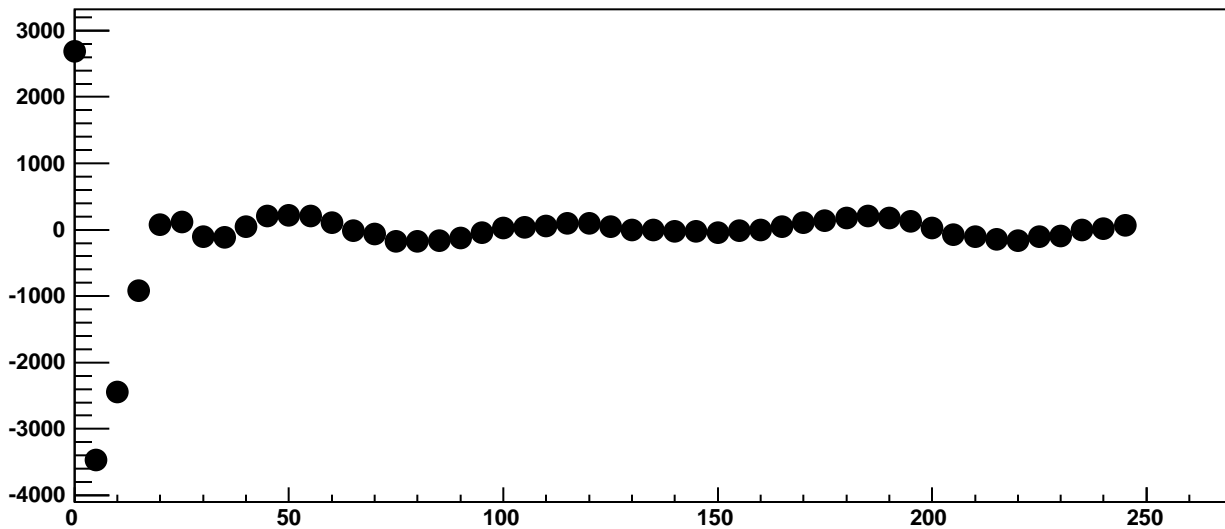


$\chi^2 / \text{ndf}$	3359 / 42
p0	$-3670 \pm 4.223$
p1	$0.3572 \pm 0.02472$
p2	$3.129\text{e}+04 \pm 5.237$
p3	$29.1 \pm 0.01272$

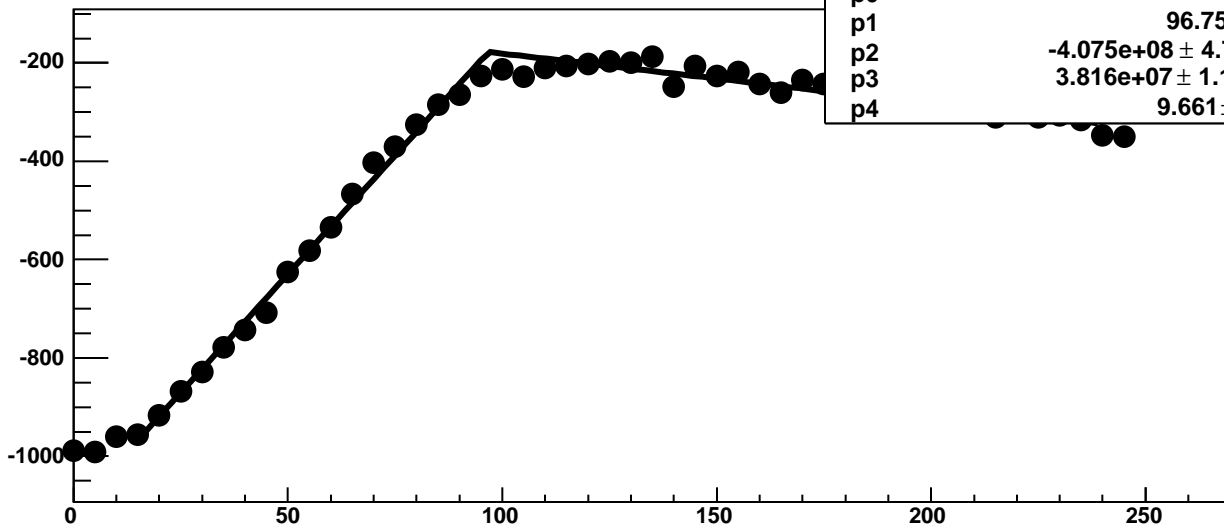
Chip 4, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold

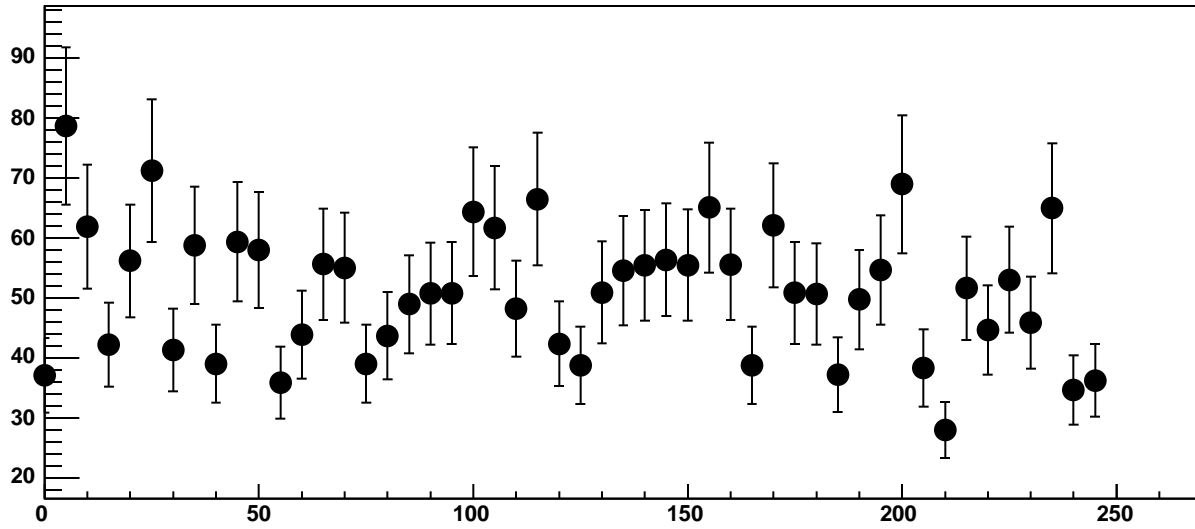


Chip 4, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

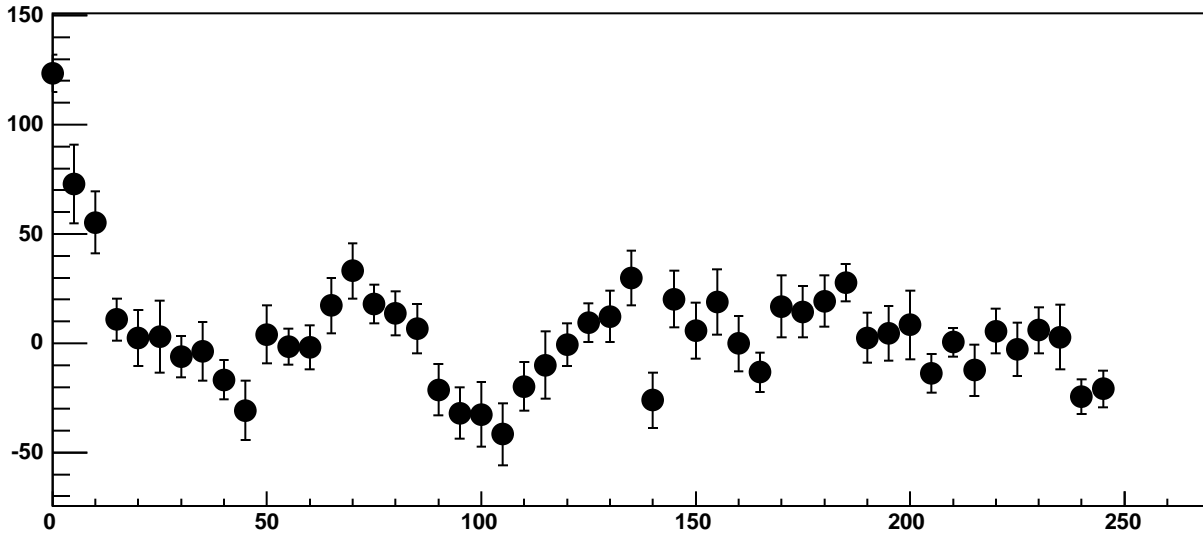


$\chi^2 / \text{ndf}$	102.1 / 41
p0	$-177.7 \pm 4.026$
p1	$96.75 \pm 0.642$
p2	$-4.075\text{e}+08 \pm 4.763\text{e}+06$
p3	$3.816\text{e}+07 \pm 1.159\text{e}+05$
p4	$9.661 \pm 0.1105$

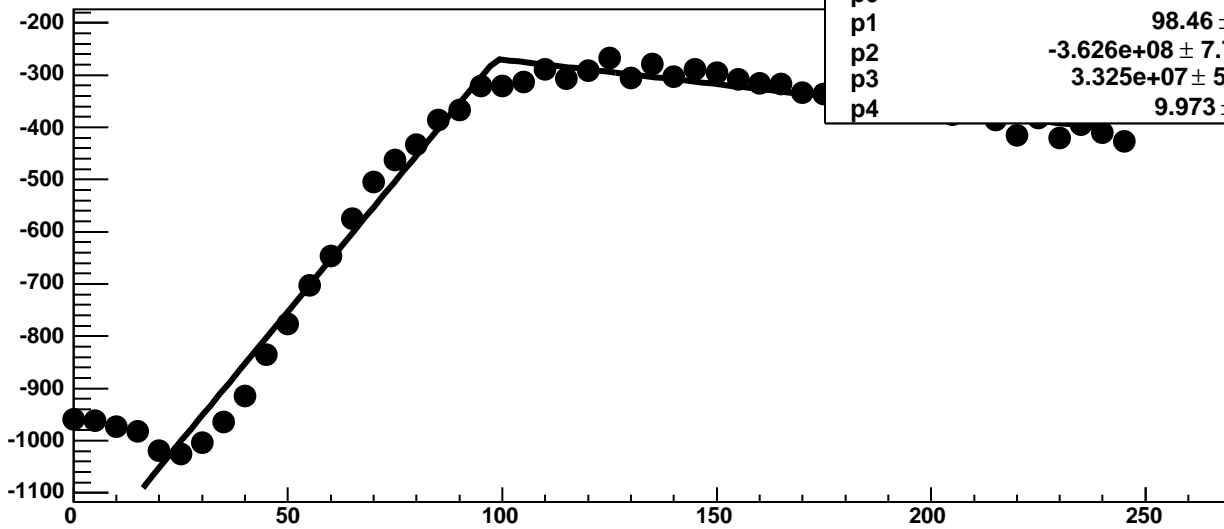
Chip 4, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

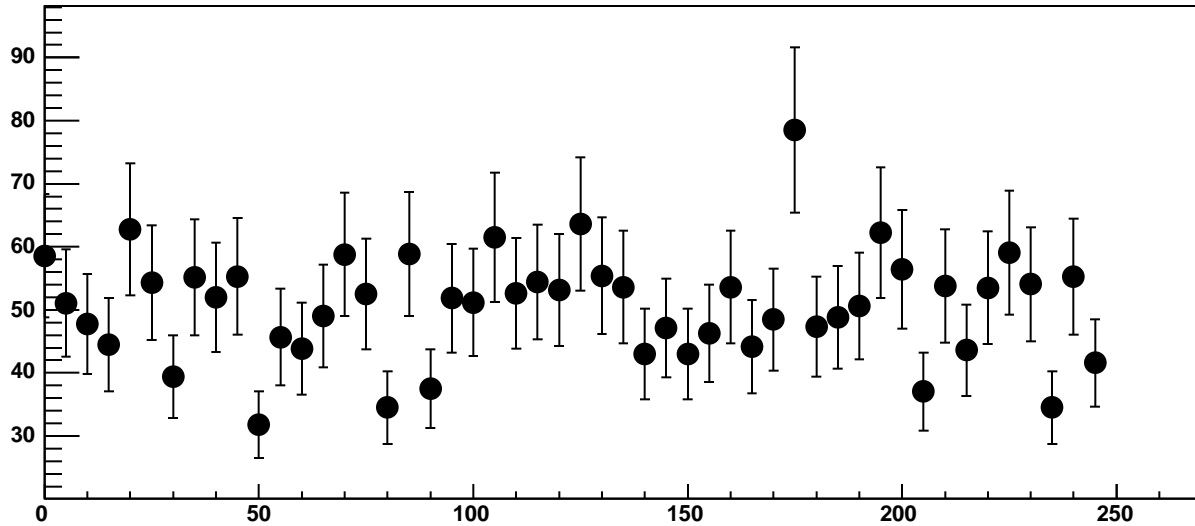


Chip 4, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

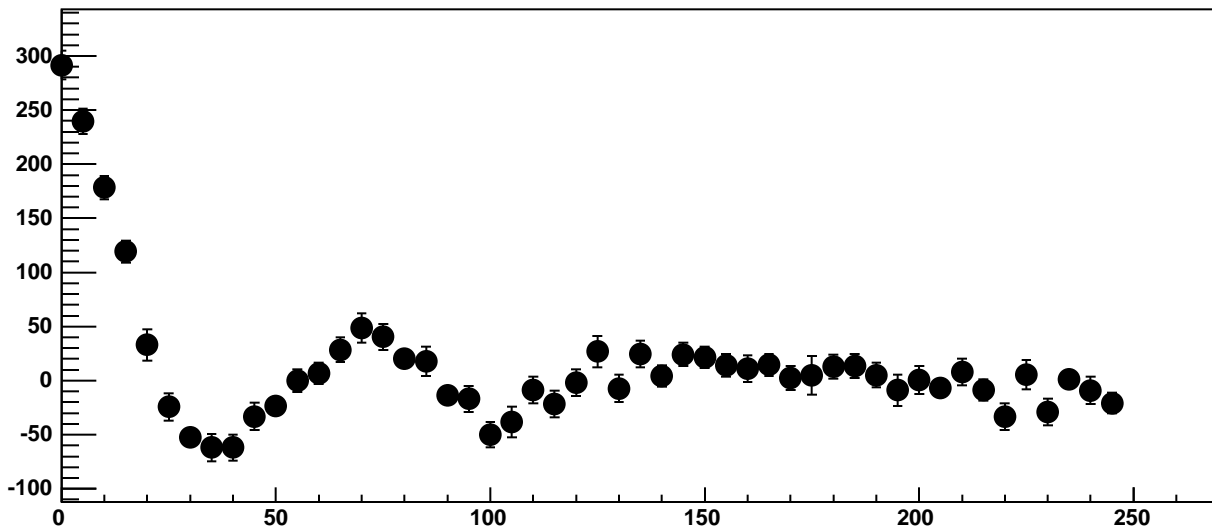


$\chi^2 / \text{ndf}$	361.4 / 41
p0	-269.1 ± 4.066
p1	98.46 ± 0.6204
p2	-3.626e+08 ± 7.703e+06
p3	3.325e+07 ± 5.65e+05
p4	9.973 ± 0.1068

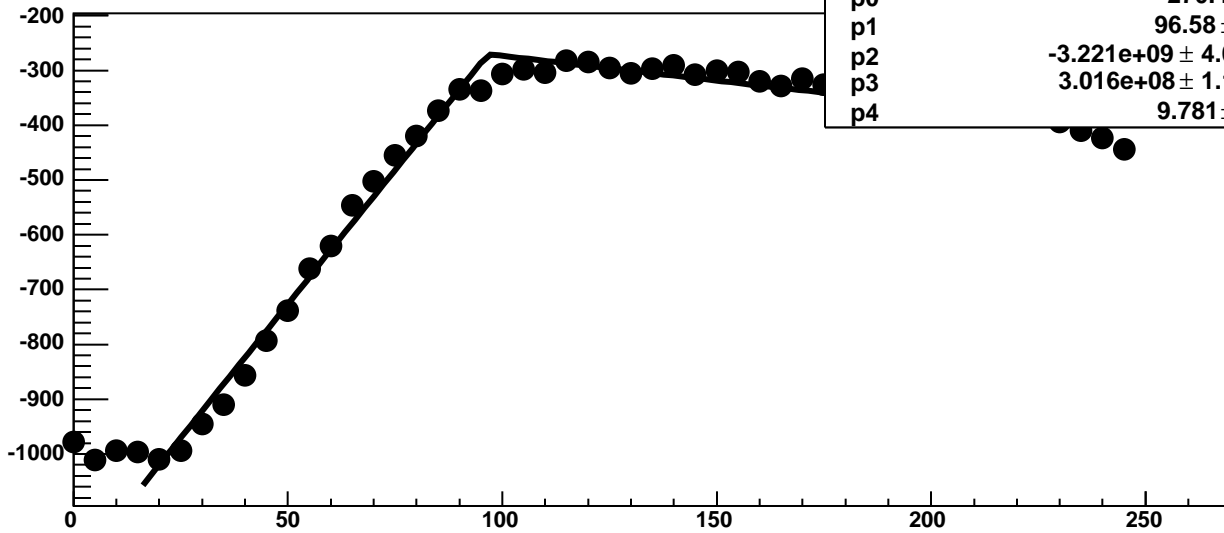
Chip 4, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

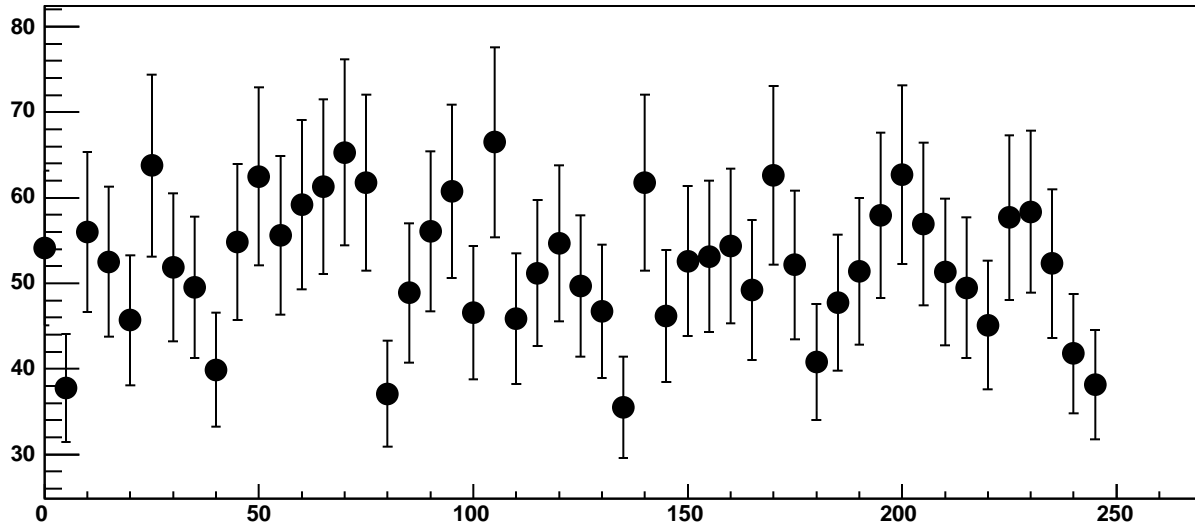


Chip 4, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold

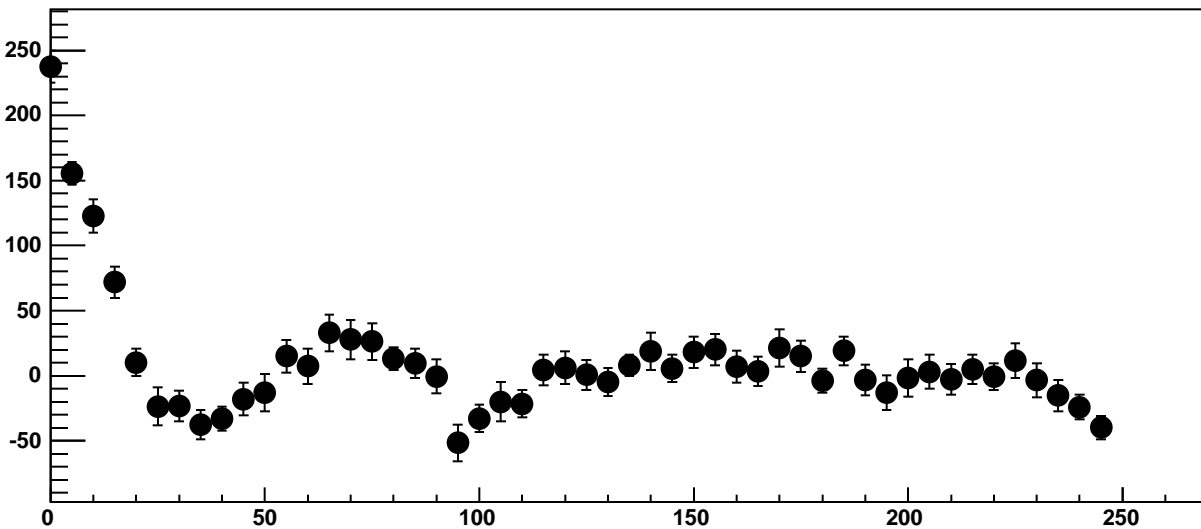


$\chi^2 / \text{ndf}$	141.9 / 41
p0	-270.4 ± 3.919
p1	96.58 ± 0.6522
p2	-3.221e+09 ± 4.026e+07
p3	3.016e+08 ± 1.133e+06
p4	9.781 ± 0.1163

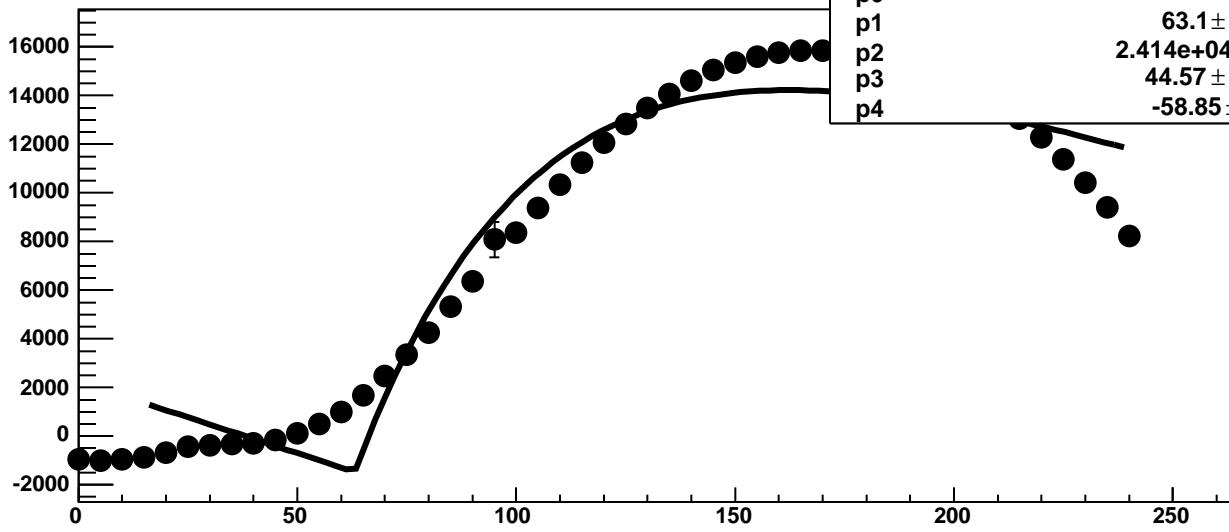
Chip 4, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



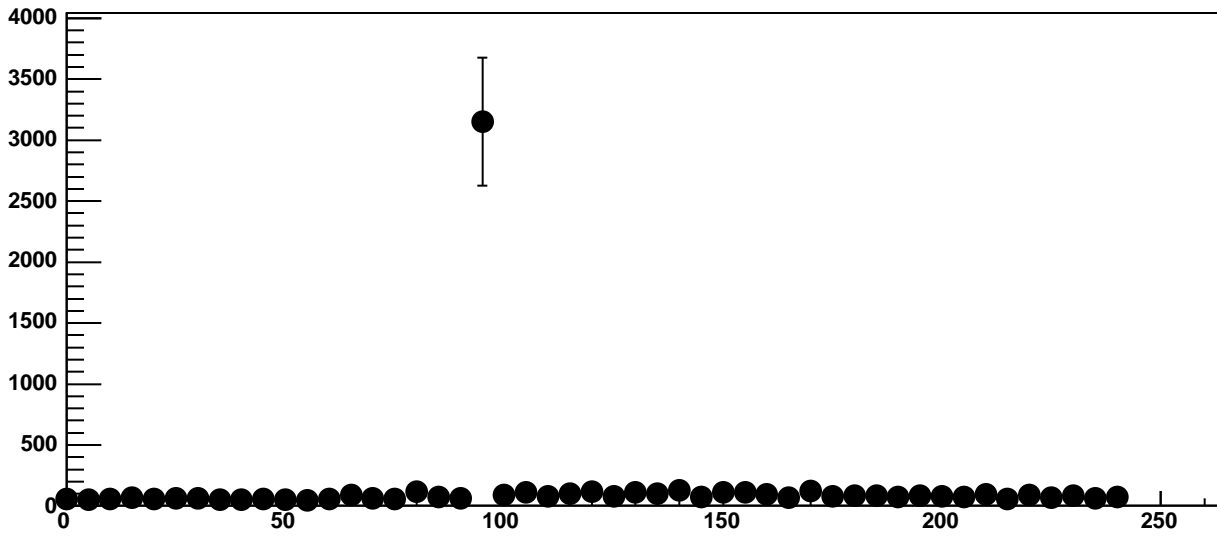
Chip 4, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold



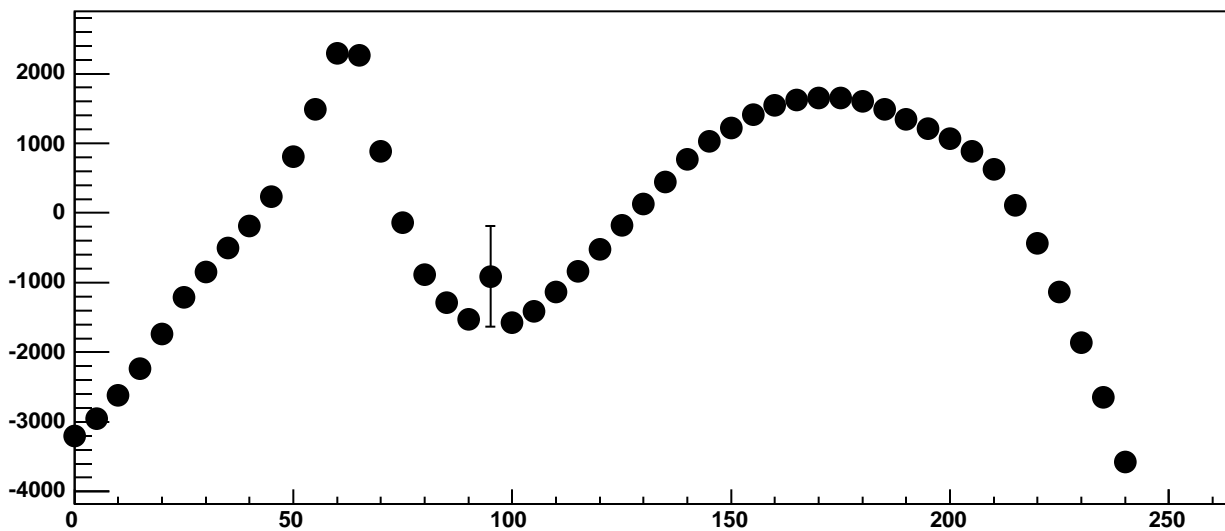
Chip 4, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold



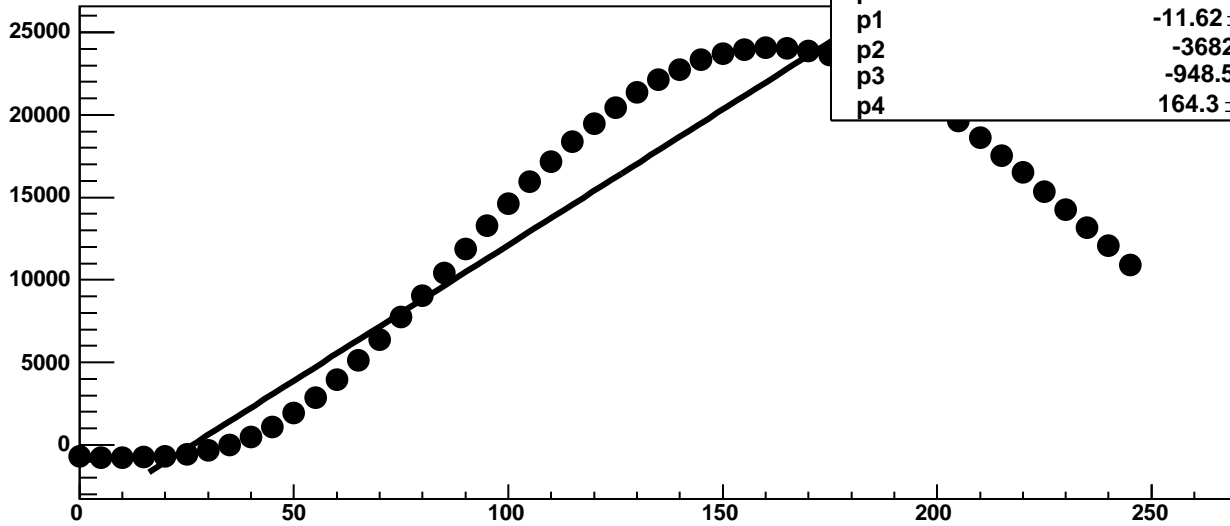
Chip 4, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

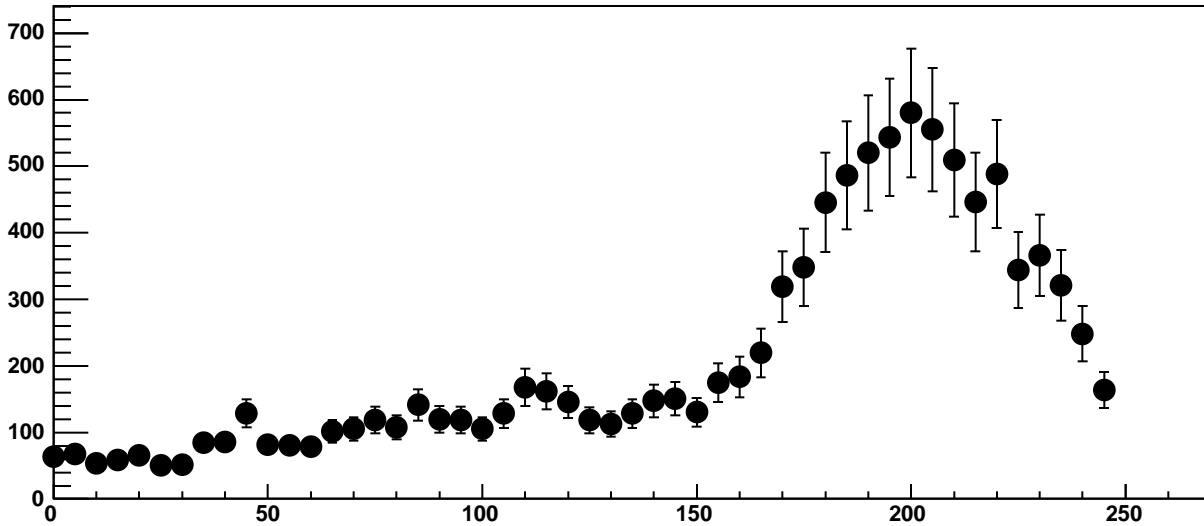


Chip 4, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

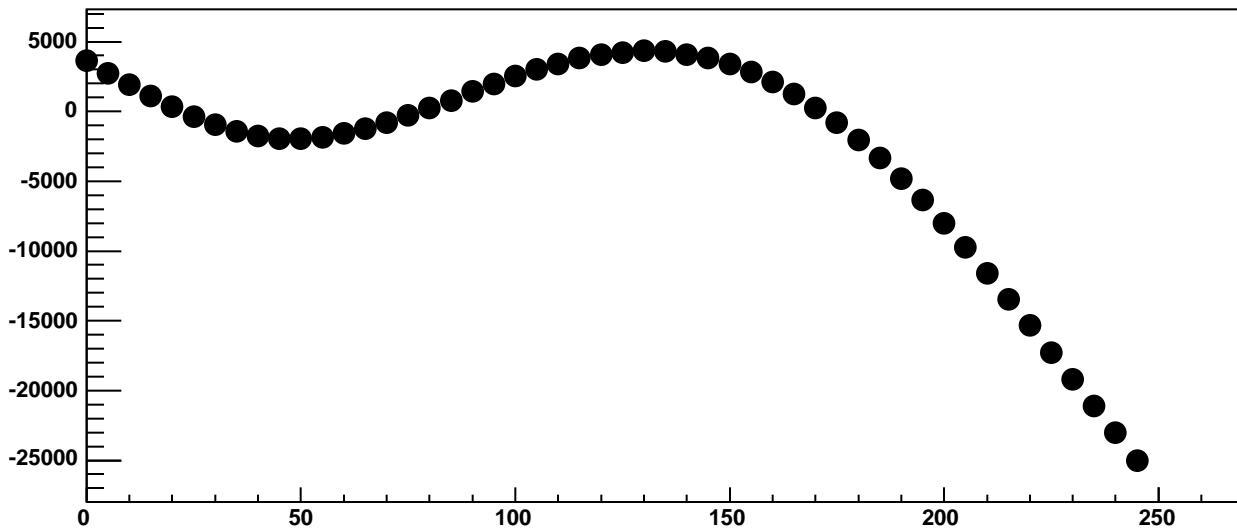


$\chi^2 / \text{ndf}$	6.574e+05 / 41
p0	-2549 ± 22.2
p1	-11.62 ± 0.1303
p2	-3682 ± 25.88
p3	-948.5 ± 34.17
p4	164.3 ± 0.1575

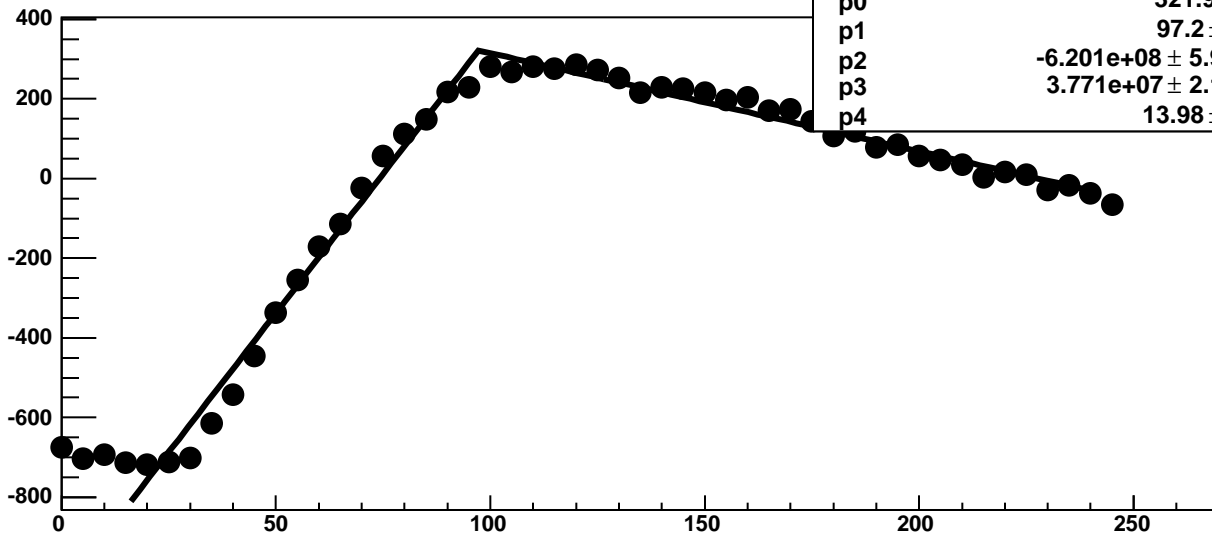
Chip 4, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

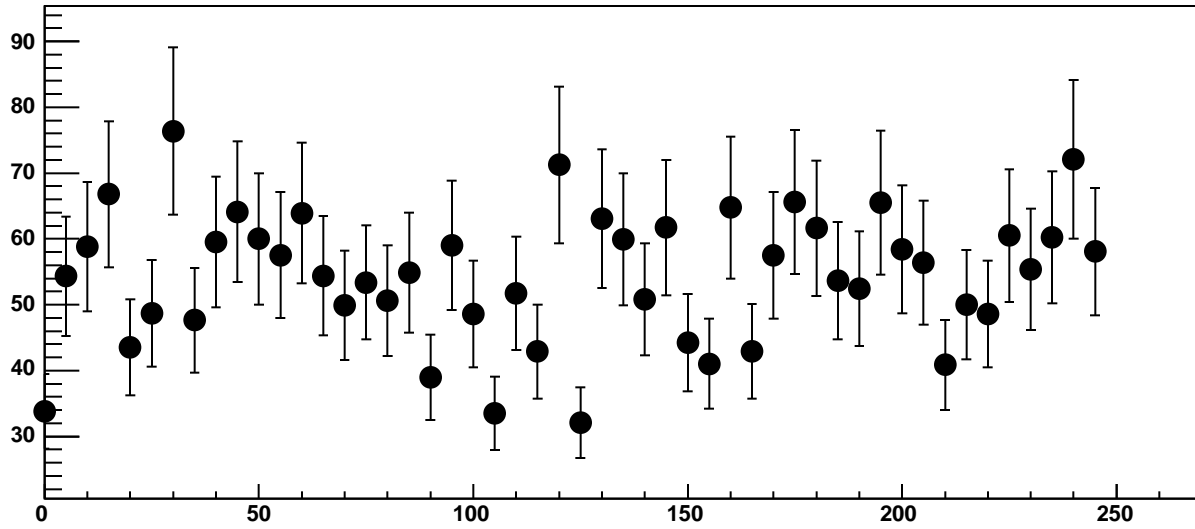


Chip 4, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold

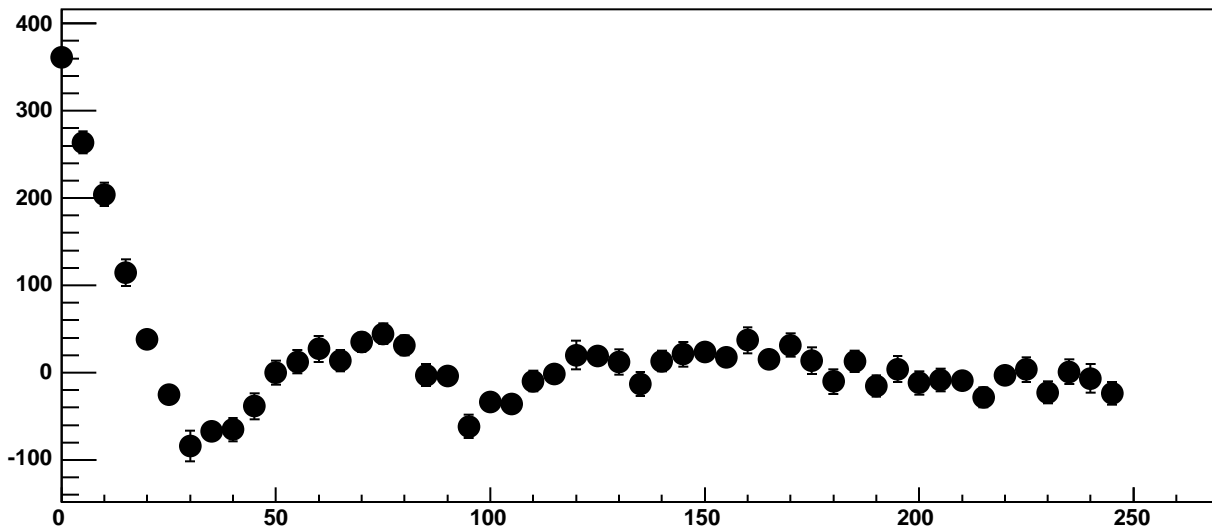


$\chi^2 / \text{ndf}$	306.6 / 41
p0	$321.9 \pm 3.473$
p1	$97.2 \pm 0.4179$
p2	$-6.201\text{e}+08 \pm 5.954\text{e}+06$
p3	$3.771\text{e}+07 \pm 2.119\text{e}+05$
p4	$13.98 \pm 0.1172$

Chip 4, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

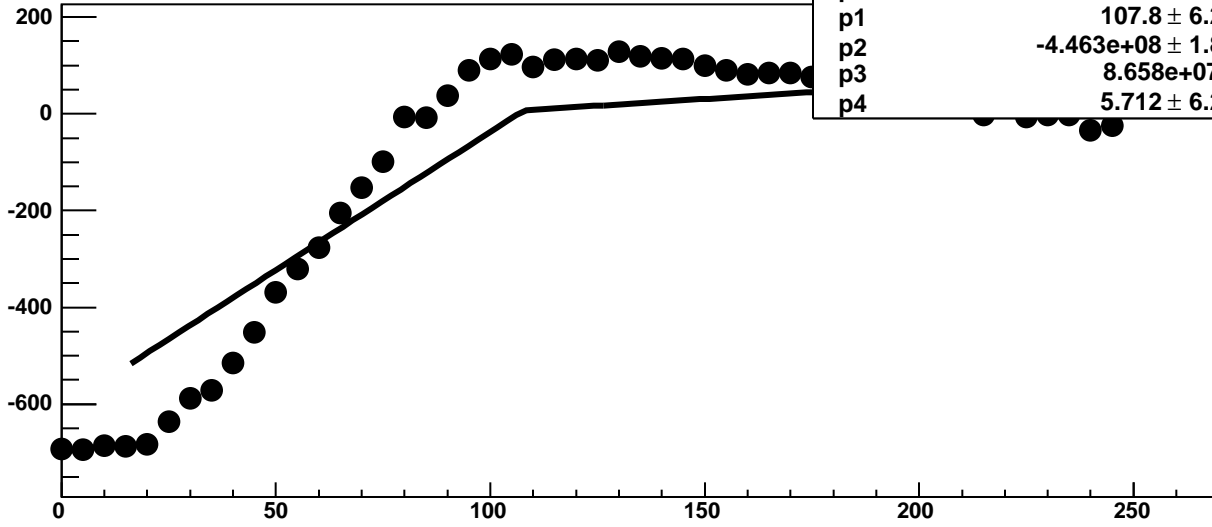


Chip 4, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold



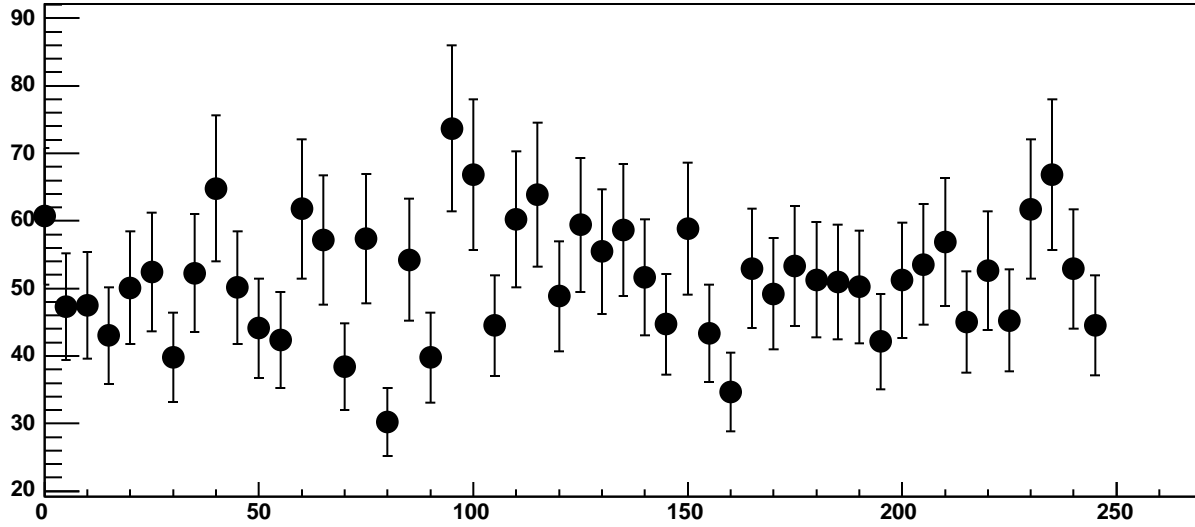


Chip 4, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

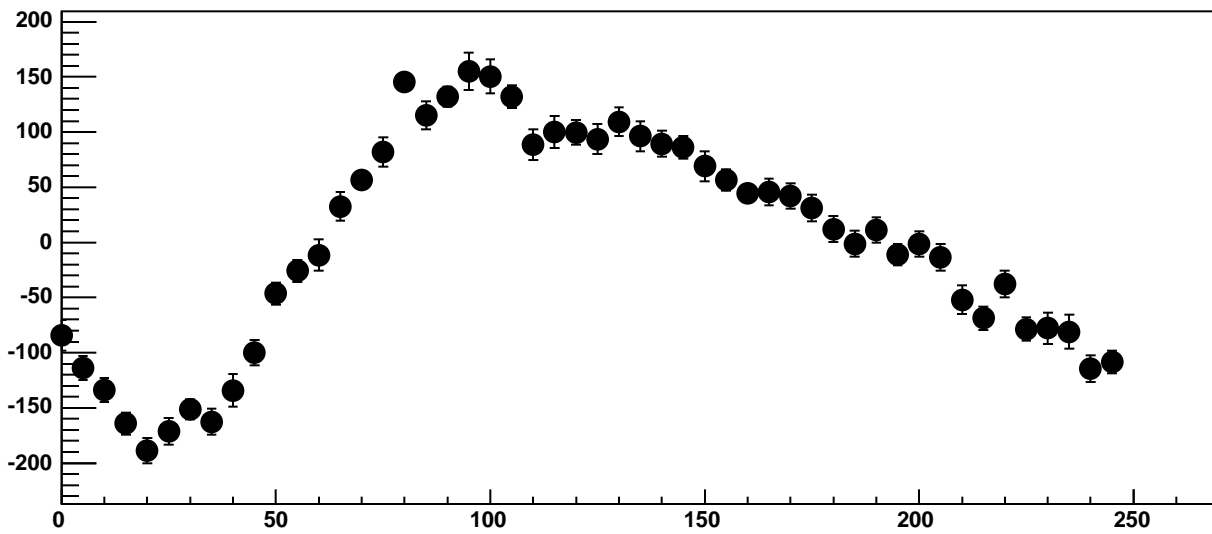


$\chi^2 / \text{ndf}$	3426 / 41
p0	$7.144 \pm 6.294\text{e}+08$
p1	$107.8 \pm 6.294\text{e}+08$
p2	$-4.463\text{e}+08 \pm 1.891\text{e}+09$
p3	$8.658\text{e}+07 \pm 710.1$
p4	$5.712 \pm 6.294\text{e}+08$

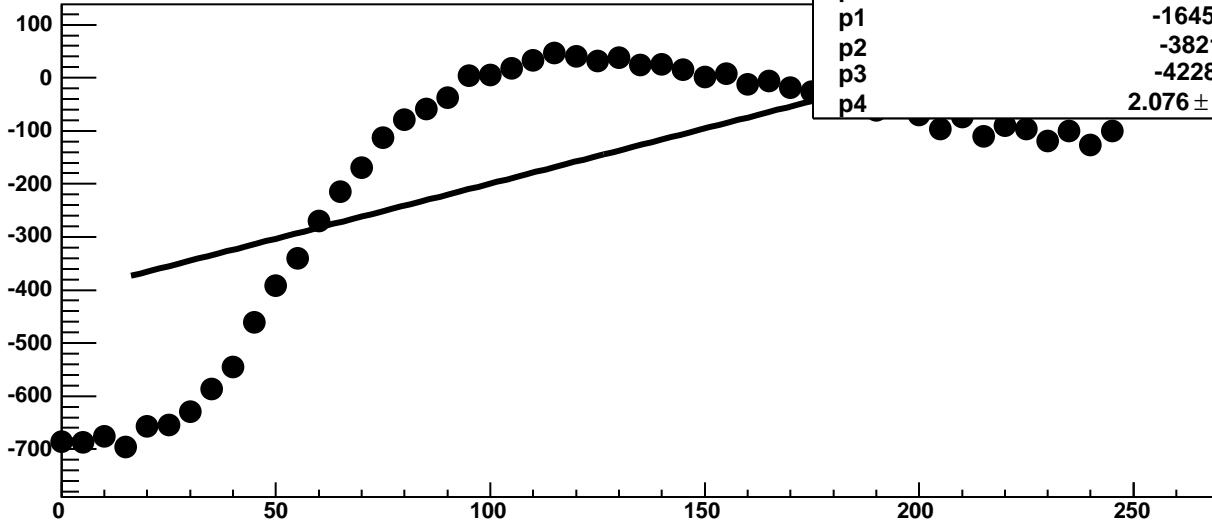
Chip 4, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

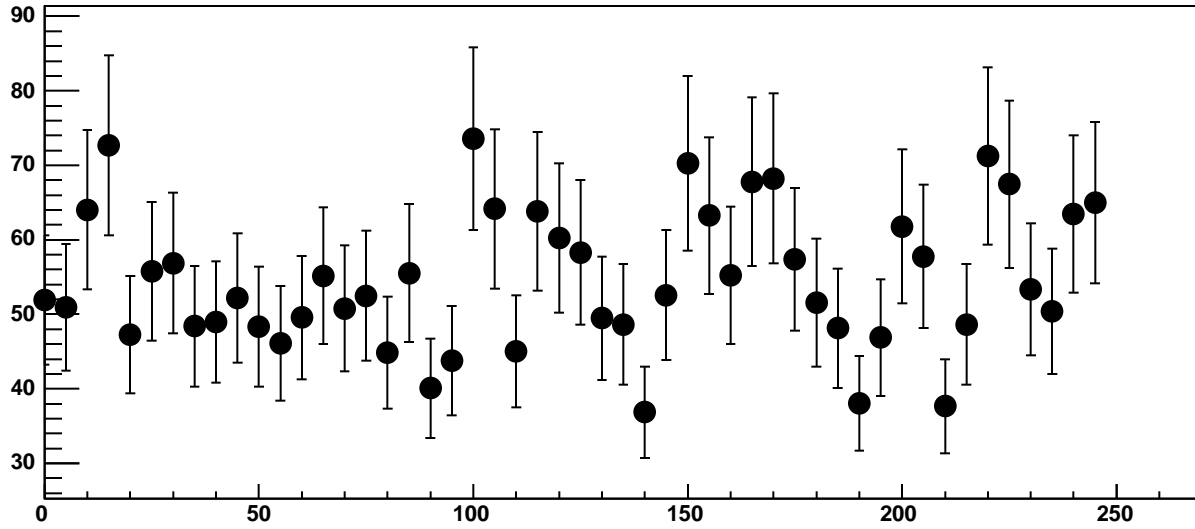


Chip 4, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

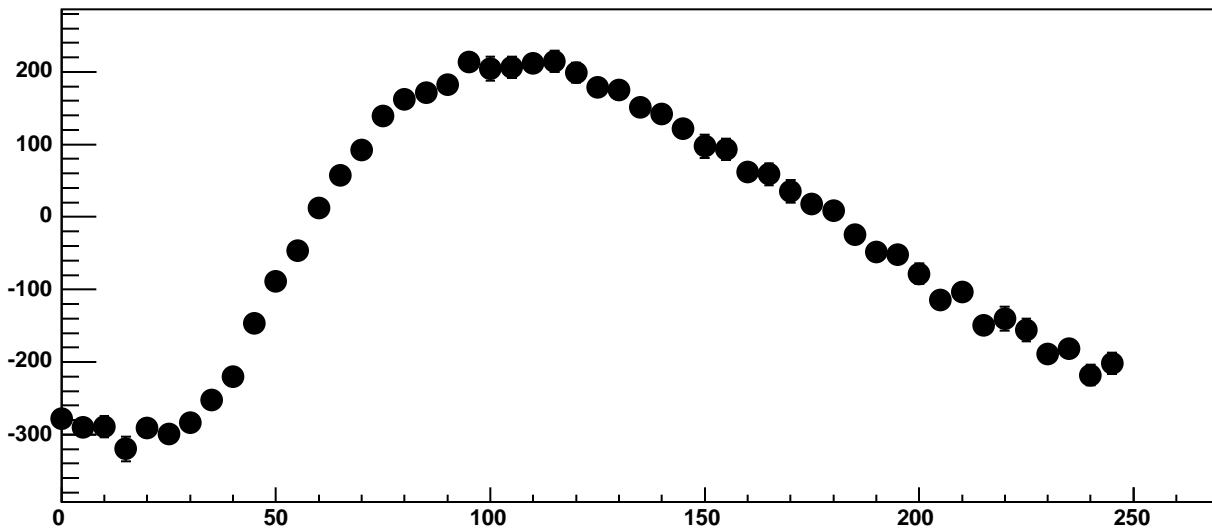


$\chi^2 / \text{ndf}$	8406 / 41
p0	-0.8042 ± 4.301
p1	-1645 ± 1.169
p2	-3821 ± 44.21
p3	-4228 ± 62.67
p4	2.076 ± 0.02682

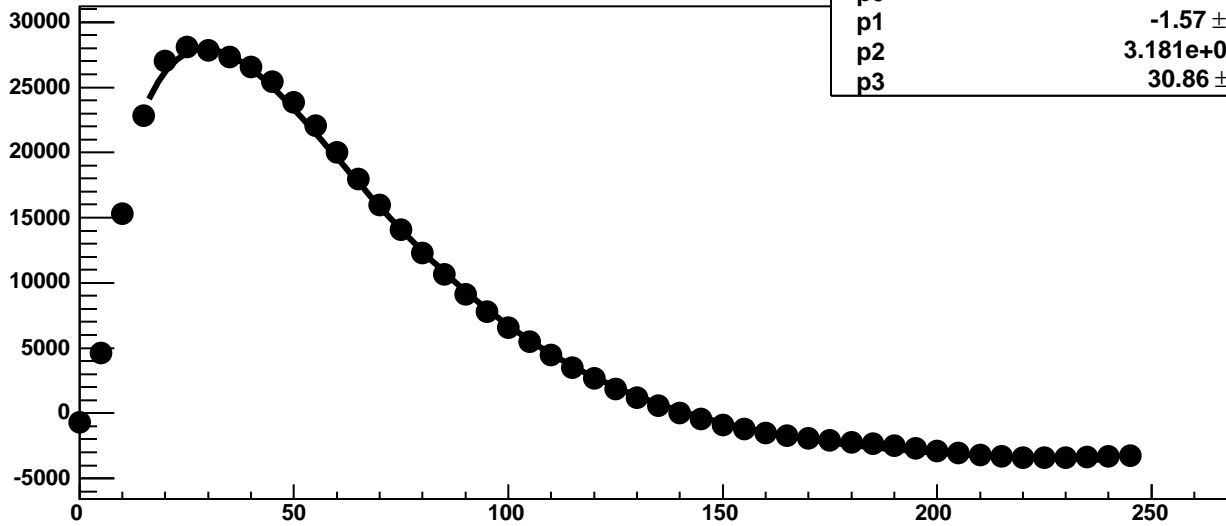
Chip 4, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

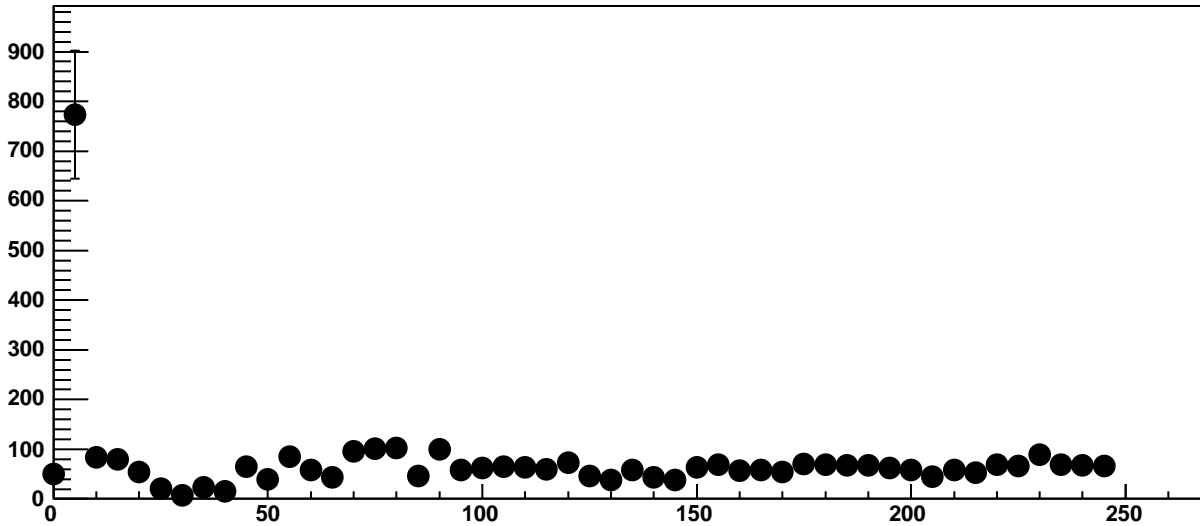


Chip 4, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

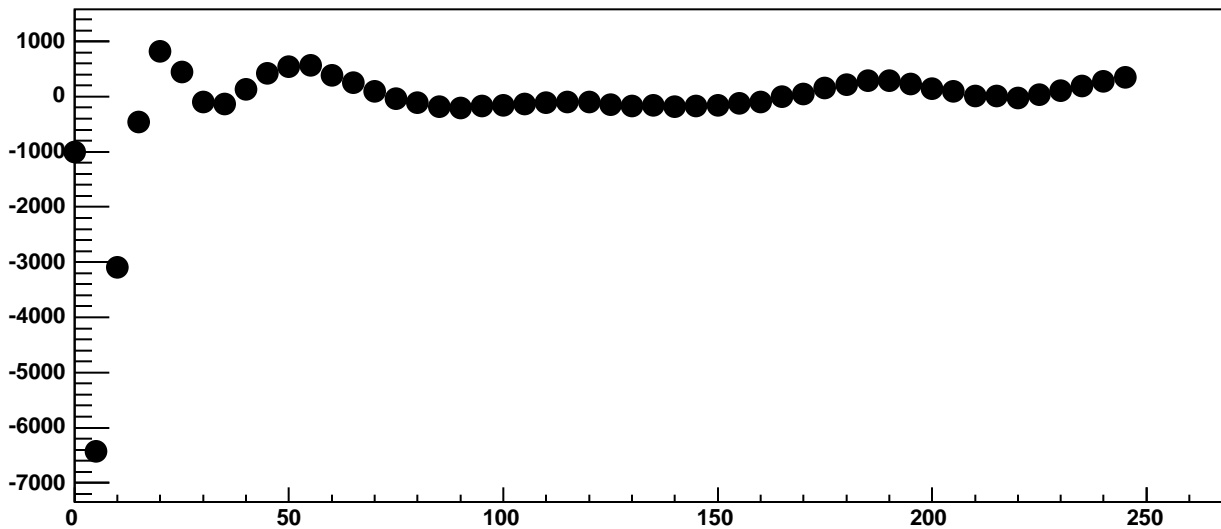


$\chi^2 / \text{ndf}$	3.038e+04 / 42
p0	-3852 ± 4.156
p1	-1.57 ± 0.01773
p2	3.181e+04 ± 4.29
p3	30.86 ± 0.01091

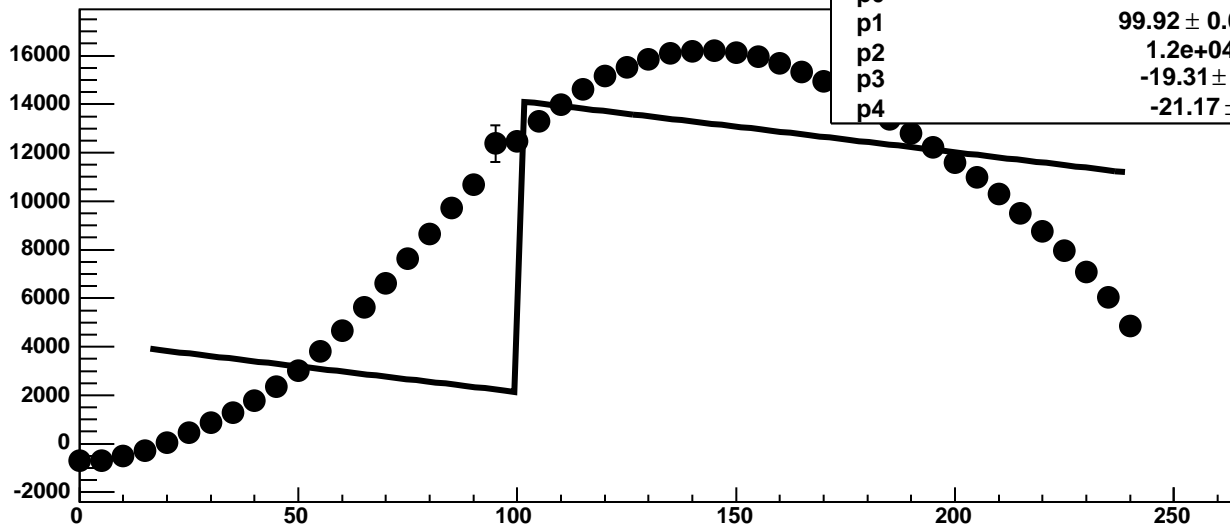
Chip 4, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

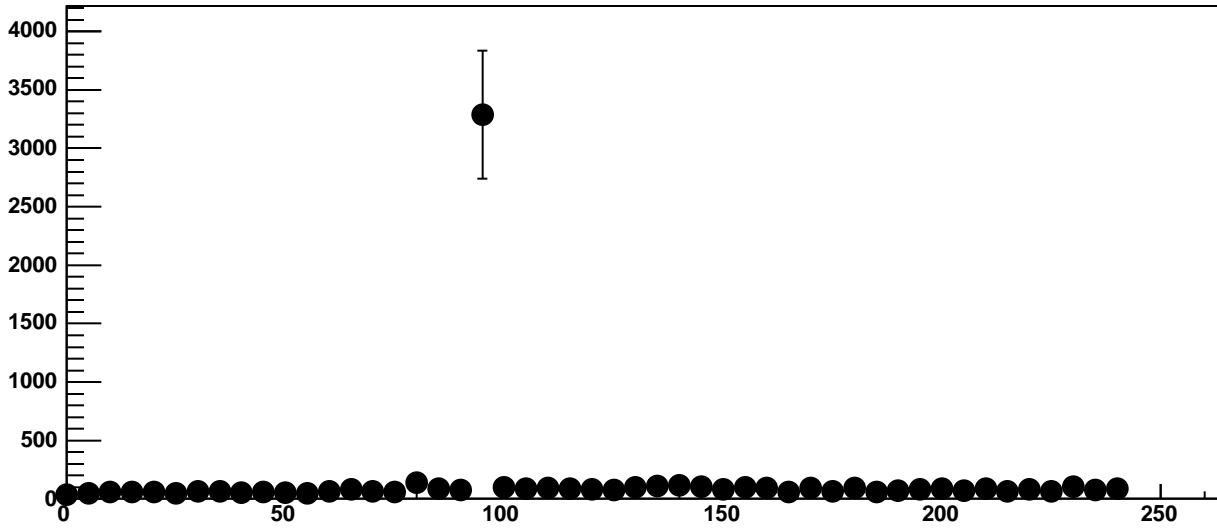


Chip 4, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

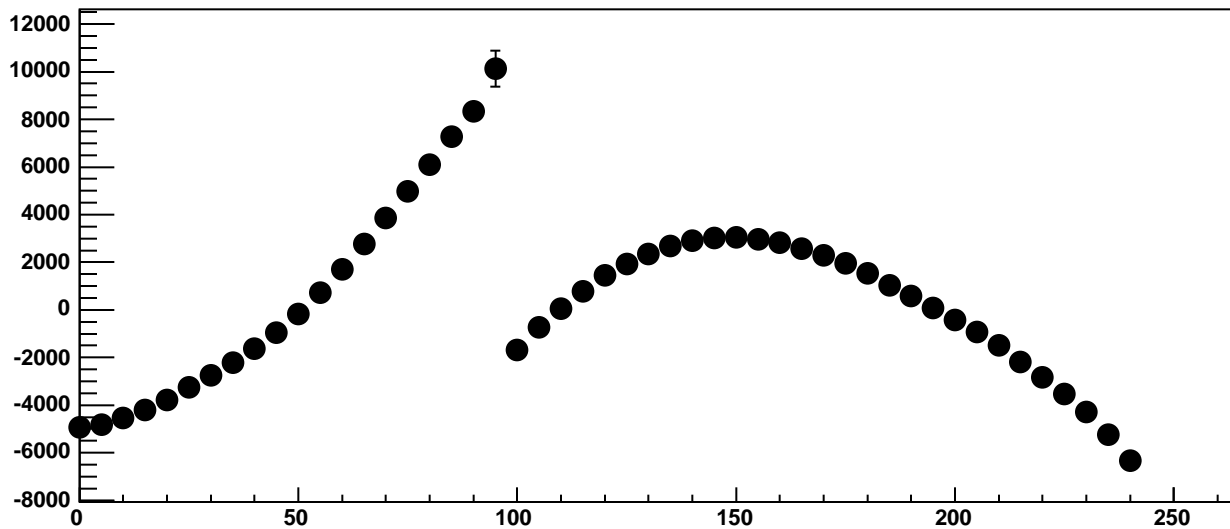


$\chi^2 / \text{ndf}$	1.499e+06 / 41
p0	2134 ± 5.284
p1	99.92 ± 0.0003739
p2	1.2e+04 ± 11.34
p3	-19.31 ± 0.02012
p4	-21.17 ± 0.0754

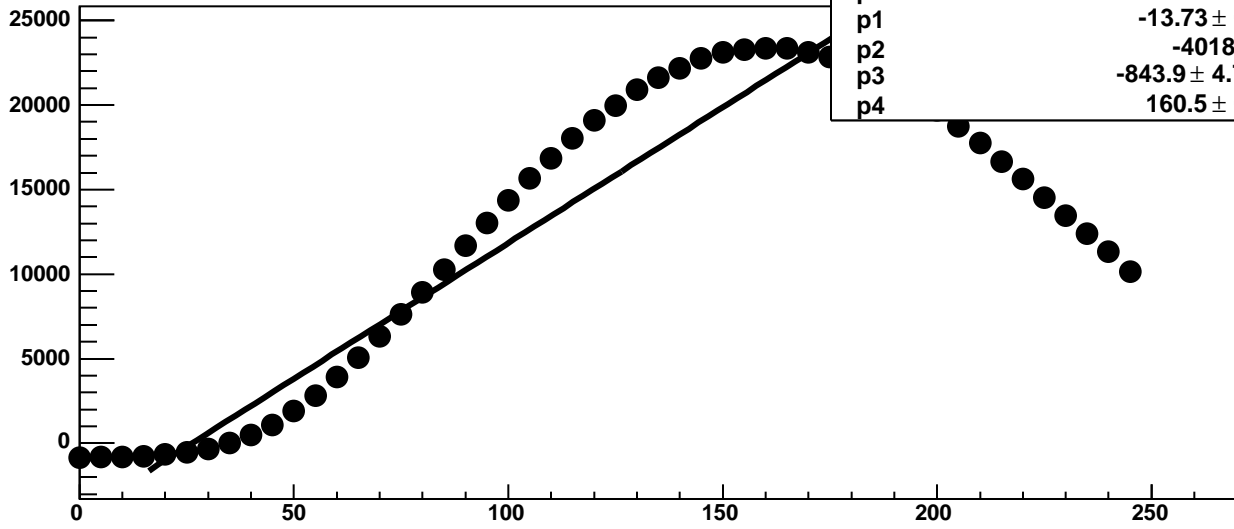
Chip 4, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold

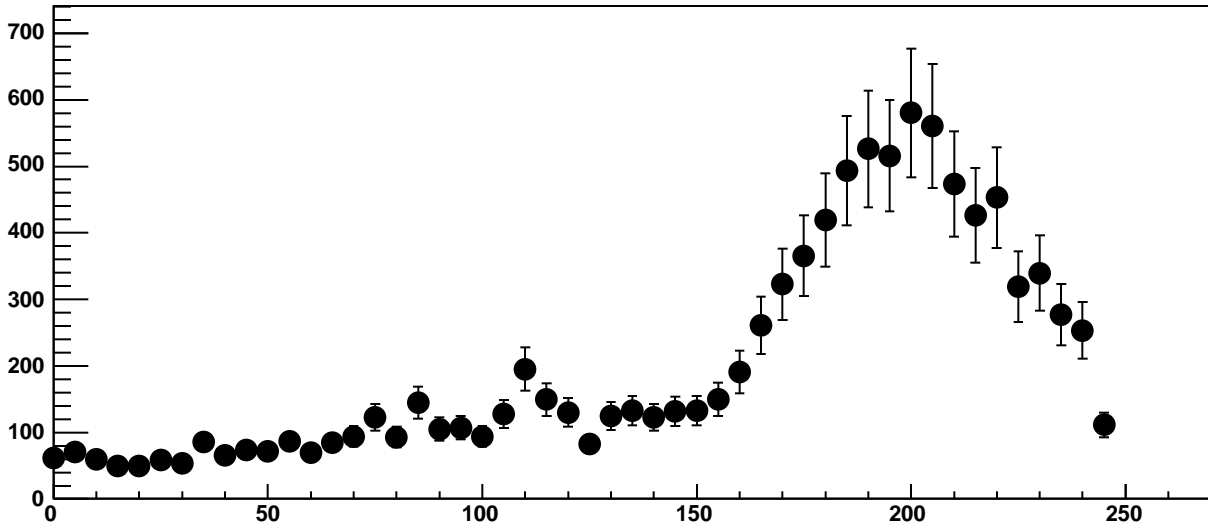


Chip 4, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

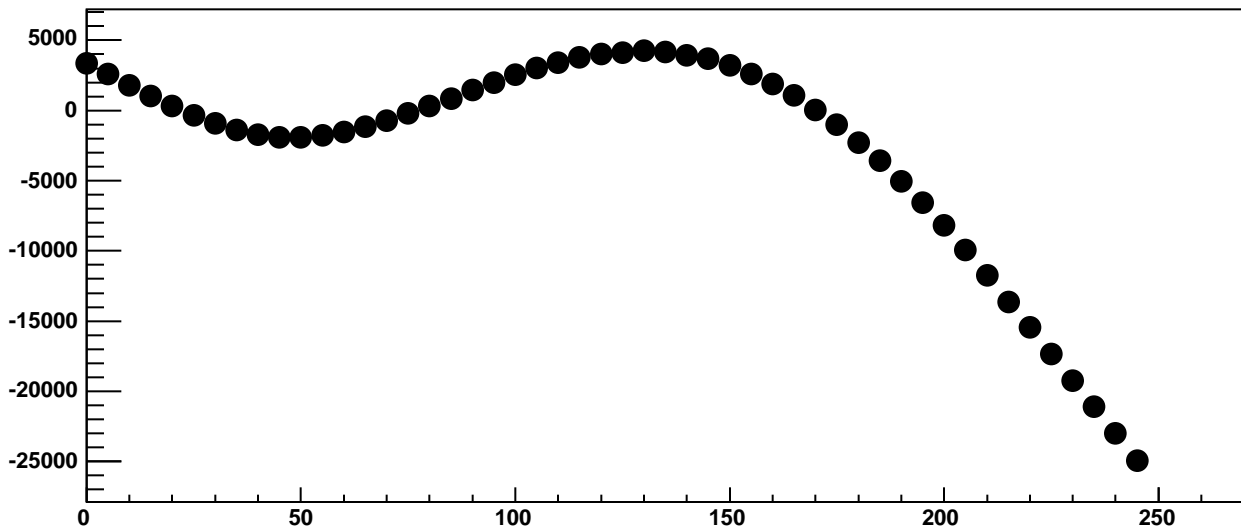


$\chi^2 / \text{ndf}$	7.473e+05 / 41
p0	-2391 ± 2.856
p1	-13.73 ± 0.03752
p2	-4018 ± 4.506
p3	-843.9 ± 4.725e-05
p4	160.5 ± 0.08636

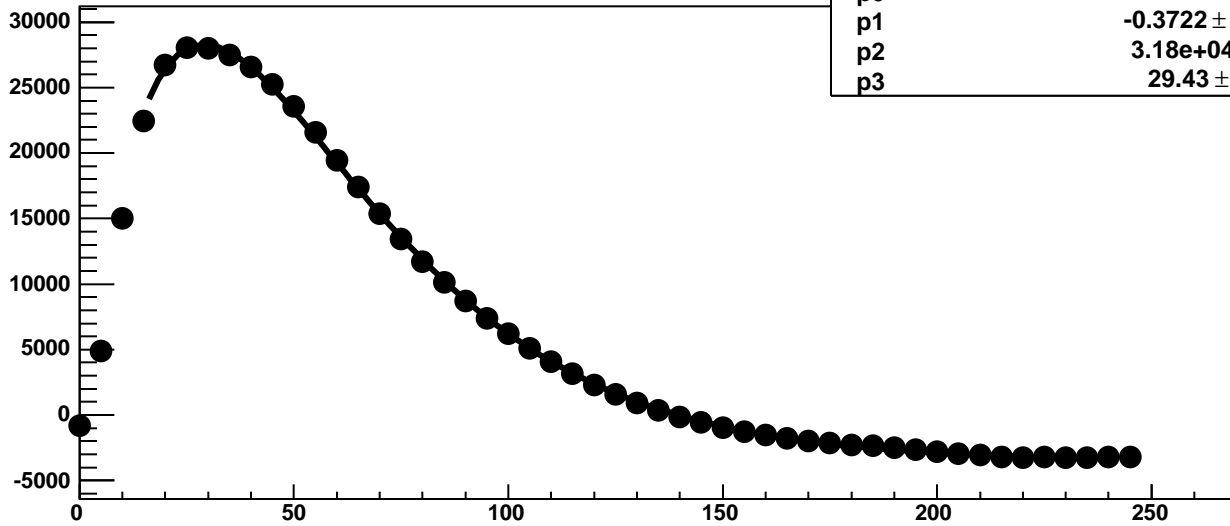
Chip 4, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

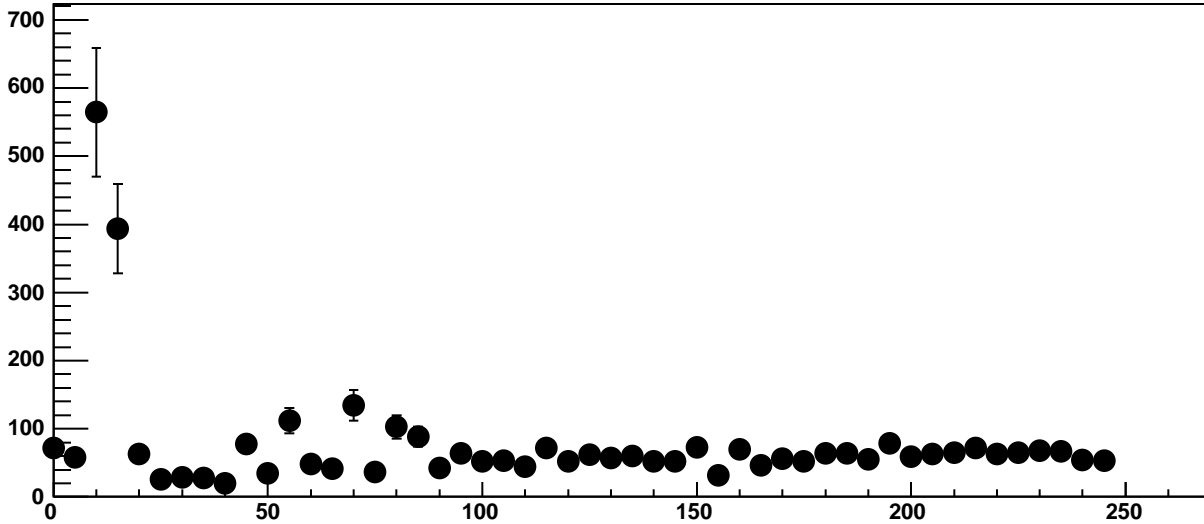


Chip 4, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold

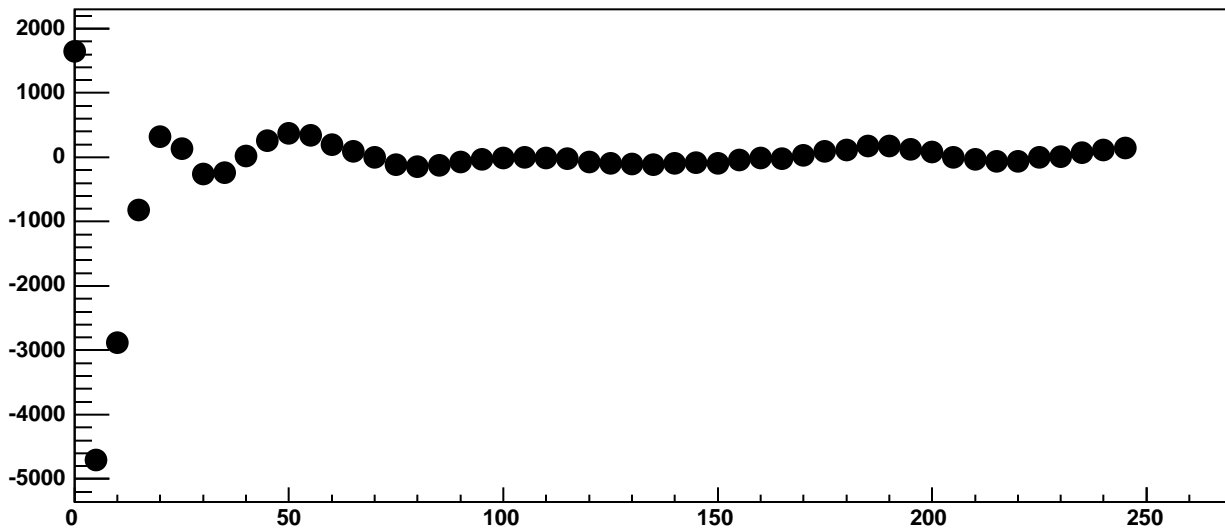


$\chi^2 / \text{ndf}$	8370 / 42
p0	$-3531 \pm 3.975$
p1	$-0.3722 \pm 0.02169$
p2	$3.18e+04 \pm 4.797$
p3	$29.43 \pm 0.01147$

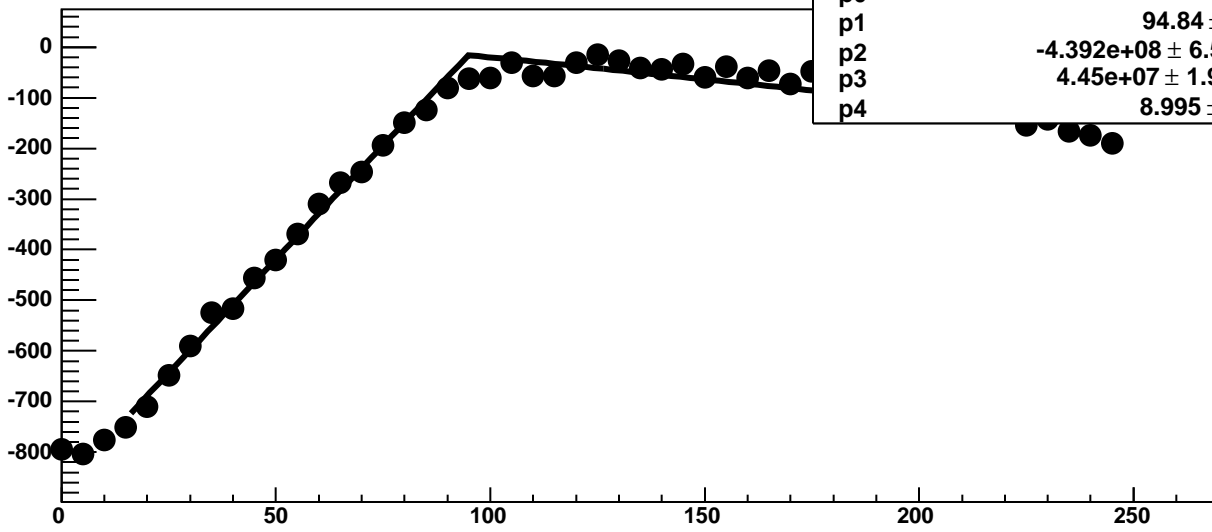
Chip 4, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

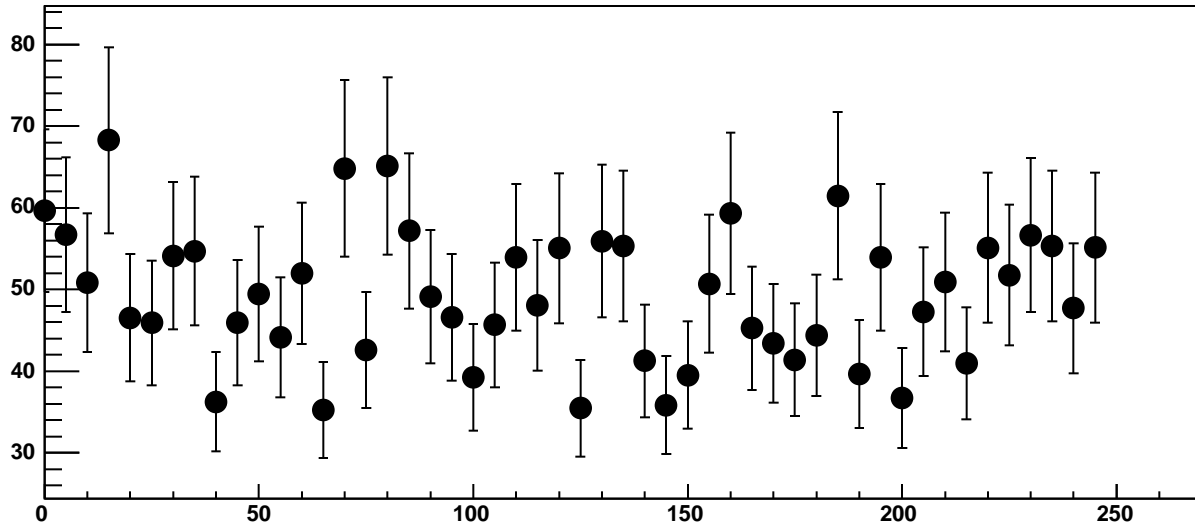


Chip 4, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

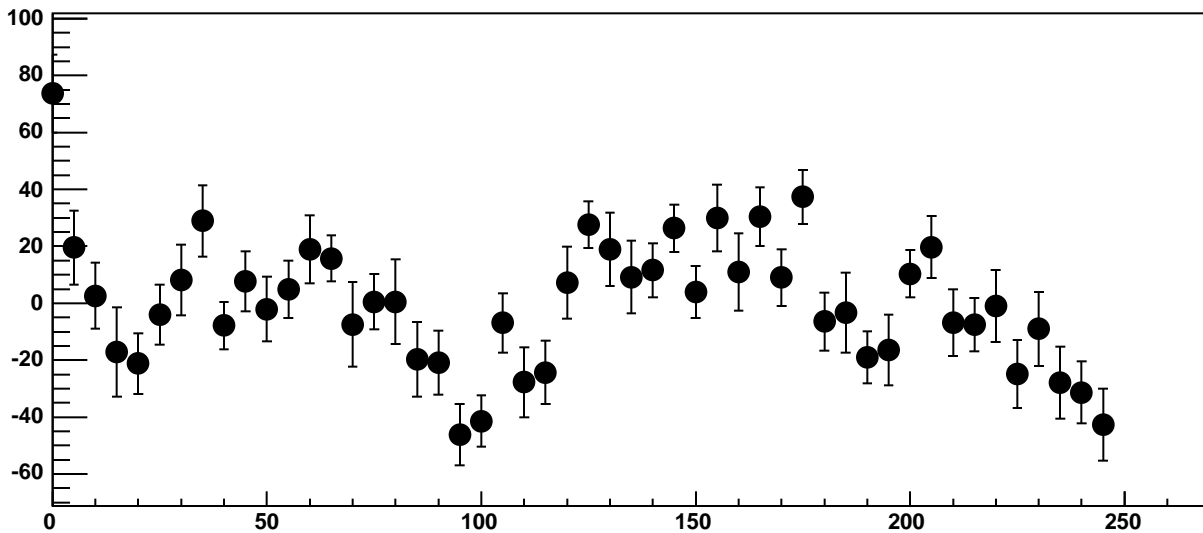


$\chi^2 / \text{ndf}$	164.1 / 41
p0	$-15.53 \pm 3.481$
p1	$94.84 \pm 0.7297$
p2	$-4.392\text{e}+08 \pm 6.545\text{e}+06$
p3	$4.45\text{e}+07 \pm 1.953\text{e}+05$
p4	$8.995 \pm 0.1295$

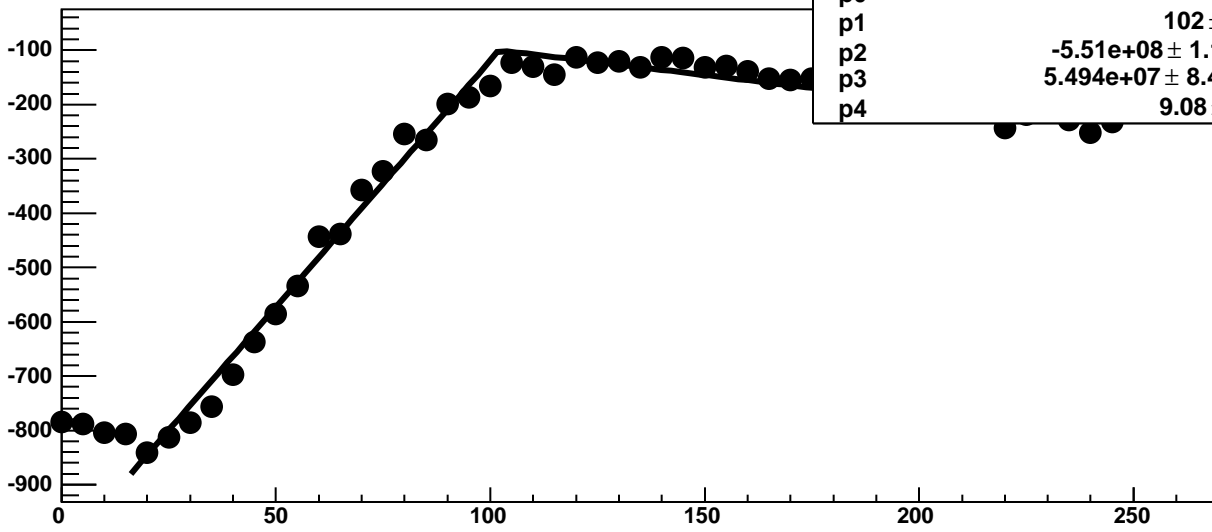
Chip 4, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

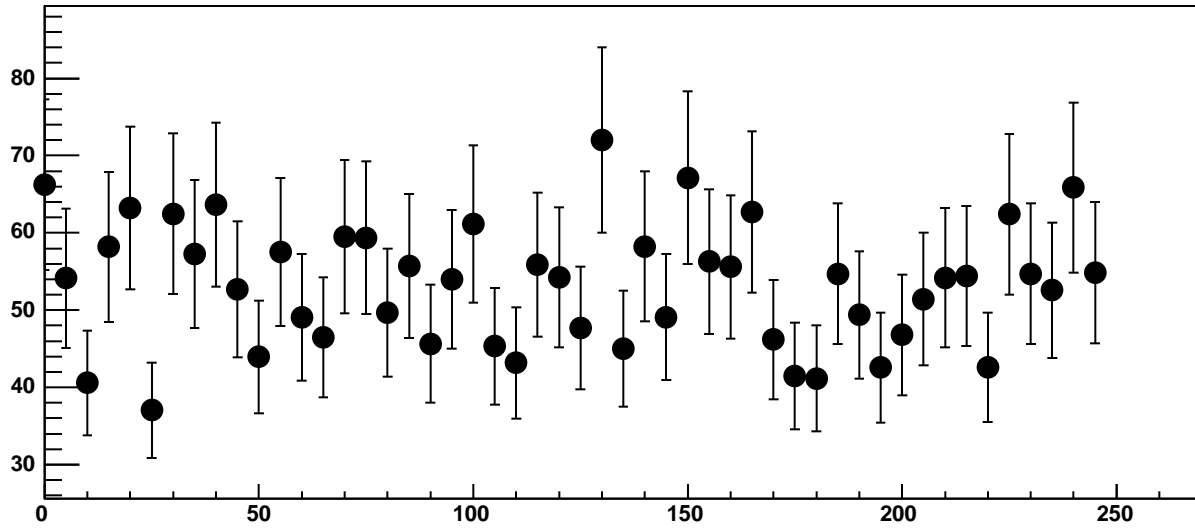


Chip 4, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

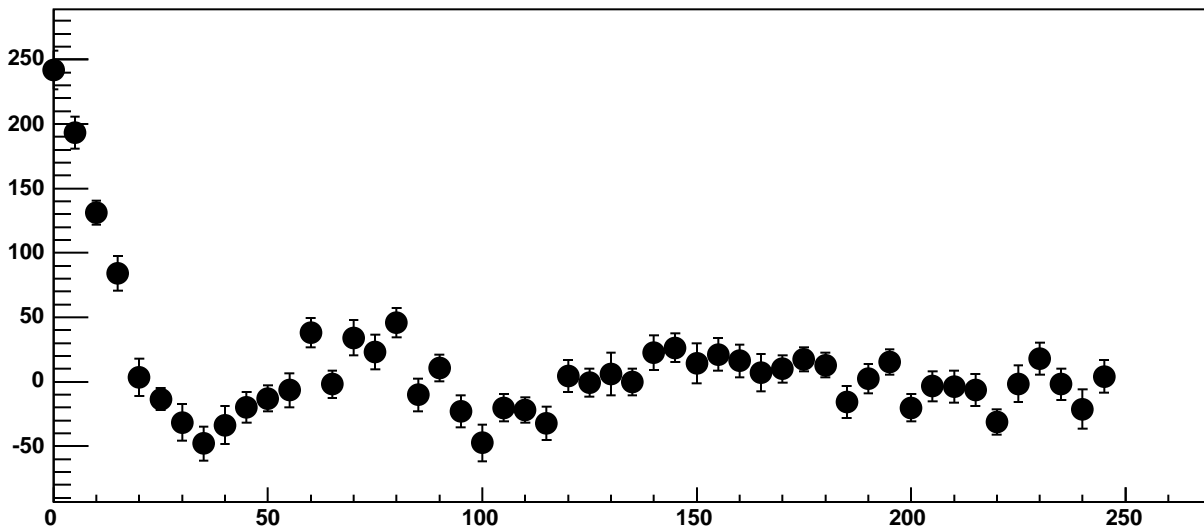


$\chi^2 / \text{ndf}$	181.4 / 41
p0	-100.1 ± 4.074
p1	102 ± 0.7289
p2	-5.51e+08 ± 1.136e+07
p3	5.494e+07 ± 8.475e+05
p4	9.08 ± 0.1116

Chip 4, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

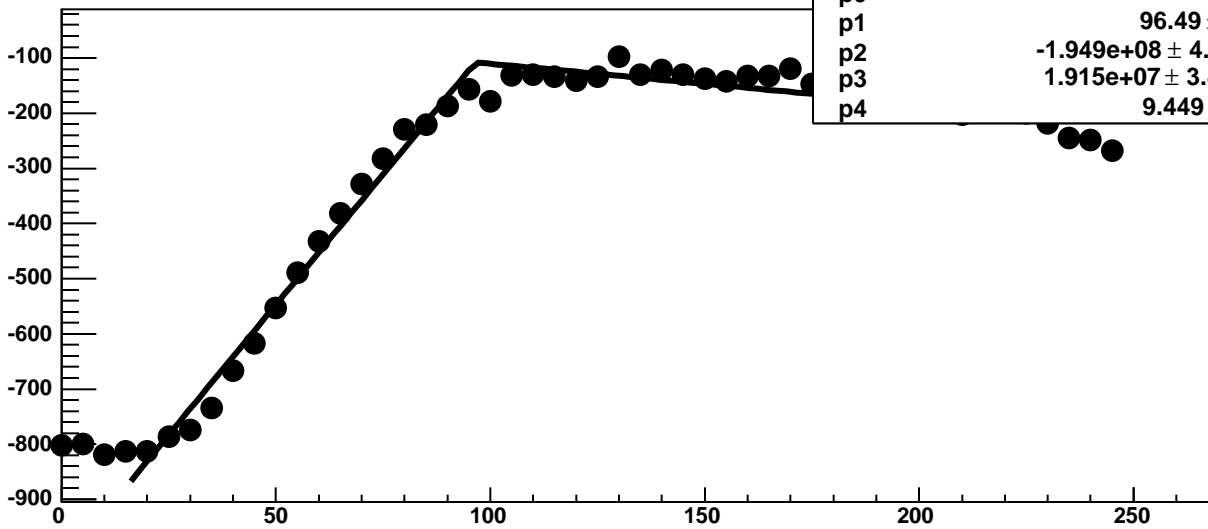


Chip 4, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold



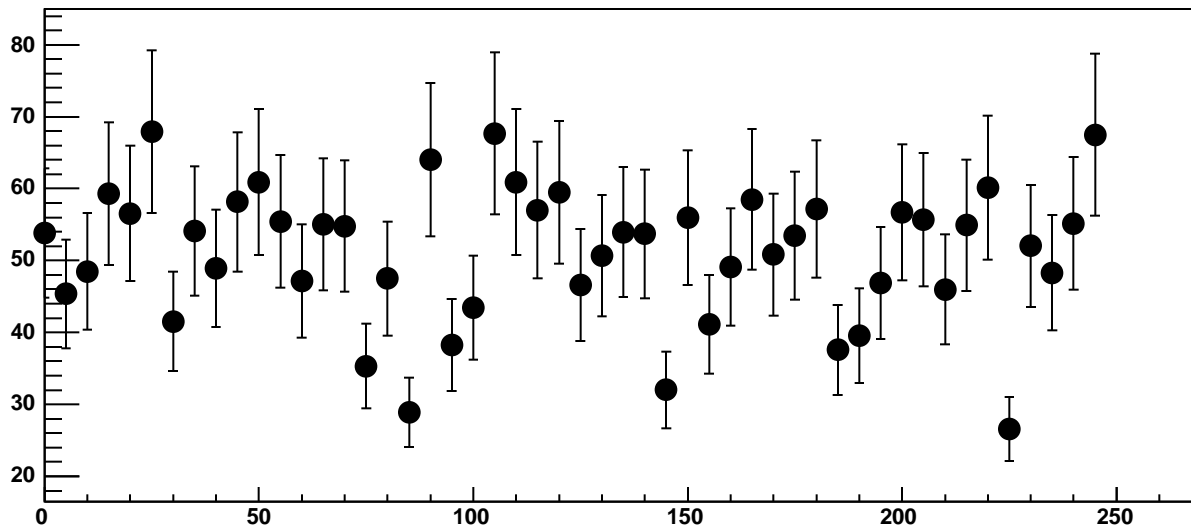


Chip 4, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold

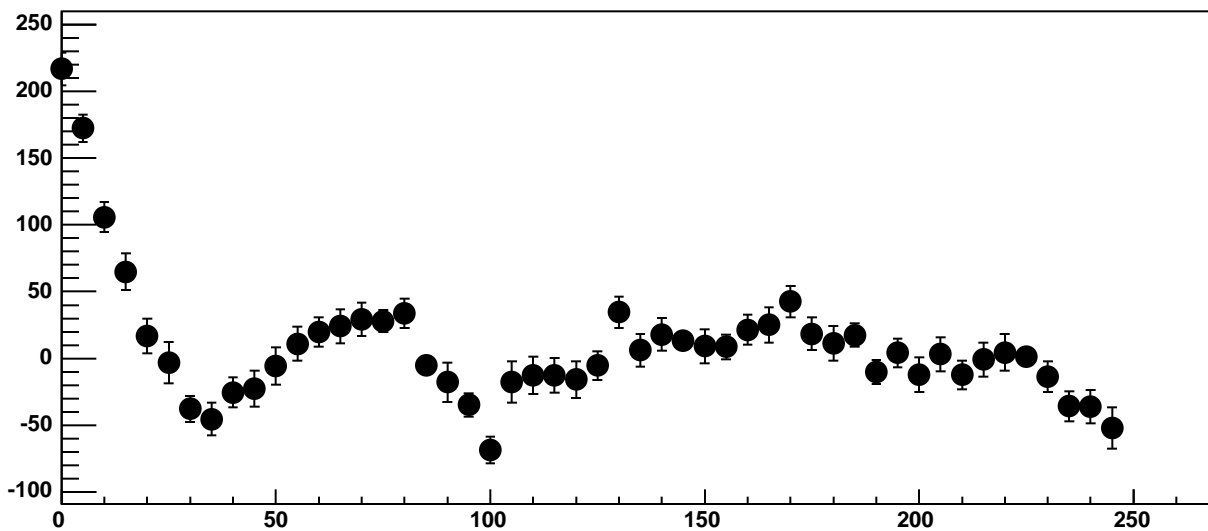


$\chi^2 / \text{ndf}$	233.1 / 41
p0	$-107.7 \pm 4.052$
p1	$96.49 \pm 0.6215$
p2	$-1.949\text{e}+08 \pm 4.448\text{e}+06$
p3	$1.915\text{e}+07 \pm 3.485\text{e}+05$
p4	$9.449 \pm 0.1078$

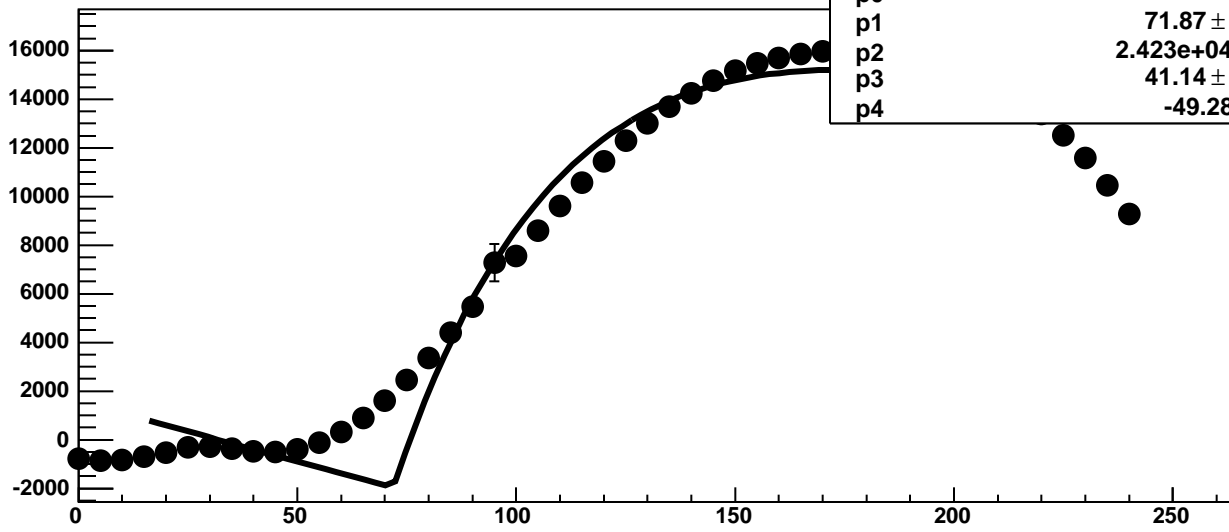
Chip 4, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold

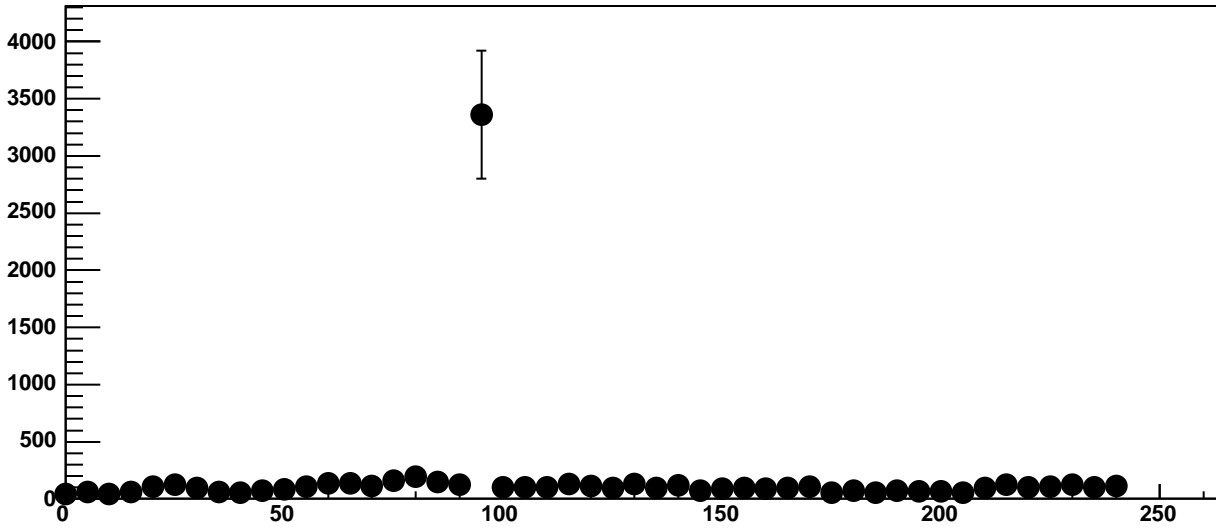


Chip 4, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

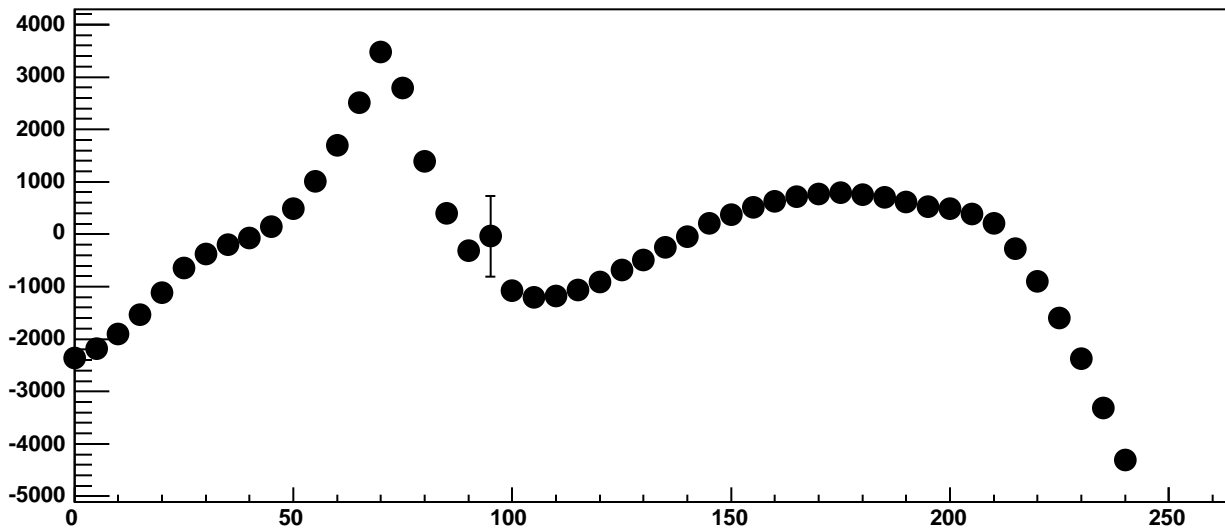


$\chi^2 / \text{ndf}$	1.407e+05 / 41
p0	-1969 ± 9.073
p1	71.87 ± 0.04642
p2	2.423e+04 ± 46.32
p3	41.14 ± 0.09786
p4	-49.28 ± 0.237

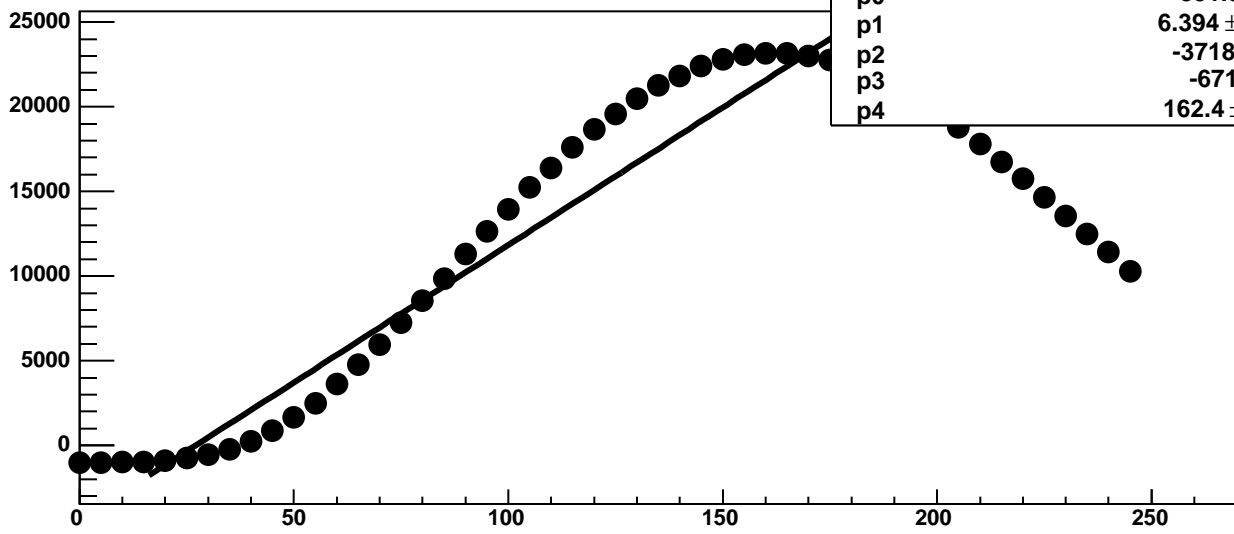
Chip 4, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

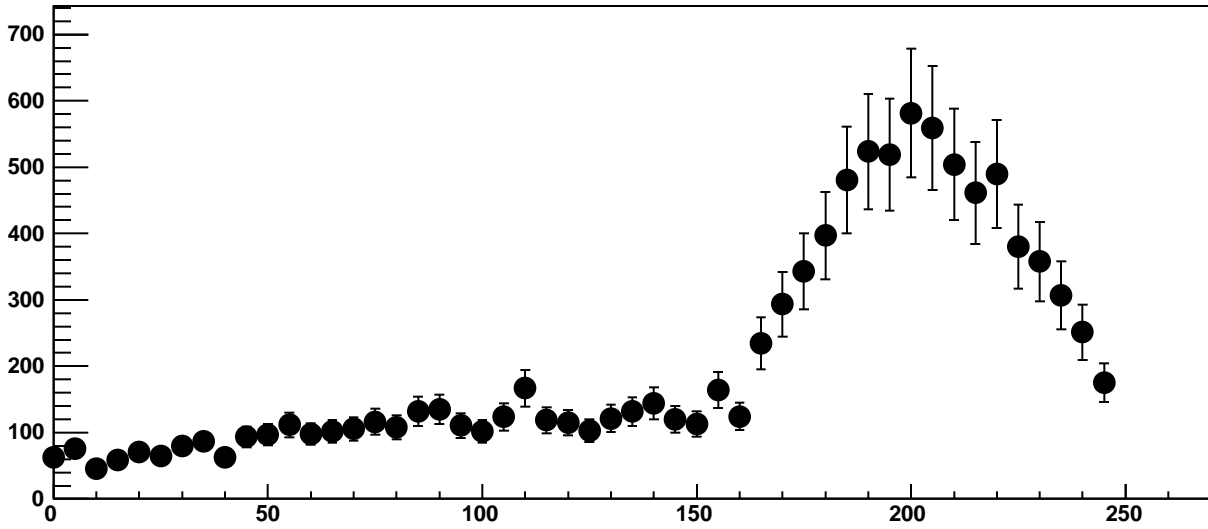


Chip 4, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

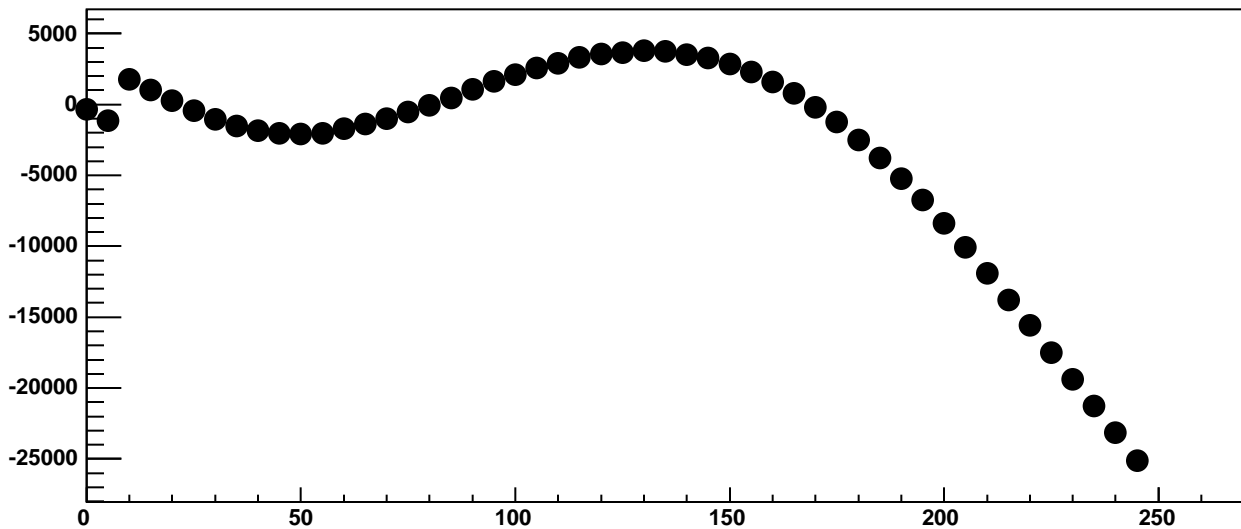


$\chi^2 / \text{ndf}$	6.436e+05 / 41
p0	351.3 ± 24.3
p1	6.394 ± 0.1415
p2	-3718 ± 26.87
p3	-671 ± 24.17
p4	162.4 ± 0.1571

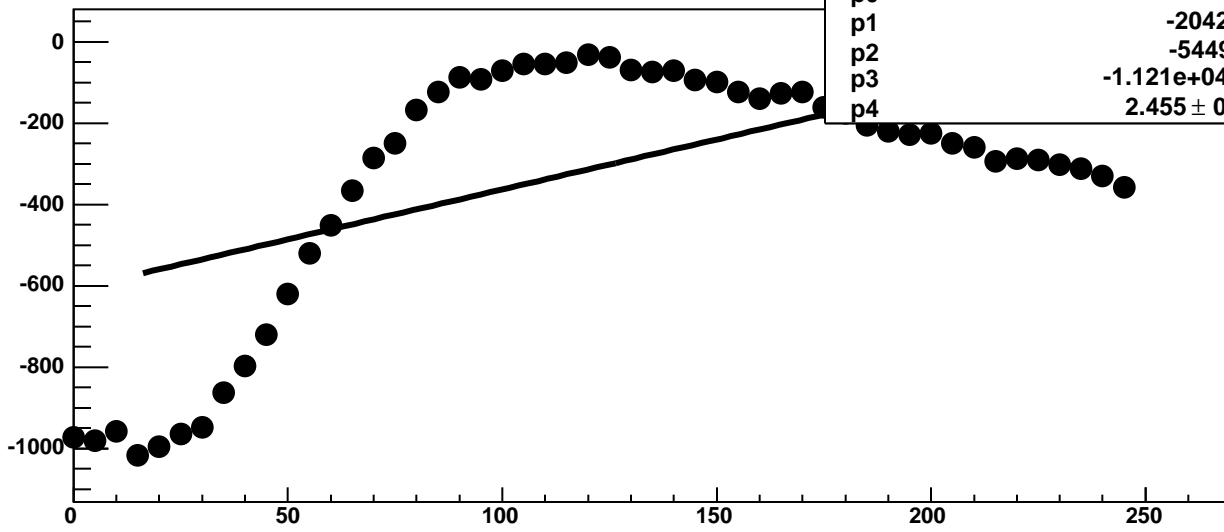
Chip 4, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

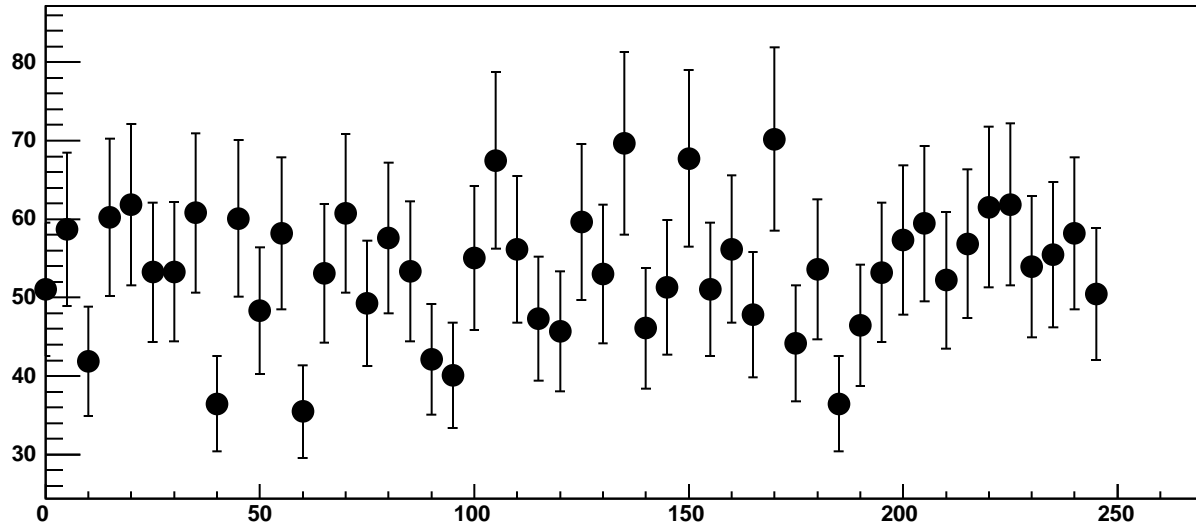


Chip 4, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

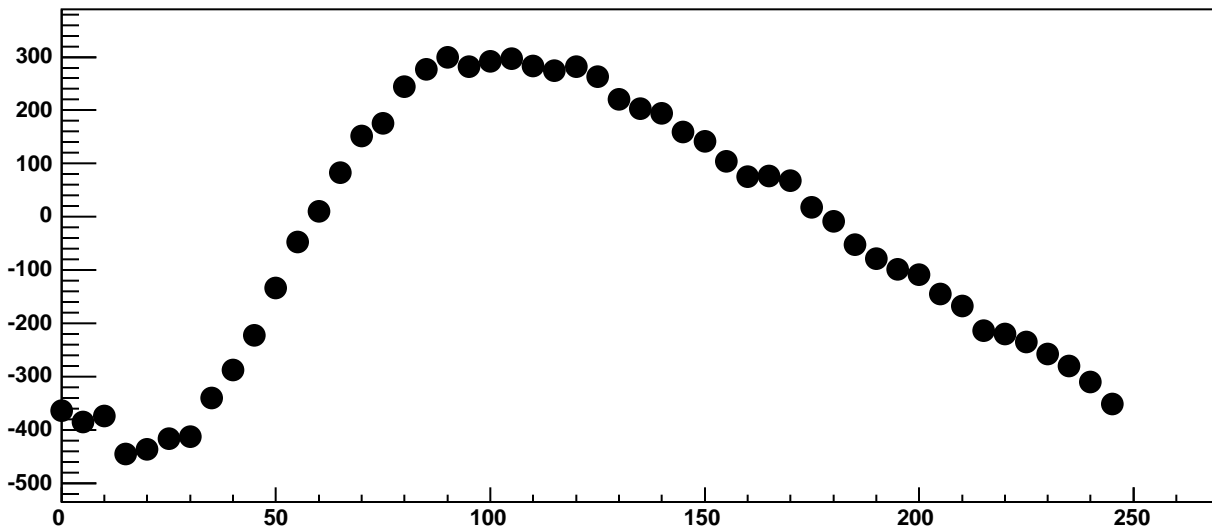


$\chi^2 / \text{ndf}$	1.683e+04 / 41
p0	-173.9 ± 8.978
p1	-2042 ± 2.959
p2	-5449 ± 11.29
p3	-1.121e+04 ± 167.7
p4	2.455 ± 0.004136

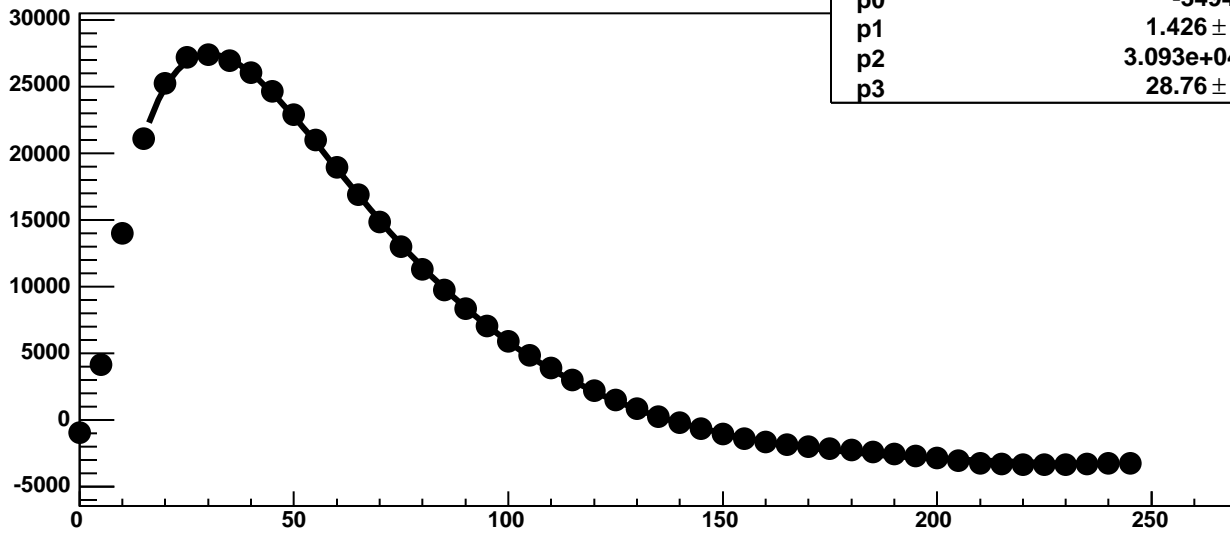
Chip 4, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



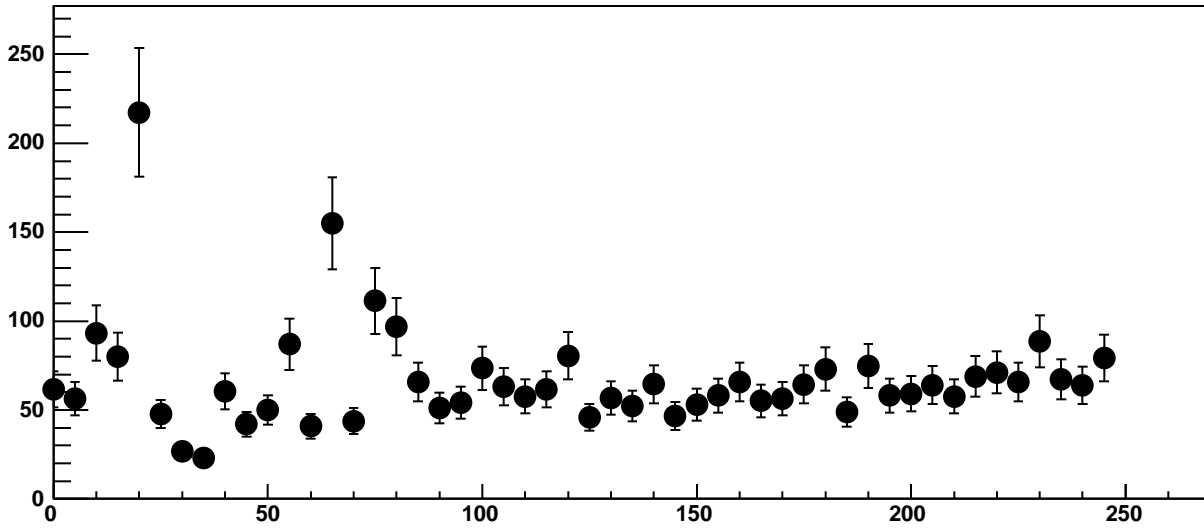
Chip 4, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



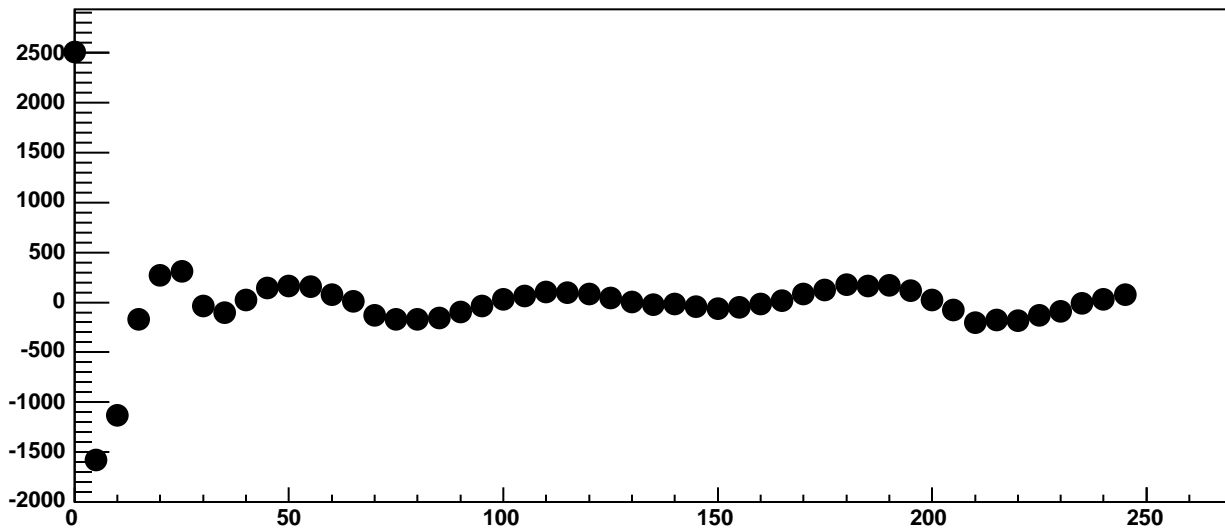
Chip 4, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold



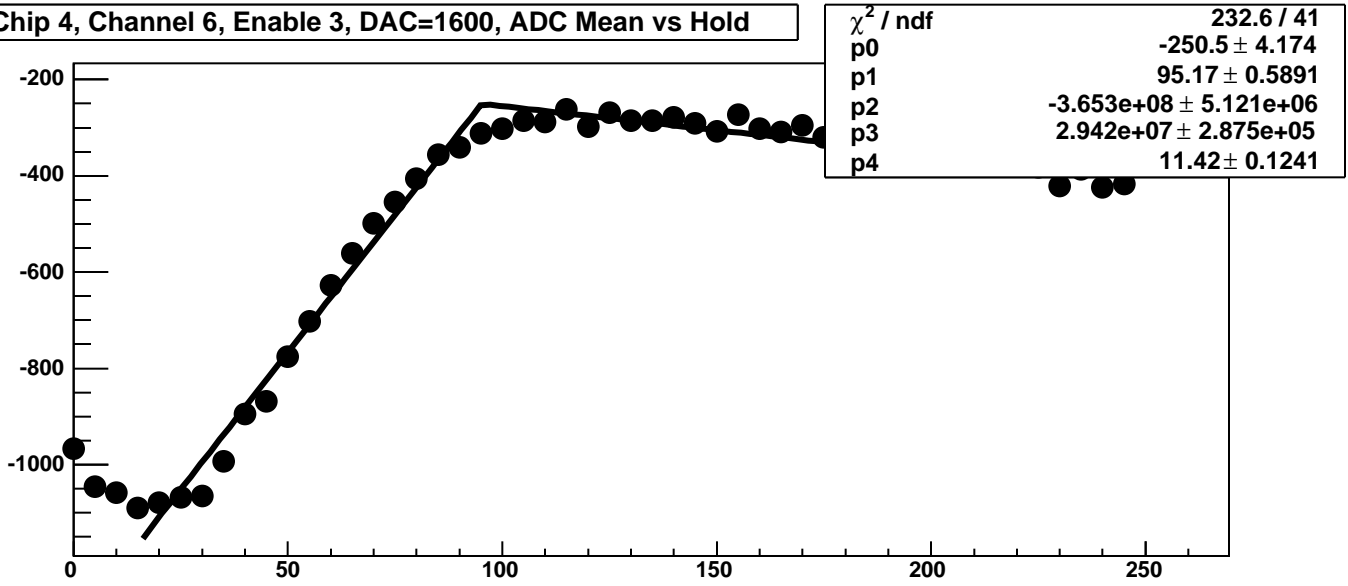
Chip 4, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



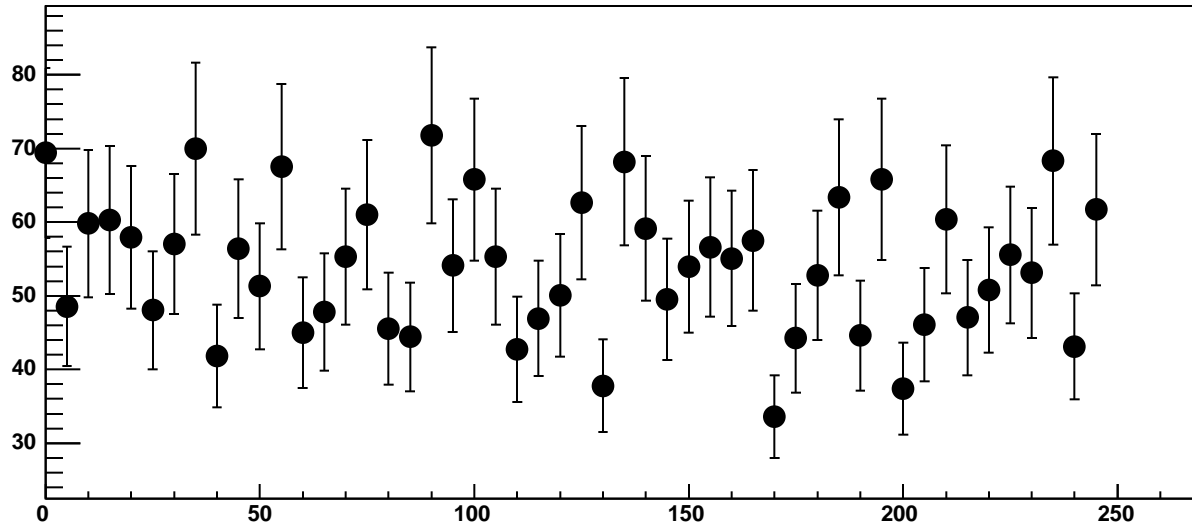
Chip 4, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold



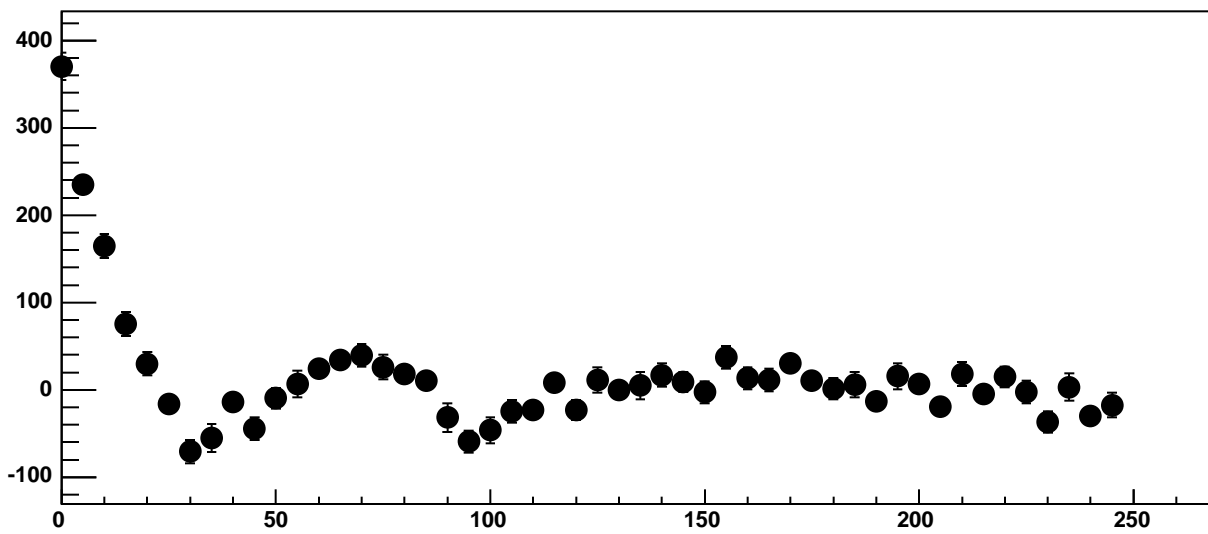
Chip 4, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold



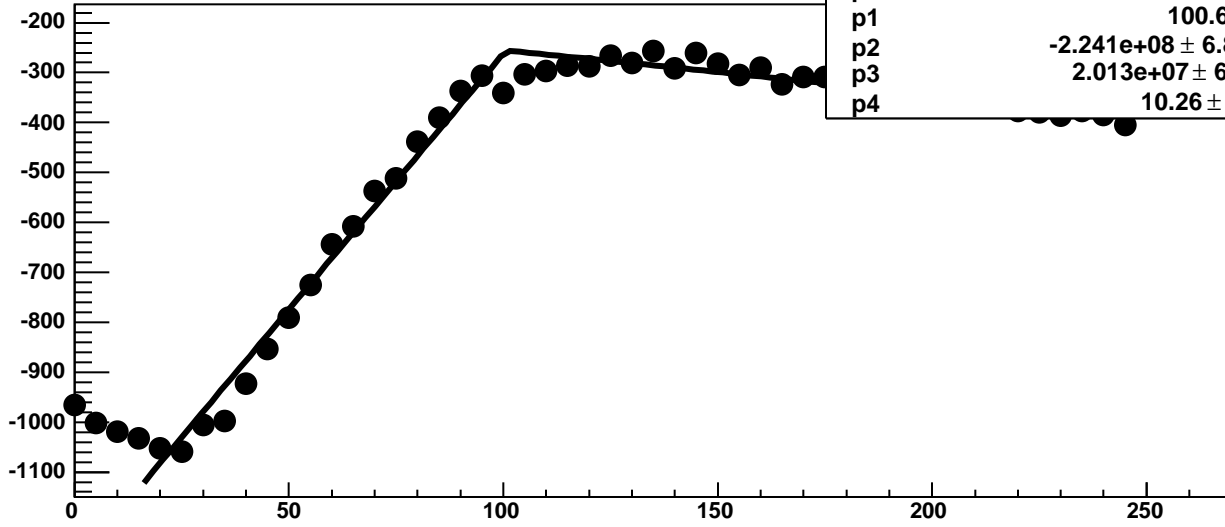
Chip 4, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

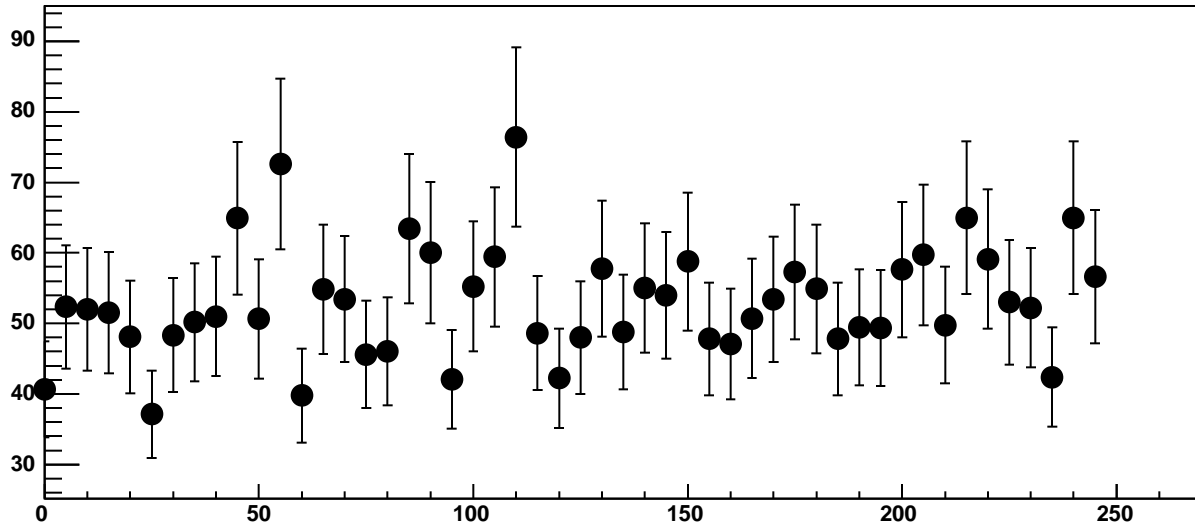


Chip 4, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

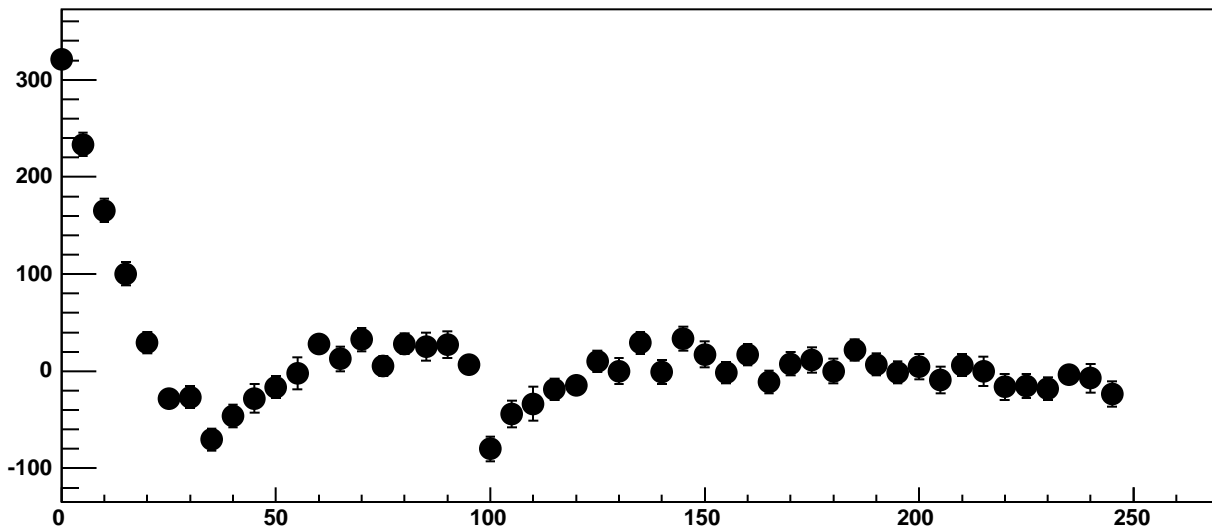


$\chi^2 / \text{ndf}$	278 / 41
p0	$-255.3 \pm 4.214$
p1	$100.6 \pm 0.603$
p2	$-2.241\text{e}+08 \pm 6.814\text{e}+06$
p3	$2.013\text{e}+07 \pm 6.49\text{e}+05$
p4	$10.26 \pm 0.09567$

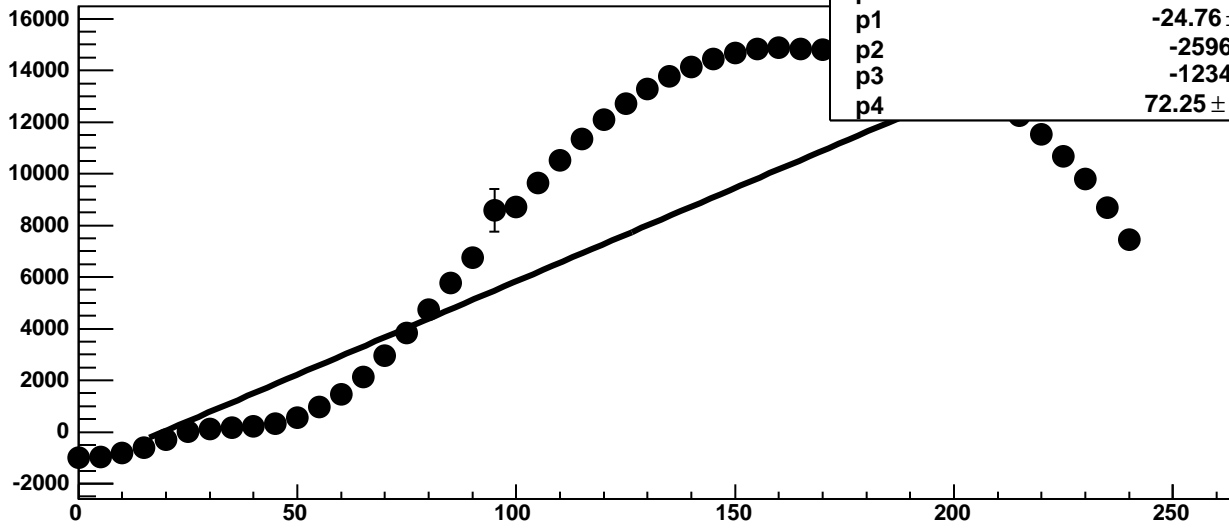
Chip 4, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

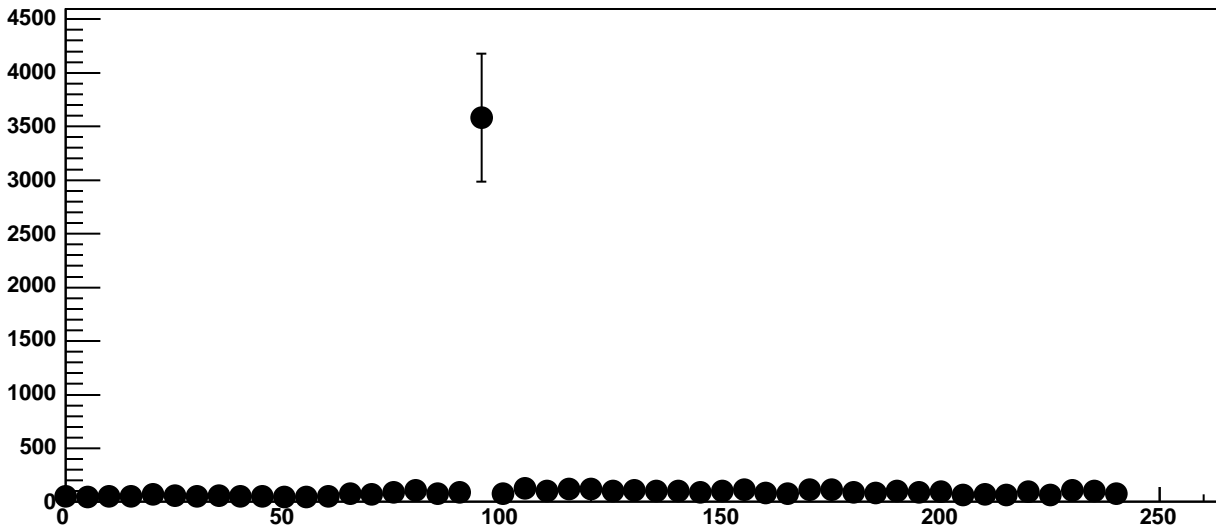


Chip 4, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold

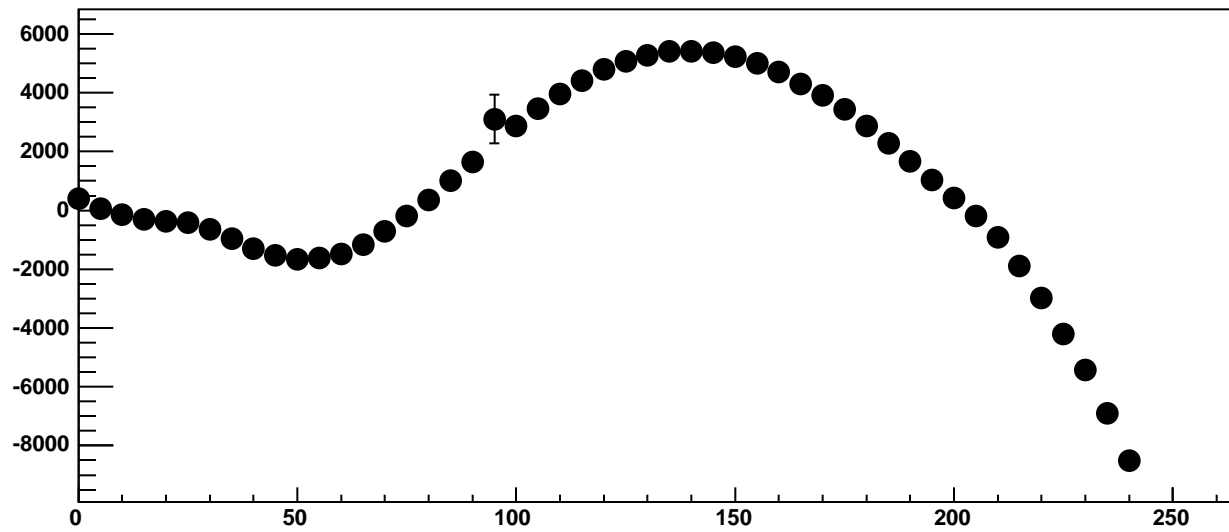


$\chi^2 / \text{ndf}$	1.264e+06 / 41
p0	-581.9 ± 15.37
p1	-24.76 ± 0.1903
p2	-2596 ± 16.54
p3	-1234 ± 30.37
p4	72.25 ± 0.06229

Chip 4, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

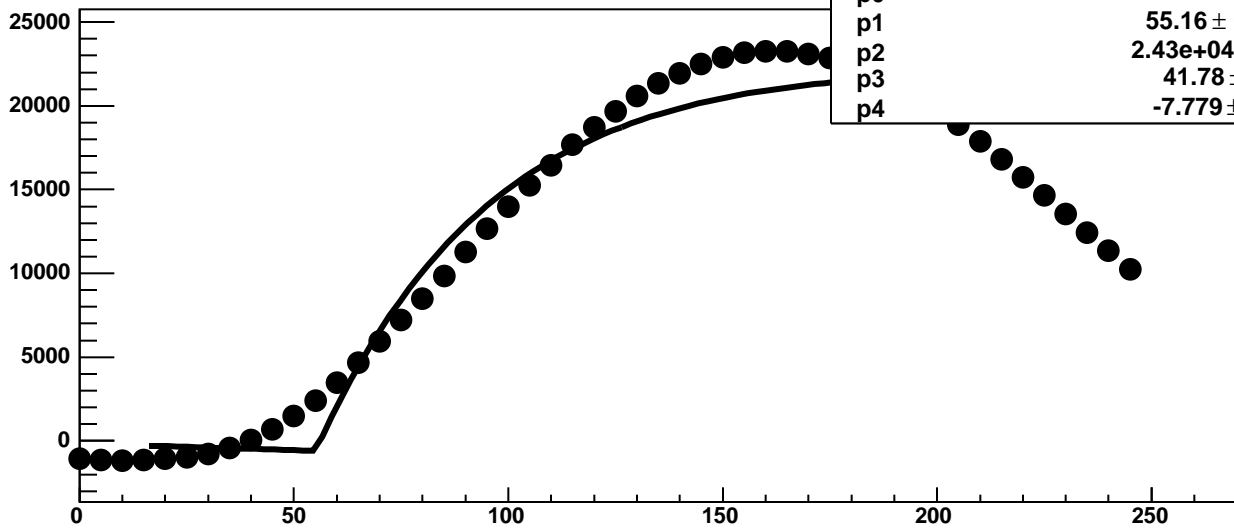


Chip 4, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold



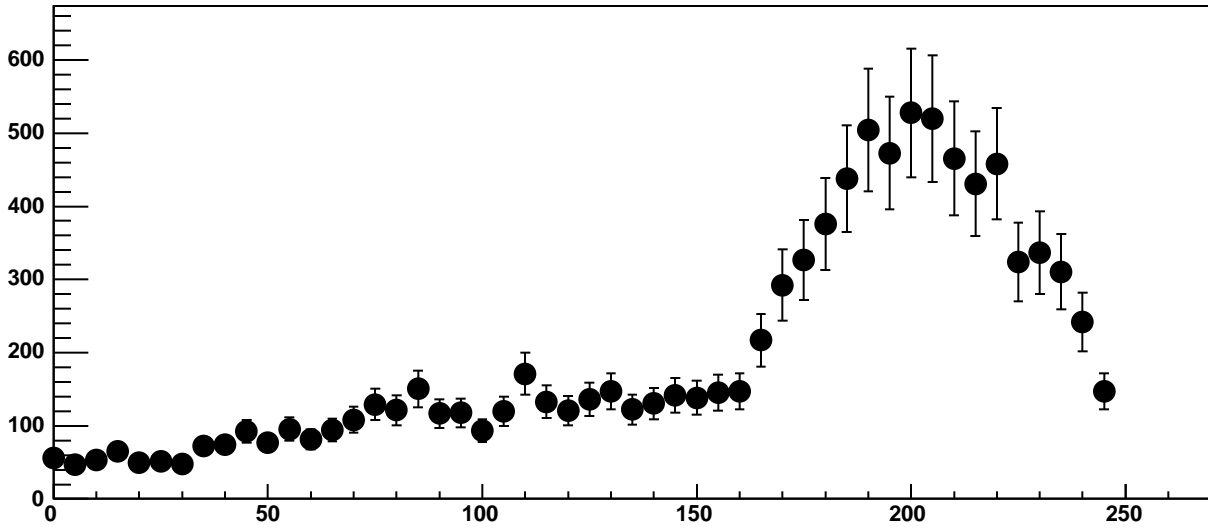


Chip 4, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

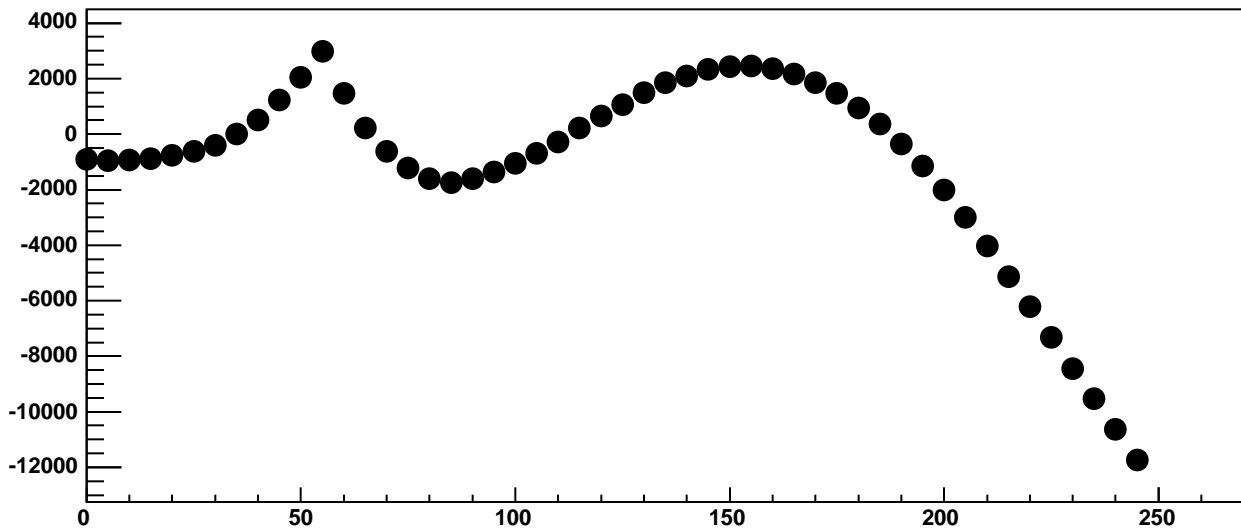


$\chi^2 / \text{ndf}$	1.94e+05 / 41
p0	-594.3 ± 8.947
p1	55.16 ± 0.03445
p2	2.43e+04 ± 54.65
p3	41.78 ± 0.1081
p4	-7.779 ± 0.3107

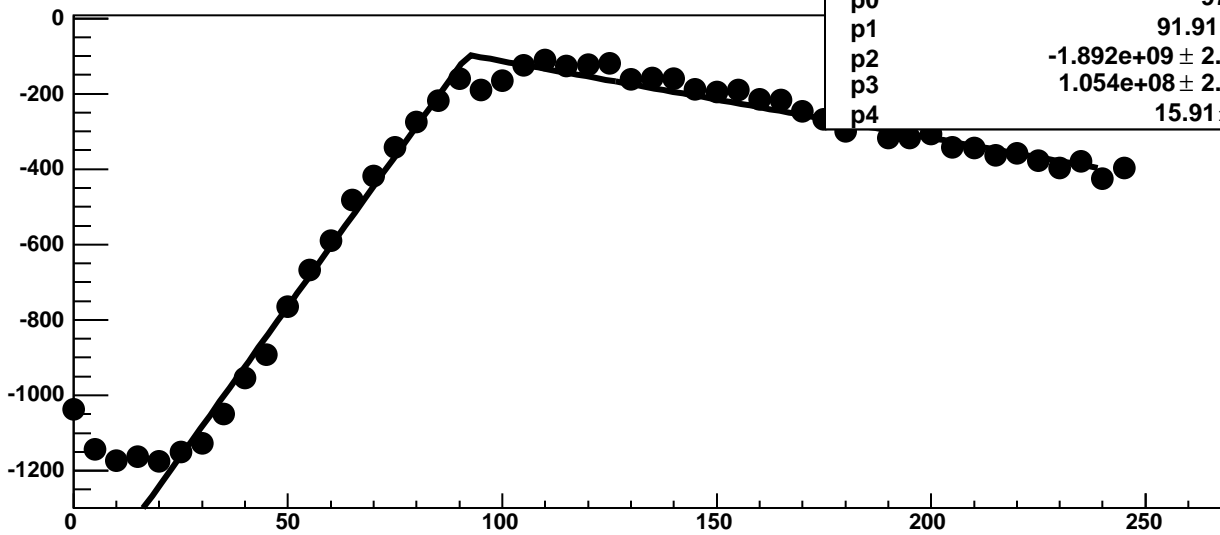
Chip 4, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

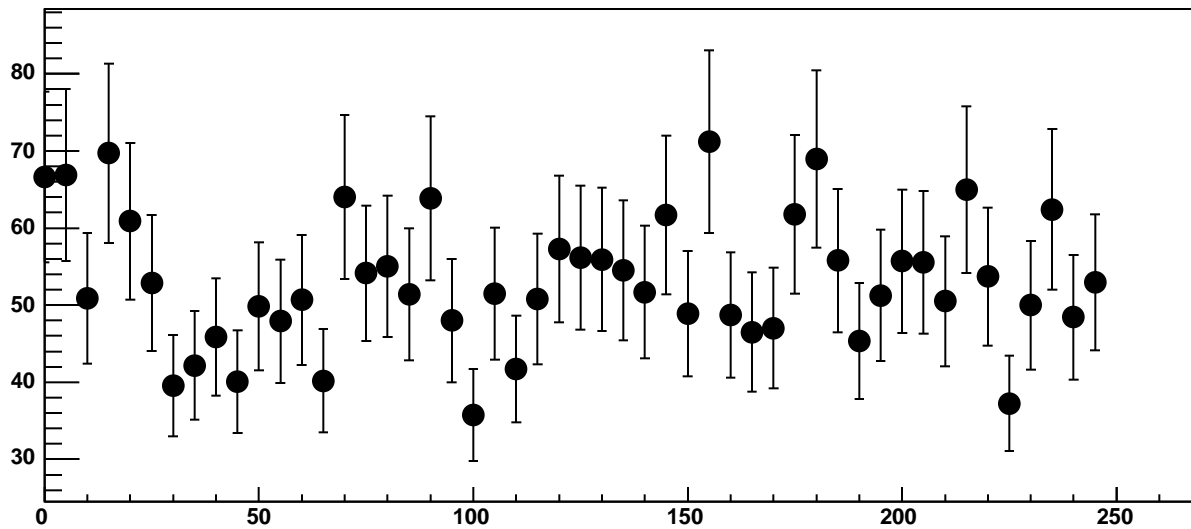


Chip 4, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

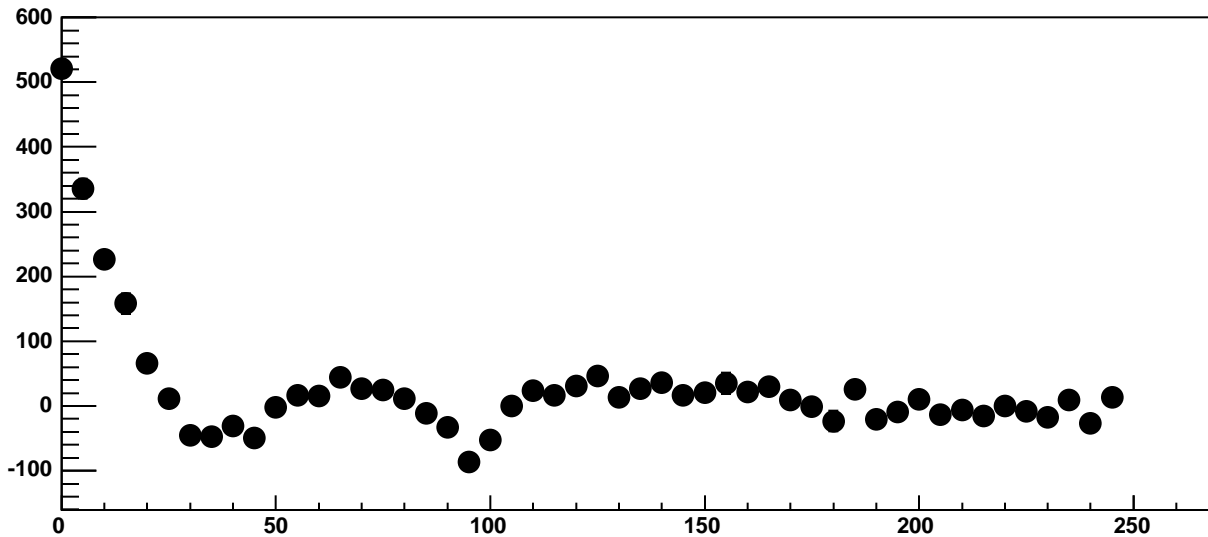


$\chi^2 / \text{ndf}$	436.8 / 41
p0	$-97 \pm 3.959$
p1	$91.91 \pm 0.3169$
p2	$-1.892\text{e}+09 \pm 2.101\text{e}+07$
p3	$1.054\text{e}+08 \pm 2.146\text{e}+06$
p4	$15.91 \pm 0.1425$

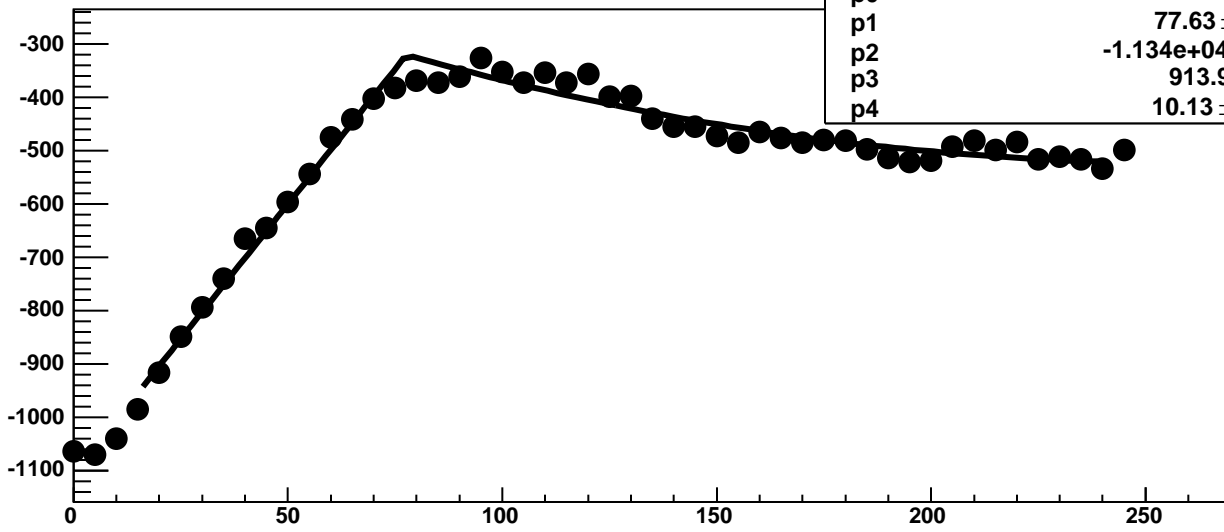
Chip 4, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

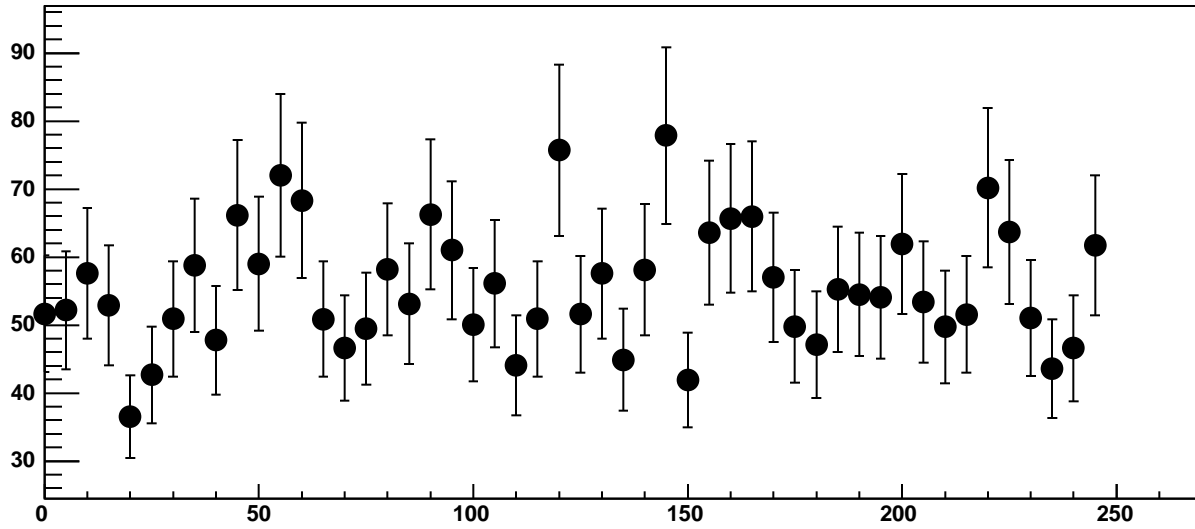


Chip 4, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold

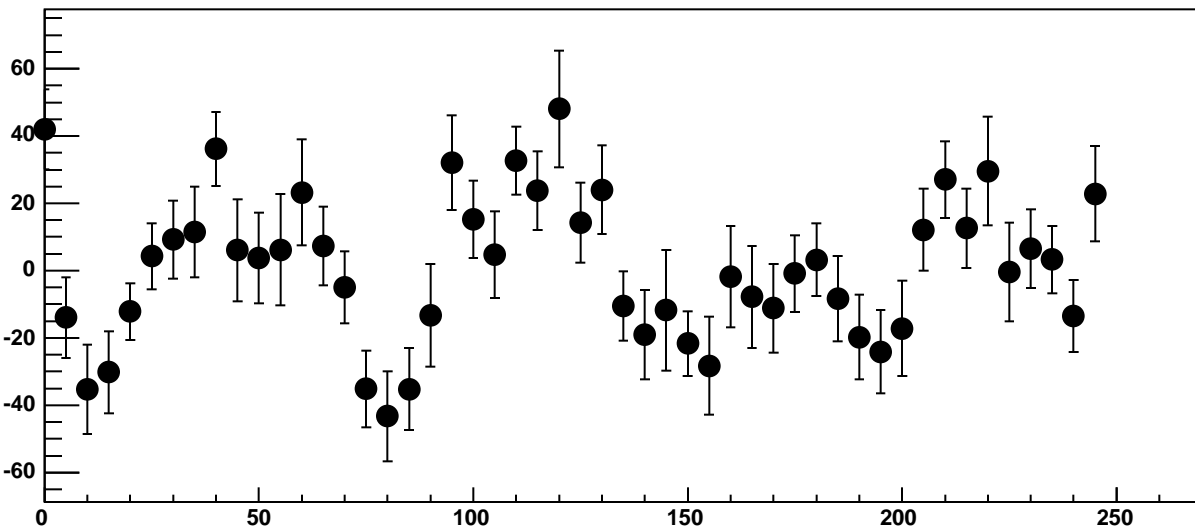


$\chi^2 / \text{ndf}$	122 / 41
p0	$-319.9 \pm 5.242$
p1	$77.63 \pm 0.7218$
p2	$-1.134e+04 \pm 1492$
p3	$913.9 \pm 130.1$
p4	$10.13 \pm 0.1625$

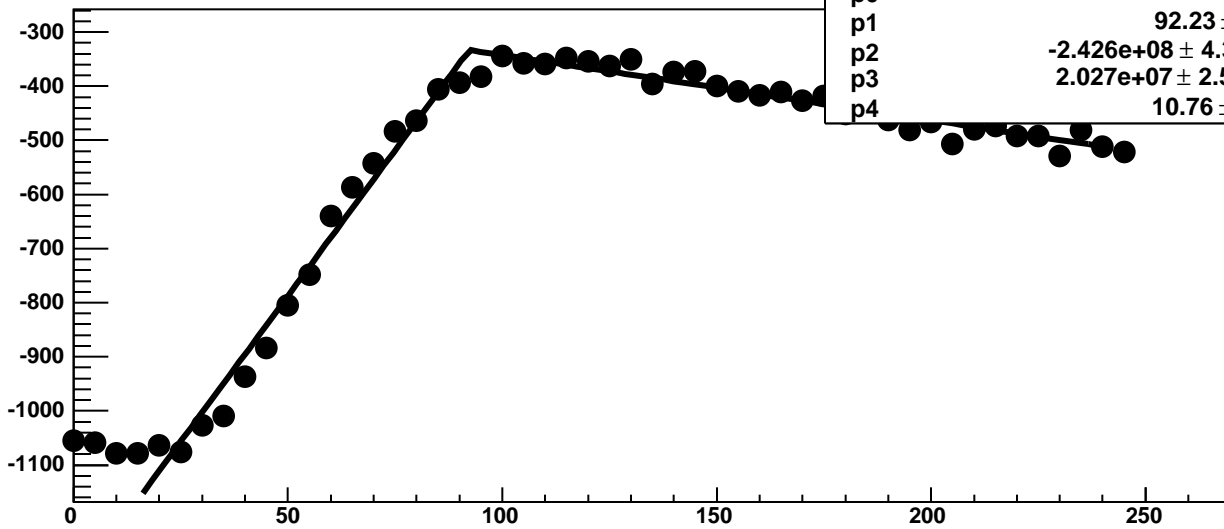
Chip 4, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold

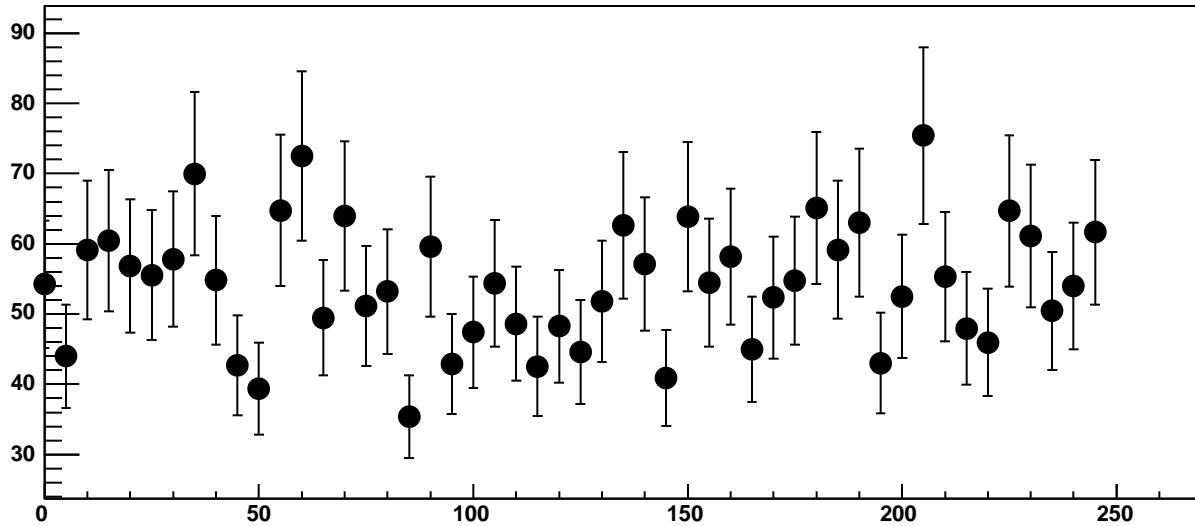


Chip 4, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

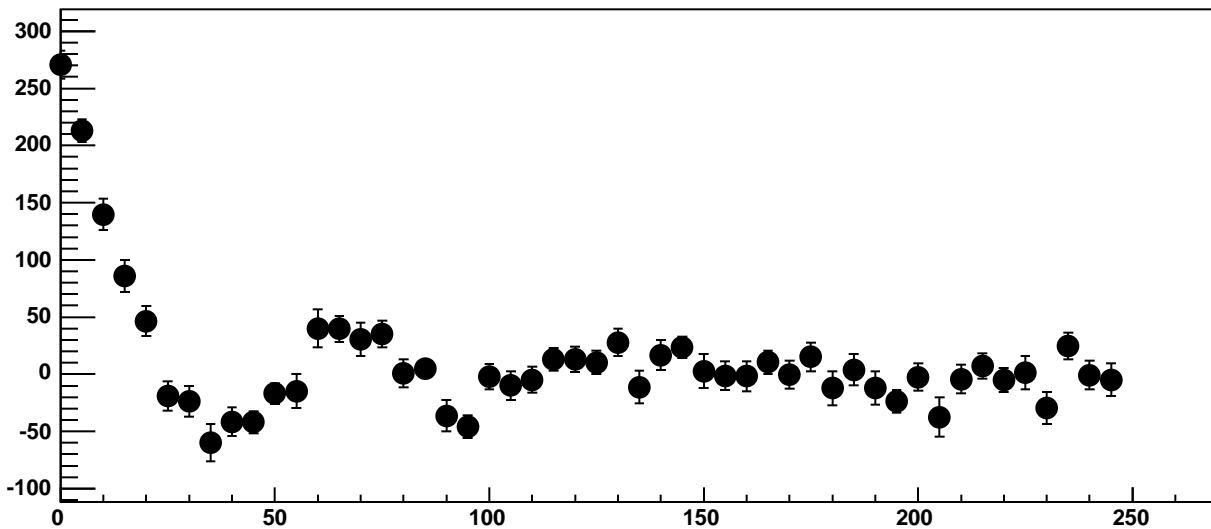


$\chi^2 / \text{ndf}$	208 / 41
p0	-333.1 ± 3.742
p1	92.23 ± 0.5858
p2	-2.426e+08 ± 4.367e+06
p3	2.027e+07 ± 2.588e+05
p4	10.76 ± 0.1314

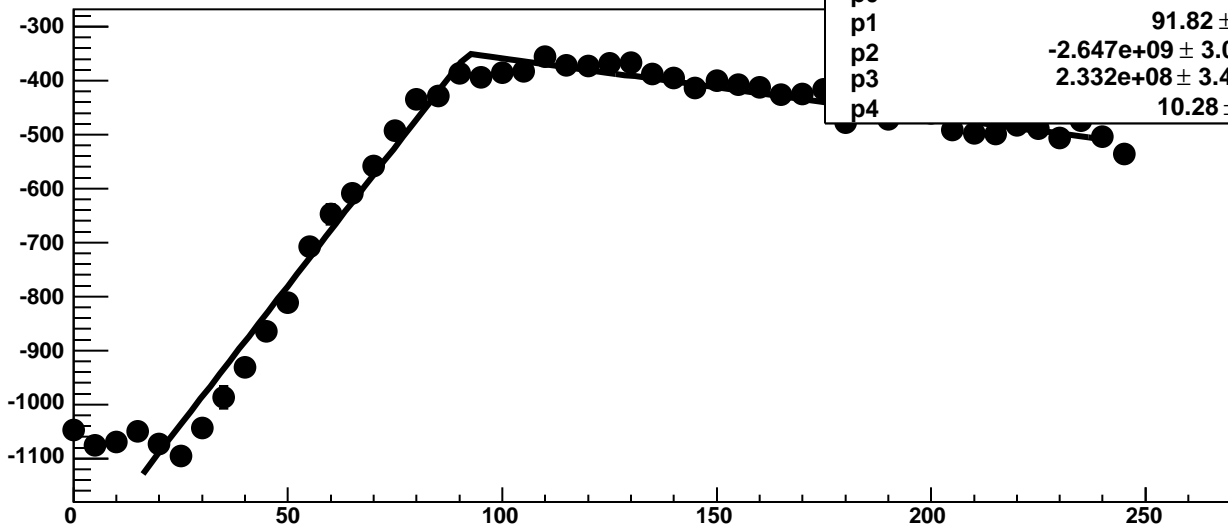
Chip 4, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

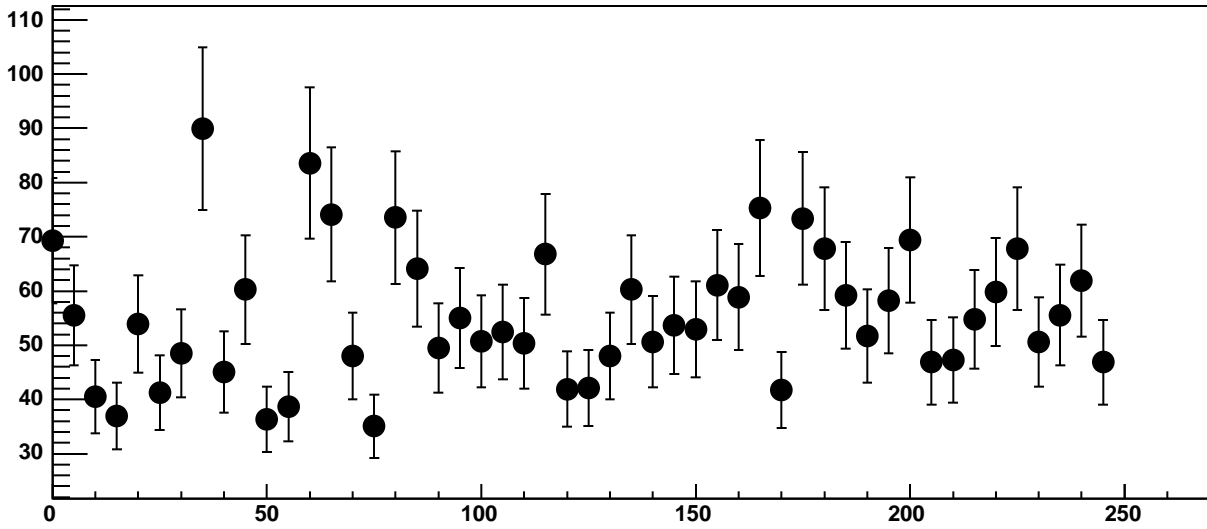


Chip 4, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

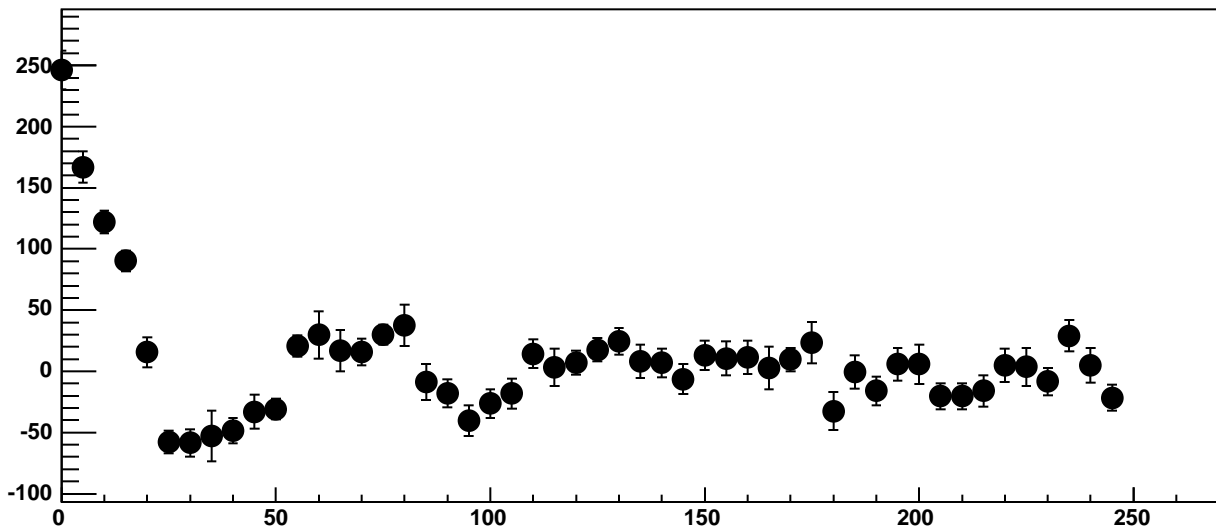


$\chi^2 / \text{ndf}$	316.1 / 41
p0	$-350.2 \pm 4.007$
p1	$91.82 \pm 0.6334$
p2	$-2.647\text{e}+09 \pm 3.048\text{e}+07$
p3	$2.332\text{e}+08 \pm 3.424\text{e}+05$
p4	$10.28 \pm 0.1191$

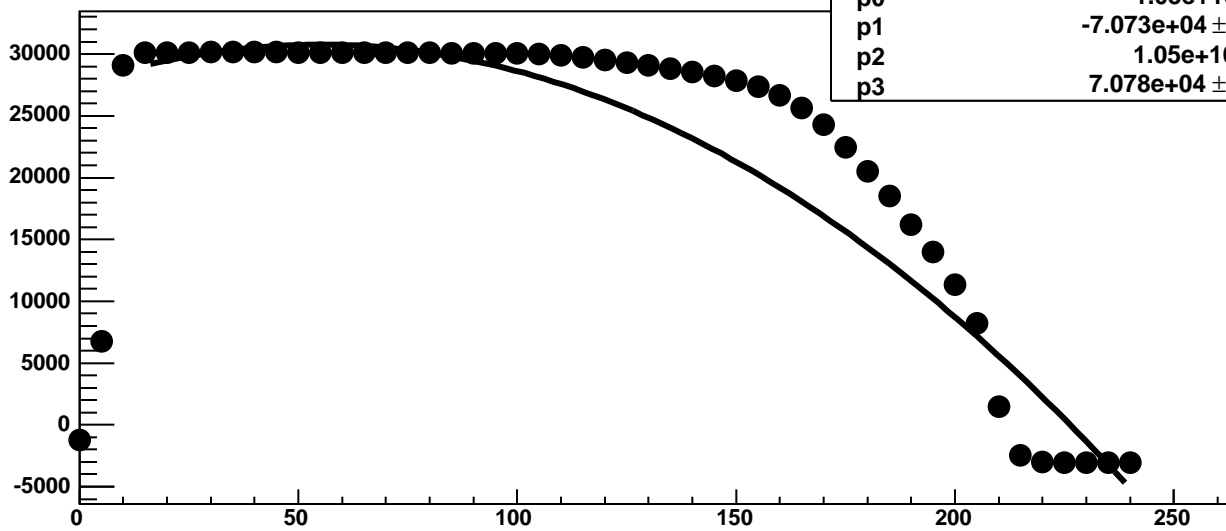
Chip 4, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

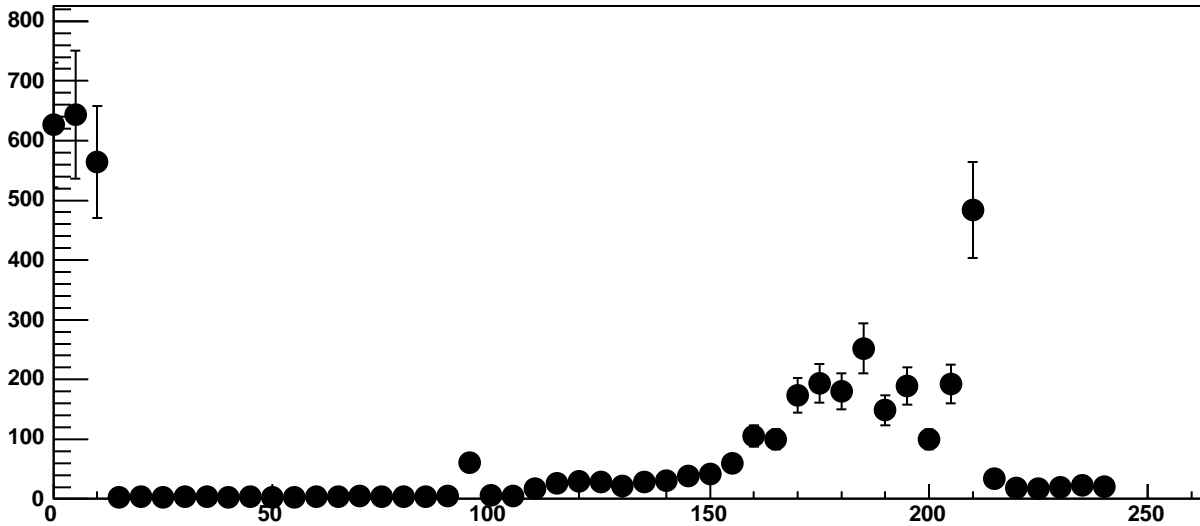


Chip 4, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold

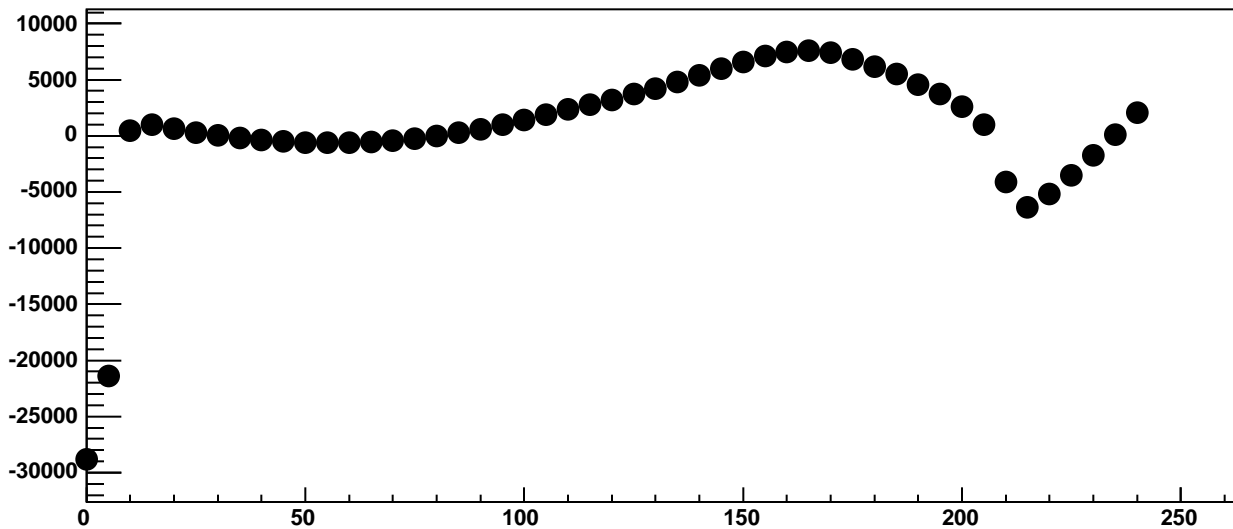


$\chi^2 / \text{ndf}$	1.819e+07 / 42
p0	-1.05e+10 ± 3.061
p1	-7.073e+04 ± 0.04783
p2	1.05e+10 ± 3.061
p3	7.078e+04 ± 0.04779

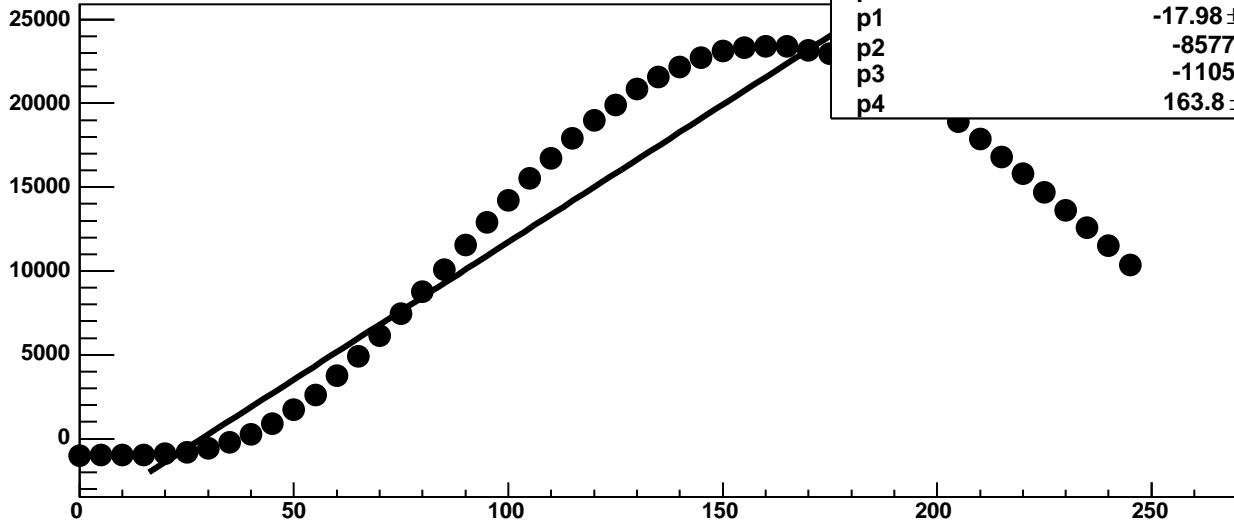
Chip 4, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold

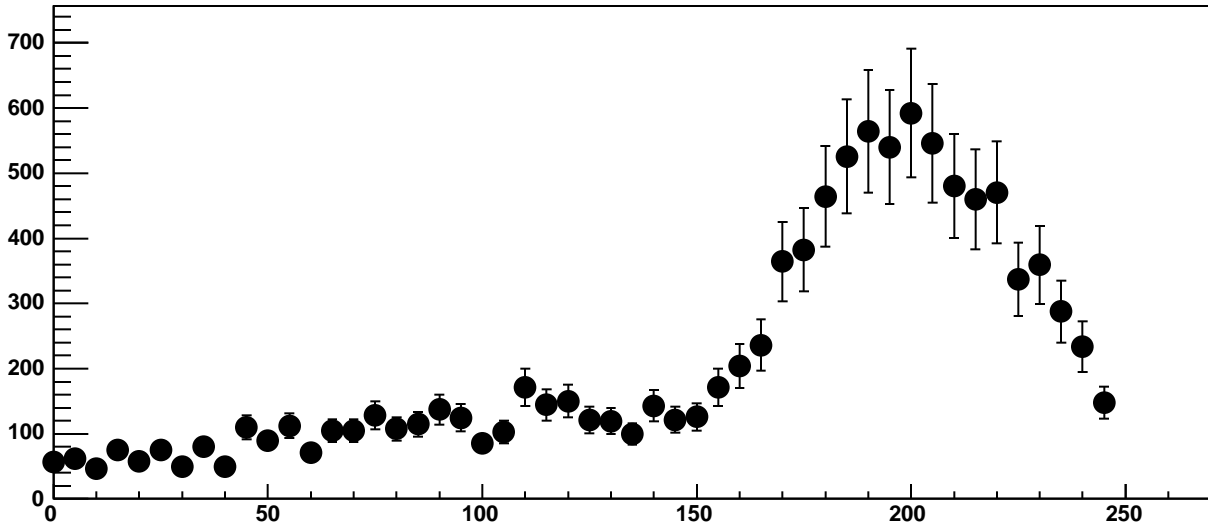


Chip 4, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

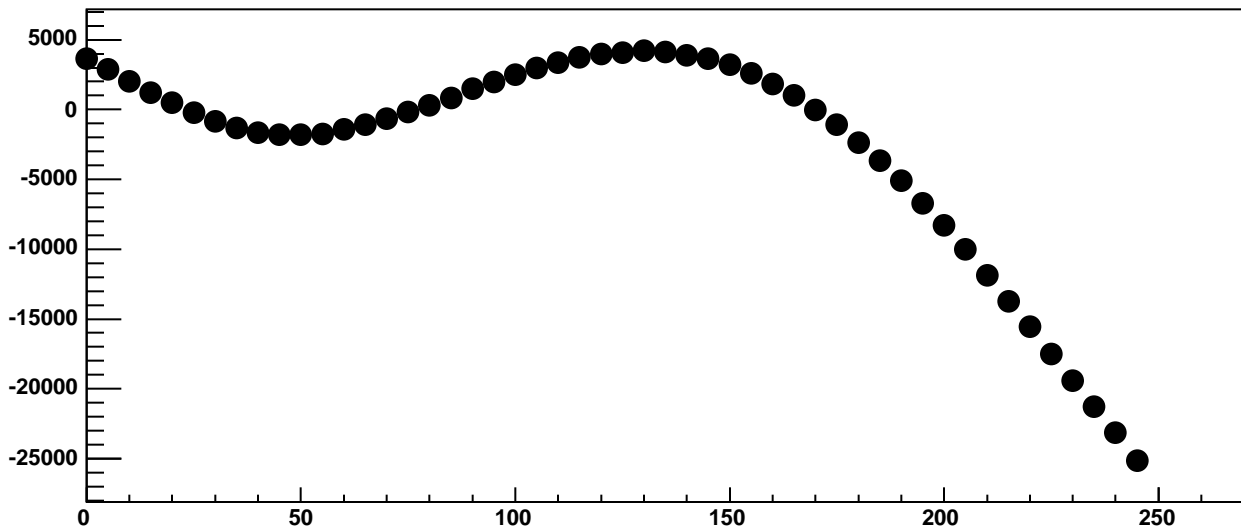


$\chi^2 / \text{ndf}$	7.298e+05 / 41
p0	971.4 ± 21.7
p1	-17.98 ± 0.1213
p2	-8577 ± 25.22
p3	-1105 ± 15.26
p4	163.8 ± 0.1521

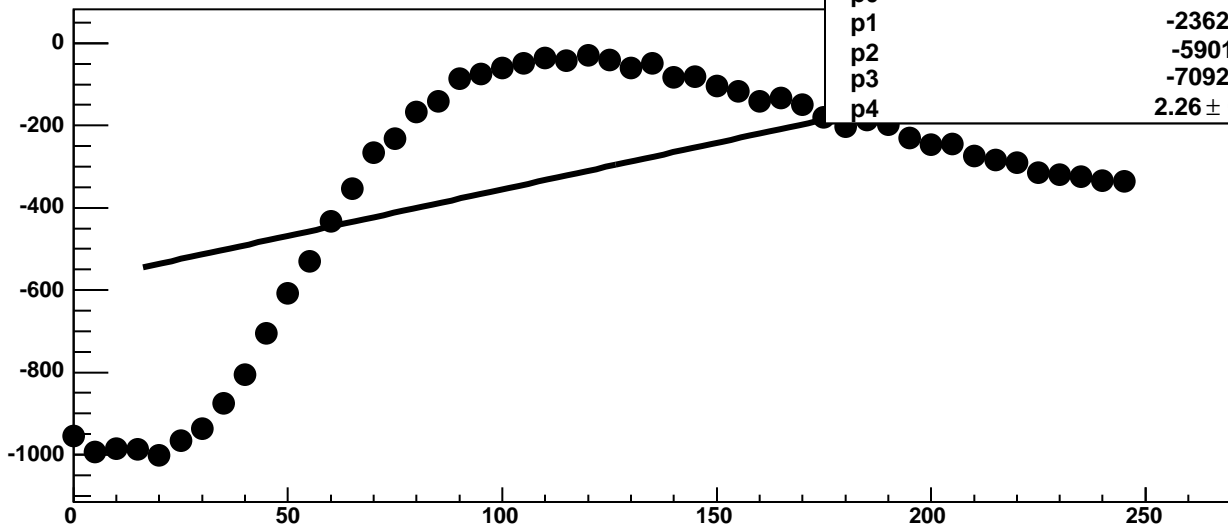
Chip 4, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



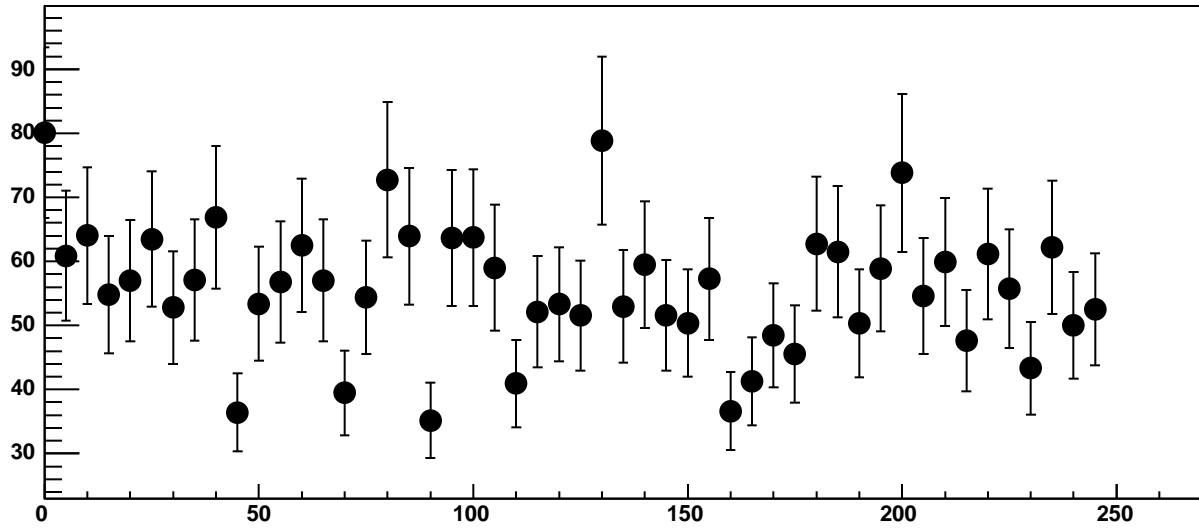
Chip 4, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold



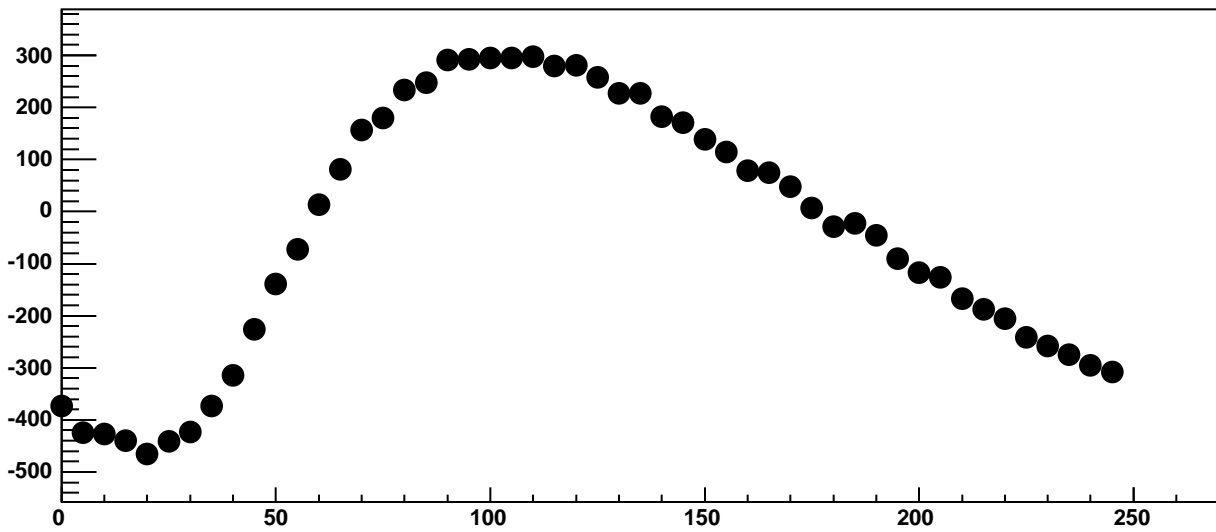
Chip 4, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 4, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

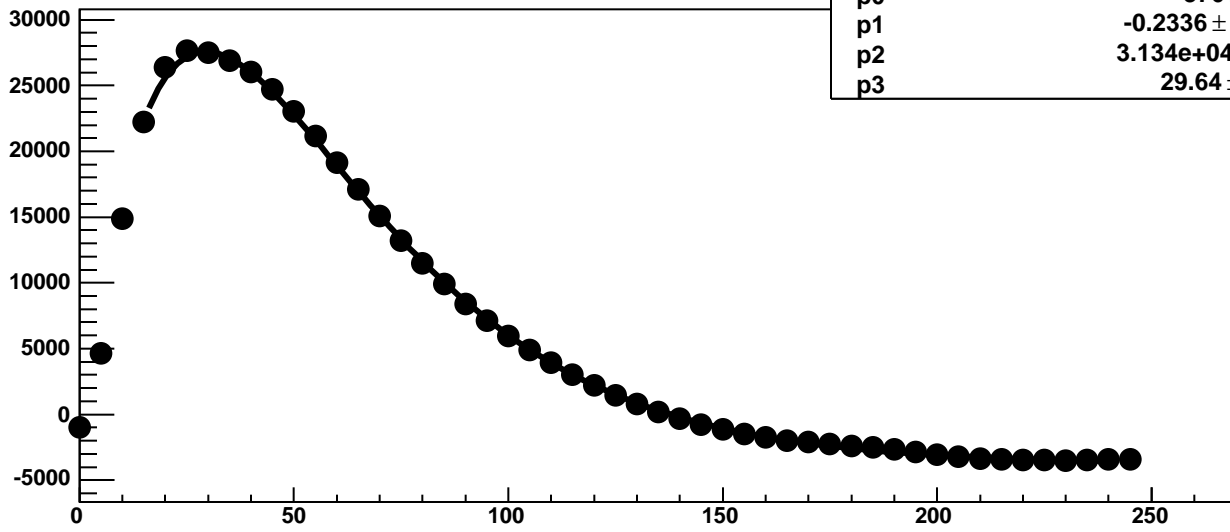


Chip 4, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



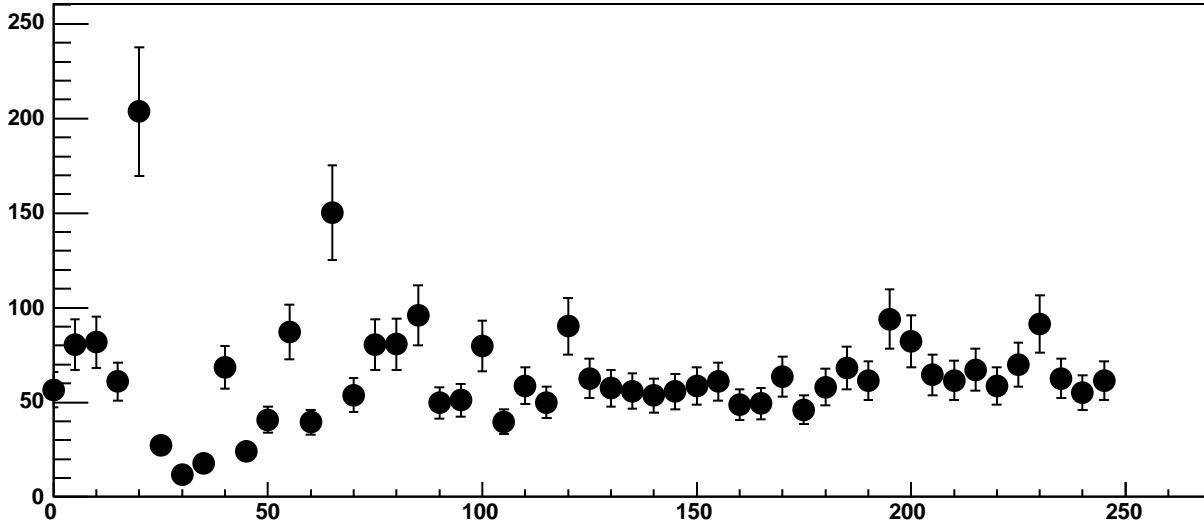


Chip 4, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold

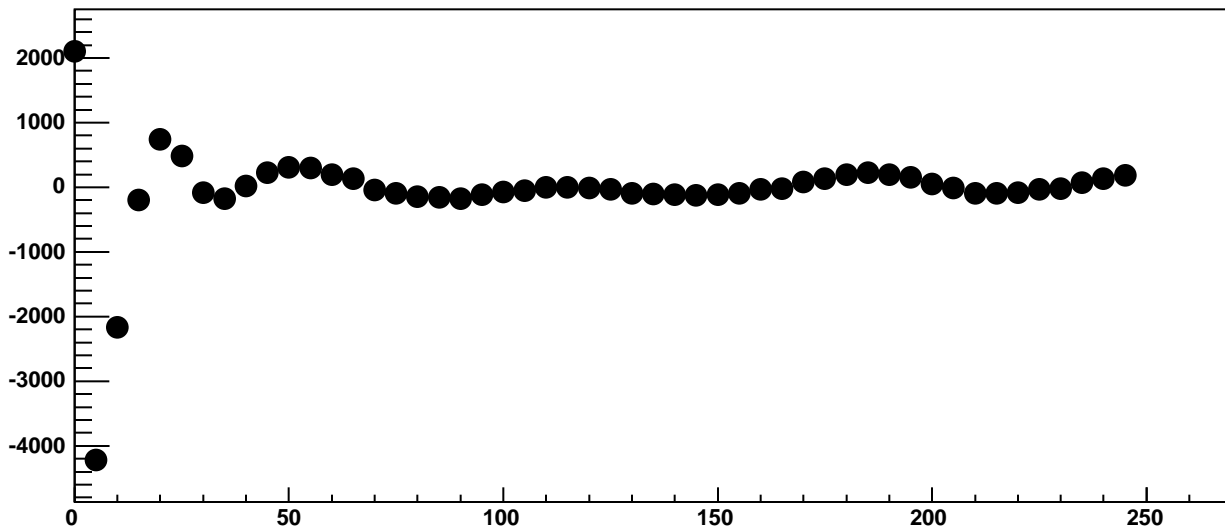


$\chi^2 / \text{ndf}$  1.49e+04 / 42  
p0 -3761 ± 4.045  
p1 -0.2336 ± 0.01692  
p2 3.134e+04 ± 4.334  
p3 29.64 ± 0.0103

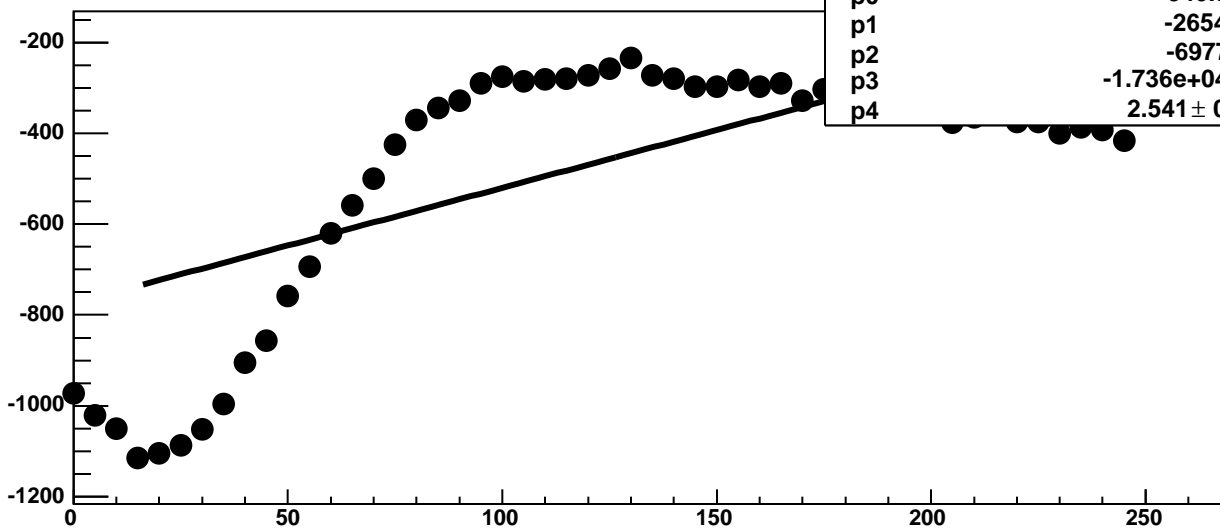
Chip 4, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold

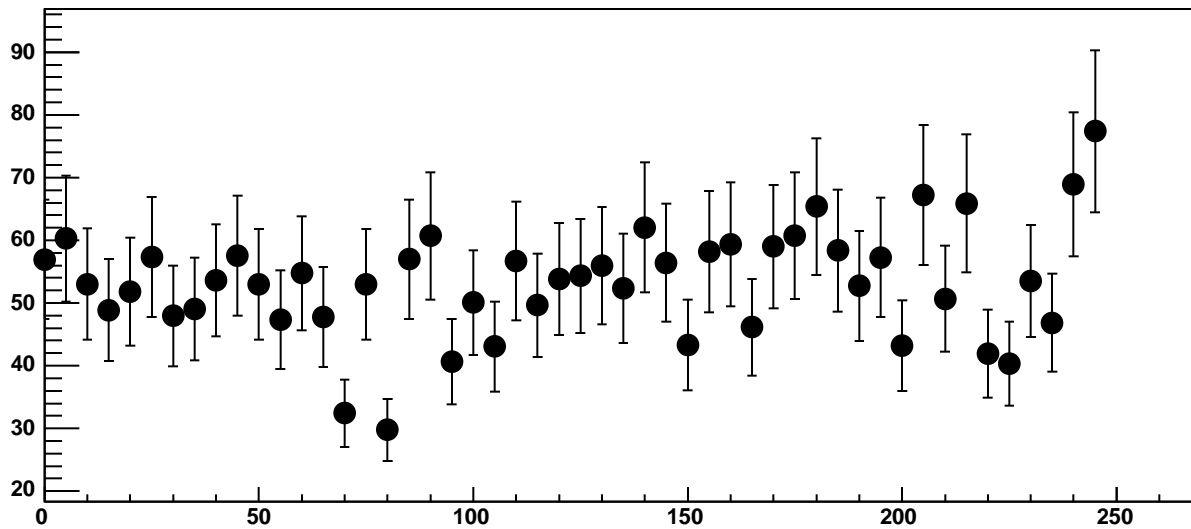


Chip 4, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

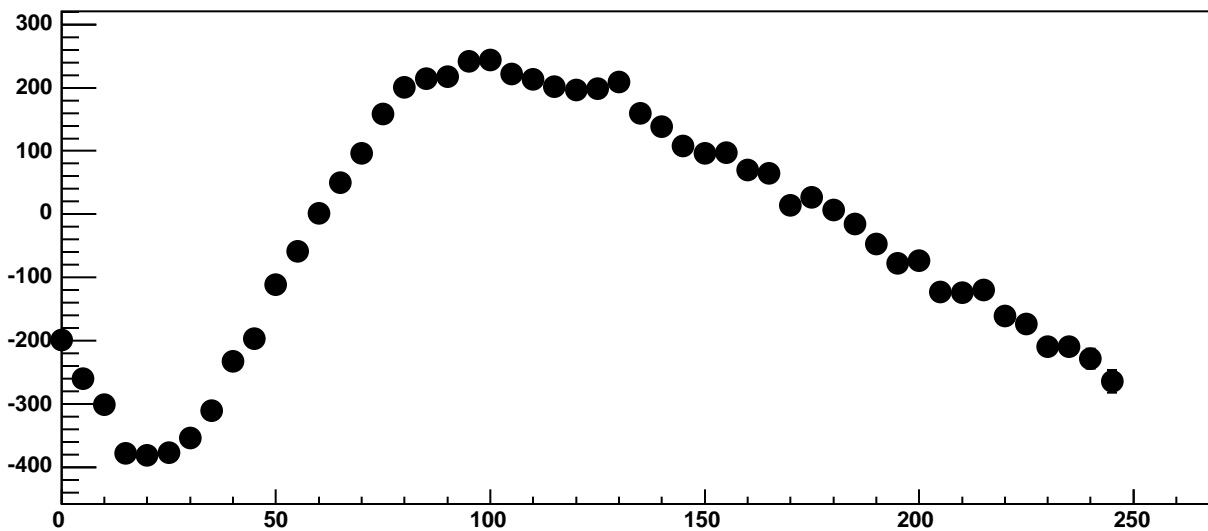


$\chi^2 / \text{ndf}$	1.261e+04 / 41
p0	-540.7 ± 9.396
p1	-2654 ± 2.255
p2	-6977 ± 10.54
p3	-1.736e+04 ± 122.7
p4	2.541 ± 0.003379

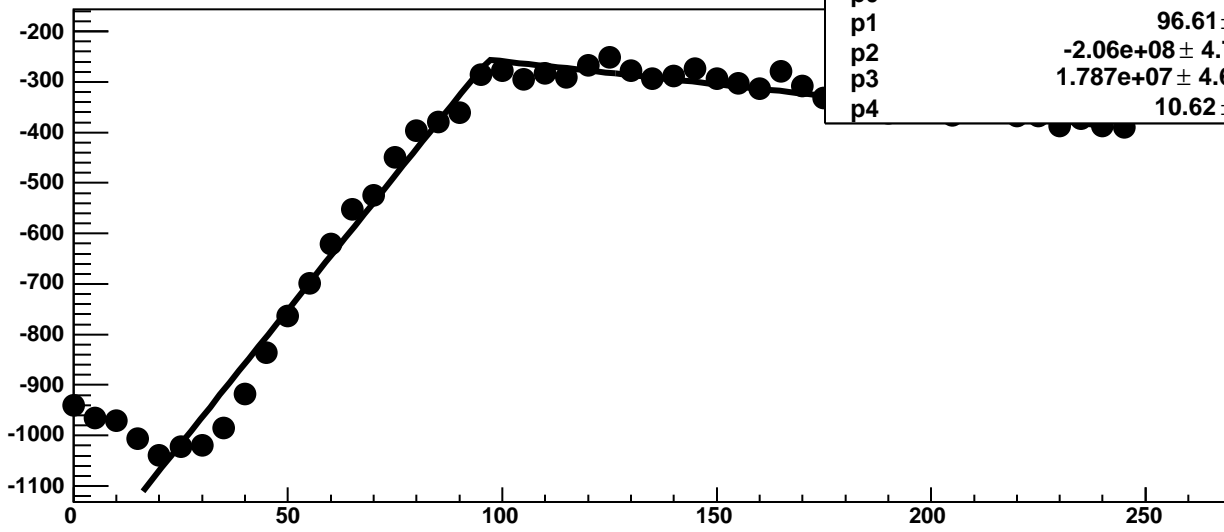
Chip 4, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

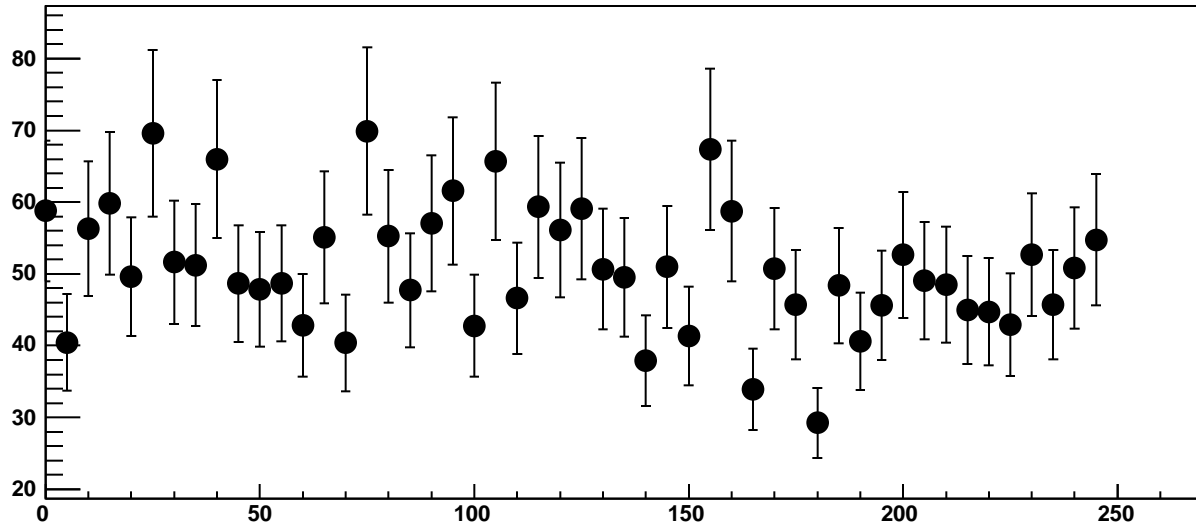


Chip 4, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

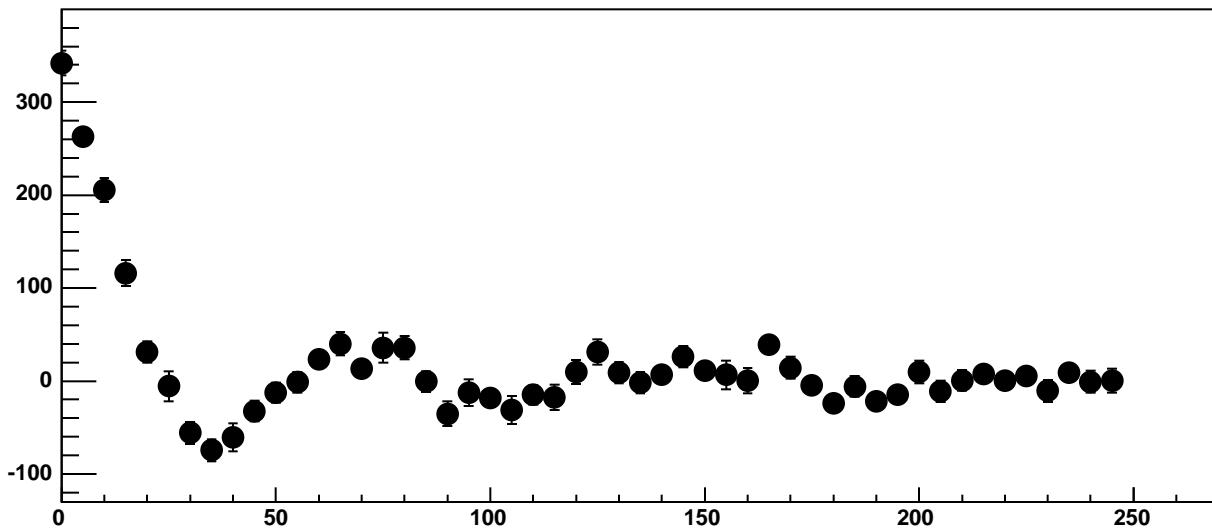


$\chi^2 / \text{ndf}$	282.5 / 41
p0	-256 ± 3.873
p1	96.61 ± 0.5817
p2	-2.06e+08 ± 4.759e+06
p3	1.787e+07 ± 4.601e+05
p4	10.62 ± 0.1108

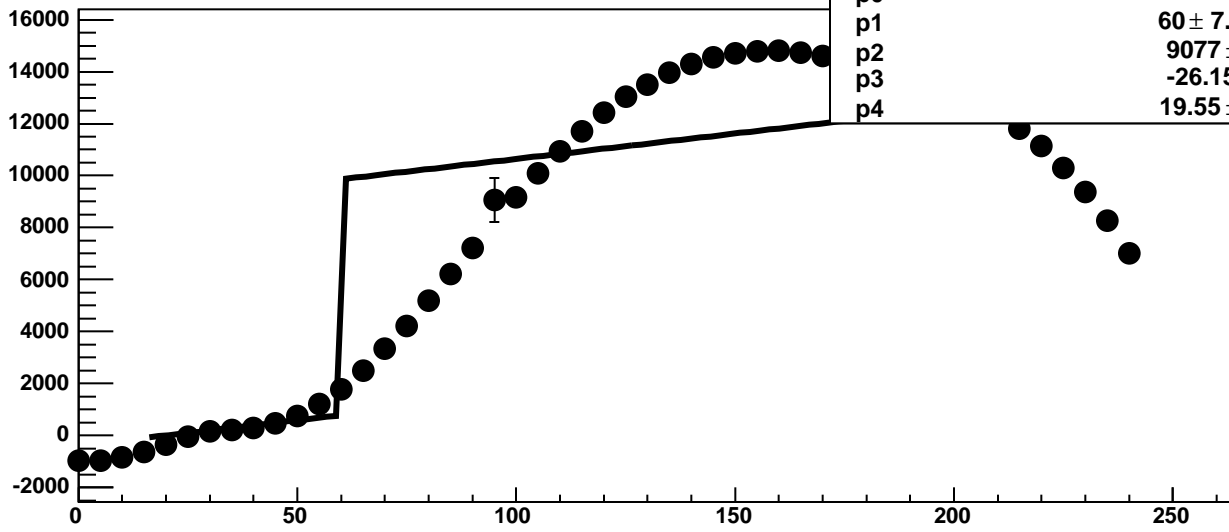
Chip 4, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

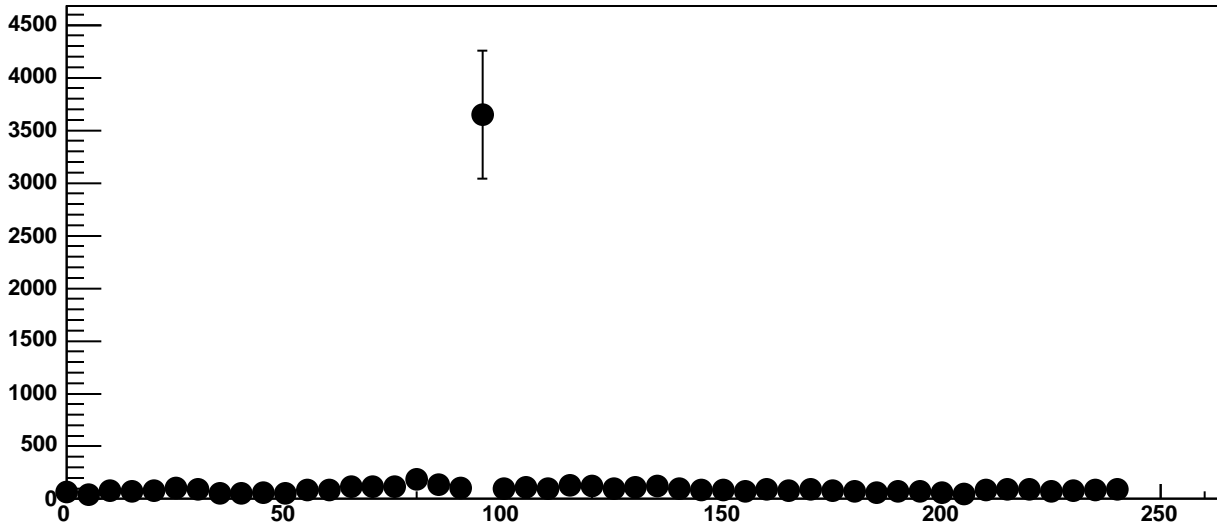


Chip 4, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold

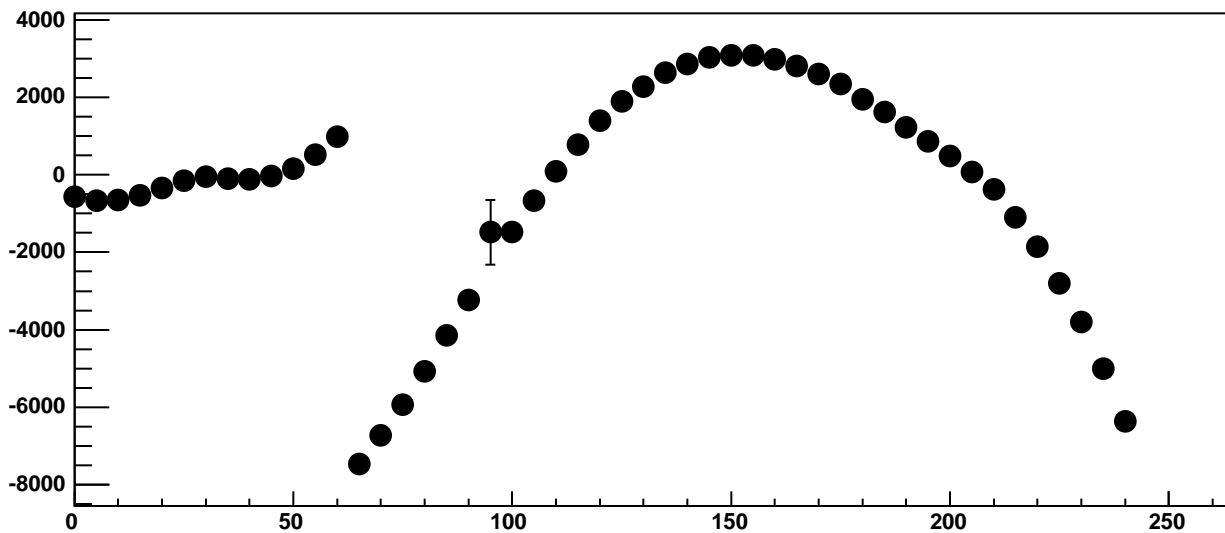


$\chi^2 / \text{ndf}$	7.241e+05 / 41
p0	783.5 ± 0.3981
p1	60 ± 7.809e-05
p2	9077 ± 0.3743
p3	-26.15 ± 19.81
p4	19.55 ± 0.3678

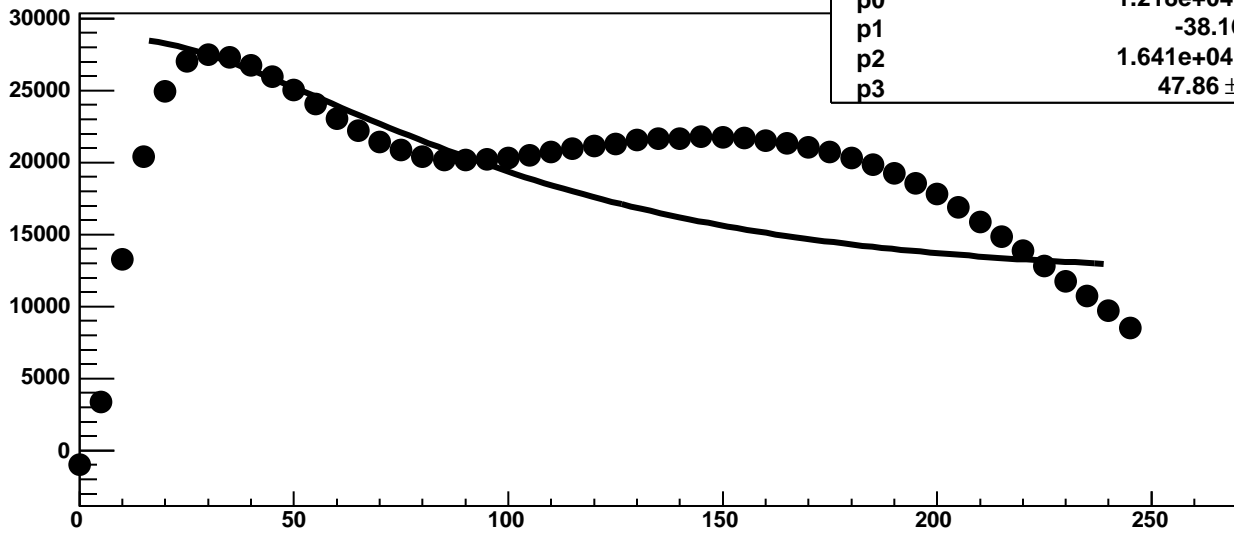
Chip 4, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold

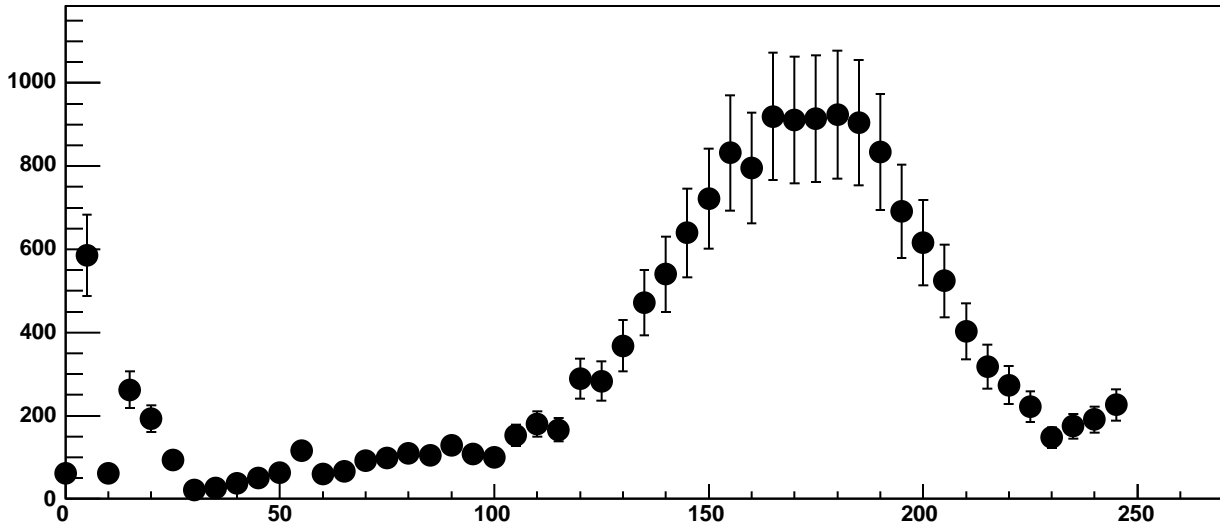


Chip 4, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold

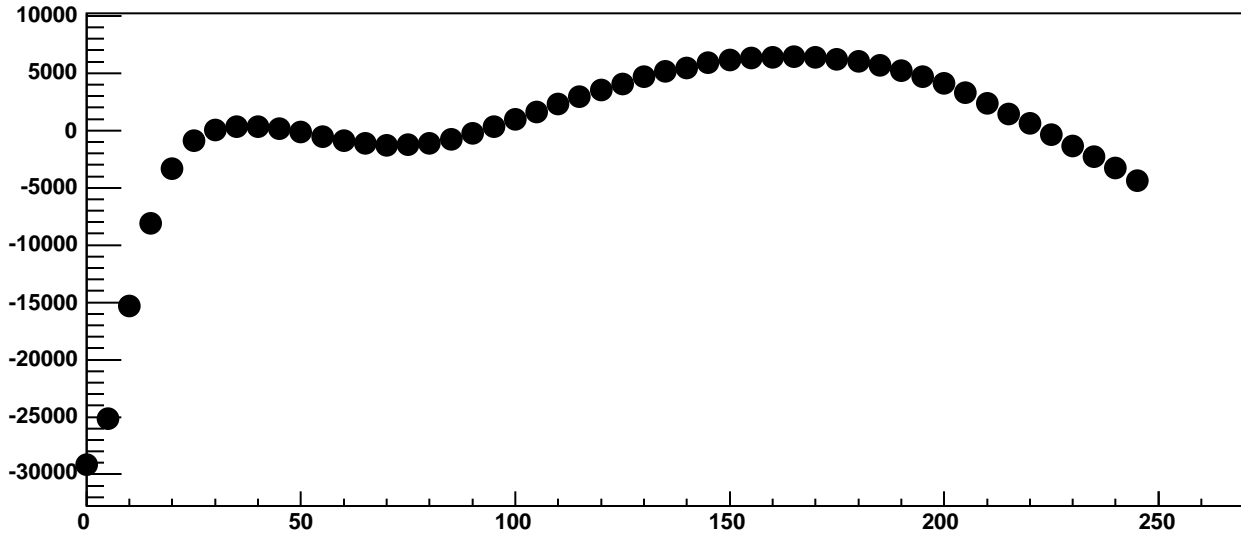


$\chi^2 / \text{ndf}$	1.017e+05 / 42
p0	1.218e+04 $\pm$ 50.74
p1	-38.16 $\pm$ 1.21
p2	1.641e+04 $\pm$ 109.3
p3	47.86 $\pm$ 0.4645

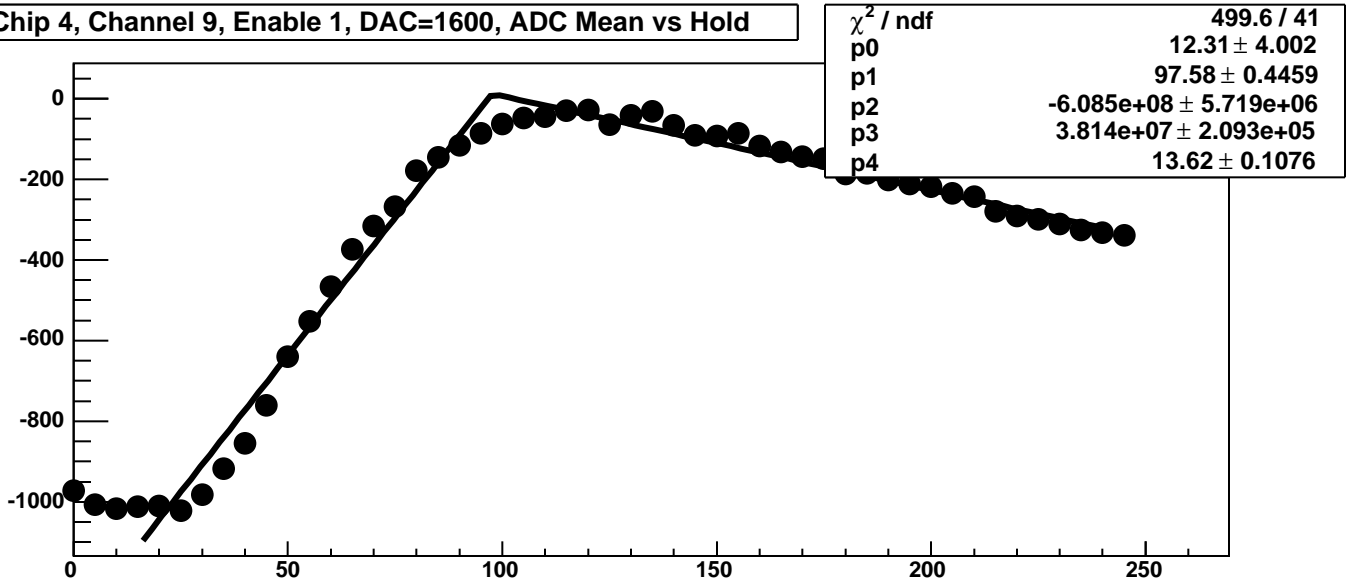
Chip 4, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



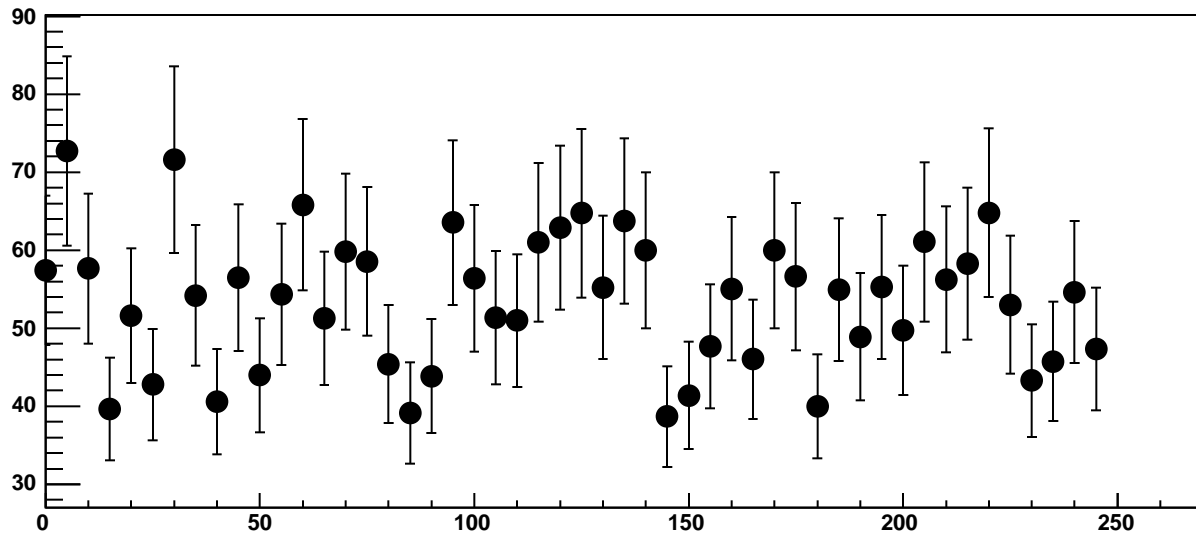
Chip 4, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold



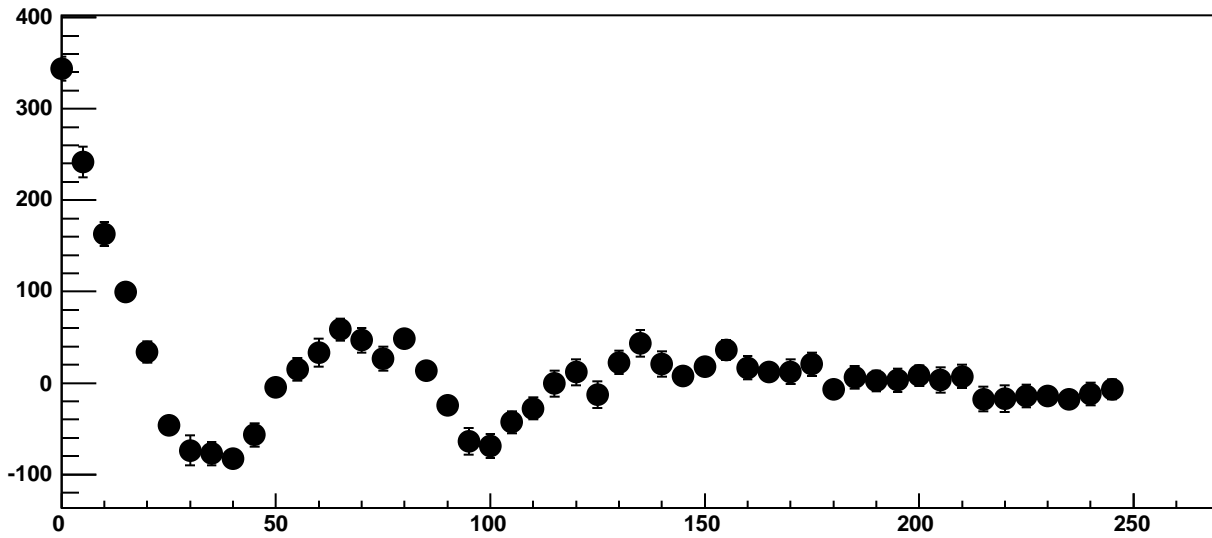
Chip 4, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold



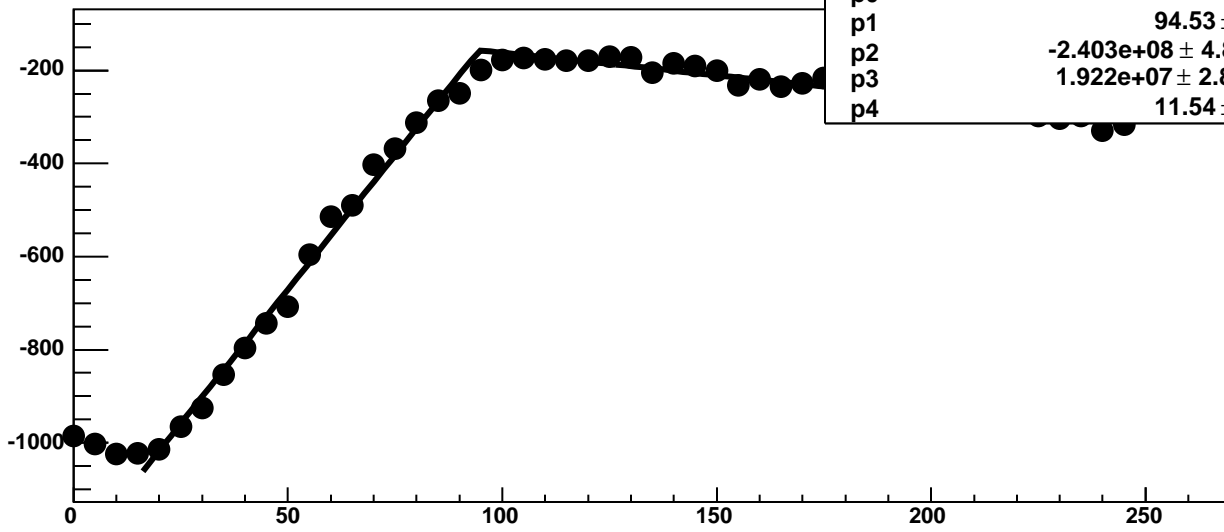
Chip 4, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

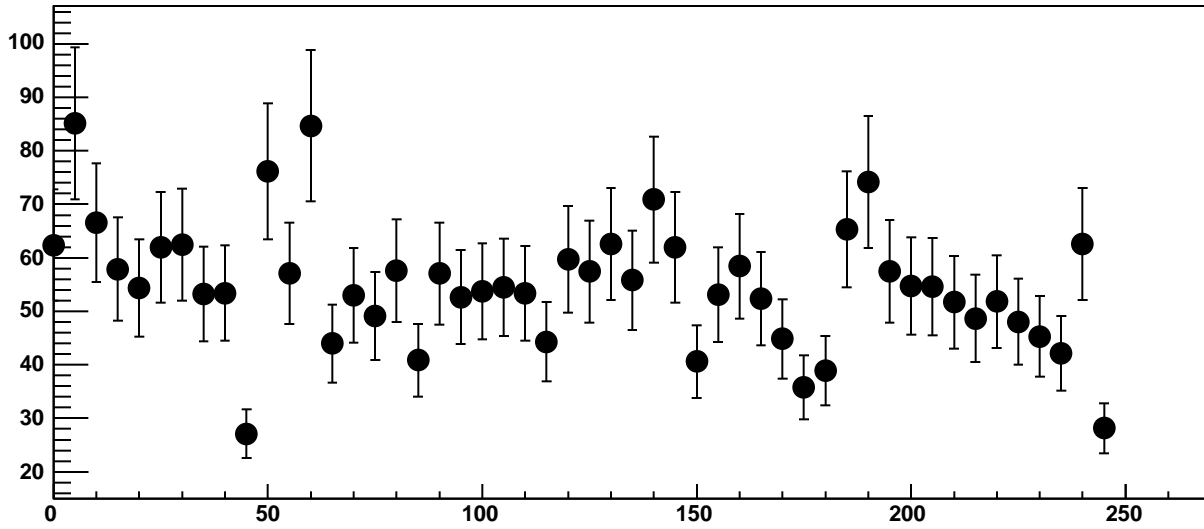


Chip 4, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

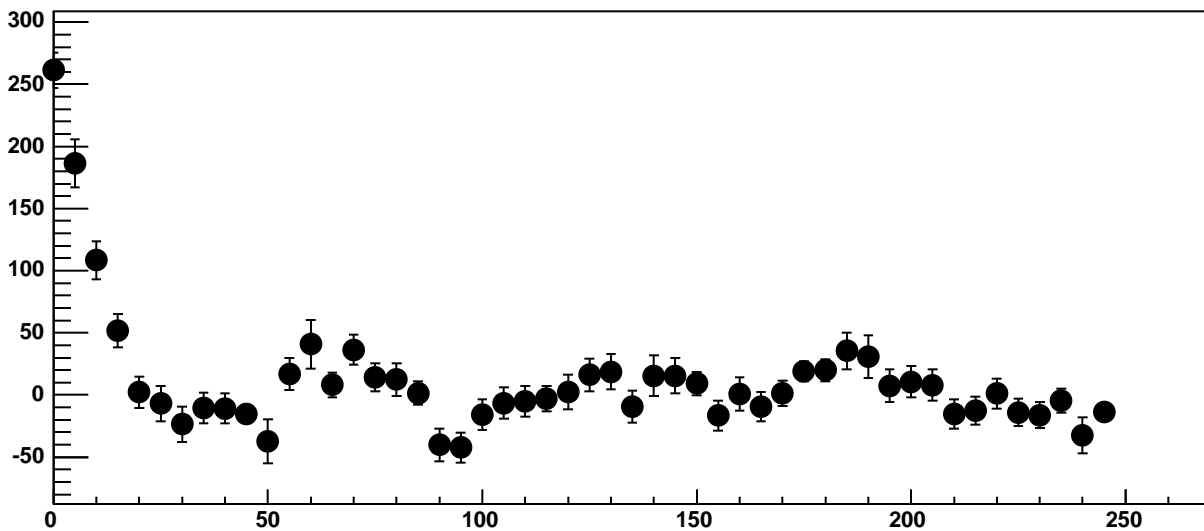


$\chi^2 / \text{ndf}$	114.6 / 41
p0	$-156.7 \pm 4.042$
p1	$94.53 \pm 0.5997$
p2	$-2.403\text{e}+08 \pm 4.808\text{e}+06$
p3	$1.922\text{e}+07 \pm 2.899\text{e}+05$
p4	$11.54 \pm 0.1318$

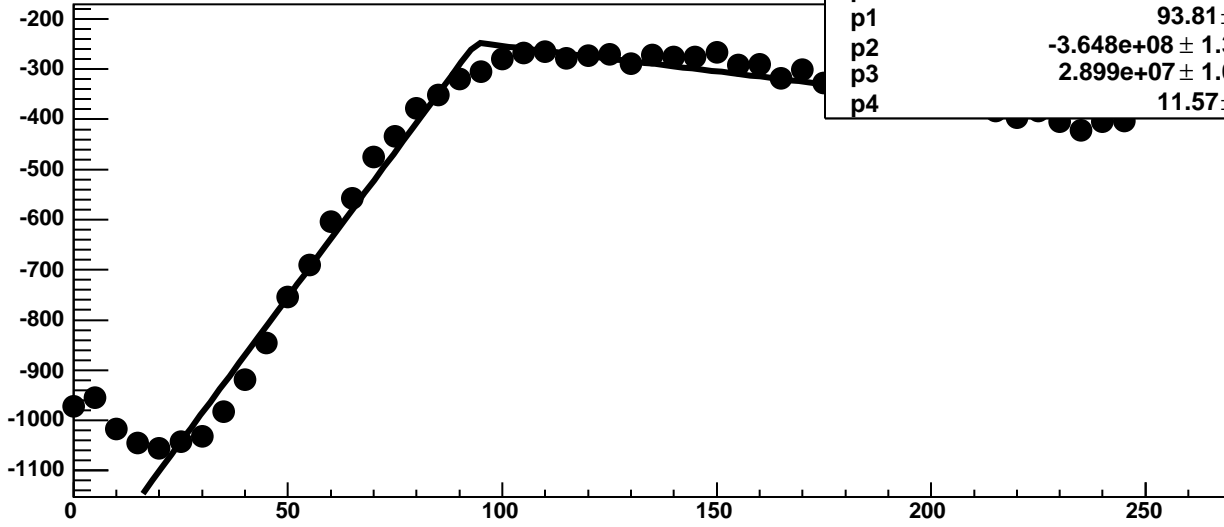
Chip 4, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

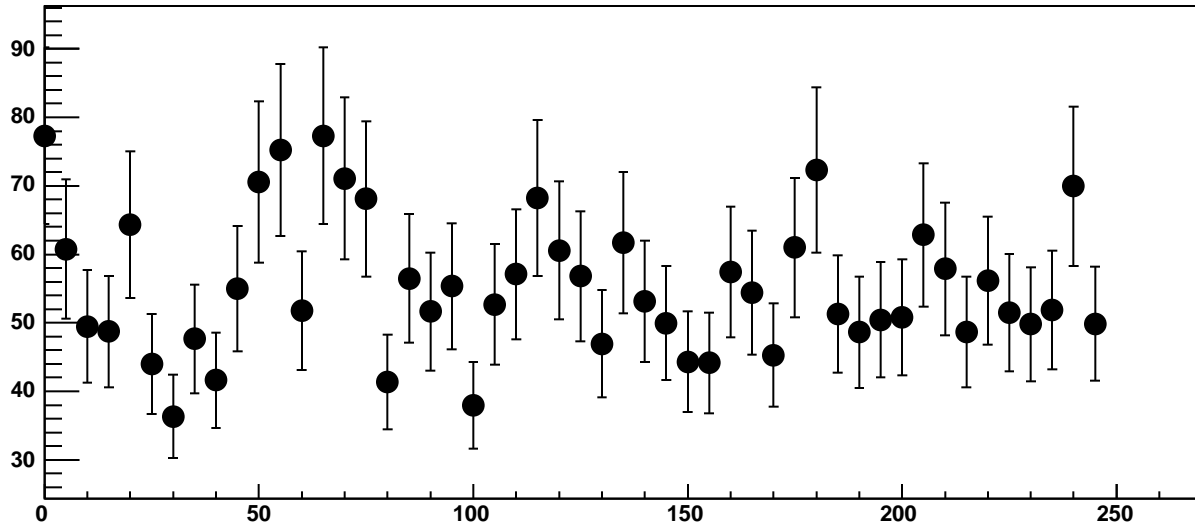


Chip 4, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold

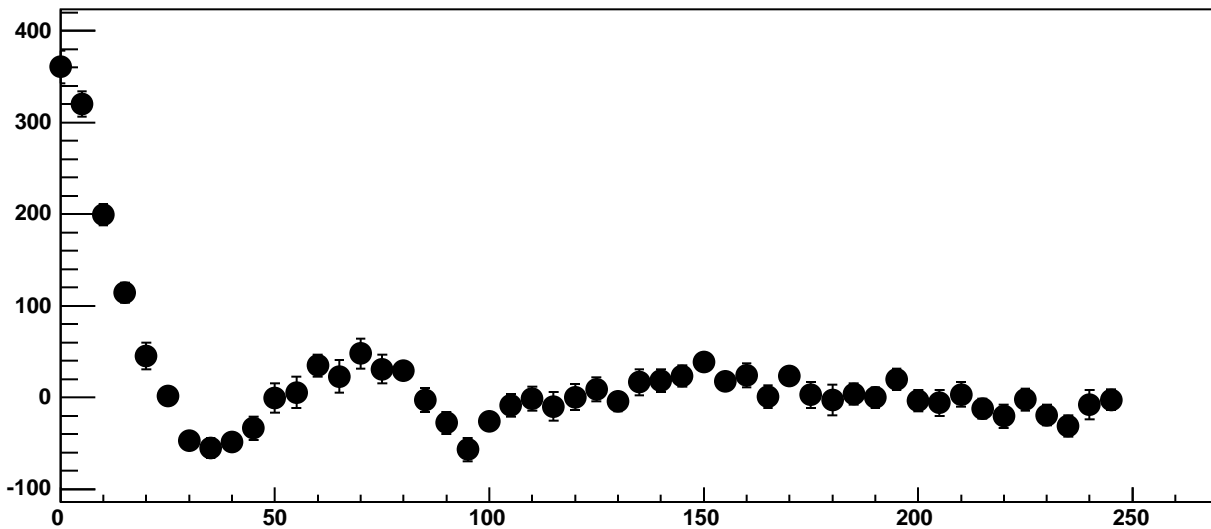


$\chi^2 / \text{ndf}$	323.9 / 41
p0	$-247.3 \pm 3.99$
p1	$93.81 \pm 0.6188$
p2	$-3.648\text{e}+08 \pm 1.387\text{e}+07$
p3	$2.899\text{e}+07 \pm 1.085\text{e}+06$
p4	$11.57 \pm 0.1269$

Chip 4, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

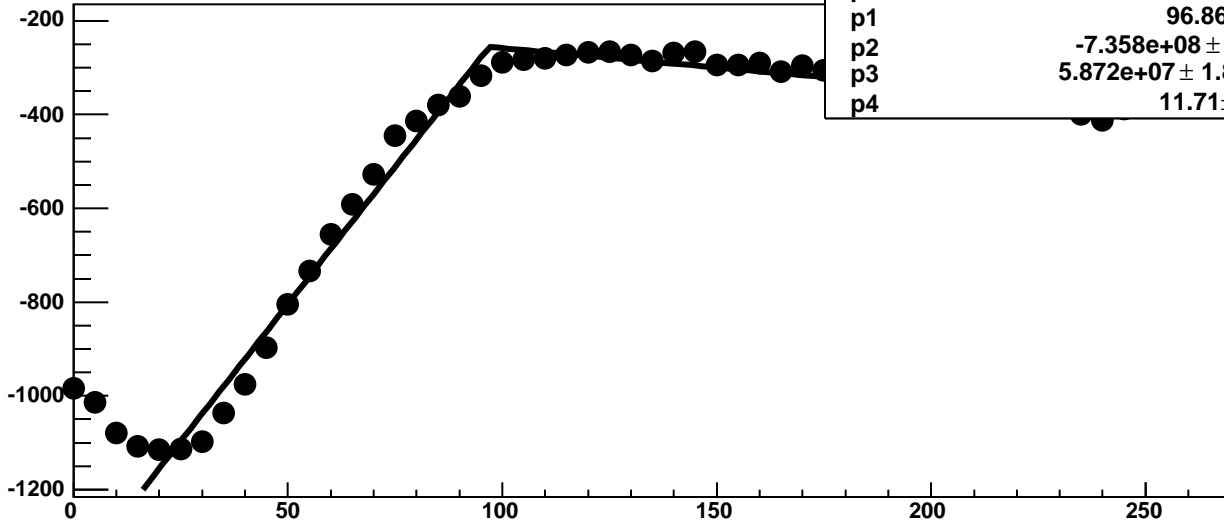


Chip 4, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold



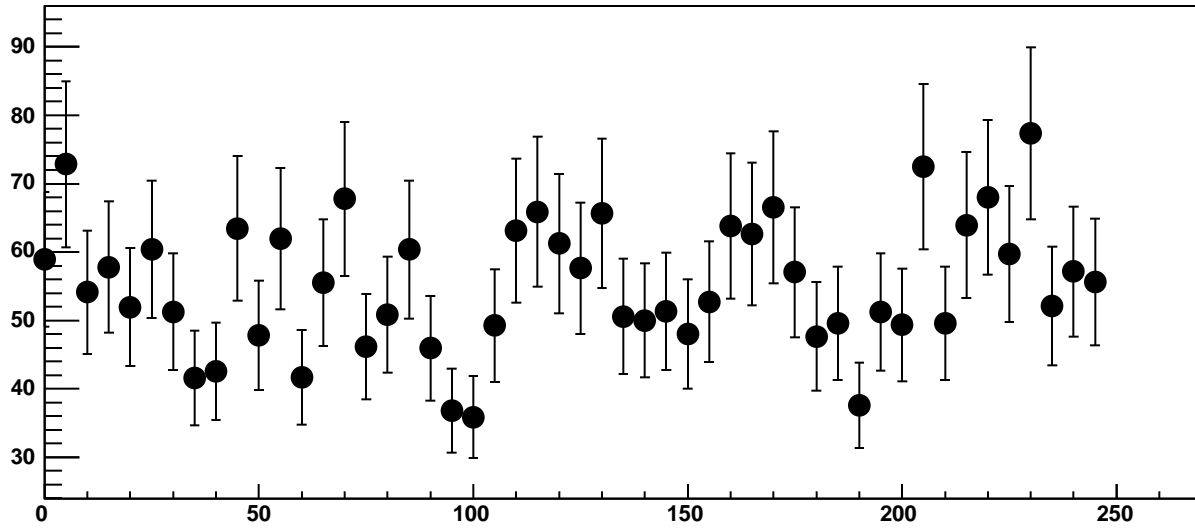


Chip 4, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

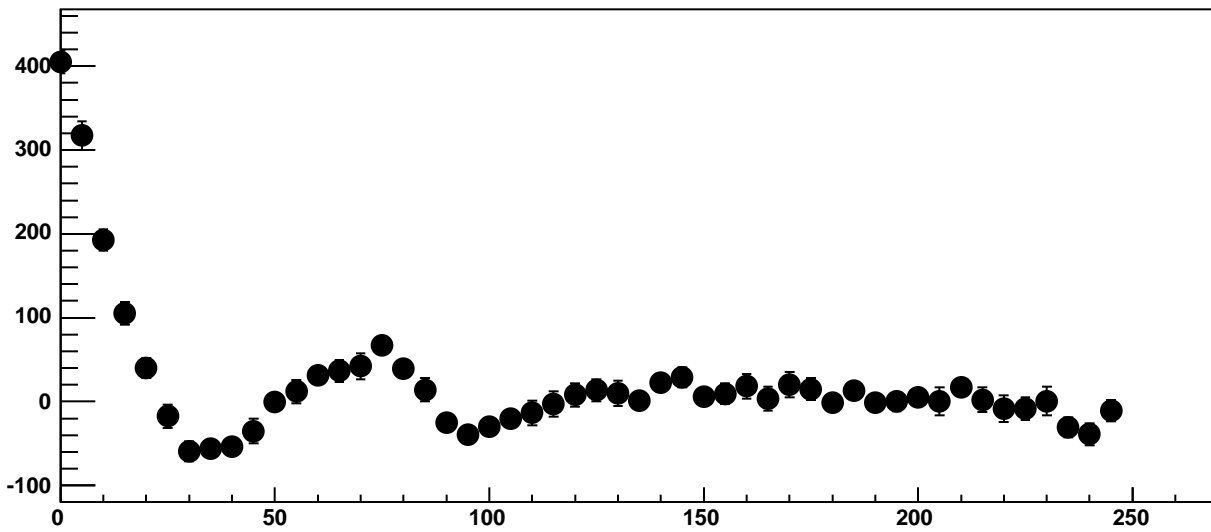


$\chi^2 / \text{ndf}$	332.4 / 41
p0	$-255.6 \pm 4.186$
p1	$96.86 \pm 0.545$
p2	$-7.358\text{e}+08 \pm 2.4\text{e}+07$
p3	$5.872\text{e}+07 \pm 1.825\text{e}+06$
p4	$11.71 \pm 0.1104$

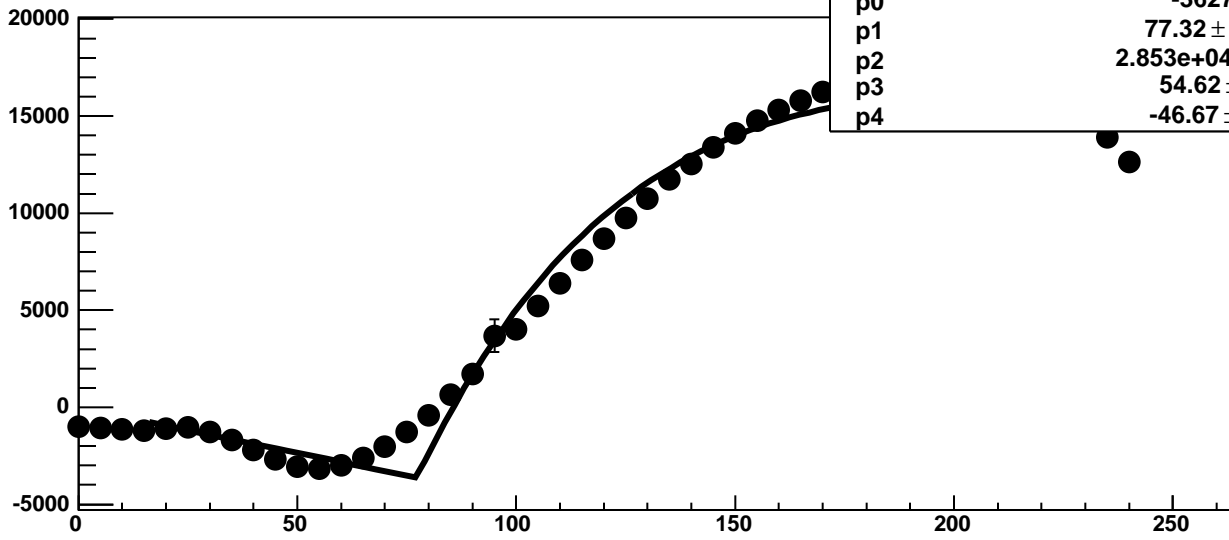
Chip 4, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

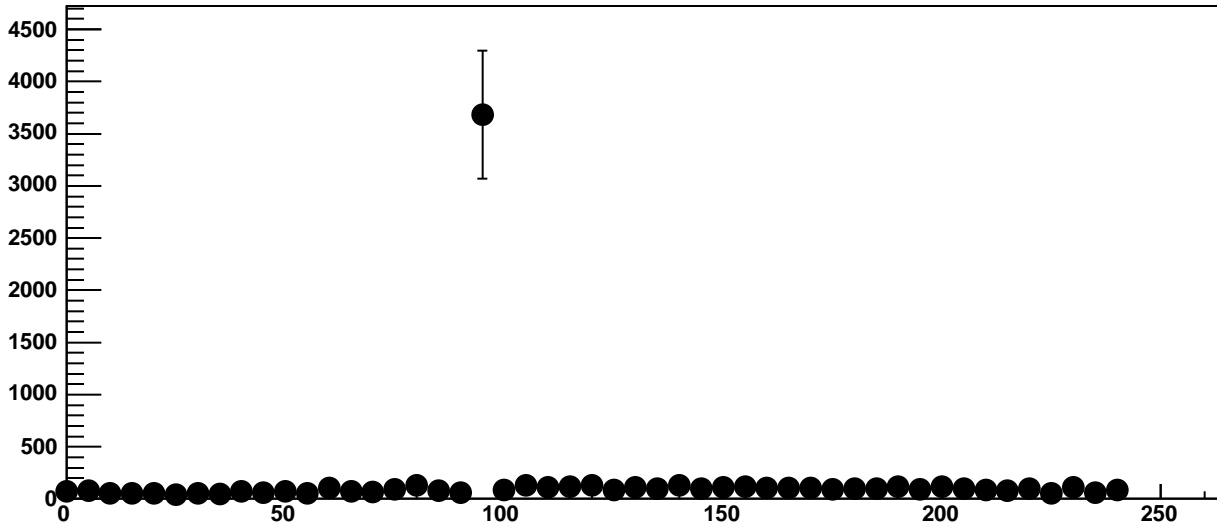


Chip 4, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

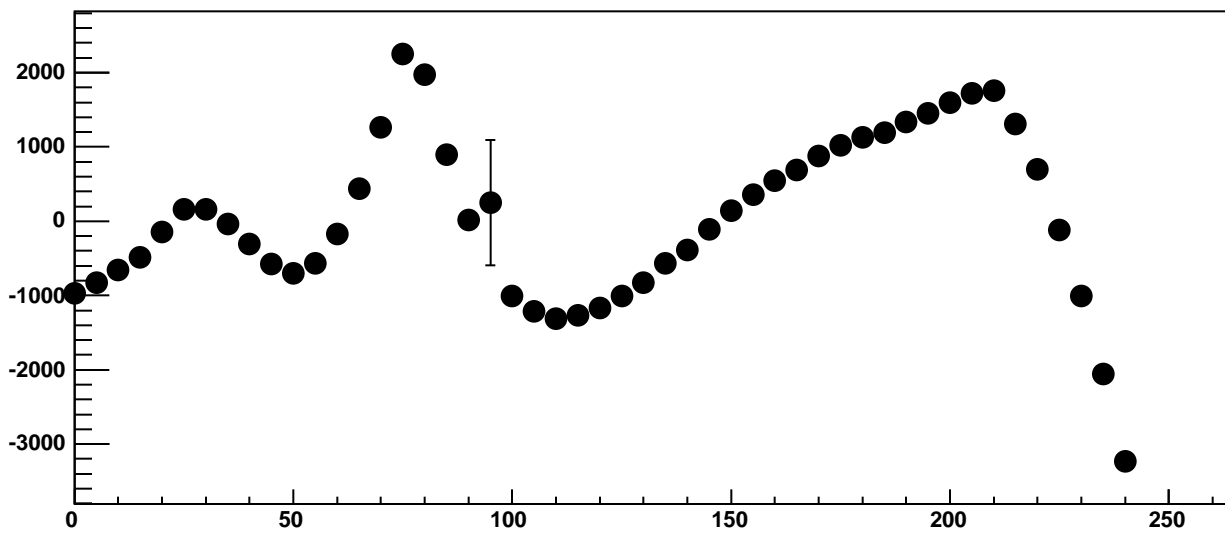


$\chi^2 / \text{ndf}$	1.417e+05 / 41
p0	-3627 ± 7.726
p1	77.32 ± 0.03323
p2	2.853e+04 ± 45.94
p3	54.62 ± 0.1032
p4	-46.67 ± 0.1965

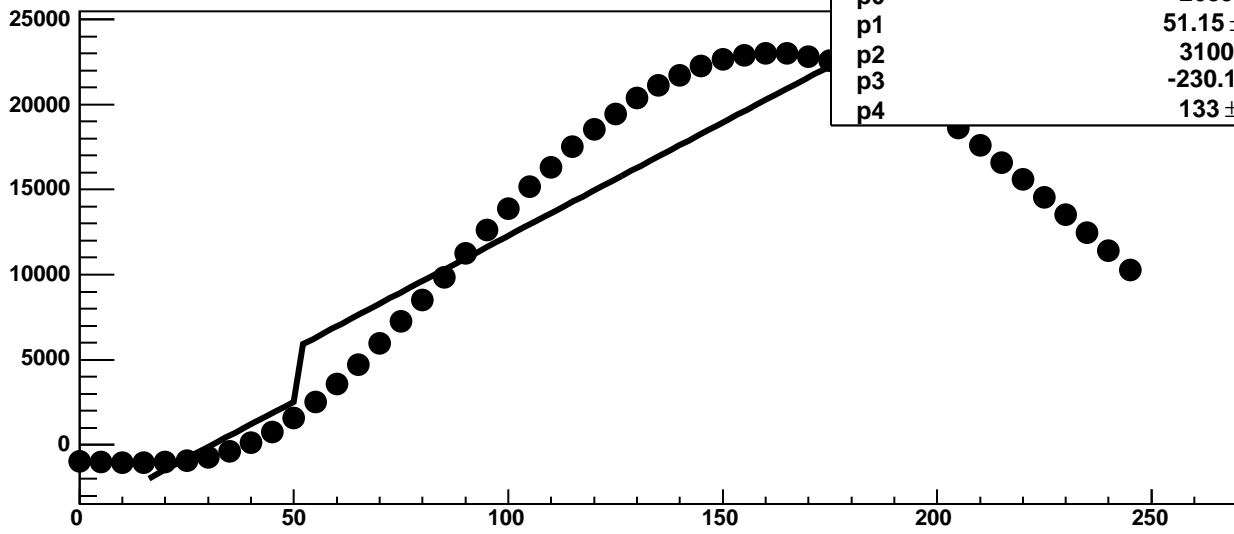
Chip 4, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



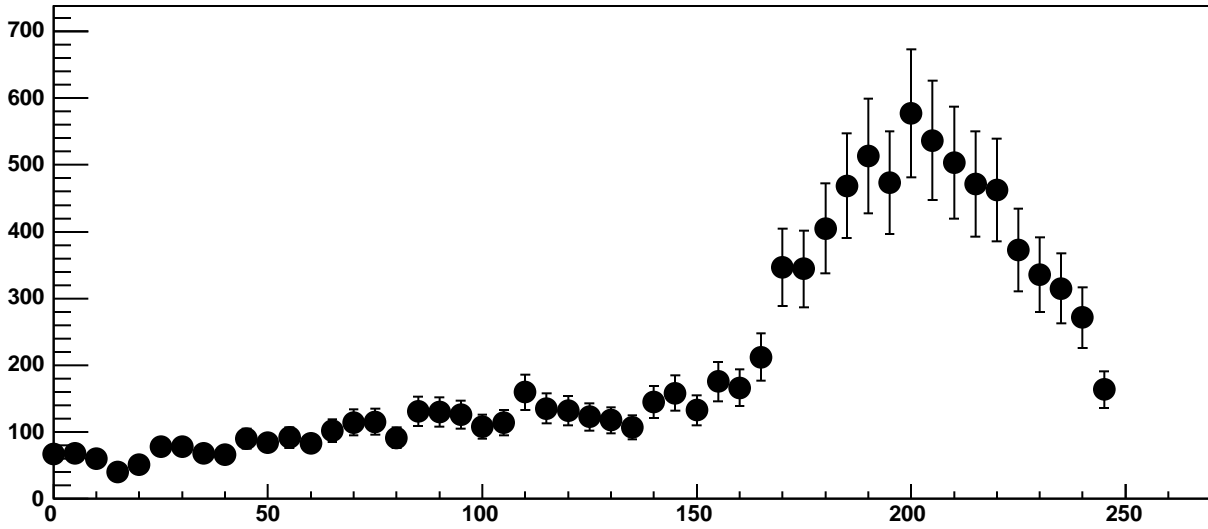
Chip 4, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold



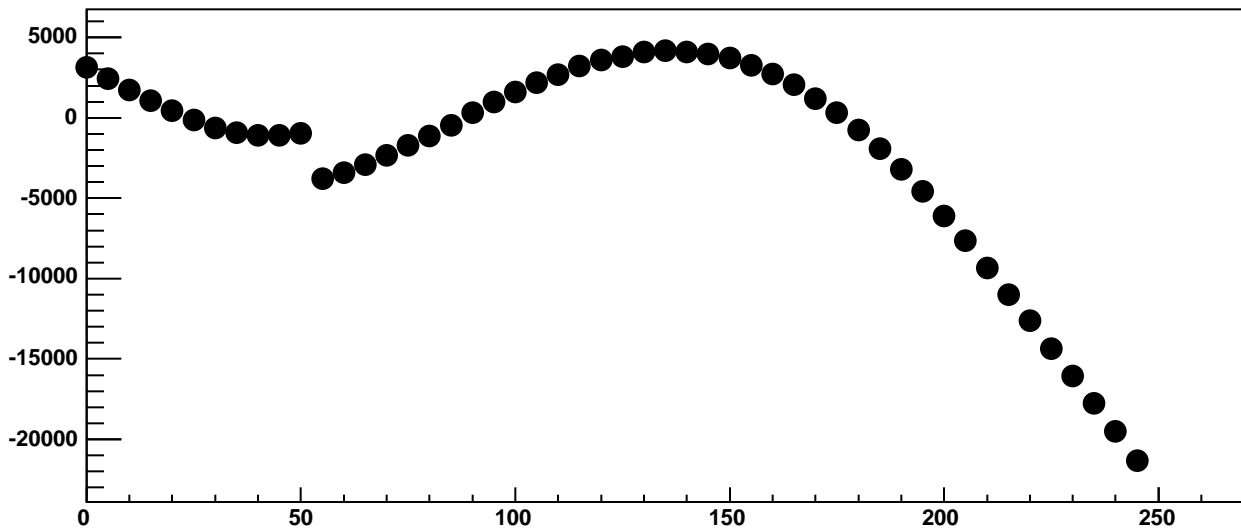
Chip 4, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold



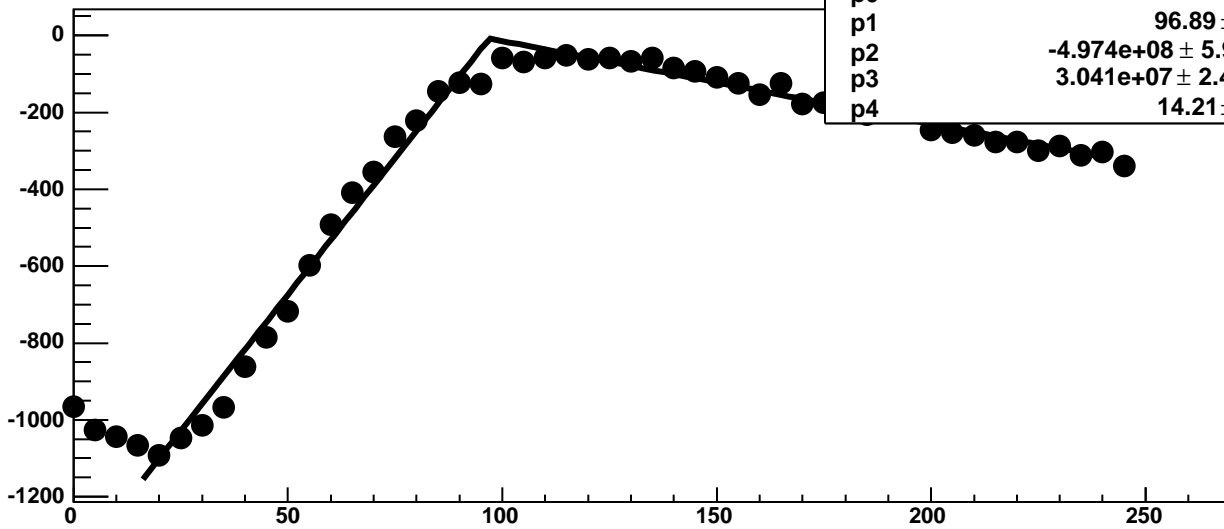
Chip 4, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold

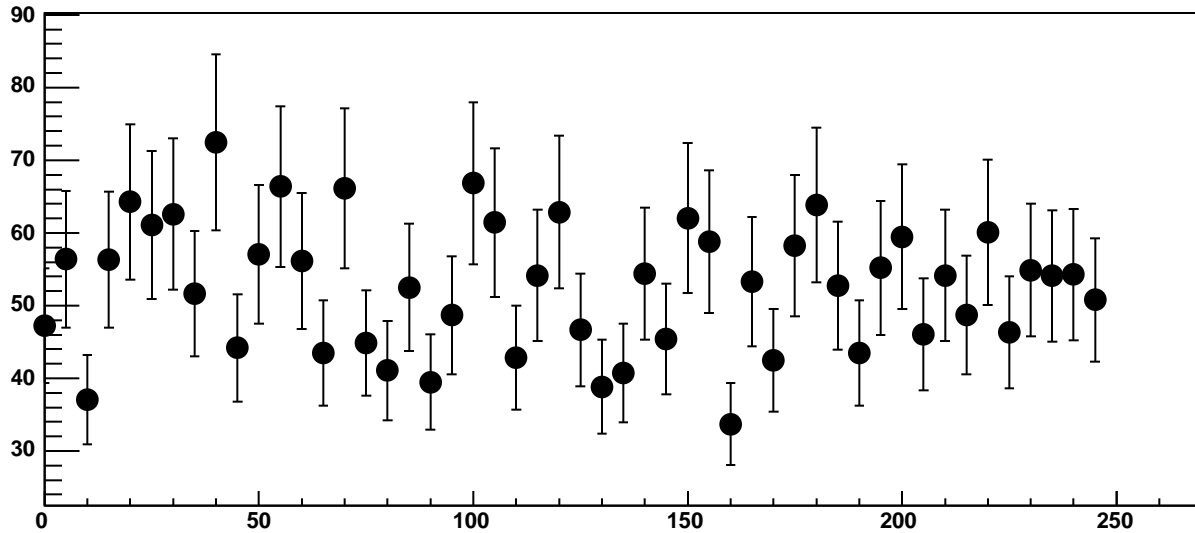


Chip 4, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

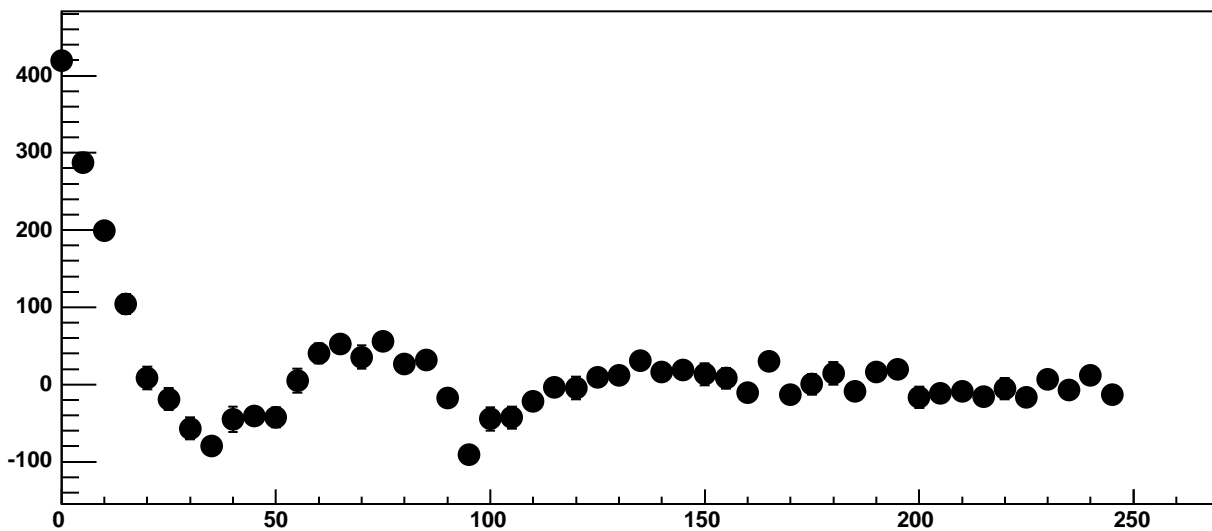


$\chi^2 / \text{ndf}$	387.9 / 41
p0	$-7.832 \pm 3.876$
p1	$96.89 \pm 0.4159$
p2	$-4.974\text{e}+08 \pm 5.914\text{e}+06$
p3	$3.041\text{e}+07 \pm 2.479\text{e}+05$
p4	$14.21 \pm 0.1185$

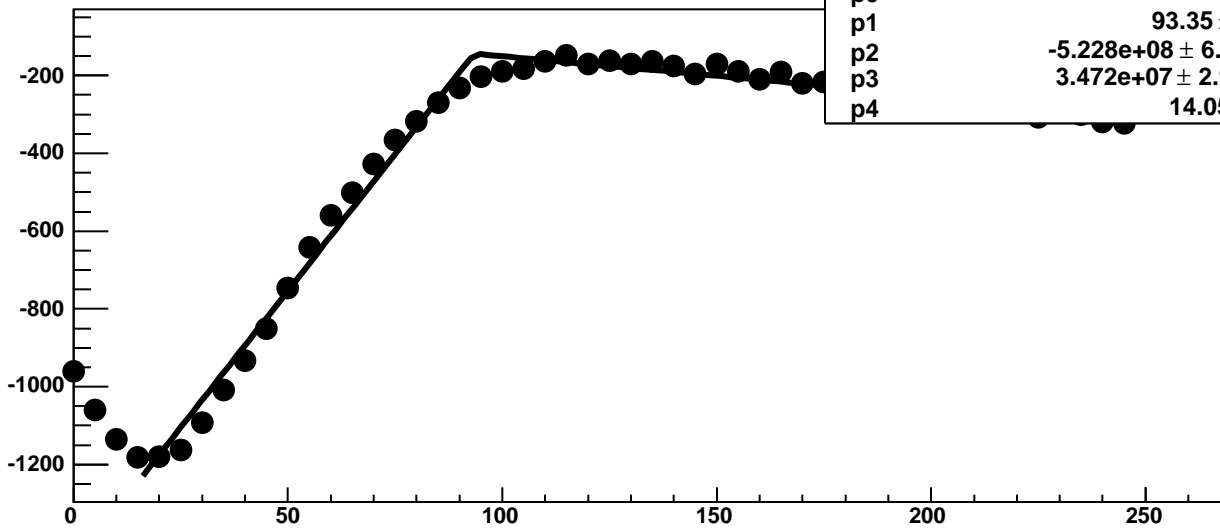
Chip 4, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

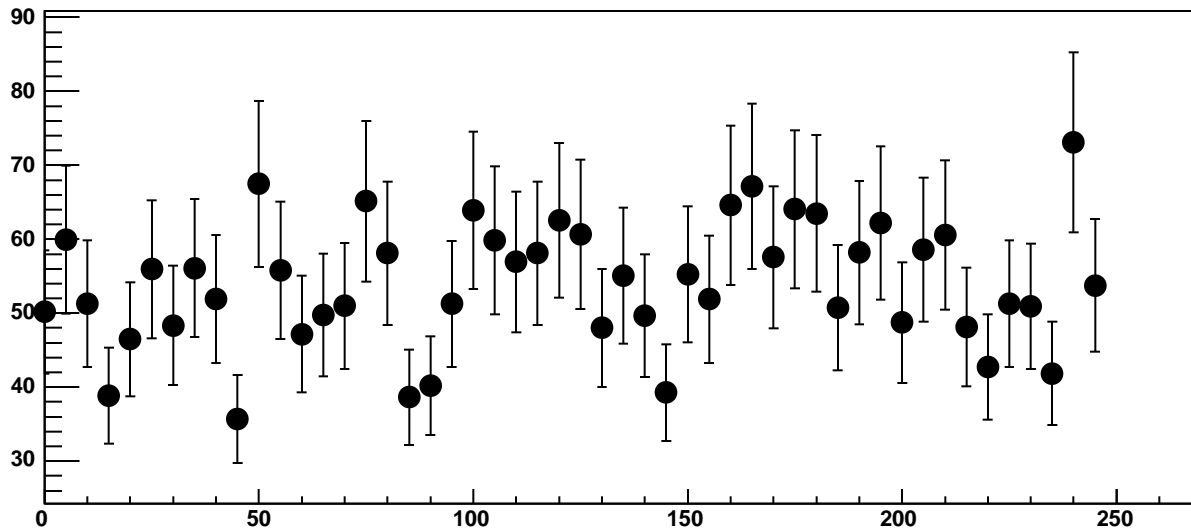


Chip 4, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

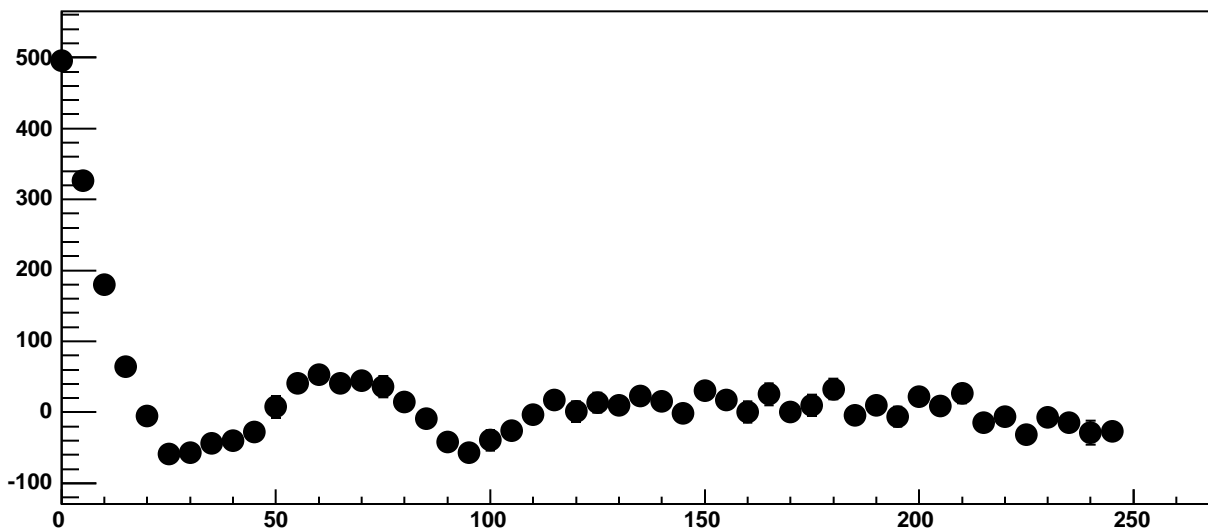


$\chi^2 / \text{ndf}$	308.1 / 41
p0	$-144 \pm 4.312$
p1	$93.35 \pm 0.4676$
p2	$-5.228\text{e}+08 \pm 6.466\text{e}+06$
p3	$3.472\text{e}+07 \pm 2.923\text{e}+05$
p4	$14.05 \pm 0.112$

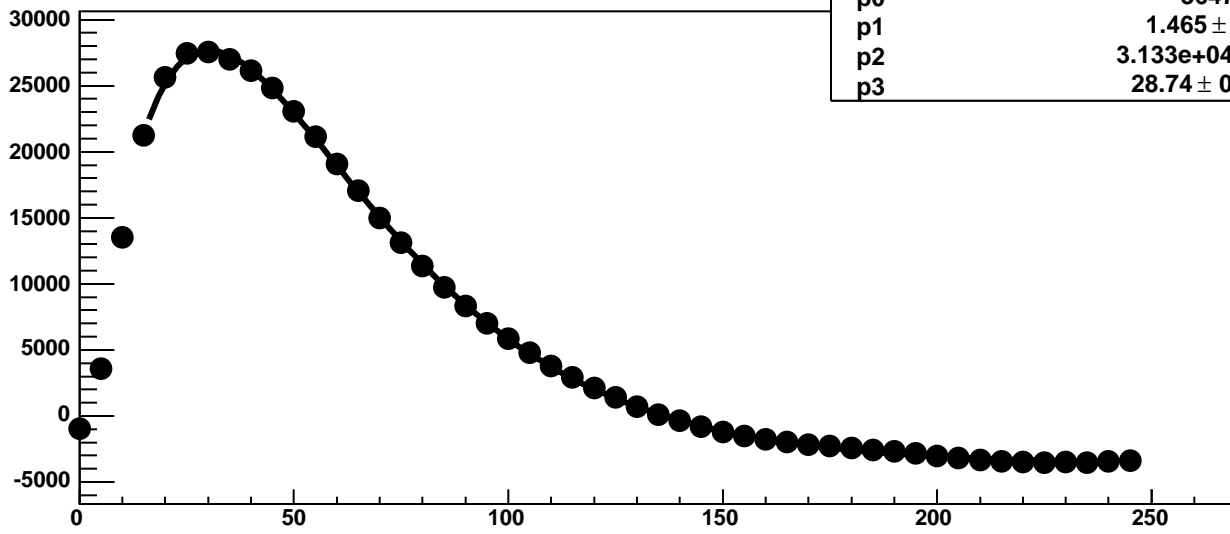
Chip 4, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

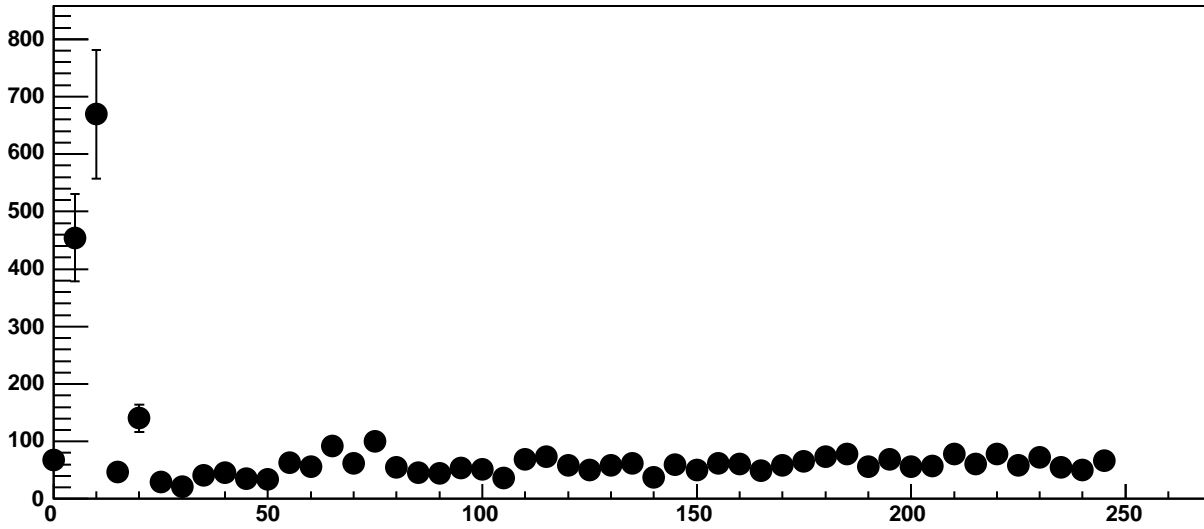


Chip 4, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold

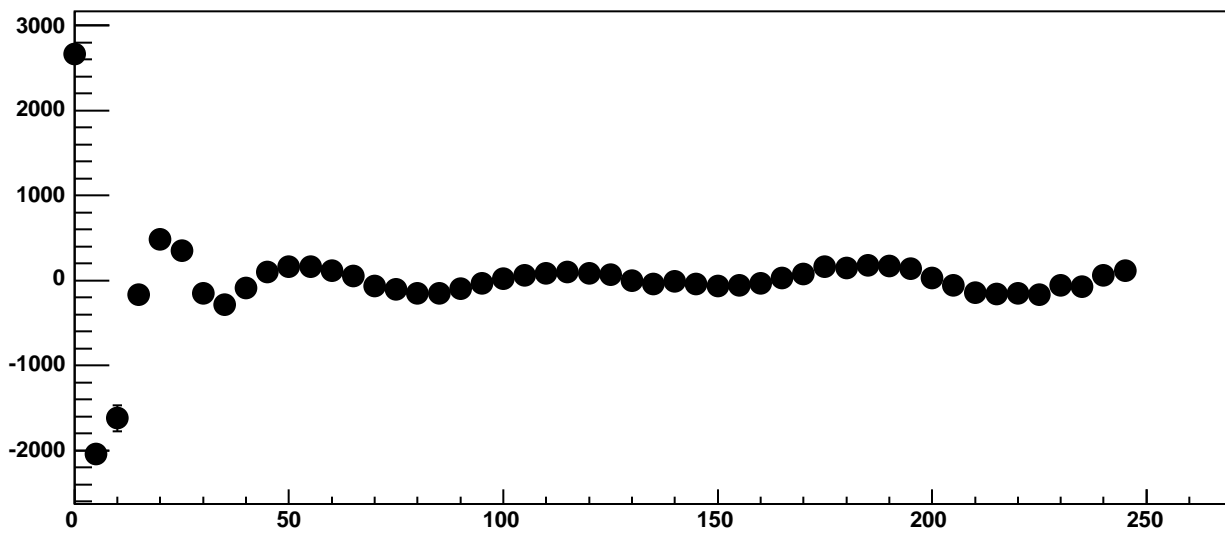


$\chi^2 / \text{ndf}$	7788 / 42
p0	-3647 $\pm$ 3.789
p1	1.465 $\pm$ 0.01296
p2	3.133e+04 $\pm$ 4.433
p3	28.74 $\pm$ 0.008868

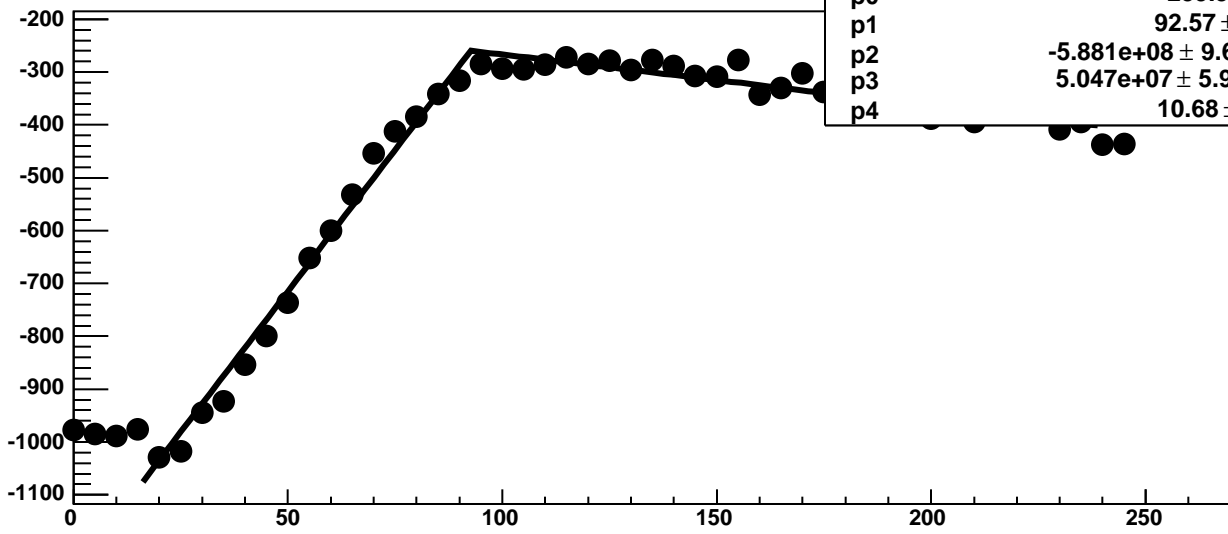
Chip 4, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold

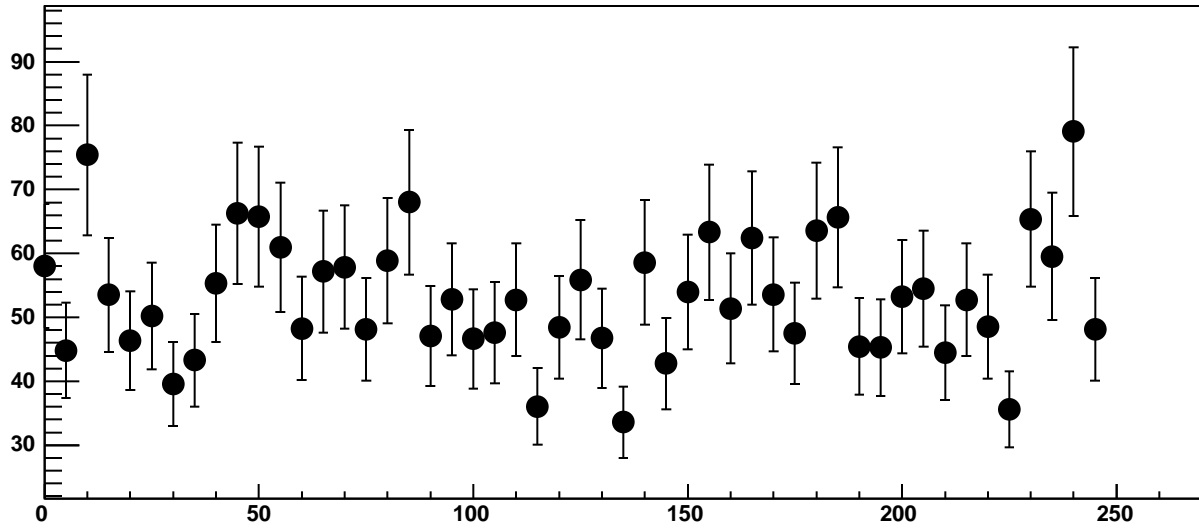


Chip 4, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

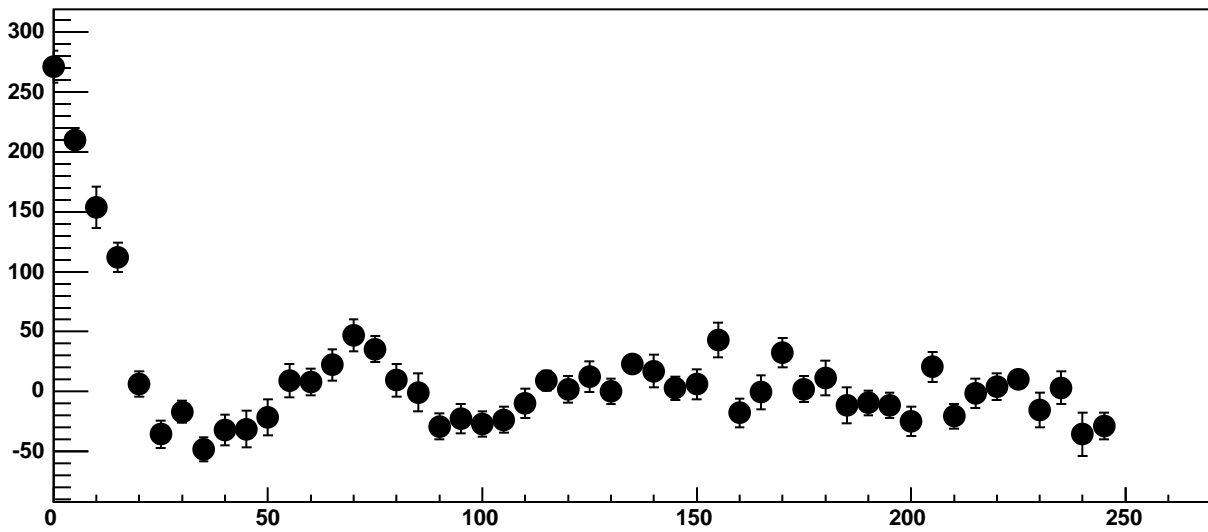


$\chi^2 / \text{ndf}$	234.8 / 41
p0	$-259.5 \pm 3.702$
p1	$92.57 \pm 0.6329$
p2	$-5.881\text{e}+08 \pm 9.653\text{e}+06$
p3	$5.047\text{e}+07 \pm 5.917\text{e}+05$
p4	$10.68 \pm 0.1271$

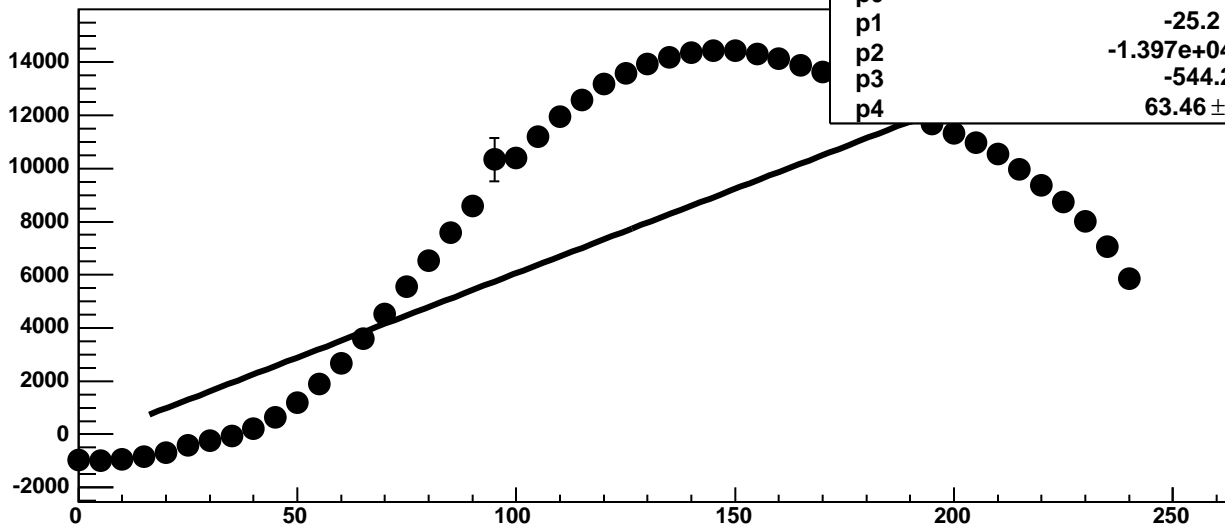
Chip 4, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

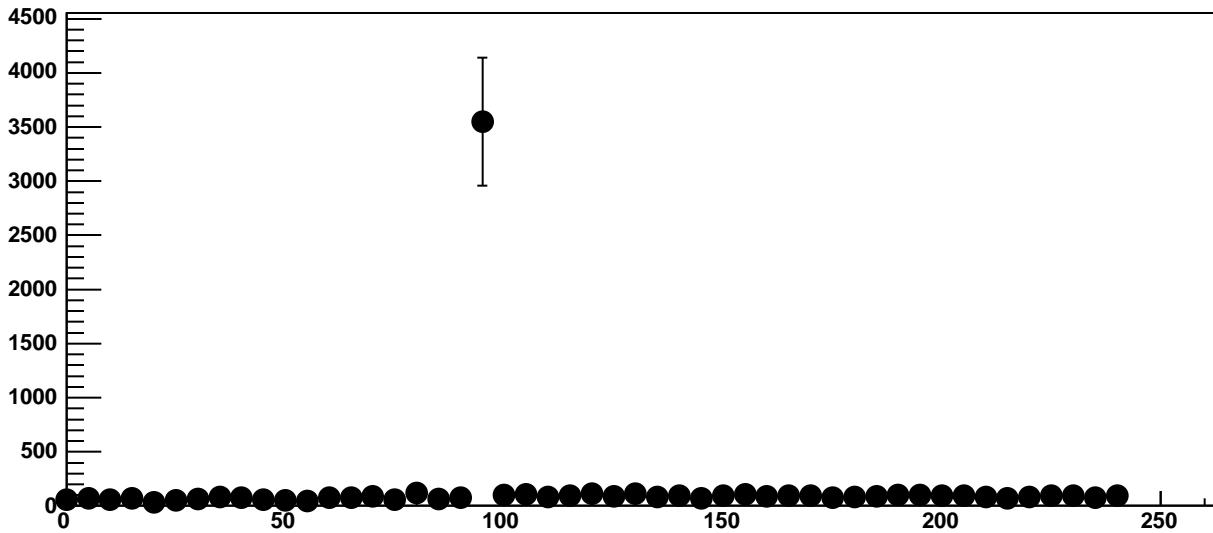


Chip 4, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

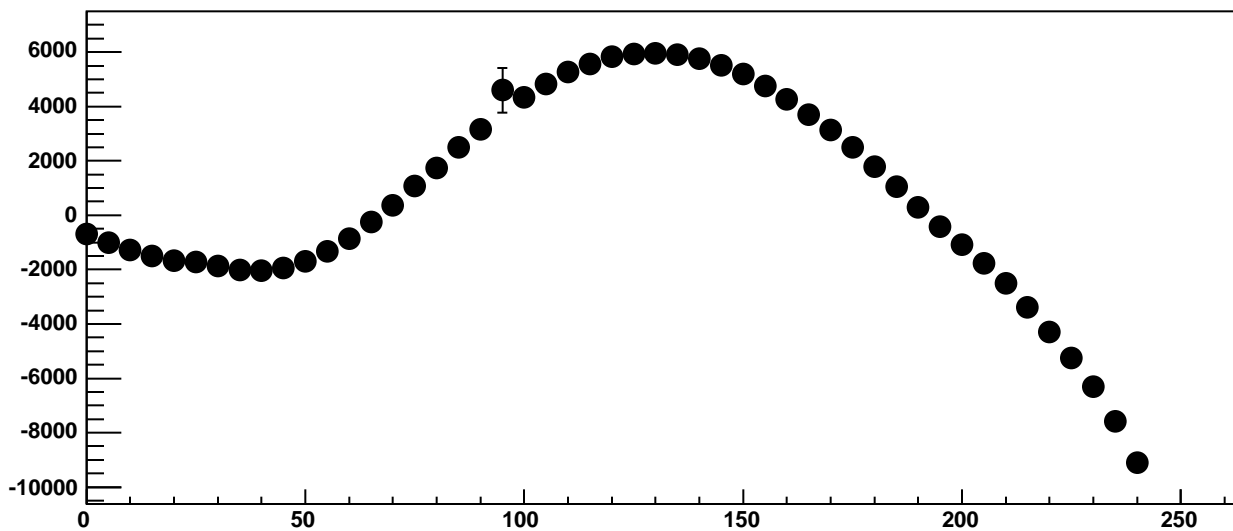


$\chi^2 / \text{ndf}$	1.764e+06 / 41
p0	1.208e+04 ± 22.22
p1	-25.2 ± 0.3709
p2	-1.397e+04 ± 6.388
p3	-544.2 ± 3.808
p4	63.46 ± 0.04228

Chip 4, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



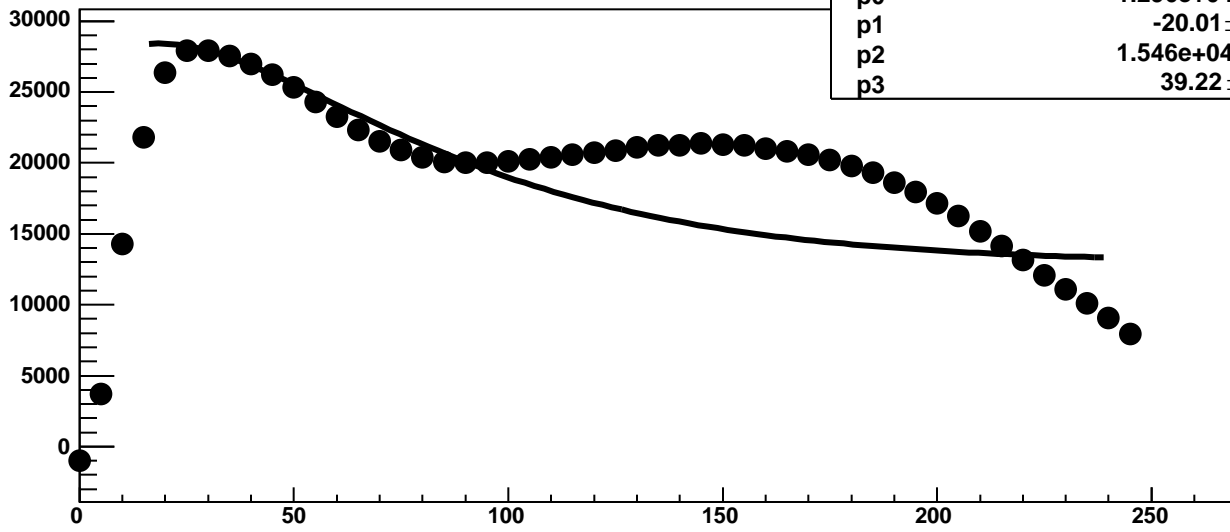
Chip 4, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



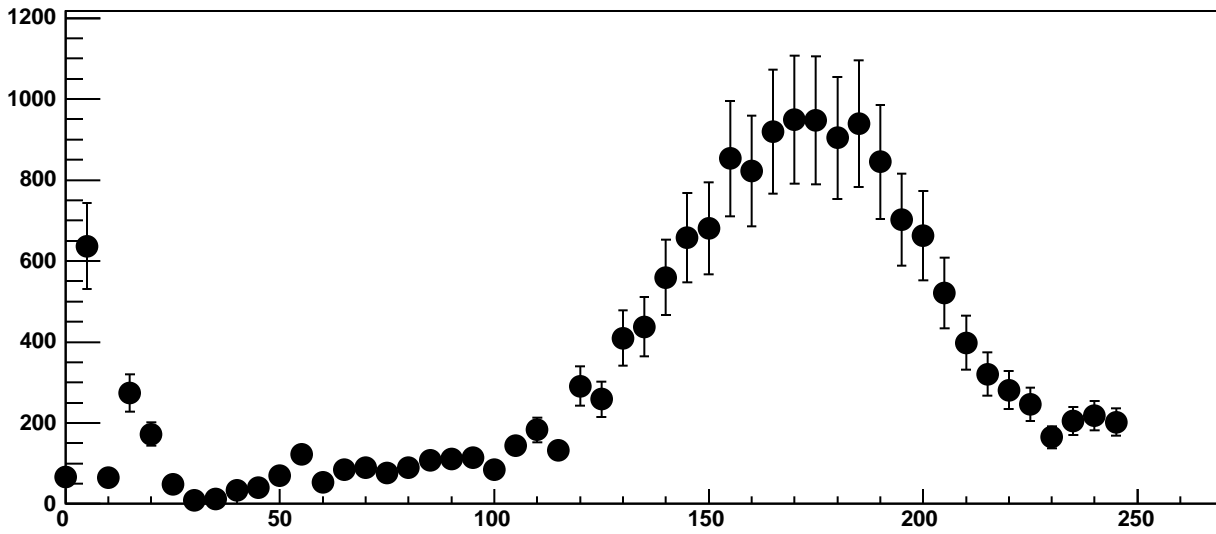


Chip 4, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold

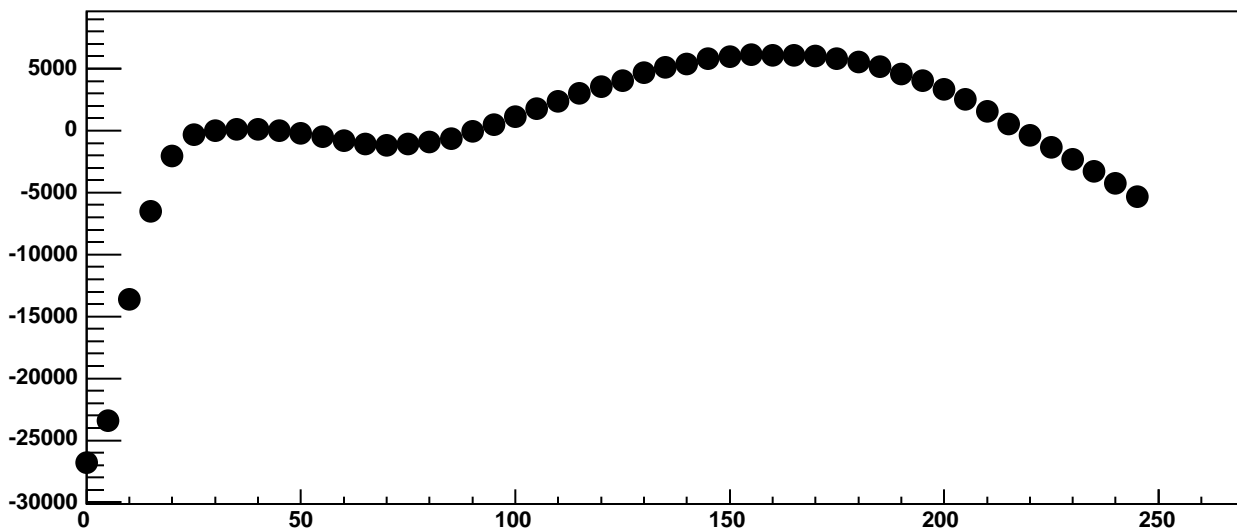
$\chi^2 / \text{ndf}$	9.475e+04 / 42
p0	1.296e+04 $\pm$ 31.44
p1	-20.01 $\pm$ 0.3475
p2	1.546e+04 $\pm$ 41.34
p3	39.22 $\pm$ 0.1703



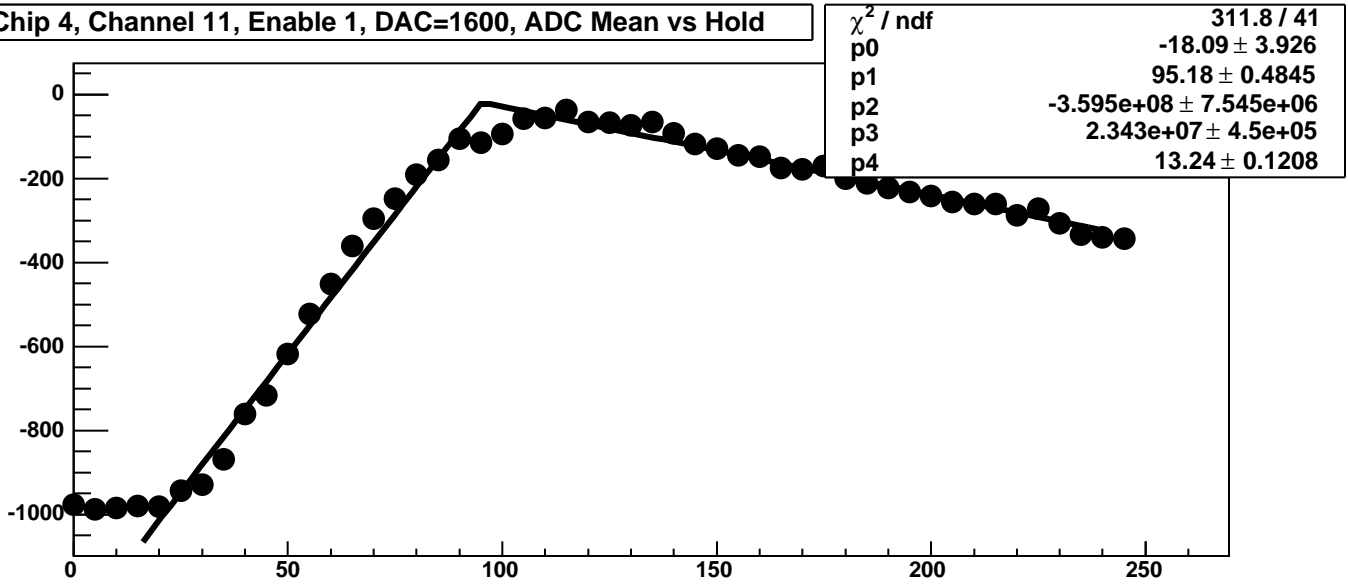
Chip 4, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



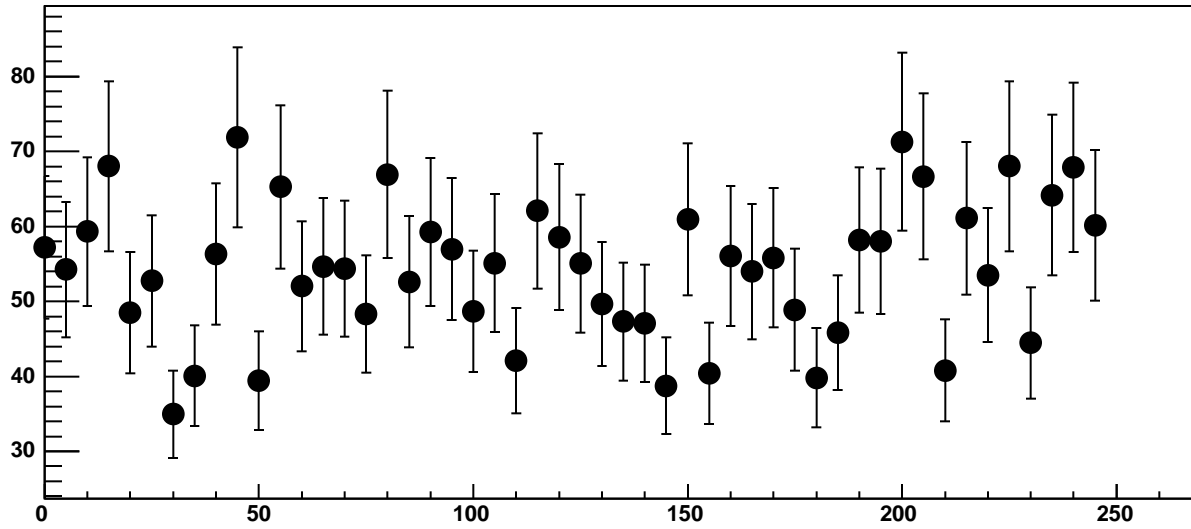
Chip 4, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold



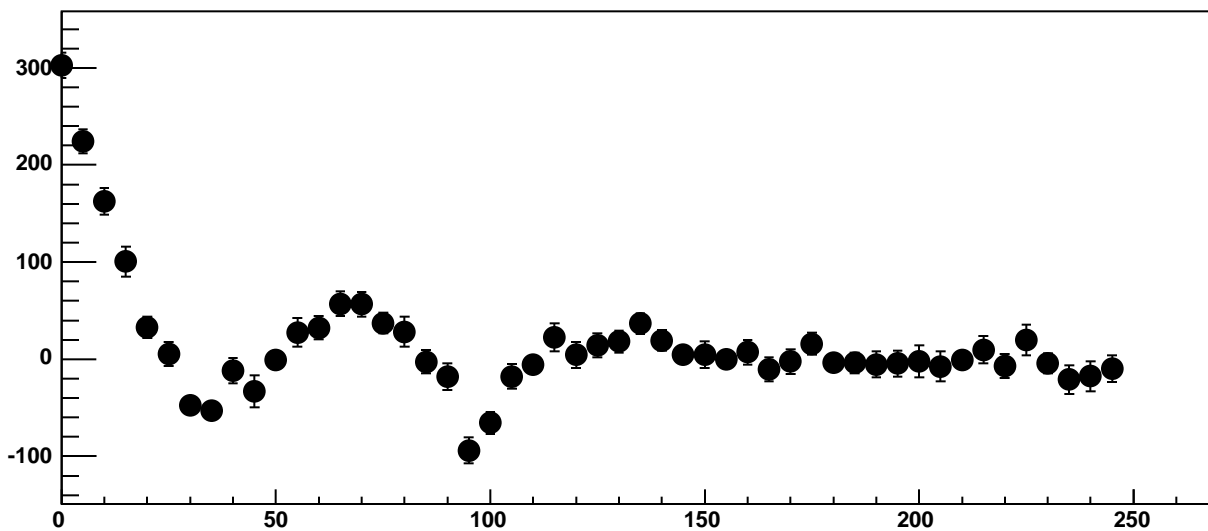
Chip 4, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold



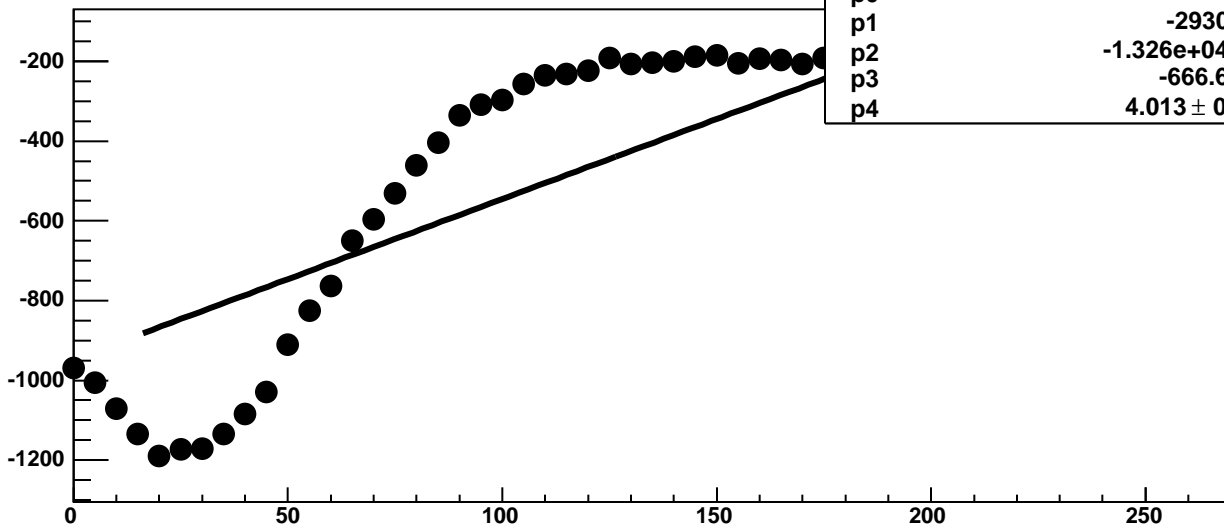
Chip 4, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

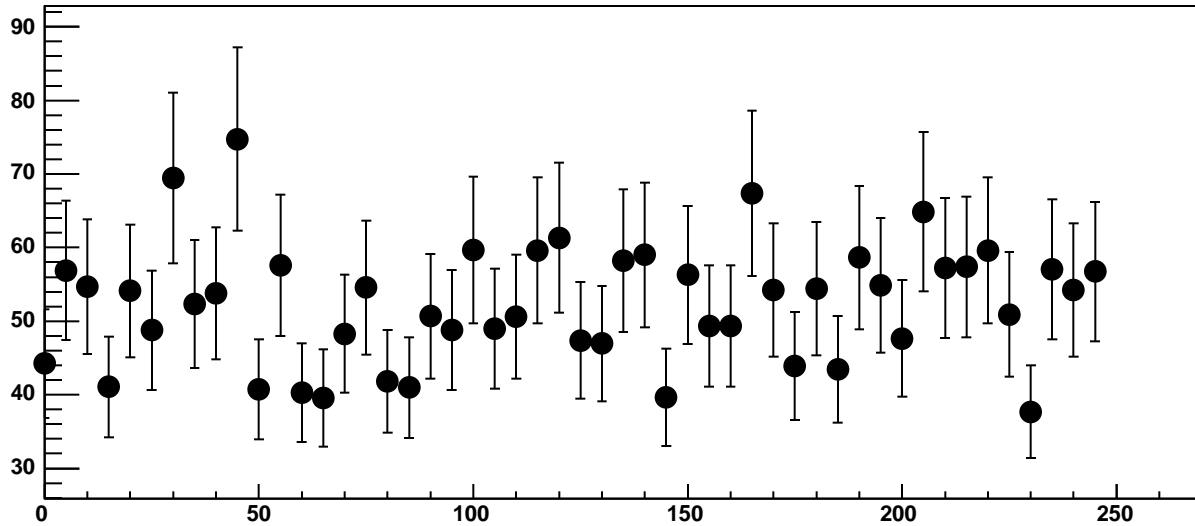


Chip 4, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

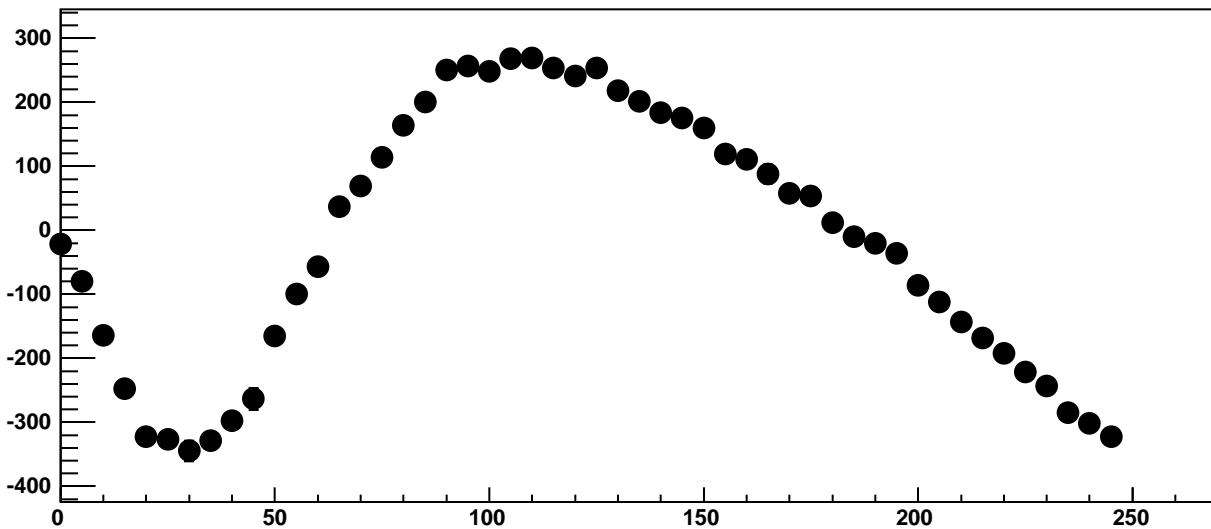


$\chi^2 / \text{ndf}$	1.361e+04 / 41
p0	553.4 ± 11.32
p1	-2930 ± 1.158
p2	-1.326e+04 ± 2.228
p3	-666.6 ± 18.82
p4	4.013 ± 0.003694

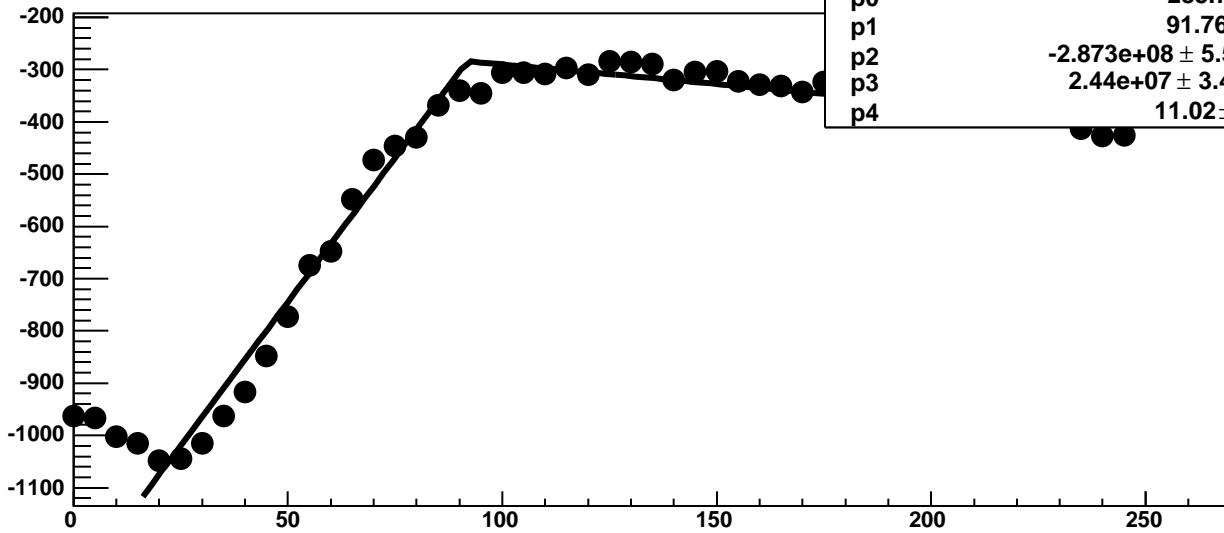
Chip 4, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

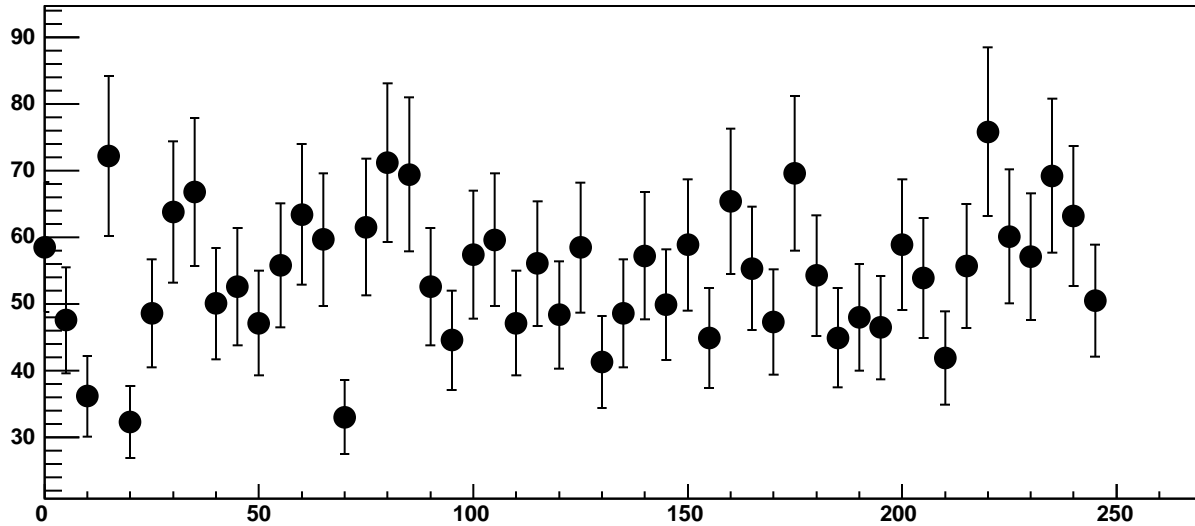


Chip 4, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold

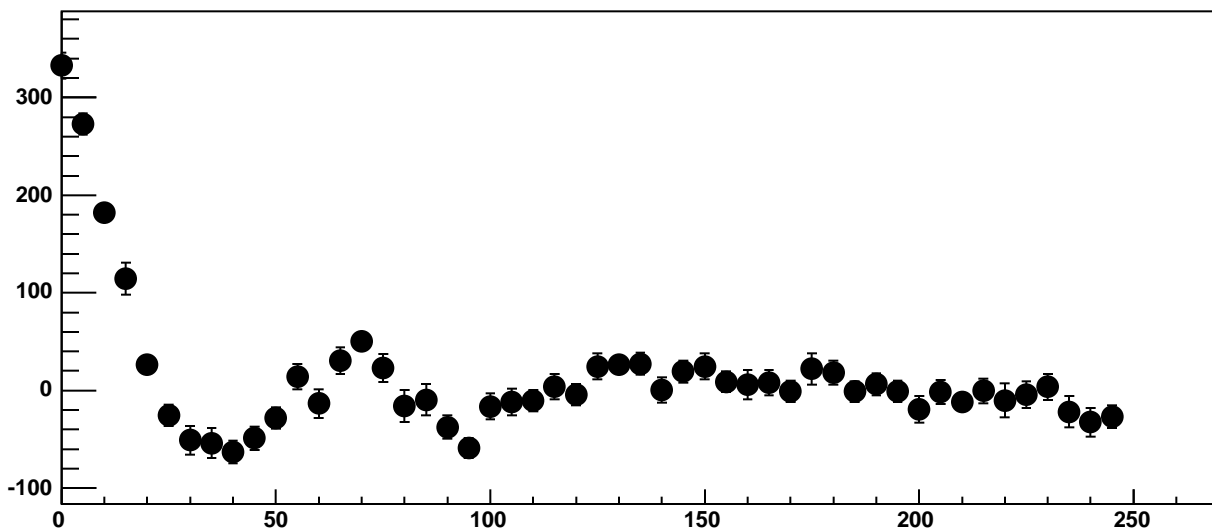


$\chi^2 / \text{ndf}$	283.9 / 41
p0	$-283.7 \pm 4.156$
p1	$91.76 \pm 0.639$
p2	$-2.873\text{e}+08 \pm 5.519\text{e}+06$
p3	$2.44\text{e}+07 \pm 3.414\text{e}+05$
p4	$11.02 \pm 0.1286$

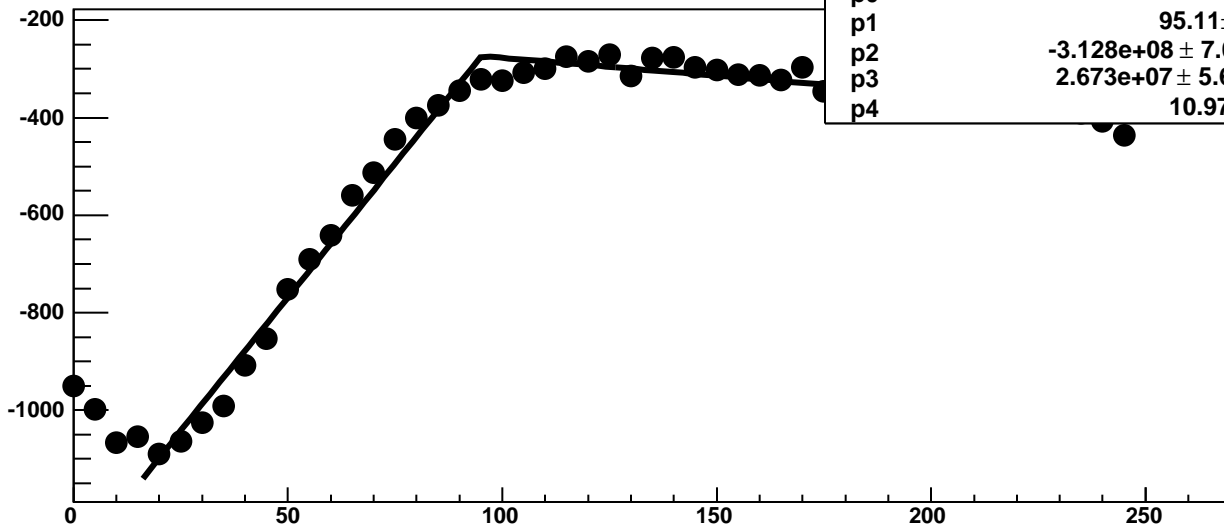
Chip 4, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

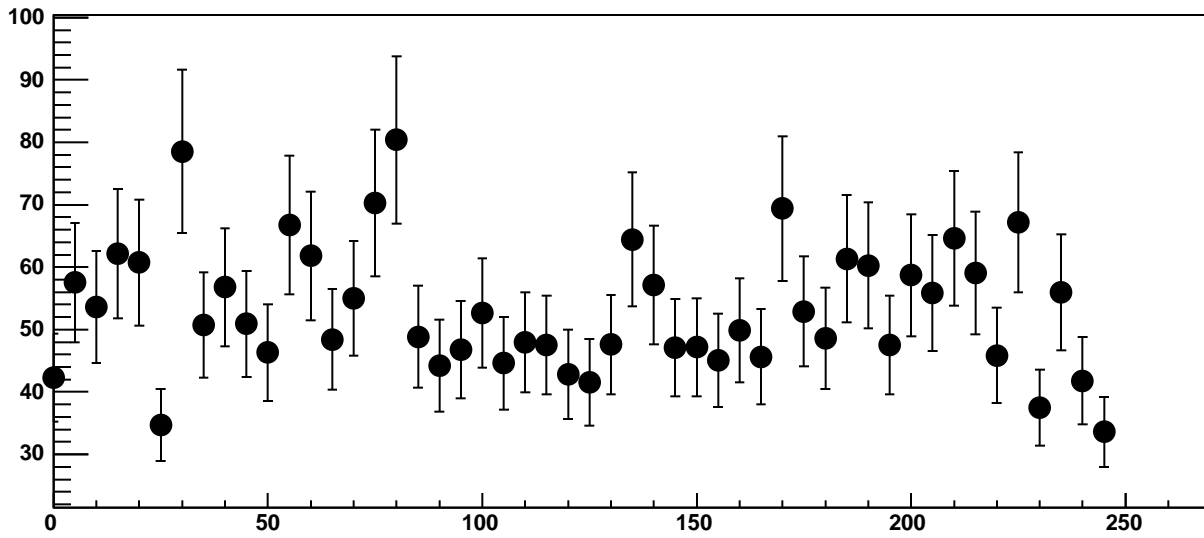


Chip 4, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

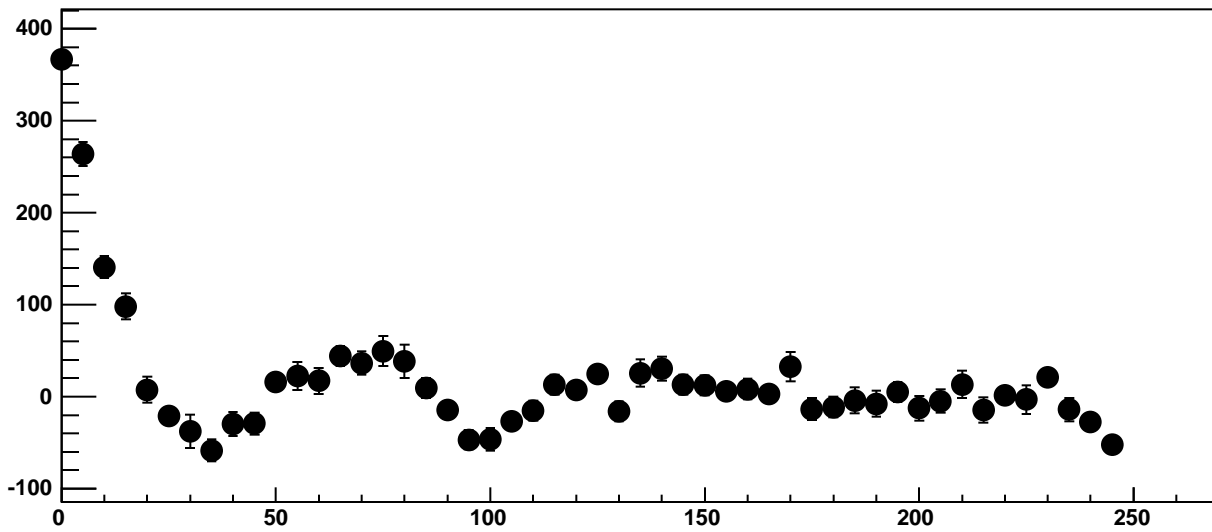


$\chi^2 / \text{ndf}$	233.3 / 41
p0	-273.6 ± 3.918
p1	95.11 ± 0.5892
p2	-3.128e+08 ± 7.016e+06
p3	2.673e+07 ± 5.651e+05
p4	10.97 ± 0.116

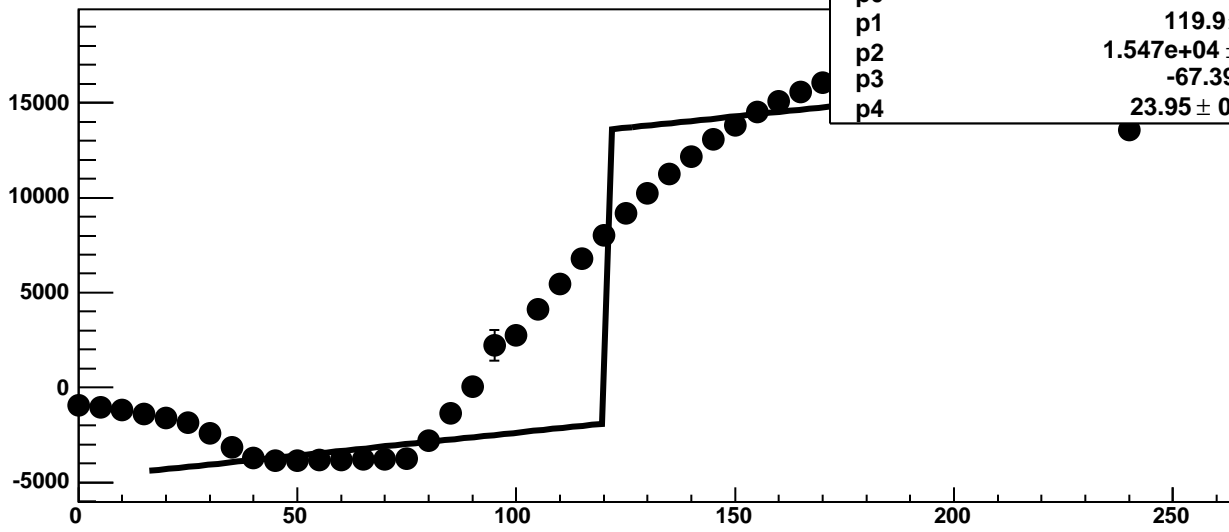
Chip 4, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



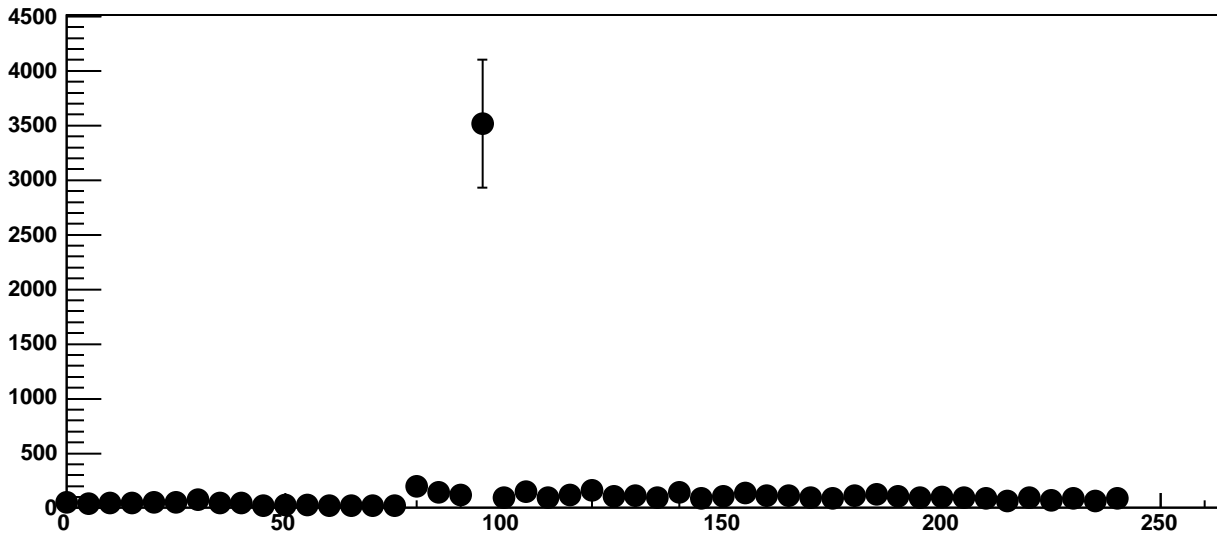
Chip 4, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold



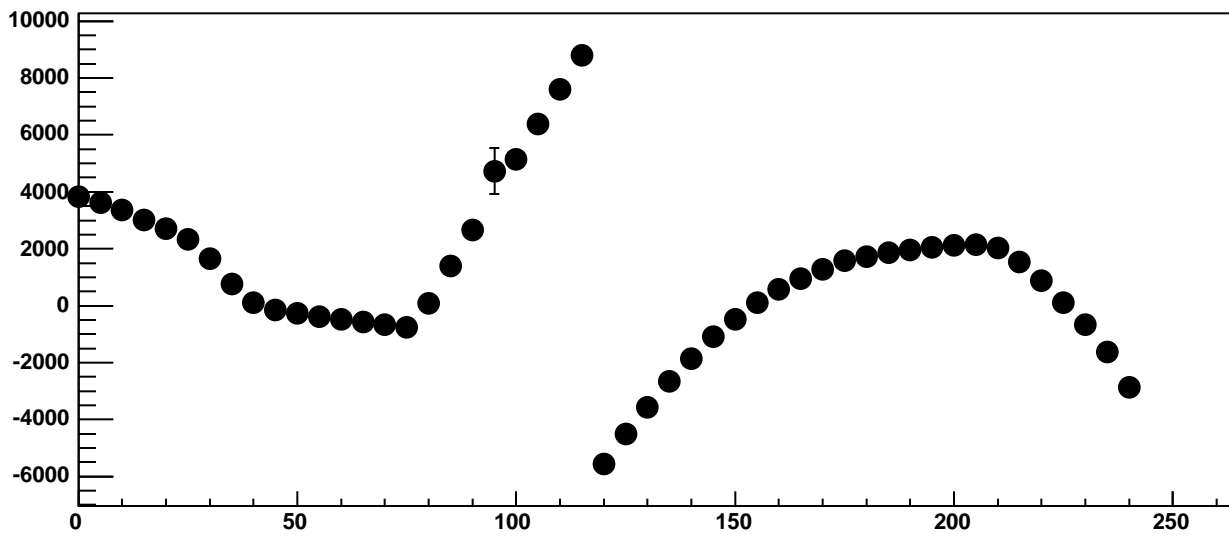
Chip 4, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold



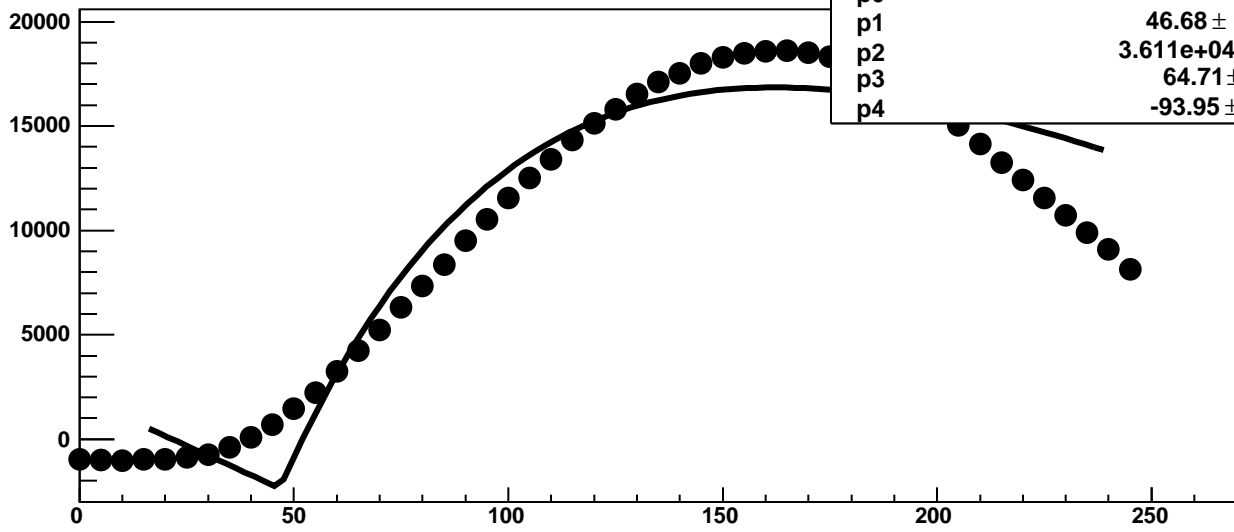
Chip 4, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

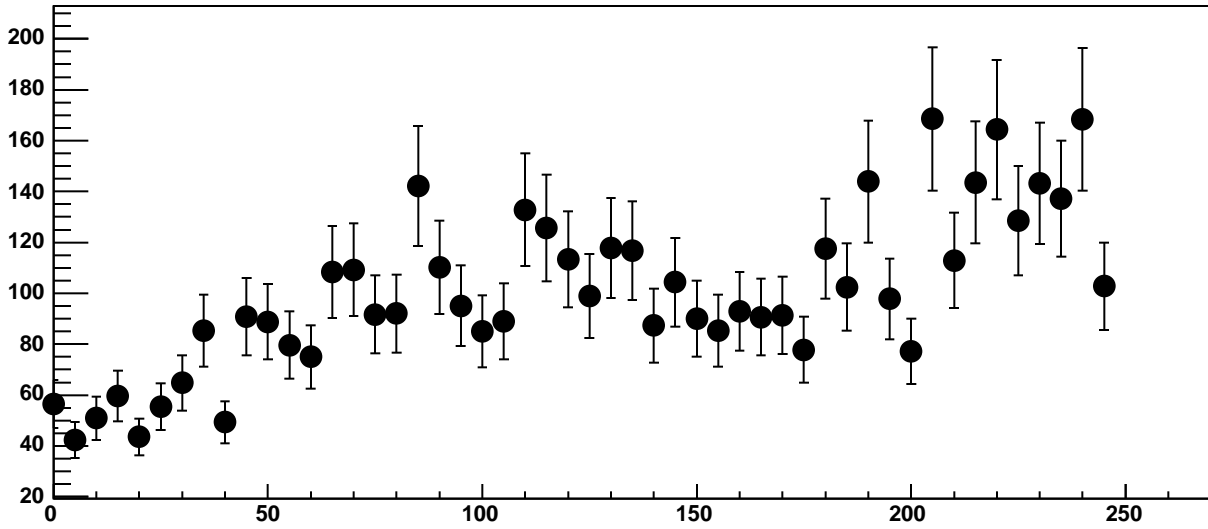


Chip 4, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold

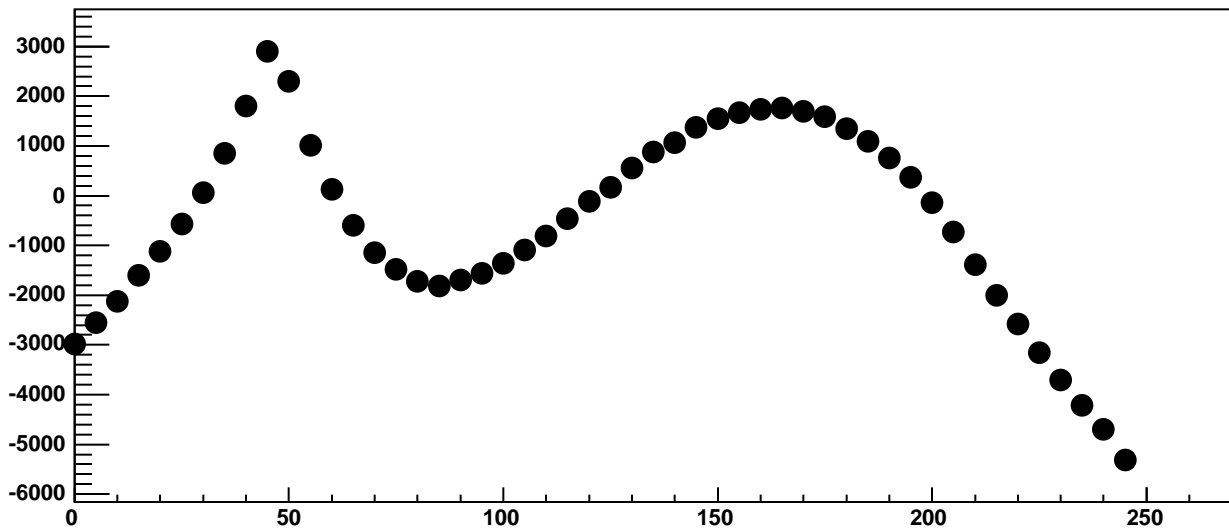


$\chi^2 / \text{ndf}$	2.496e+05 / 41
p0	-2350 ± 6.906
p1	46.68 ± 0.02792
p2	3.611e+04 ± 76.37
p3	64.71 ± 0.1289
p4	-93.95 ± 0.3306

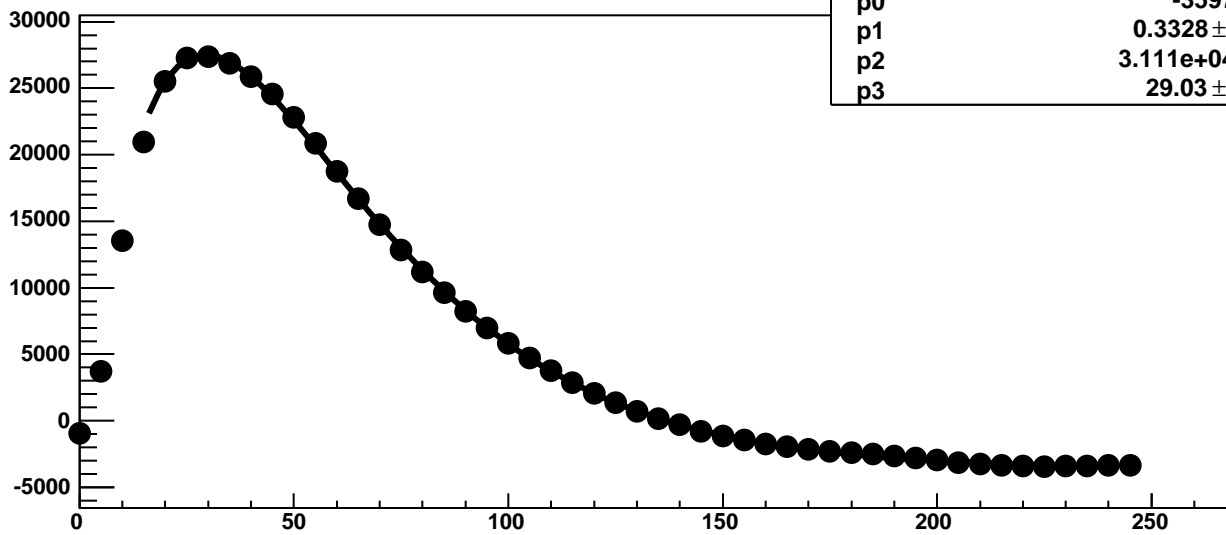
Chip 4, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

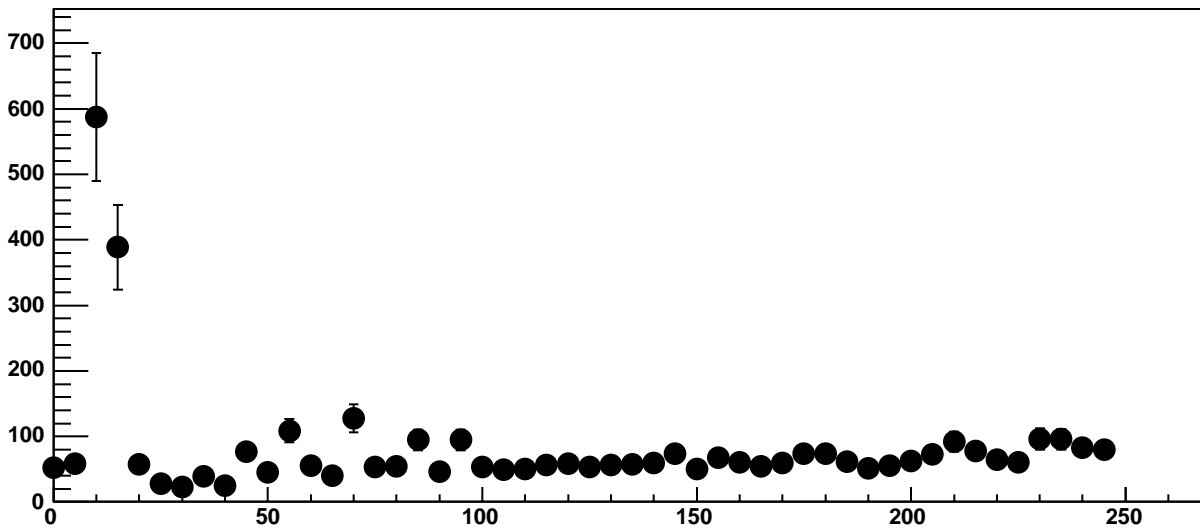


Chip 4, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

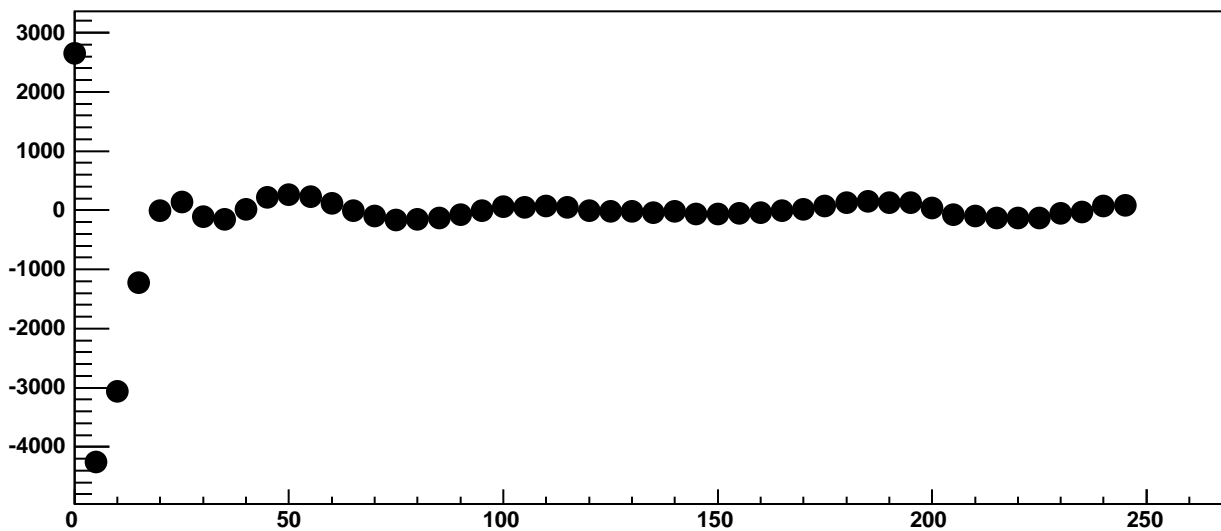


$\chi^2 / \text{ndf}$	3602 / 42
p0	$-3597 \pm 4.402$
p1	$0.3328 \pm 0.02278$
p2	$3.111\text{e}+04 \pm 5.035$
p3	$29.03 \pm 0.01235$

Chip 4, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

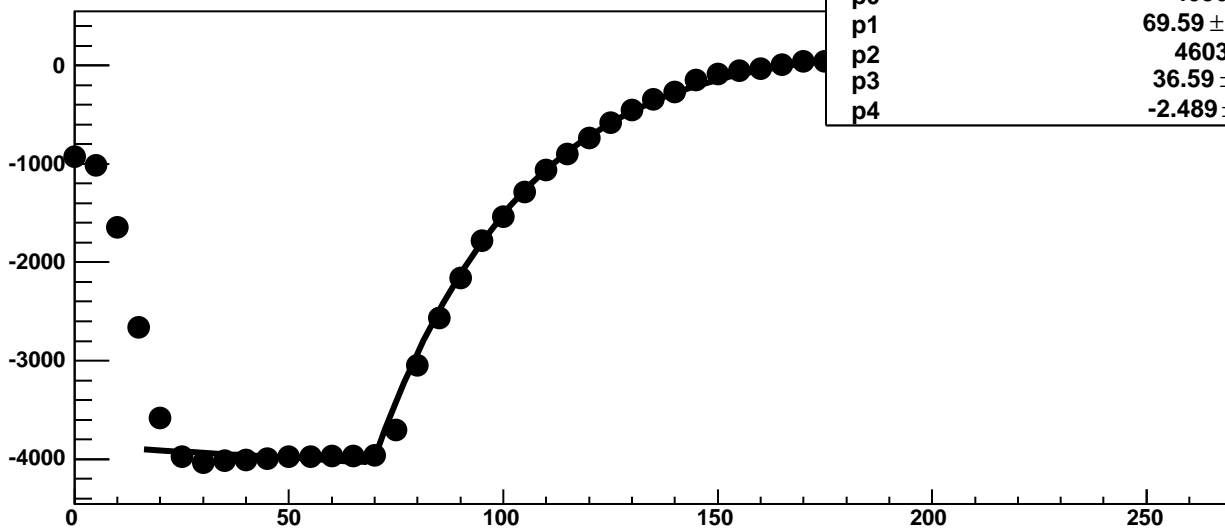


Chip 4, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



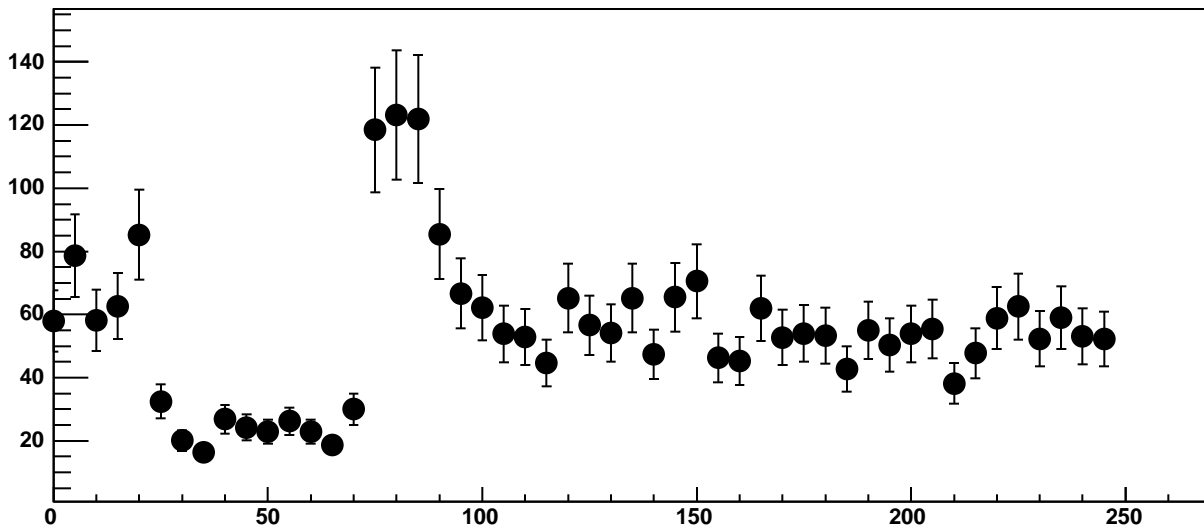


Chip 4, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

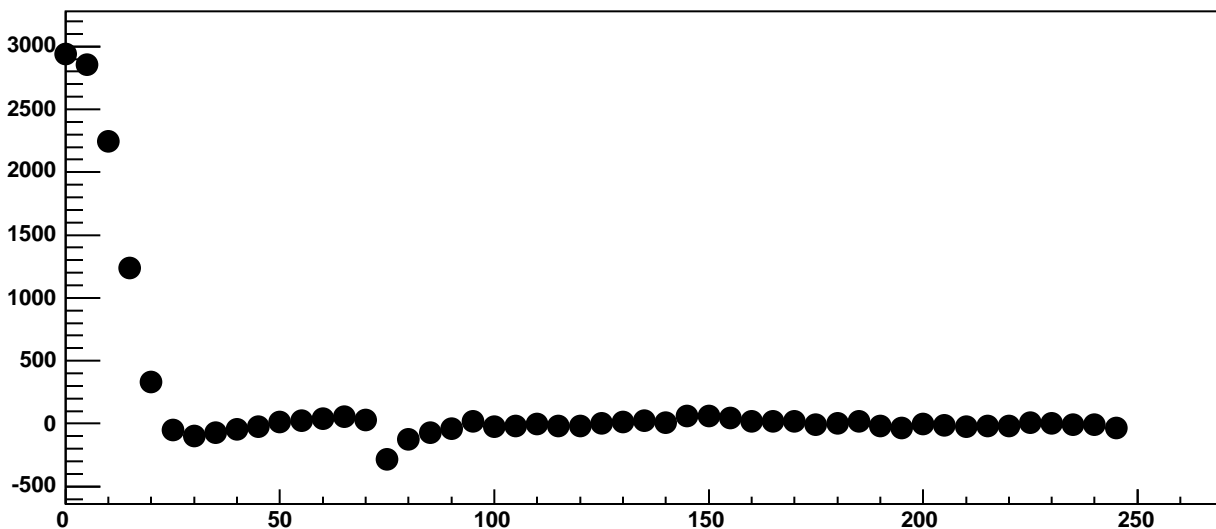


$\chi^2 / \text{ndf}$	9117 / 41
p0	$-4036 \pm 3.054$
p1	$69.59 \pm 0.06071$
p2	$4603 \pm 19.84$
p3	$36.59 \pm 0.2205$
p4	$-2.489 \pm 0.1063$

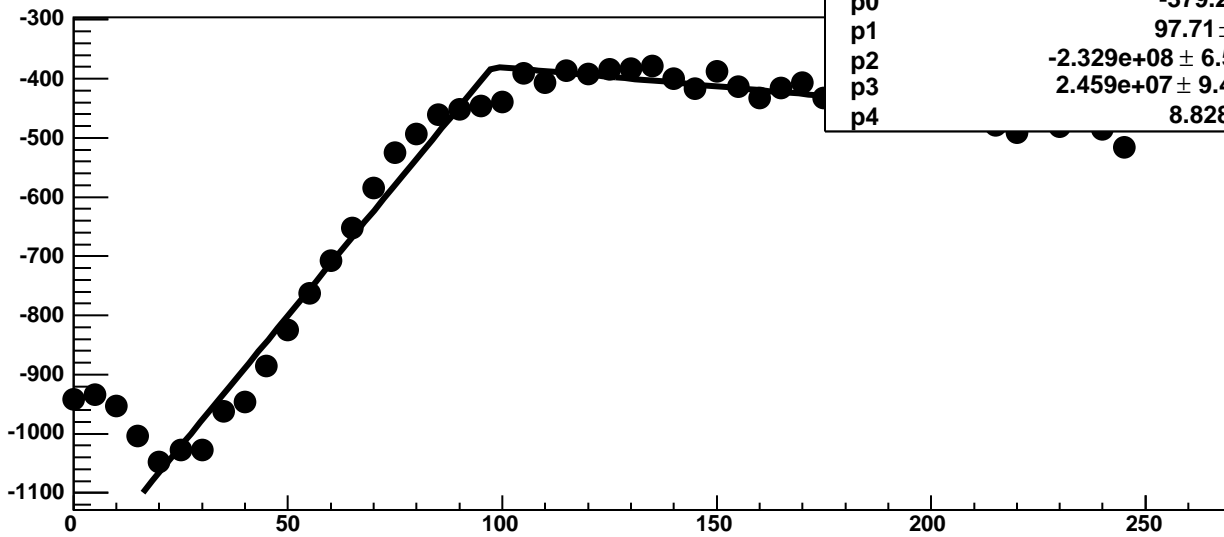
Chip 4, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

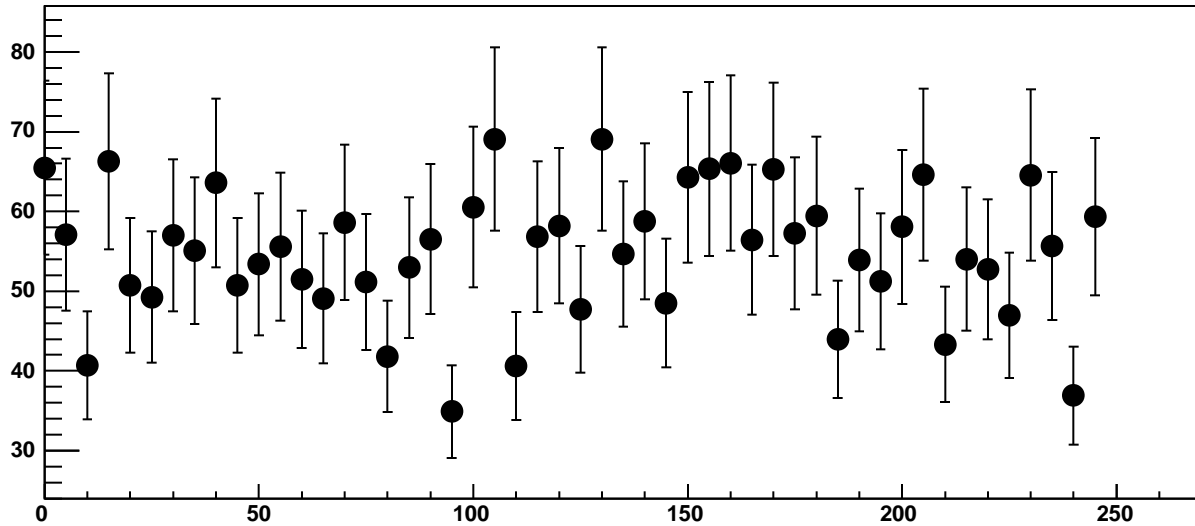


Chip 4, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

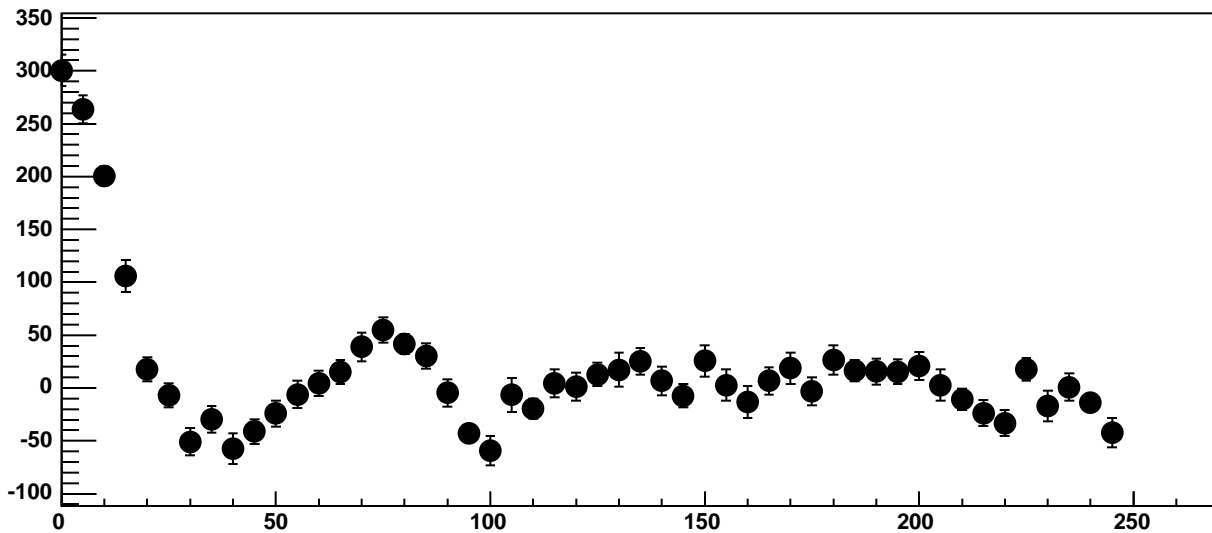


$\chi^2 / \text{ndf}$	257.2 / 41
p0	$-379.2 \pm 4.356$
p1	$97.71 \pm 0.6174$
p2	$-2.329\text{e}+08 \pm 6.541\text{e}+06$
p3	$2.459\text{e}+07 \pm 9.486\text{e}+05$
p4	$8.828 \pm 0.112$

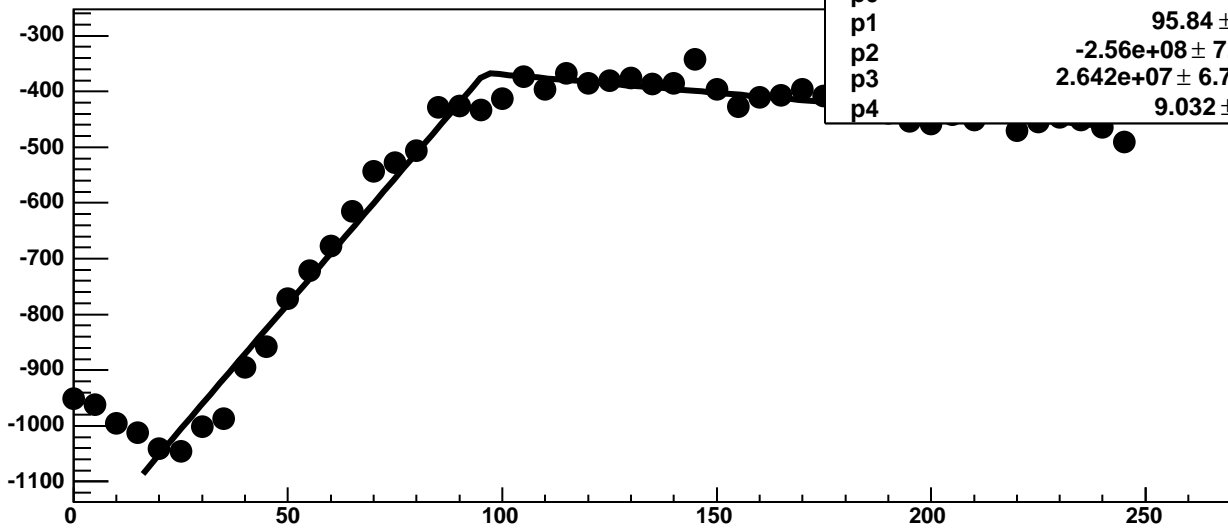
Chip 4, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

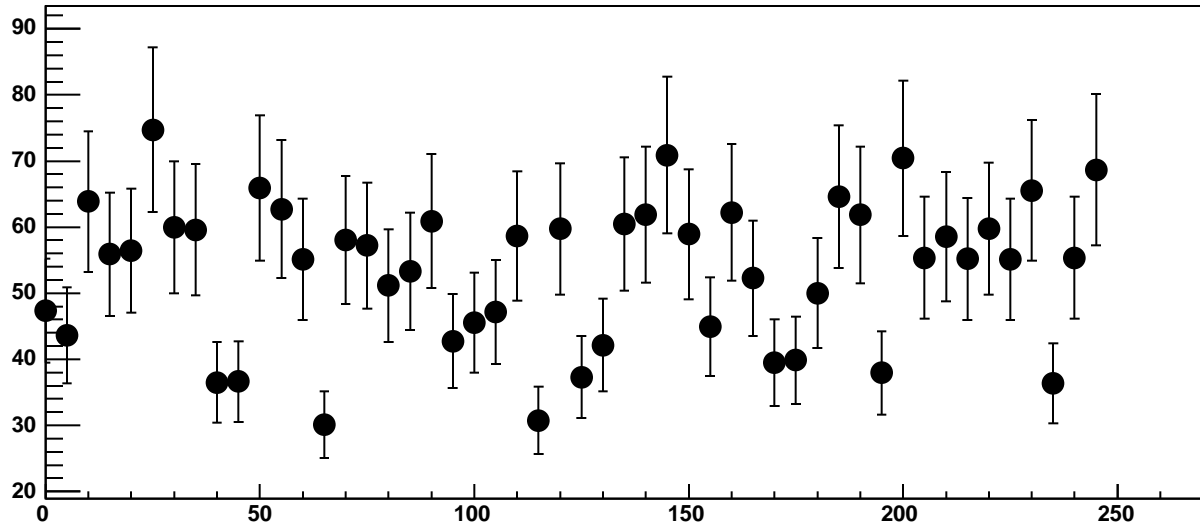


Chip 4, Channel 12, Enable 4, DAC=1600, ADC Mean vs Hold

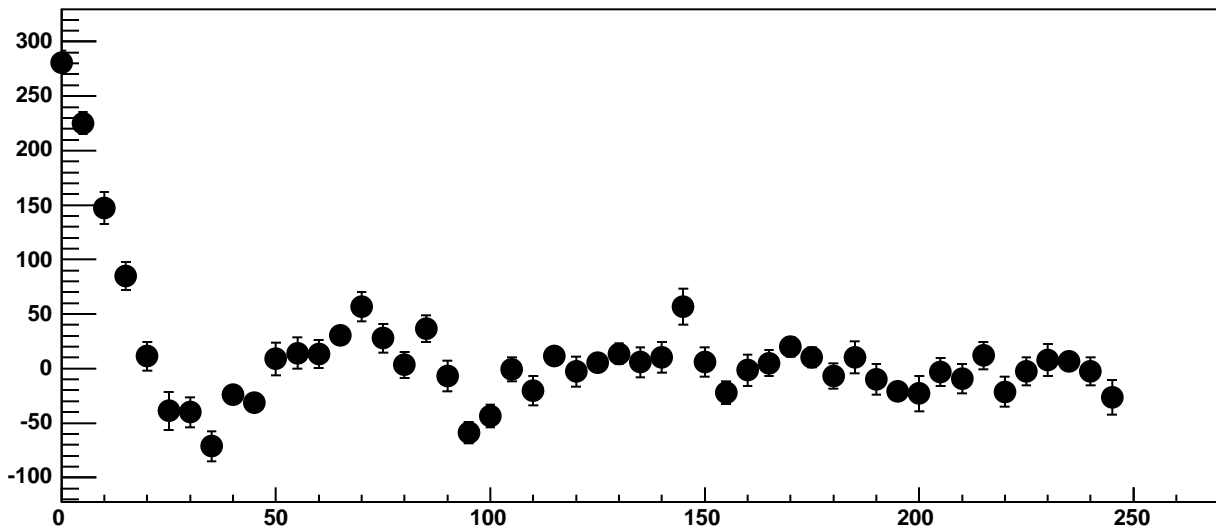


$\chi^2 / \text{ndf}$	260.5 / 41
p0	$-366.8 \pm 3.76$
p1	$95.84 \pm 0.6926$
p2	$-2.56e+08 \pm 7.53e+06$
p3	$2.642e+07 \pm 6.712e+05$
p4	$9.032 \pm 0.1197$

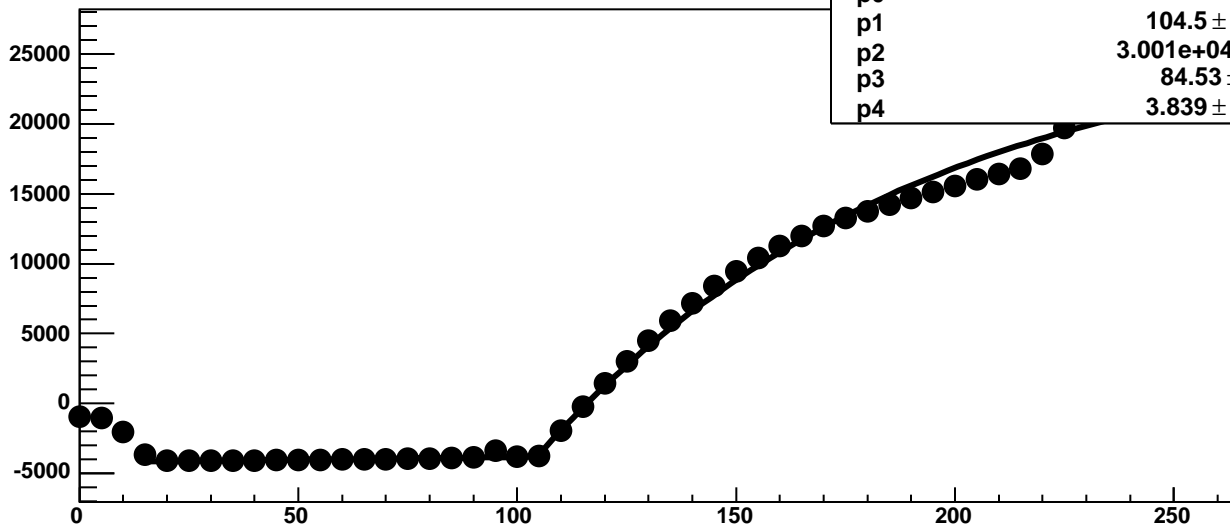
Chip 4, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold

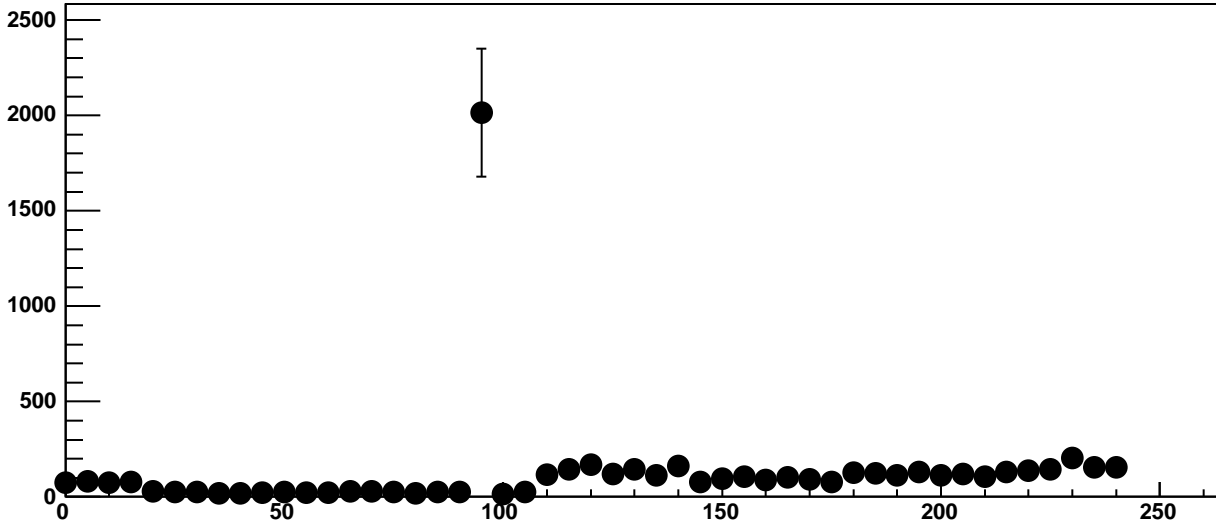


Chip 4, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

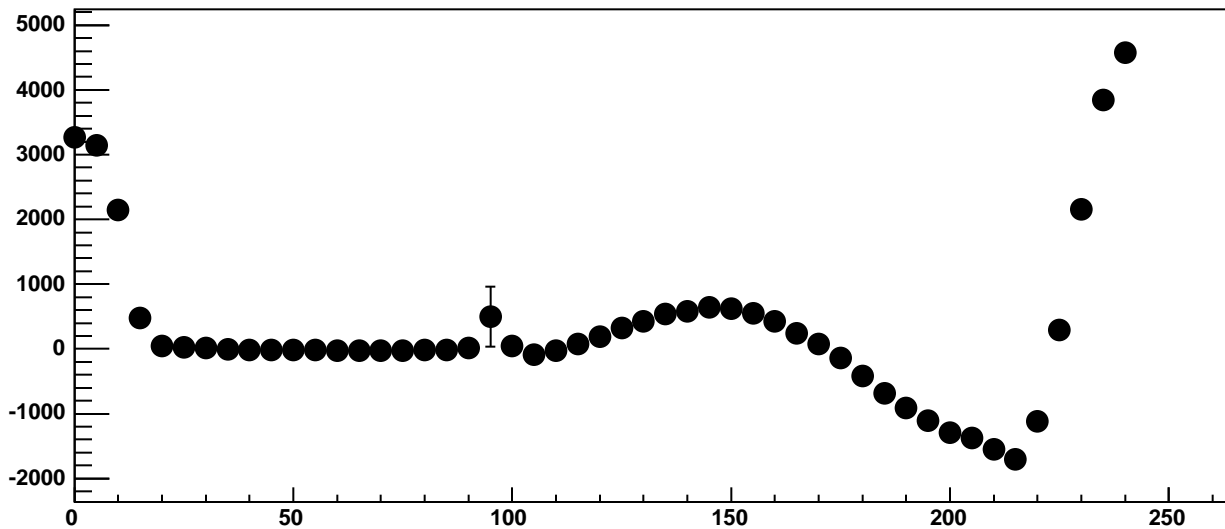


$\chi^2 / \text{ndf}$	5.254e+04 / 41
p0	-3816 ± 2.84
p1	104.5 ± 0.01924
p2	3.001e+04 ± 55.13
p3	84.53 ± 0.2598
p4	3.839 ± 0.05475

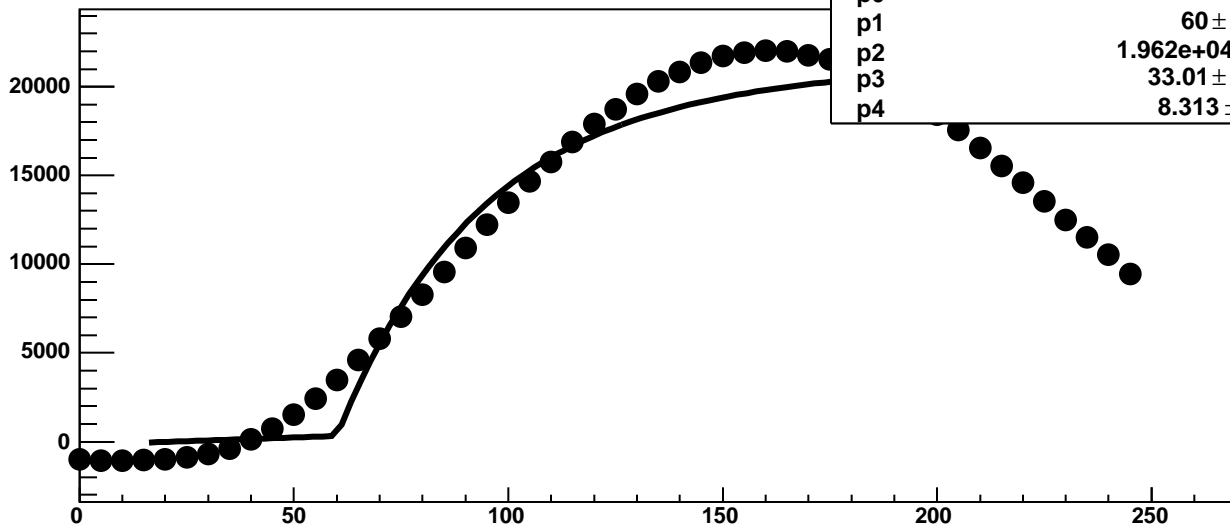
Chip 4, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold

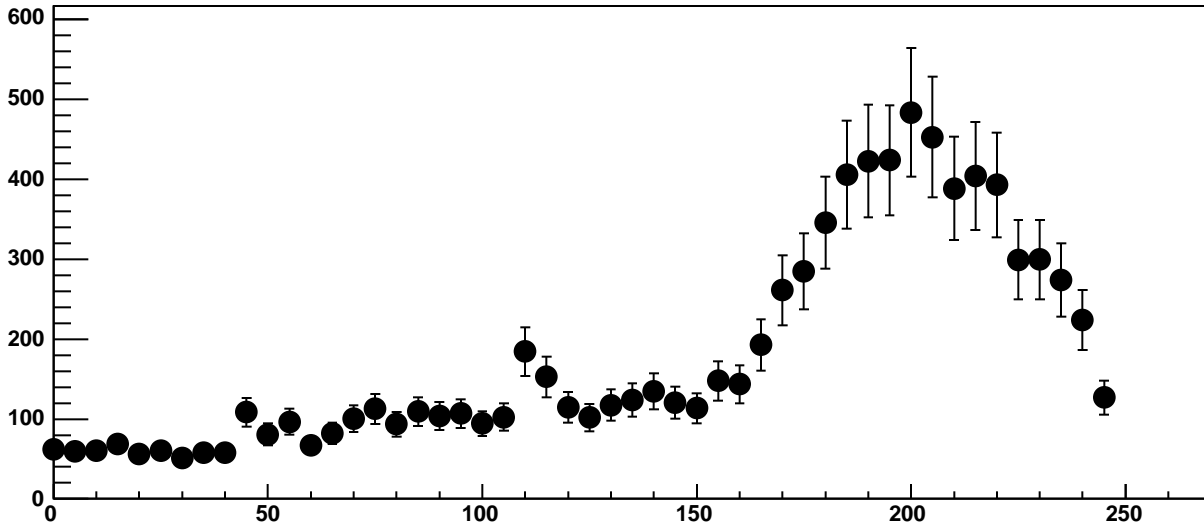


Chip 4, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

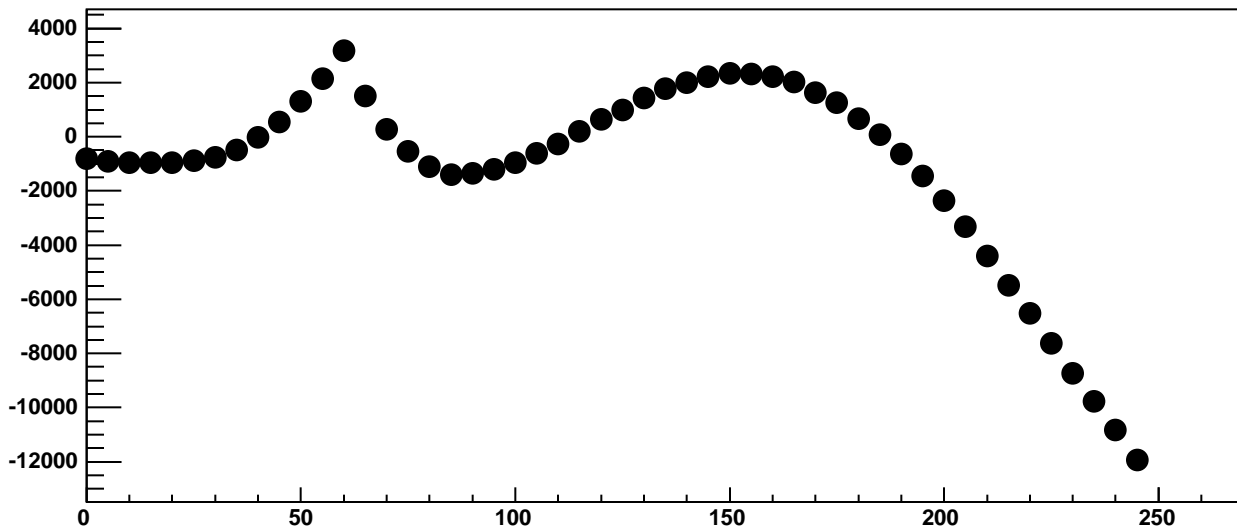


$\chi^2 / \text{ndf}$	2.468e+05 / 41
p0	313.1 ± 8.073
p1	60 ± 0.03503
p2	1.962e+04 ± 39.34
p3	33.01 ± 0.08524
p4	8.313 ± 0.2505

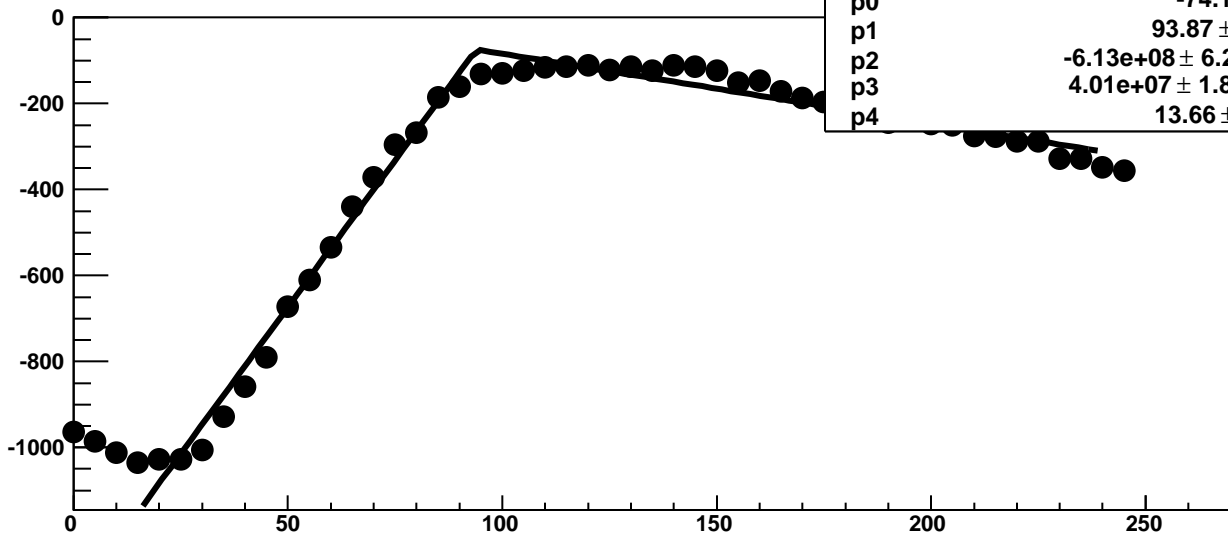
Chip 4, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

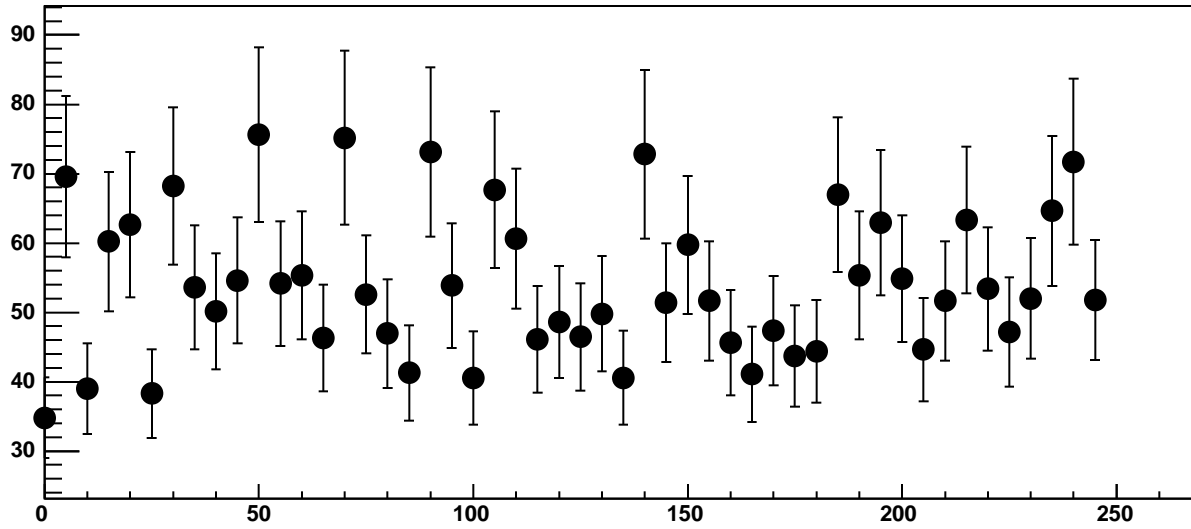


Chip 4, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold

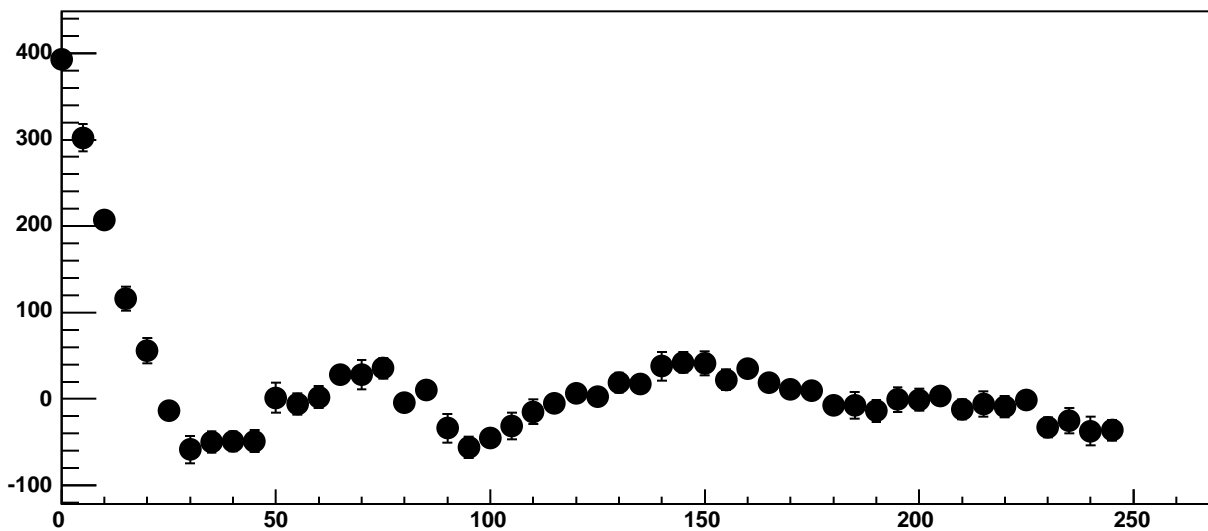


$\chi^2 / \text{ndf}$	298.9 / 41
p0	$-74.1 \pm 3.826$
p1	$93.87 \pm 0.4895$
p2	$-6.13\text{e}+08 \pm 6.287\text{e}+06$
p3	$4.01\text{e}+07 \pm 1.859\text{e}+05$
p4	$13.66 \pm 0.1318$

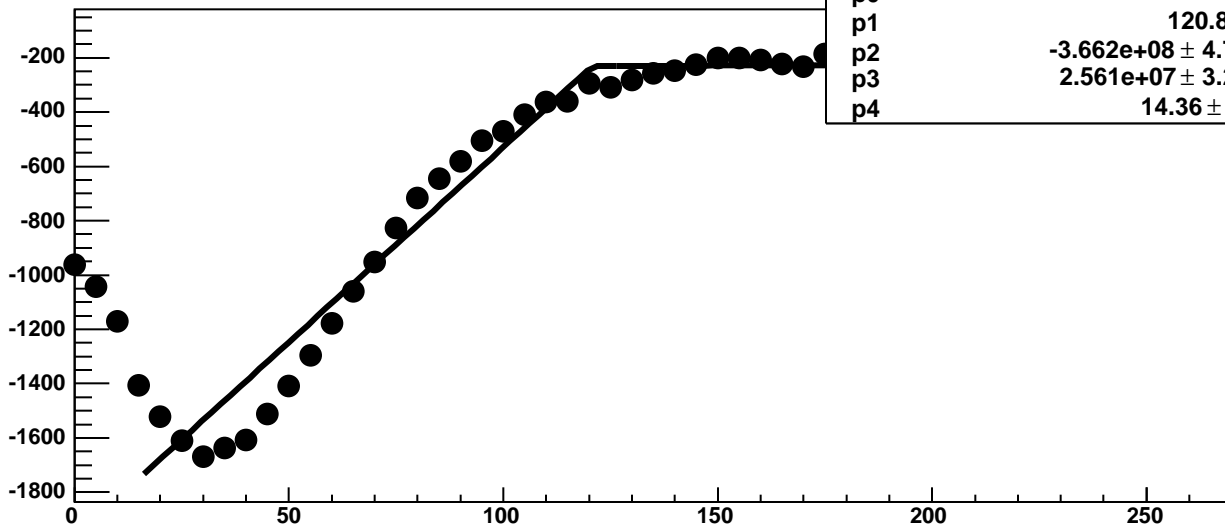
Chip 4, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold

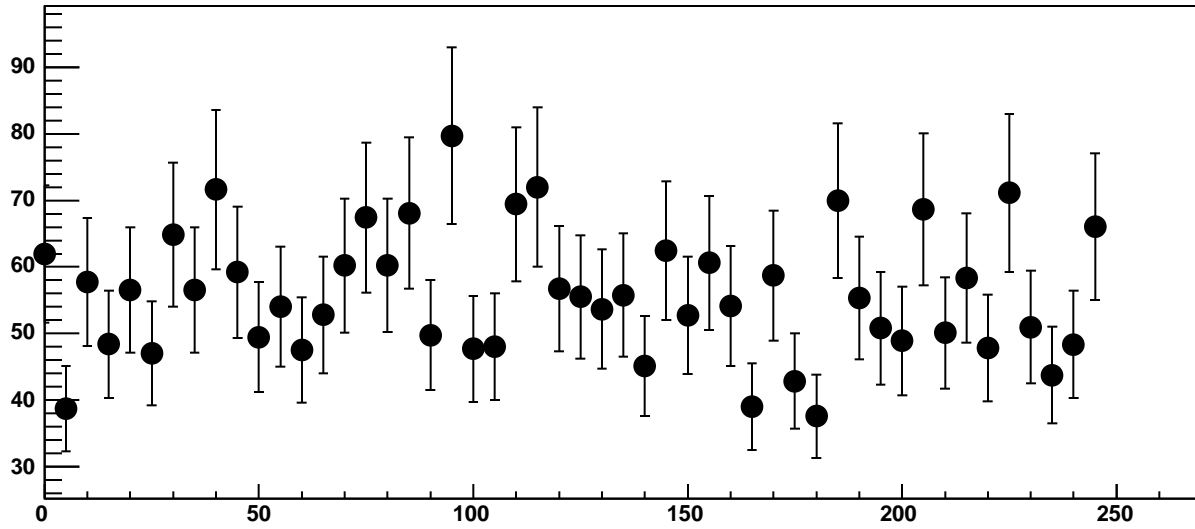


Chip 4, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

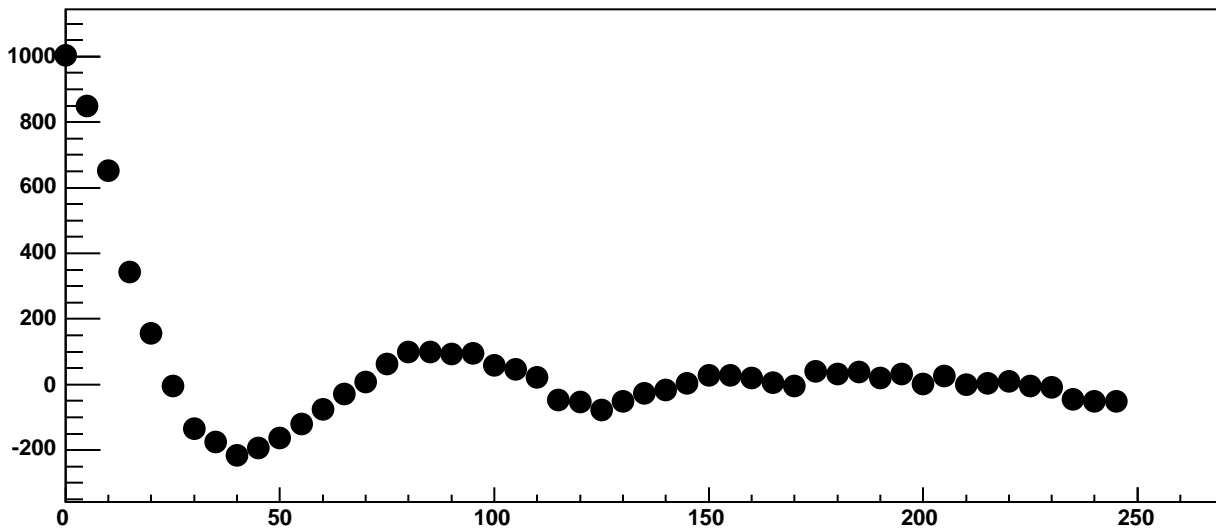


$\chi^2 / \text{ndf}$	2529 / 41
p0	$-230.7 \pm 4.991$
p1	$120.8 \pm 0.518$
p2	$-3.662\text{e}+08 \pm 4.771\text{e}+07$
p3	$2.561\text{e}+07 \pm 3.294\text{e}+06$
p4	$14.36 \pm 0.08683$

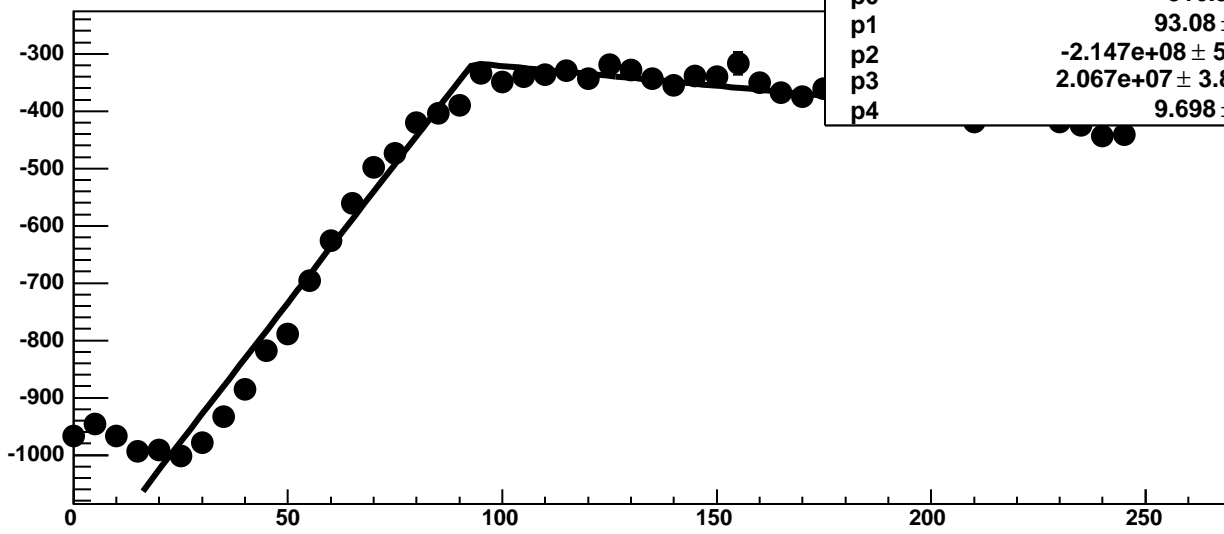
Chip 4, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

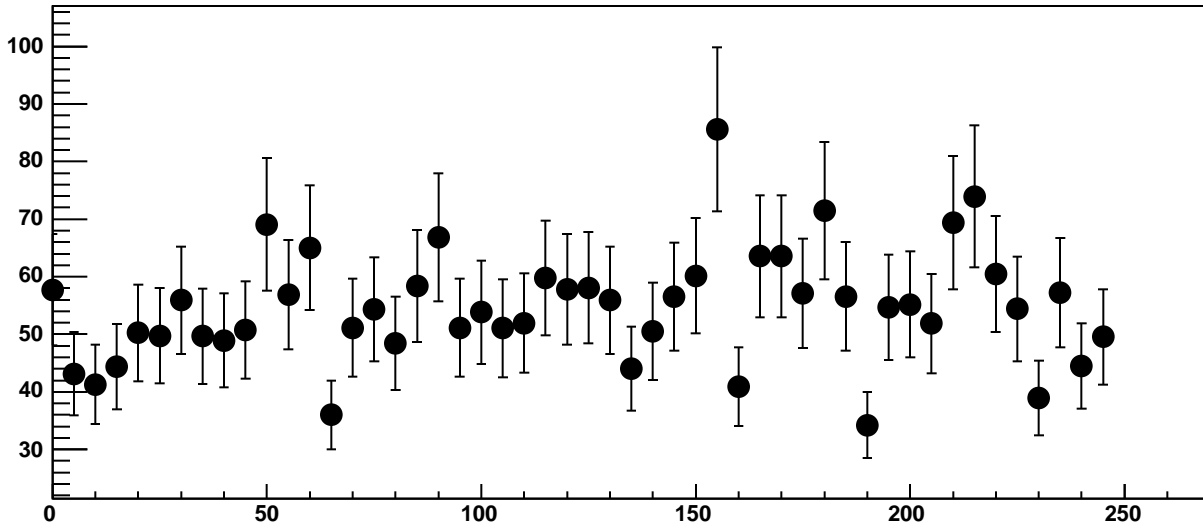


Chip 4, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

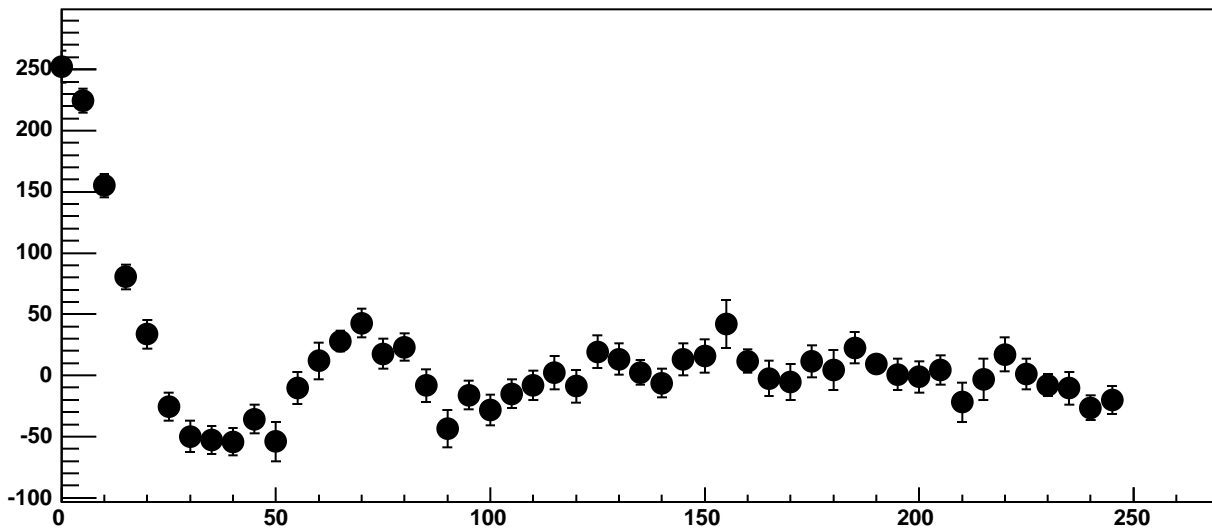


$\chi^2 / \text{ndf}$	236.9 / 41
p0	$-316.5 \pm 4.162$
p1	$93.08 \pm 0.7299$
p2	$-2.147\text{e}+08 \pm 5.19\text{e}+06$
p3	$2.067\text{e}+07 \pm 3.805\text{e}+05$
p4	$9.698 \pm 0.1278$

Chip 4, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

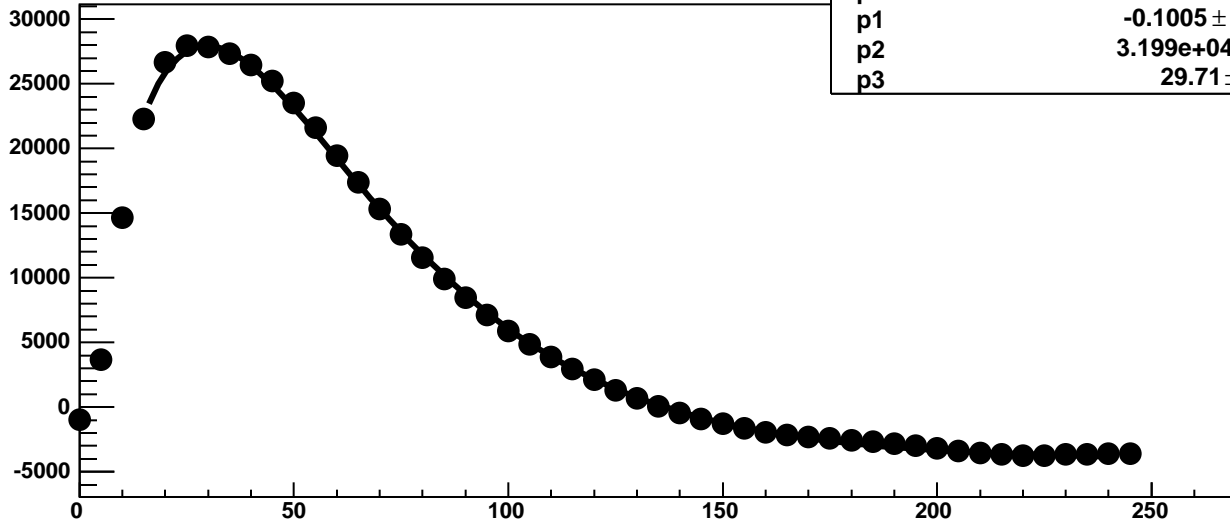


Chip 4, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold



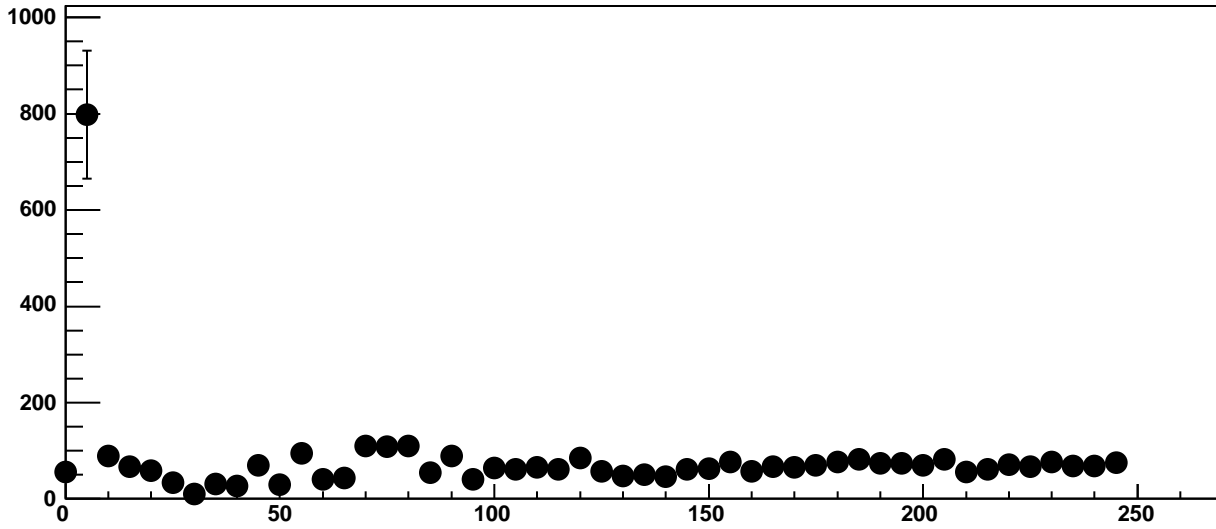


Chip 4, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold

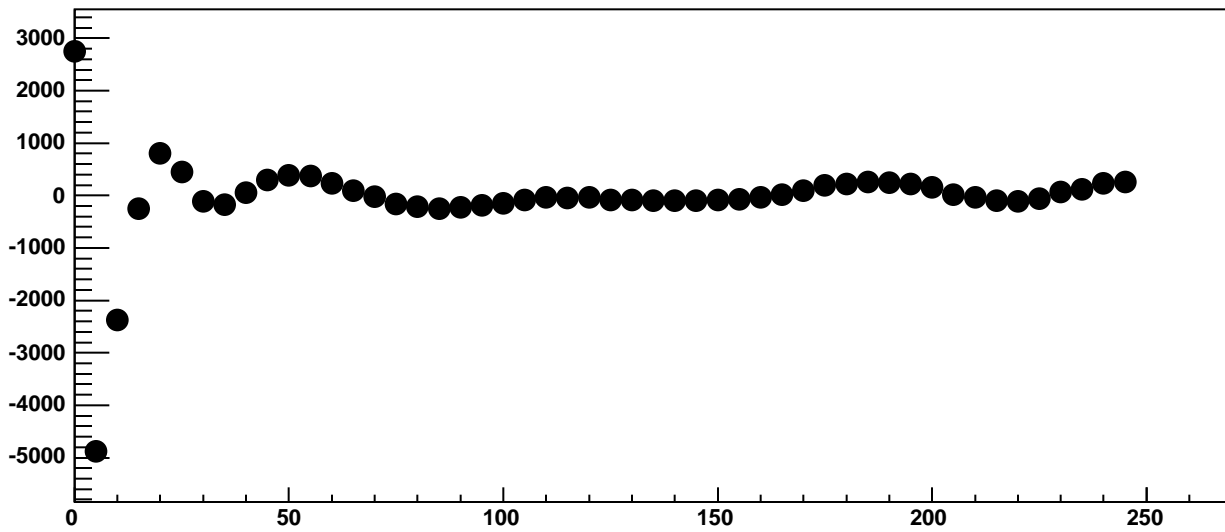


$\chi^2 / \text{ndf}$	1.679e+04 / 42
p0	-4027 ± 4.329
p1	-0.1005 ± 0.01694
p2	3.199e+04 ± 4.579
p3	29.71 ± 0.0104

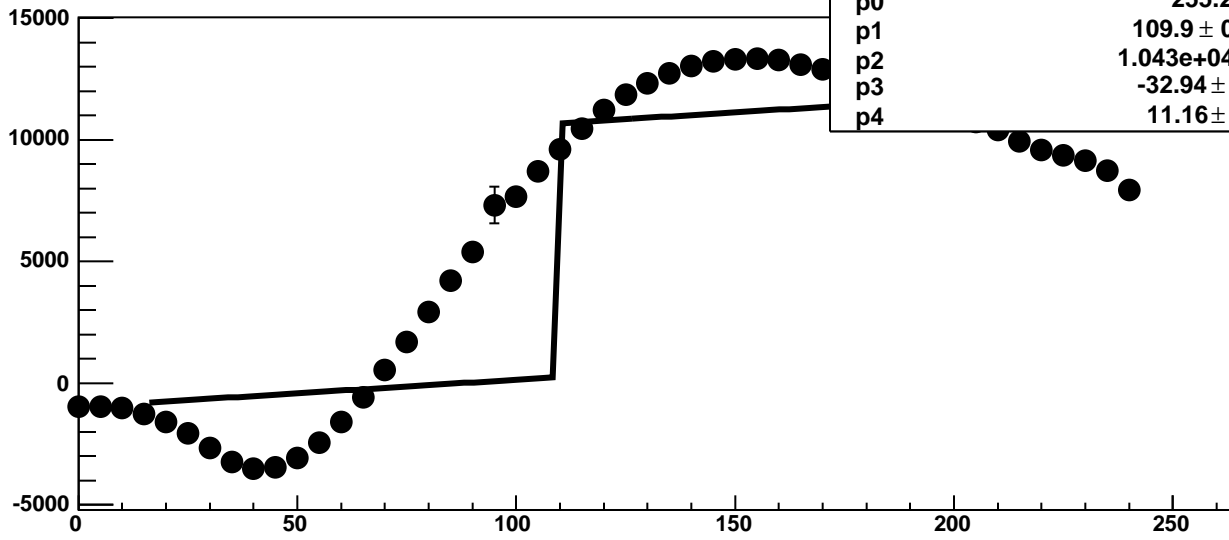
Chip 4, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



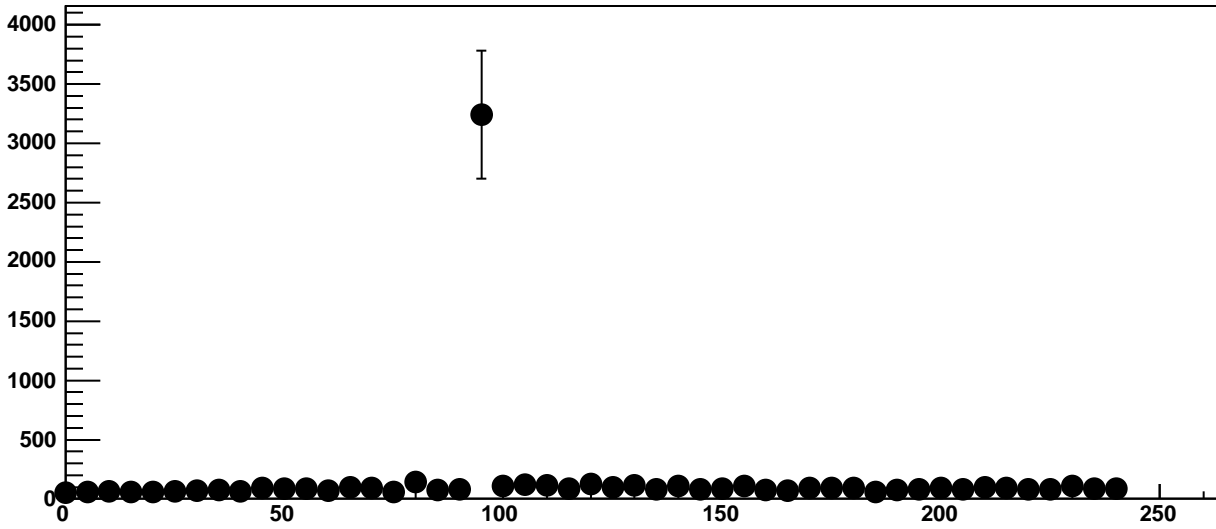
Chip 4, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold



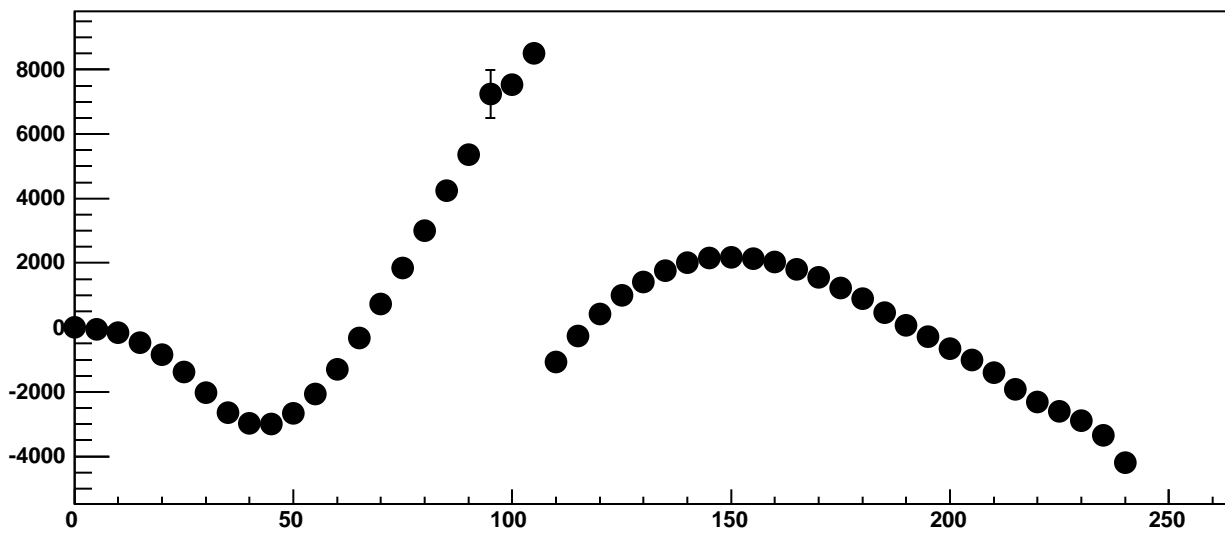
Chip 4, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold



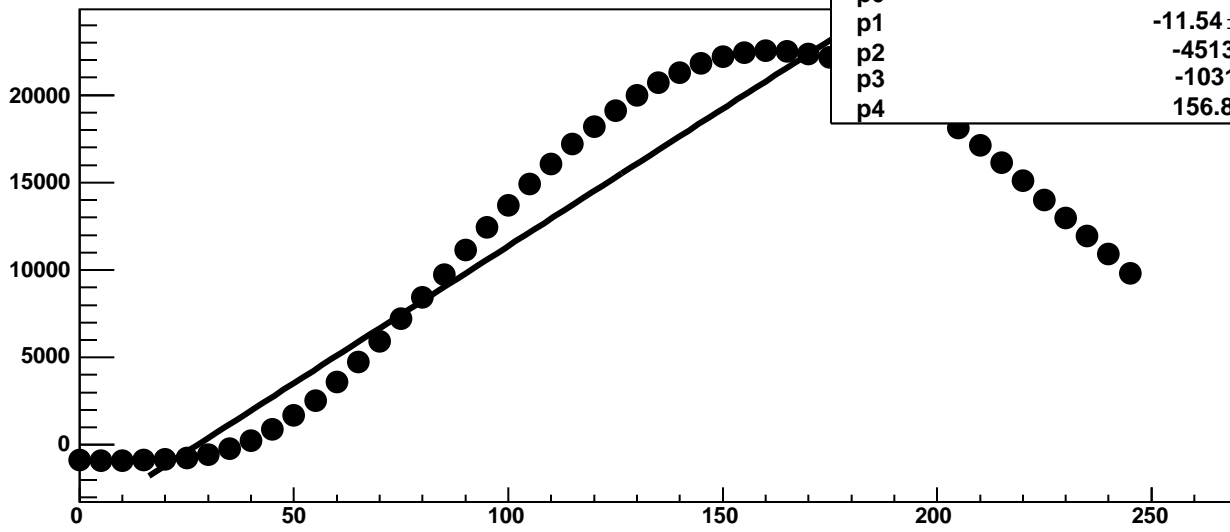
Chip 4, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

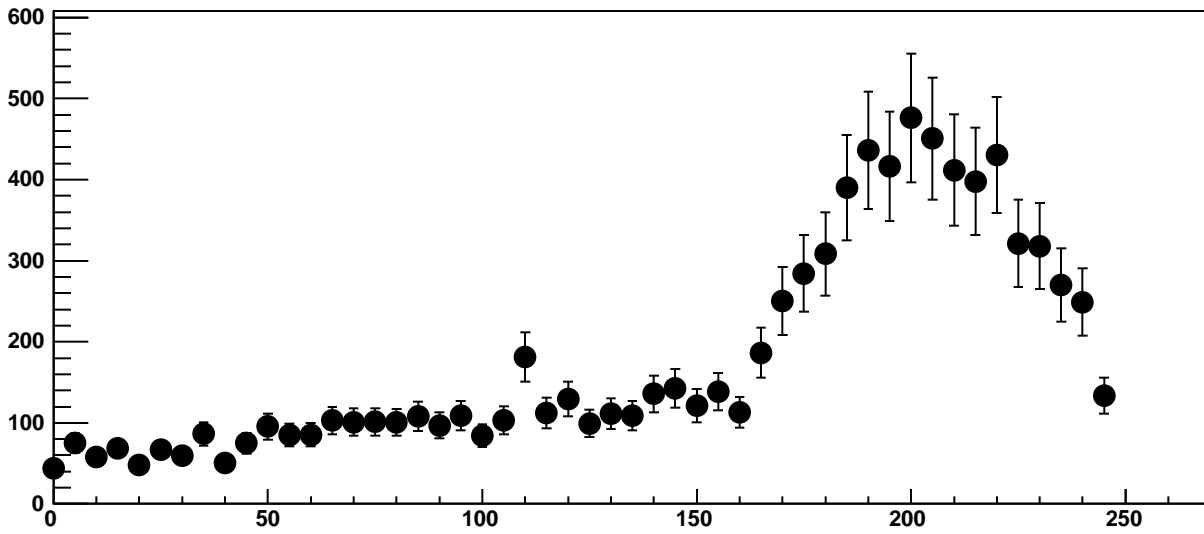


Chip 4, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

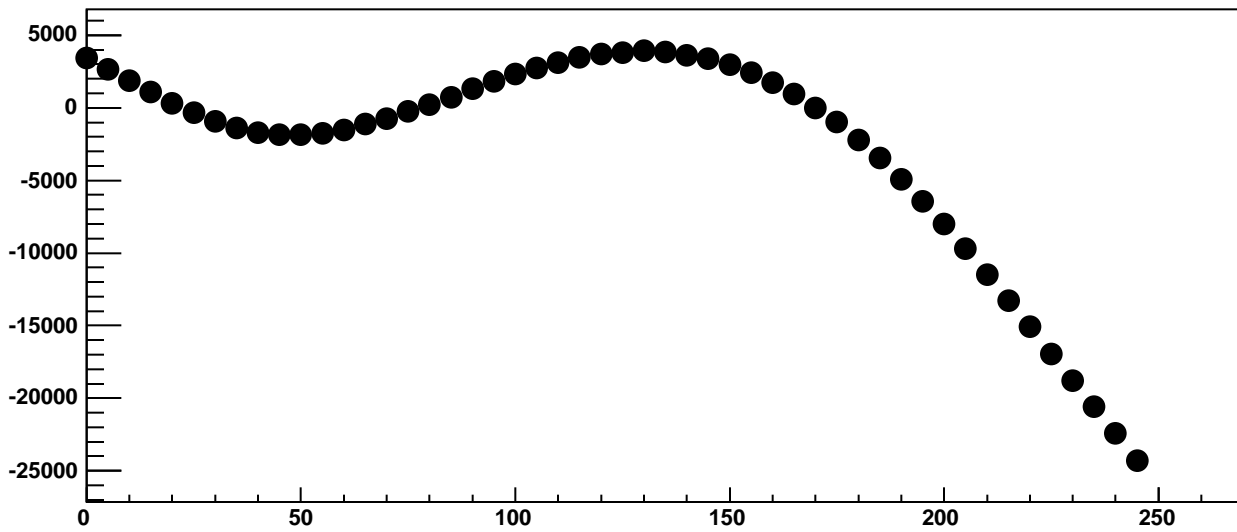


$\chi^2 / \text{ndf}$	7.403e+05 / 41
p0	-1607 ± 22.35
p1	-11.54 ± 0.1212
p2	-4513 ± 23.17
p3	-1031 ± 18.25
p4	156.8 ± 0.129

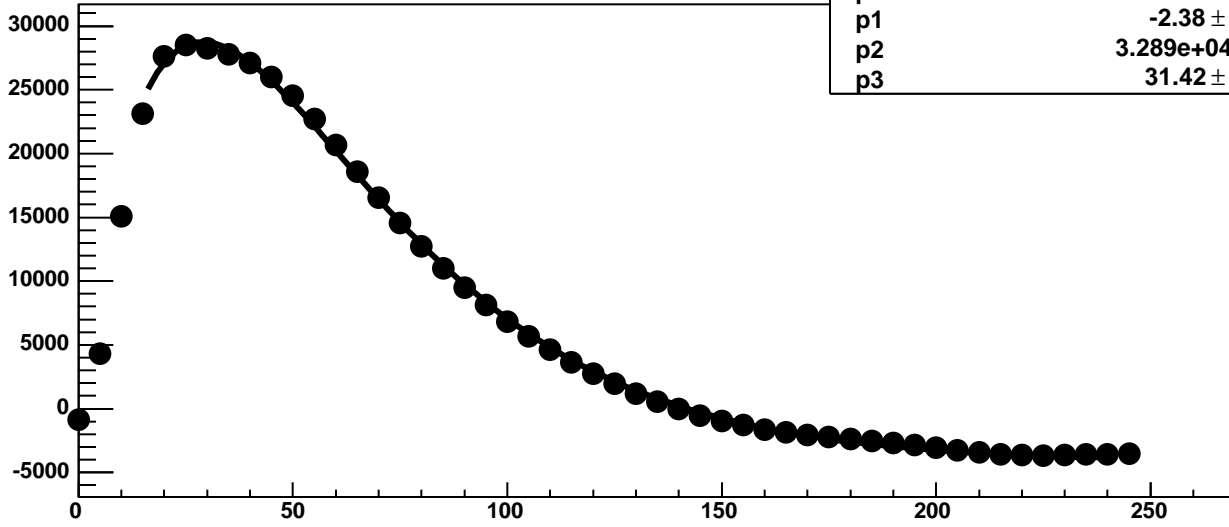
Chip 4, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



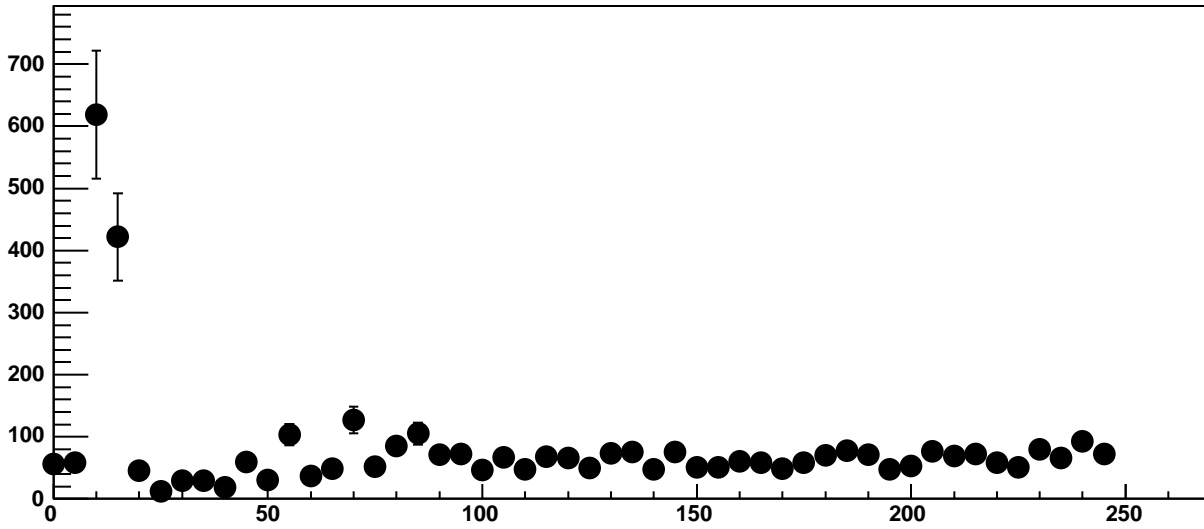
Chip 4, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold



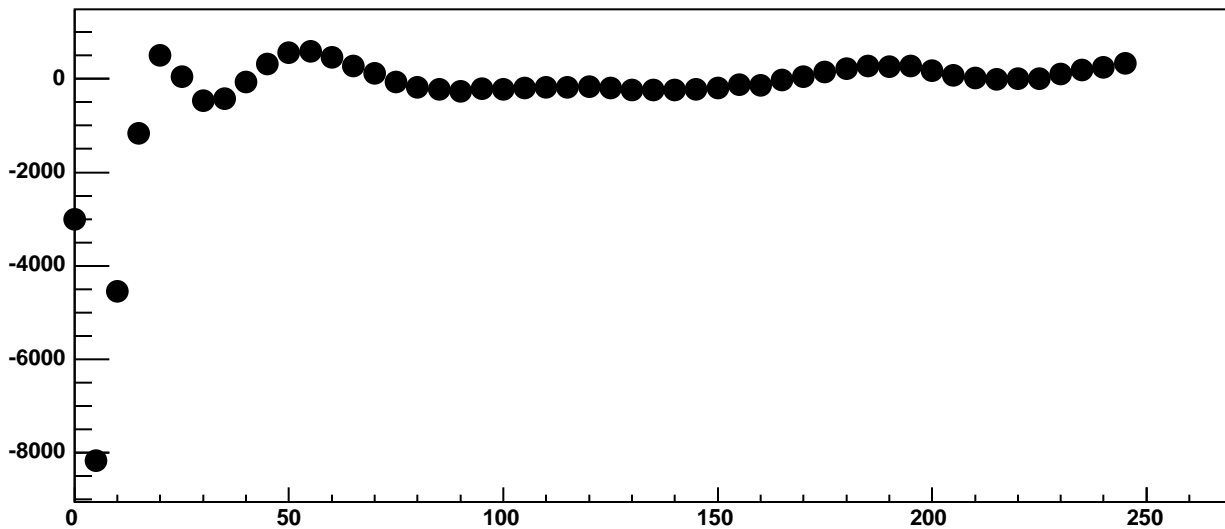
Chip 4, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold



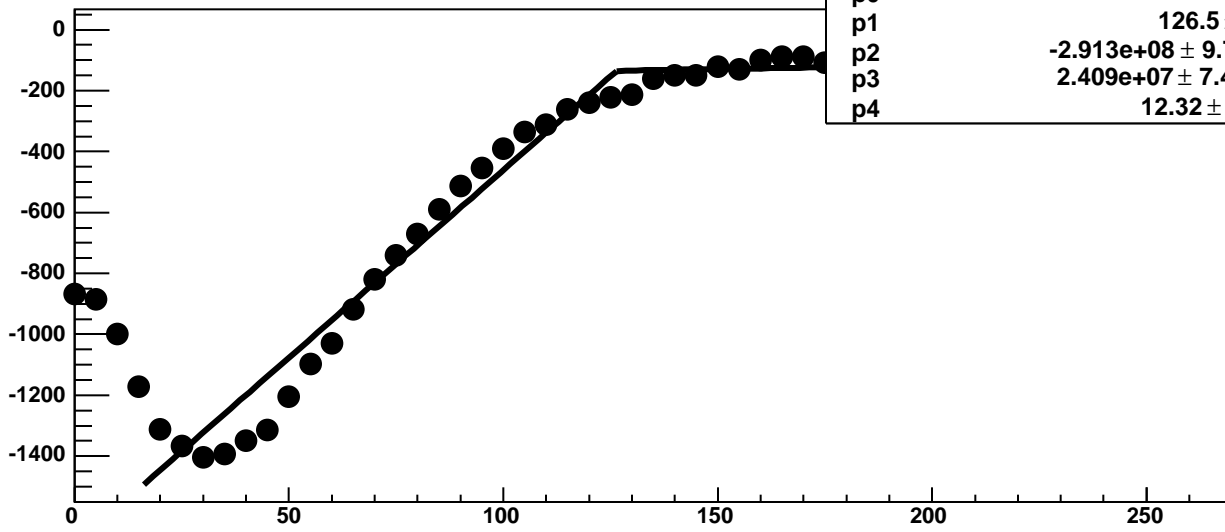
Chip 4, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

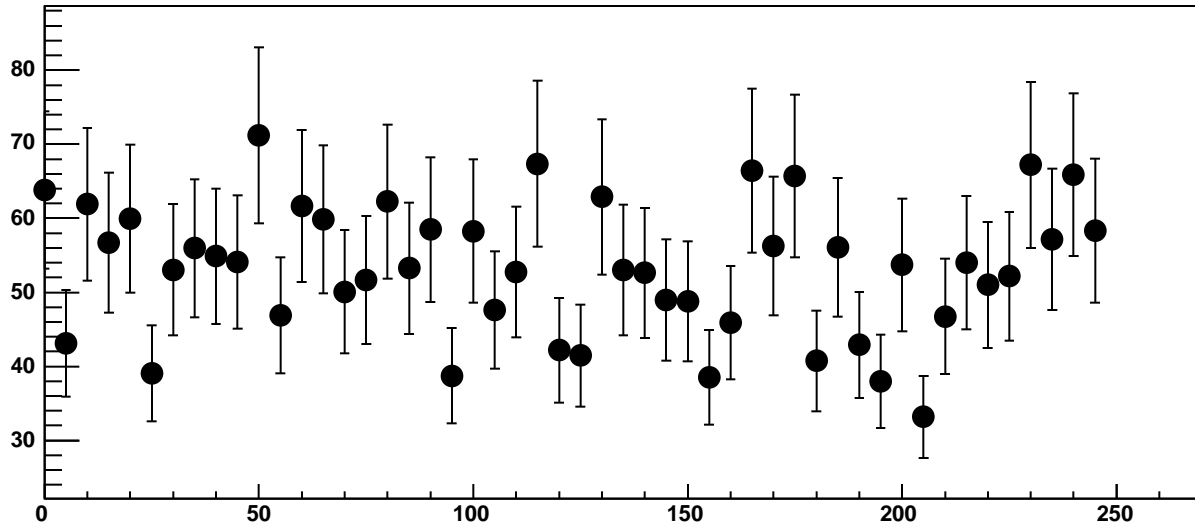


Chip 4, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

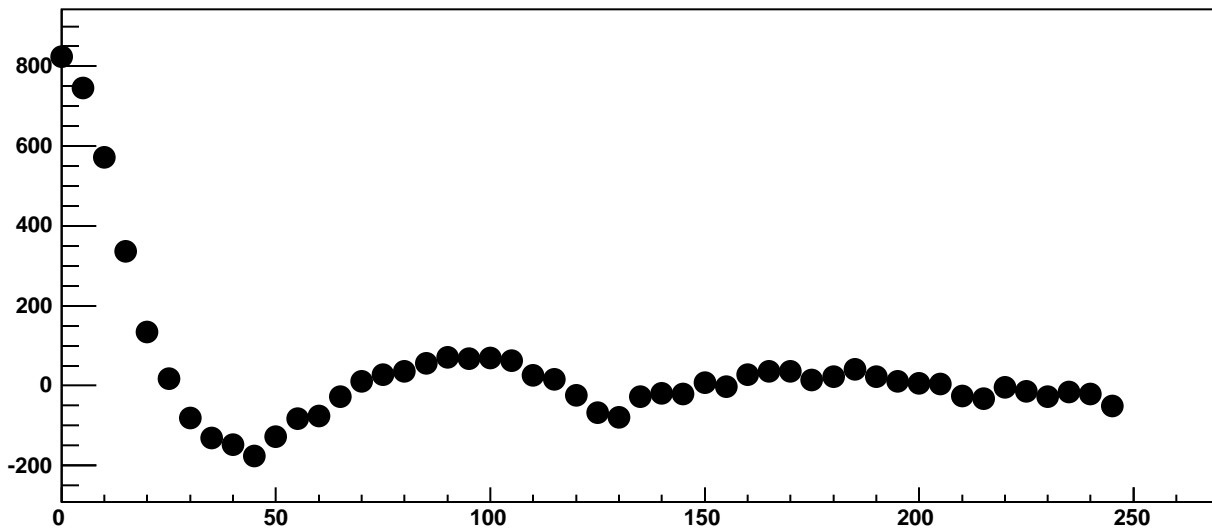


$\chi^2 / \text{ndf}$	1761 / 41
p0	-134.3 ± 5.171
p1	126.5 ± 0.5661
p2	-2.913e+08 ± 9.793e+06
p3	2.409e+07 ± 7.473e+05
p4	12.32 ± 0.07185

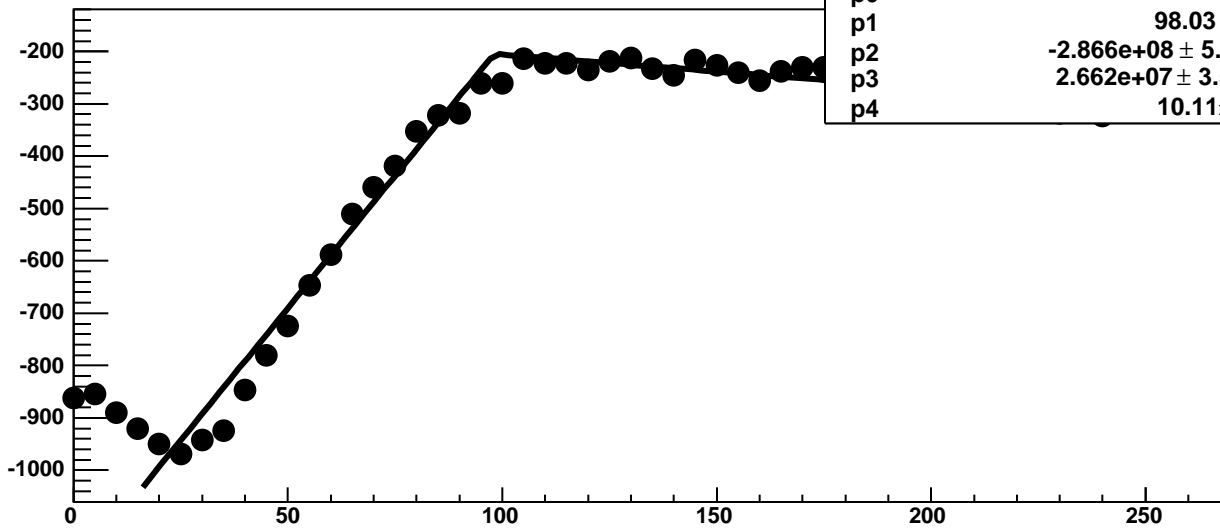
Chip 4, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

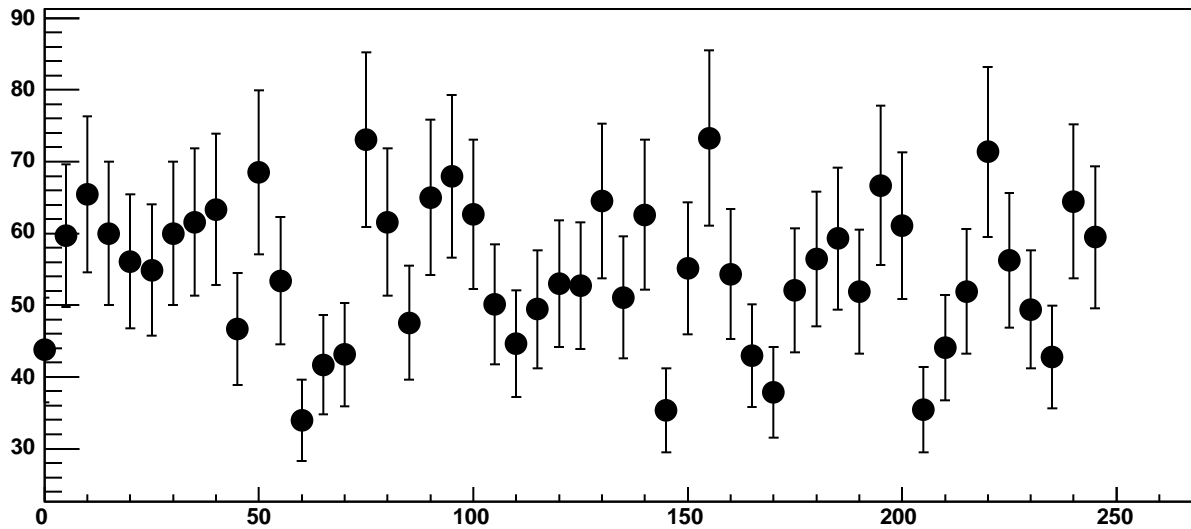


Chip 4, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

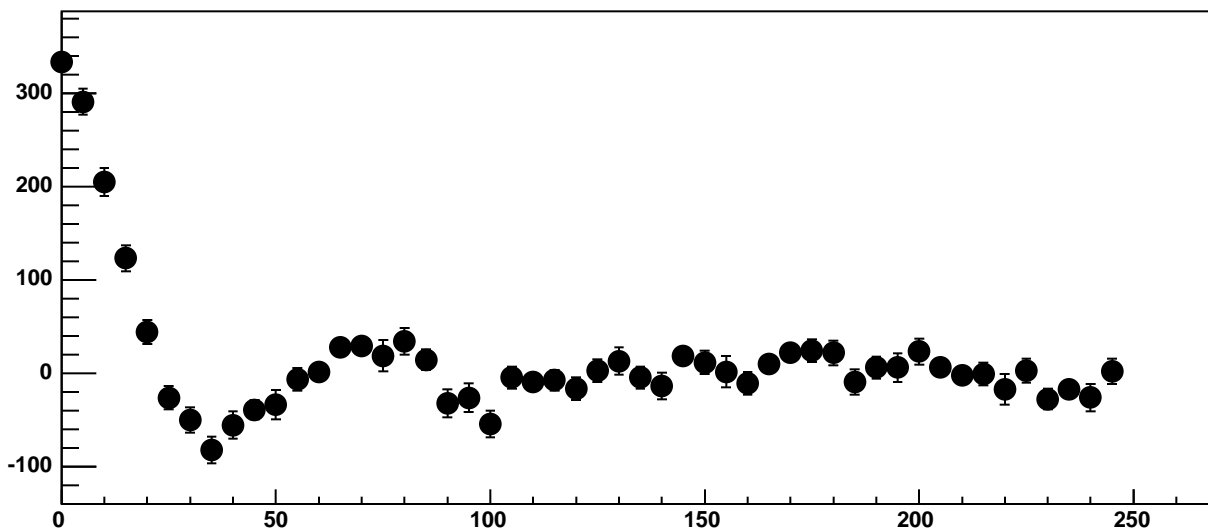


$\chi^2 / \text{ndf}$	268.3 / 41
p0	$-204.4 \pm 4.136$
p1	$98.03 \pm 0.7138$
p2	$-2.866\text{e}+08 \pm 5.709\text{e}+06$
p3	$2.662\text{e}+07 \pm 3.518\text{e}+05$
p4	$10.11 \pm 0.1326$

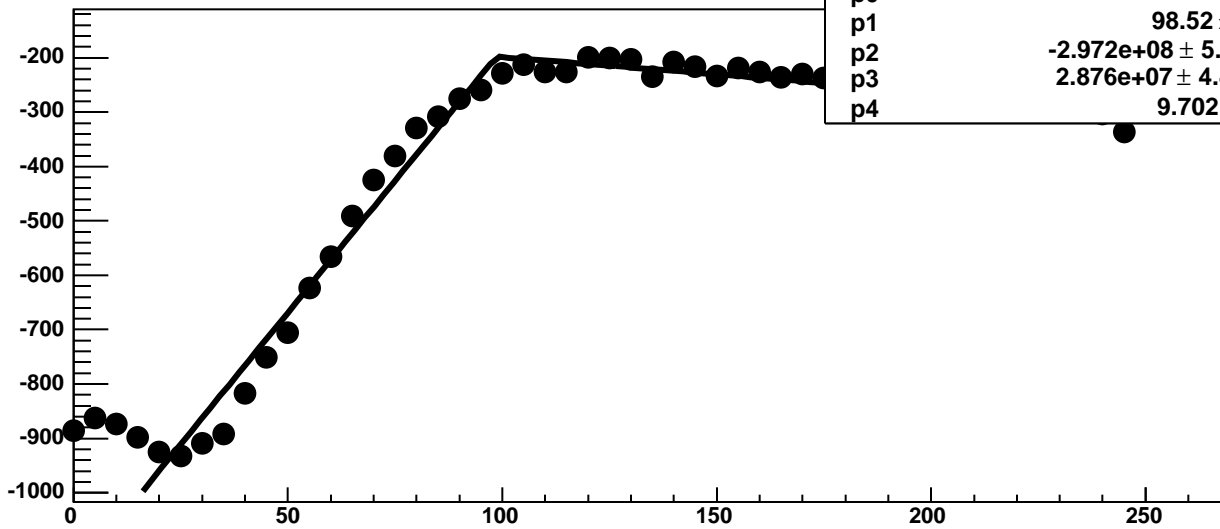
Chip 4, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

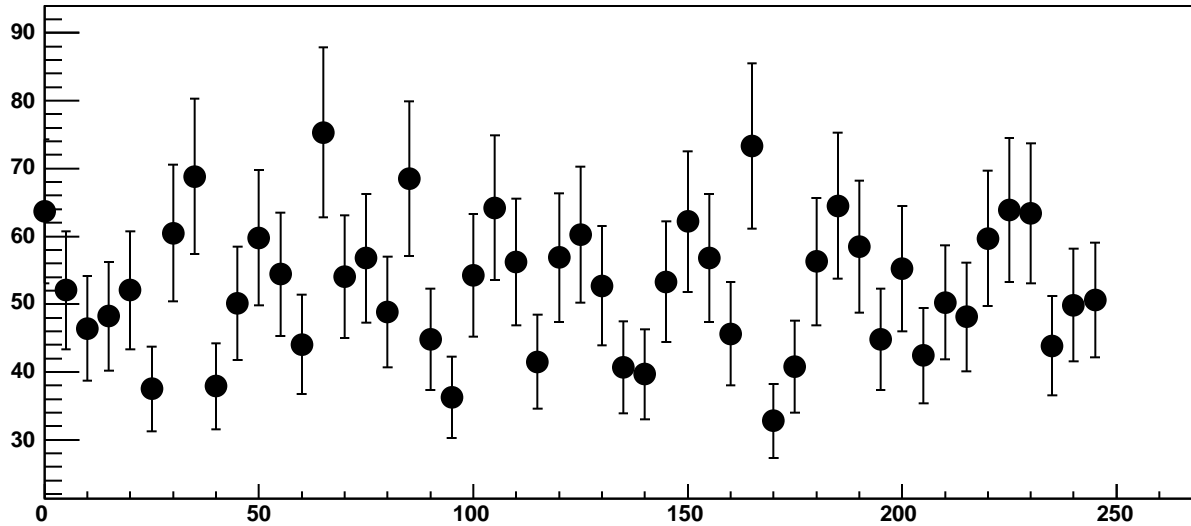


Chip 4, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold

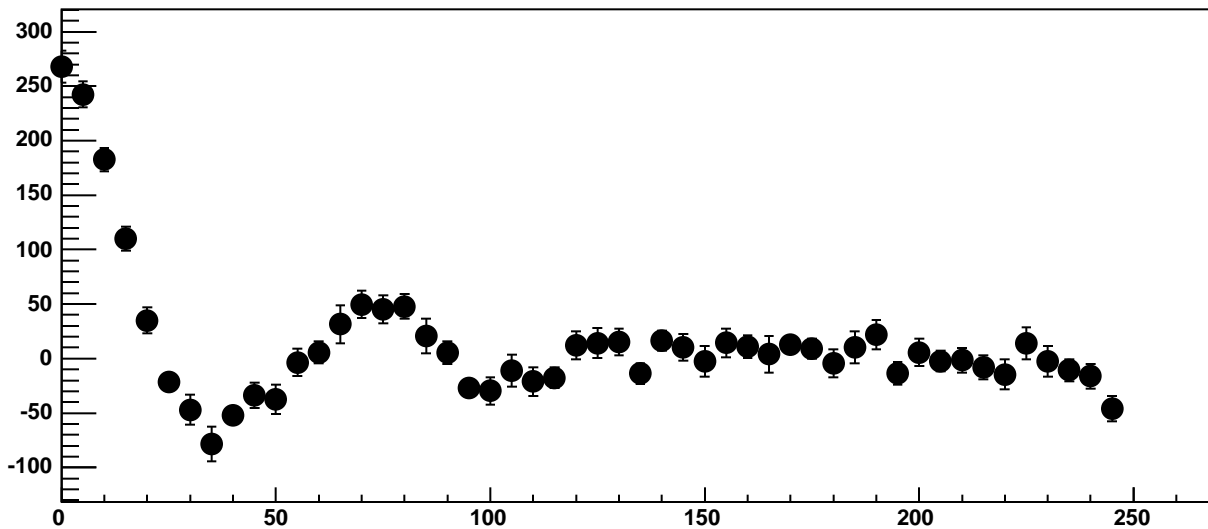


$\chi^2 / \text{ndf}$	303.7 / 41
p0	$-197.8 \pm 4.083$
p1	$98.52 \pm 0.6634$
p2	$-2.972\text{e}+08 \pm 5.592\text{e}+06$
p3	$2.876\text{e}+07 \pm 4.414\text{e}+05$
p4	$9.702 \pm 0.1051$

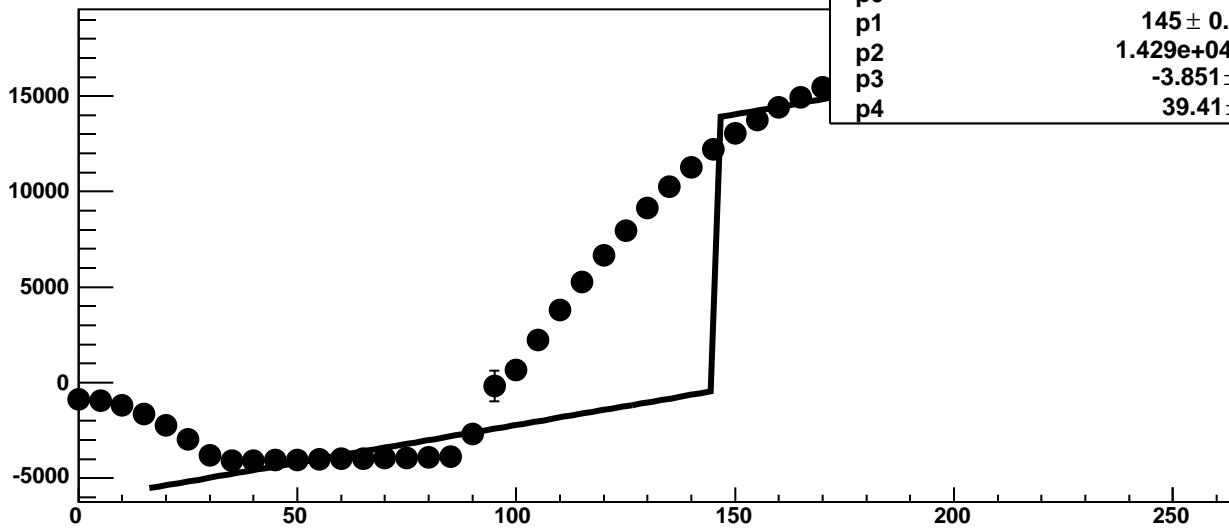
Chip 4, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

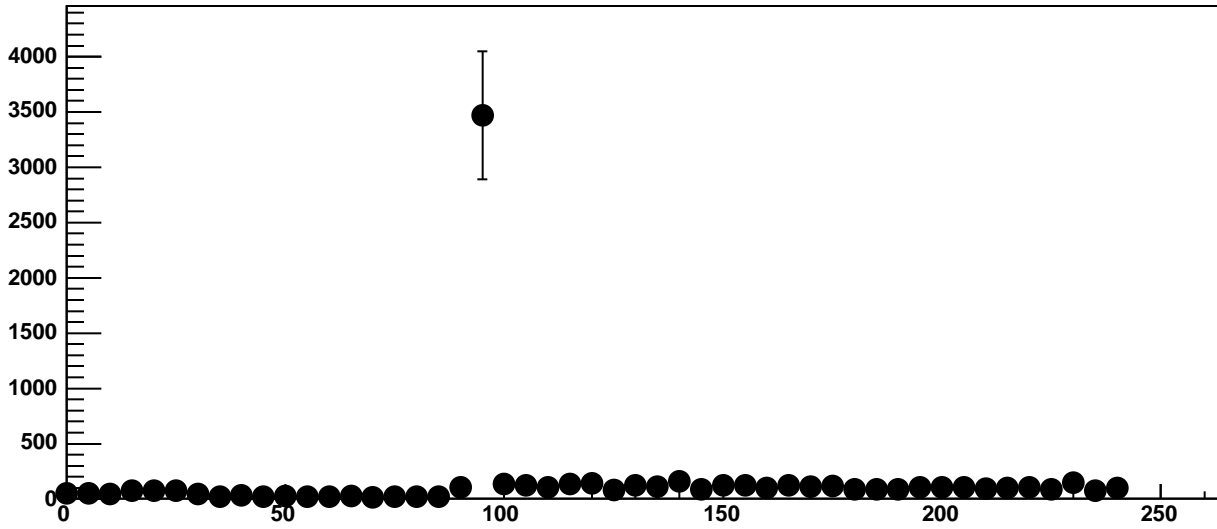


Chip 4, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

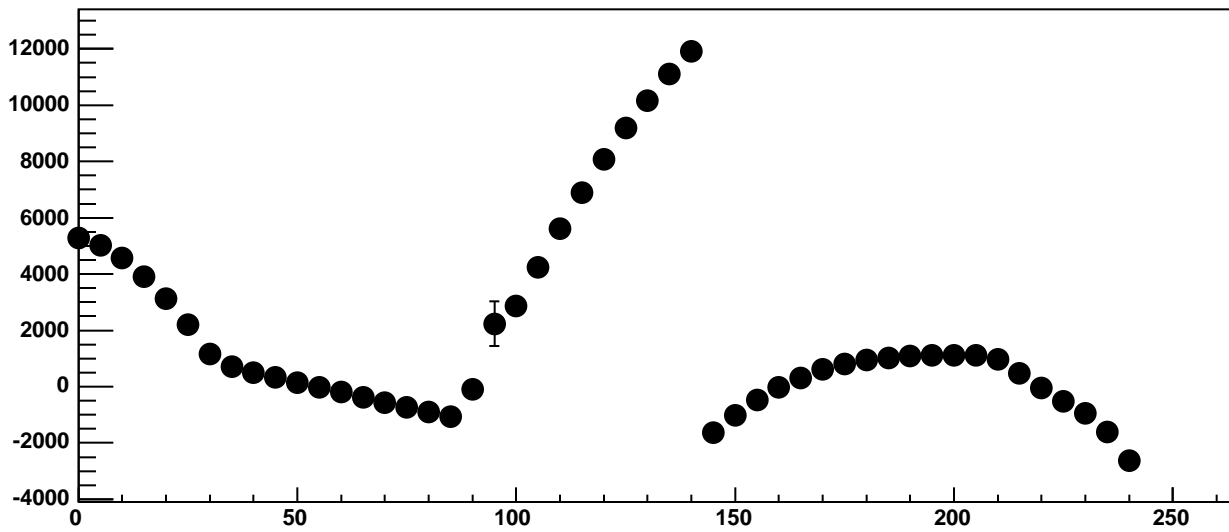


$\chi^2 / \text{ndf}$	1.215e+06 / 41
p0	-441.5 ± 20.02
p1	145 ± 0.0001951
p2	1.429e+04 ± 16.87
p3	-3.851 ± 0.2535
p4	39.41 ± 0.2228

Chip 4, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

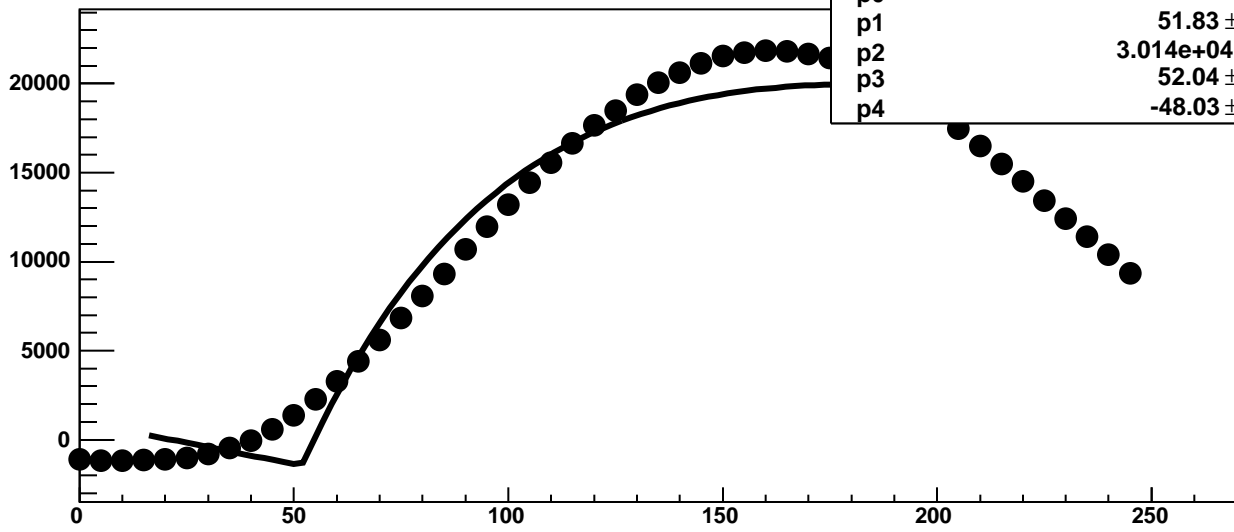


Chip 4, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold



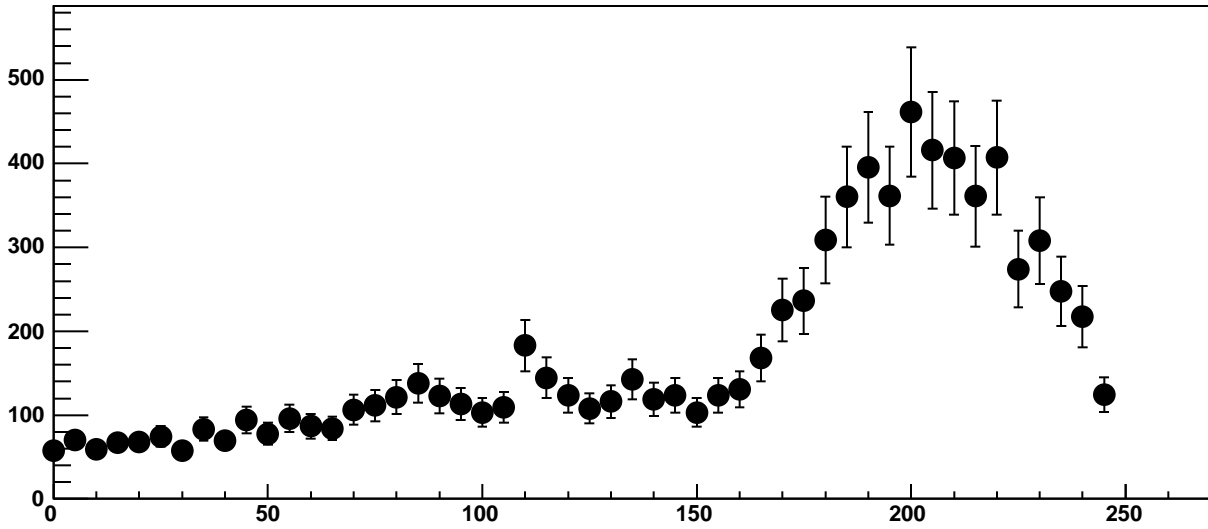


Chip 4, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

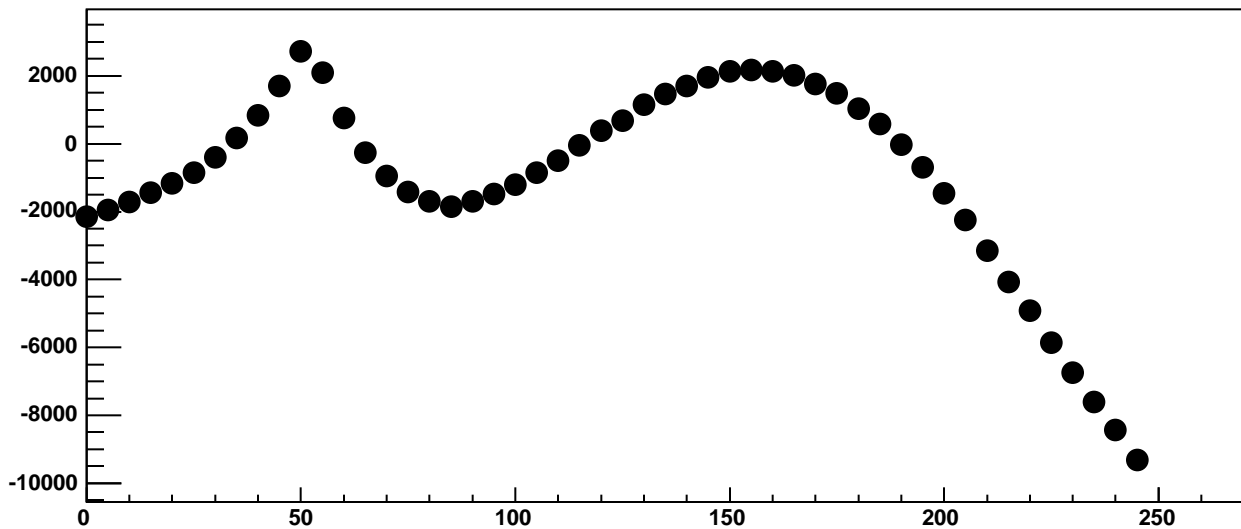


$\chi^2 / \text{ndf}$	1.92e+05 / 41
p0	-1458 ± 8.809
p1	51.83 ± 0.0315
p2	3.014e+04 ± 70.34
p3	52.04 ± 0.1244
p4	-48.03 ± 0.3586

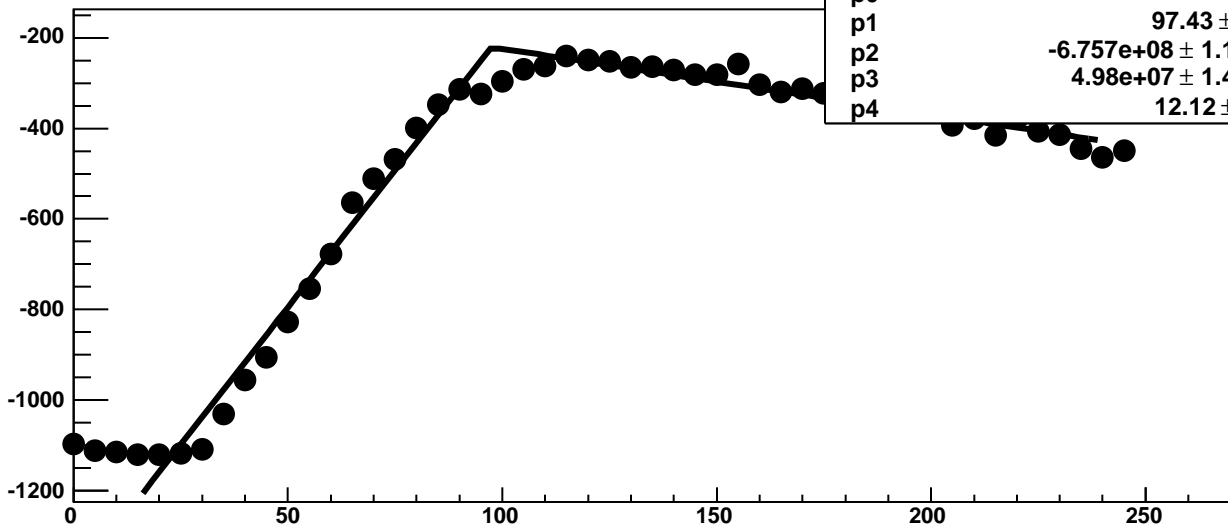
Chip 4, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

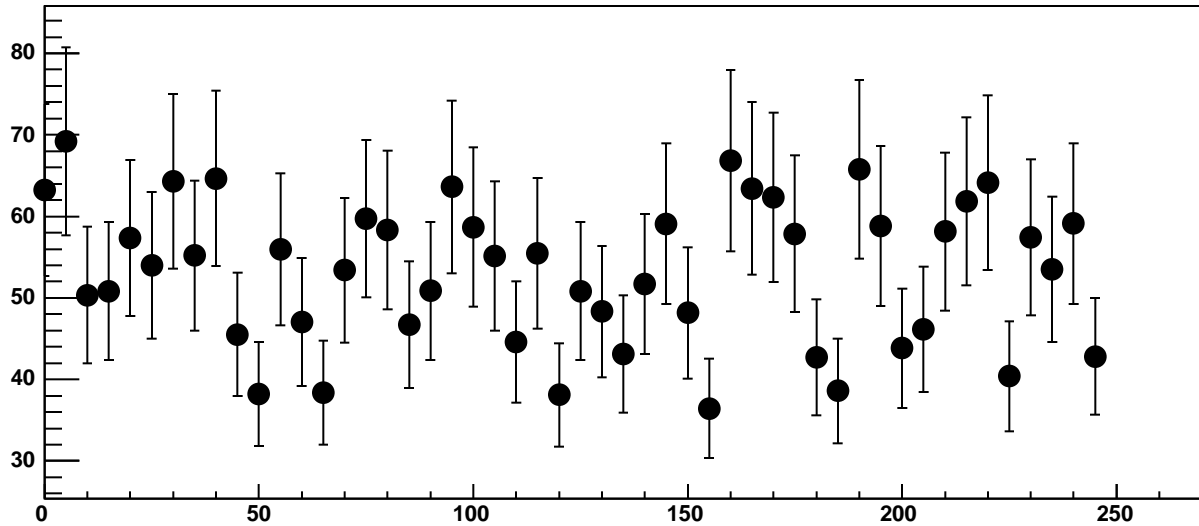


Chip 4, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

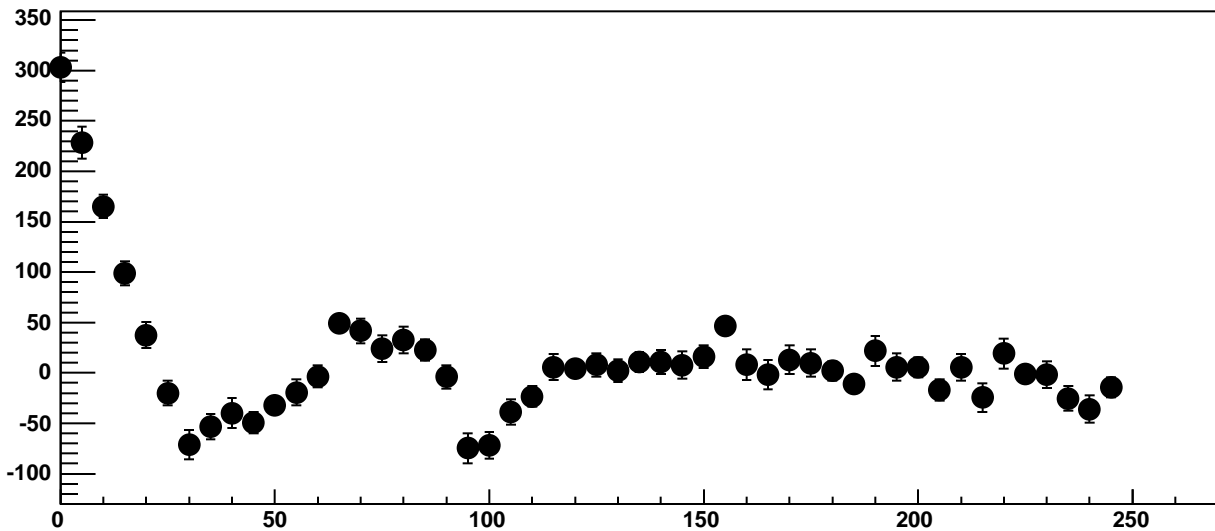


$\chi^2 / \text{ndf}$	356.4 / 41
p0	$-220.3 \pm 4.536$
p1	$97.43 \pm 0.3915$
p2	$-6.757\text{e}+08 \pm 1.185\text{e}+07$
p3	$4.98\text{e}+07 \pm 1.407\text{e}+06$
p4	$12.12 \pm 0.1242$

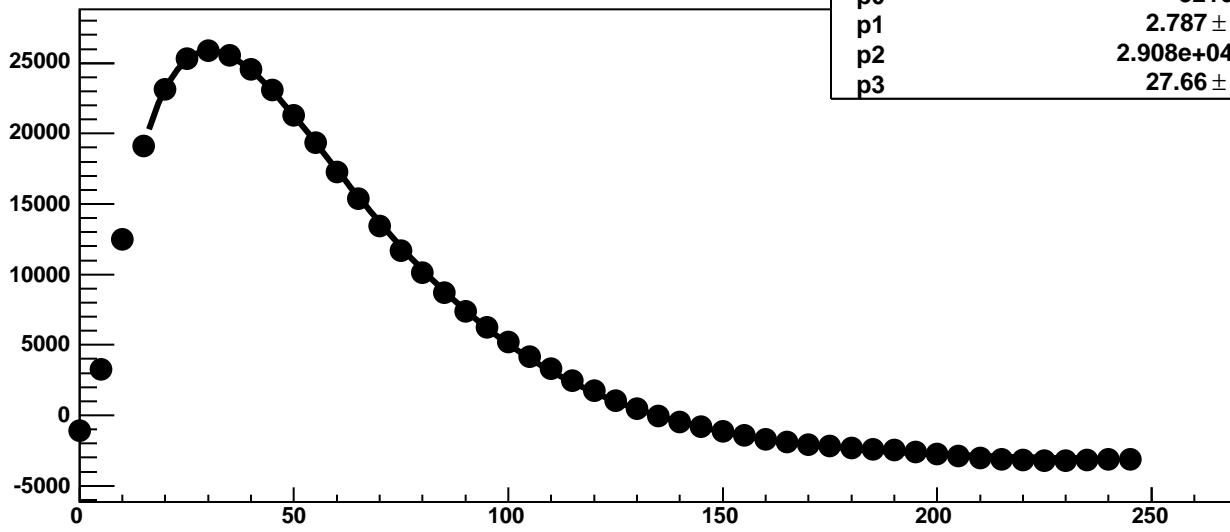
Chip 4, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

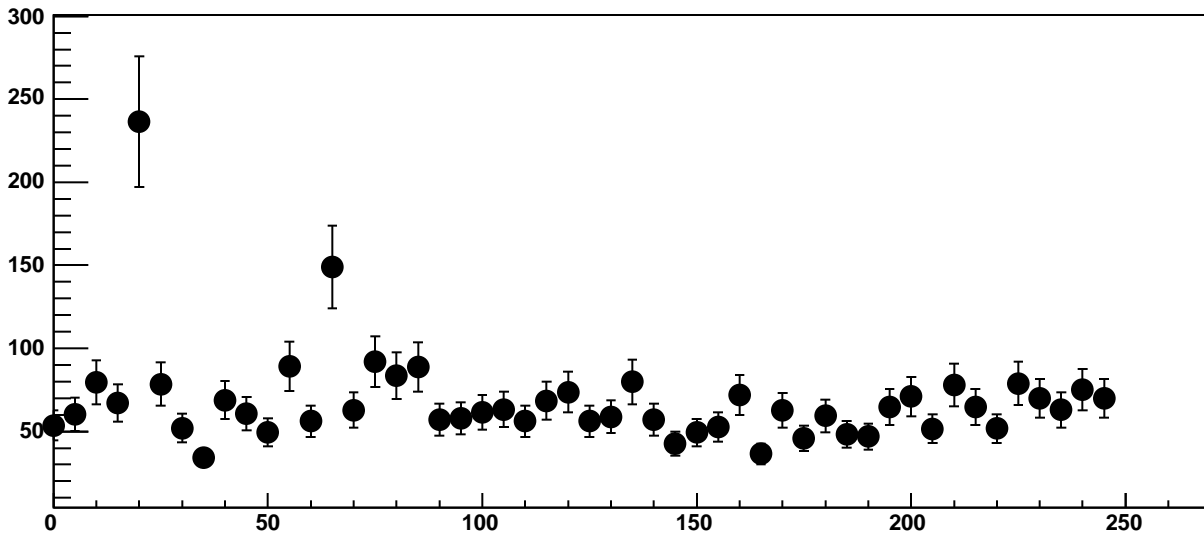


Chip 4, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold

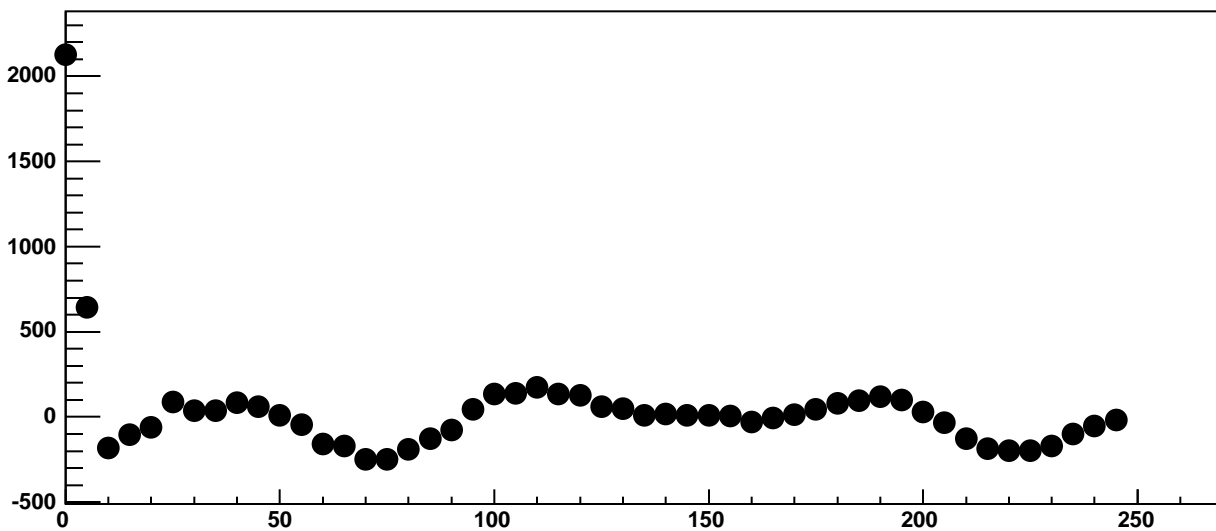


$\chi^2 / \text{ndf}$	2571 / 42
p0	-3216 ± 3.715
p1	2.787 ± 0.01736
p2	2.908e+04 ± 5.742
p3	27.66 ± 0.01144

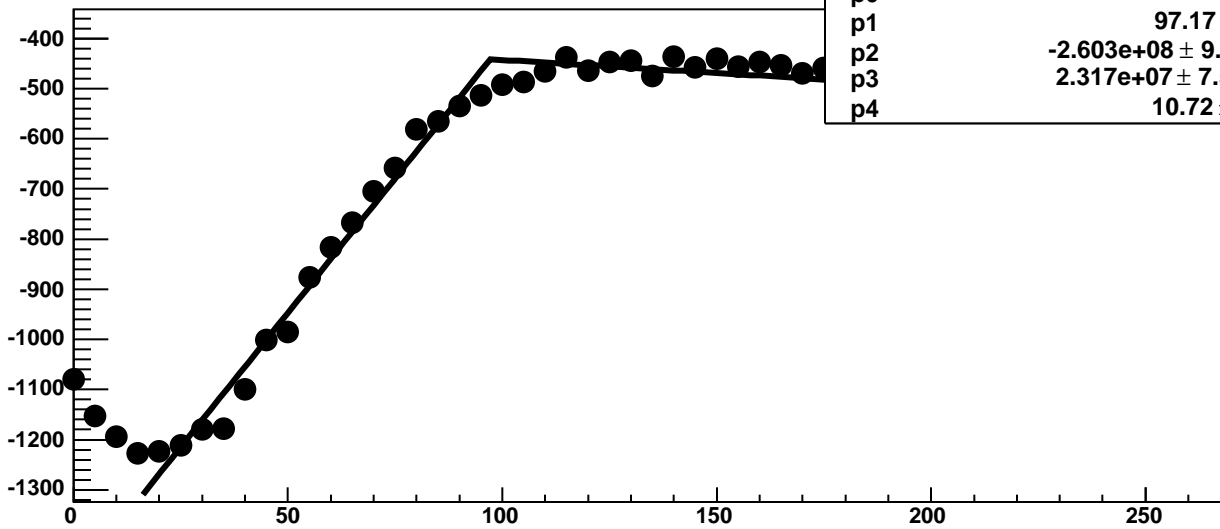
Chip 4, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

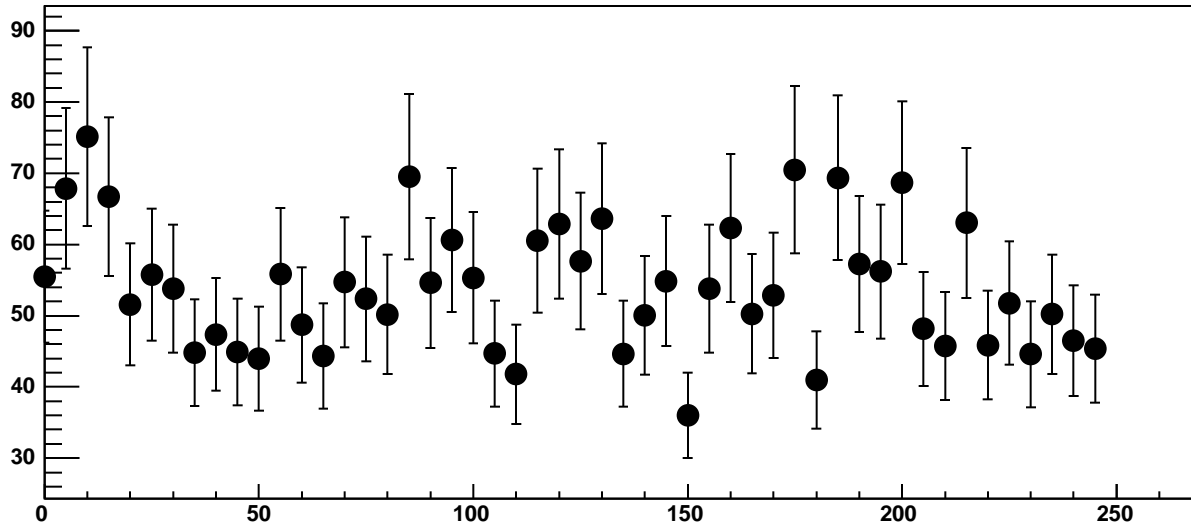


Chip 4, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

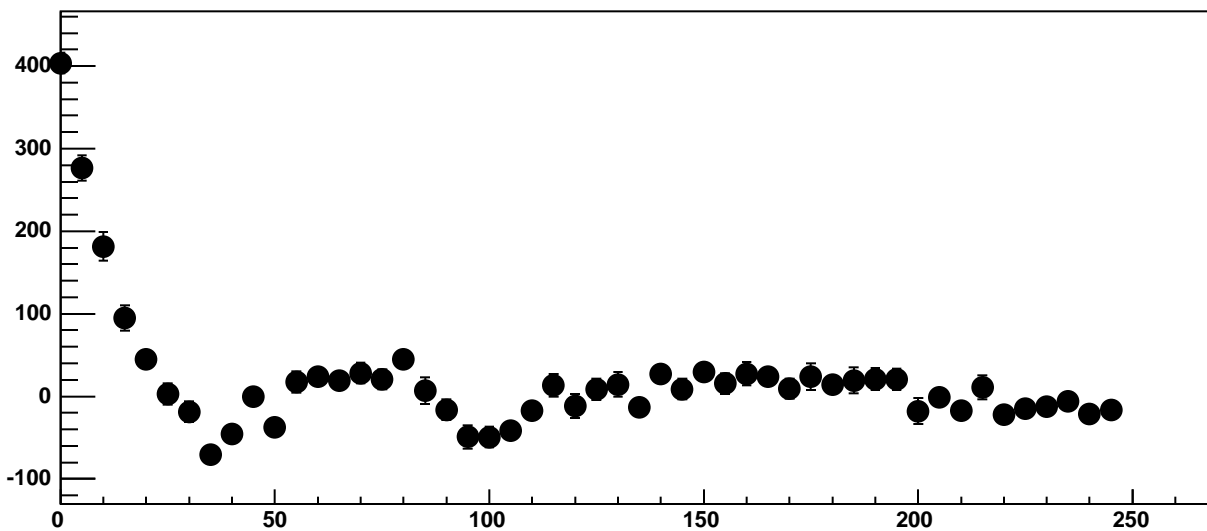


$\chi^2 / \text{ndf}$	275.9 / 41
p0	-441.2 ± 4.128
p1	97.17 ± 0.6727
p2	-2.603e+08 ± 9.091e+06
p3	2.317e+07 ± 7.599e+05
p4	10.72 ± 0.1274

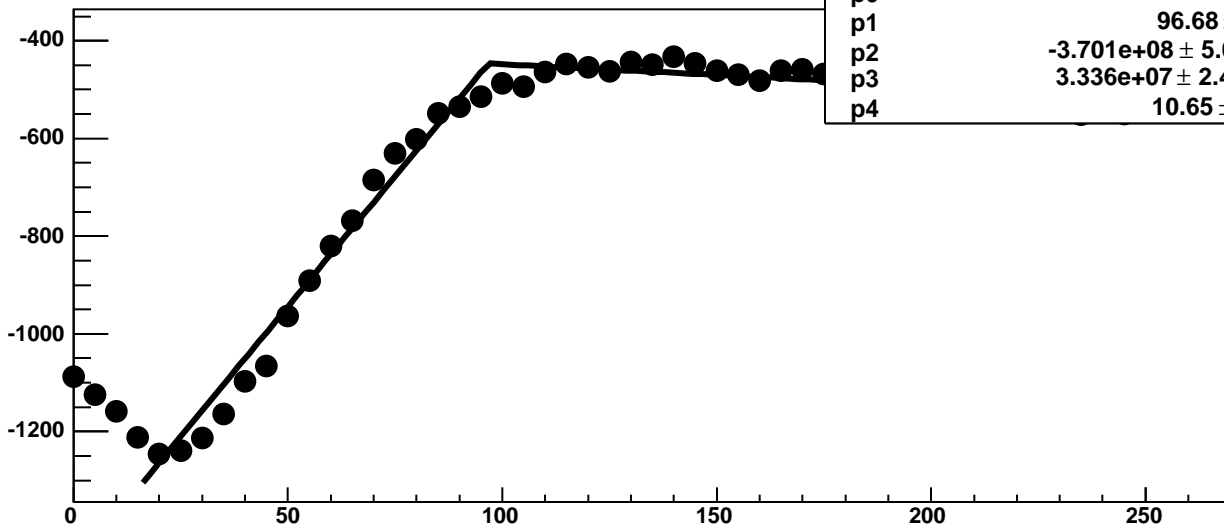
Chip 4, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

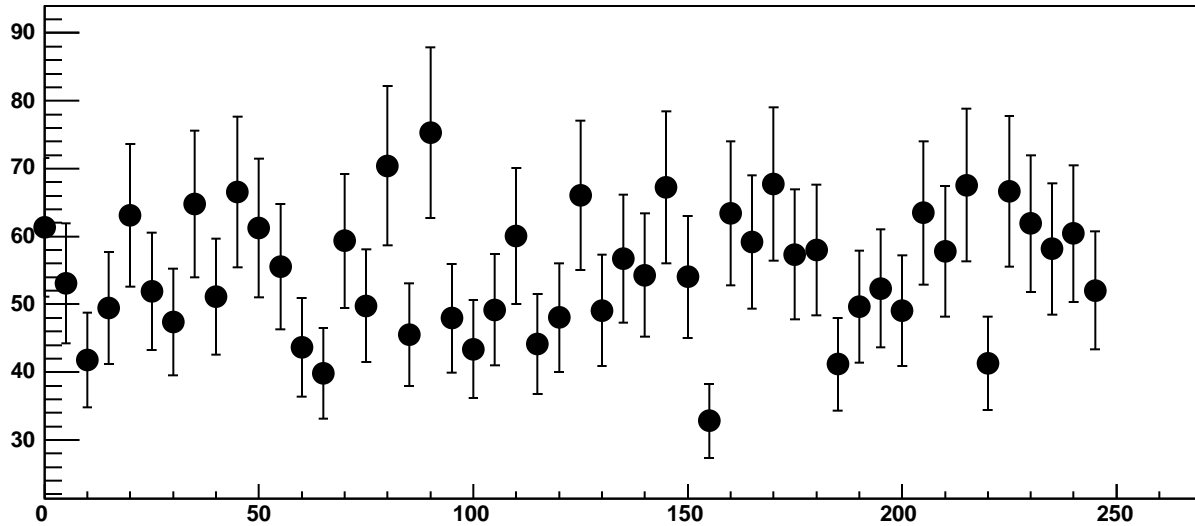


Chip 4, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

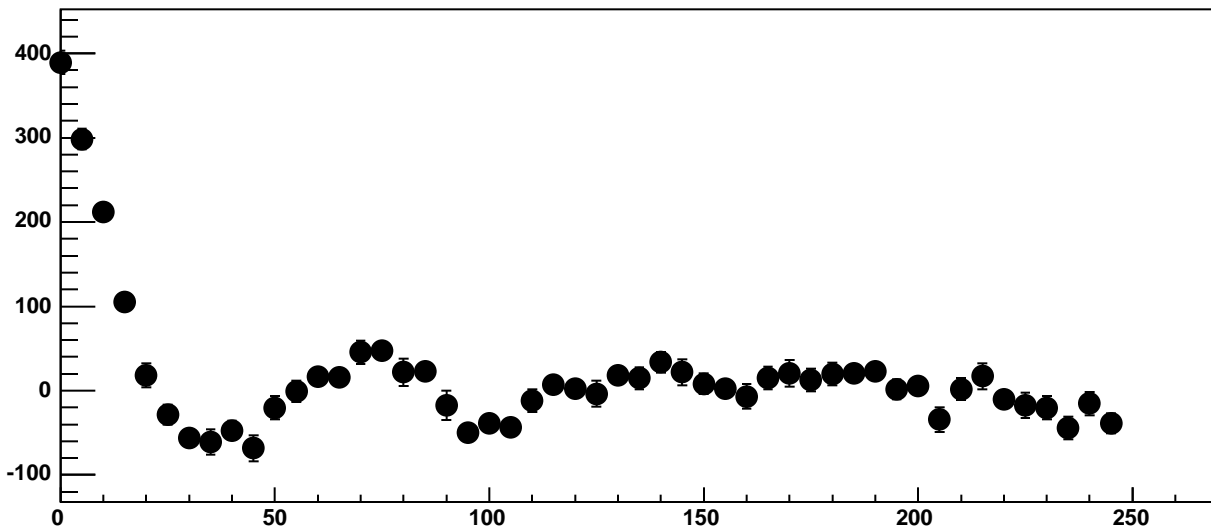


$\chi^2 / \text{ndf}$	320.7 / 41
p0	-446.6 ± 4.23
p1	96.68 ± 0.6591
p2	-3.701e+08 ± 5.093e+06
p3	3.336e+07 ± 2.436e+05
p4	10.65 ± 0.1215

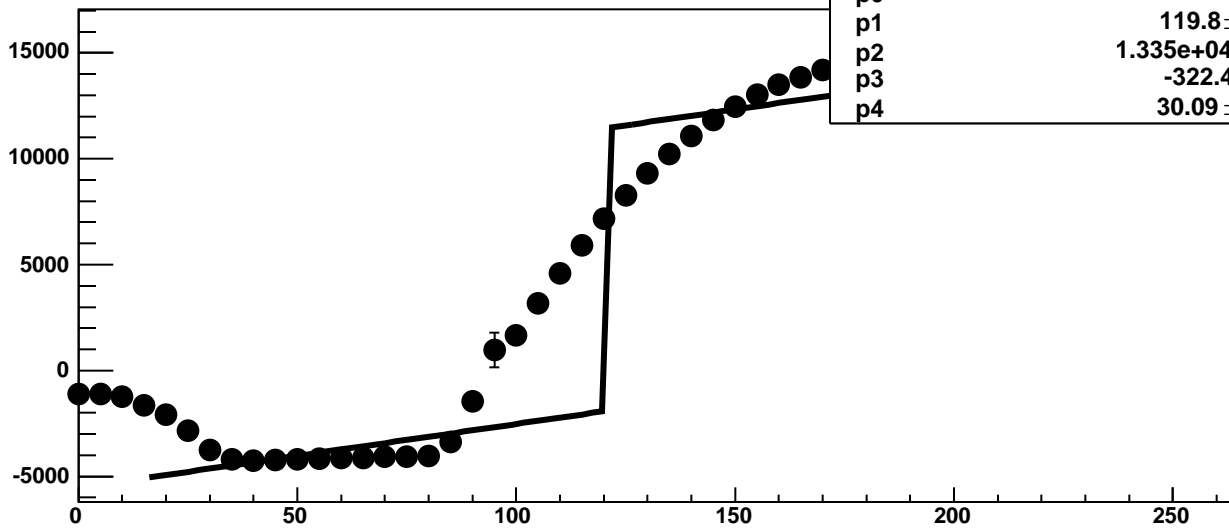
Chip 4, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

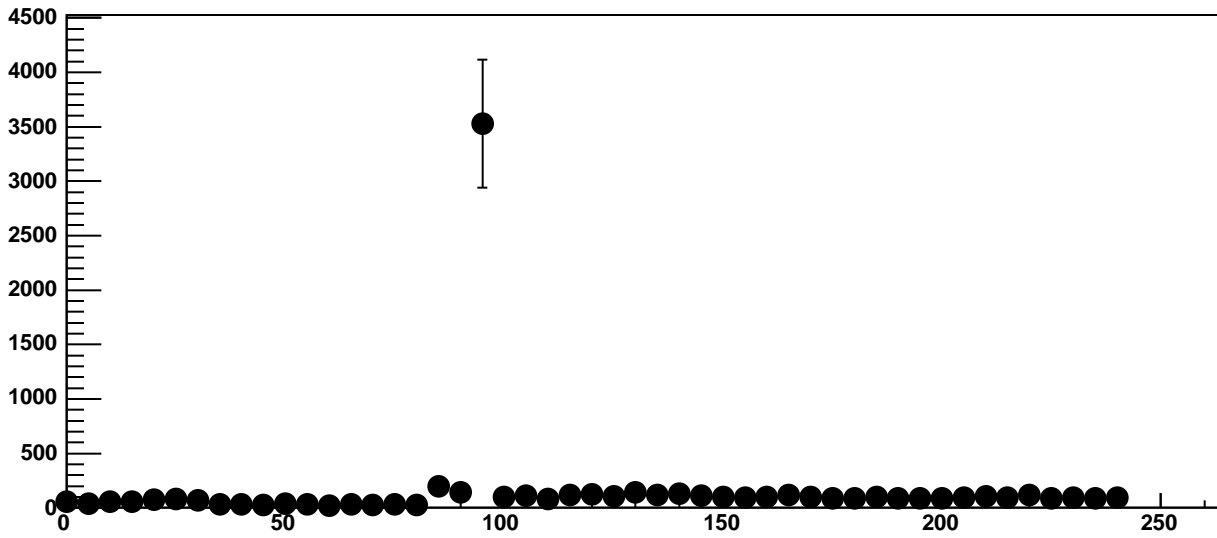


Chip 4, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

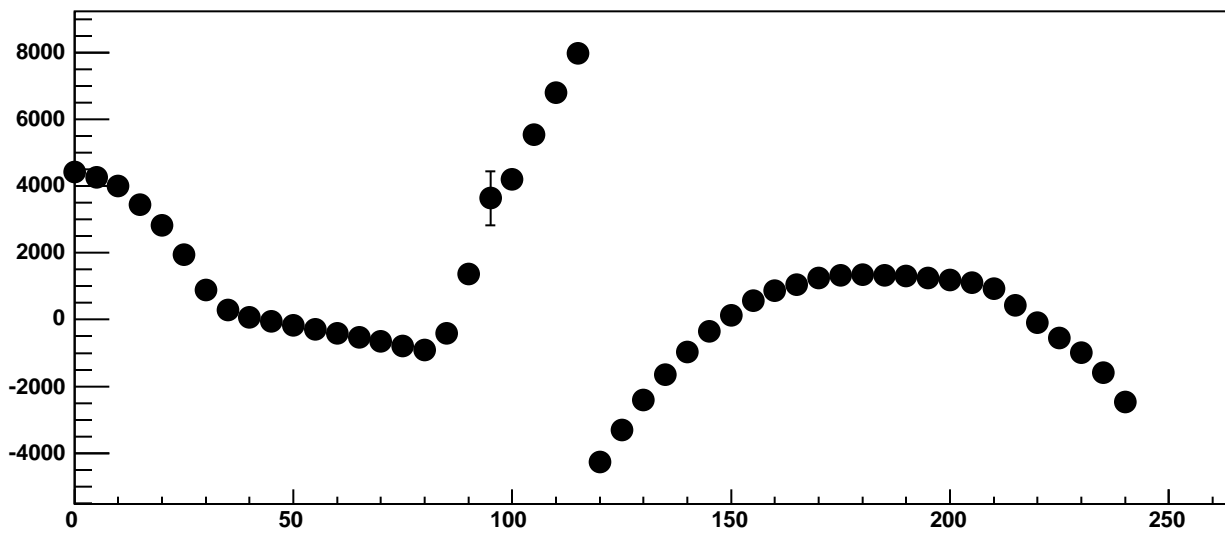


$\chi^2 / \text{ndf}$	5.774e+05 / 41
p0	-1927 ± 2.412
p1	119.8 ± 0.6926
p2	1.335e+04 ± 3.193
p3	-322.4 ± 3.916
p4	30.09 ± 0.1345

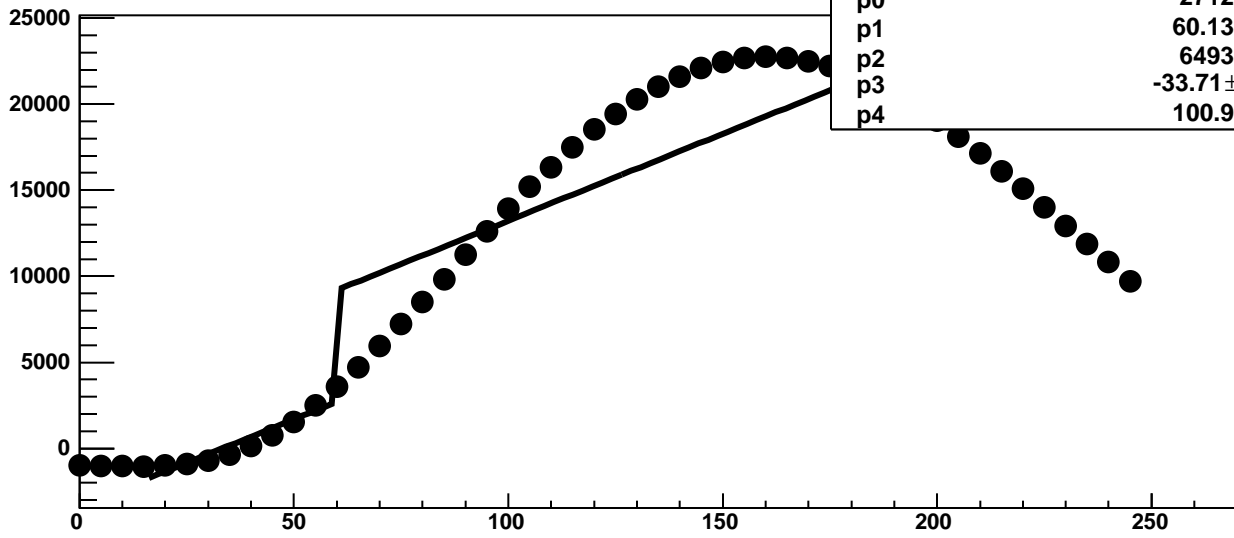
Chip 4, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold

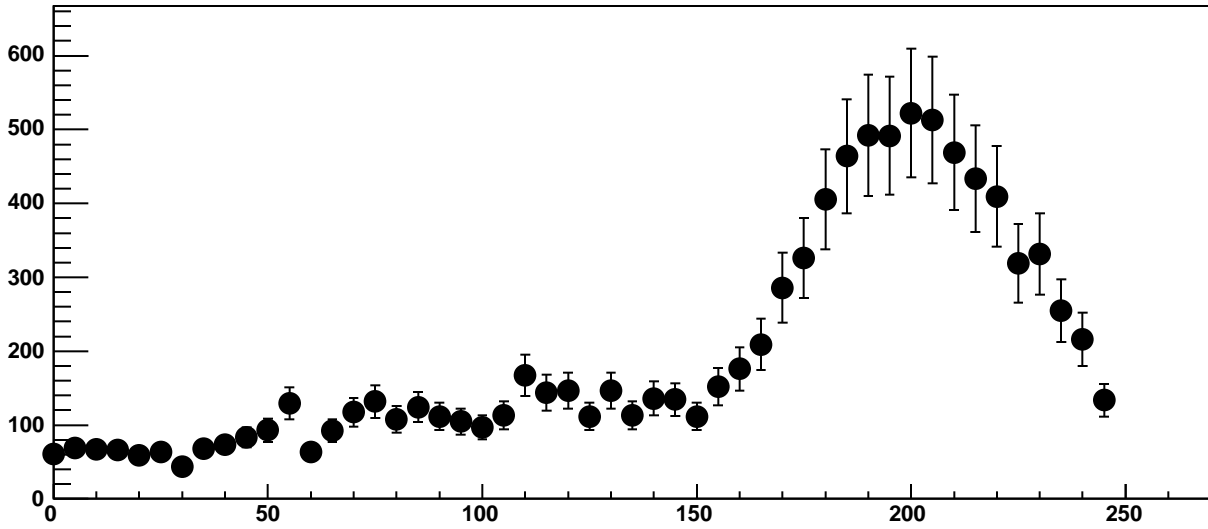


Chip 4, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

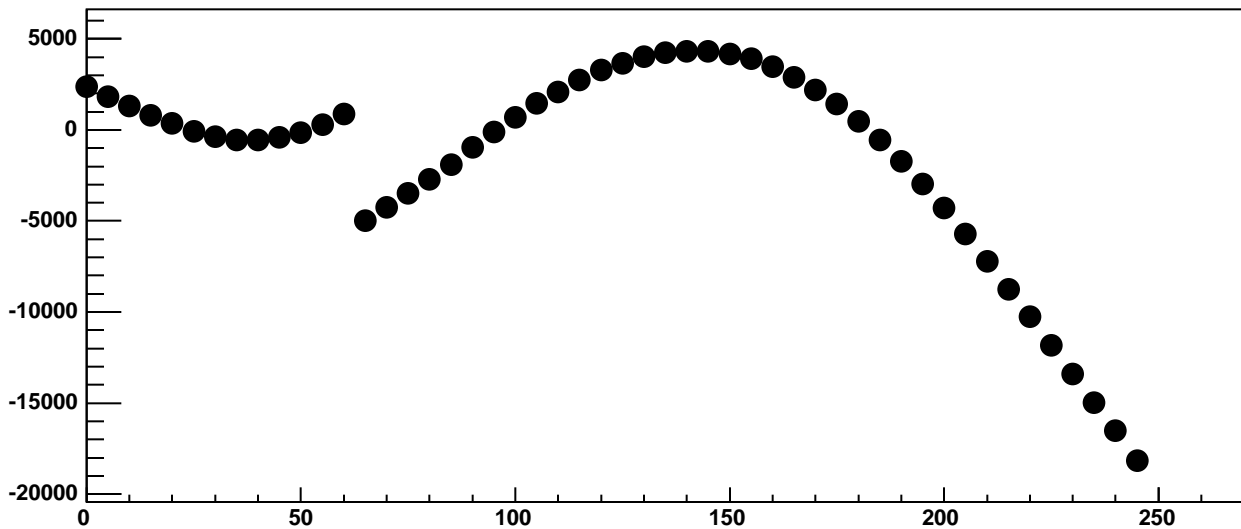


$\chi^2 / \text{ndf}$	5.605e+05 / 41
p0	2712 ± 3.675
p1	60.13 ± 15.56
p2	6493 ± 16.07
p3	-33.71 ± 0.2185
p4	100.9 ± 25.22

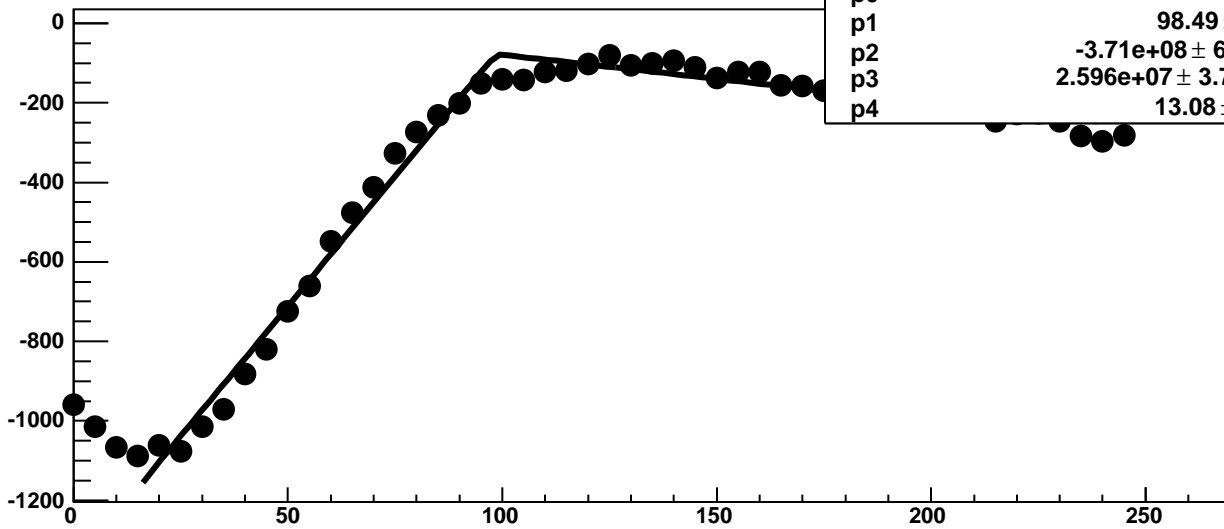
Chip 4, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

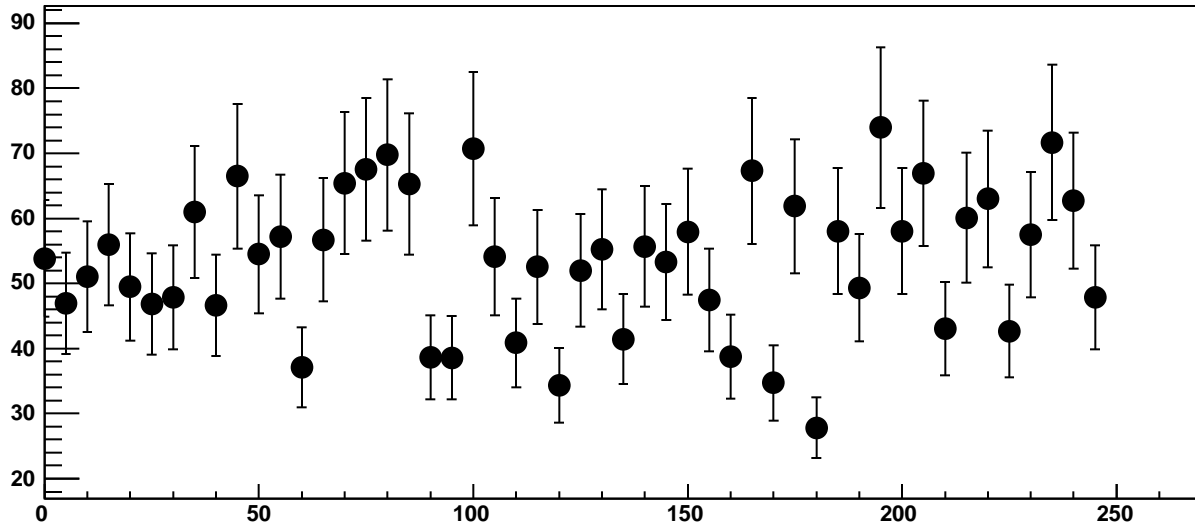


Chip 4, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

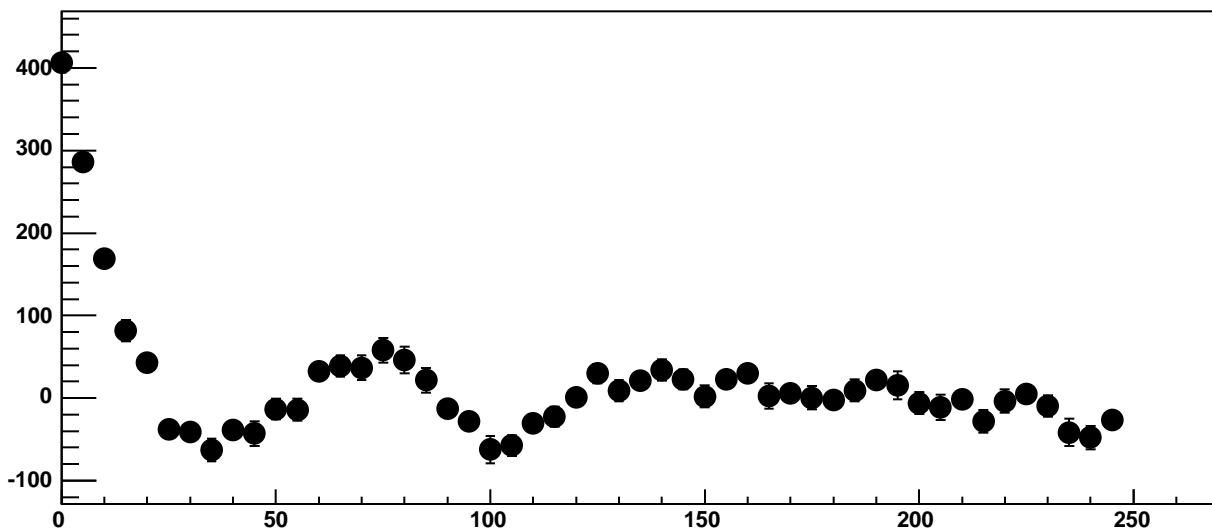


$\chi^2 / \text{ndf}$	308.3 / 41
p0	$-77.37 \pm 3.882$
p1	$98.49 \pm 0.4811$
p2	$-3.71\text{e}+08 \pm 6.57\text{e}+06$
p3	$2.596\text{e}+07 \pm 3.788\text{e}+05$
p4	$13.08 \pm 0.1103$

Chip 4, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

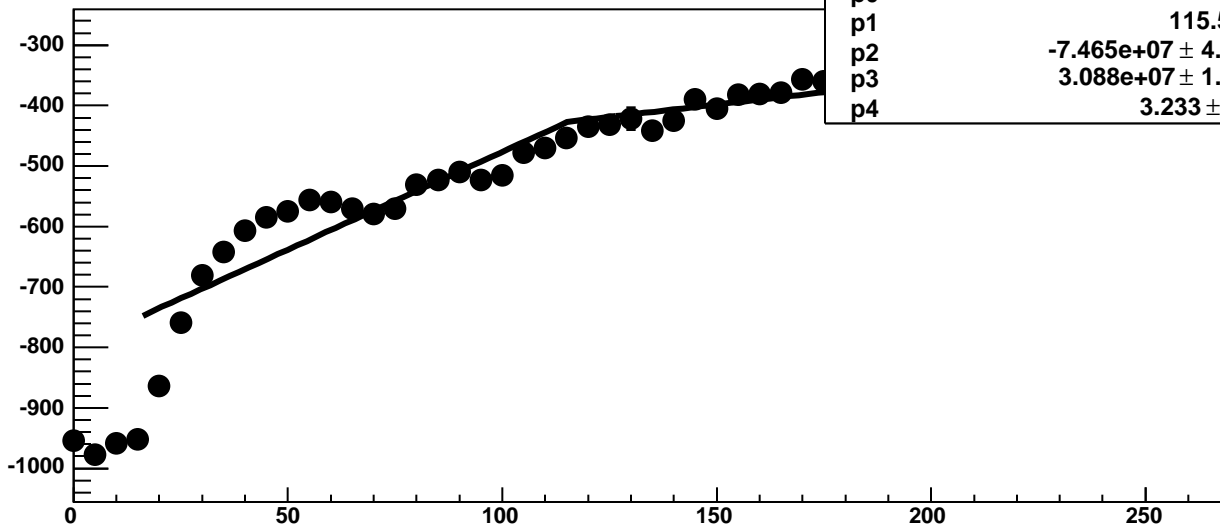


Chip 4, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



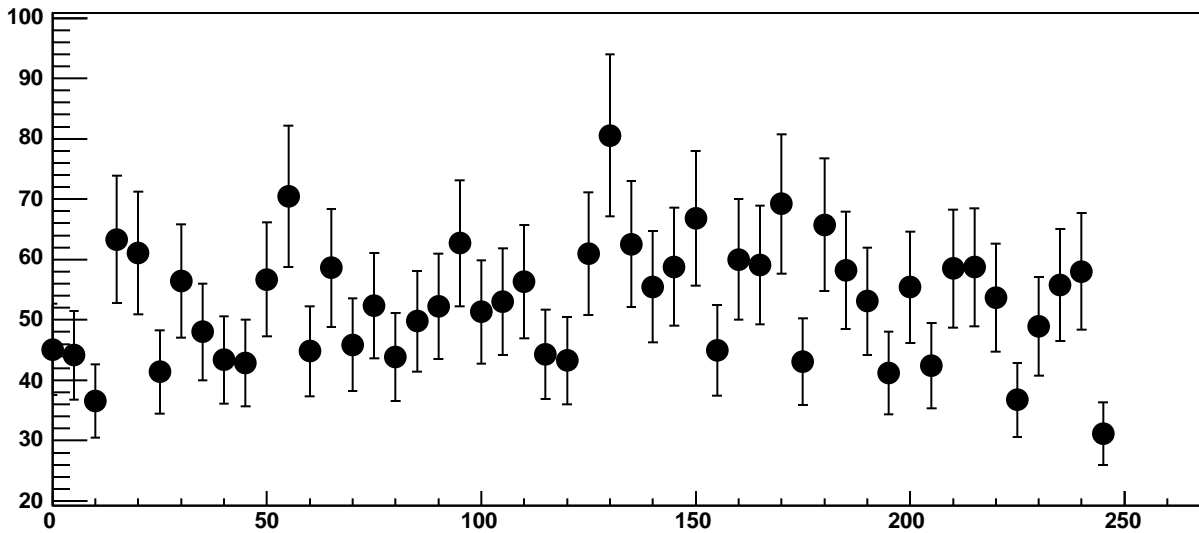


Chip 4, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold

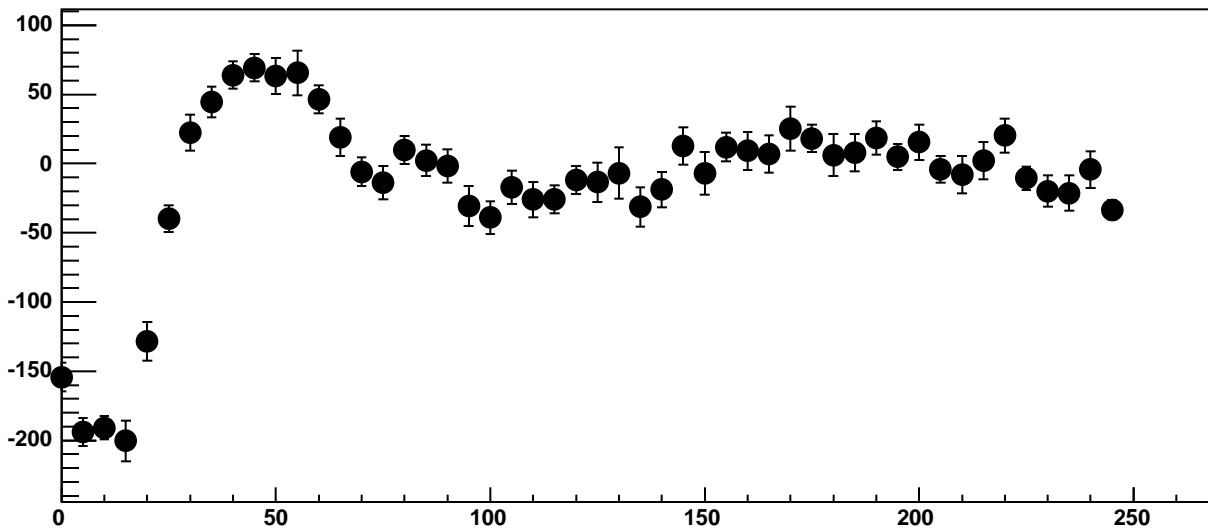


$\chi^2 / \text{ndf}$	529.3 / 41
p0	$-426.2 \pm 7.165$
p1	$115.5 \pm 2.975$
p2	$-7.465\text{e}+07 \pm 4.683\text{e}+06$
p3	$3.088\text{e}+07 \pm 1.294\text{e}+06$
p4	$3.233 \pm 0.08483$

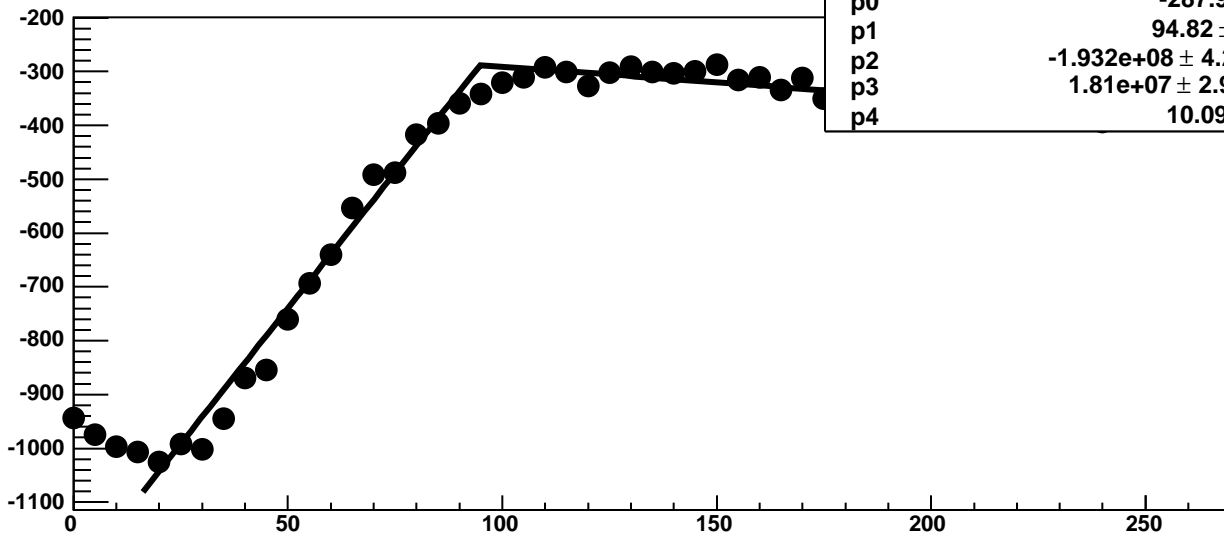
Chip 4, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

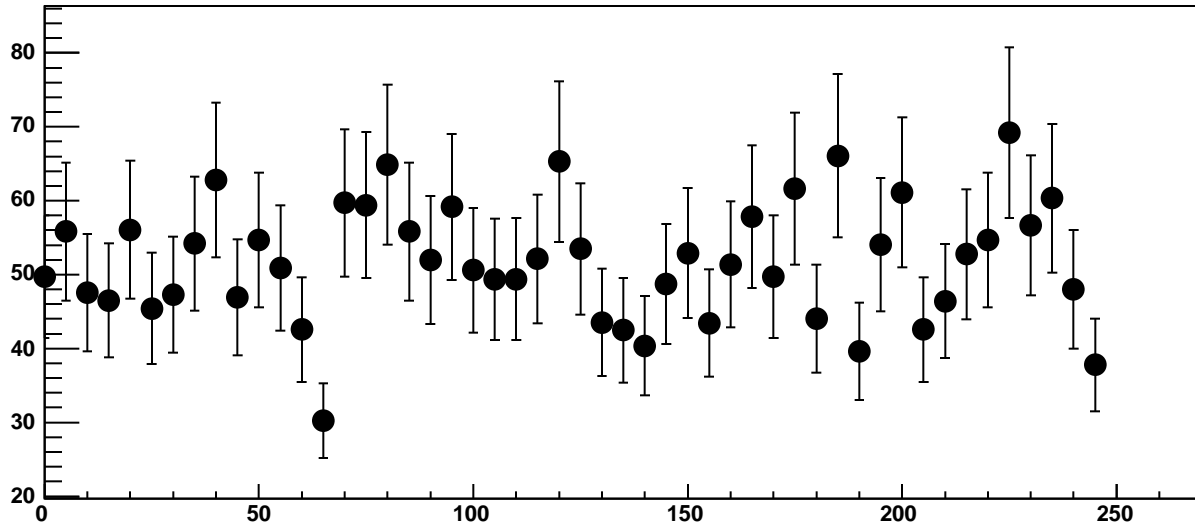


Chip 4, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

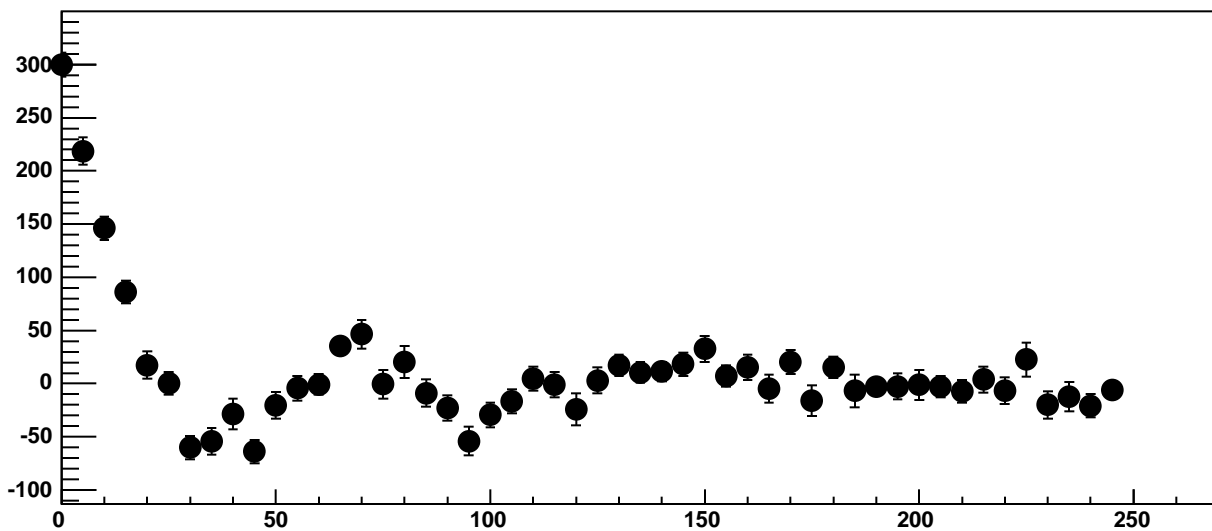


$\chi^2 / \text{ndf}$	264.2 / 41
p0	$-287.9 \pm 3.965$
p1	$94.82 \pm 0.6975$
p2	$-1.932\text{e}+08 \pm 4.282\text{e}+06$
p3	$1.81\text{e}+07 \pm 2.936\text{e}+05$
p4	$10.09 \pm 0.128$

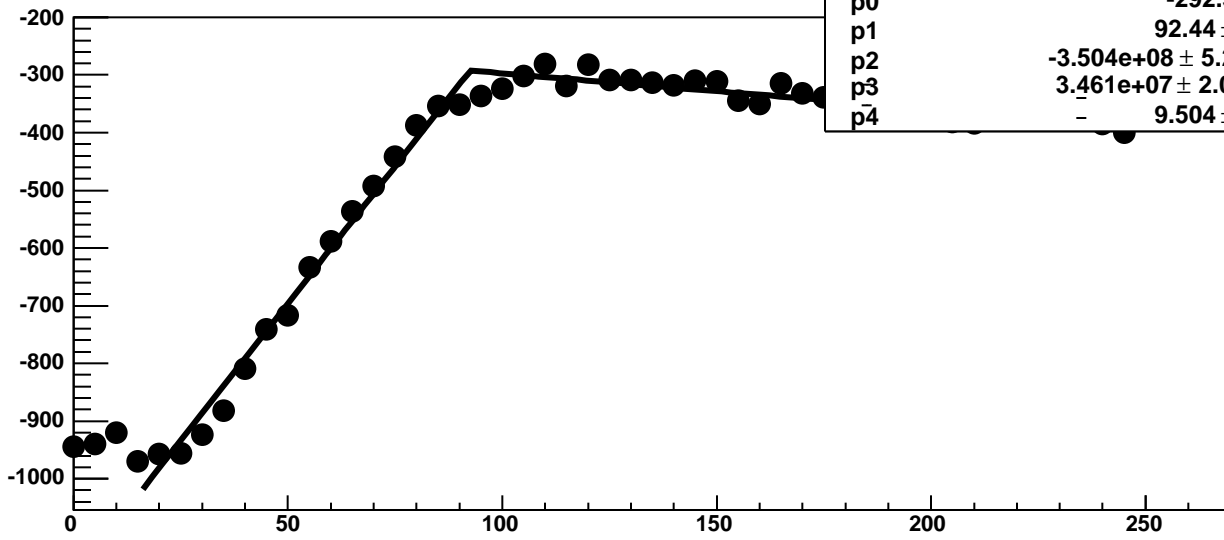
Chip 4, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

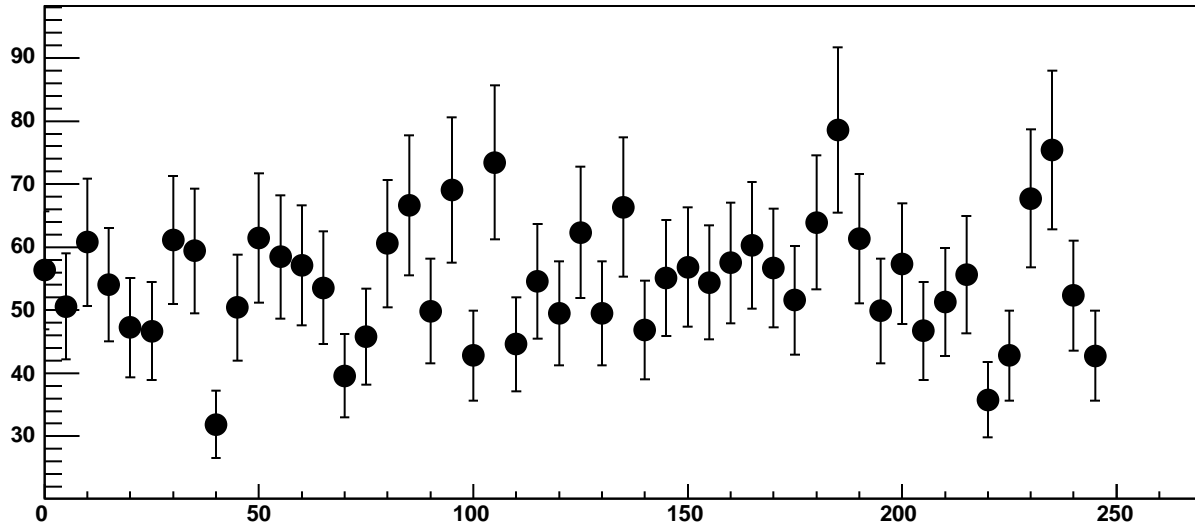


Chip 4, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

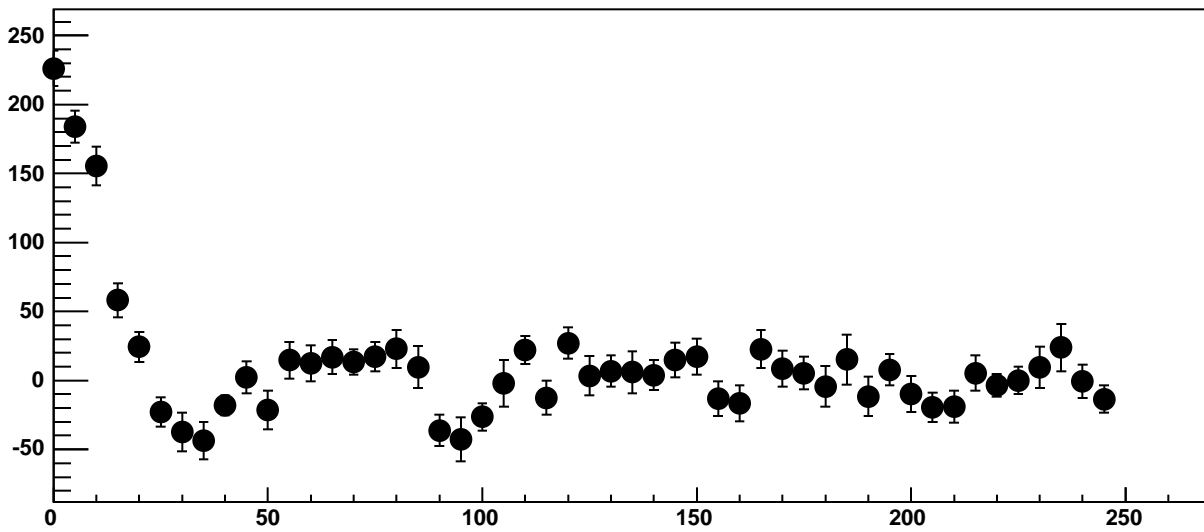


$\chi^2 / \text{ndf}$	126.1 / 41
p0	$-292.5 \pm 4.25$
p1	$92.44 \pm 0.7407$
p2	$-3.504\text{e}+08 \pm 5.266\text{e}+06$
p3	$3.461\text{e}+07 \pm 2.042\text{e}+05$
p4	$- 9.504 \pm 0.1282$

Chip 4, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold

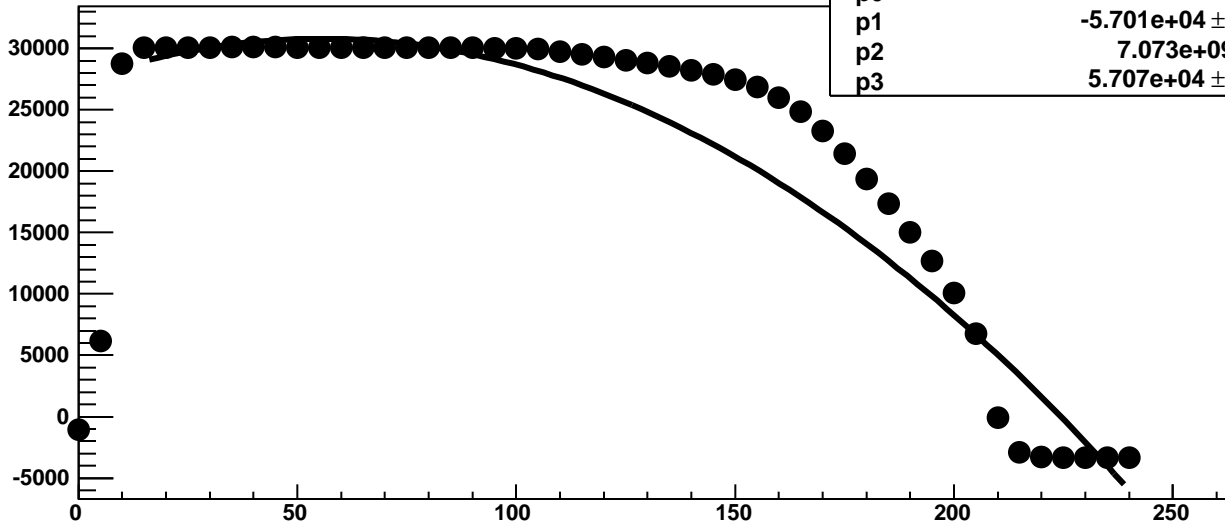


Chip 4, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

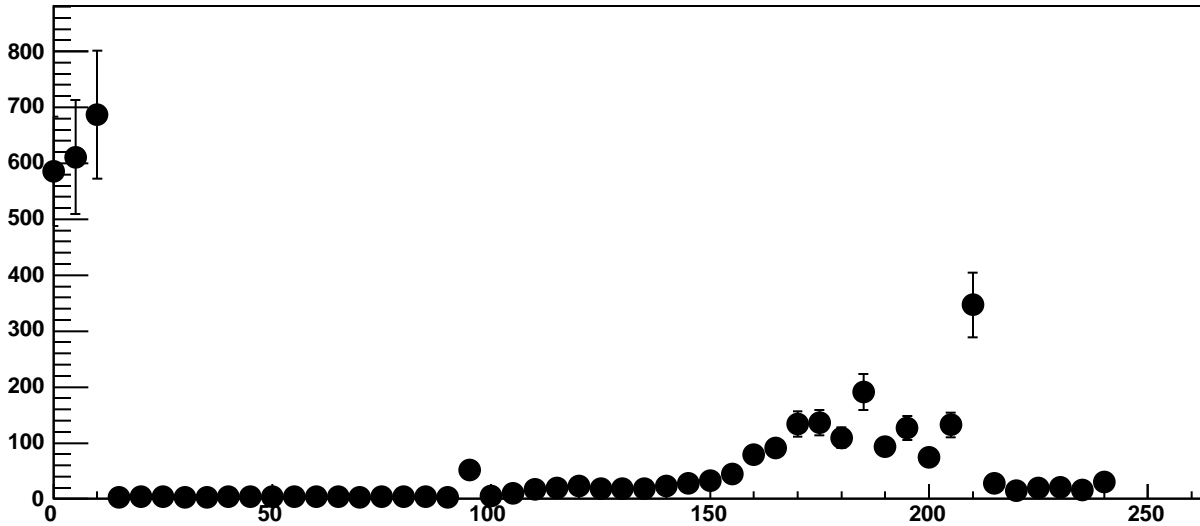


Chip 4, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

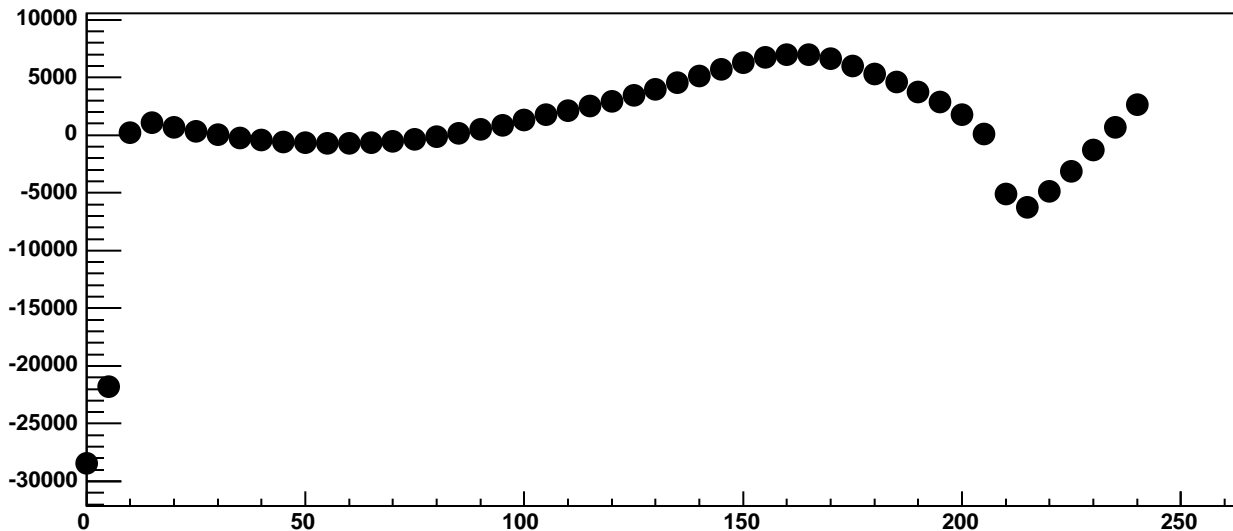
$\chi^2 / \text{ndf}$	1.918e+07 / 42
p0	-7.073e+09 $\pm$ 3.107
p1	-5.701e+04 $\pm$ 0.04202
p2	7.073e+09 $\pm$ 3.107
p3	5.707e+04 $\pm$ 0.04198



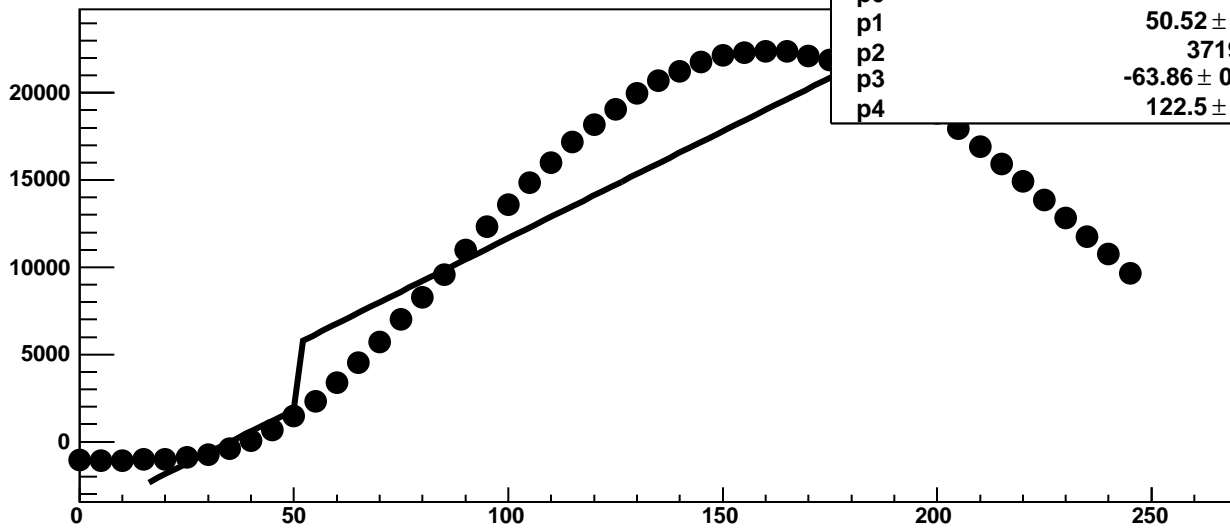
Chip 4, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

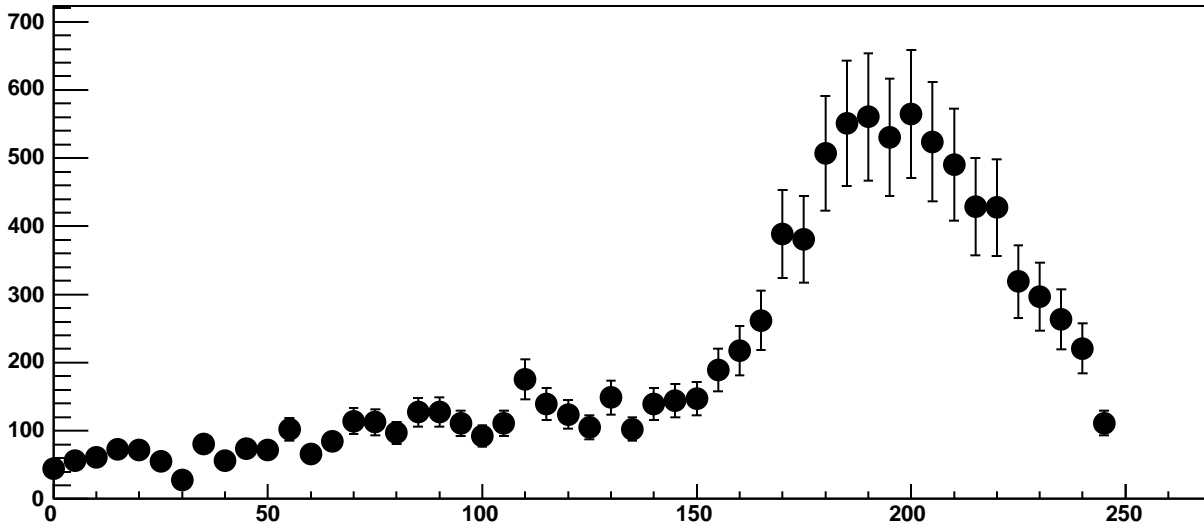


Chip 4, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

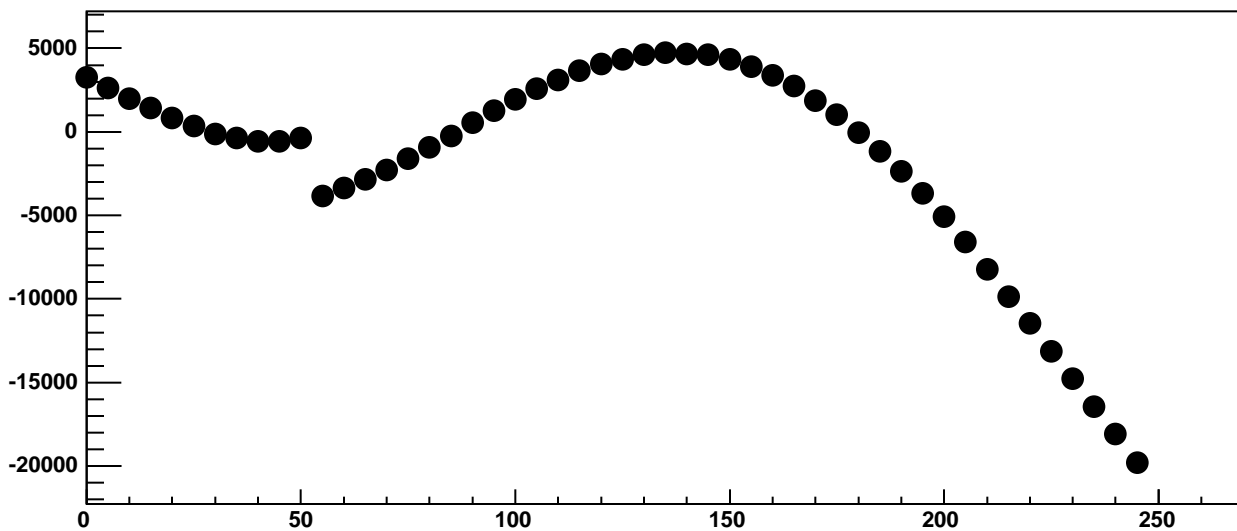


$\chi^2 / \text{ndf}$	6.657e+05 / 41
p0	1888 ± 0.4401
p1	50.52 ± 0.02019
p2	3719 ± 0.45
p3	-63.86 ± 0.001384
p4	122.5 ± 0.04508

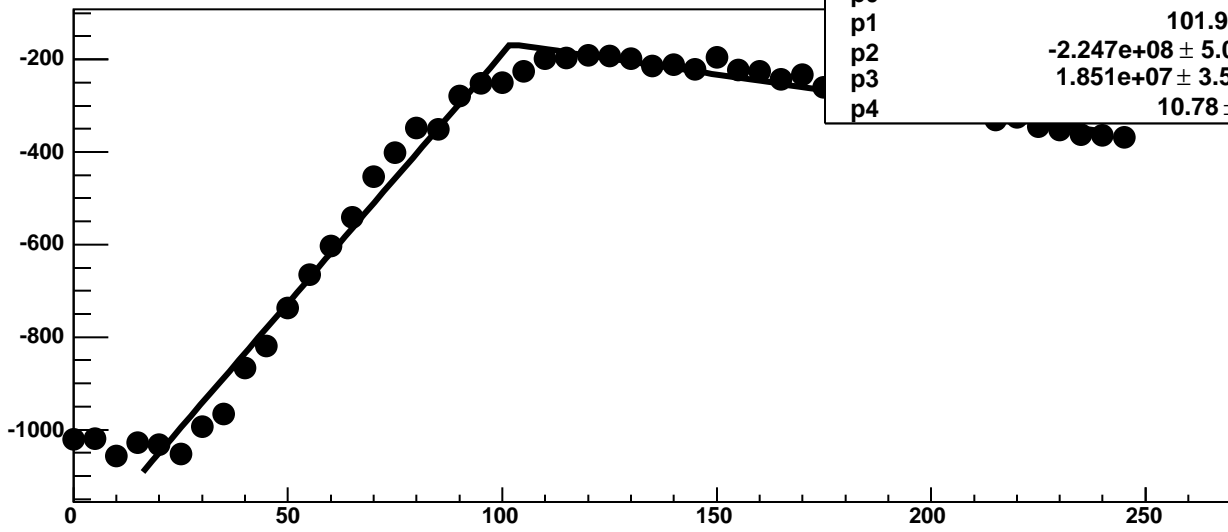
Chip 4, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

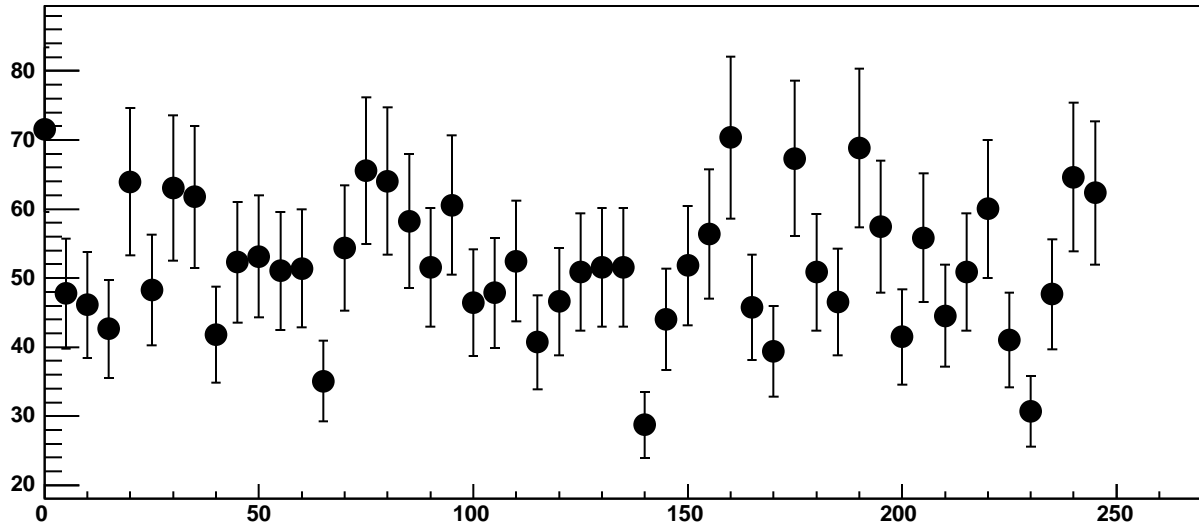


Chip 4, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

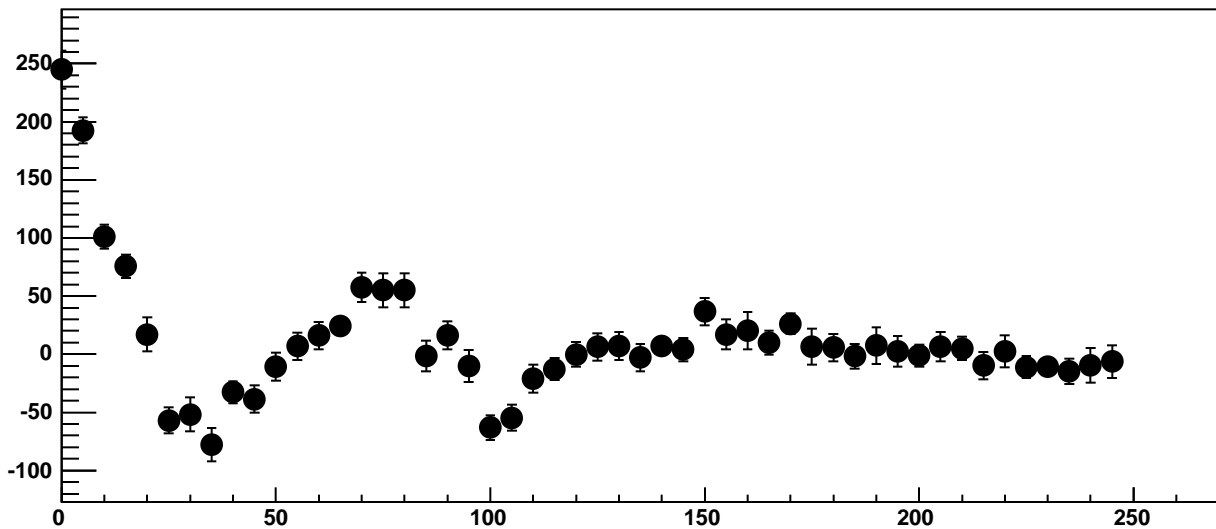


$\chi^2 / \text{ndf}$	313 / 41
p0	$-166.8 \pm 3.657$
p1	$101.9 \pm 0.576$
p2	$-2.247\text{e}+08 \pm 5.028\text{e}+06$
p3	$1.851\text{e}+07 \pm 3.526\text{e}+05$
p4	$10.78 \pm 0.1091$

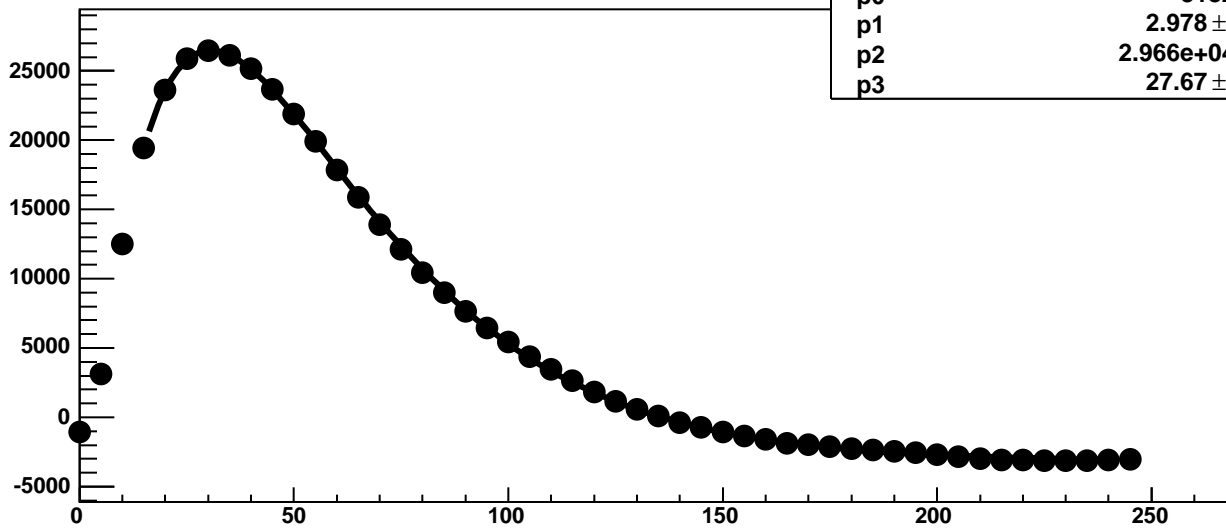
Chip 4, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

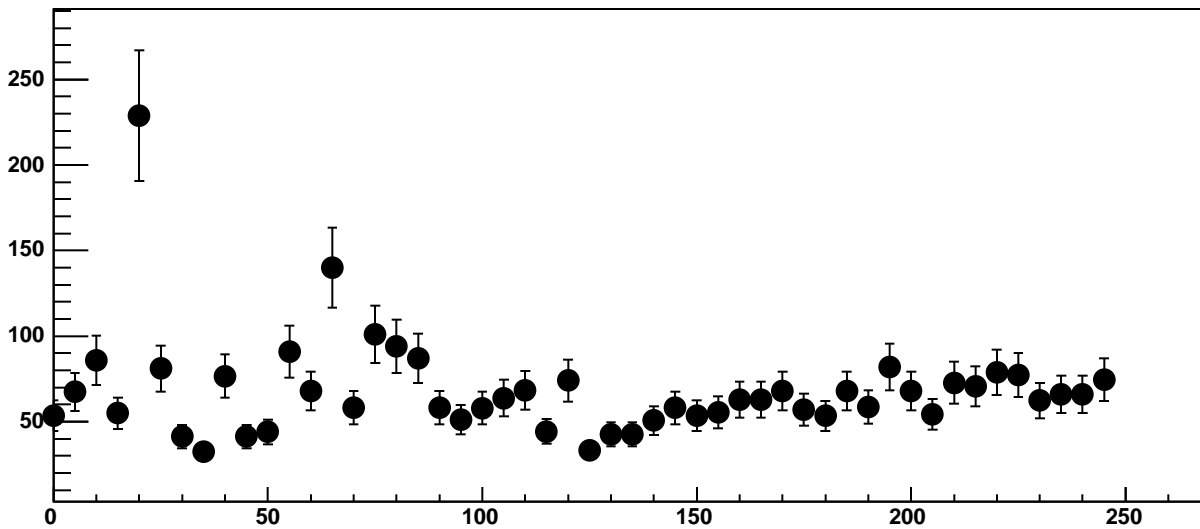


Chip 4, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

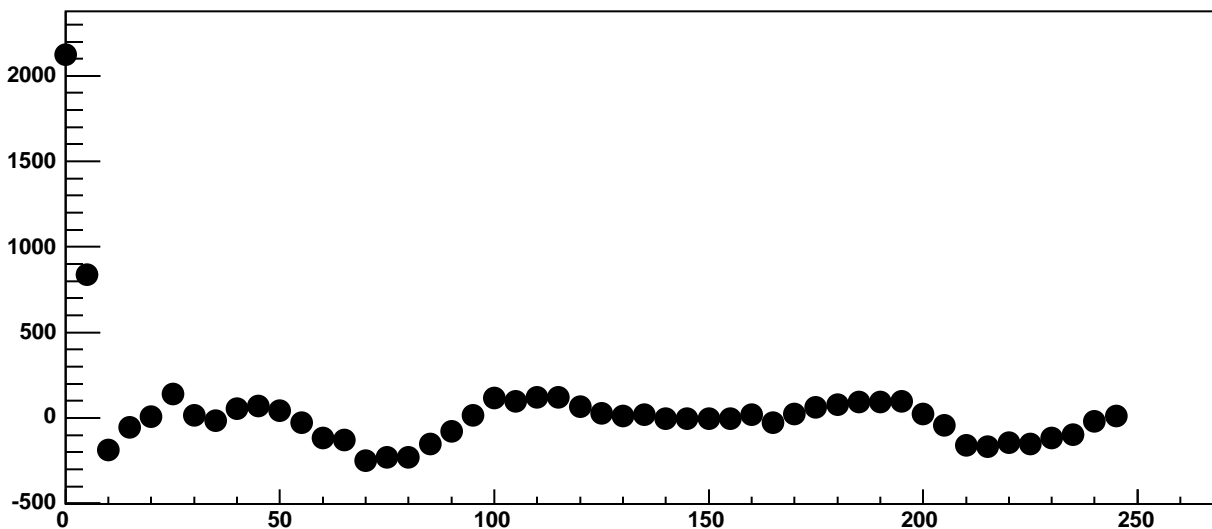


$\chi^2 / \text{ndf}$	1894 / 42
p0	$-3182 \pm 4.013$
p1	$2.978 \pm 0.01428$
p2	$2.966\text{e}+04 \pm 5.401$
p3	$27.67 \pm 0.01044$

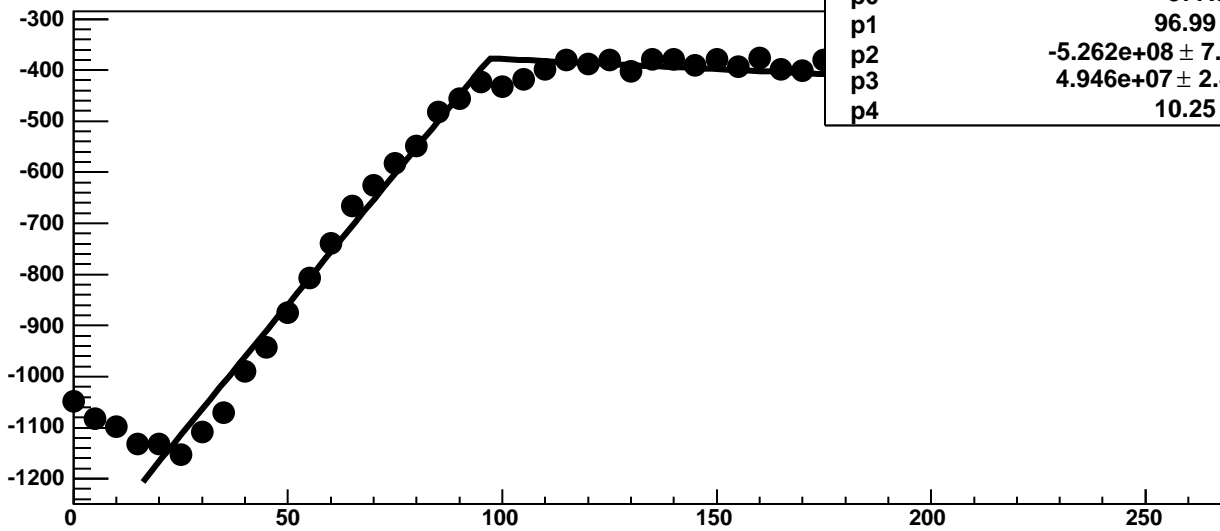
Chip 4, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

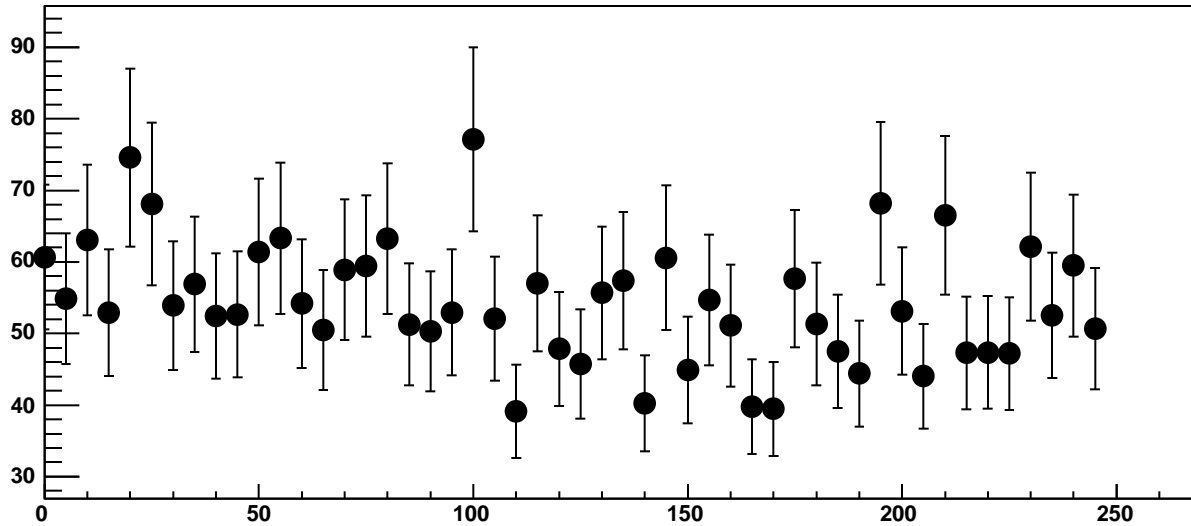


Chip 4, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

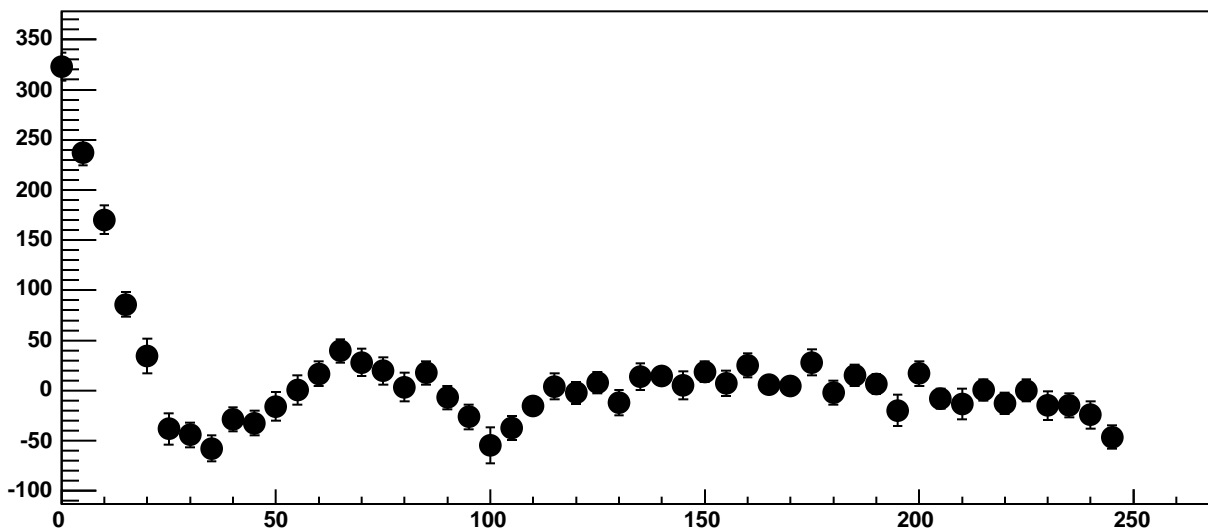


$\chi^2 / \text{ndf}$	189.2 / 41
p0	$-377.3 \pm 4.222$
p1	$96.99 \pm 0.7002$
p2	$-5.262\text{e}+08 \pm 7.347\text{e}+06$
p3	$4.946\text{e}+07 \pm 2.459\text{e}+05$
p4	$10.25 \pm 0.1282$

Chip 4, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold

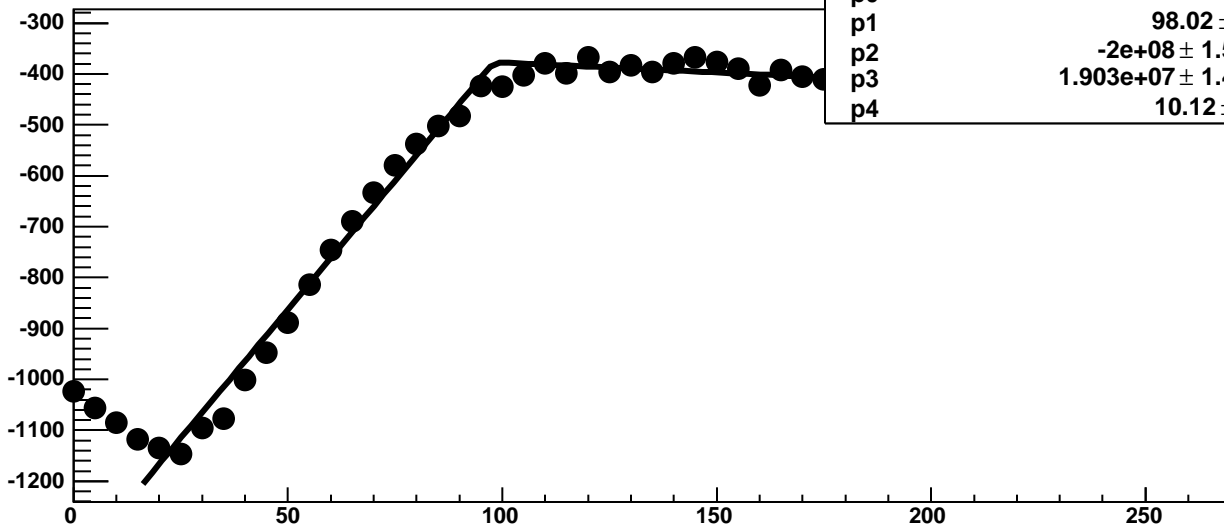


Chip 4, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



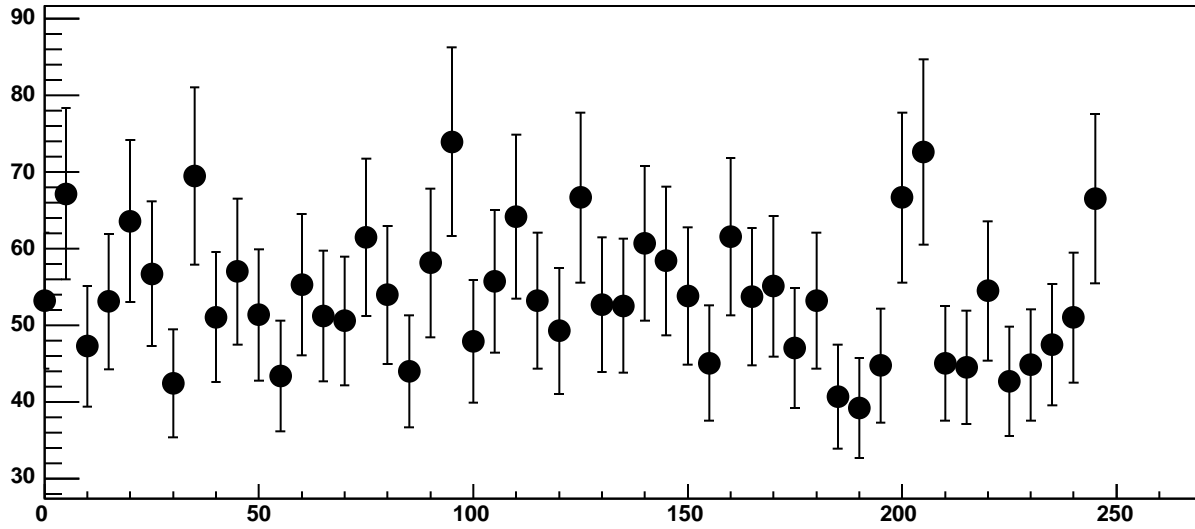


Chip 4, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

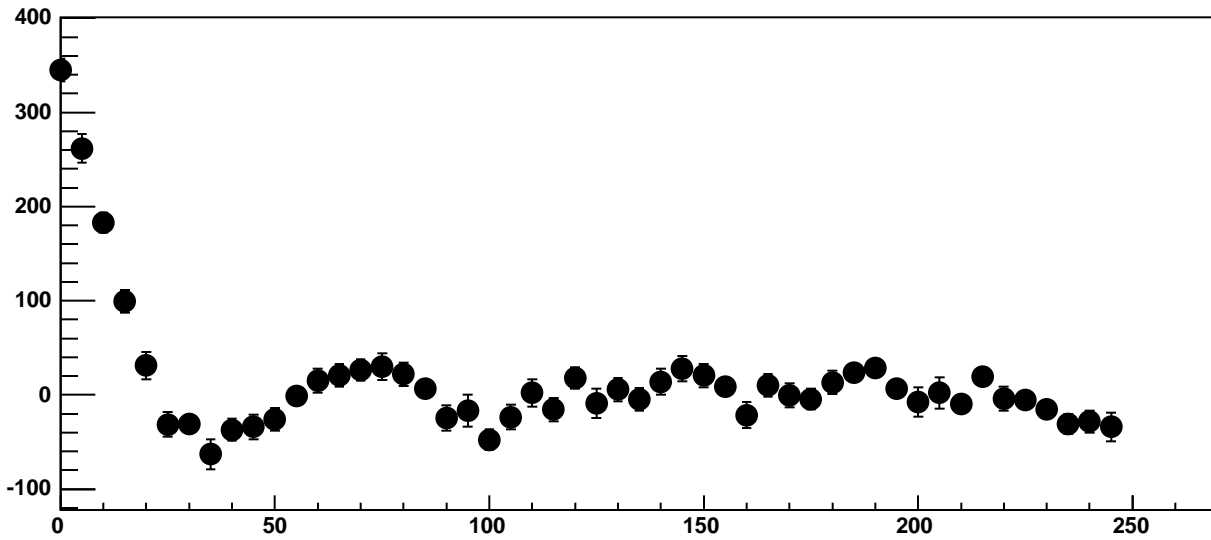


$\chi^2 / \text{ndf}$	224.7 / 41
p0	$-376.7 \pm 4.392$
p1	$98.02 \pm 0.7376$
p2	$-2e+08 \pm 1.557e+07$
p3	$1.903e+07 \pm 1.431e+06$
p4	$10.12 \pm 0.1267$

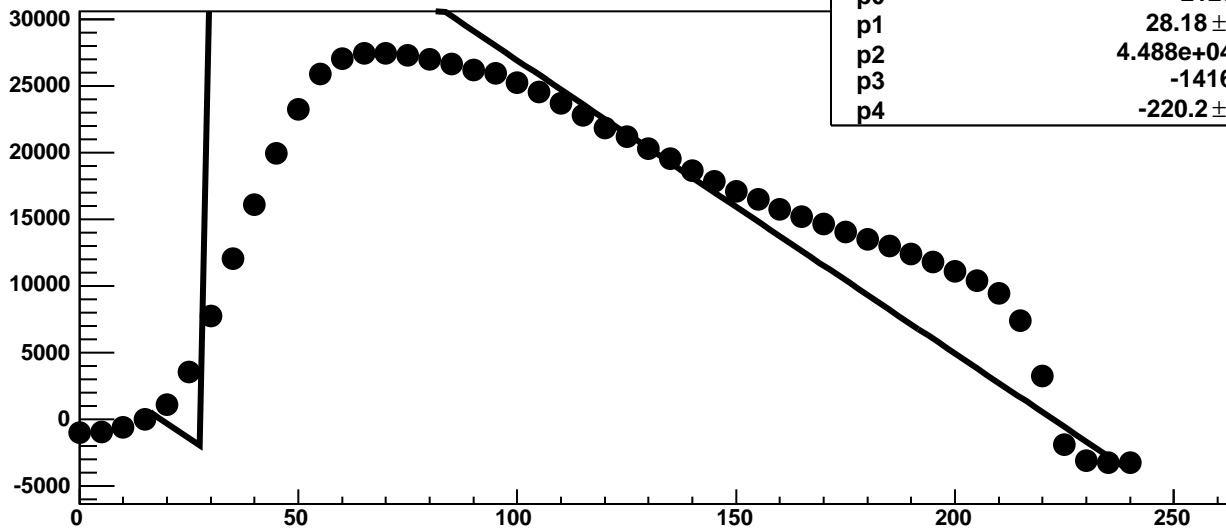
Chip 4, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

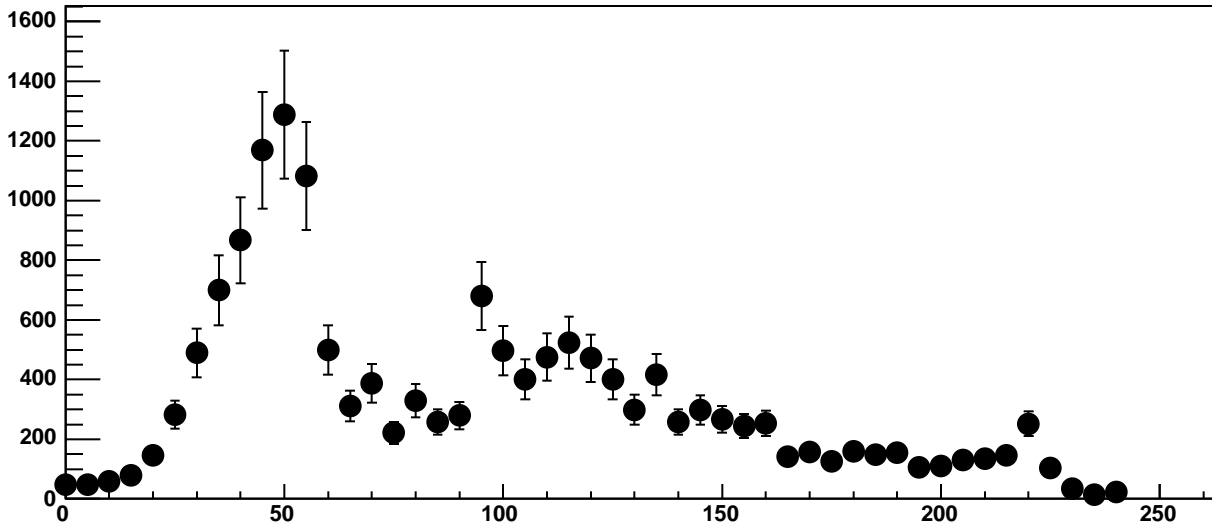


Chip 4, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold

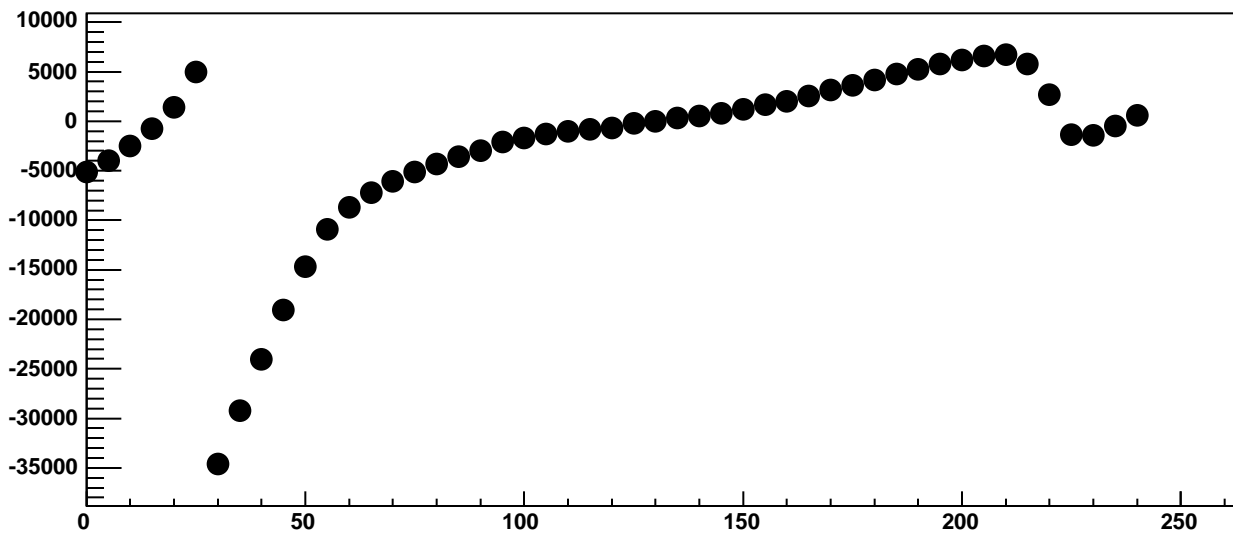


$\chi^2 / \text{ndf}$	6.021e+05 / 41
p0	-2120 ± 14.15
p1	28.18 ± 0.03087
p2	4.488e+04 ± 14.96
p3	-1416 ± 2.064
p4	-220.2 ± 0.07249

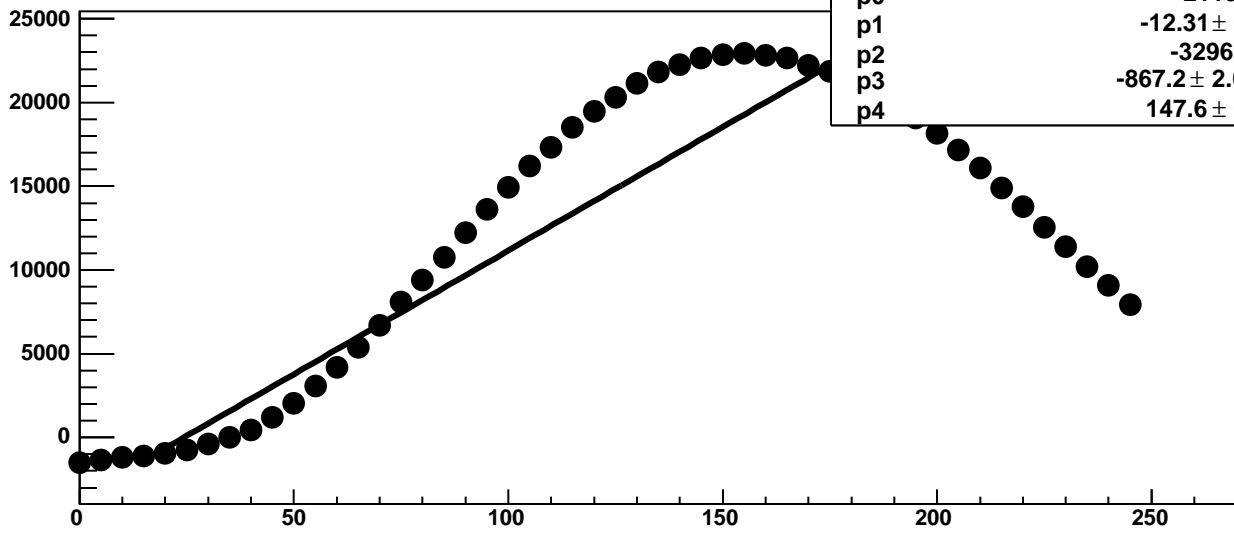
Chip 4, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 4, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold

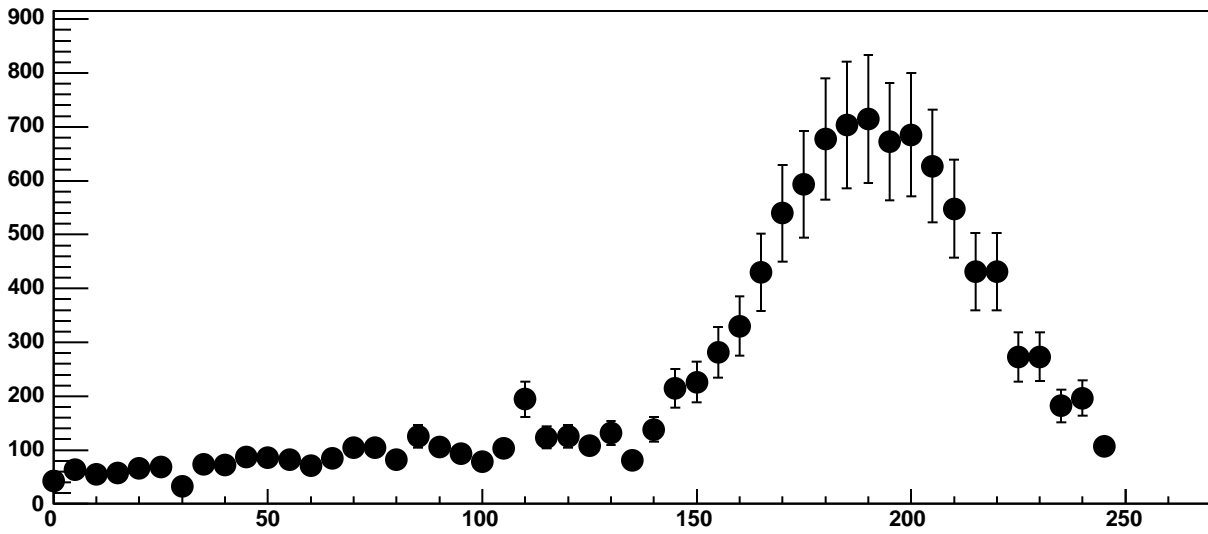


Chip 5, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold

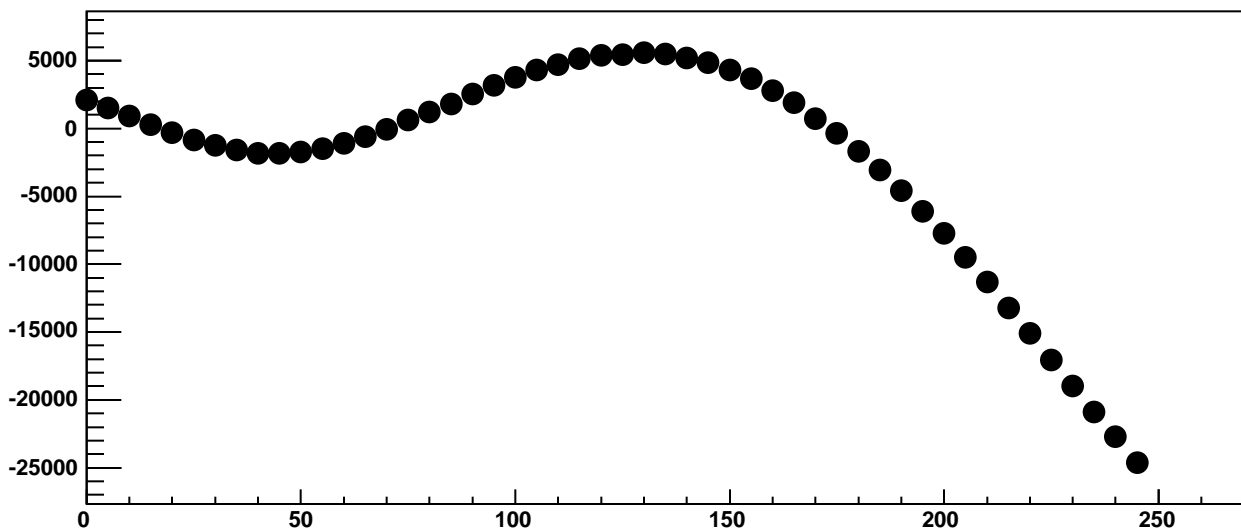


$\chi^2 / \text{ndf}$	1.223e+06 / 41
p0	-2115 ± 3.691
p1	-12.31 ± 0.04539
p2	-3296 ± 3.004
p3	-867.2 ± 2.033e-05
p4	147.6 ± 0.07485

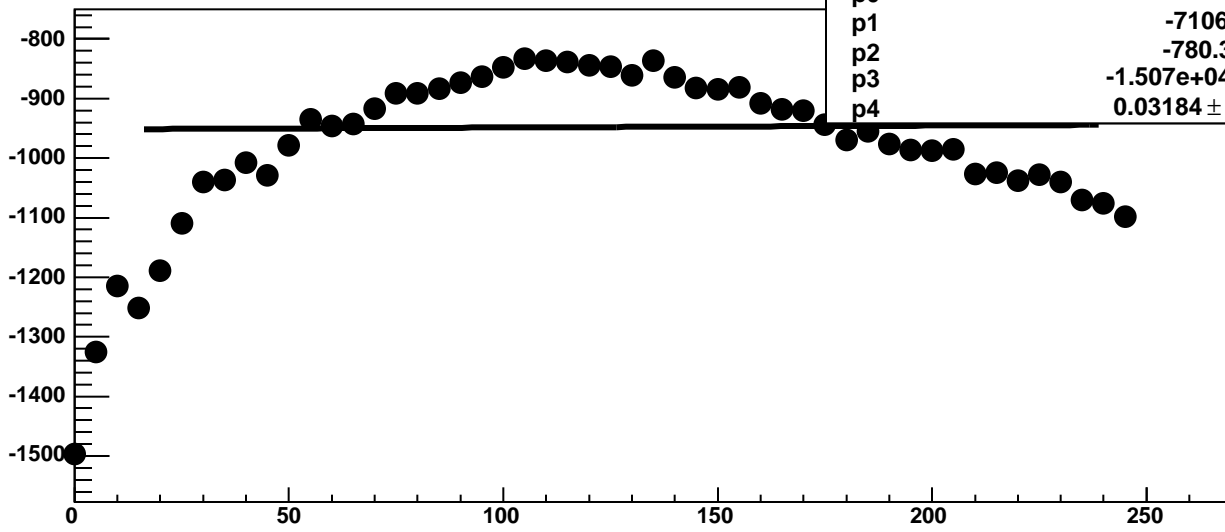
Chip 5, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold



Chip 5, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

3528 / 41

p0  $-397.8 \pm 61.14$

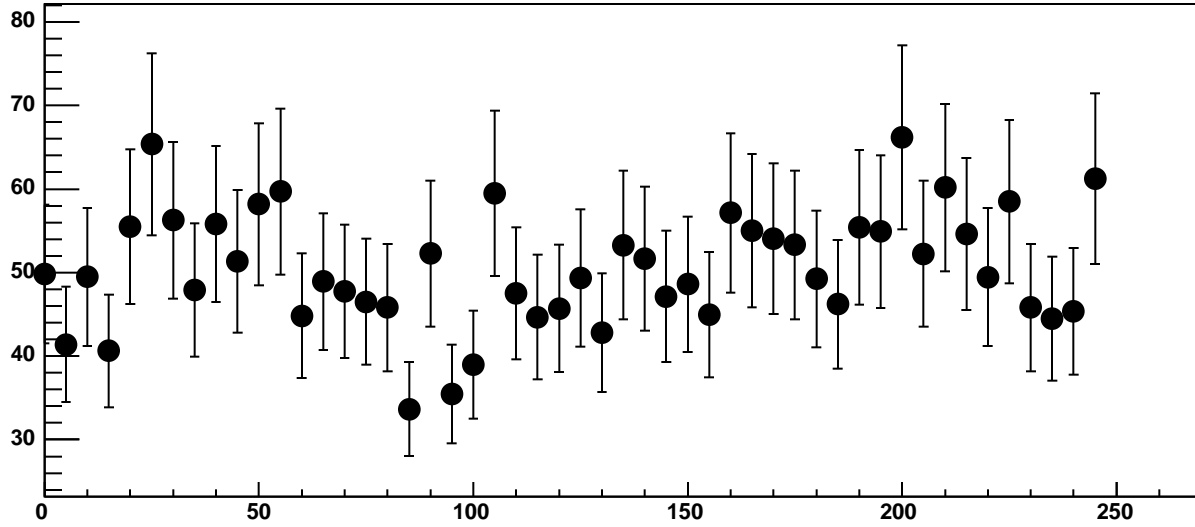
p1  $-7106 \pm 210.7$

p2  $-780.3 \pm 131.1$

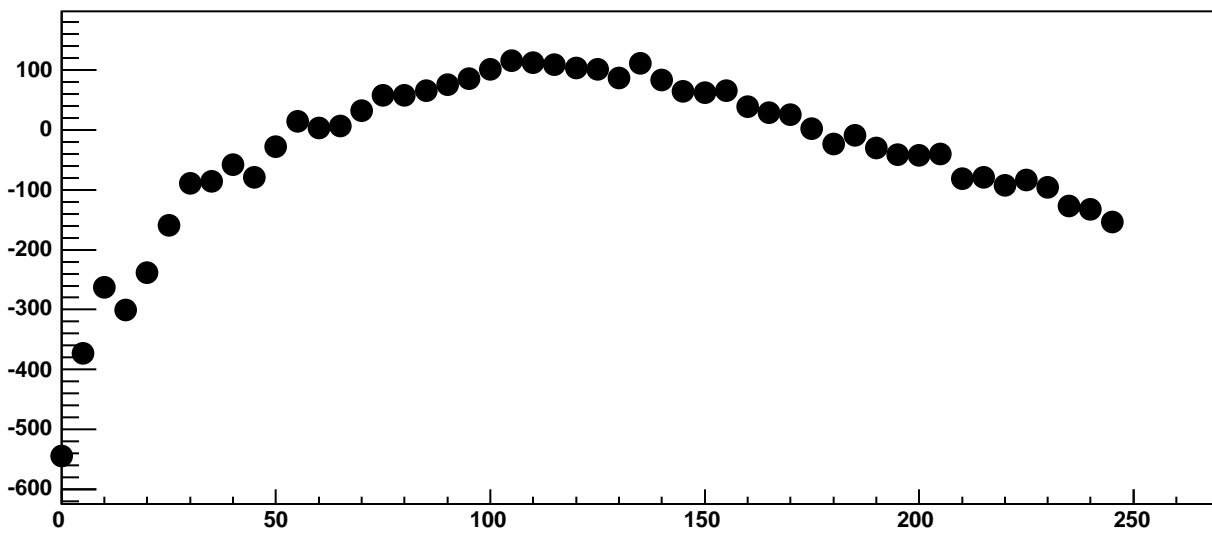
p3  $-1.507\text{e}+04 \pm 1921$

p4  $0.03184 \pm 0.02566$

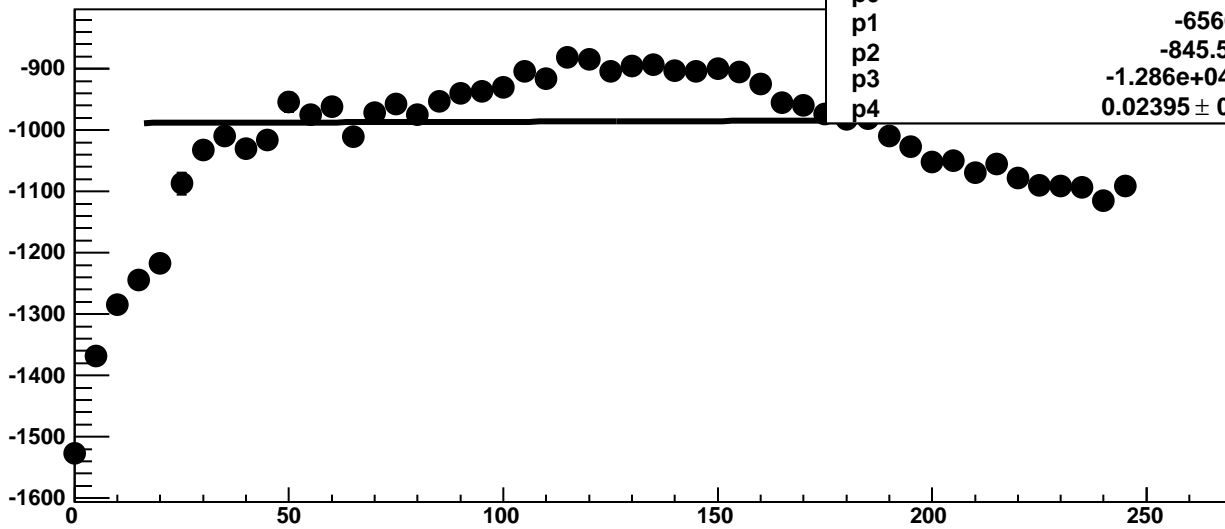
Chip 5, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



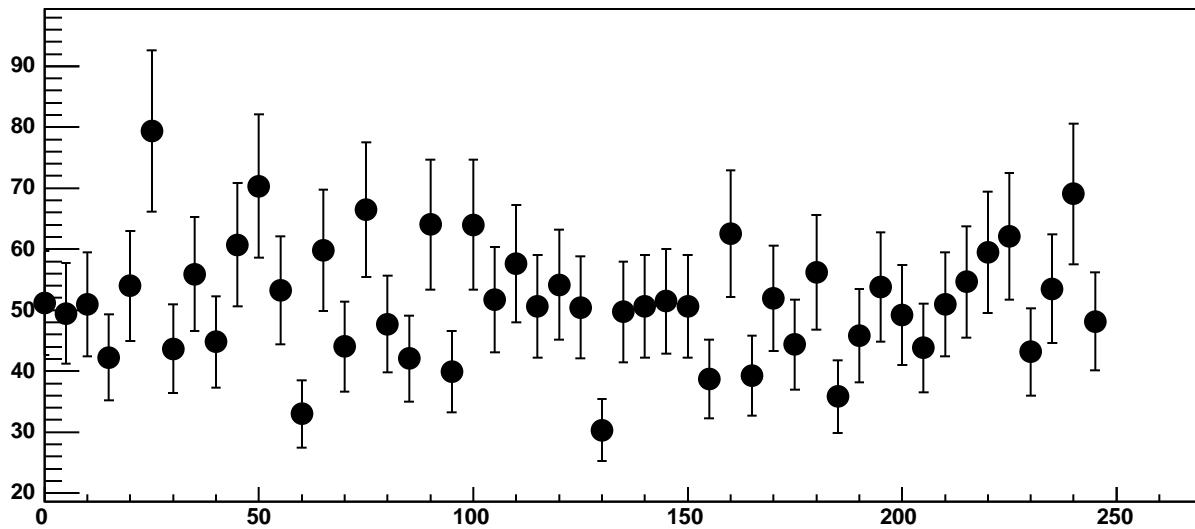
Chip 5, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



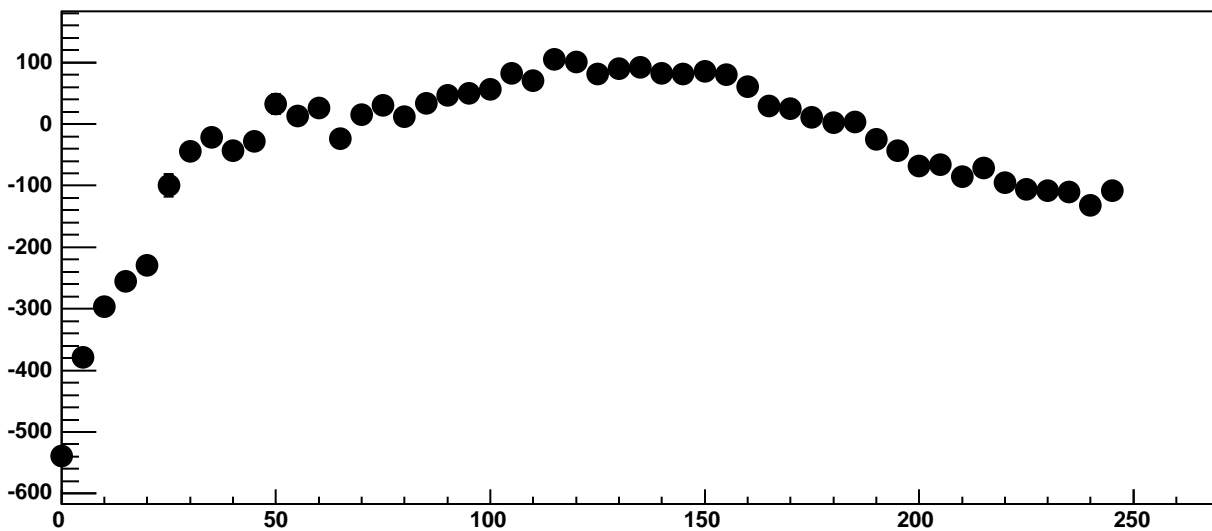
Chip 5, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold



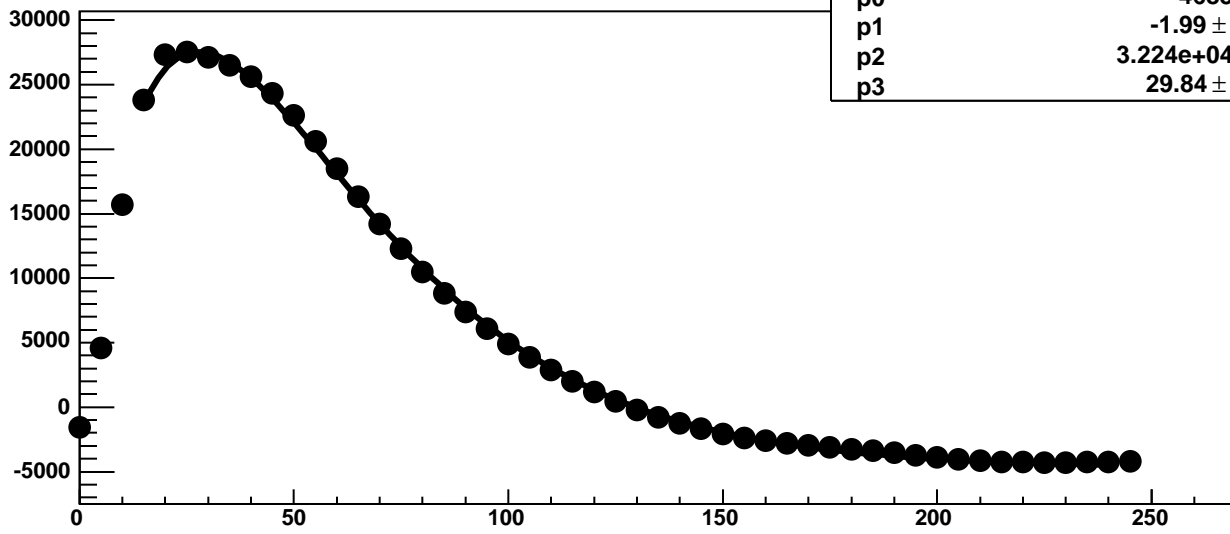
Chip 5, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



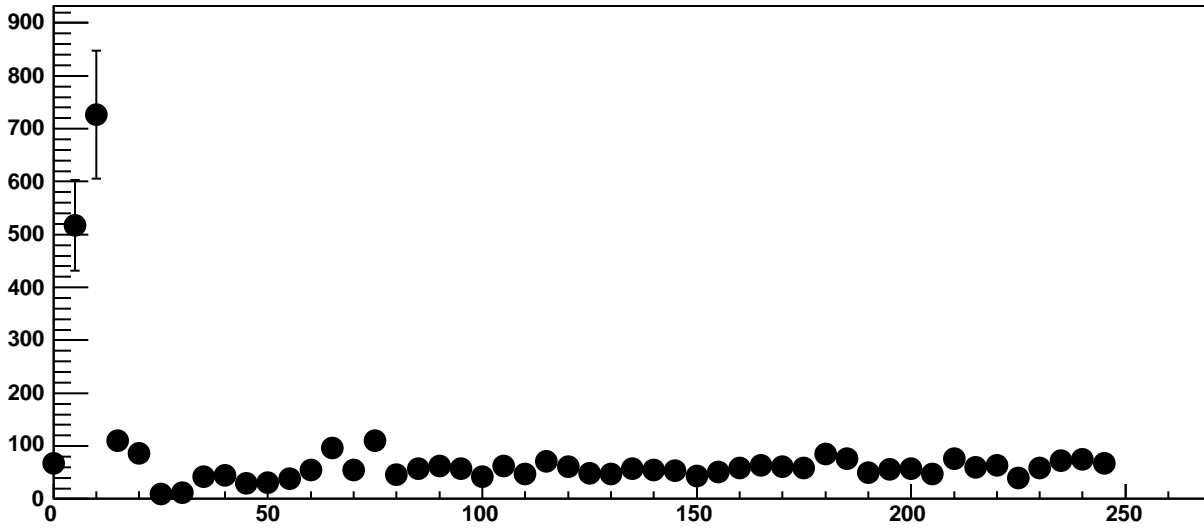
Chip 5, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



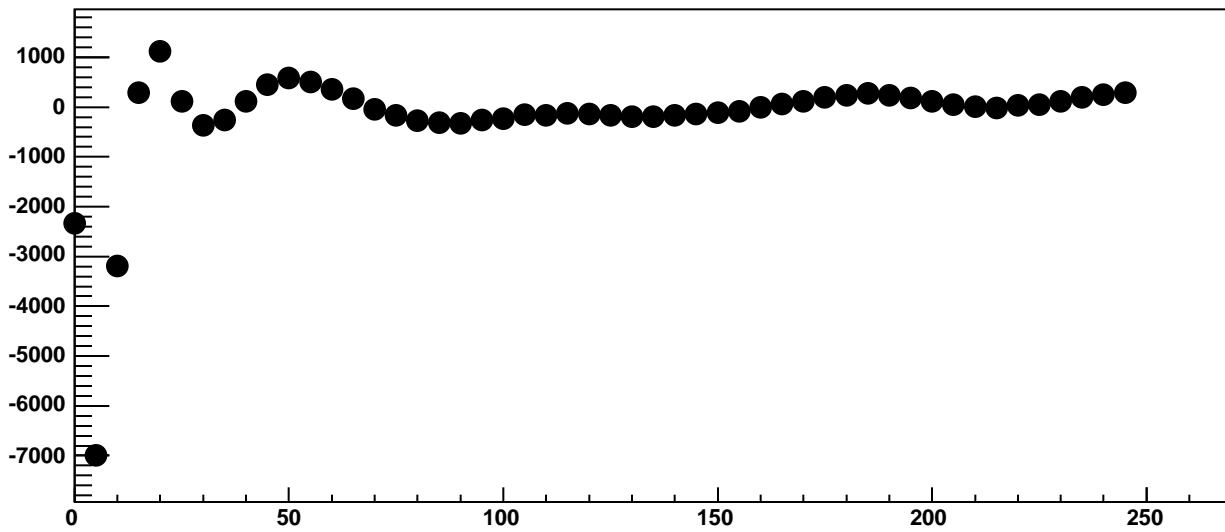
Chip 5, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold



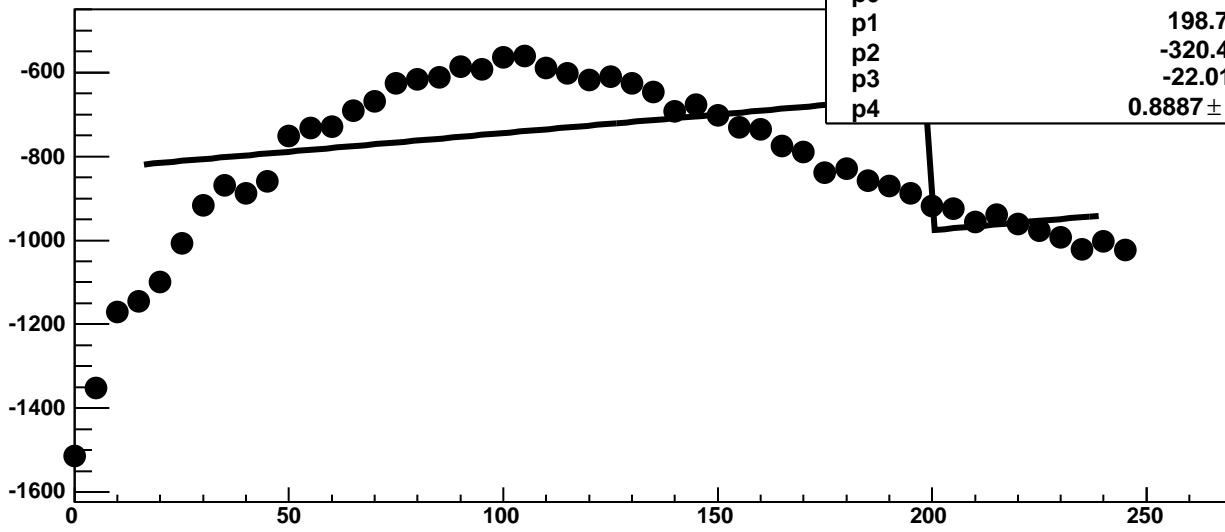
Chip 5, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



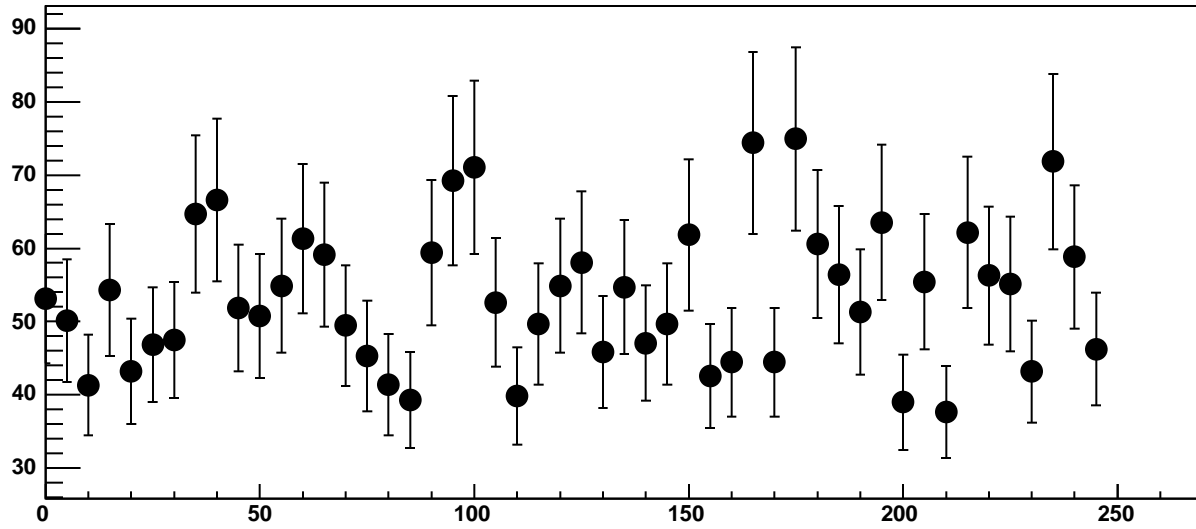
Chip 5, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold



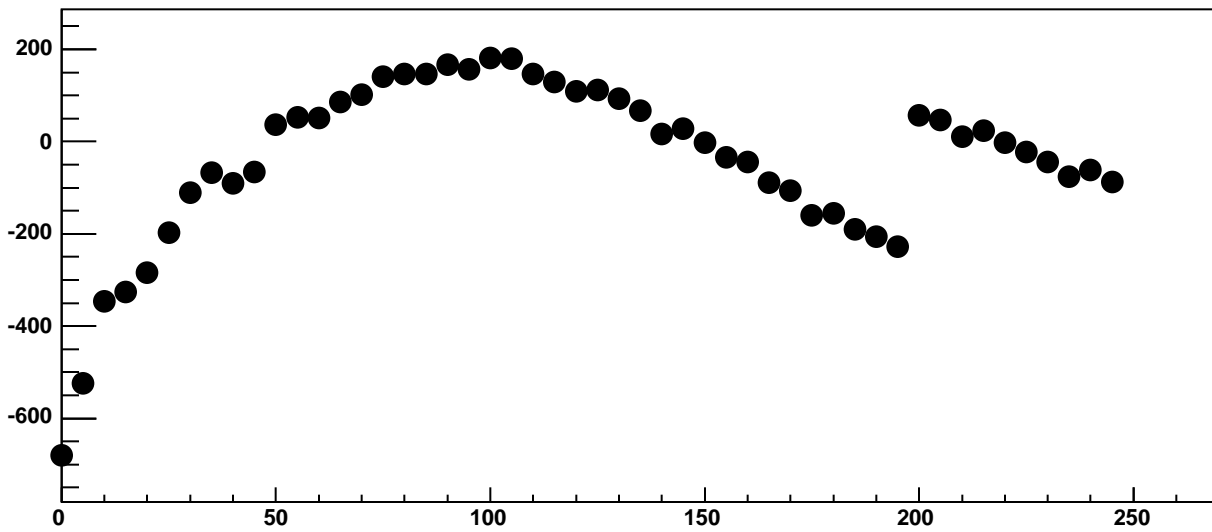
Chip 5, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold



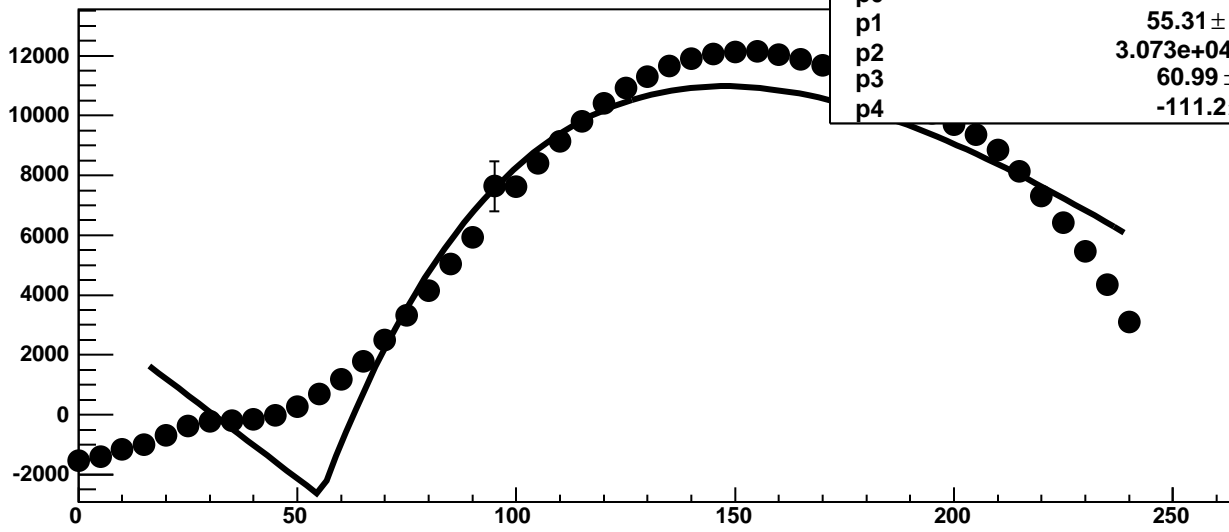
Chip 5, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

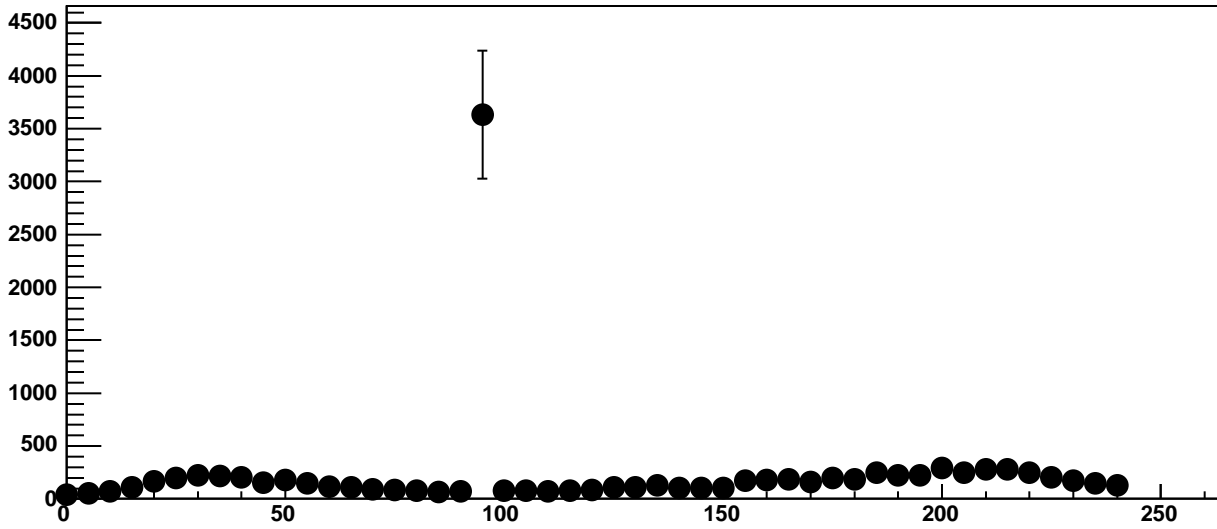


Chip 5, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

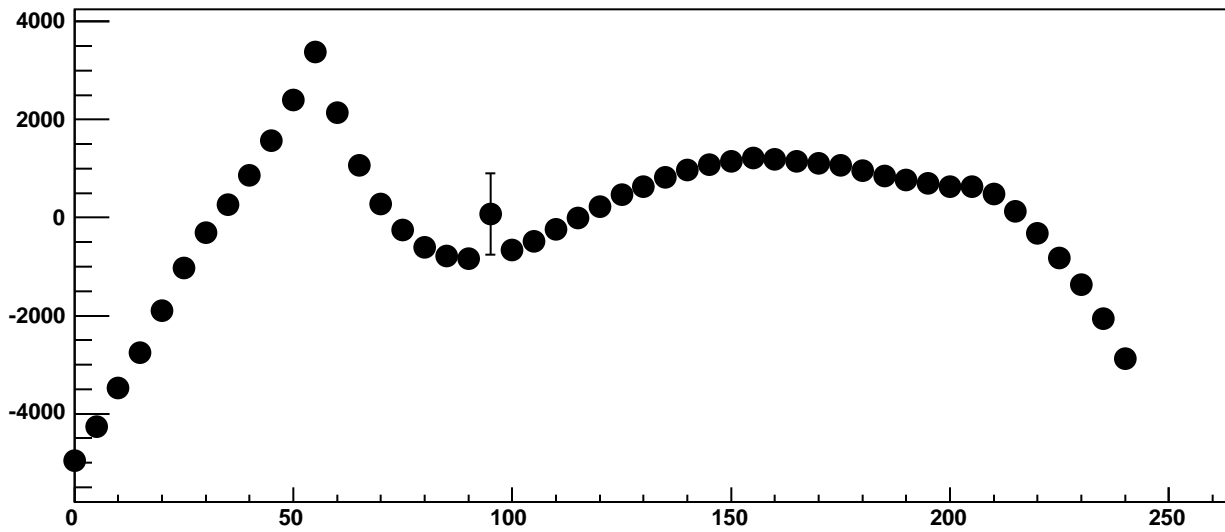


$\chi^2 / \text{ndf}$	7.397e+04 / 41
p0	-2722 ± 12.61
p1	55.31 ± 0.04904
p2	3.073e+04 ± 106.3
p3	60.99 ± 0.1936
p4	-111.2 ± 0.4671

Chip 5, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

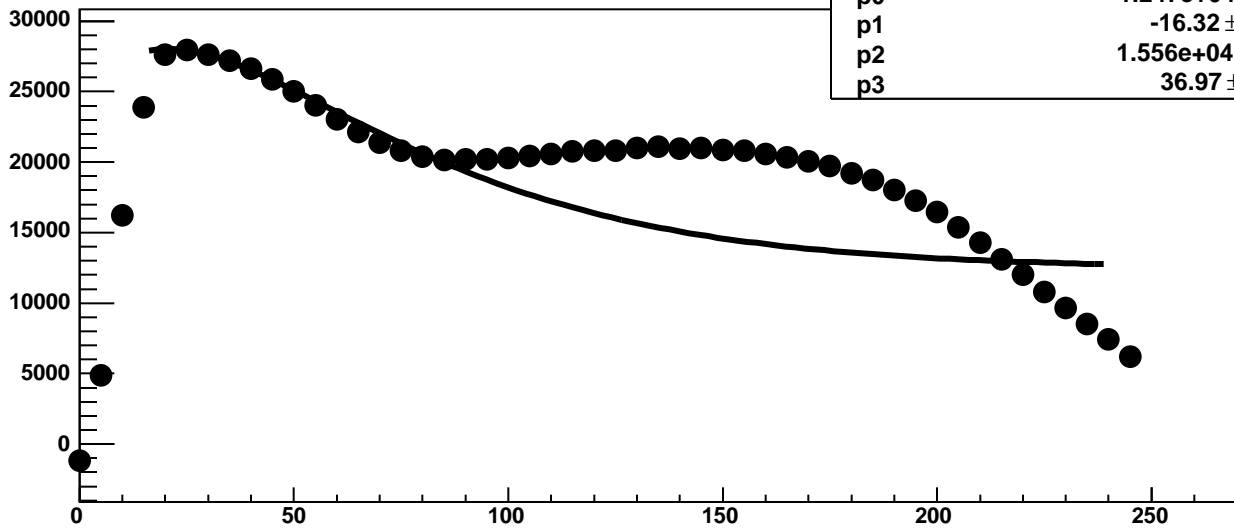


Chip 5, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold



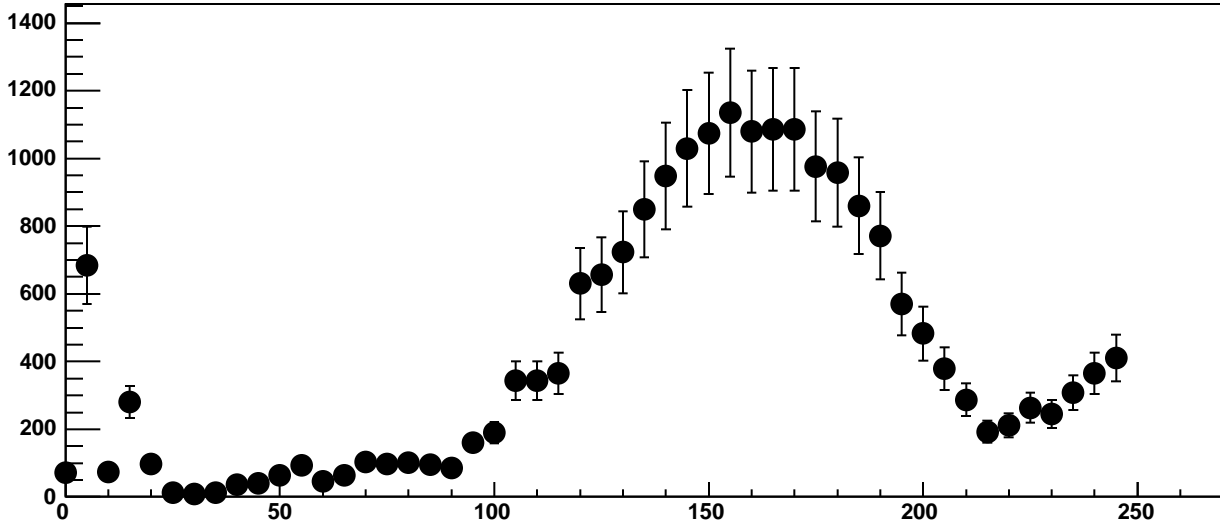


Chip 5, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold

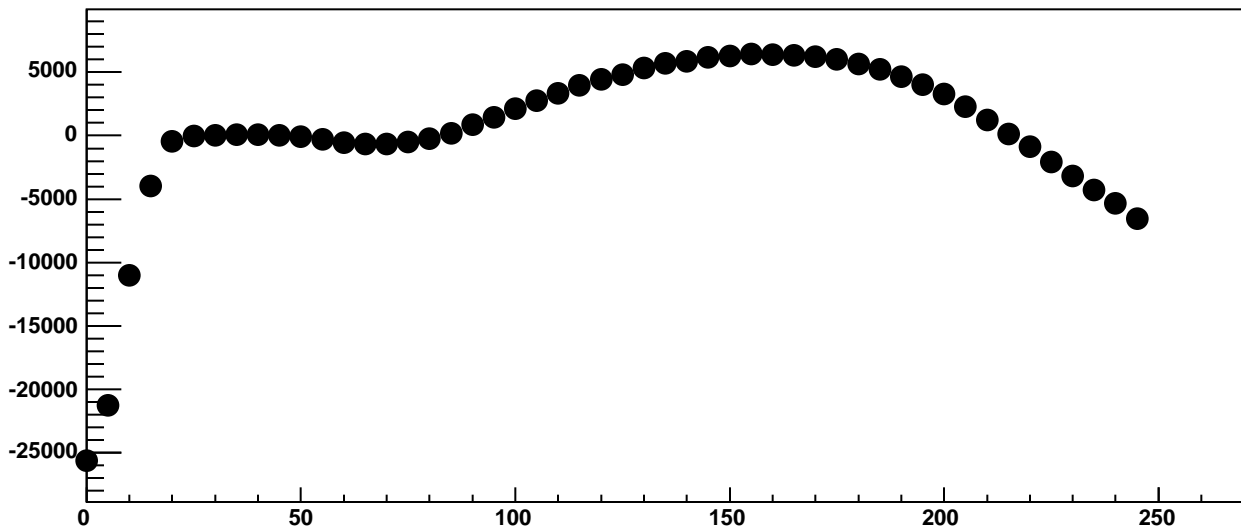


$\chi^2 / \text{ndf}$	4.865e+04 / 42
p0	1.247e+04 $\pm$ 25.41
p1	-16.32 $\pm$ 0.1745
p2	1.556e+04 $\pm$ 27.69
p3	36.97 $\pm$ 0.1003

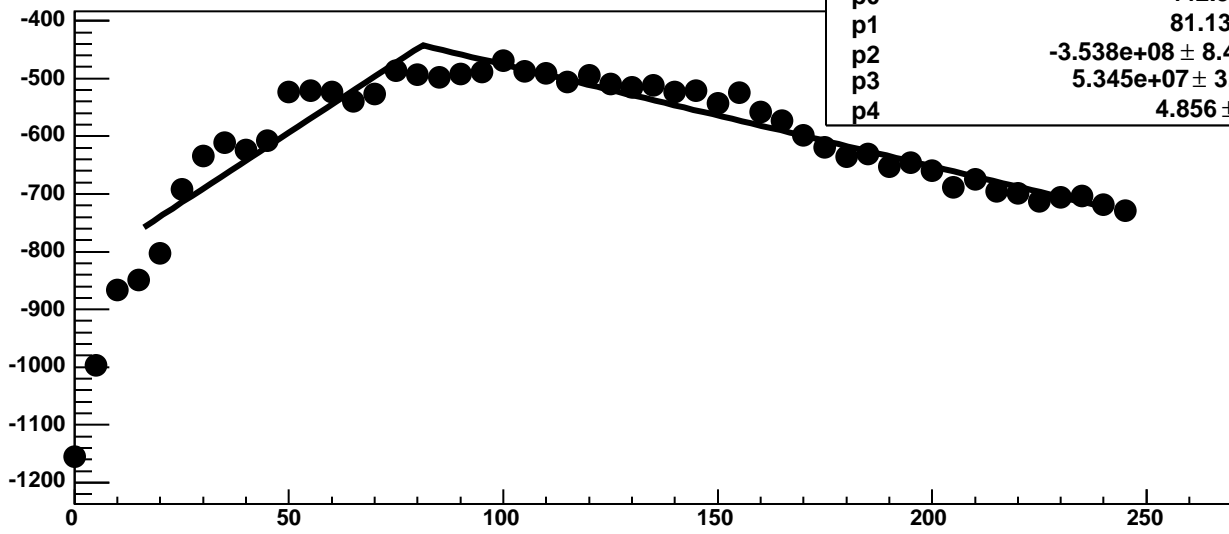
Chip 5, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



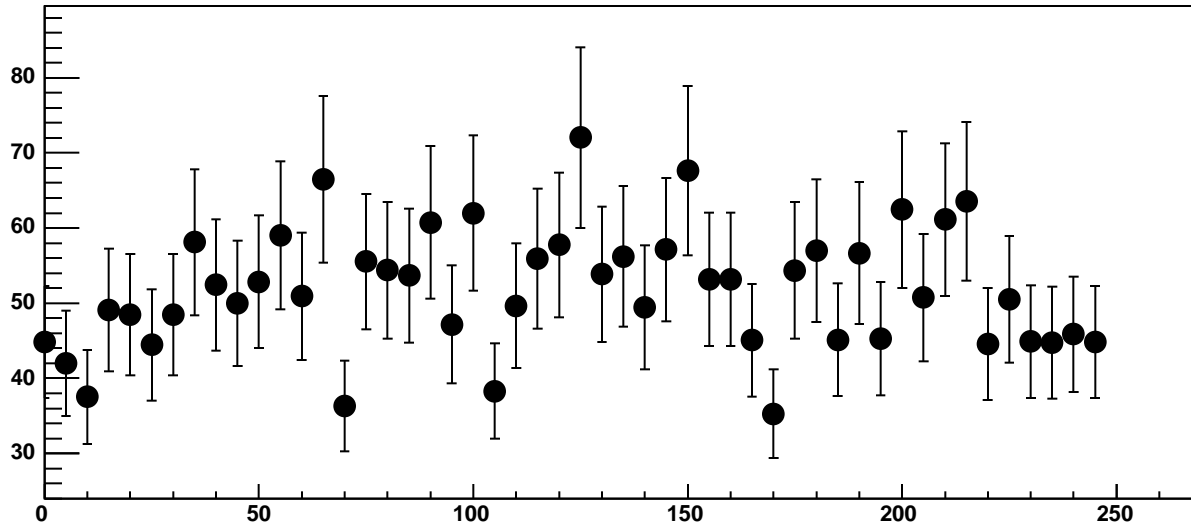
Chip 5, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold



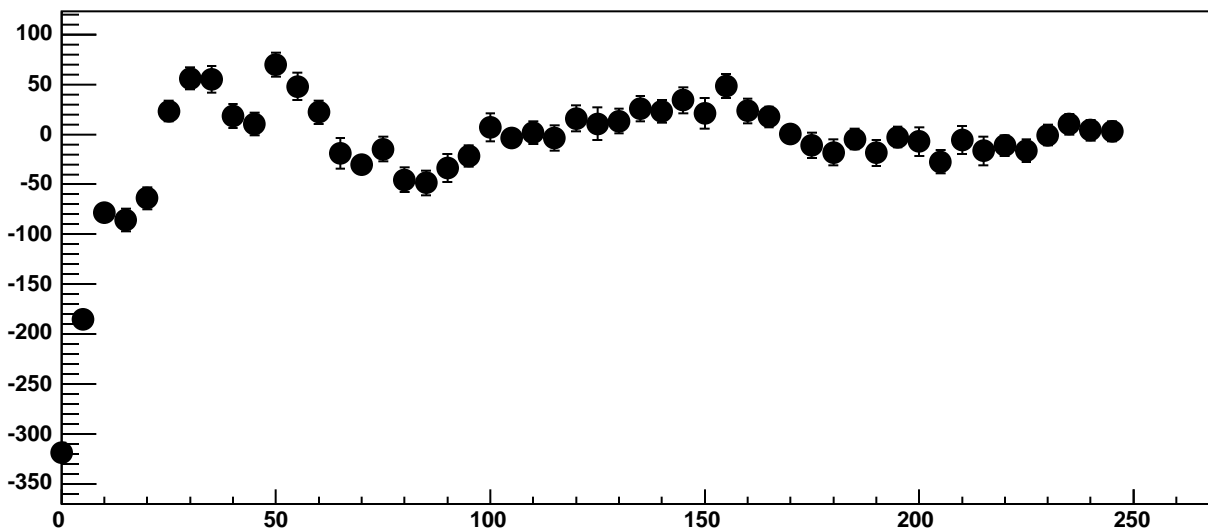
Chip 5, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold



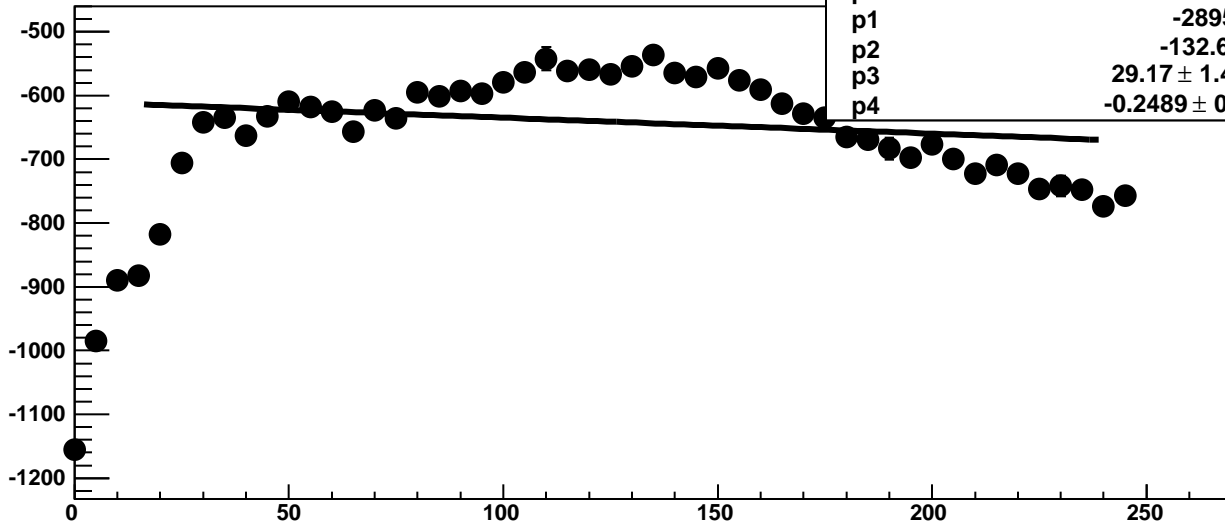
Chip 5, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

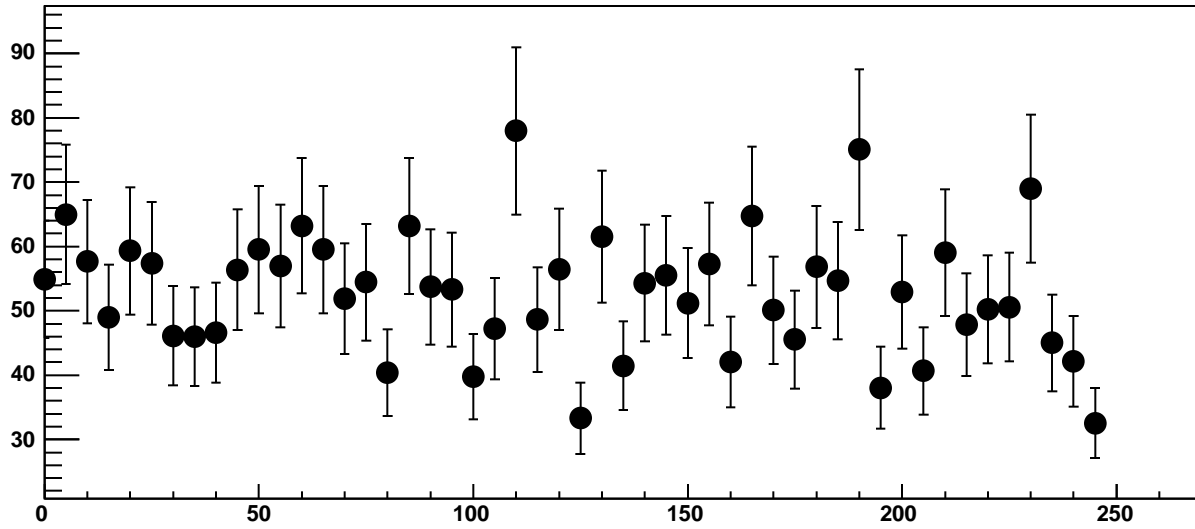


Chip 5, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

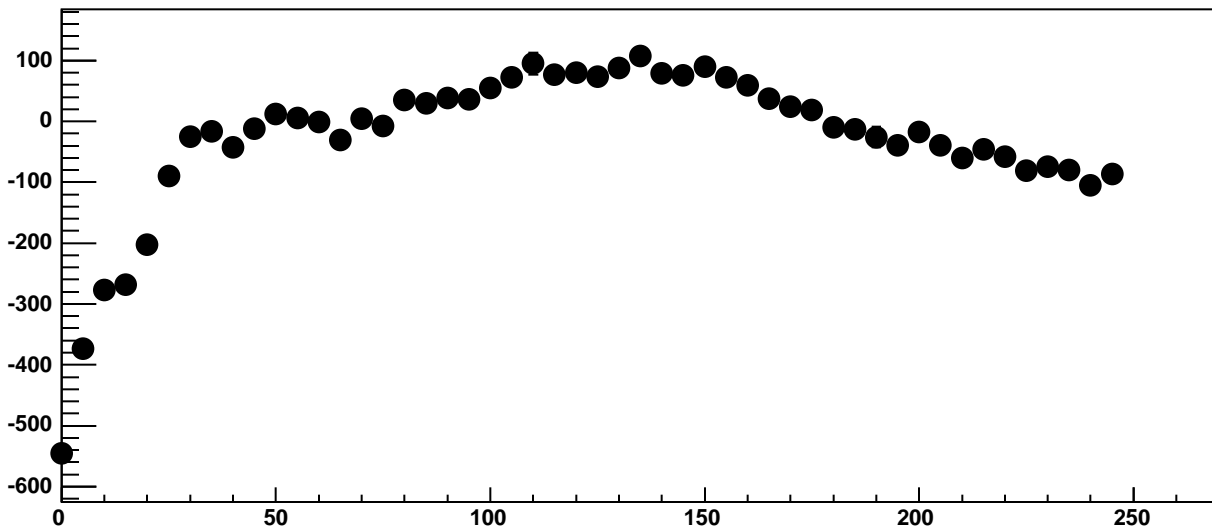


$\chi^2 / \text{ndf}$	1931 / 41
p0	$243.2 \pm 23.24$
p1	$-2895 \pm 92.7$
p2	$-132.6 \pm 23.24$
p3	$29.17 \pm 1.413e+05$
p4	$-0.2489 \pm 0.007339$

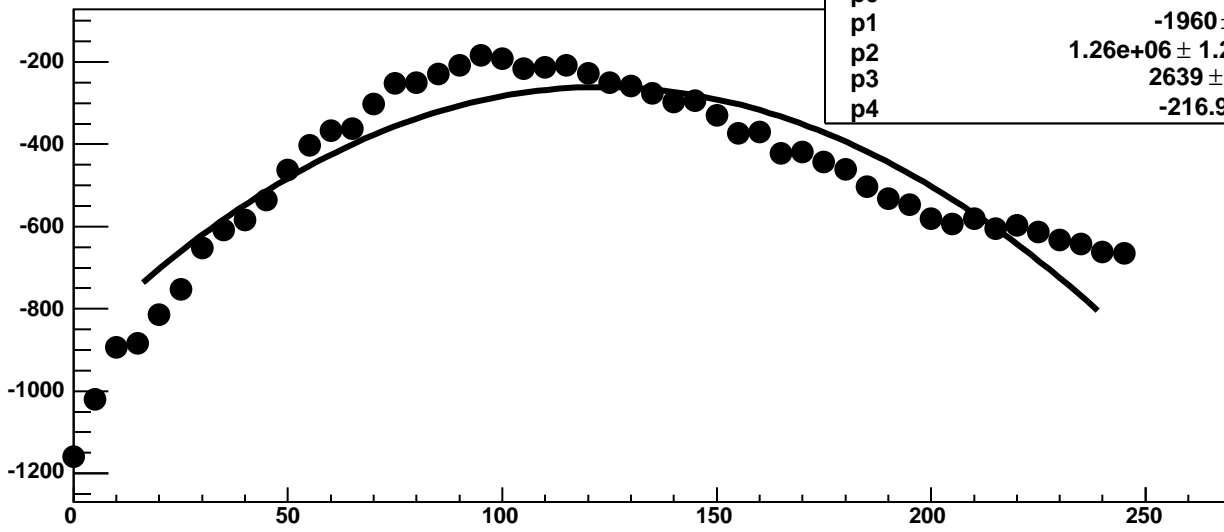
Chip 5, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



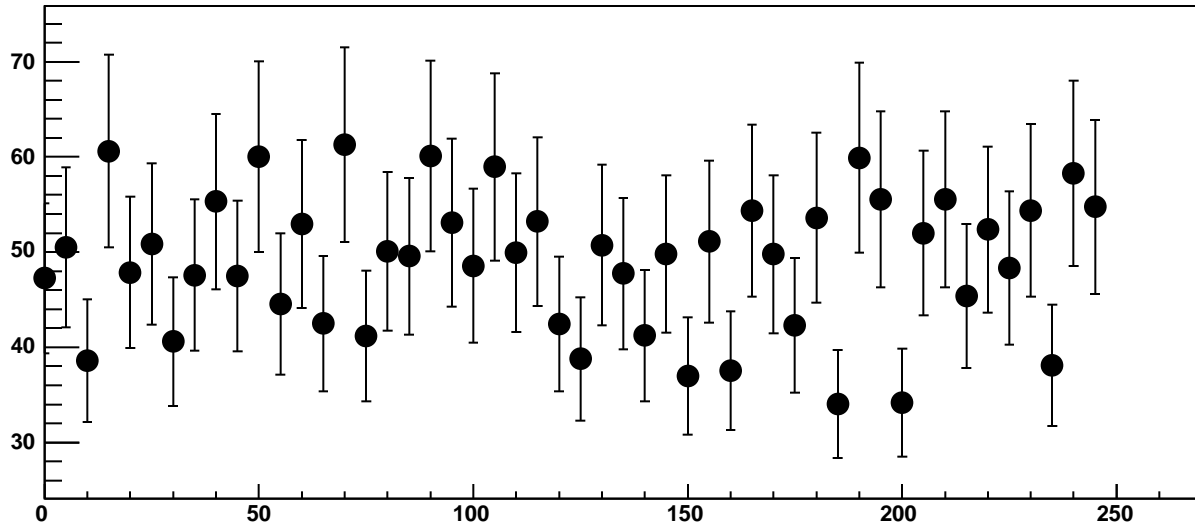
Chip 5, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold



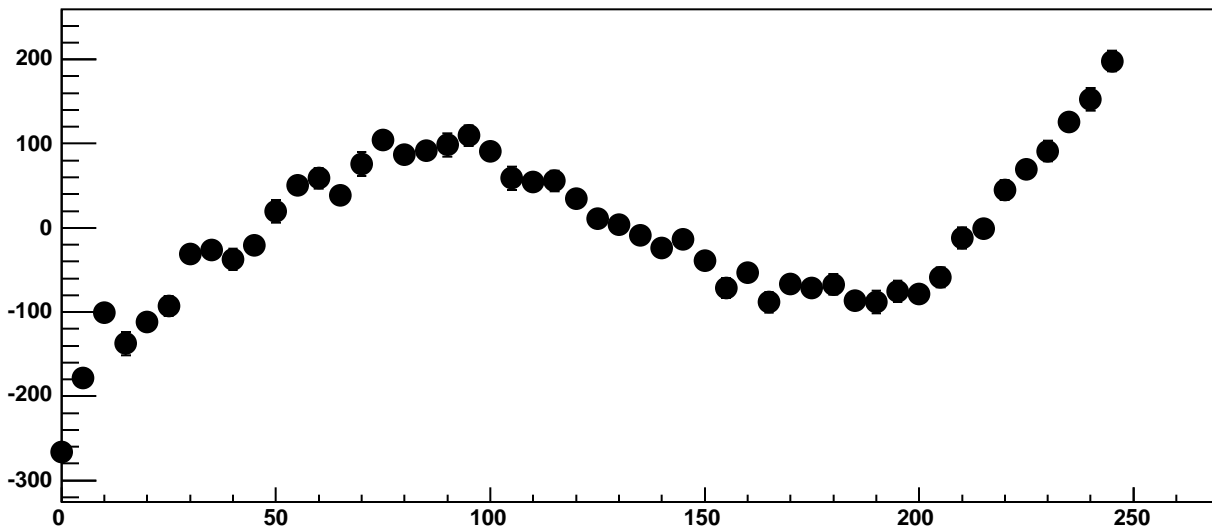
Chip 5, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold



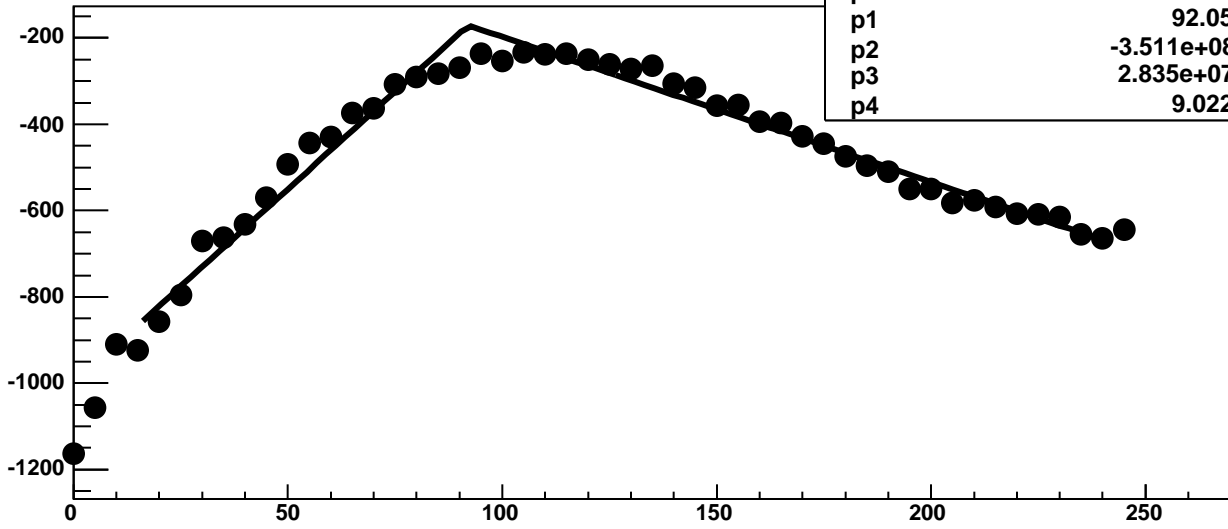
Chip 5, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold

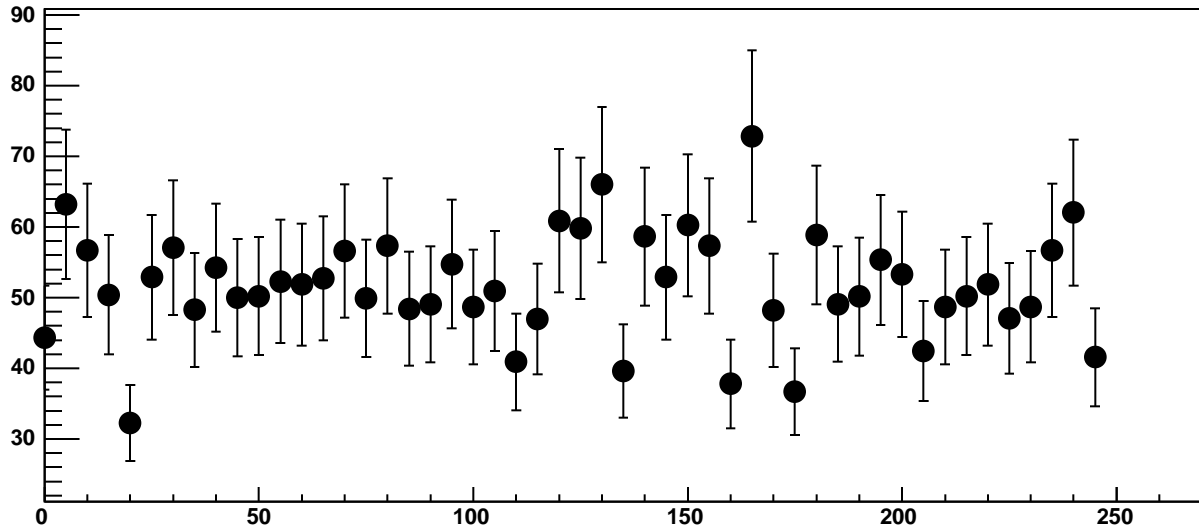


Chip 5, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

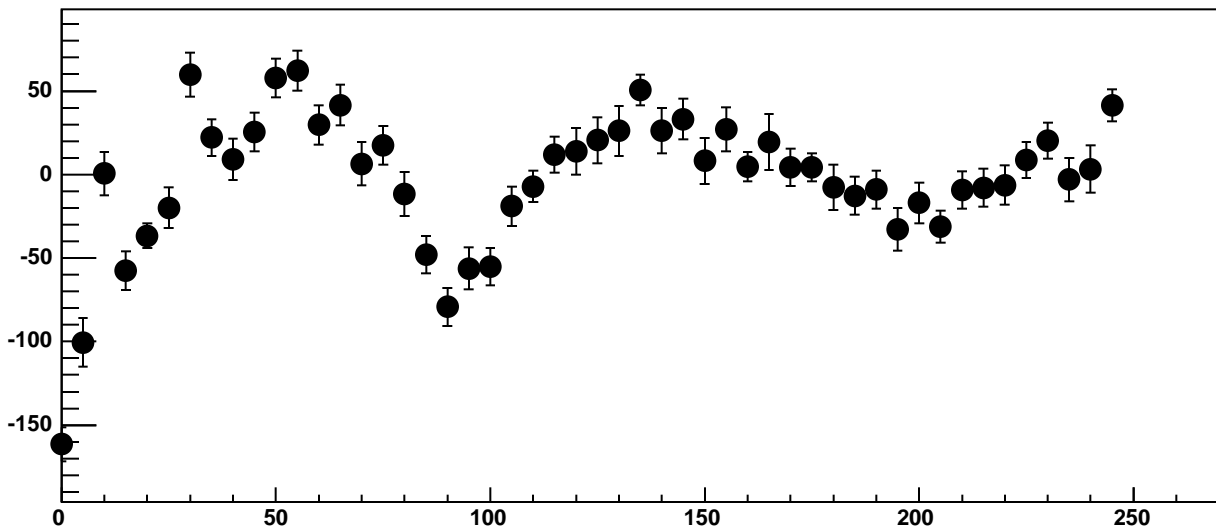


$\chi^2 / \text{ndf}$	354.7 / 41
p0	-170.7 ± nan
p1	92.05 ± nan
p2	-3.511e+08 ± nan
p3	2.835e+07 ± nan
p4	9.022 ± nan

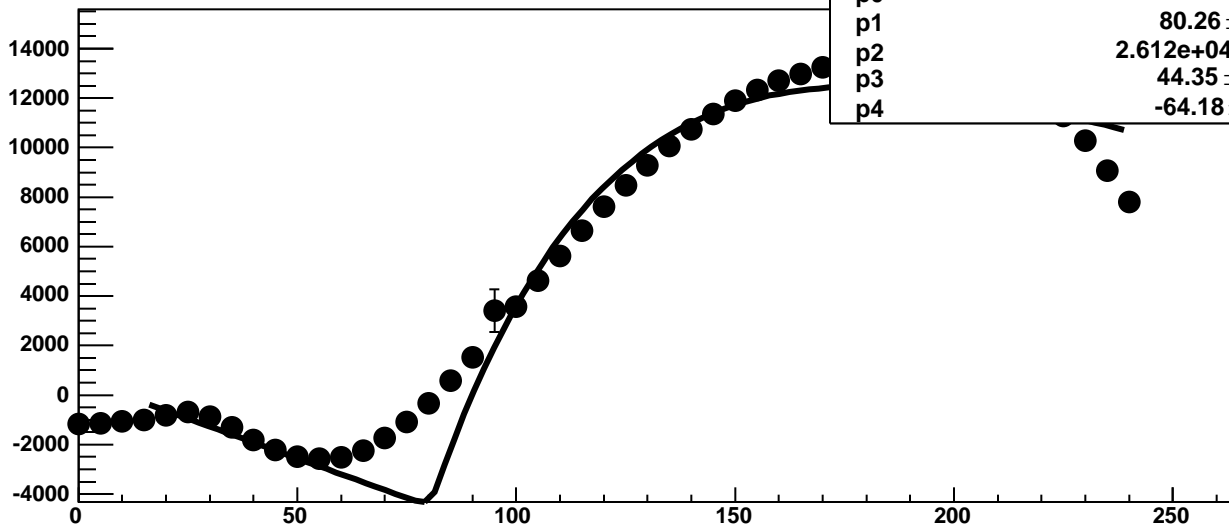
Chip 5, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

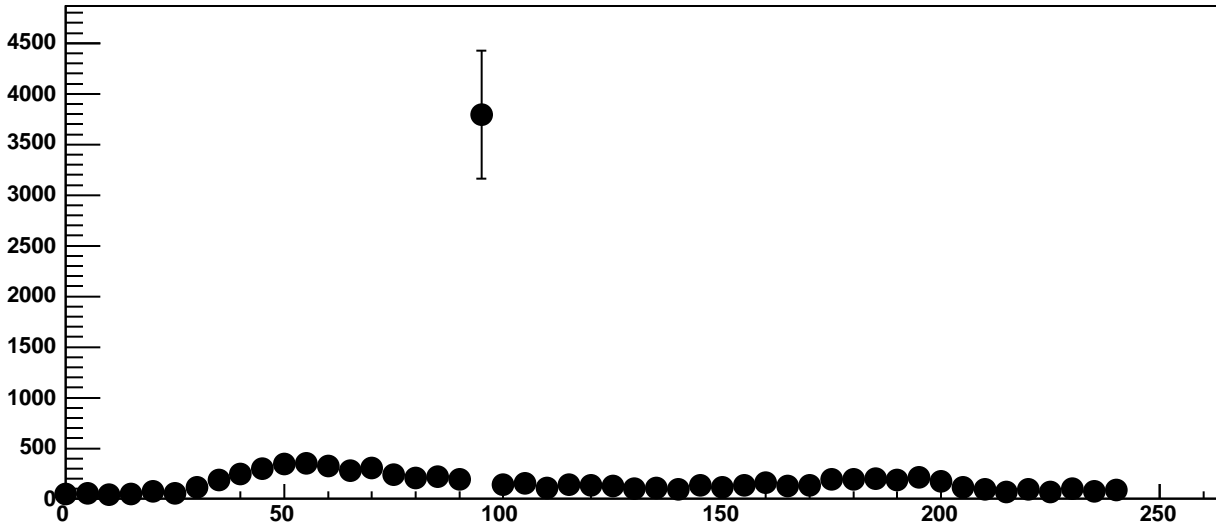


Chip 5, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

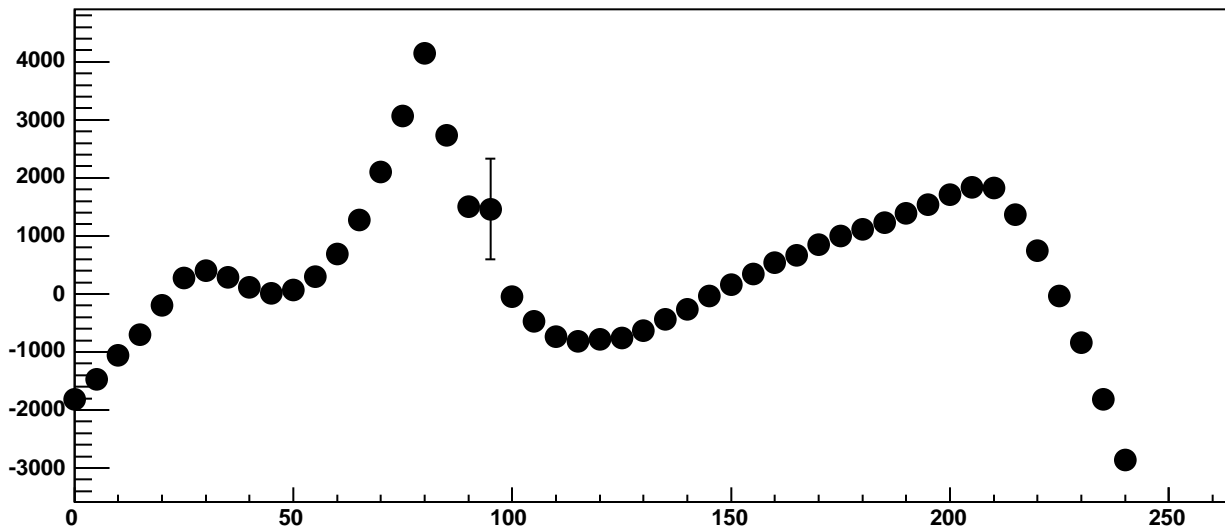


$\chi^2 / \text{ndf}$	8.605e+04 / 41
p0	-4497 ± 18.15
p1	80.26 ± 0.0708
p2	2.612e+04 ± 78.65
p3	44.35 ± 0.1416
p4	-64.18 ± 0.3441

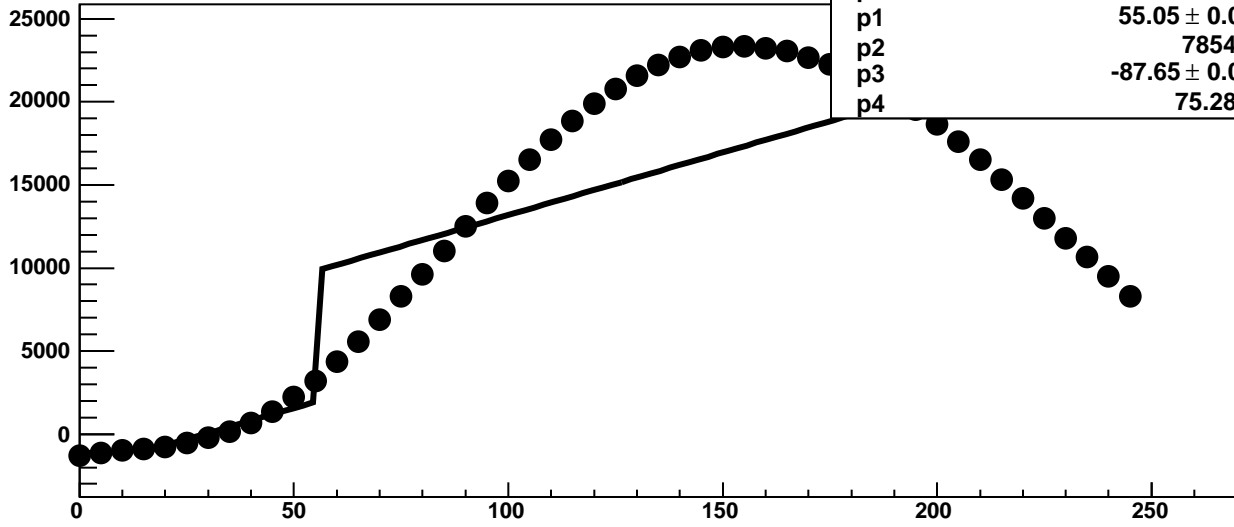
Chip 5, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

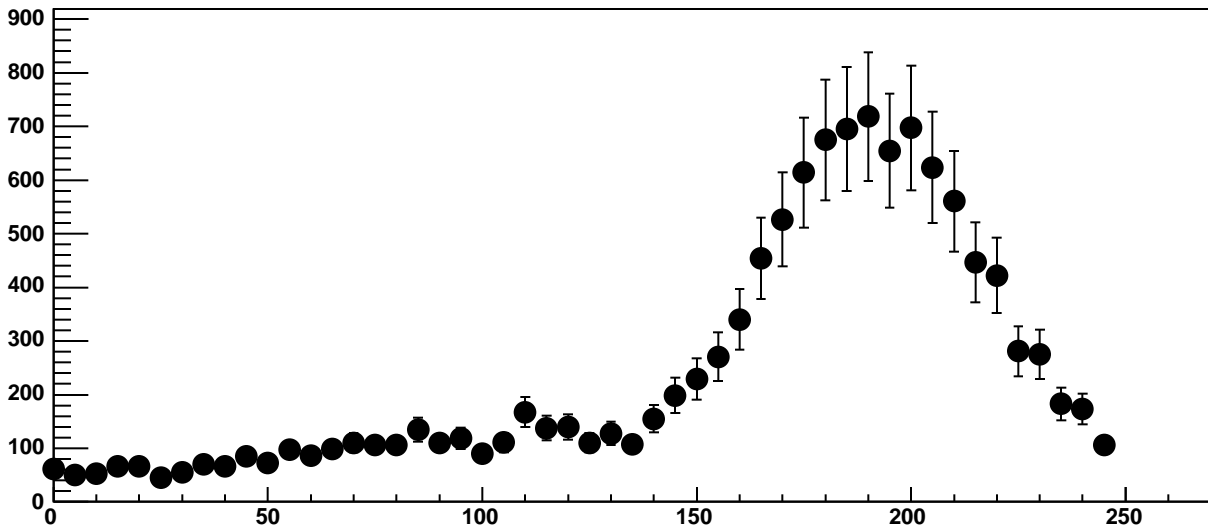


Chip 5, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold

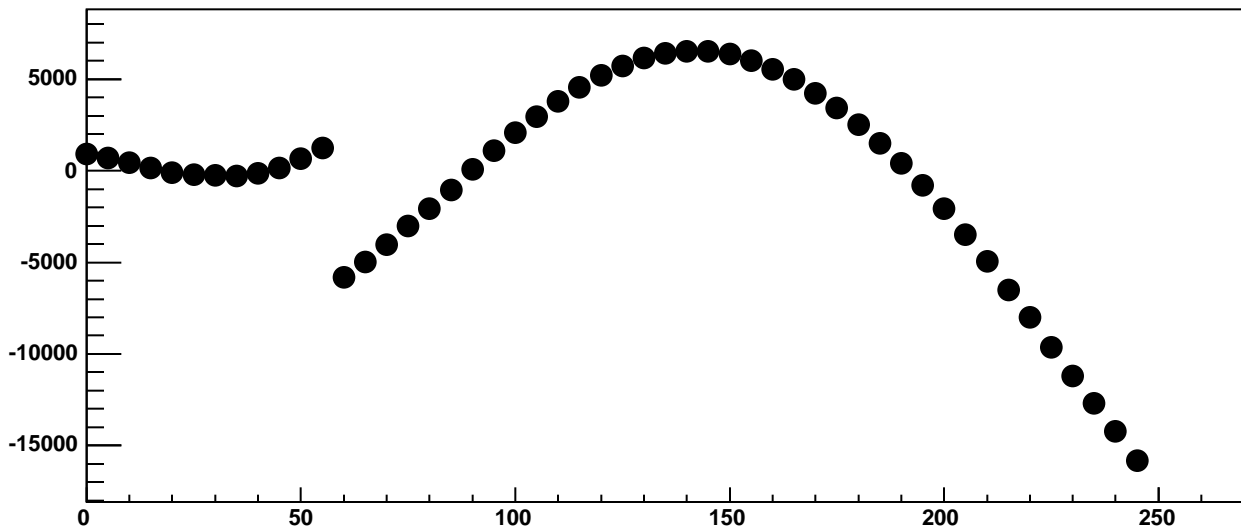


$\chi^2 / \text{ndf}$	8.052e+05 / 41
p0	1953 $\pm$ 6.342
p1	55.05 $\pm$ 0.0002006
p2	7854 $\pm$ 13.51
p3	-87.65 $\pm$ 0.0002804
p4	75.28 $\pm$ 0.115

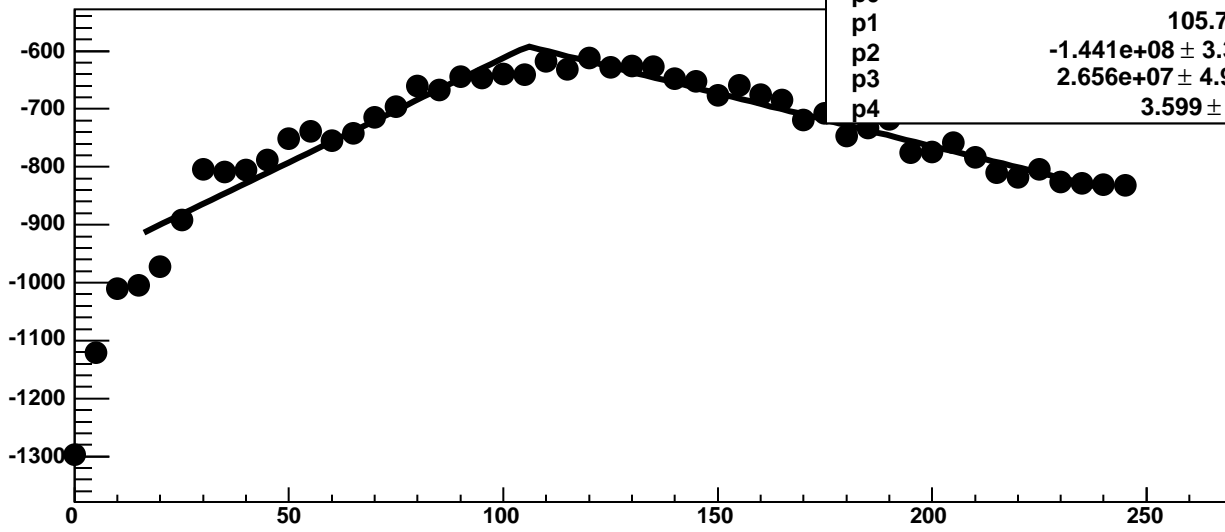
Chip 5, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

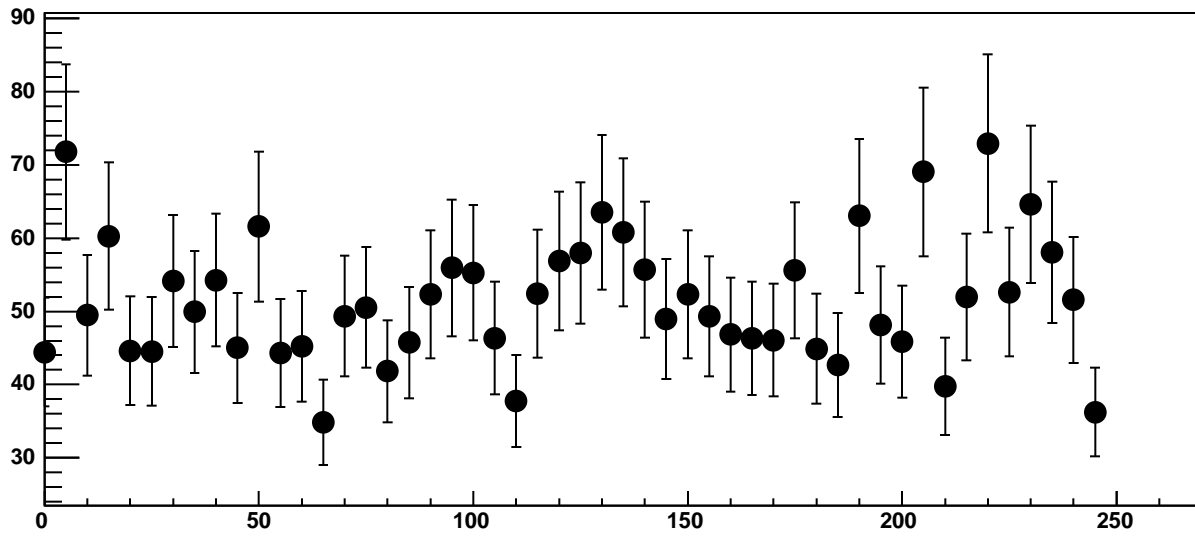


Chip 5, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

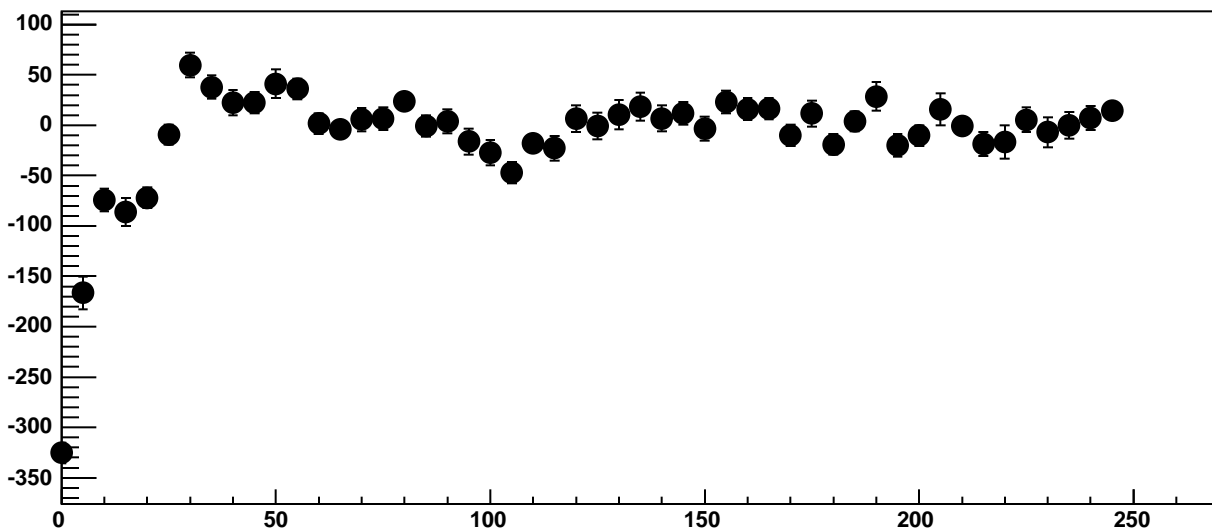


$\chi^2 / \text{ndf}$	224.5 / 41
p0	$-591.9 \pm 3.494$
p1	$105.7 \pm 1.254$
p2	$-1.441\text{e}+08 \pm 3.391\text{e}+06$
p3	$2.656\text{e}+07 \pm 4.906\text{e}+05$
p4	$3.599 \pm 0.09652$

Chip 5, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

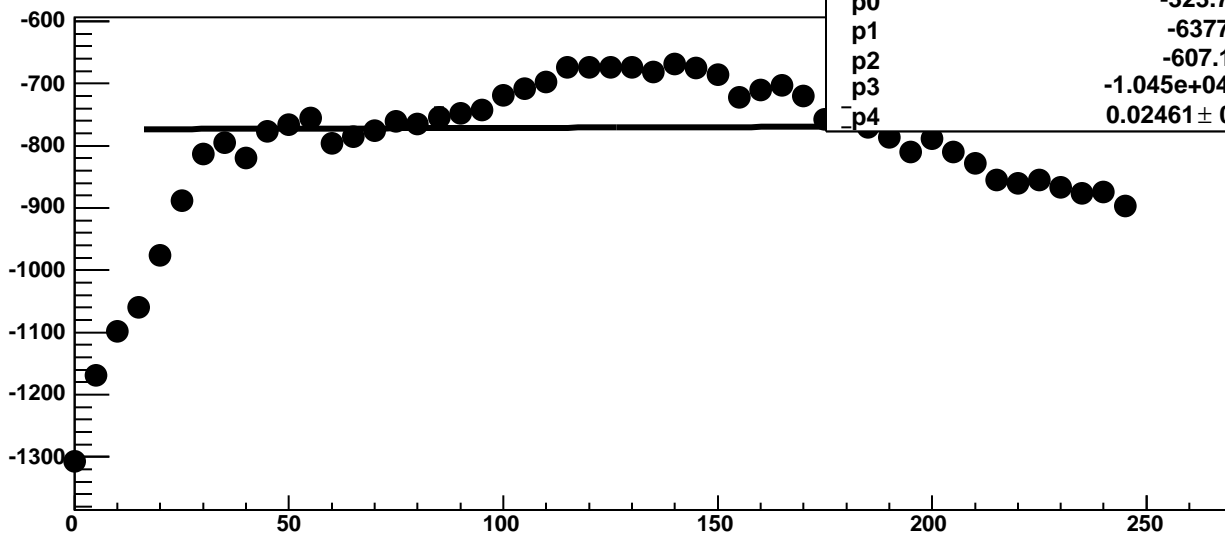


Chip 5, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



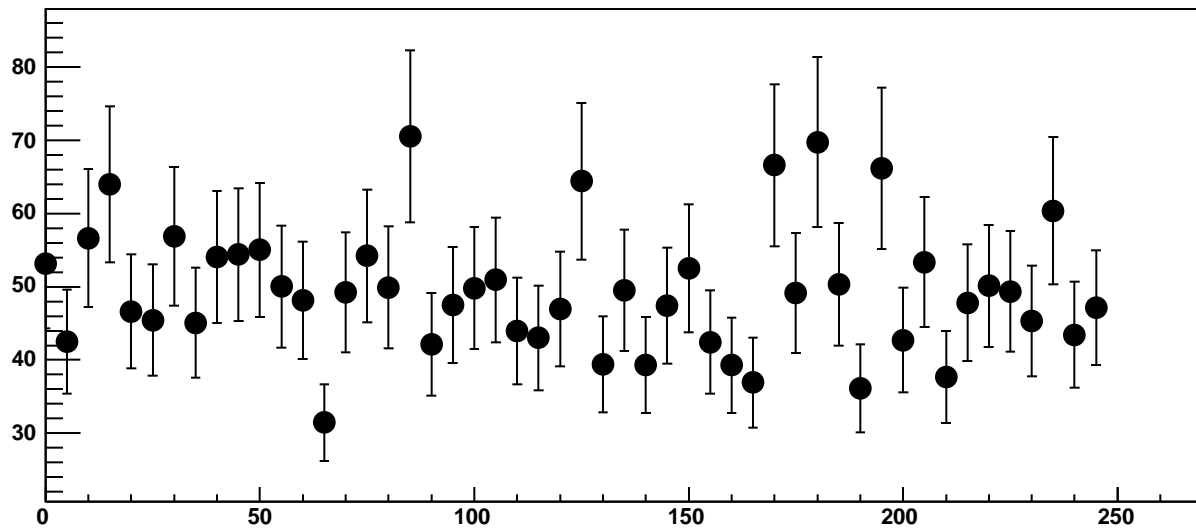


Chip 5, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

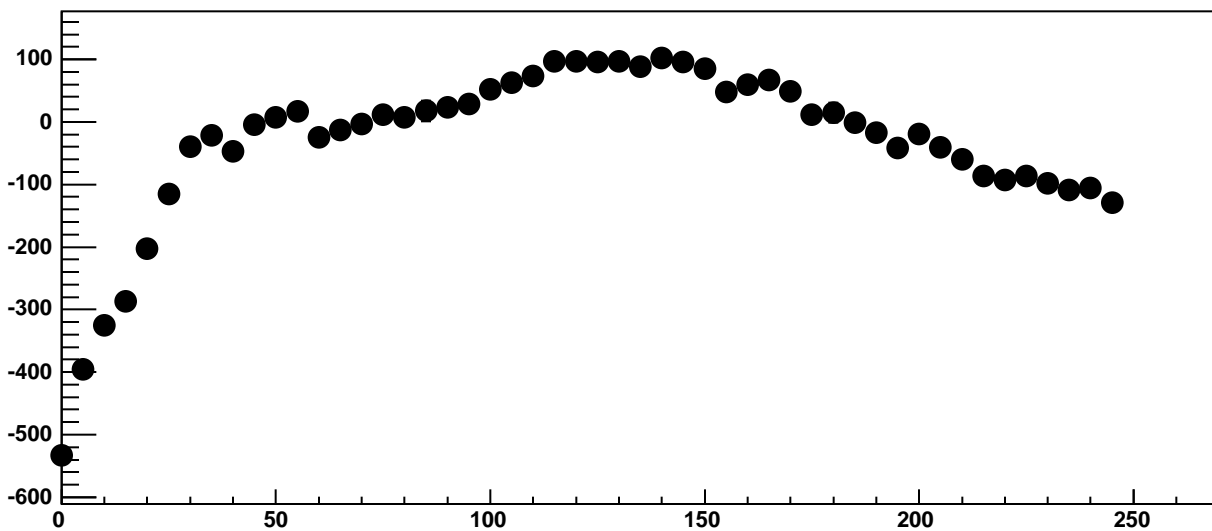


$\chi^2 / \text{ndf}$	2332 / 41
p0	$-323.7 \pm 8.405$
p1	$-6377 \pm 441.2$
p2	$-607.1 \pm 5.967$
p3	$-1.045e+04 \pm 3544$
p4	$0.02461 \pm 0.001291$

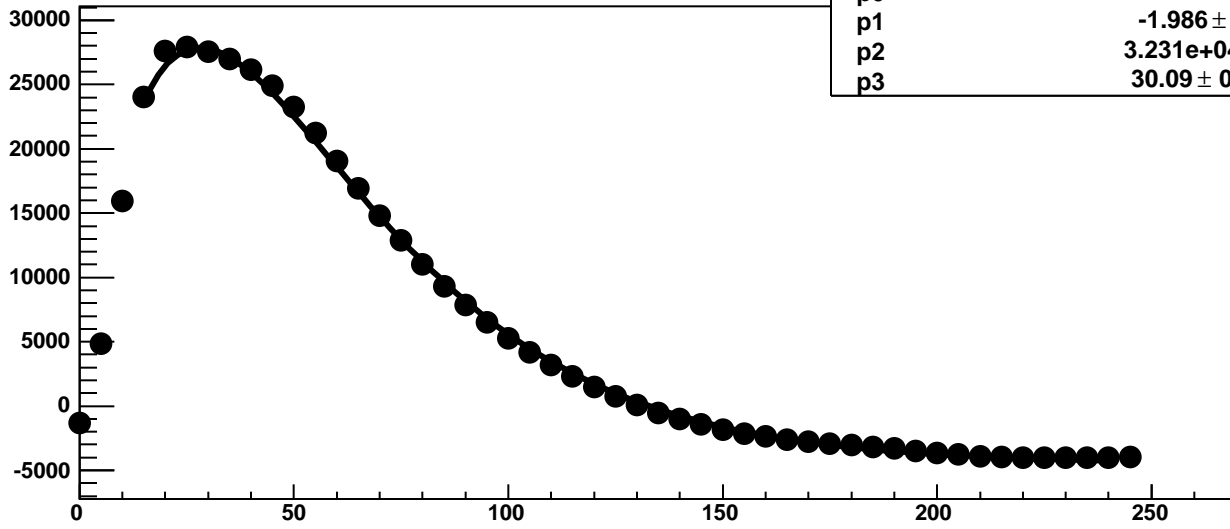
Chip 5, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

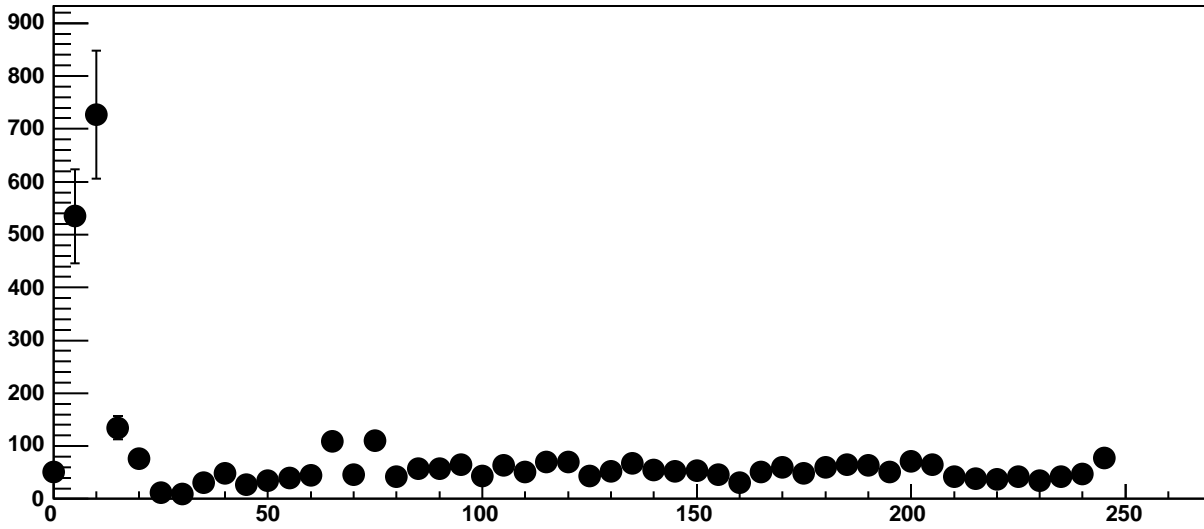


Chip 5, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

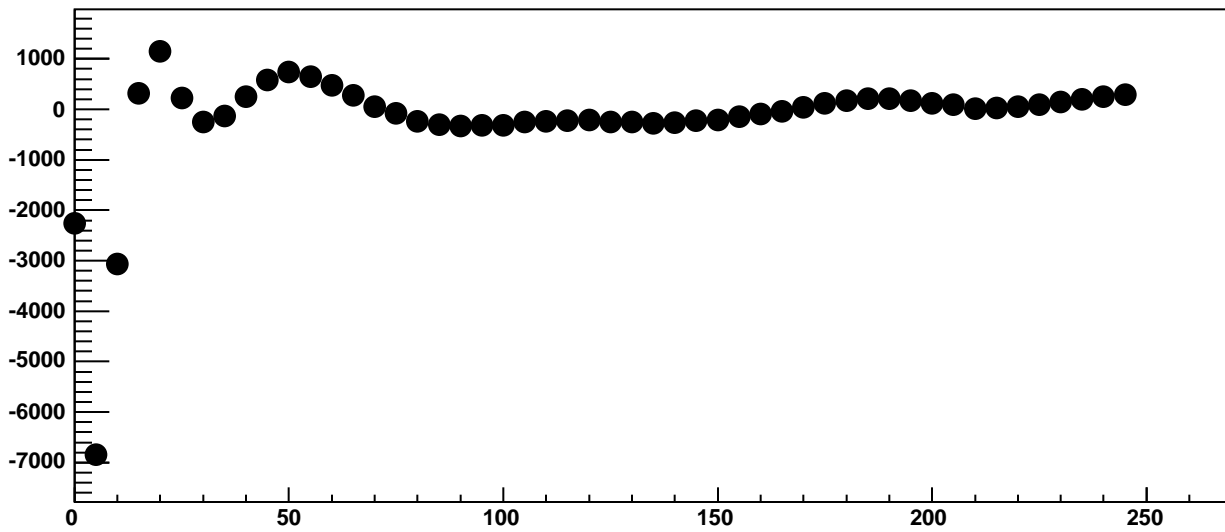


$\chi^2 / \text{ndf}$	6.199e+04 / 42
p0	-4462 ± 3.089
p1	-1.986 ± 0.01843
p2	3.231e+04 ± 3.35
p3	30.09 ± 0.009909

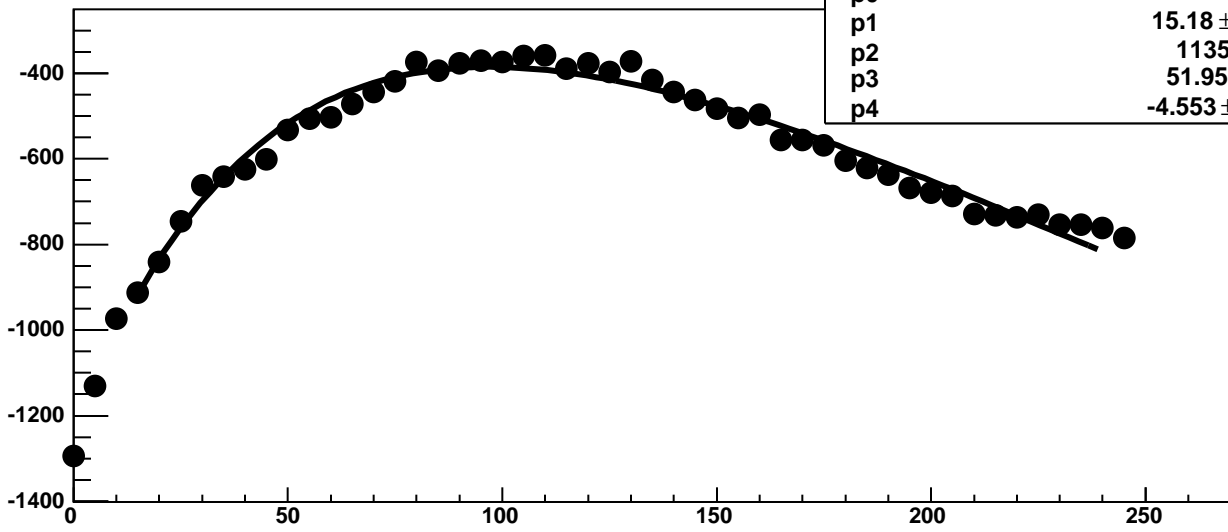
Chip 5, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



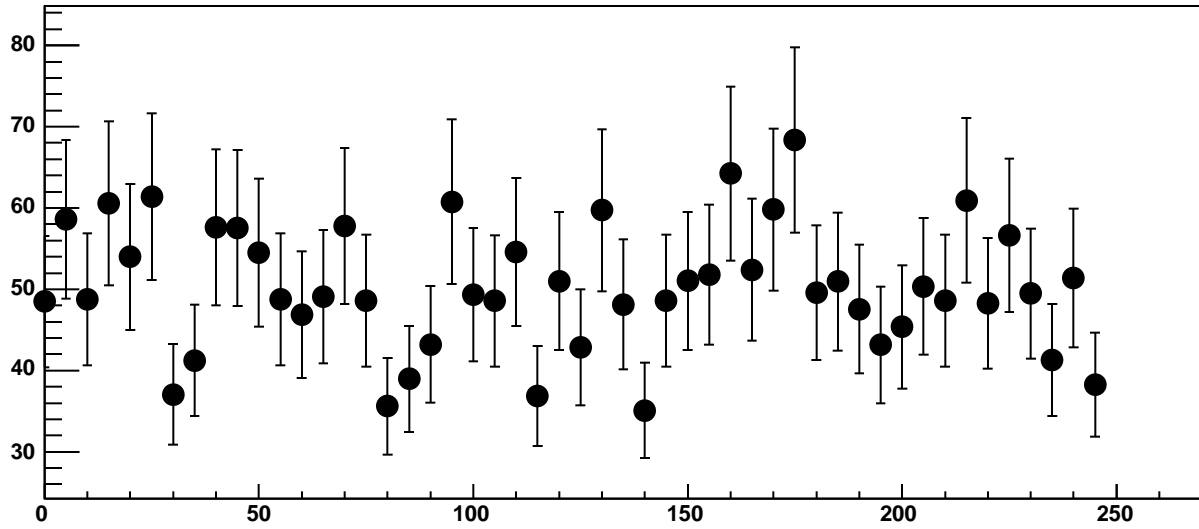
Chip 5, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold



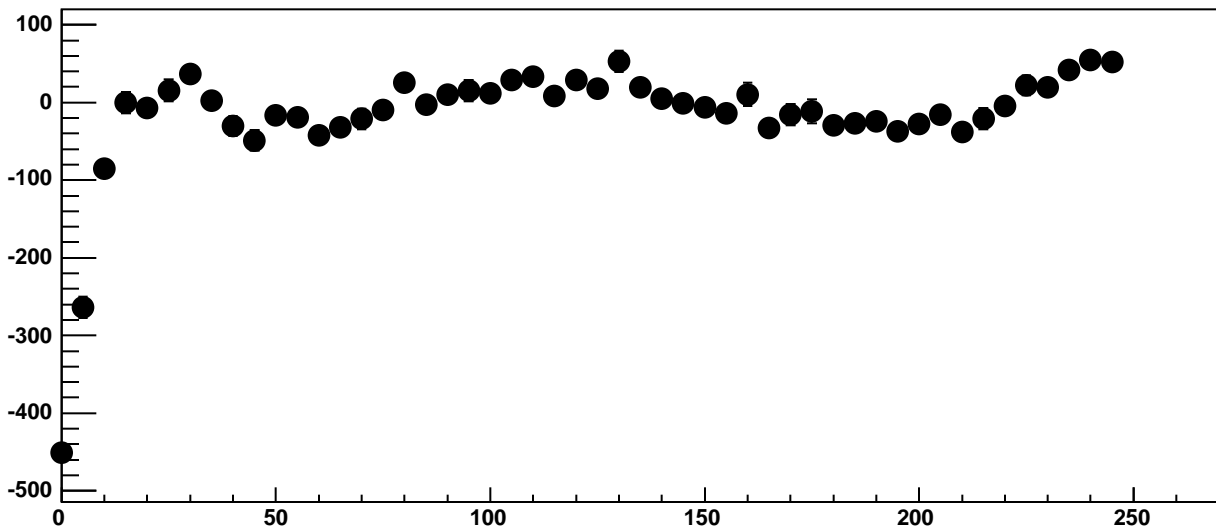
Chip 5, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold



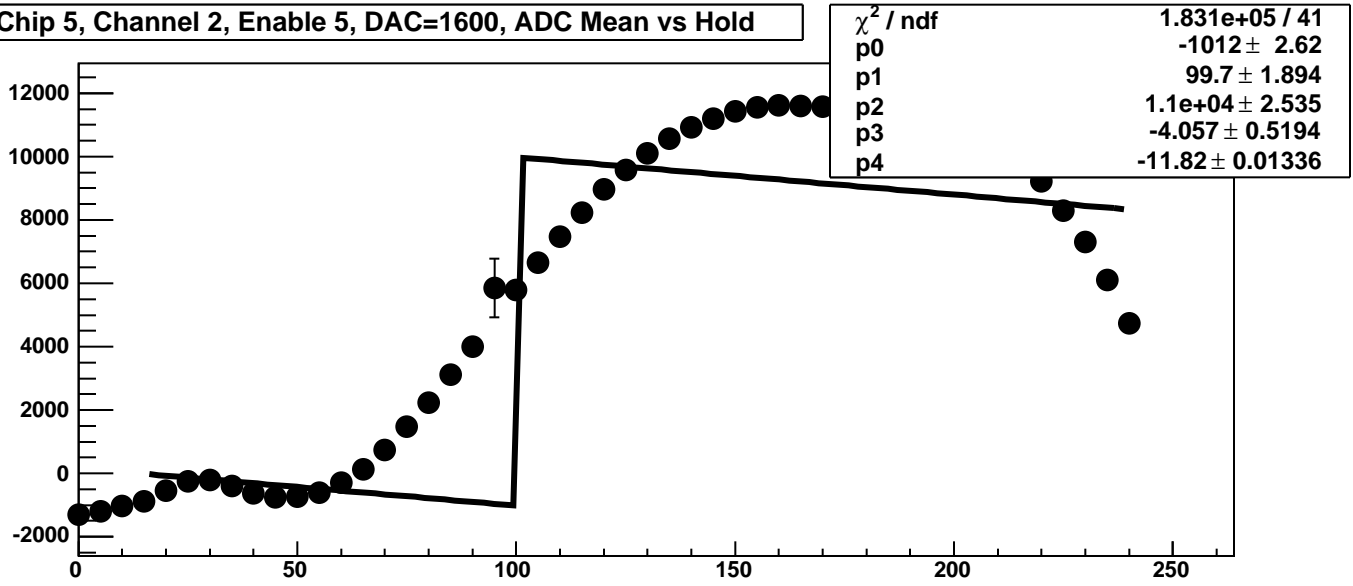
Chip 5, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



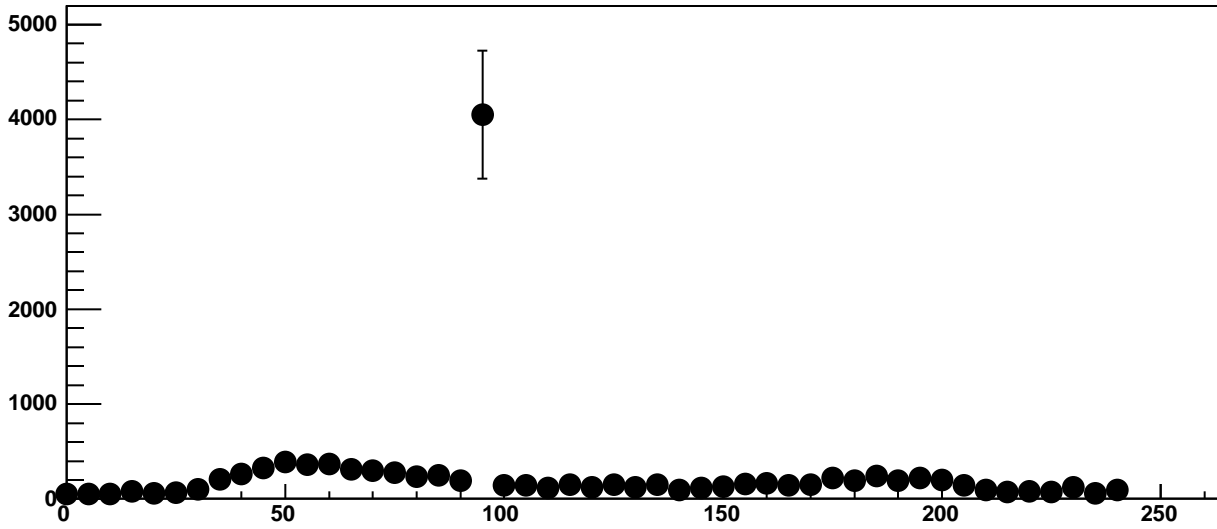
Chip 5, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold



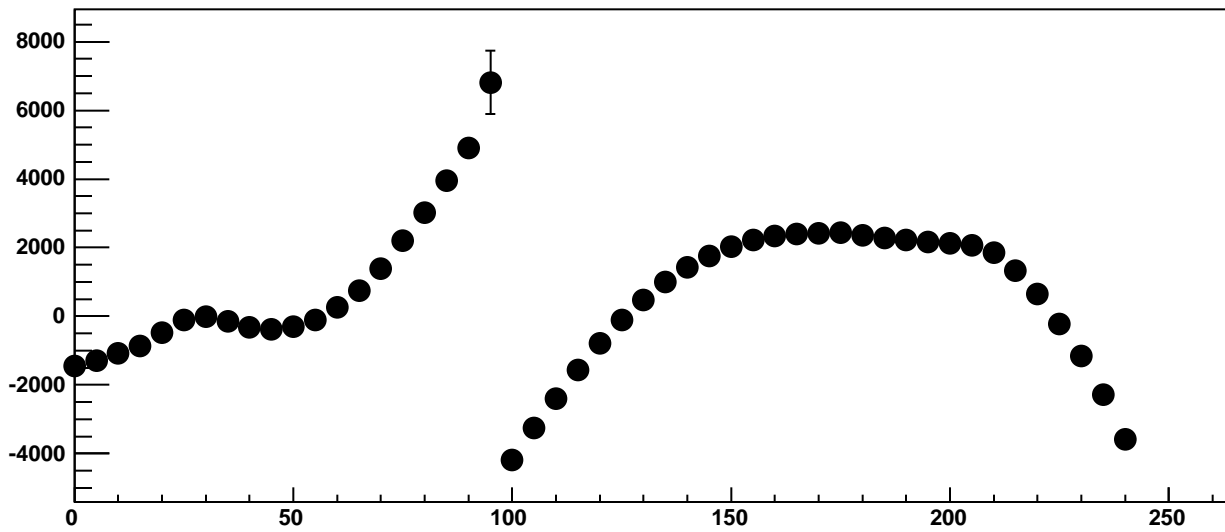
Chip 5, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold



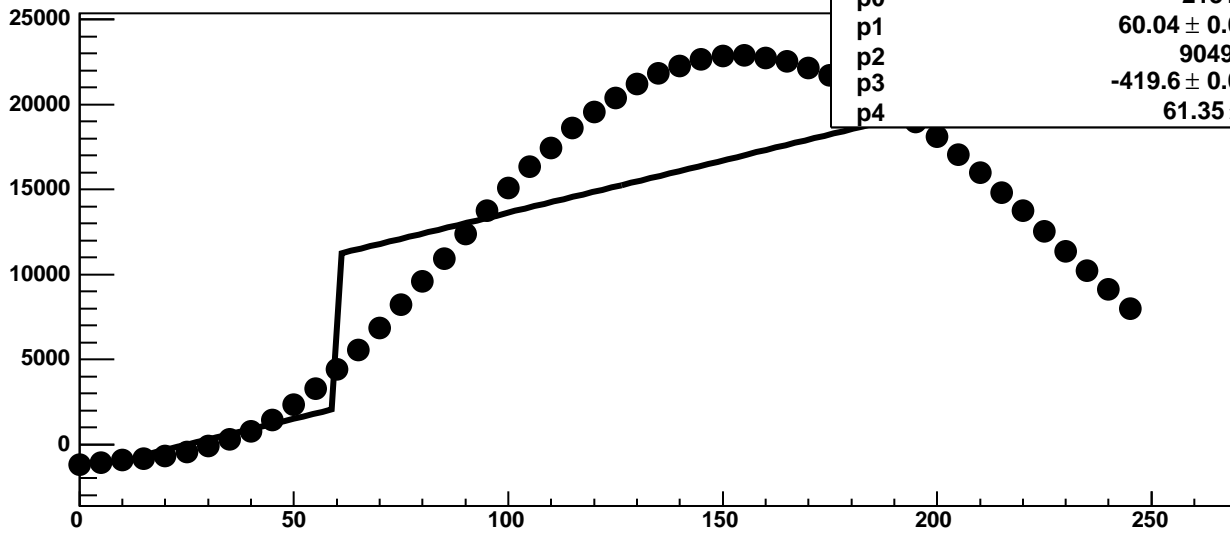
Chip 5, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

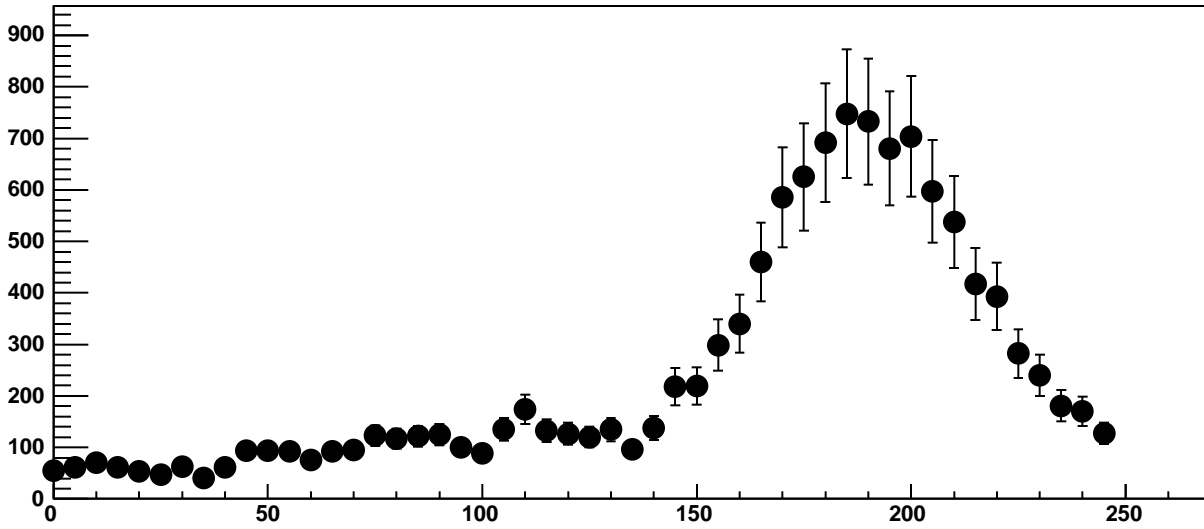


Chip 5, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

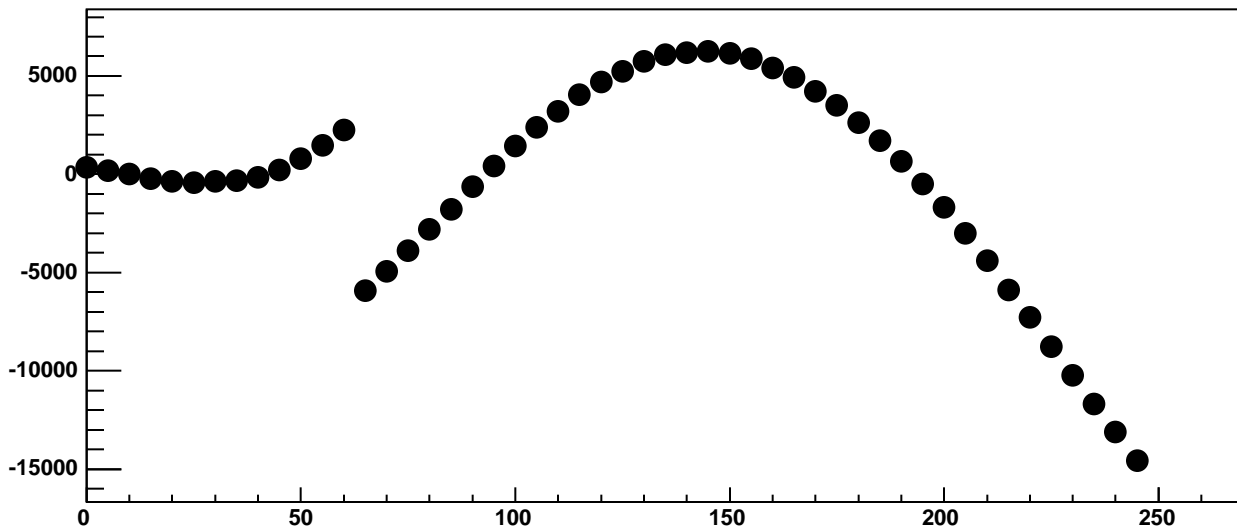


$\chi^2 / \text{ndf}$	7.405e+05 / 41
p0	2131 ± 5.638
p1	60.04 ± 0.0001359
p2	9049 ± 16.08
p3	-419.6 ± 0.0003408
p4	61.35 ± 0.1401

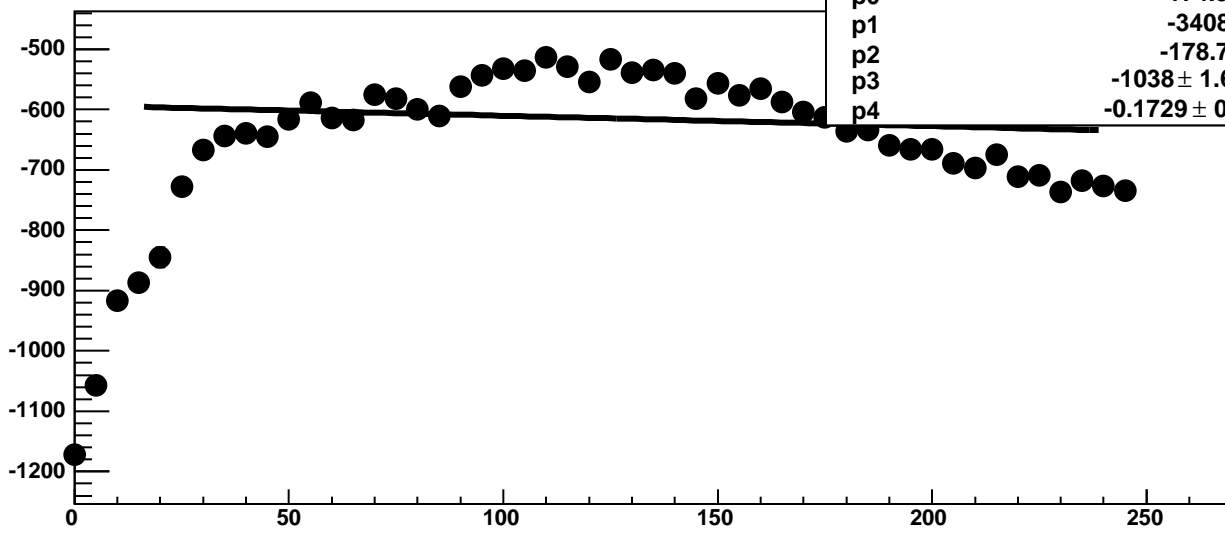
Chip 5, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

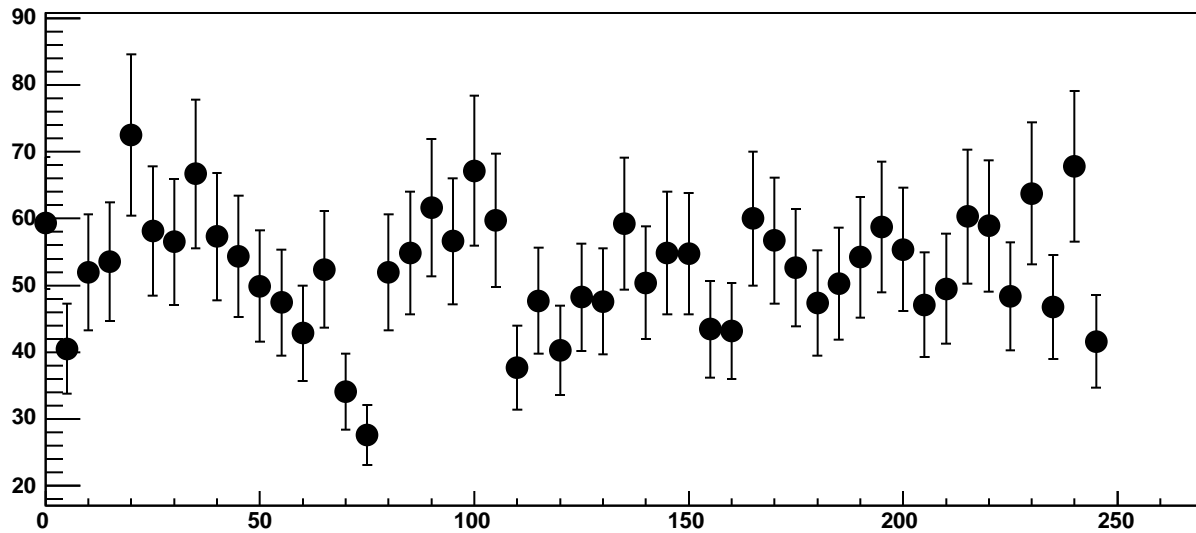


Chip 5, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

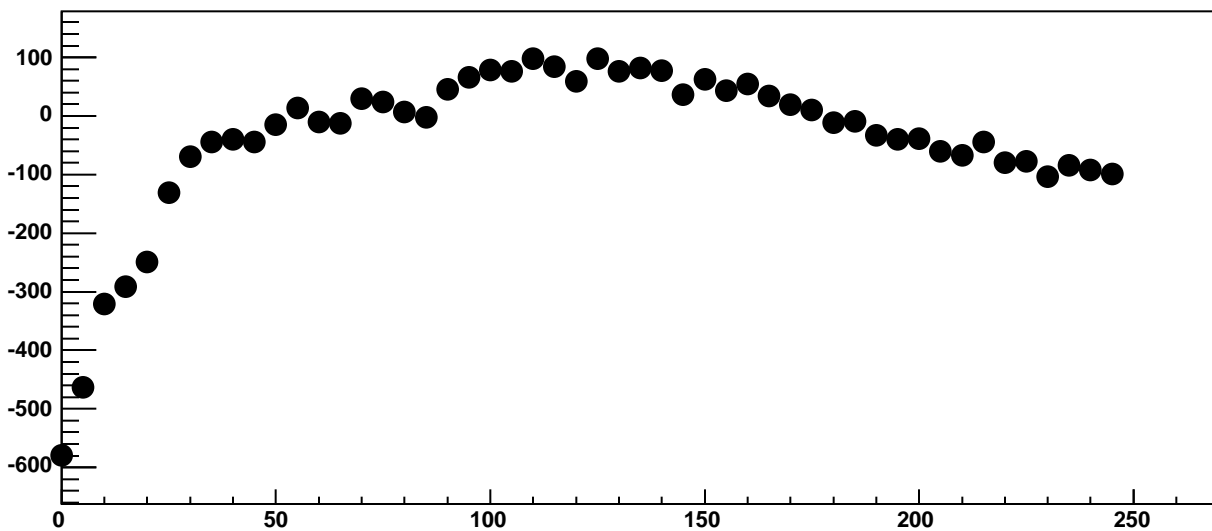


$\chi^2 / \text{ndf}$	1931 / 41
p0	$174.9 \pm 8.037$
p1	$-3408 \pm 47.35$
p2	$-178.7 \pm 10.93$
p3	$-1038 \pm 1.647\text{e}+04$
p4	$-0.1729 \pm 0.002275$

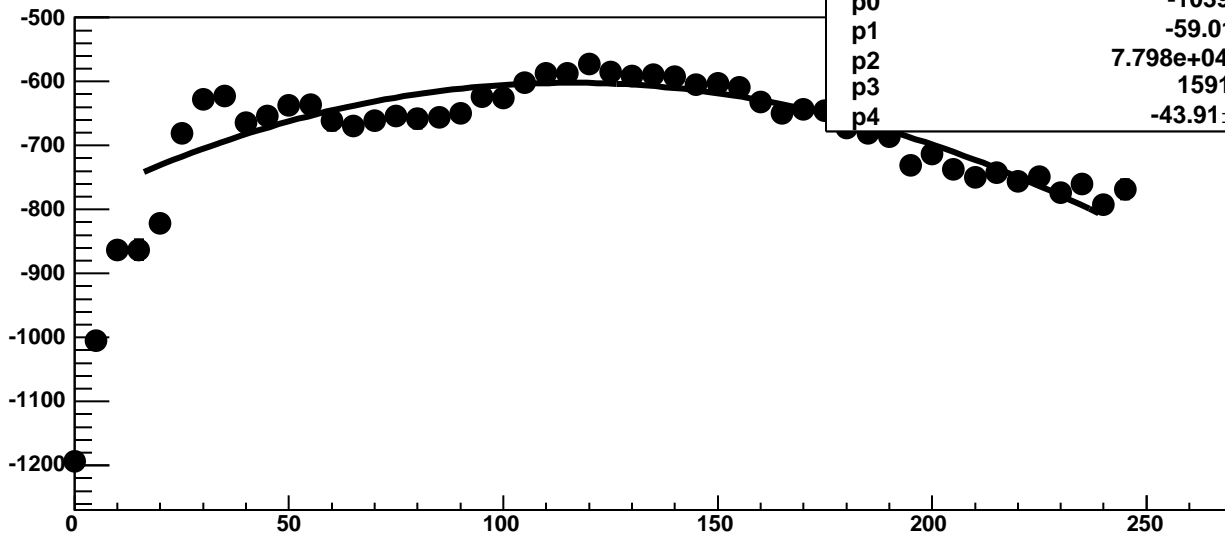
Chip 5, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold

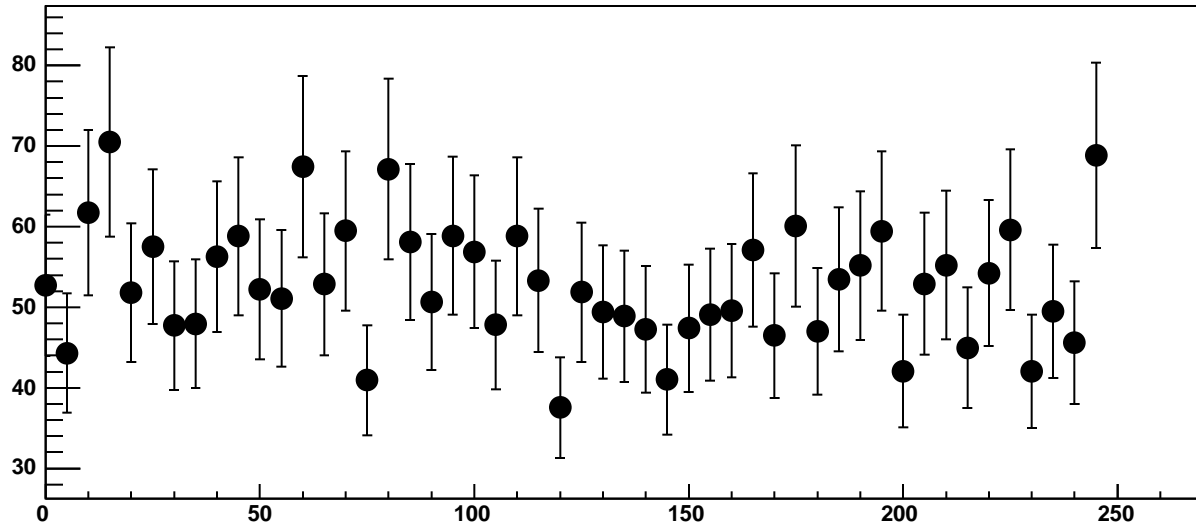


Chip 5, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

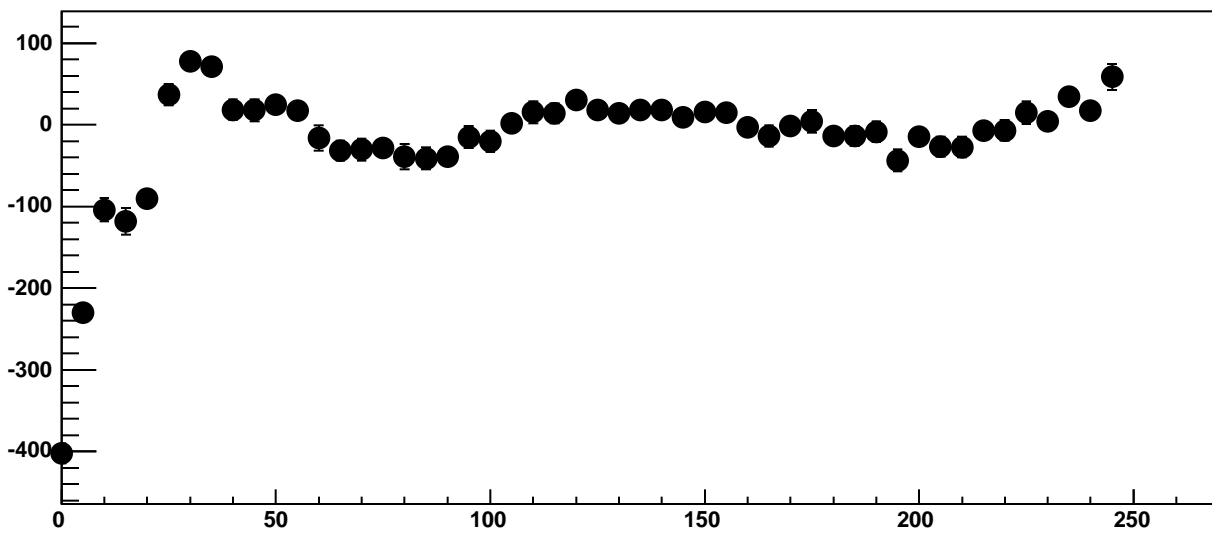


$\chi^2 / \text{ndf}$	343.5 / 41
p0	$-1039 \pm 21.35$
p1	$-59.01 \pm 4.301$
p2	$7.798e+04 \pm 196.4$
p3	$1591 \pm 4.285$
p4	$-43.91 \pm 0.1143$

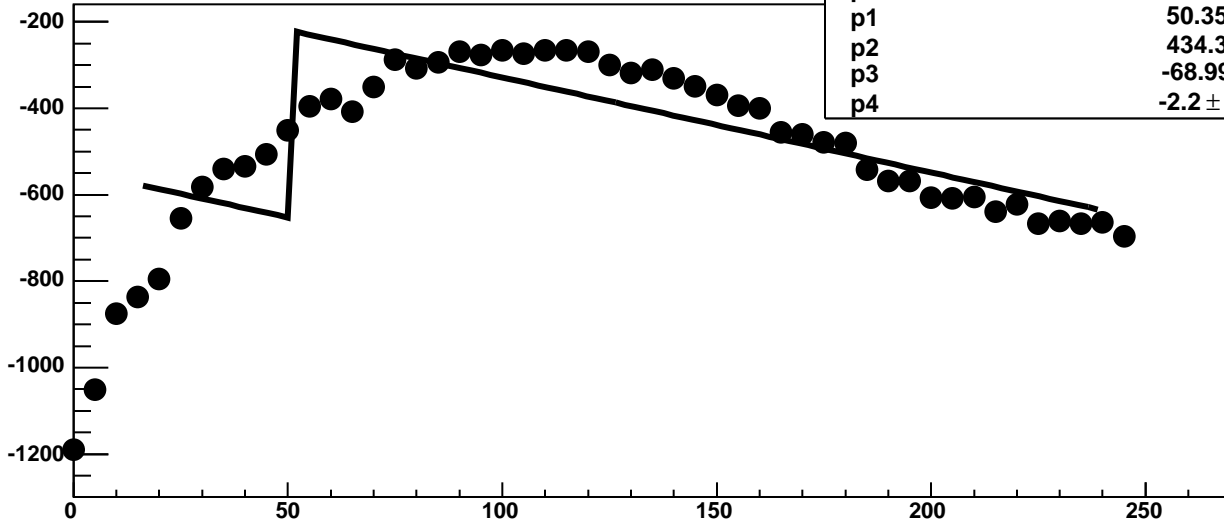
Chip 5, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

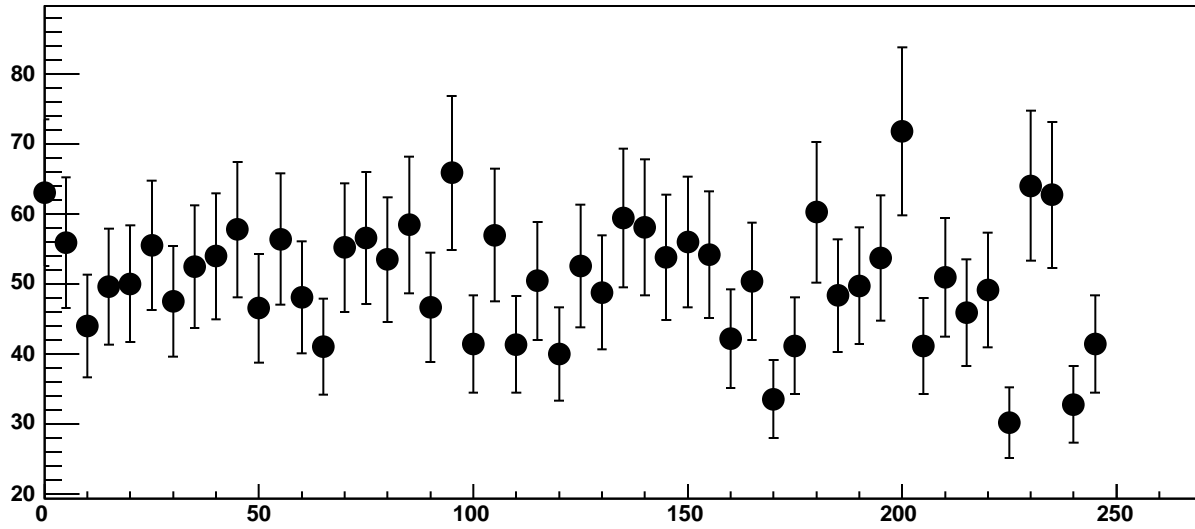


Chip 5, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

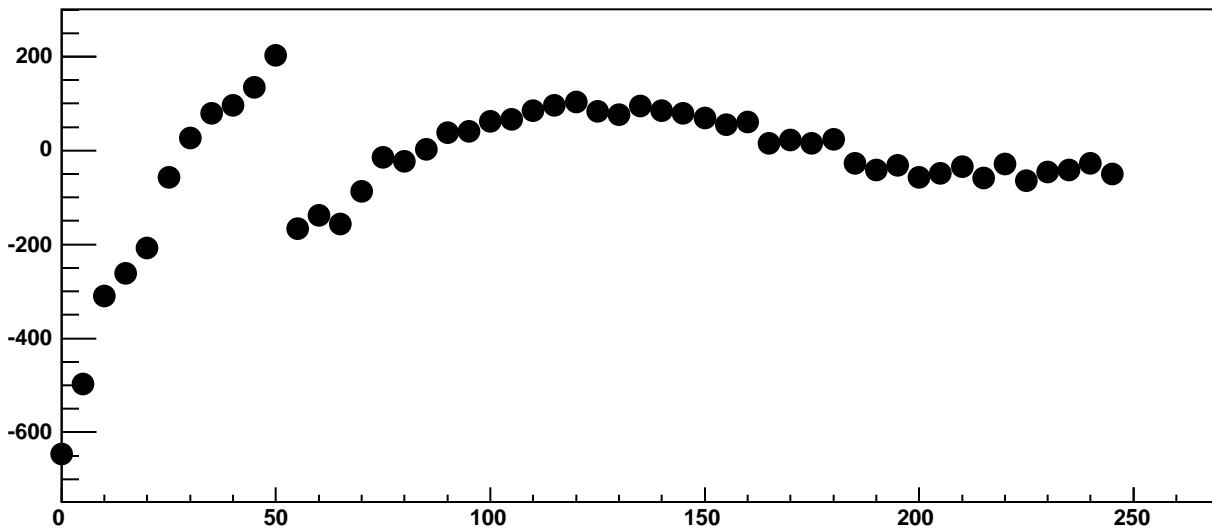


$\chi^2 / \text{ndf}$	3010 / 41
p0	$-653.5 \pm 14.87$
p1	$50.35 \pm 6.404$
p2	$434.3 \pm 3.207$
p3	$-68.99 \pm 18.71$
p4	$-2.2 \pm 0.04519$

Chip 5, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

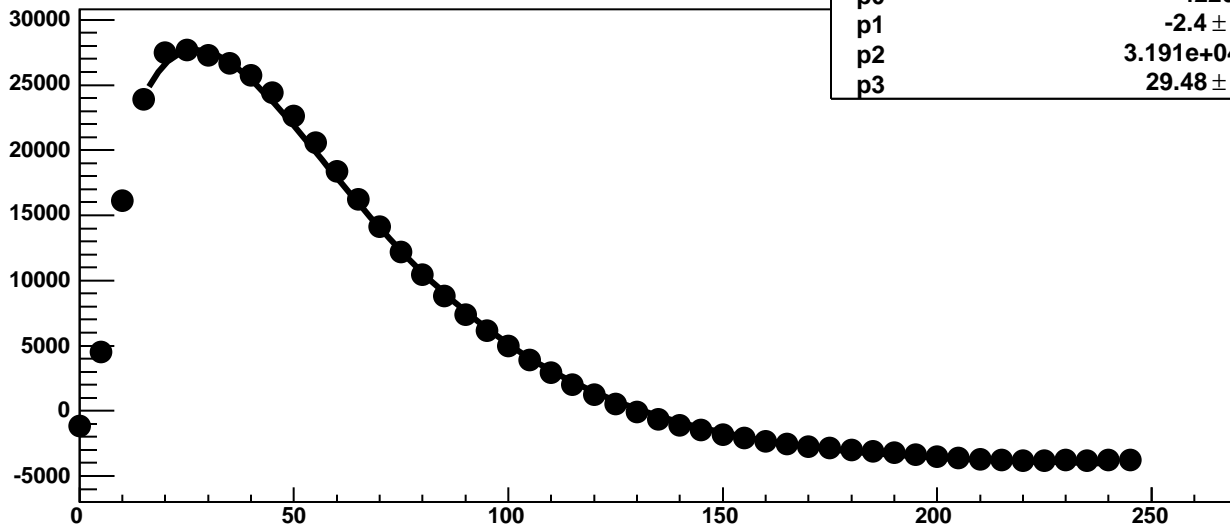


Chip 5, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

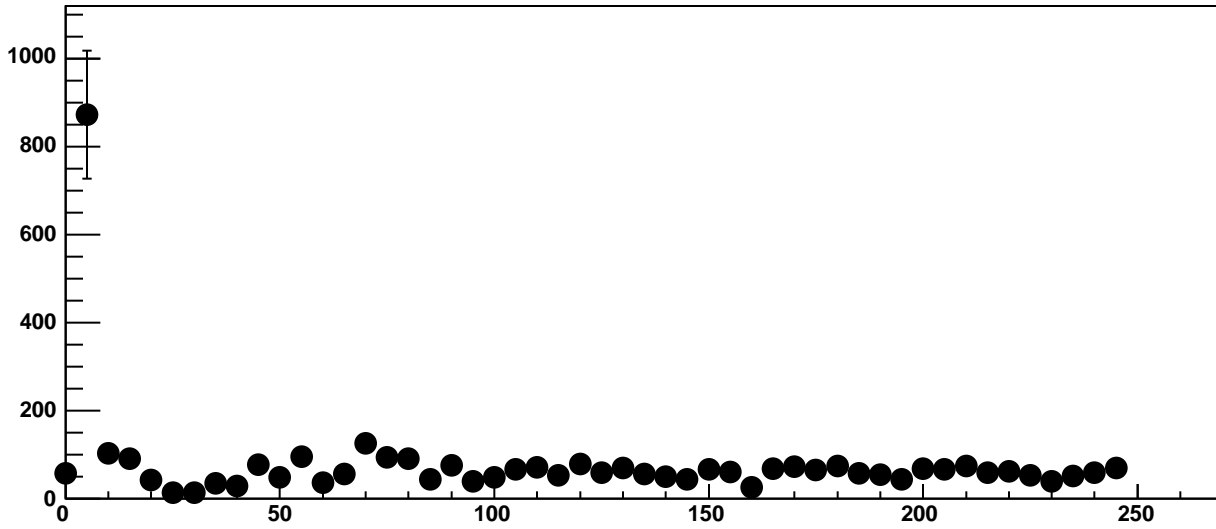




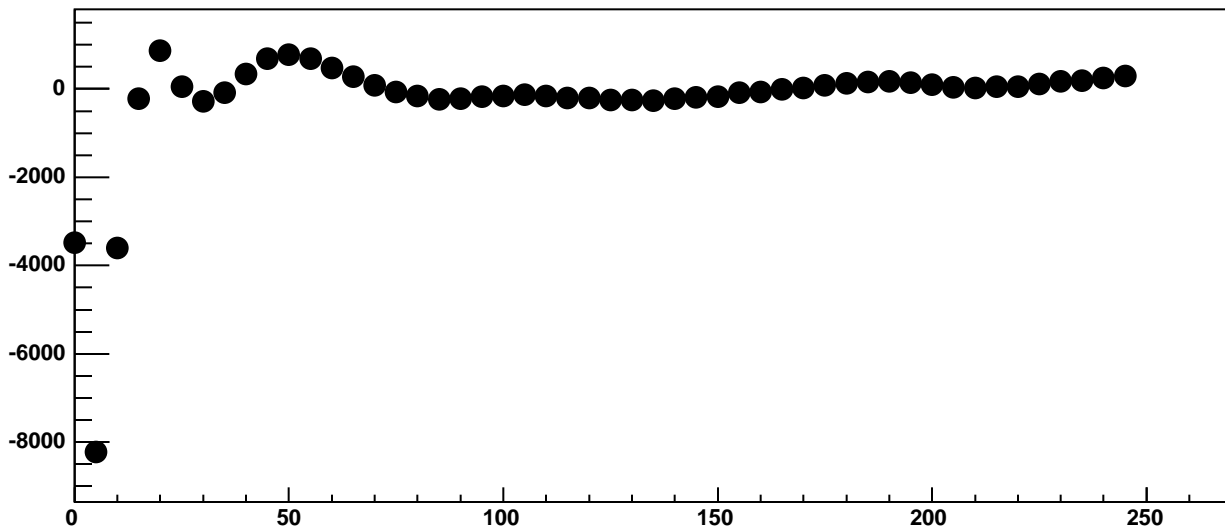
Chip 5, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold



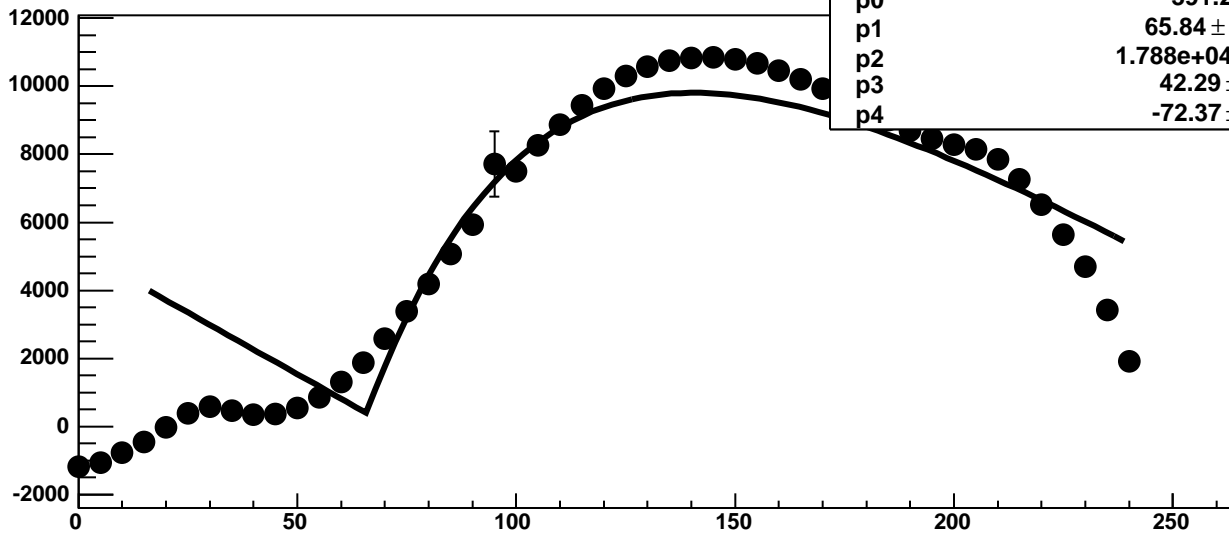
Chip 5, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold

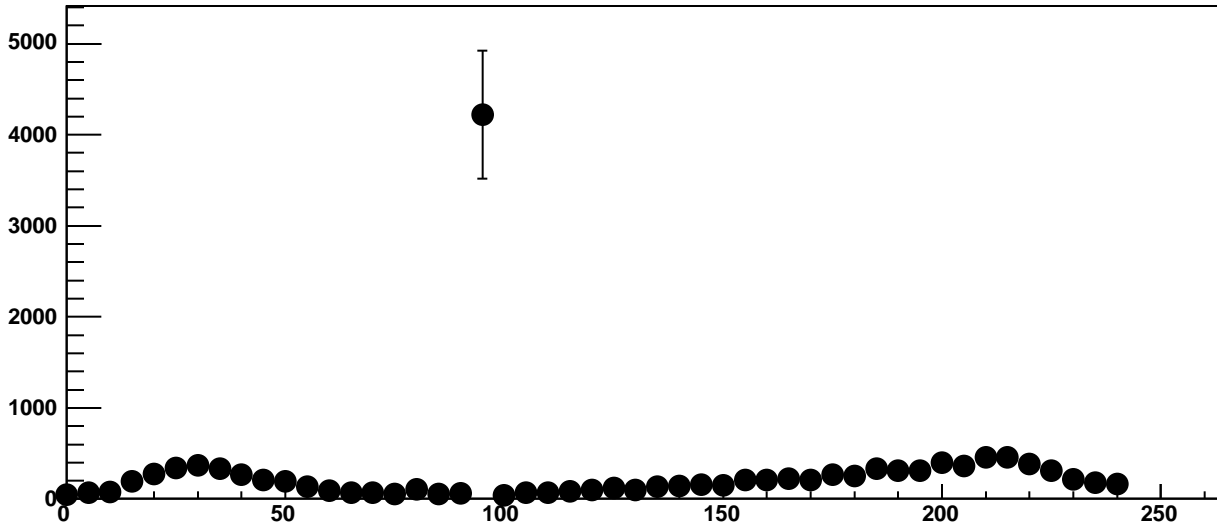


Chip 5, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

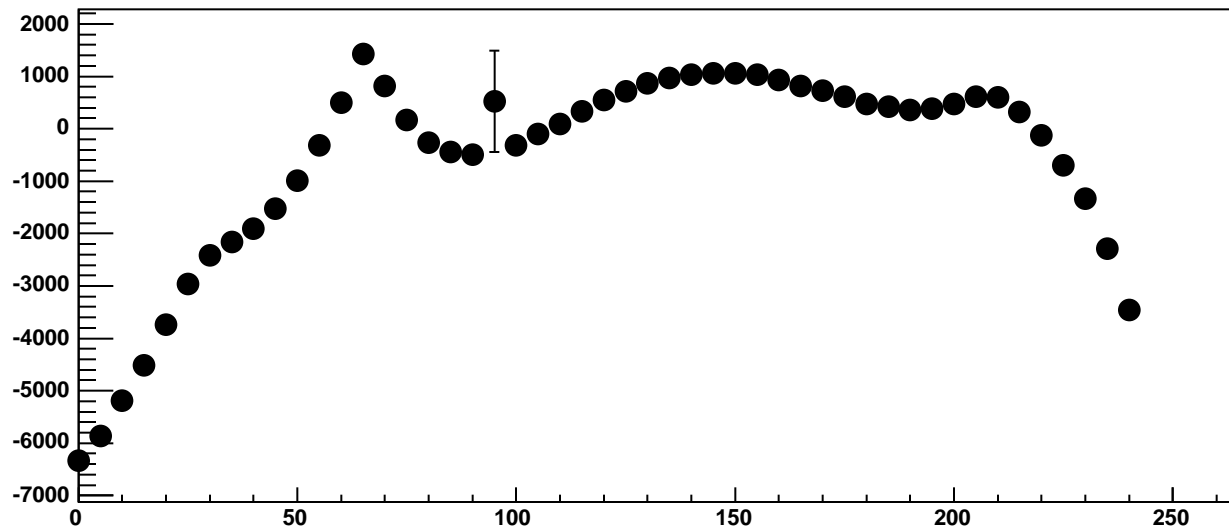


$\chi^2 / \text{ndf}$	5.456e+04 / 41
p0	391.2 ± 9.458
p1	65.84 ± 0.04325
p2	1.788e+04 ± 65.97
p3	42.29 ± 0.1663
p4	-72.37 ± 0.3832

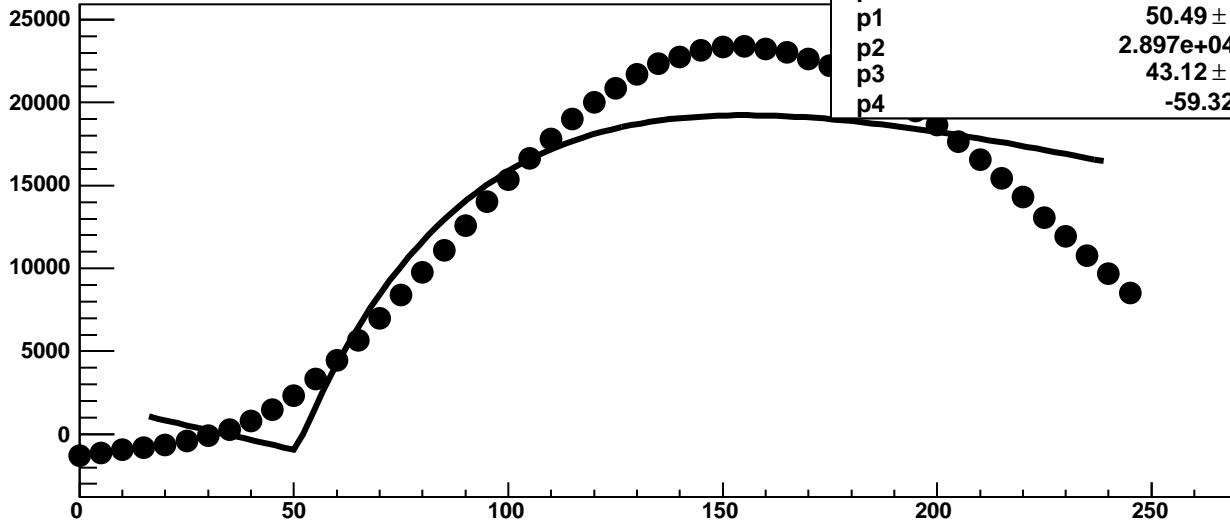
Chip 5, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

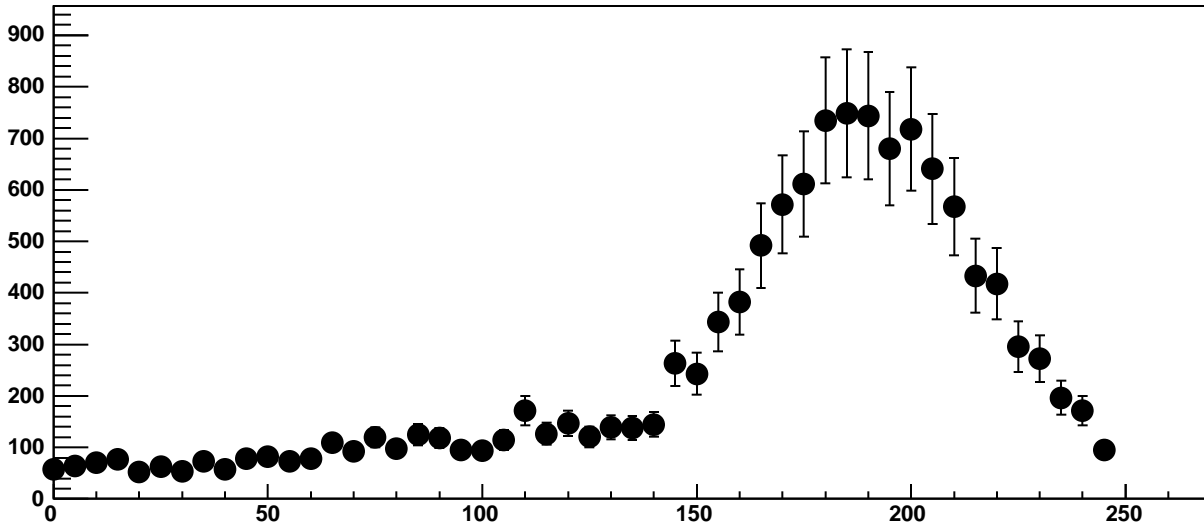


Chip 5, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

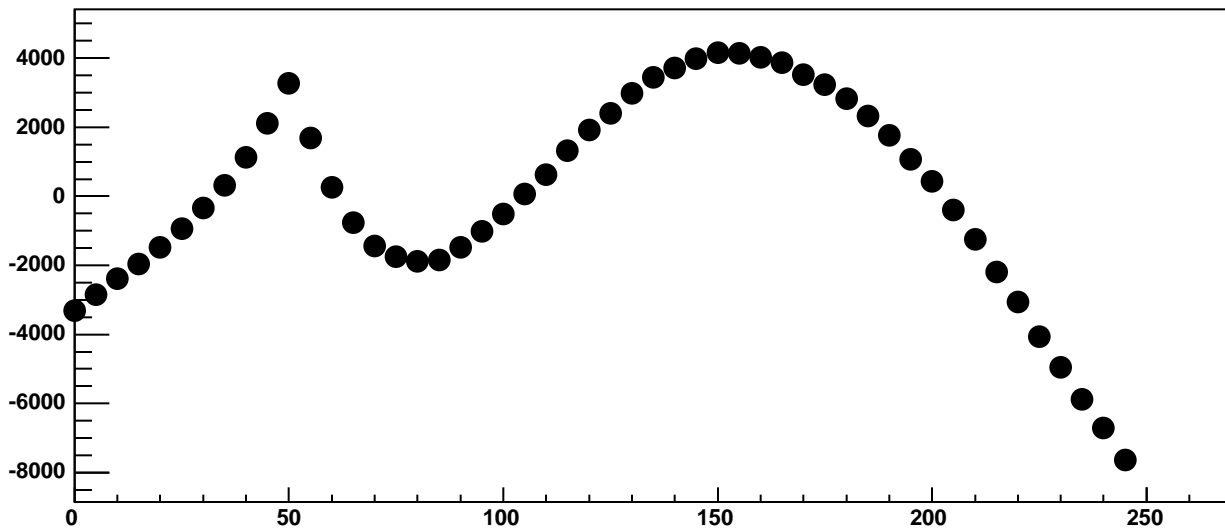


$\chi^2 / \text{ndf}$	2.437e+05 / 41
p0	-970.8 ± 7.218
p1	50.49 ± 0.02633
p2	2.897e+04 ± 56.61
p3	43.12 ± 0.09603
p4	-59.32 ± 0.305

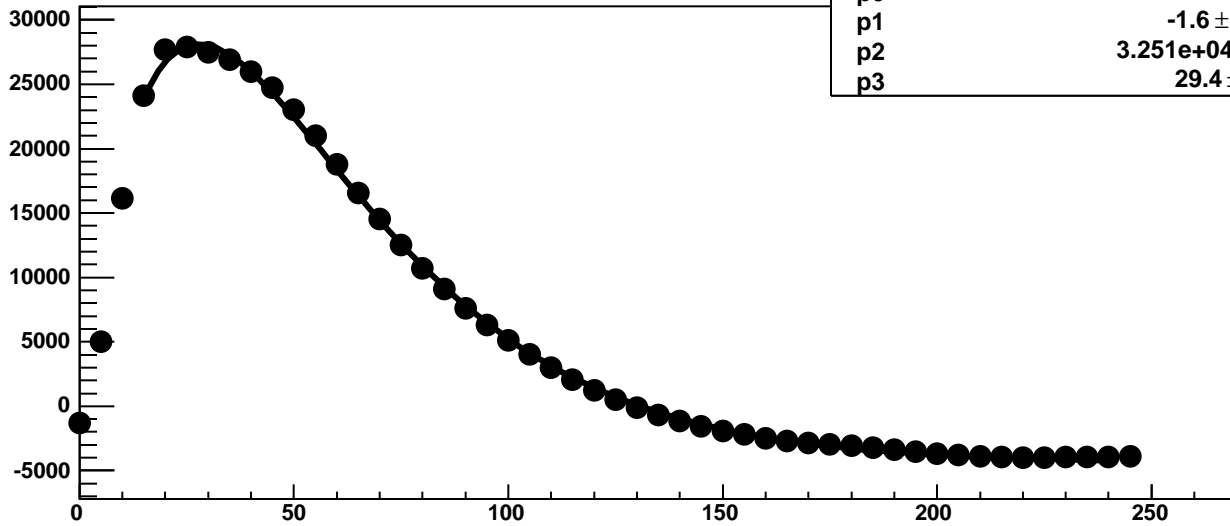
Chip 5, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

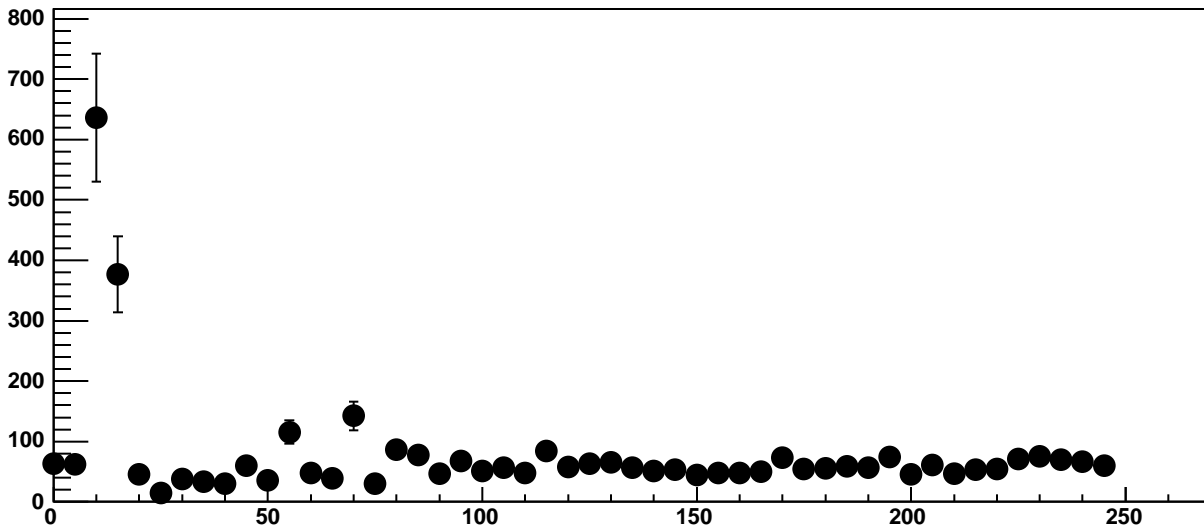


Chip 5, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold

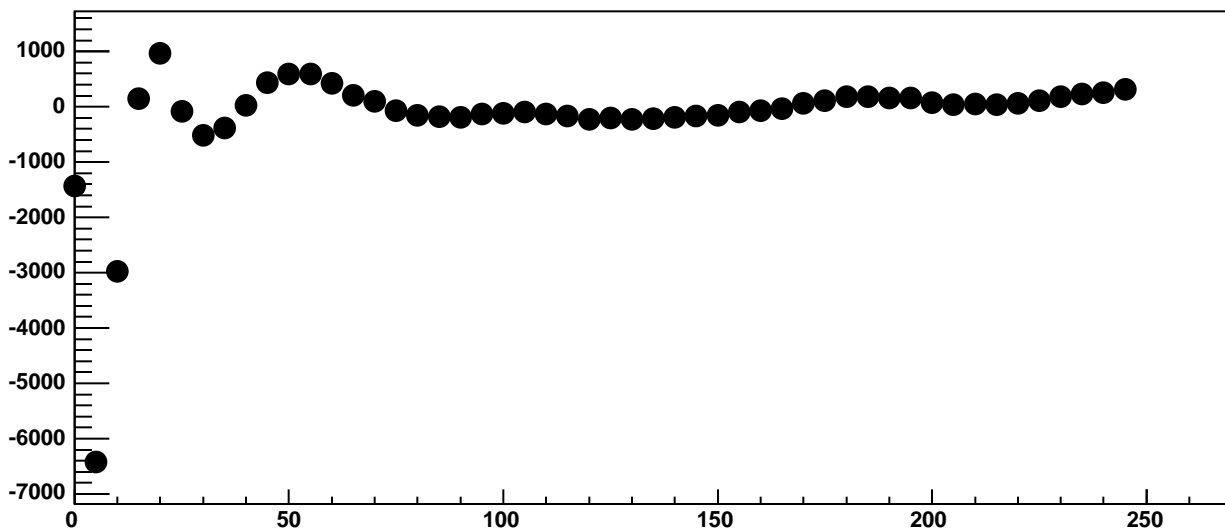


$\chi^2 / \text{ndf}$	2.813e+04 / 42
p0	-4402 ± 3.759
p1	-1.6 ± 0.02131
p2	3.251e+04 ± 4.197
p3	29.4 ± 0.0115

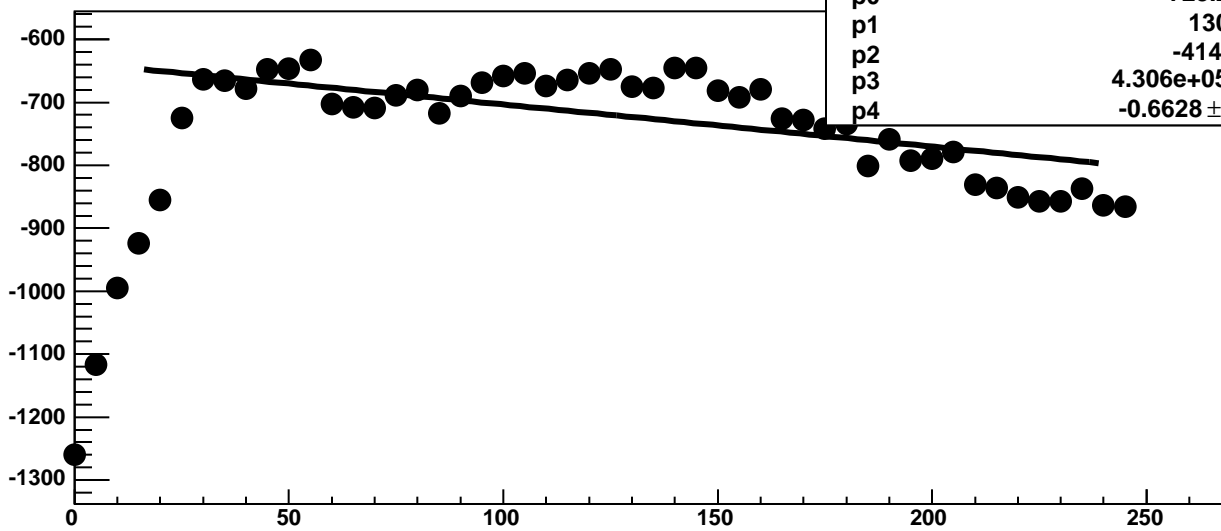
Chip 5, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



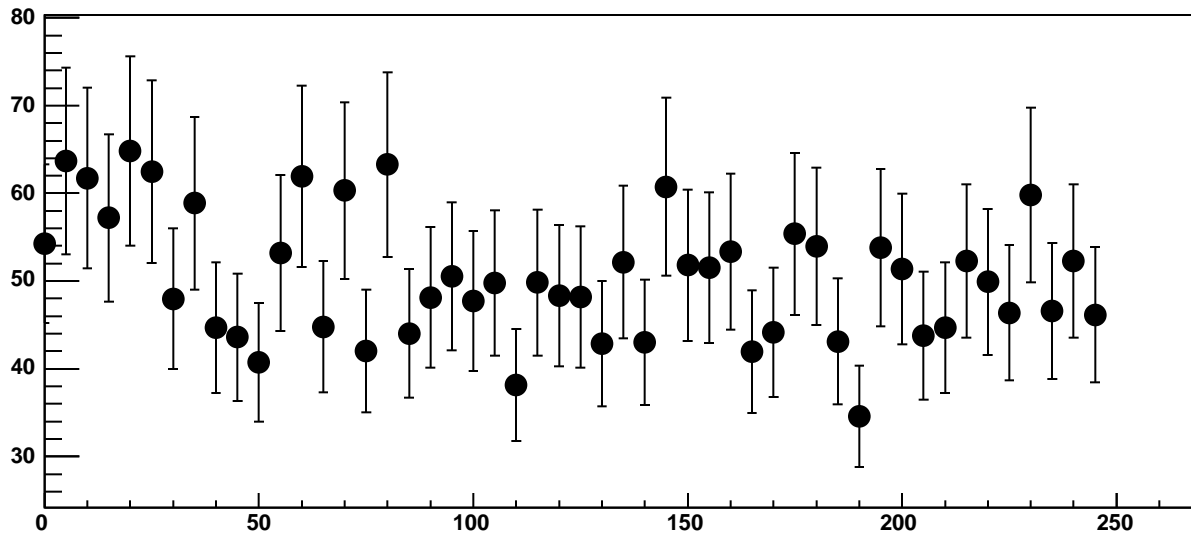
Chip 5, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold



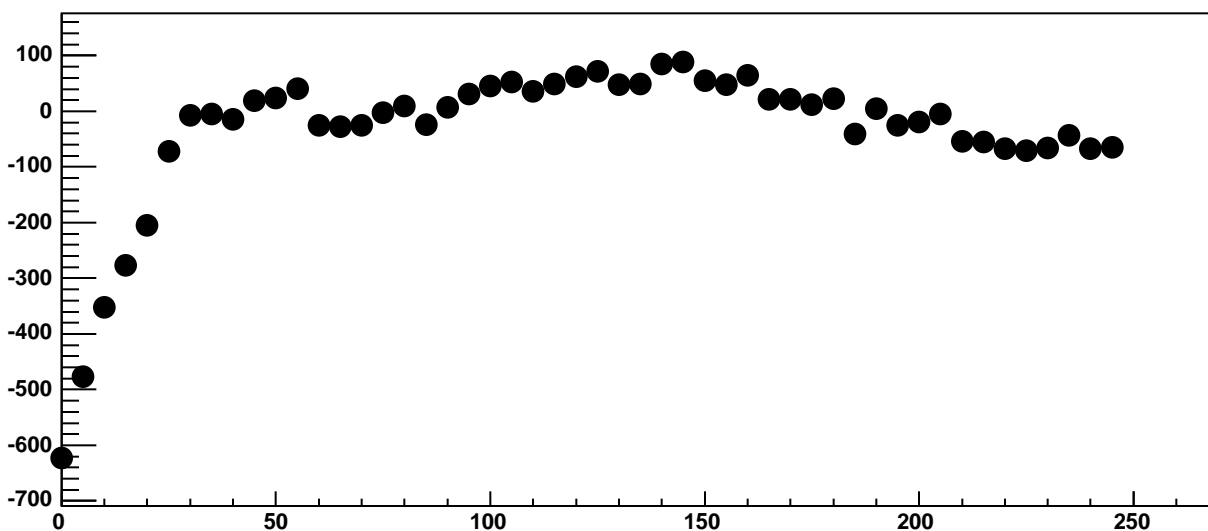
Chip 5, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold



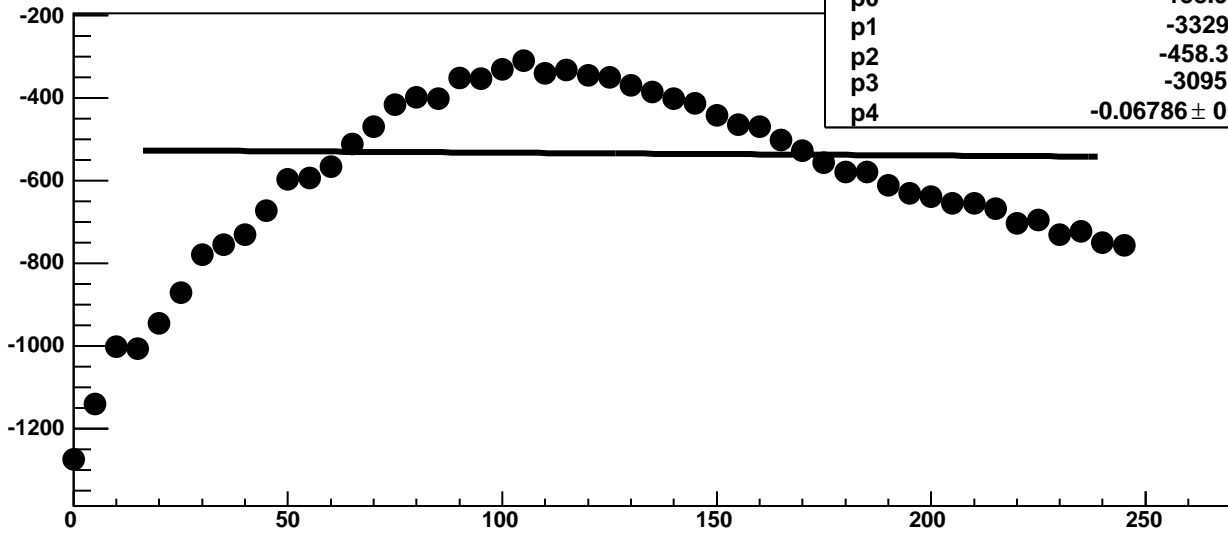
Chip 5, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



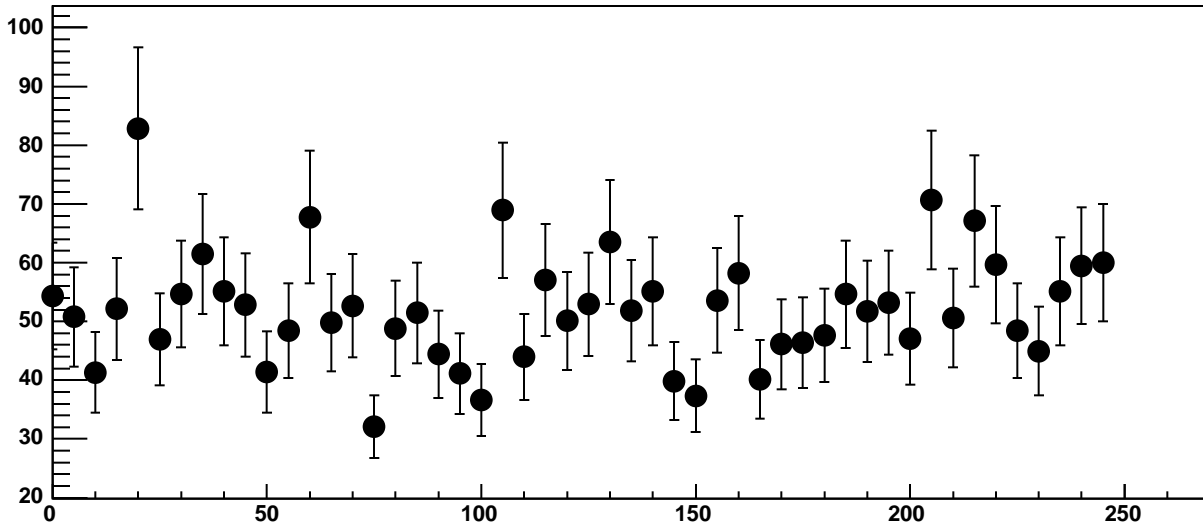
Chip 5, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold



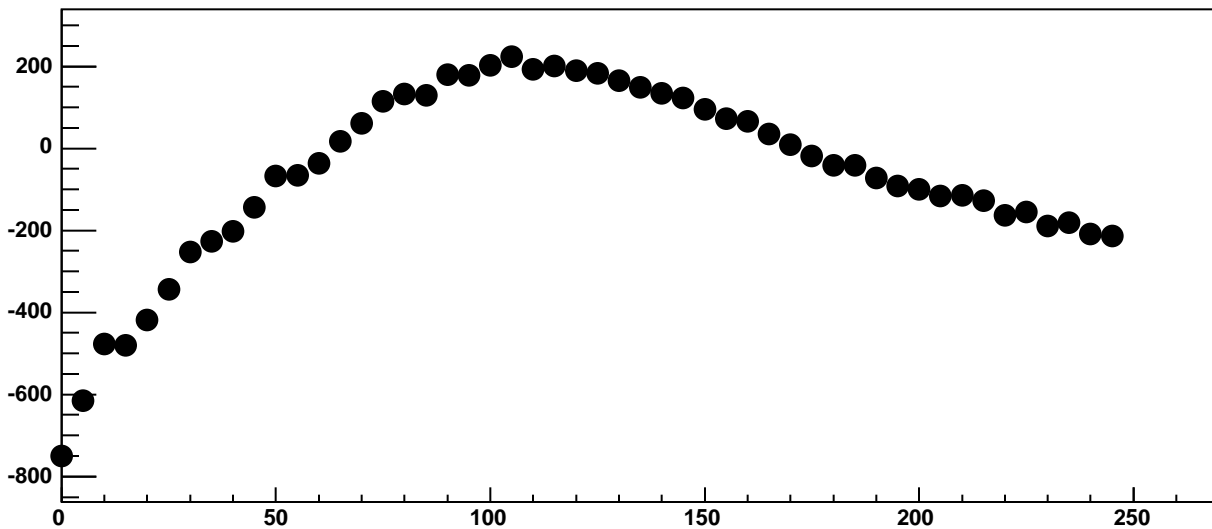
Chip 5, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold



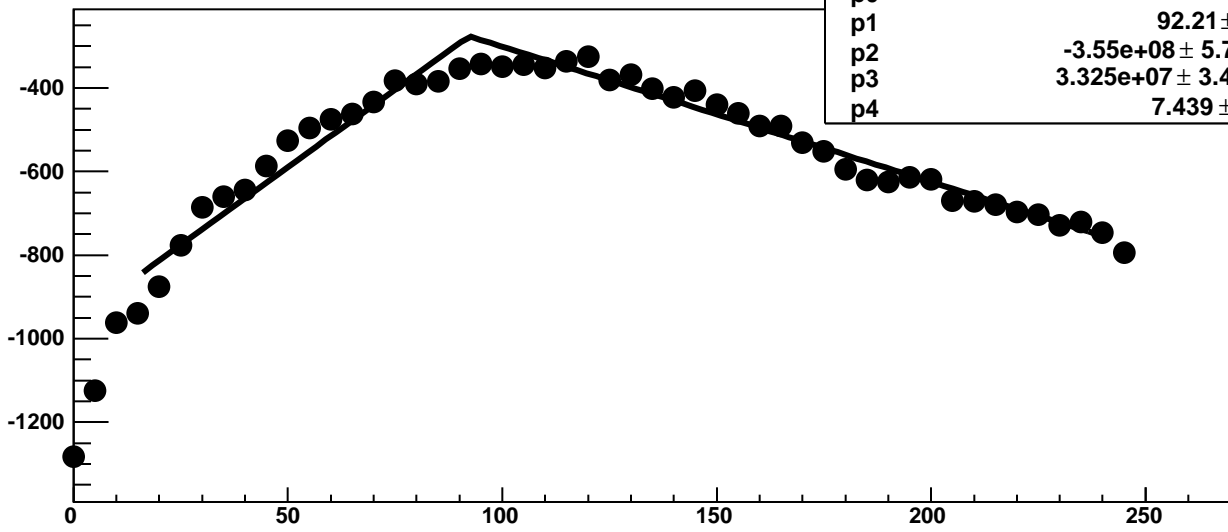
Chip 5, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

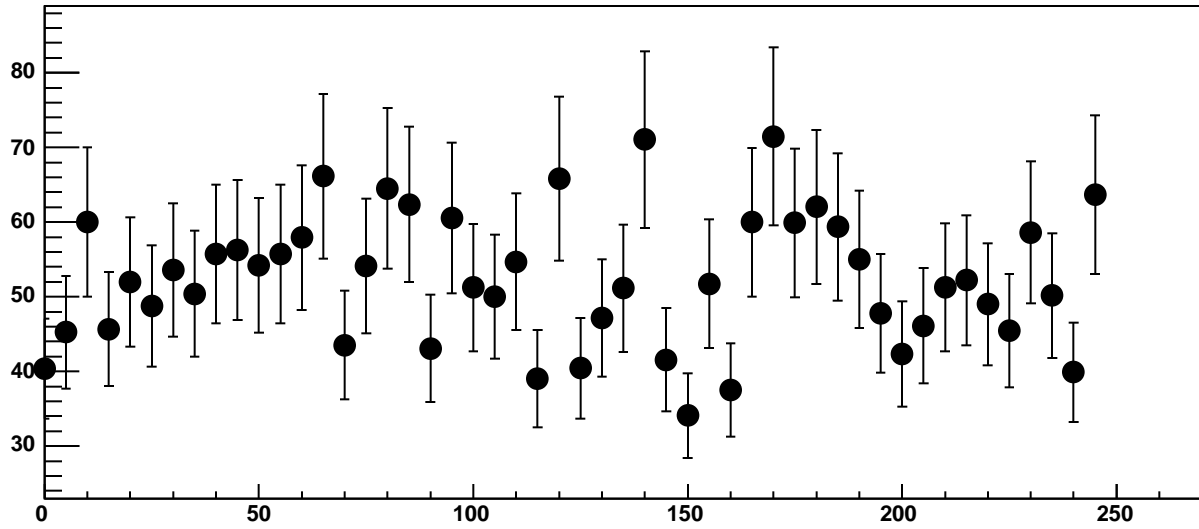


Chip 5, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold

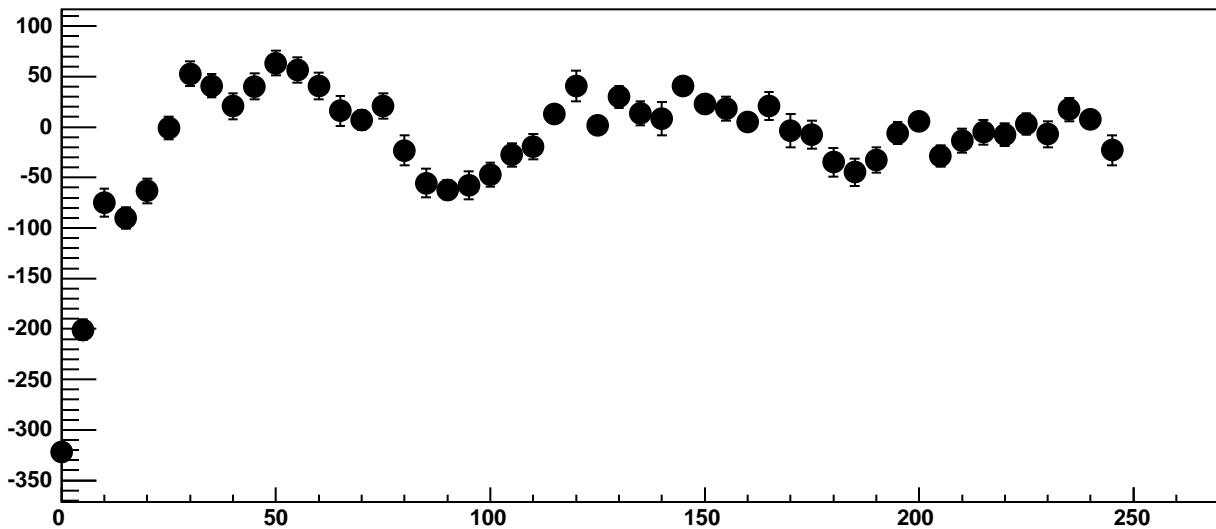


$\chi^2 / \text{ndf}$	390.3 / 41
p0	$-275.7 \pm 3.396$
p1	$92.21 \pm 0.6773$
p2	$-3.55\text{e}+08 \pm 5.761\text{e}+06$
p3	$3.325\text{e}+07 \pm 3.419\text{e}+05$
p4	$7.439 \pm 0.1254$

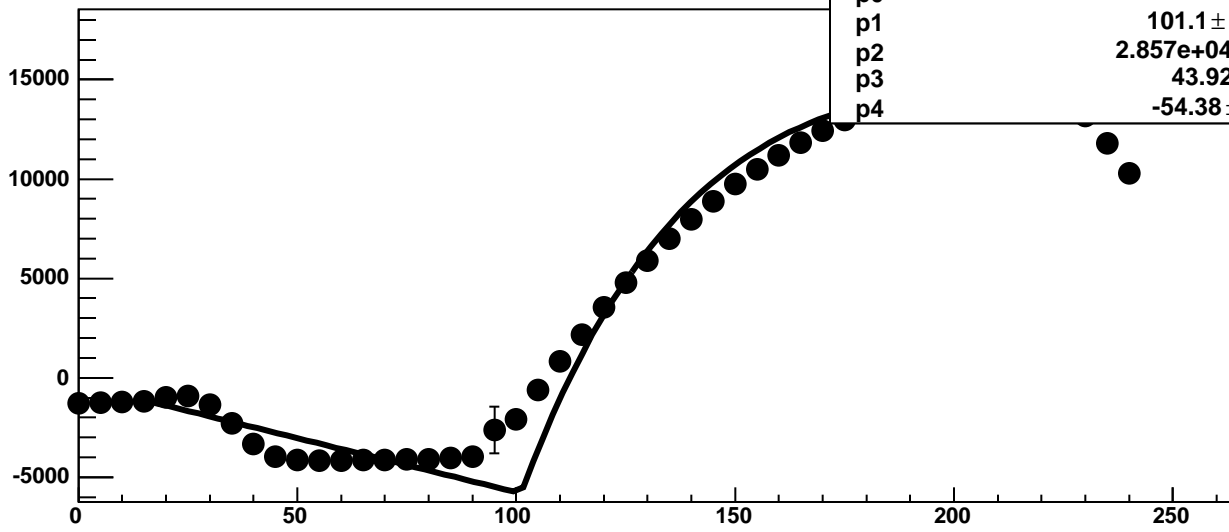
Chip 5, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



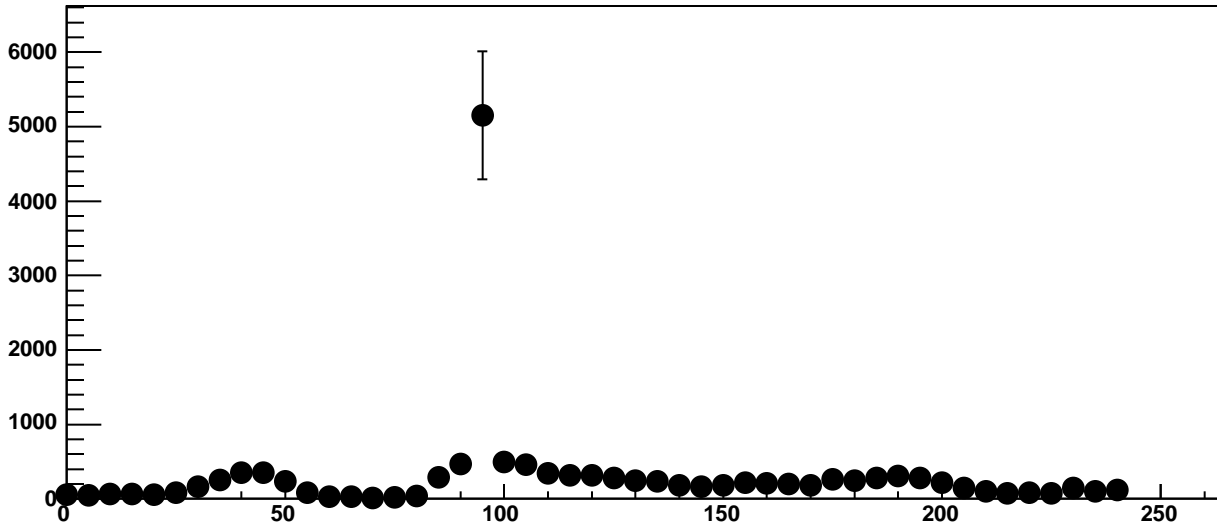
Chip 5, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold



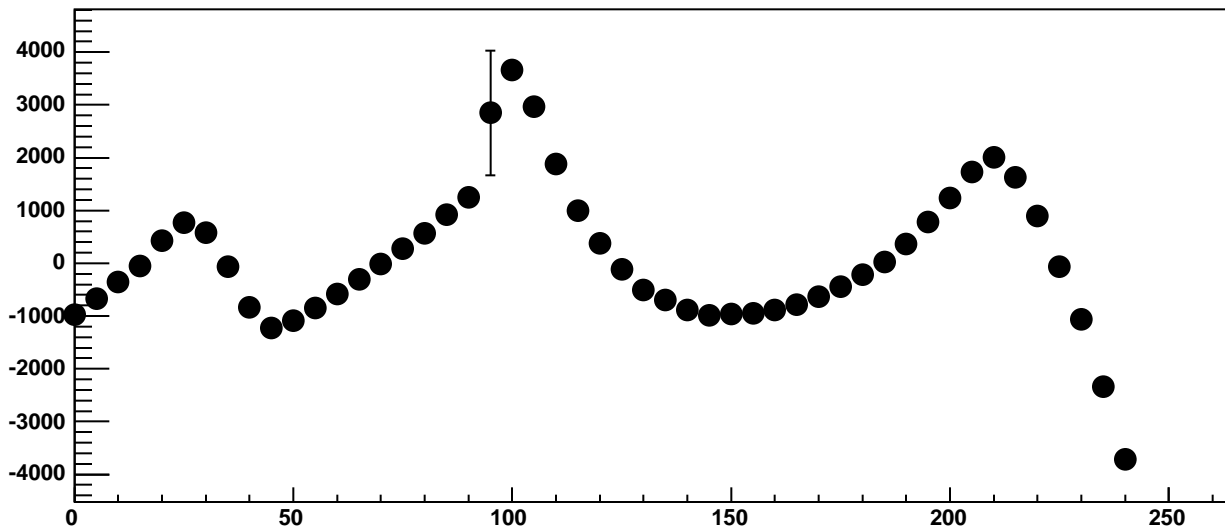
Chip 5, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 5, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

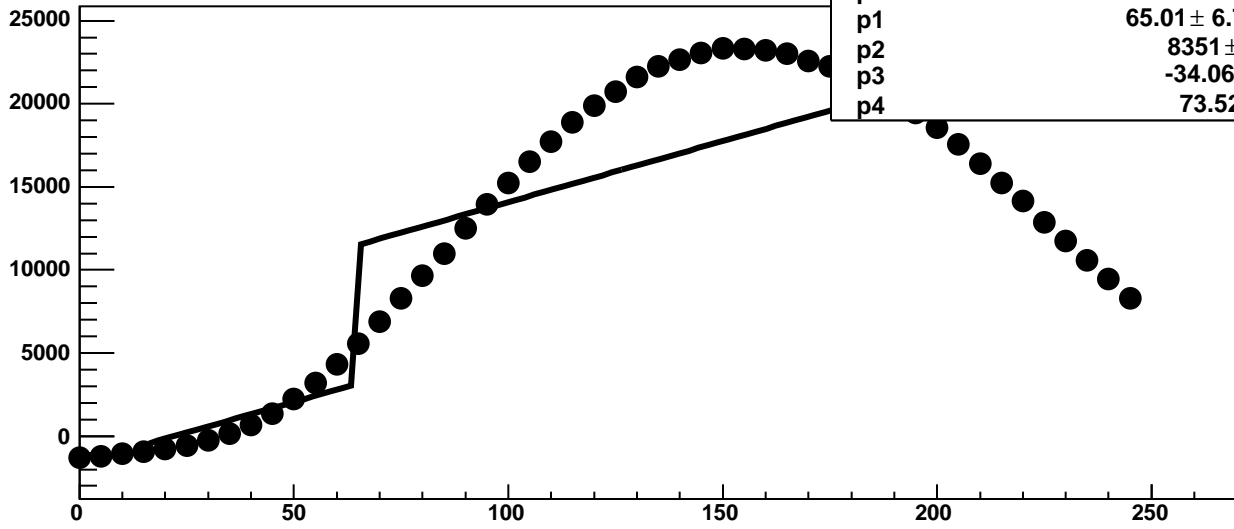


Chip 5, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



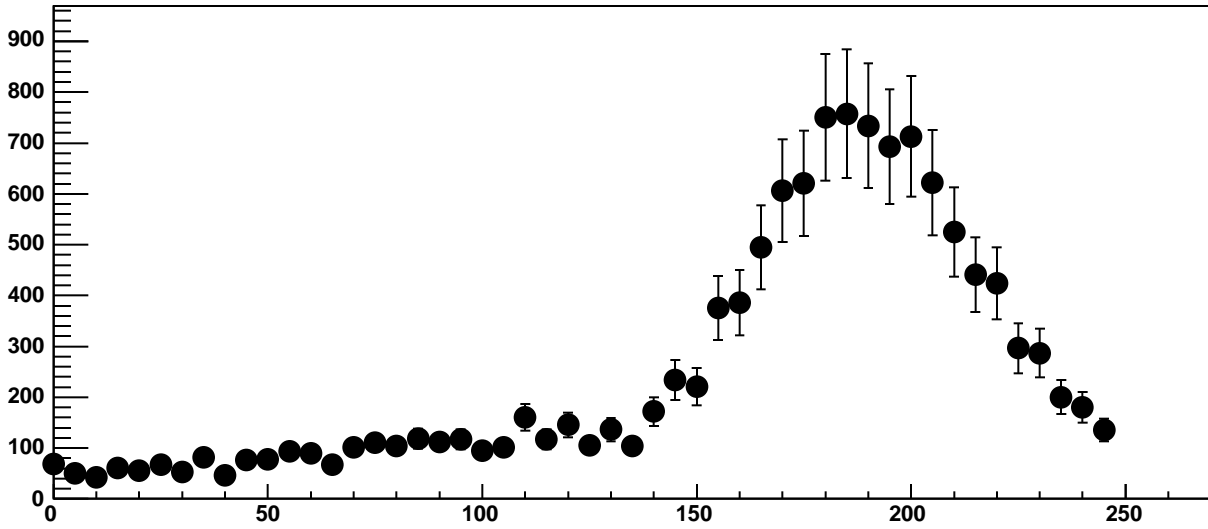


Chip 5, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

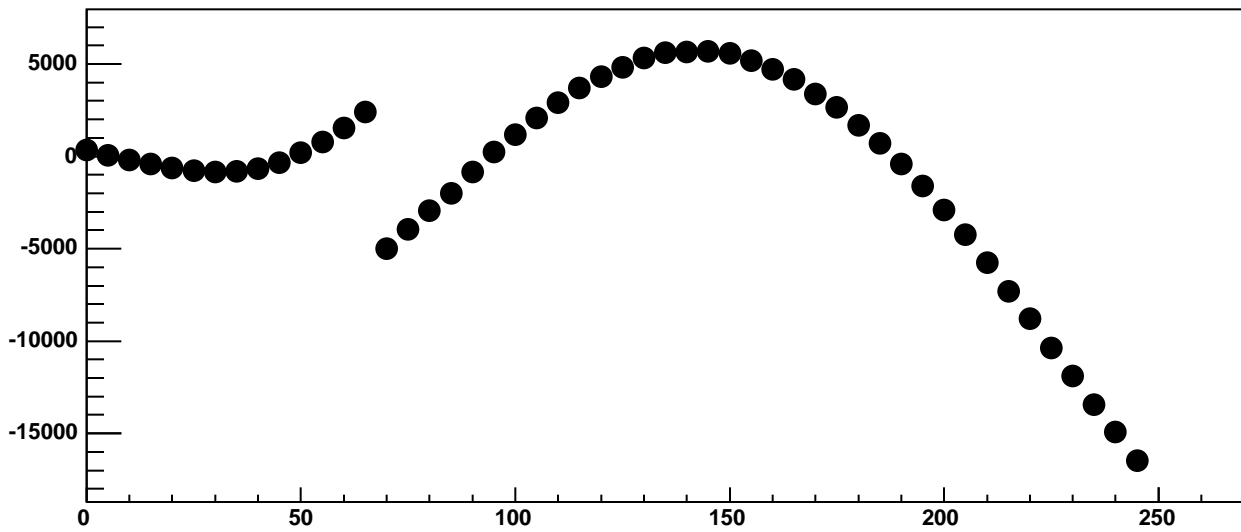


$\chi^2 / \text{ndf}$	6.555e+05 / 41
p0	3161 ± 0.8542
p1	65.01 ± 6.753e-05
p2	8351 ± 0.6985
p3	-34.06 ± 21.26
p4	73.52 ± 1.12

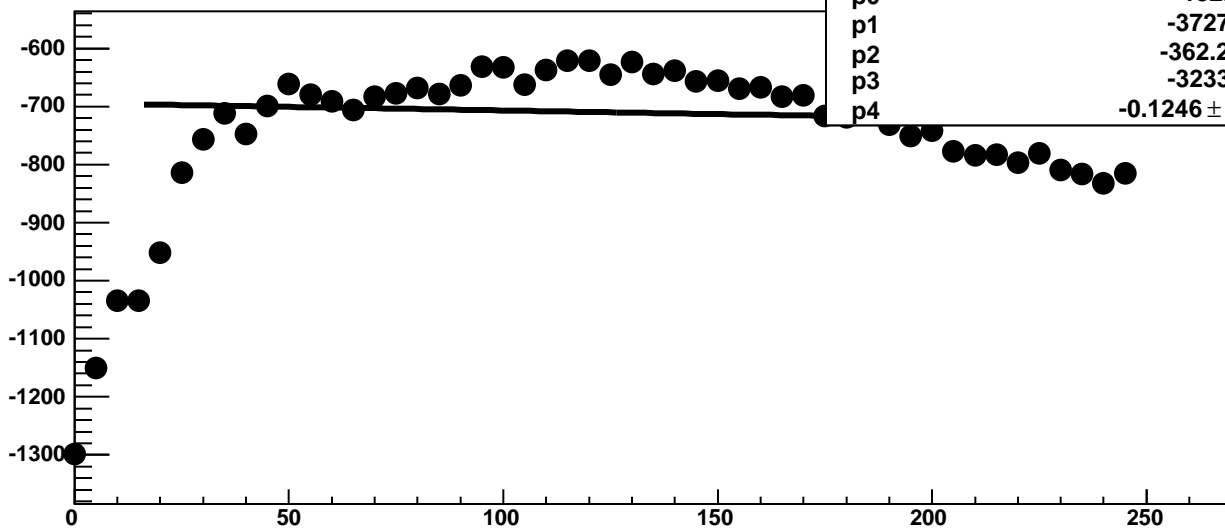
Chip 5, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

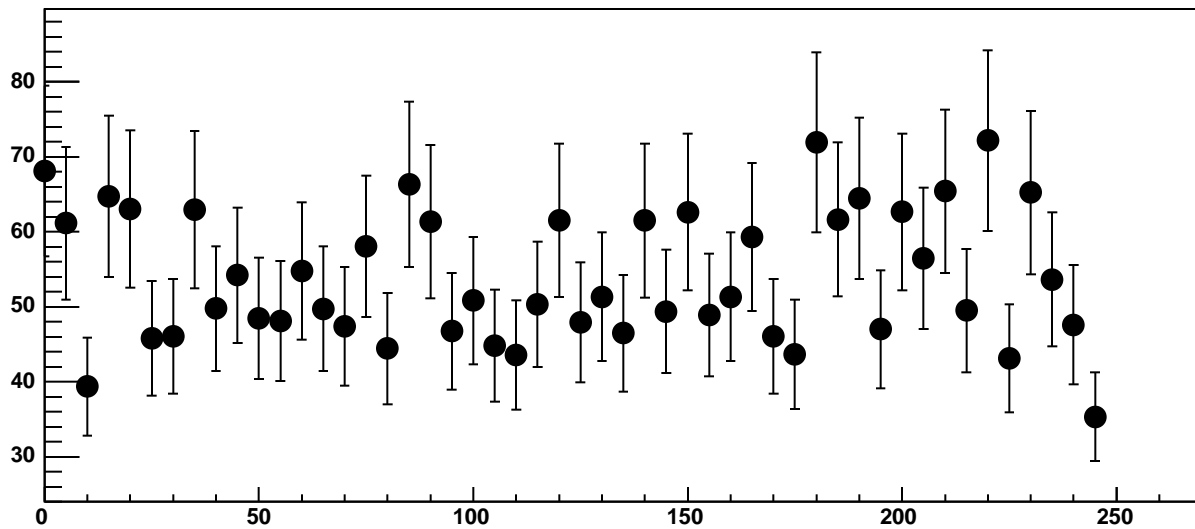


Chip 5, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

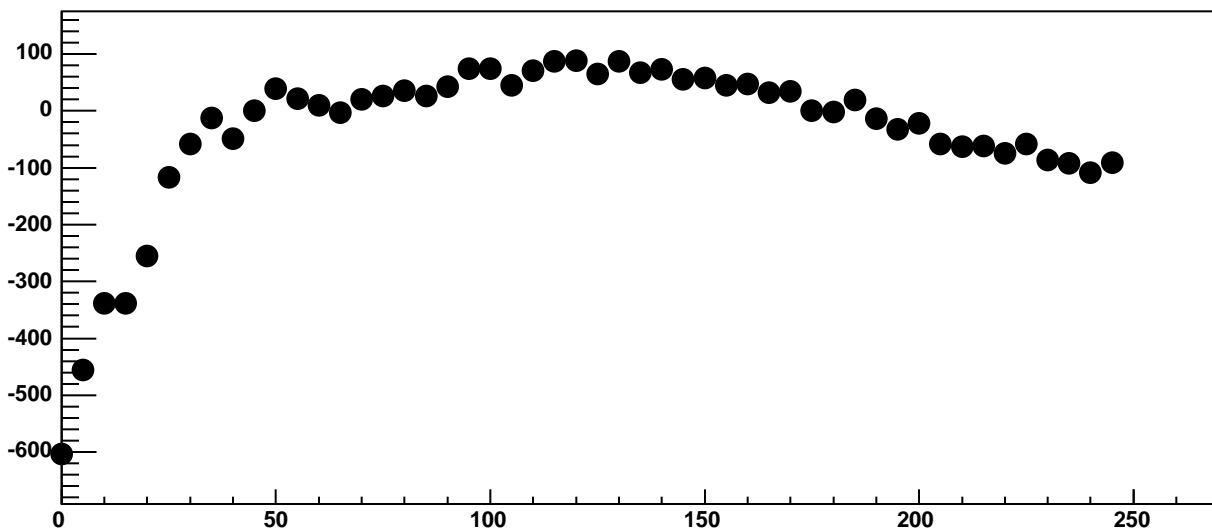


$\chi^2 / \text{ndf}$	1880 / 41
p0	$132.2 \pm 6.9$
p1	$-3727 \pm 93.02$
p2	$-362.2 \pm 8.217$
p3	$-3233 \pm 1244$
p4	$-0.1246 \pm 0.00179$

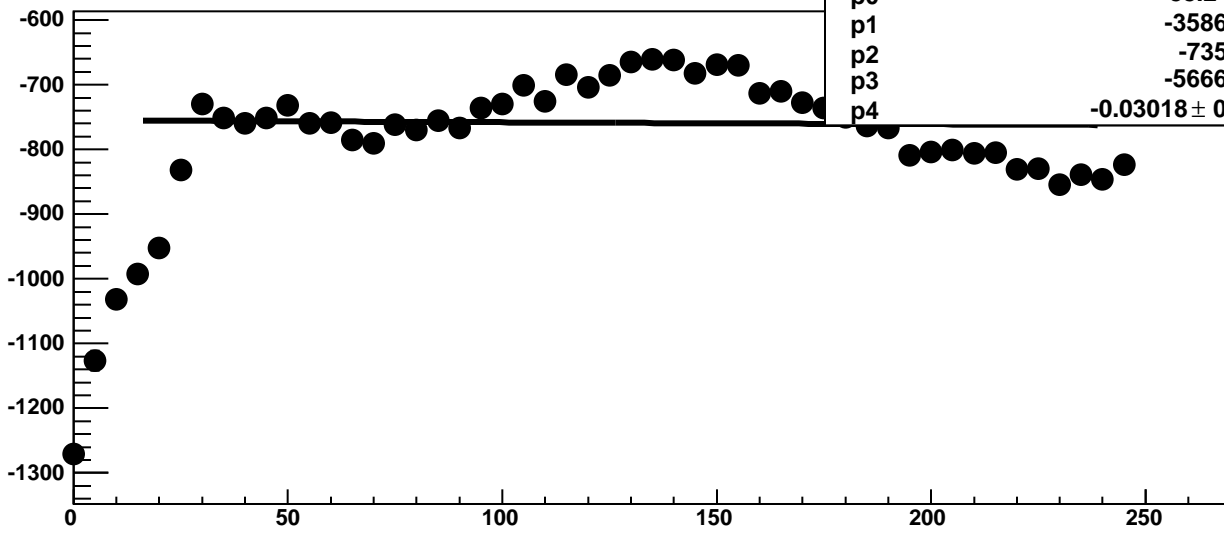
Chip 5, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



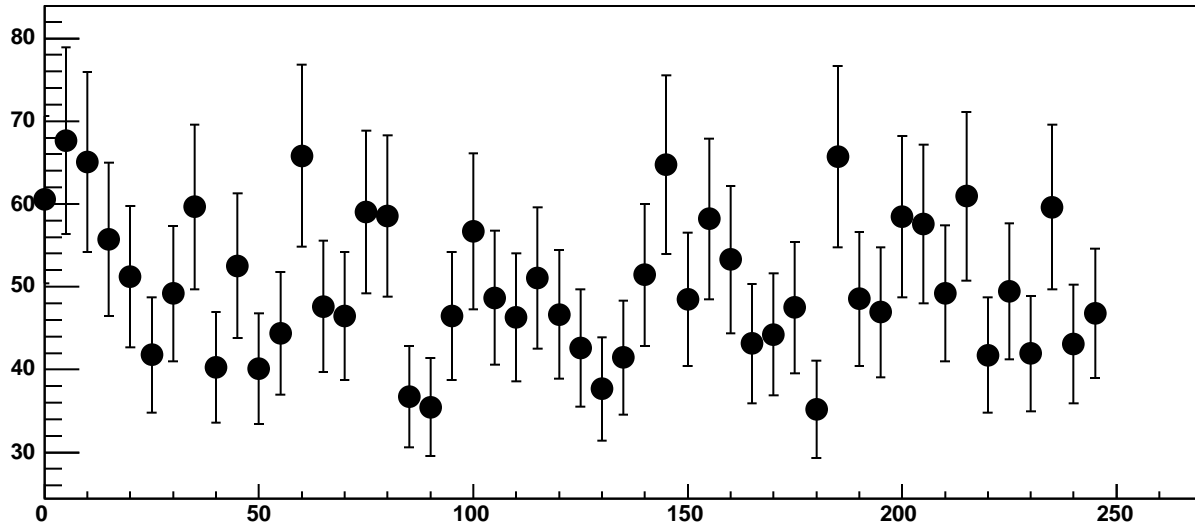
Chip 5, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold



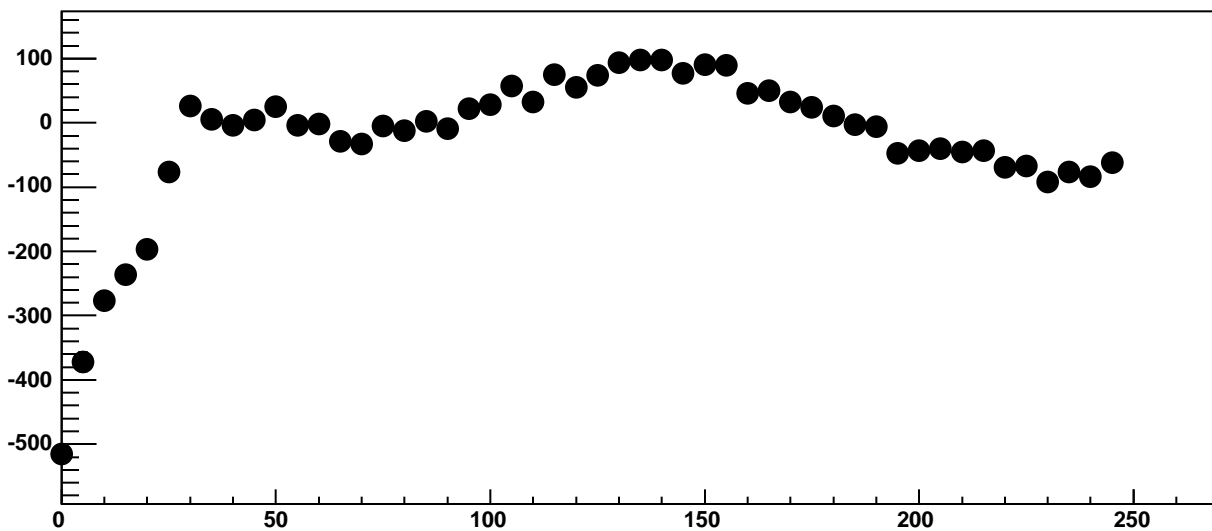
Chip 5, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold



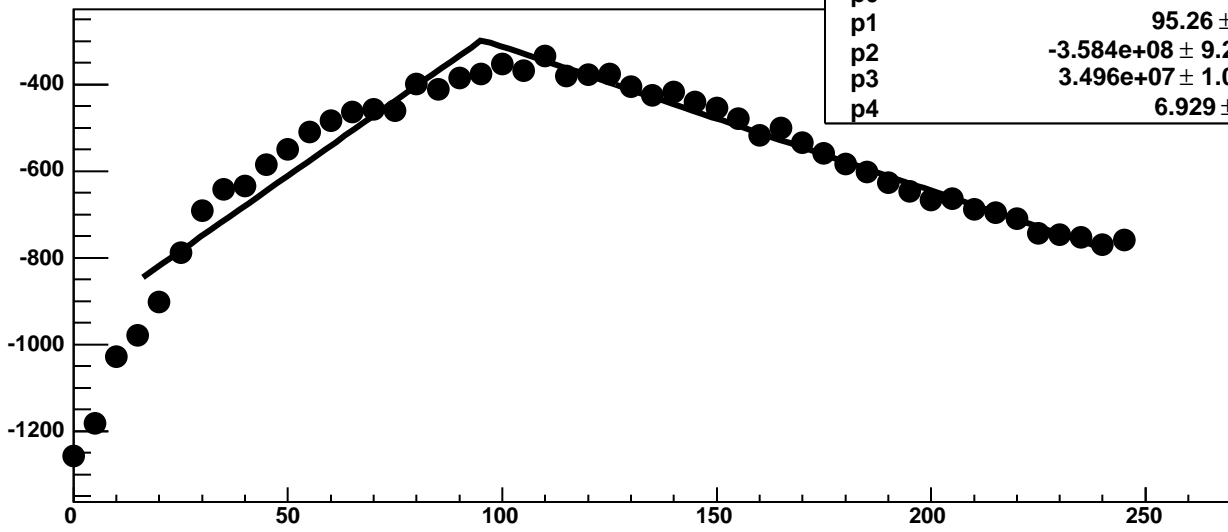
Chip 5, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

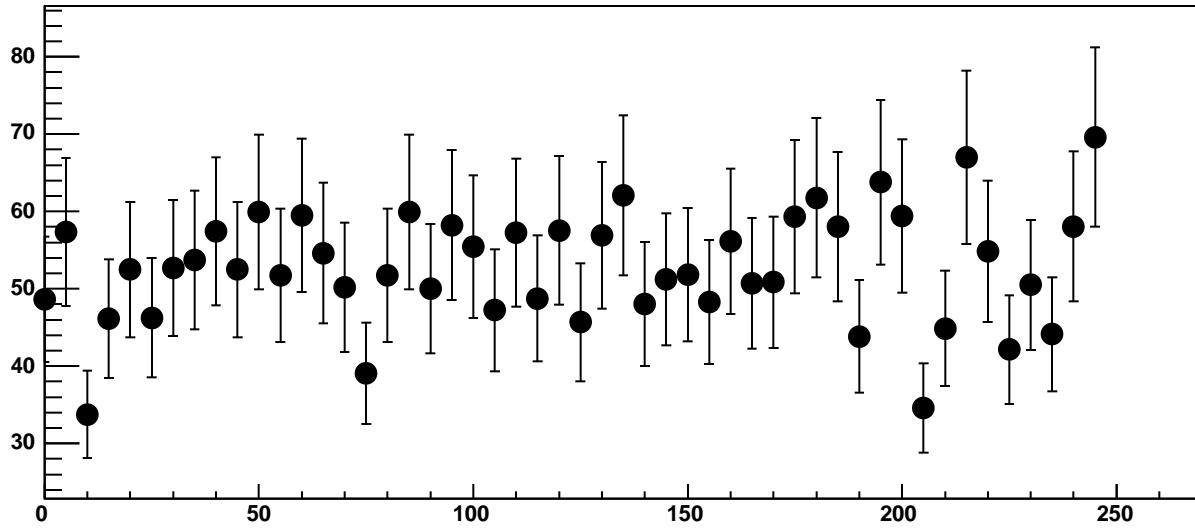


Chip 5, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

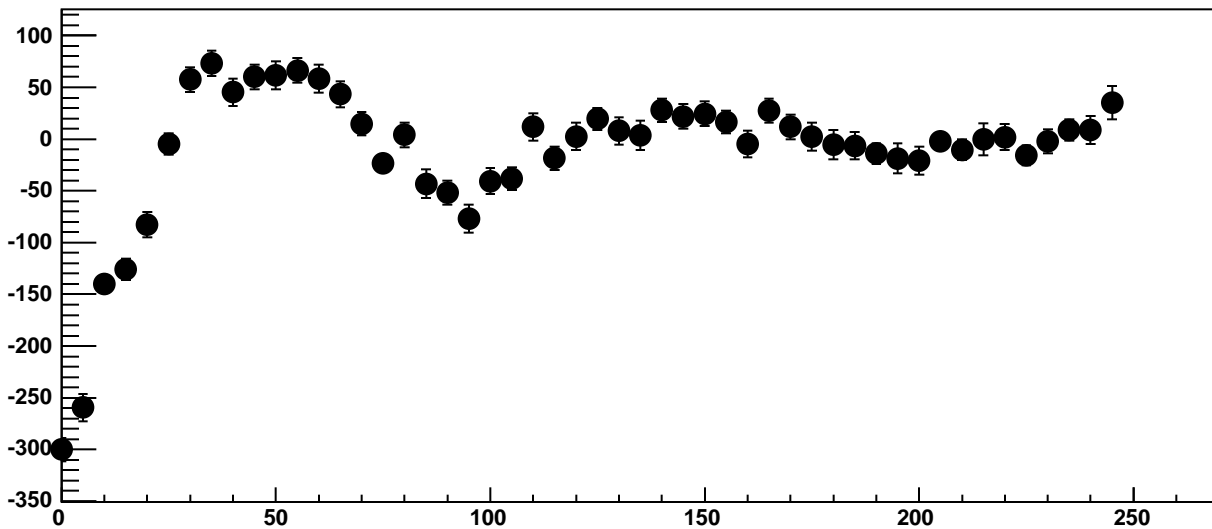


$\chi^2 / \text{ndf}$	501.2 / 41
p0	$-296.9 \pm 3.523$
p1	$95.26 \pm 0.6394$
p2	$-3.584\text{e}+08 \pm 9.266\text{e}+06$
p3	$3.496\text{e}+07 \pm 1.091\text{e}+06$
p4	$6.929 \pm 0.1047$

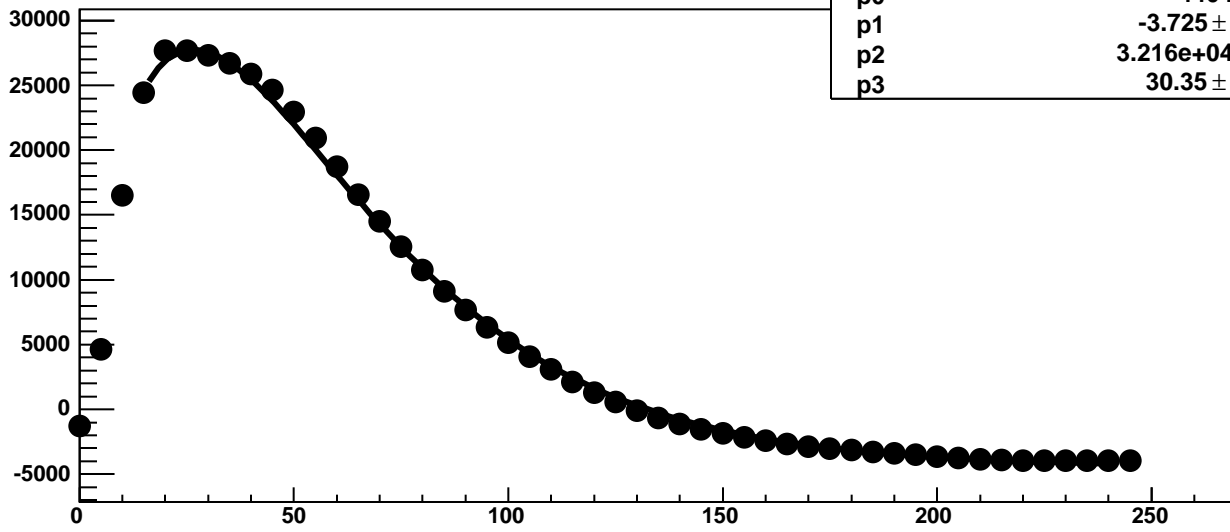
Chip 5, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

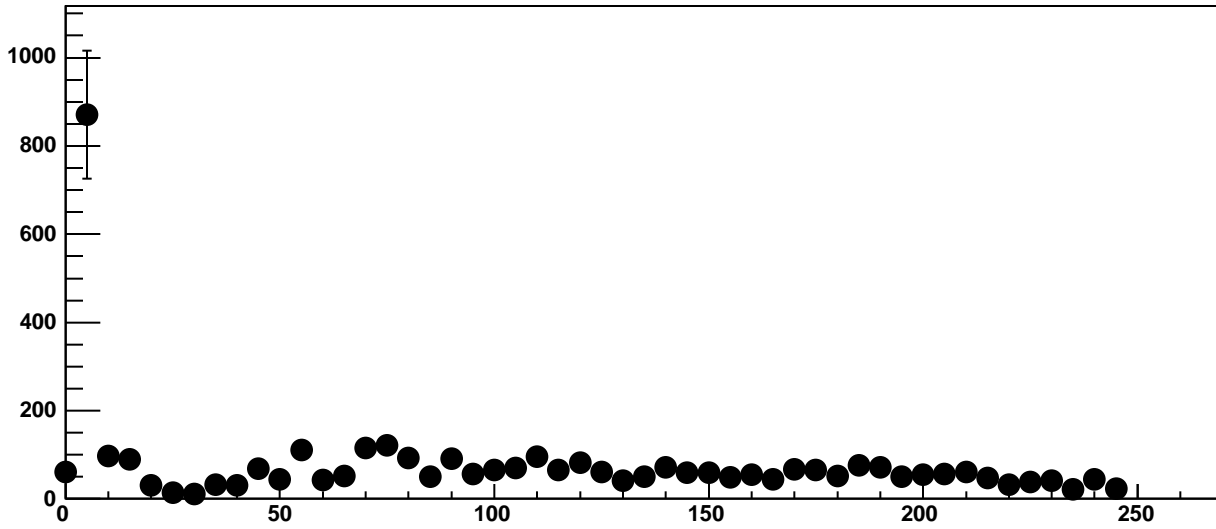


Chip 5, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

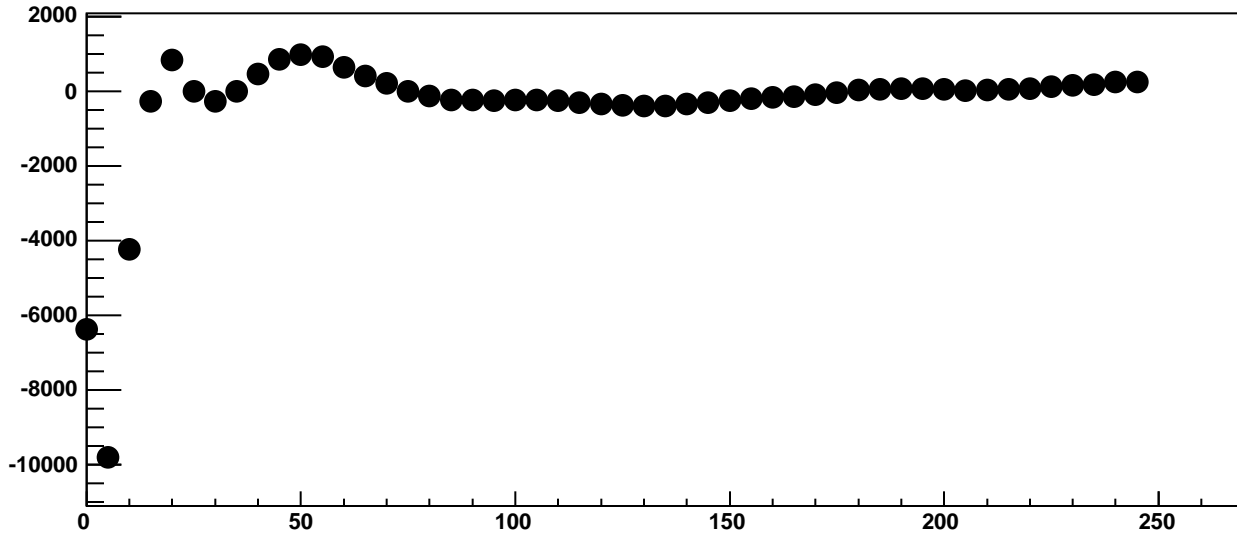


$\chi^2 / \text{ndf}$	5.741e+04 / 42
p0	-4404 ± 2.952
p1	-3.725 ± 0.01933
p2	3.216e+04 ± 3.436
p3	30.35 ± 0.01053

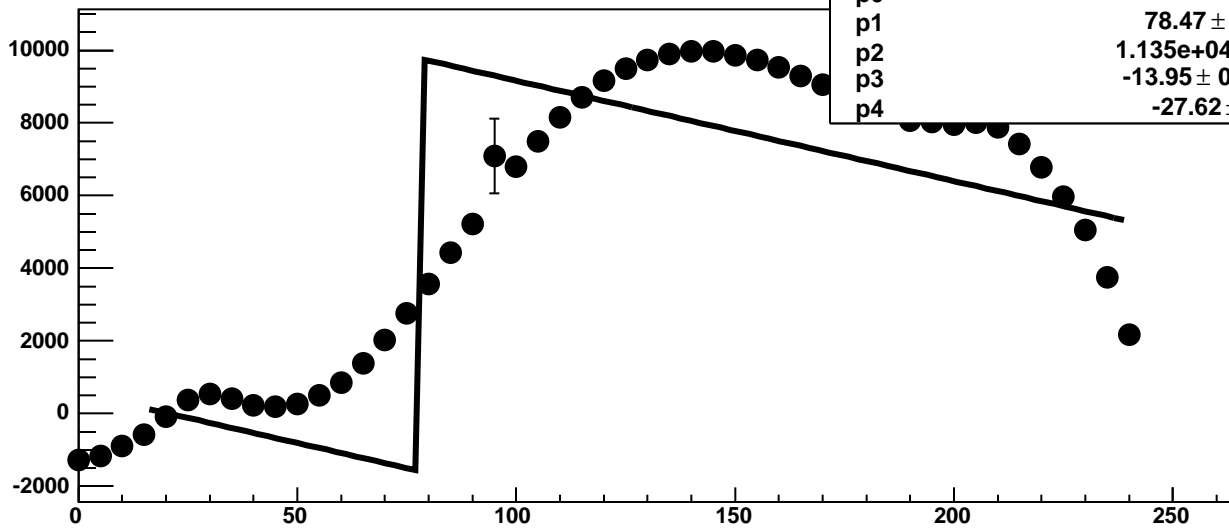
Chip 5, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold

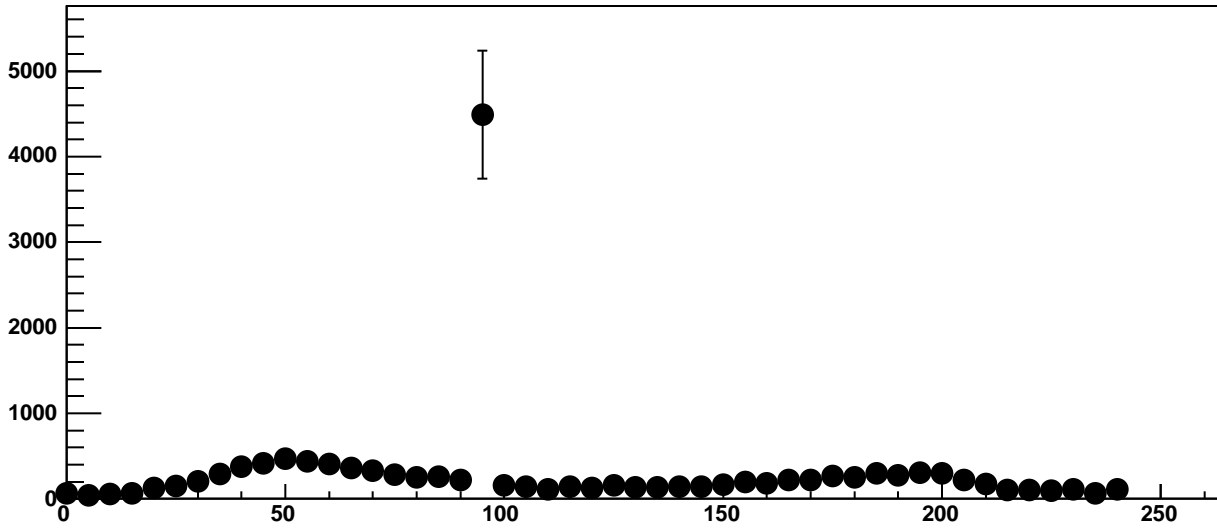


Chip 5, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

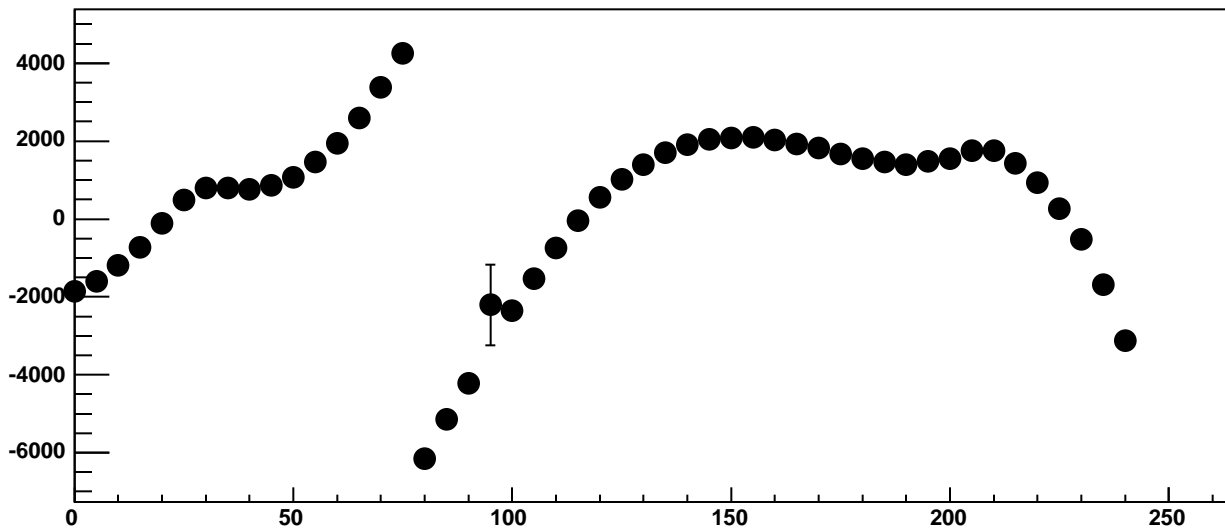


$\chi^2 / \text{ndf}$	1.045e+05 / 41
p0	-1597 ± 11.78
p1	78.47 ± 0.02812
p2	1.135e+04 ± 20.97
p3	-13.95 ± 0.003305
p4	-27.62 ± 0.1114

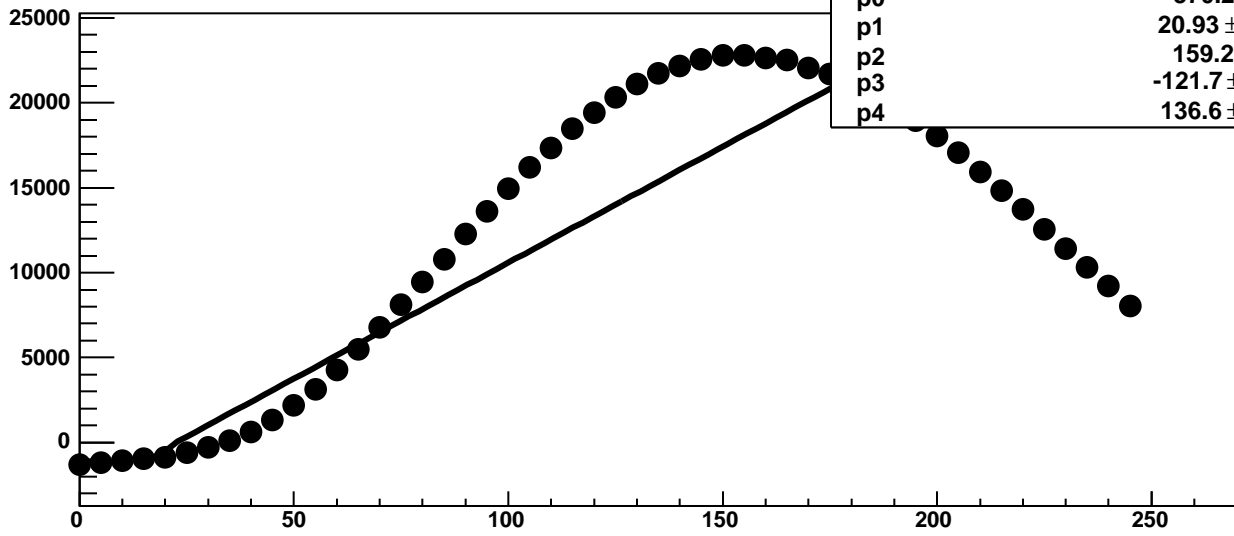
Chip 5, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

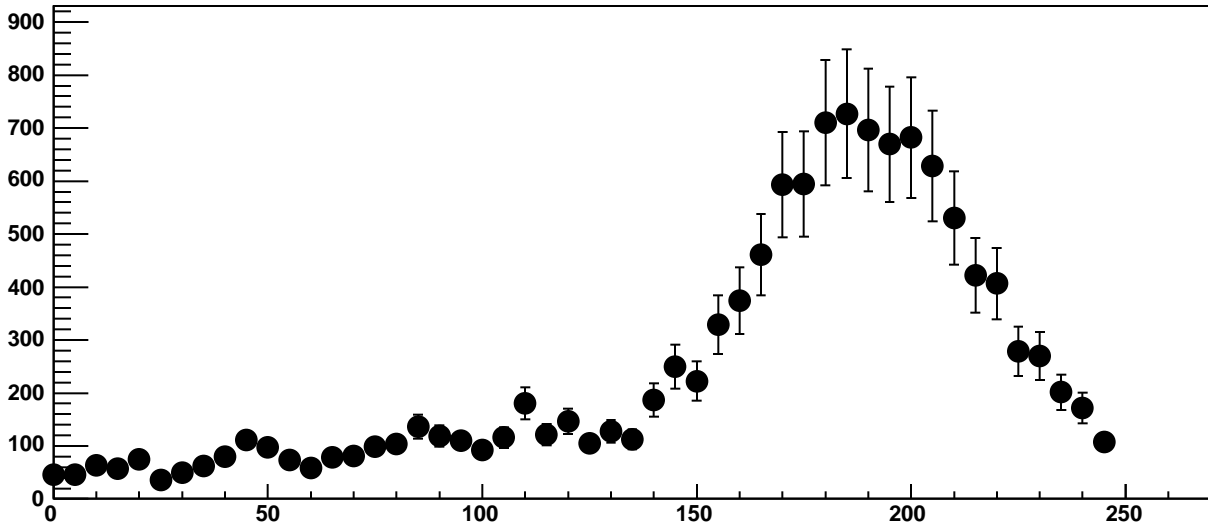


Chip 5, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

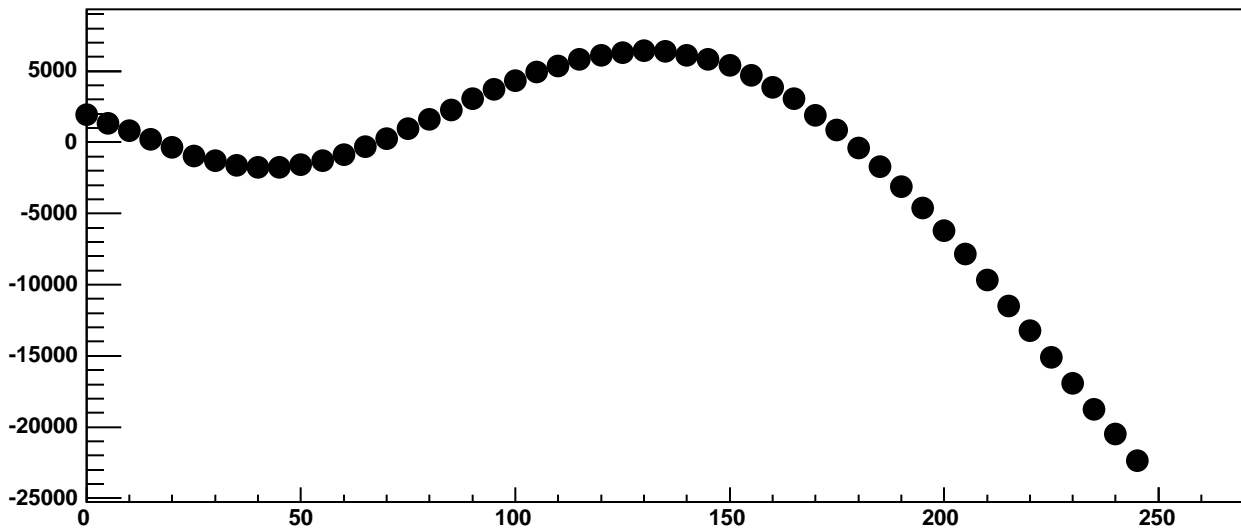


$\chi^2 / \text{ndf}$	1.124e+06 / 41
p0	-370.2 ± 1.398
p1	20.93 ± 0.0366
p2	159.2 ± 1.388
p3	-121.7 ± 0.1163
p4	136.6 ± 0.0783

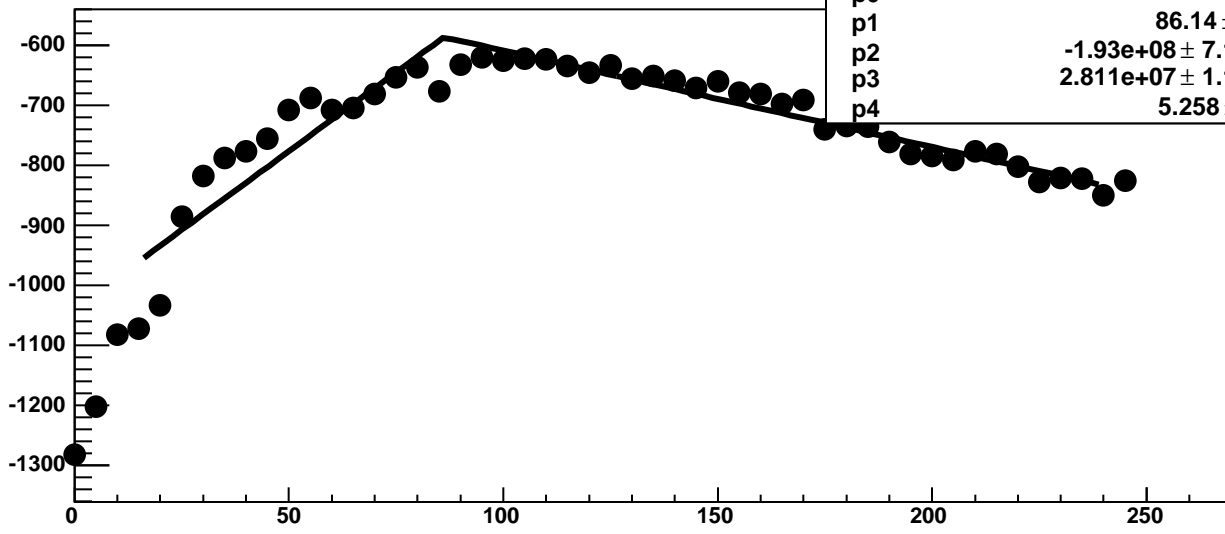
Chip 5, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



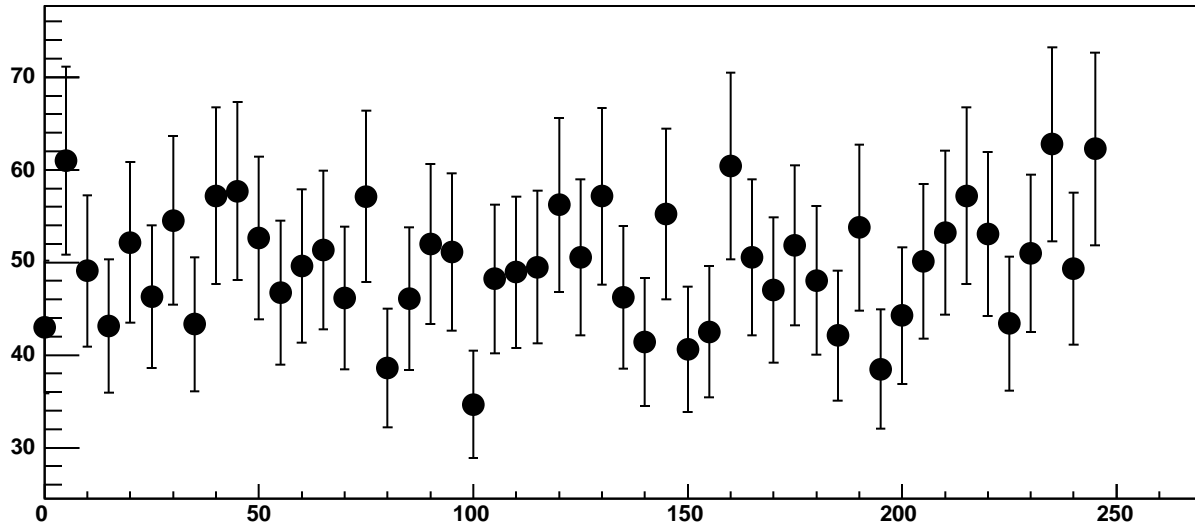
Chip 5, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



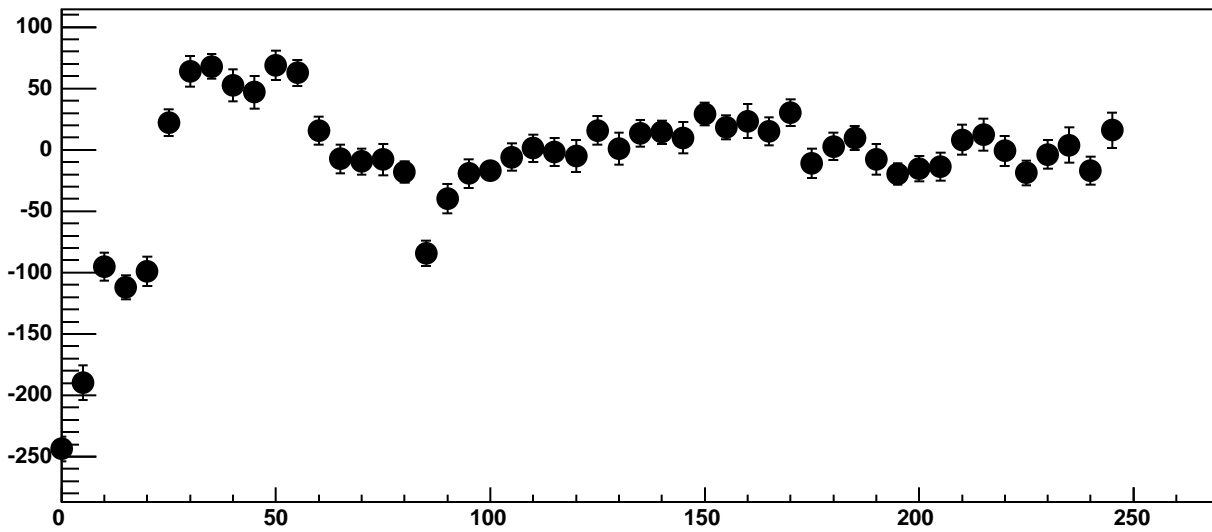
Chip 5, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 5, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

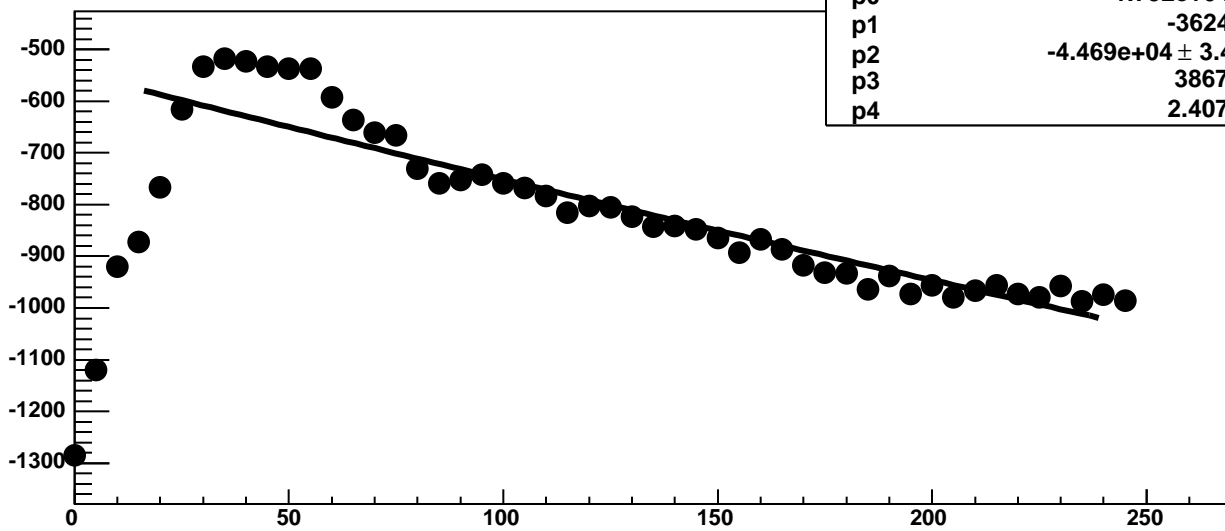


Chip 5, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



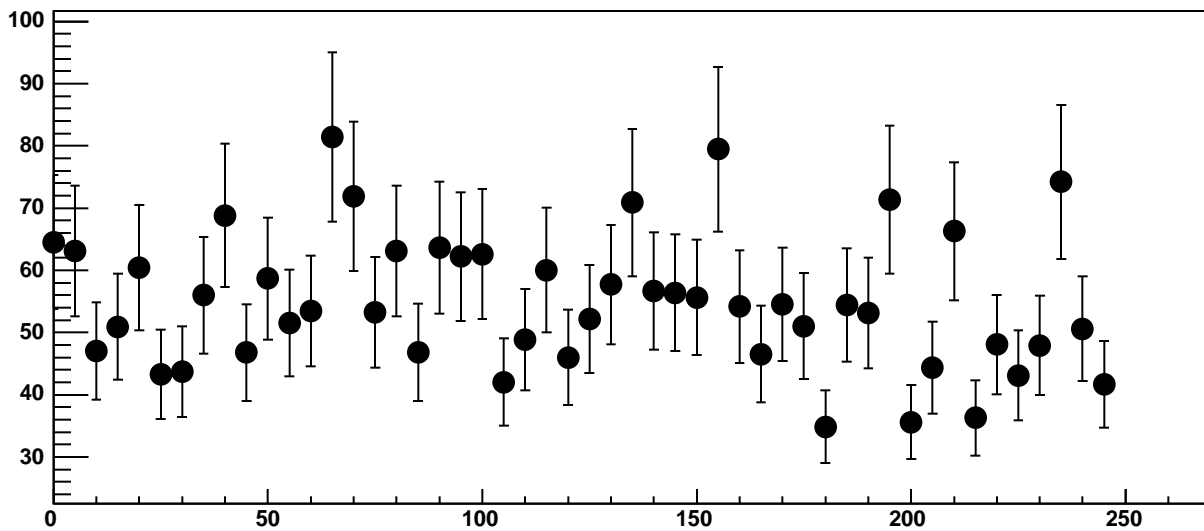


Chip 5, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold

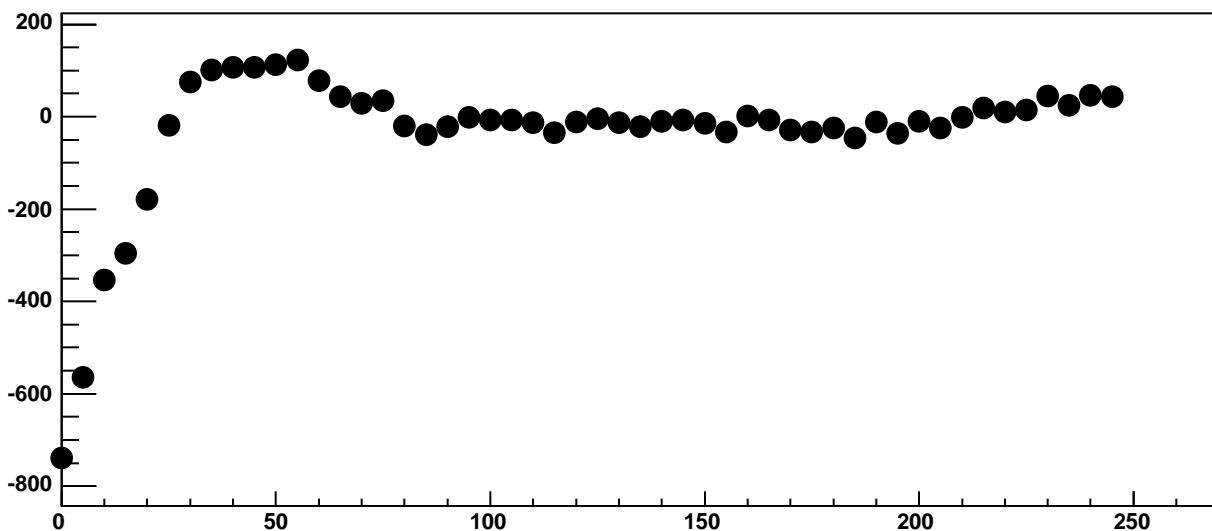


$\chi^2 / \text{ndf}$	1432 / 41
p0	$1.792\text{e}+04 \pm 7921$
p1	$-3624 \pm 117.5$
p2	$-4.469\text{e}+04 \pm 3.427\text{e}+04$
p3	$3867 \pm 6.506$
p4	$2.407 \pm 3.493$

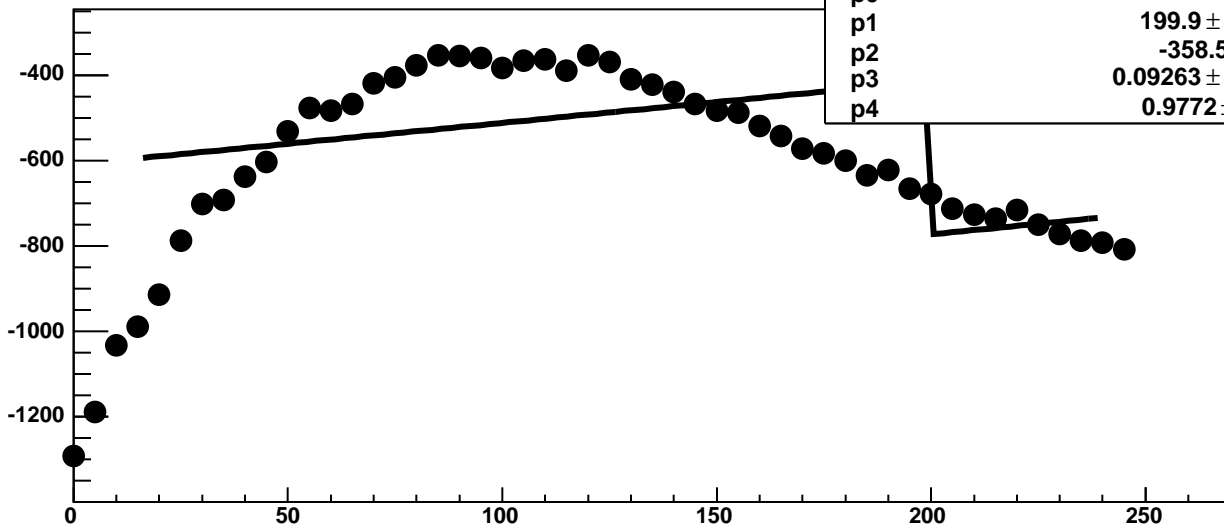
Chip 5, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



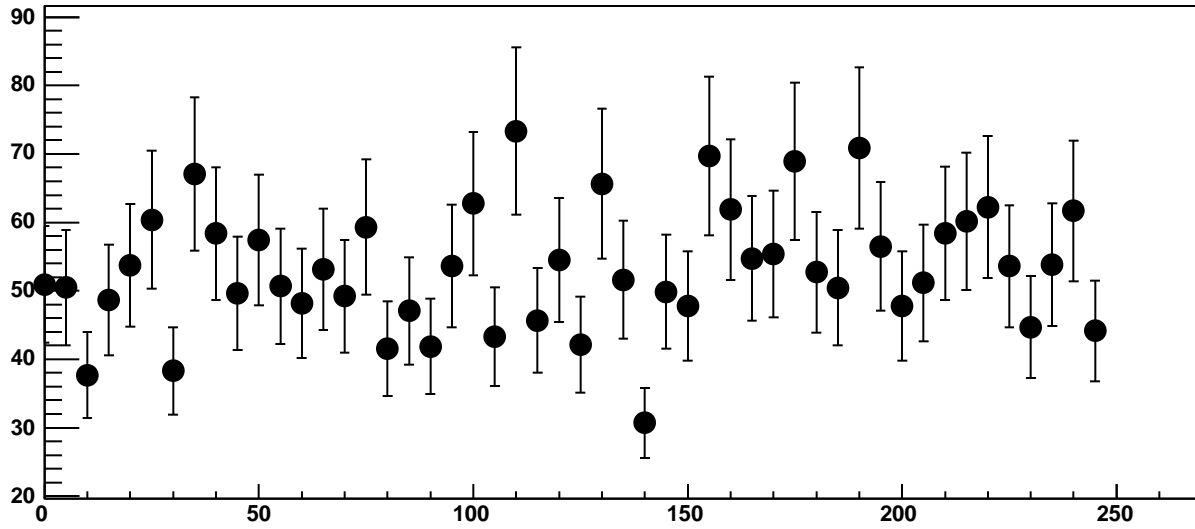
Chip 5, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold



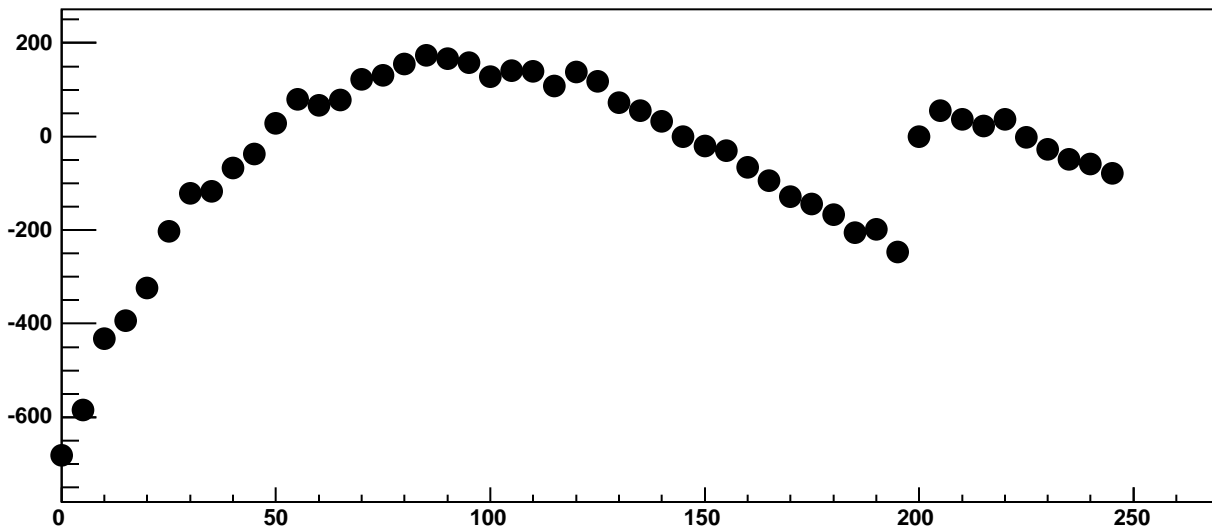
Chip 5, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold



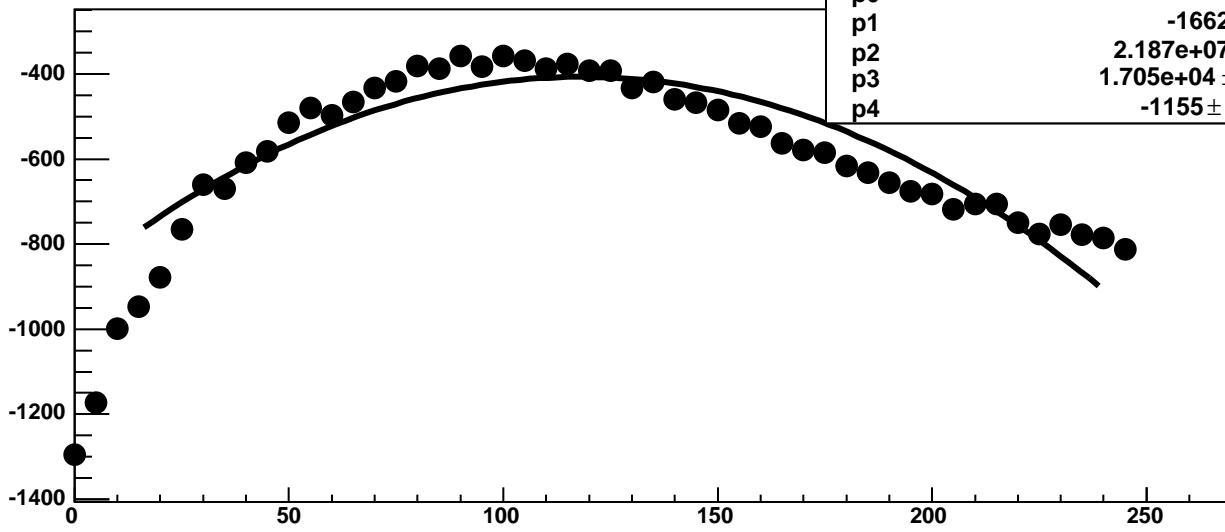
Chip 5, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

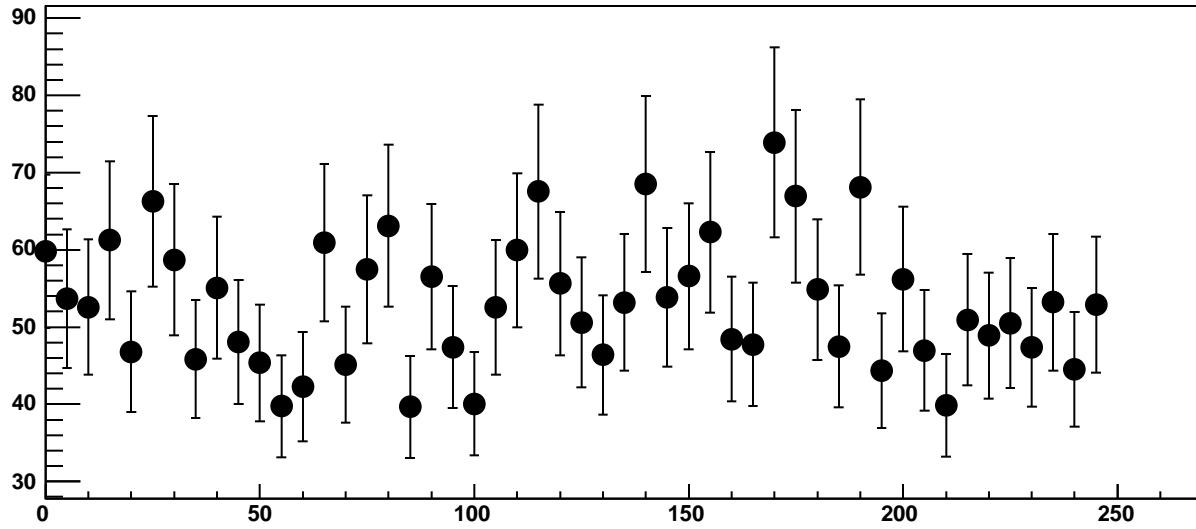


Chip 5, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

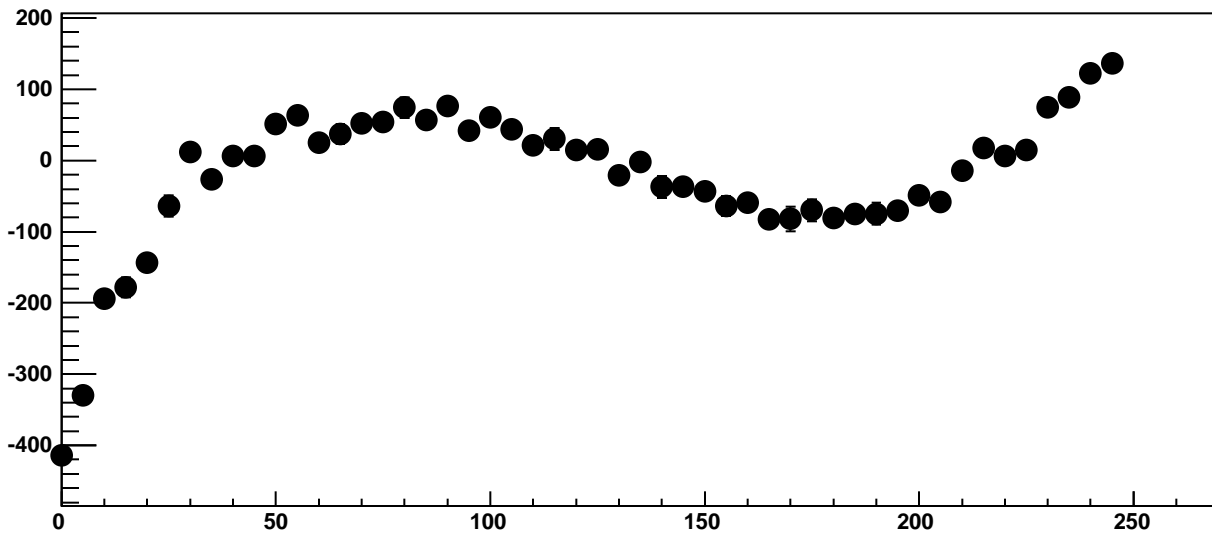


$\chi^2 / \text{ndf}$	1308 / 41
p0	$-1.117\text{e}+05 \pm 23.45$
p1	$-1662 \pm 0.419$
p2	$2.187\text{e}+07 \pm 235.7$
p3	$1.705\text{e}+04 \pm 0.1939$
p4	$-1155 \pm 0.01312$

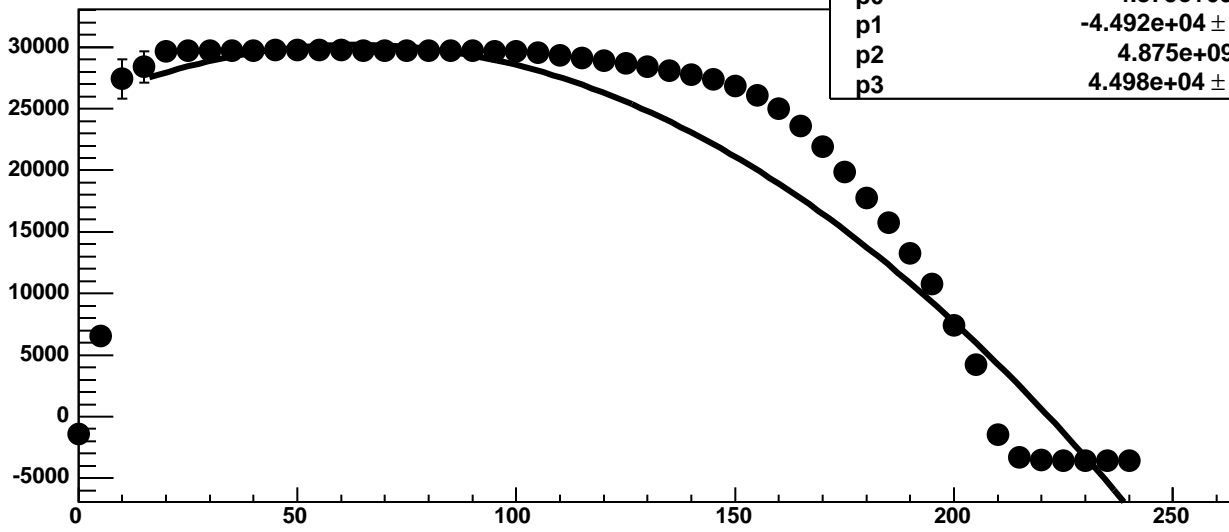
Chip 5, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

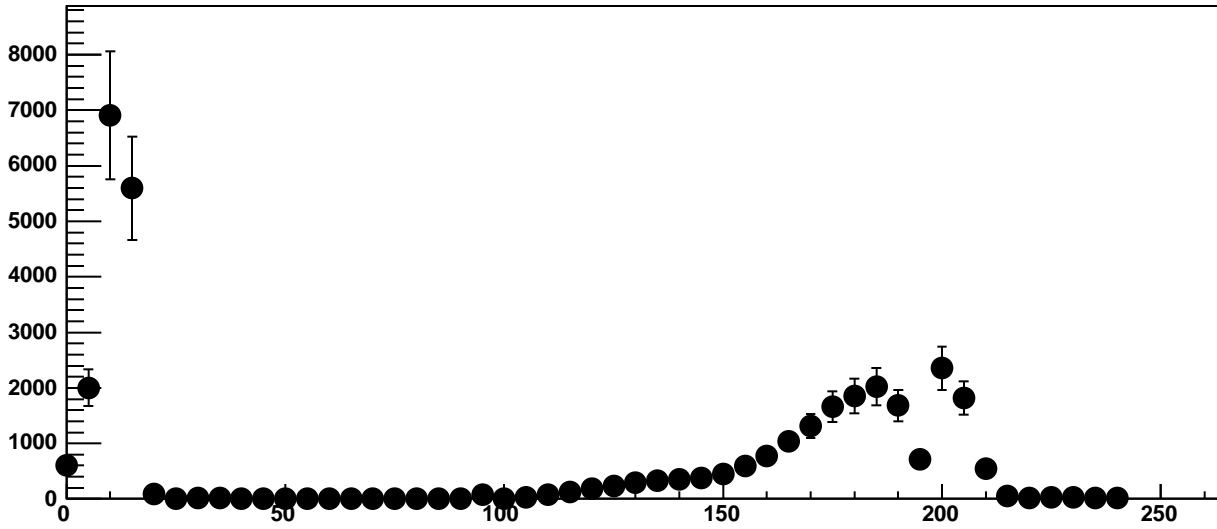


Chip 5, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

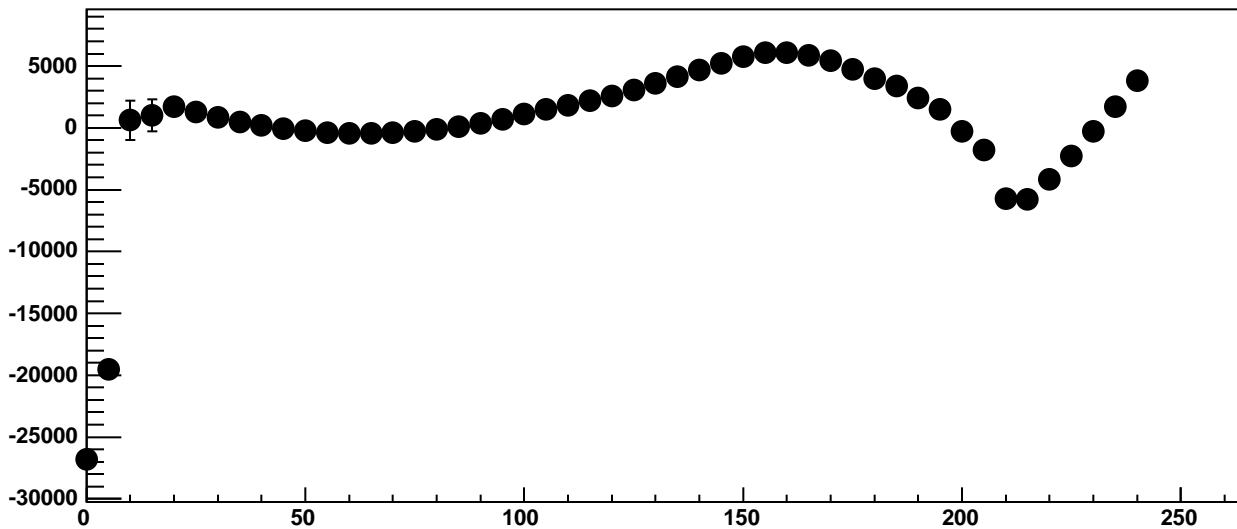


$\chi^2 / \text{ndf}$	3.49e+06 / 42
p0	-4.875e+09 $\pm$ 5.768
p1	-4.492e+04 $\pm$ 0.05833
p2	4.875e+09 $\pm$ 5.768
p3	4.498e+04 $\pm$ 0.05817

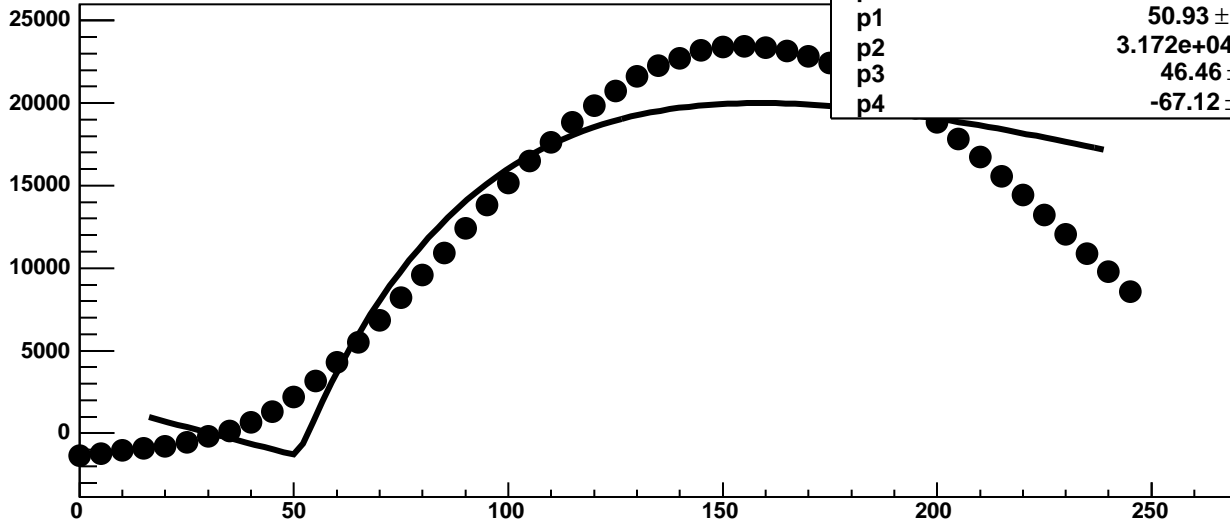
Chip 5, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold

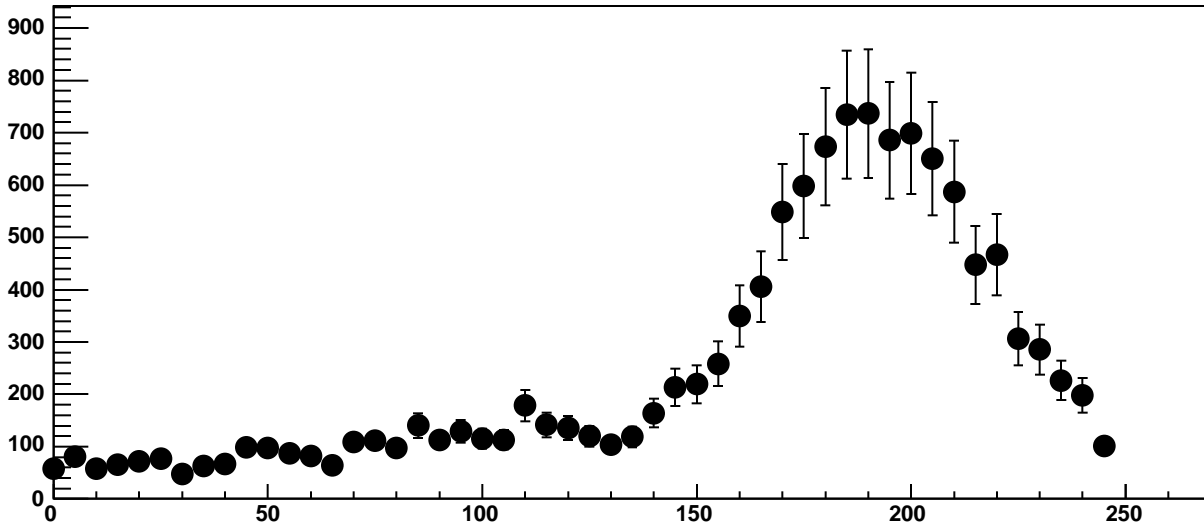


Chip 5, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

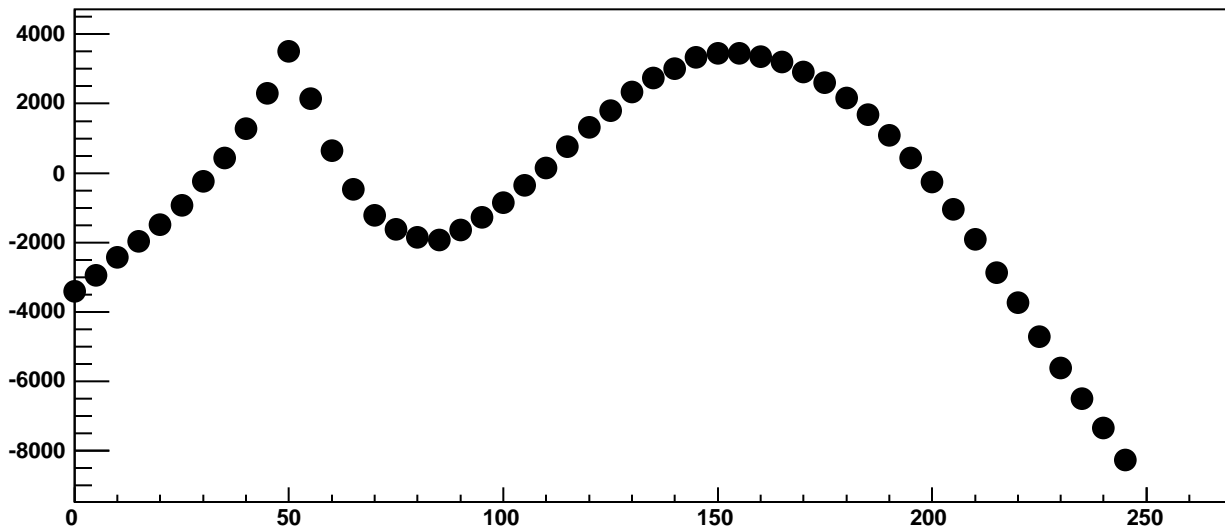


$\chi^2 / \text{ndf}$	2.143e+05 / 41
p0	-1368 ± 8.241
p1	50.93 ± 0.02691
p2	3.172e+04 ± 66.18
p3	46.46 ± 0.1057
p4	-67.12 ± 0.3496

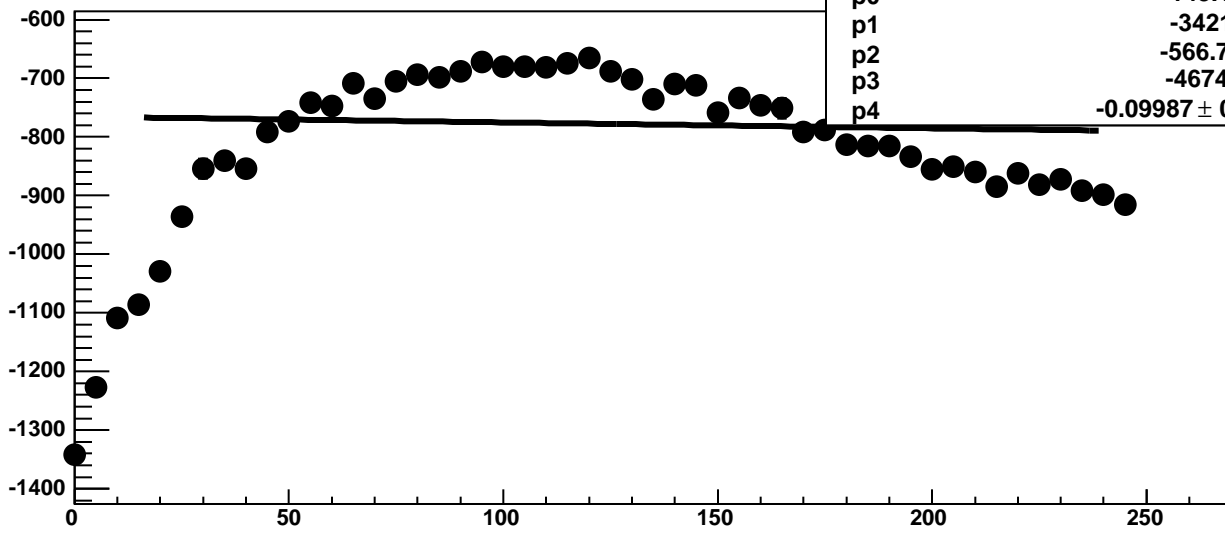
Chip 5, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

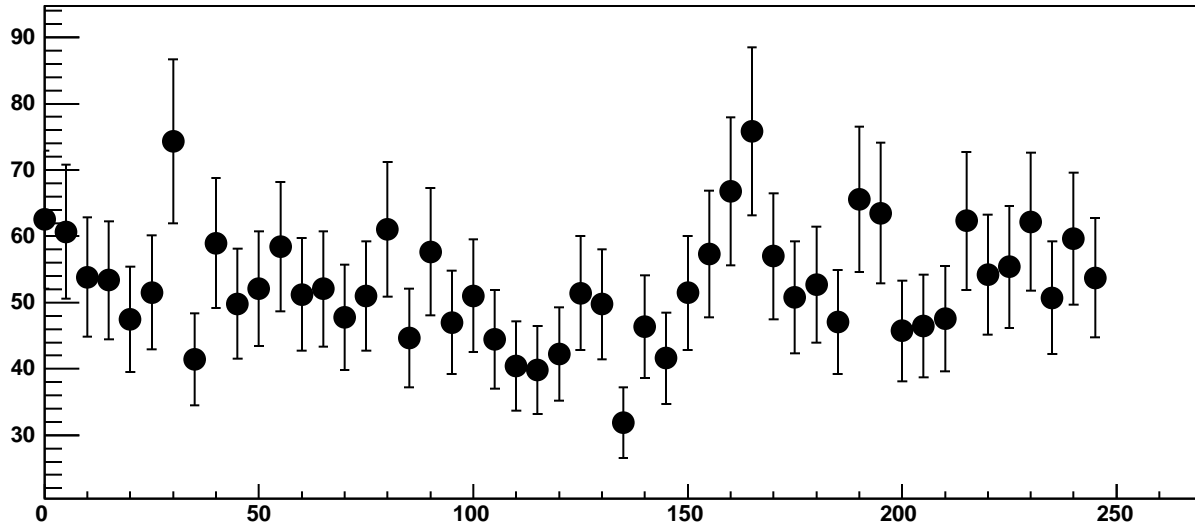


Chip 5, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

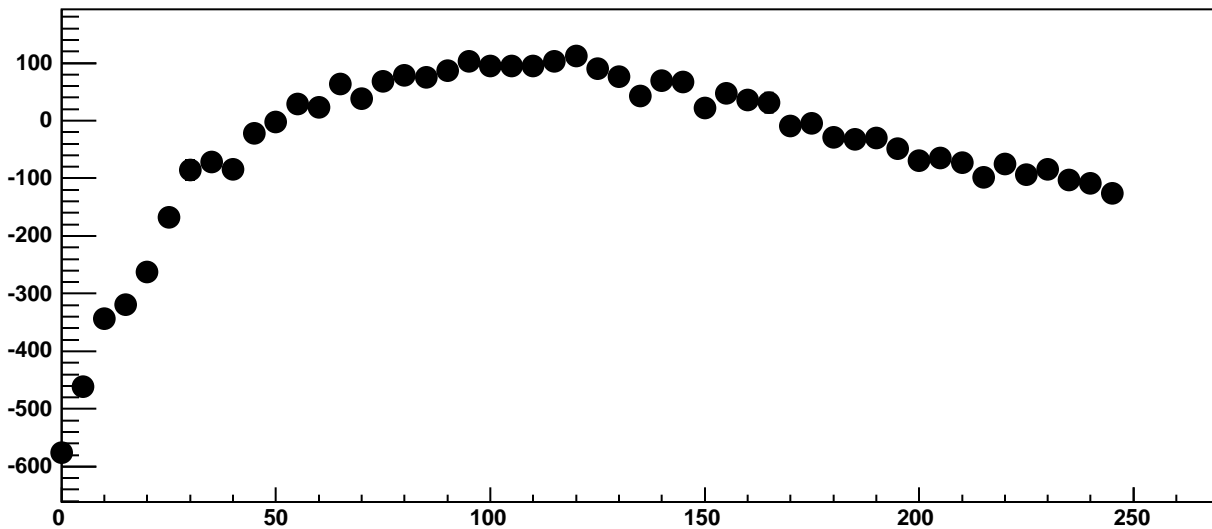


$\chi^2 / \text{ndf}$	3129 / 41
p0	$143.1 \pm 5.679$
p1	$-3421 \pm 122.2$
p2	$-566.7 \pm 7.603$
p3	$-4674 \pm 870.3$
p4	$-0.09987 \pm 0.001601$

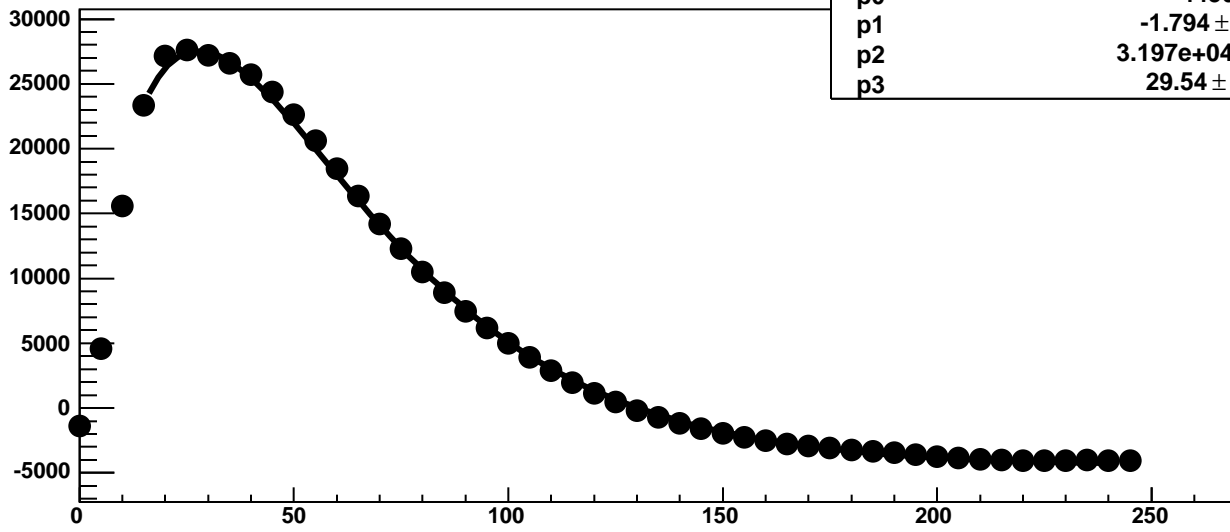
Chip 5, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



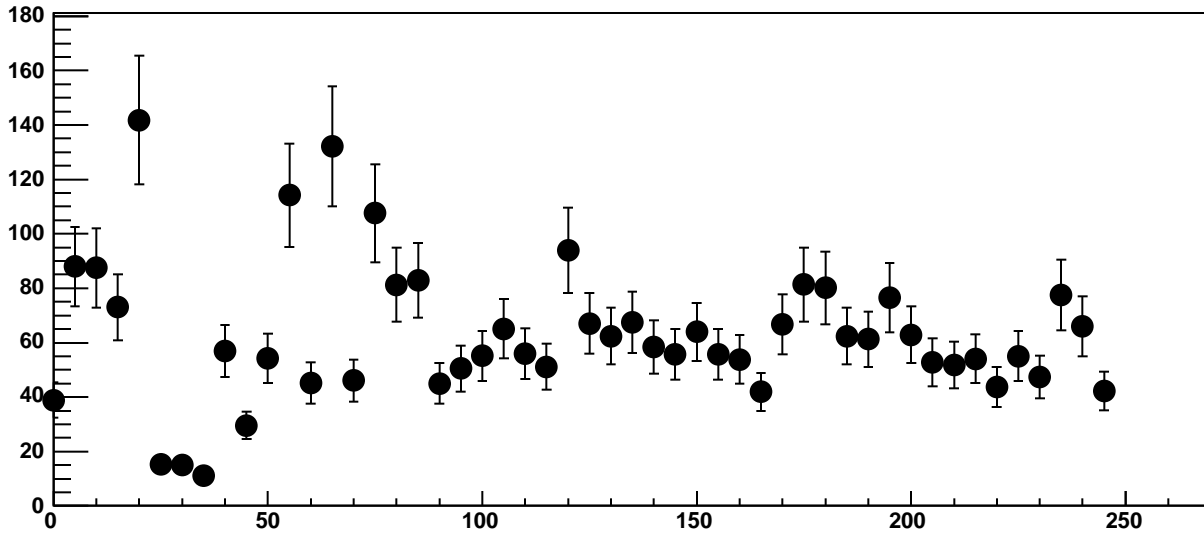
Chip 5, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold



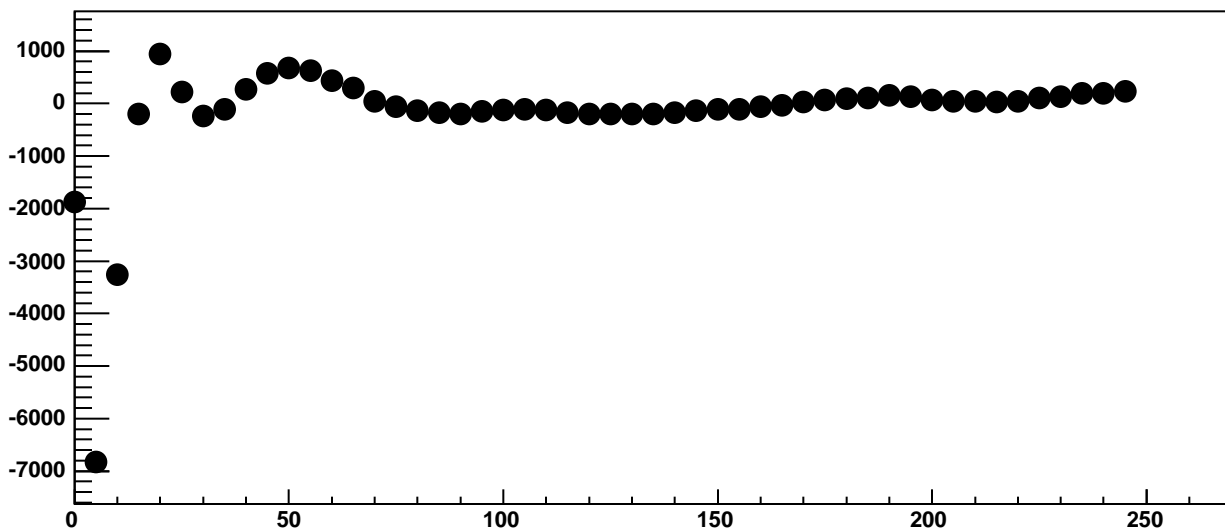
Chip 5, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold



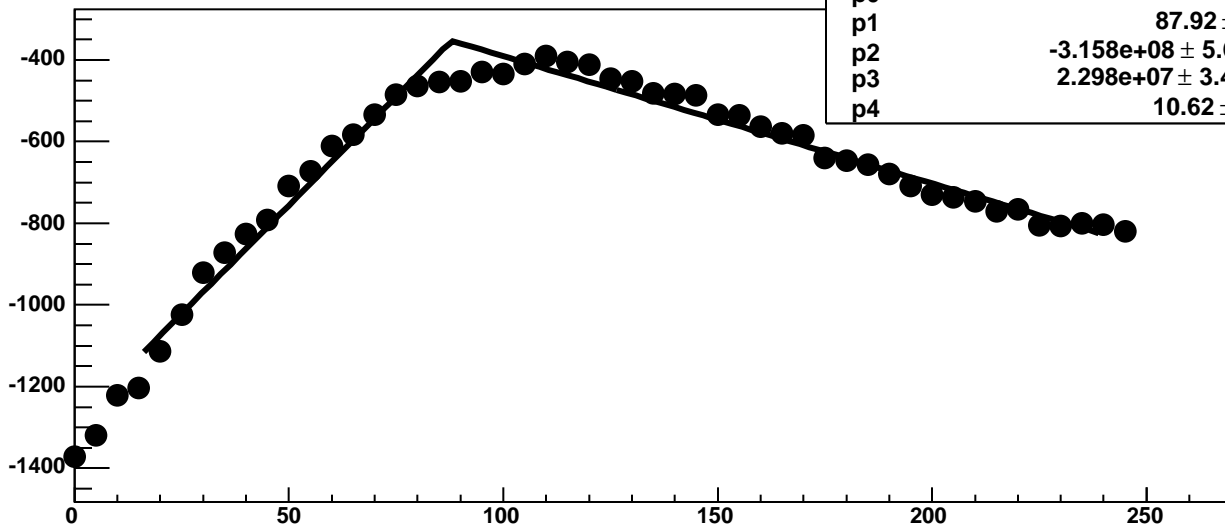
Chip 5, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold

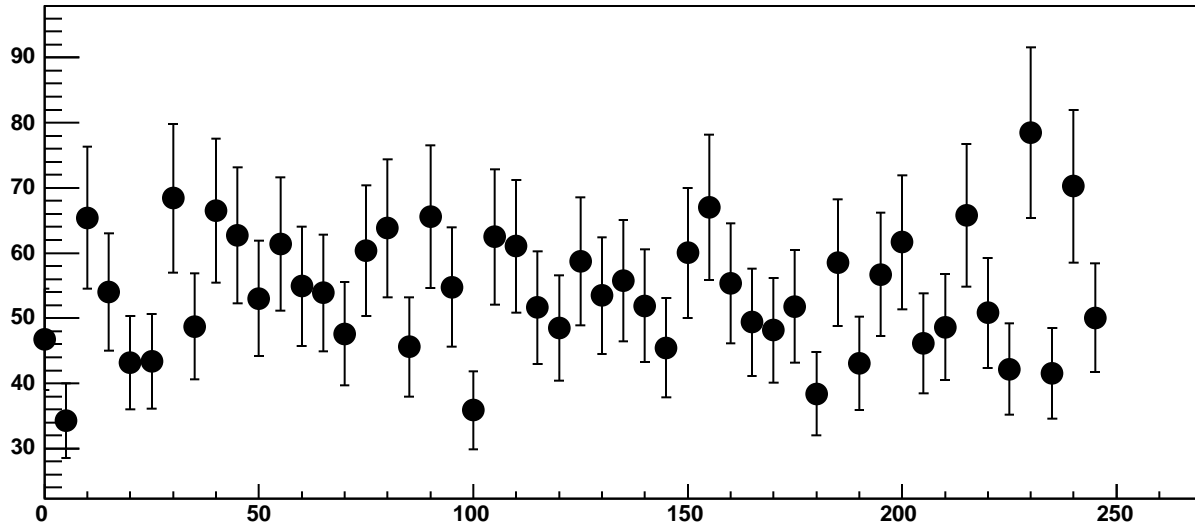


Chip 5, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

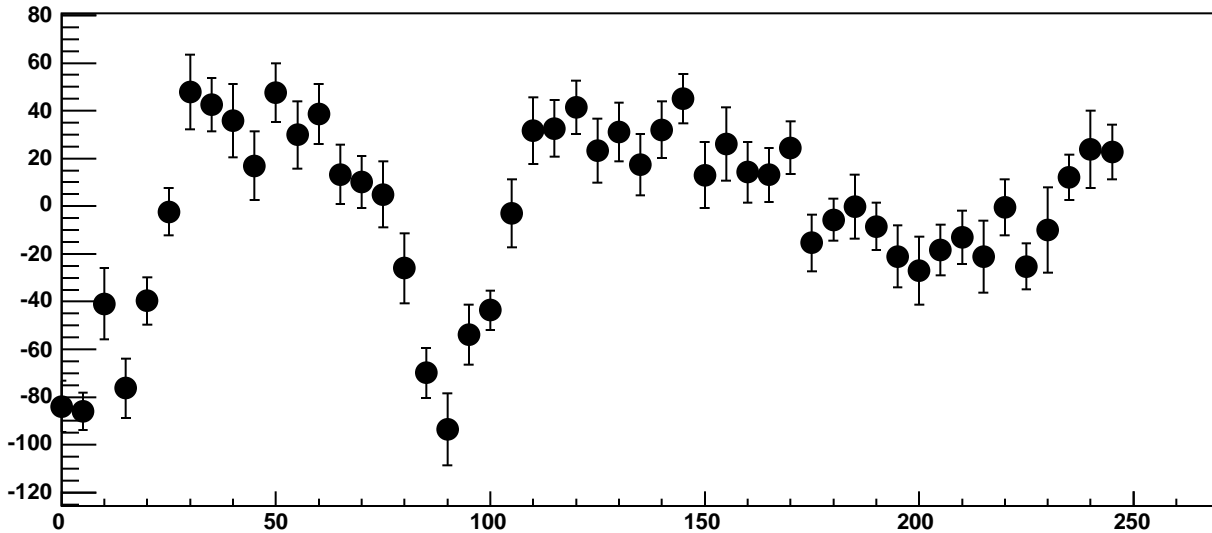


$\chi^2 / \text{ndf}$	350.2 / 41
p0	$-353.1 \pm 3.578$
p1	$87.92 \pm 0.5549$
p2	$-3.158\text{e}+08 \pm 5.604\text{e}+06$
p3	$2.298\text{e}+07 \pm 3.459\text{e}+05$
p4	$10.62 \pm 0.1386$

Chip 5, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

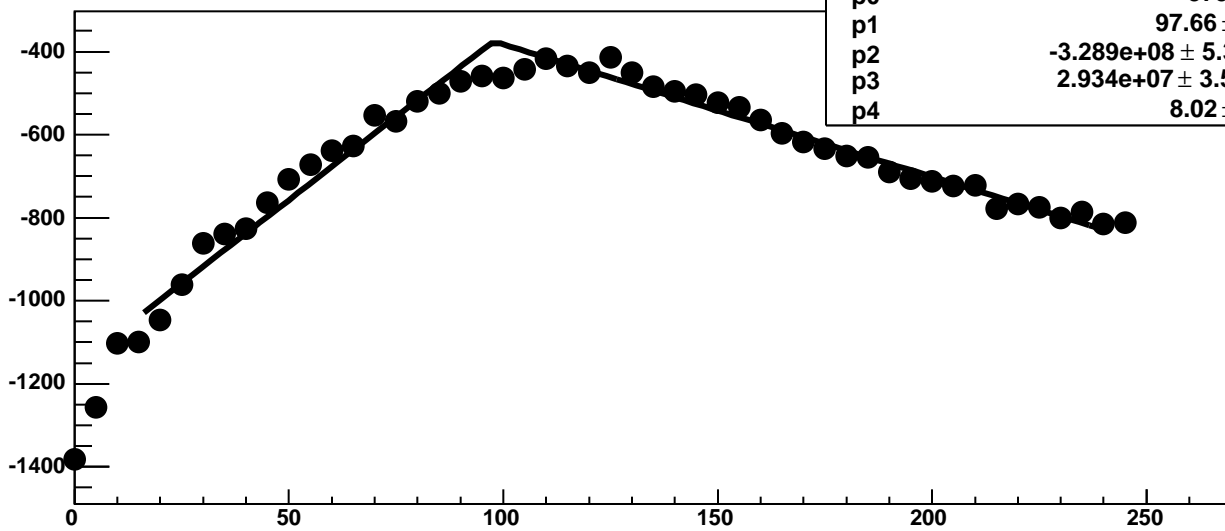


Chip 5, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

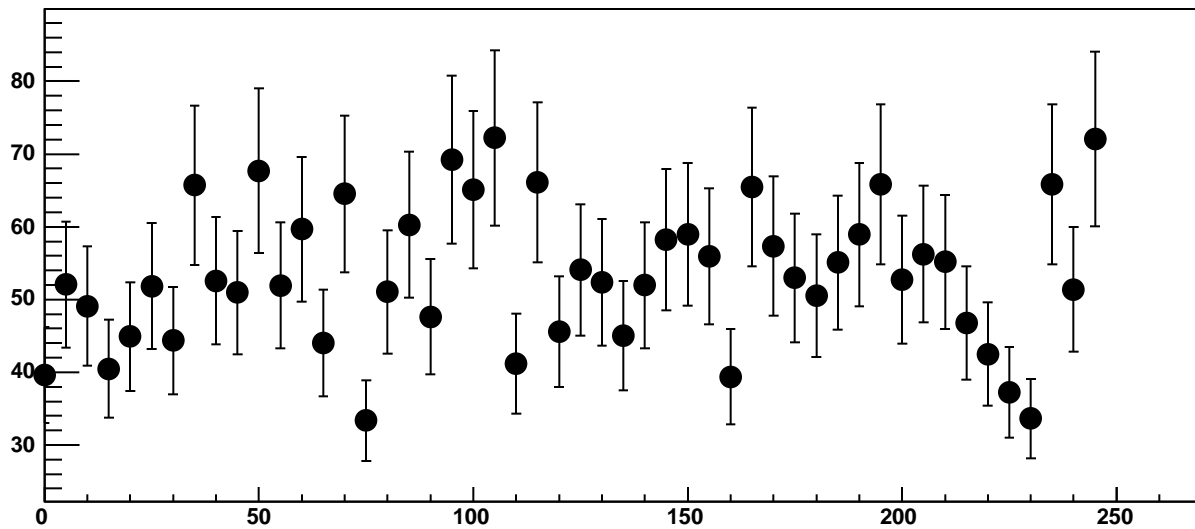




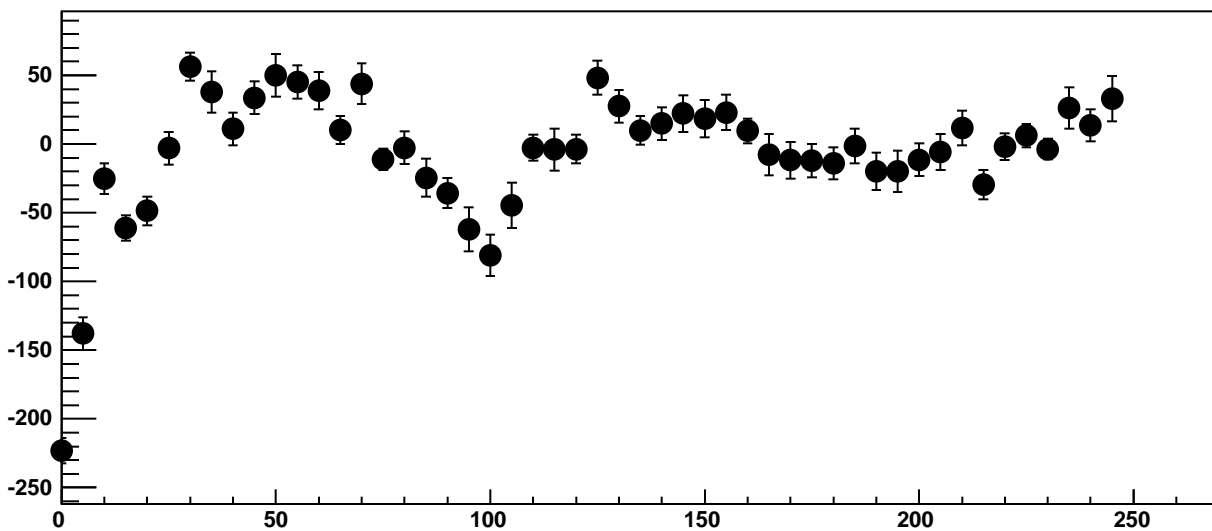
Chip 5, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold



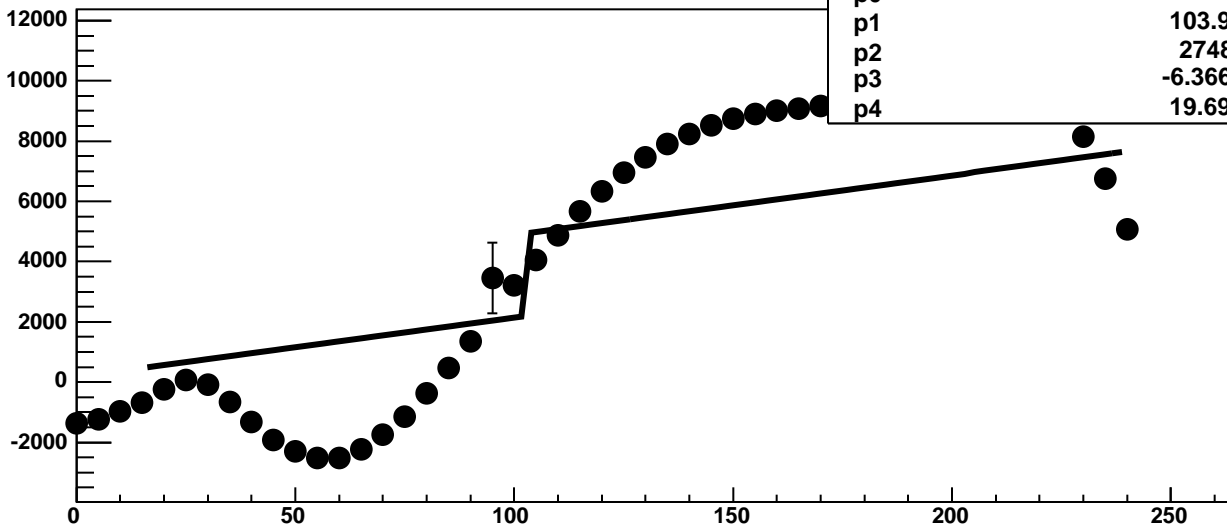
Chip 5, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

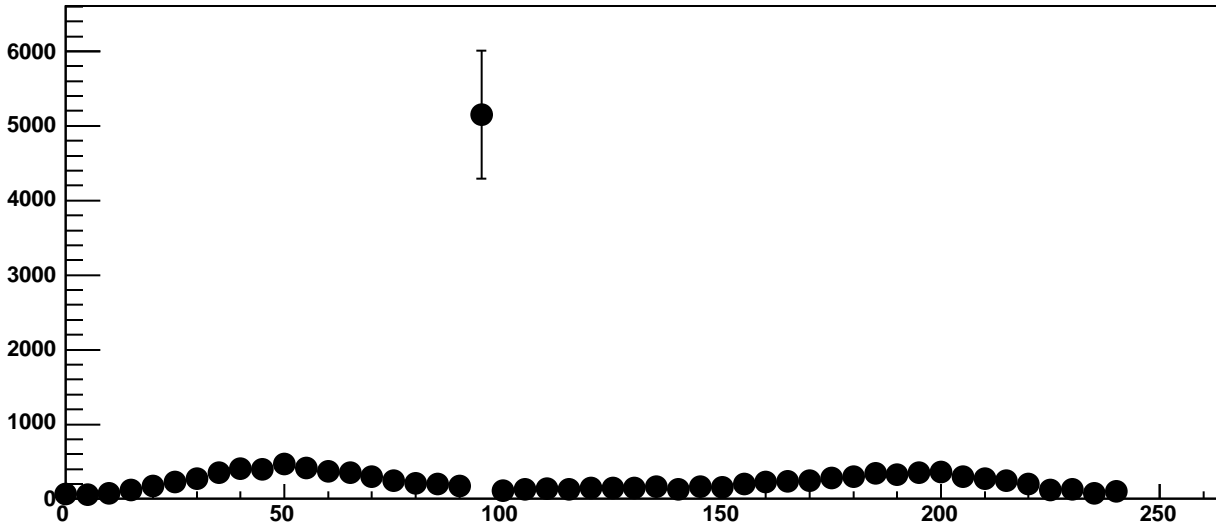


Chip 5, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold

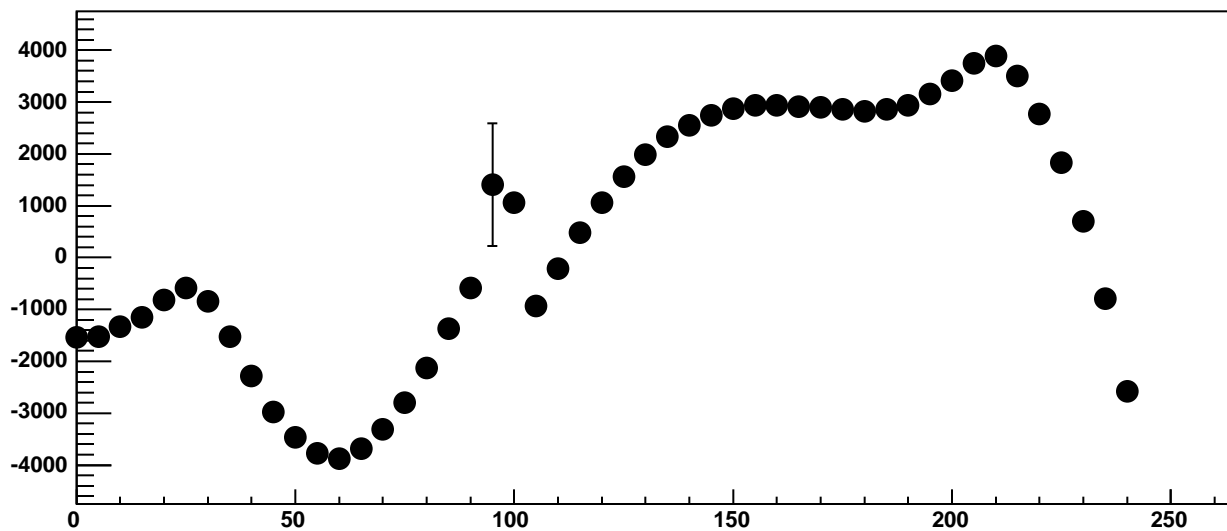


$\chi^2 / \text{ndf}$	1.072e+05 / 41
p0	2223 ± 6.51
p1	103.9 ± 3.068
p2	2748 ± 12.91
p3	-6.366 ± 2.087
p4	19.69 ± 0.042

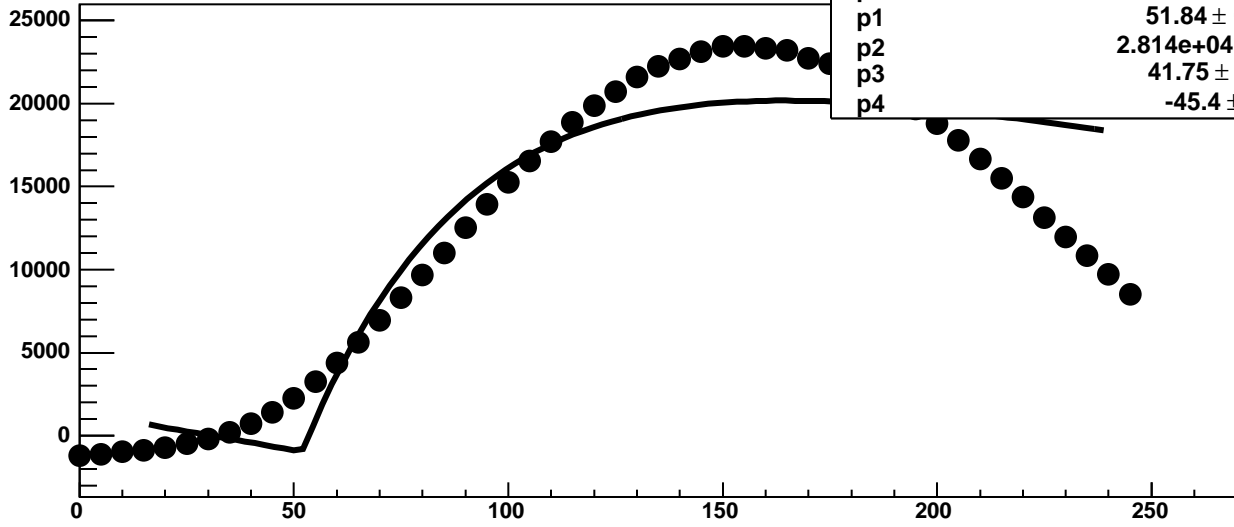
Chip 5, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold

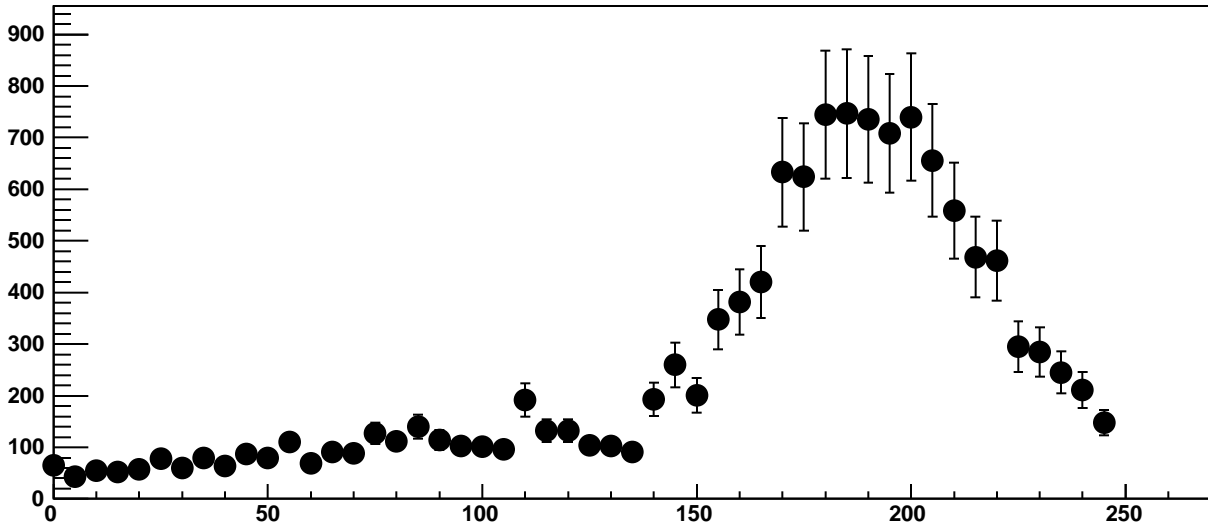


Chip 5, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

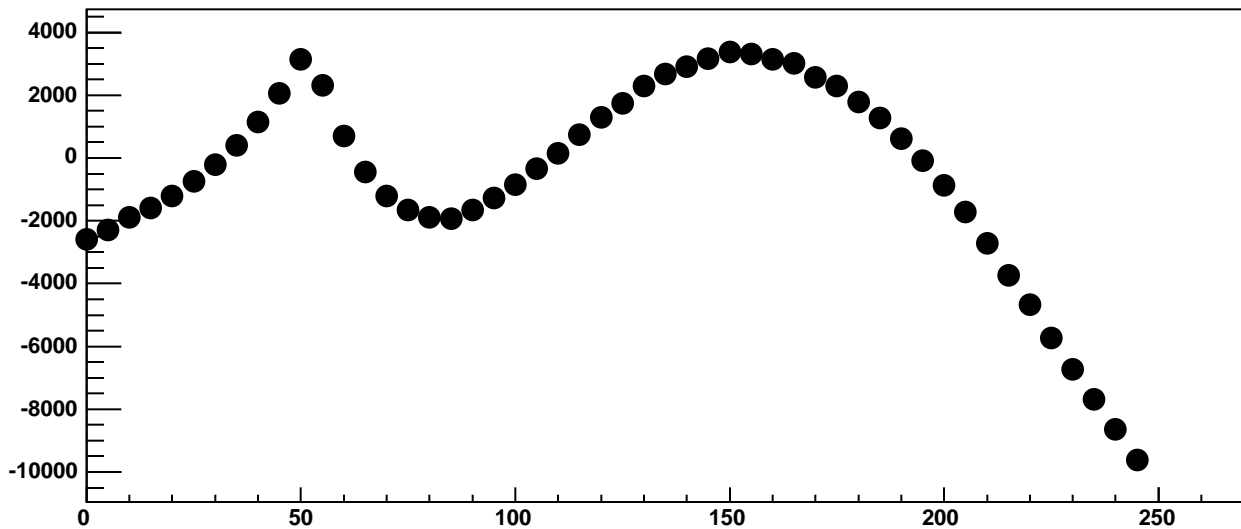


$\chi^2 / \text{ndf}$	2.331e+05 / 41
p0	-953.8 ± 8.187
p1	51.84 ± 0.02763
p2	2.814e+04 ± 54.78
p3	41.75 ± 0.09441
p4	-45.4 ± 0.3073

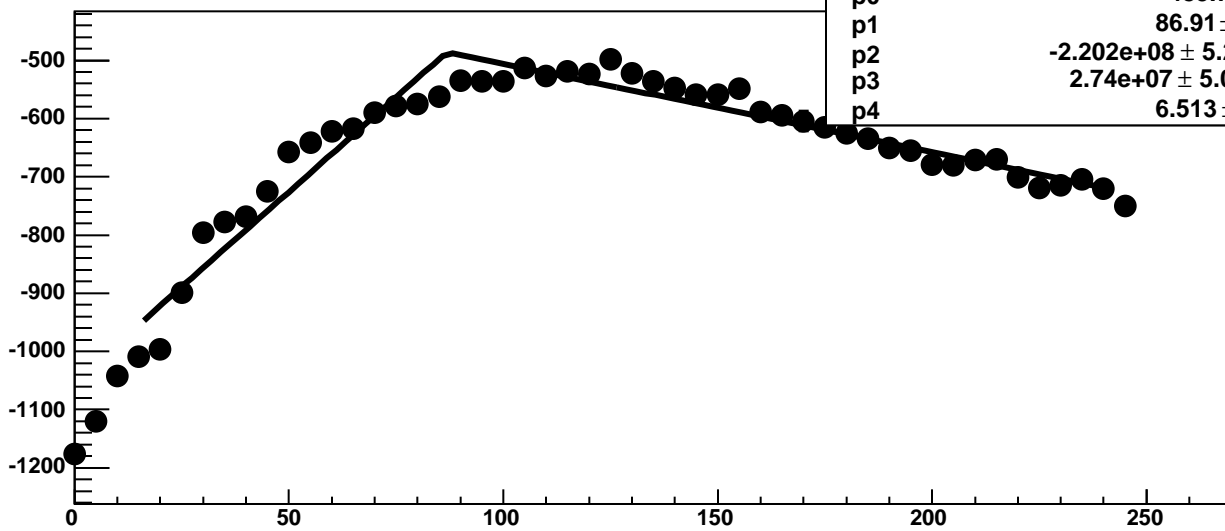
Chip 5, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



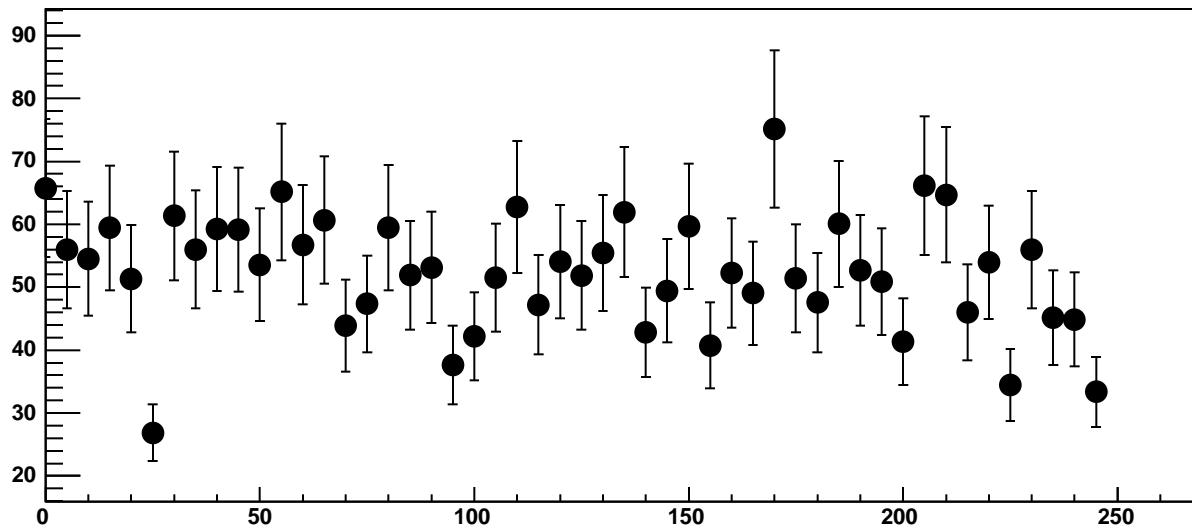
Chip 5, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold



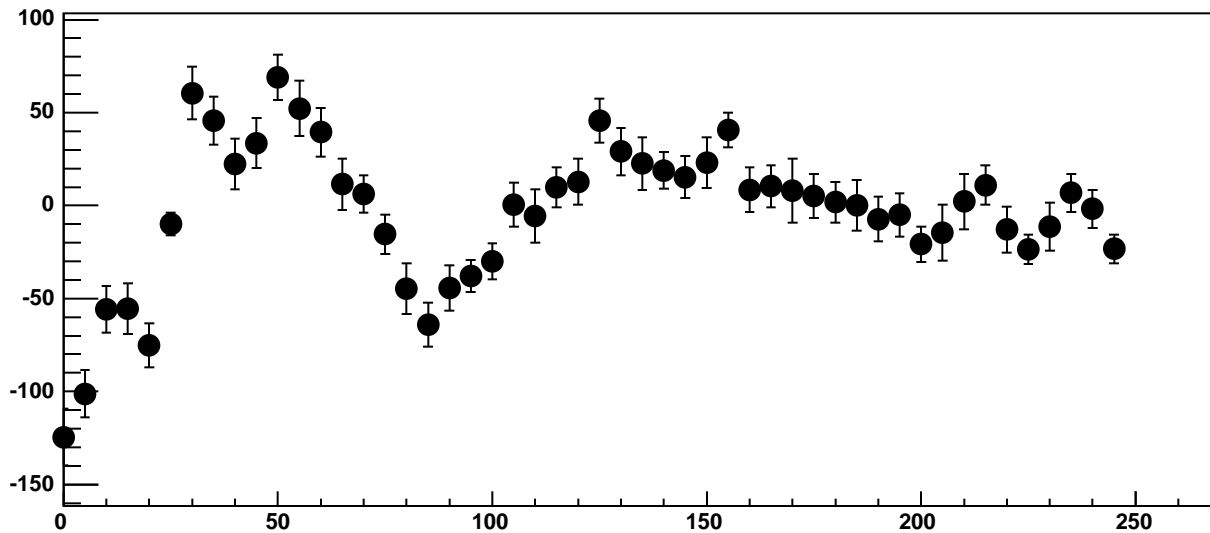
Chip 5, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold



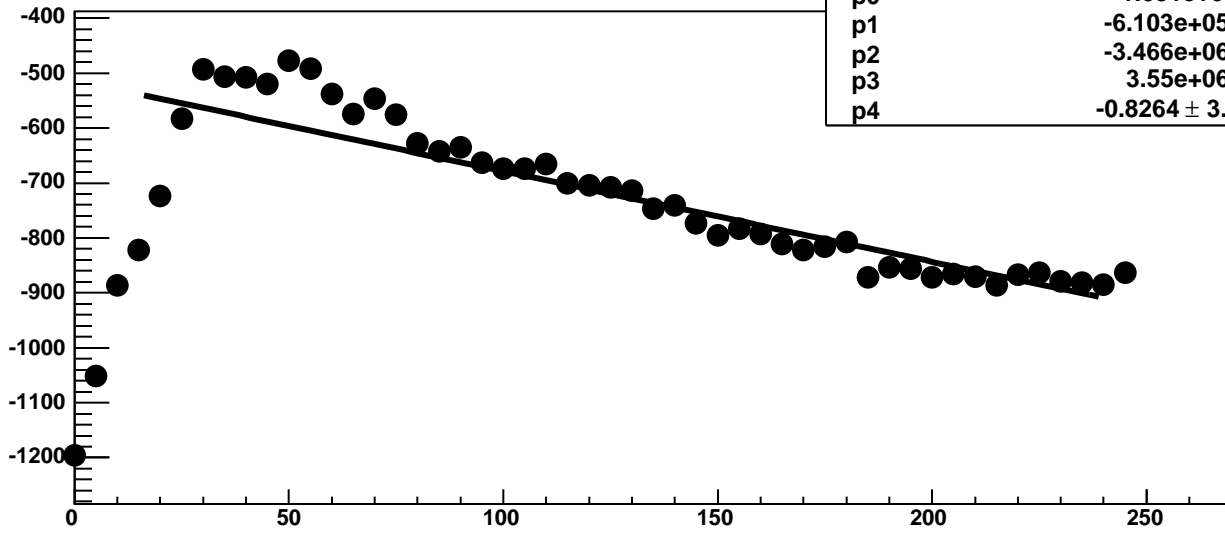
Chip 5, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

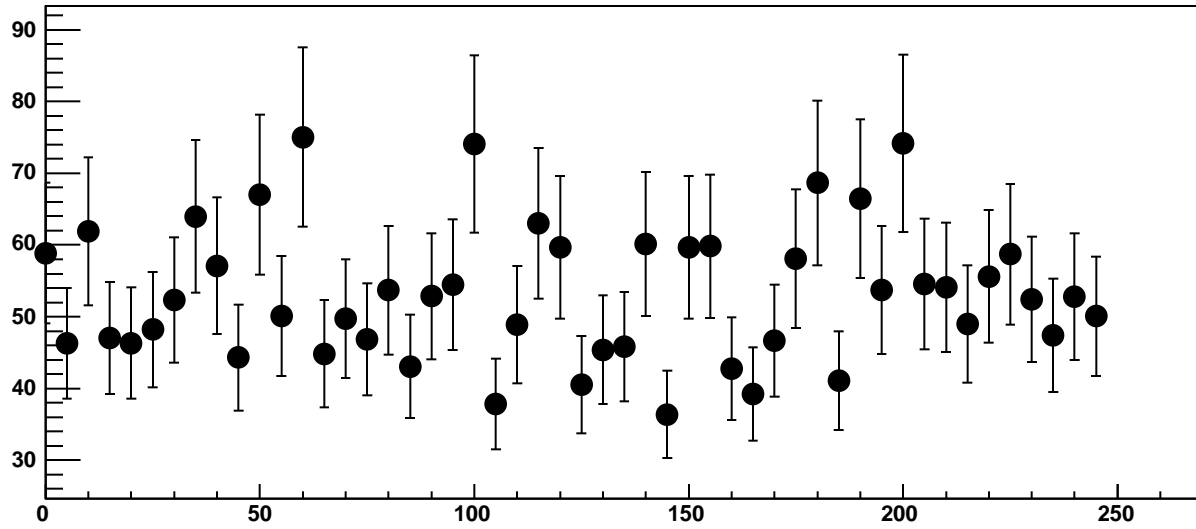


Chip 5, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold

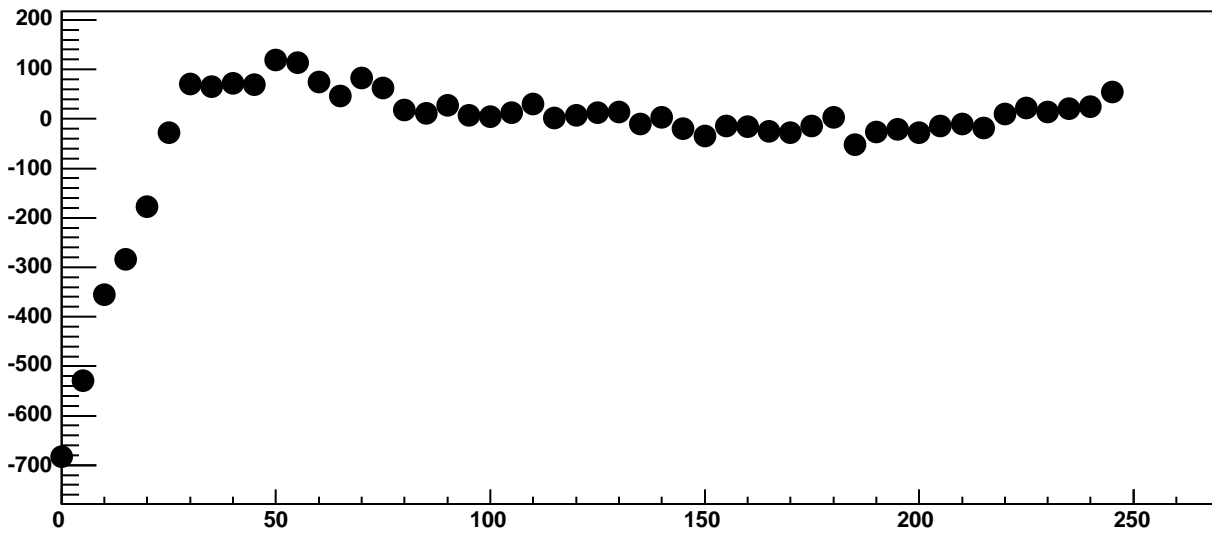


$\chi^2 / \text{ndf}$	1495 / 41
p0	$1.051\text{e}+06 \pm 21.7$
p1	$-6.103\text{e}+05 \pm 13.16$
p2	$-3.466\text{e}+06 \pm 137.3$
p3	$3.55\text{e}+06 \pm 153.5$
p4	$-0.8264 \pm 3.55\text{e}-05$

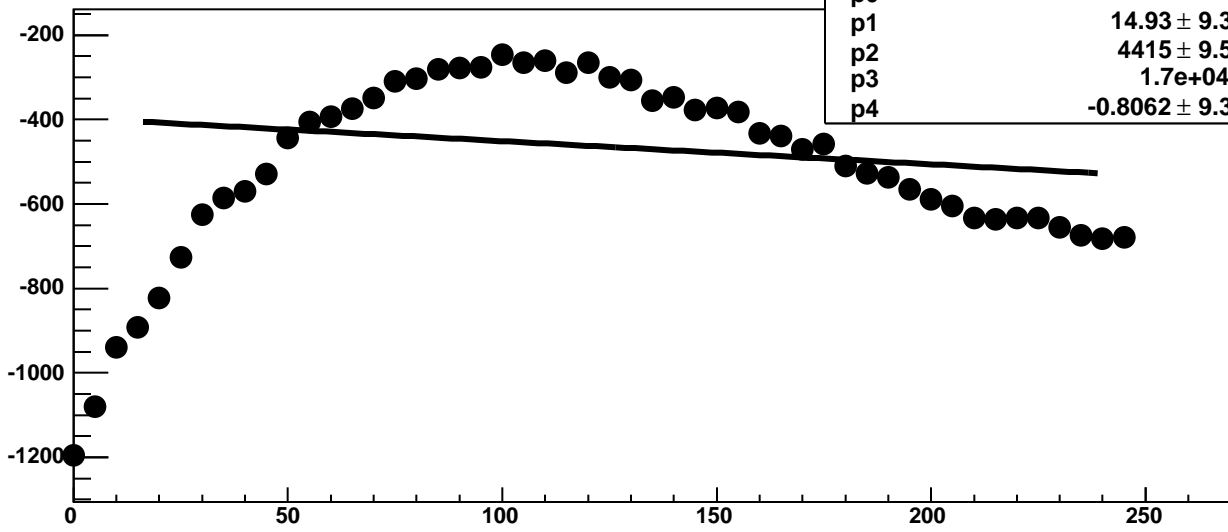
Chip 5, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold

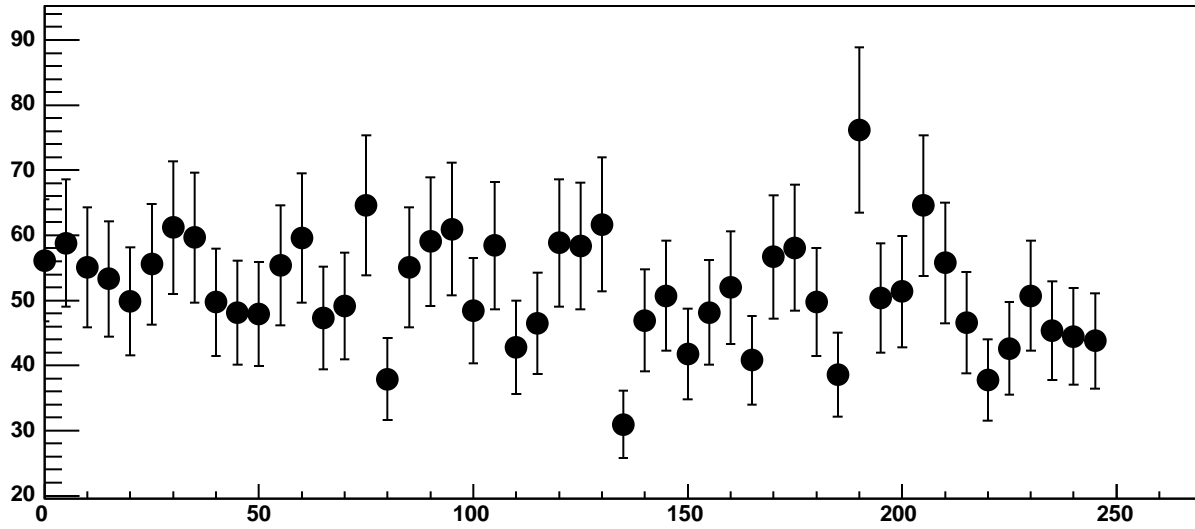


Chip 5, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

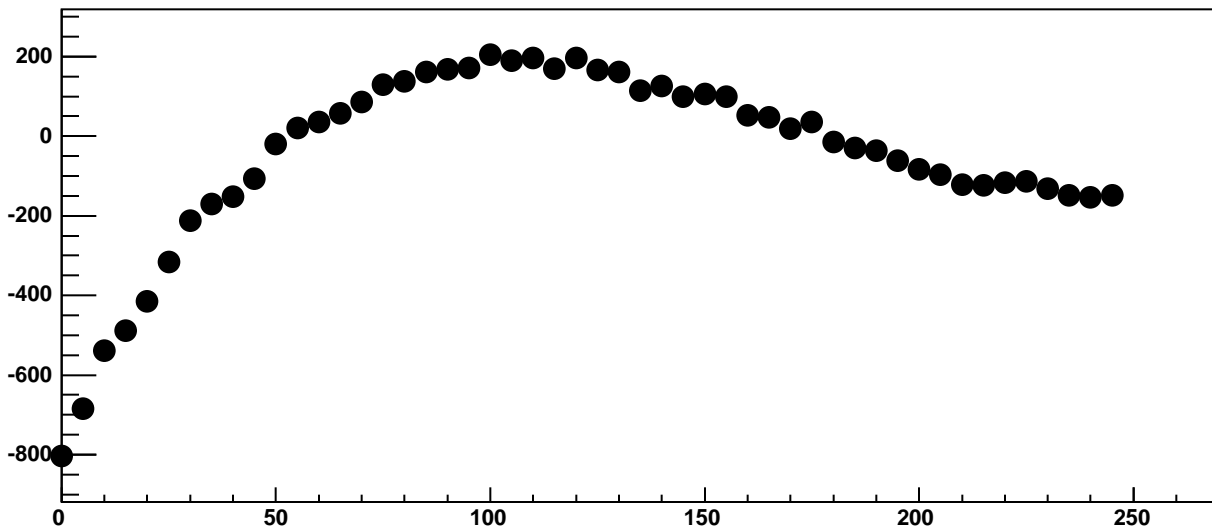


$\chi^2 / \text{ndf}$	8732 / 41
p0	$-404.5 \pm 9.319e+04$
p1	$14.93 \pm 9.319e+04$
p2	$4415 \pm 9.573e+04$
p3	$1.7e+04 \pm 16.08$
p4	$-0.8062 \pm 9.319e+04$

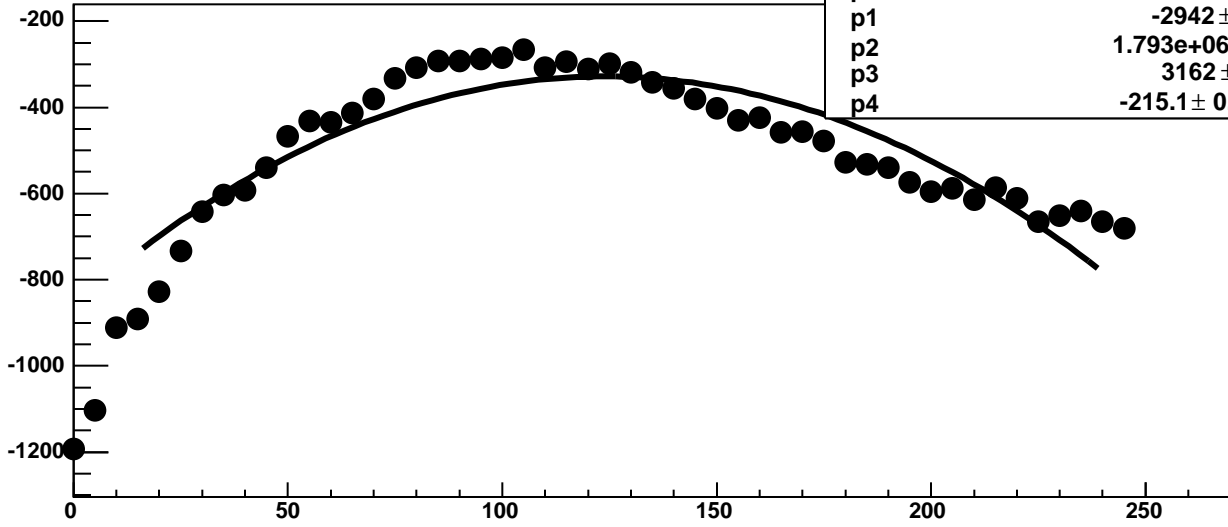
Chip 5, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



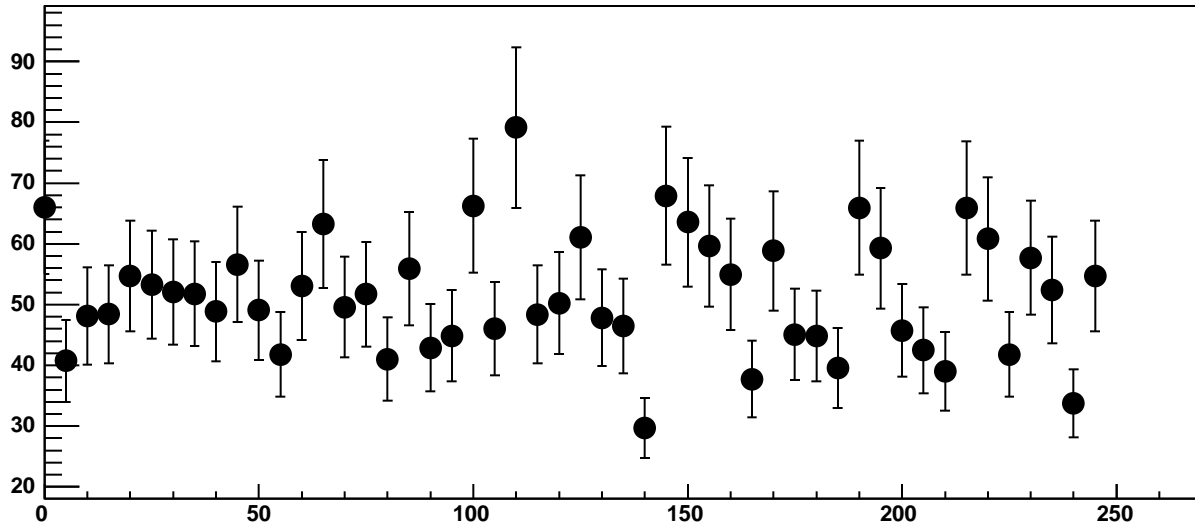
Chip 5, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold



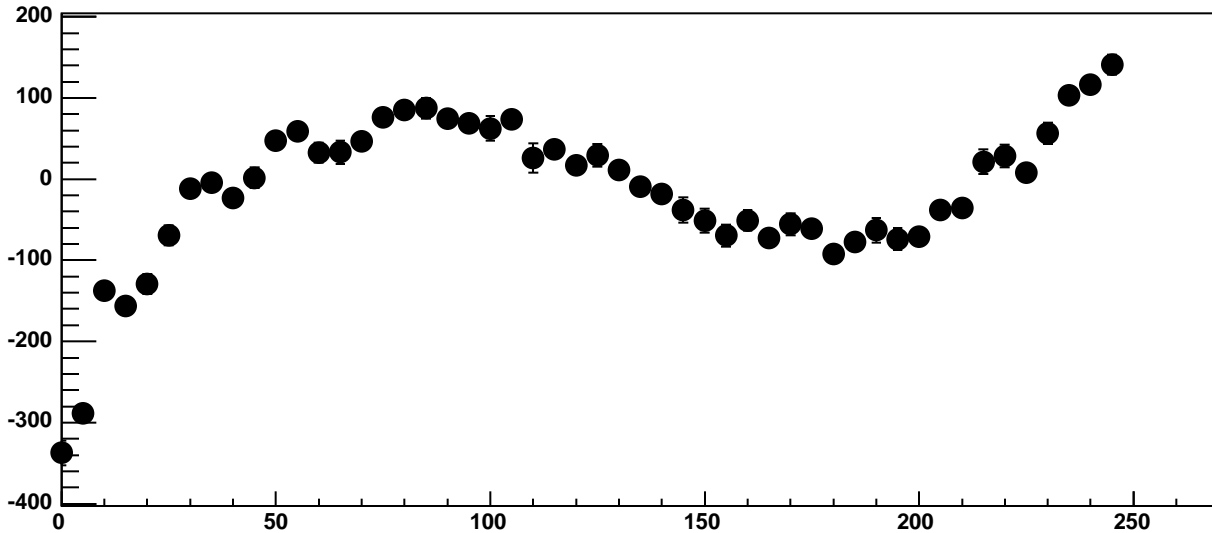
Chip 5, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold



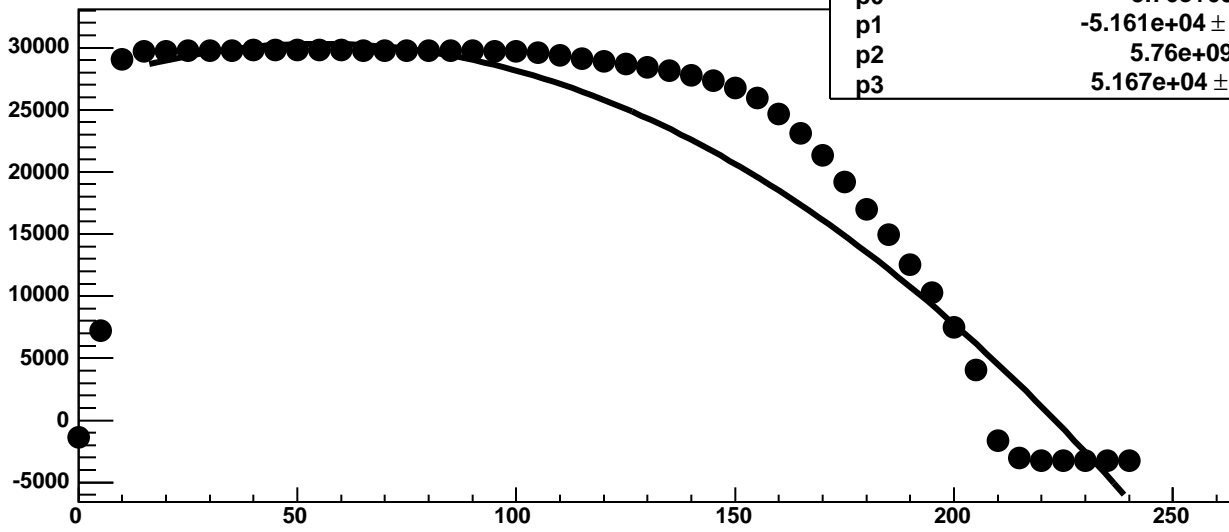
Chip 5, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

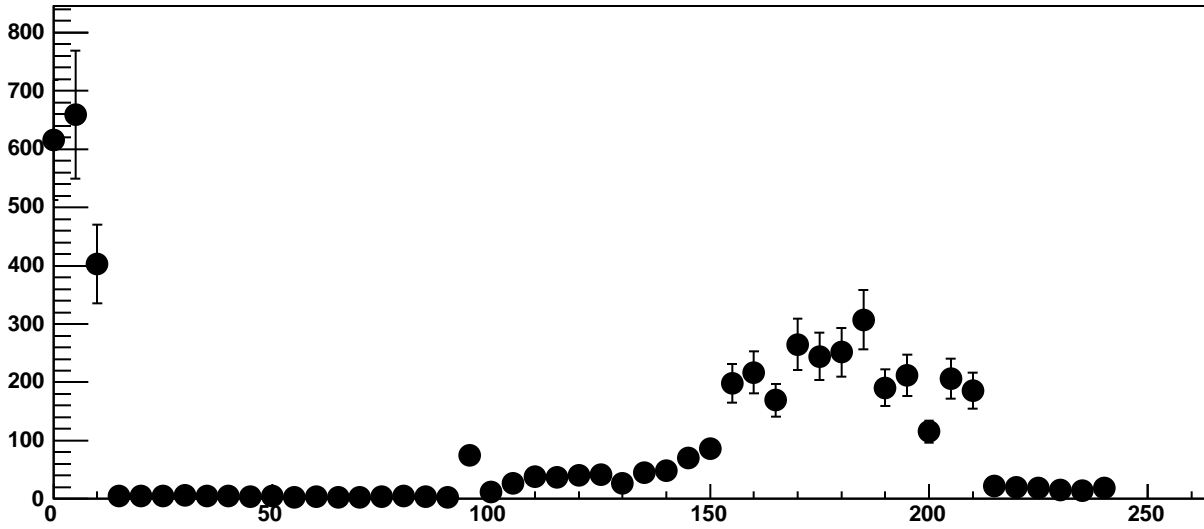


Chip 5, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold

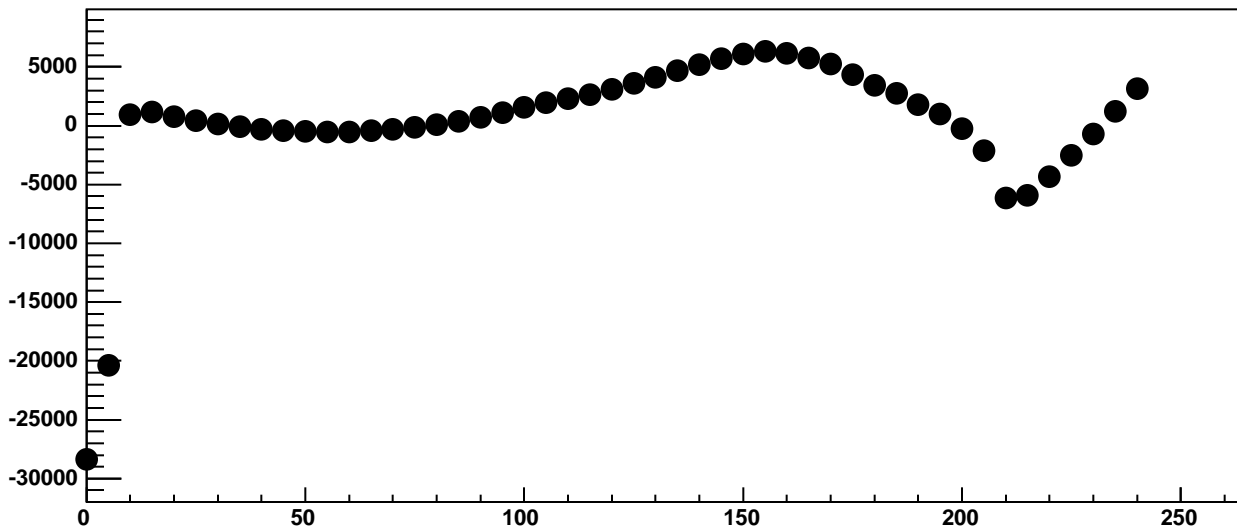


$\chi^2 / \text{ndf}$	1.013e+07 / 42
p0	-5.76e+09 ± 3.202
p1	-5.161e+04 ± 0.04049
p2	5.76e+09 ± 3.202
p3	5.167e+04 ± 0.04041

Chip 5, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

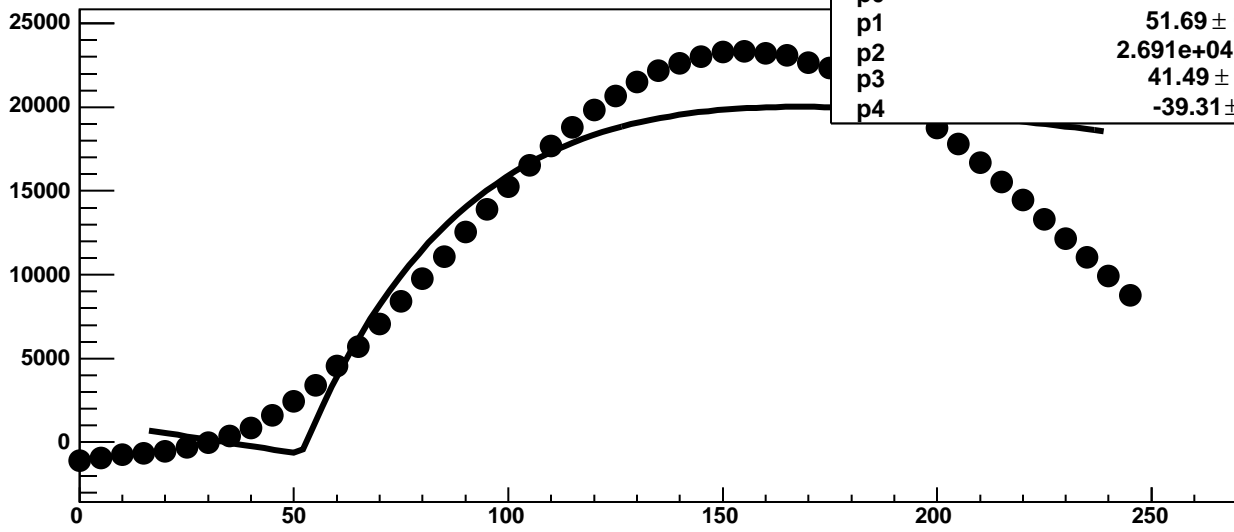


Chip 5, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold



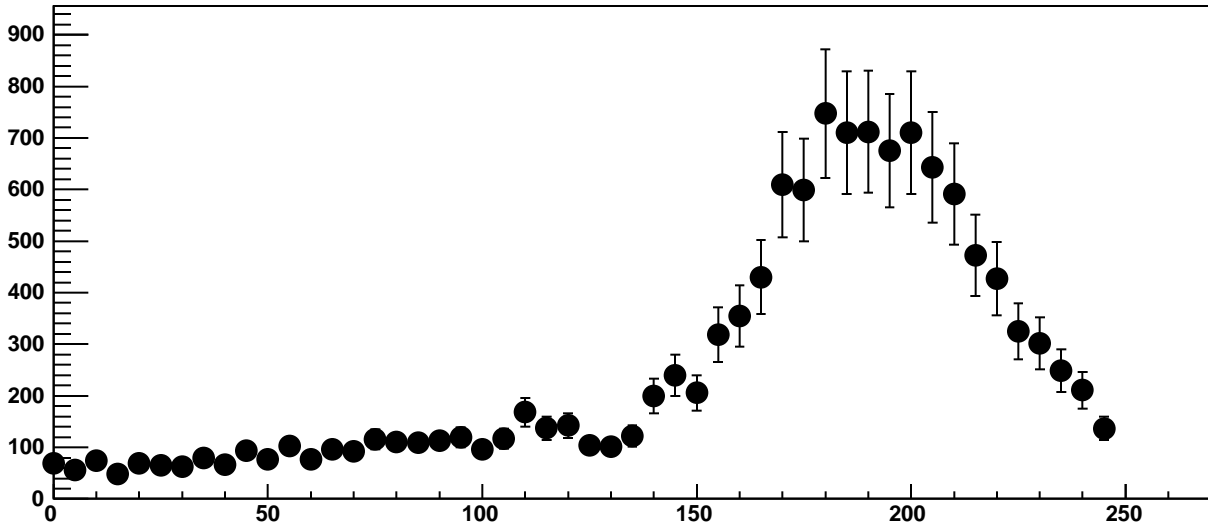


Chip 5, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold

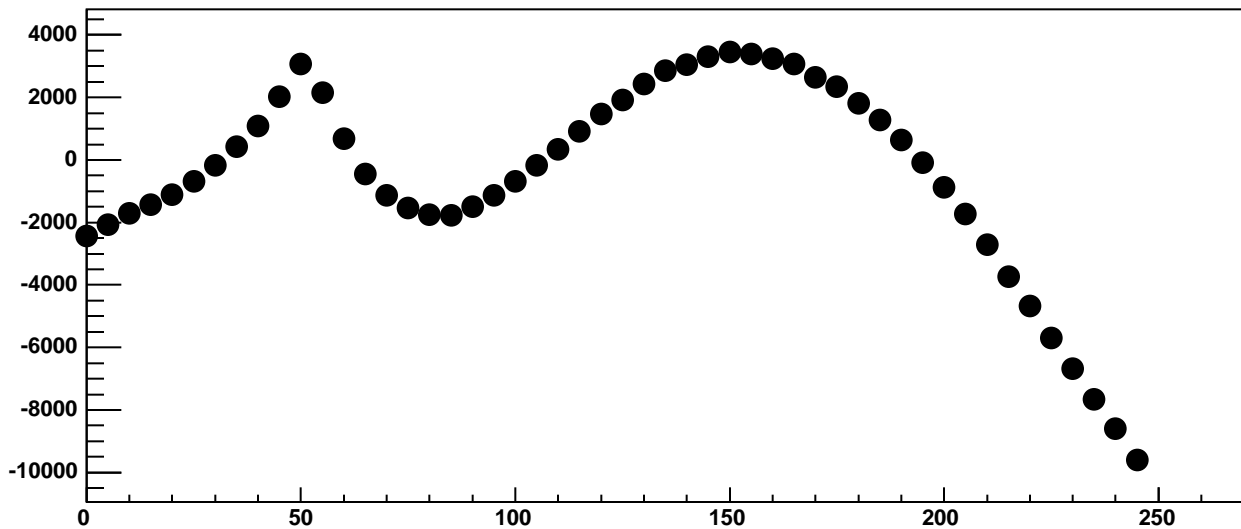


$\chi^2 / \text{ndf}$	2.189e+05 / 41
p0	-688.8 ± 8.324
p1	51.69 ± 0.02938
p2	2.691e+04 ± 54.85
p3	41.49 ± 0.09761
p4	-39.31 ± 0.3075

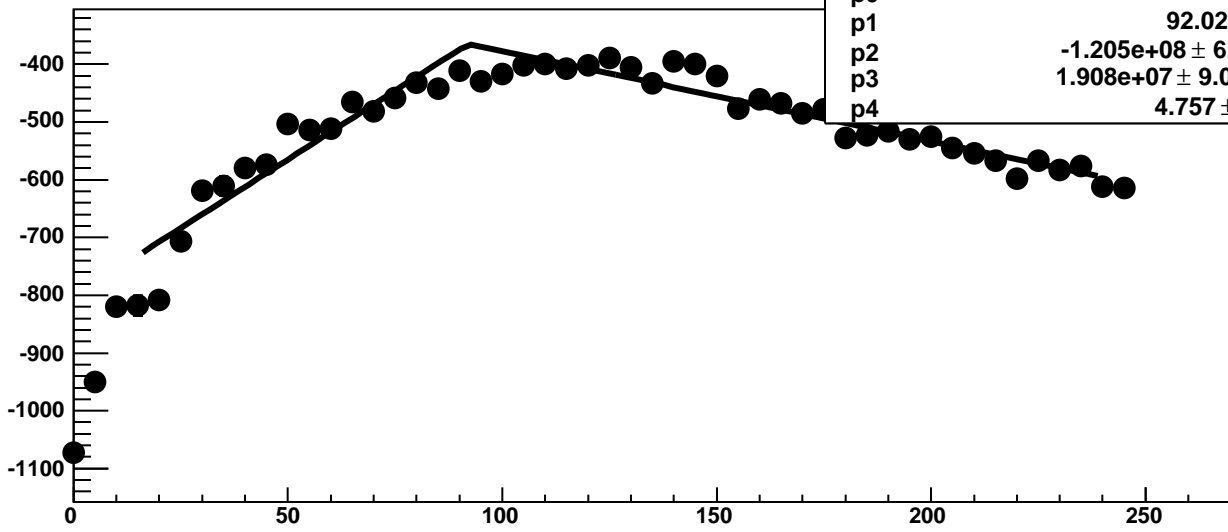
Chip 5, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



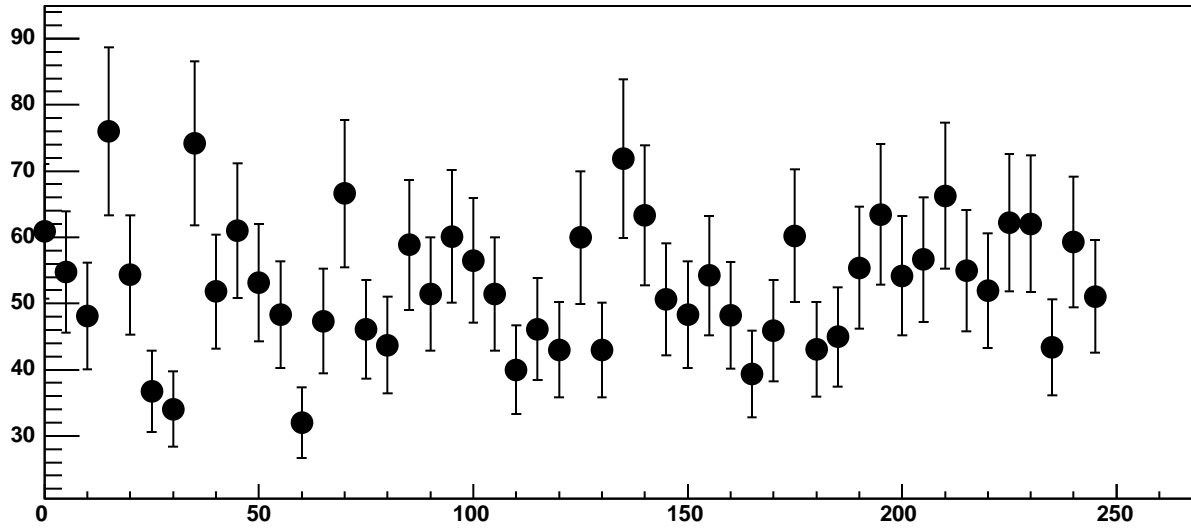
Chip 5, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold



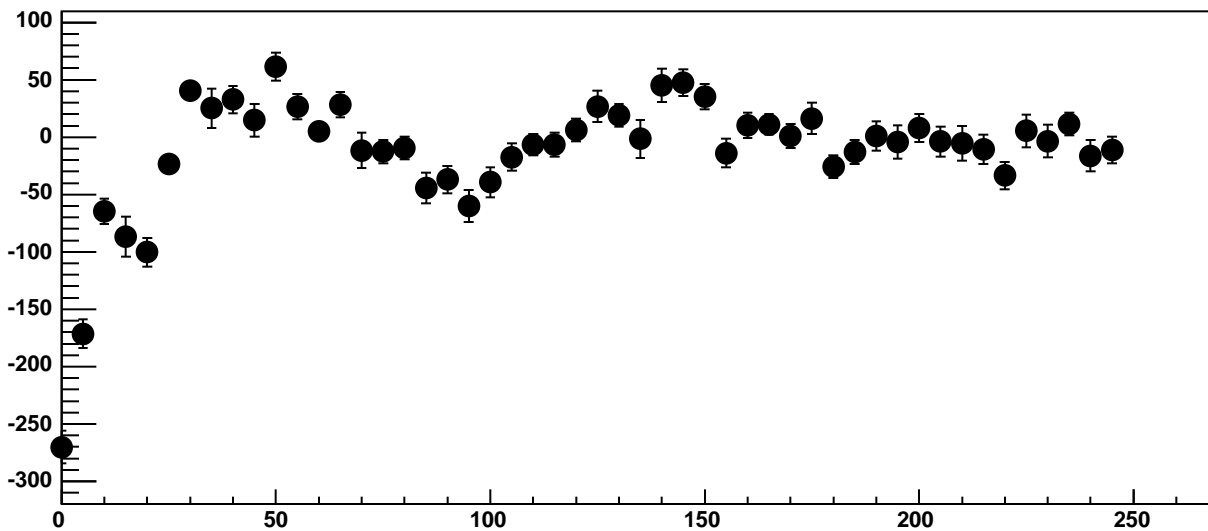
Chip 5, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold



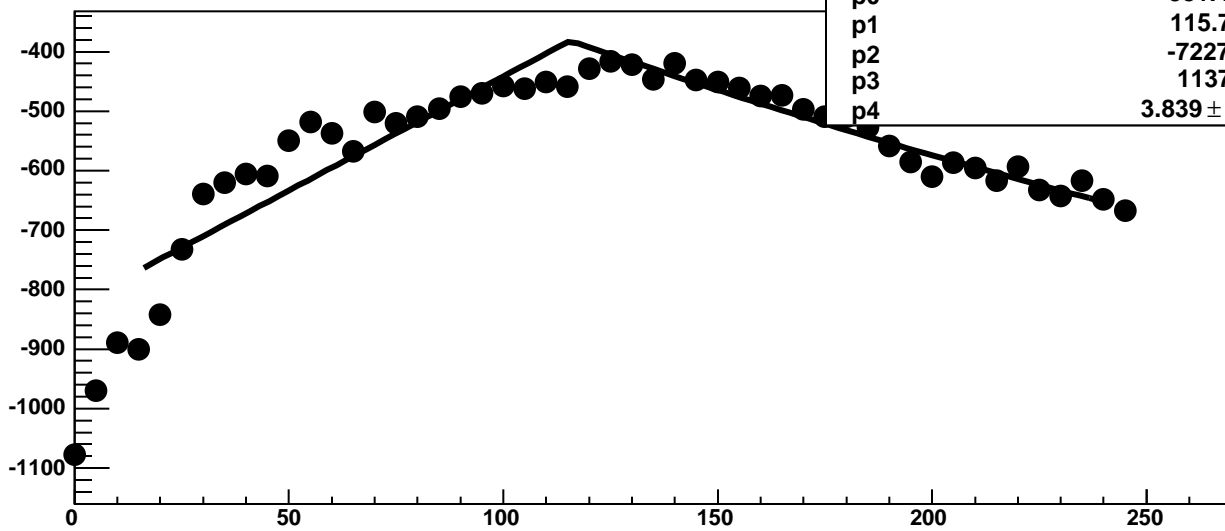
Chip 5, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold



Chip 5, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

668 / 41

p0  $-381.4 \pm 3.828$

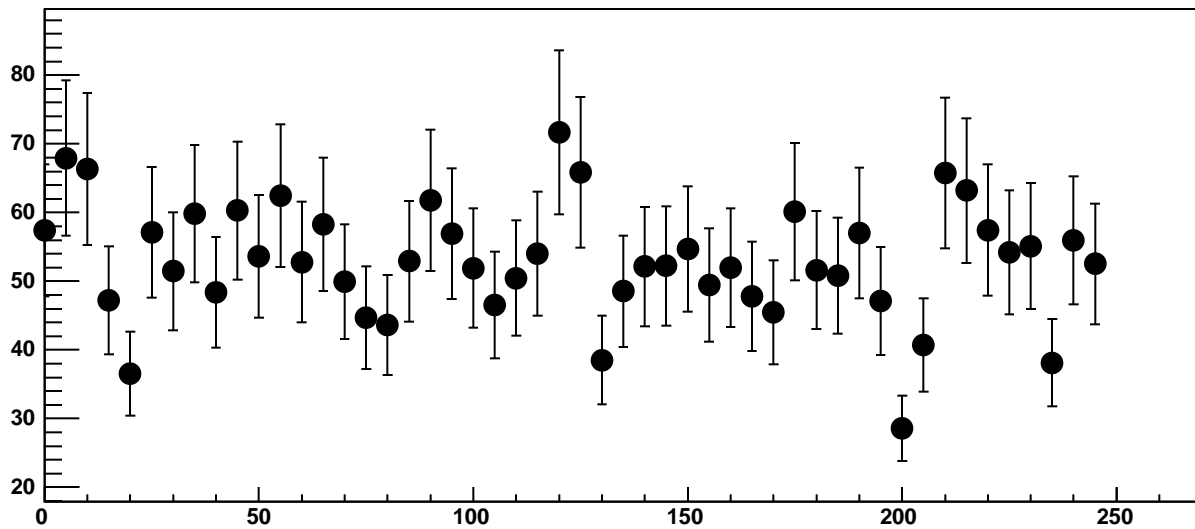
p1  $115.7 \pm 1.138$

p2  $-7227 \pm 1716$

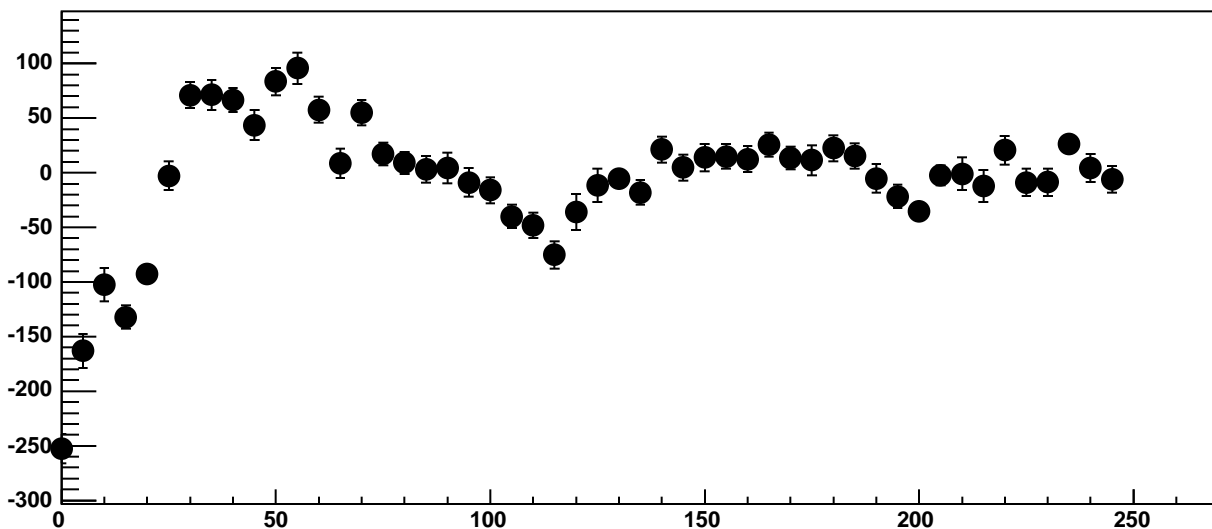
p3  $1137 \pm 285.5$

p4  $3.839 \pm 0.08154$

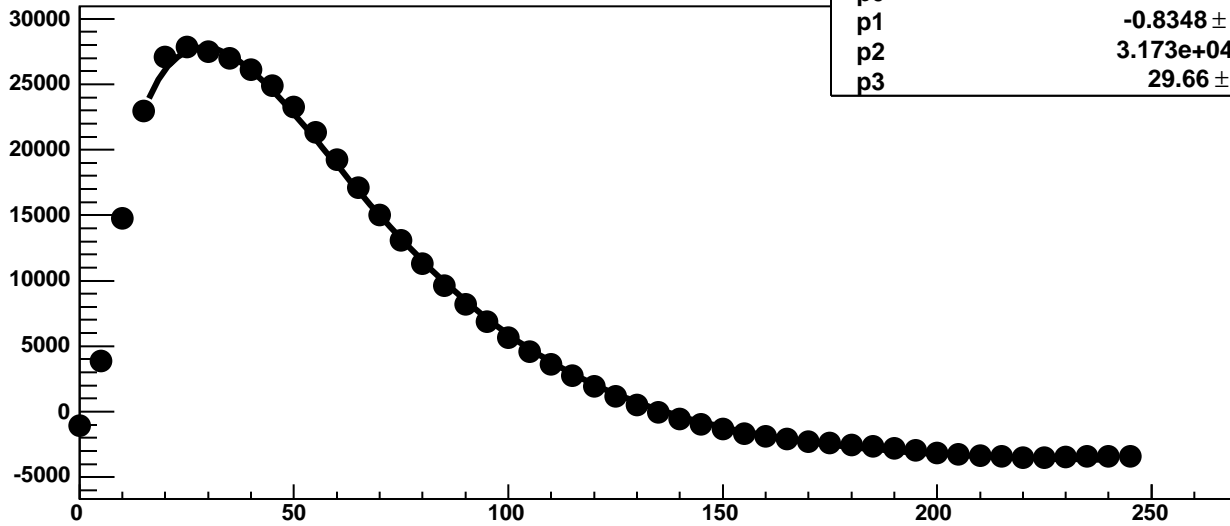
Chip 5, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



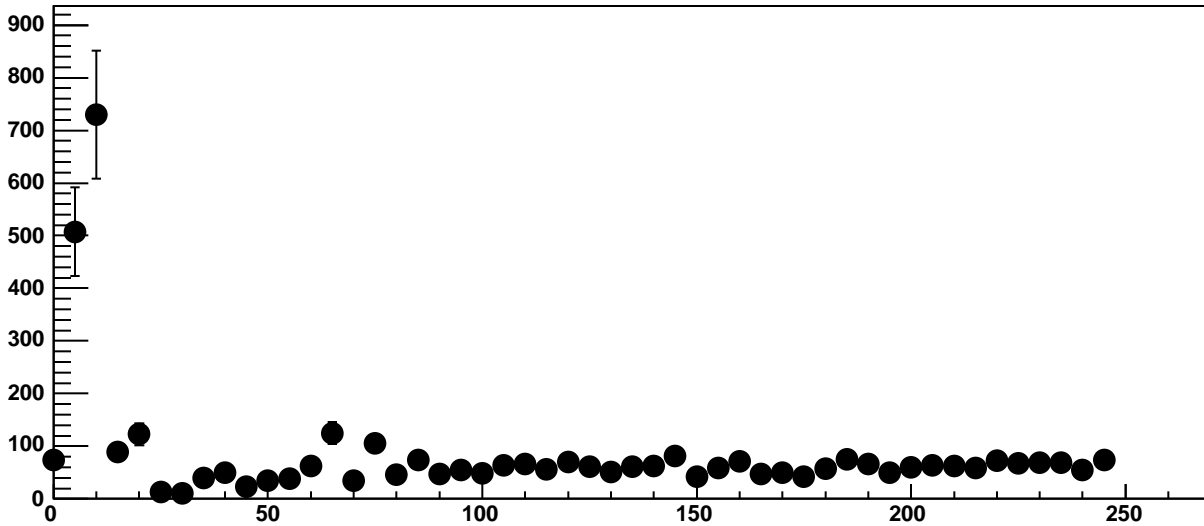
Chip 5, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold



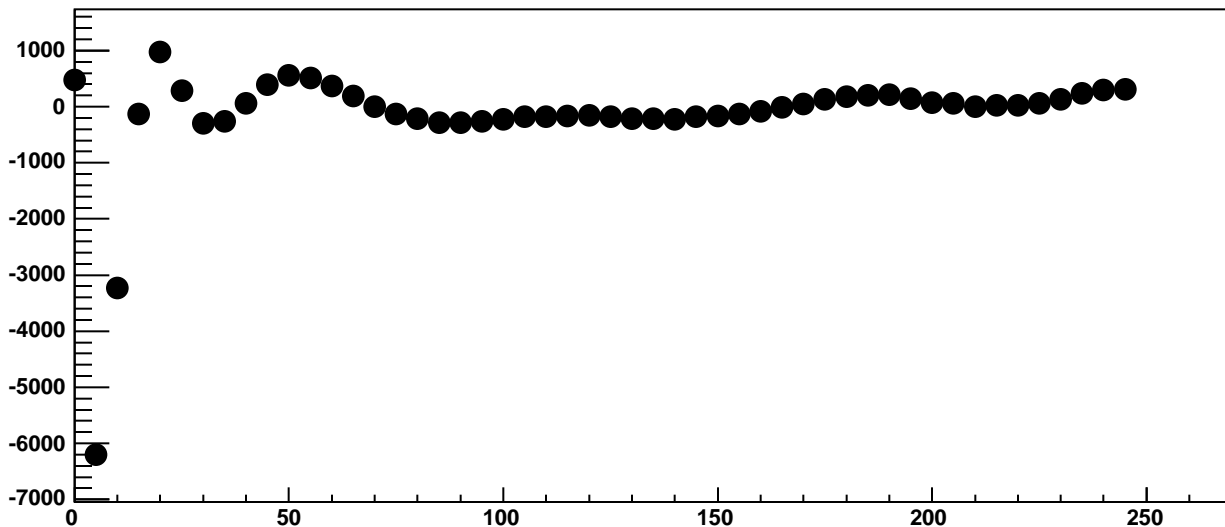
Chip 5, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold



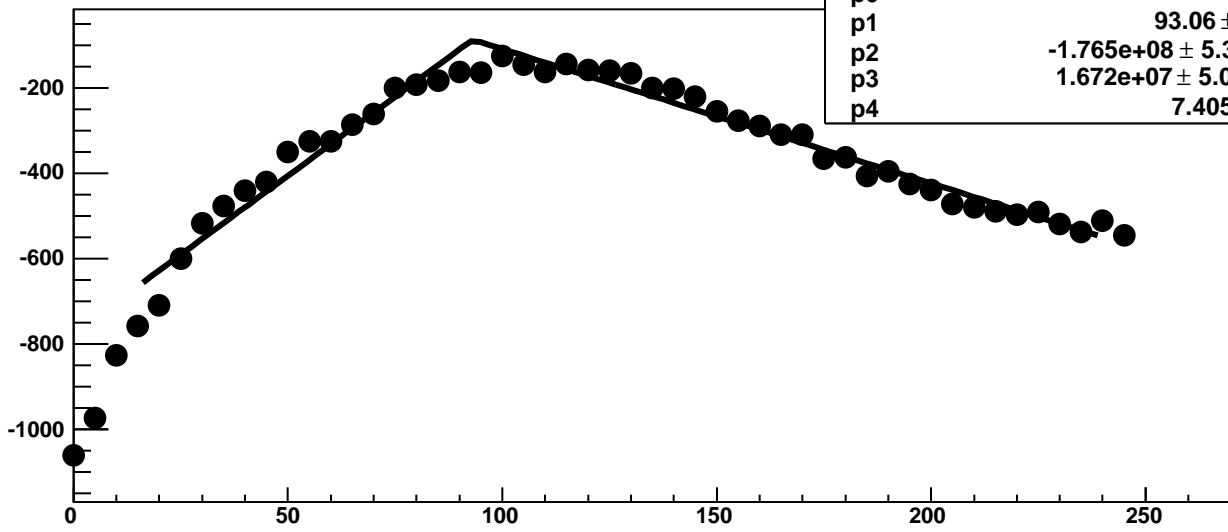
Chip 5, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold

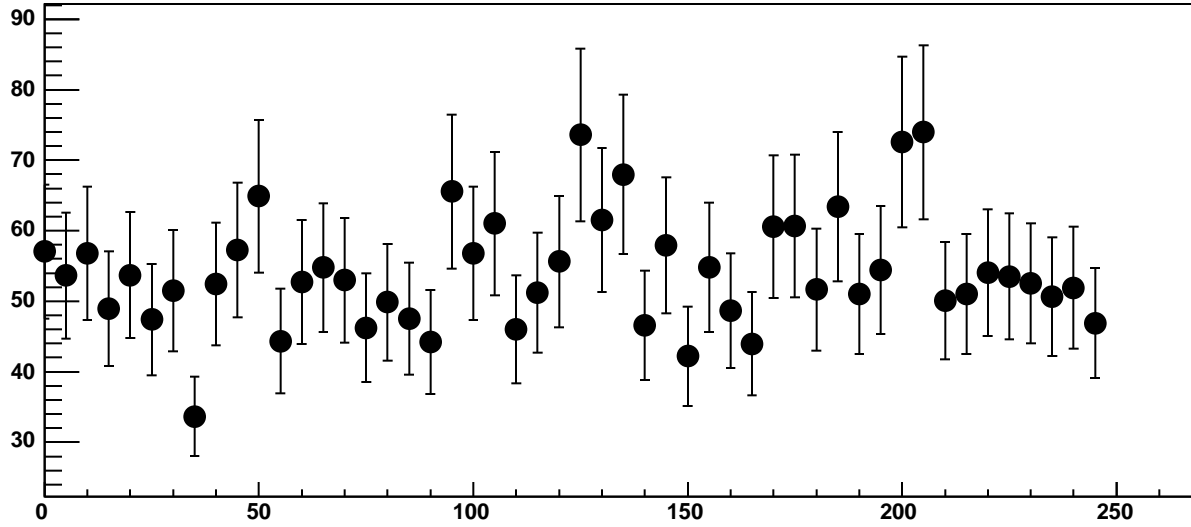


Chip 5, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

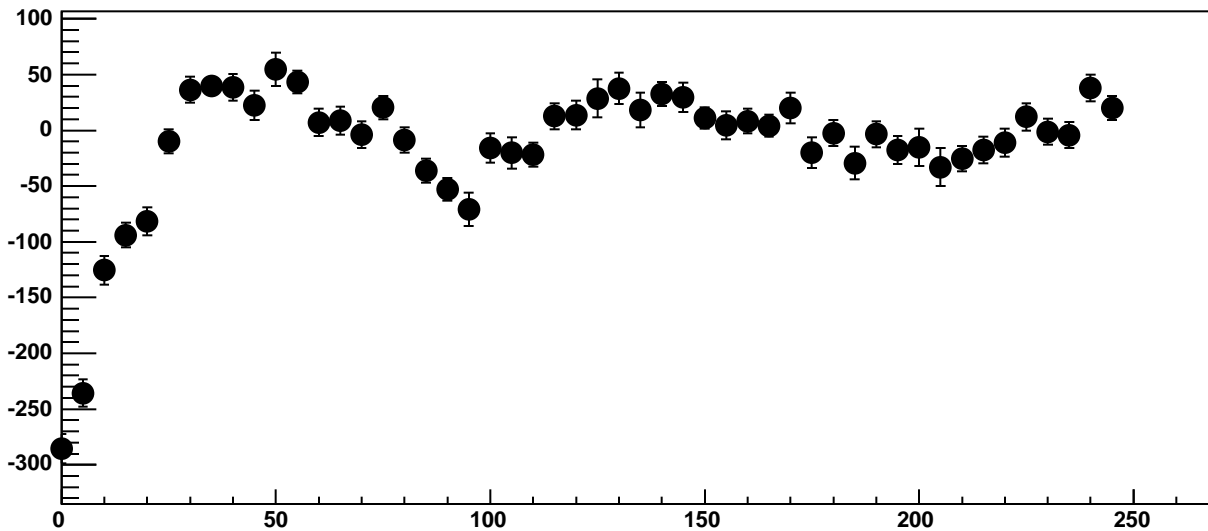


$\chi^2 / \text{ndf}$	333.6 / 41
p0	$-86.53 \pm 3.562$
p1	$93.06 \pm 0.6657$
p2	$-1.765\text{e}+08 \pm 5.303\text{e}+06$
p3	$1.672\text{e}+07 \pm 5.041\text{e}+05$
p4	$7.405 \pm 0.111$

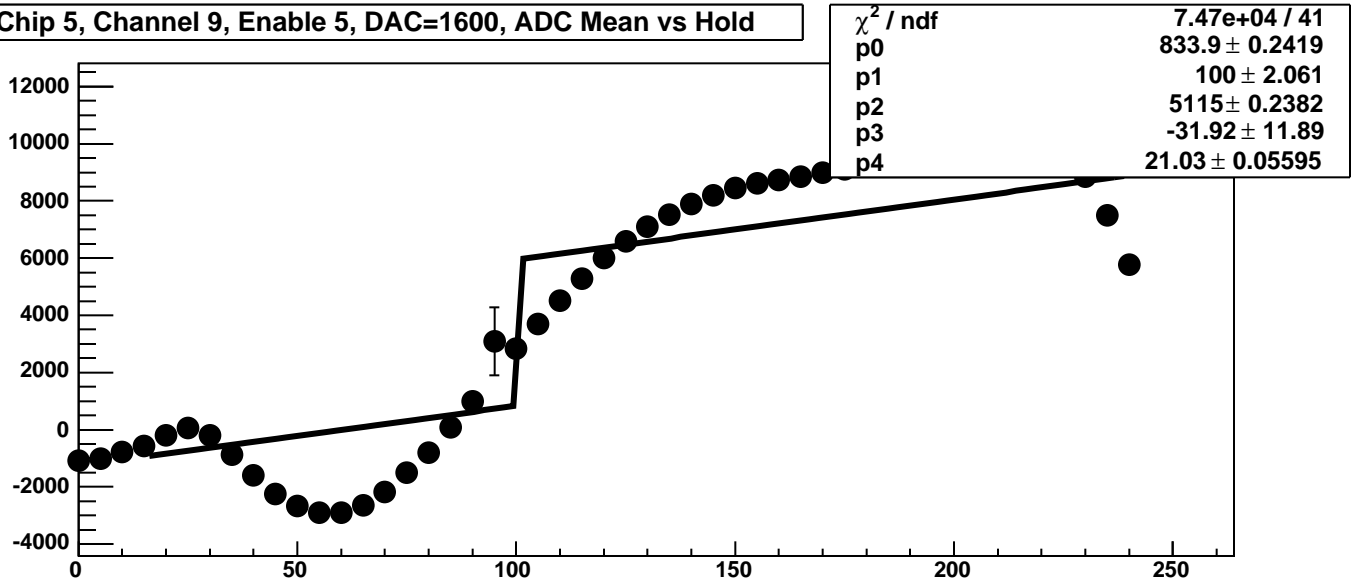
Chip 5, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



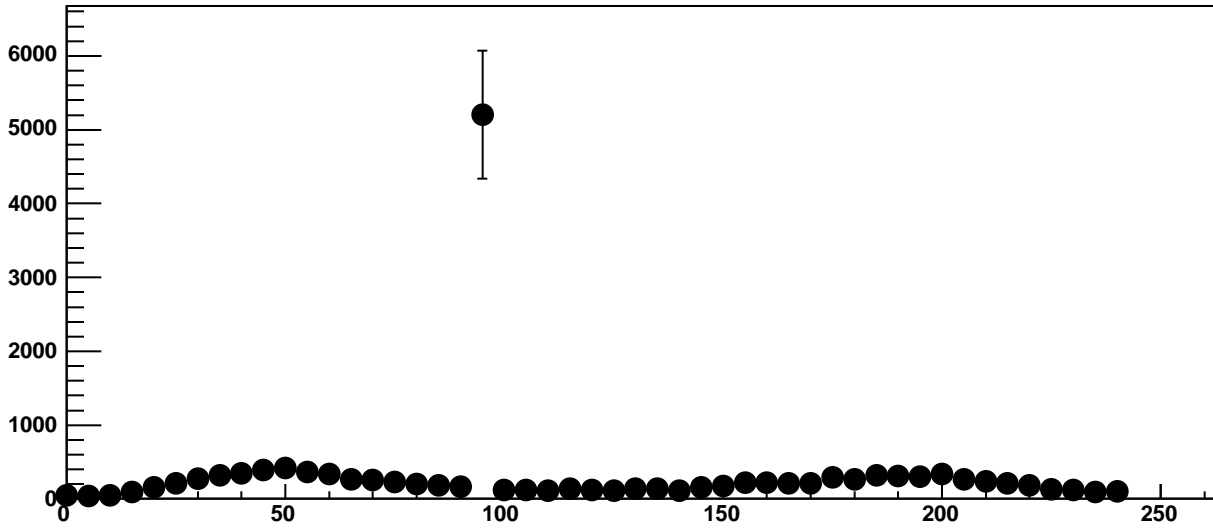
Chip 5, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold



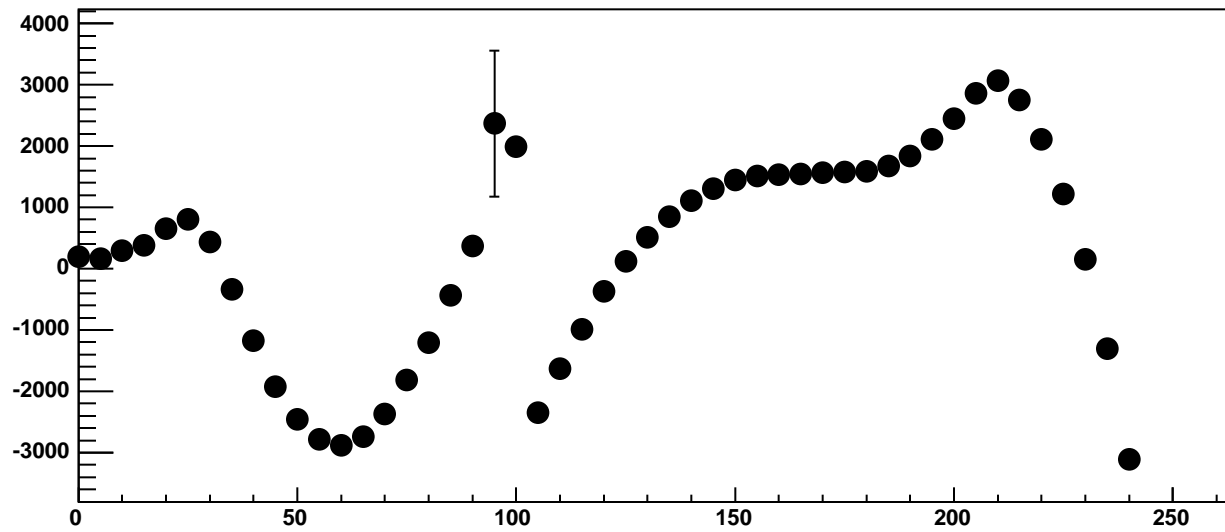
Chip 5, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 5, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold

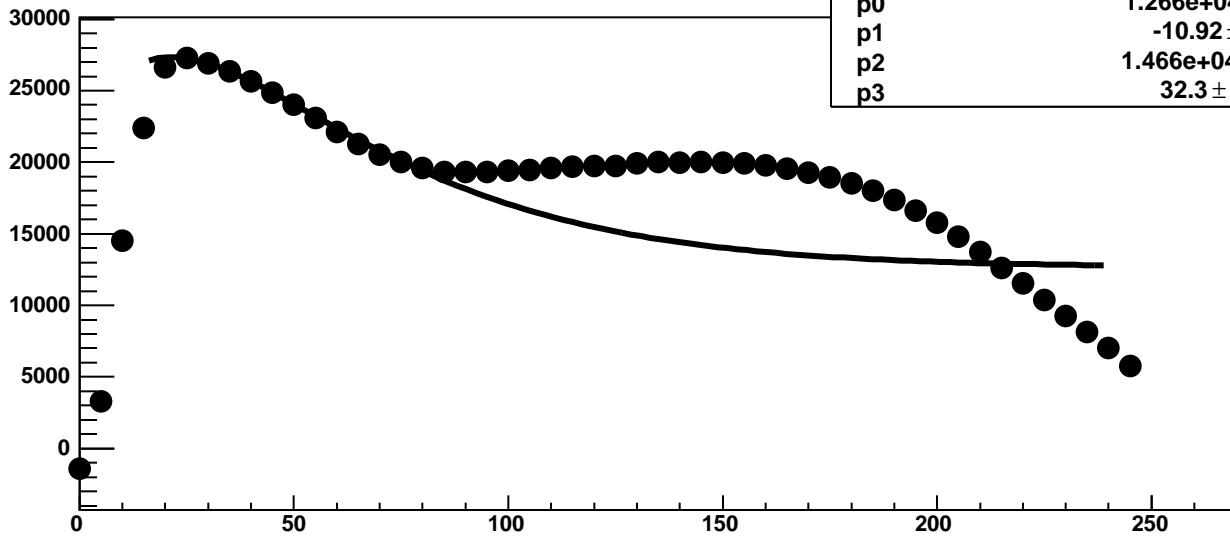


Chip 5, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

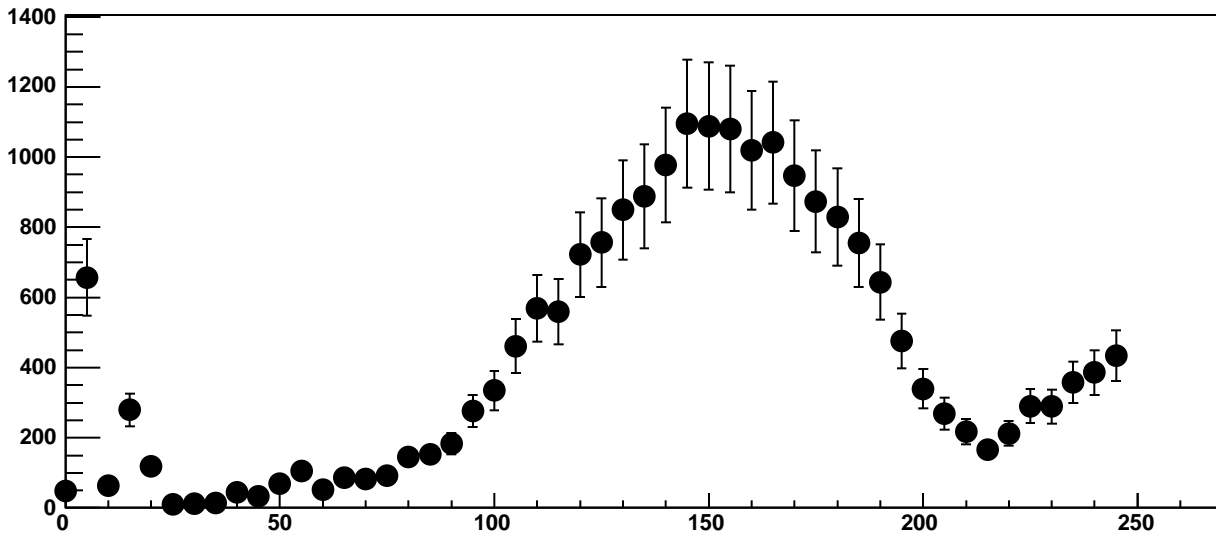


Chip 5, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

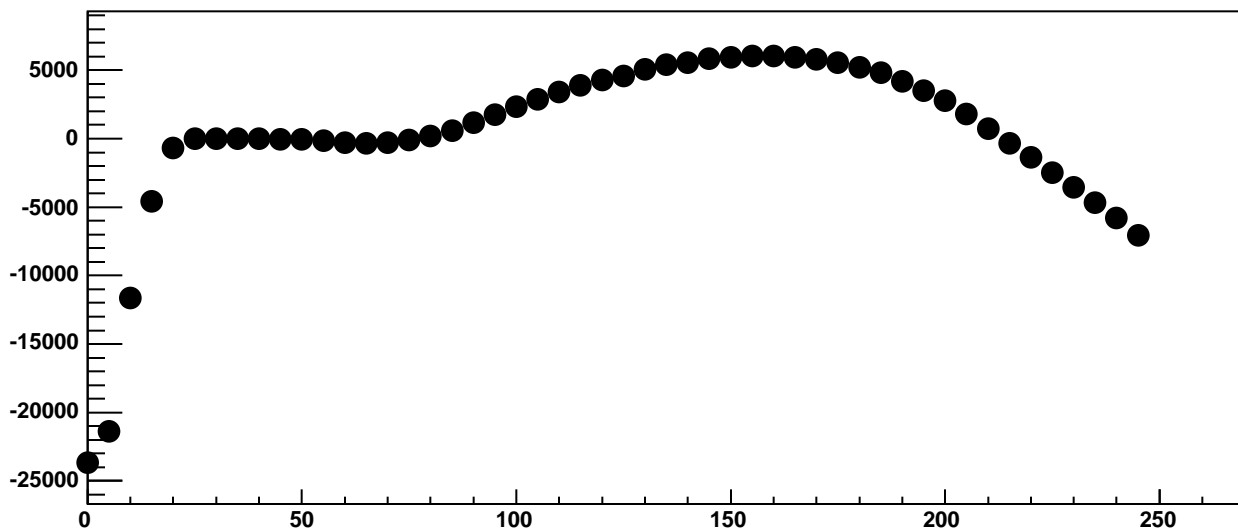
$\chi^2 / \text{ndf}$	3.825e+04 / 42
p0	1.266e+04 $\pm$ 21.4
p1	-10.92 $\pm$ 0.1503
p2	1.466e+04 $\pm$ 23.11
p3	32.3 $\pm$ 0.08619



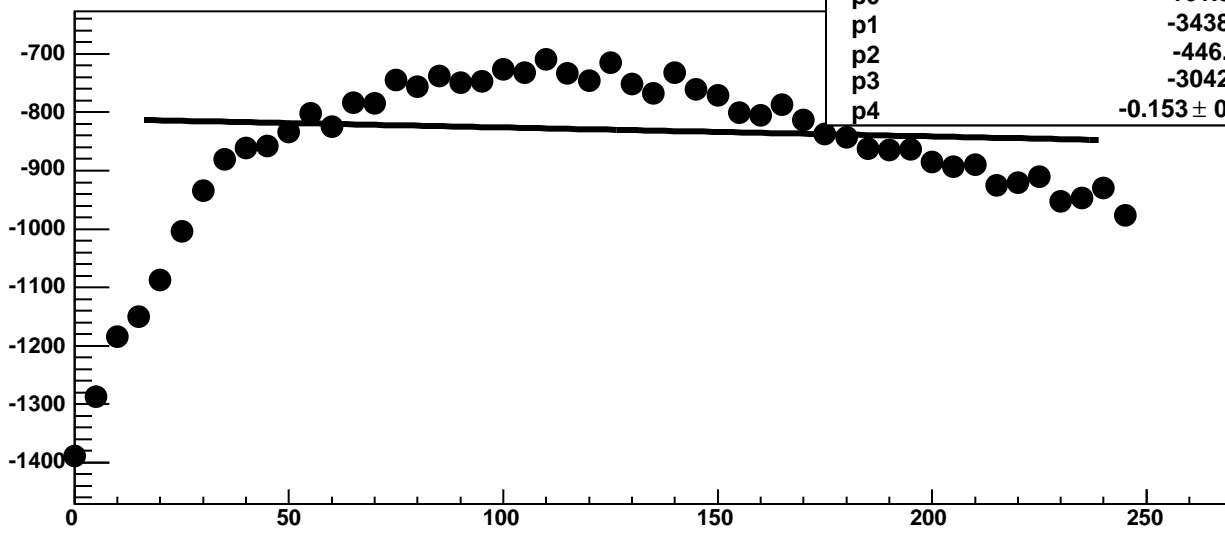
Chip 5, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

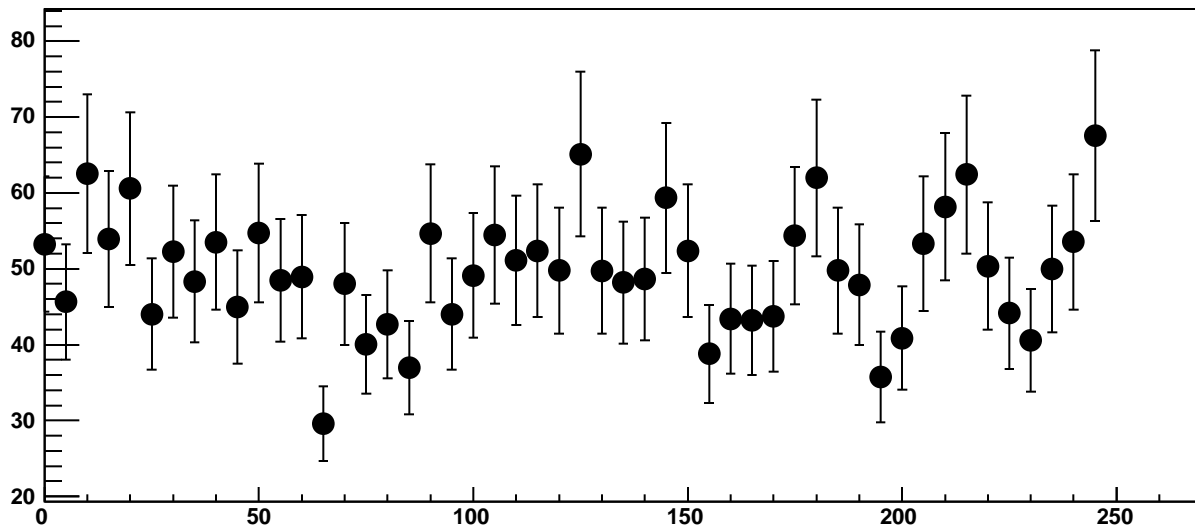


Chip 5, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

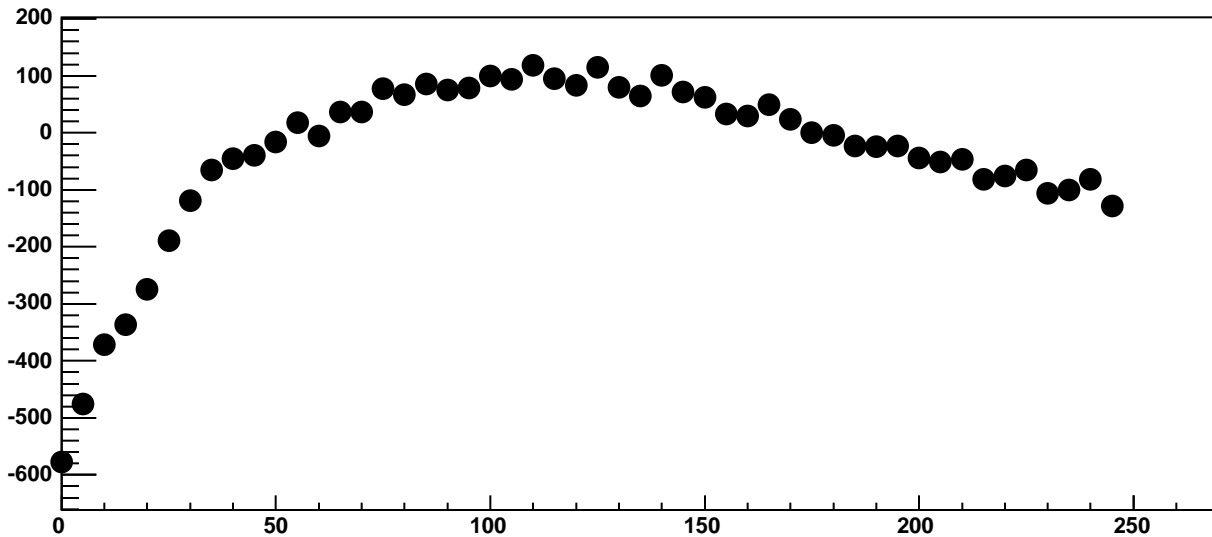


$\chi^2 / \text{ndf}$	3132 / 41
p0	$161.5 \pm 6.551$
p1	$-3438 \pm 64.43$
p2	$-446.4 \pm 8.4$
p3	$-3042 \pm 998.9$
p4	$-0.153 \pm 0.001837$

Chip 5, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold

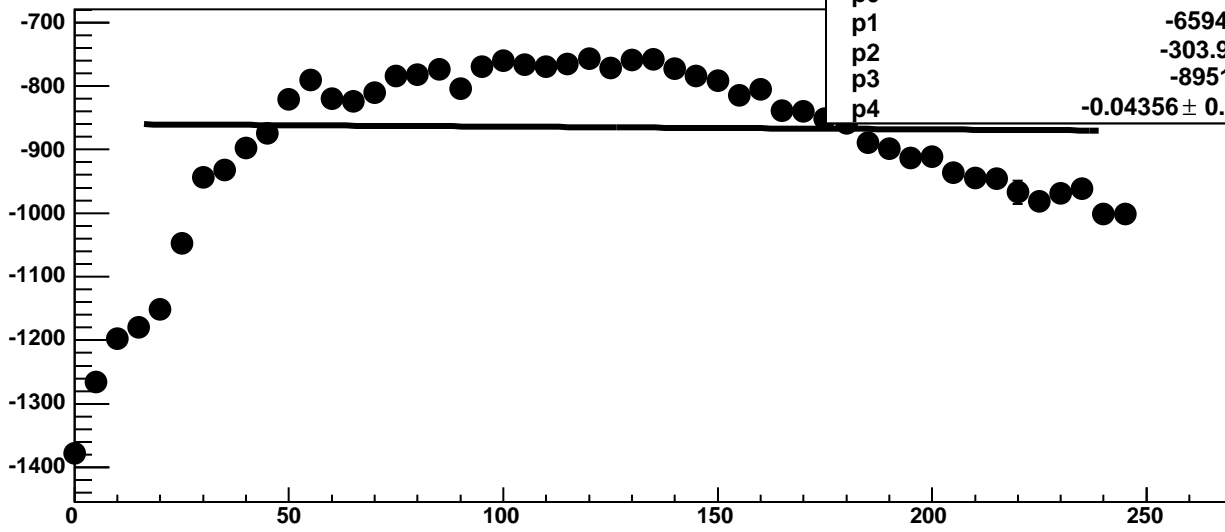


Chip 5, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold



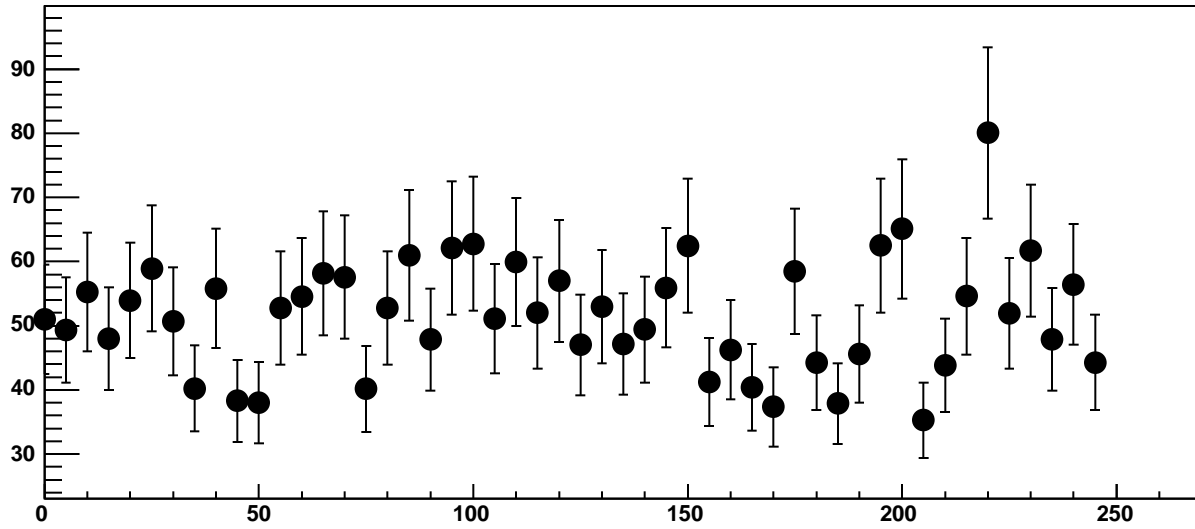


Chip 5, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

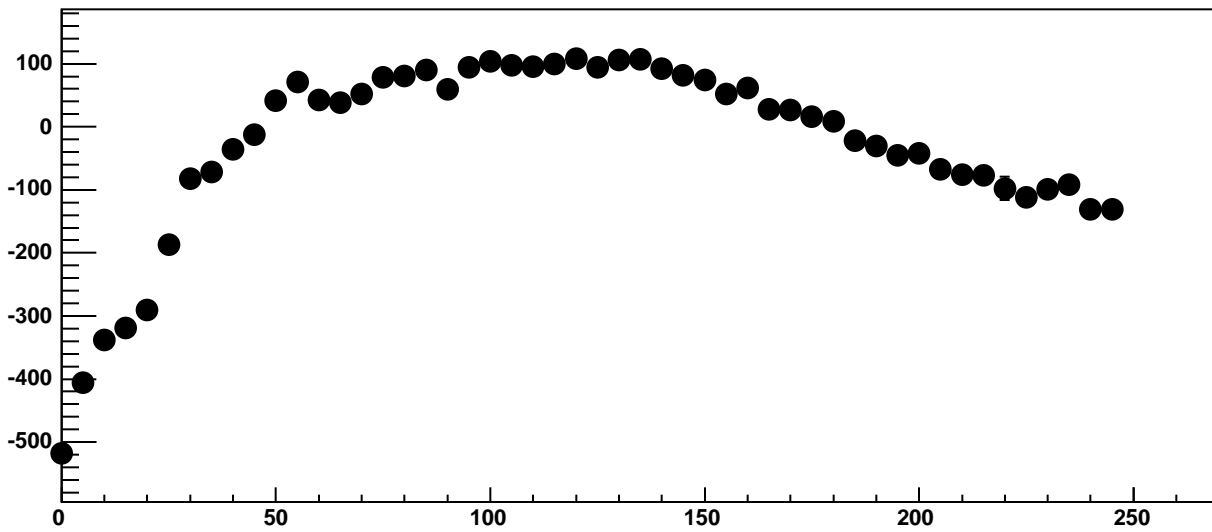


$\chi^2 / \text{ndf}$	3336 / 41
p0	-268.5 ± 4.852
p1	-6594 ± 291.2
p2	-303.9 ± 4.049
p3	-8951 ± 3104
p4	-0.04356 ± 0.0007221

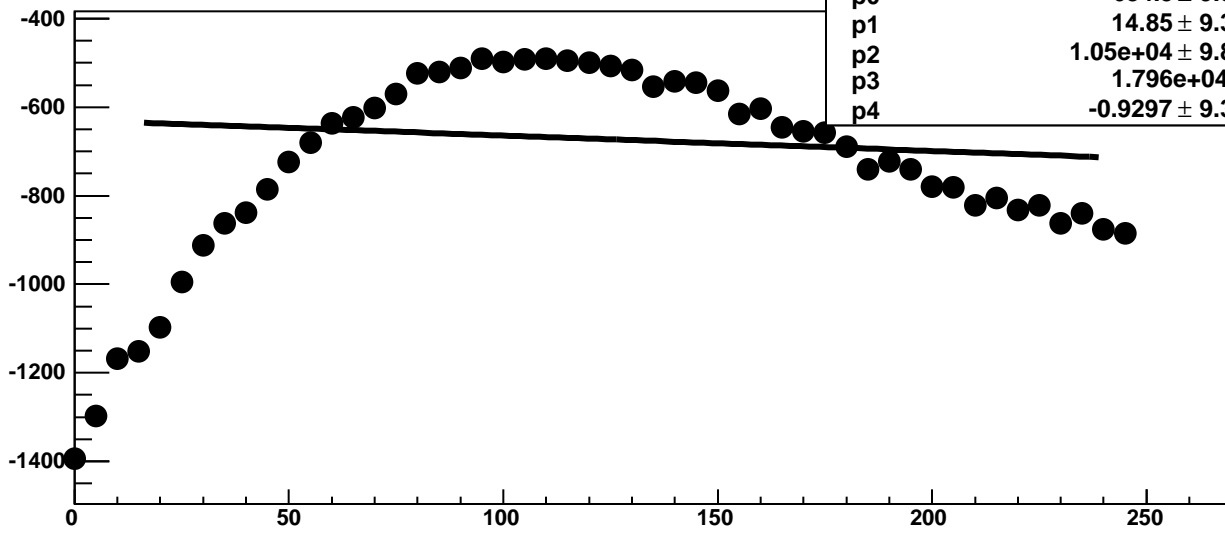
Chip 5, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

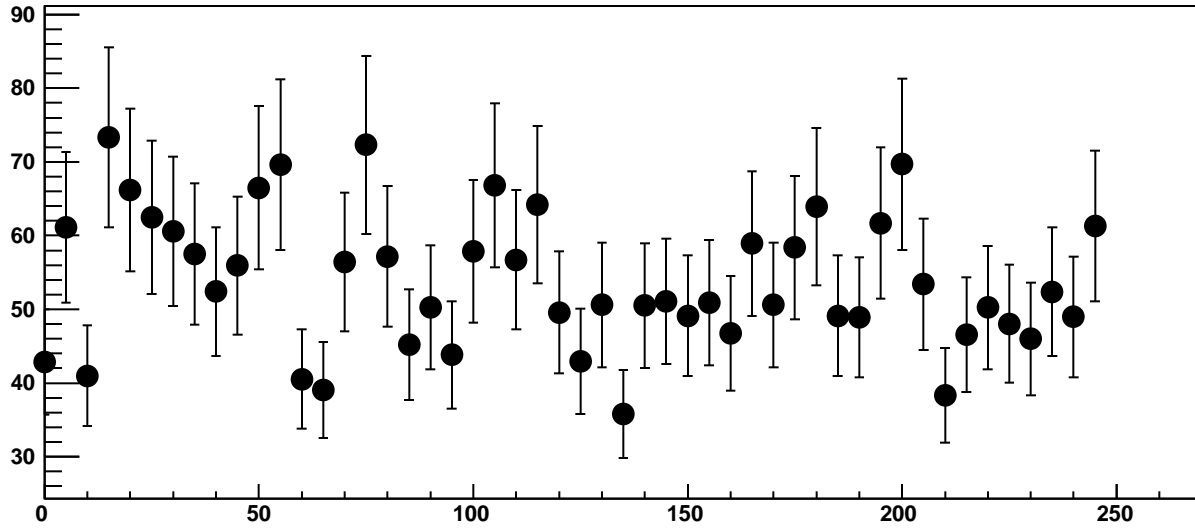


Chip 5, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold

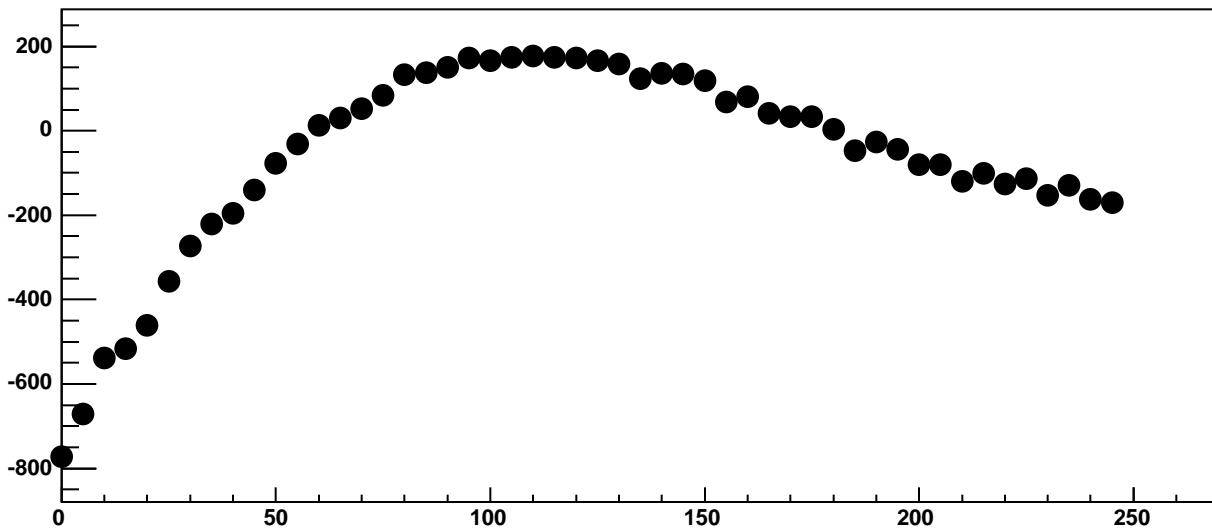


$\chi^2 / \text{ndf}$	7523 / 41
p0	$-634.5 \pm 9.357e+04$
p1	$14.85 \pm 9.357e+04$
p2	$1.05e+04 \pm 9.859e+04$
p3	$1.796e+04 \pm 12.26$
p4	$-0.9297 \pm 9.357e+04$

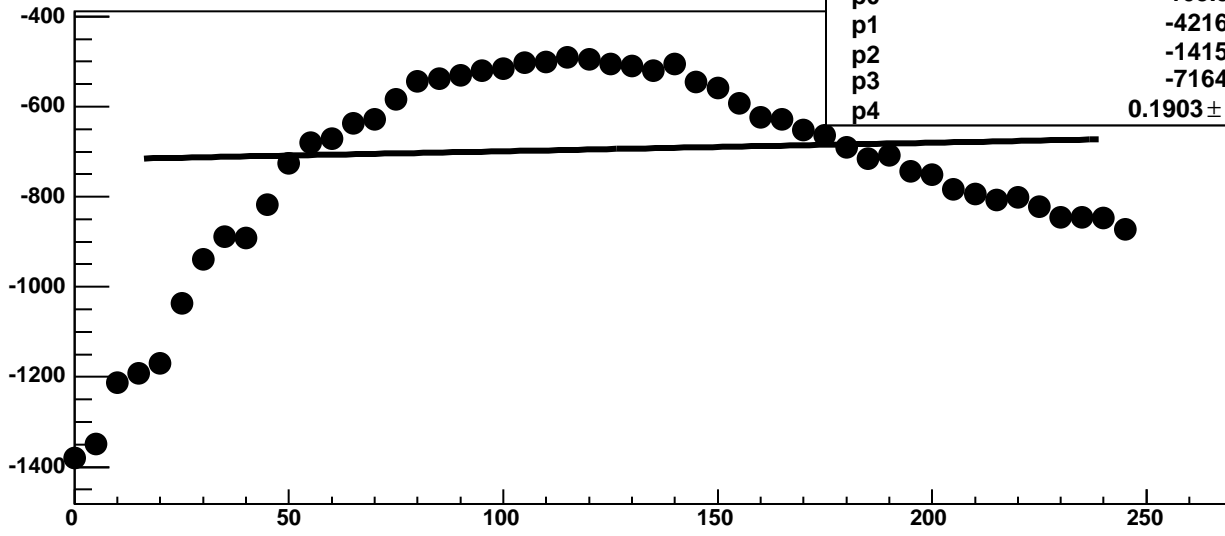
Chip 5, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold

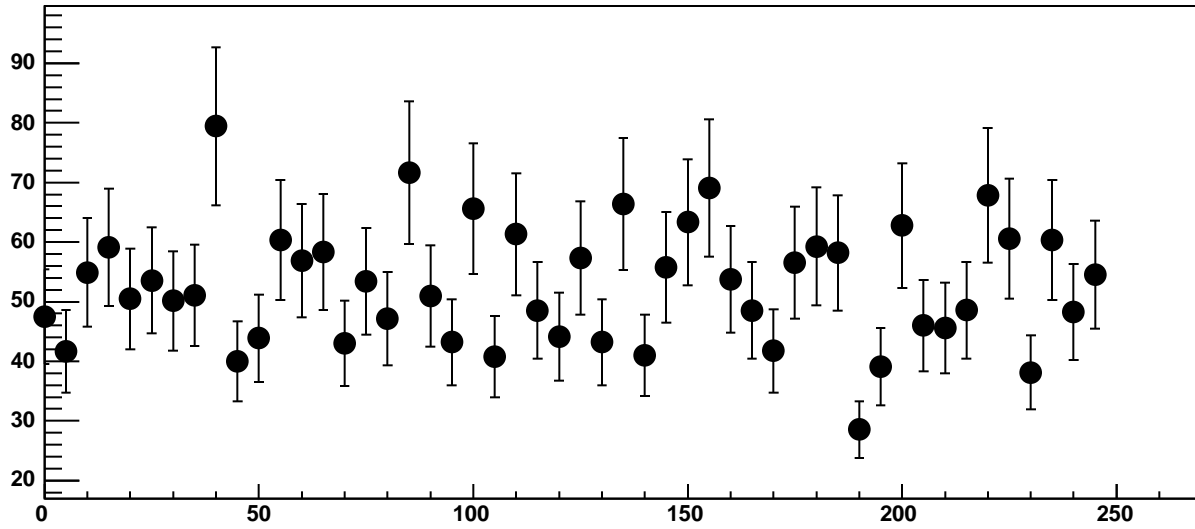


Chip 5, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

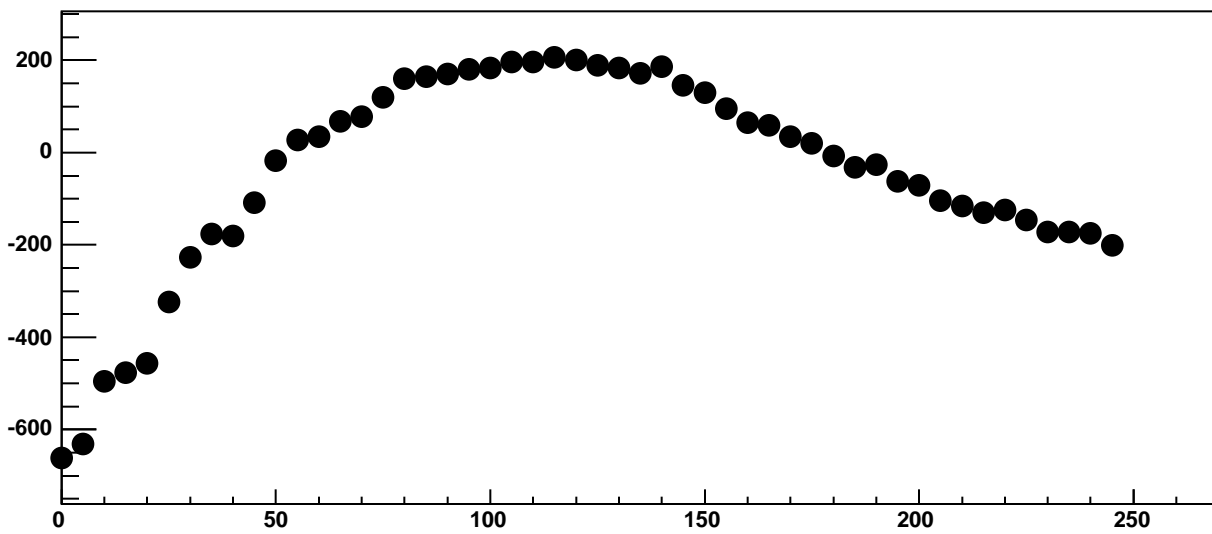


$\chi^2 / \text{ndf}$	9739 / 41
p0	$-105.3 \pm 10.26$
p1	$-4216 \pm 17.29$
p2	$-1415 \pm 10.26$
p3	$-7164 \pm 532.4$
p4	$0.1903 \pm 0.00236$

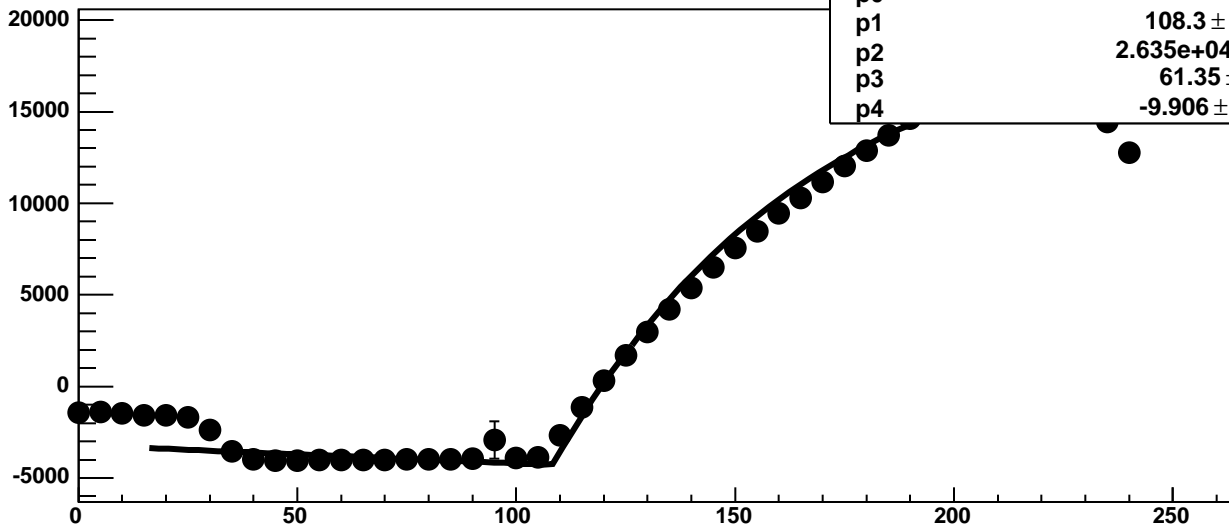
Chip 5, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

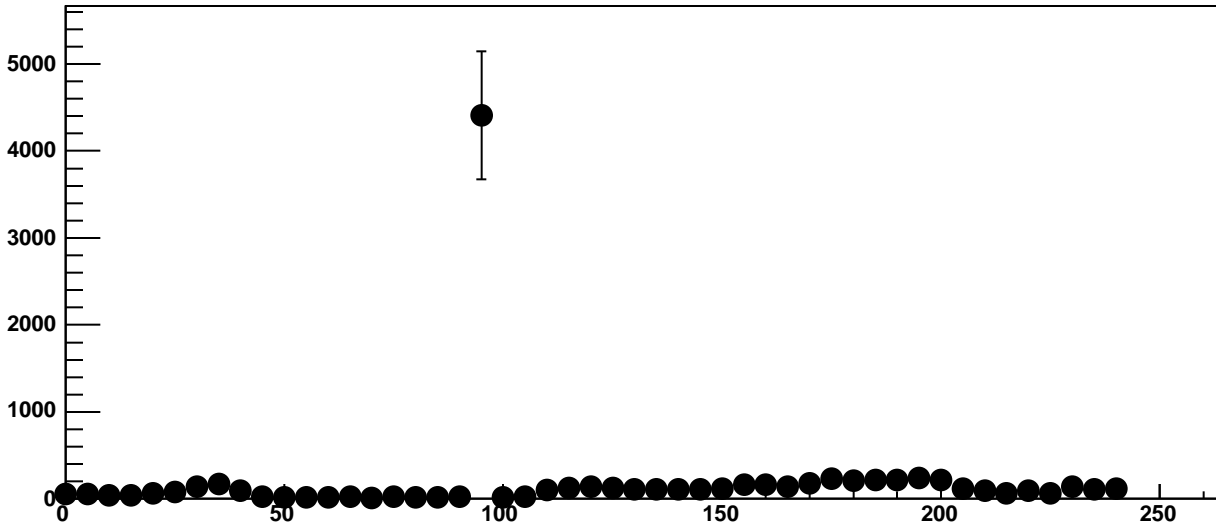


Chip 5, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

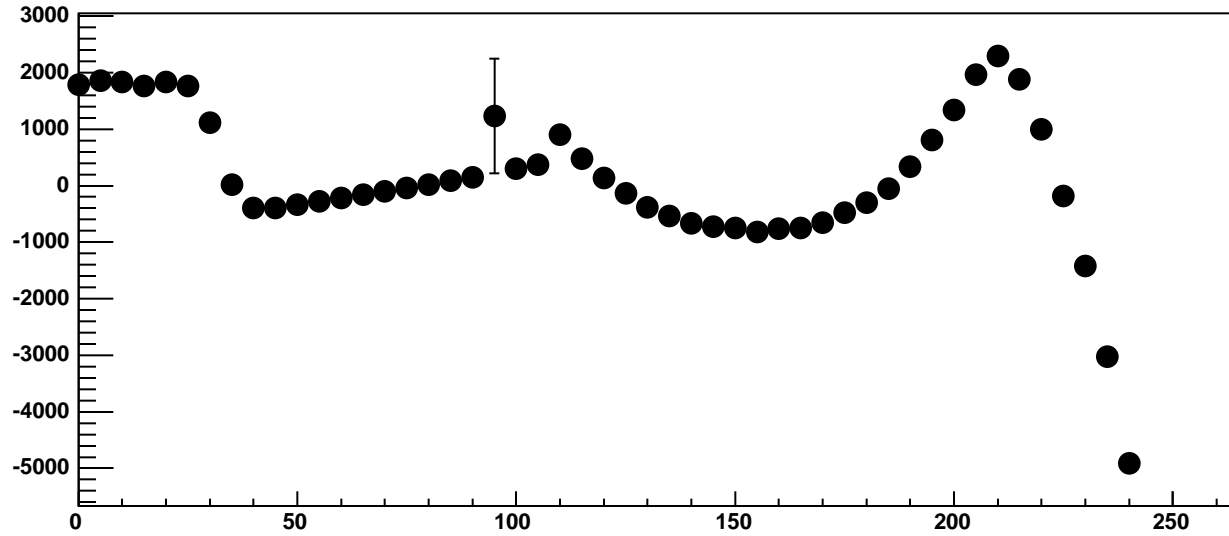


$\chi^2 / \text{ndf}$	1.77e+05 / 41
p0	-4284 ± 2.902
p1	108.3 ± 0.04286
p2	2.635e+04 ± 32.08
p3	61.35 ± 0.1798
p4	-9.906 ± 0.06821

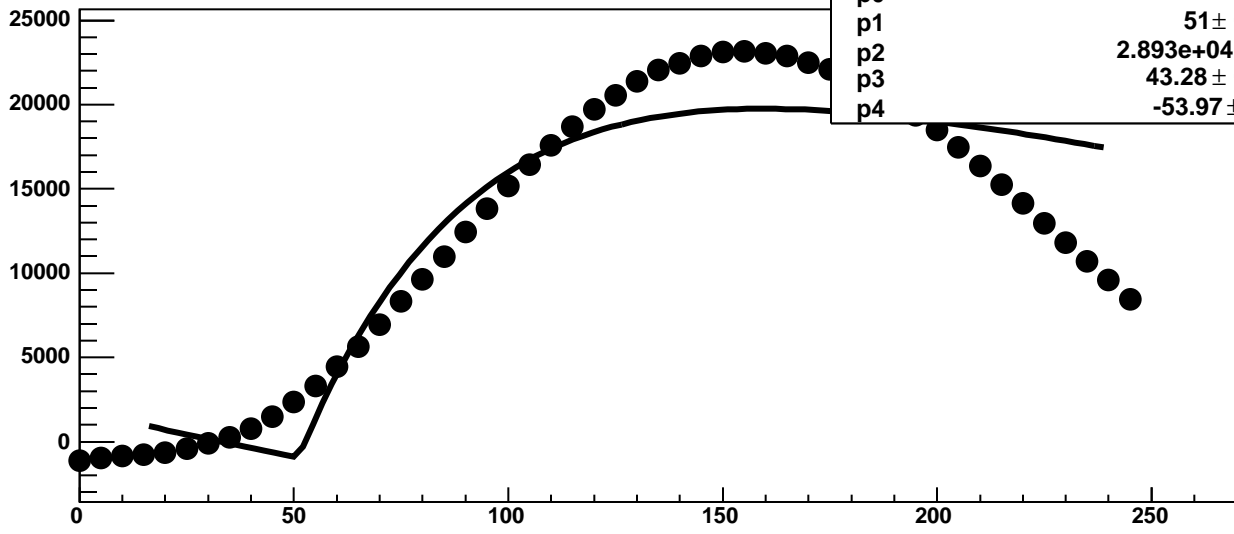
Chip 5, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold

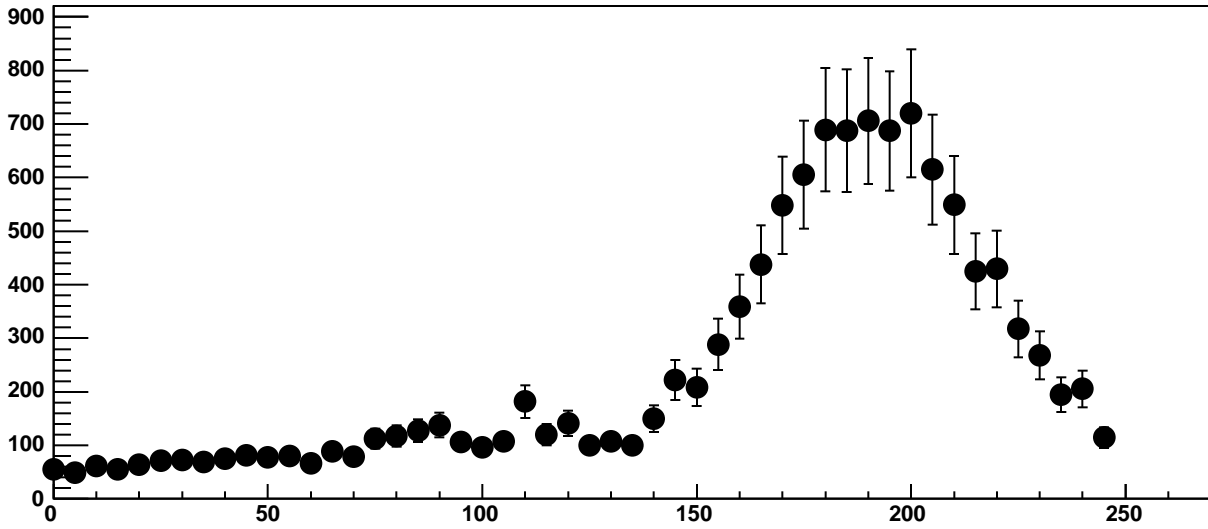


Chip 5, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold

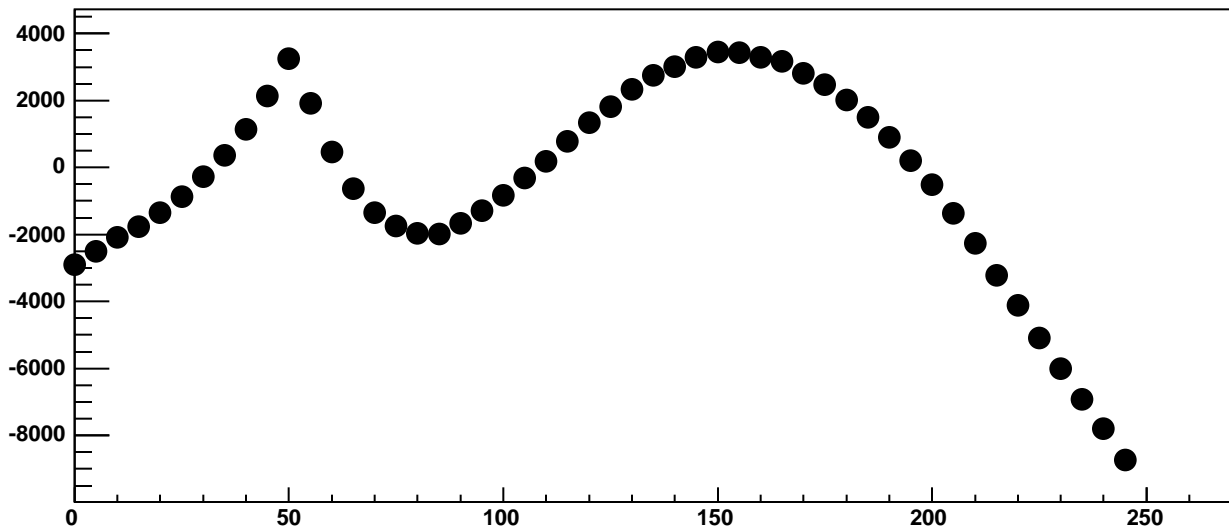


$\chi^2 / \text{ndf}$	2.469e+05 / 41
p0	-965.5 ± 8.018
p1	51 ± 0.02543
p2	2.893e+04 ± 55.28
p3	43.28 ± 0.09313
p4	-53.97 ± 0.3037

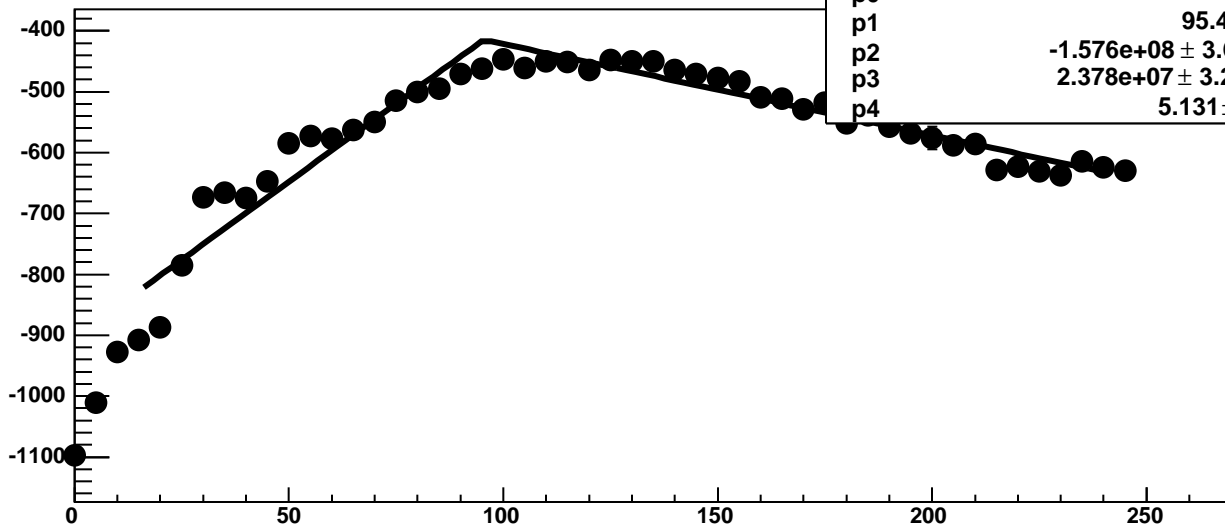
Chip 5, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold

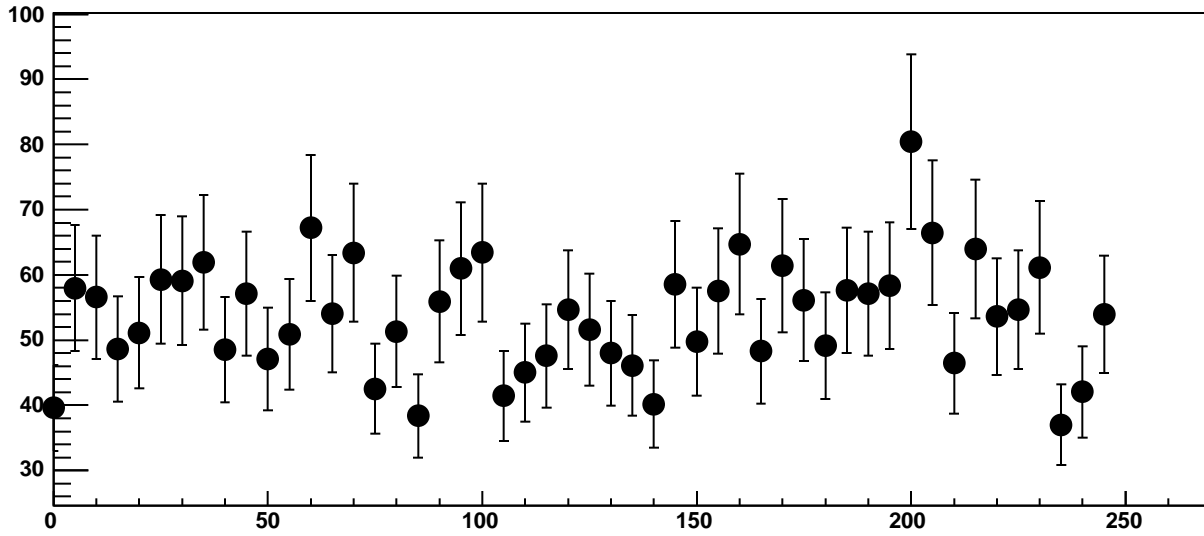


Chip 5, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

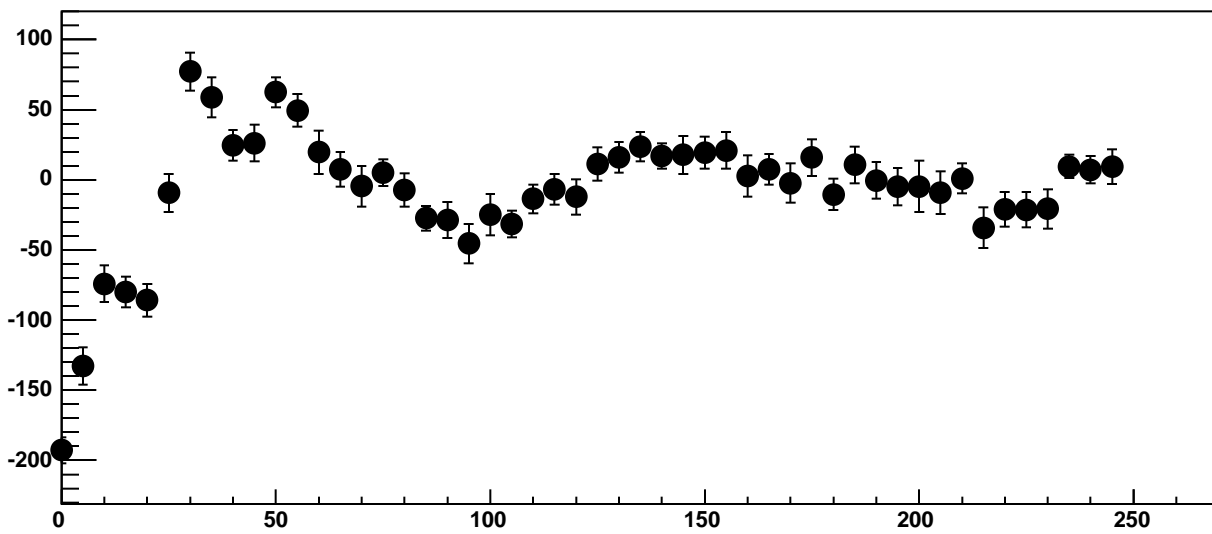


$\chi^2 / \text{ndf}$	298 / 41
p0	$-414.8 \pm 3.498$
p1	$95.4 \pm 1.037$
p2	$-1.576\text{e}+08 \pm 3.673\text{e}+06$
p3	$2.378\text{e}+07 \pm 3.243\text{e}+05$
p4	$5.131 \pm 0.1174$

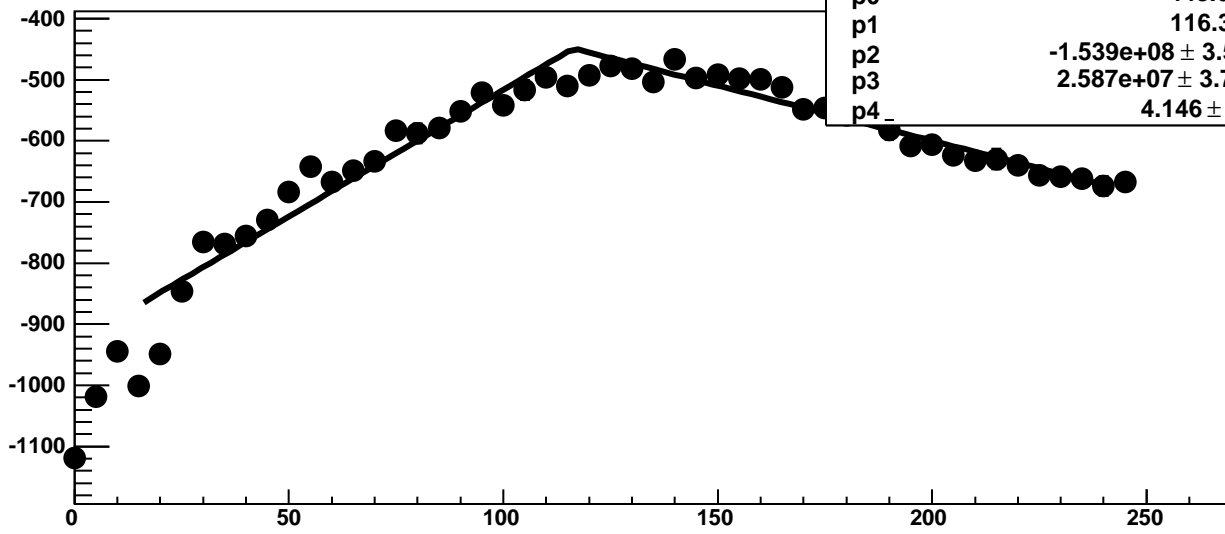
Chip 5, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



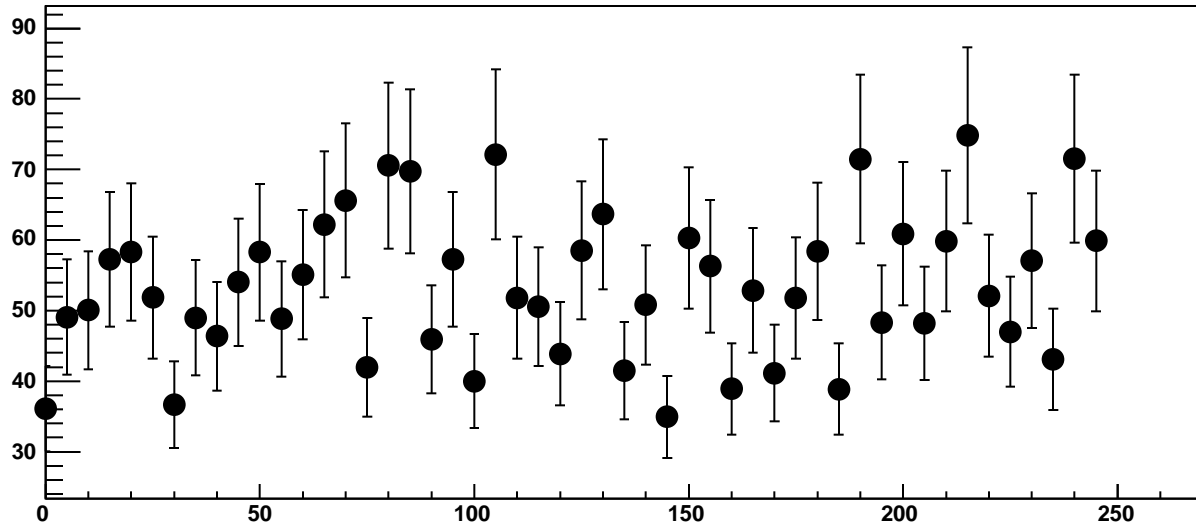
Chip 5, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold



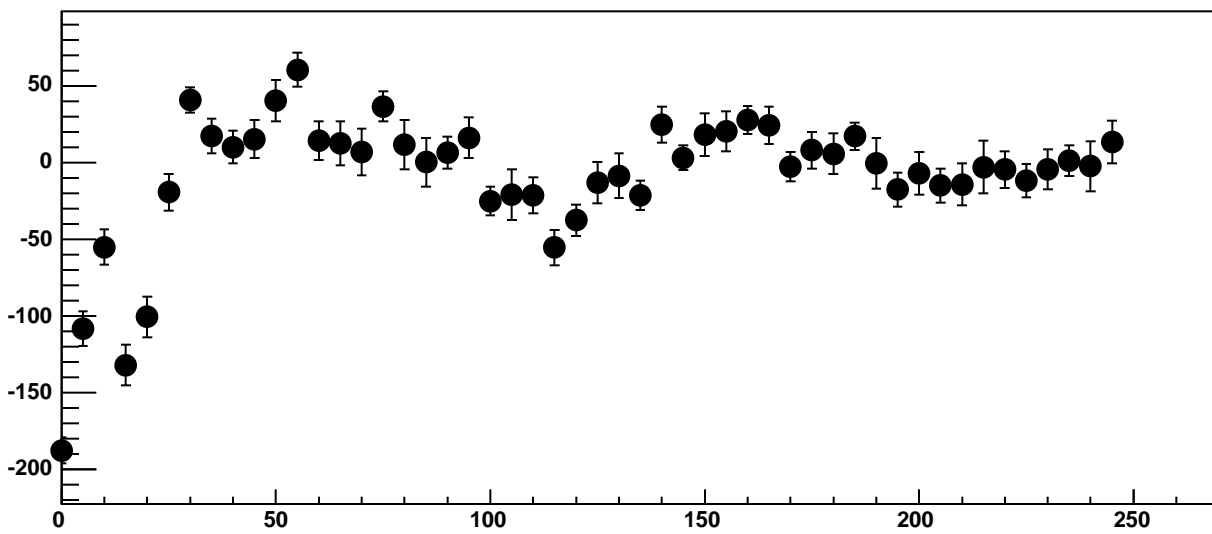
Chip 5, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold



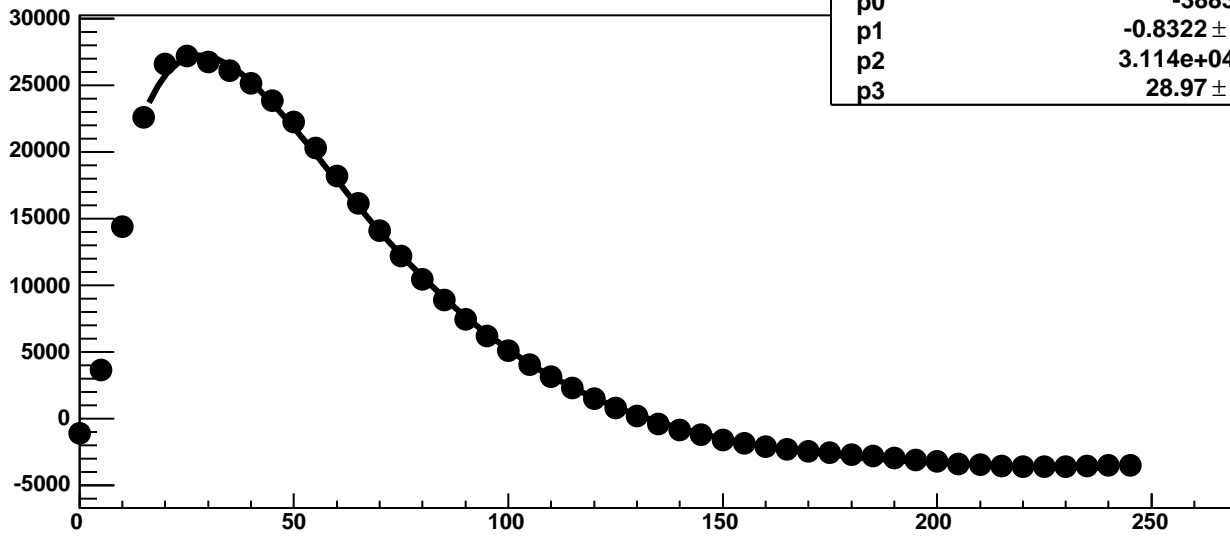
Chip 5, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

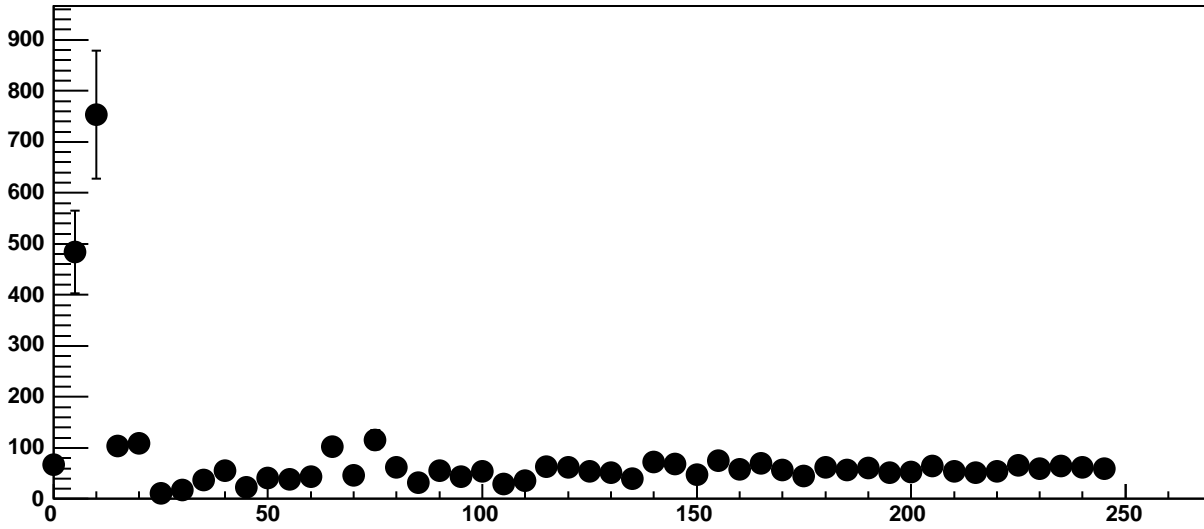


Chip 5, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

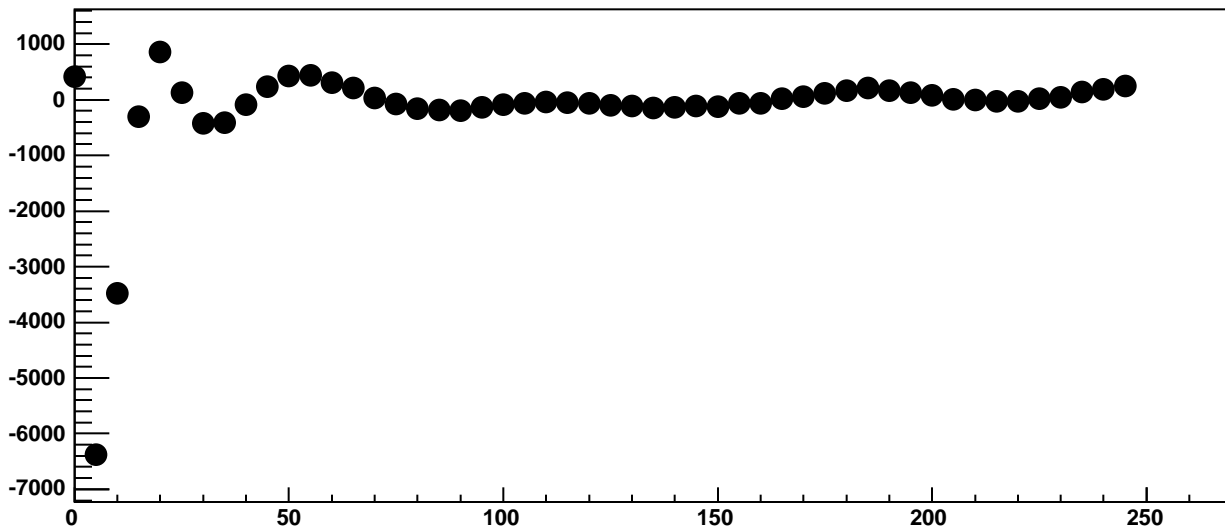


$\chi^2 / \text{ndf}$	2.879e+04 / 42
p0	-3883 ± 3.664
p1	-0.8322 ± 0.01852
p2	3.114e+04 ± 3.897
p3	28.97 ± 0.01007

Chip 5, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

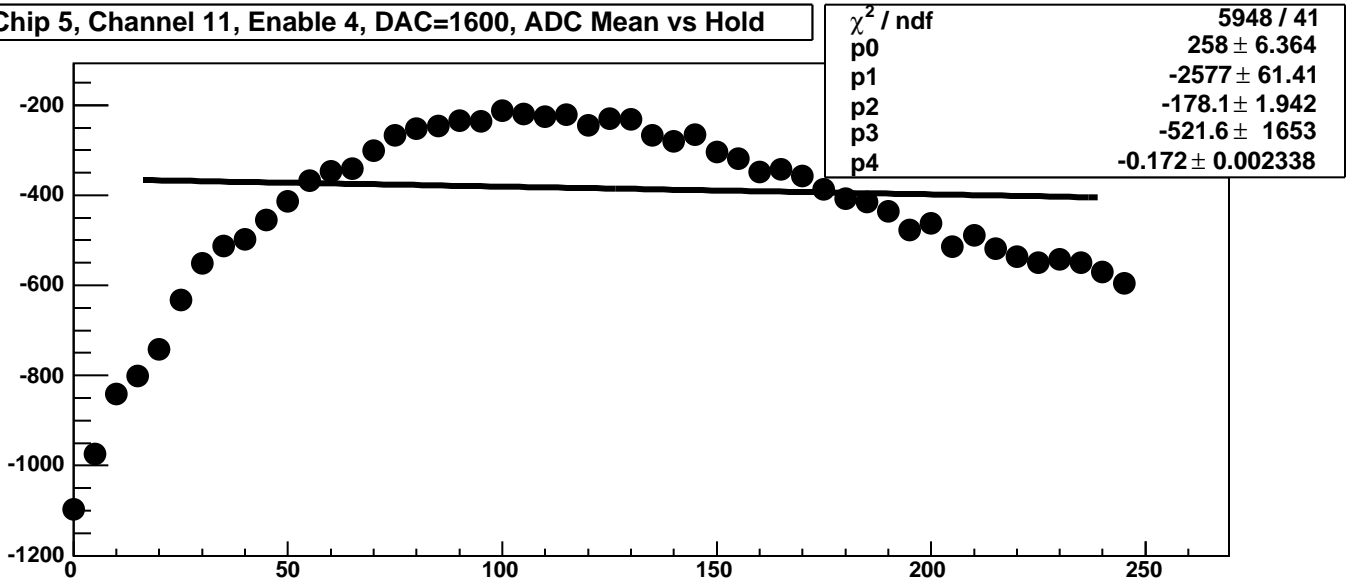


Chip 5, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold

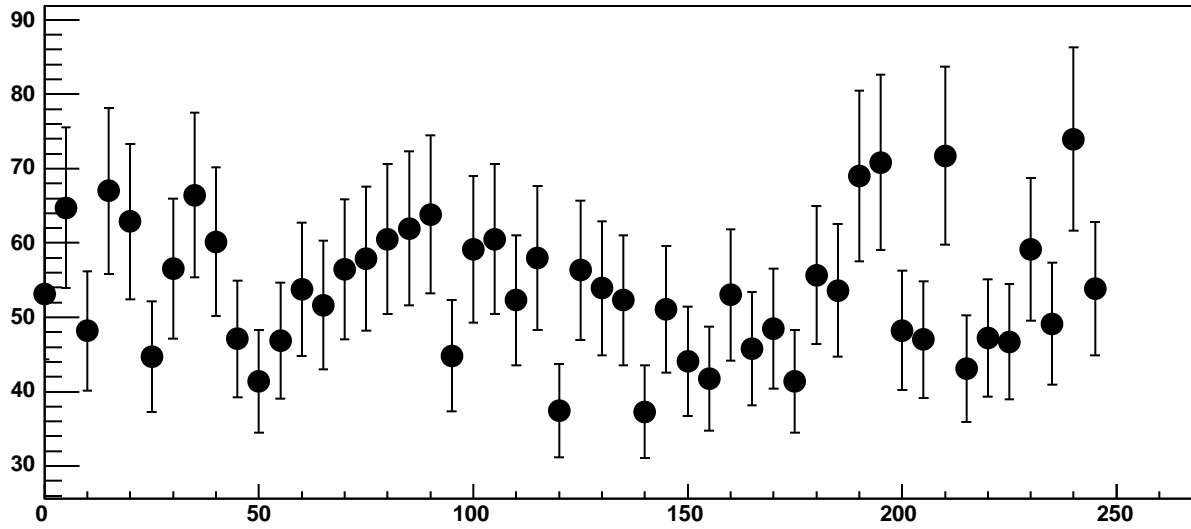




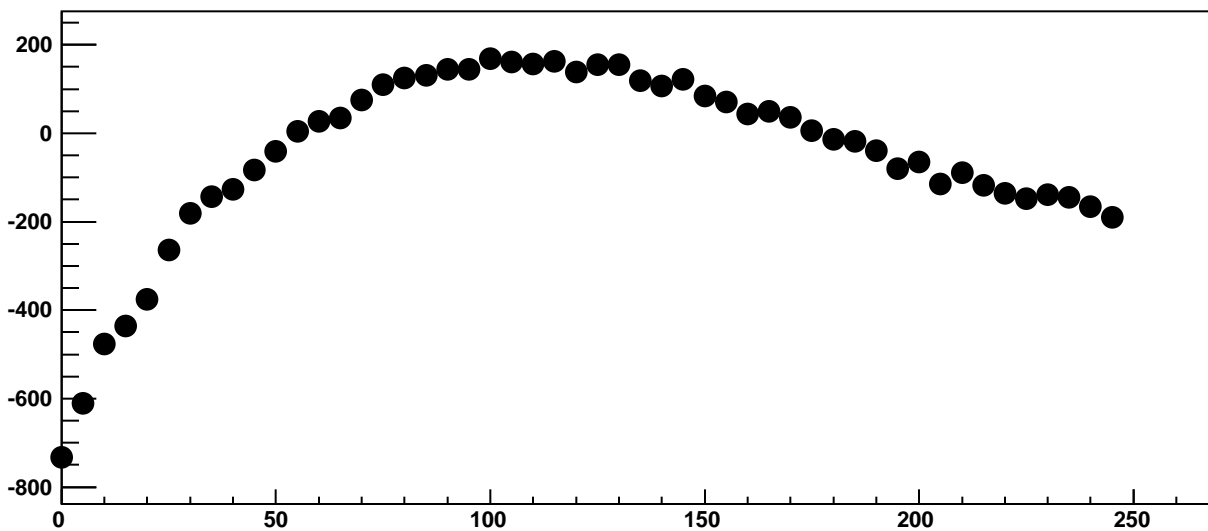
Chip 5, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold



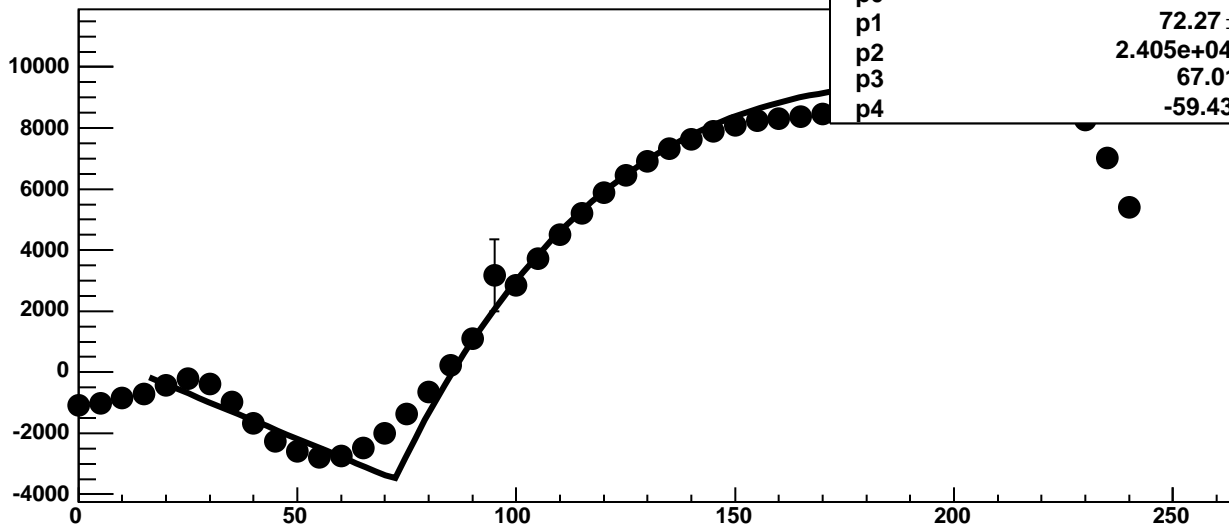
Chip 5, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

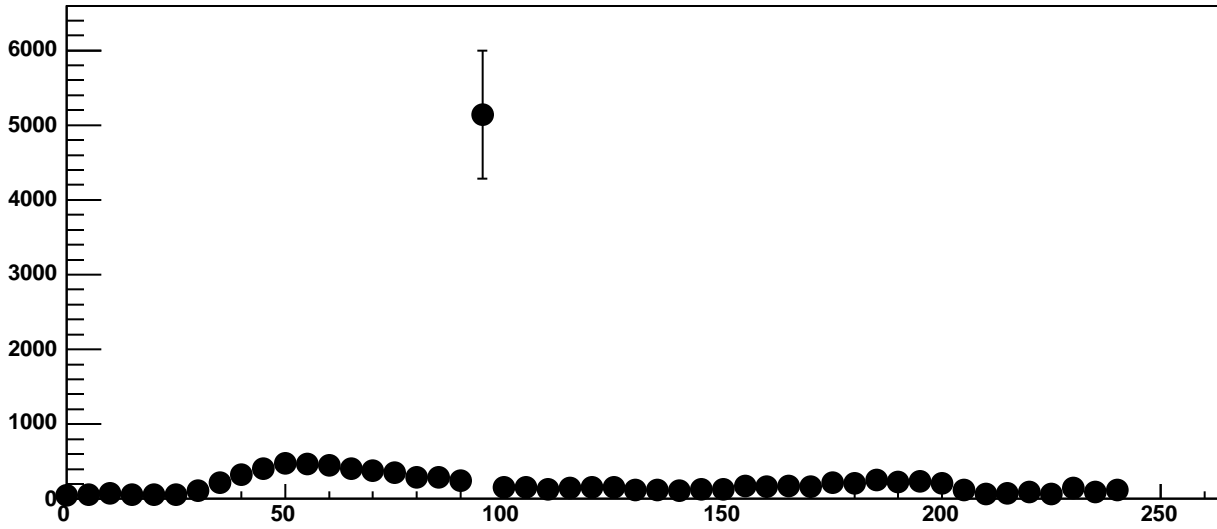


Chip 5, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

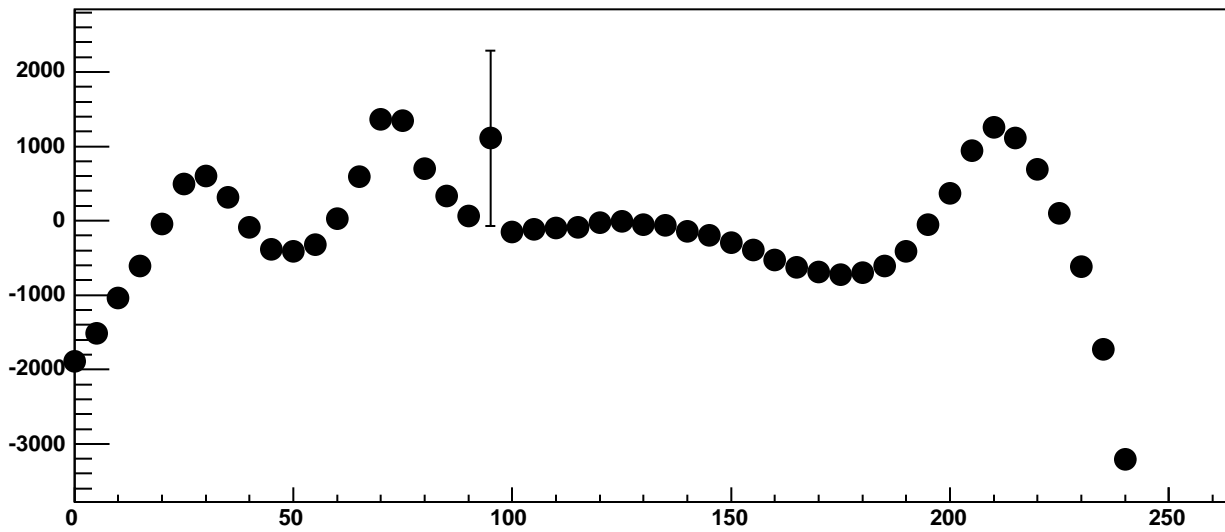


$\chi^2 / \text{ndf}$	3.908e+04 / 41
p0	-3503 ± 27.93
p1	72.27 ± 0.1503
p2	2.405e+04 ± 176.7
p3	67.01 ± 0.431
p4	-59.43 ± 0.652

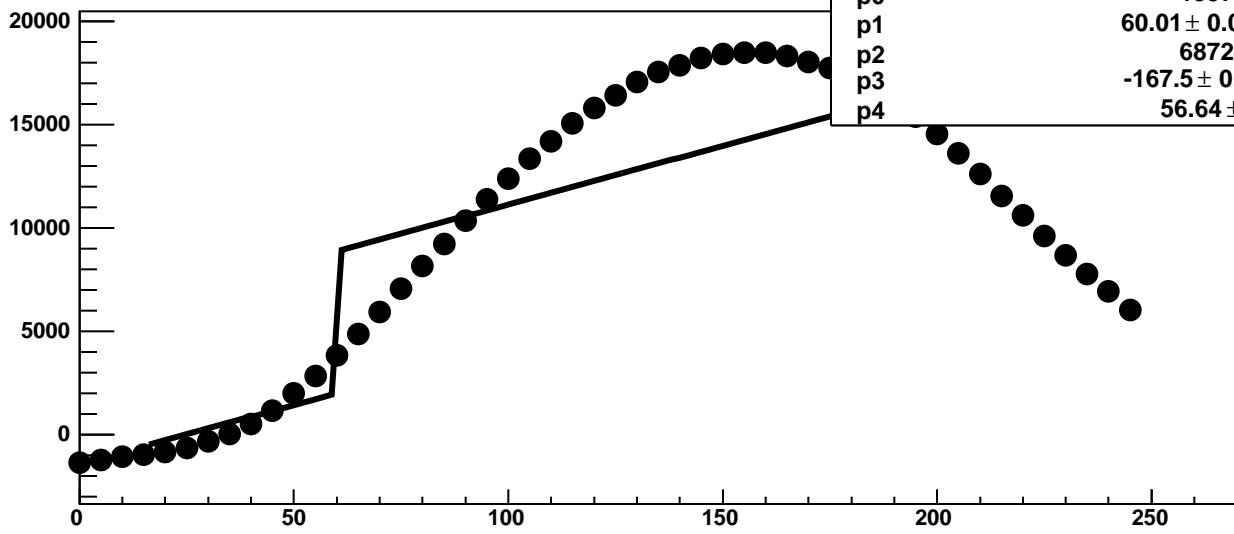
Chip 5, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

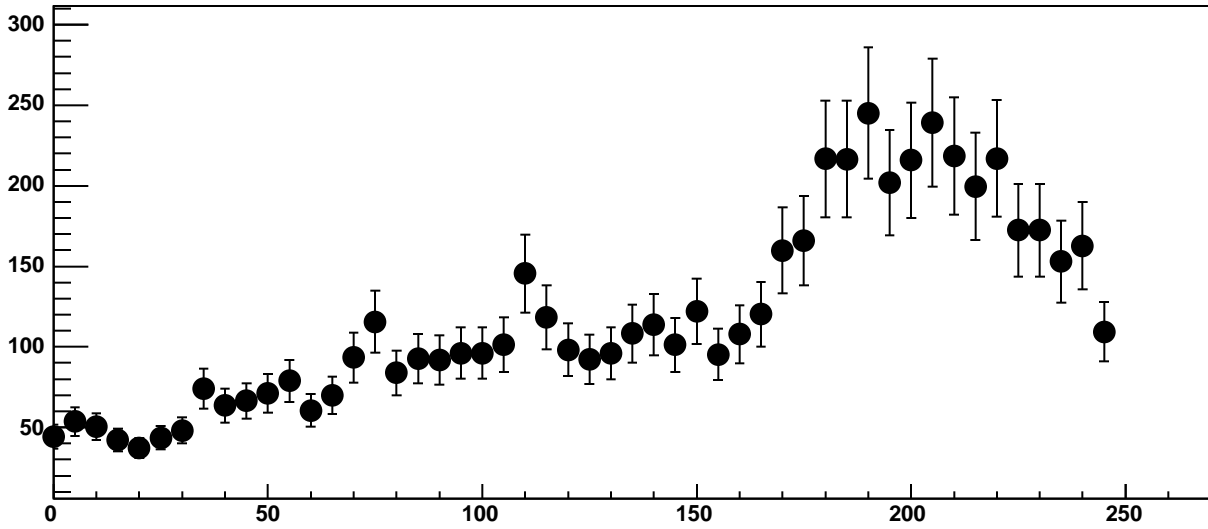


Chip 5, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold

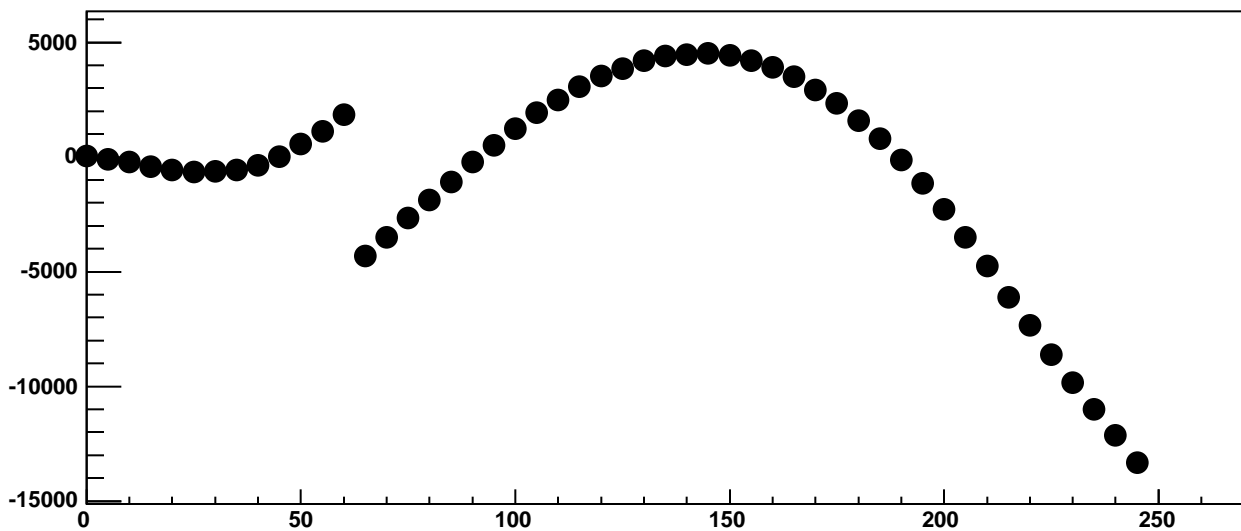


$\chi^2 / \text{ndf}$	8.646e+05 / 41
p0	1997 ± 3.676
p1	60.01 ± 0.0002177
p2	6872 ± 4.416
p3	-167.5 ± 0.002554
p4	56.64 ± 0.1223

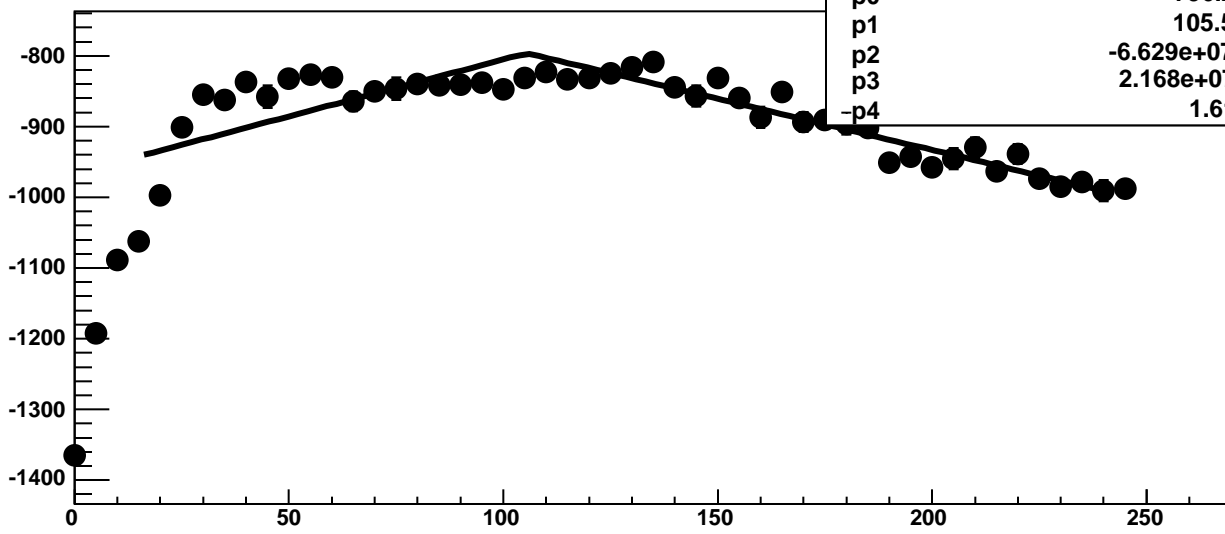
Chip 5, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

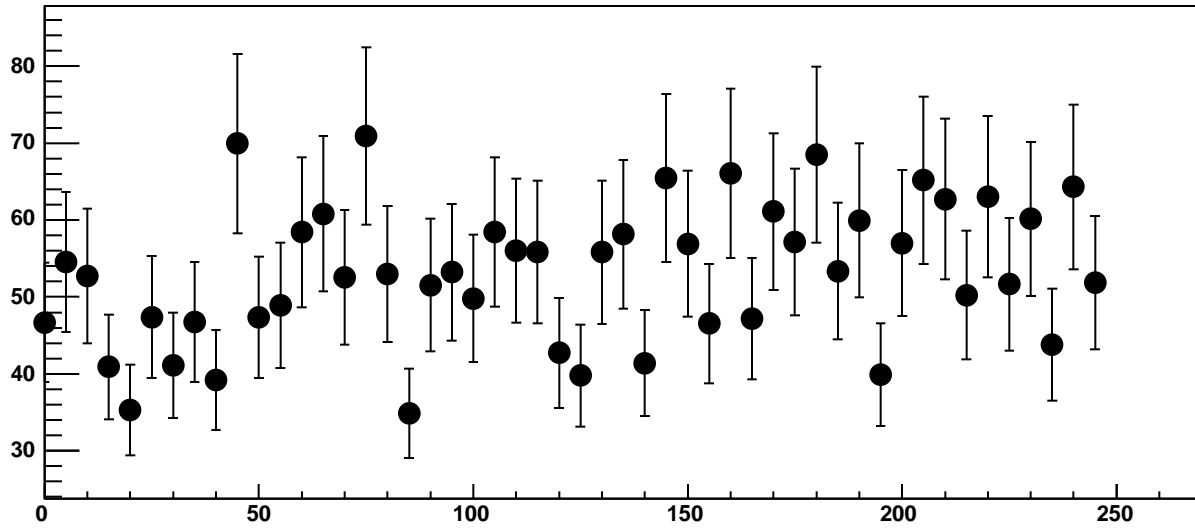


Chip 5, Channel 12, Enable 1, DAC=1600, ADC Mean vs Hold

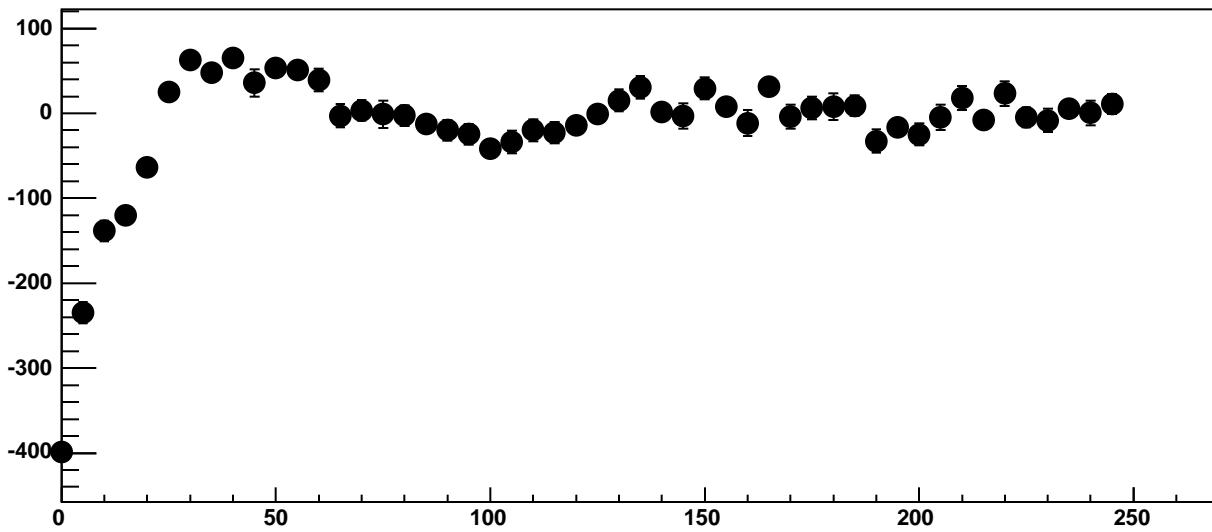


$\chi^2 / \text{ndf}$	483.7 / 41
p0	-796.2 ± nan
p1	105.5 ± nan
p2	-6.629e+07 ± nan
p3	2.168e+07 ± nan
p4	1.61 ± nan

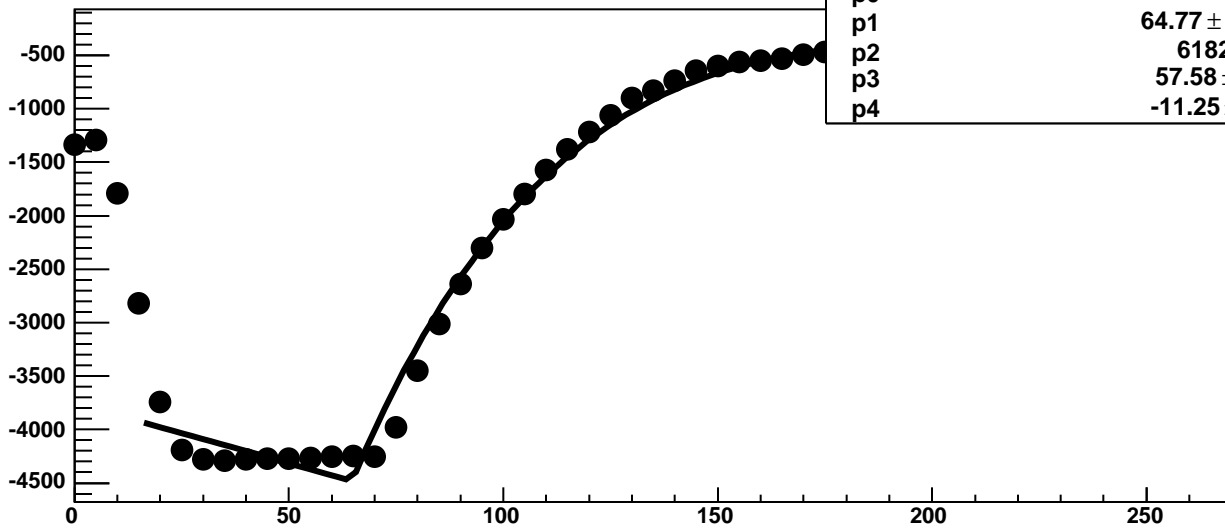
Chip 5, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold



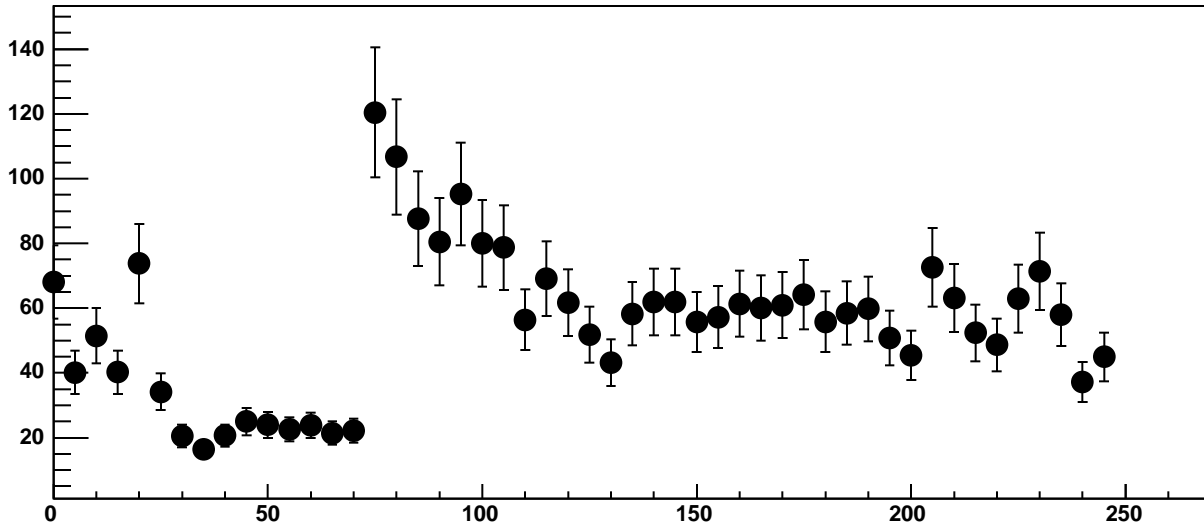
Chip 5, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold



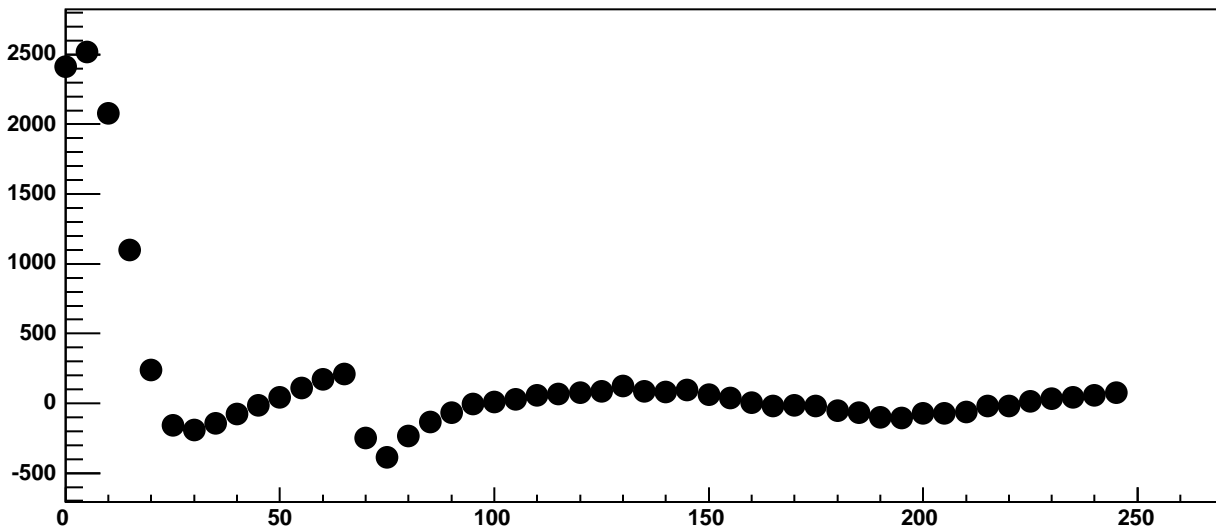
Chip 5, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold



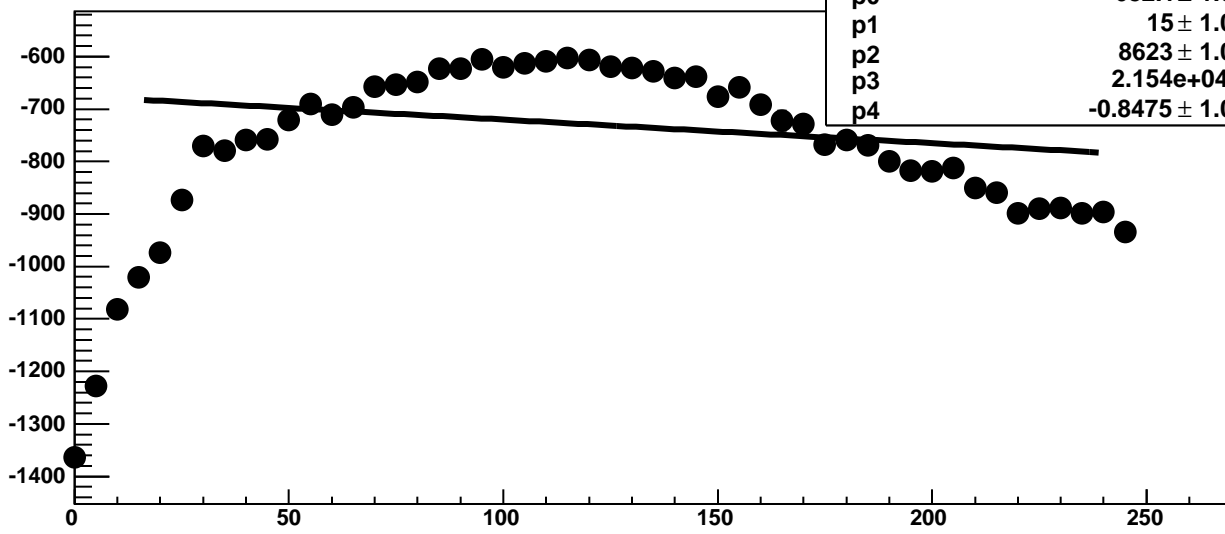
Chip 5, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

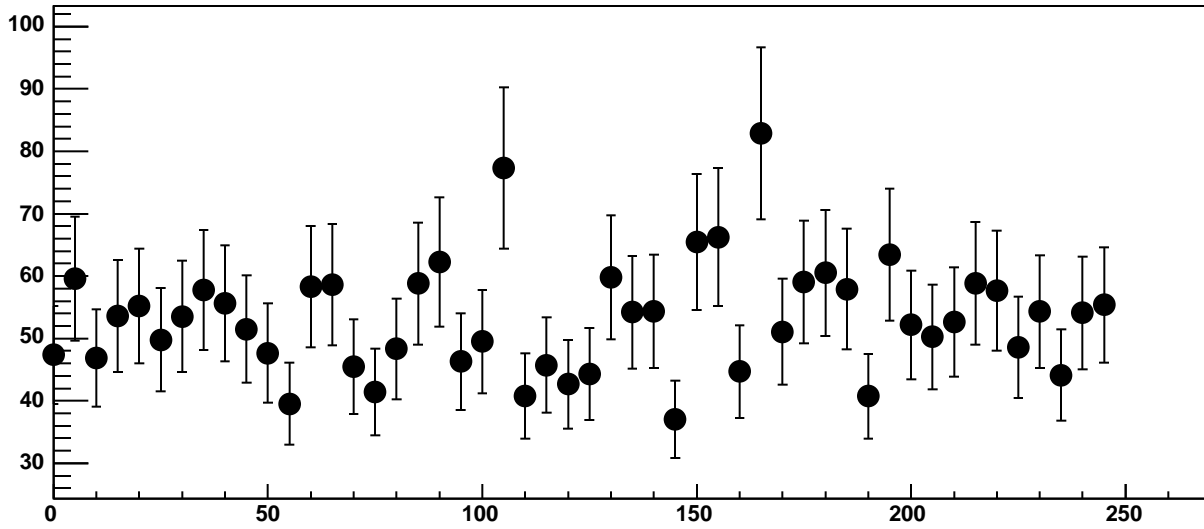


Chip 5, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

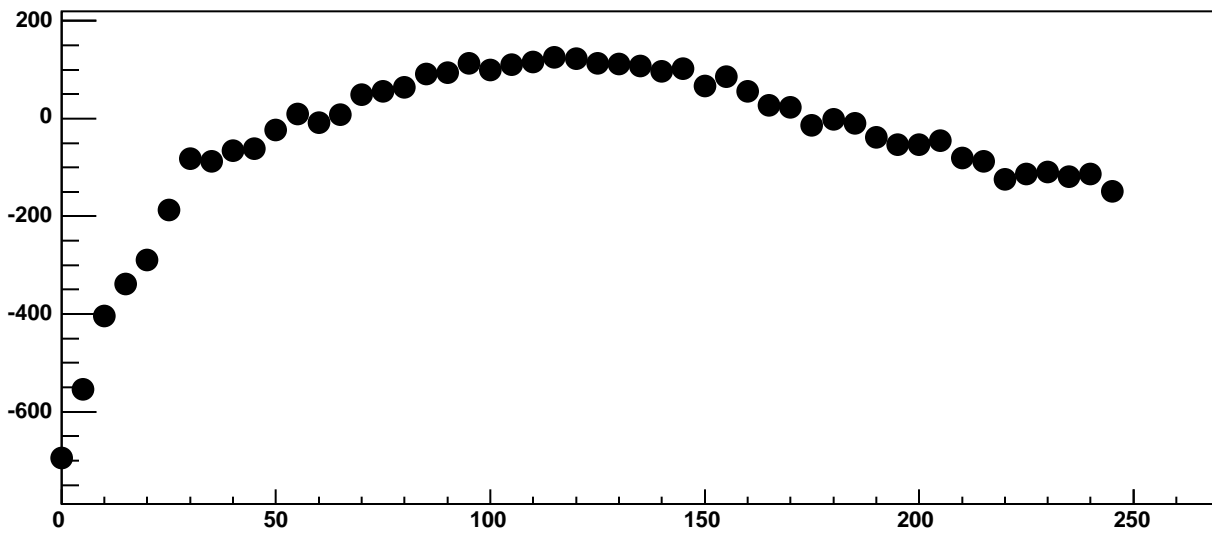


$\chi^2 / \text{ndf}$	3754 / 41
p0	$-682.1 \pm 1.065e+05$
p1	$15 \pm 1.065e+05$
p2	$8623 \pm 1.095e+05$
p3	$2.154e+04 \pm 7.908$
p4	$-0.8475 \pm 1.065e+05$

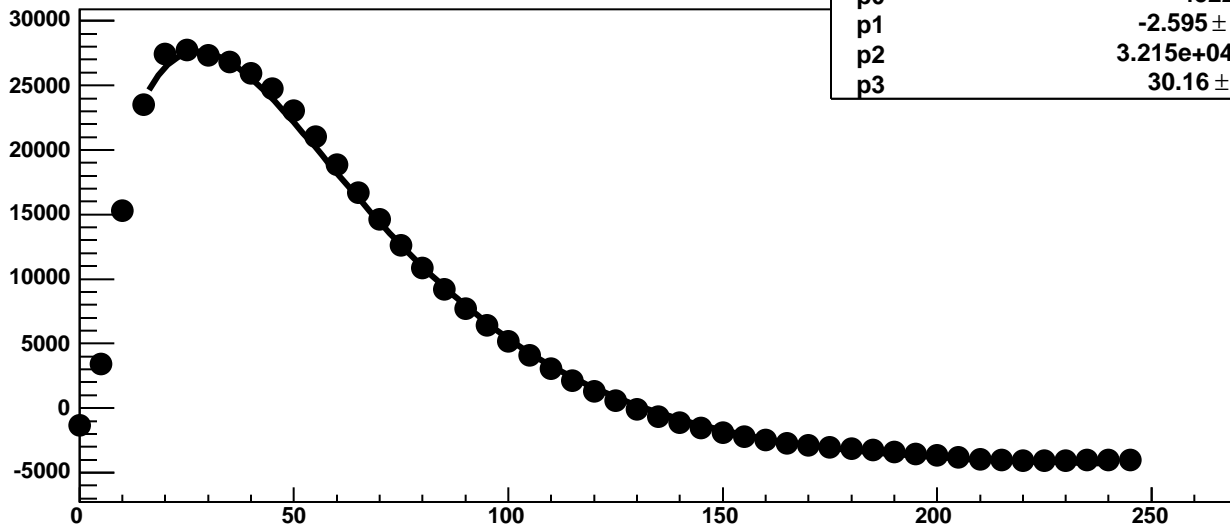
Chip 5, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



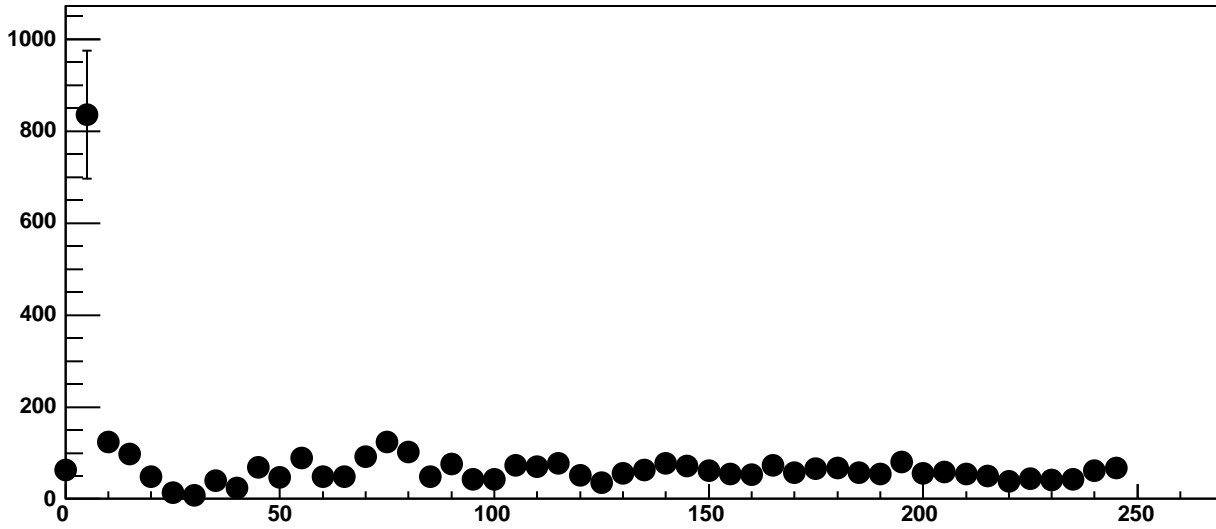
Chip 5, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold



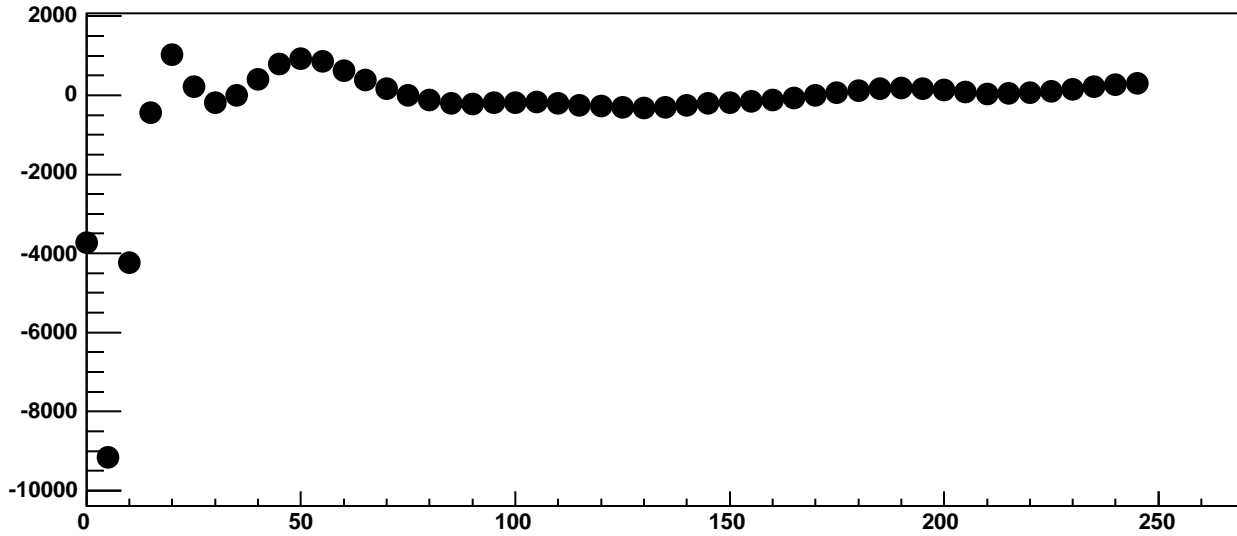
Chip 5, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold



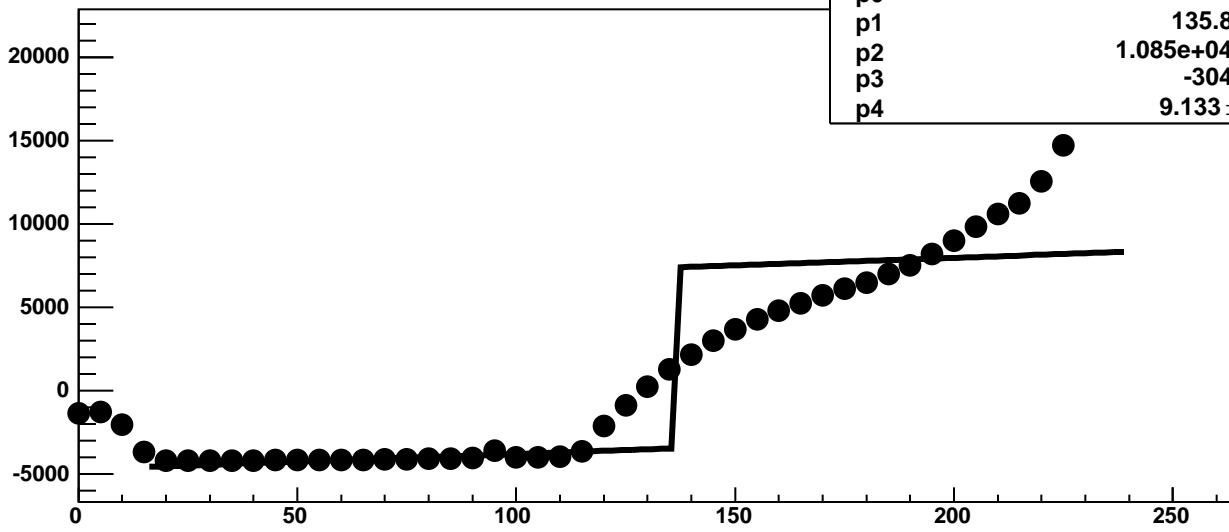
Chip 5, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold

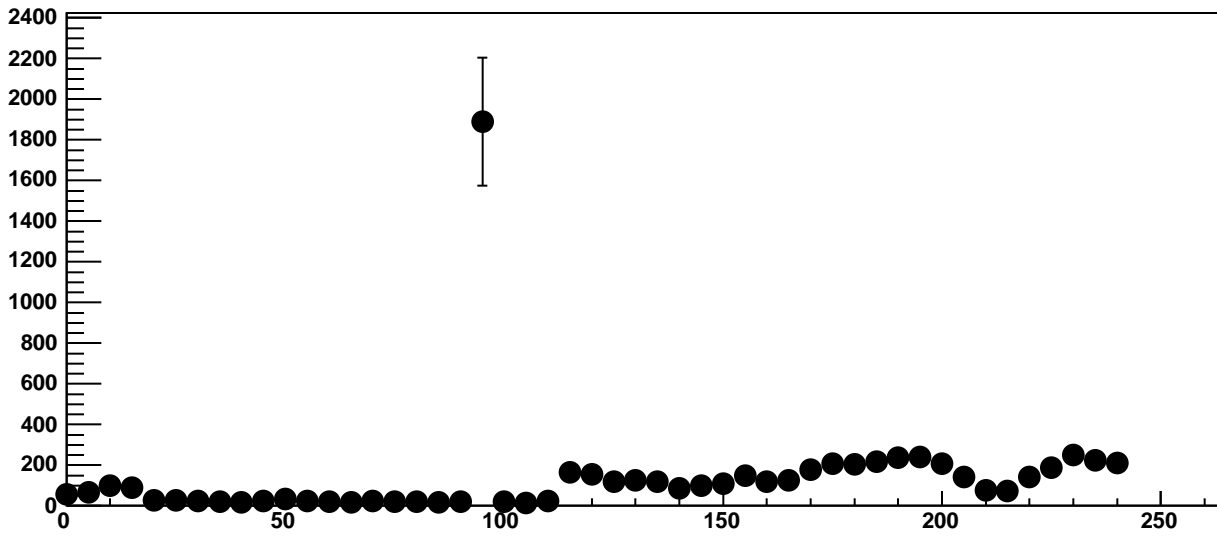


Chip 5, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

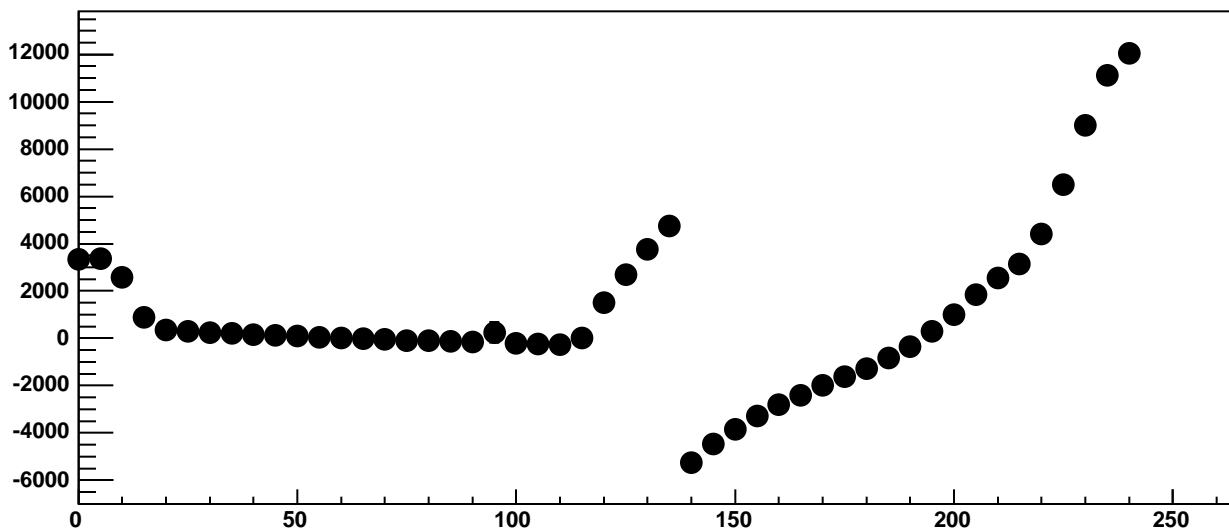


$\chi^2 / \text{ndf}$	4.788e+05 / 41
p0	-3466 ± 3.574
p1	135.8 ± 1.635
p2	1.085e+04 ± 5.734
p3	-304 ± 6.156
p4	9.133 ± 0.1138

Chip 5, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

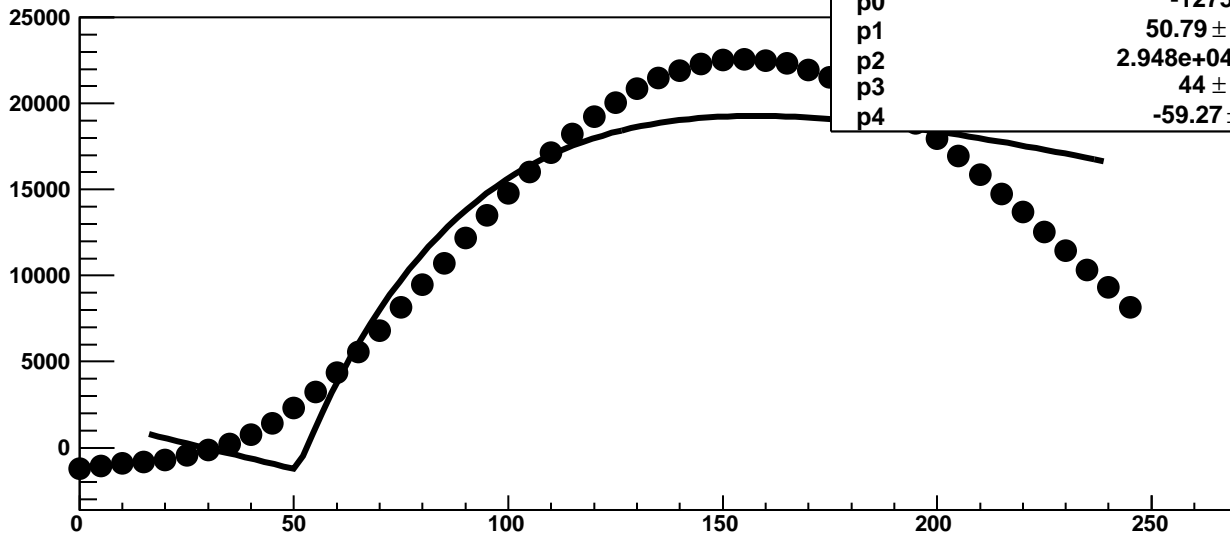


Chip 5, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



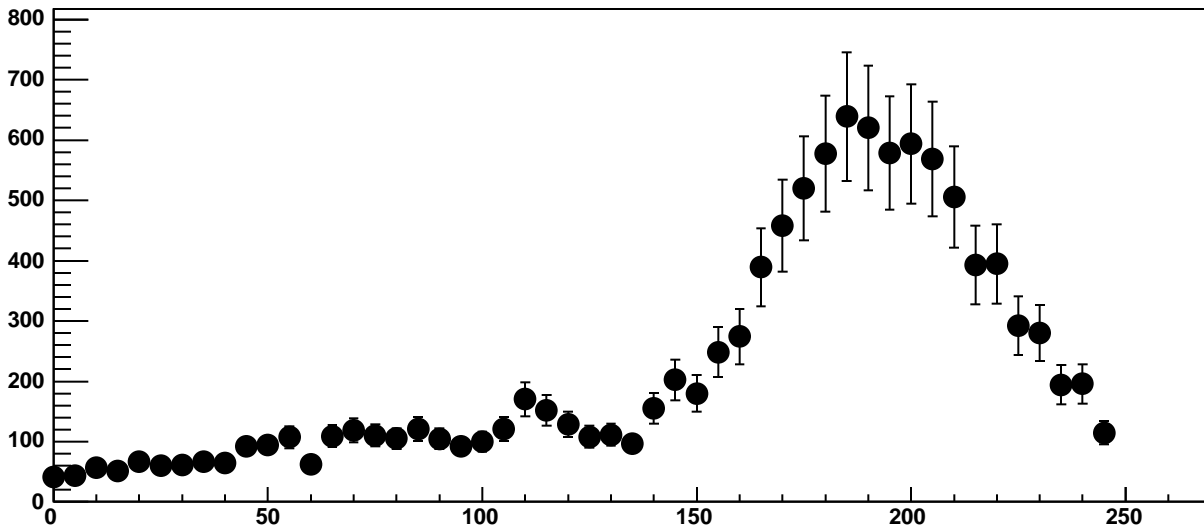


Chip 5, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

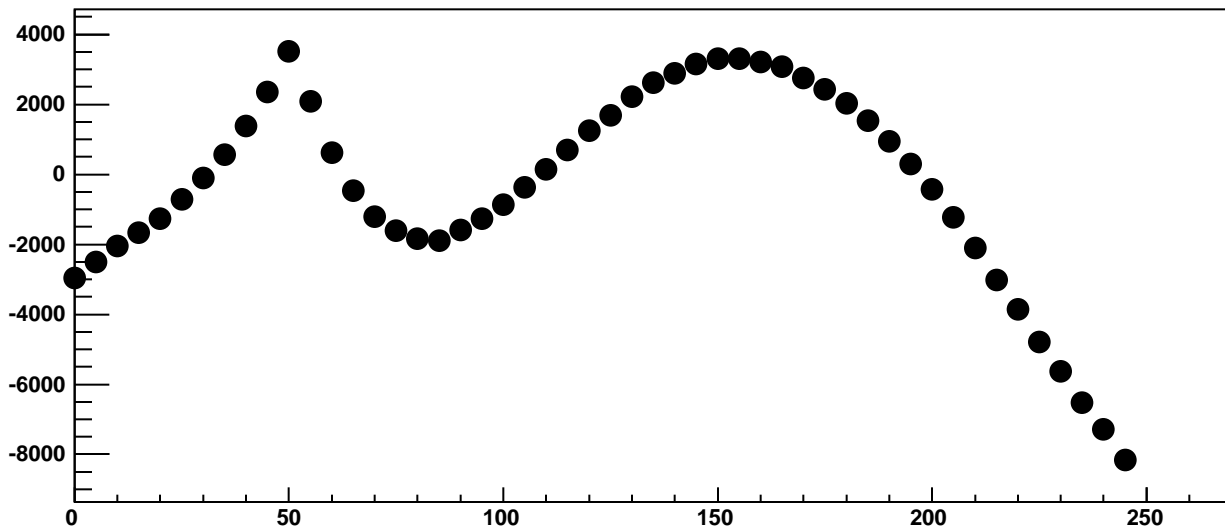


$\chi^2 / \text{ndf}$	2.321e+05 / 41
p0	-1275 ± 7.863
p1	50.79 ± 0.02818
p2	2.948e+04 ± 57.48
p3	44 ± 0.09827
p4	-59.27 ± 0.3079

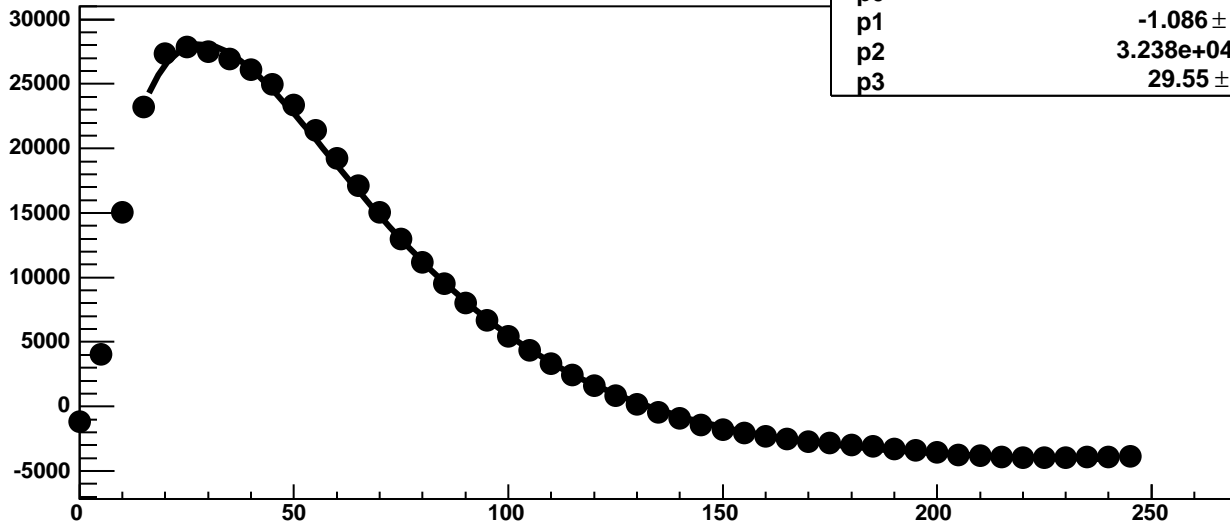
Chip 5, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



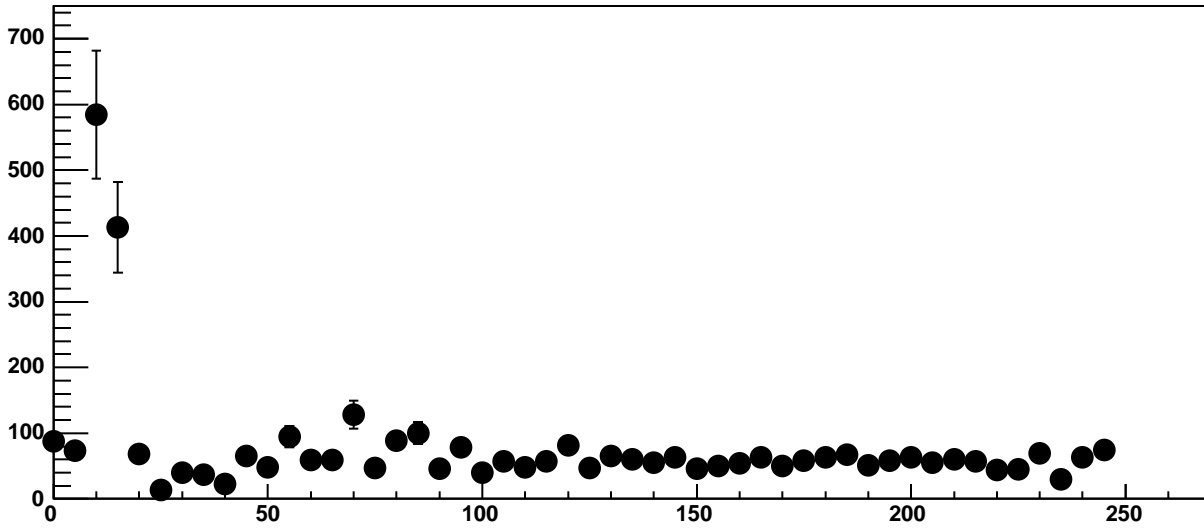
Chip 5, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold



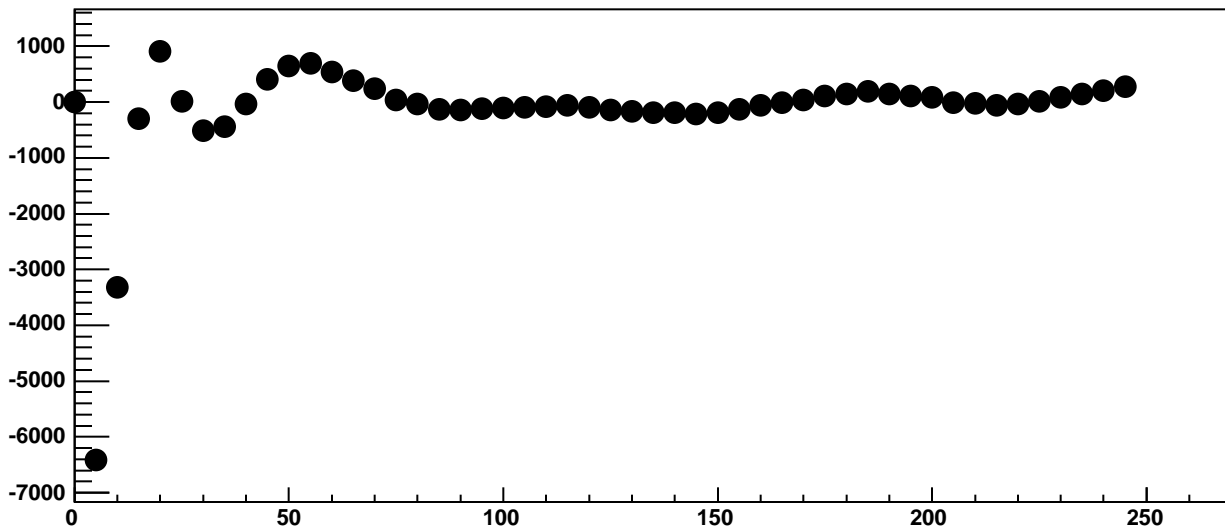
Chip 5, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold



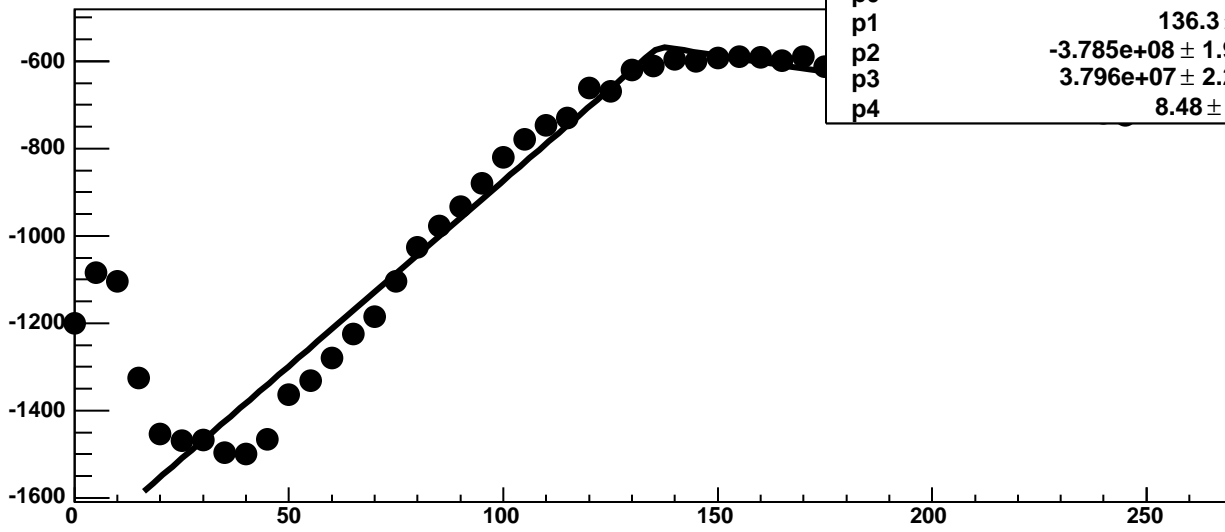
Chip 5, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

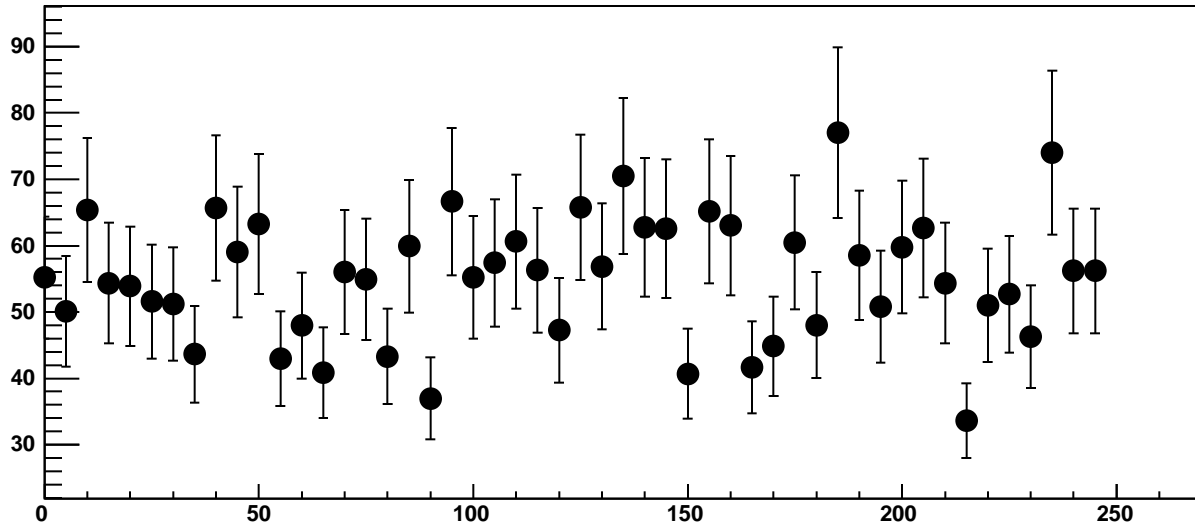


Chip 5, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

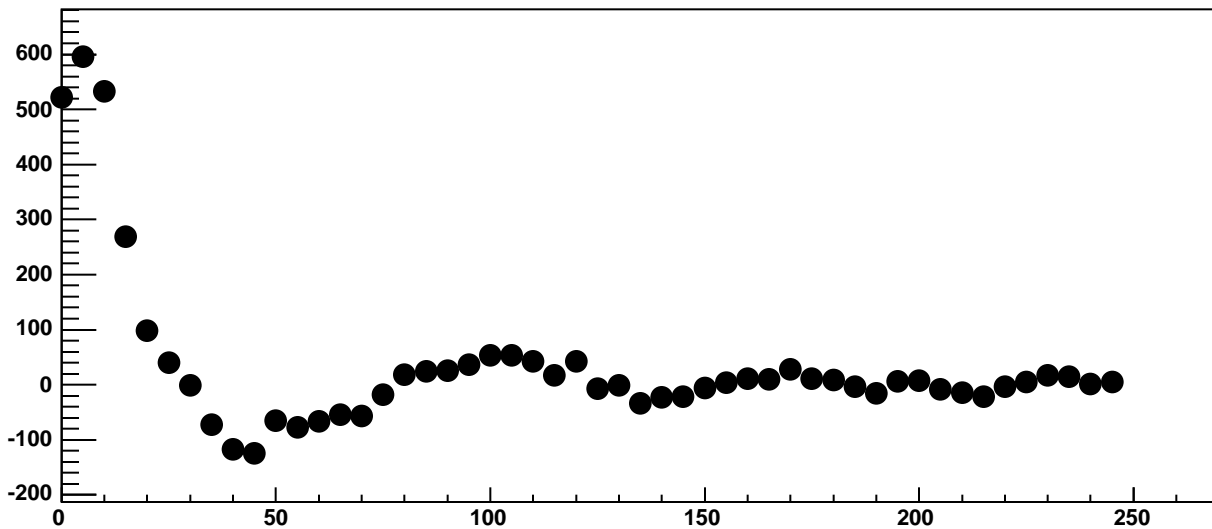


$\chi^2 / \text{ndf}$	1026 / 41
p0	$-566.2 \pm 4.856$
p1	$136.3 \pm 0.6571$
p2	$-3.785\text{e}+08 \pm 1.996\text{e}+07$
p3	$3.796\text{e}+07 \pm 2.291\text{e}+06$
p4	$8.48 \pm 0.06805$

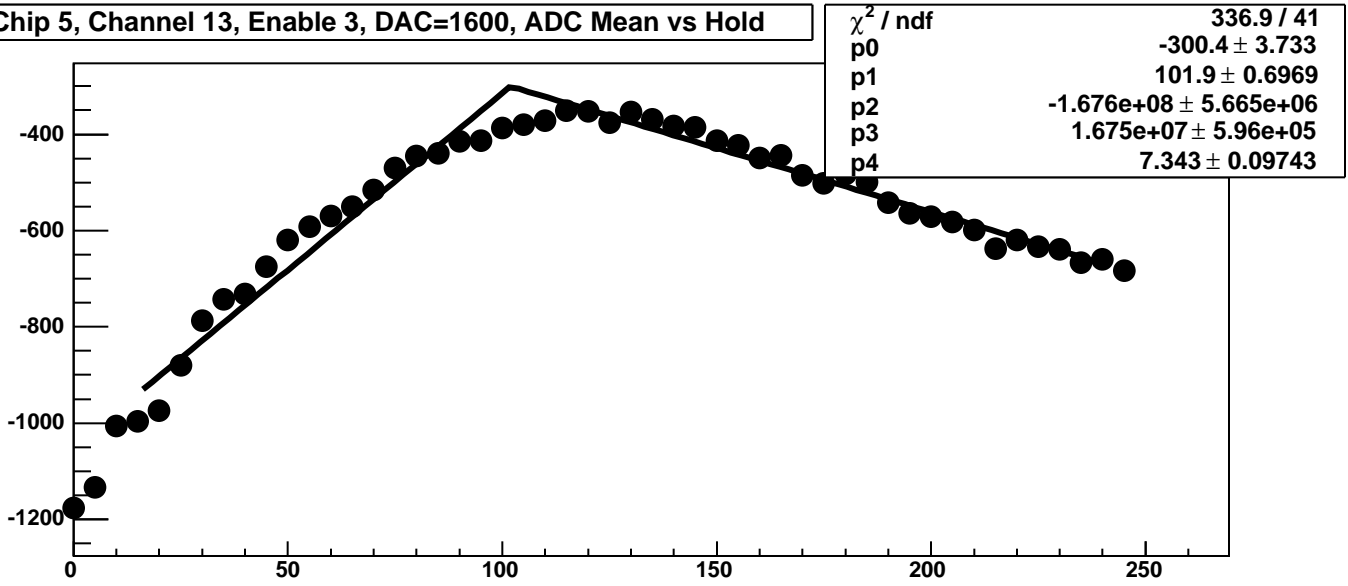
Chip 5, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



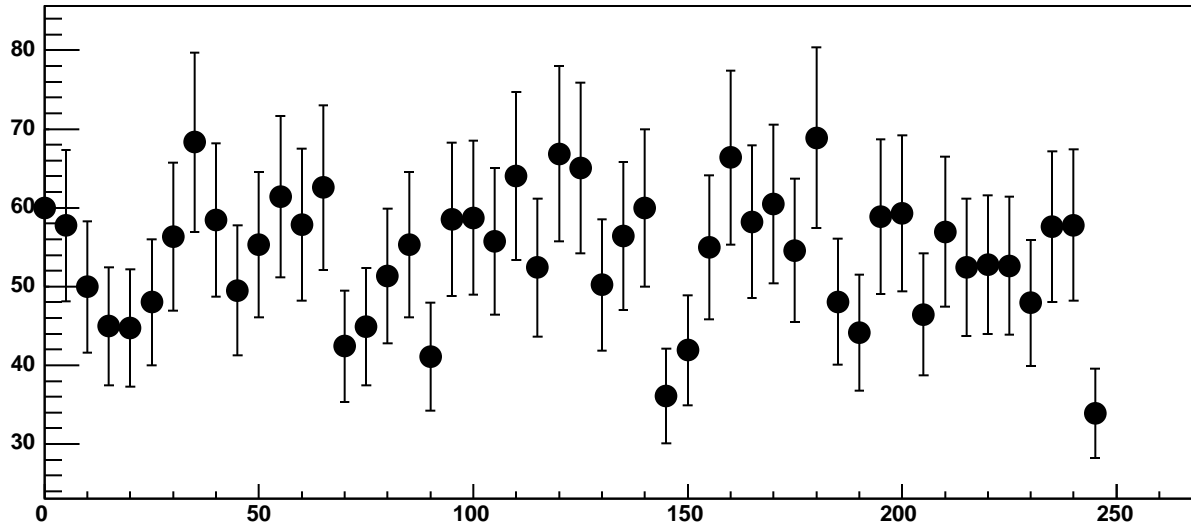
Chip 5, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold



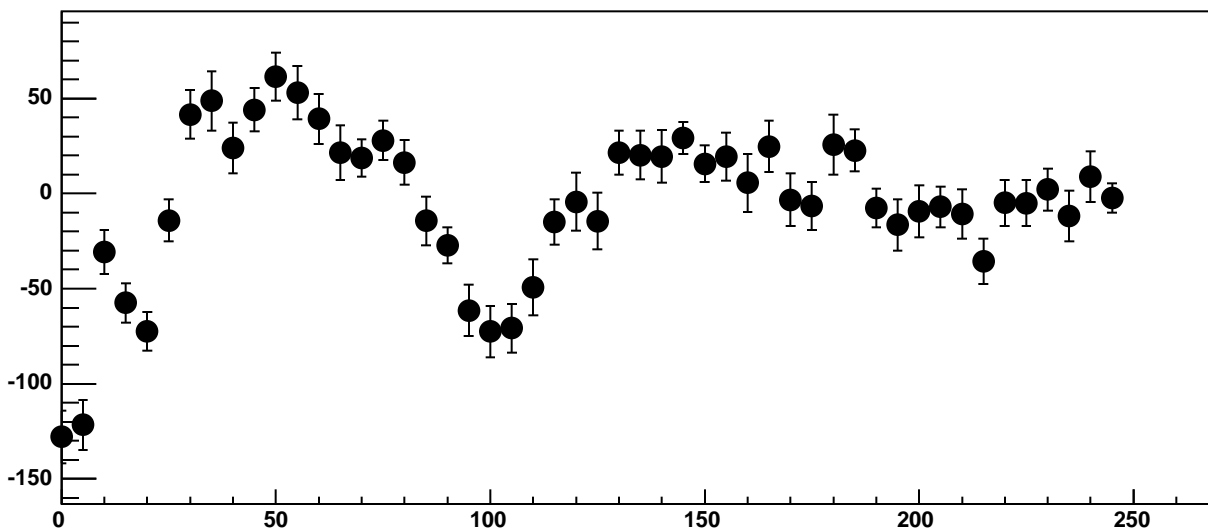
Chip 5, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold



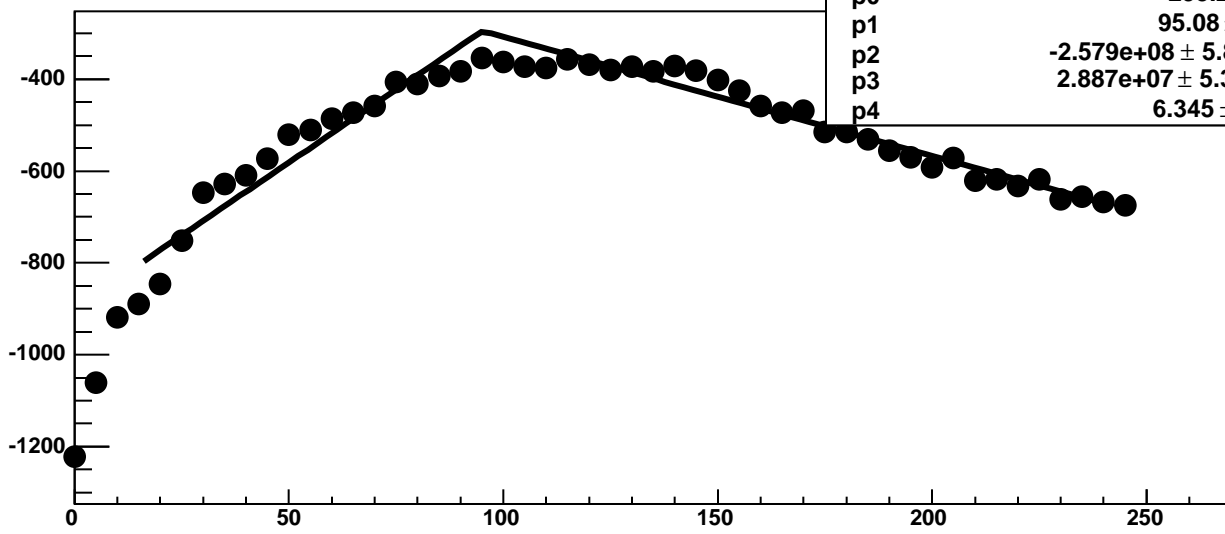
Chip 5, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

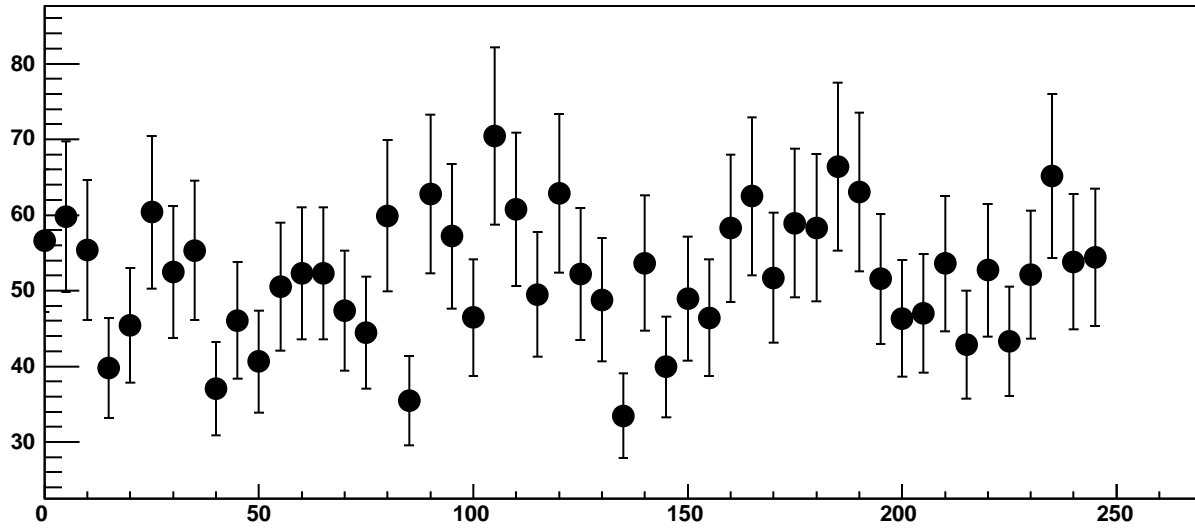


Chip 5, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold

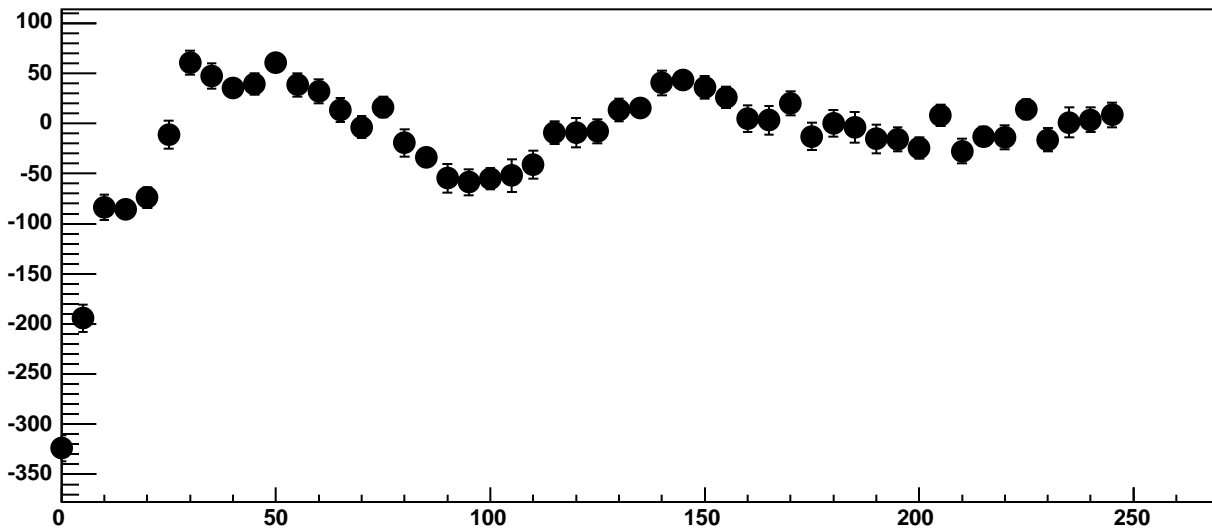


$\chi^2 / \text{ndf}$	454.7 / 41
p0	$-295.2 \pm 3.506$
p1	$95.08 \pm 0.7671$
p2	$-2.579\text{e}+08 \pm 5.812\text{e}+06$
p3	$2.887\text{e}+07 \pm 5.359\text{e}+05$
p4	$6.345 \pm 0.1085$

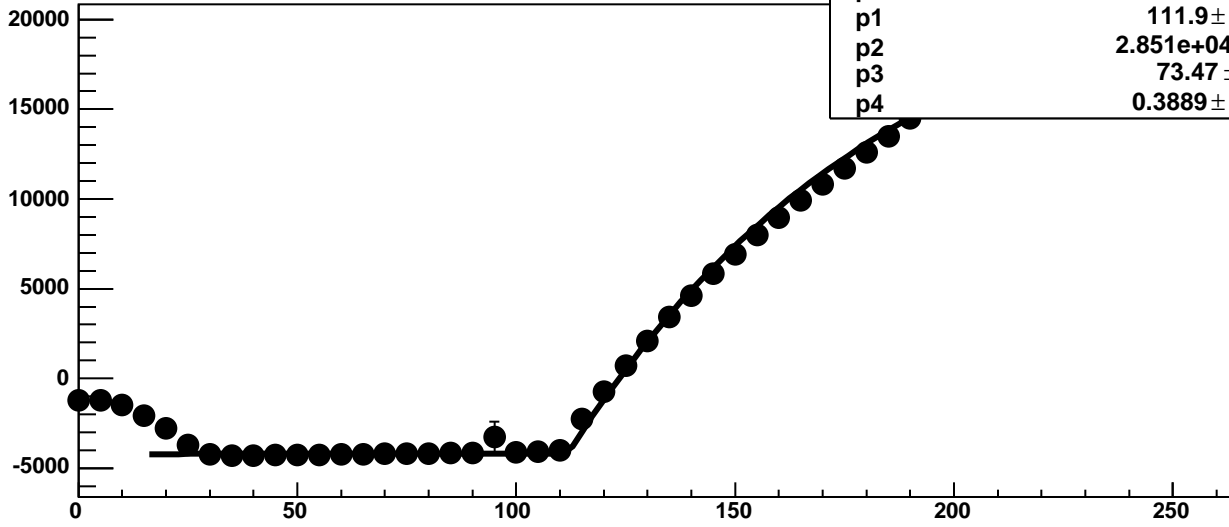
Chip 5, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

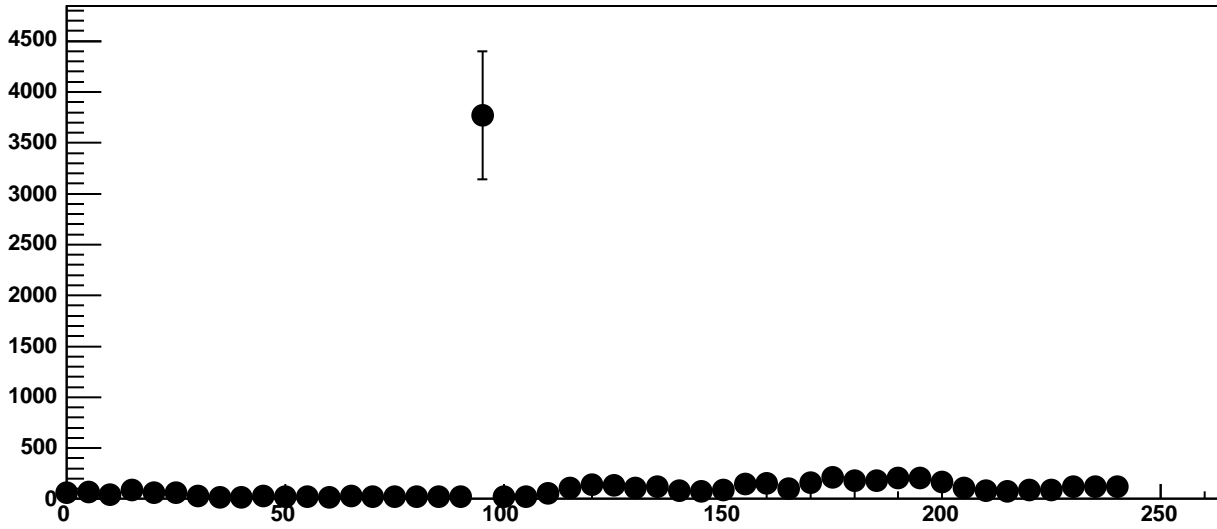


Chip 5, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

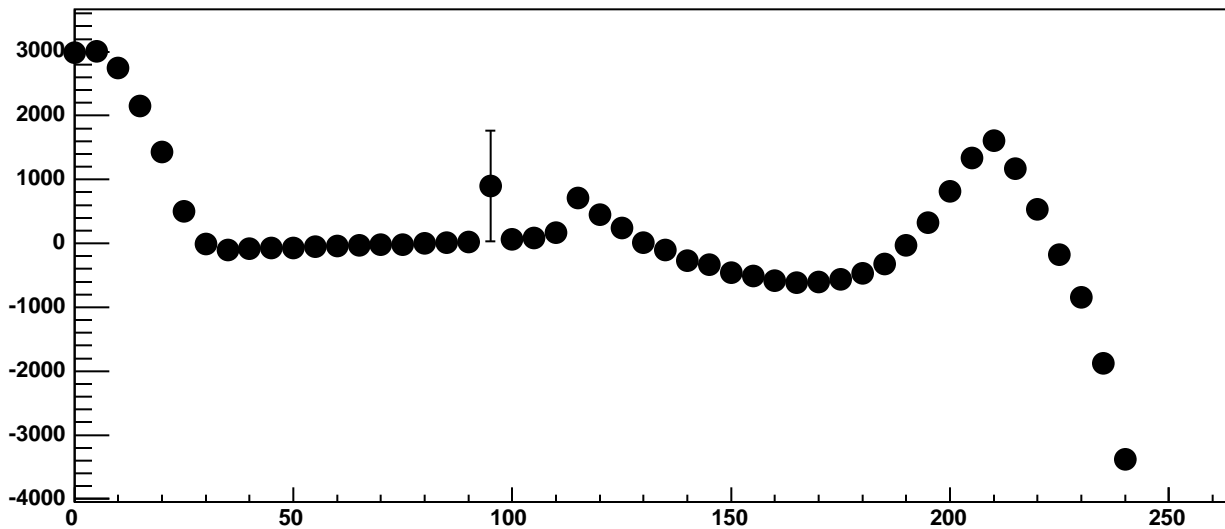


$\chi^2 / \text{ndf}$	6.651e+04 / 41
p0	-4172 ± 2.844
p1	111.9 ± 0.05083
p2	2.851e+04 ± 46.22
p3	73.47 ± 0.2625
p4	0.3889 ± 0.05296

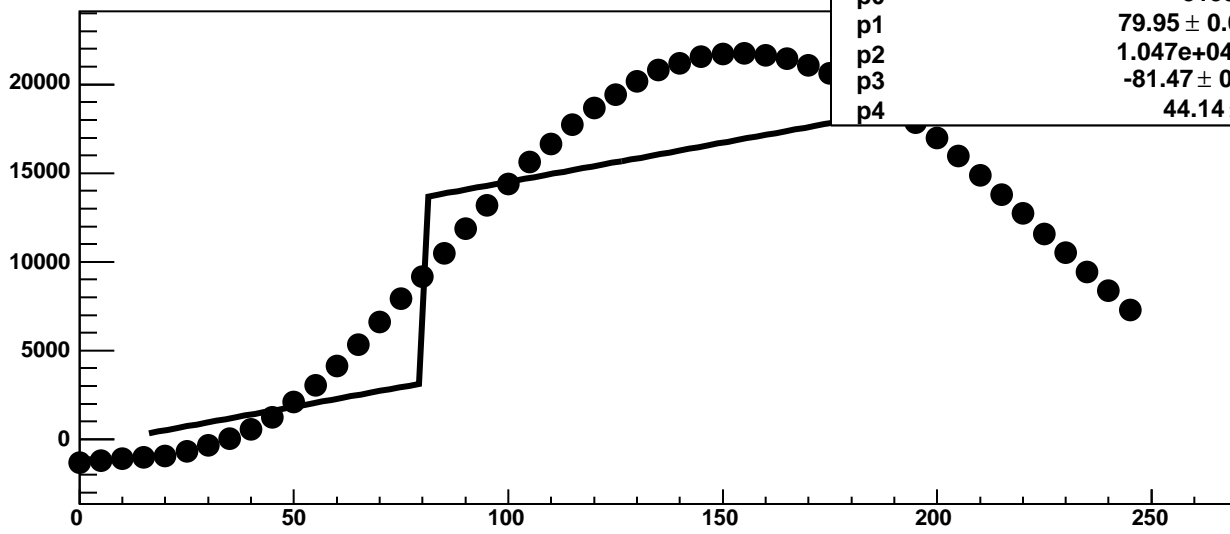
Chip 5, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

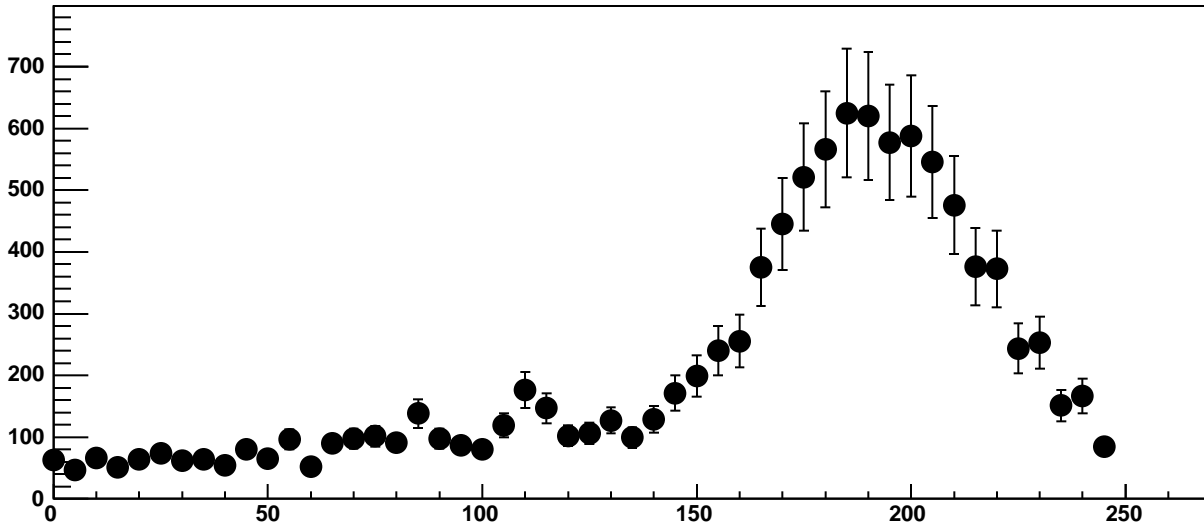


Chip 5, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

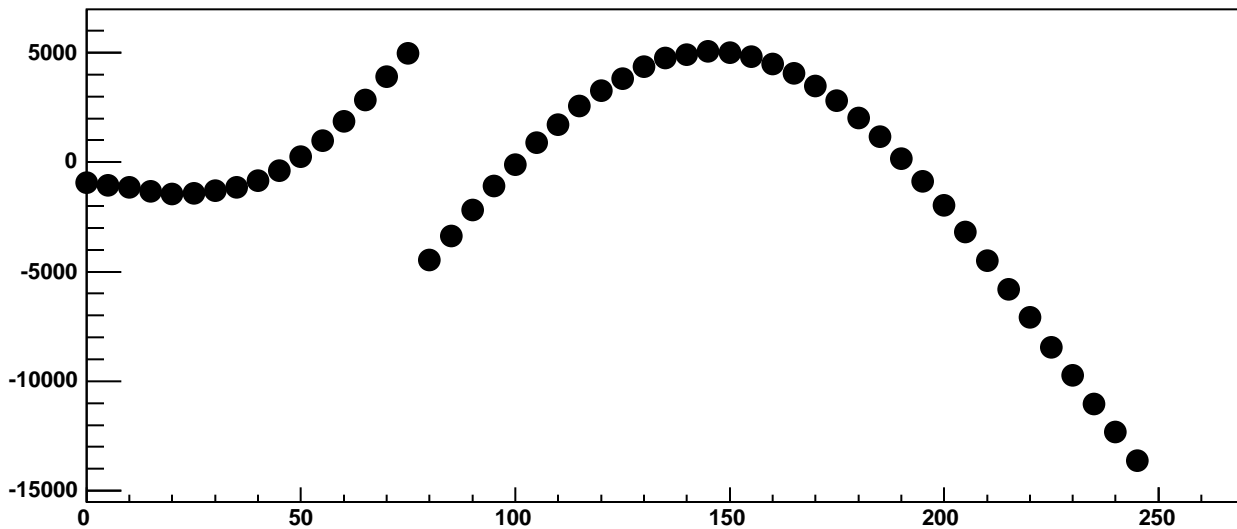


$\chi^2 / \text{ndf}$	7.01e+05 / 41
p0	3155 ± 6.221
p1	79.95 ± 0.0001782
p2	1.047e+04 ± 12.67
p3	-81.47 ± 0.002019
p4	44.14 ± 0.1116

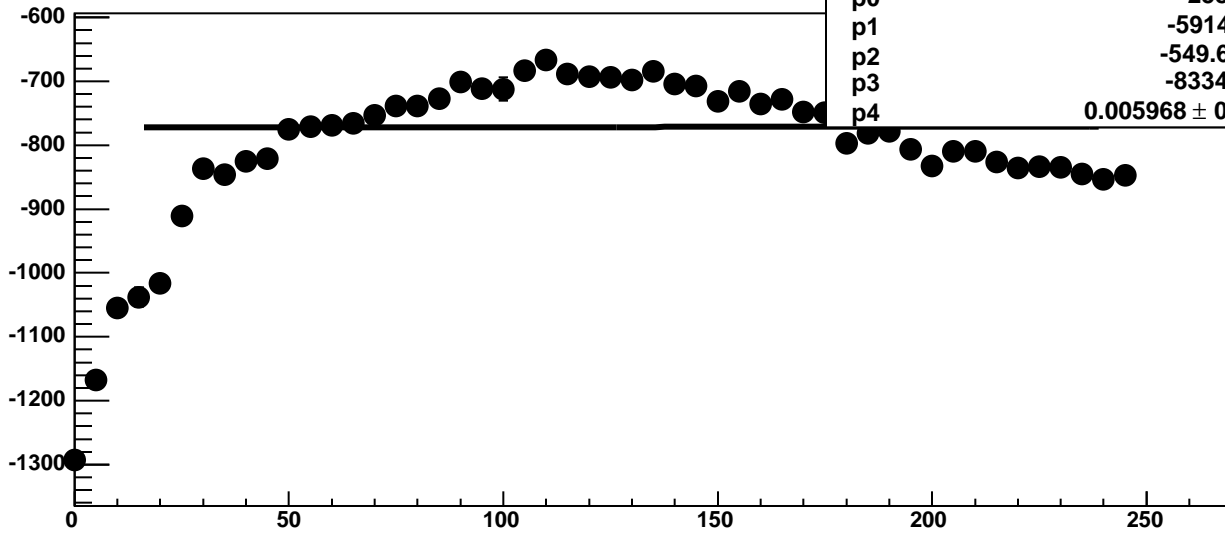
Chip 5, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold



Chip 5, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

1945 / 41

p0

$-258 \pm 3.725$

p1

$-5914 \pm 2171$

p2

$-549.6 \pm 2.992$

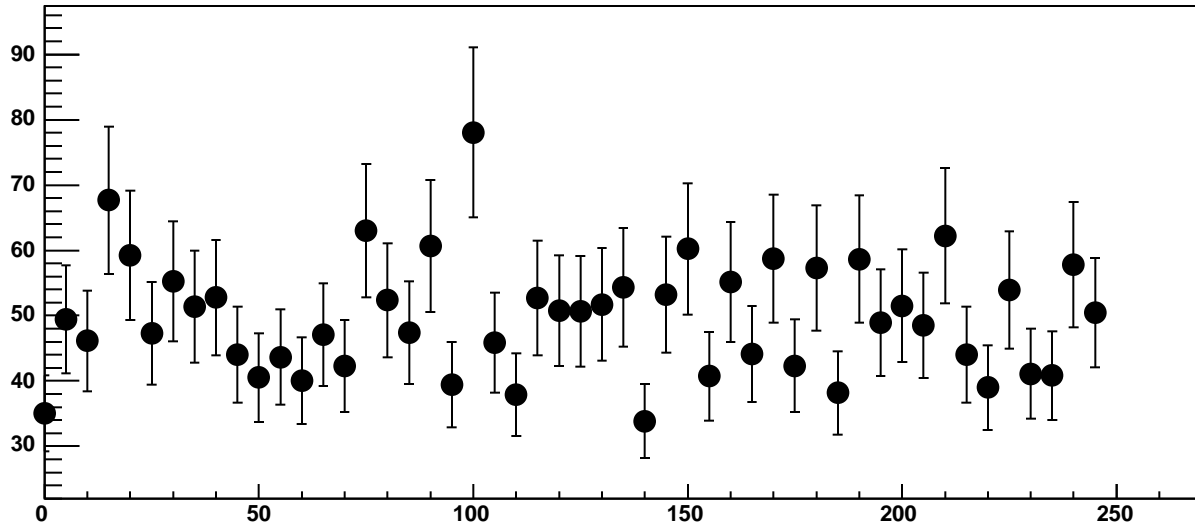
p3

$-8334 \pm 1825$

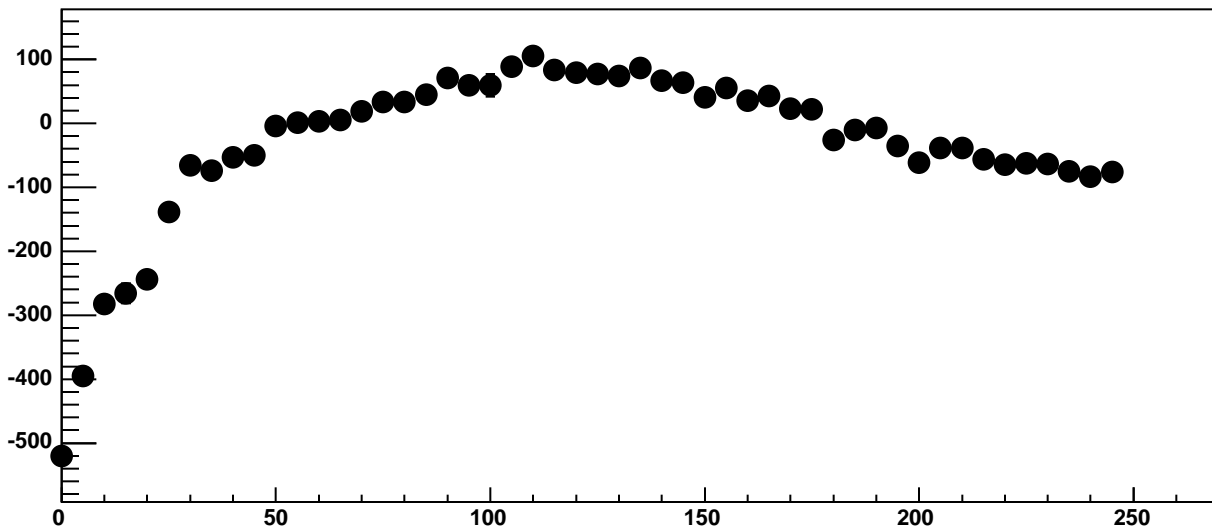
p4

$0.005968 \pm 0.000616$

Chip 5, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

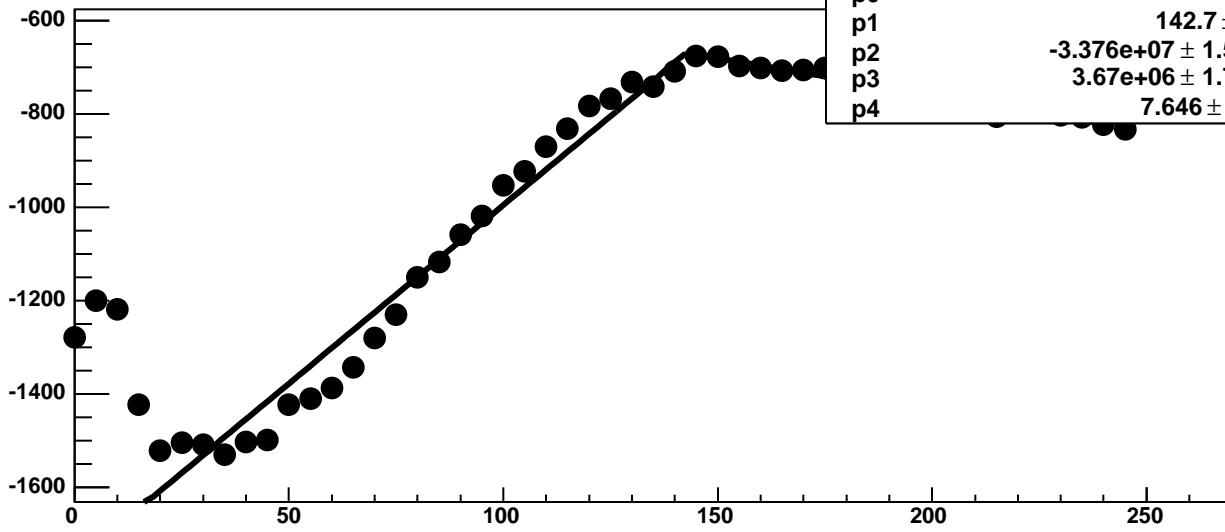


Chip 5, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold



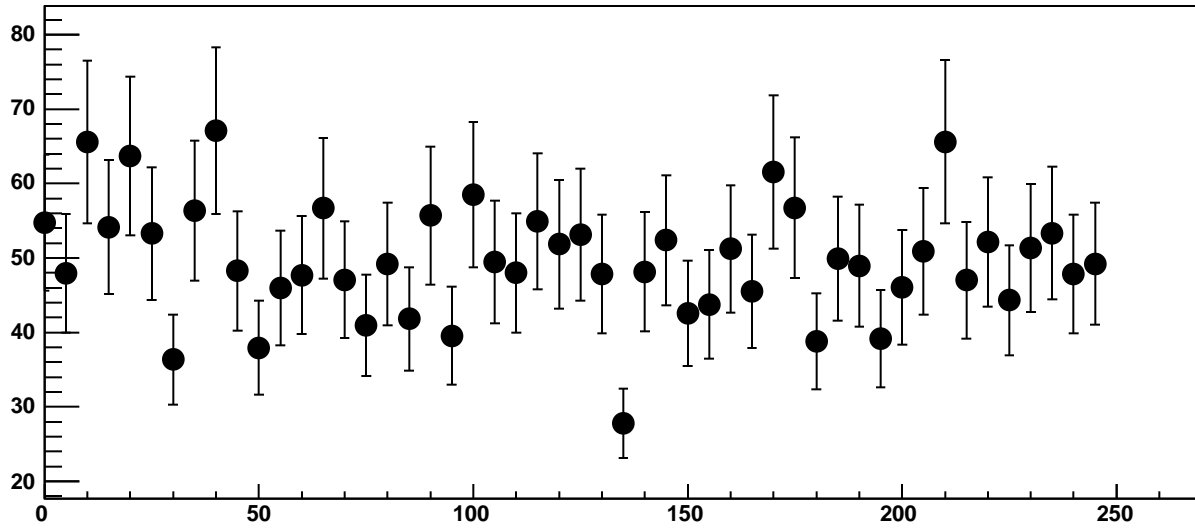


Chip 5, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

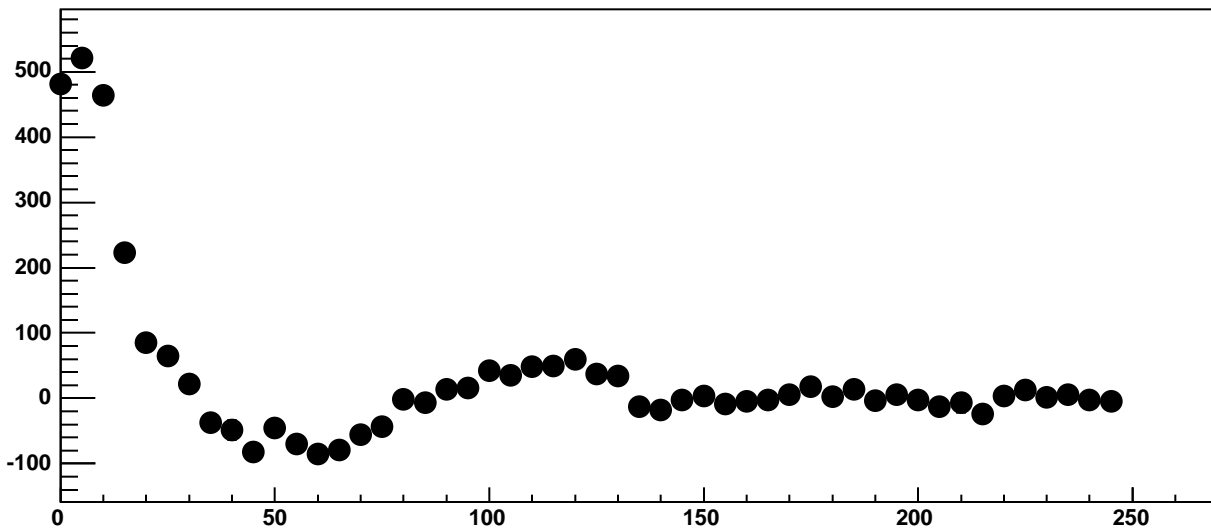


$\chi^2 / \text{ndf}$	802.6 / 41
p0	-668.8 ± 4.105
p1	142.7 ± 0.6818
p2	-3.376e+07 ± 1.596e+07
p3	3.67e+06 ± 1.725e+06
p4	7.646 ± 0.05533

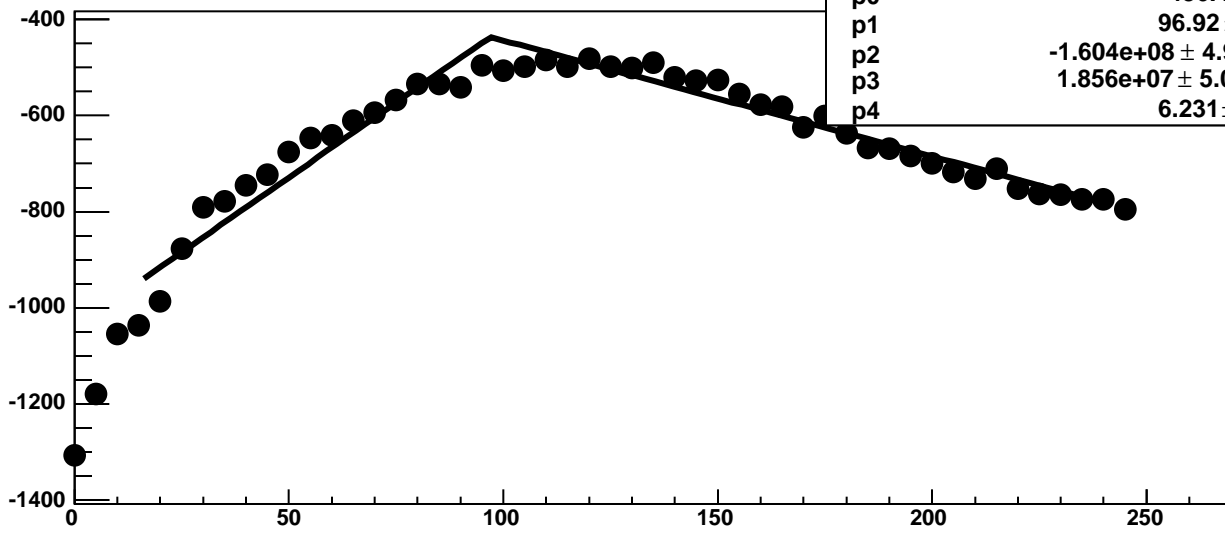
Chip 5, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

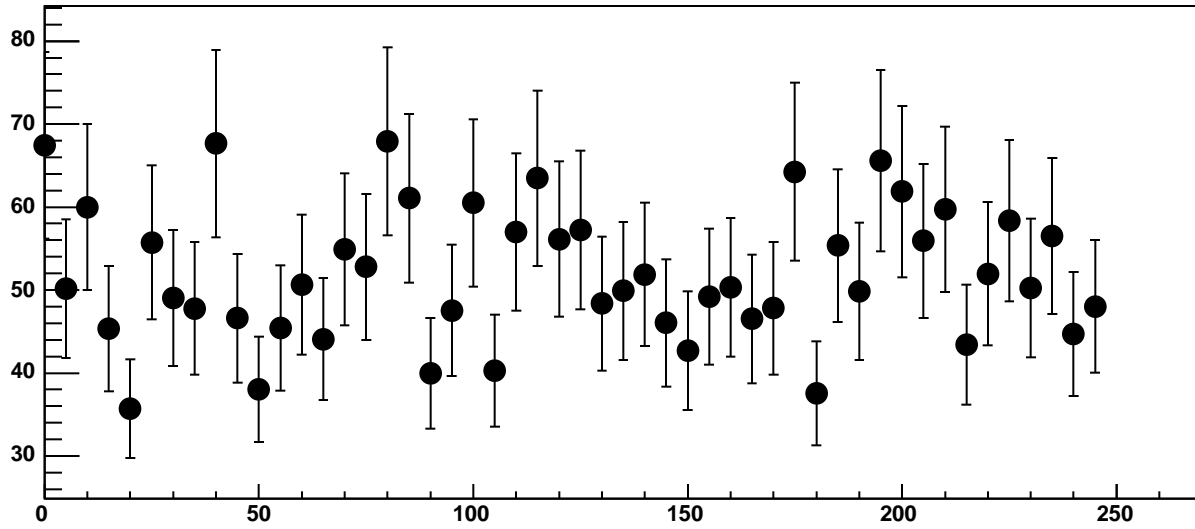


Chip 5, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

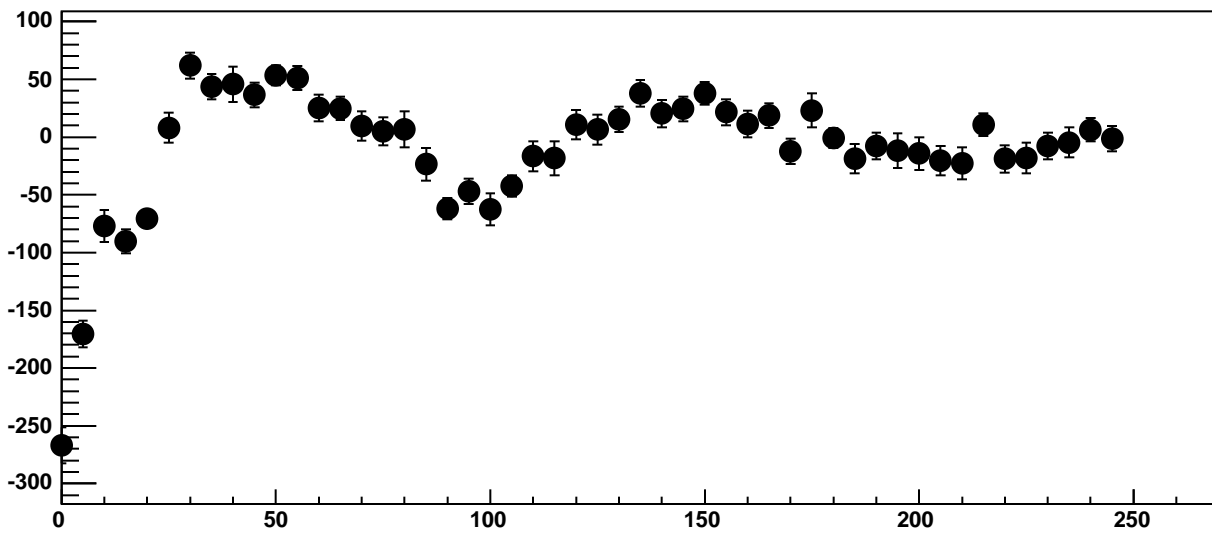


$\chi^2 / \text{ndf}$	466 / 41
p0	$-436.4 \pm 3.518$
p1	$96.92 \pm 0.8031$
p2	$-1.604\text{e}+08 \pm 4.979\text{e}+06$
p3	$1.856\text{e}+07 \pm 5.042\text{e}+05$
p4	$6.231 \pm 0.1059$

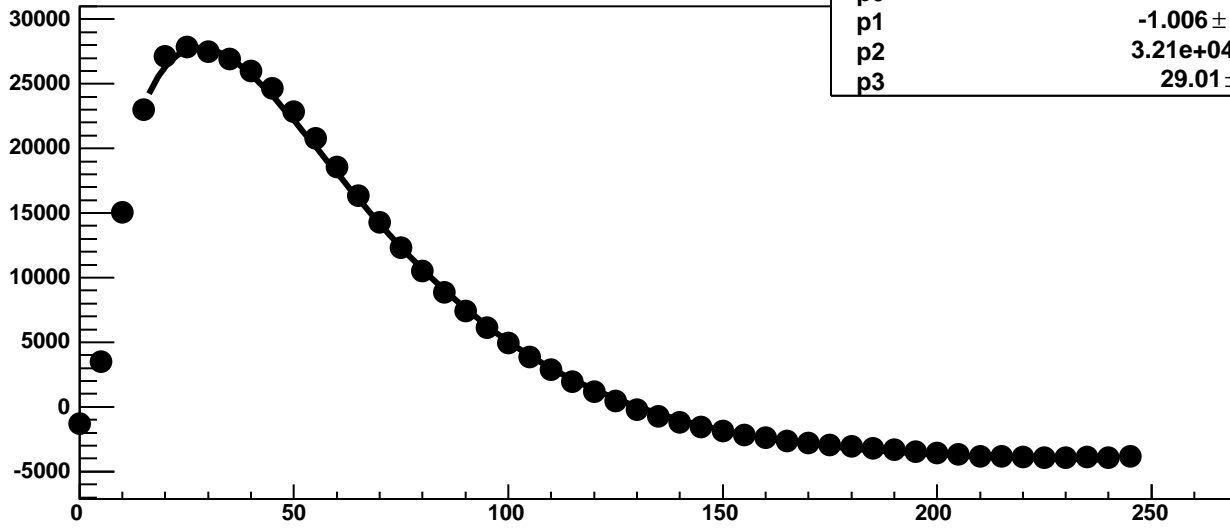
Chip 5, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

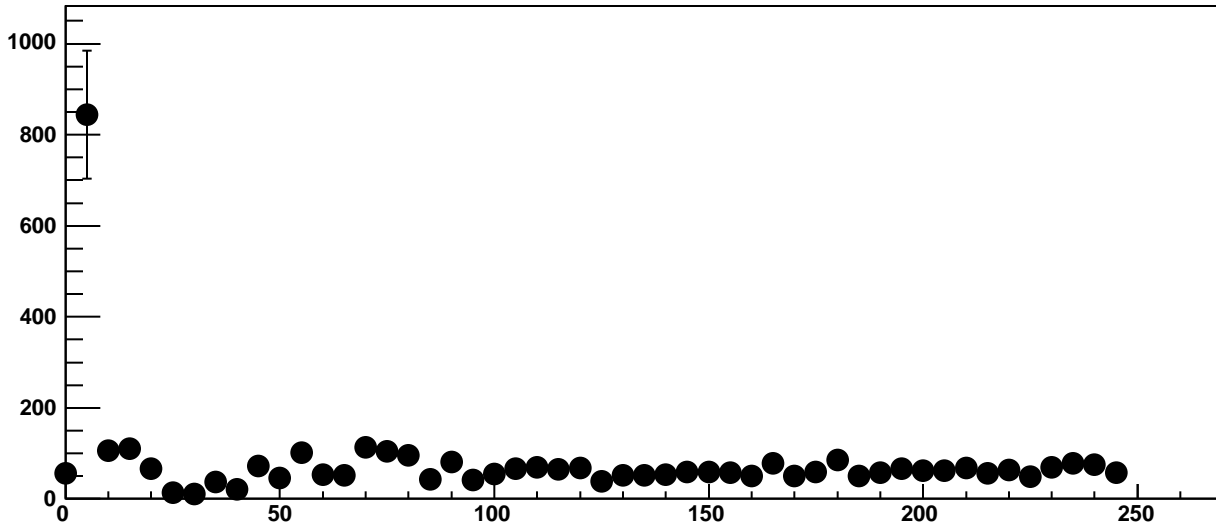


Chip 5, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold

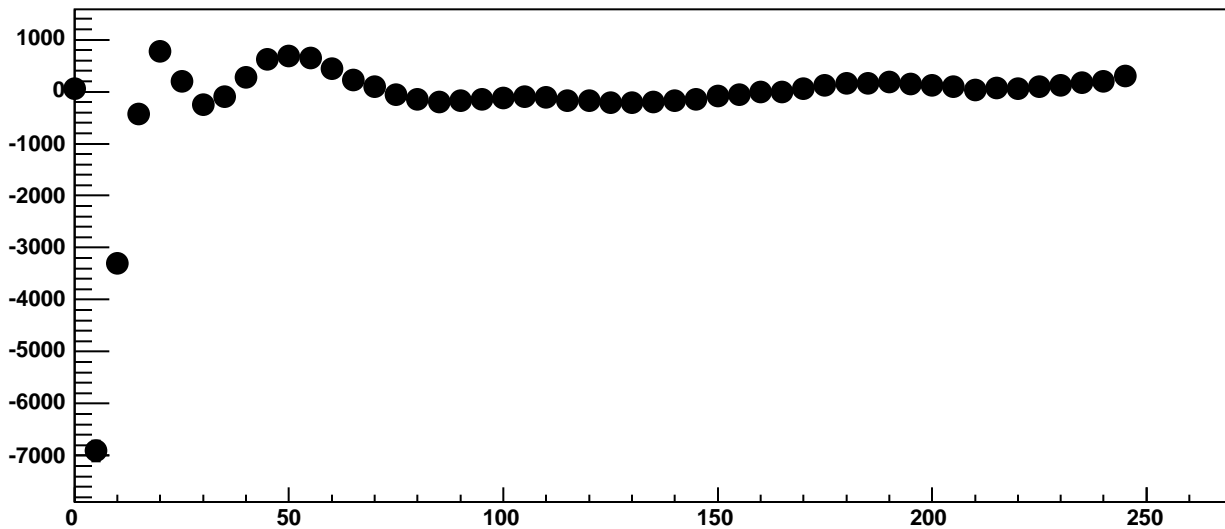


$\chi^2 / \text{ndf}$	3.198e+04 / 42
p0	-4282 ± 3.895
p1	-1.006 ± 0.01873
p2	3.21e+04 ± 4.163
p3	29.01 ± 0.0106

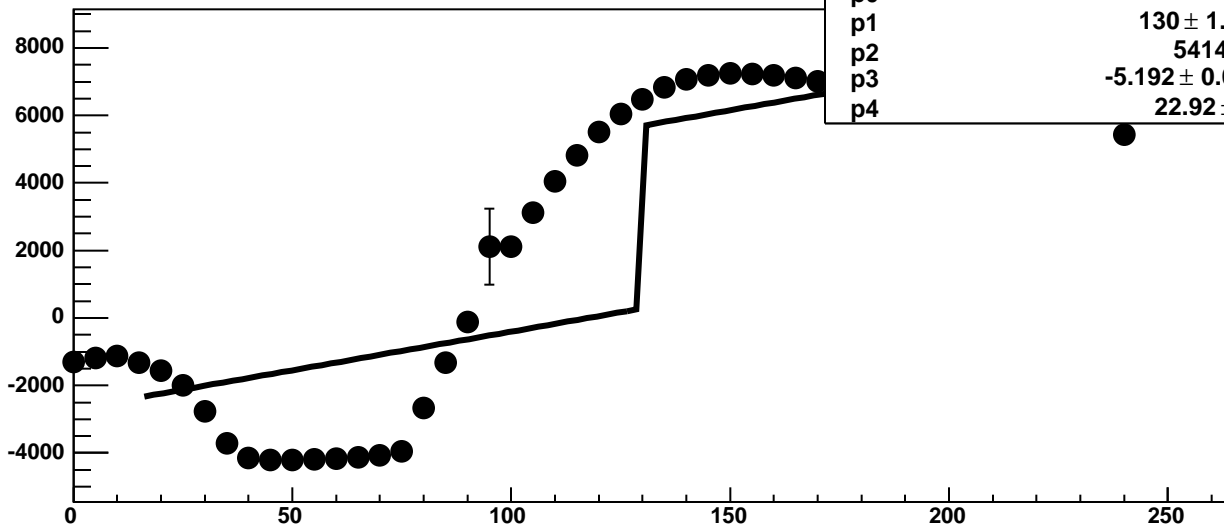
Chip 5, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold

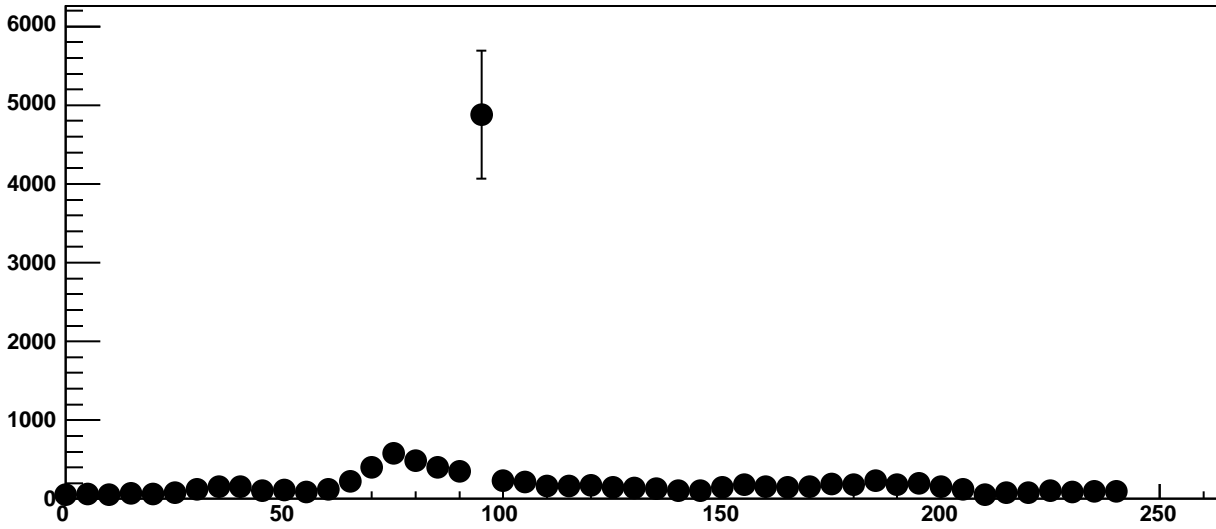


Chip 5, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

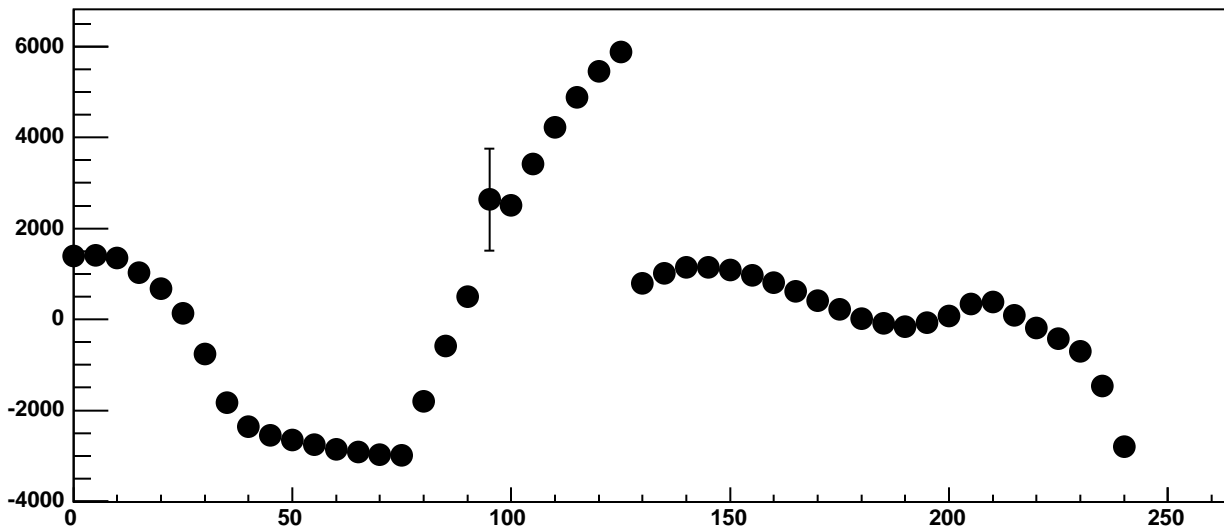


$\chi^2 / \text{ndf}$	1.852e+05 / 41
p0	283.3 ± 12.24
p1	130 ± 1.816e-07
p2	5414 ± 20.73
p3	-5.192 ± 0.0003502
p4	22.92 ± 0.1229

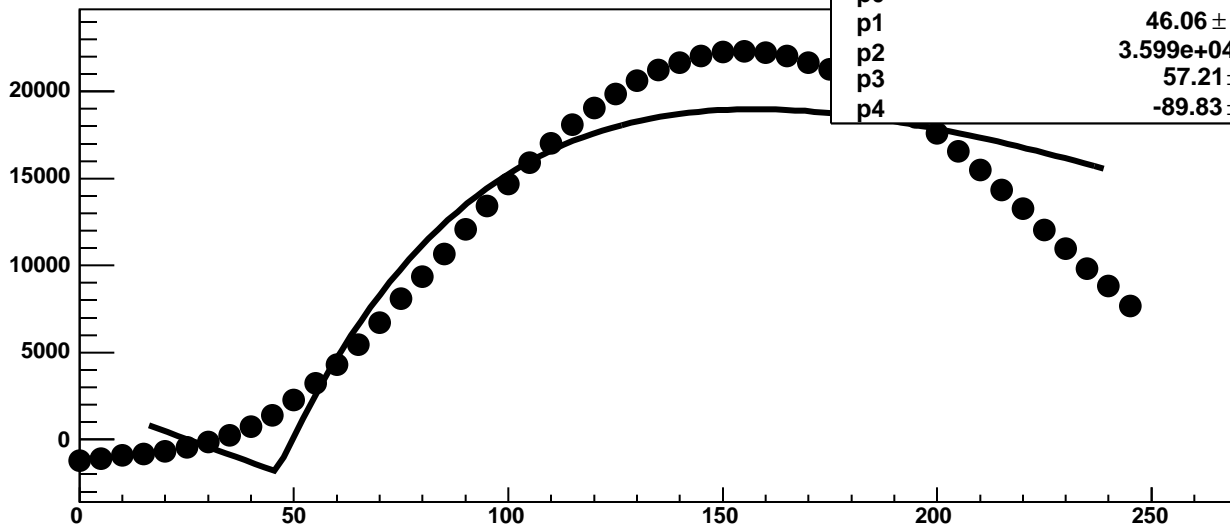
Chip 5, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

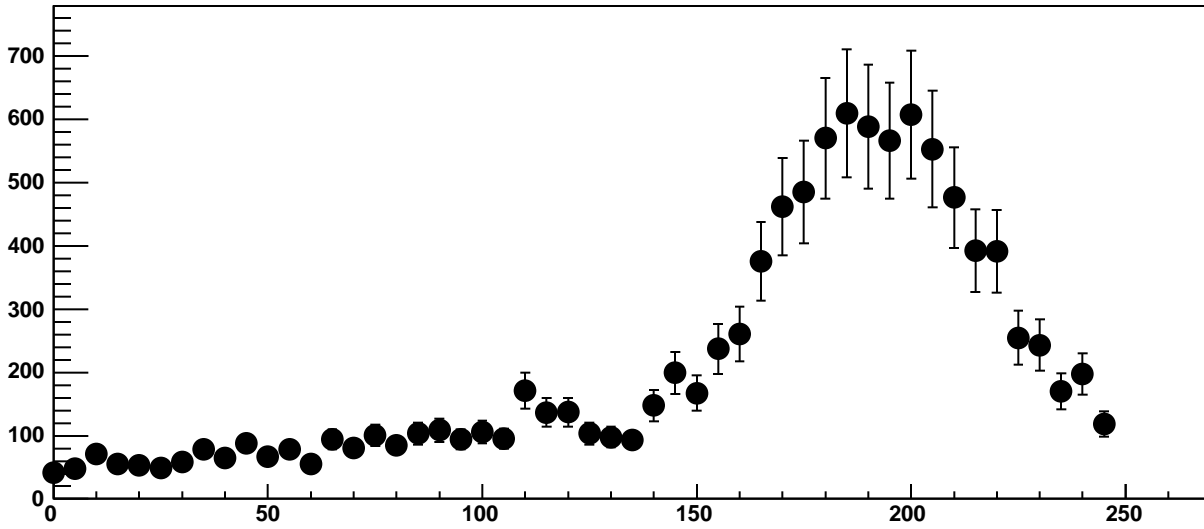


Chip 5, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

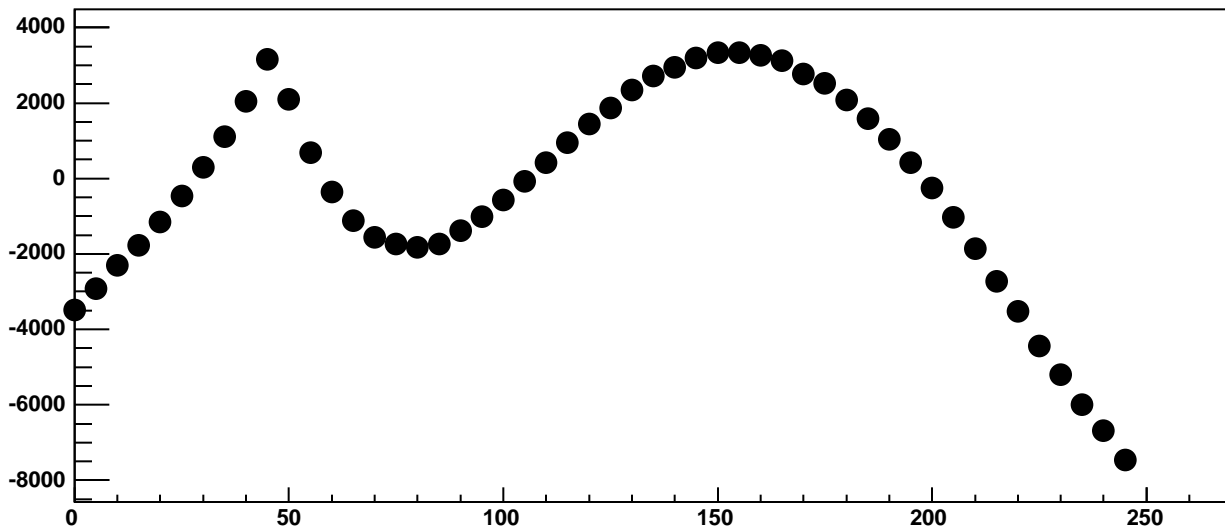


$\chi^2 / \text{ndf}$	2.627e+05 / 41
p0	-1865 ± 7.442
p1	46.06 ± 0.02397
p2	3.599e+04 ± 74.71
p3	57.21 ± 0.1155
p4	-89.83 ± 0.3543

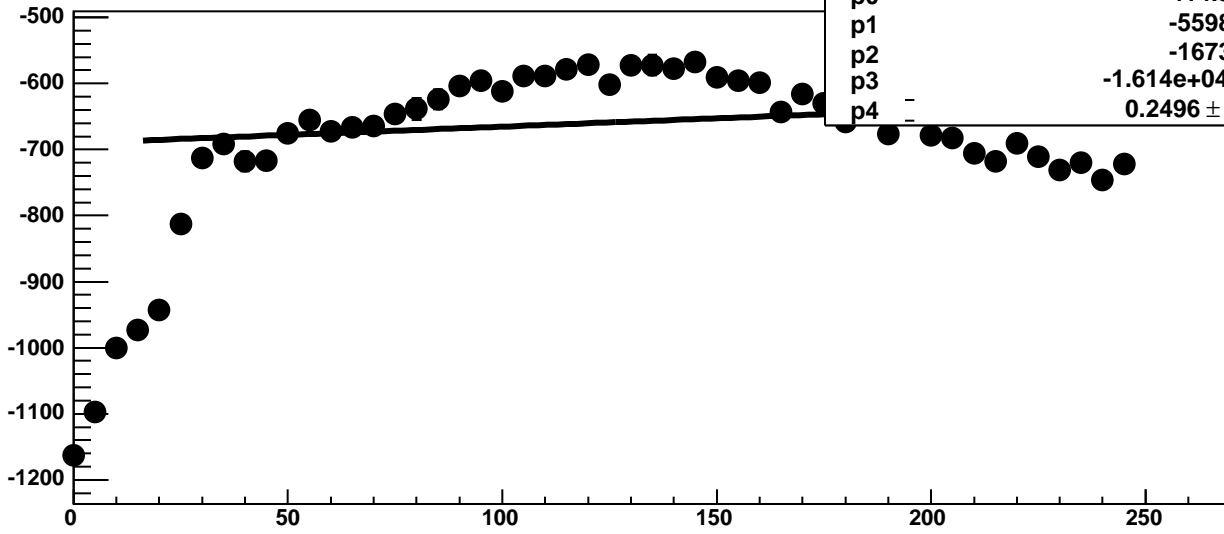
Chip 5, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

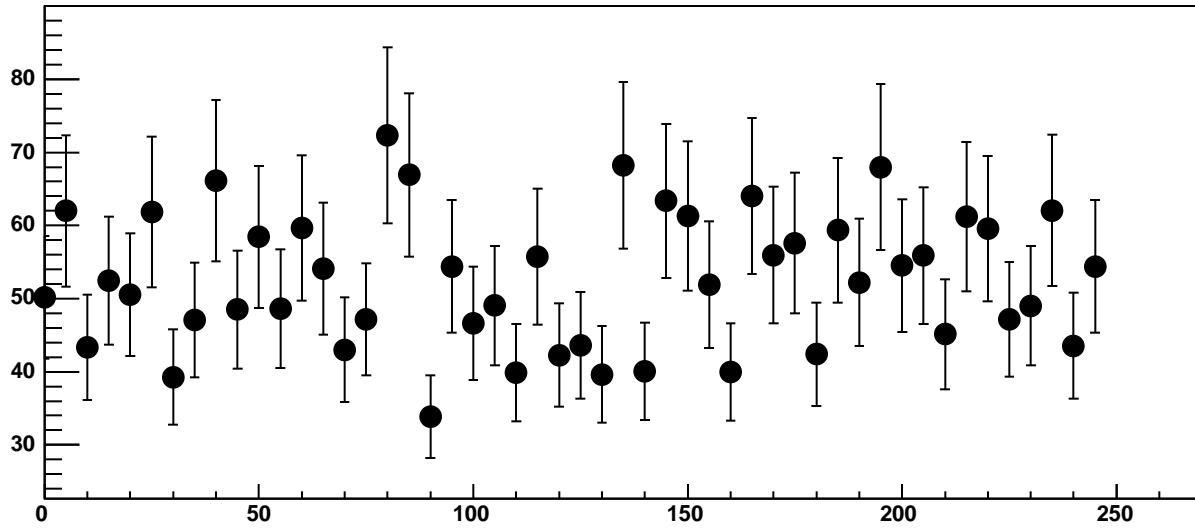


Chip 5, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

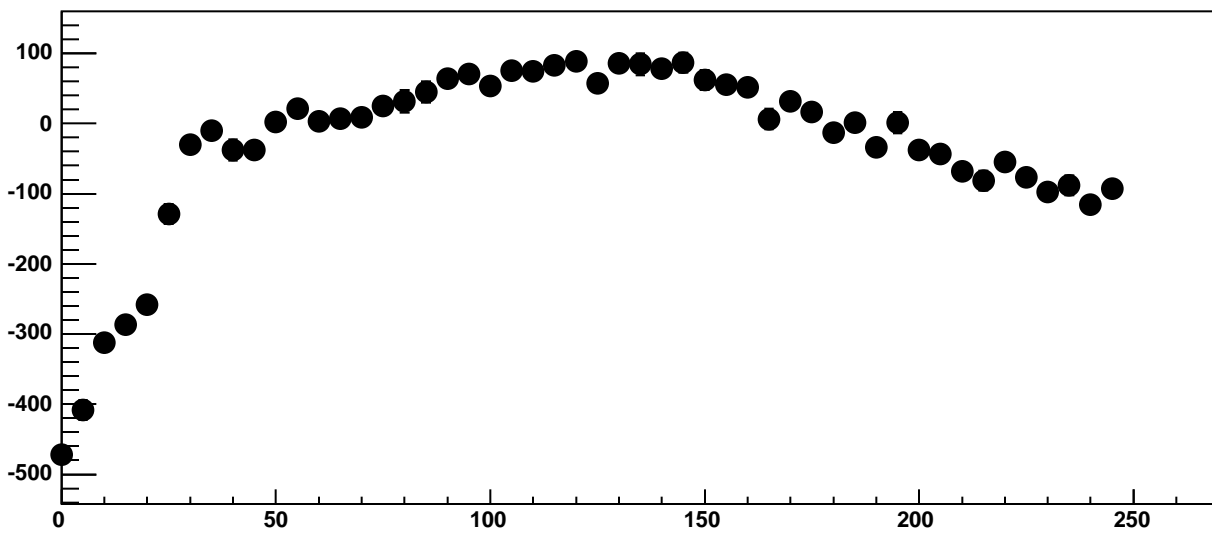


$\chi^2 / \text{ndf}$	2317 / 41
p0	$-414.9 \pm 37.41$
p1	$-5598 \pm 47.61$
p2	$-1673 \pm 124.1$
p3	$-1.614\text{e}+04 \pm 934.5$
p4	$0.2496 \pm 0.02615$

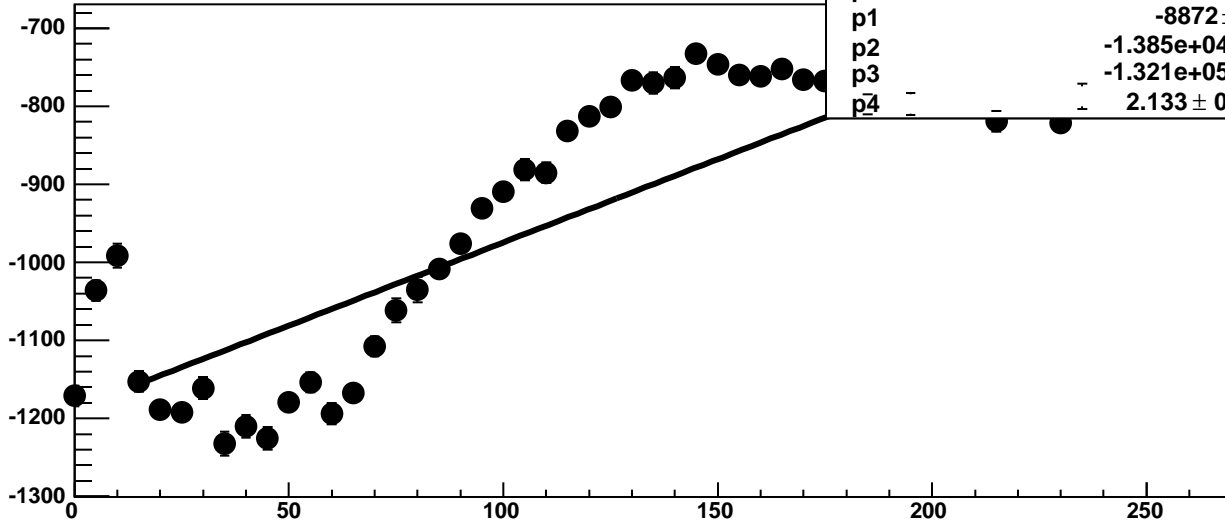
Chip 5, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

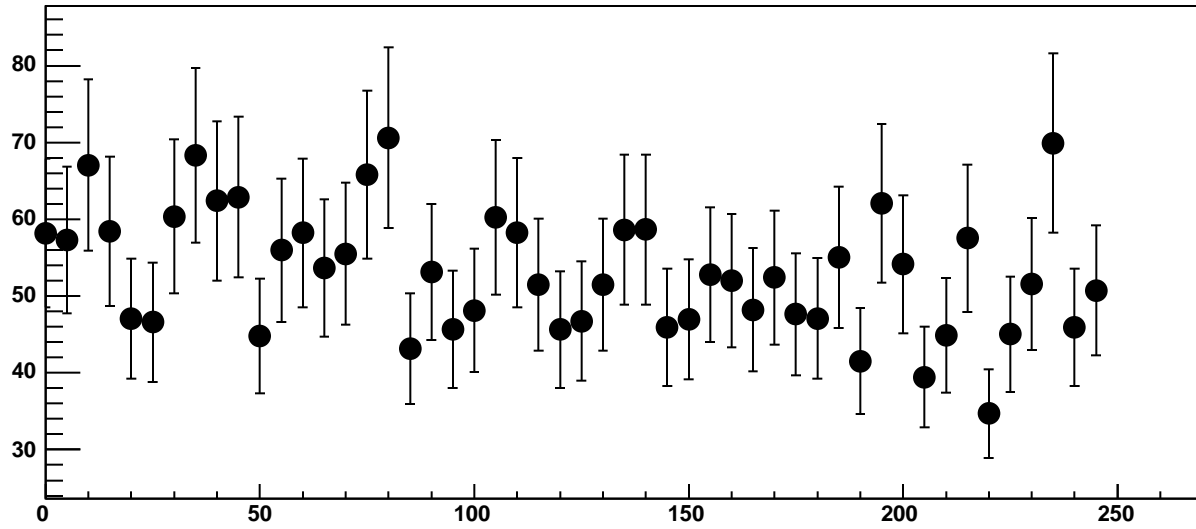


Chip 5, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

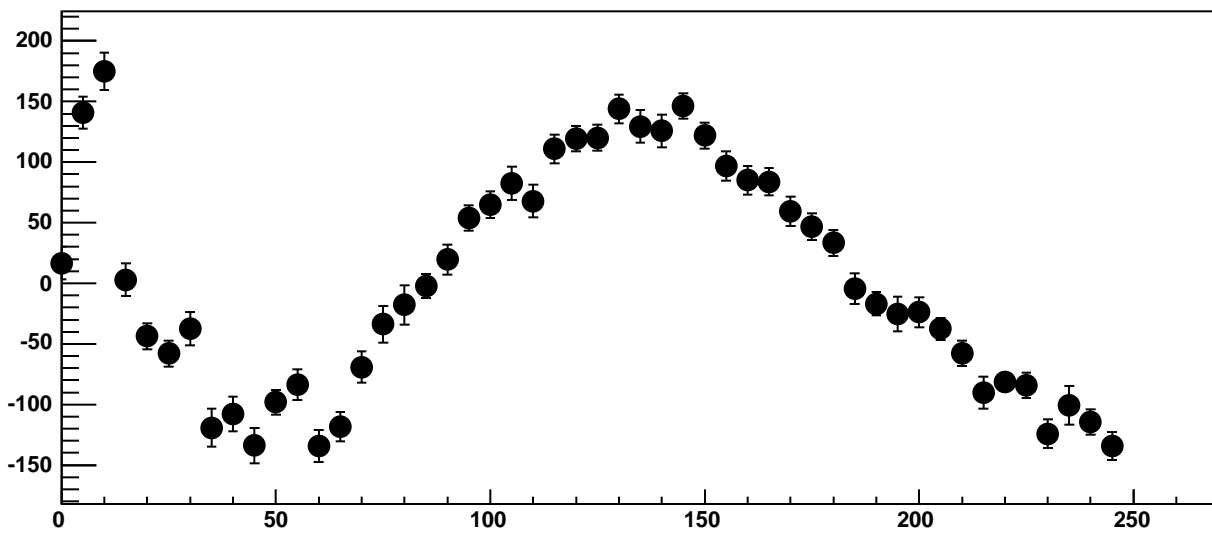


$\chi^2 / \text{ndf}$	2503 / 41
p0	$-6260 \pm 11.14$
p1	$-8872 \pm 0.9292$
p2	$-1.385\text{e}+04 \pm 4.907$
p3	$-1.321\text{e}+05 \pm 648.6$
p4	$2.133 \pm 0.001237$

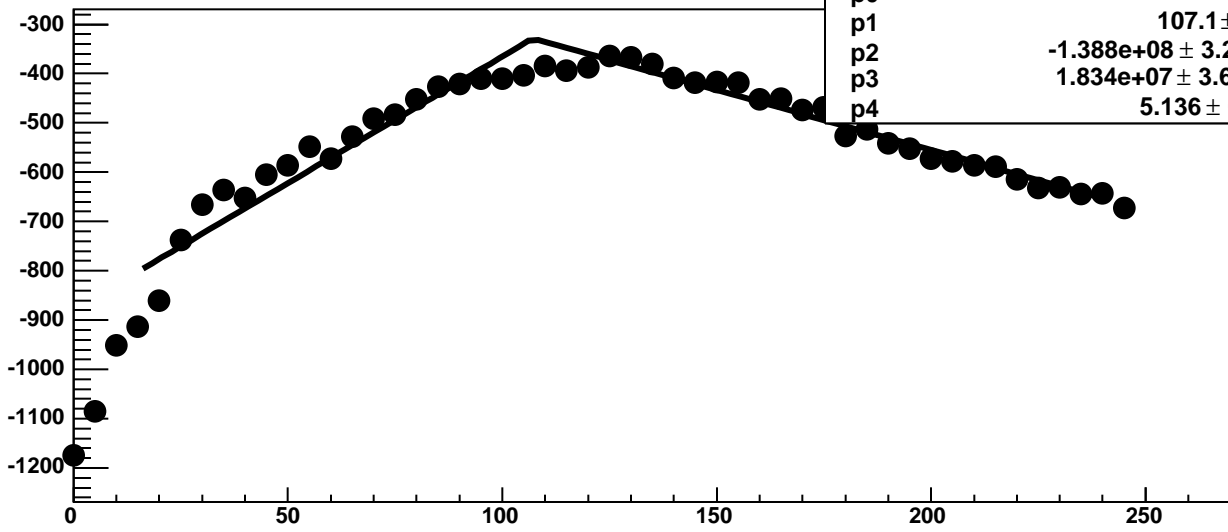
Chip 5, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



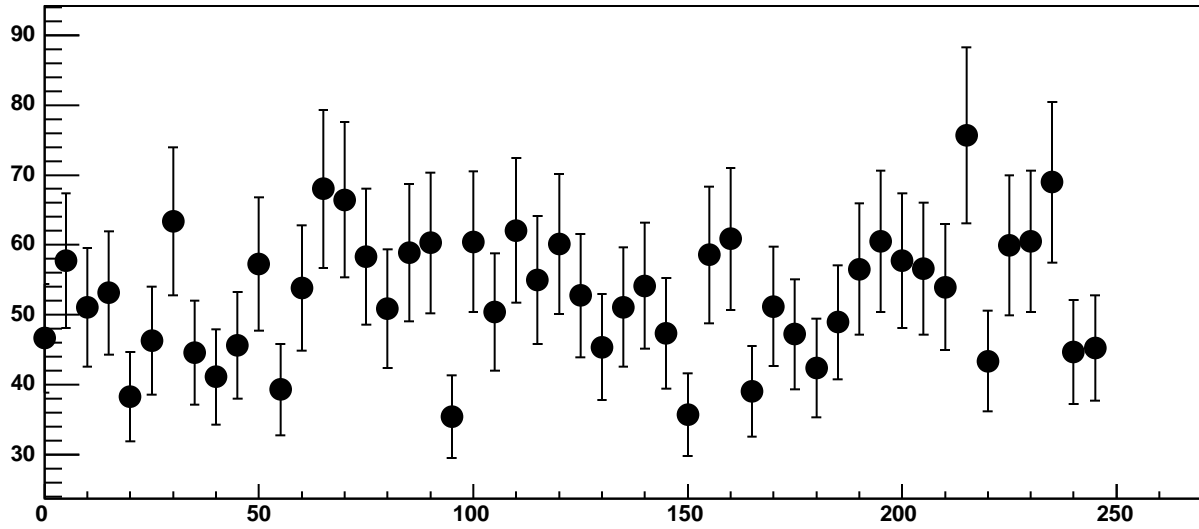
Chip 5, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold



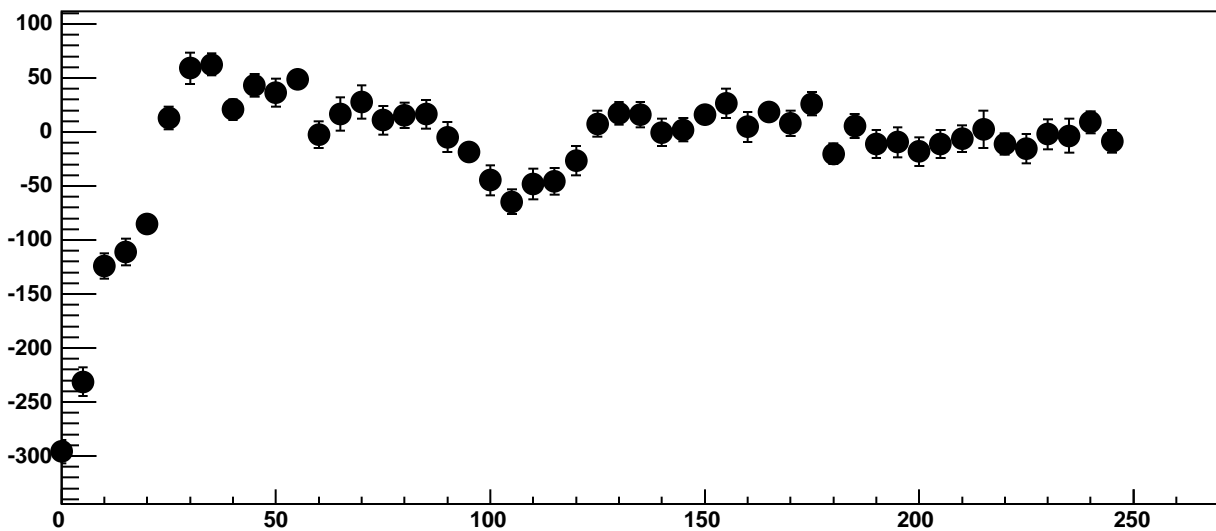
Chip 5, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold



Chip 5, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

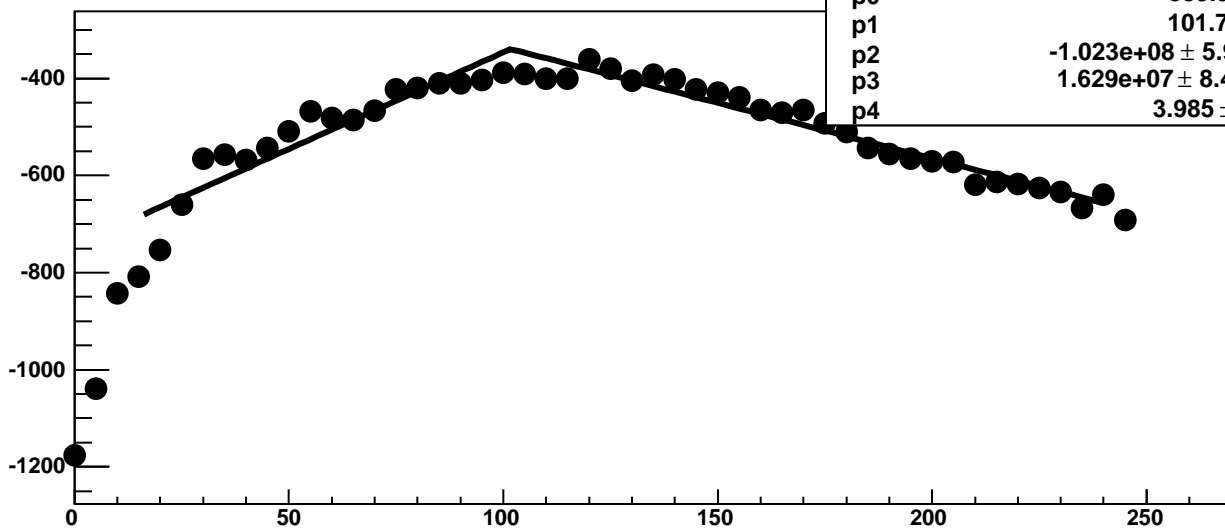


Chip 5, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold



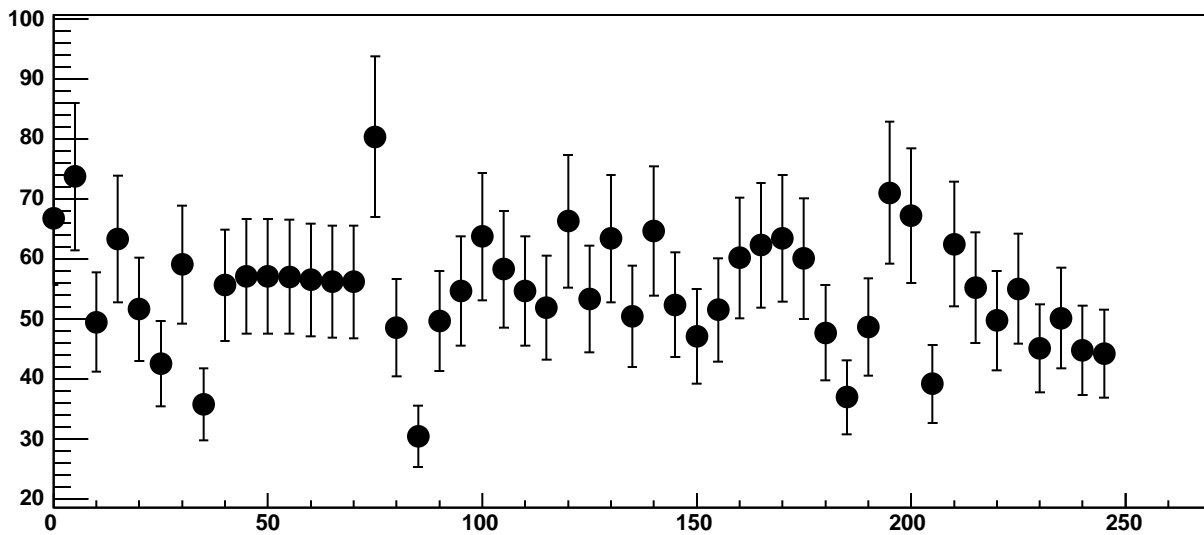


Chip 5, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

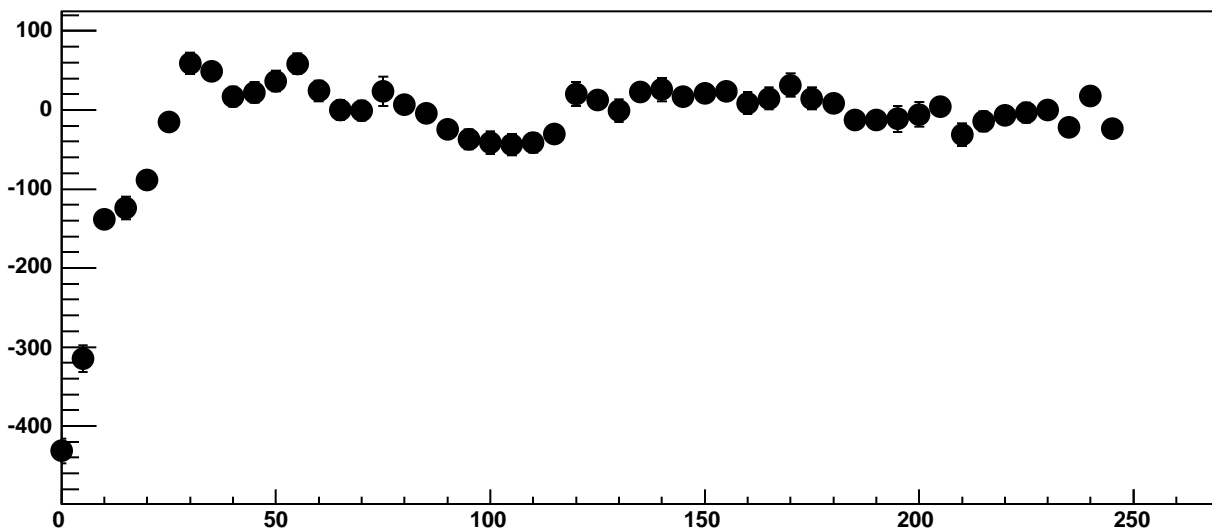


$\chi^2 / \text{ndf}$	318 / 41
p0	$-339.5 \pm 3.626$
p1	$101.7 \pm 1.139$
p2	$-1.023\text{e}+08 \pm 5.928\text{e}+06$
p3	$1.629\text{e}+07 \pm 8.489\text{e}+05$
p4	$3.985 \pm 0.1045$

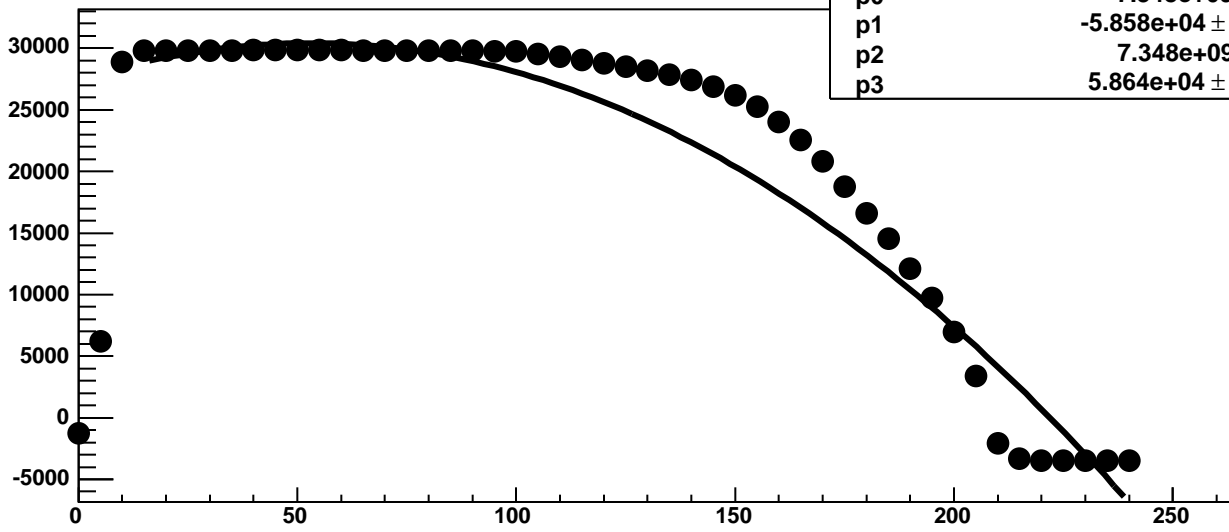
Chip 5, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



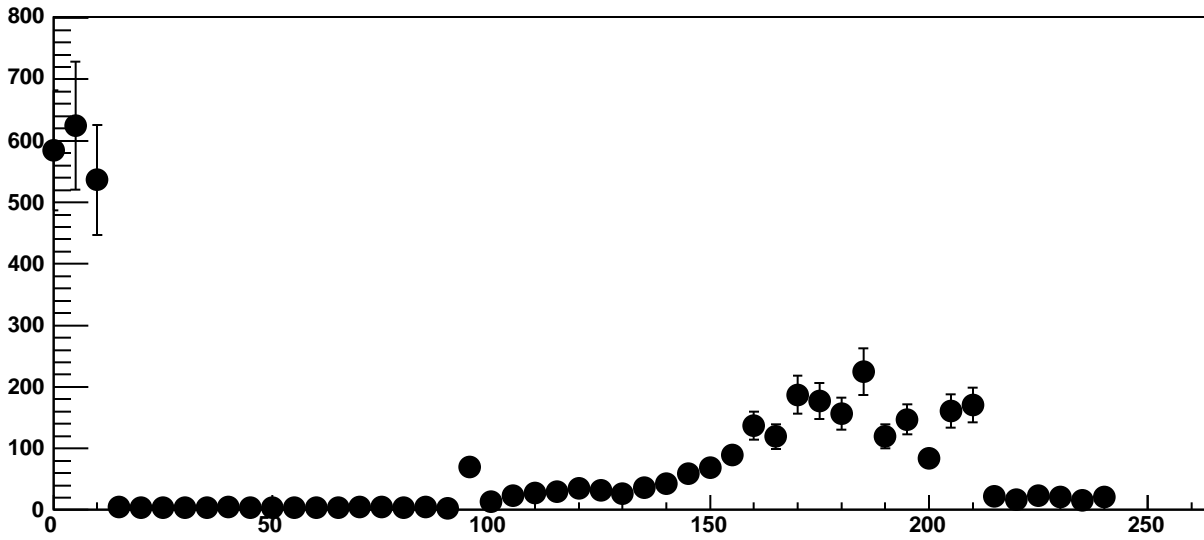
Chip 5, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold



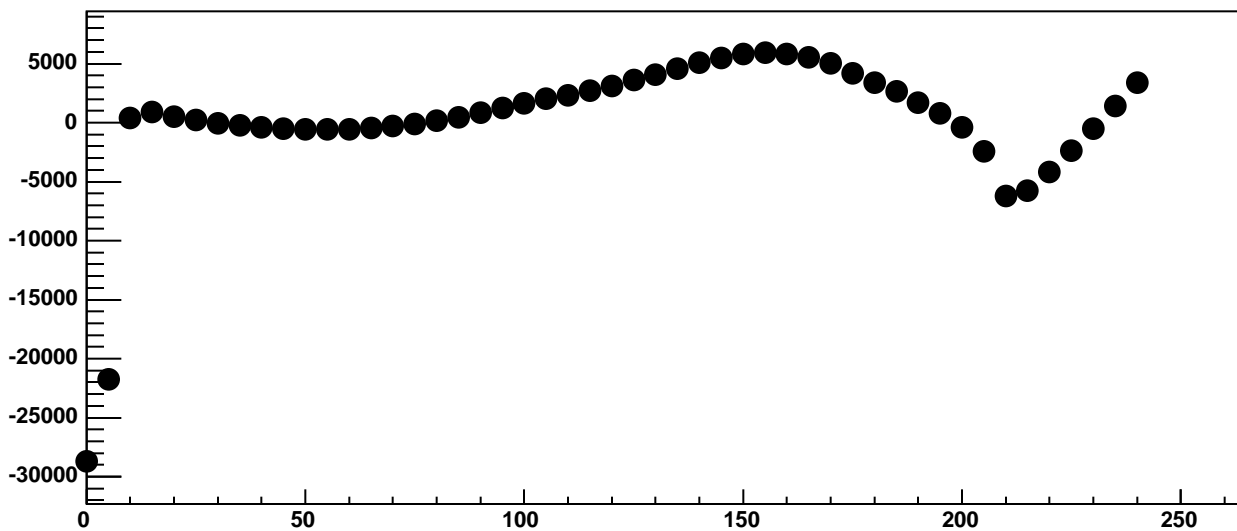
Chip 5, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold



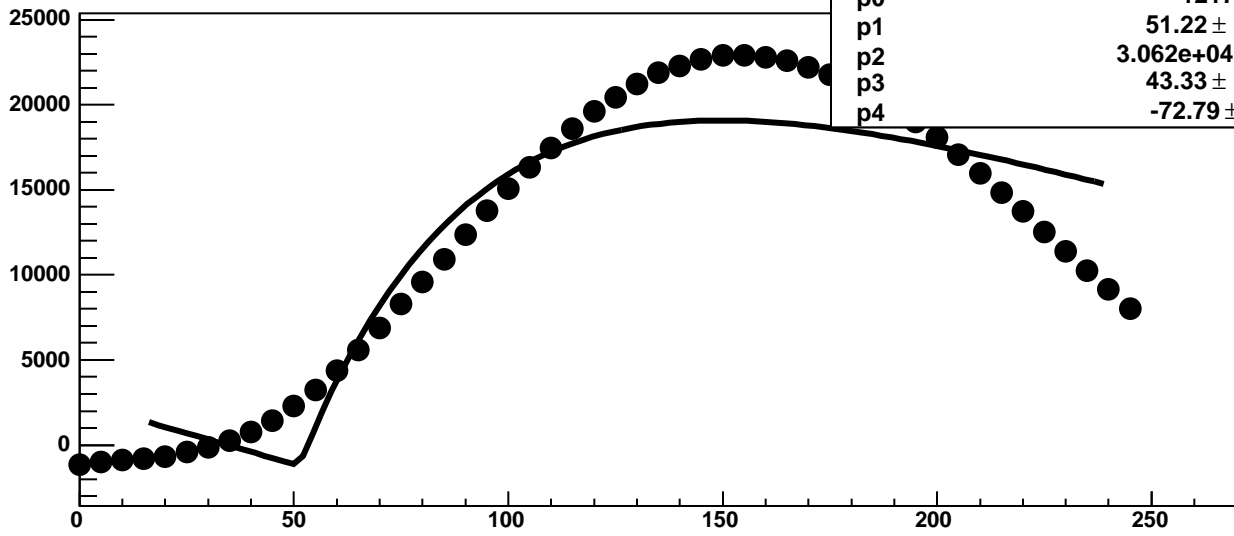
Chip 5, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

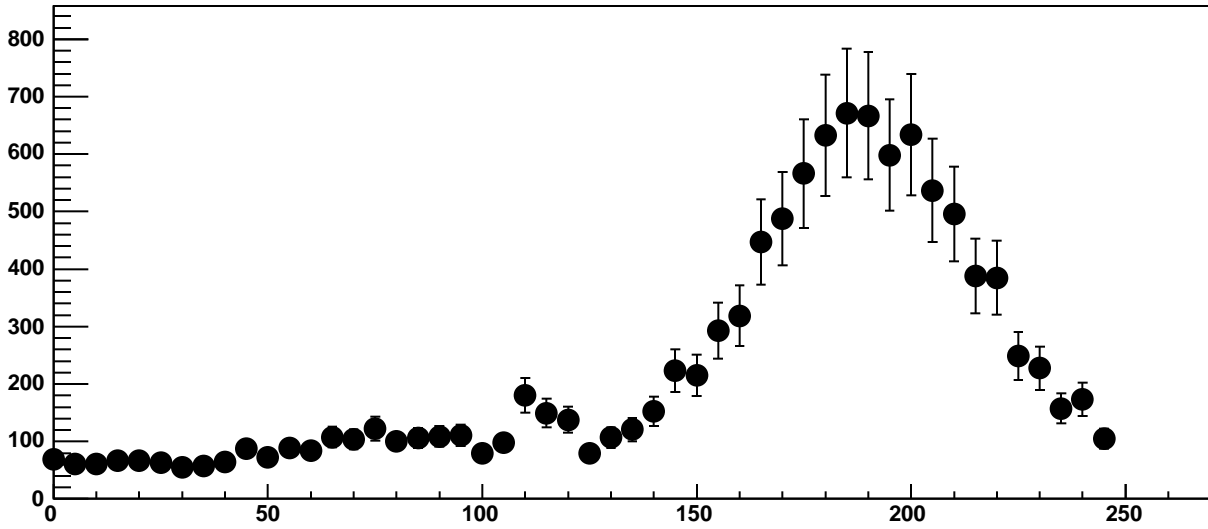


Chip 5, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

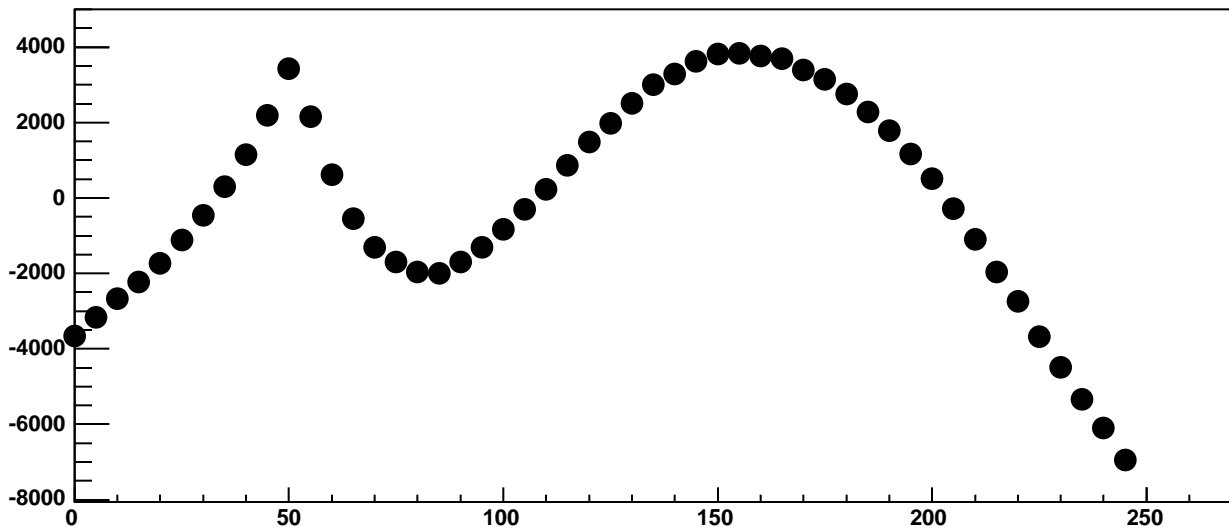


$\chi^2 / \text{ndf}$	2.702e+05 / 41
p0	-1217 ± 7.157
p1	51.22 ± 0.02609
p2	3.062e+04 ± 53.69
p3	43.33 ± 0.08868
p4	-72.79 ± 0.2806

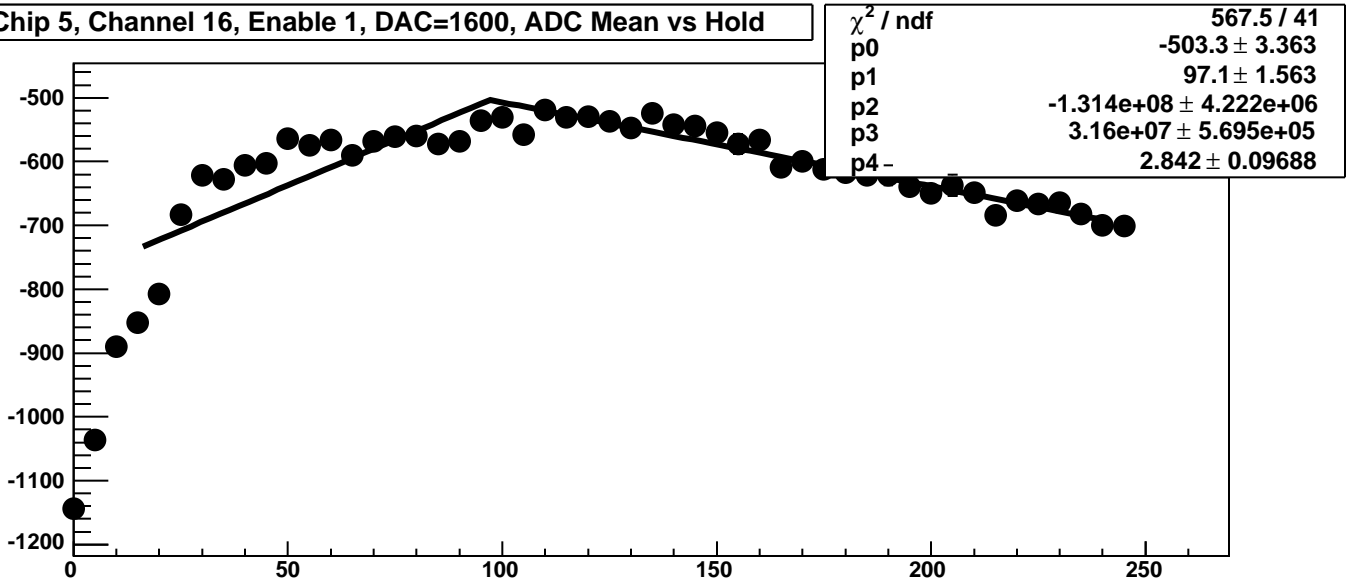
Chip 5, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



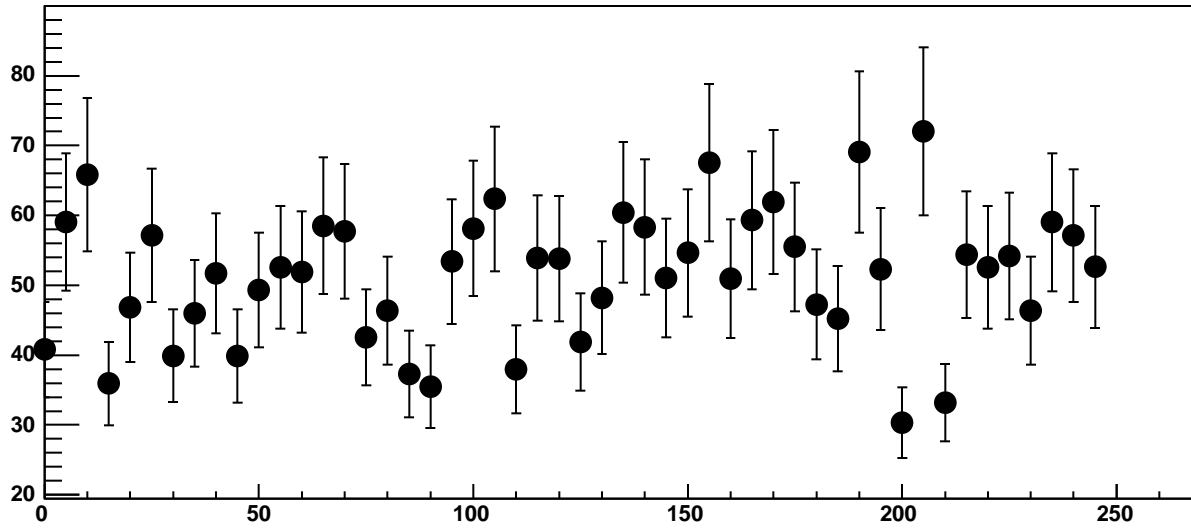
Chip 5, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold



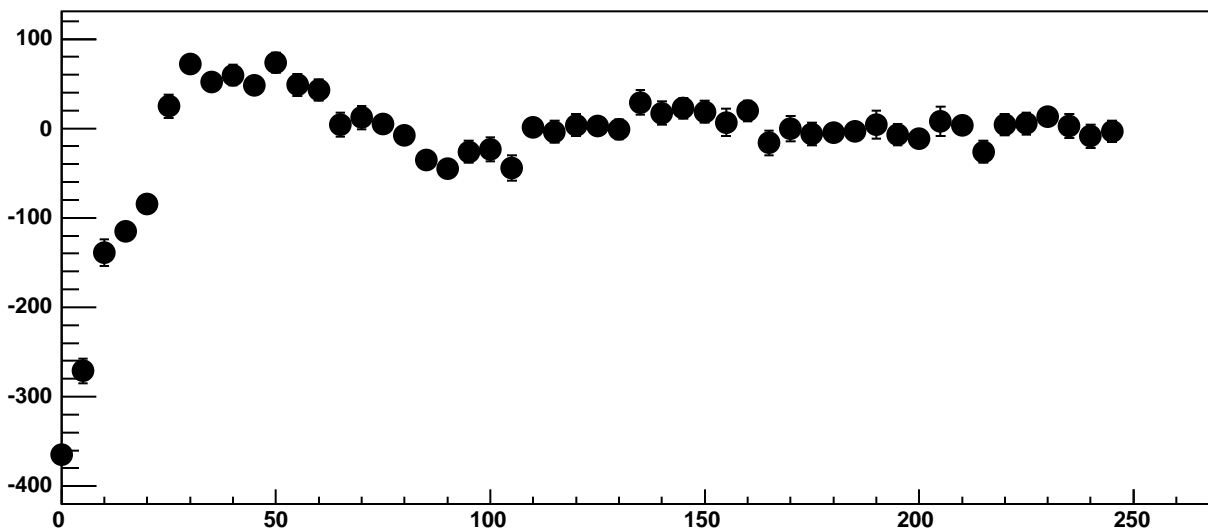
Chip 5, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold



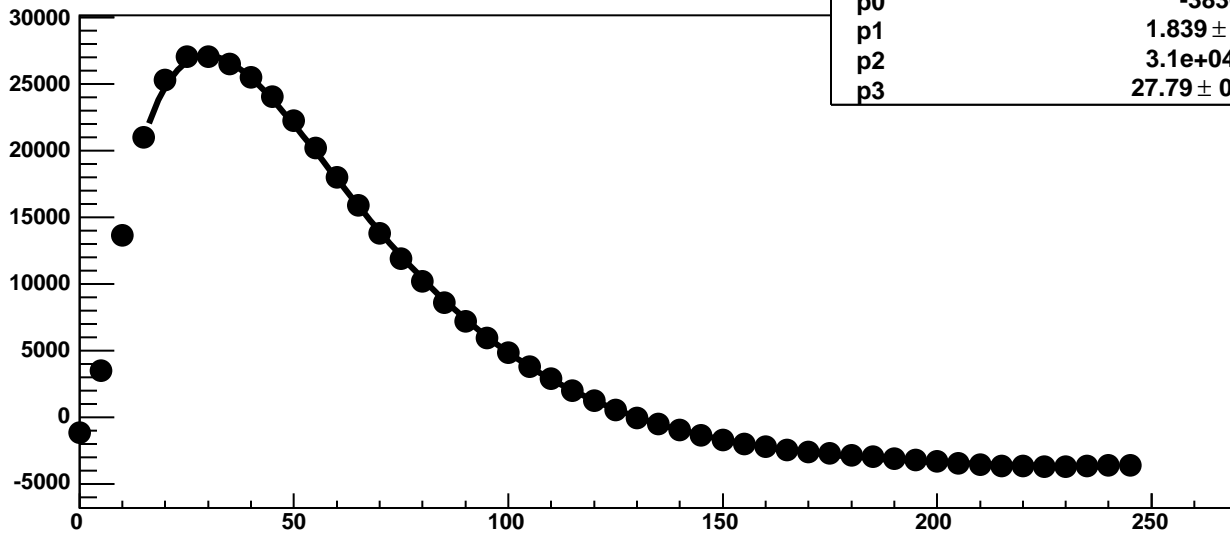
Chip 5, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold

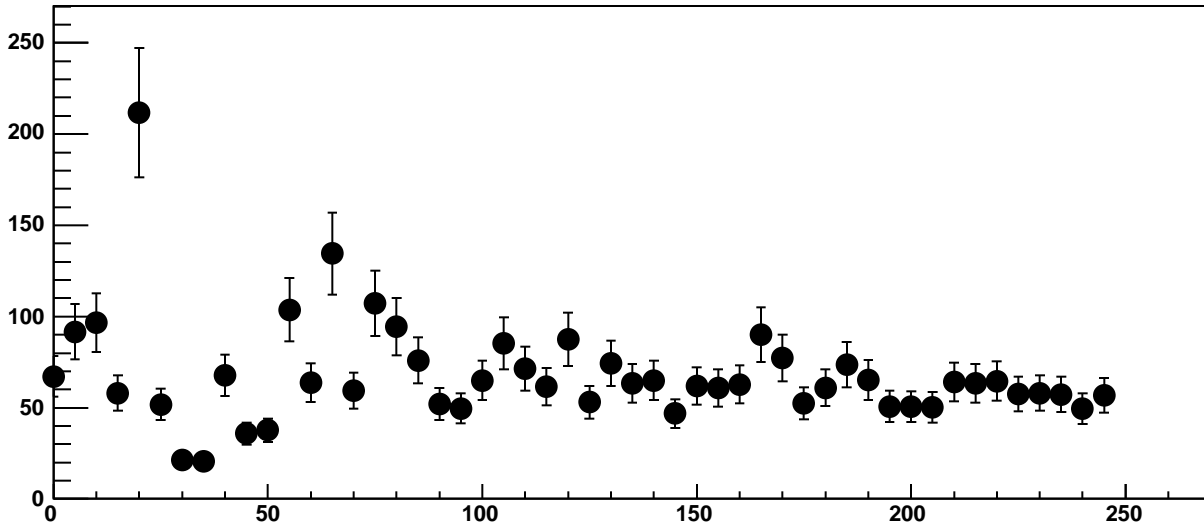


Chip 5, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold

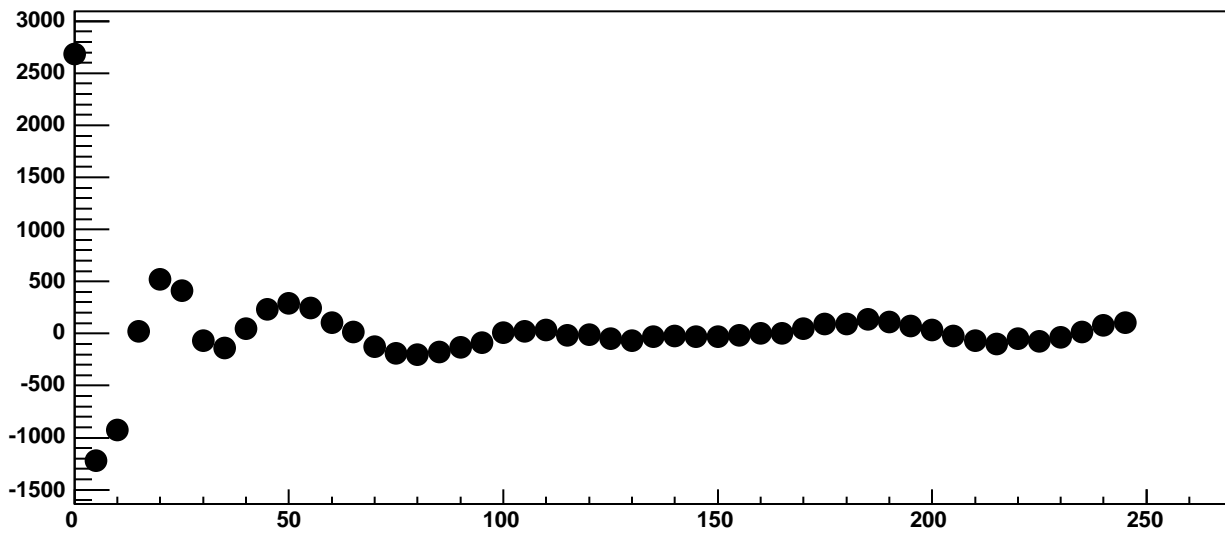


$\chi^2 / \text{ndf}$	5415 / 42
p0	-3836 ± 3.61
p1	1.839 ± 0.01484
p2	3.1e+04 ± 4.402
p3	27.79 ± 0.009654

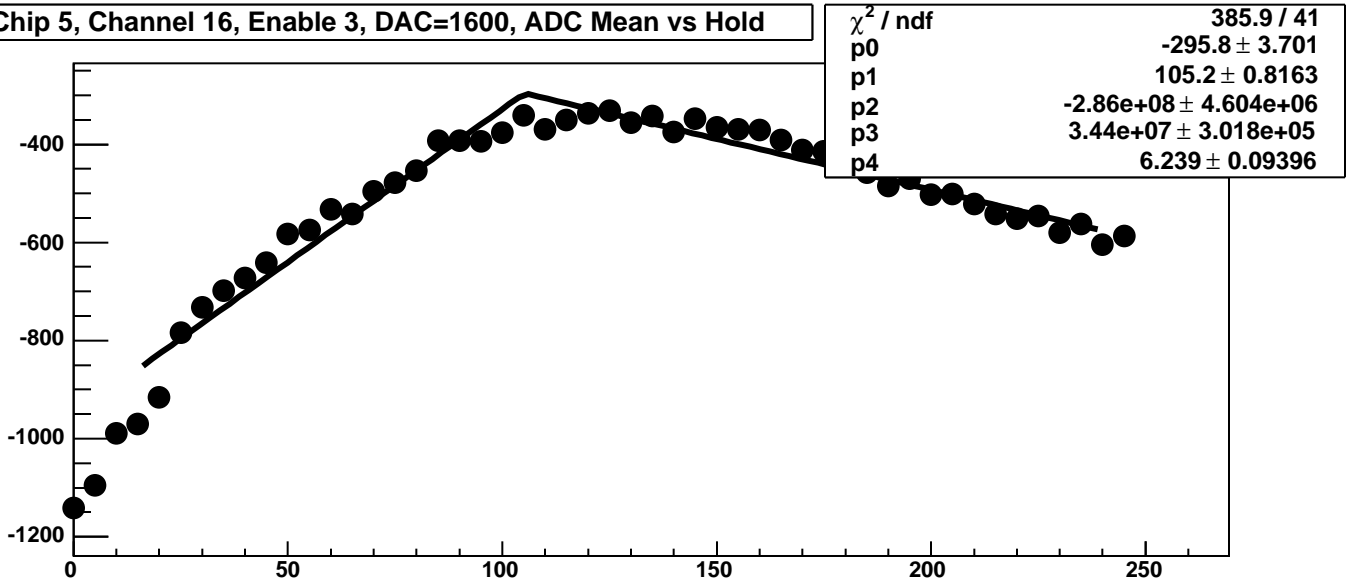
Chip 5, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



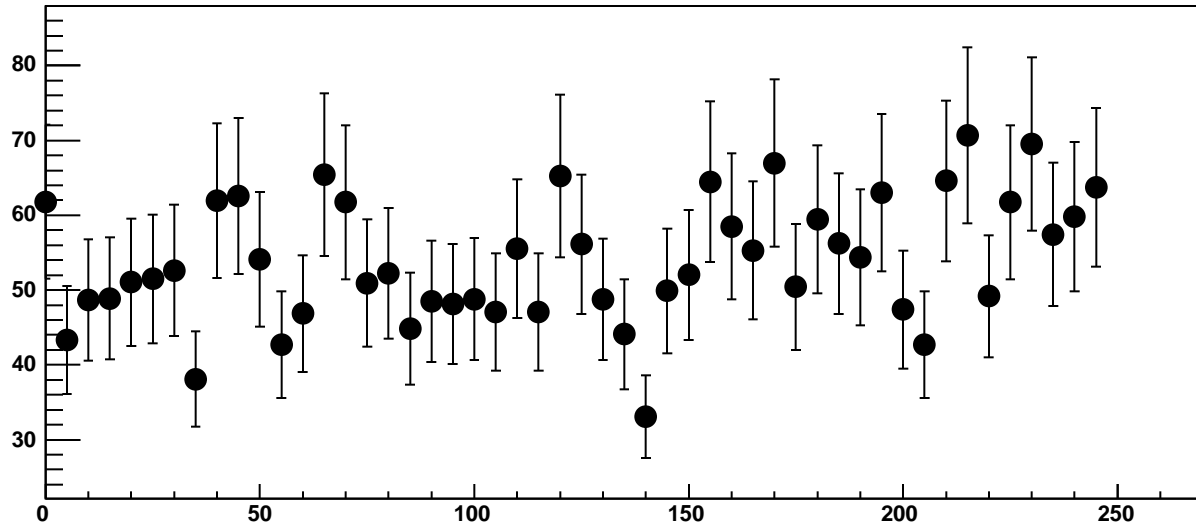
Chip 5, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold



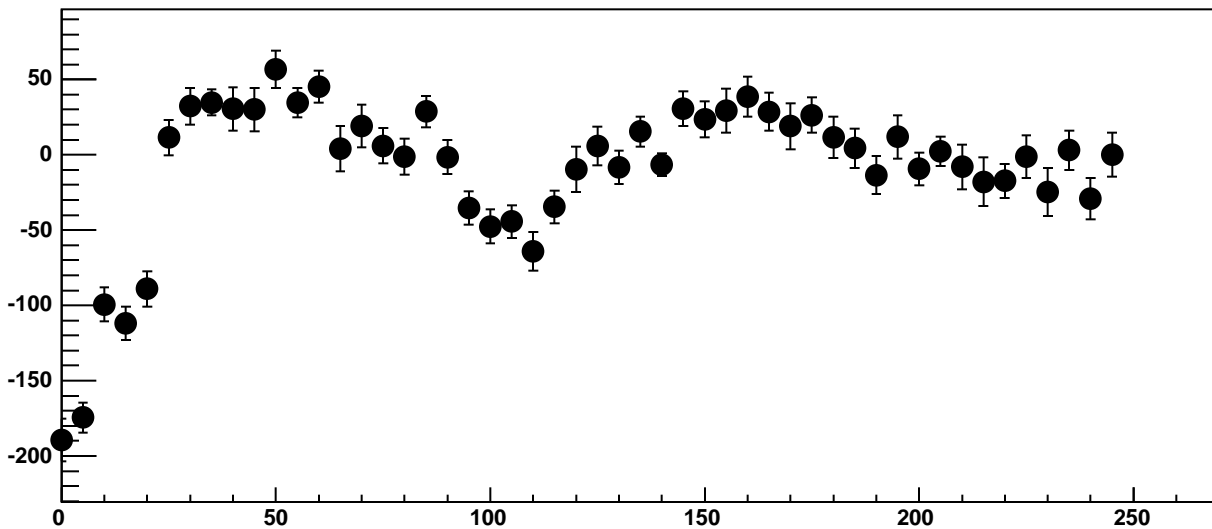
Chip 5, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold



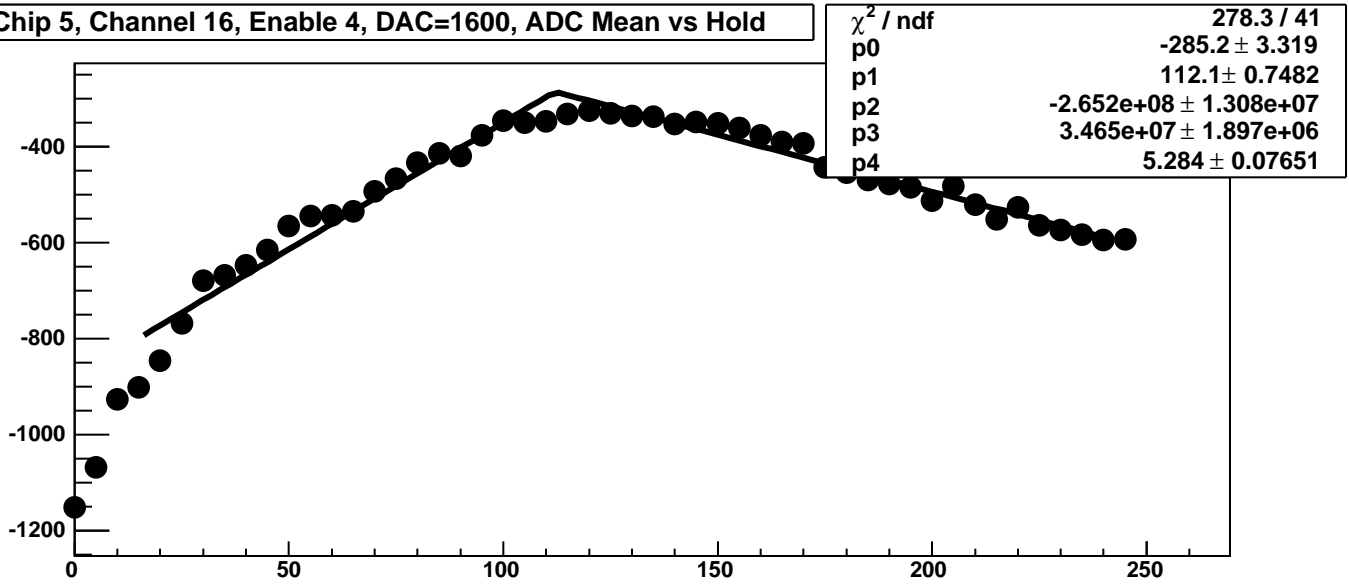
Chip 5, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



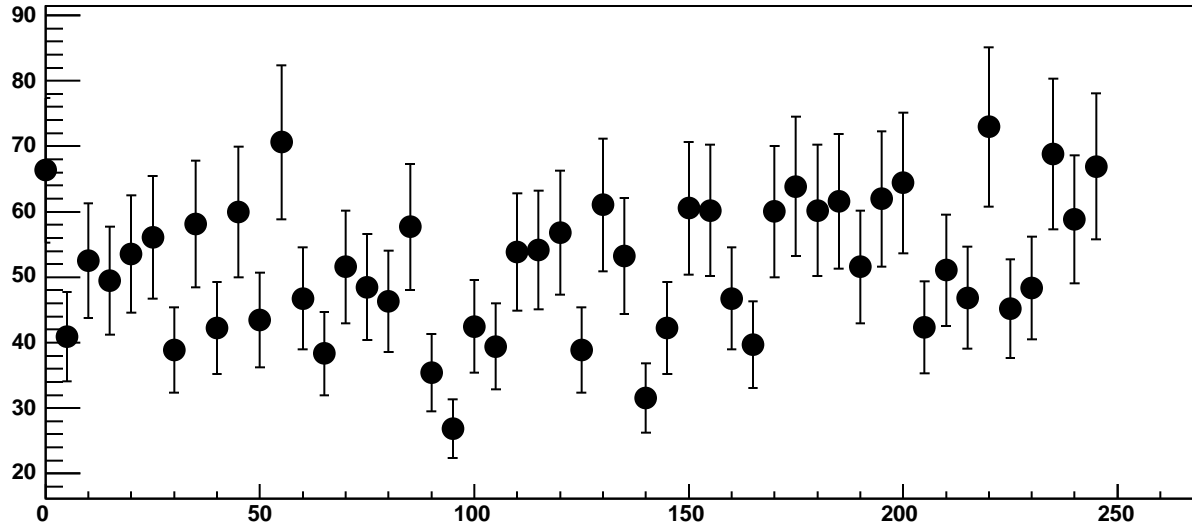
Chip 5, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold



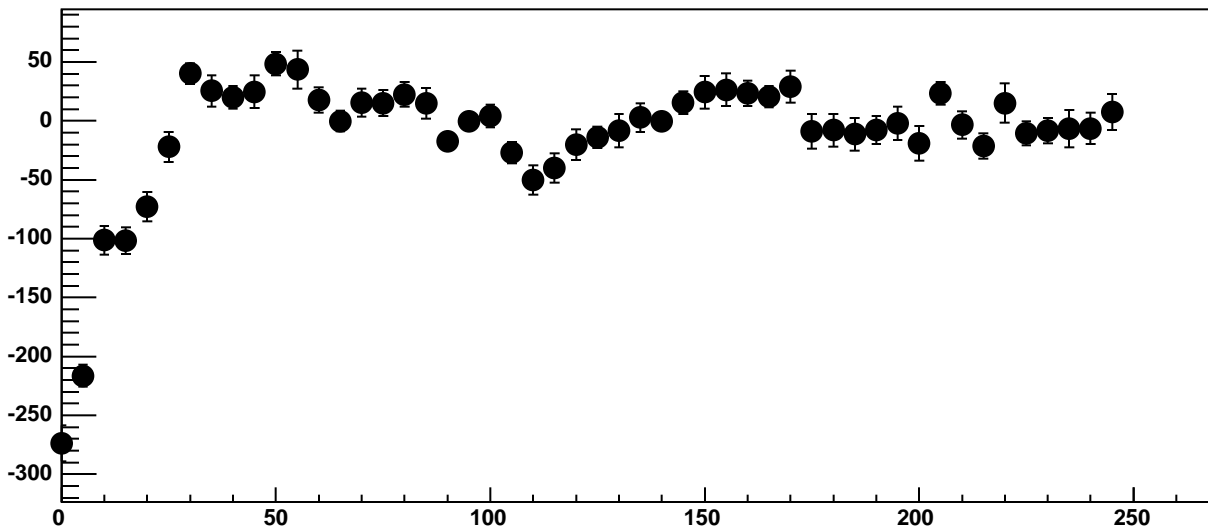
Chip 5, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold



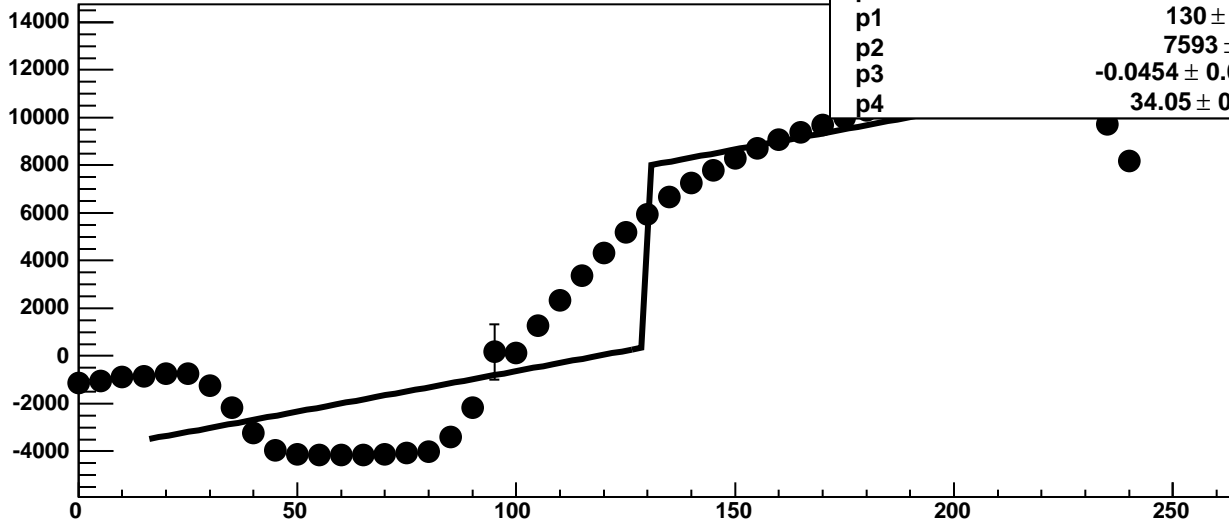
Chip 5, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



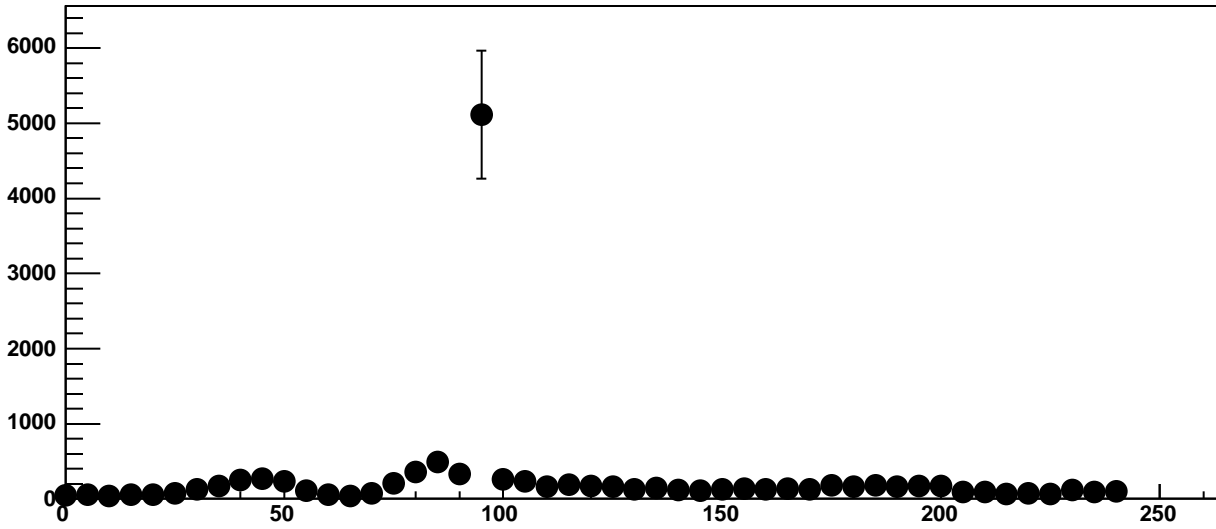
Chip 5, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold



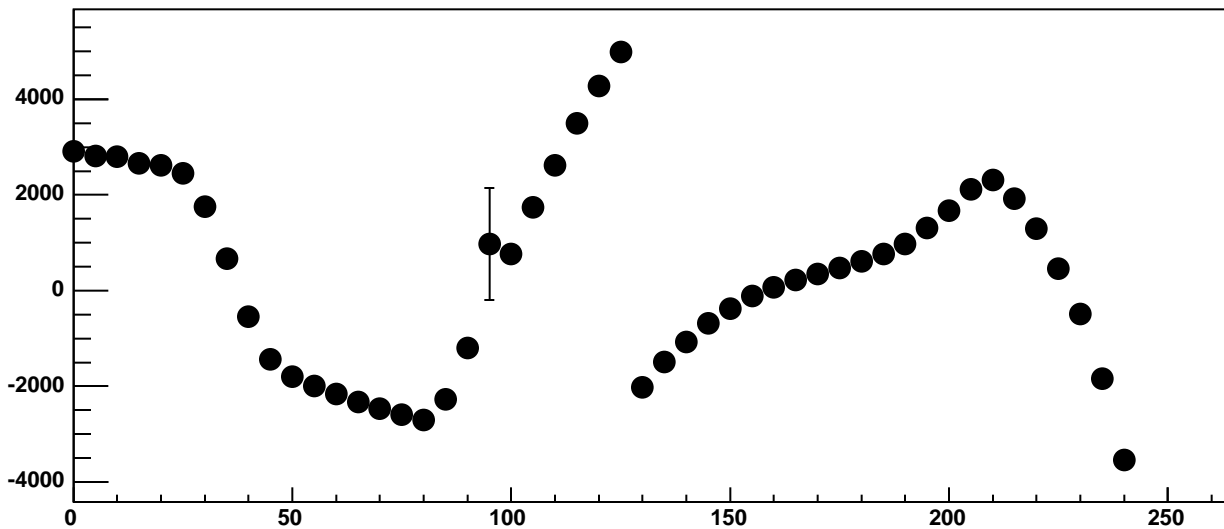
Chip 5, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 5, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold

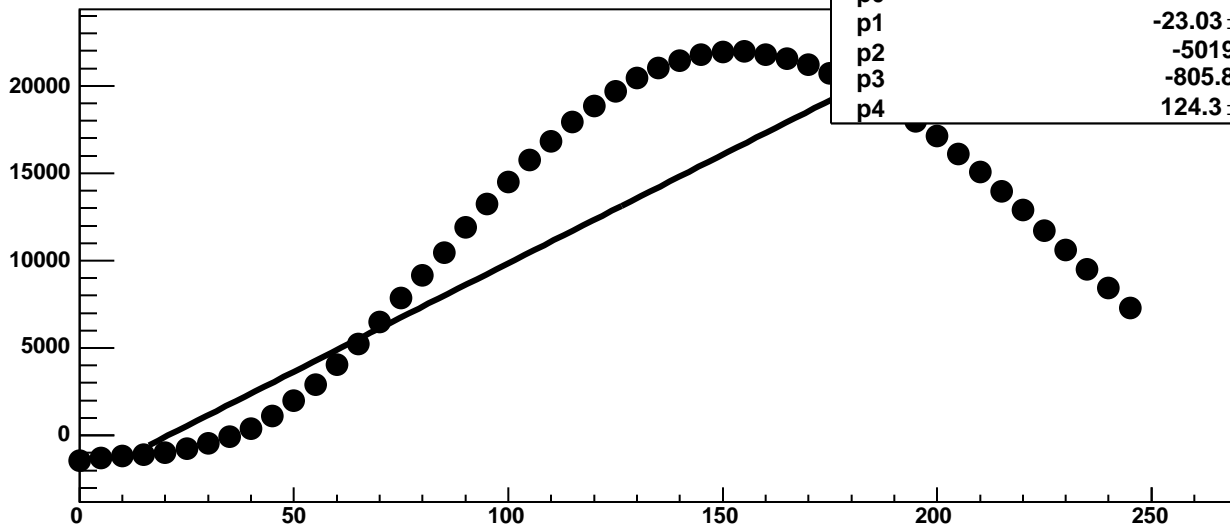


Chip 5, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold



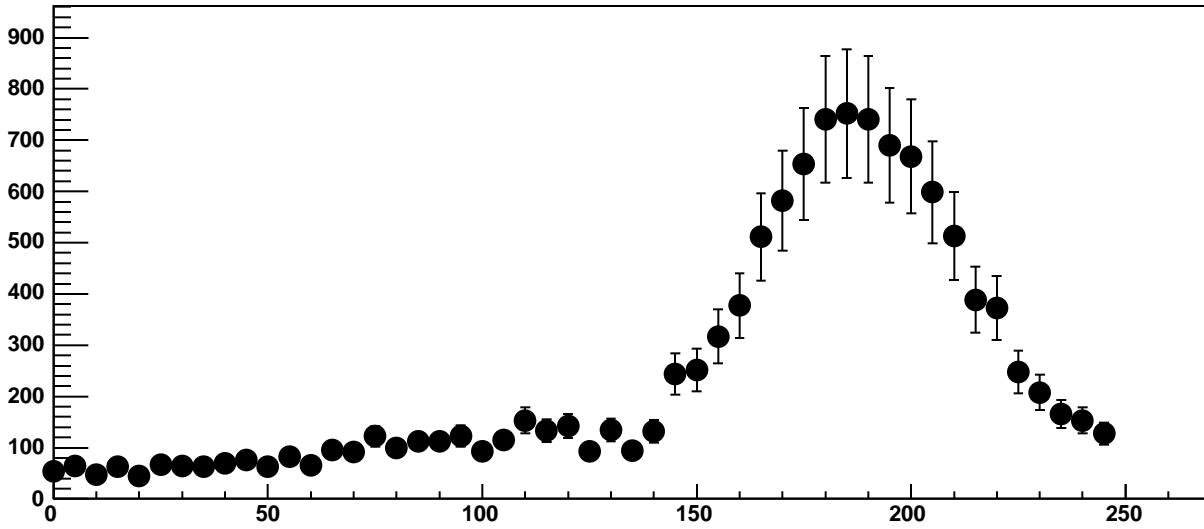


Chip 5, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

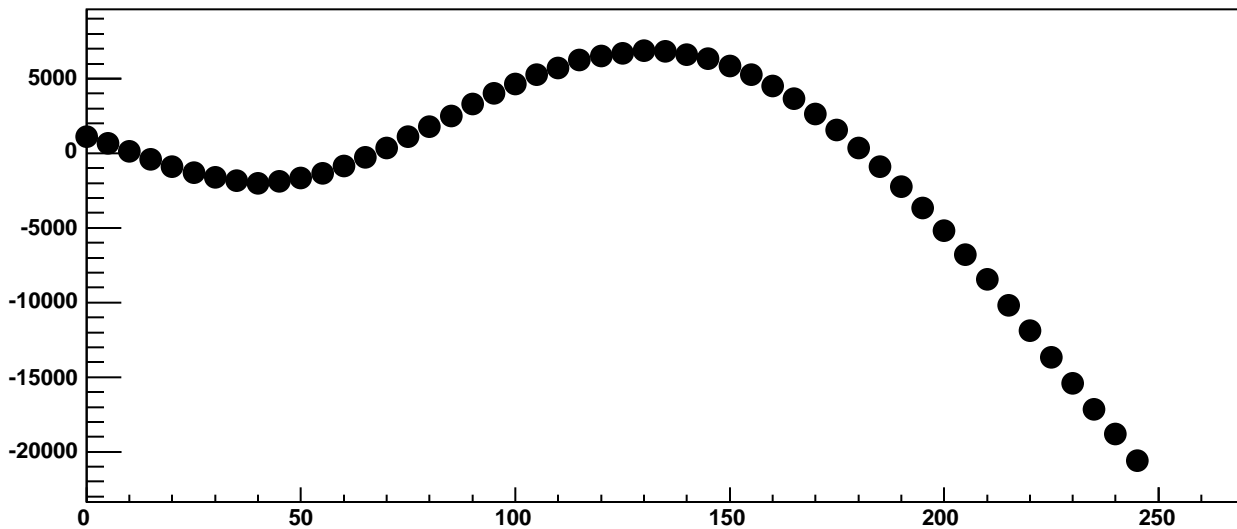


$\chi^2 / \text{ndf}$	1.363e+06 / 41
p0	-418.6 ± 21.26
p1	-23.03 ± 0.1509
p2	-5019 ± 23.66
p3	-805.8 ± 16.37
p4	124.3 ± 0.1368

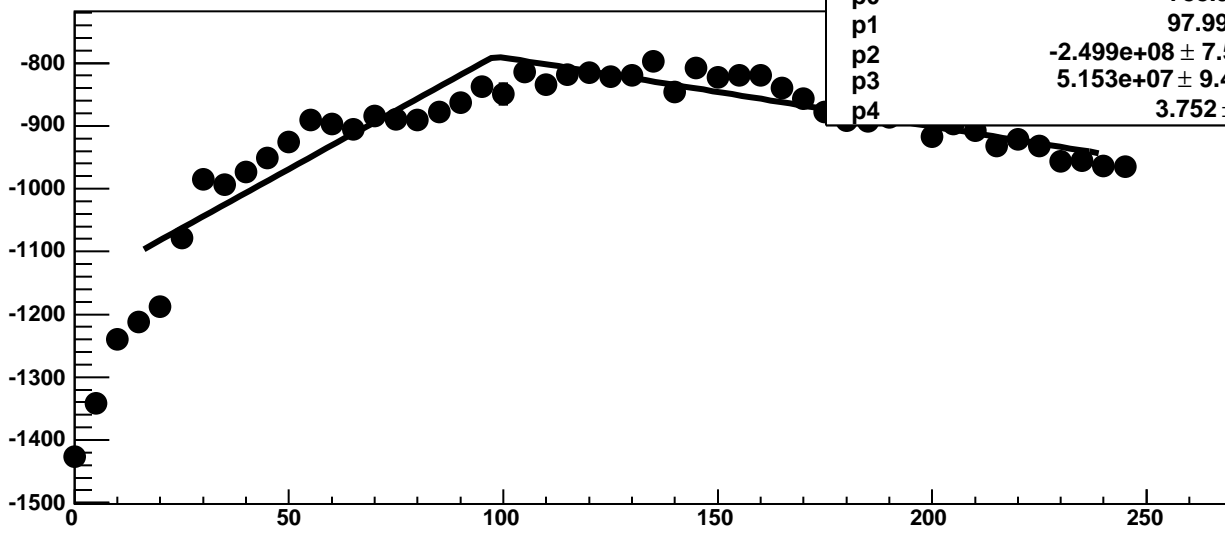
Chip 5, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



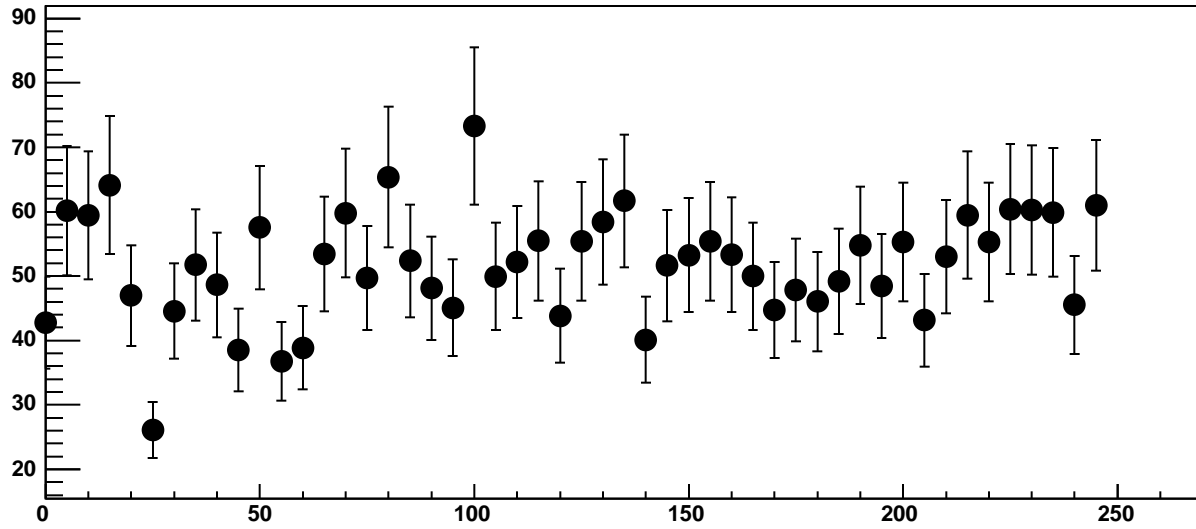
Chip 5, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold



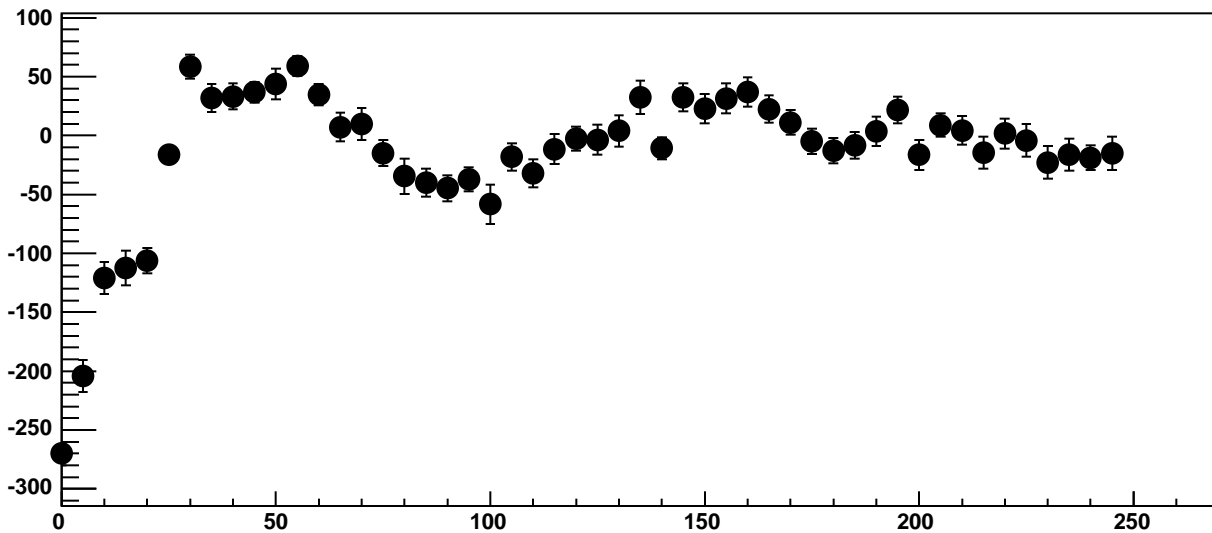
Chip 5, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold



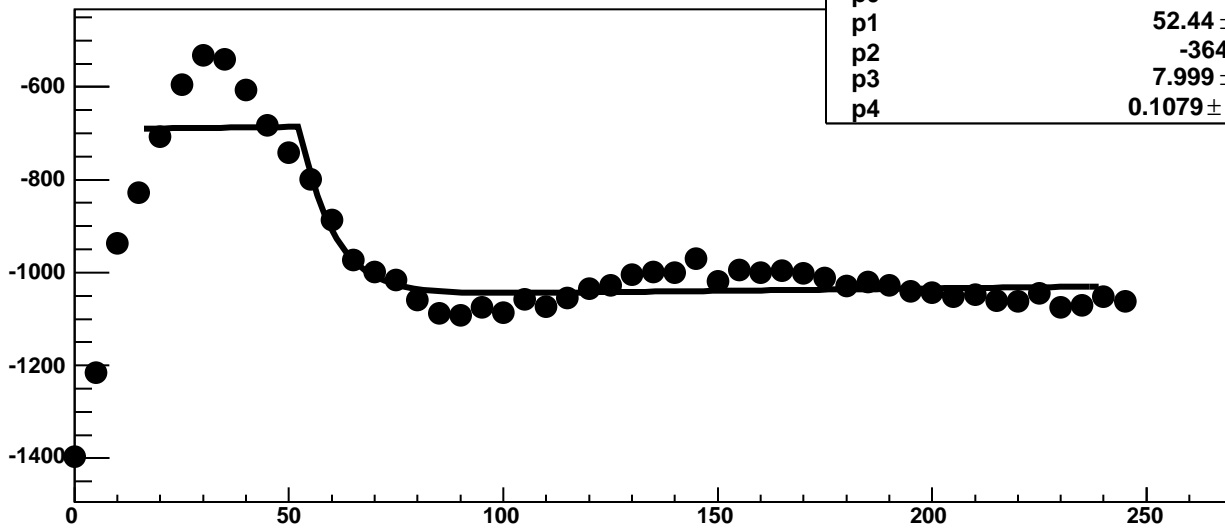
Chip 5, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

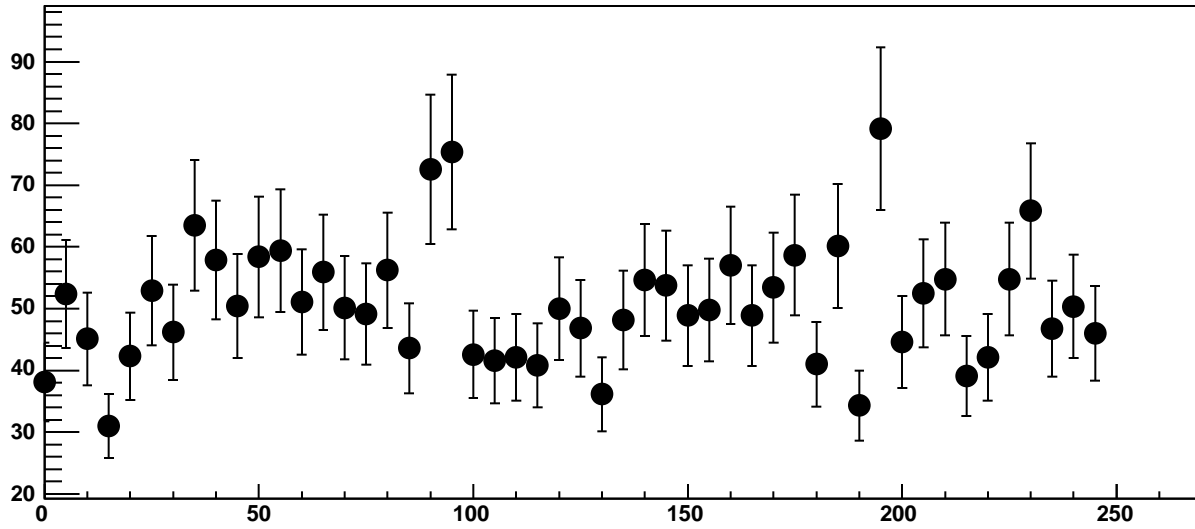


Chip 5, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold

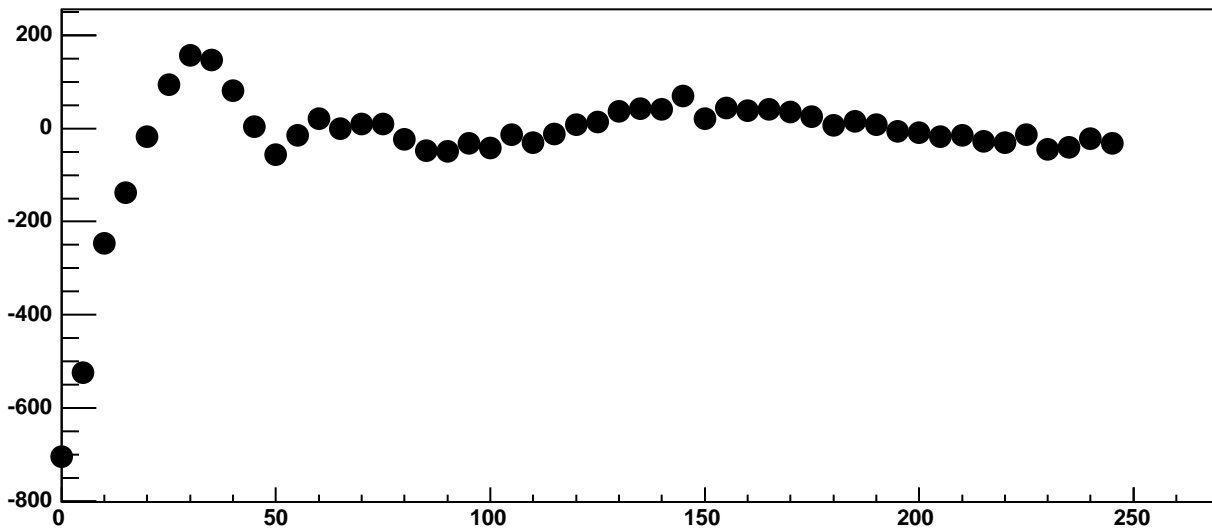


$\chi^2 / \text{ndf}$	1073 / 41
p0	$-685.9 \pm 3.915$
p1	$52.44 \pm 0.4935$
p2	$-364 \pm 6.965$
p3	$7.999 \pm 0.6254$
p4	$0.1079 \pm 0.04157$

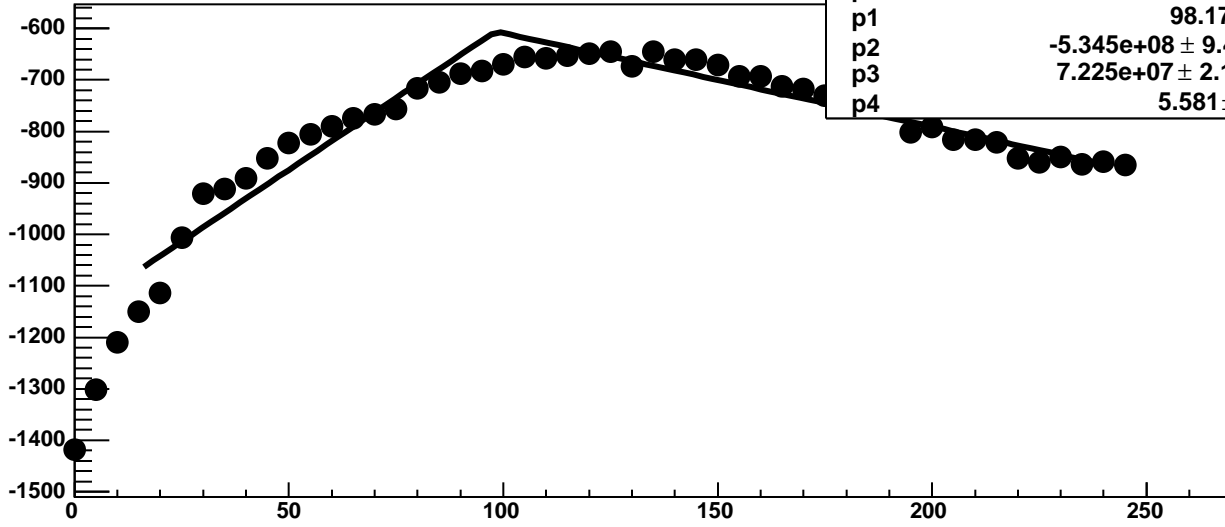
Chip 5, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

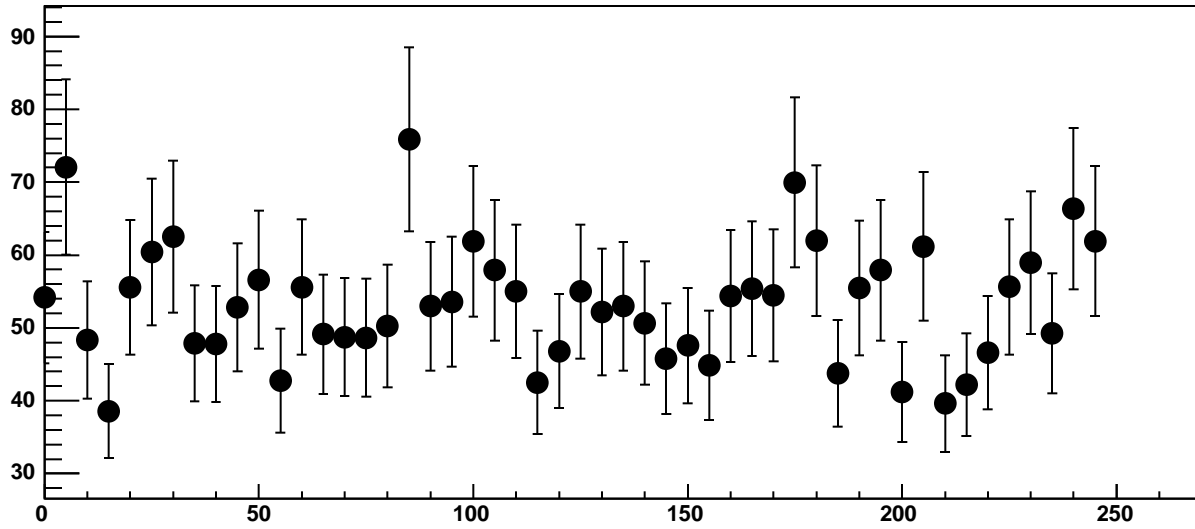


Chip 5, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

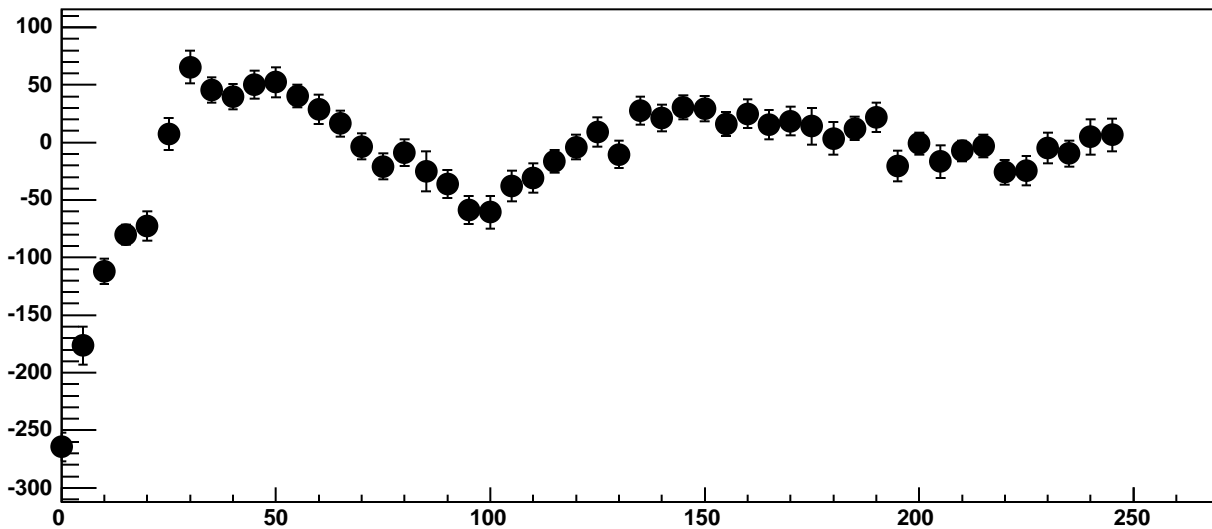


$\chi^2 / \text{ndf}$	352.5 / 41
p0	$-605.6 \pm 3.648$
p1	$98.17 \pm 1.001$
p2	$-5.345\text{e}+08 \pm 9.408\text{e}+06$
p3	$7.225\text{e}+07 \pm 2.186\text{e}+05$
p4	$5.581 \pm 0.1165$

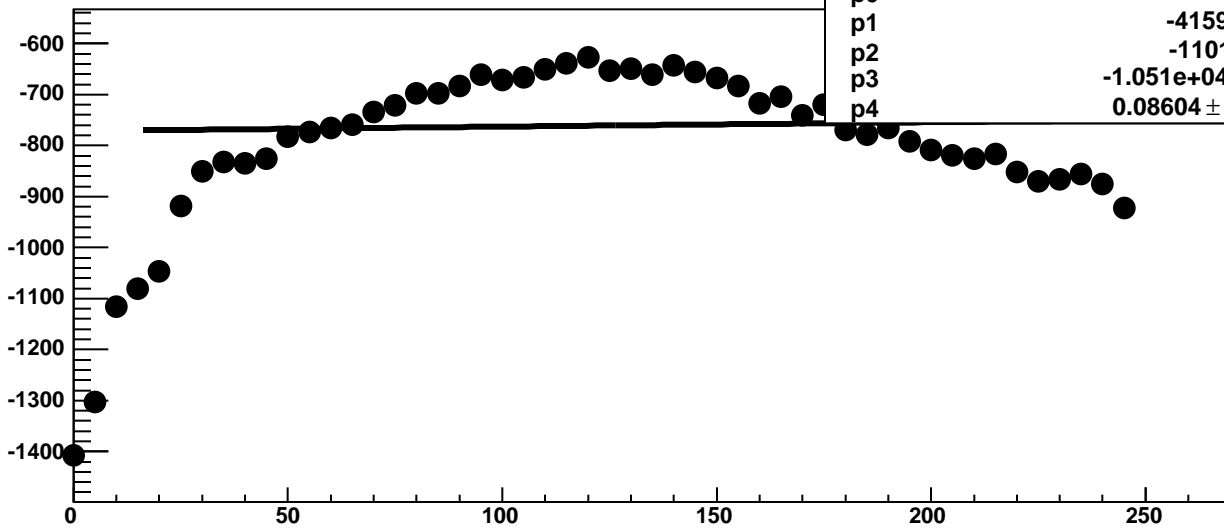
Chip 5, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold

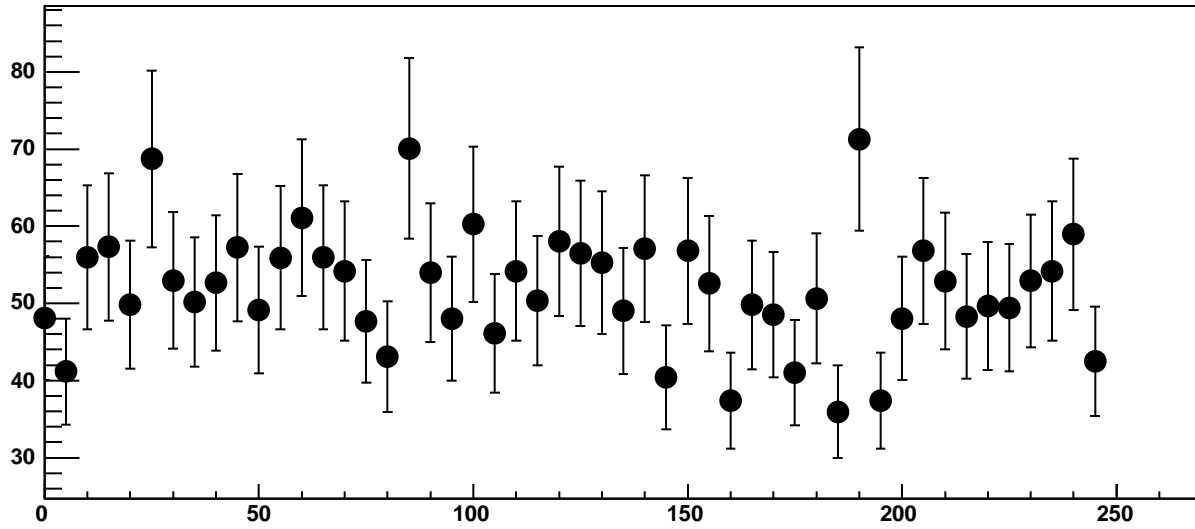


Chip 5, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

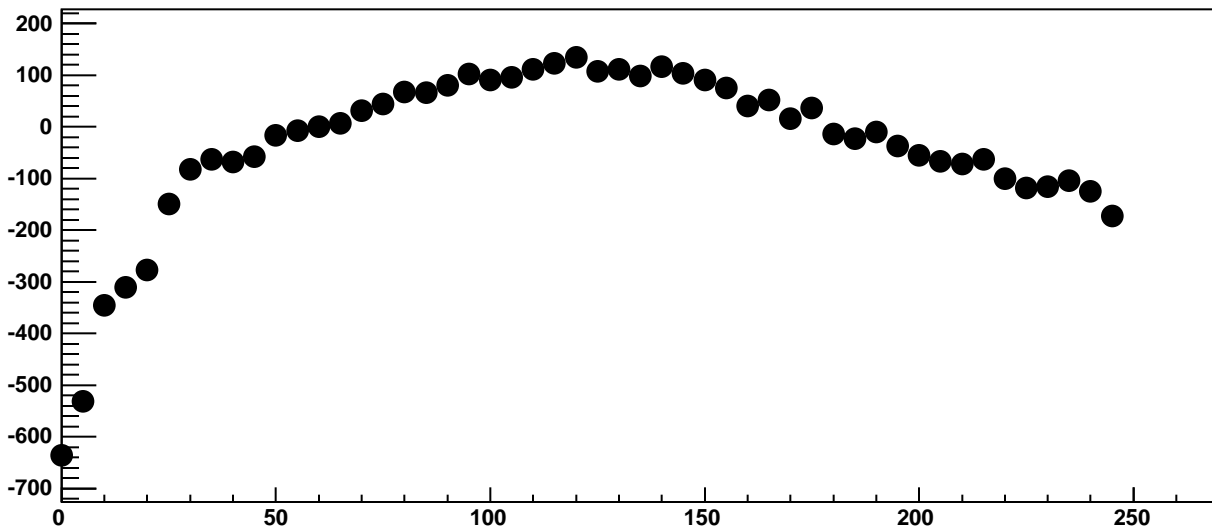


$\chi^2 / \text{ndf}$	3156 / 41
p0	-28.24 ± 23.05
p1	-4159 ± 51.18
p2	-1101 ± 95.26
p3	-1.051e+04 ± 903.2
p4	0.08604 ± 0.02653

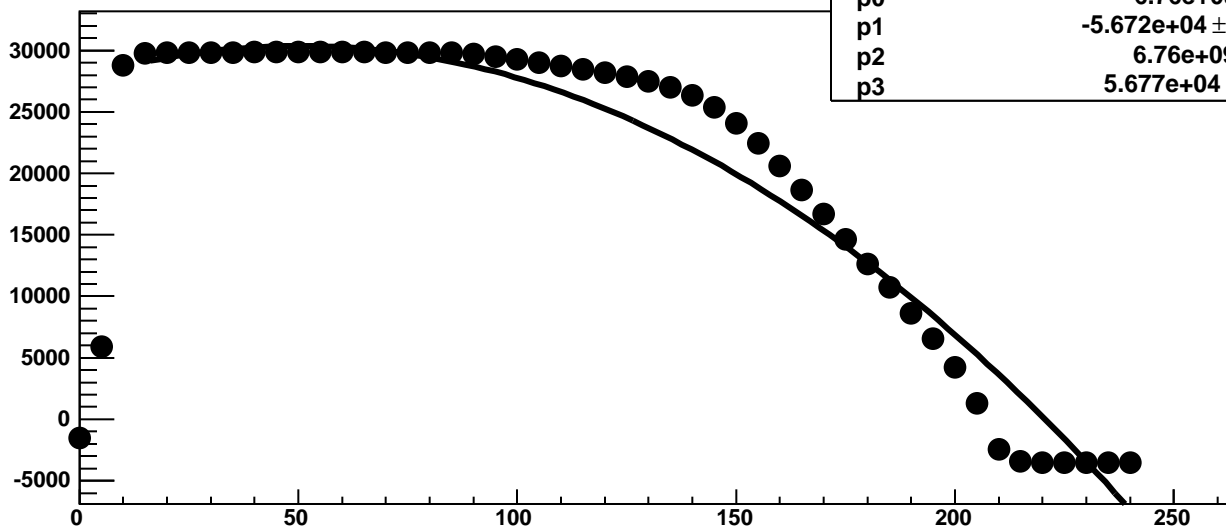
Chip 5, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 5, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

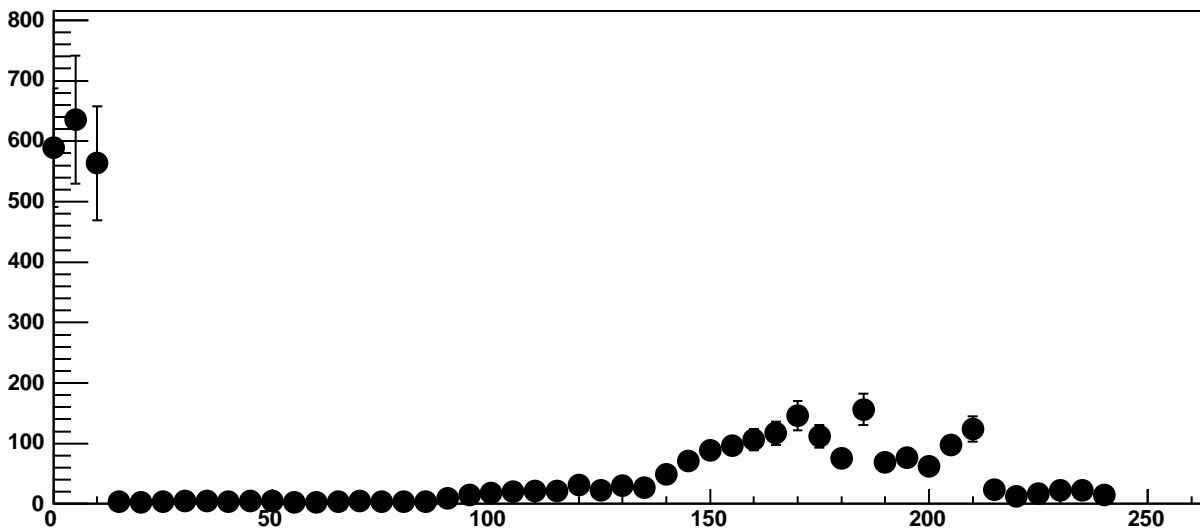


Chip 5, Channel 17, Enable 5!, DAC=1600, ADC Mean vs Hold

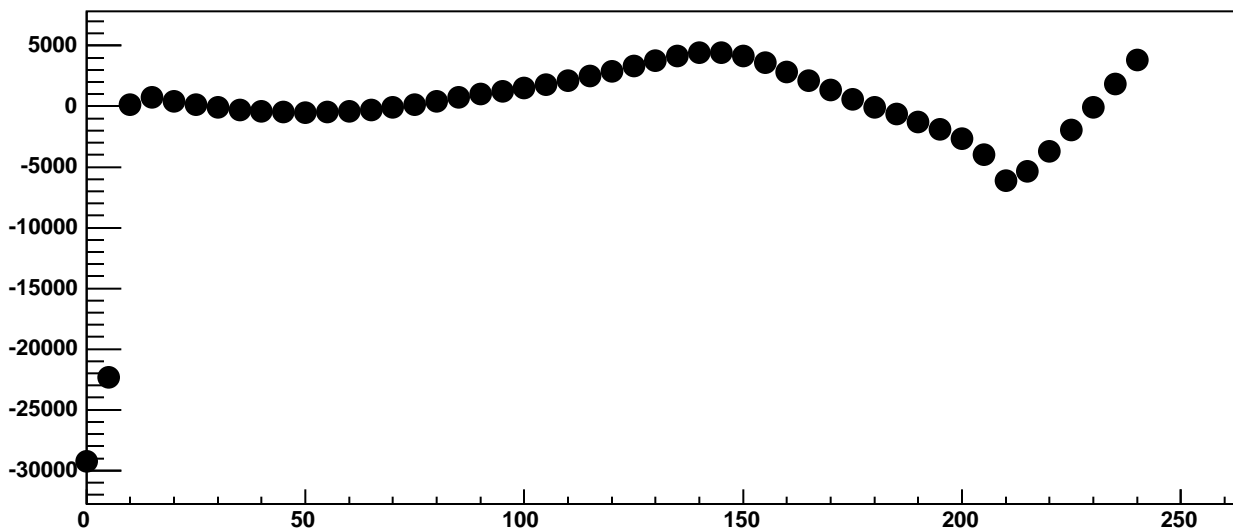


$\chi^2 / \text{ndf}$	1.061e+07 / 42
p0	-6.76e+09 $\pm$ 3.201
p1	-5.672e+04 $\pm$ 0.04227
p2	6.76e+09 $\pm$ 3.201
p3	5.677e+04 $\pm$ 0.0422

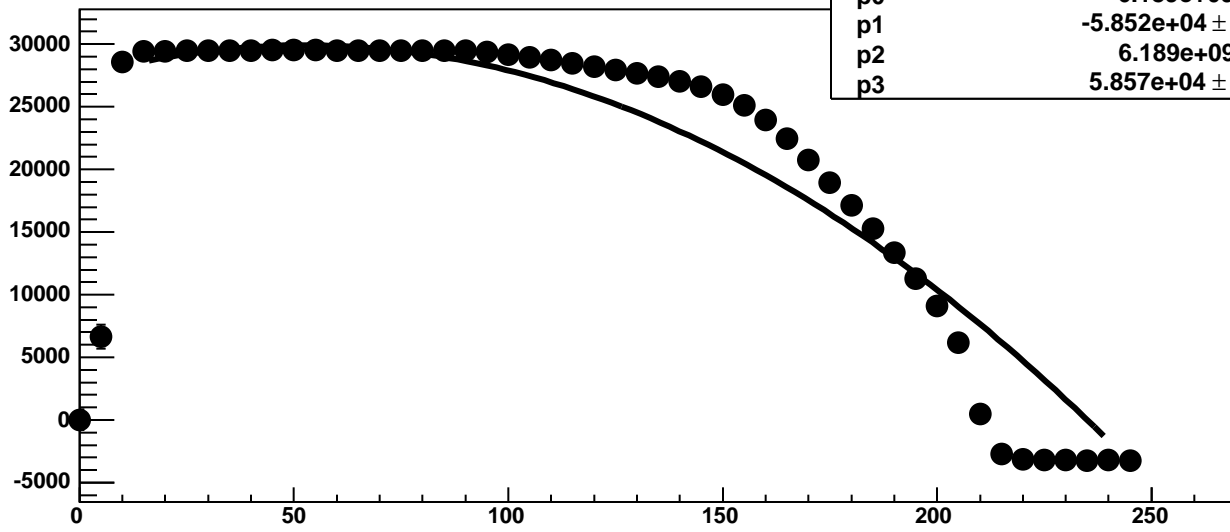
Chip 5, Channel 17, Enable 5!, DAC=1600, ADC Noise vs Hold



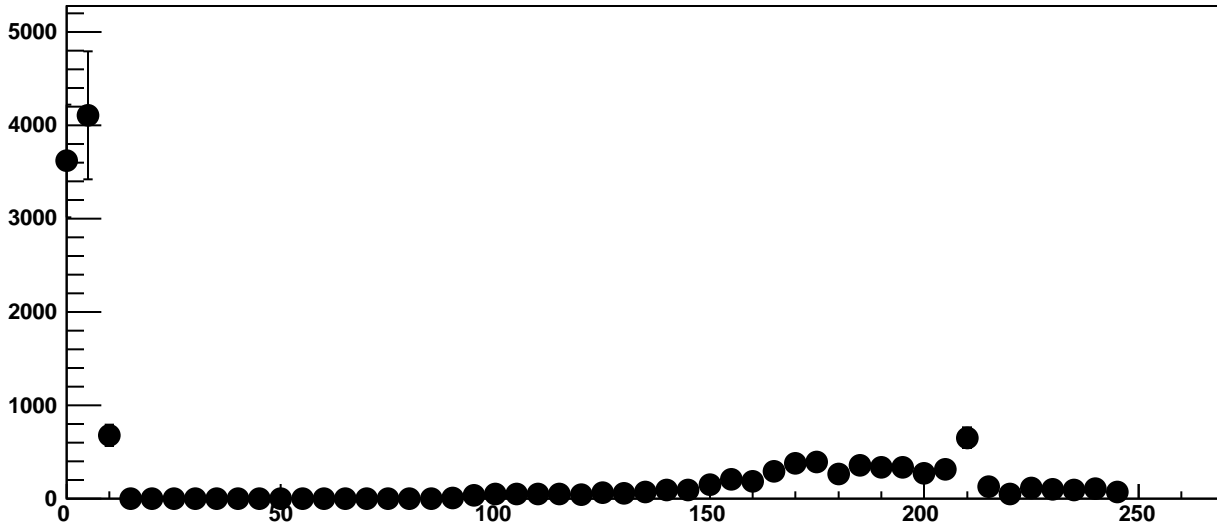
Chip 5, Channel 17, Enable 5!, DAC=1600, ADC Residuals vs Hold



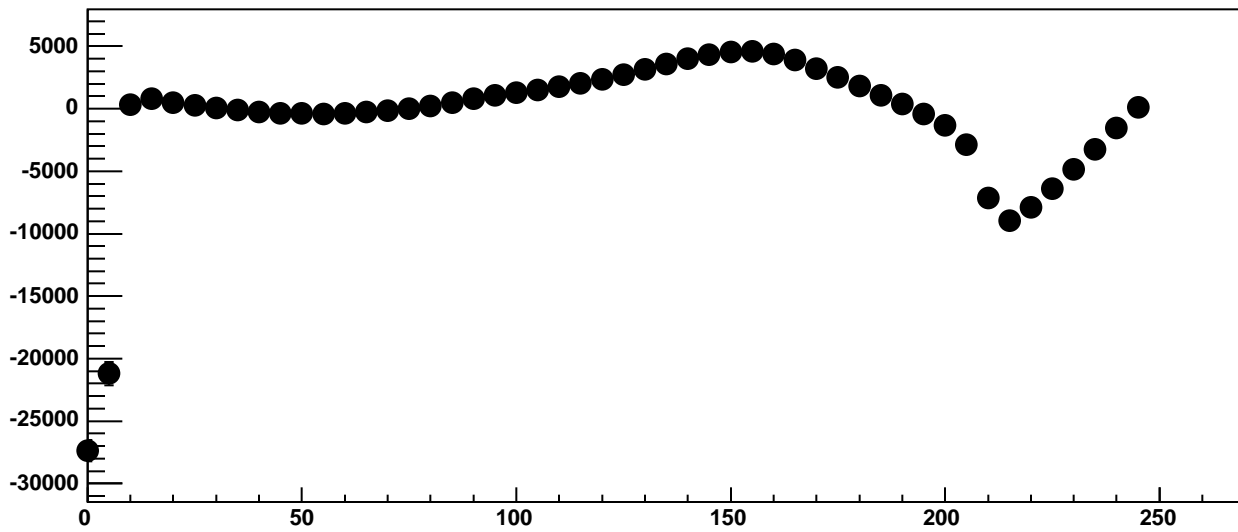
Chip 6, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold



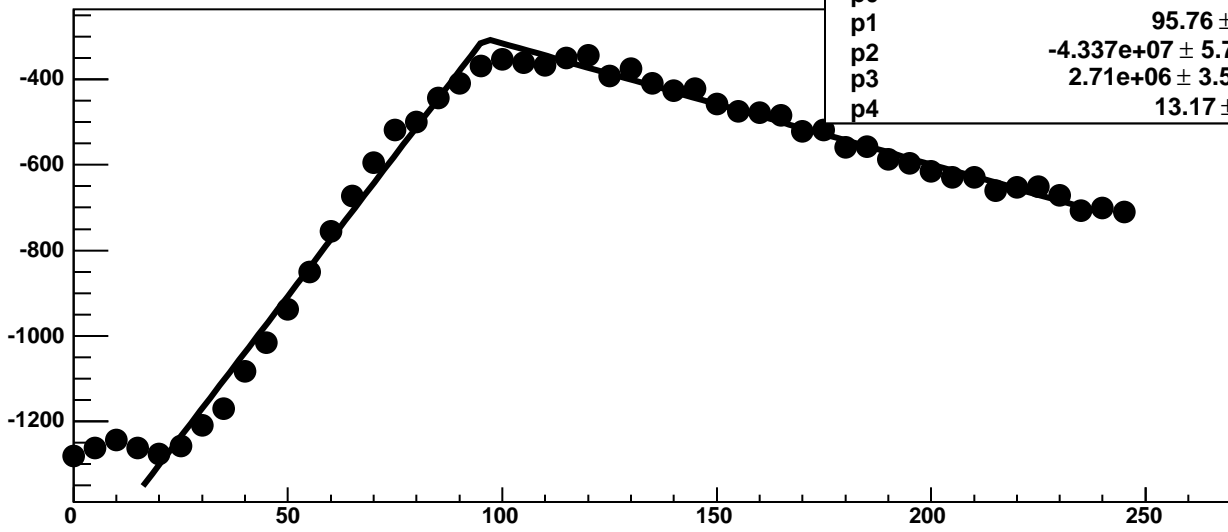
Chip 6, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



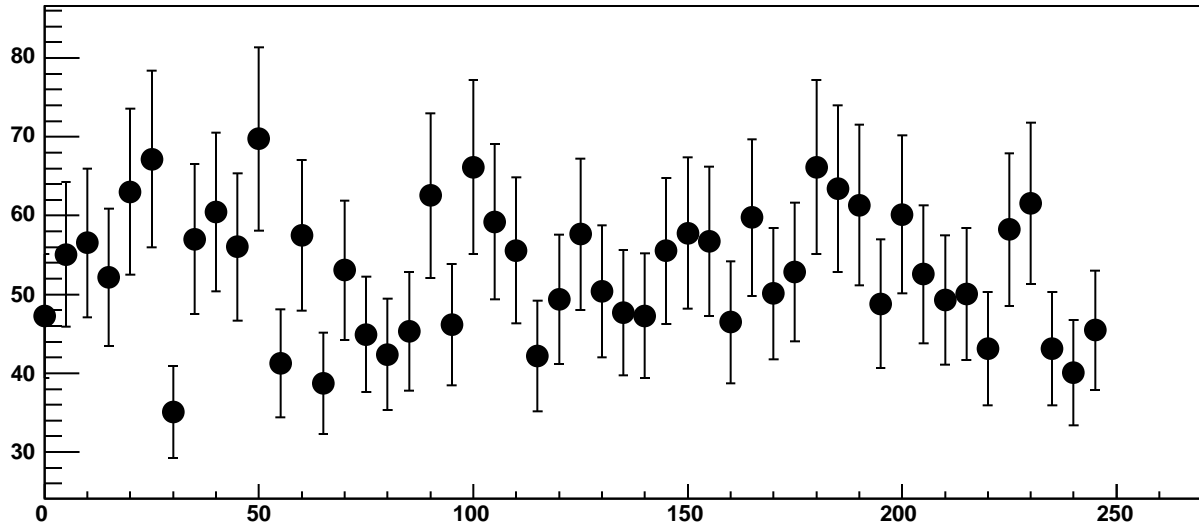
Chip 6, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold



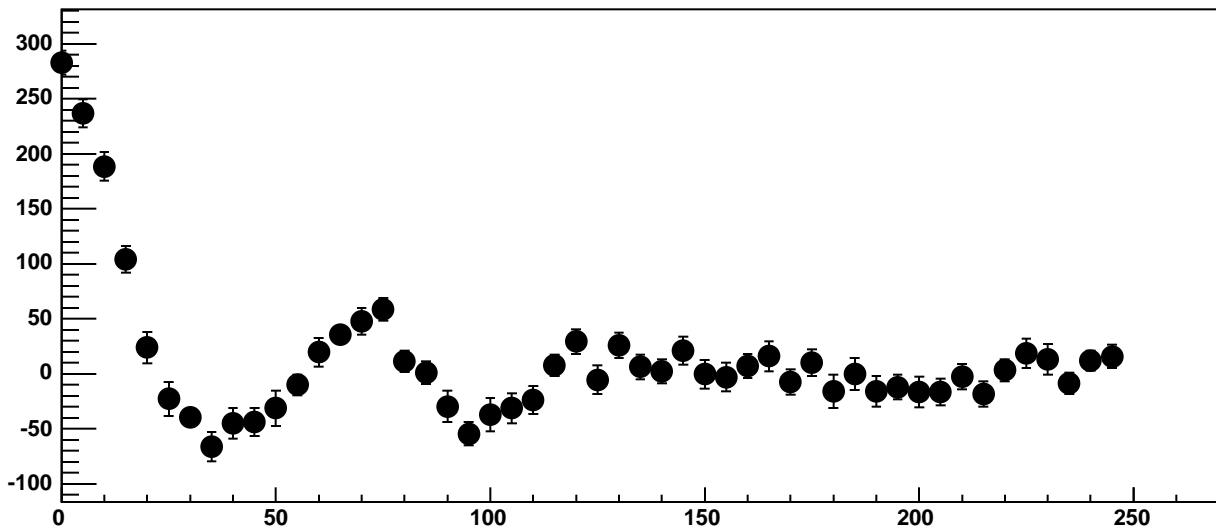
Chip 6, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 6, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

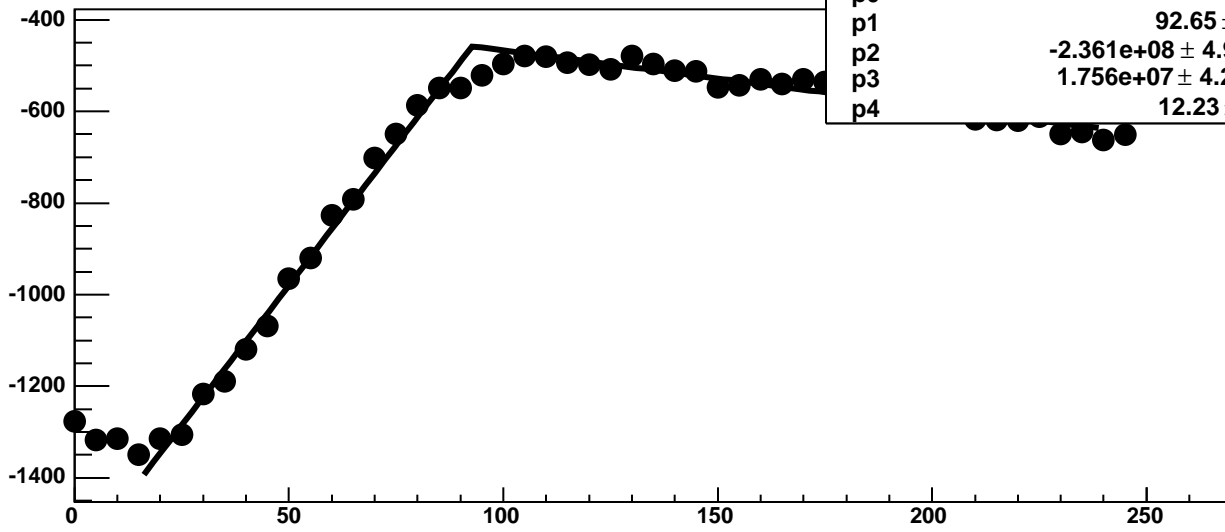


Chip 6, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



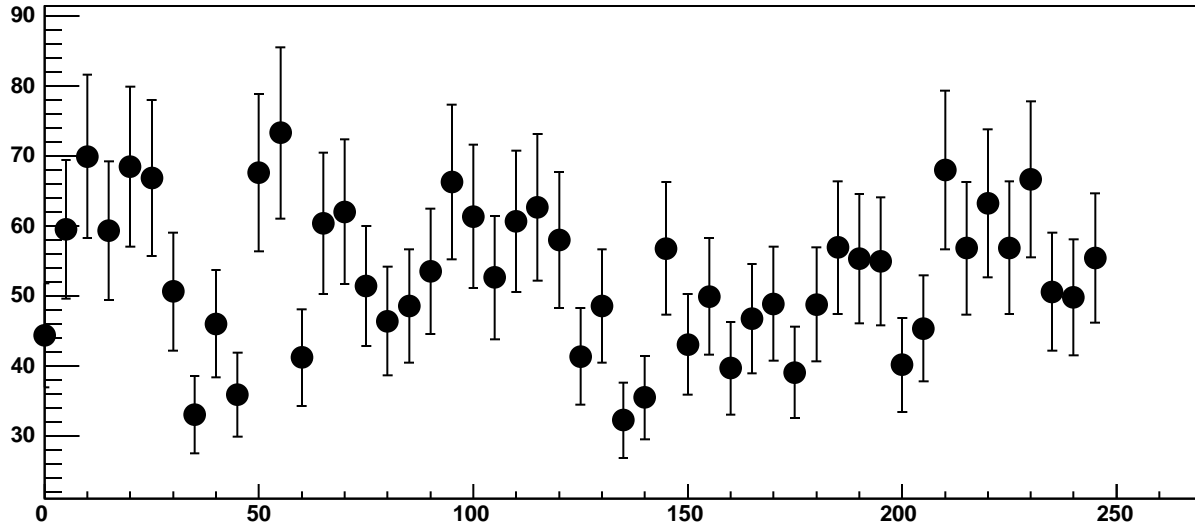


Chip 6, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

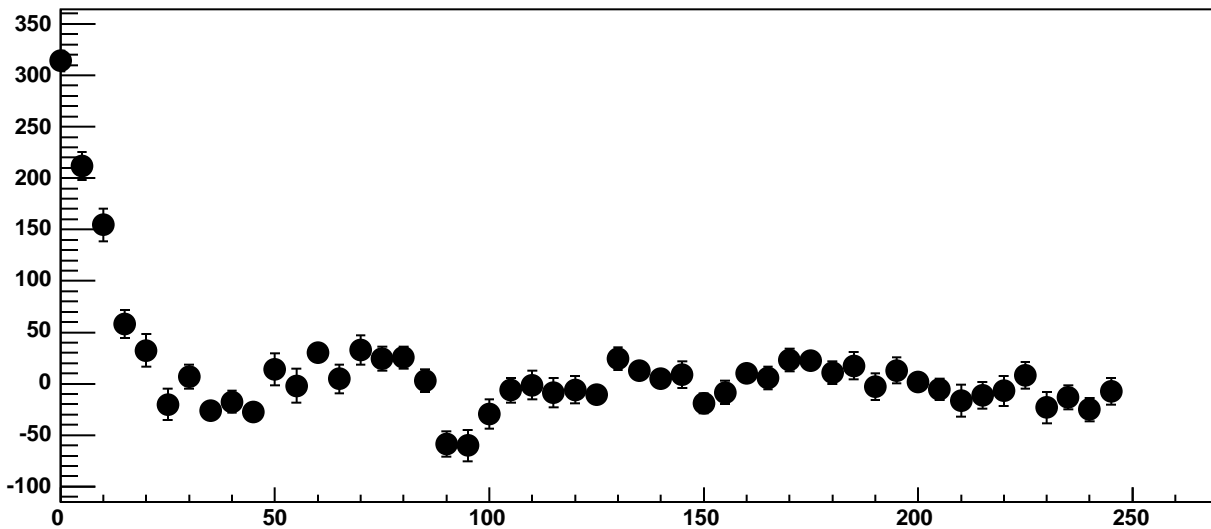


$\chi^2 / \text{ndf}$	161.5 / 41
p0	$-457.9 \pm 3.935$
p1	$92.65 \pm 0.4883$
p2	$-2.361\text{e}+08 \pm 4.928\text{e}+06$
p3	$1.756\text{e}+07 \pm 4.279\text{e}+05$
p4	$12.23 \pm 0.1131$

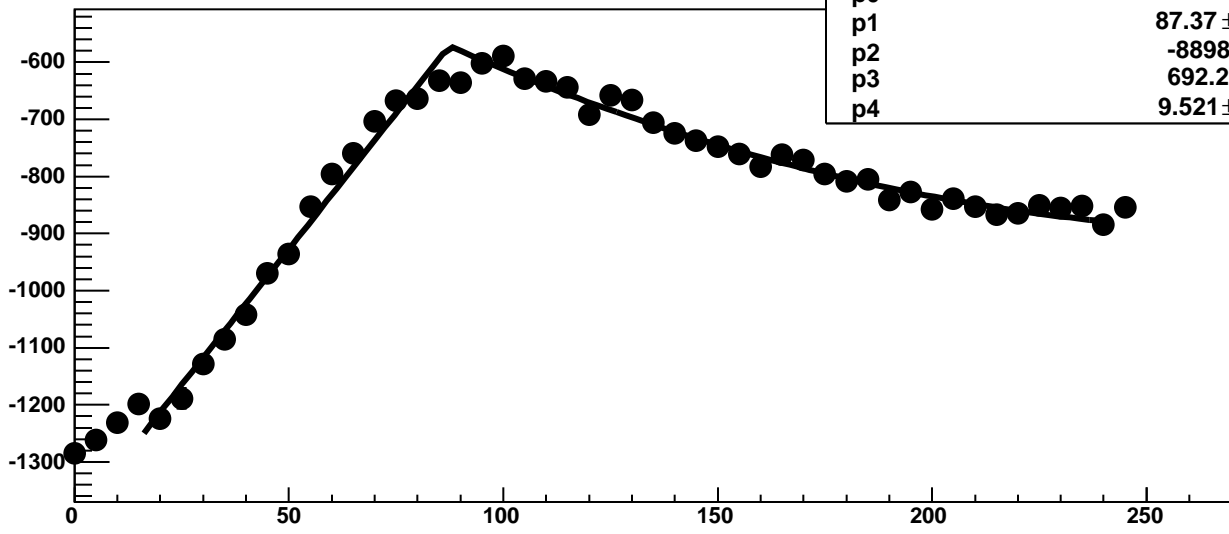
Chip 6, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold

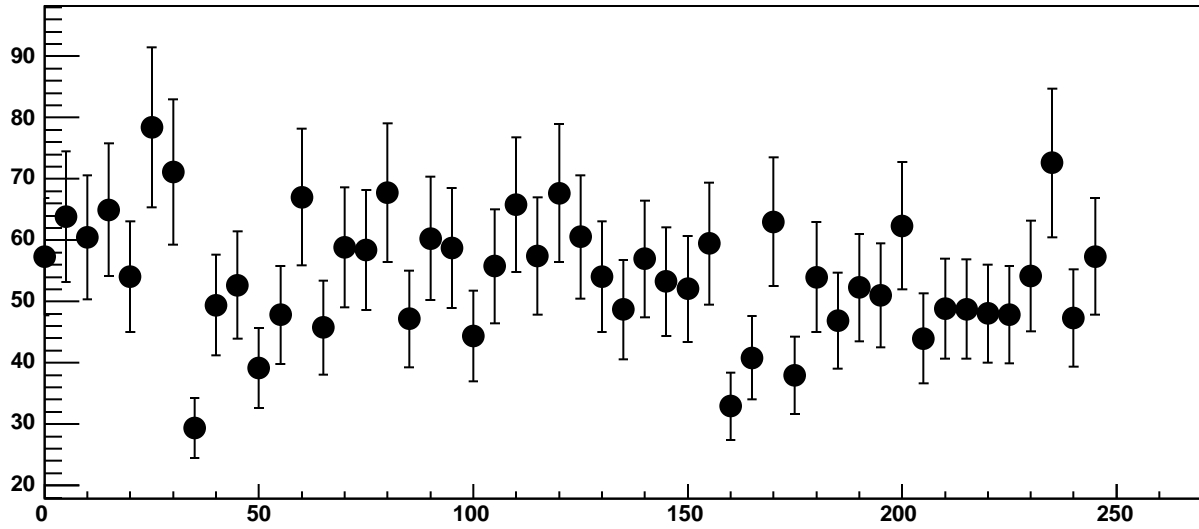


Chip 6, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold

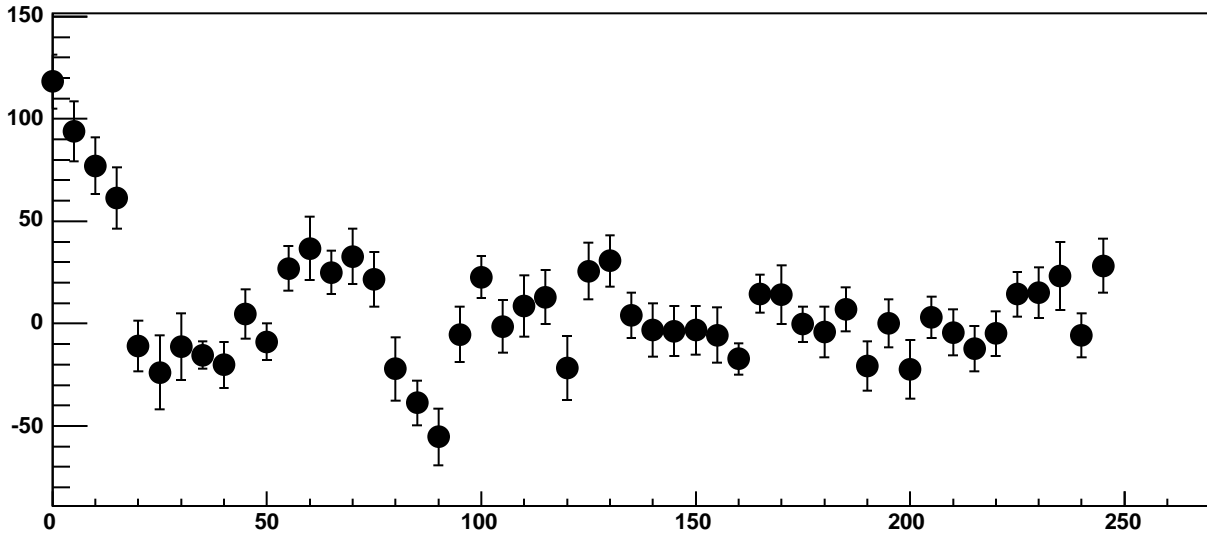


$\chi^2 / \text{ndf}$	126.2 / 41
p0	-571.3 $\pm$ 5.157
p1	87.37 $\pm$ 0.7092
p2	-8898 $\pm$ 1014
p3	692.2 $\pm$ 86.73
p4	9.521 $\pm$ 0.1519

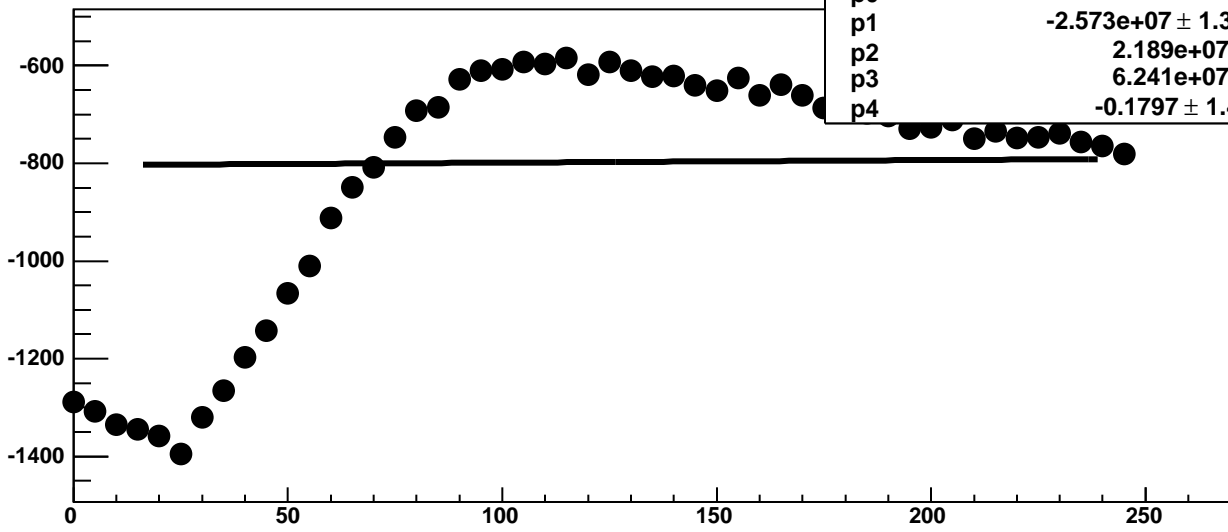
Chip 6, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold

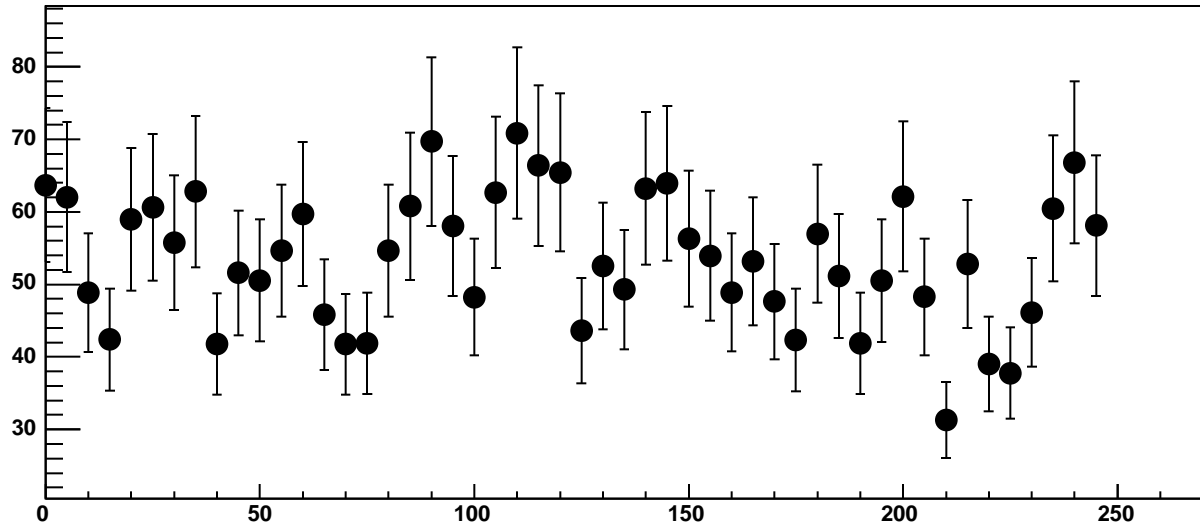


Chip 6, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

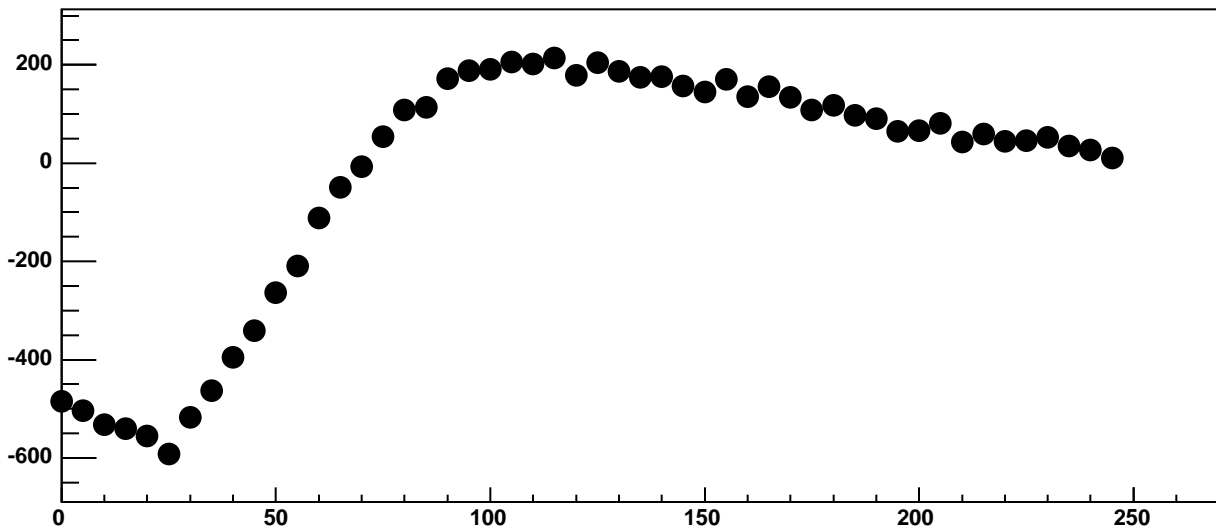


$\chi^2 / \text{ndf}$	1.669e+04 / 41
p0	-2.775e+06 ± 243
p1	-2.573e+07 ± 1.358e+04
p2	2.189e+07 ± 904.2
p3	6.241e+07 ± 3015
p4	-0.1797 ± 1.417e-05

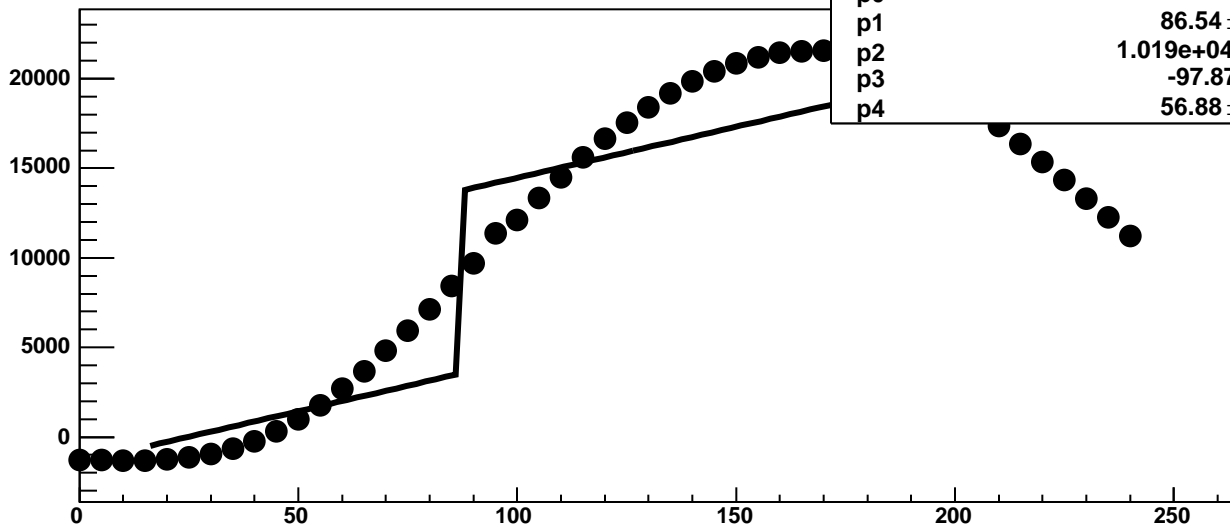
Chip 6, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



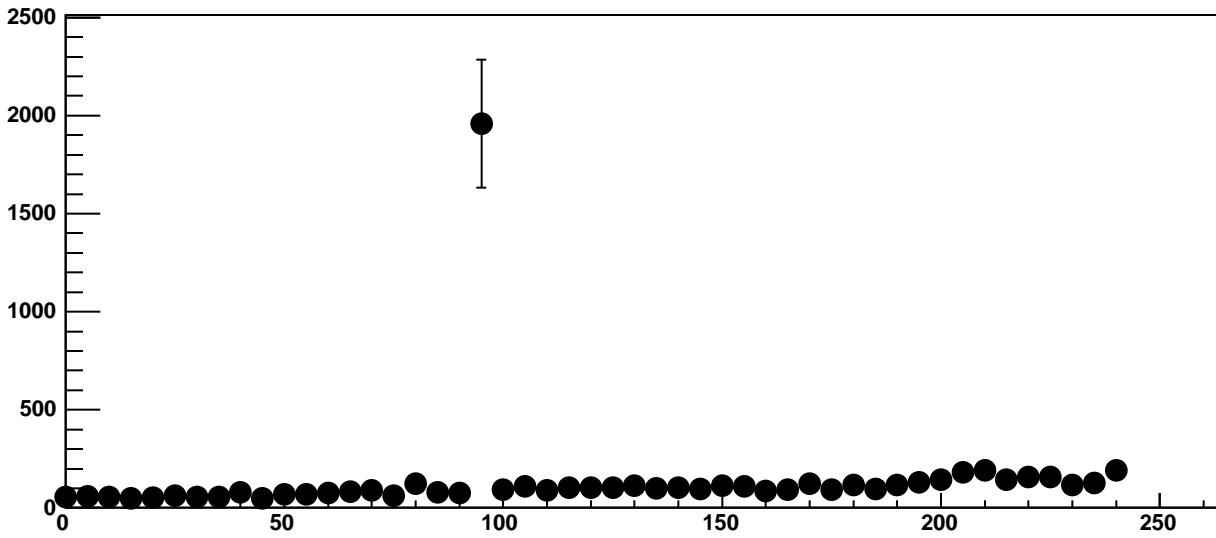
Chip 6, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold



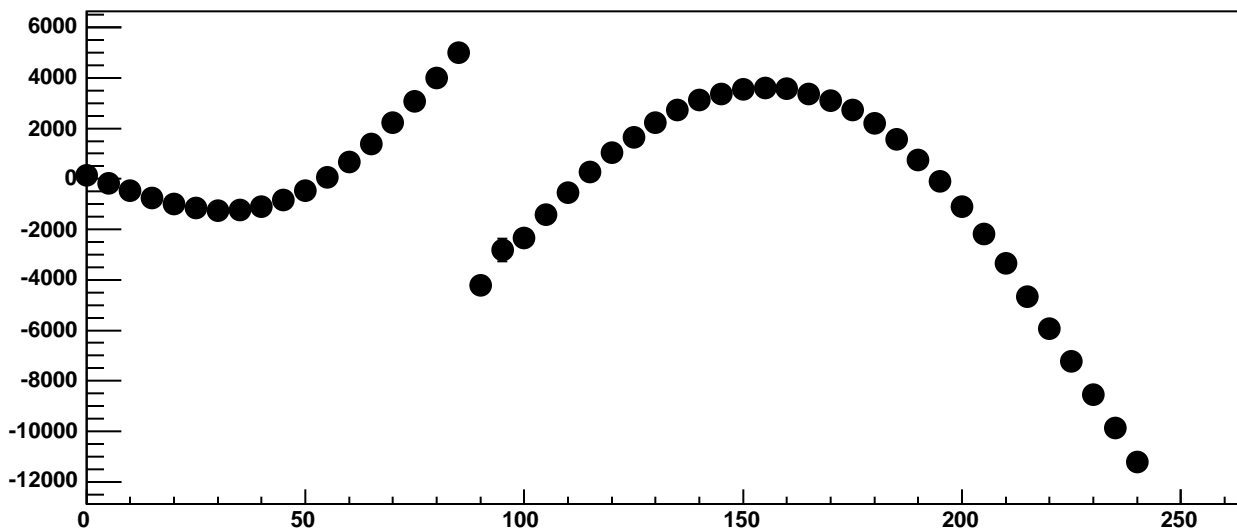
Chip 6, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold



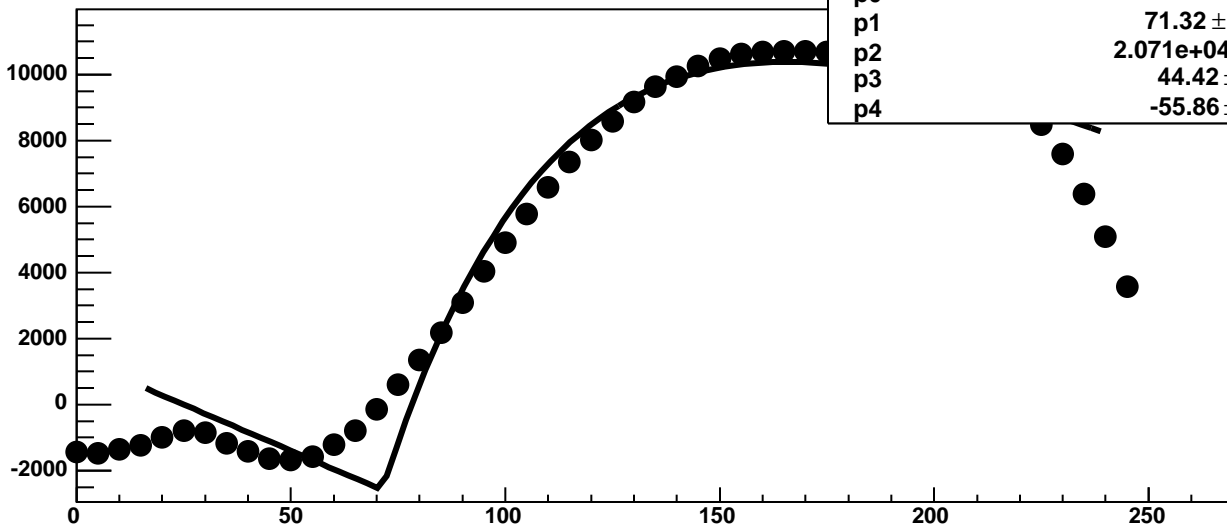
Chip 6, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

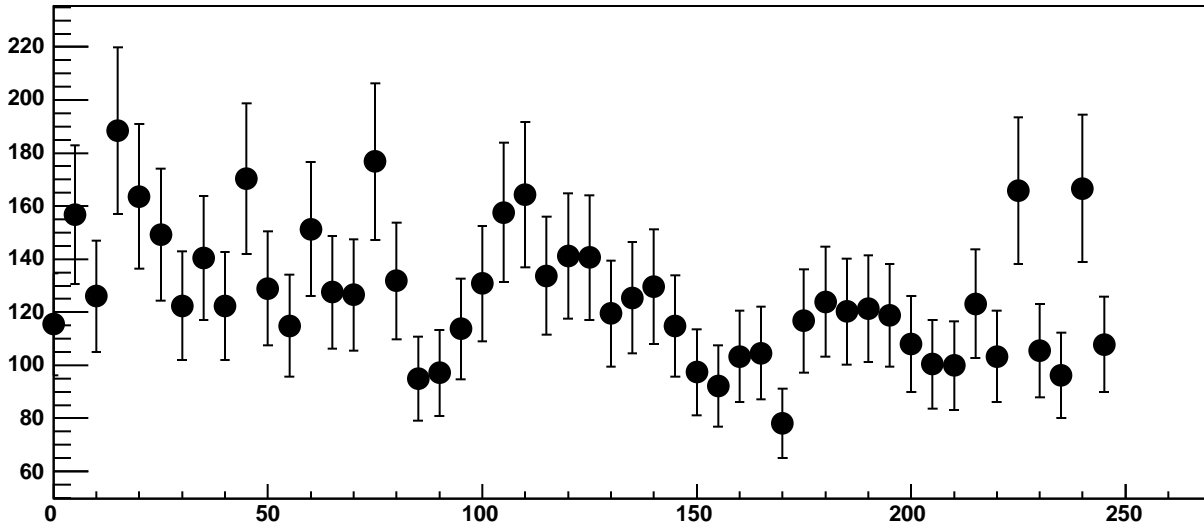


Chip 6, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

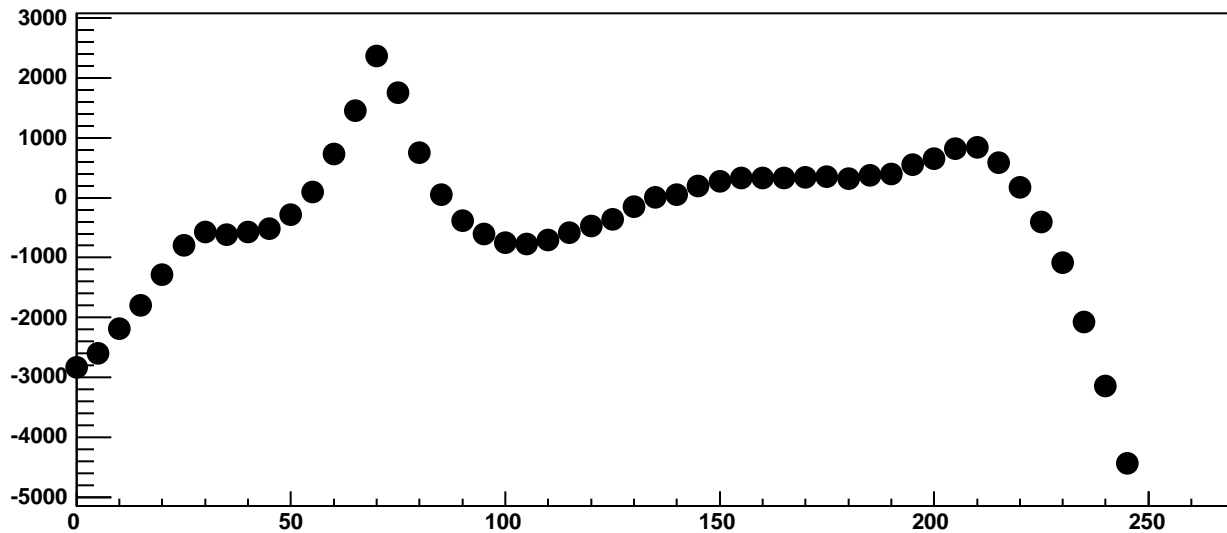


$\chi^2 / \text{ndf}$	4.371e+04 / 41
p0	-2589 ± 11.36
p1	71.32 ± 0.06081
p2	2.071e+04 ± 69.95
p3	44.42 ± 0.1787
p4	-55.86 ± 0.3503

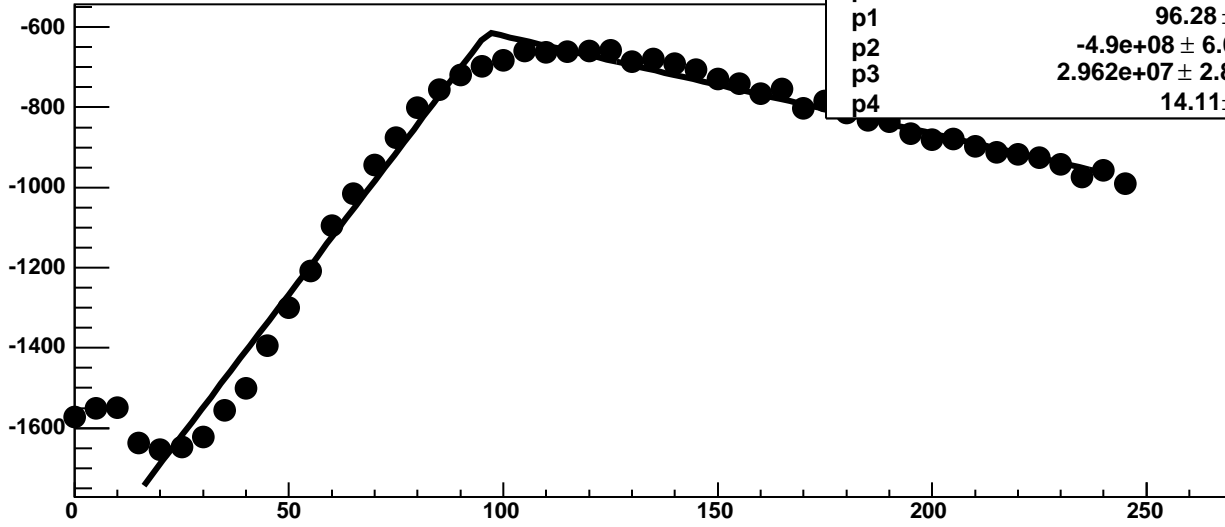
Chip 6, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold

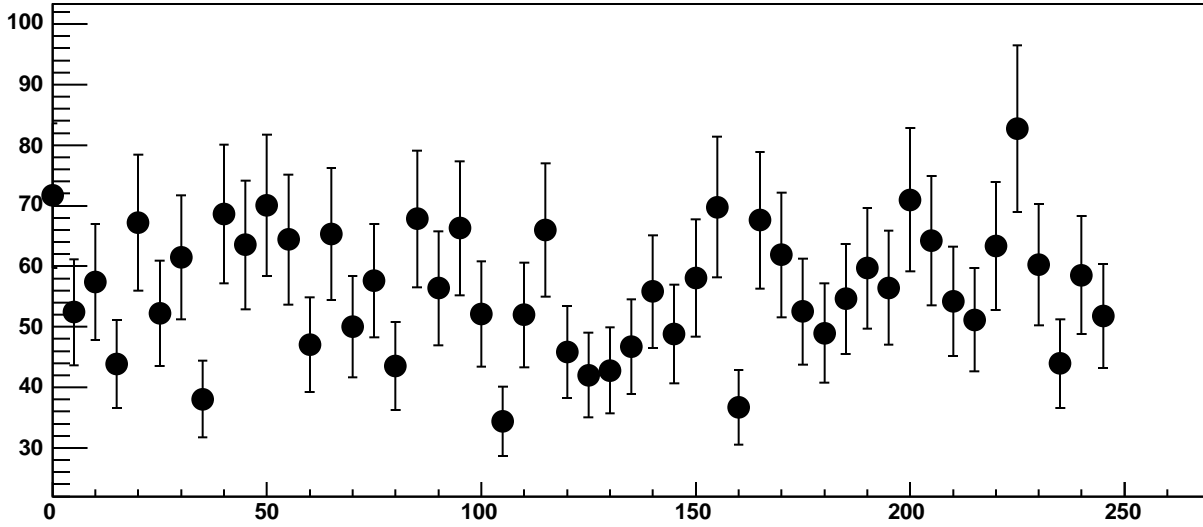


Chip 6, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

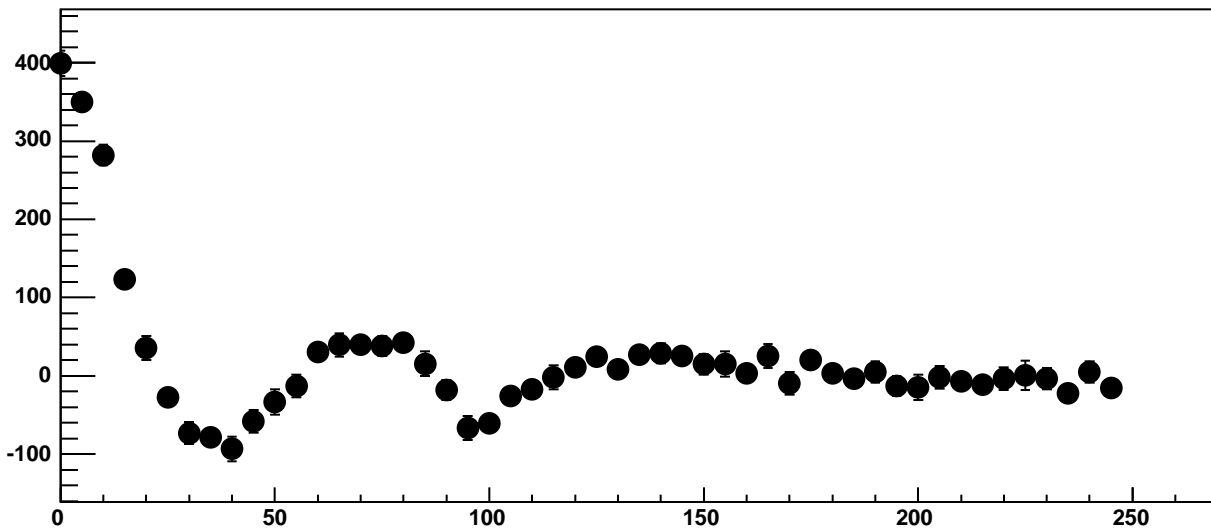


$\chi^2 / \text{ndf}$	480.7 / 41
p0	$-613 \pm 3.615$
p1	$96.28 \pm 0.4453$
p2	$-4.9\text{e}+08 \pm 6.079\text{e}+06$
p3	$2.962\text{e}+07 \pm 2.836\text{e}+05$
p4	$14.11 \pm 0.1232$

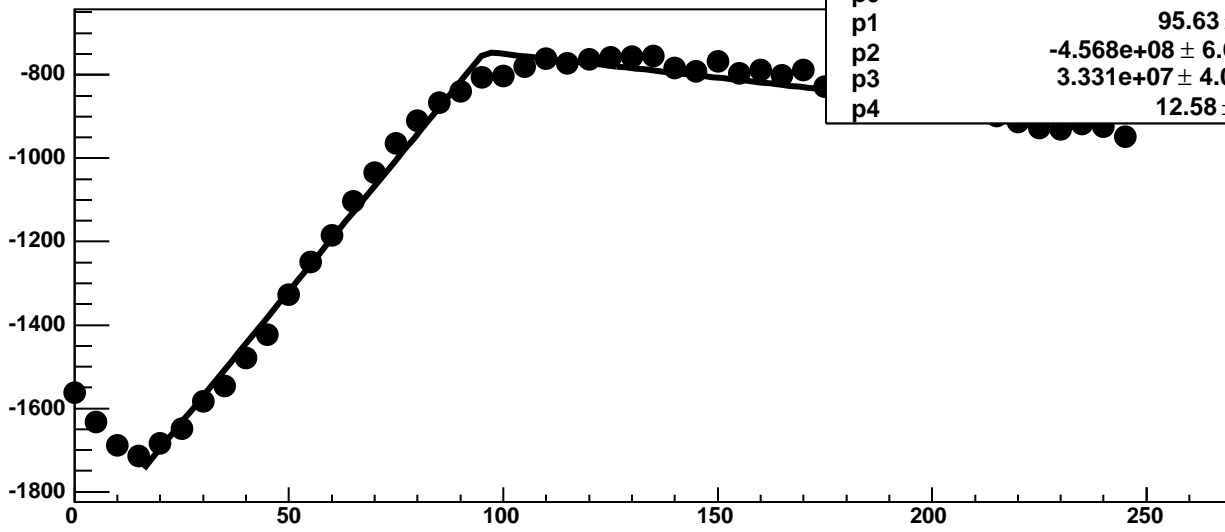
Chip 6, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

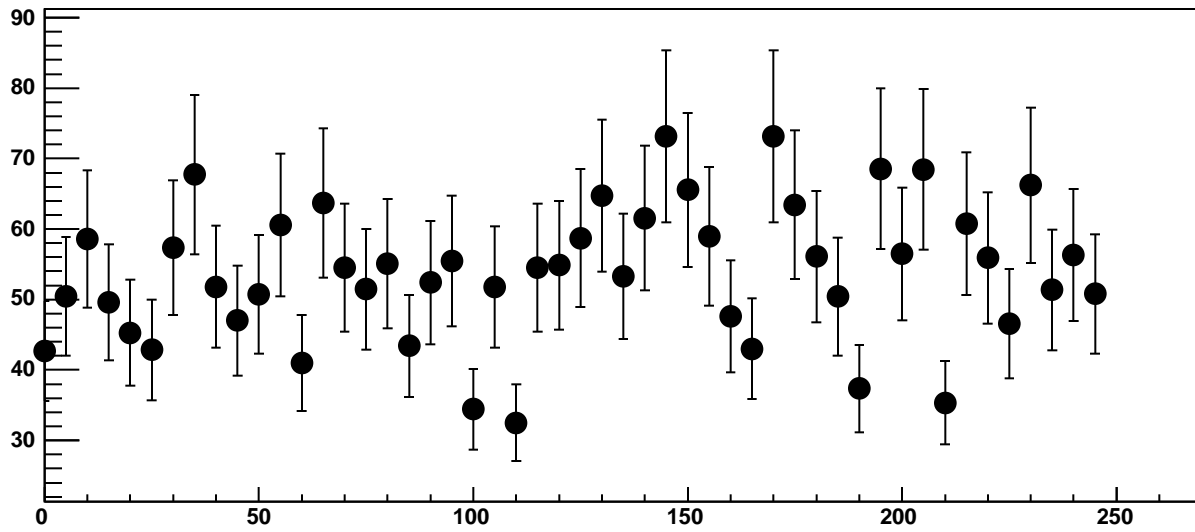


Chip 6, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

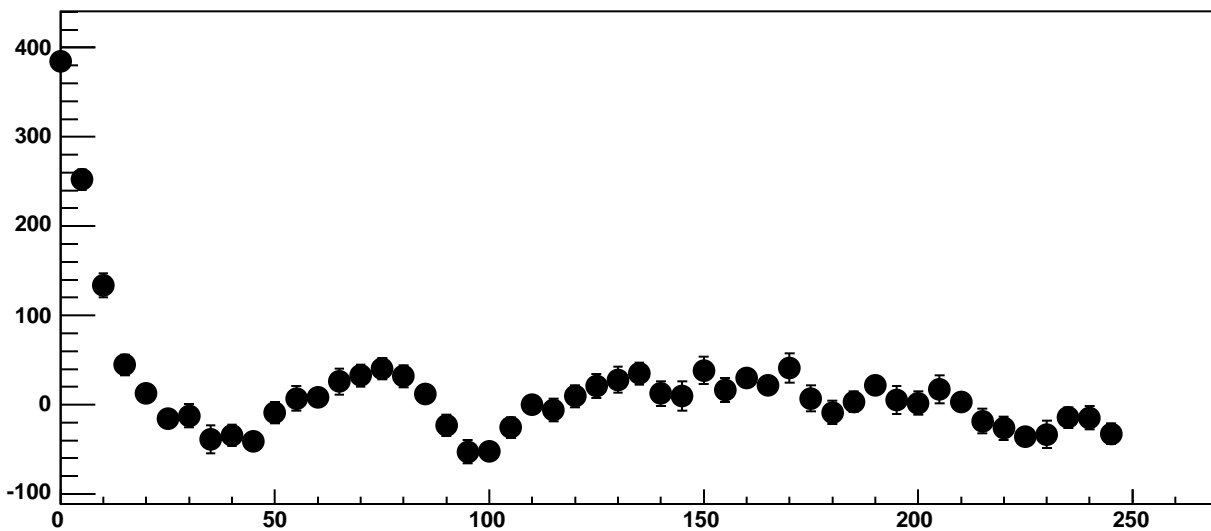


$\chi^2 / \text{ndf}$	225.4 / 41
p0	-744.8 ± 3.765
p1	95.63 ± 0.5001
p2	-4.568e+08 ± 6.641e+06
p3	3.331e+07 ± 4.079e+05
p4	12.58 ± 0.1137

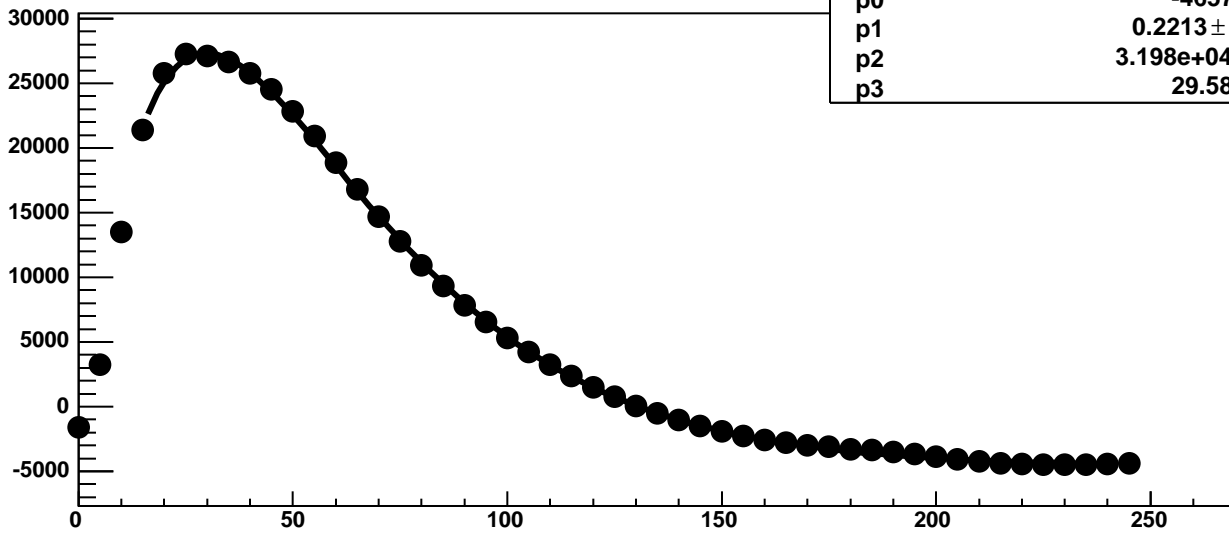
Chip 6, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

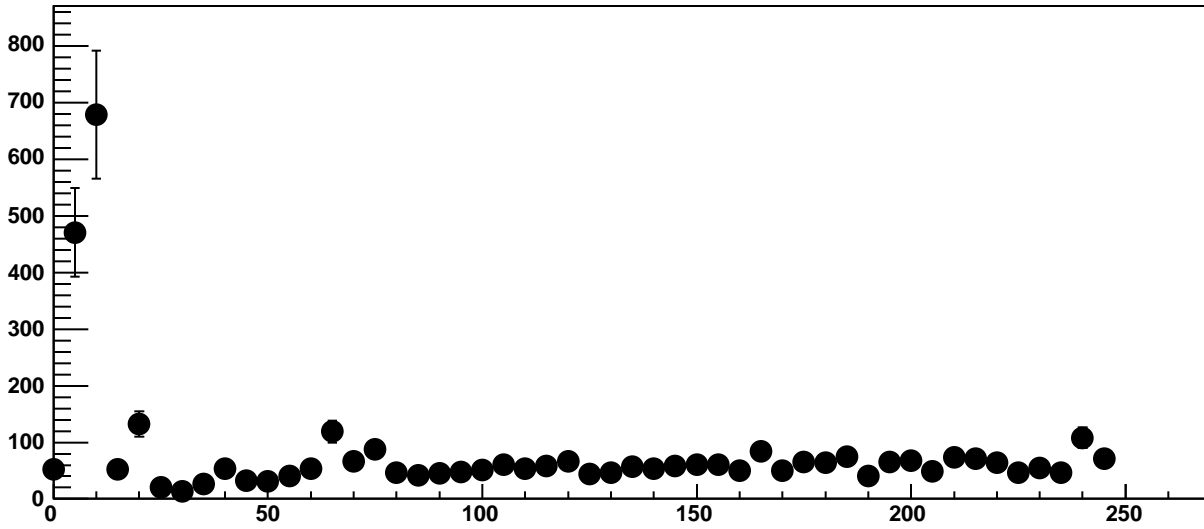


Chip 6, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

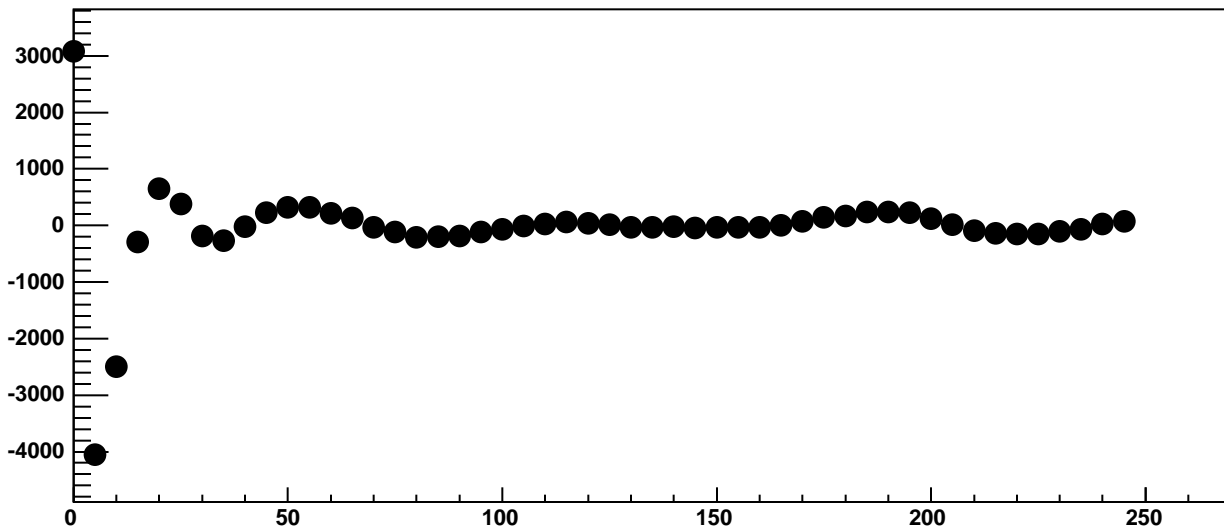


$\chi^2 / \text{ndf}$	2.124e+04 / 42
p0	-4657 ± 3.693
p1	0.2213 ± 0.01439
p2	3.198e+04 ± 3.997
p3	29.58 ± 0.009

Chip 6, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

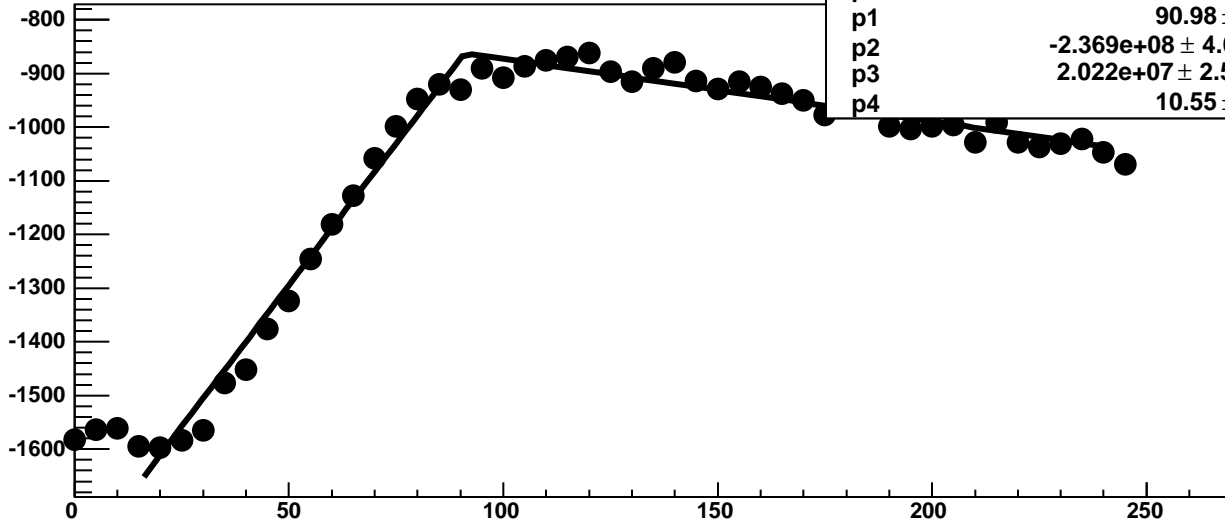


Chip 6, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold



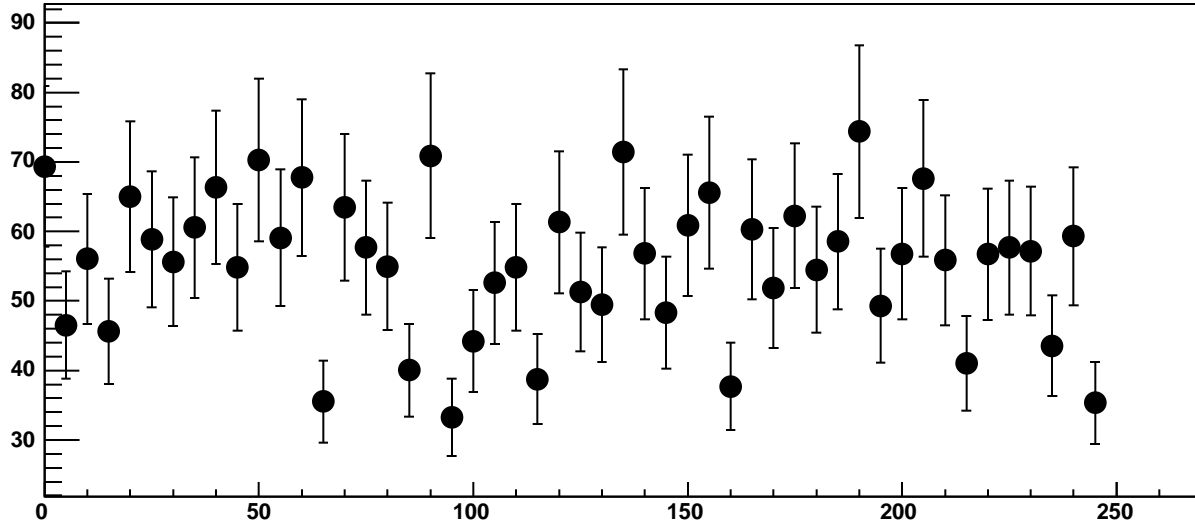


Chip 6, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

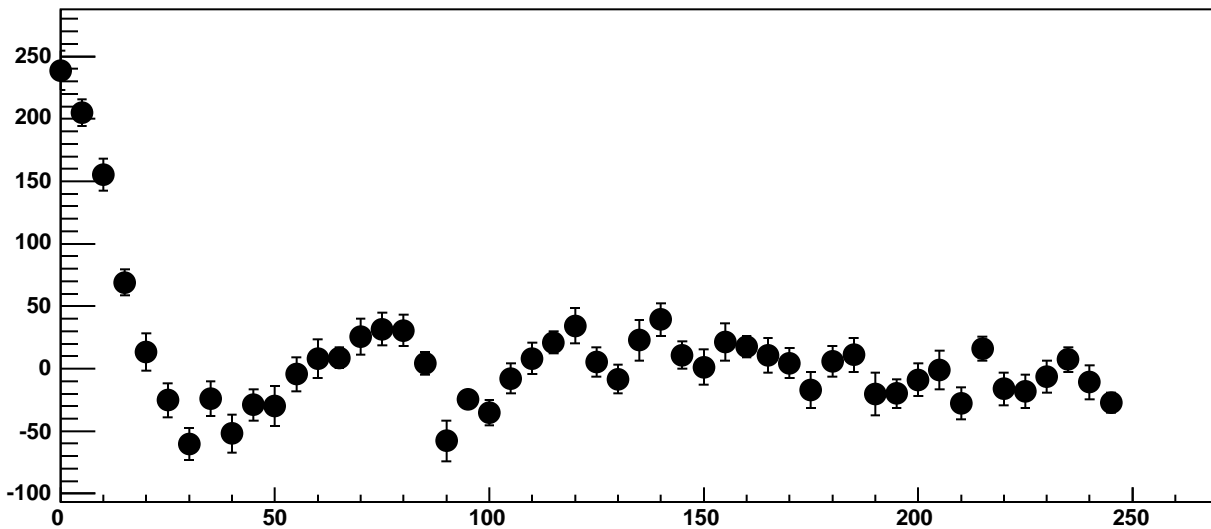


$\chi^2 / \text{ndf}$	196.5 / 41
p0	$-861.8 \pm 3.613$
p1	$90.98 \pm 0.6009$
p2	$-2.369\text{e}+08 \pm 4.035\text{e}+06$
p3	$2.022\text{e}+07 \pm 2.561\text{e}+05$
p4	$10.55 \pm 0.1327$

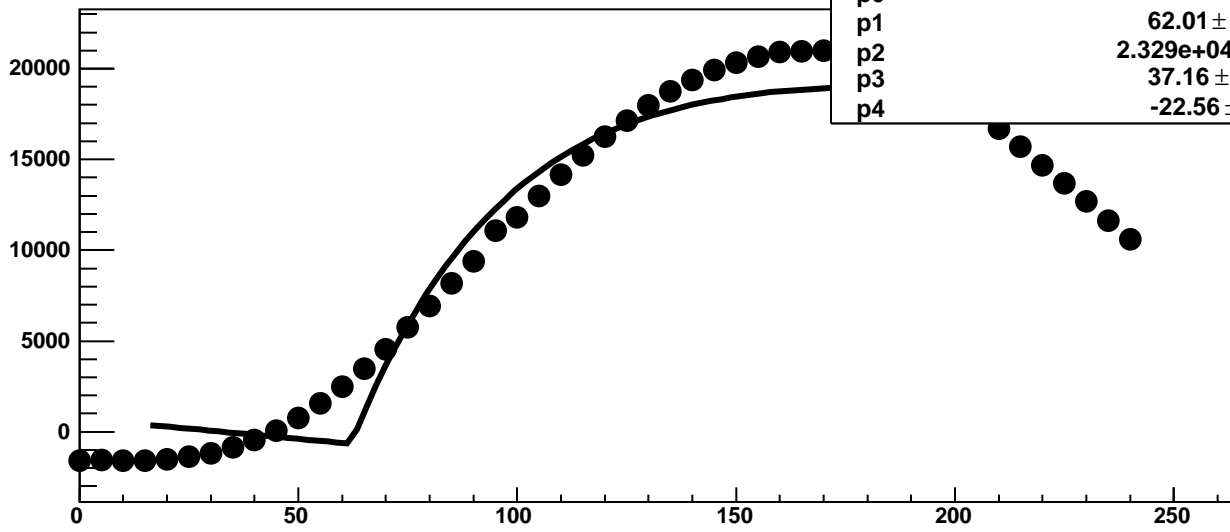
Chip 6, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

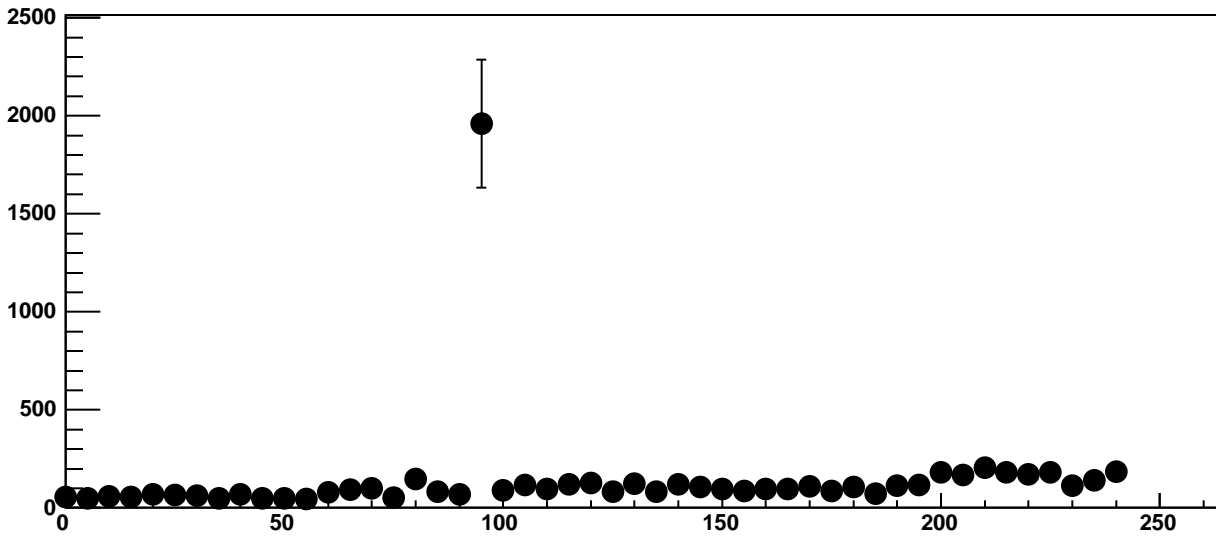


Chip 6, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

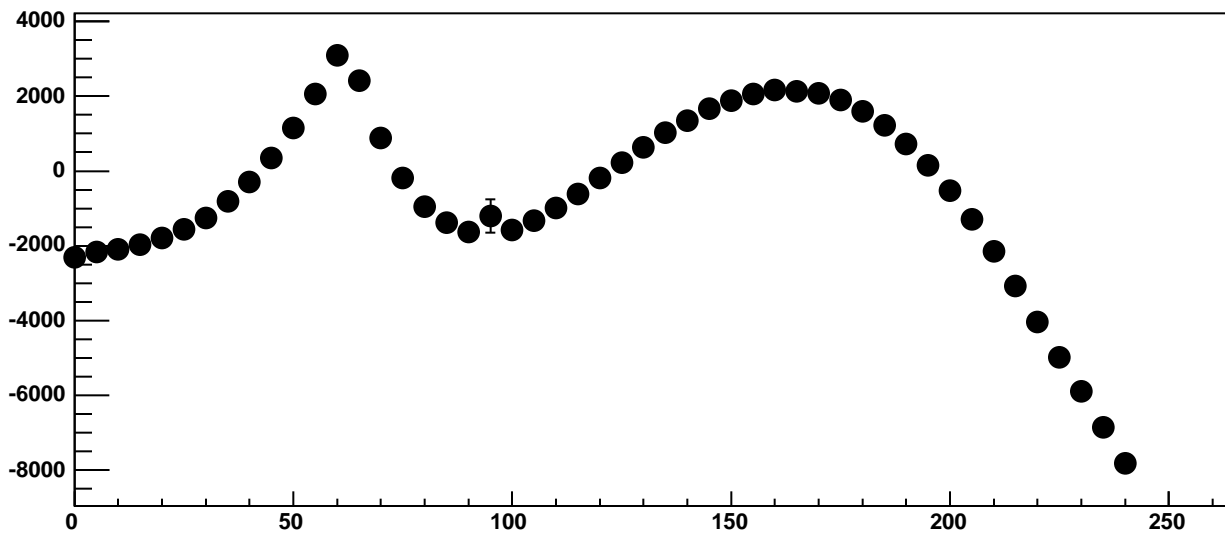


$\chi^2 / \text{ndf}$	4.166e+05 / 41
p0	-660.2 ± 6.003
p1	62.01 ± 0.02589
p2	2.329e+04 ± 33.78
p3	37.16 ± 0.06741
p4	-22.56 ± 0.1964

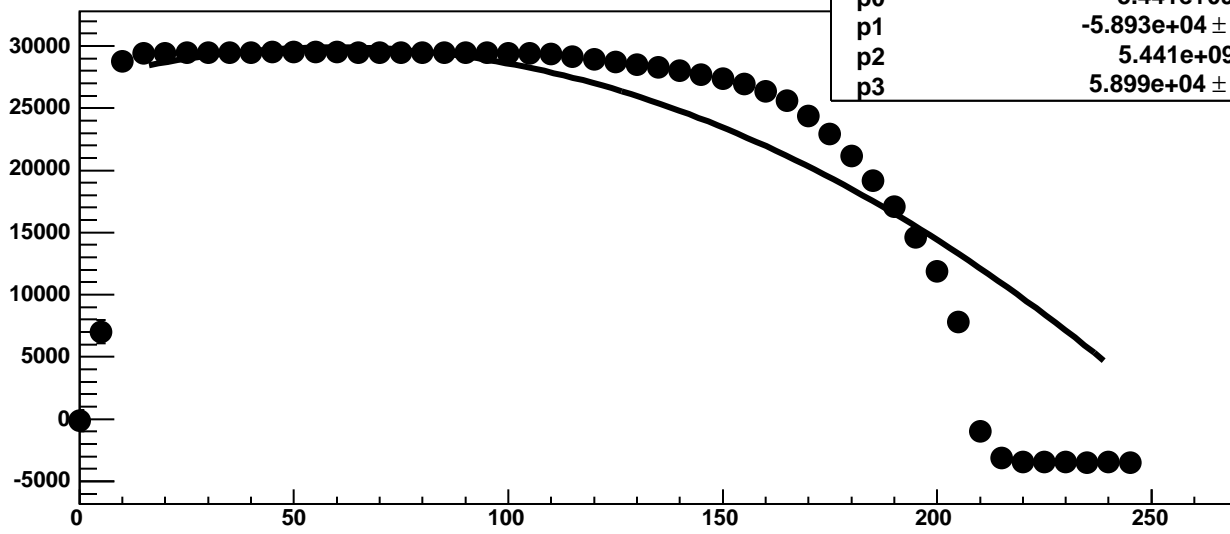
Chip 6, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



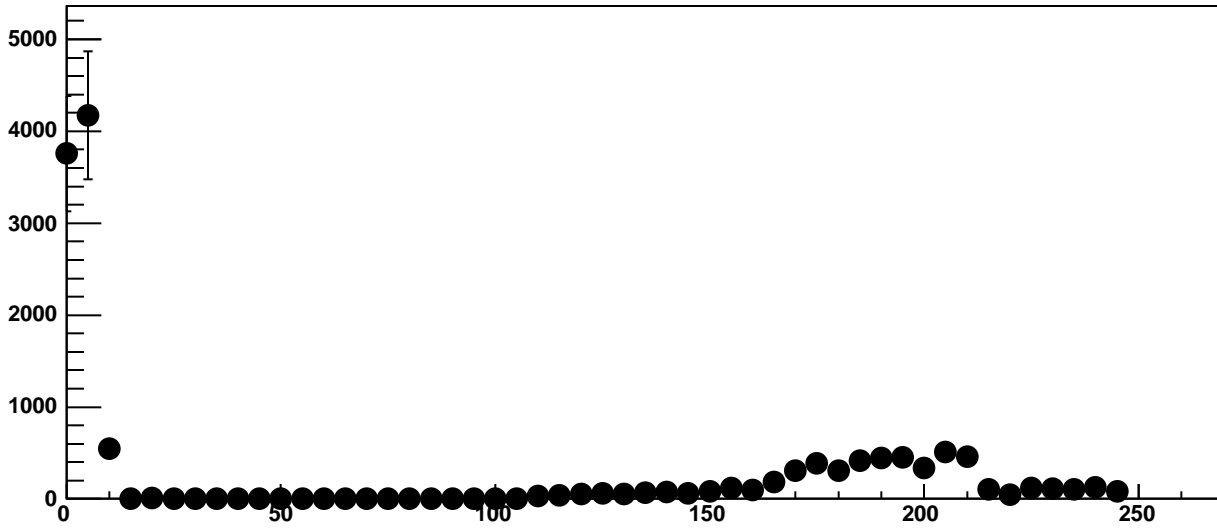
Chip 6, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold



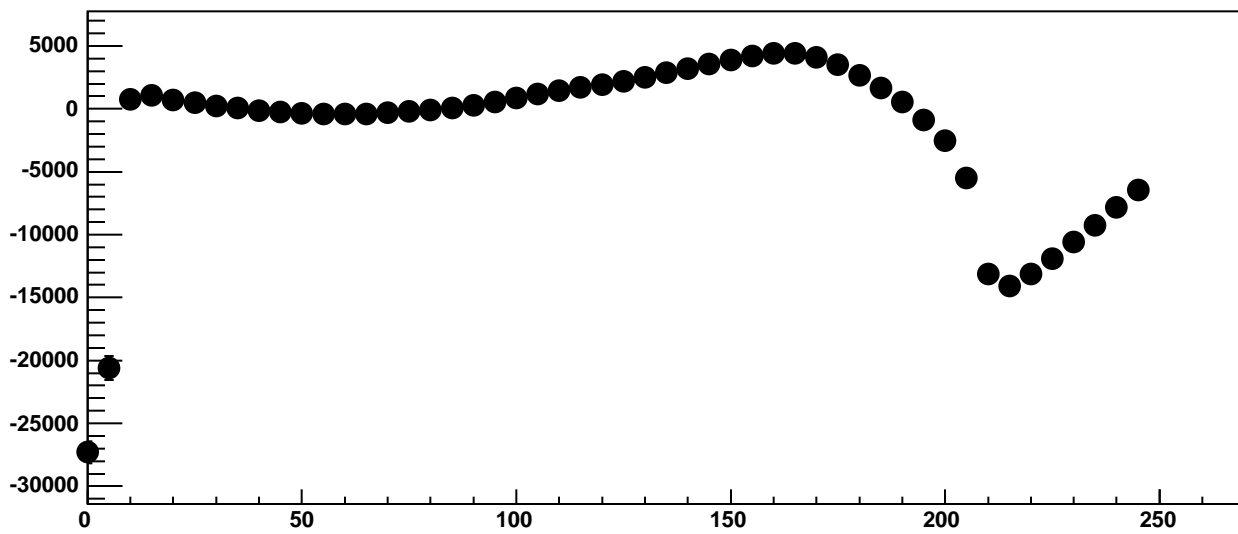
Chip 6, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold



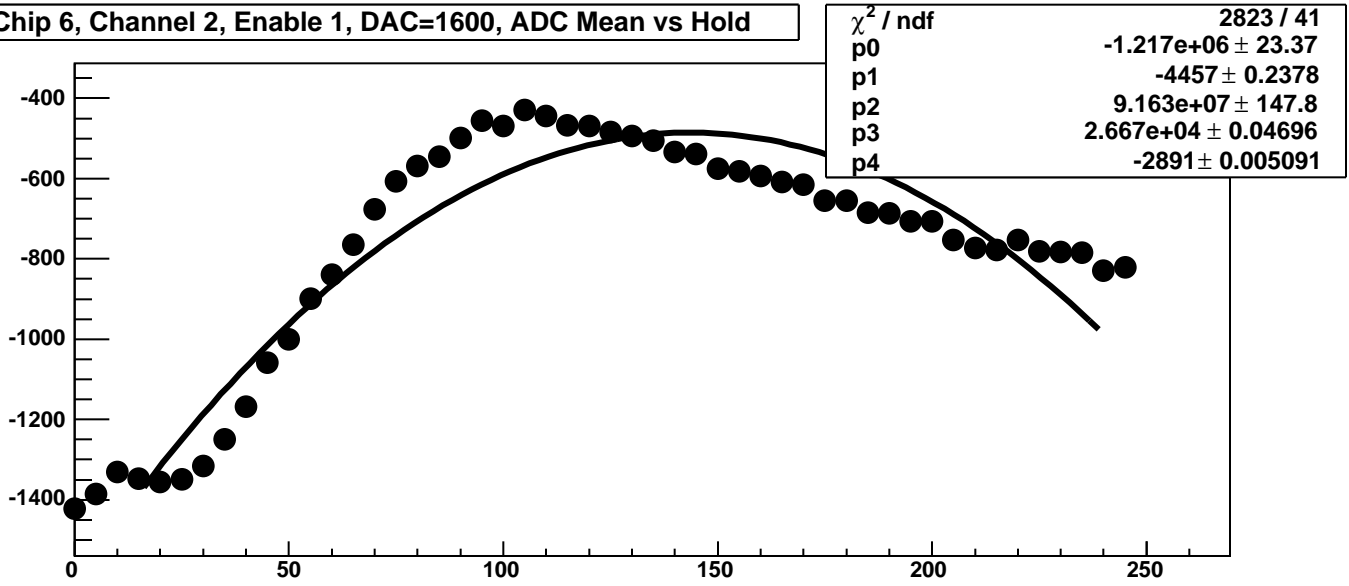
Chip 6, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



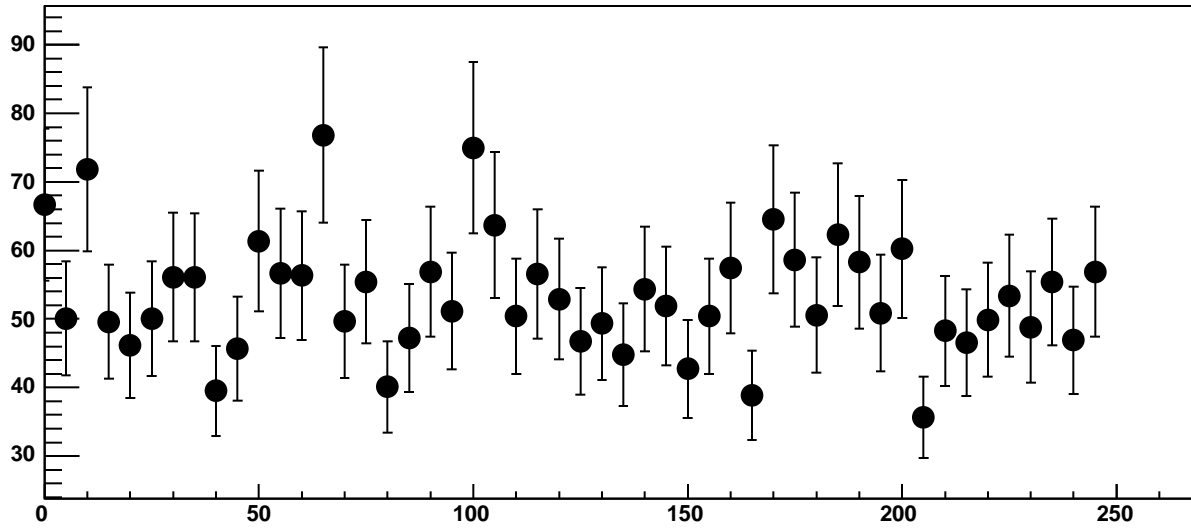
Chip 6, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold



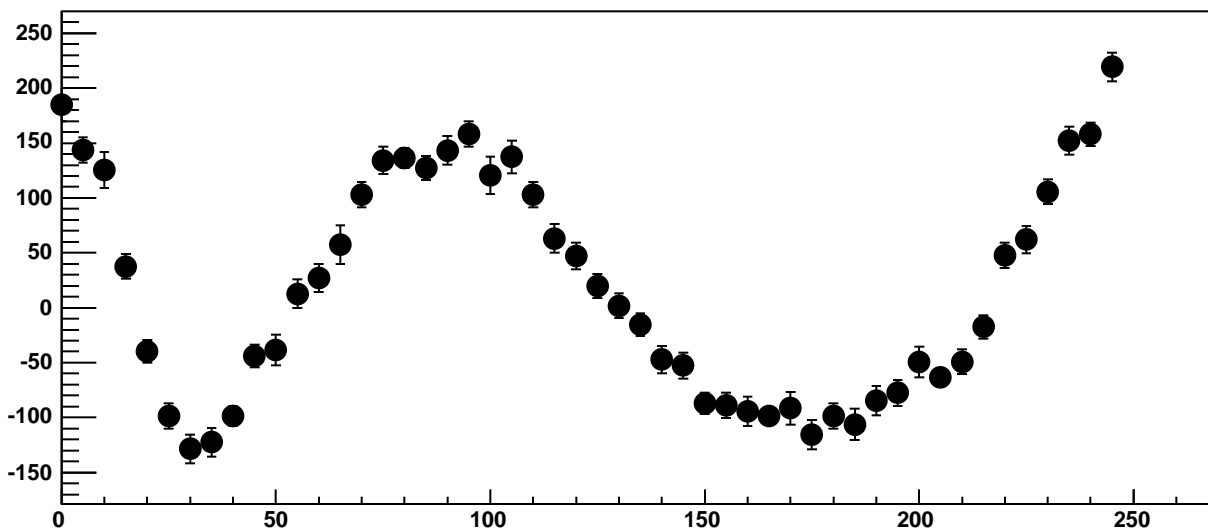
Chip 6, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold



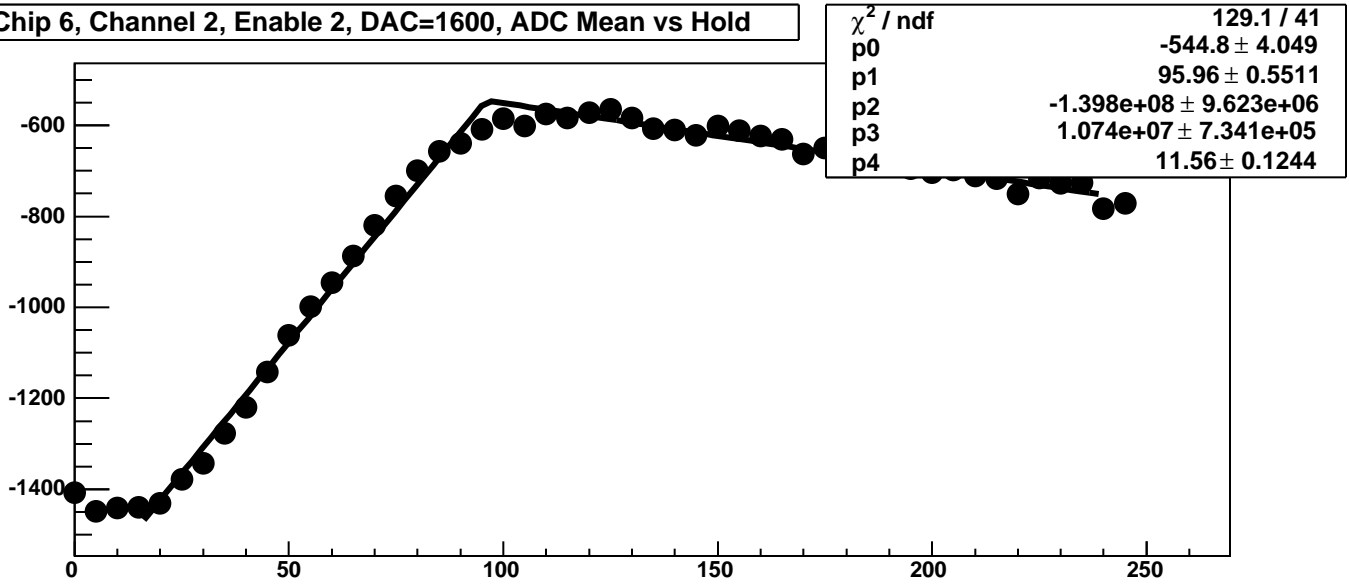
Chip 6, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



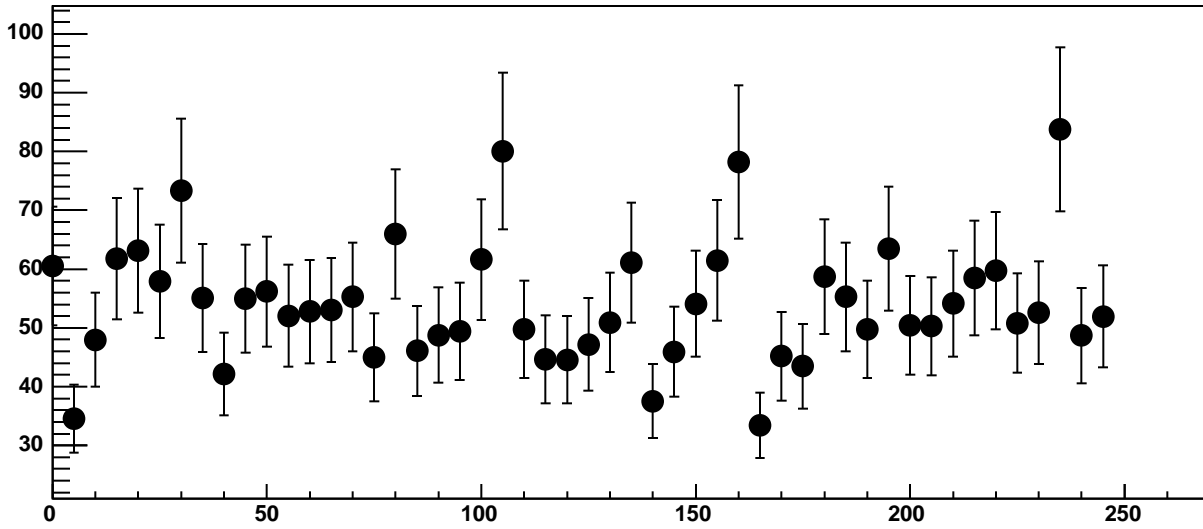
Chip 6, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



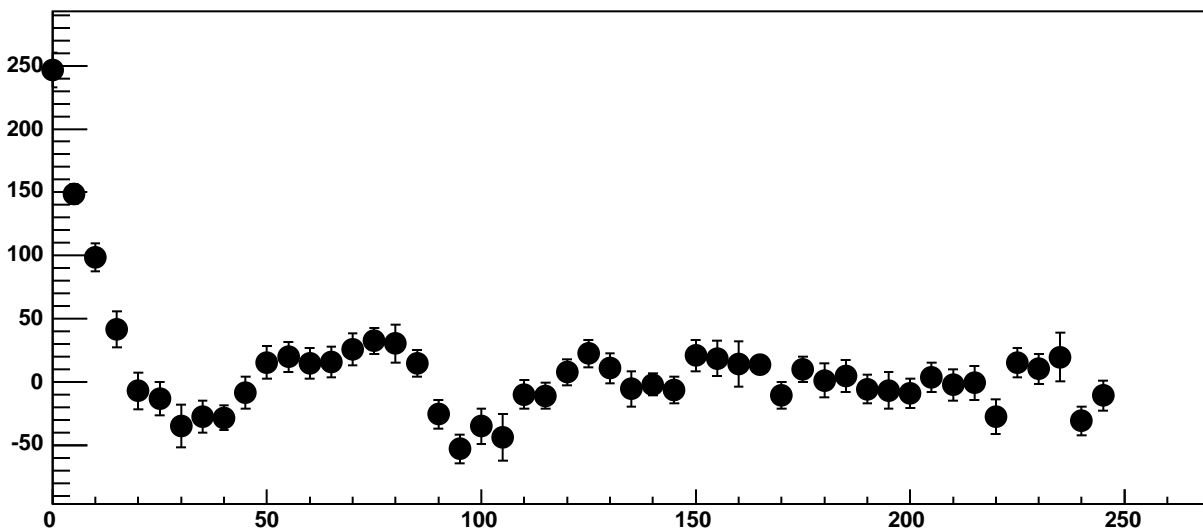
Chip 6, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold



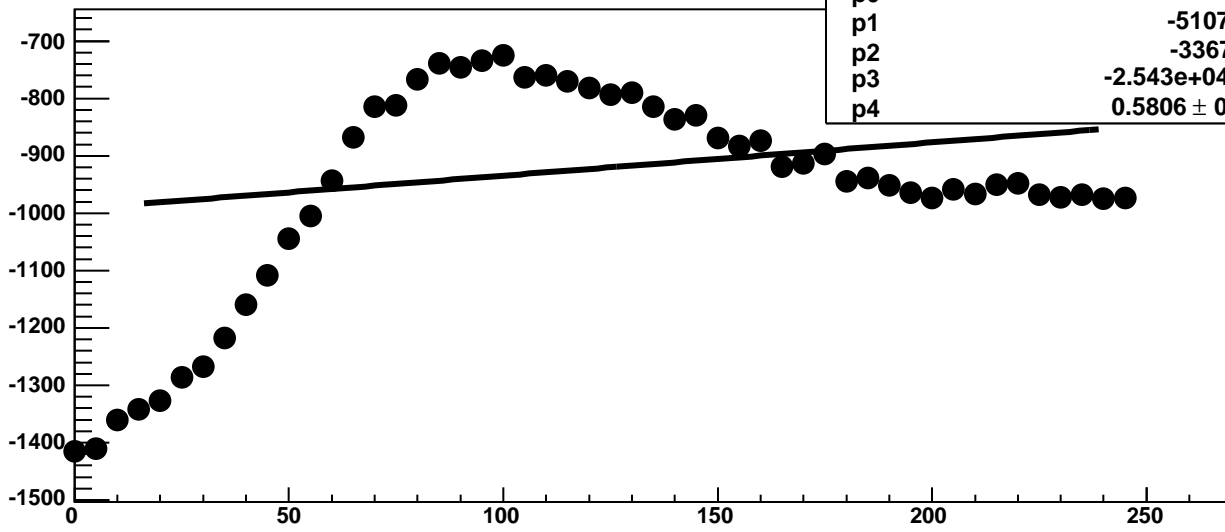
Chip 6, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

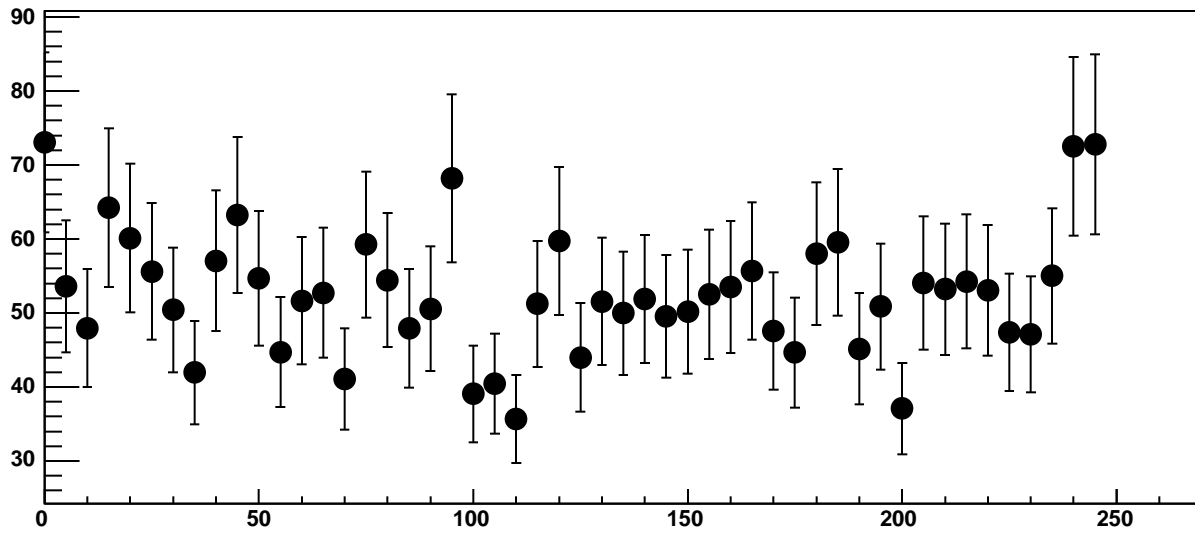


Chip 6, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

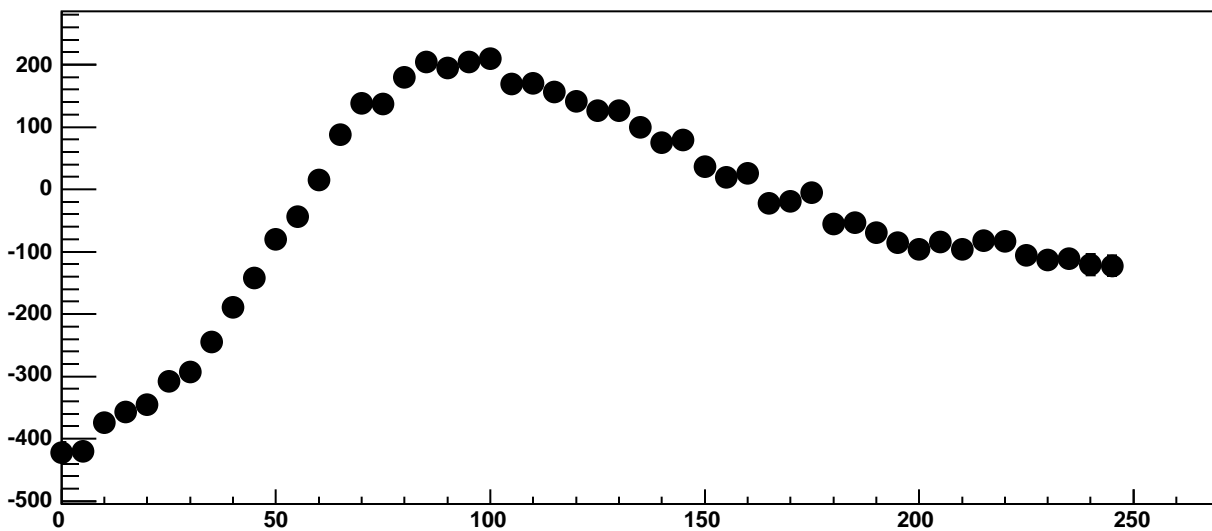


$\chi^2 / \text{ndf}$	7666 / 41
p0	$-591.3 \pm 8.255$
p1	$-5107 \pm 13.37$
p2	$-3367 \pm 11.06$
p3	$-2.543e+04 \pm 1666$
p4	$0.5806 \pm 0.001576$

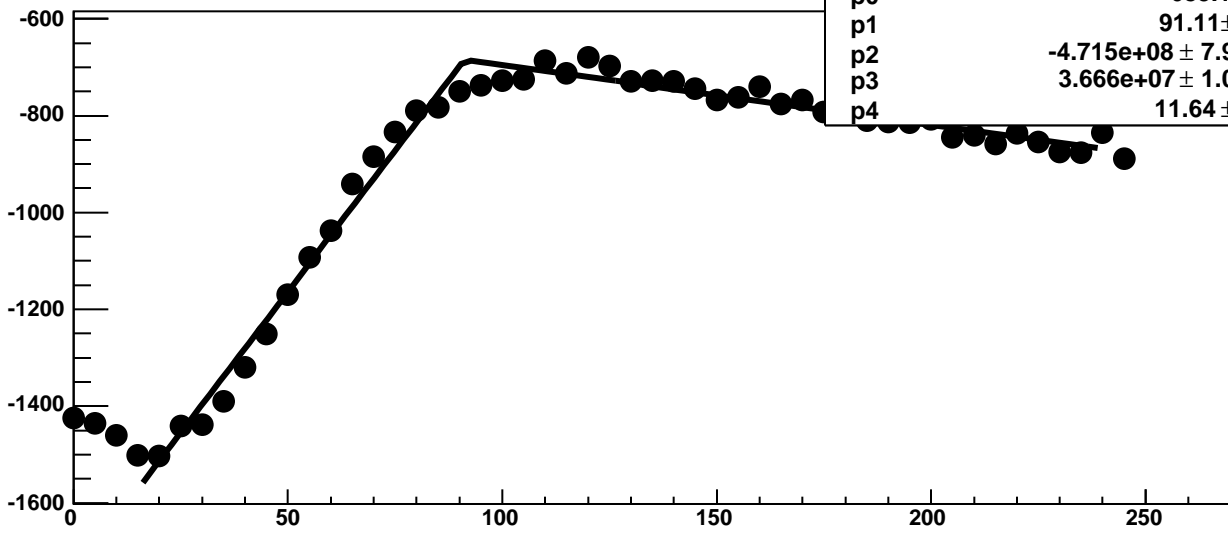
Chip 6, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold

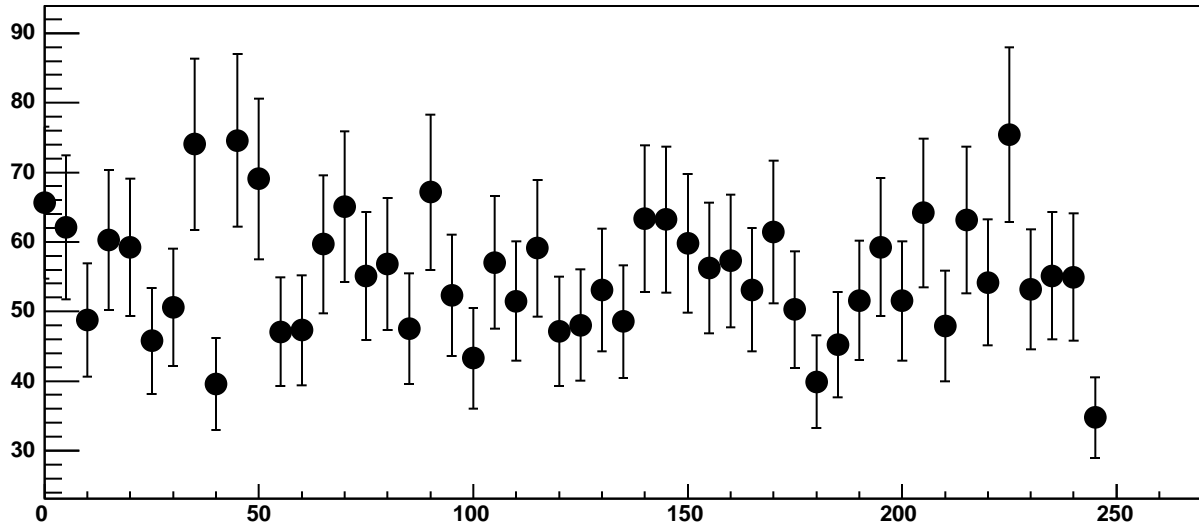


Chip 6, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

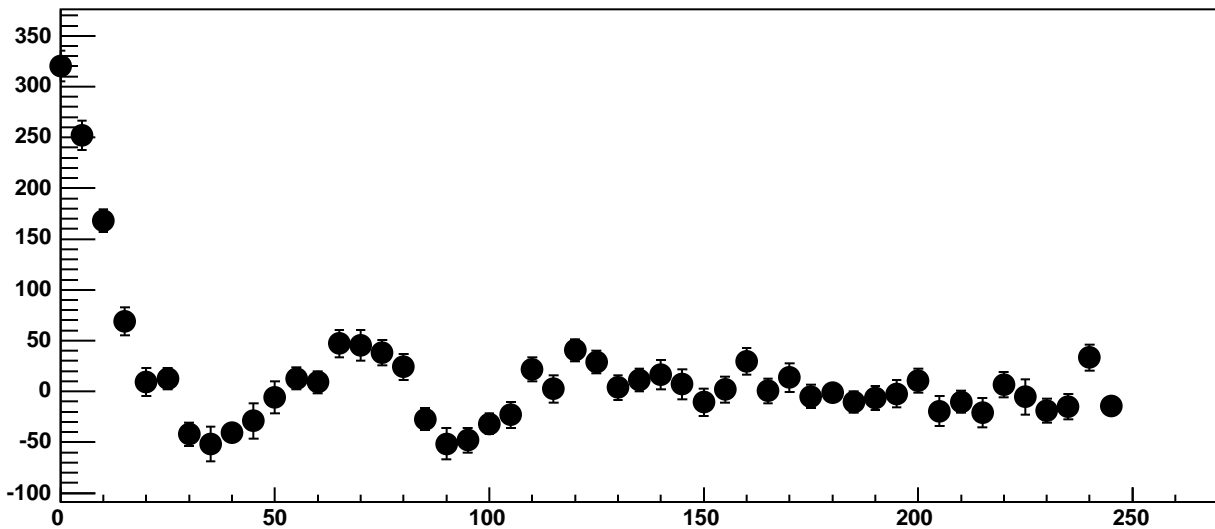


$\chi^2 / \text{ndf}$	206.7 / 41
p0	-685.1 ± 4.826
p1	91.11 ± 0.4133
p2	-4.715e+08 ± 7.967e+06
p3	3.666e+07 ± 1.085e+06
p4	11.64 ± 0.1352

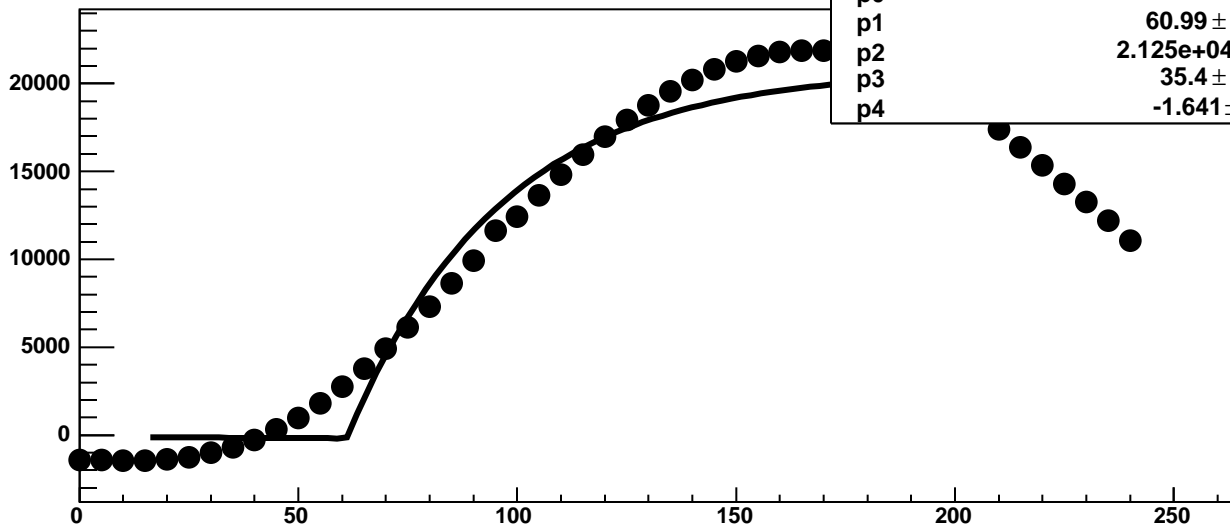
Chip 6, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



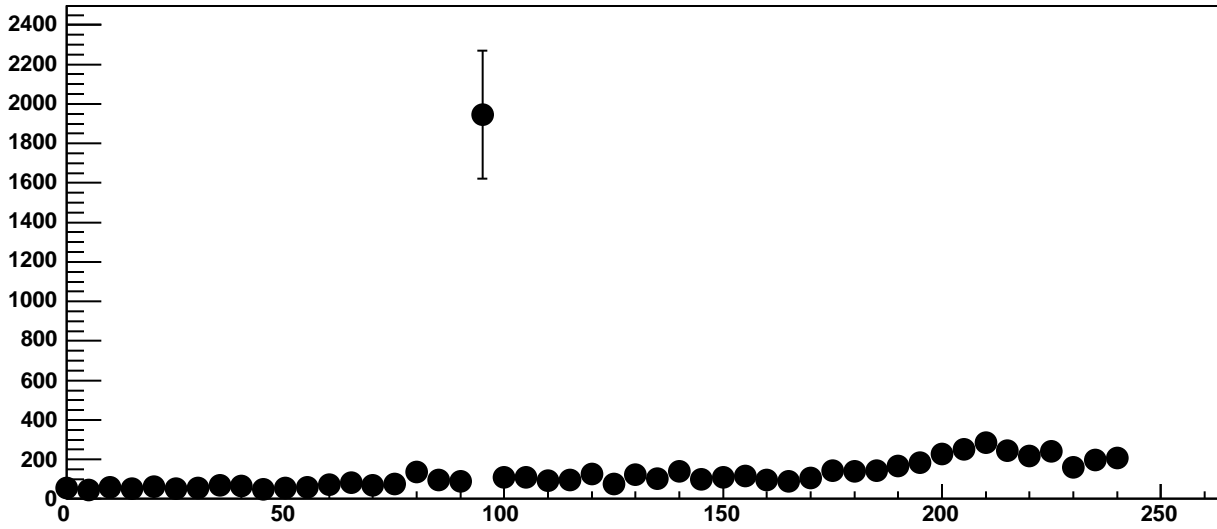
Chip 6, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold



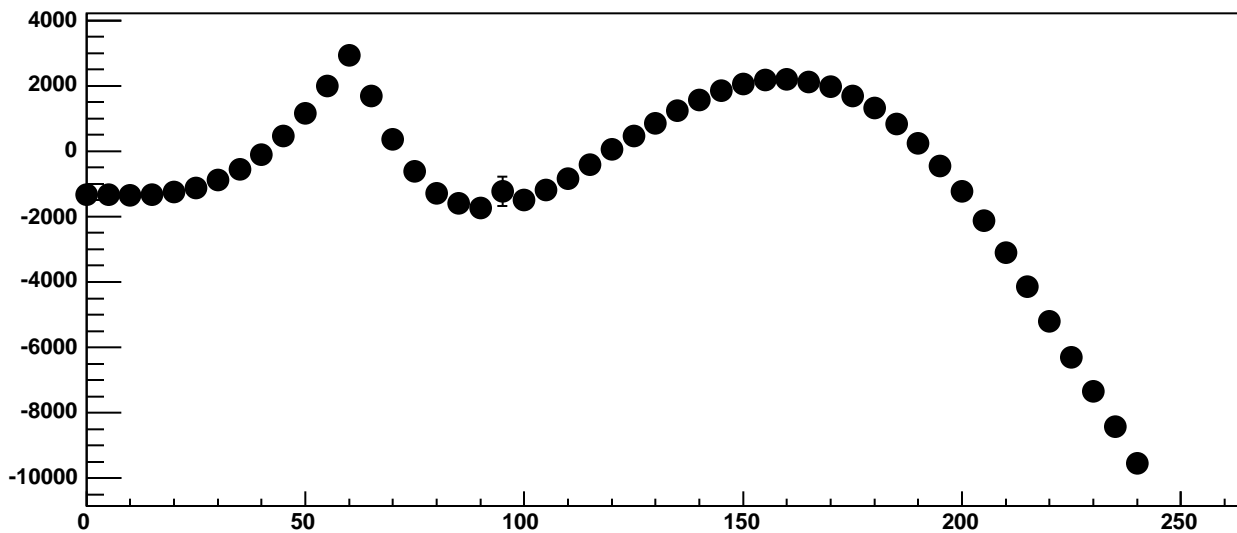
Chip 6, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 6, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

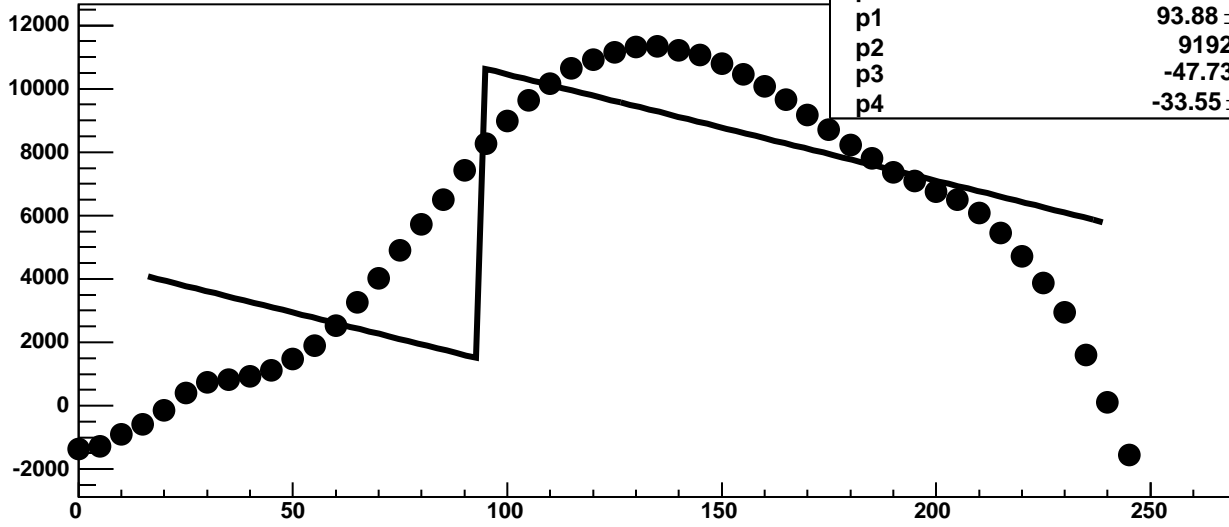


Chip 6, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

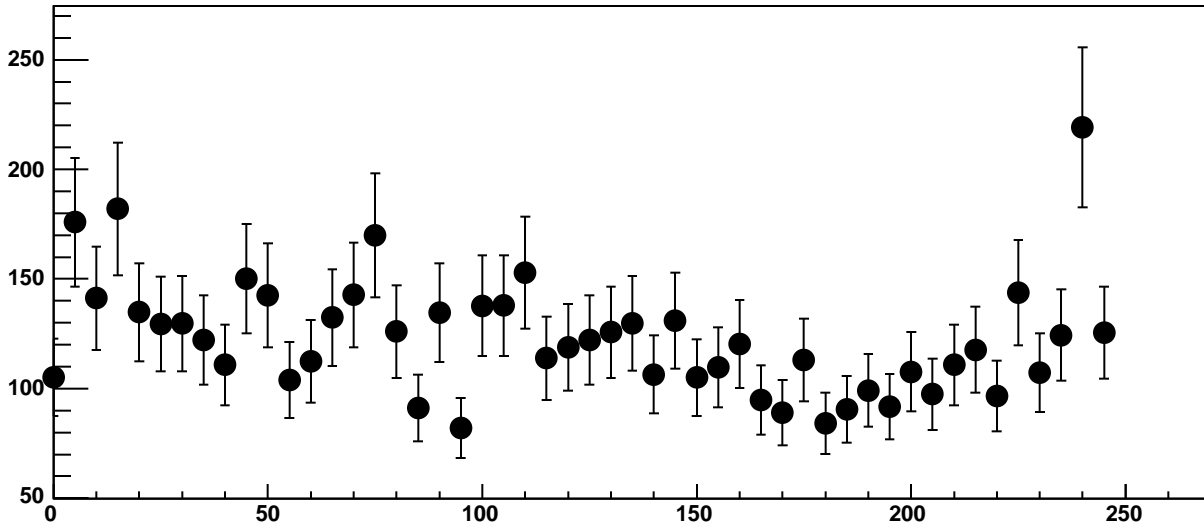




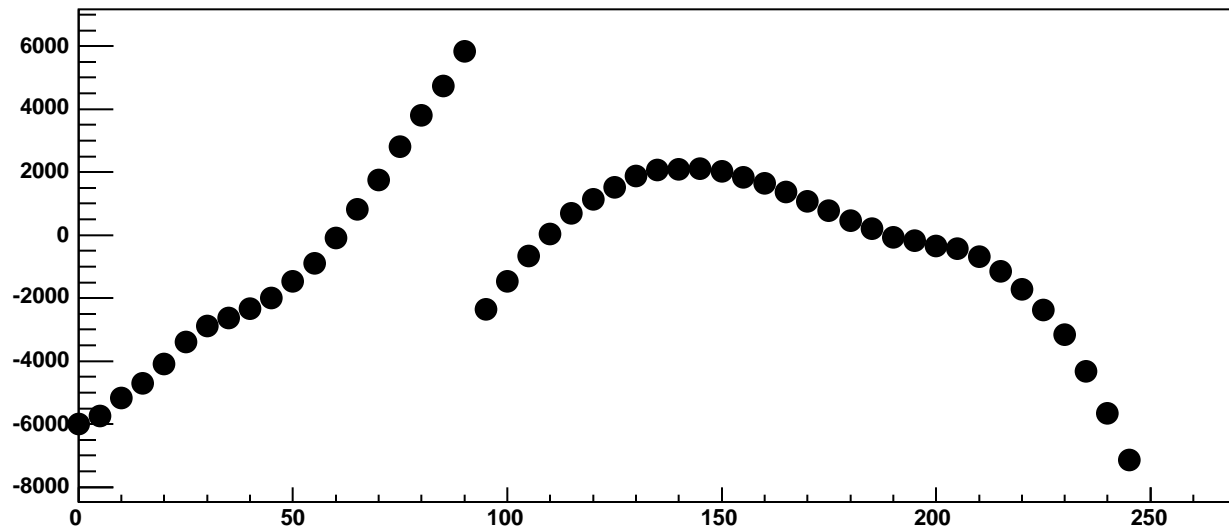
Chip 6, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold



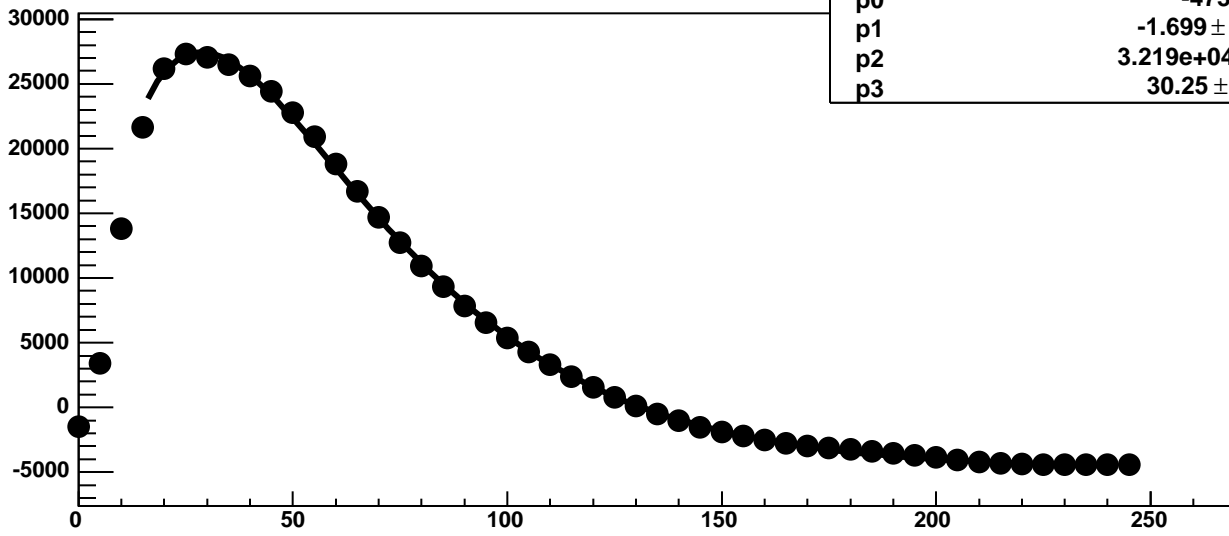
Chip 6, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

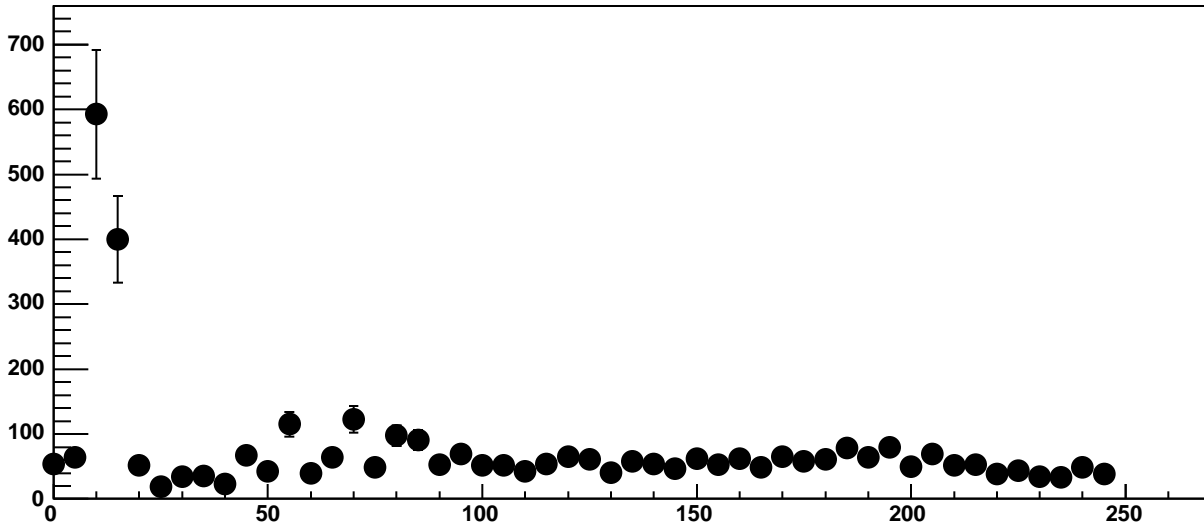


Chip 6, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold

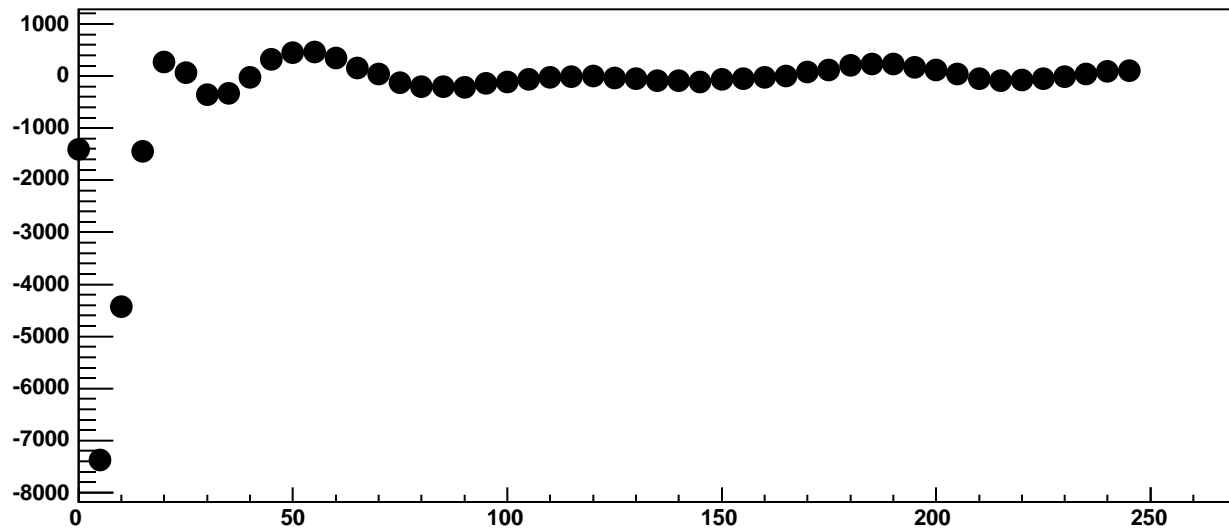


$\chi^2 / \text{ndf}$	1.151e+04 / 42
p0	-4731 ± 3.38
p1	-1.699 ± 0.02132
p2	3.219e+04 ± 4.117
p3	30.25 ± 0.01128

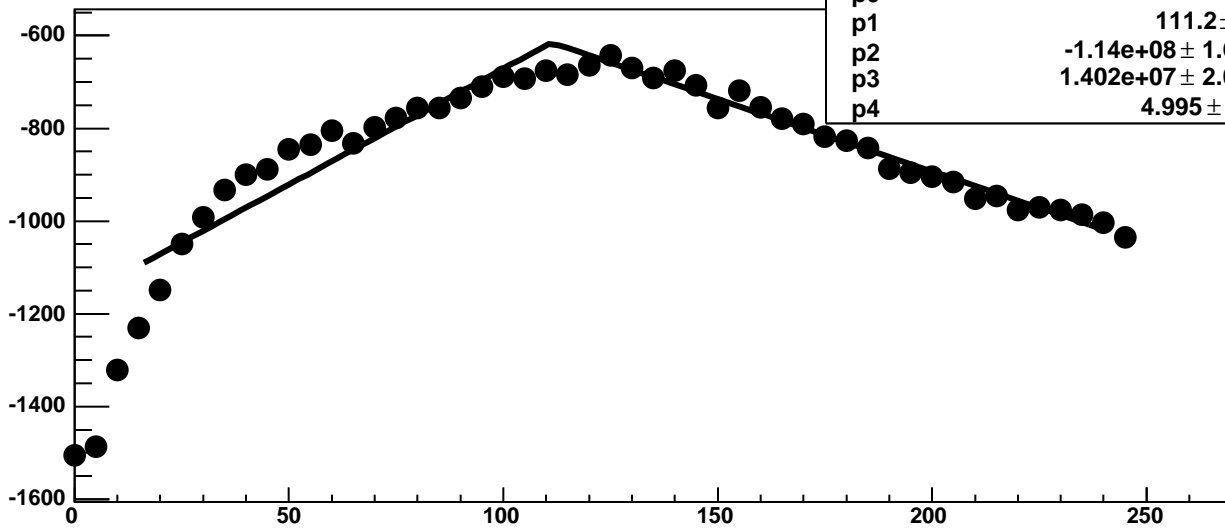
Chip 6, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold

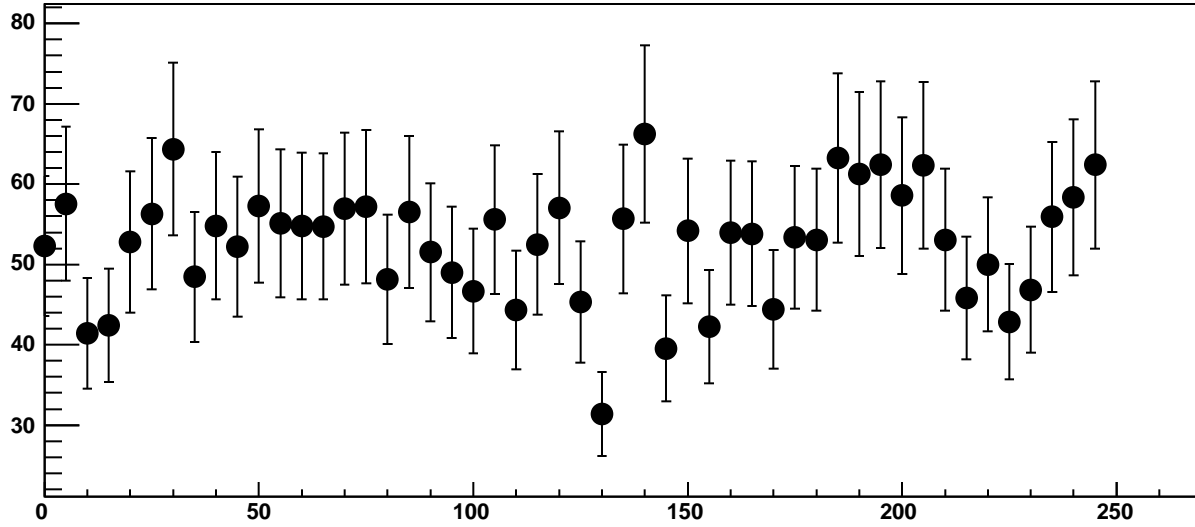


Chip 6, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

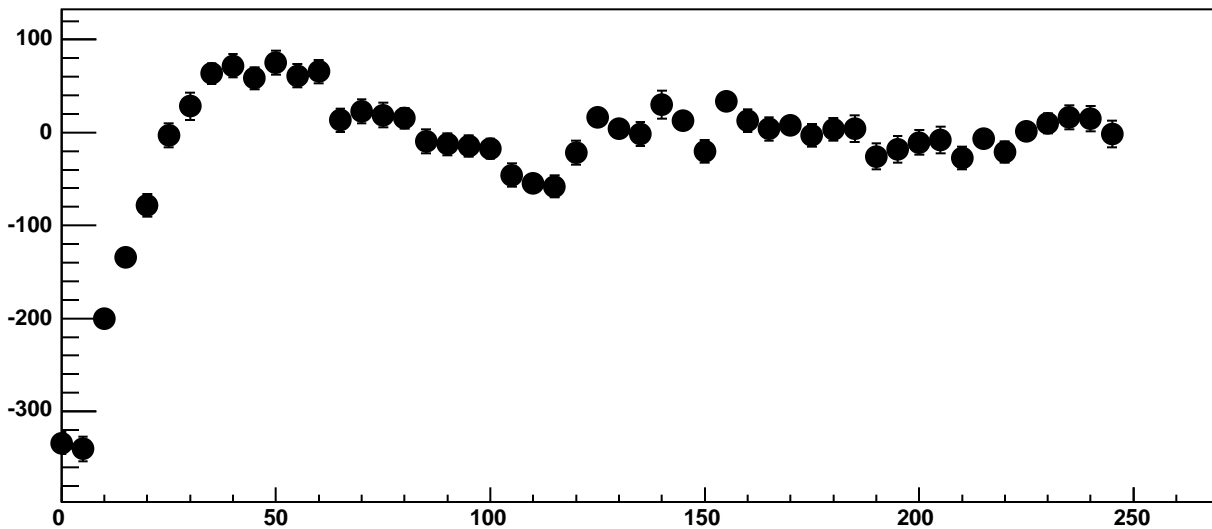


$\chi^2 / \text{ndf}$	533.1 / 41
p0	$-615.2 \pm 3.287$
p1	$111.2 \pm 0.8085$
p2	$-1.14\text{e}+08 \pm 1.673\text{e}+07$
p3	$1.402\text{e}+07 \pm 2.024\text{e}+06$
p4	$4.995 \pm 0.08858$

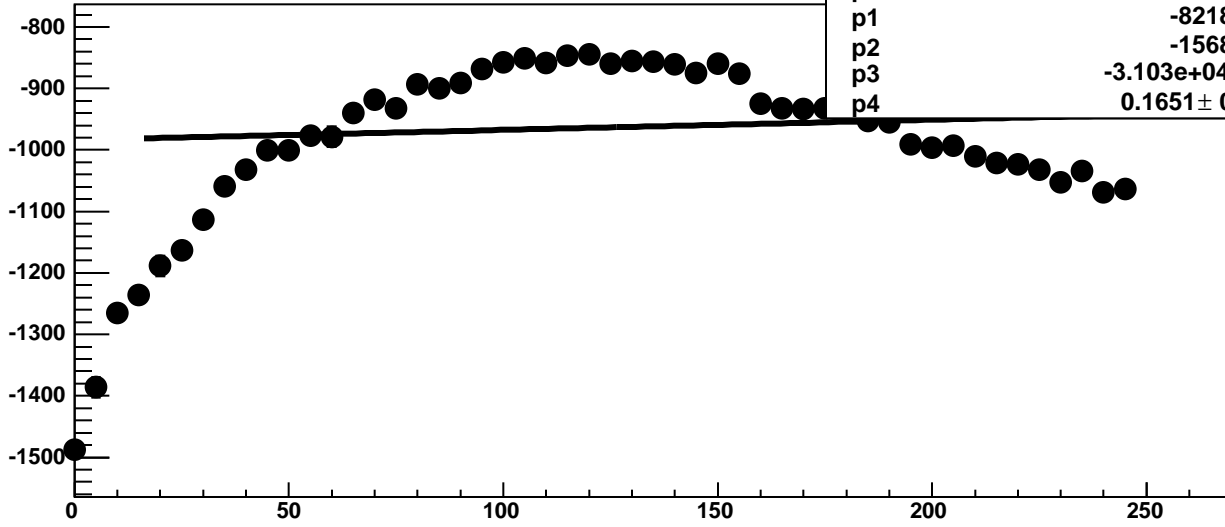
Chip 6, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

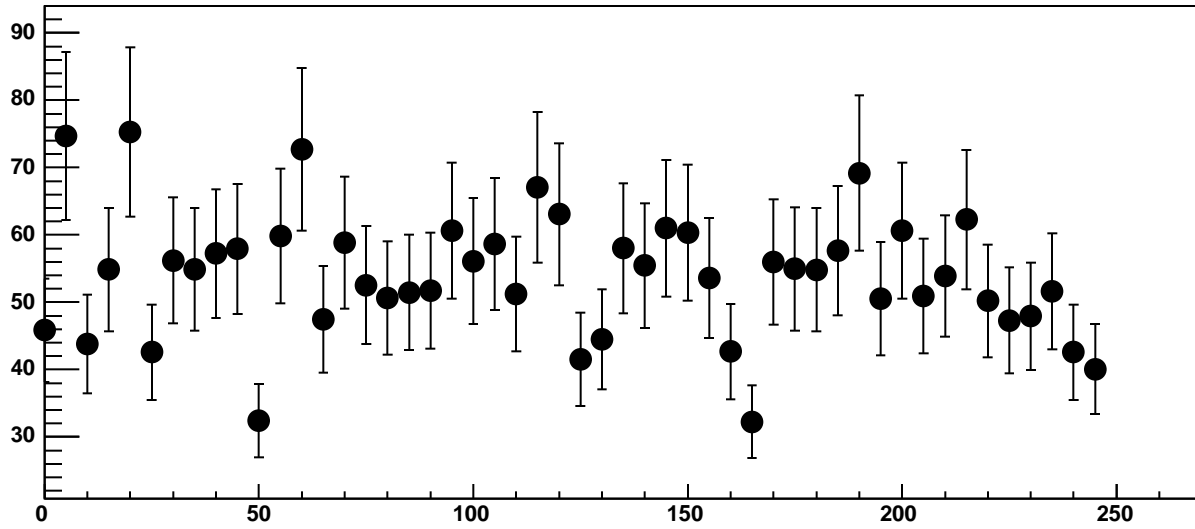


Chip 6, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

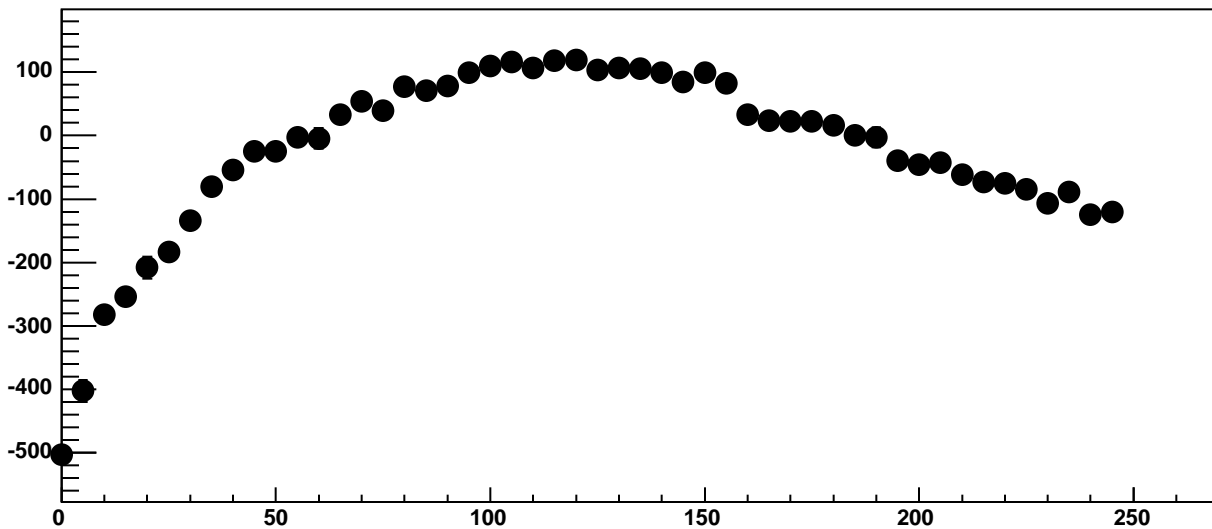


$\chi^2 / \text{ndf}$	2678 / 41
p0	-773.5 ± 8.938
p1	-8218 ± 44.31
p2	-1568 ± 11.35
p3	-3.103e+04 ± 2297
p4	0.1651 ± 0.001071

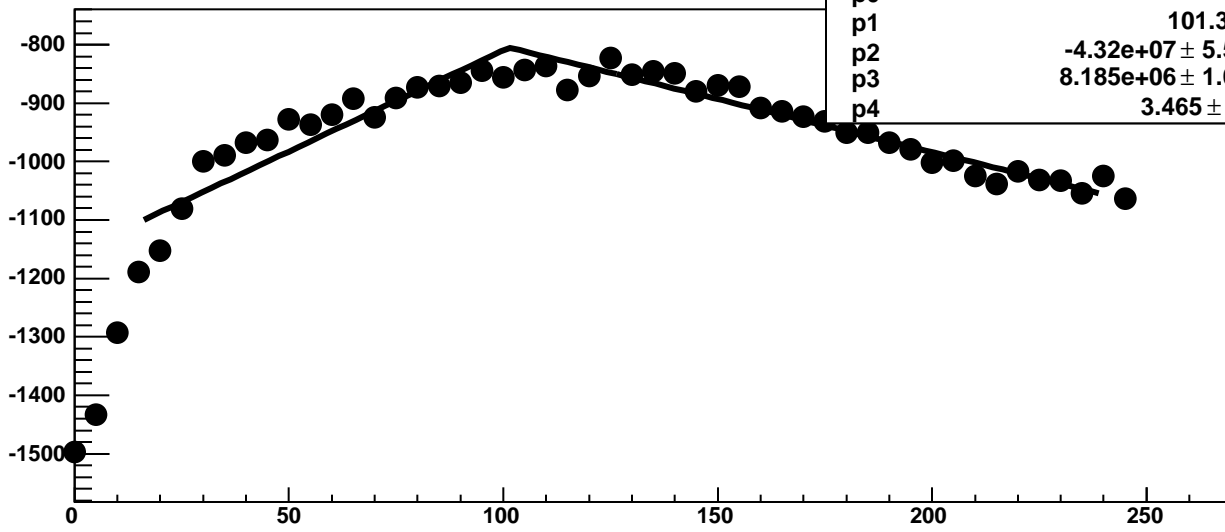
Chip 6, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

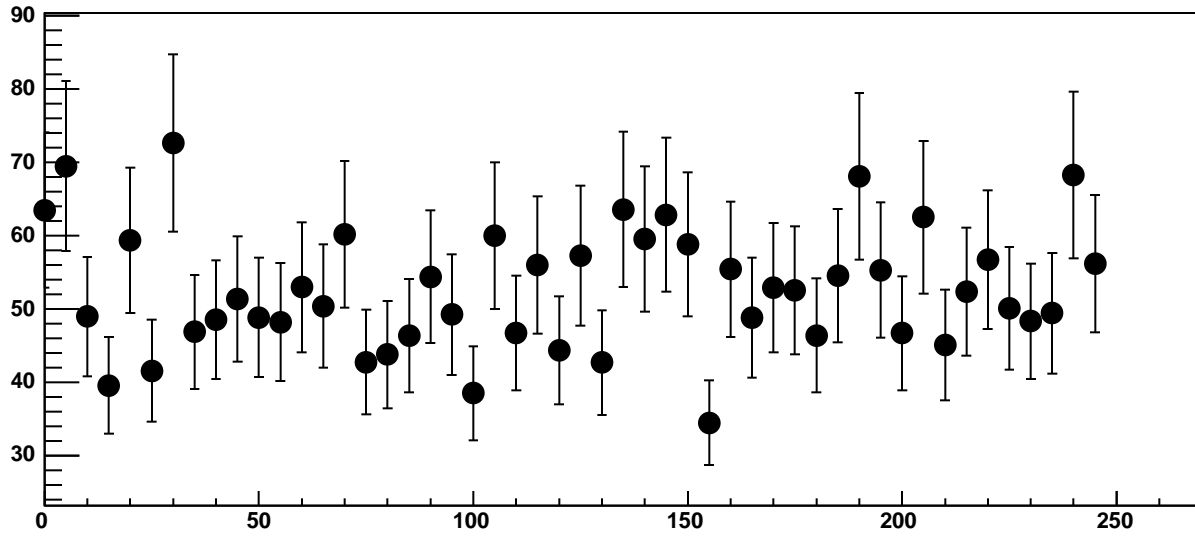


Chip 6, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold

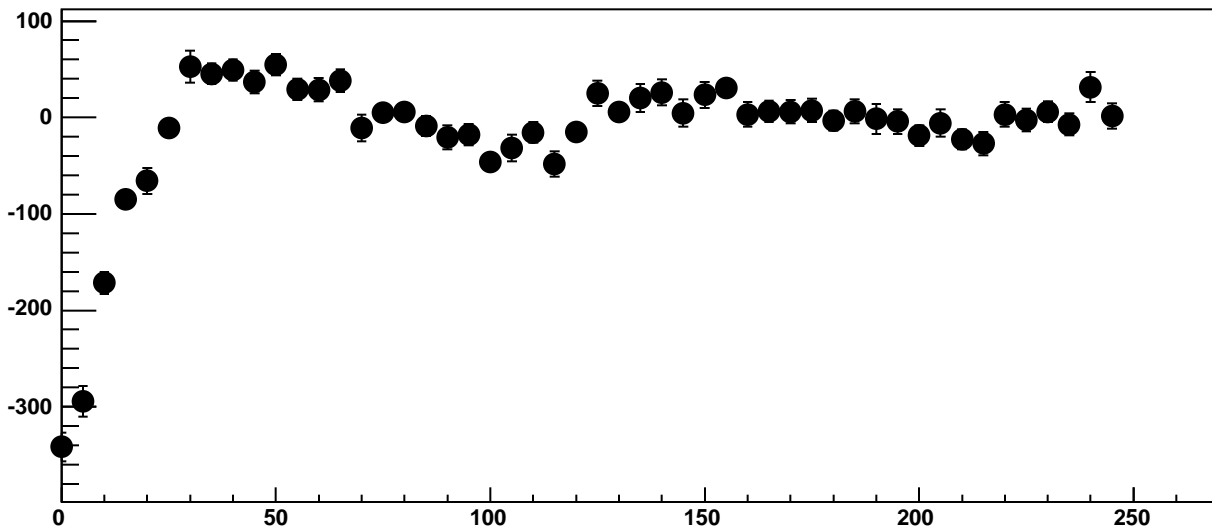


$\chi^2 / \text{ndf}$	321 / 41
p0	$-804.8 \pm 3.417$
p1	$101.3 \pm 1.259$
p2	$-4.32e+07 \pm 5.517e+06$
p3	$8.185e+06 \pm 1.032e+06$
p4	$3.465 \pm 0.09568$

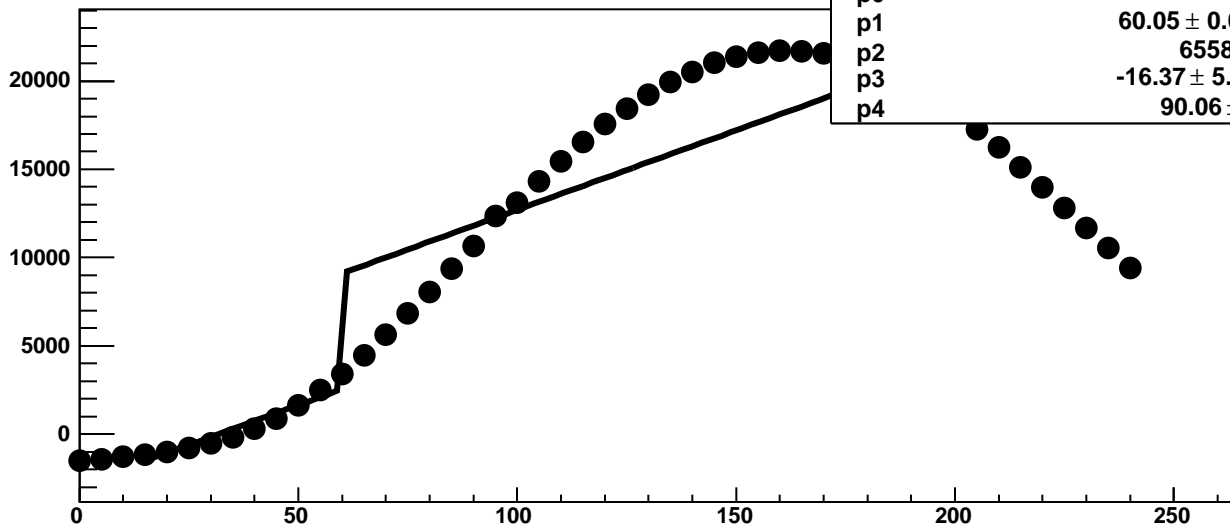
Chip 6, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold

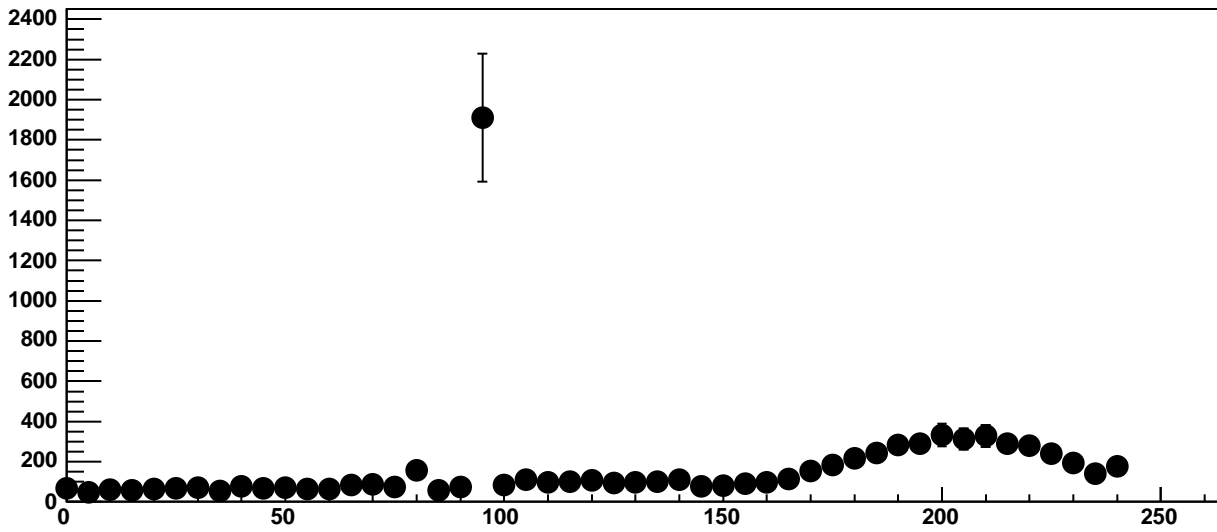


Chip 6, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

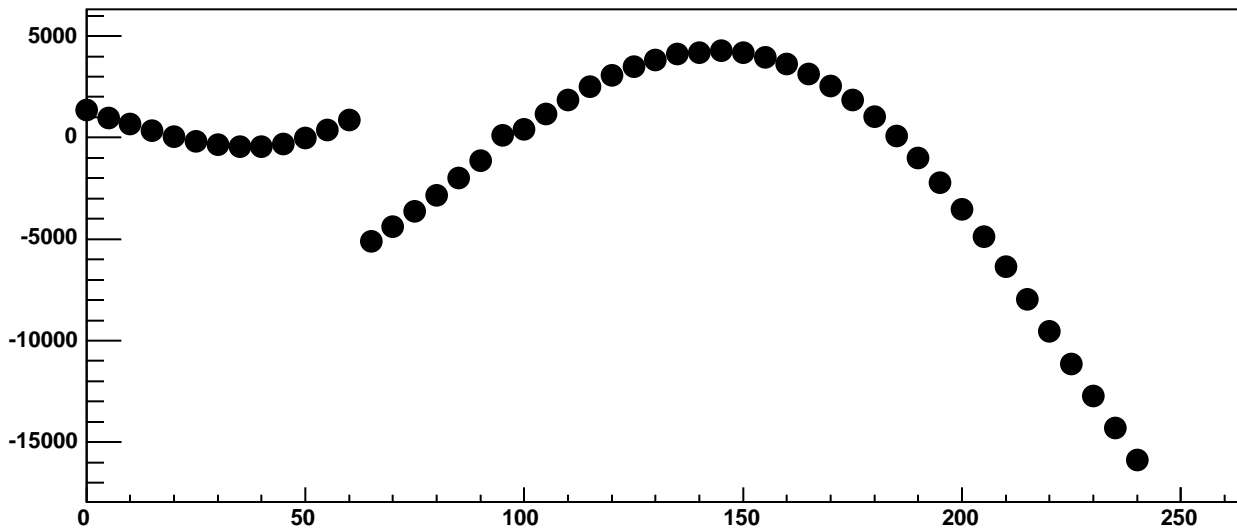


$\chi^2 / \text{ndf}$	1.069e+06 / 41
p0	2550 ± 4.96
p1	60.05 ± 0.0001122
p2	6558 ± 10.49
p3	-16.37 ± 5.365e-06
p4	90.06 ± 0.1142

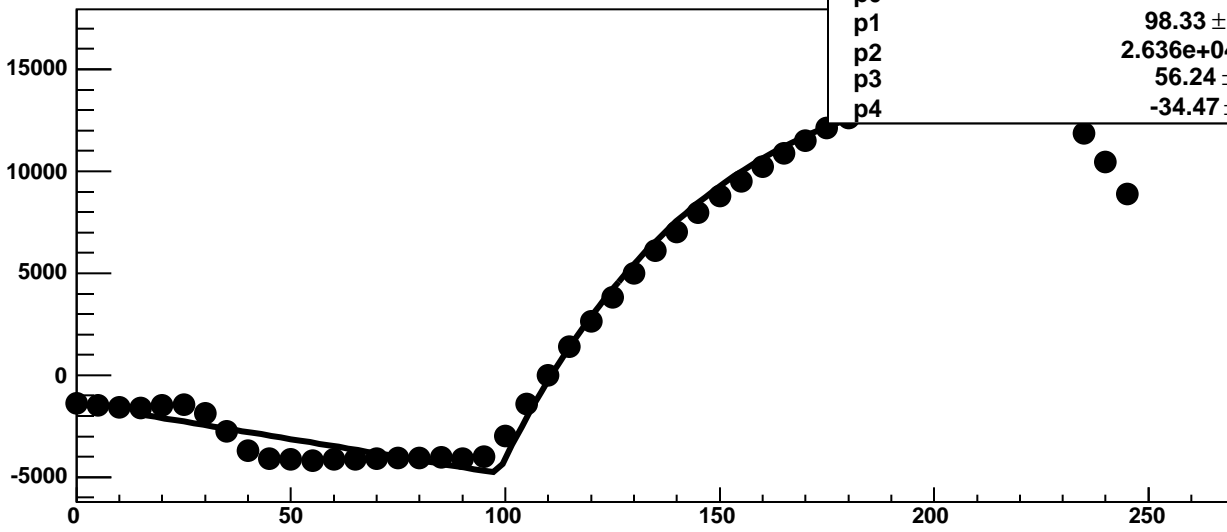
Chip 6, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

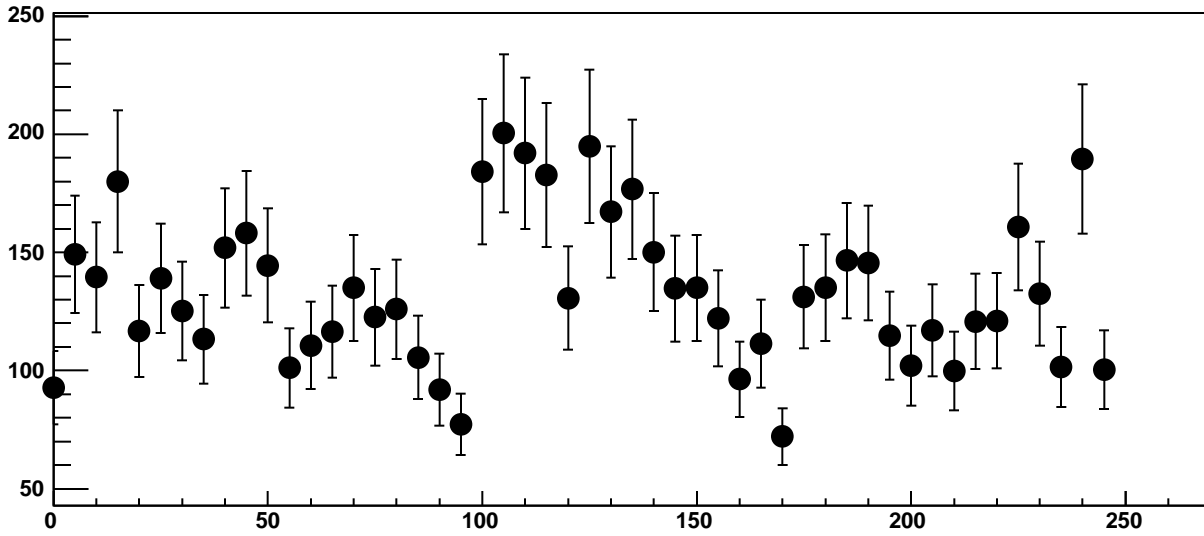


Chip 6, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

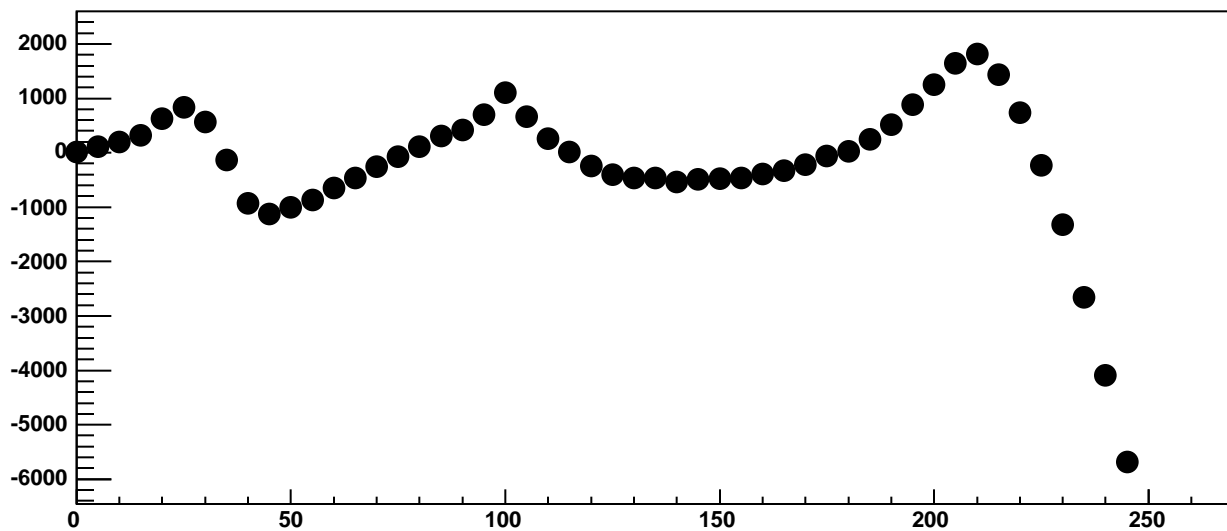


$\chi^2 / \text{ndf}$	5.33e+04 / 41
p0	-4798 ± 10.46
p1	98.33 ± 0.06221
p2	2.636e+04 ± 58.2
p3	56.24 ± 0.1746
p4	-34.47 ± 0.2469

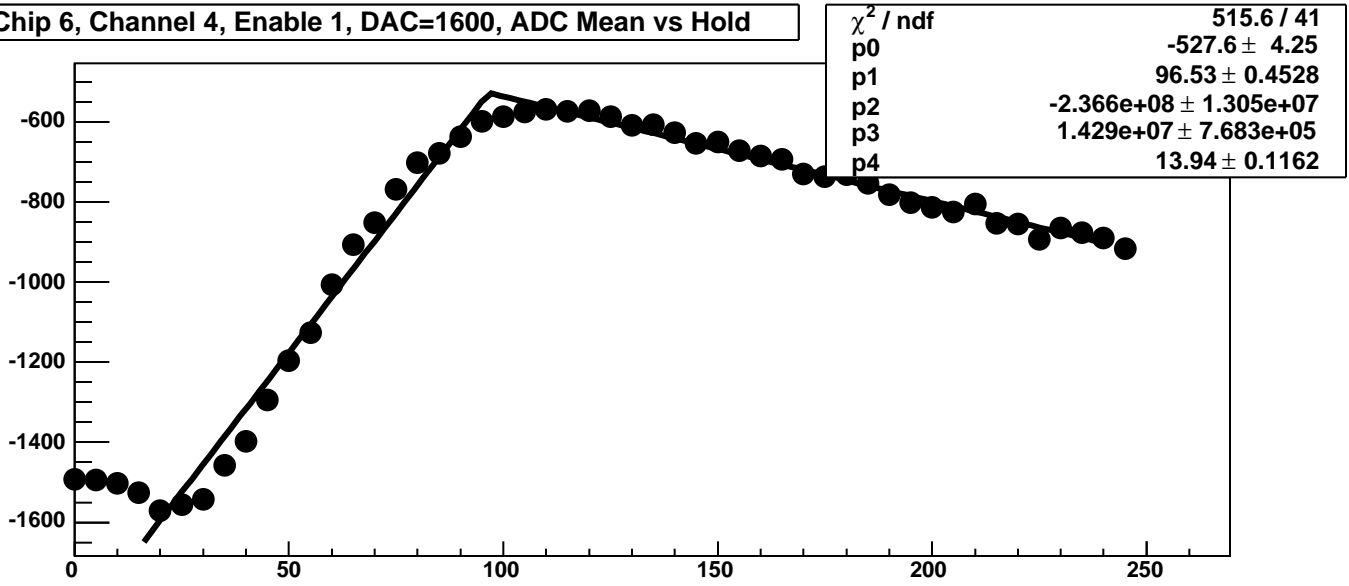
Chip 6, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



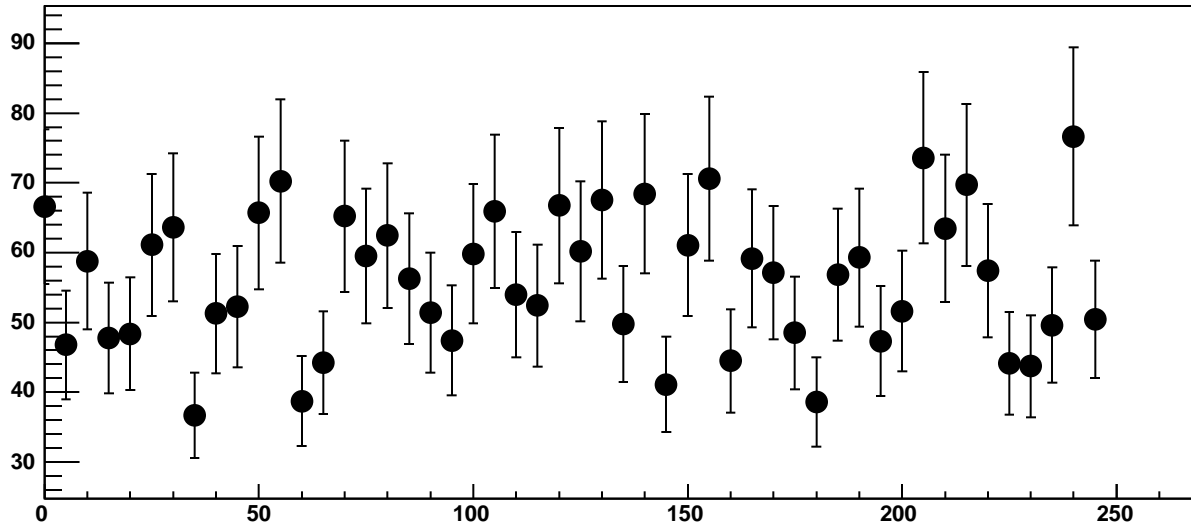
Chip 6, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



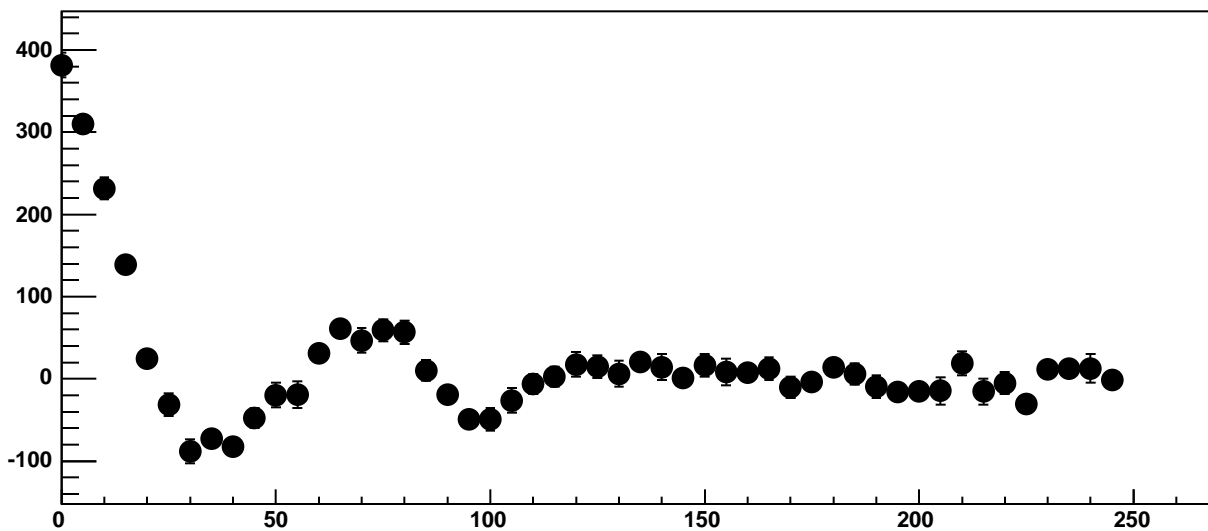
Chip 6, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 6, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

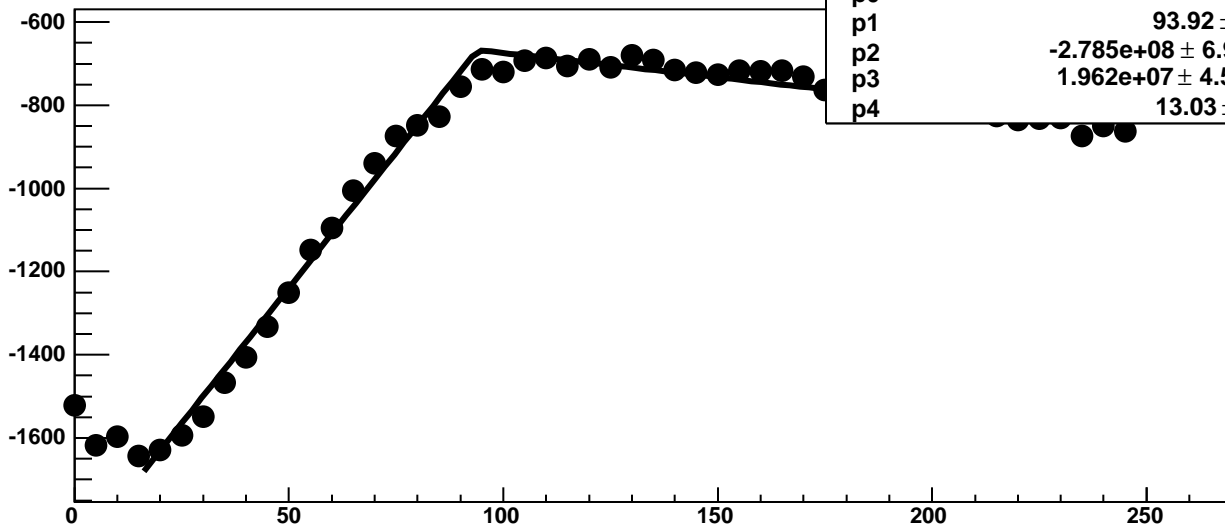


Chip 6, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold



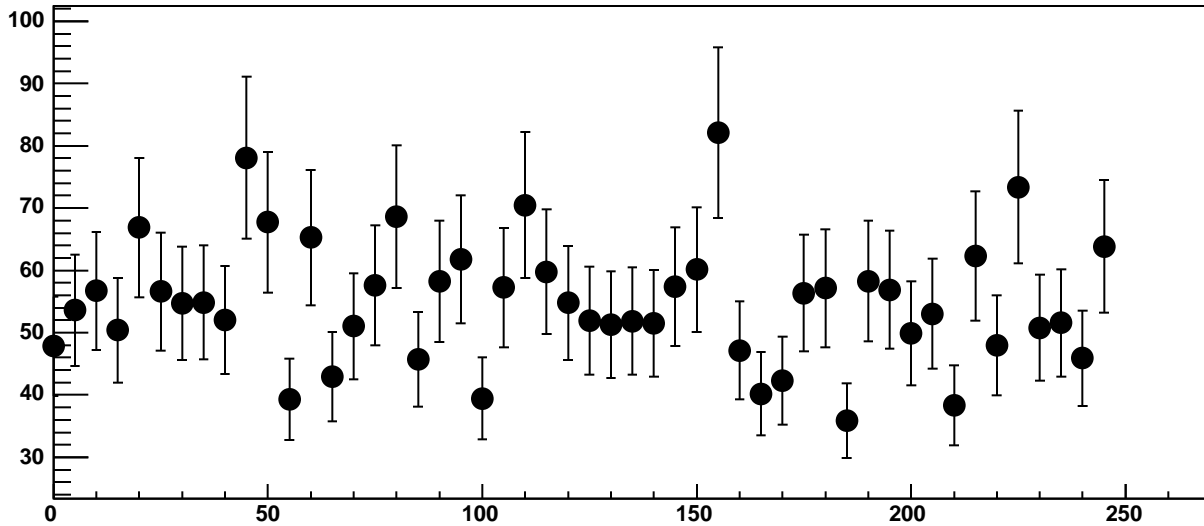


Chip 6, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

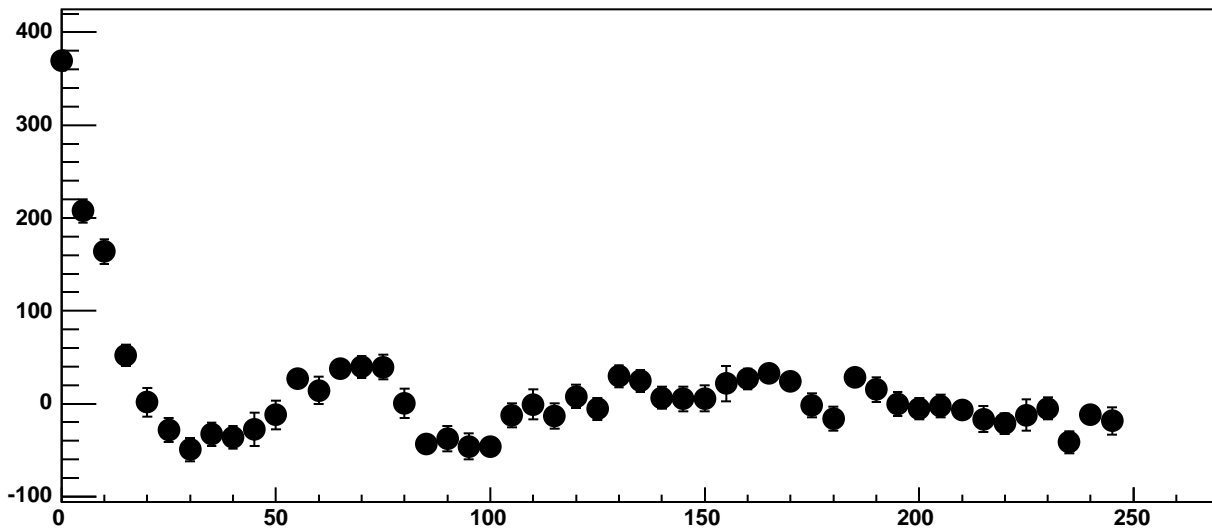


$\chi^2 / \text{ndf}$	241.4 / 41
p0	-667 ± 4.059
p1	93.92 ± 0.5435
p2	-2.785e+08 ± 6.939e+06
p3	1.962e+07 ± 4.533e+05
p4	13.03 ± 0.1369

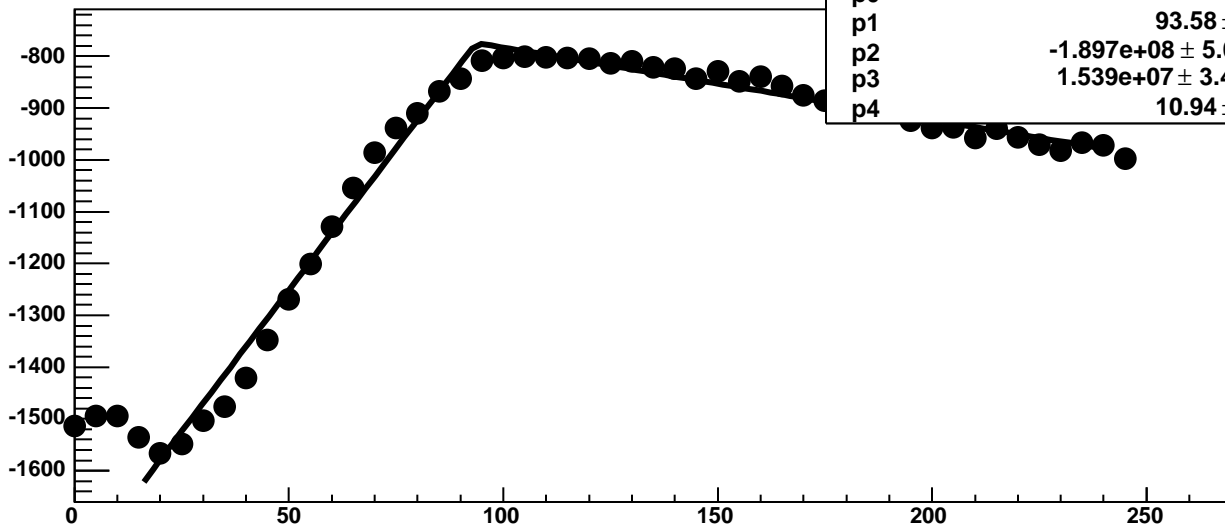
Chip 6, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

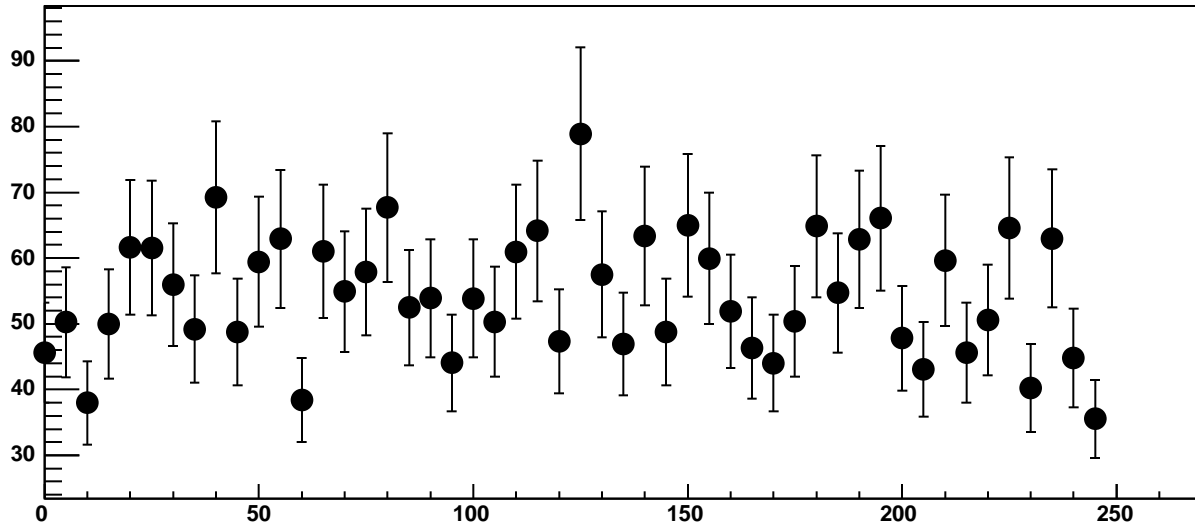


Chip 6, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

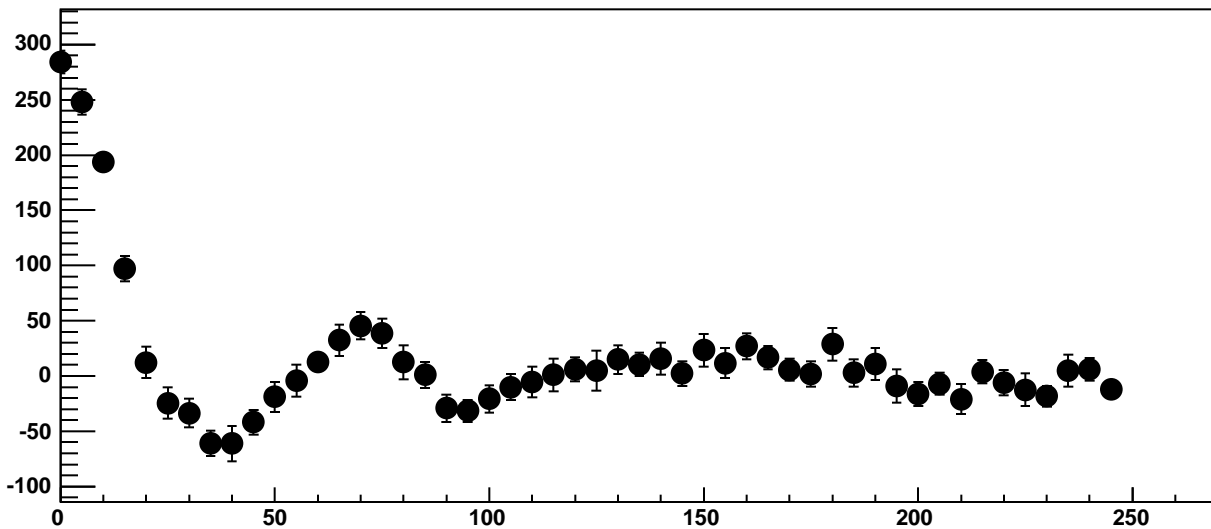


$\chi^2 / \text{ndf}$	221.8 / 41
p0	-774.2 ± 3.969
p1	93.58 ± 0.6332
p2	-1.897e+08 ± 5.095e+06
p3	1.539e+07 ± 3.446e+05
p4	10.94 ± 0.1379

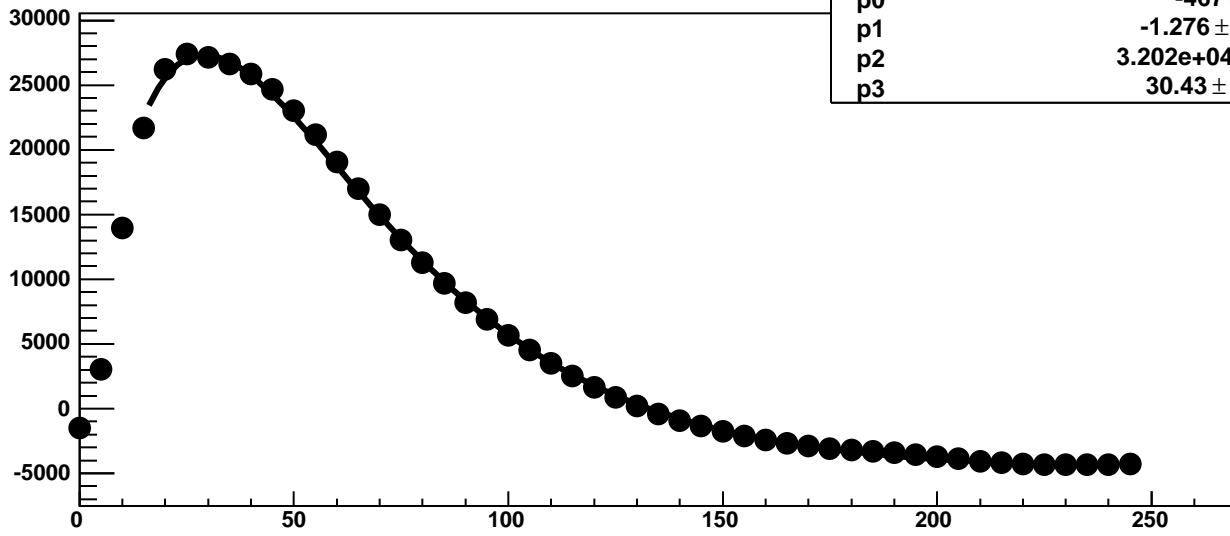
Chip 6, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

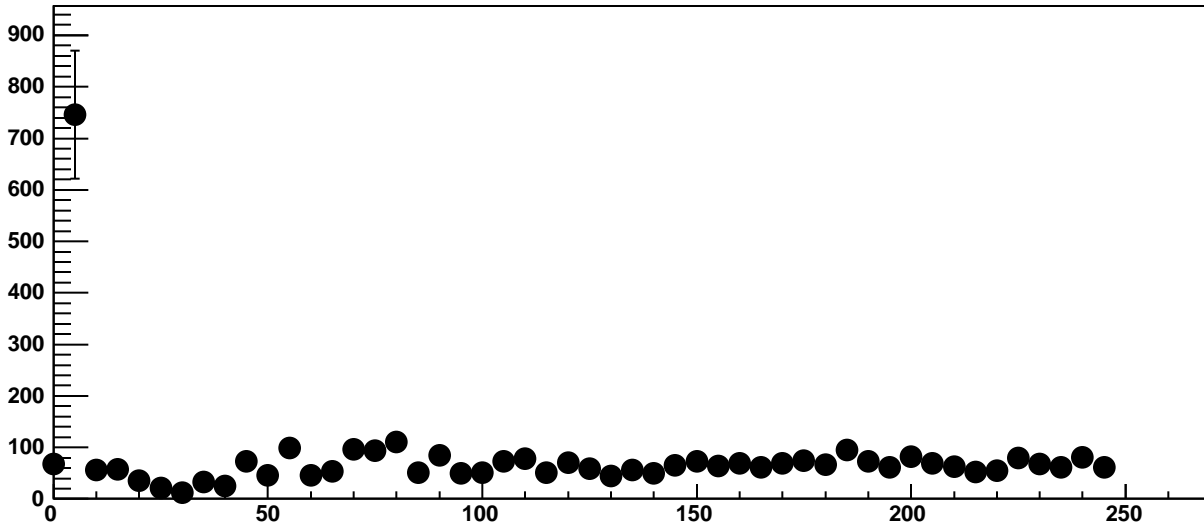


Chip 6, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

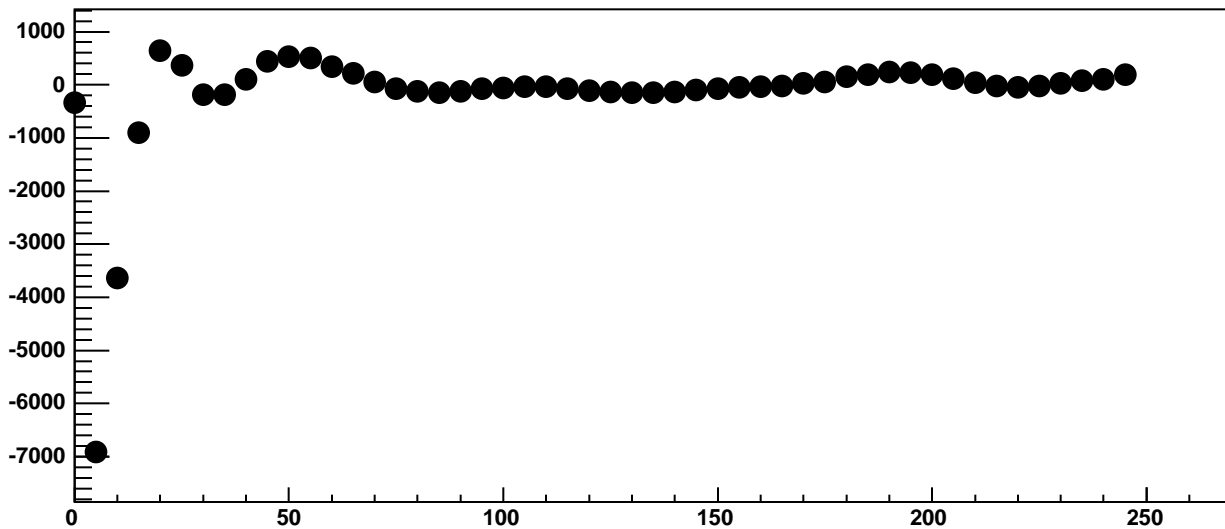


$\chi^2 / \text{ndf}$	2.91e+04 / 42
p0	-4671 ± 4.298
p1	-1.276 ± 0.01531
p2	3.202e+04 ± 4.462
p3	30.43 ± 0.01019

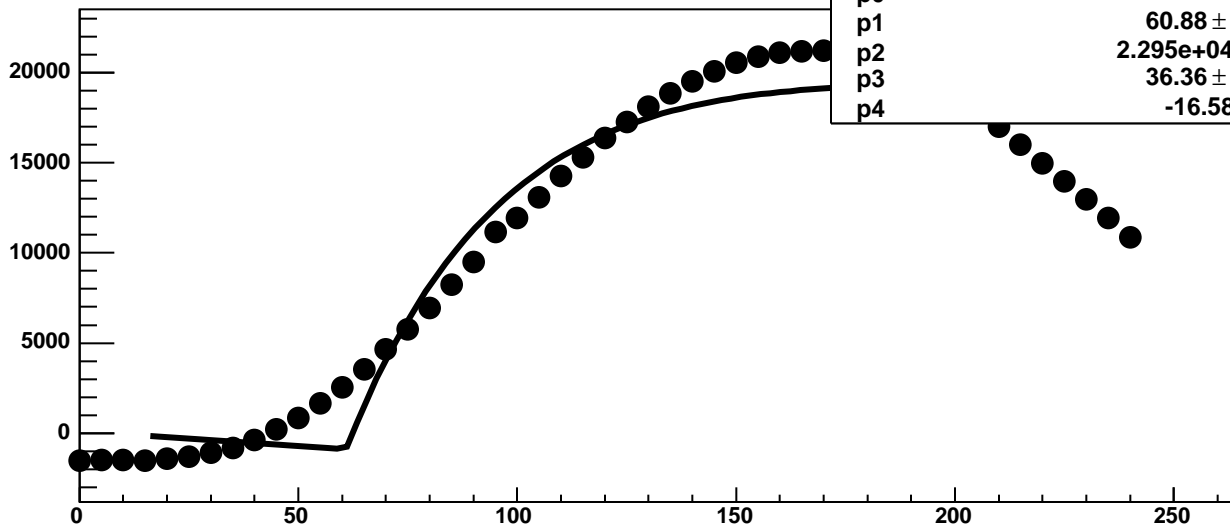
Chip 6, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

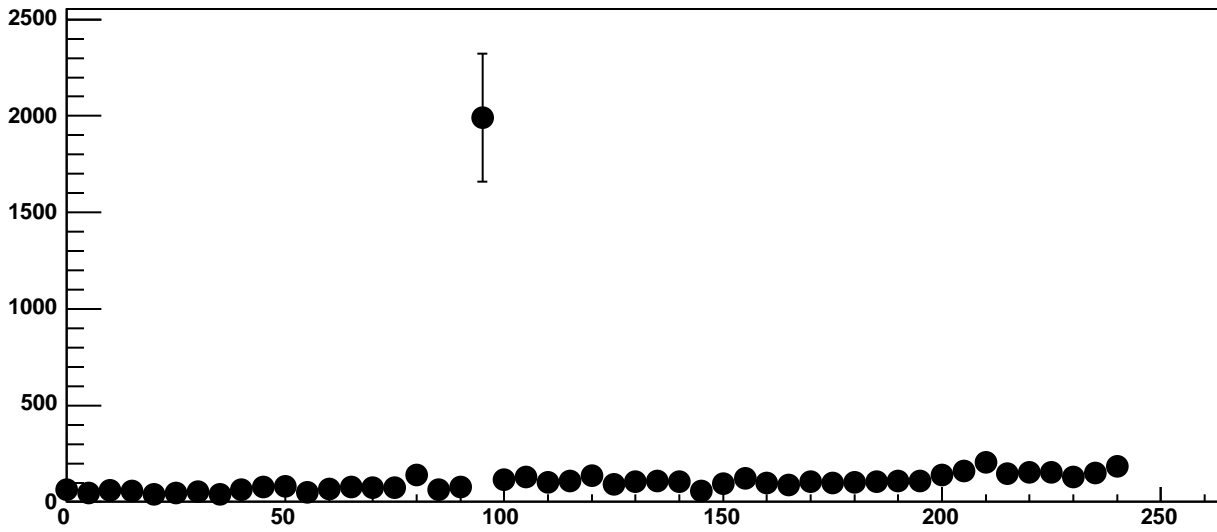


Chip 6, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

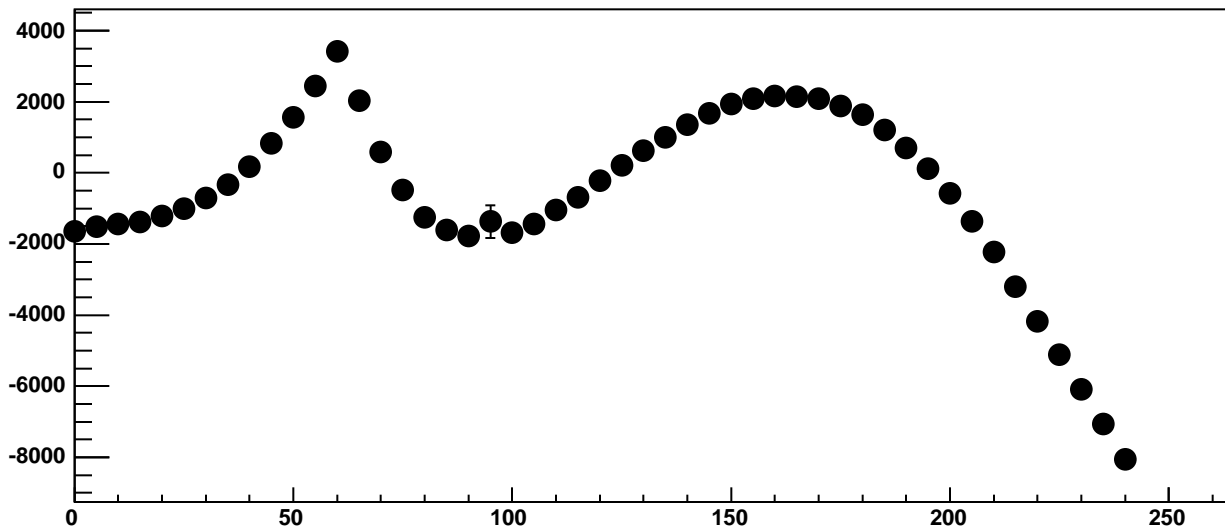


$\chi^2 / \text{ndf}$	4.41e+05 / 41
p0	-890.2 ± 6.101
p1	60.88 ± 0.02545
p2	2.295e+04 ± 32.02
p3	36.36 ± 0.06303
p4	-16.58 ± 0.184

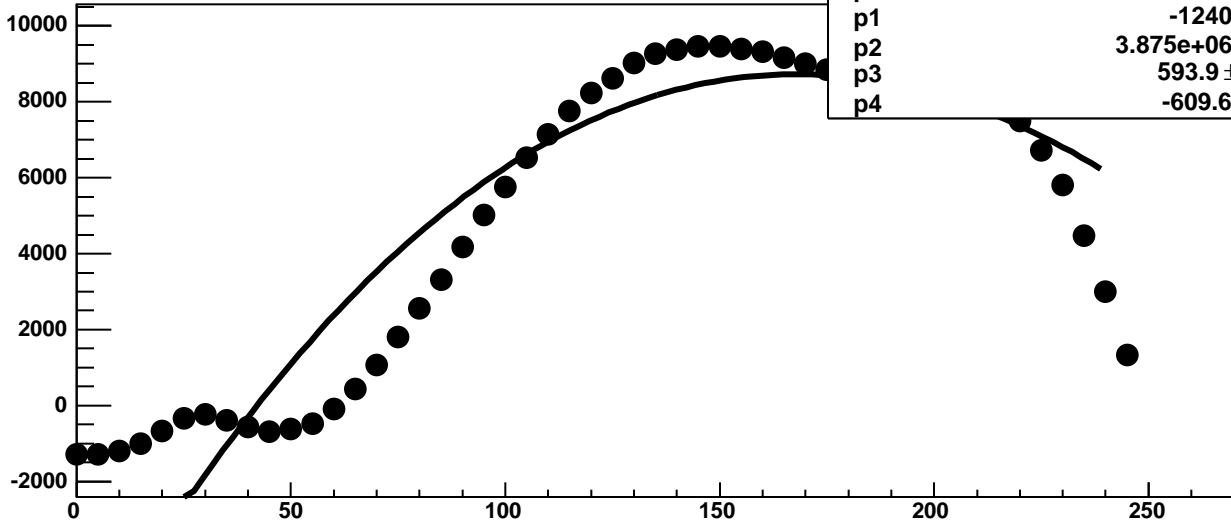
Chip 6, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold

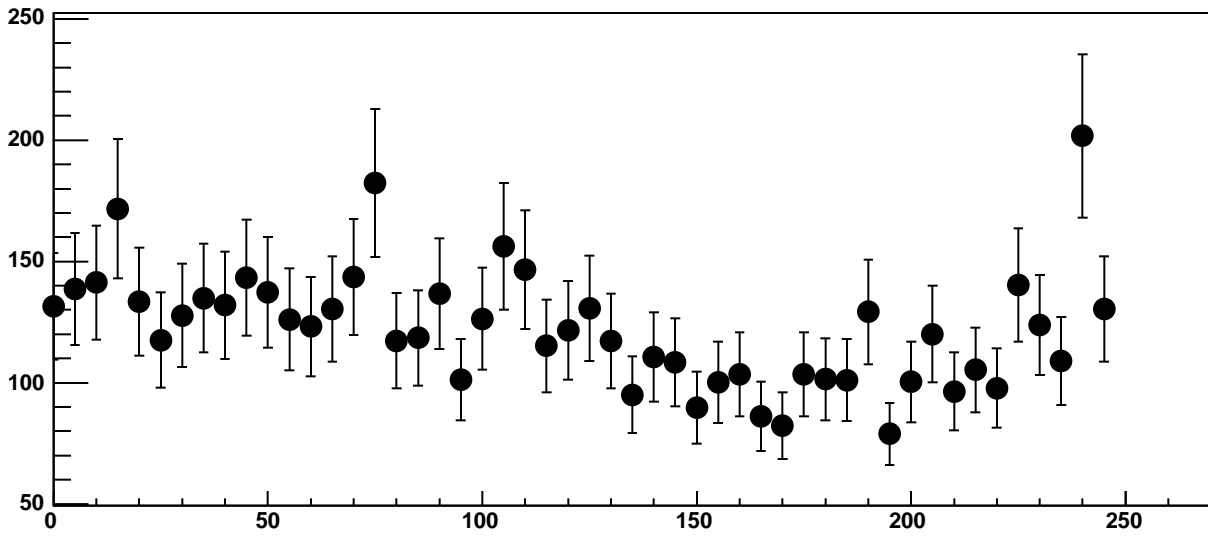


Chip 6, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

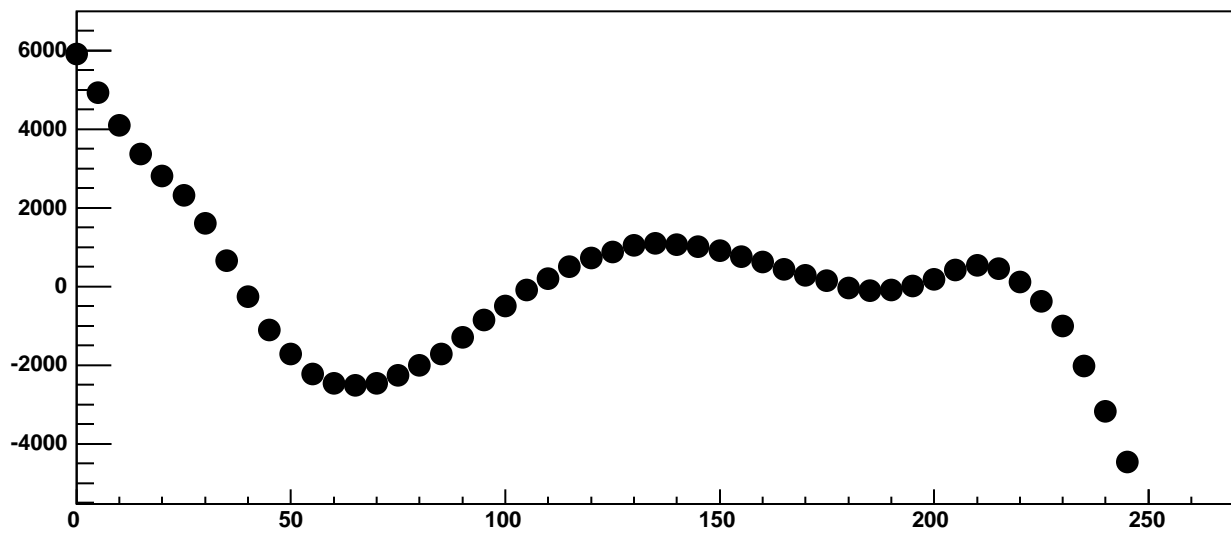


$\chi^2 / \text{ndf}$	1.005e+05 / 41
p0	-2.646e+06 ± 3938
p1	-1240 ± 1.248
p2	3.875e+06 ± 5764
p3	593.9 ± 0.5638
p4	-609.6 ± 1.164

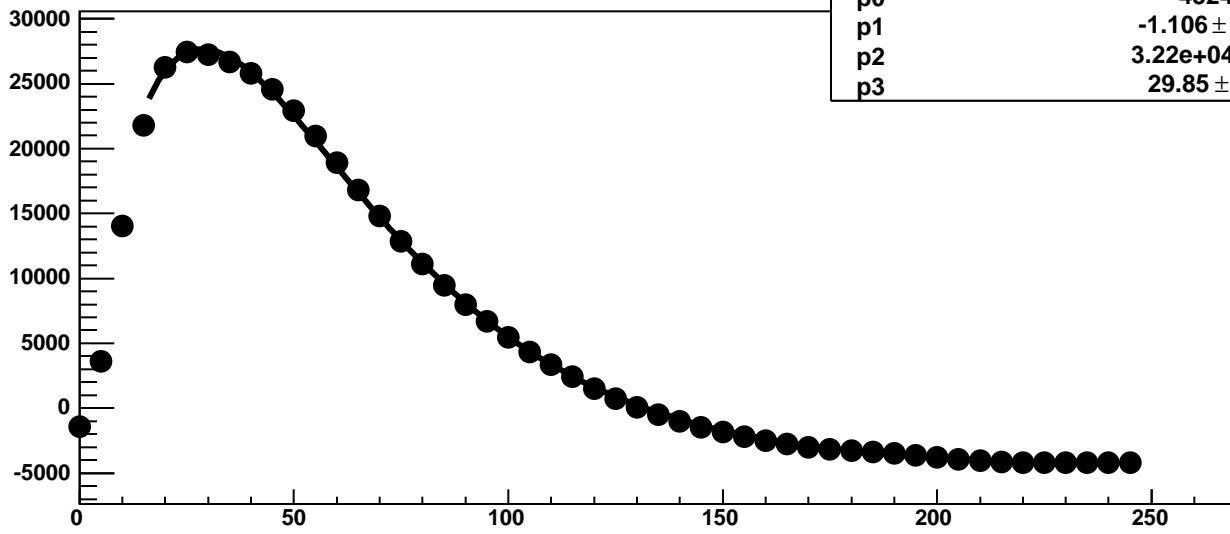
Chip 6, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

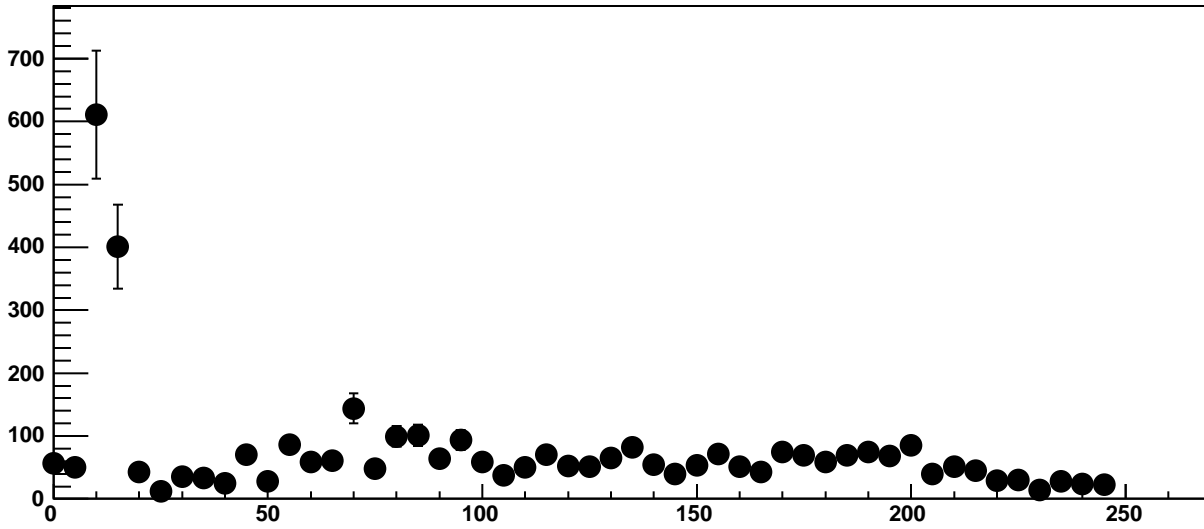


Chip 6, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold

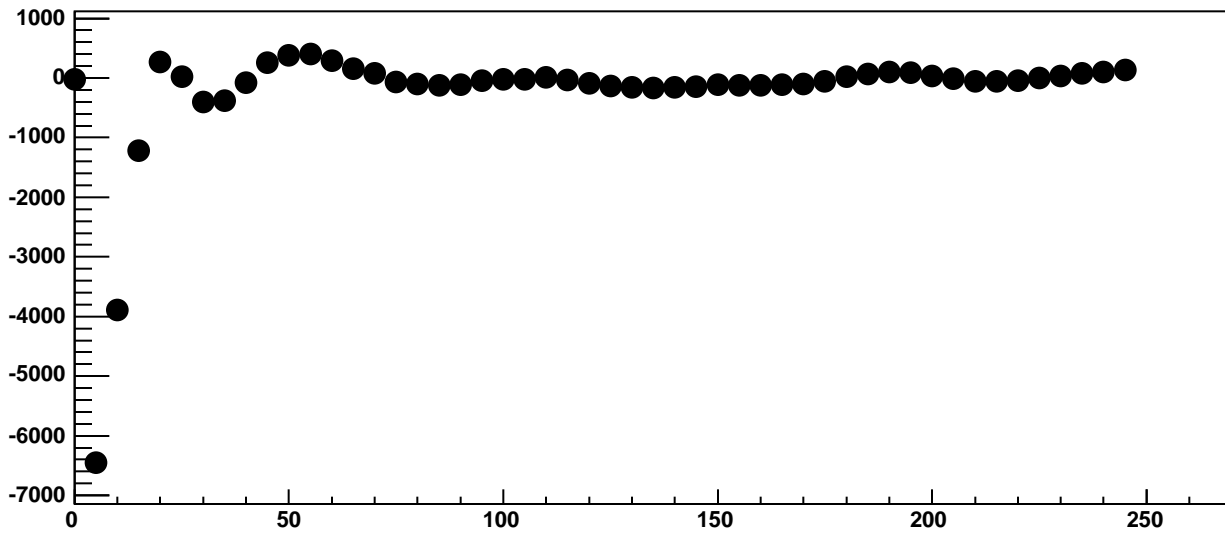


$\chi^2 / \text{ndf}$	1.301e+04 / 42
p0	-4524 $\pm$ 2.282
p1	-1.106 $\pm$ 0.01773
p2	3.22e+04 $\pm$ 2.906
p3	29.85 $\pm$ 0.00991

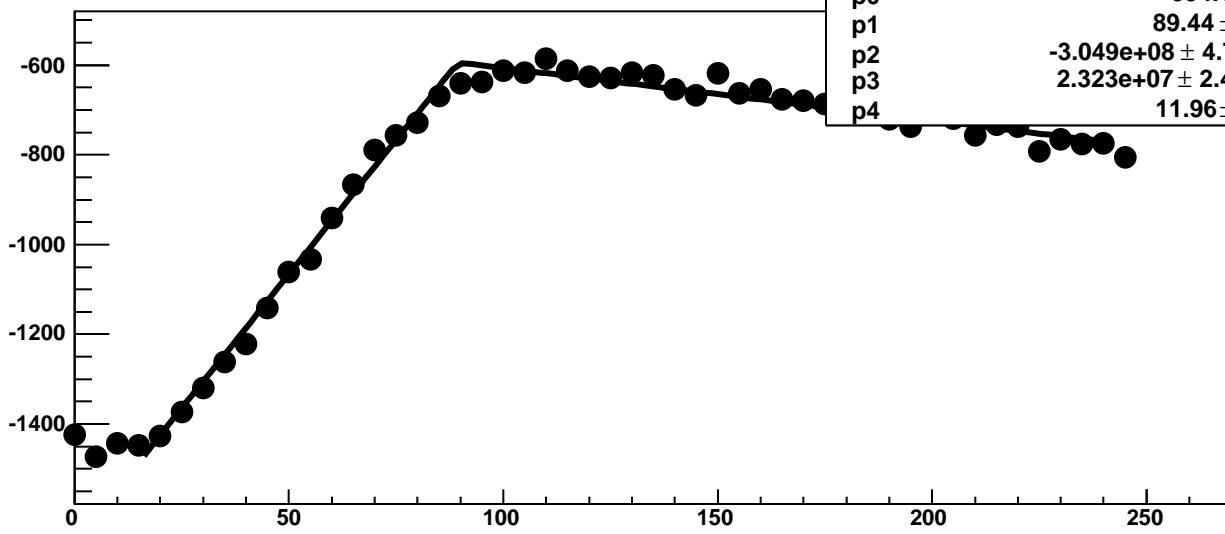
Chip 6, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

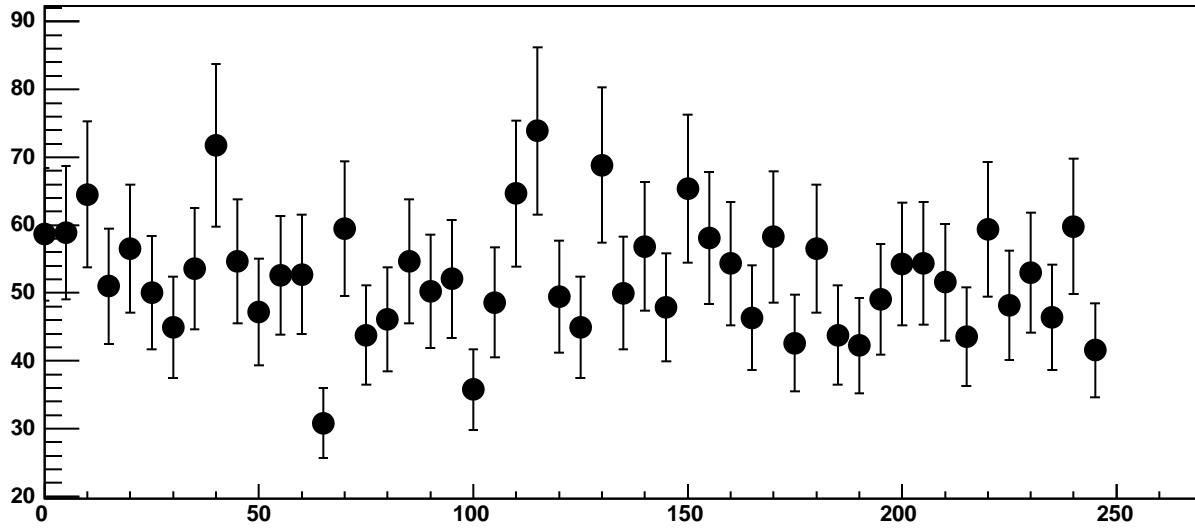


Chip 6, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

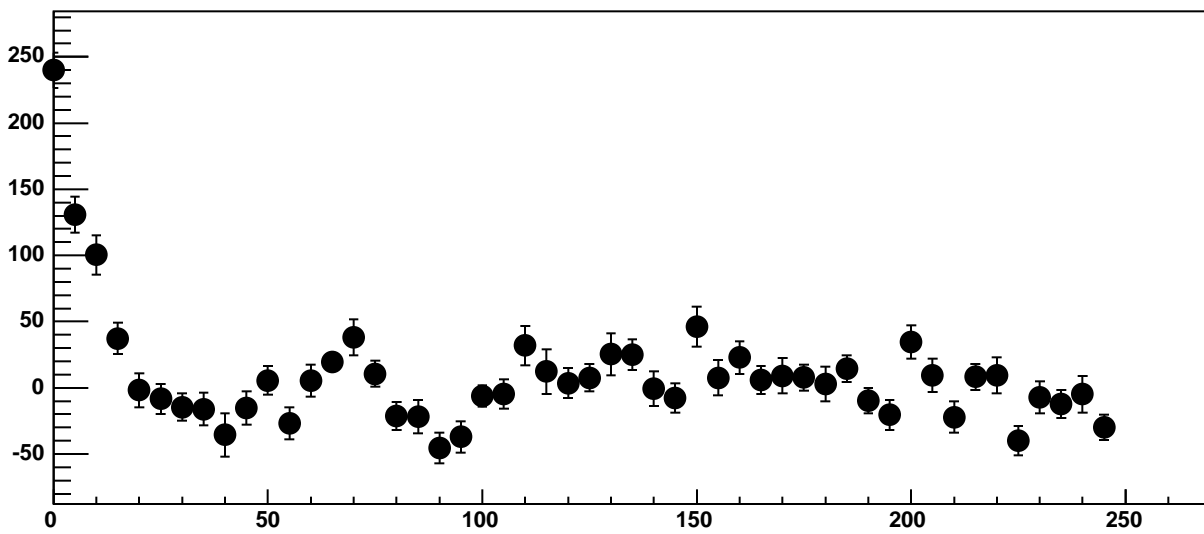


$\chi^2 / \text{ndf}$	137.6 / 41
p0	$-594.1 \pm 3.752$
p1	$89.44 \pm 0.5425$
p2	$-3.049\text{e}+08 \pm 4.783\text{e}+06$
p3	$2.323\text{e}+07 \pm 2.451\text{e}+05$
p4	$11.96 \pm 0.1366$

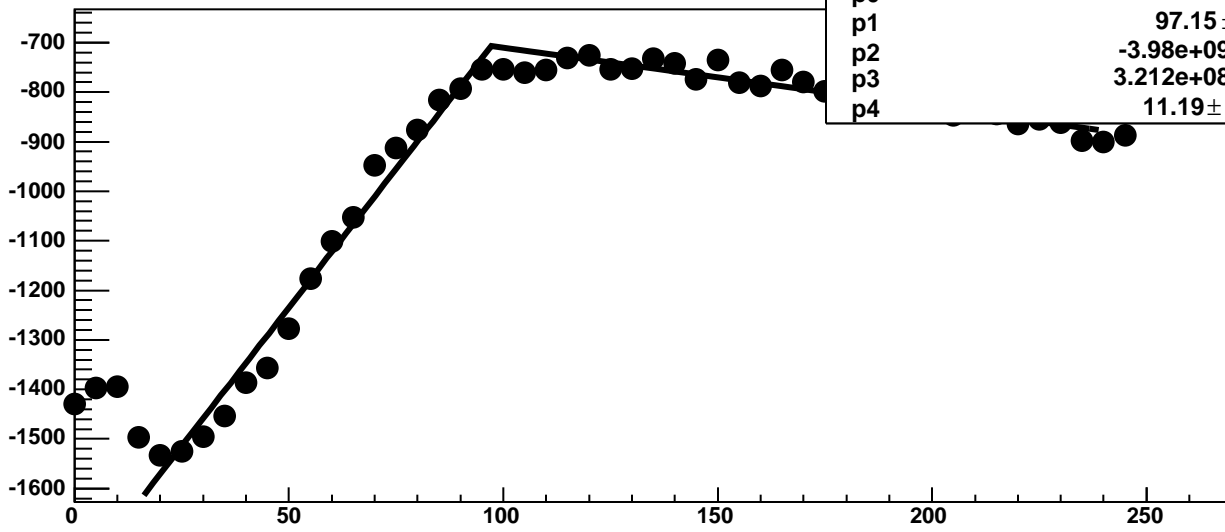
Chip 6, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

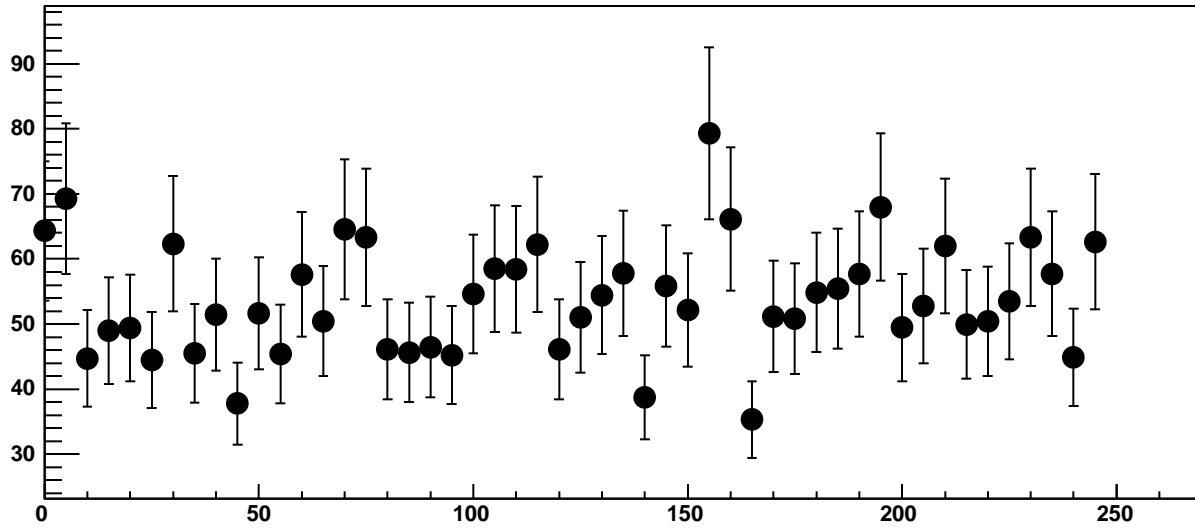


Chip 6, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

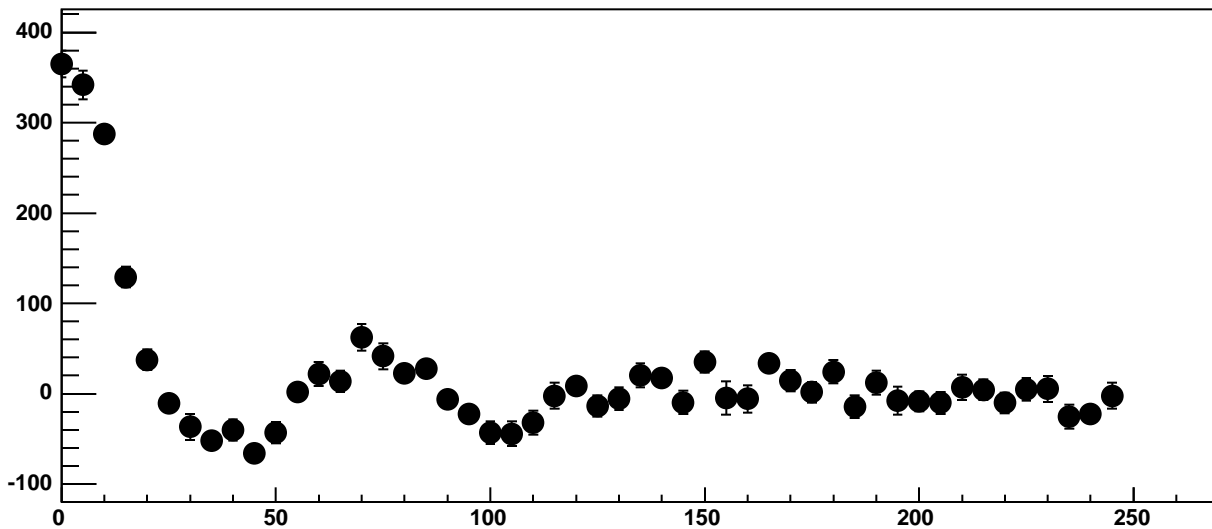


$\chi^2 / \text{ndf}$	386.4 / 41
p0	$-707 \pm 1.327$
p1	$97.15 \pm 0.3157$
p2	$-3.98e+09 \pm 1.414$
p3	$3.212e+08 \pm 1.414$
p4	$11.19 \pm 0.03214$

Chip 6, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

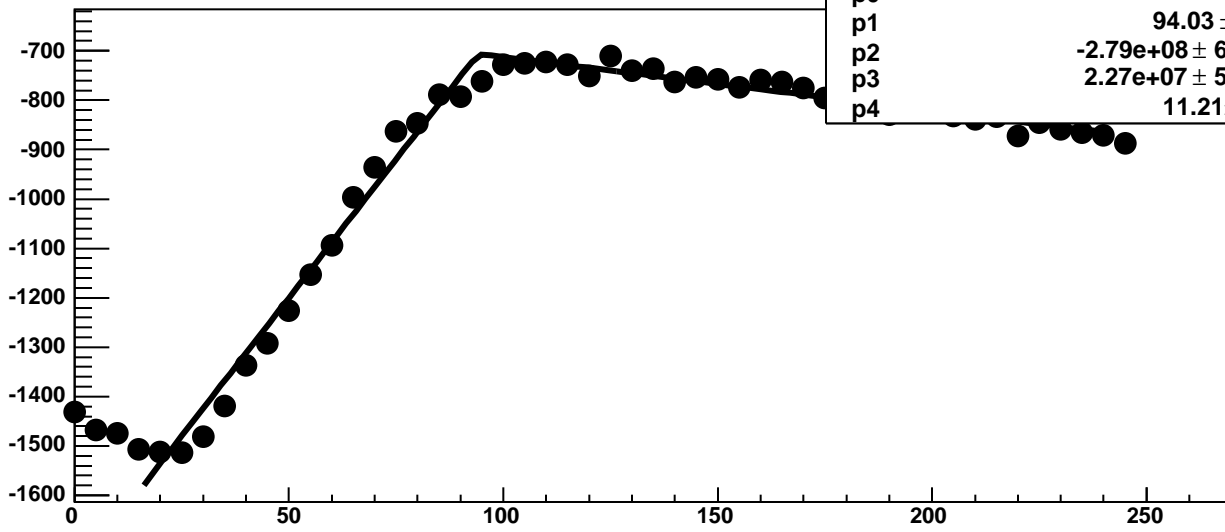


Chip 6, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold



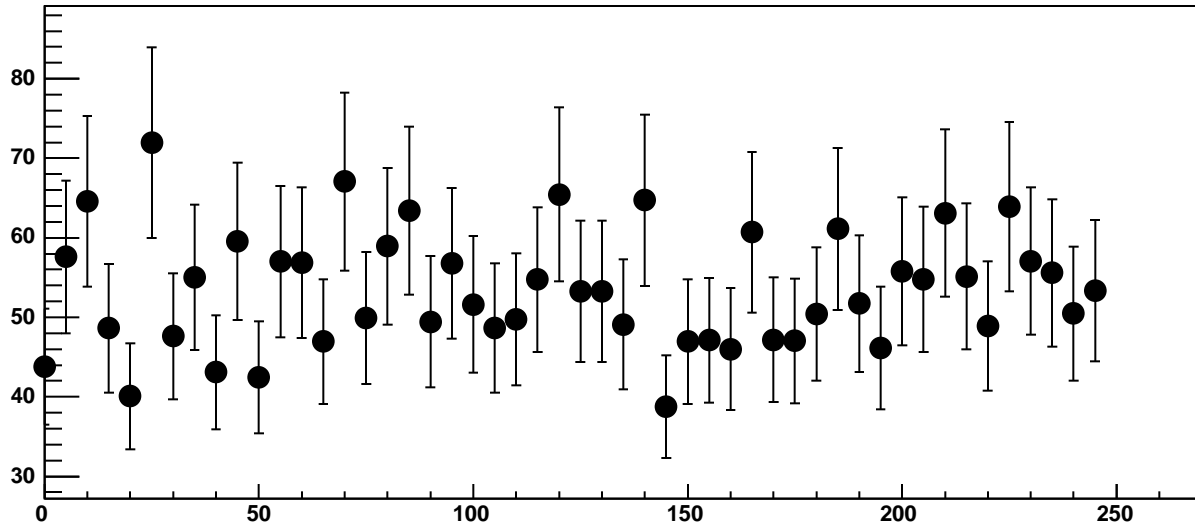


Chip 6, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold

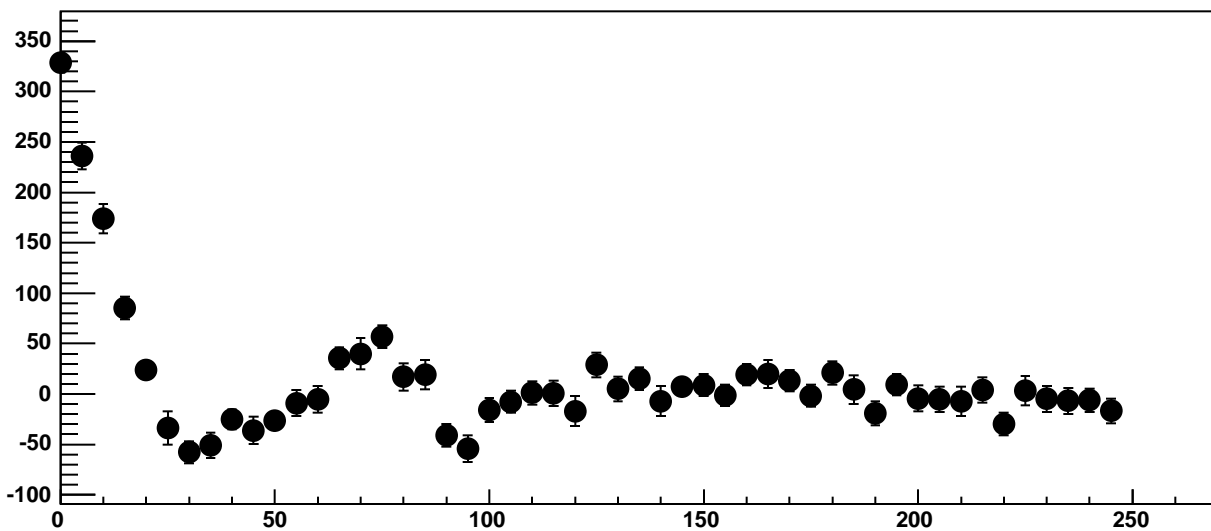


$\chi^2 / \text{ndf}$	245.5 / 41
p0	-706.3 ± 3.984
p1	94.03 ± 0.6255
p2	-2.79e+08 ± 6.88e+06
p3	2.27e+07 ± 5.01e+05
p4	11.21 ± 0.1281

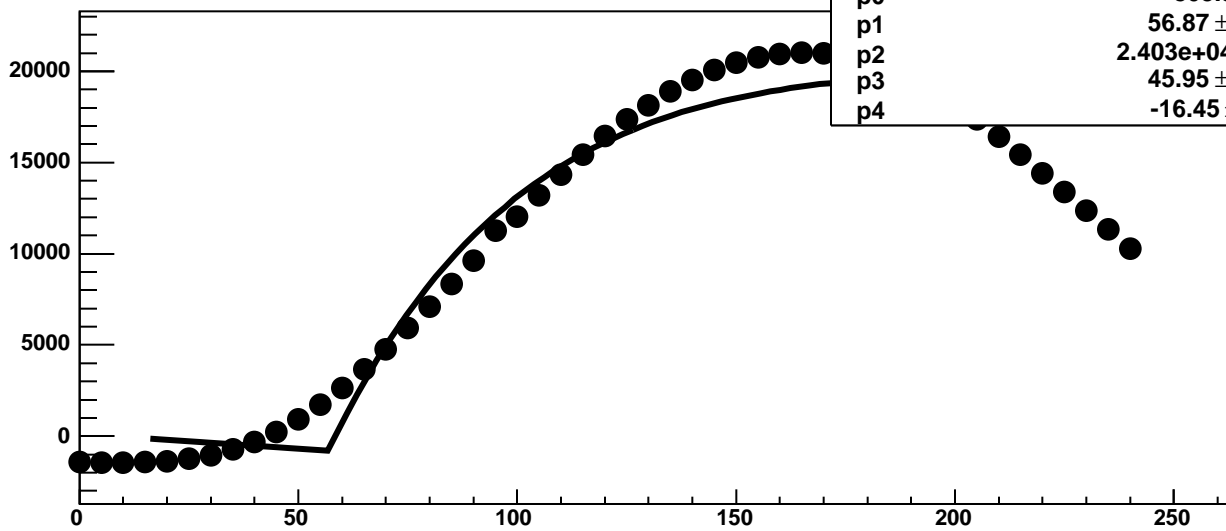
Chip 6, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold

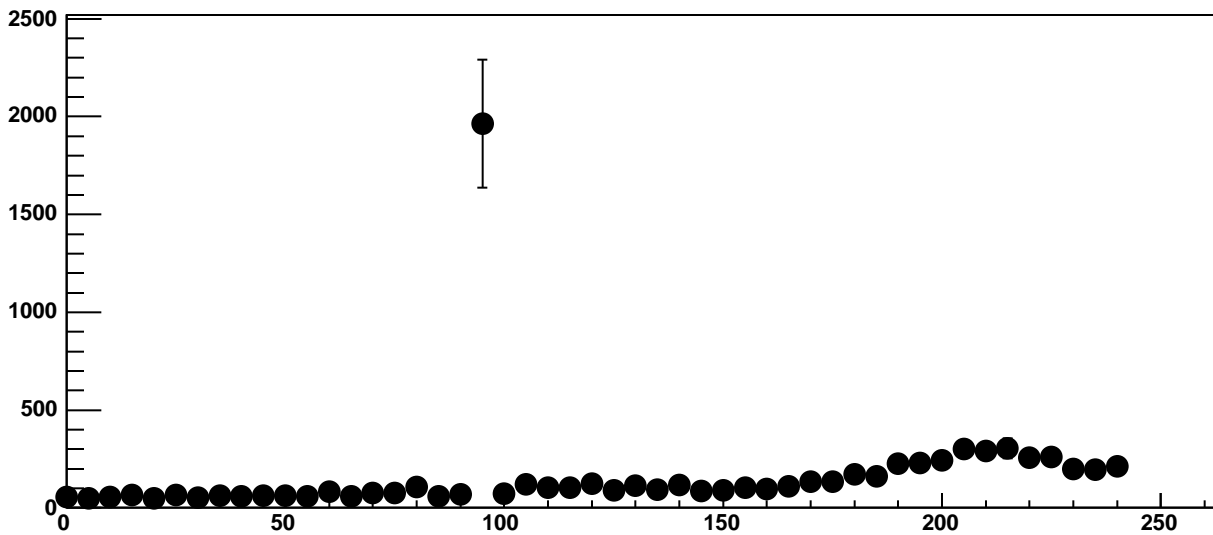


Chip 6, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

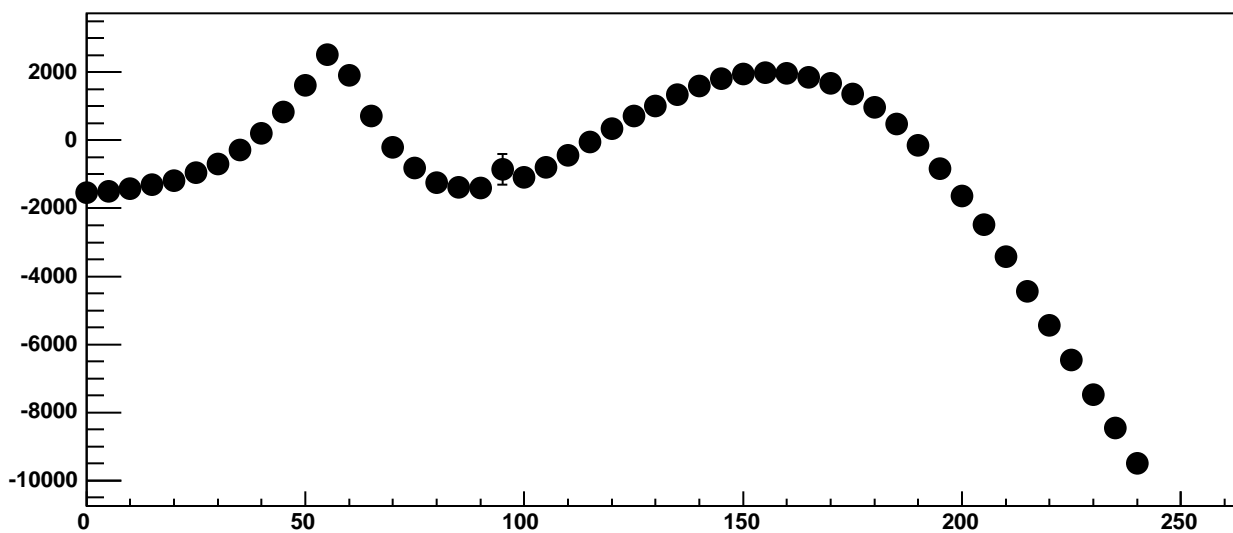


$\chi^2 / \text{ndf}$	2.968e+05 / 41
p0	-803.9 ± 7.135
p1	56.87 ± 0.02781
p2	2.403e+04 ± 46.17
p3	45.95 ± 0.09351
p4	-16.45 ± 0.2536

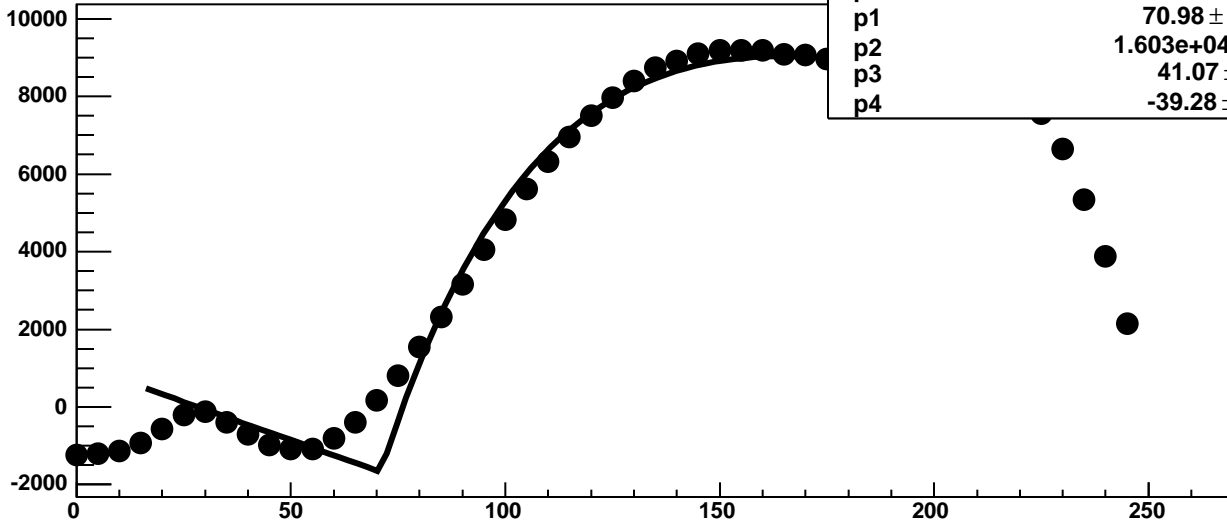
Chip 6, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

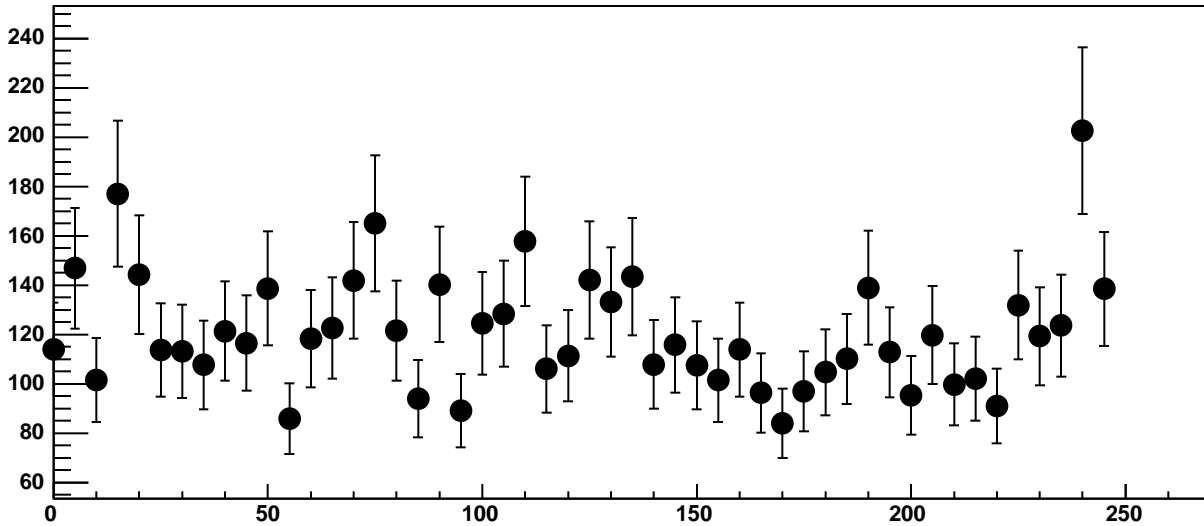


Chip 6, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

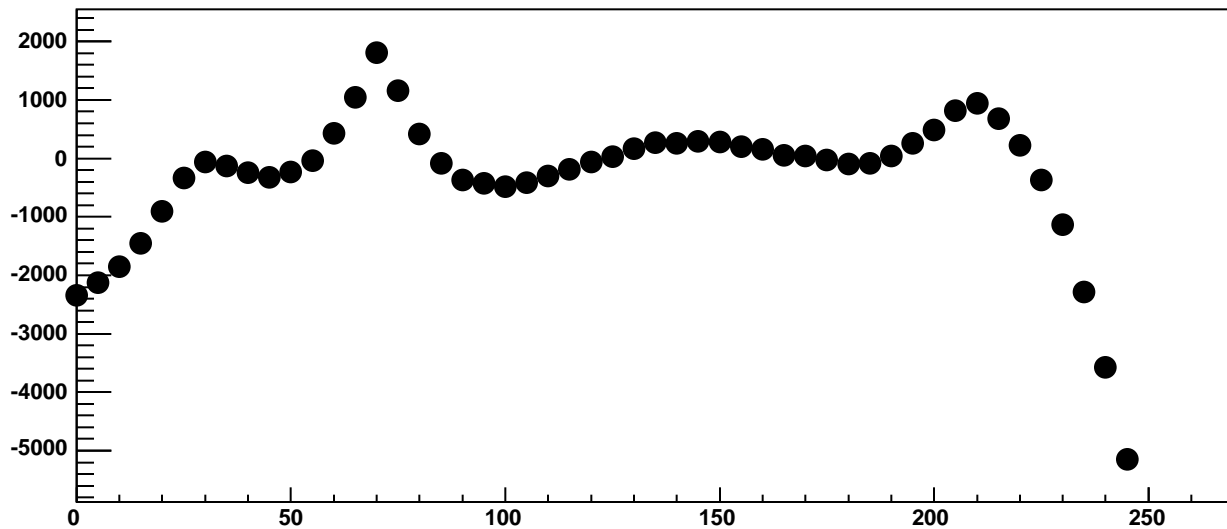


$\chi^2 / \text{ndf}$	2.861e+04 / 41
p0	-1675 ± 10.6
p1	70.98 ± 0.07438
p2	1.603e+04 ± 64.35
p3	41.07 ± 0.2068
p4	-39.28 ± 0.3334

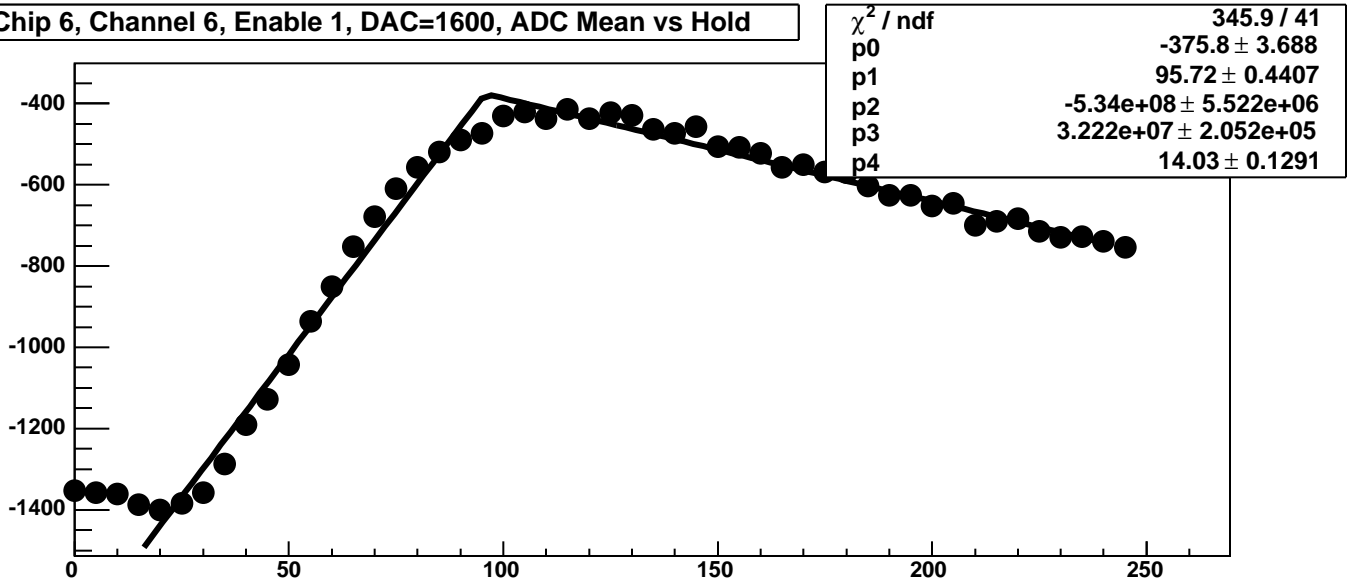
Chip 6, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



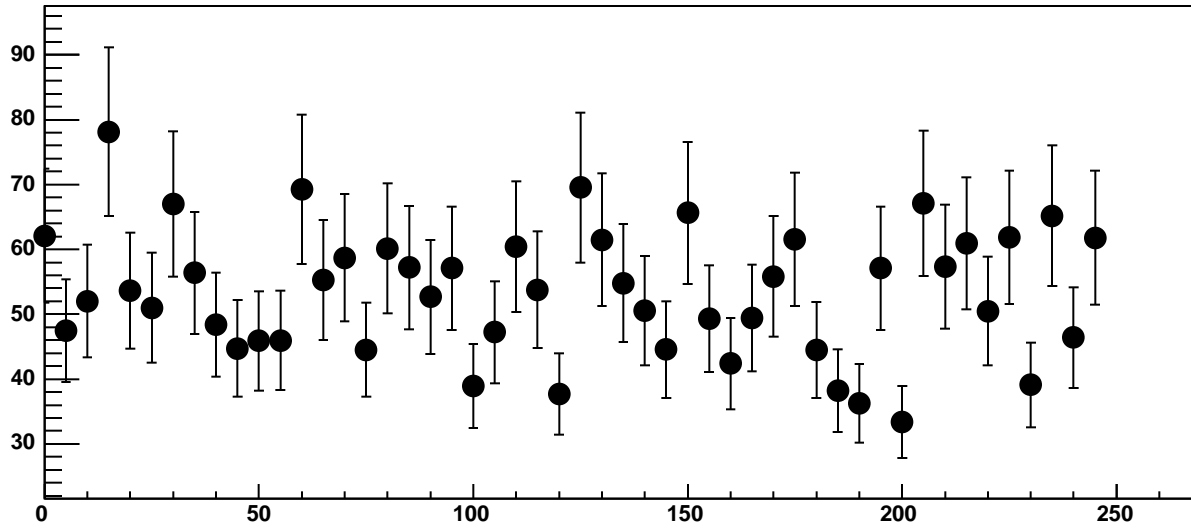
Chip 6, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



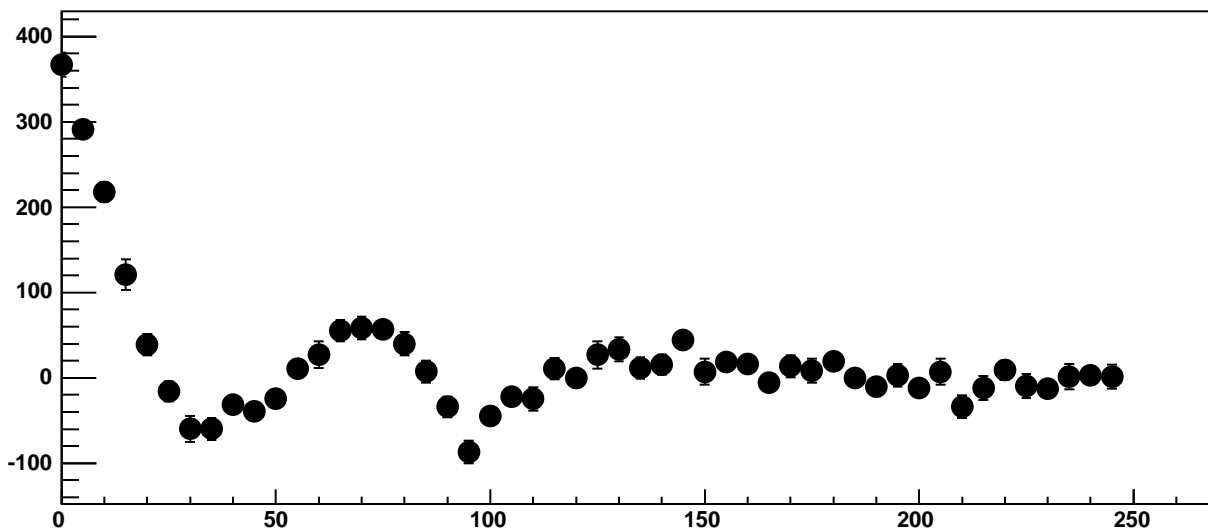
Chip 6, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



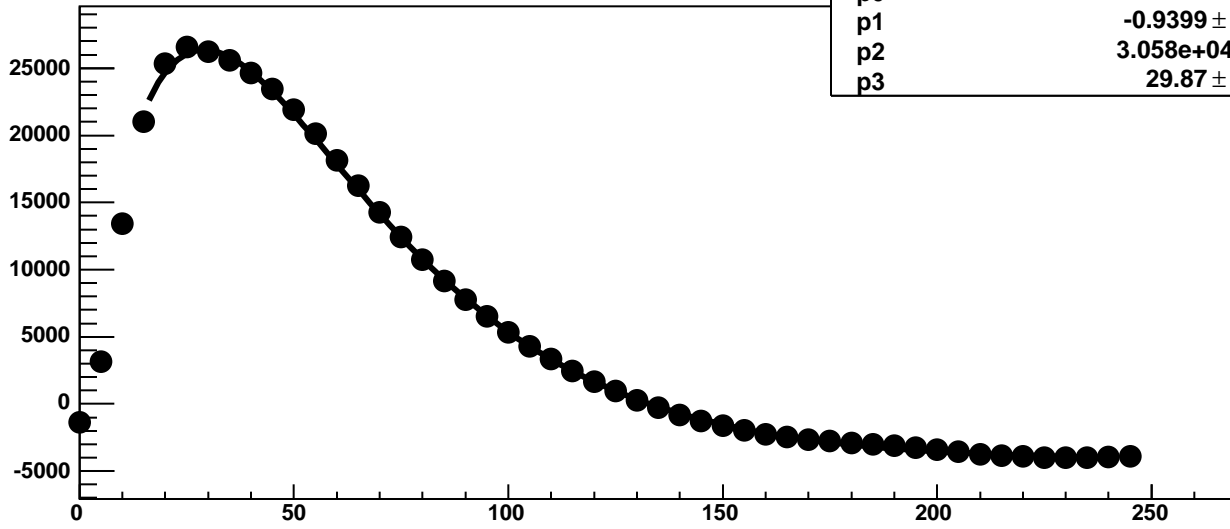
Chip 6, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

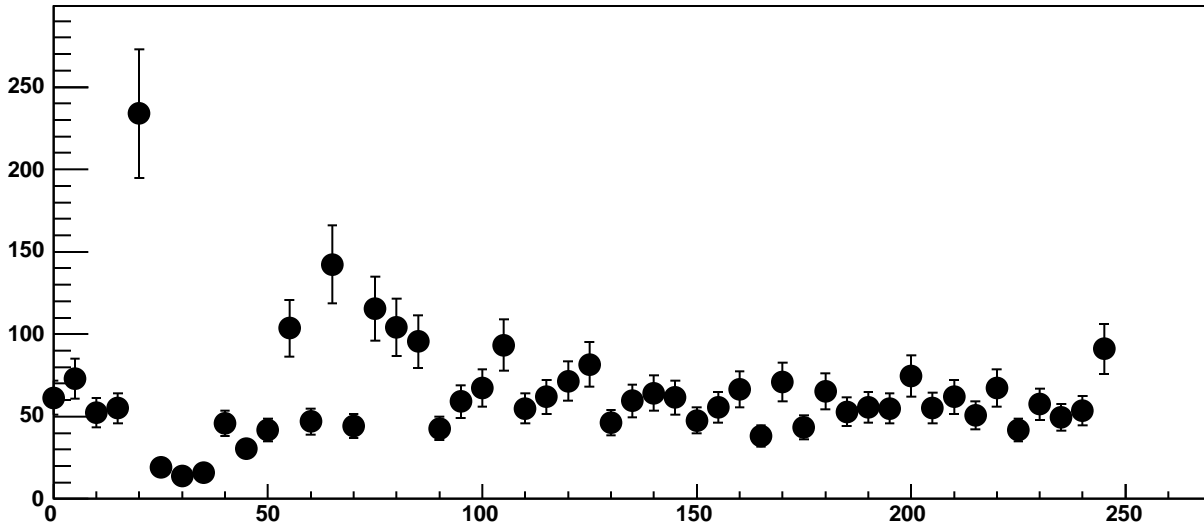


Chip 6, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold

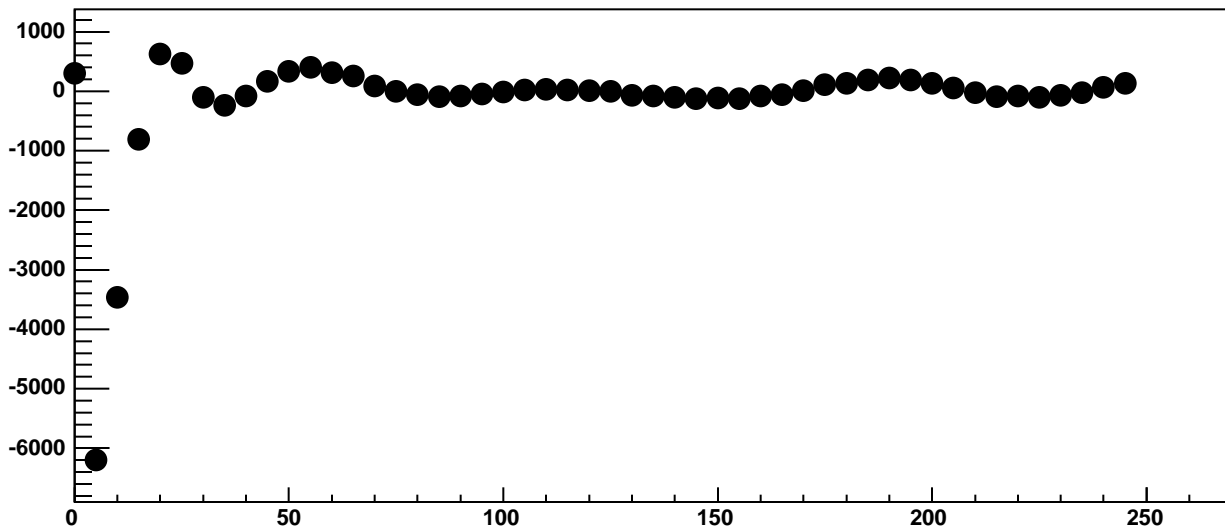


$\chi^2 / \text{ndf}$	2.603e+04 / 42
p0	-4208 ± 3.536
p1	-0.9399 ± 0.01688
p2	3.058e+04 ± 3.829
p3	29.87 ± 0.01052

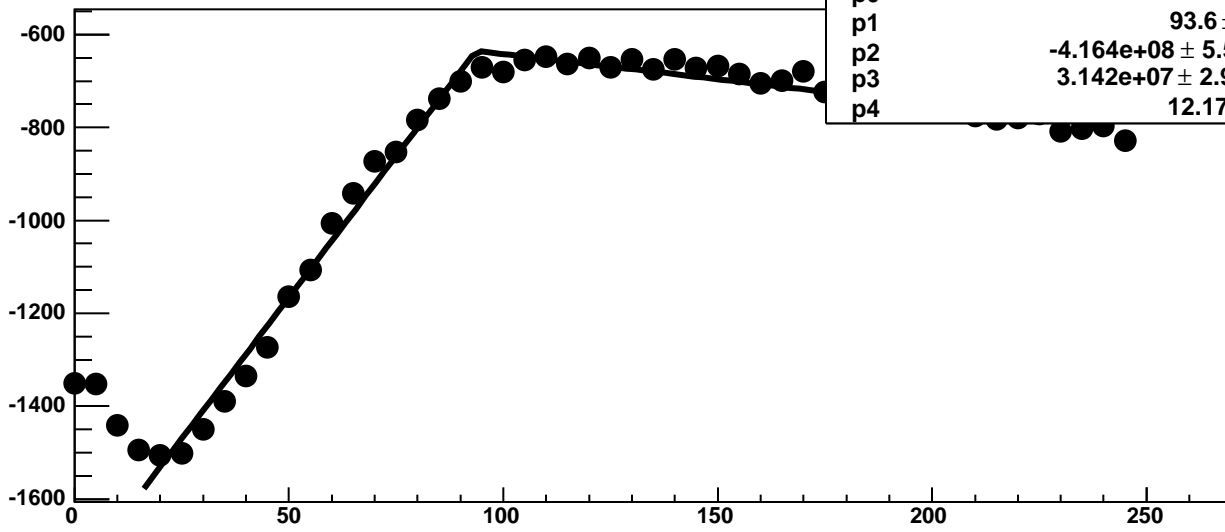
Chip 6, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold

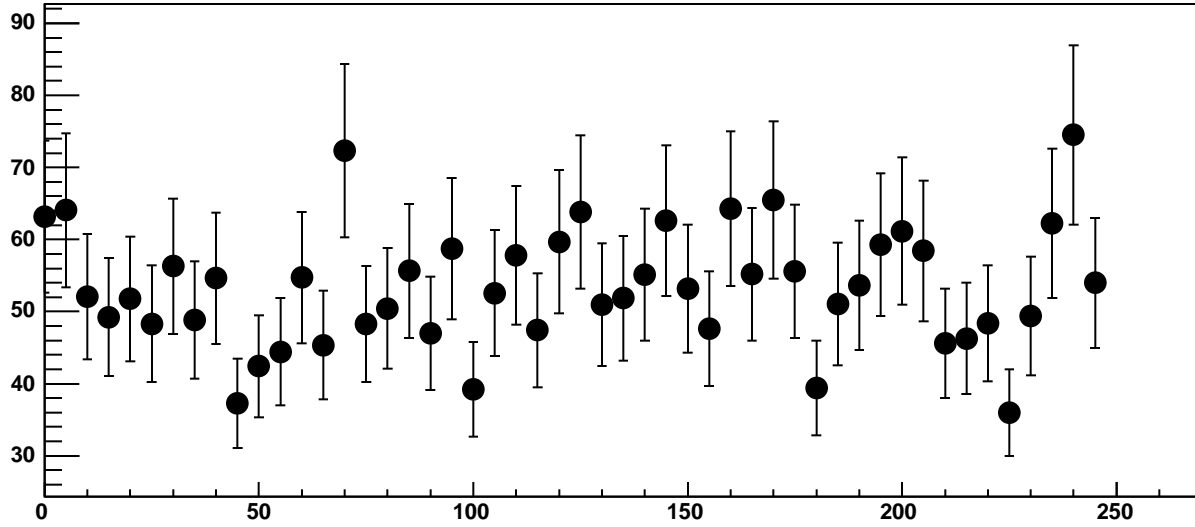


Chip 6, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

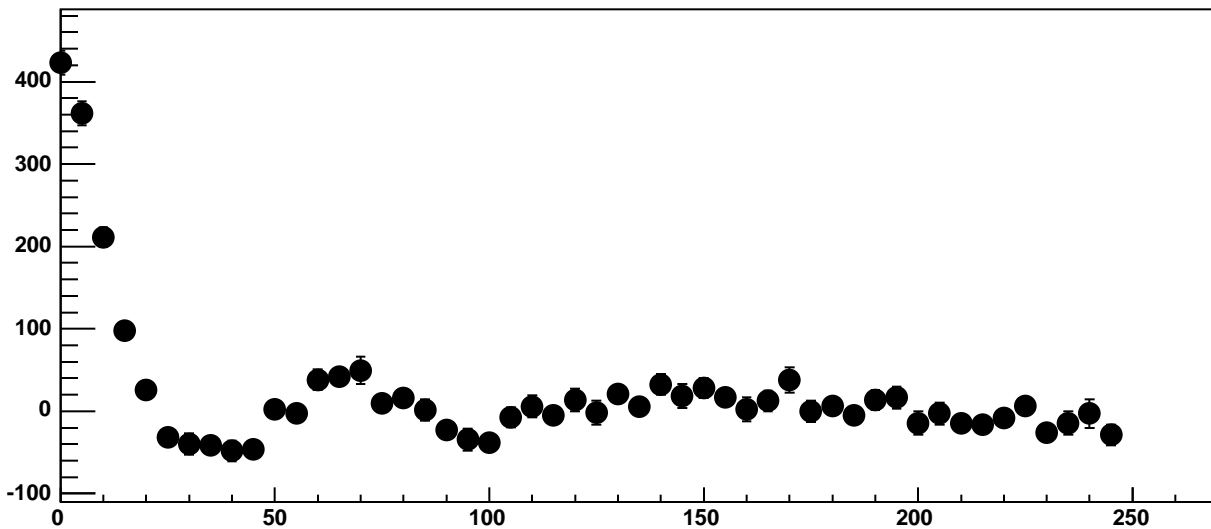


$\chi^2 / \text{ndf}$	265.1 / 41
p0	$-635 \pm 3.99$
p1	$93.6 \pm 0.5517$
p2	$-4.164e+08 \pm 5.569e+06$
p3	$3.142e+07 \pm 2.908e+05$
p4	$12.17 \pm 0.125$

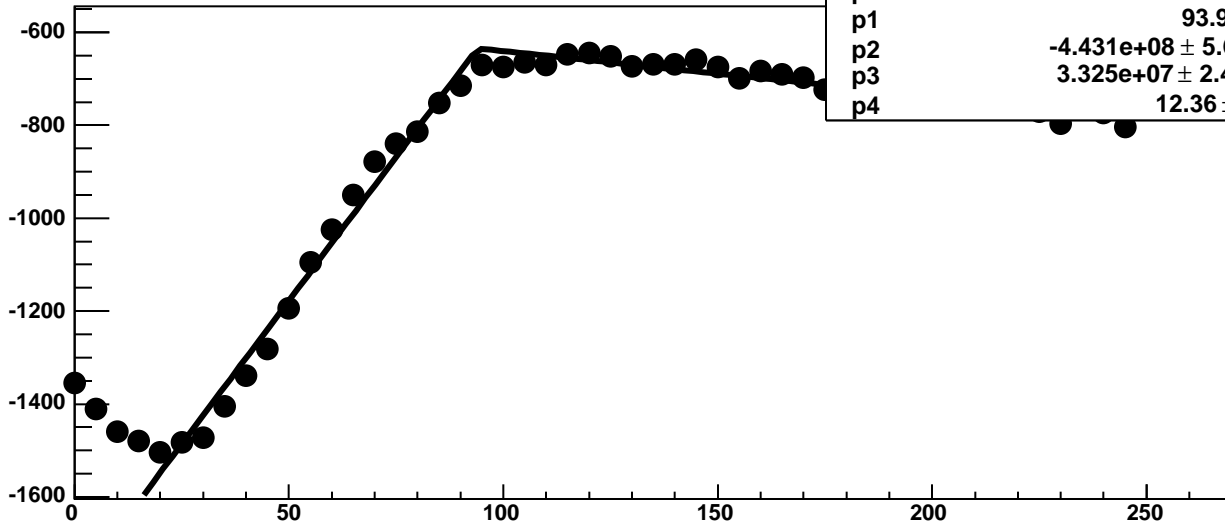
Chip 6, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

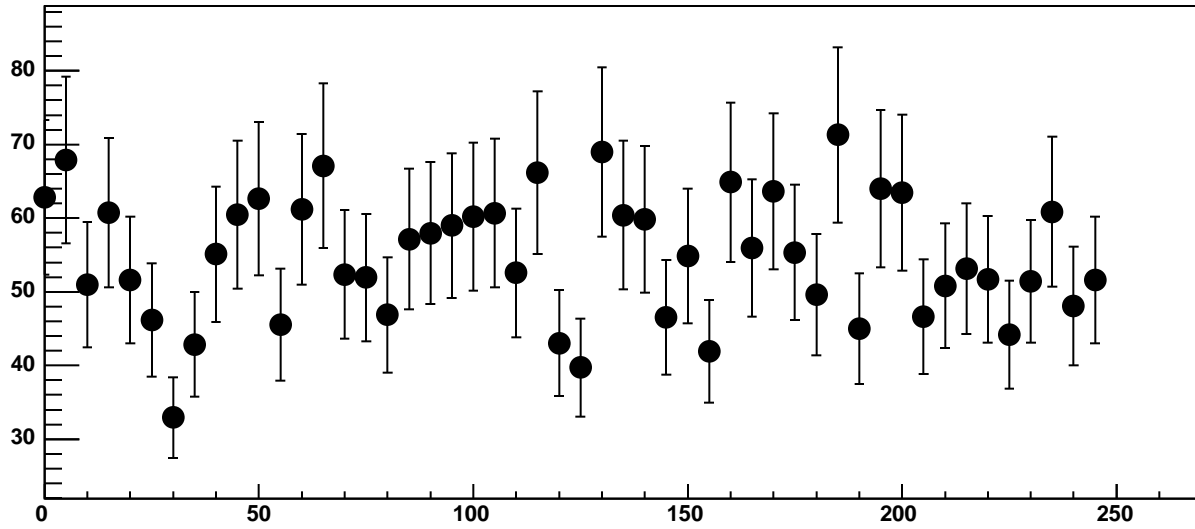


Chip 6, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

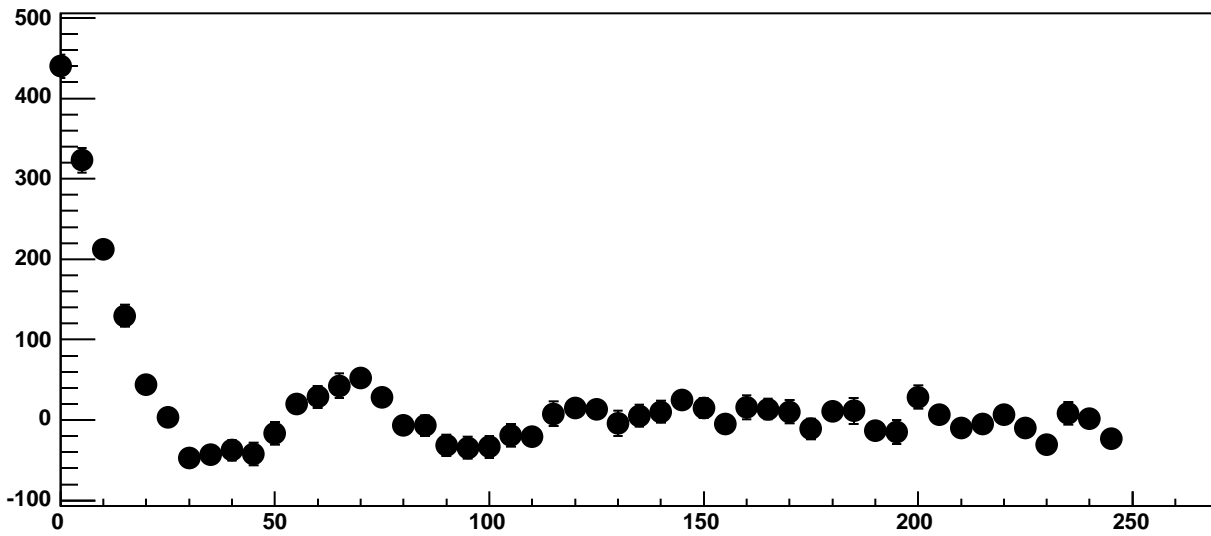


$\chi^2 / \text{ndf}$	276.3 / 41
p0	-634.6 ± 4.168
p1	93.9 ± 0.584
p2	-4.431e+08 ± 5.637e+06
p3	3.325e+07 ± 2.425e+05
p4	12.36 ± 0.1279

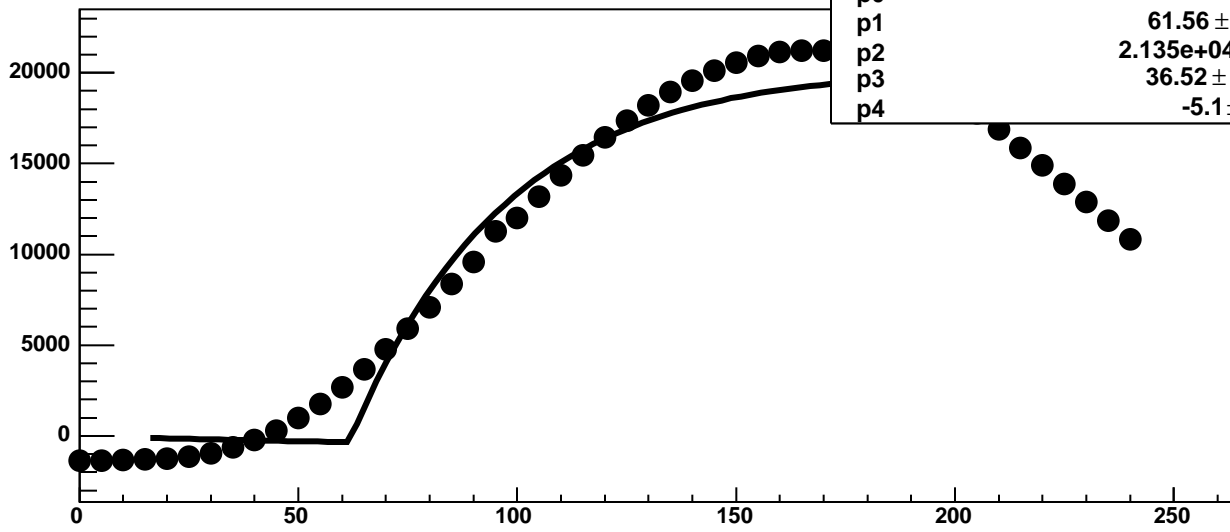
Chip 6, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

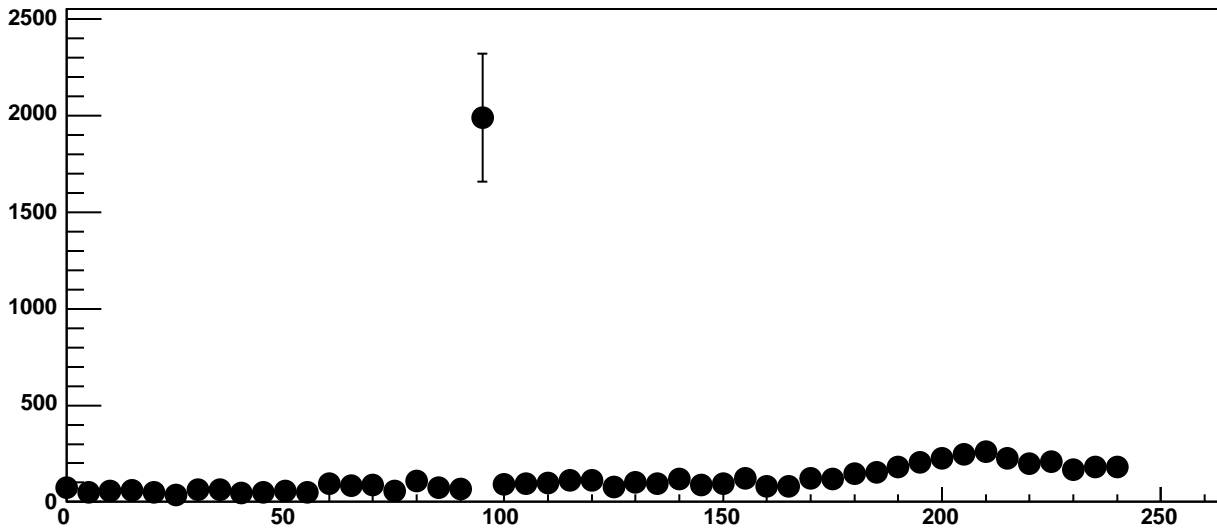


Chip 6, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold

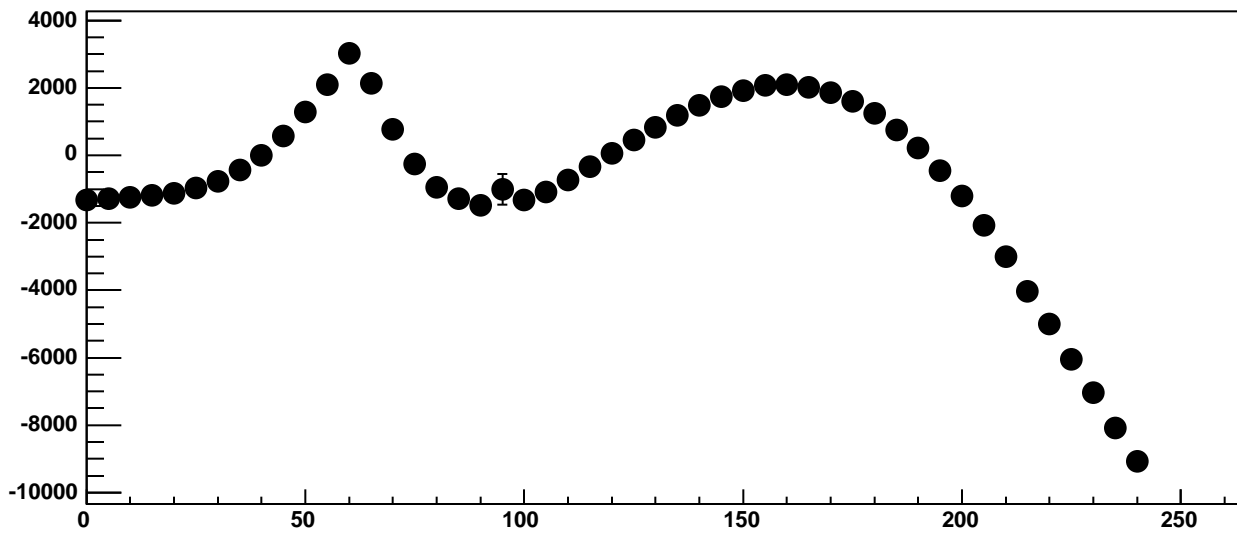


$\chi^2 / \text{ndf}$	3.621e+05 / 41
p0	-353.4 ± 6.409
p1	61.56 ± 0.02791
p2	2.135e+04 ± 33.61
p3	36.52 ± 0.07135
p4	-5.1 ± 0.1993

Chip 6, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

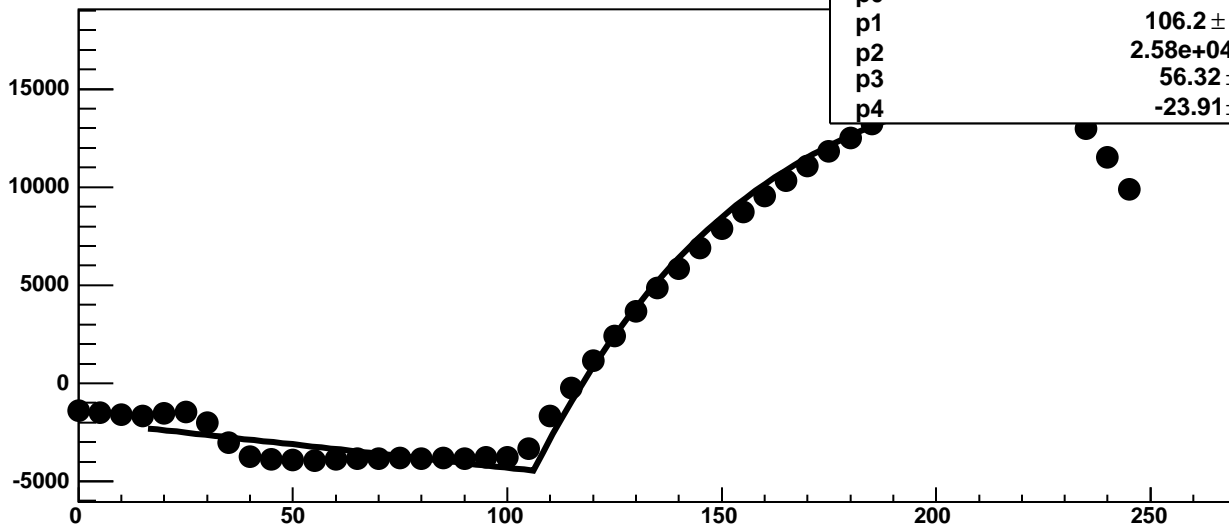


Chip 6, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold

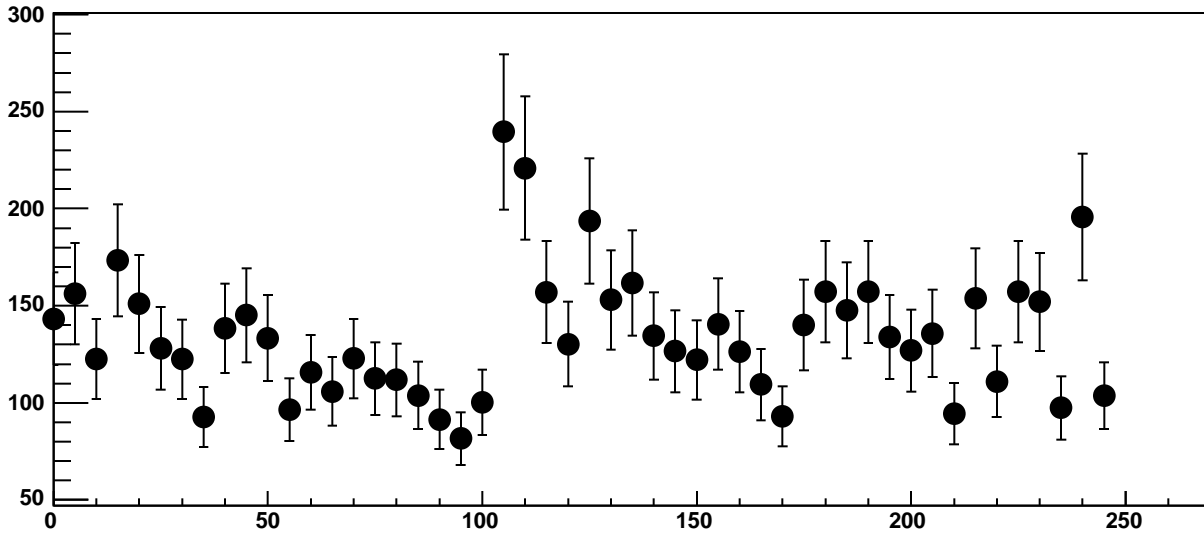




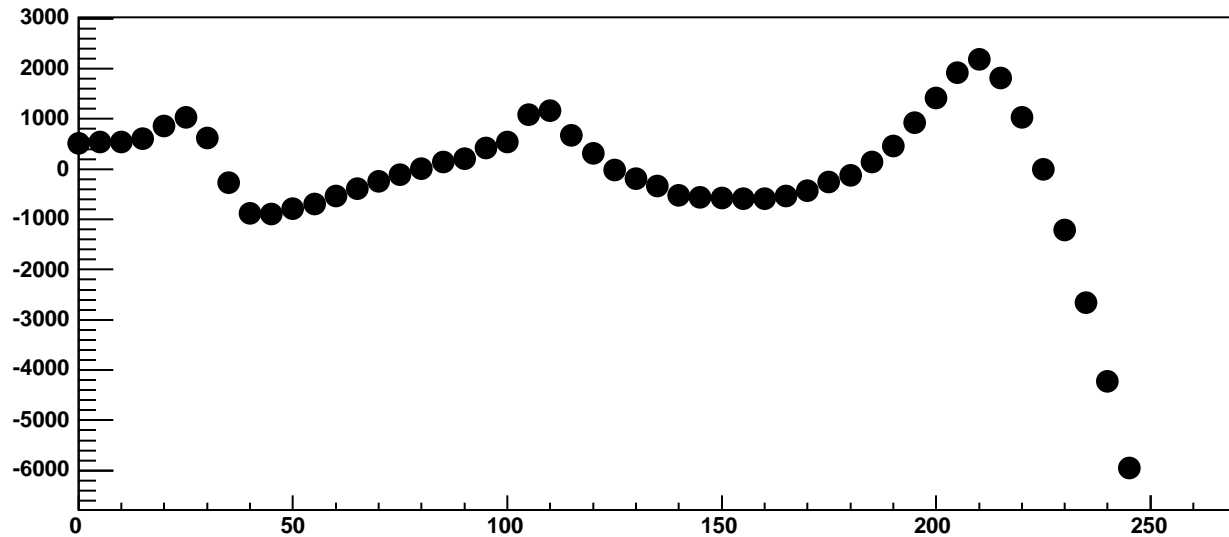
Chip 6, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold



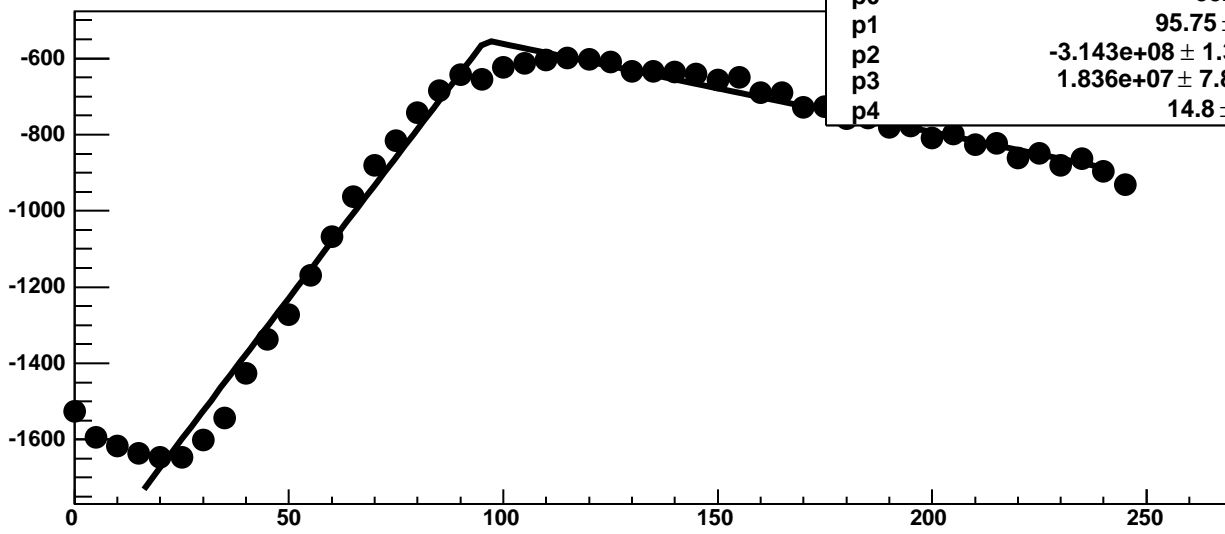
Chip 6, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

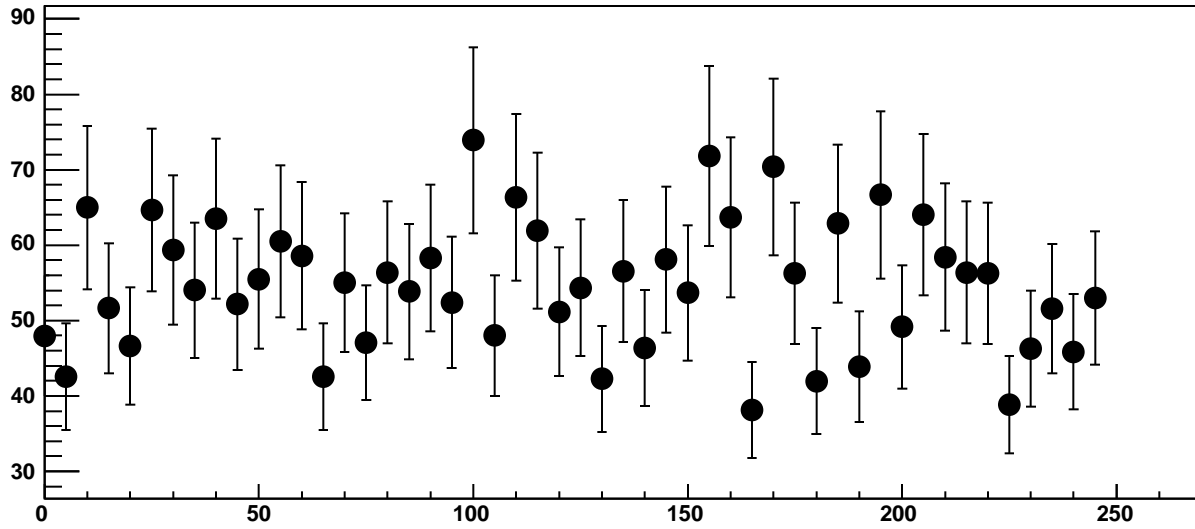


Chip 6, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

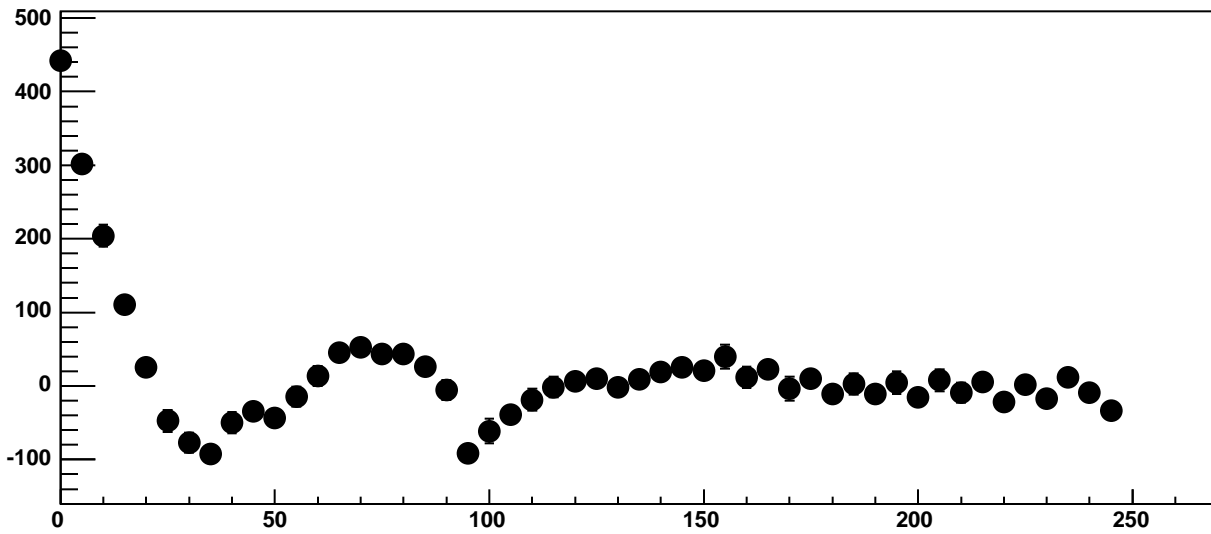


$\chi^2 / \text{ndf}$	417.8 / 41
p0	-552 ± 4.14
p1	95.75 ± 0.4329
p2	-3.143e+08 ± 1.364e+07
p3	1.836e+07 ± 7.857e+05
p4	14.8 ± 0.1214

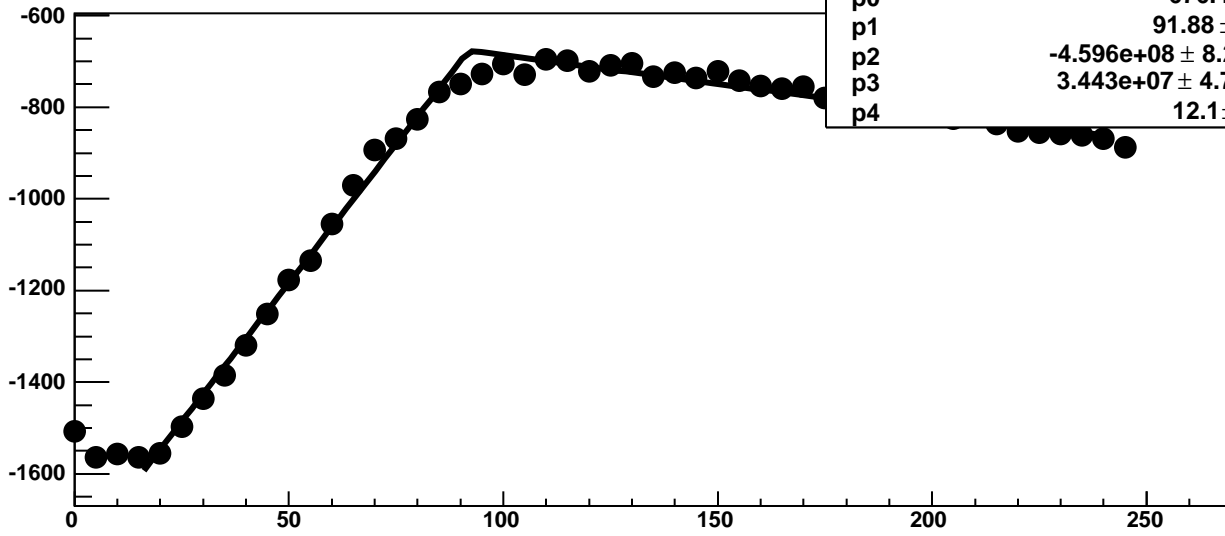
Chip 6, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

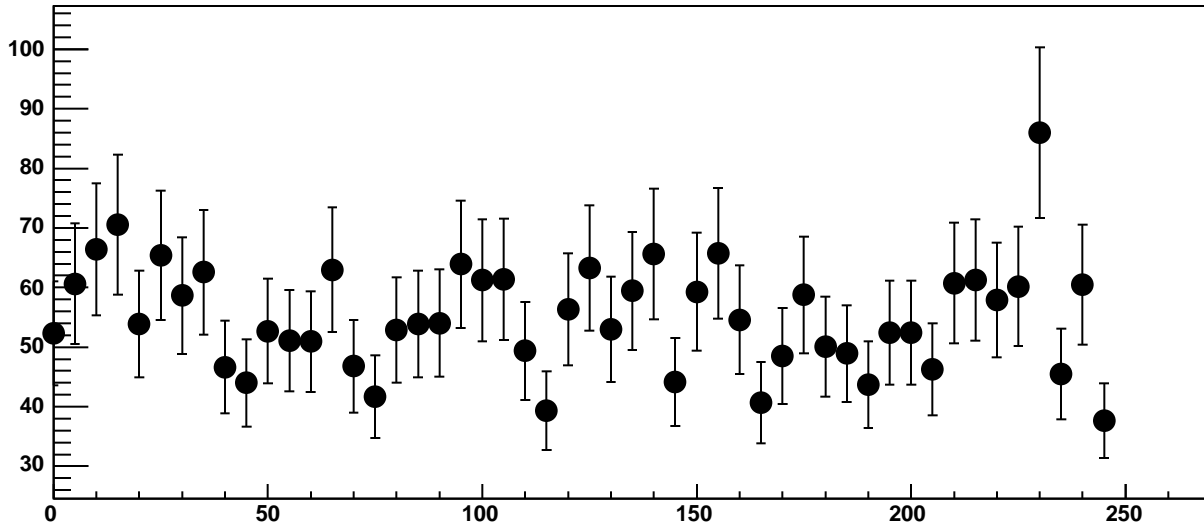


Chip 6, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold

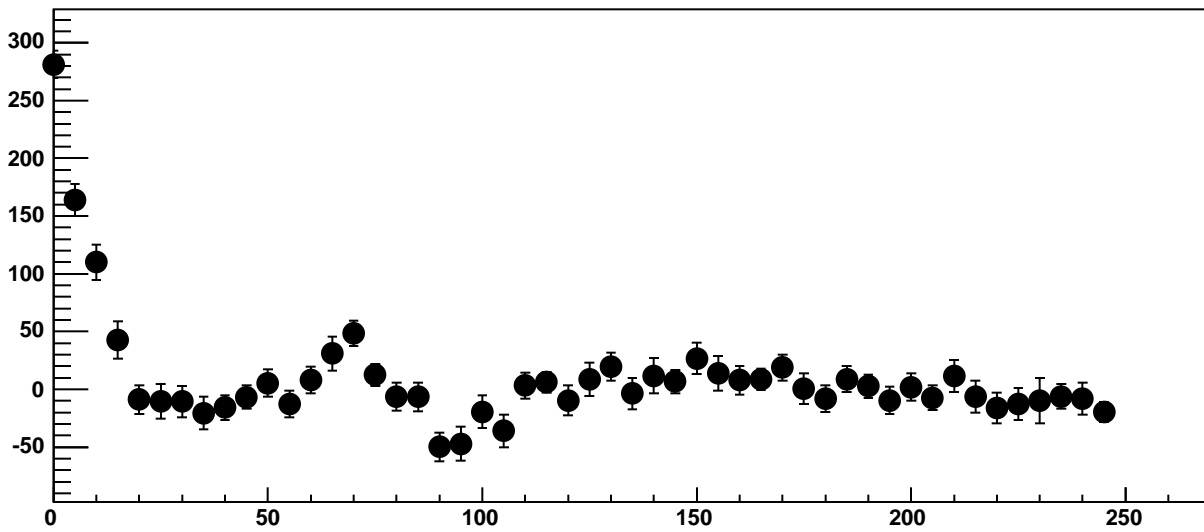


$\chi^2 / \text{ndf}$	97.57 / 41
p0	$-676.4 \pm 4.242$
p1	$91.88 \pm 0.5635$
p2	$-4.596\text{e}+08 \pm 8.213\text{e}+06$
p3	$3.443\text{e}+07 \pm 4.794\text{e}+05$
p4	$12.1 \pm 0.1389$

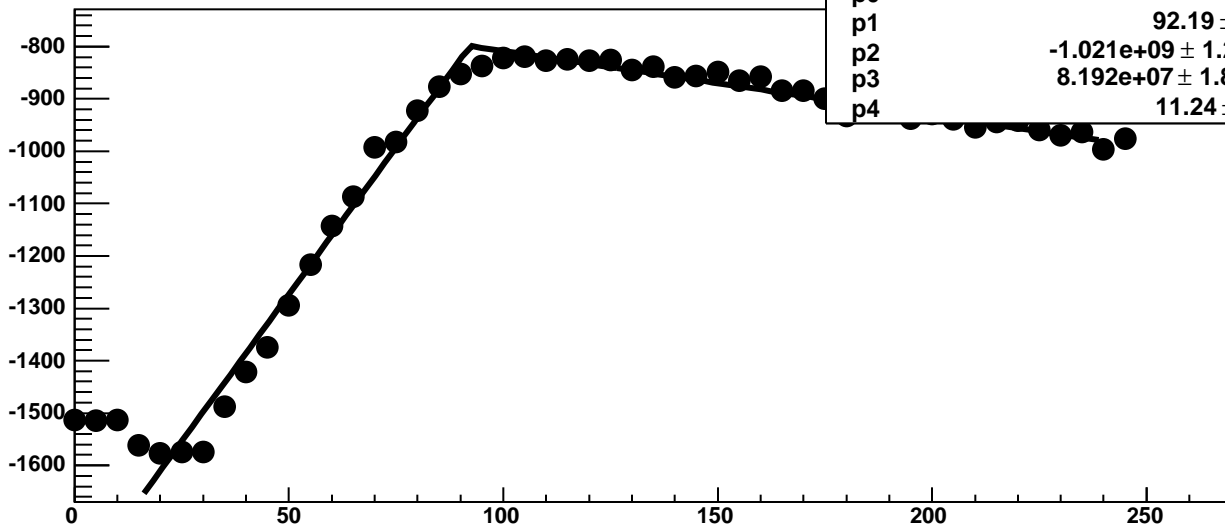
Chip 6, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold

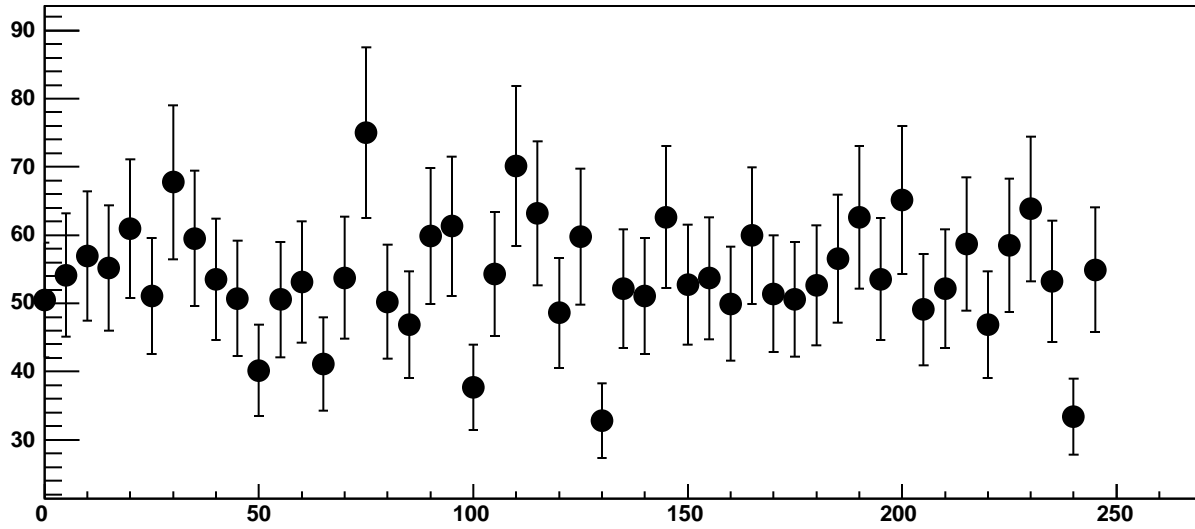


Chip 6, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

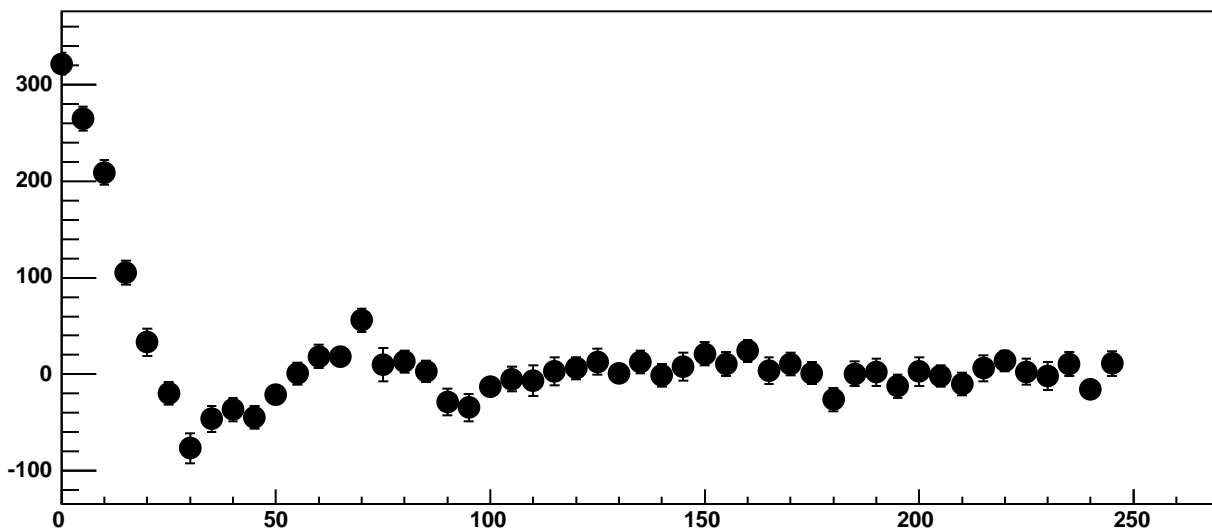


$\chi^2 / \text{ndf}$	208.8 / 41
p0	$-798.9 \pm 3.852$
p1	$92.19 \pm 0.5934$
p2	$-1.021\text{e}+09 \pm 1.207\text{e}+07$
p3	$8.192\text{e}+07 \pm 1.818\text{e}+05$
p4	$11.24 \pm 0.1372$

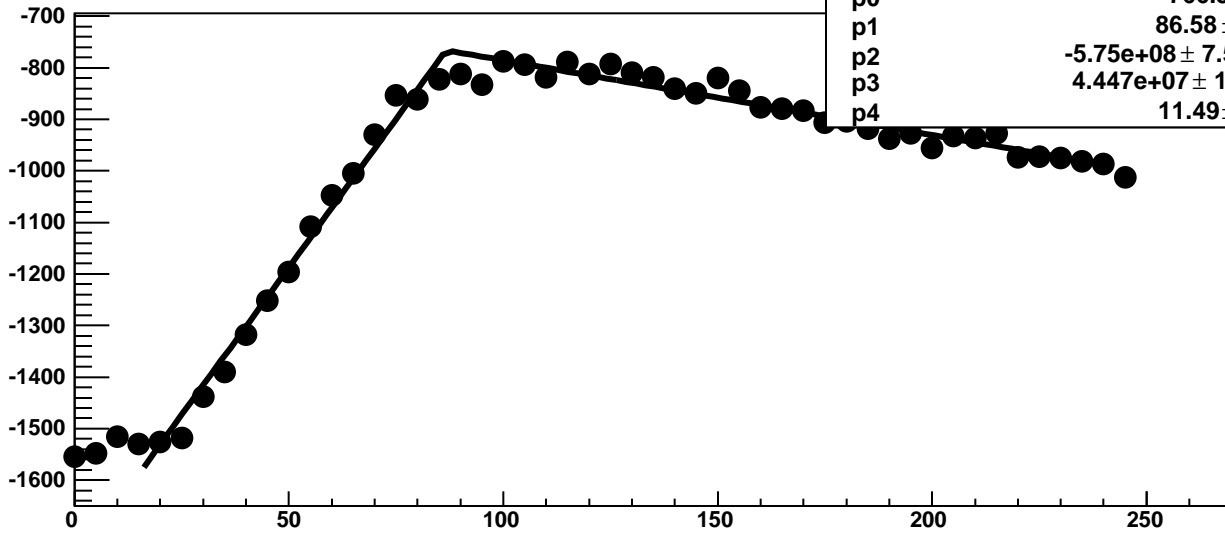
Chip 6, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

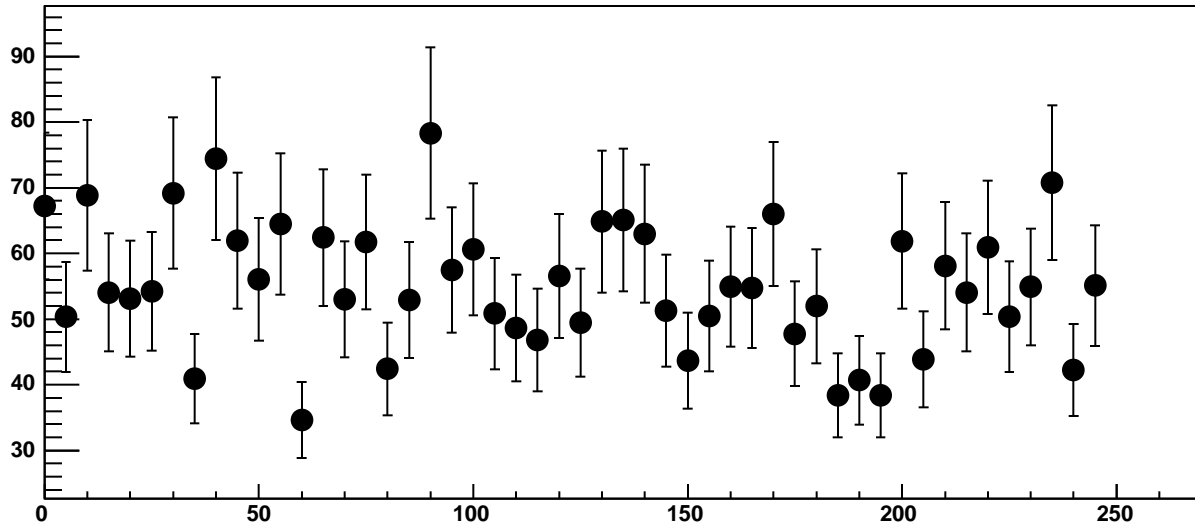


Chip 6, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

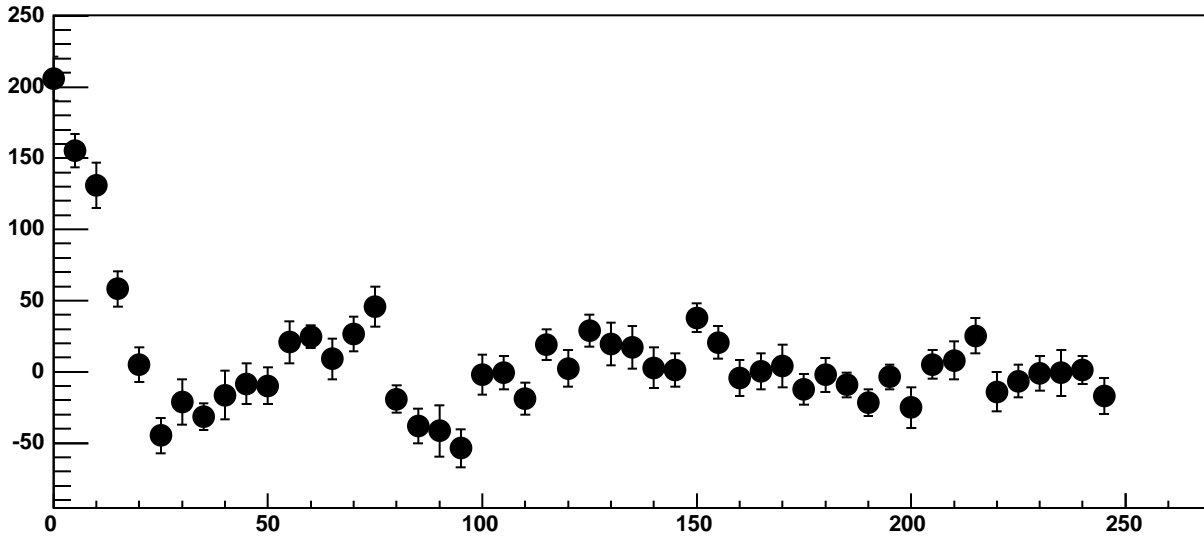


$\chi^2 / \text{ndf}$	163.4 / 41
p0	-766.3 ± 5.028
p1	86.58 ± 0.3618
p2	-5.75e+08 ± 7.503e+06
p3	4.447e+07 ± 1.18e+06
p4	11.49 ± 0.1307

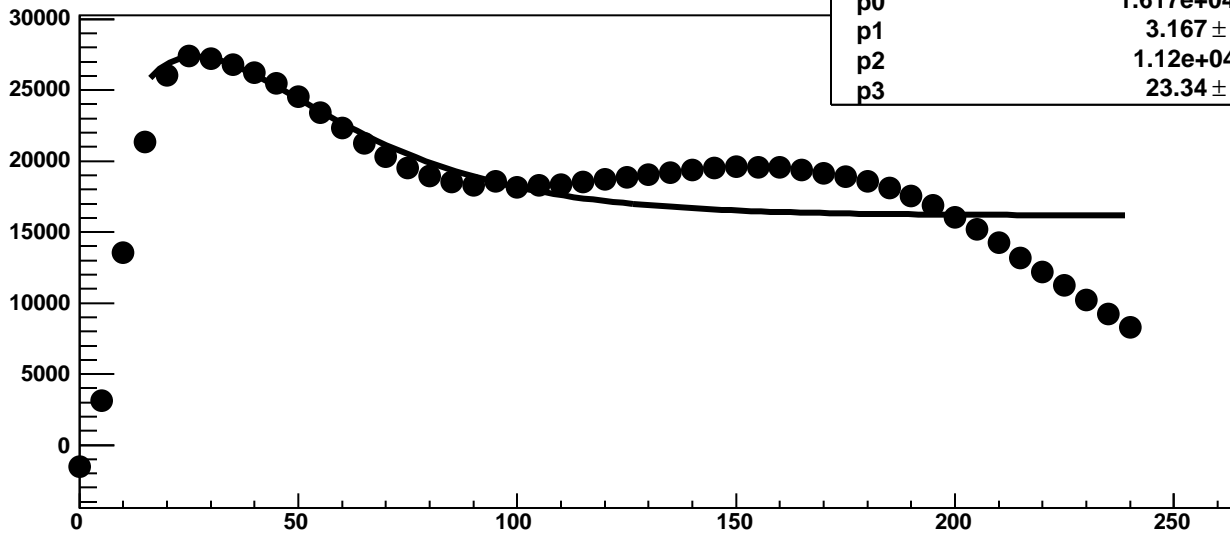
Chip 6, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

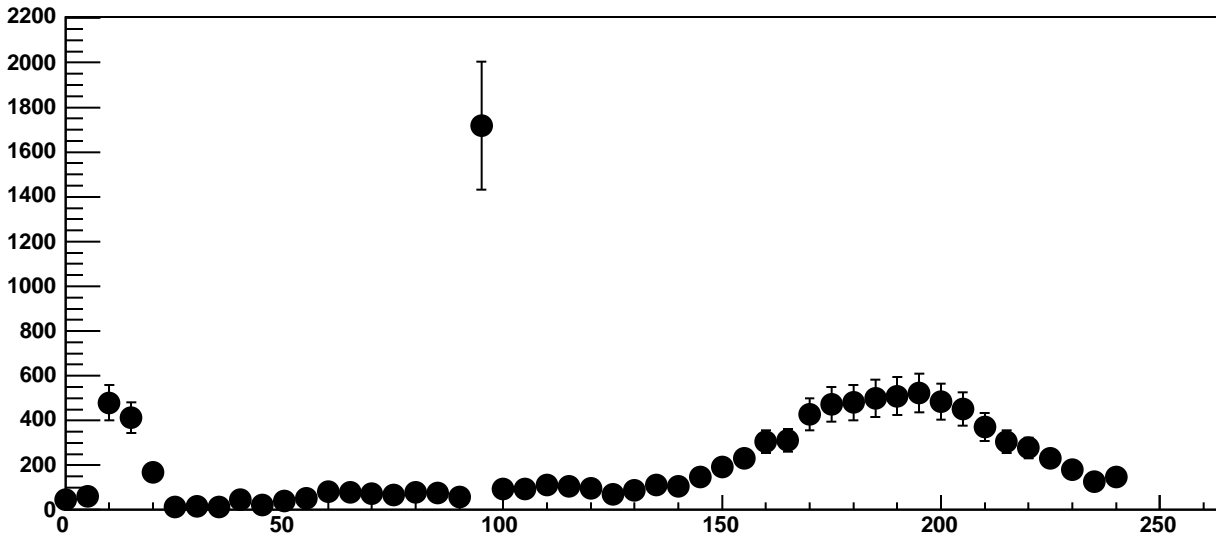


Chip 6, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold

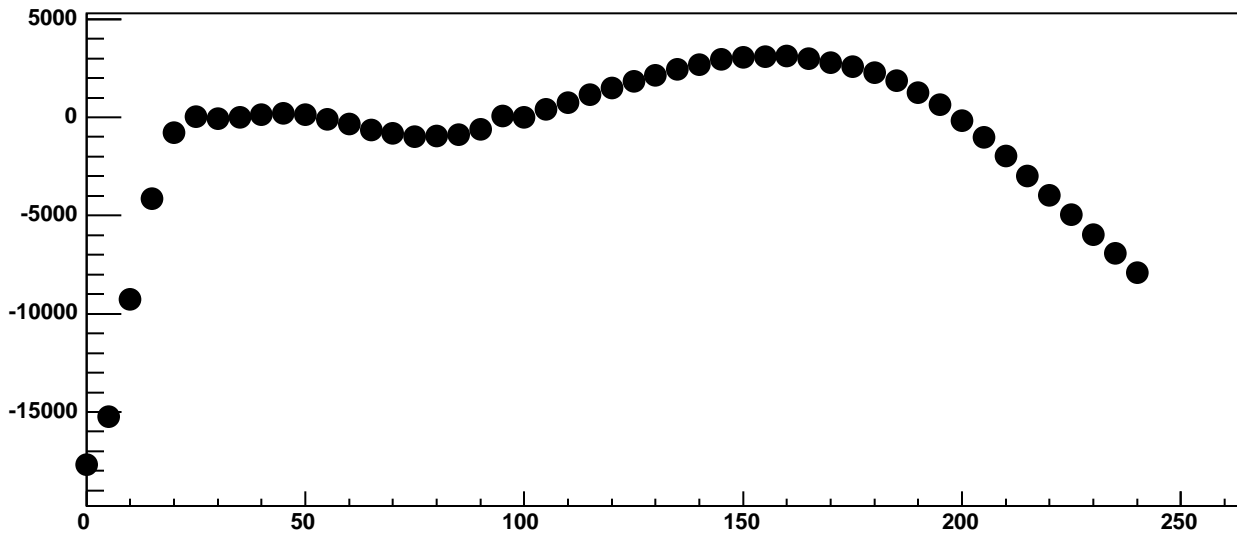


$\chi^2 / \text{ndf}$	2.441e+05 / 42
p0	1.617e+04 $\pm$ 11.59
p1	3.167 $\pm$ 0.08683
p2	1.12e+04 $\pm$ 11.82
p3	23.34 $\pm$ 0.05638

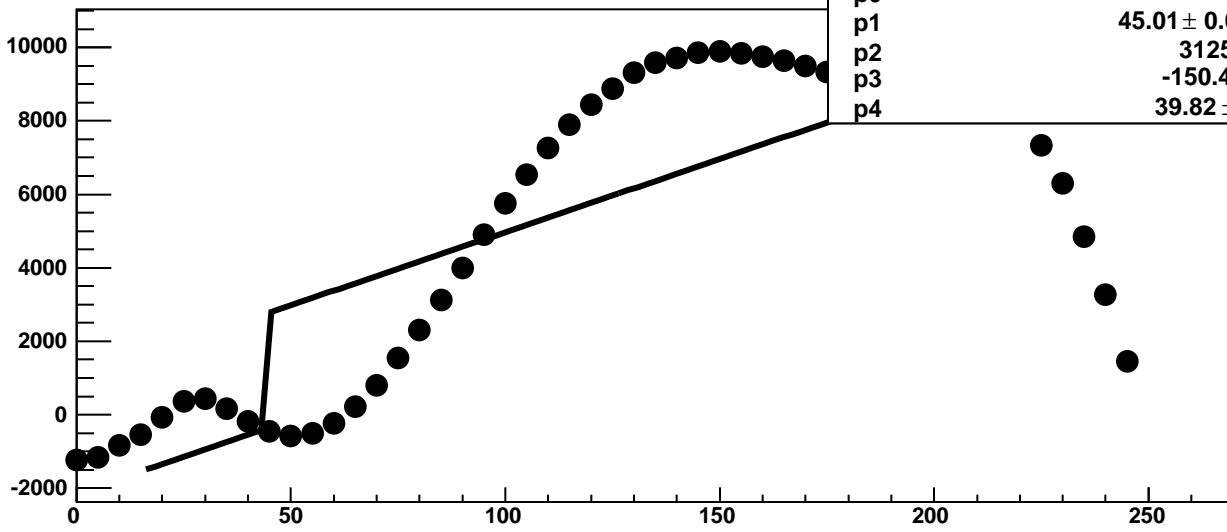
Chip 6, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



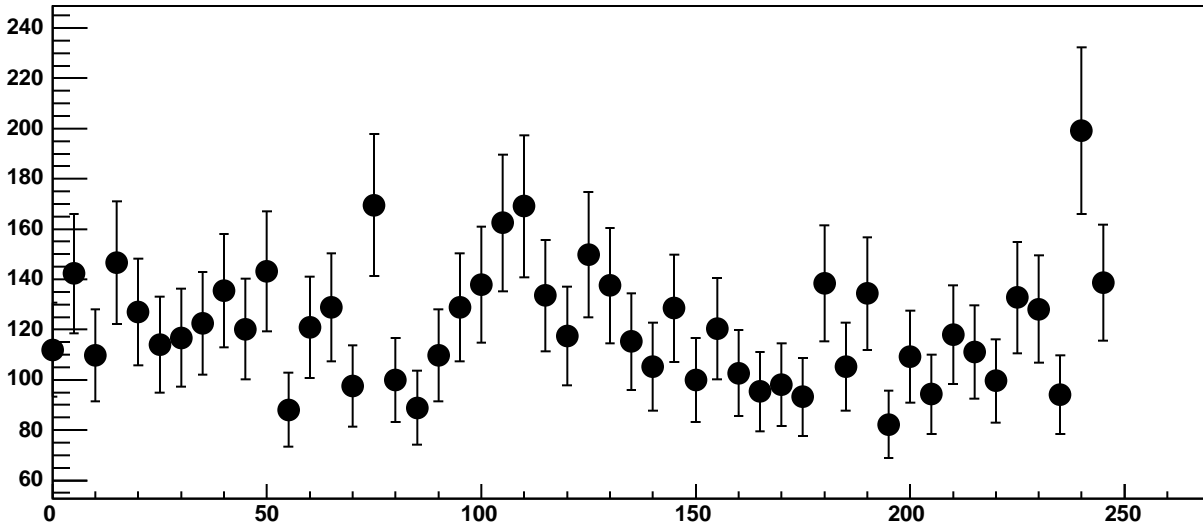
Chip 6, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold



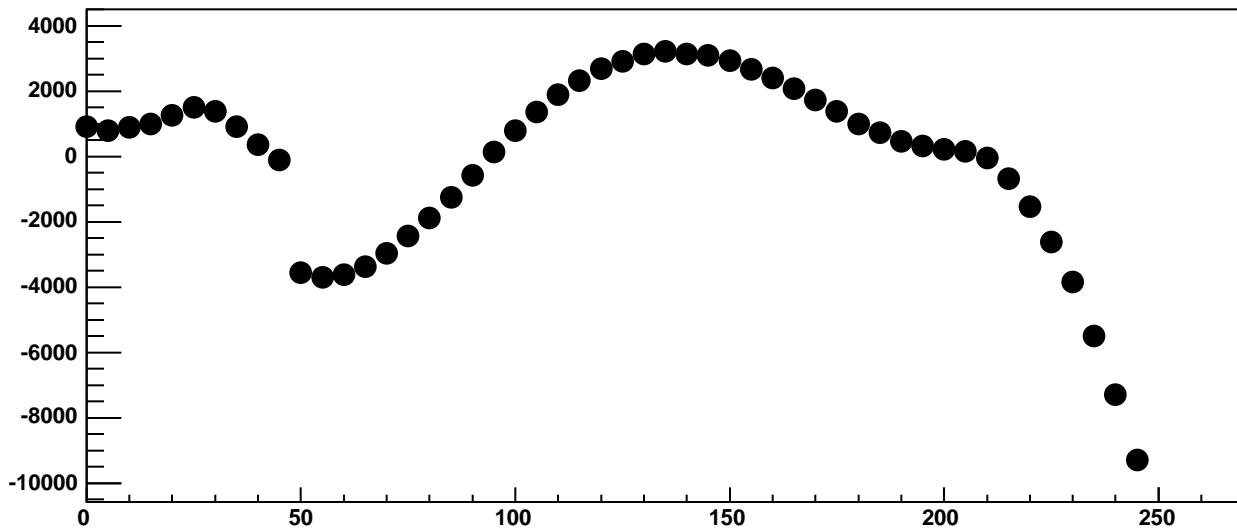
Chip 6, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold



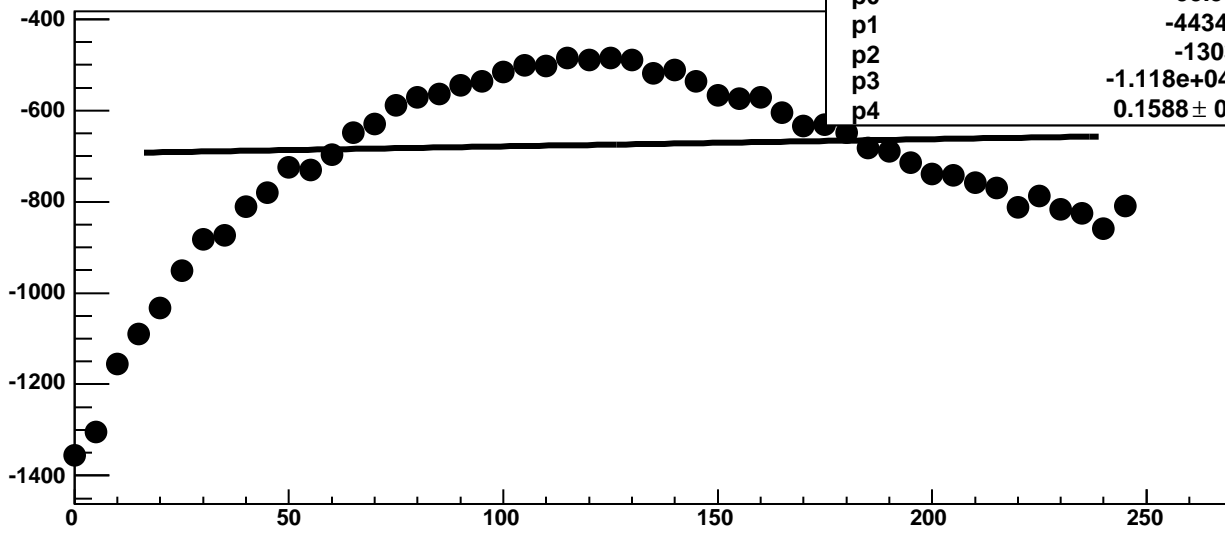
Chip 6, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

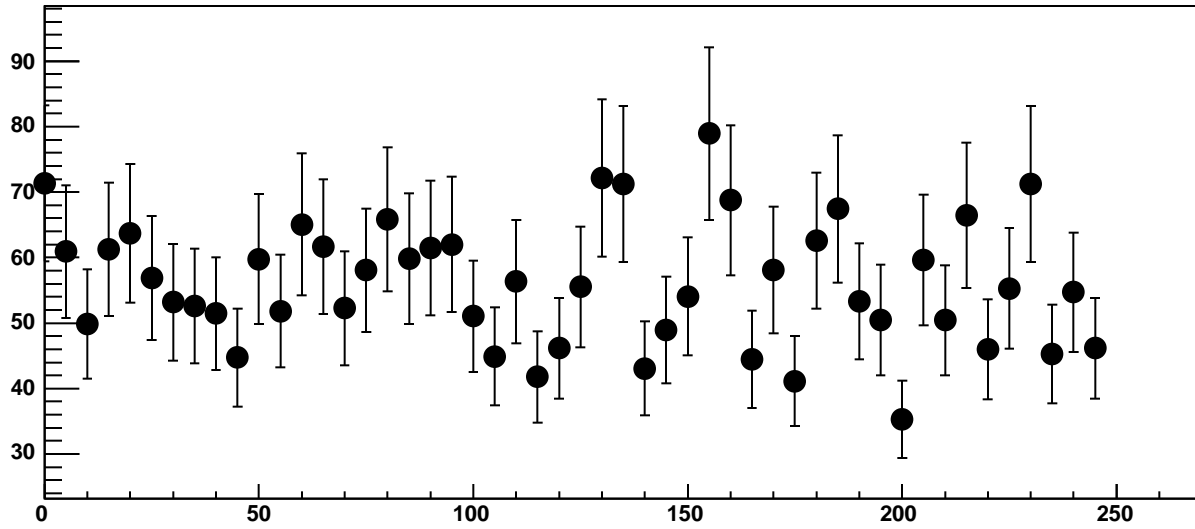


Chip 6, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

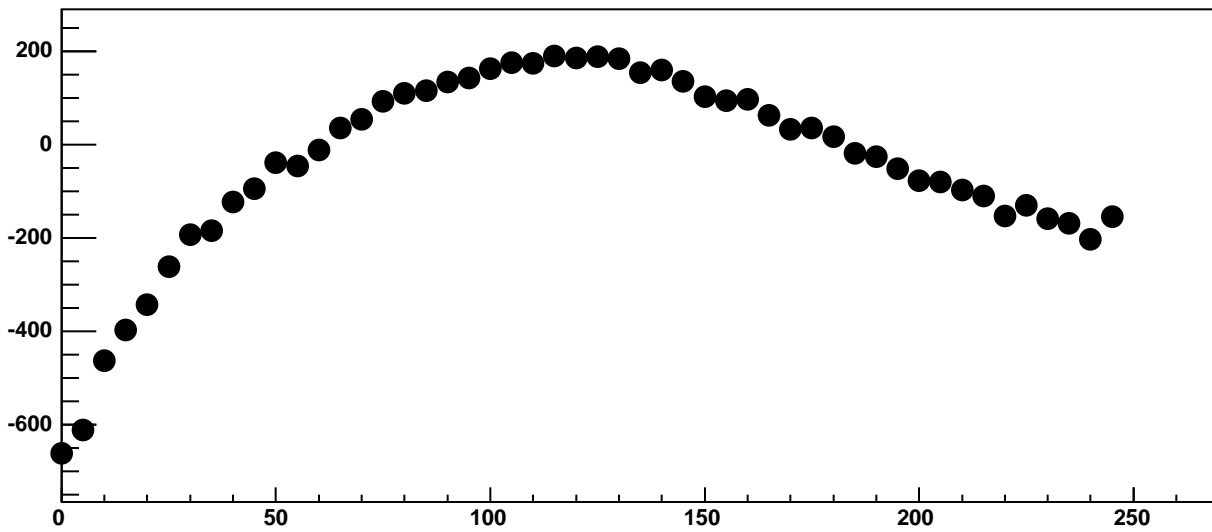


$\chi^2 / \text{ndf}$	6459 / 41
p0	$-95.53 \pm 12.4$
p1	$-4434 \pm 18.49$
p2	$-1303 \pm 8.43$
p3	$-1.118e+04 \pm 607.9$
p4	$0.1588 \pm 0.002715$

Chip 6, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

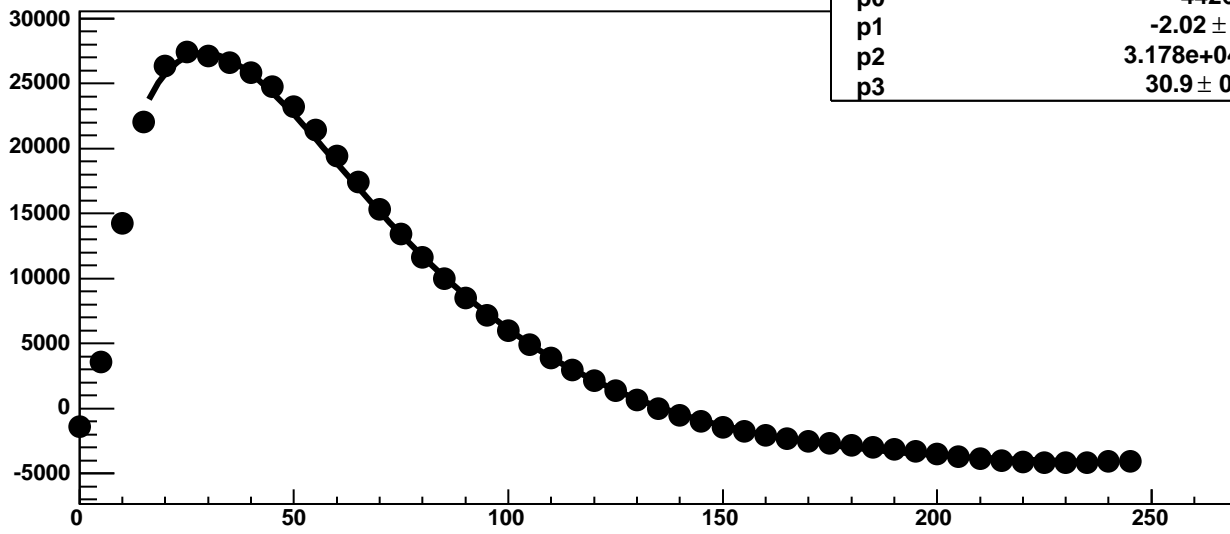


Chip 6, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



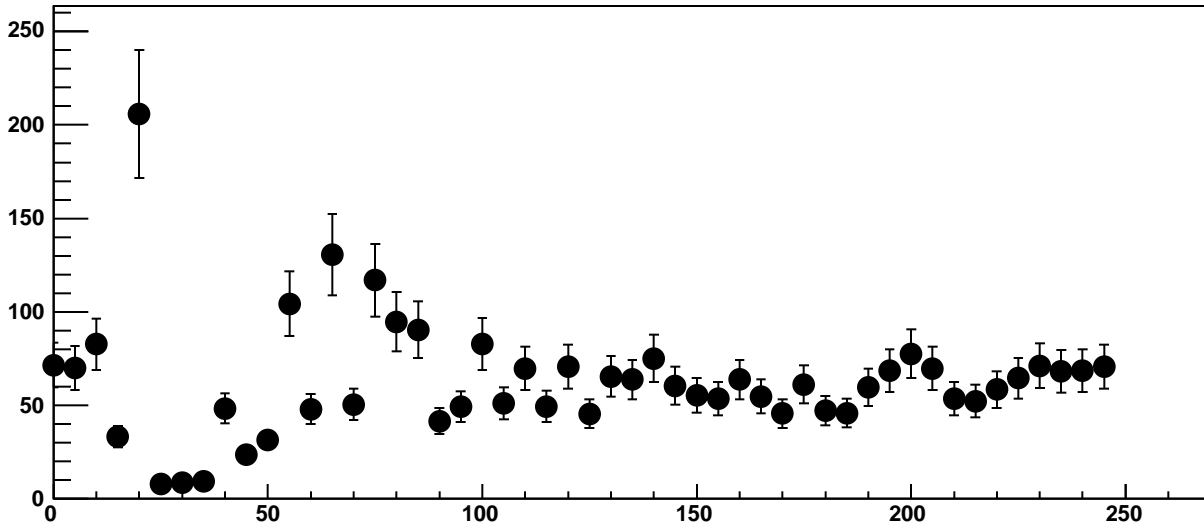


Chip 6, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold

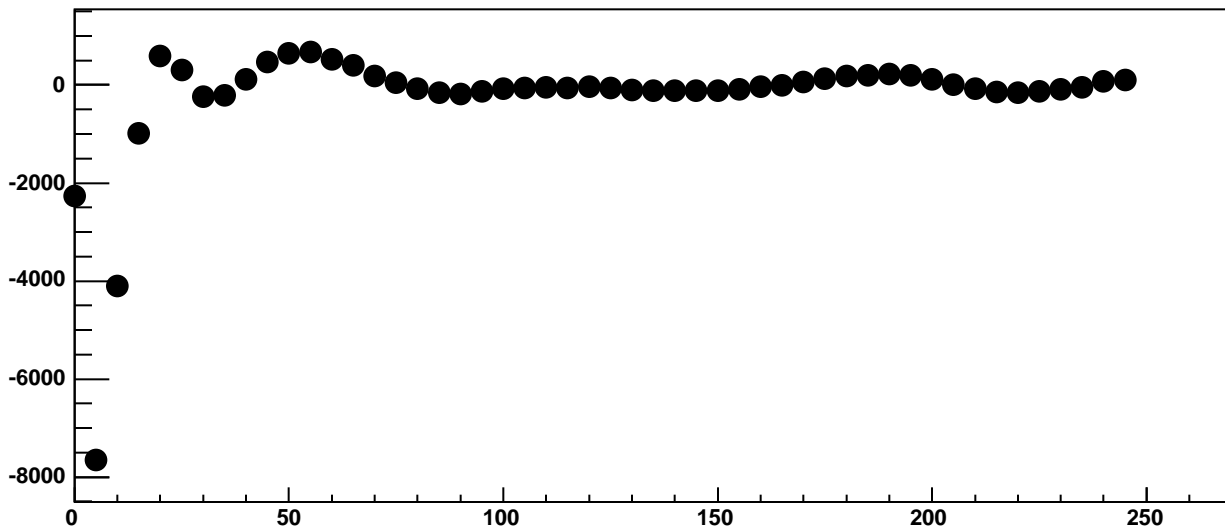


$\chi^2 / \text{ndf}$	9.106e+04 / 42
p0	-4426 ± 3.951
p1	-2.02 ± 0.01216
p2	3.178e+04 ± 3.93
p3	30.9 ± 0.009337

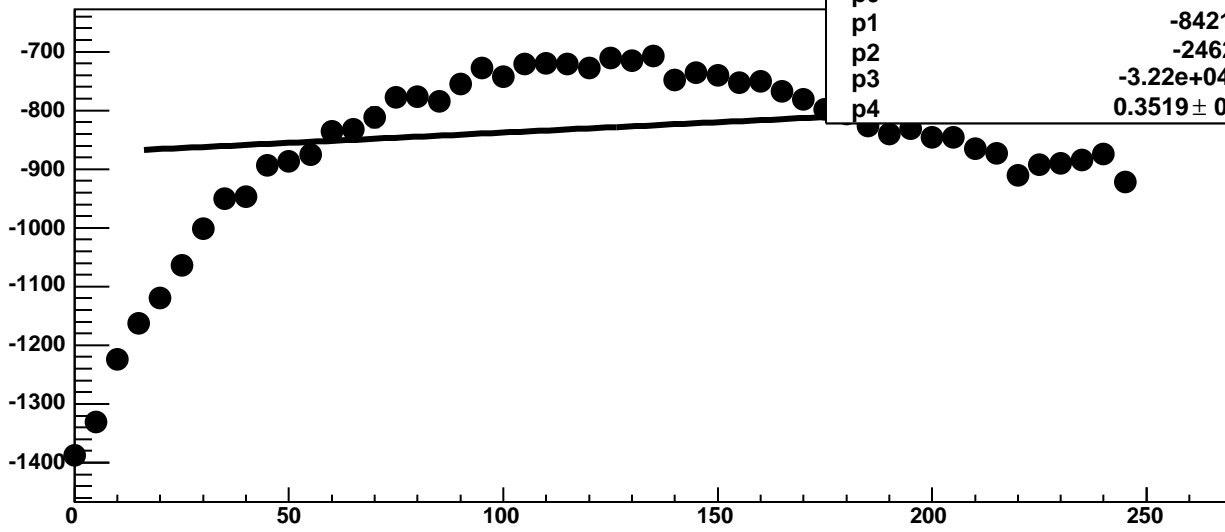
Chip 6, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold

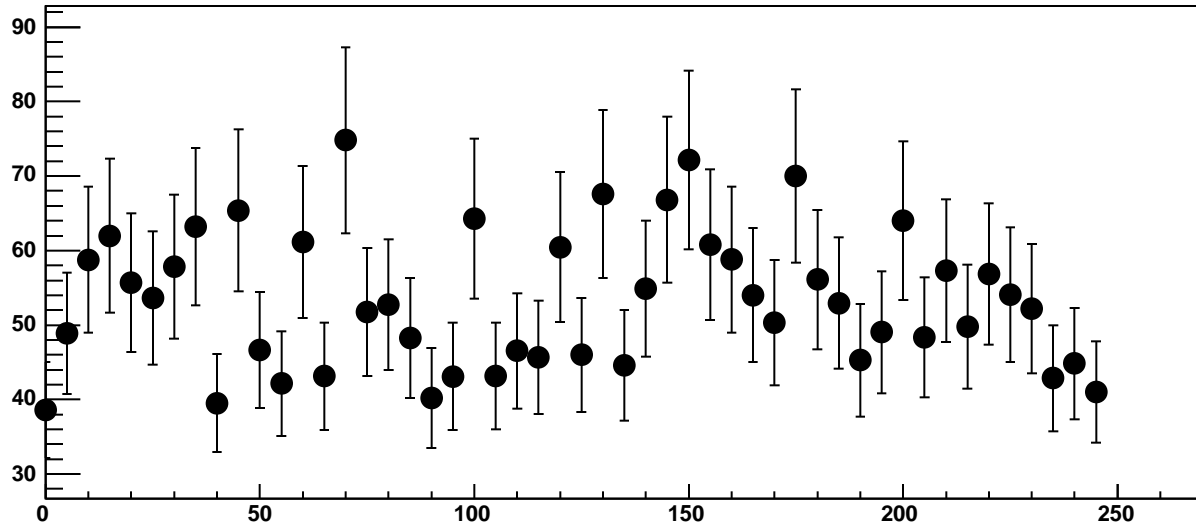


Chip 6, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

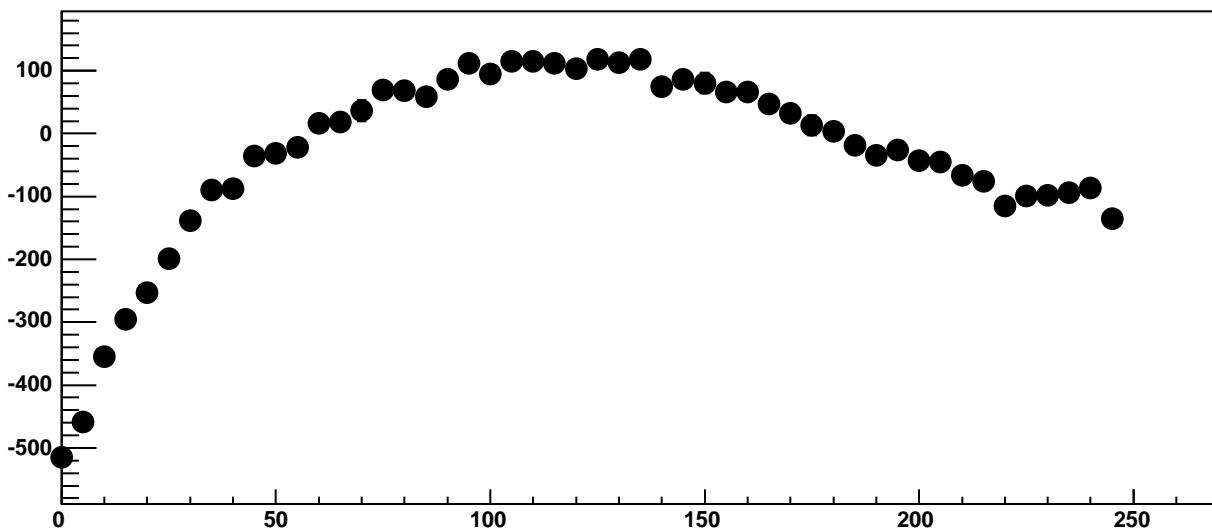


$\chi^2 / \text{ndf}$	3083 / 41
p0	$-1375 \pm 8.77$
p1	$-8421 \pm 21.82$
p2	$-2462 \pm 11.31$
p3	$-3.22\text{e}+04 \pm 1565$
p4	$0.3519 \pm 0.001026$

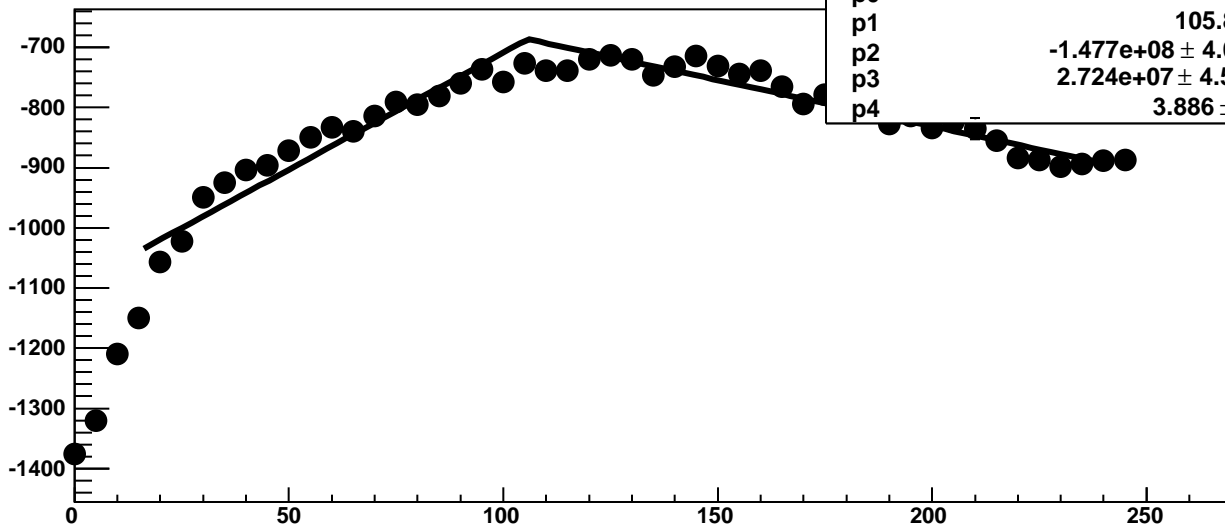
Chip 6, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

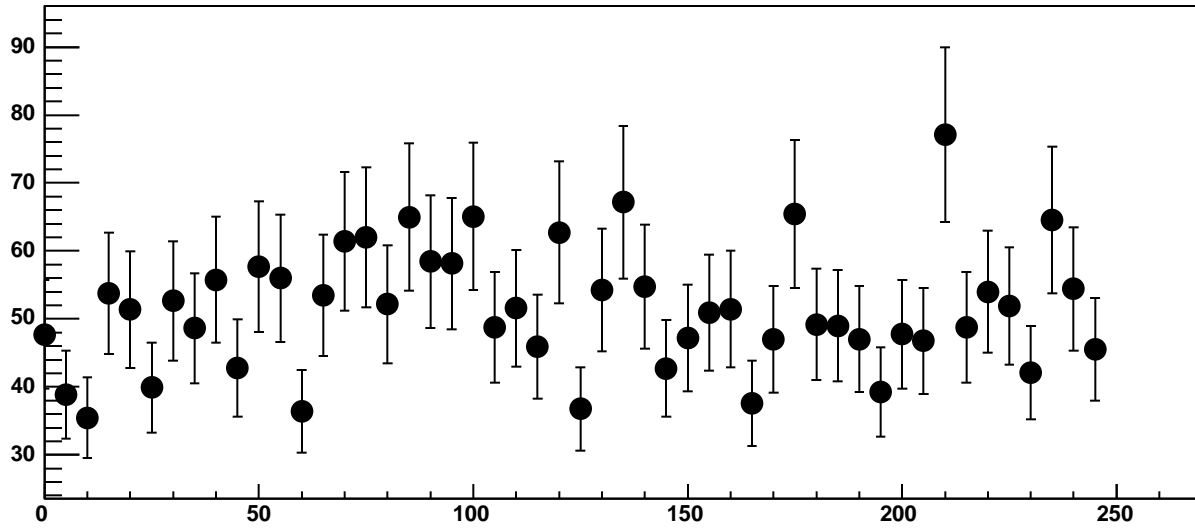


Chip 6, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

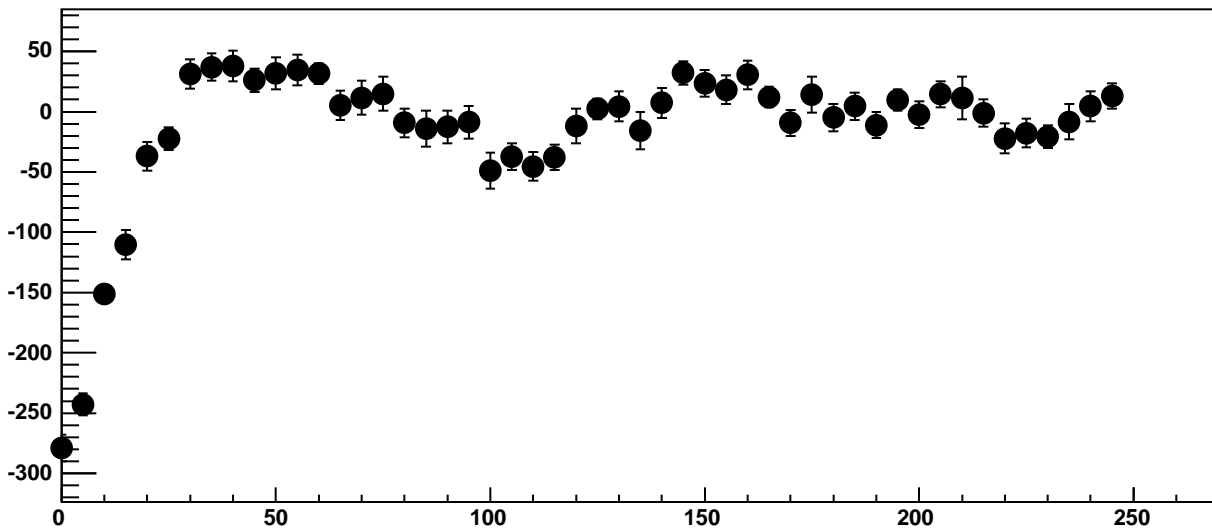


$\chi^2 / \text{ndf}$	257.1 / 41
p0	$-686.5 \pm 3.579$
p1	$105.8 \pm 1.33$
p2	$-1.477\text{e}+08 \pm 4.083\text{e}+06$
p3	$2.724\text{e}+07 \pm 4.551\text{e}+05$
p4	$3.886 \pm 0.1015$

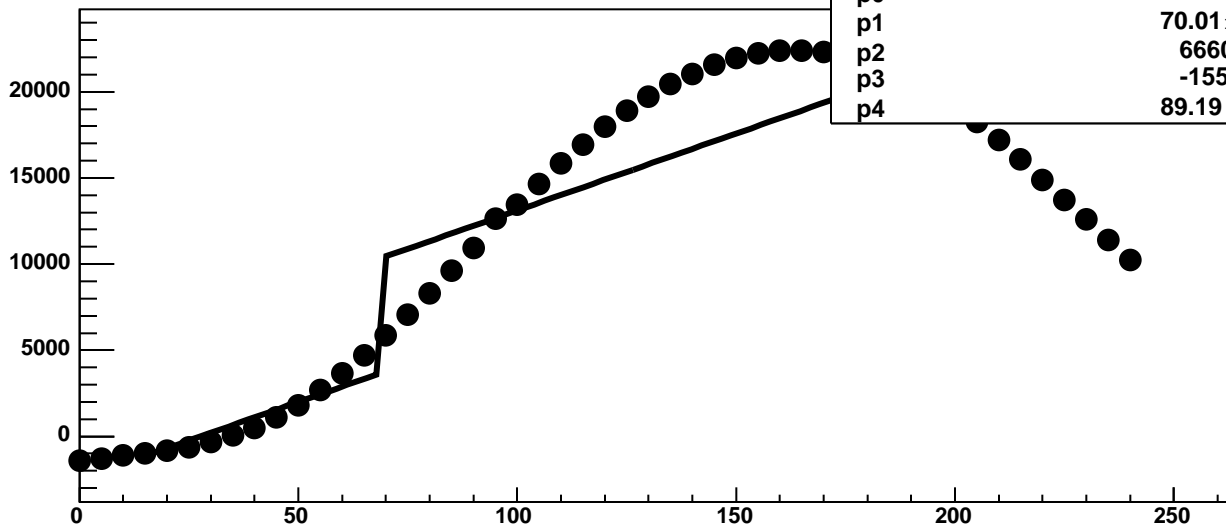
Chip 6, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

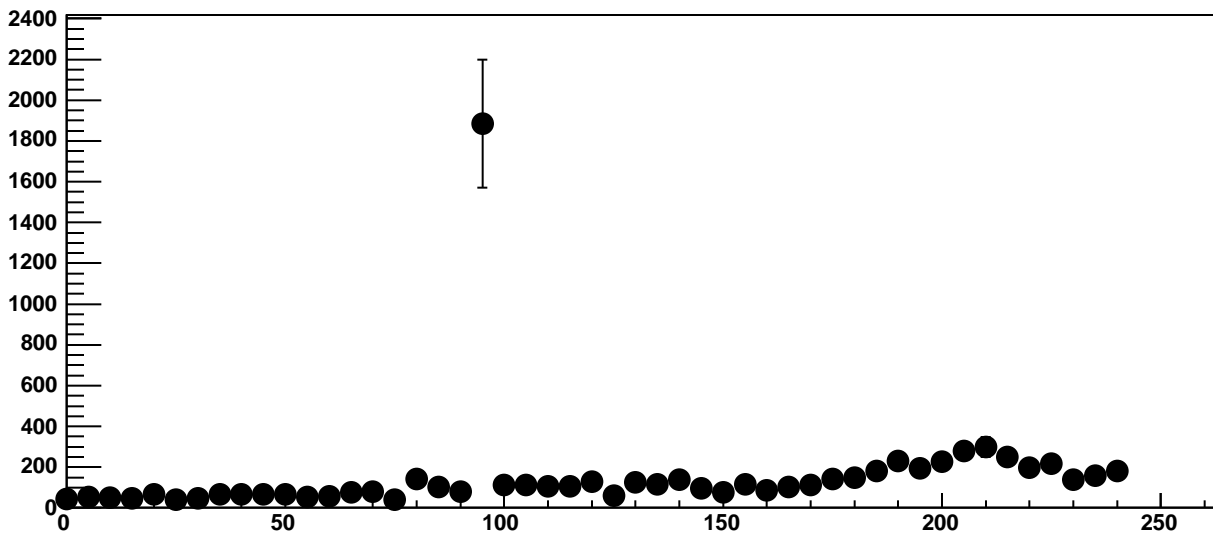


Chip 6, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold

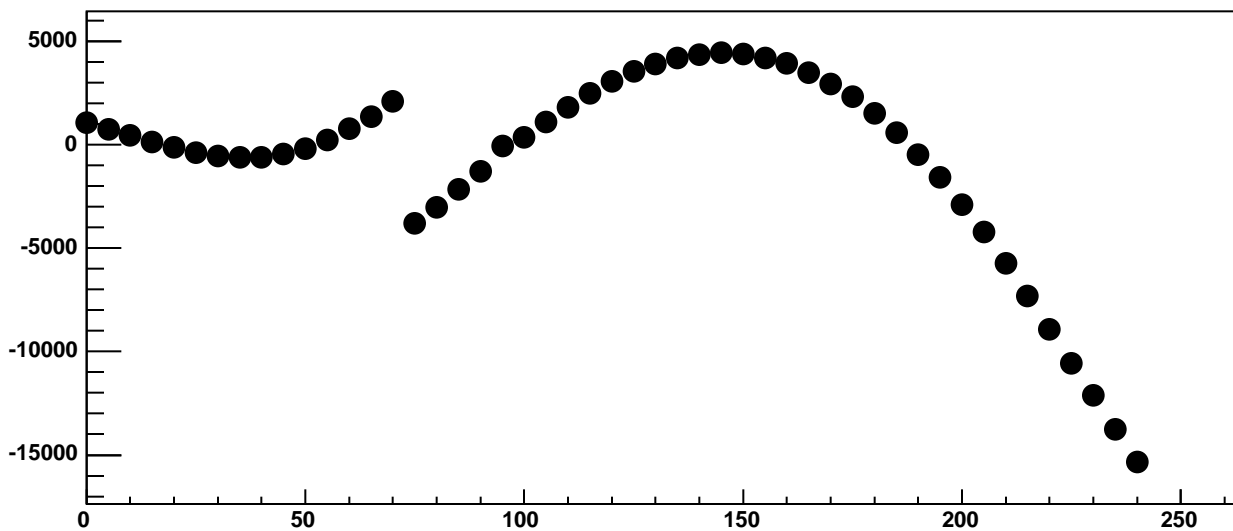


$\chi^2 / \text{ndf}$	1.125e+06 / 41
p0	3783 ± 11.98
p1	70.01 ± 0.2156
p2	6660 ± 29.03
p3	-155.3 ± 6.2
p4	89.19 ± 0.4037

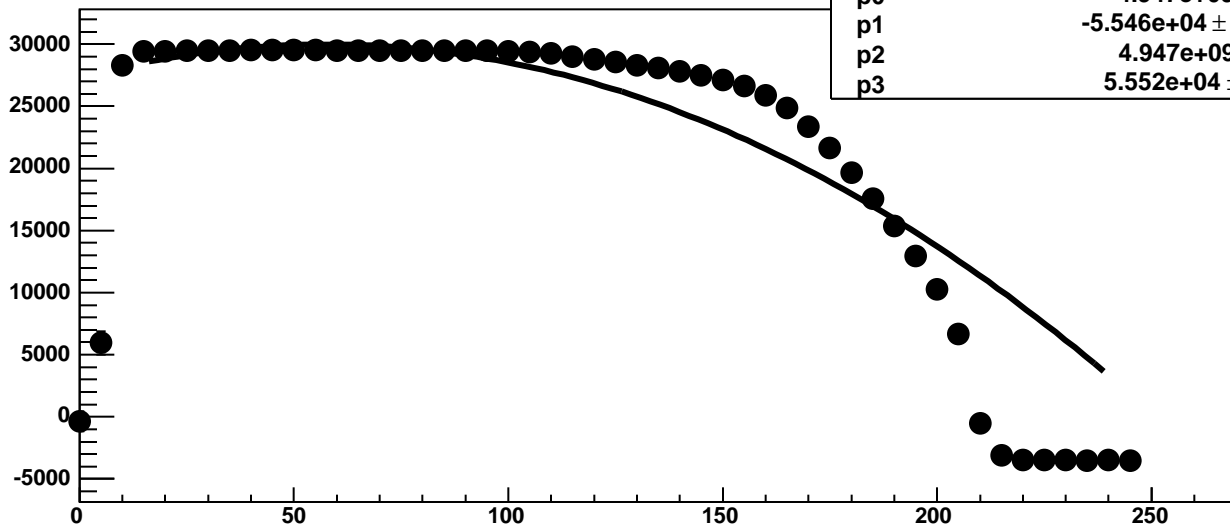
Chip 6, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



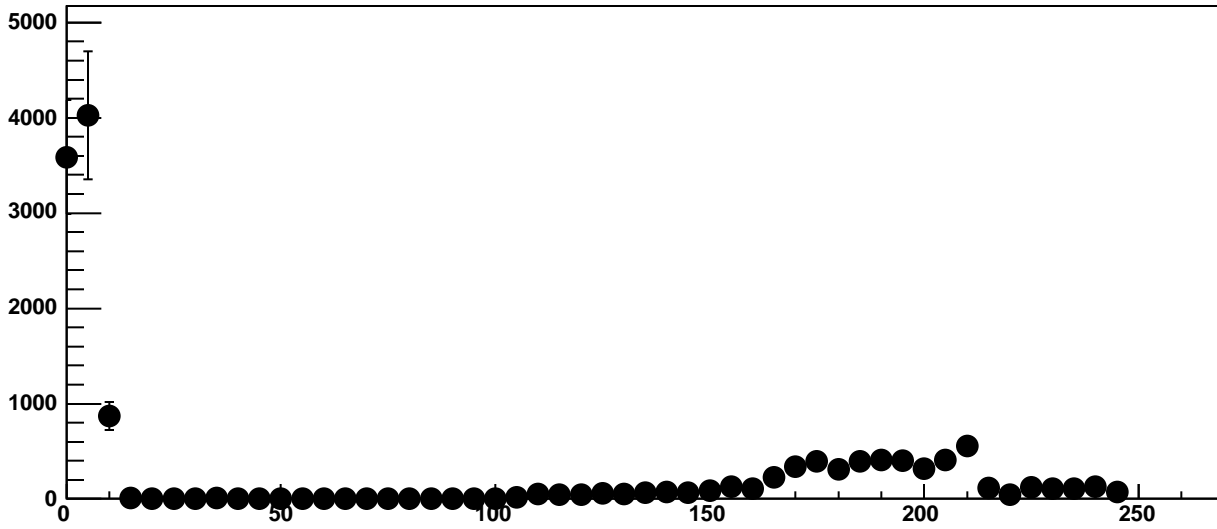
Chip 6, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold



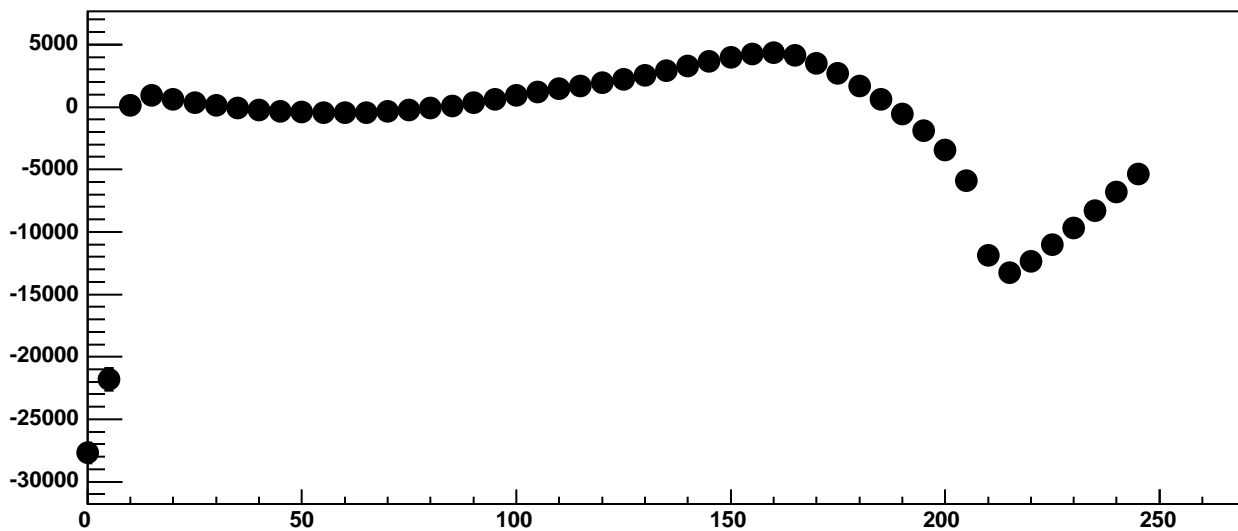
Chip 6, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold



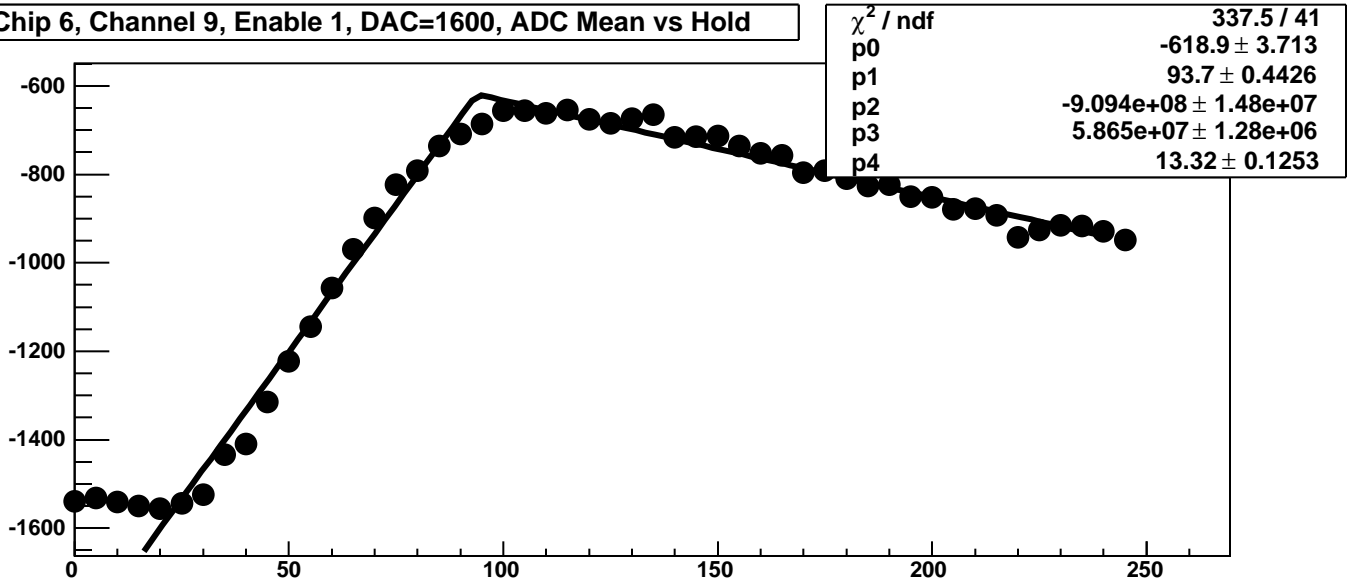
Chip 6, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



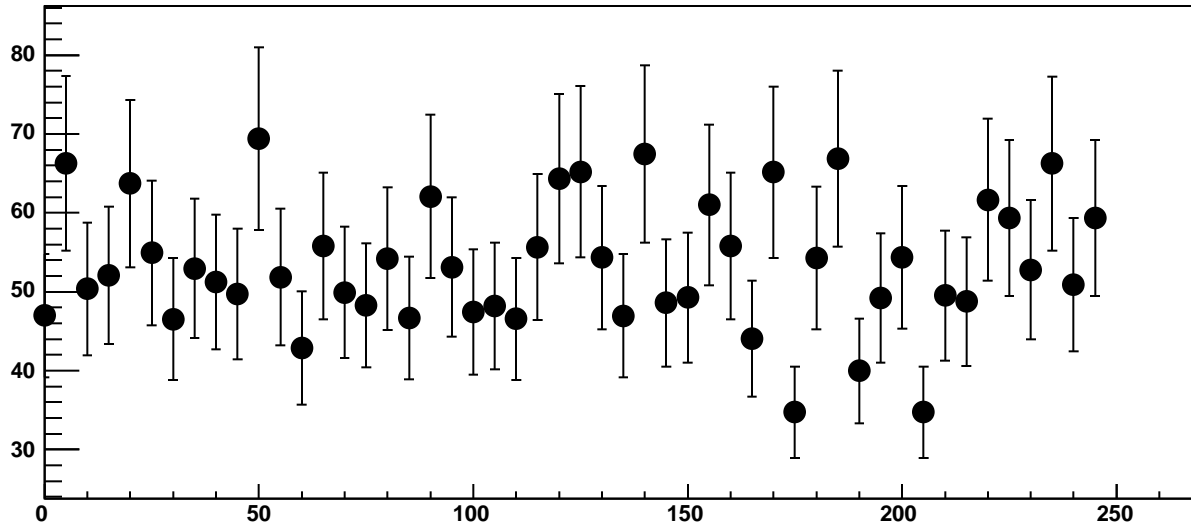
Chip 6, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold



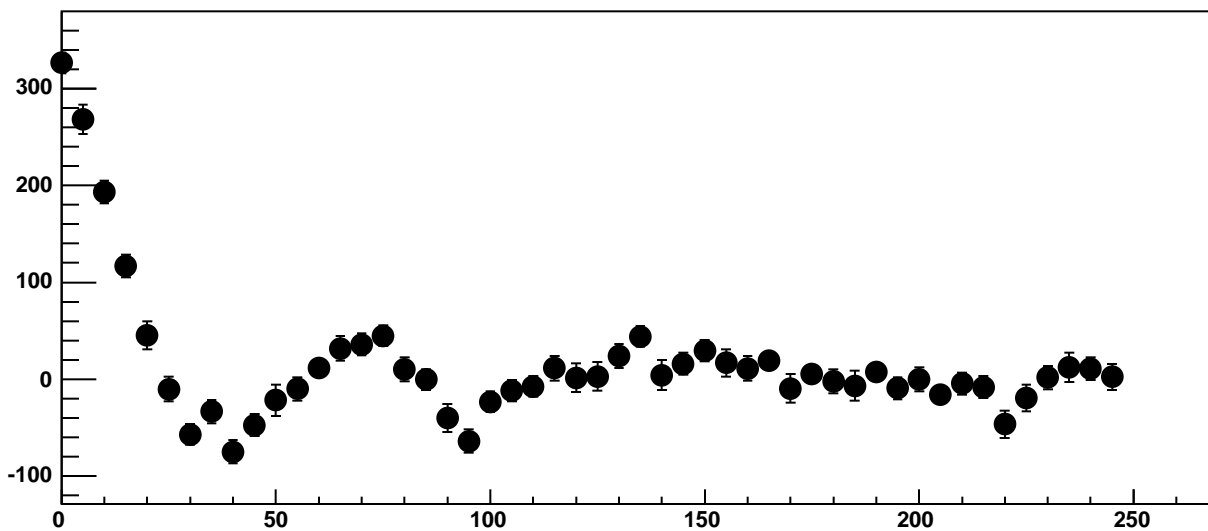
Chip 6, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold



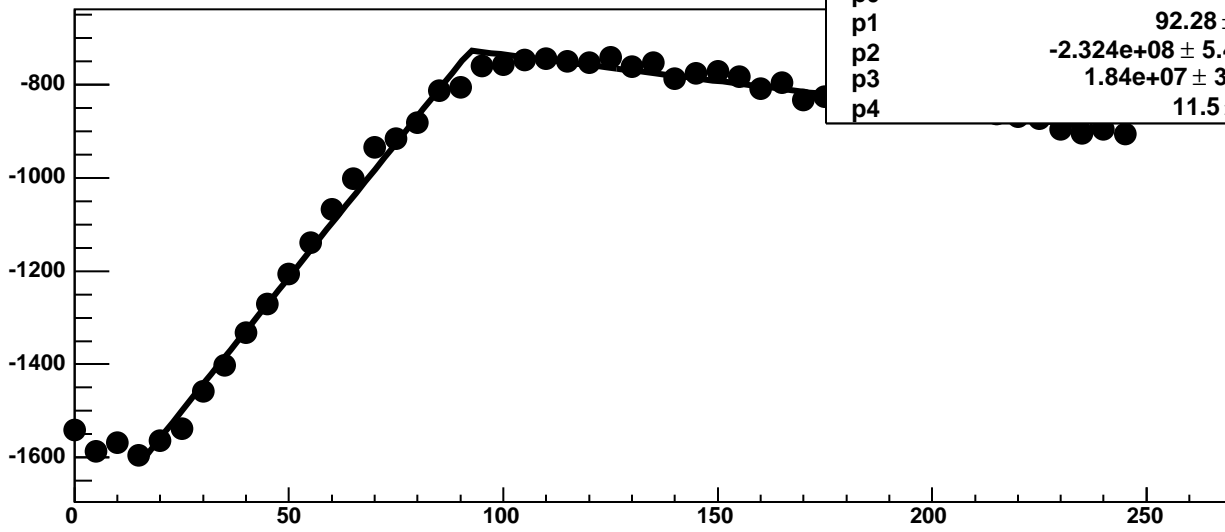
Chip 6, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

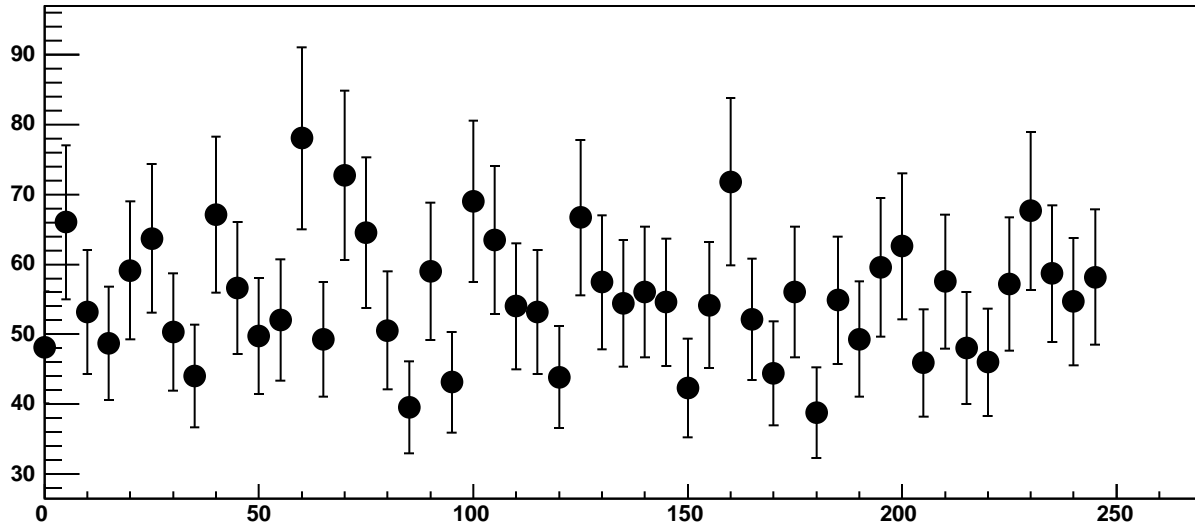


Chip 6, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

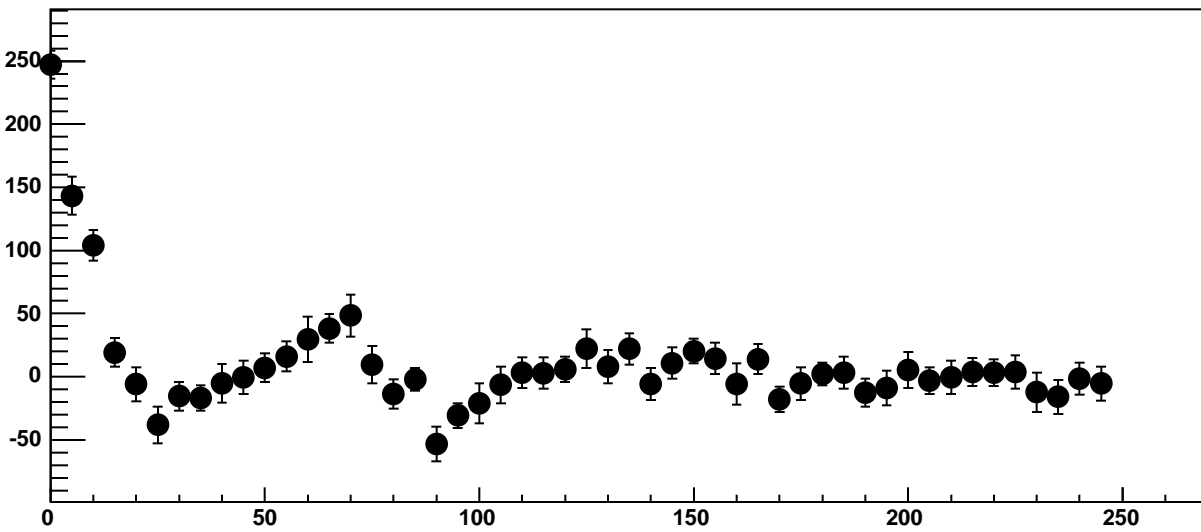


$\chi^2 / \text{ndf}$	90.42 / 41
p0	$-726.7 \pm 4.173$
p1	$92.28 \pm 0.5918$
p2	$-2.324\text{e}+08 \pm 5.415\text{e}+06$
p3	$1.84\text{e}+07 \pm 3.49\text{e}+05$
p4	$11.5 \pm 0.1301$

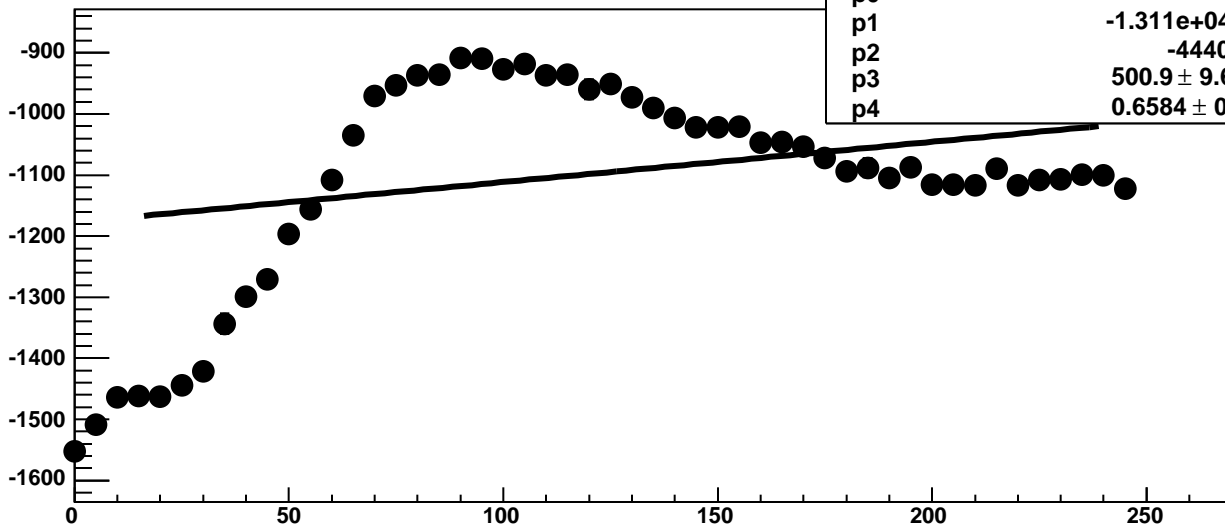
Chip 6, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

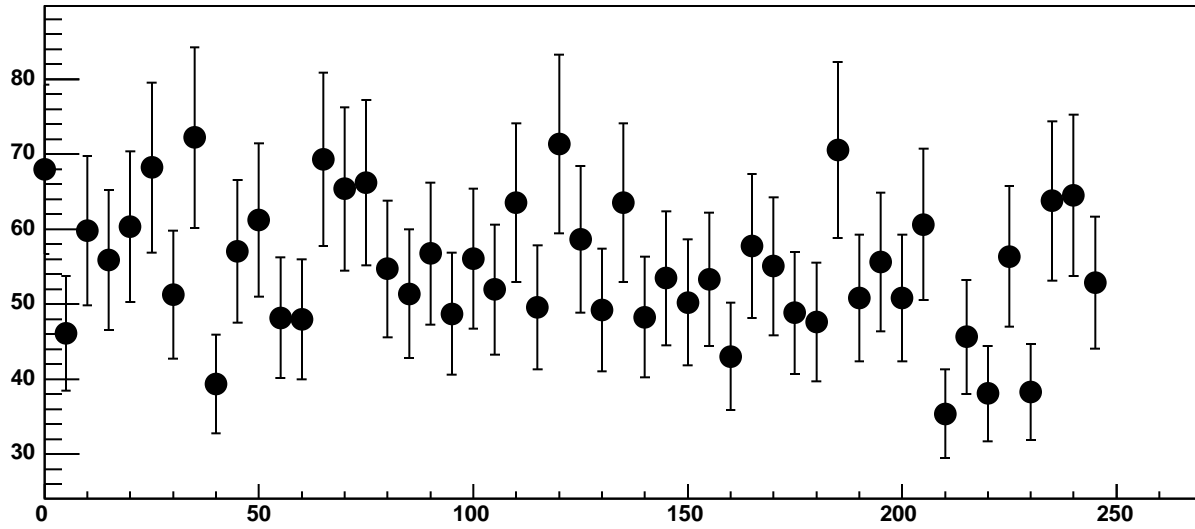


Chip 6, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold

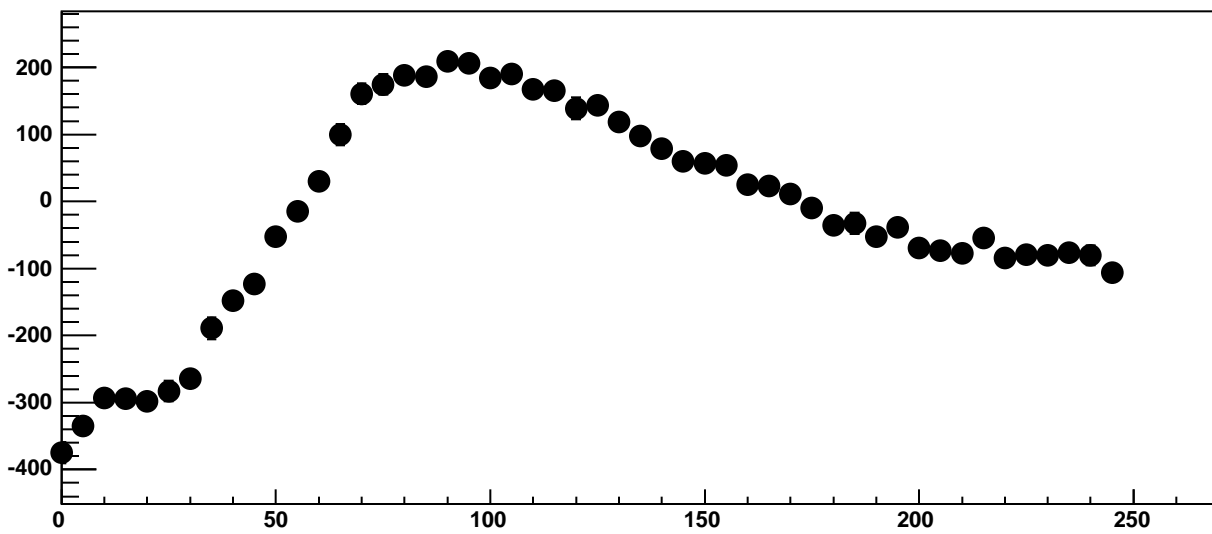


$\chi^2 / \text{ndf}$	5465 / 41
p0	$-5369 \pm 24.33$
p1	$-1.311\text{e}+04 \pm 36.96$
p2	$-4440 \pm 24.33$
p3	$500.9 \pm 9.656\text{e}+04$
p4	$0.6584 \pm 0.001833$

Chip 6, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

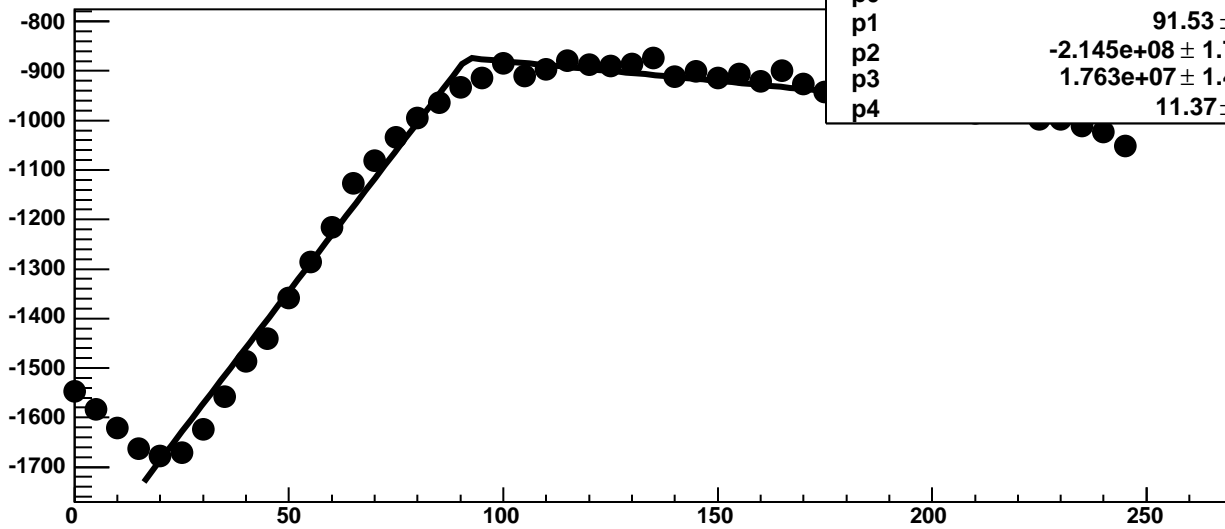


Chip 6, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold



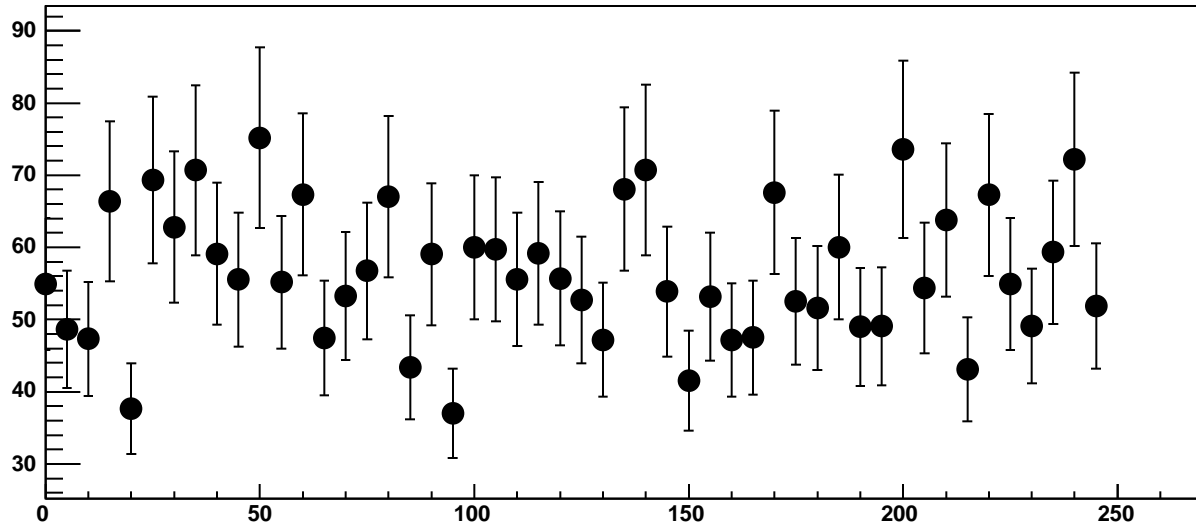


Chip 6, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

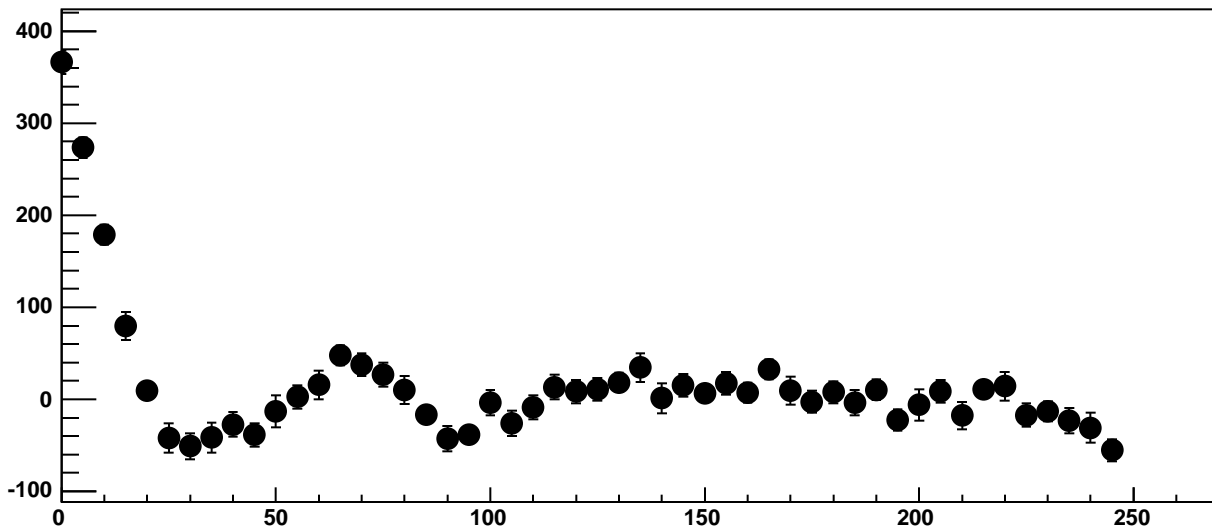


$\chi^2 / \text{ndf}$	183.6 / 41
p0	-873.4 ± 4.138
p1	91.53 ± 0.6166
p2	-2.145e+08 ± 1.791e+07
p3	1.763e+07 ± 1.457e+06
p4	11.37 ± 0.1335

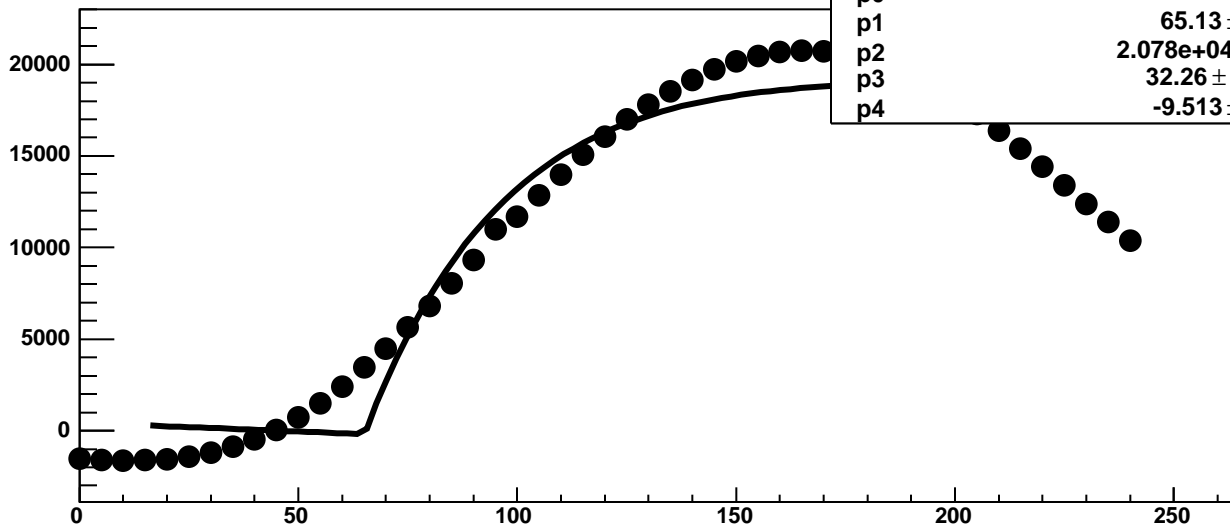
Chip 6, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

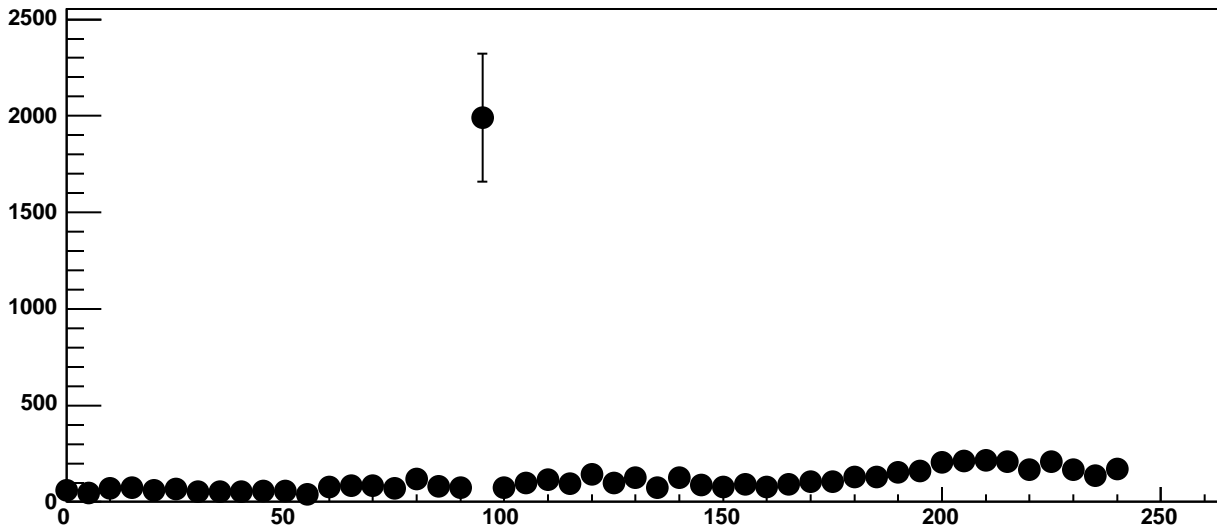


Chip 6, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

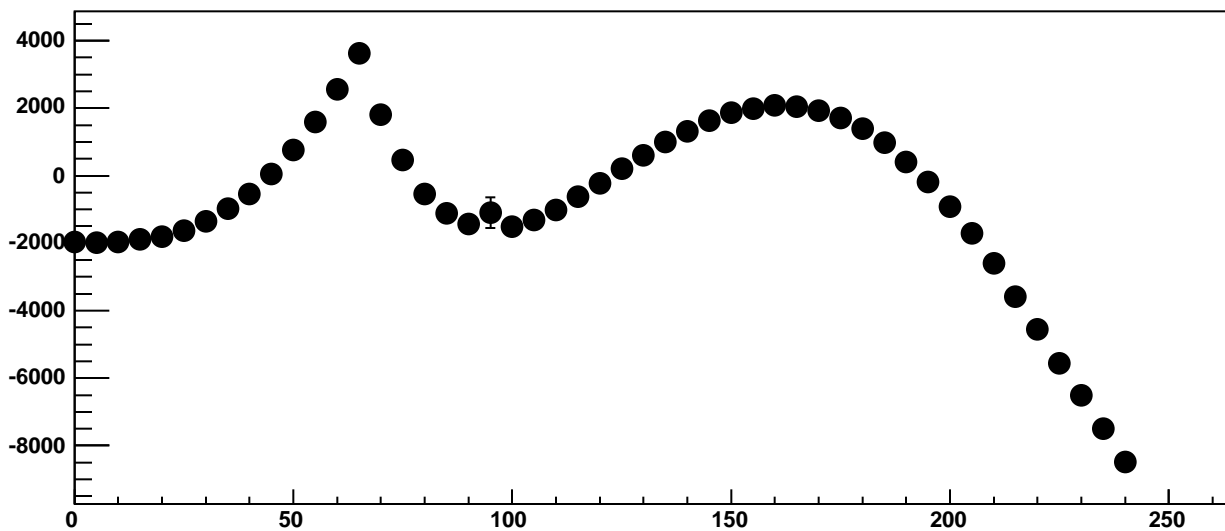


$\chi^2 / \text{ndf}$	4.27e+05 / 41
p0	-185.8 ± 5.906
p1	65.13 ± 0.0283
p2	2.078e+04 ± 29.69
p3	32.26 ± 0.06273
p4	-9.513 ± 0.1862

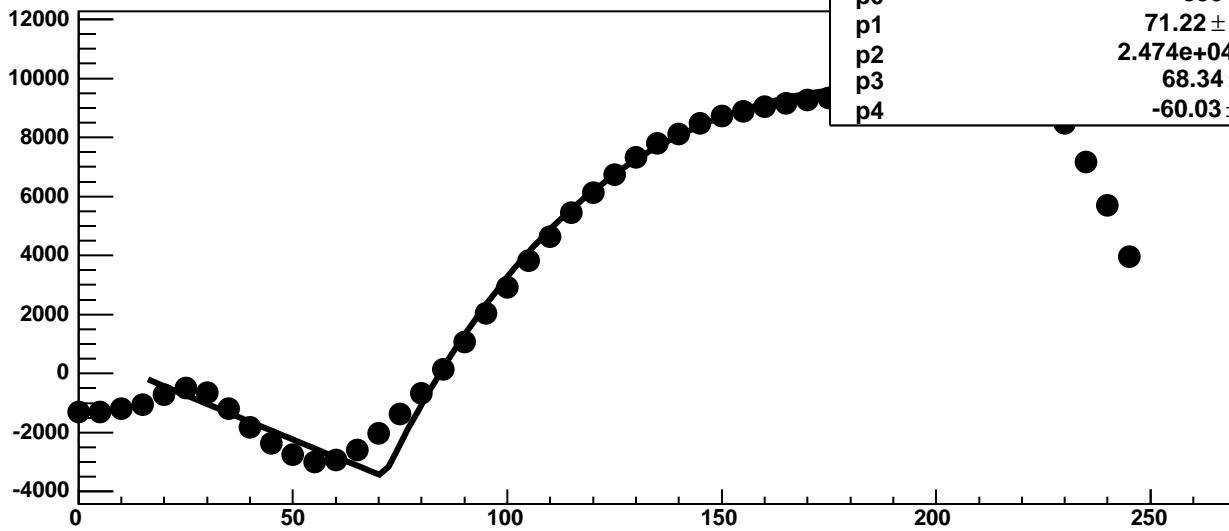
Chip 6, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

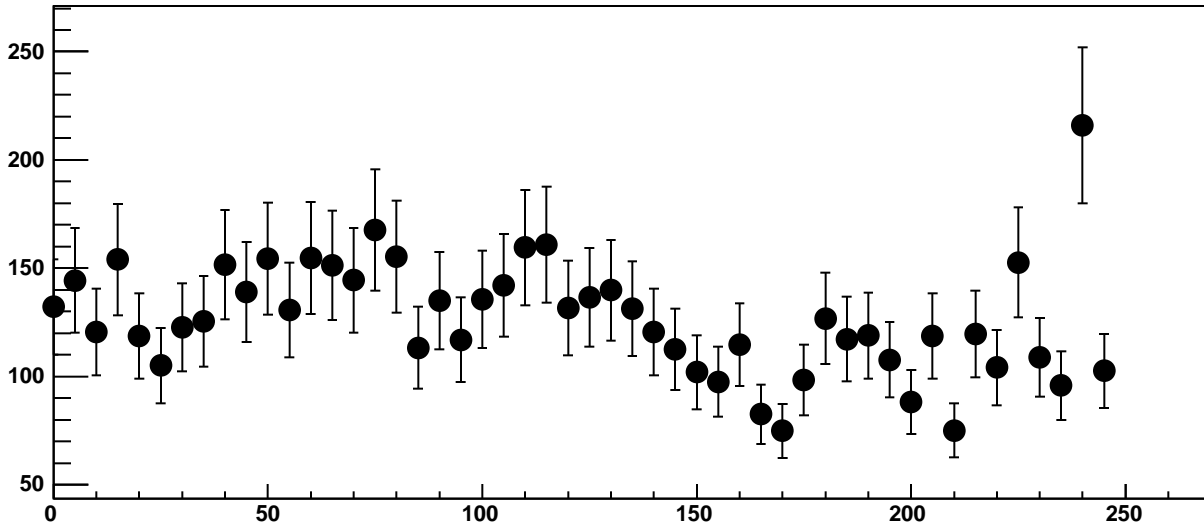


Chip 6, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold

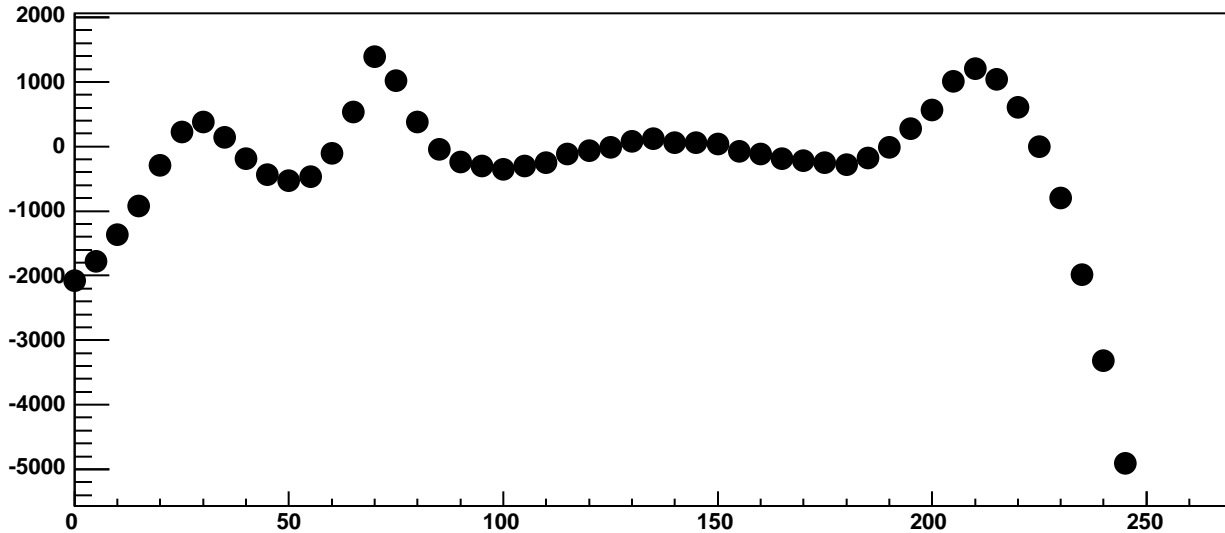


$\chi^2 / \text{ndf}$	2.858e+04 / 41
p0	-3501 ± 13.87
p1	71.22 ± 0.08228
p2	2.474e+04 ± 117.3
p3	68.34 ± 0.3161
p4	-60.03 ± 0.4589

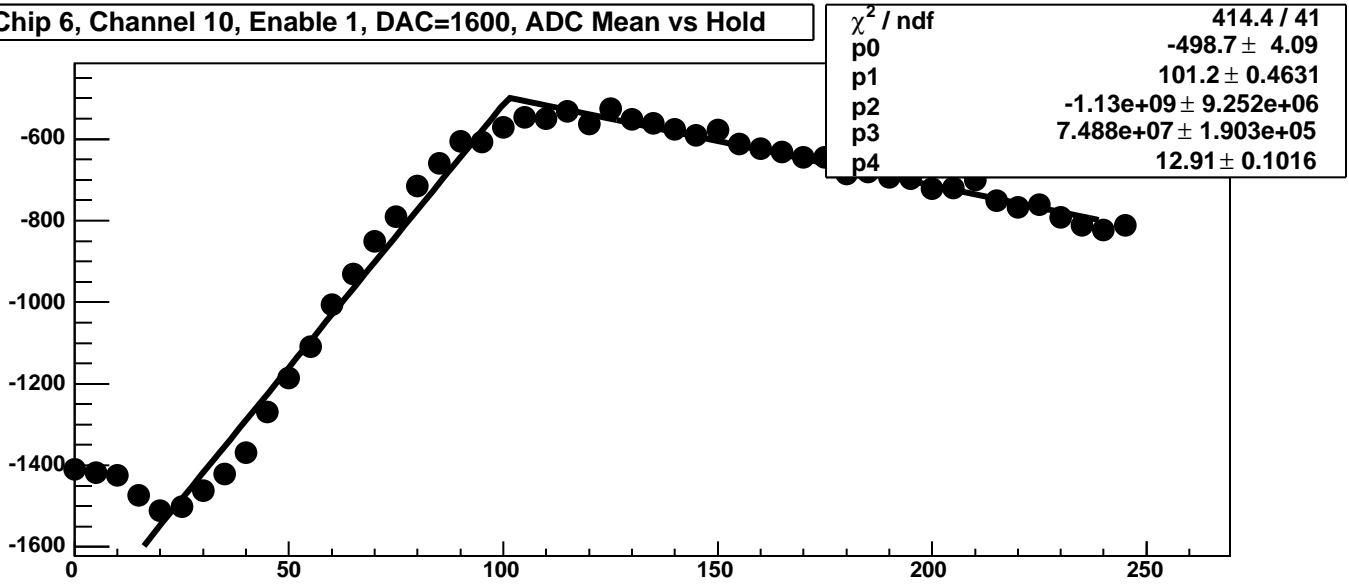
Chip 6, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



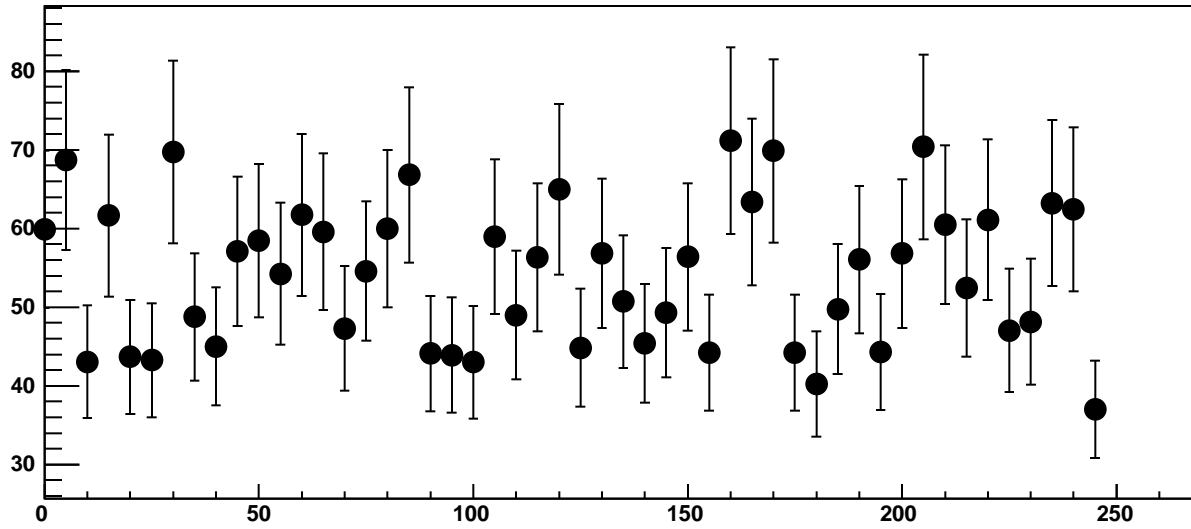
Chip 6, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold



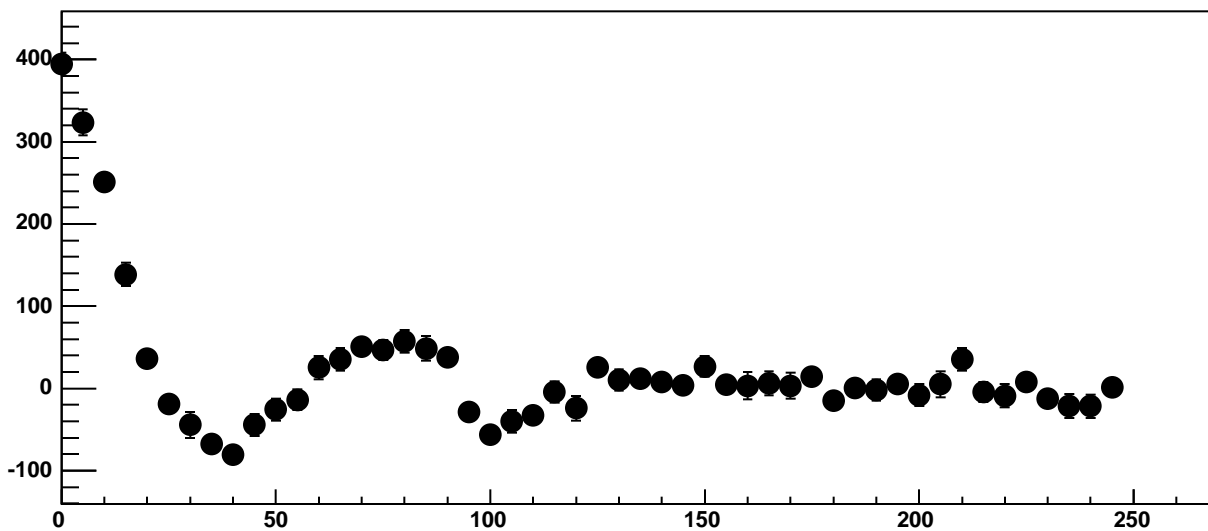
Chip 6, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold



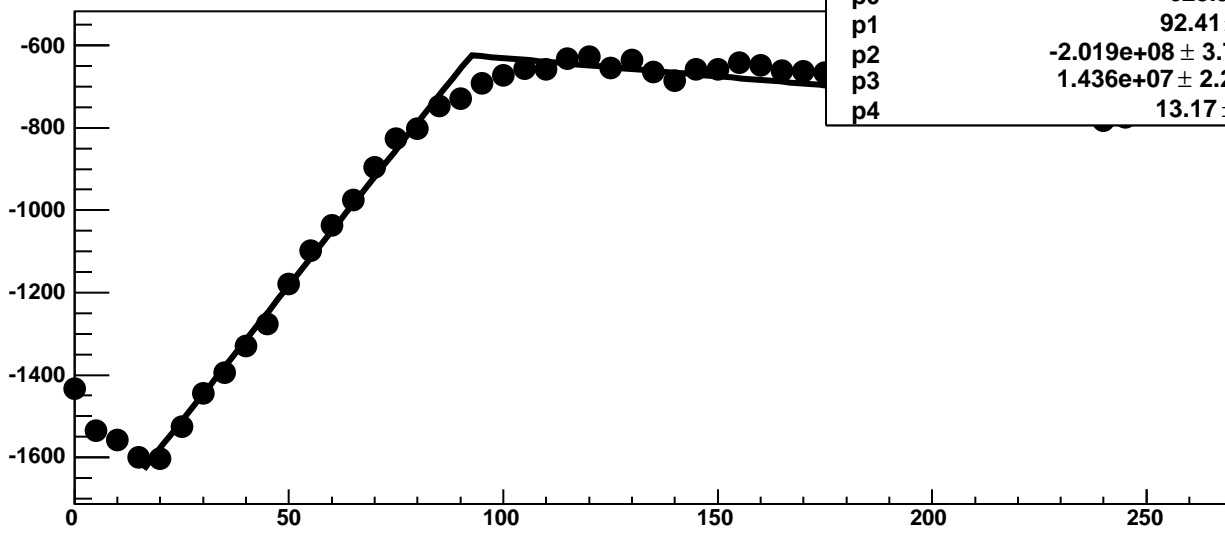
Chip 6, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

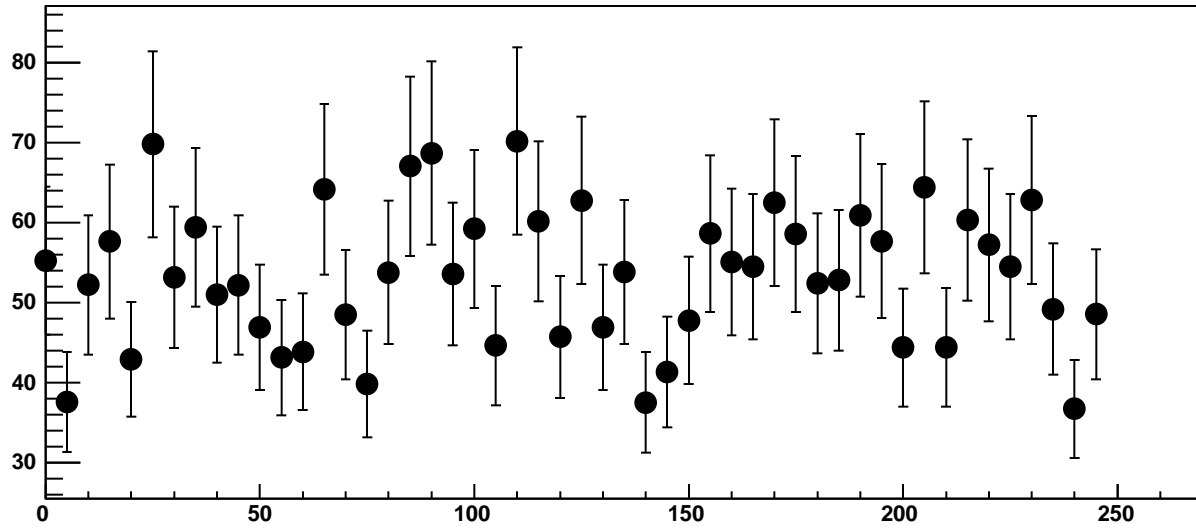


Chip 6, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

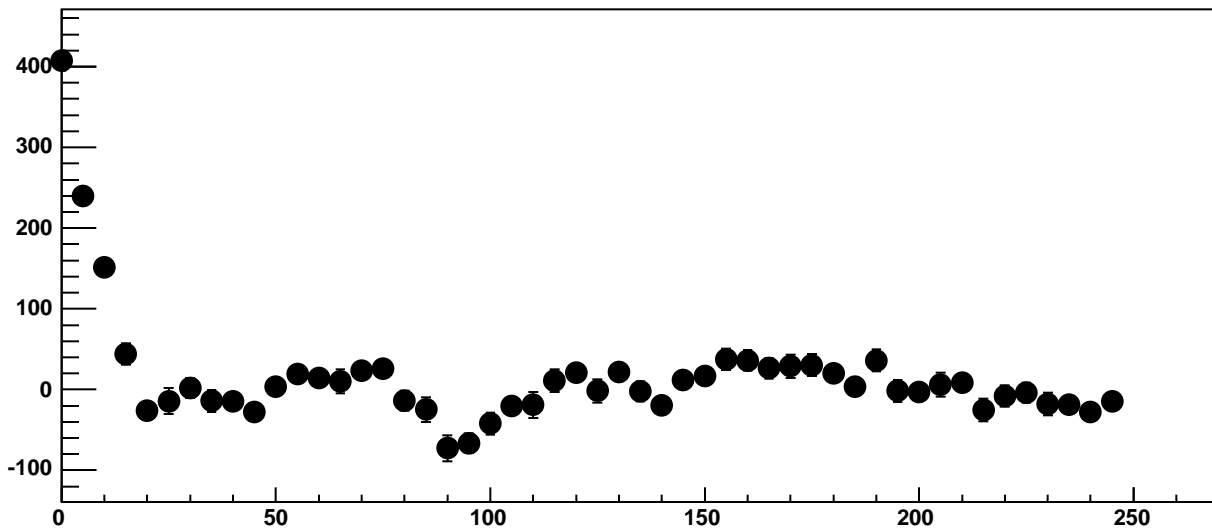


$\chi^2 / \text{ndf}$	192 / 41
p0	$-623.9 \pm 4.064$
p1	$92.41 \pm 0.5391$
p2	$-2.019\text{e}+08 \pm 3.722\text{e}+06$
p3	$1.436\text{e}+07 \pm 2.208\text{e}+05$
p4	$13.17 \pm 0.1367$

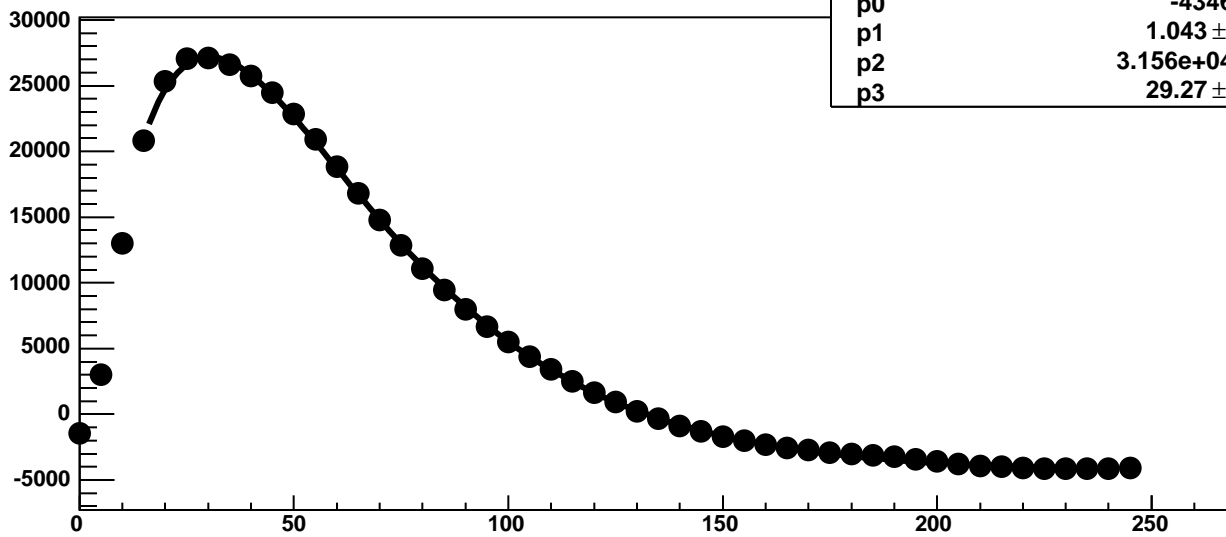
Chip 6, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



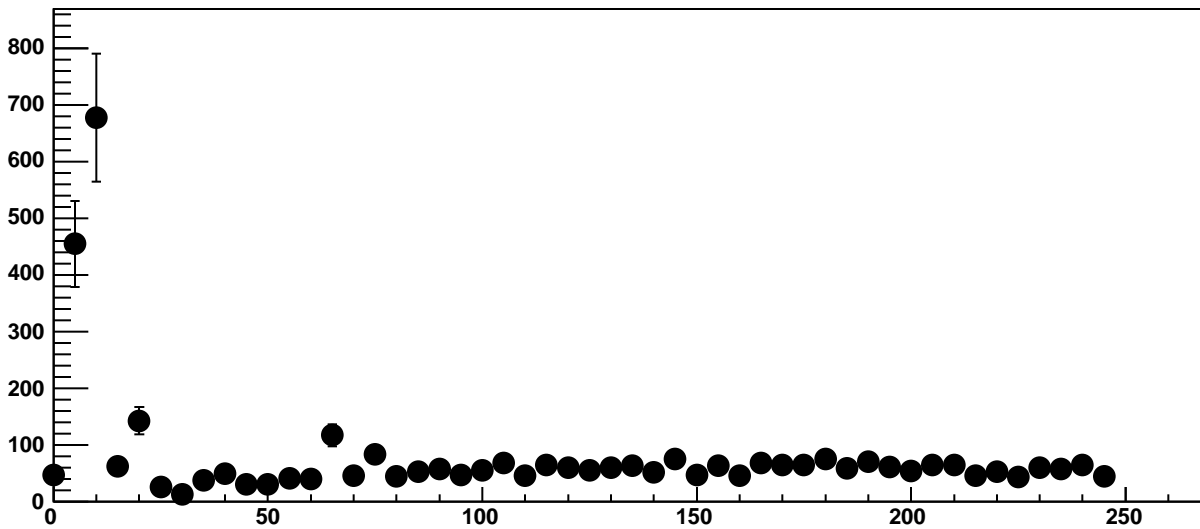
Chip 6, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold



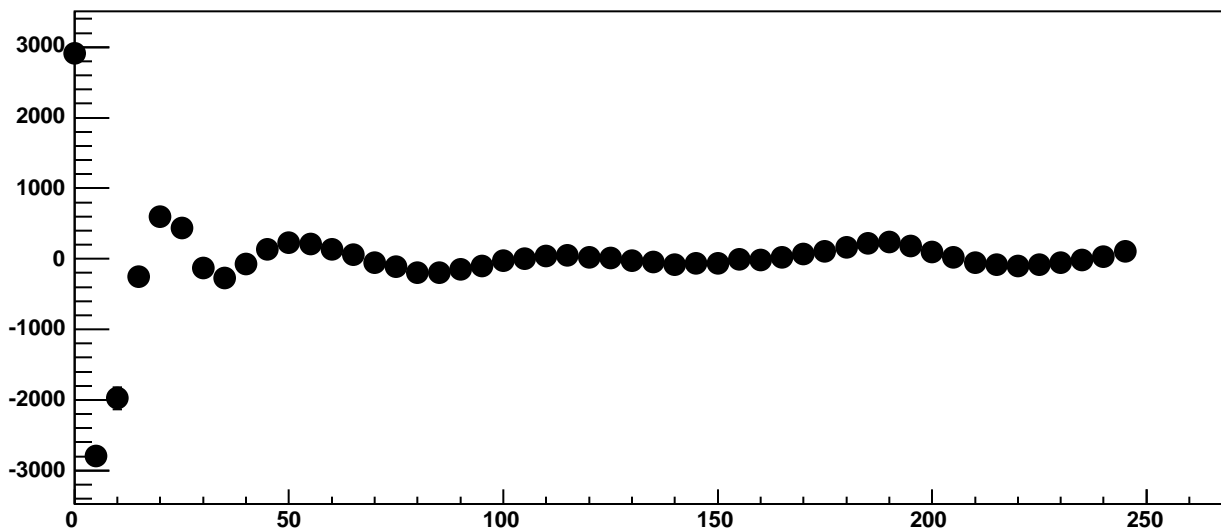
Chip 6, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold



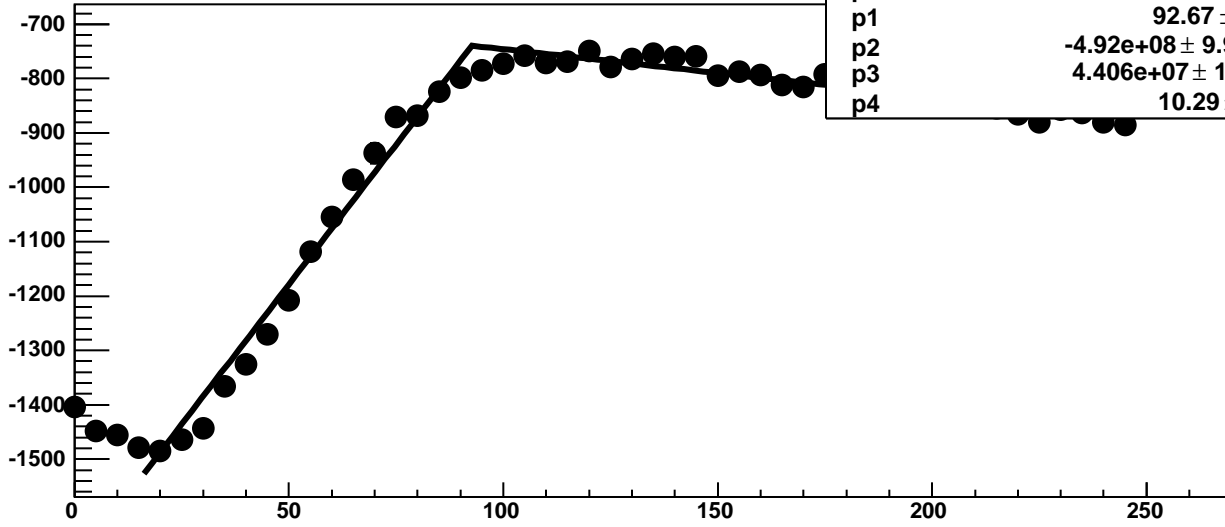
Chip 6, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold

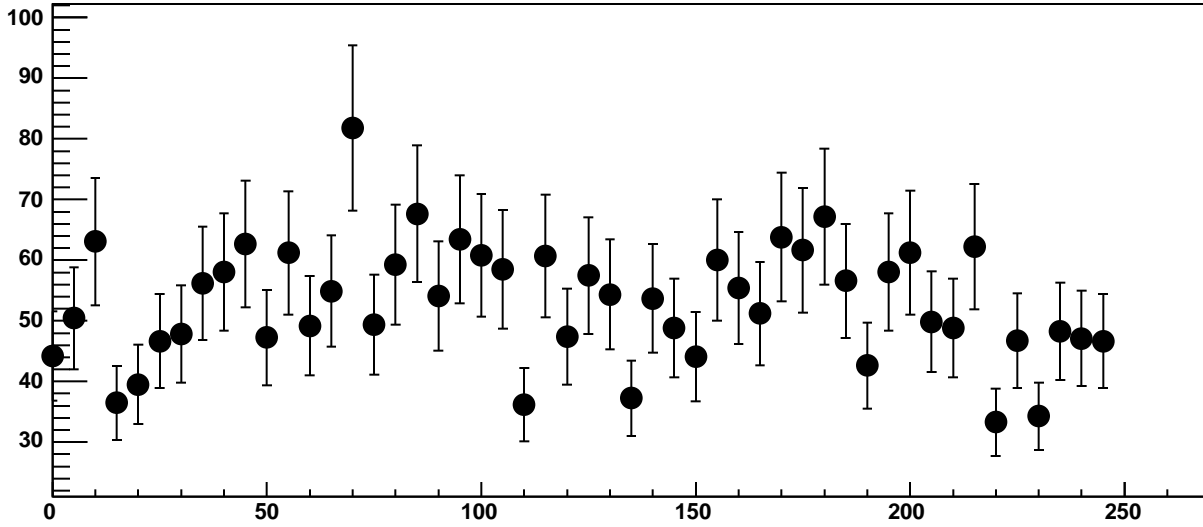


Chip 6, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

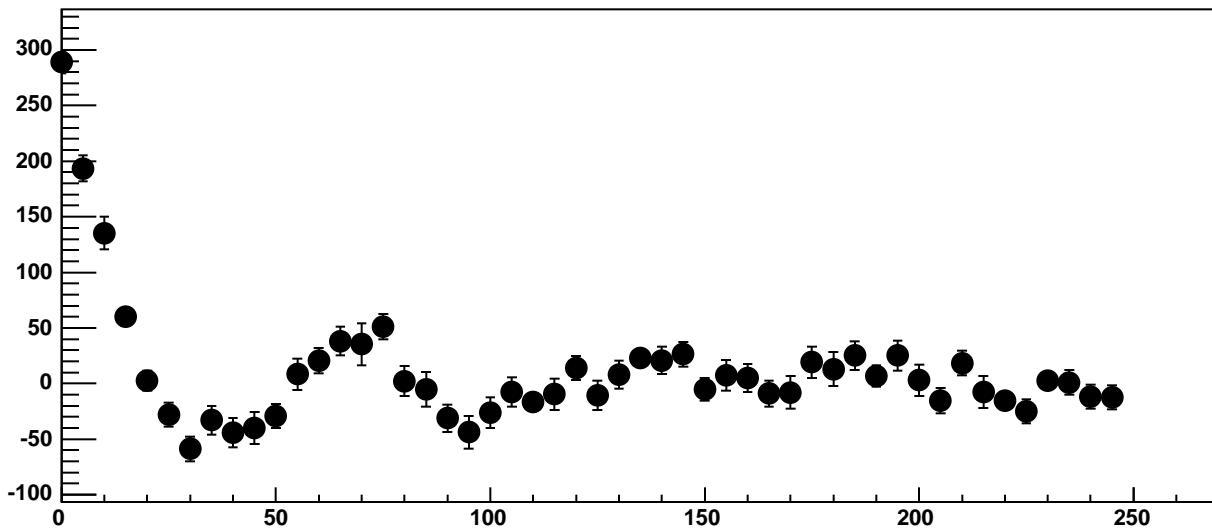


$\chi^2 / \text{ndf}$	226.9 / 41
p0	$-739.5 \pm 3.955$
p1	$92.67 \pm 0.5646$
p2	$-4.92\text{e}+08 \pm 9.943\text{e}+06$
p3	$4.406\text{e}+07 \pm 1.24\text{e}+06$
p4	$10.29 \pm 0.1101$

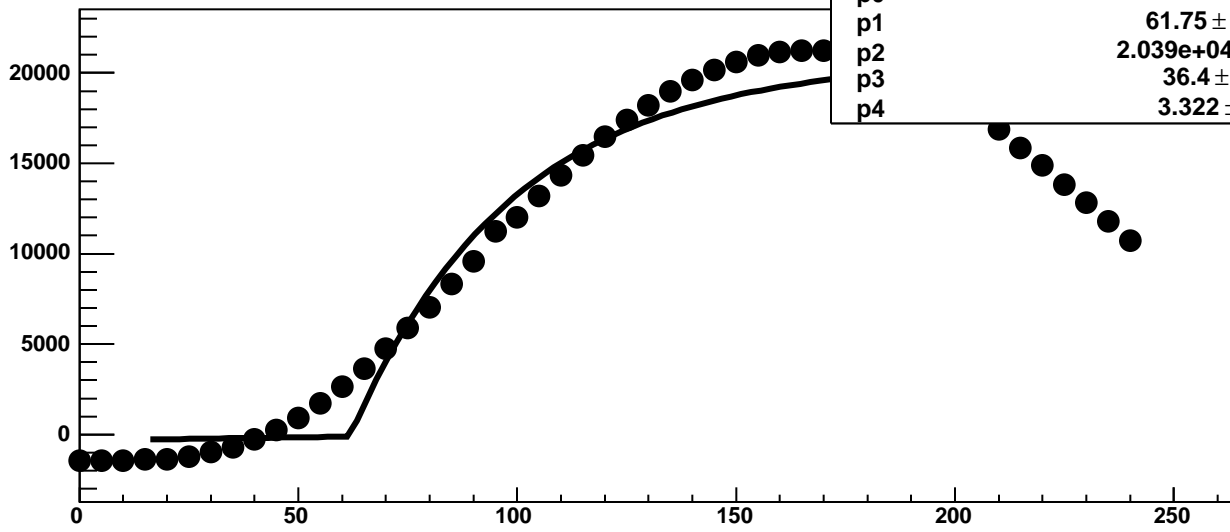
Chip 6, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



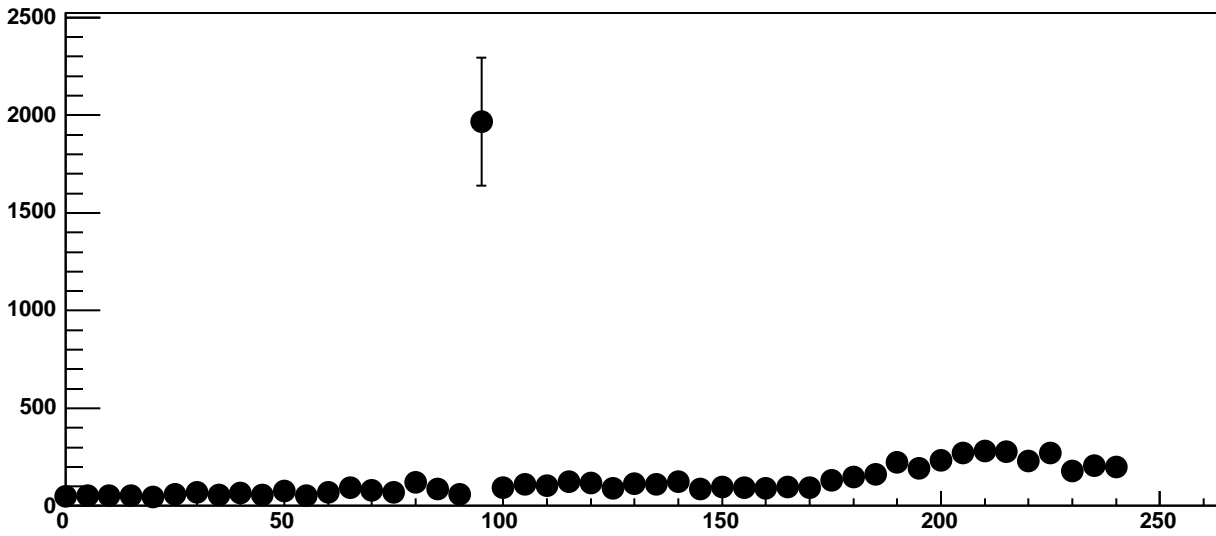
Chip 6, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold



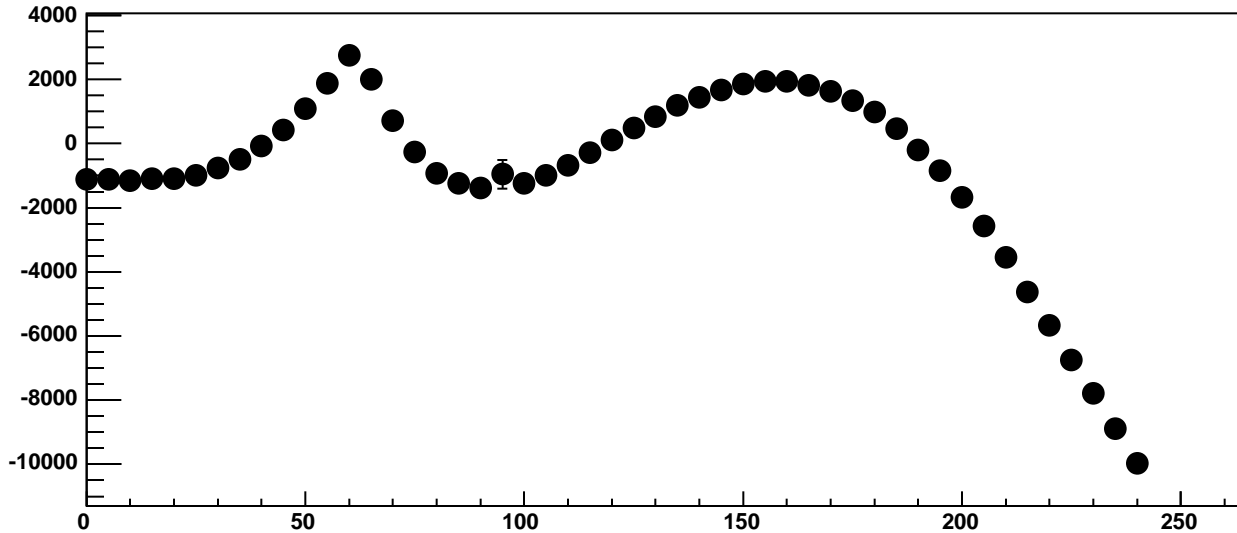
Chip 6, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 6, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold

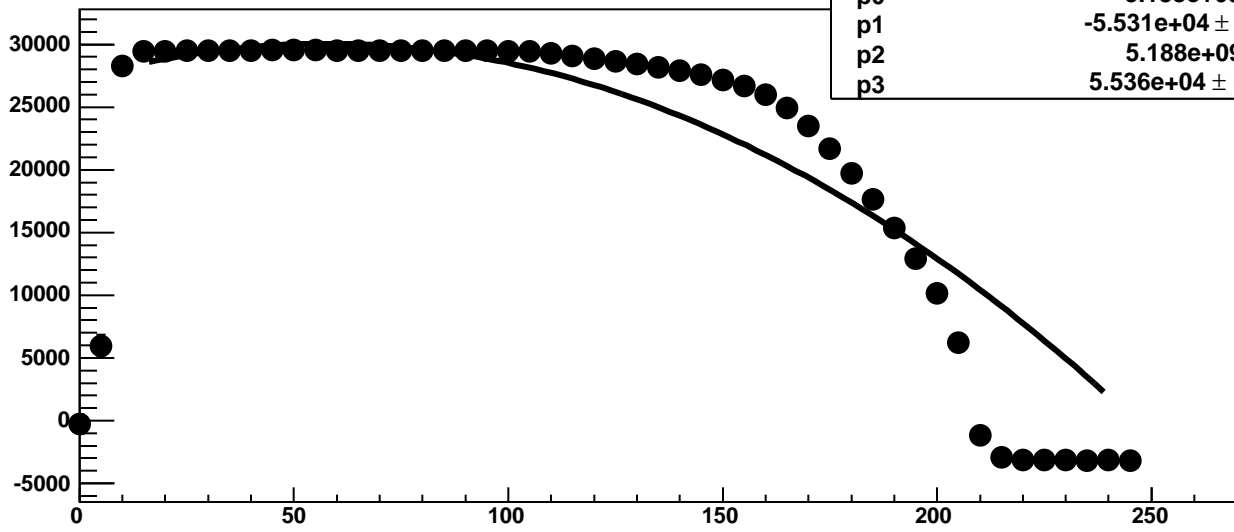


Chip 6, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold

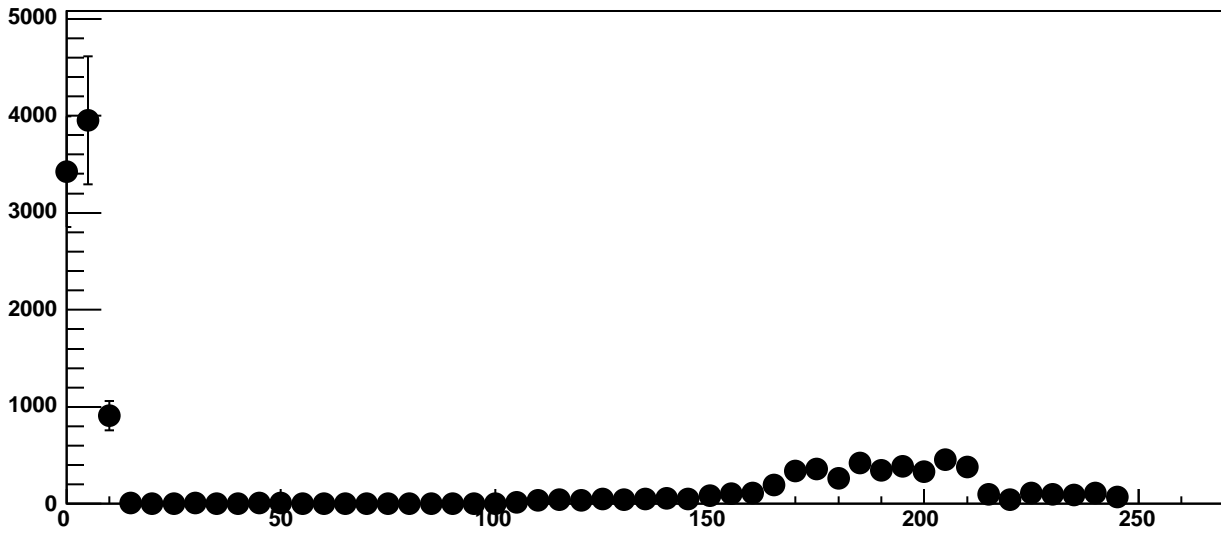




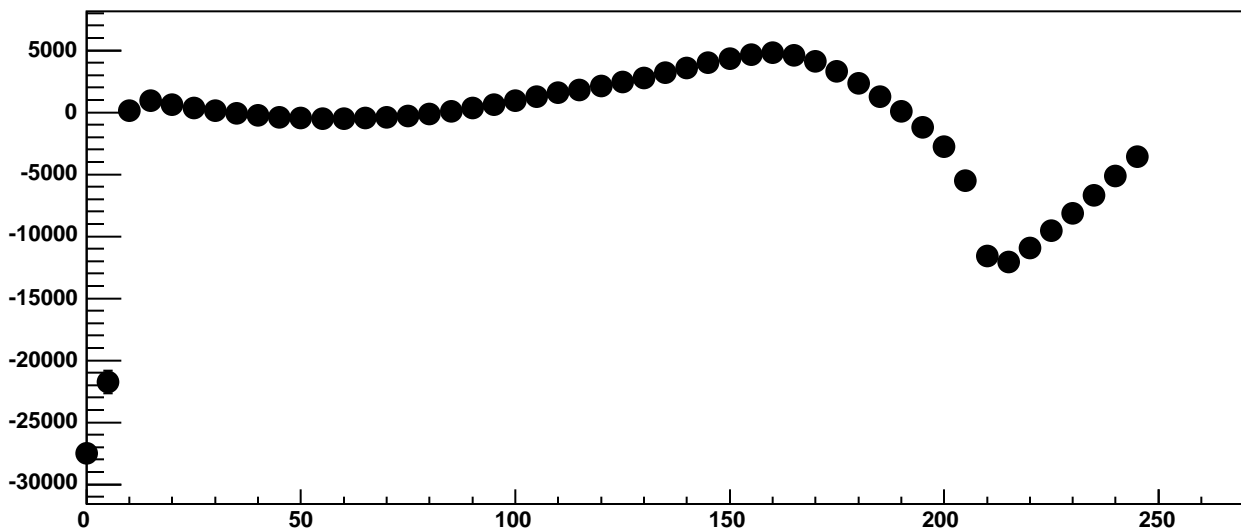
Chip 6, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold



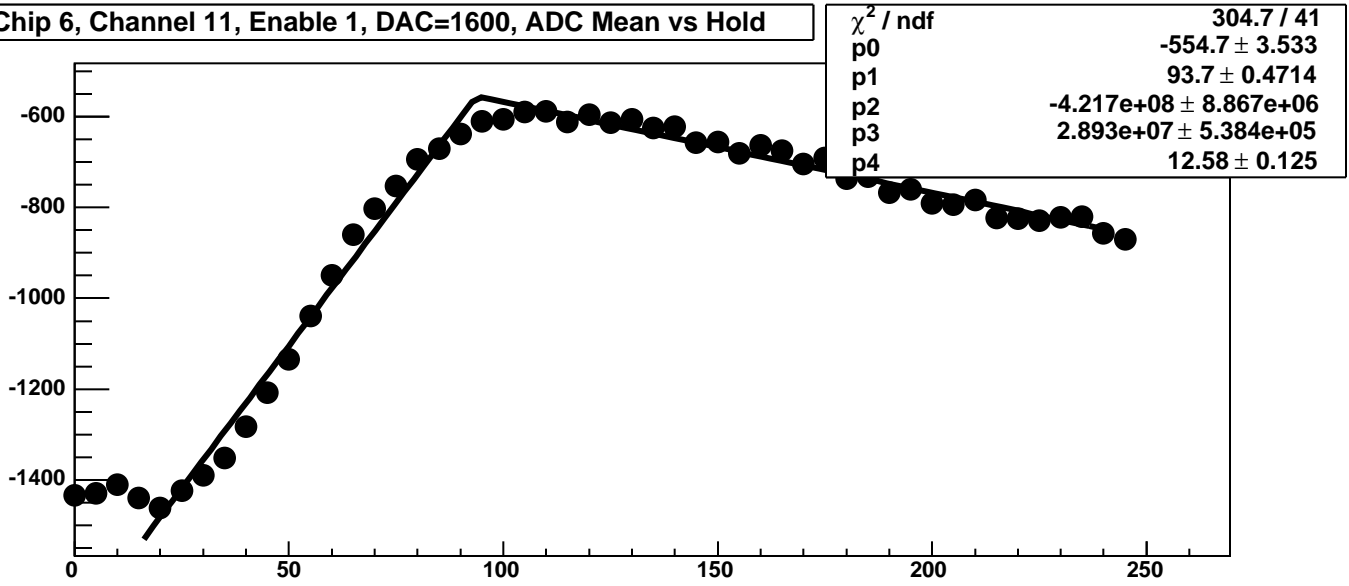
Chip 6, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



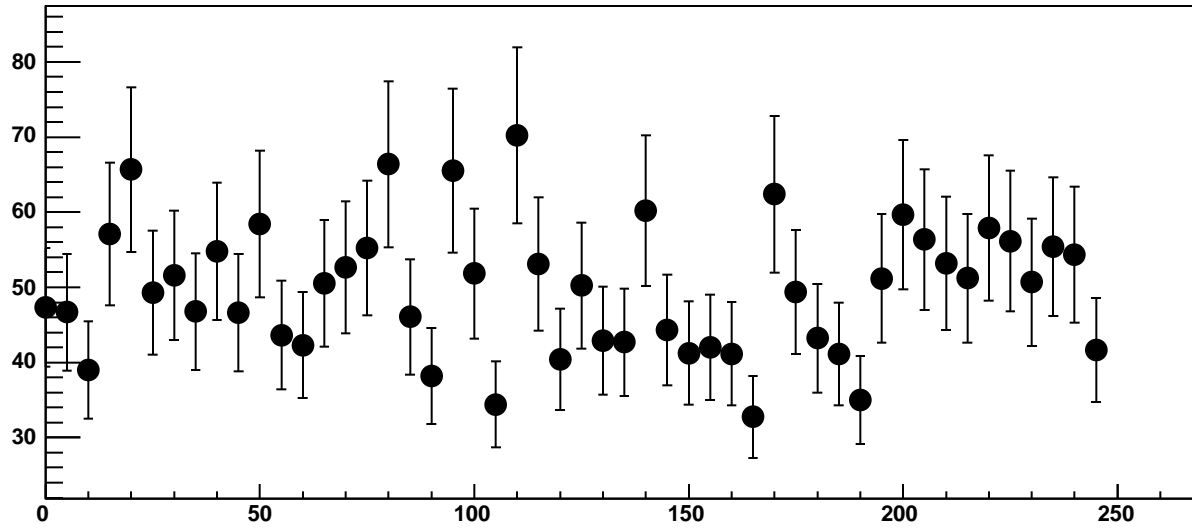
Chip 6, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold



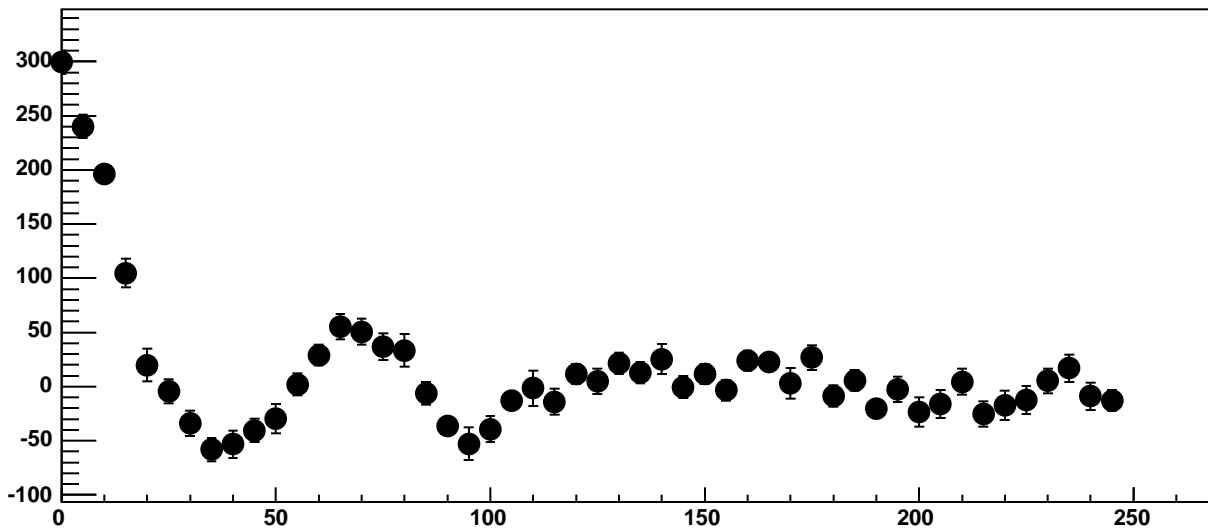
Chip 6, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold



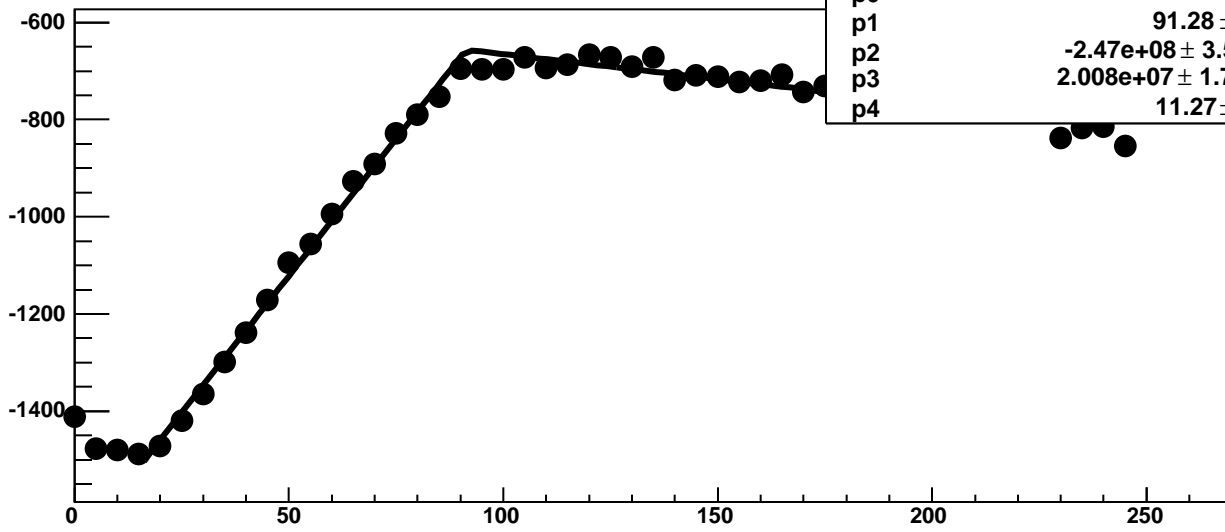
Chip 6, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

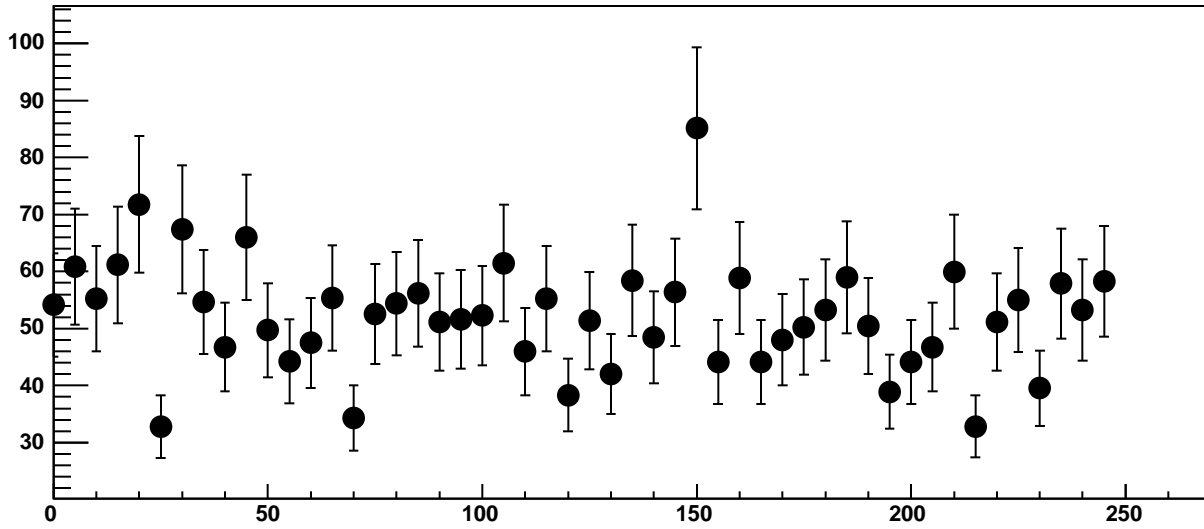


Chip 6, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

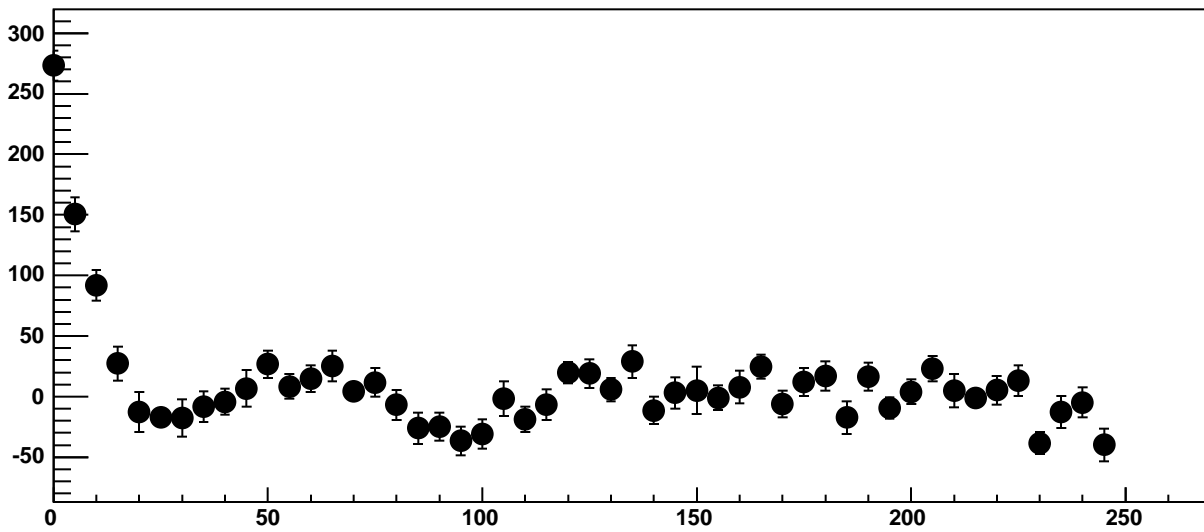


$\chi^2 / \text{ndf}$	106.7 / 41
p0	$-656.2 \pm 3.926$
p1	$91.28 \pm 0.5734$
p2	$-2.47\text{e}+08 \pm 3.515\text{e}+06$
p3	$2.008\text{e}+07 \pm 1.785\text{e}+05$
p4	$11.27 \pm 0.1276$

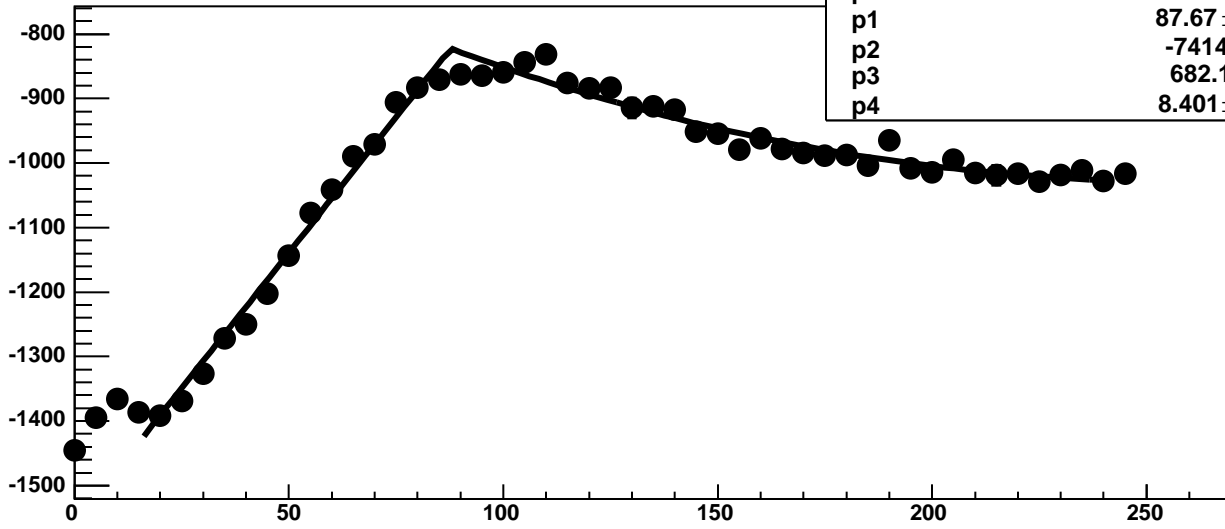
Chip 6, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

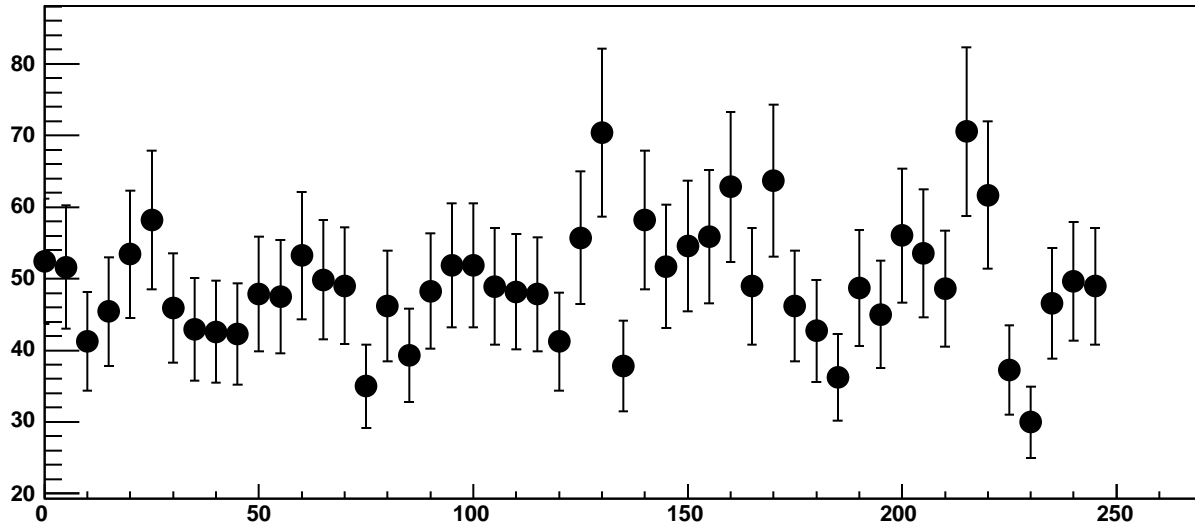


Chip 6, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold

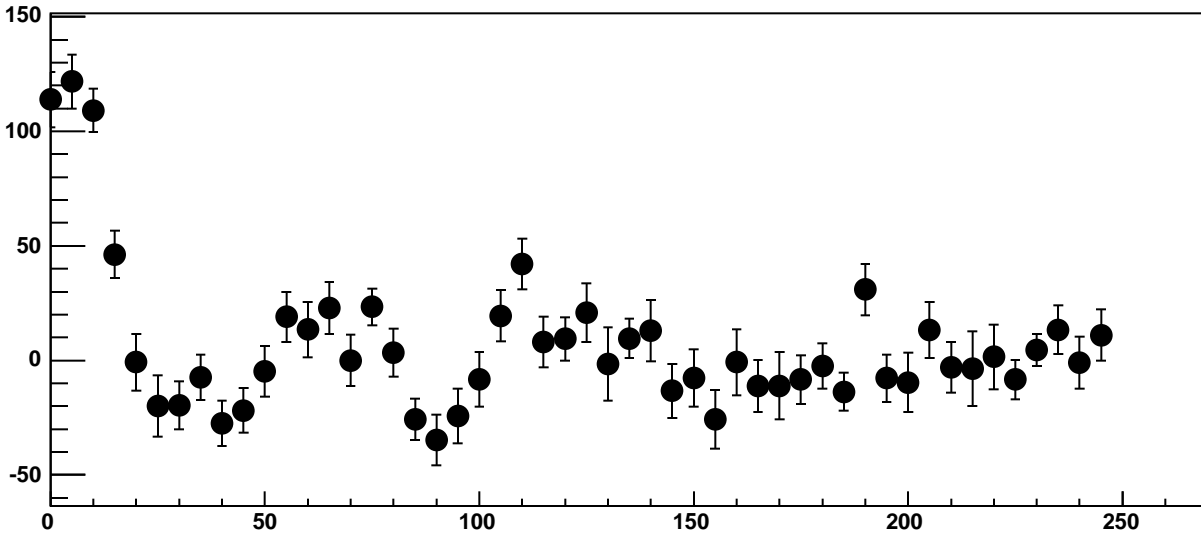


$\chi^2 / \text{ndf}$	126.2 / 41
p0	-822.3 ± 4.976
p1	87.67 ± 0.7448
p2	-7414 ± 1055
p3	682.1 ± 107.3
p4	8.401 ± 0.1239

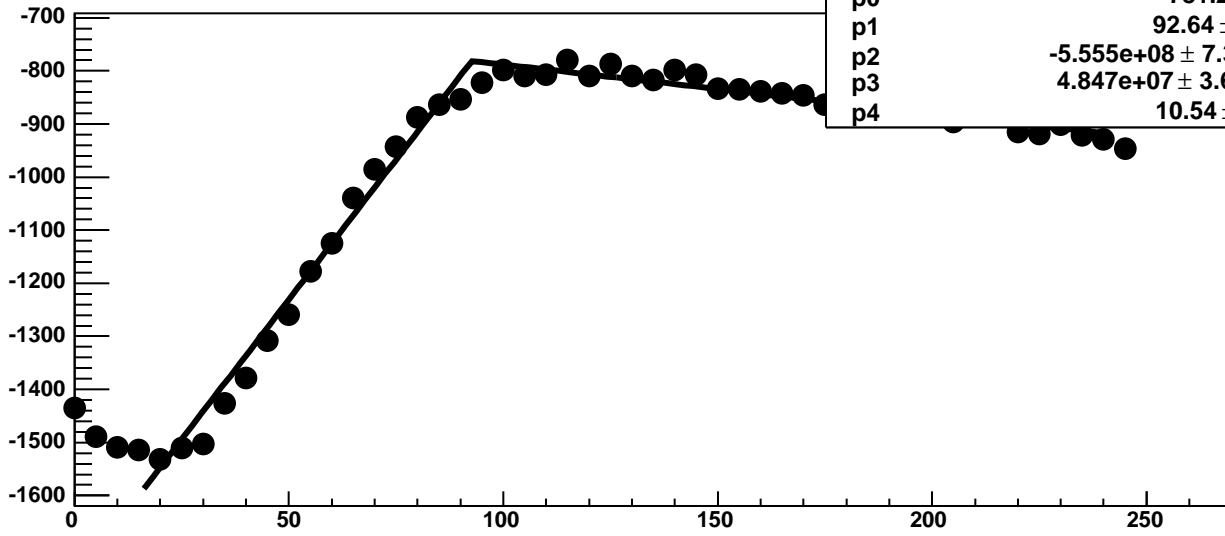
Chip 6, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

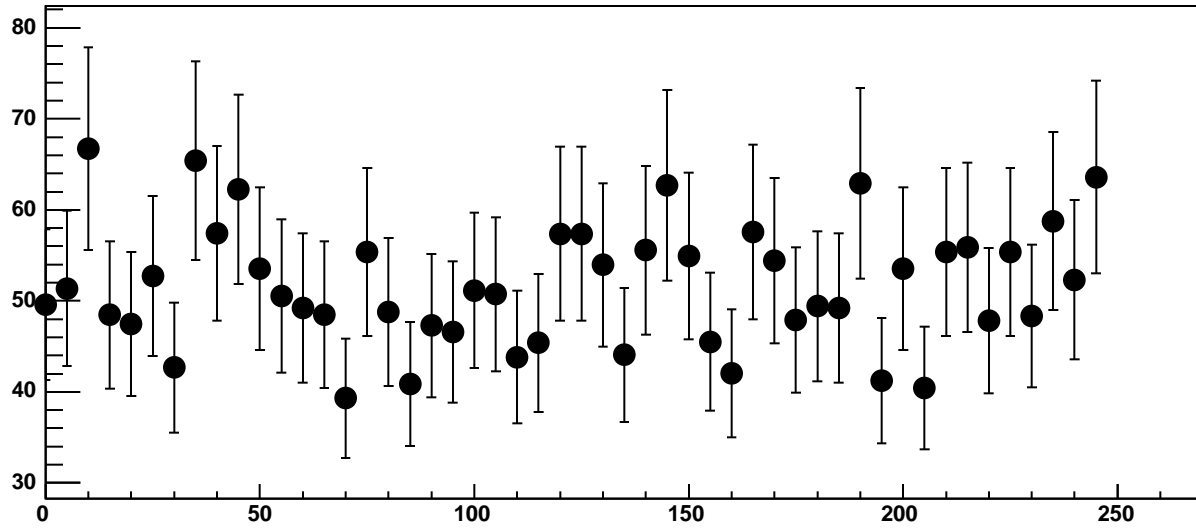


Chip 6, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

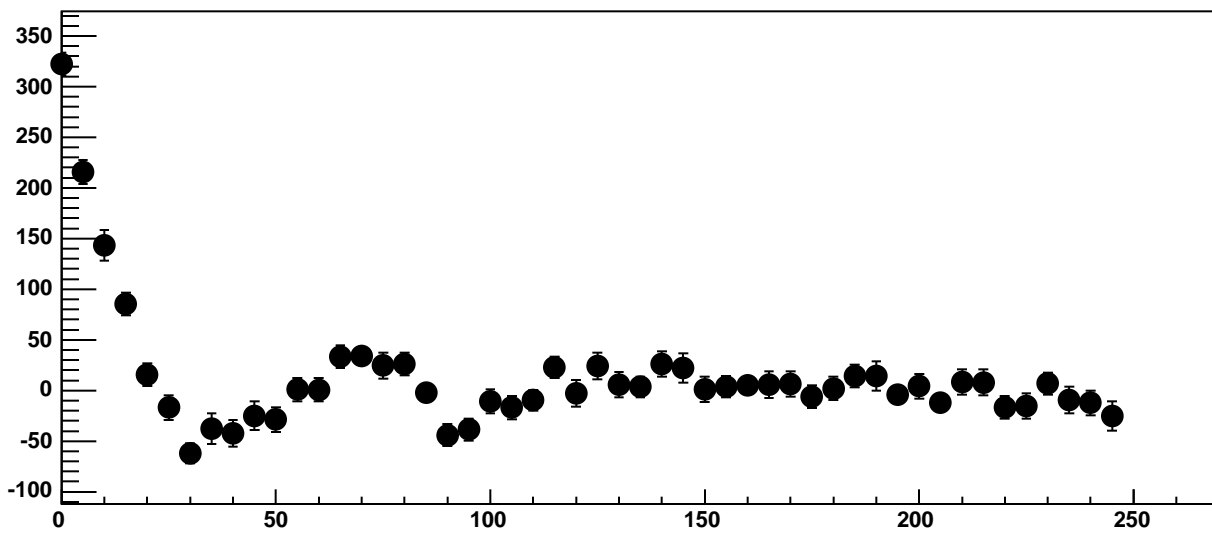


$\chi^2 / \text{ndf}$	221.4 / 41
p0	-781.2 ± 3.867
p1	92.64 ± 0.5905
p2	-5.555e+08 ± 7.397e+06
p3	4.847e+07 ± 3.678e+05
p4	10.54 ± 0.1182

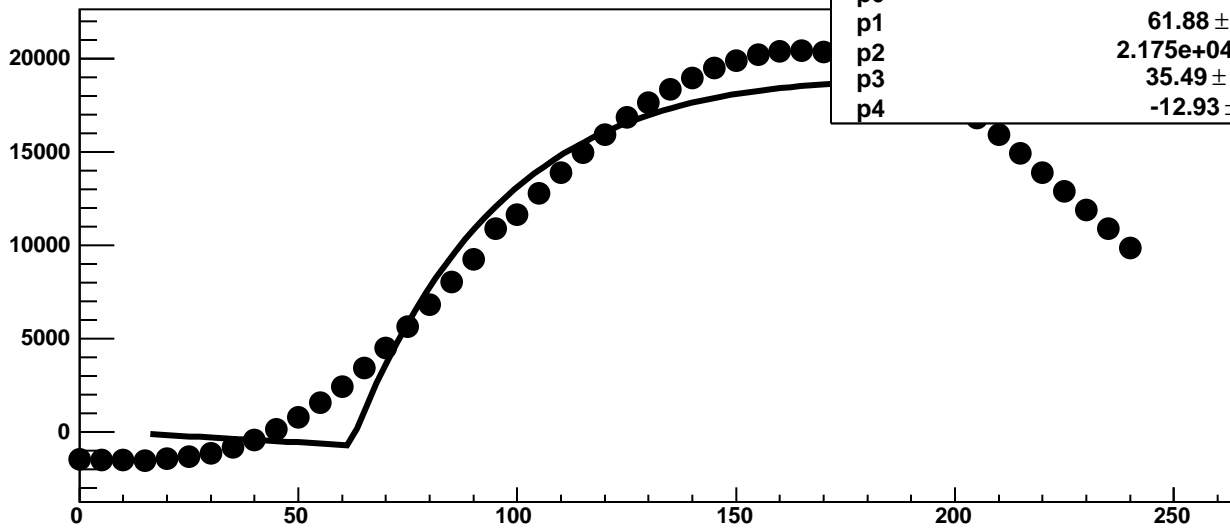
Chip 6, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

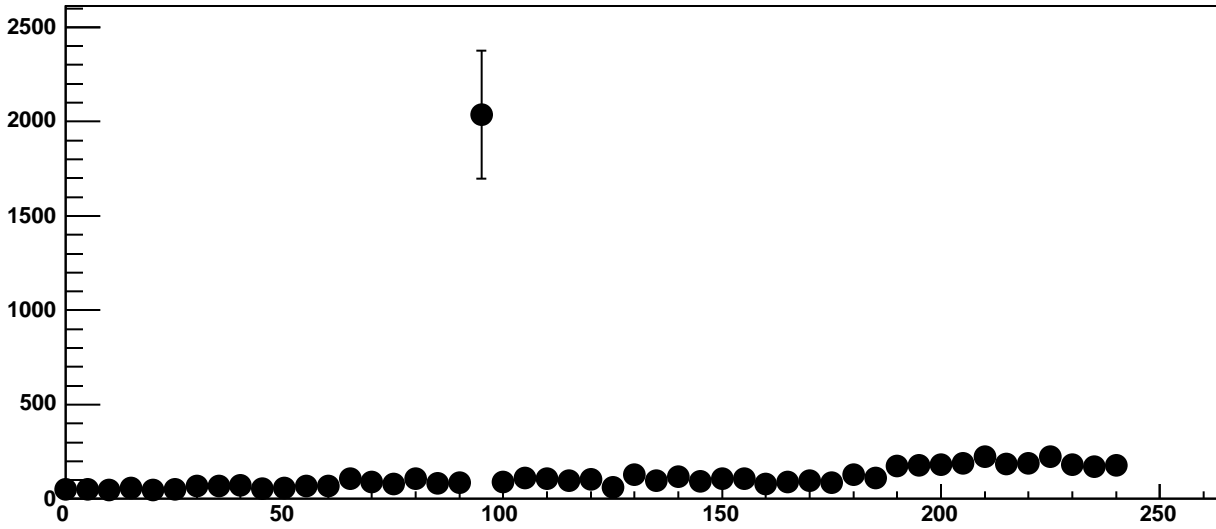


Chip 6, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

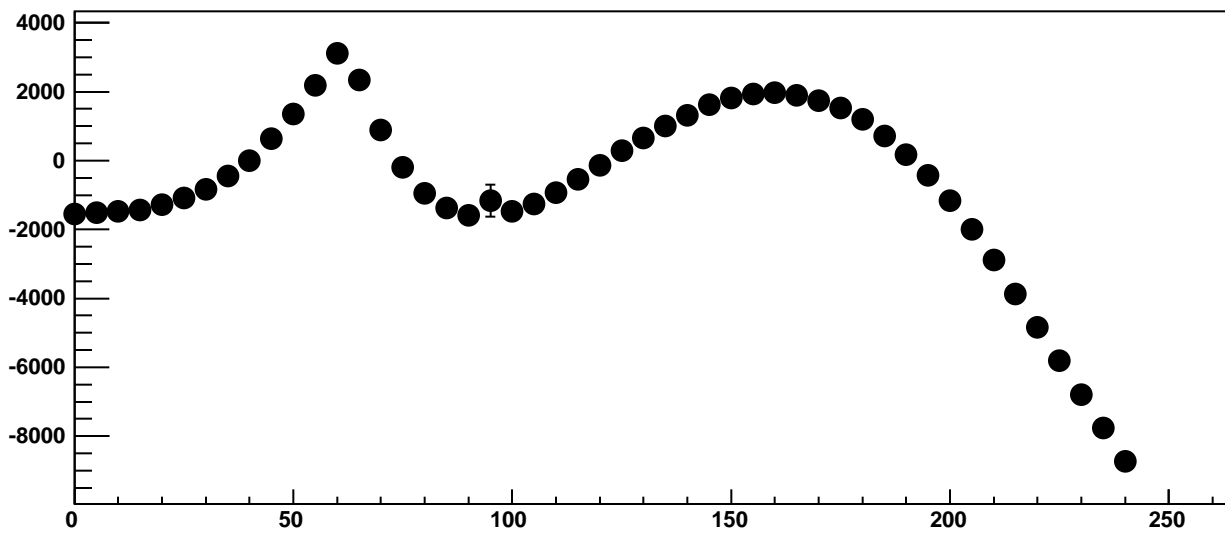


$\chi^2 / \text{ndf}$	3.488e+05 / 41
p0	-697.8 ± 6.799
p1	61.88 ± 0.03021
p2	2.175e+04 ± 34.45
p3	35.49 ± 0.07103
p4	-12.93 ± 0.2036

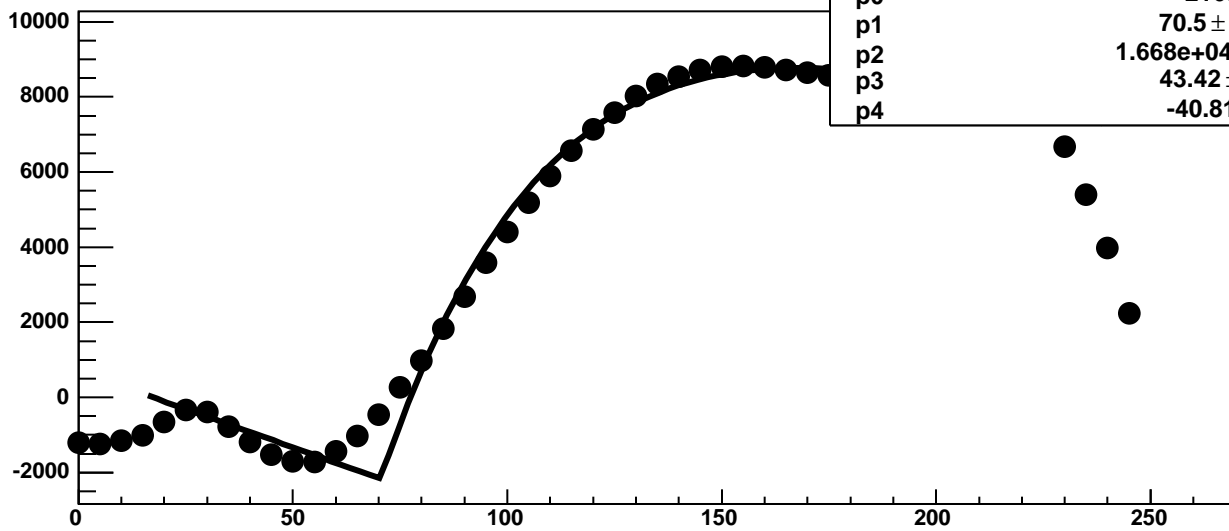
Chip 6, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



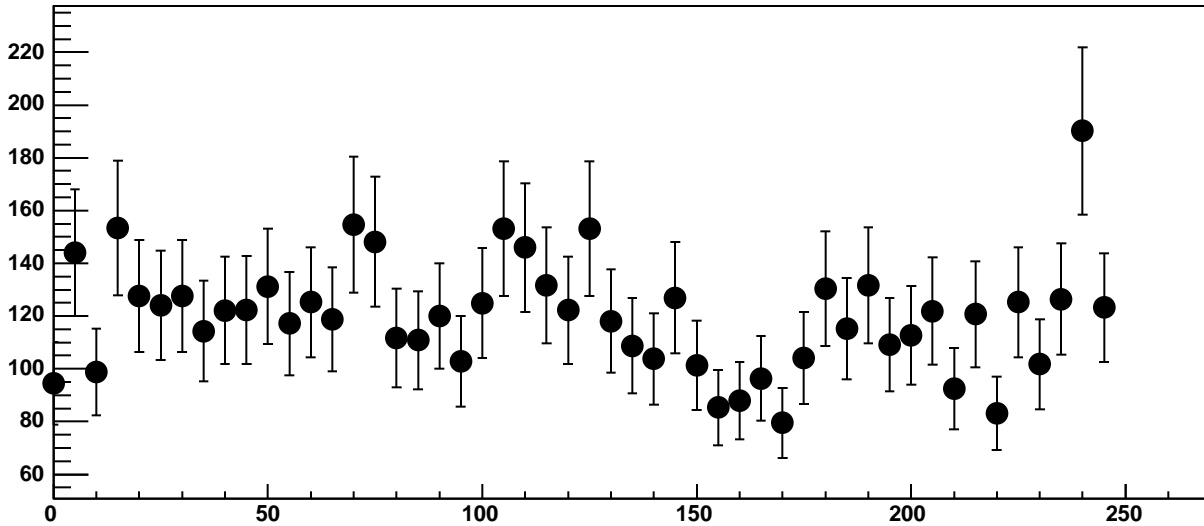
Chip 6, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



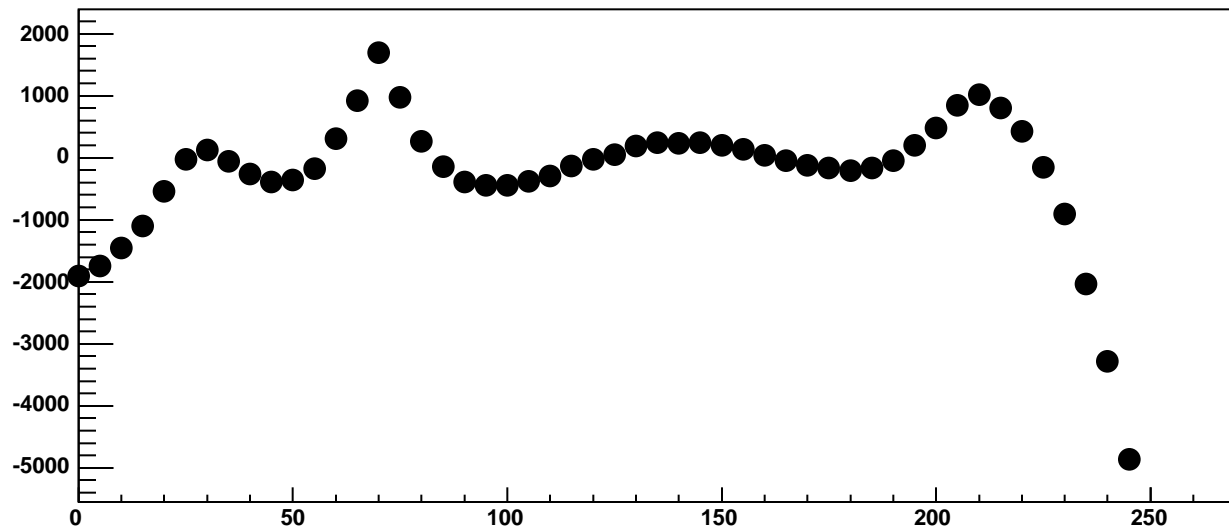
Chip 6, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



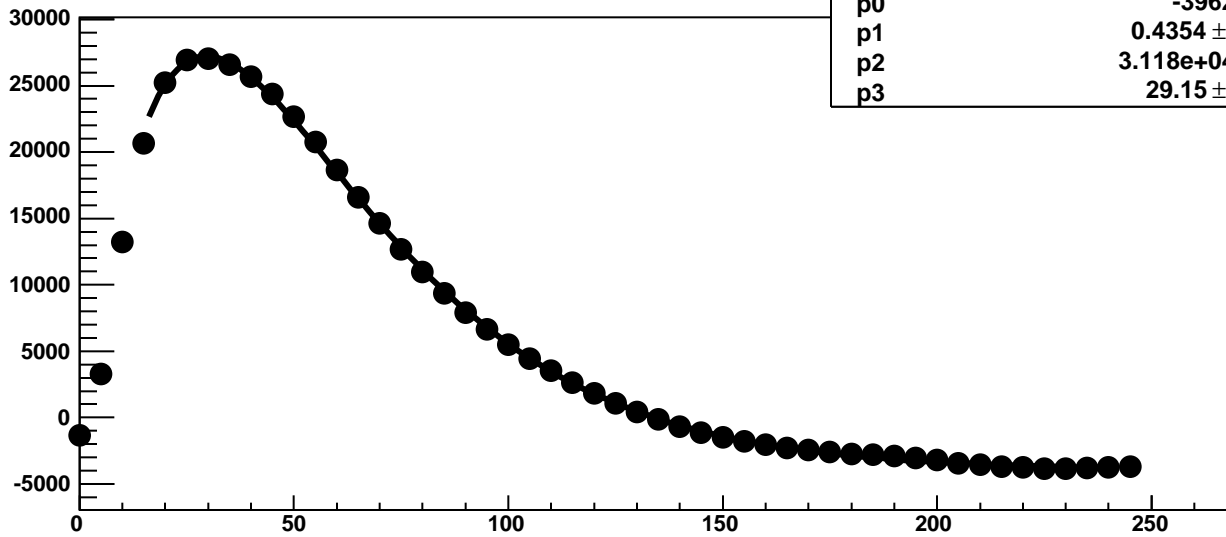
Chip 6, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

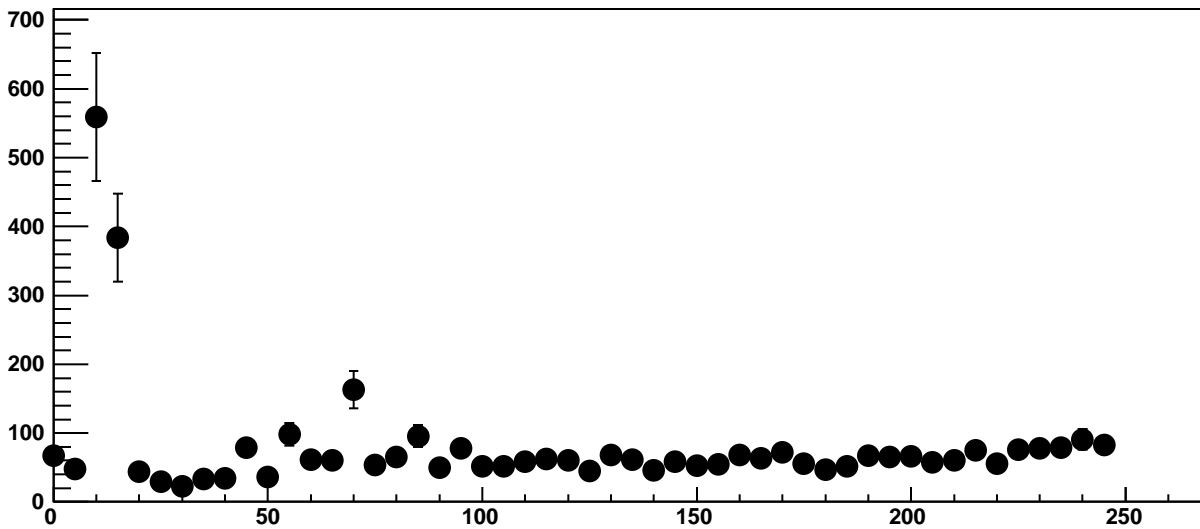


Chip 6, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

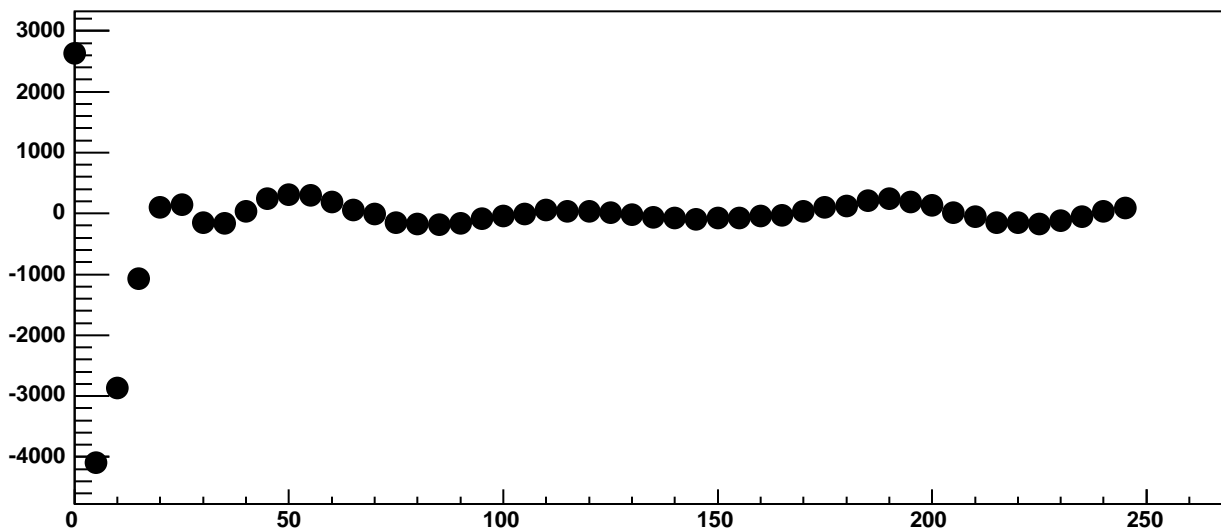


$\chi^2 / \text{ndf}$	6295 / 42
p0	$-3962 \pm 4.204$
p1	$0.4354 \pm 0.02105$
p2	$3.118\text{e}+04 \pm 4.787$
p3	$29.15 \pm 0.01203$

Chip 6, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

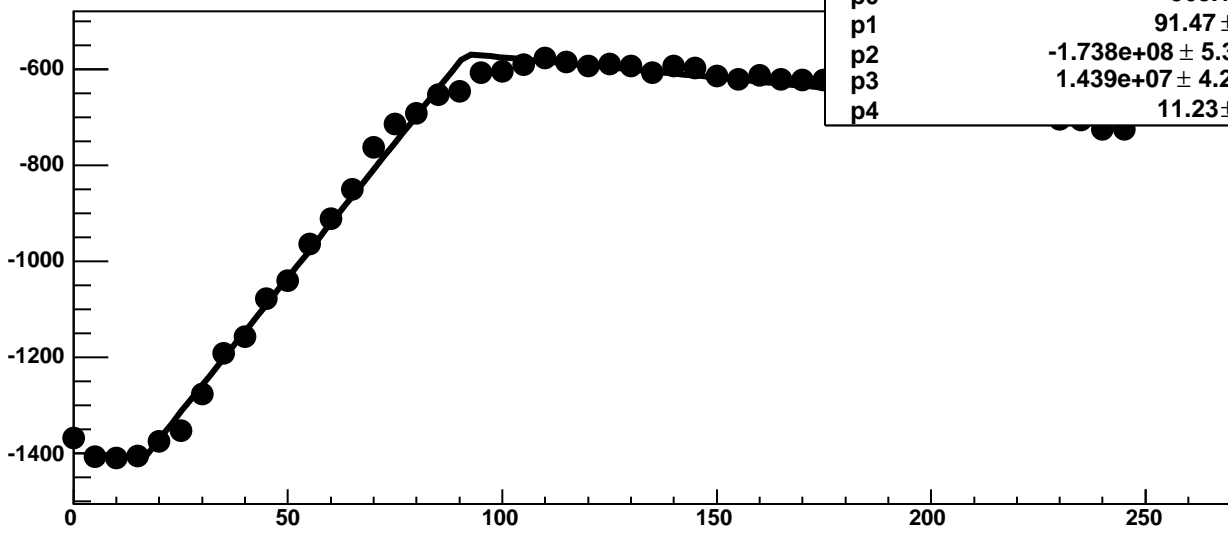


Chip 6, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



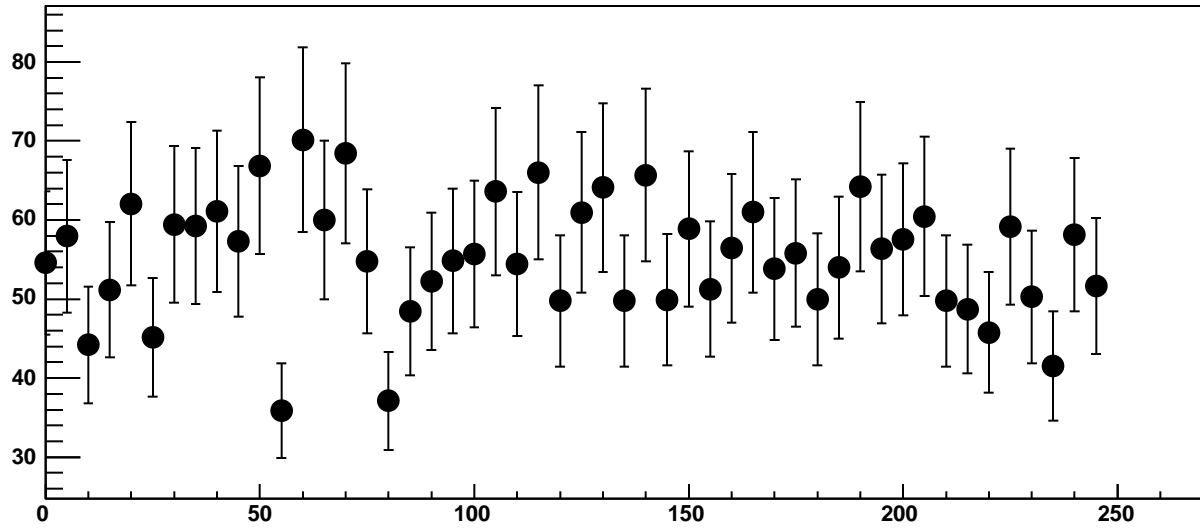


Chip 6, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

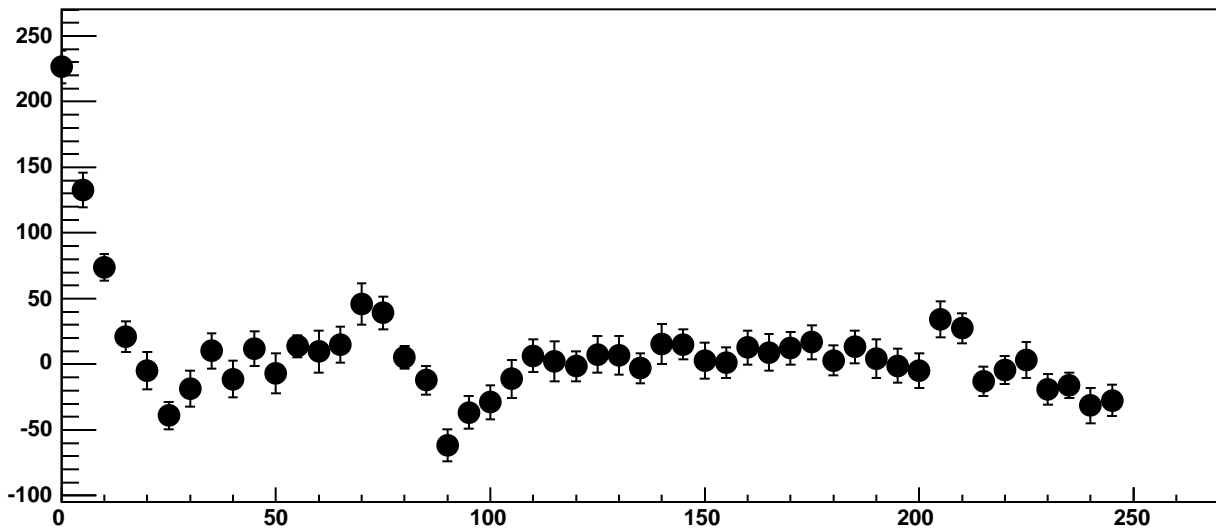


$\chi^2 / \text{ndf}$	120.3 / 41
p0	-568.1 ± 4.433
p1	91.47 ± 0.6078
p2	-1.738e+08 ± 5.398e+06
p3	1.439e+07 ± 4.212e+05
p4	11.23 ± 0.1273

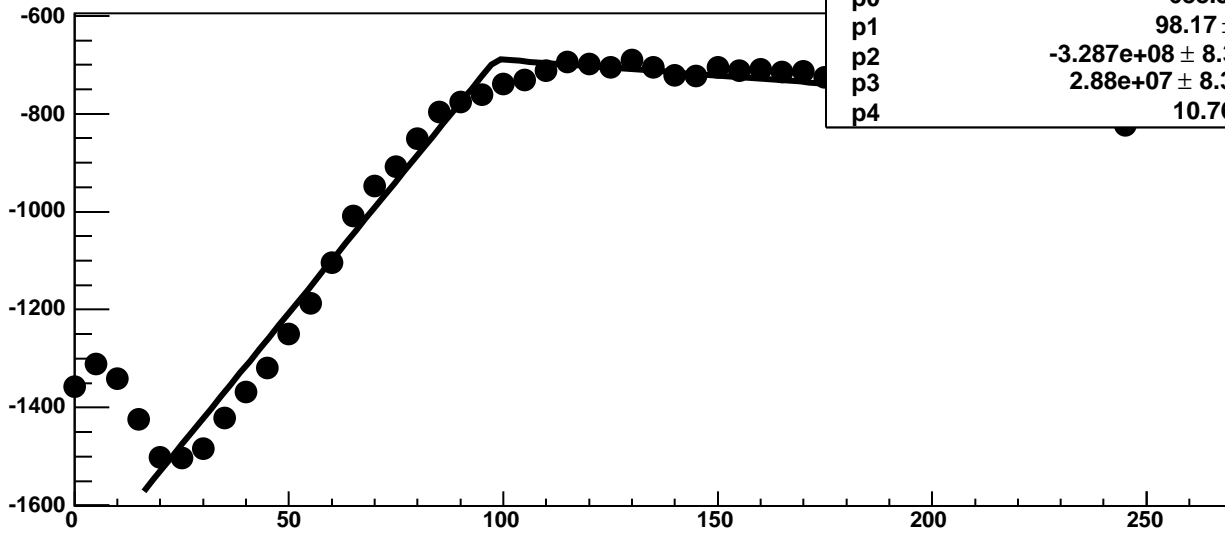
Chip 6, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

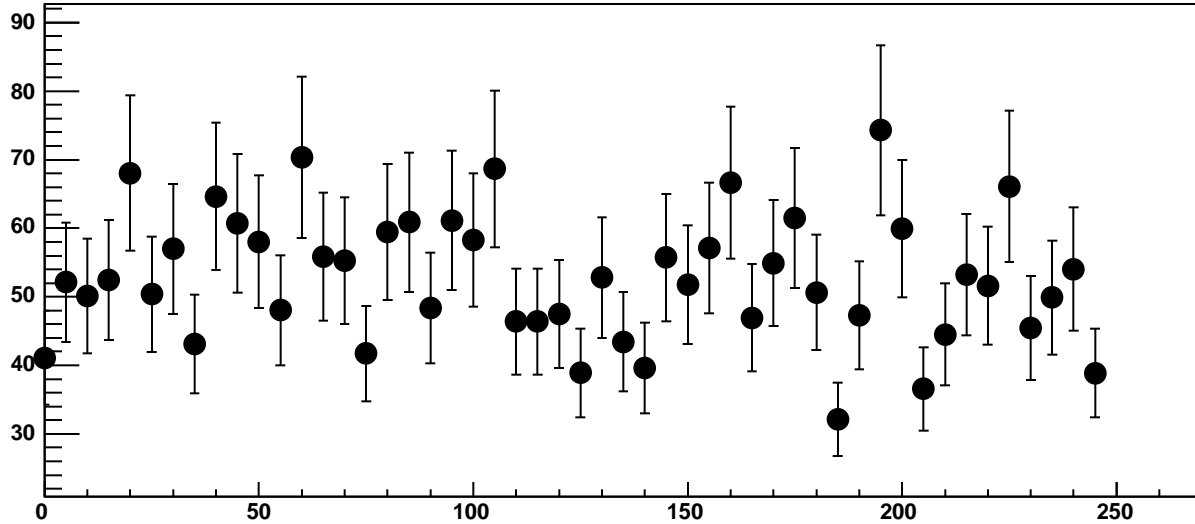


Chip 6, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

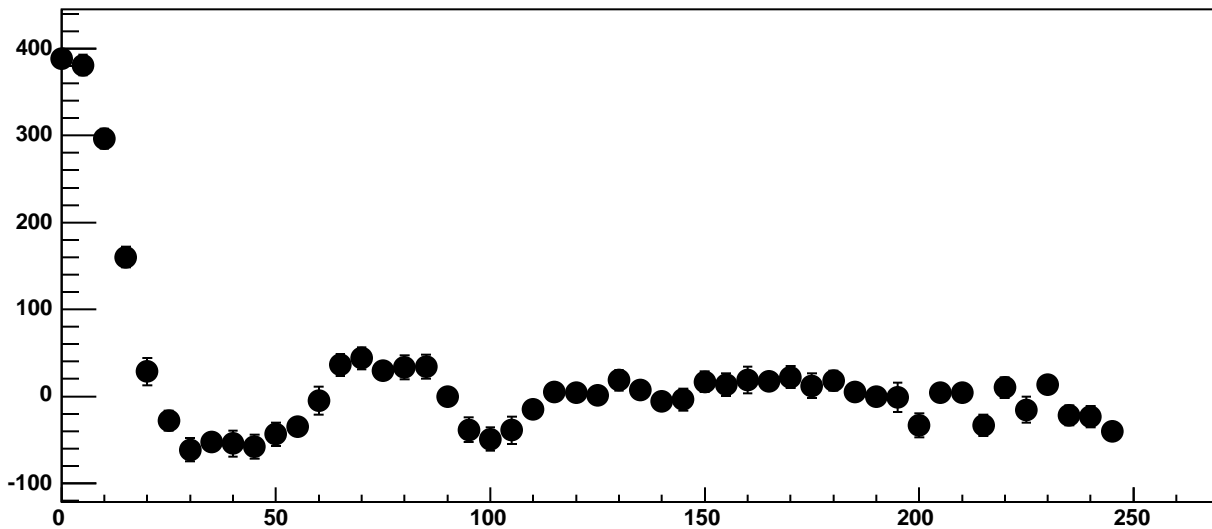


$\chi^2 / \text{ndf}$	400.1 / 41
p0	$-688.3 \pm 3.905$
p1	$98.17 \pm 0.5933$
p2	$-3.287\text{e}+08 \pm 8.331\text{e}+06$
p3	$2.88\text{e}+07 \pm 8.397\text{e}+05$
p4	$10.76 \pm 0.111$

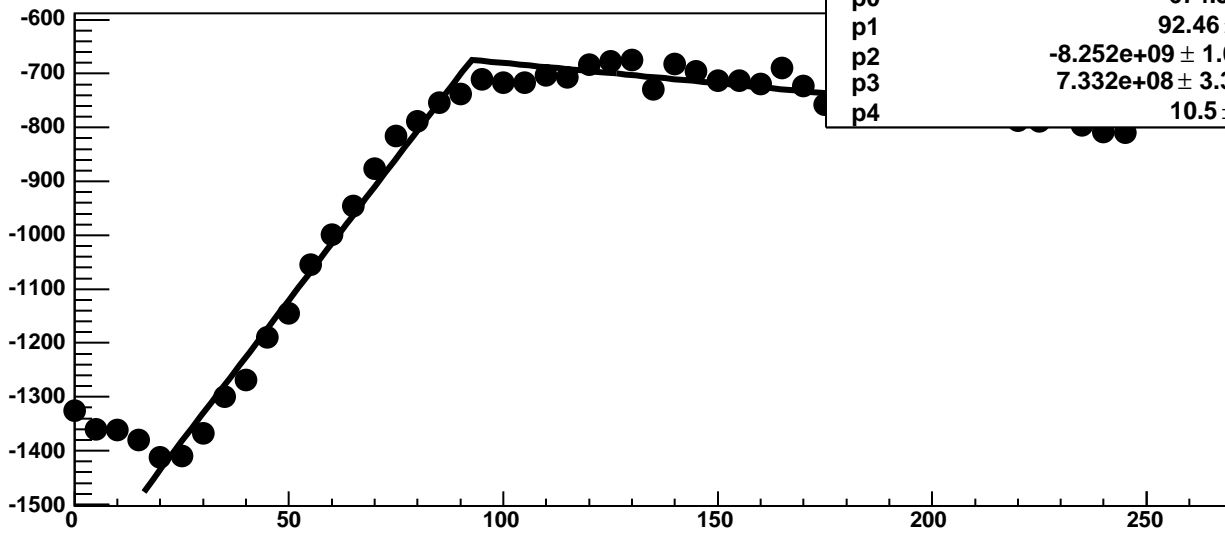
Chip 6, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

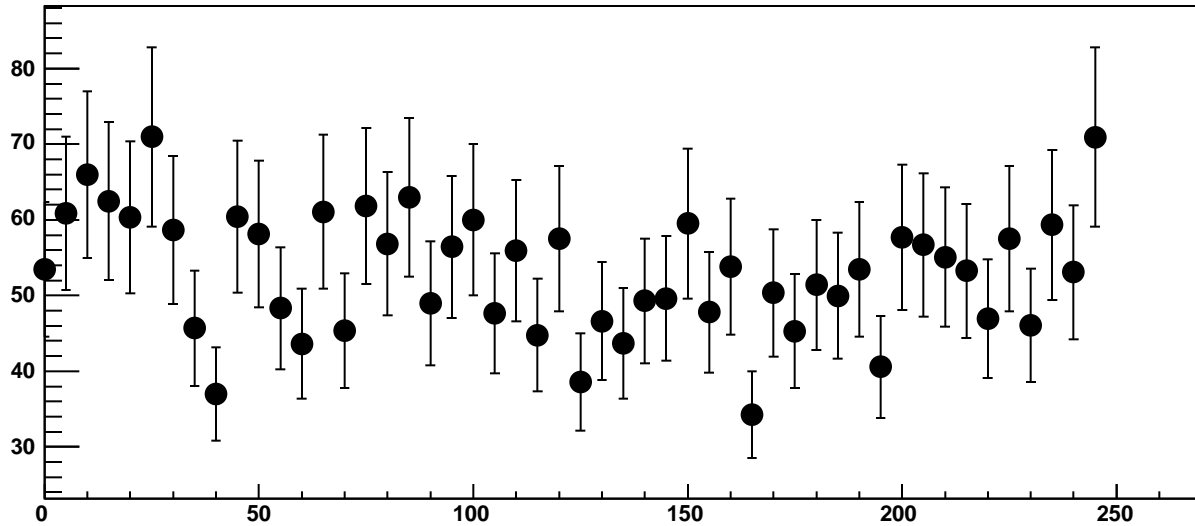


Chip 6, Channel 12, Enable 4, DAC=1600, ADC Mean vs Hold

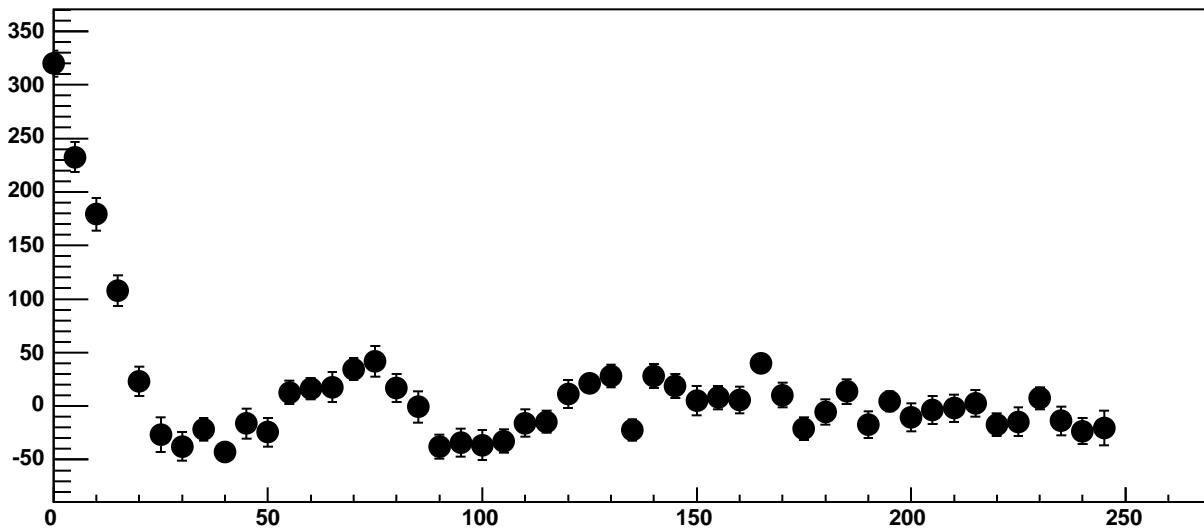


$\chi^2 / \text{ndf}$	241 / 41
p0	$-674.5 \pm 3.953$
p1	$92.46 \pm 0.6701$
p2	$-8.252\text{e}+09 \pm 1.087\text{e}+08$
p3	$7.332\text{e}+08 \pm 3.318\text{e}+05$
p4	$10.5 \pm 0.1403$

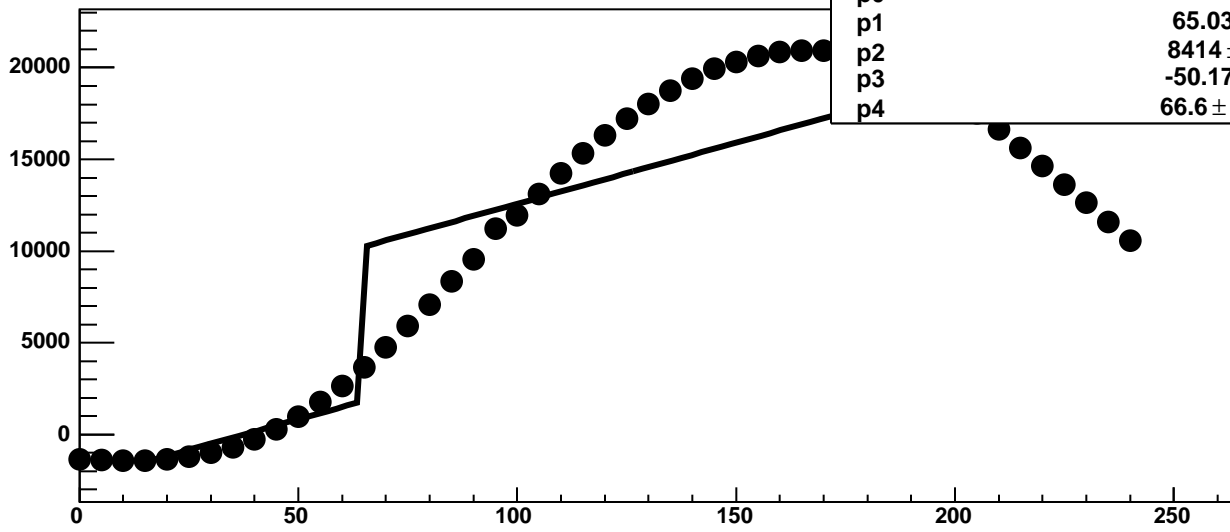
Chip 6, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold

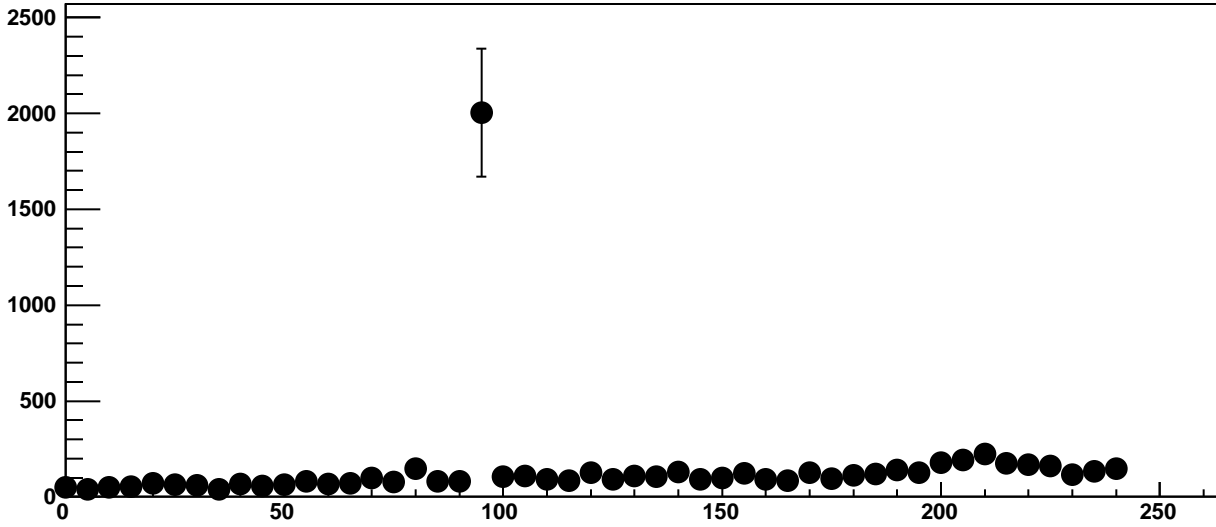


Chip 6, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

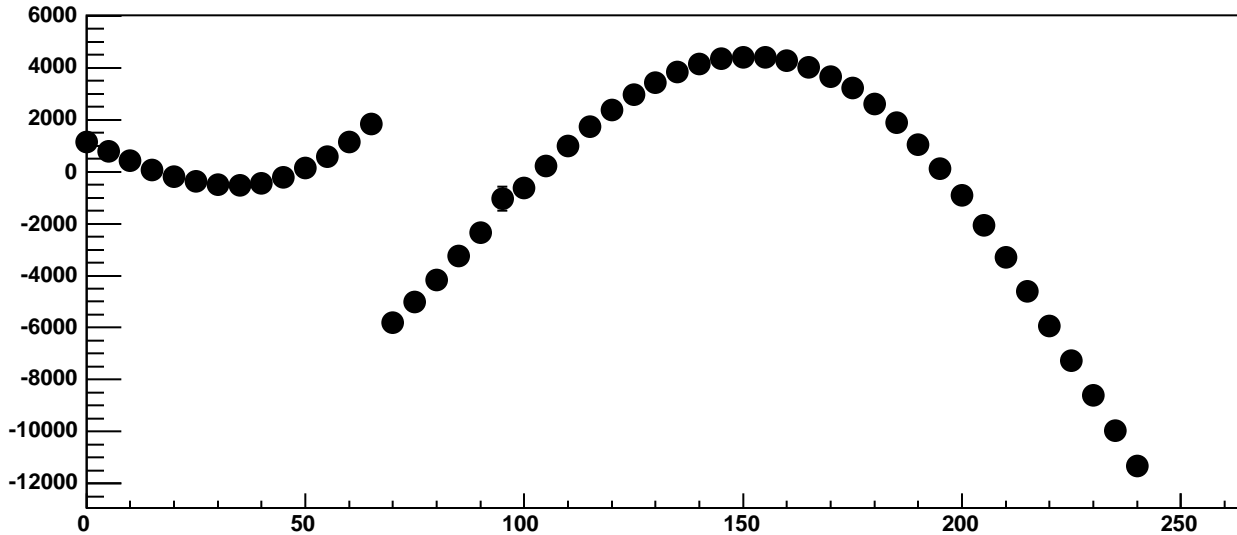


$\chi^2 / \text{ndf}$	9.78e+05 / 41
p0	1837 ± 1.408
p1	65.03 ± 0.568
p2	8414 ± 0.8297
p3	-50.17 ± 17.46
p4	66.6 ± 0.09079

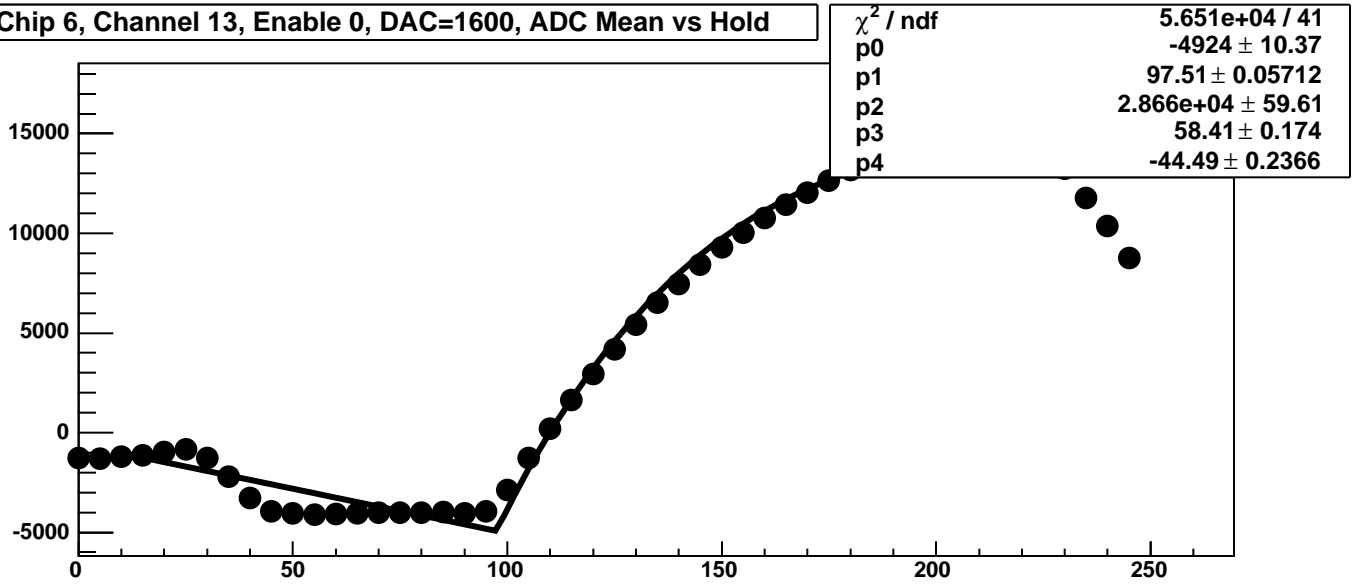
Chip 6, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold



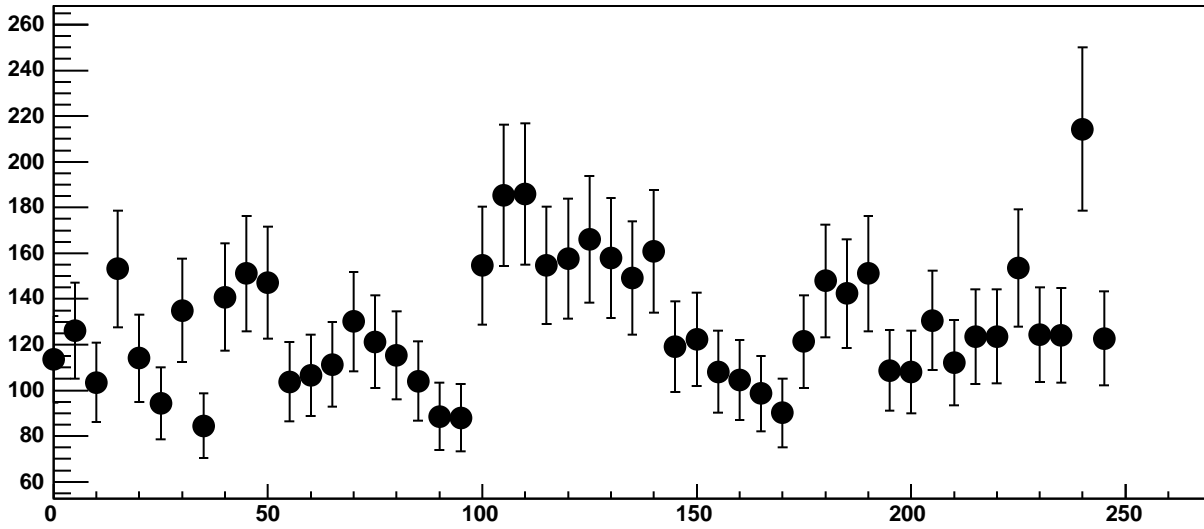
Chip 6, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



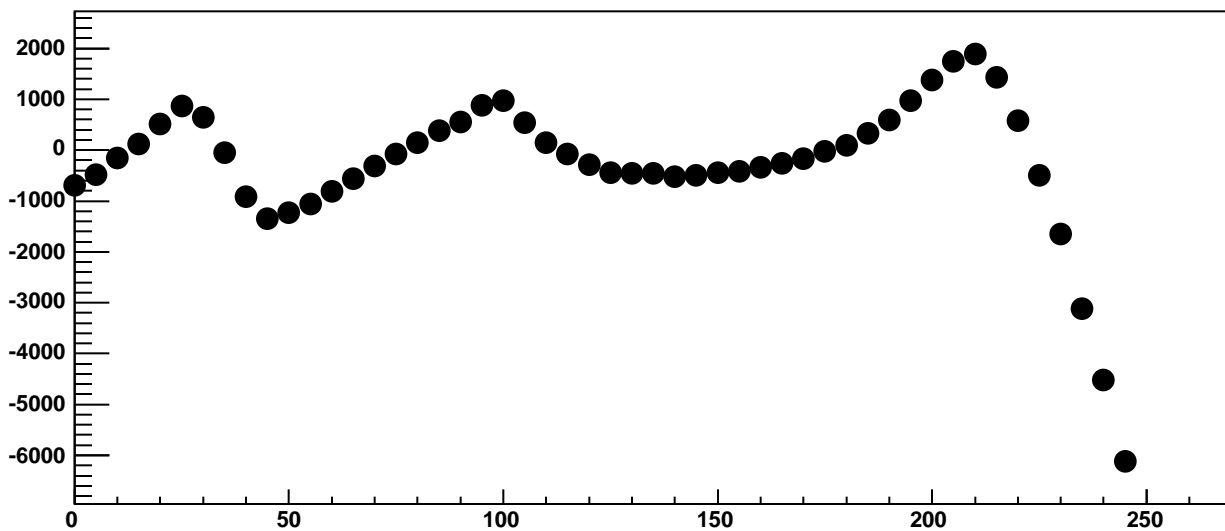
Chip 6, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold



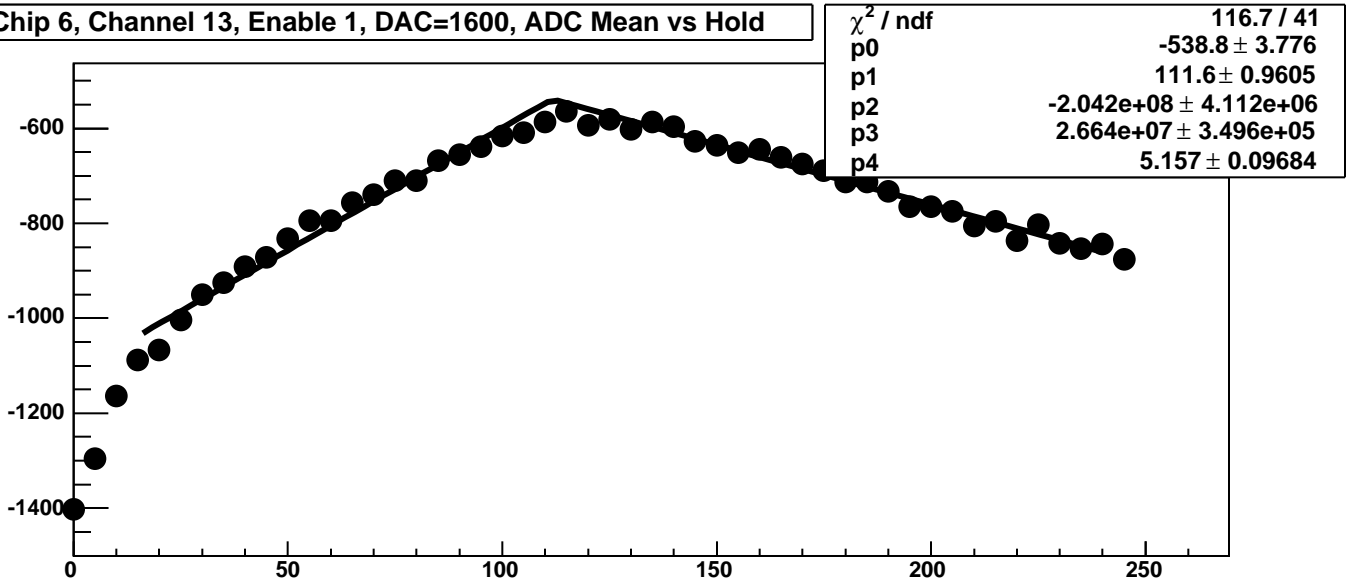
Chip 6, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



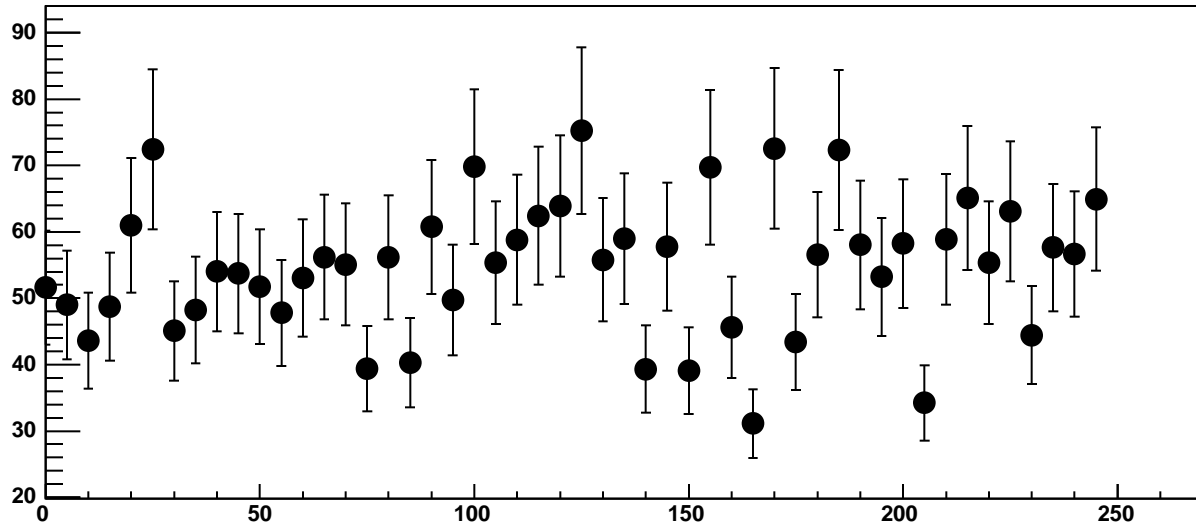
Chip 6, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold



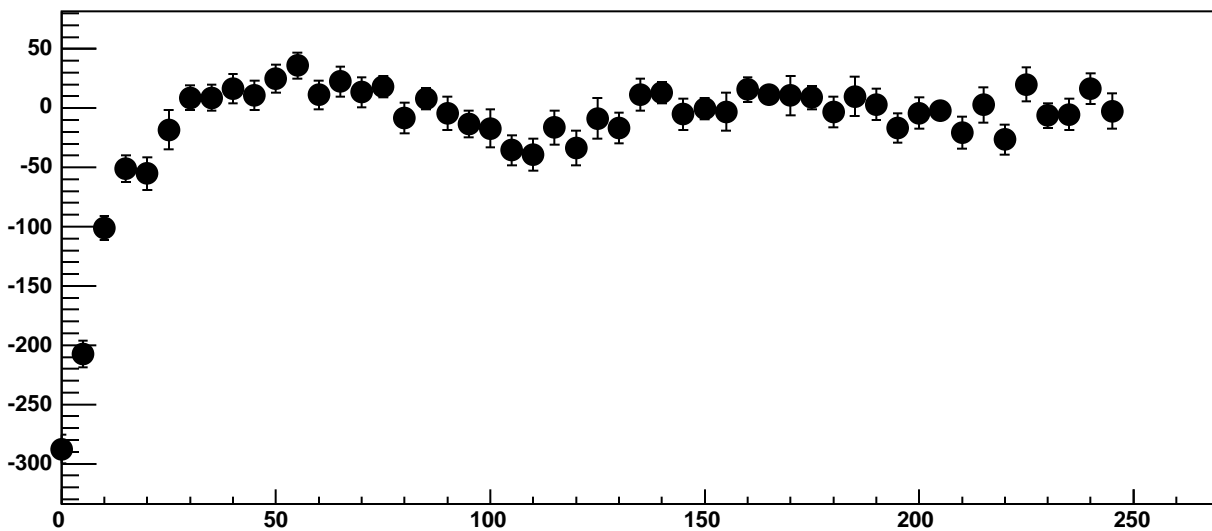
Chip 6, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold



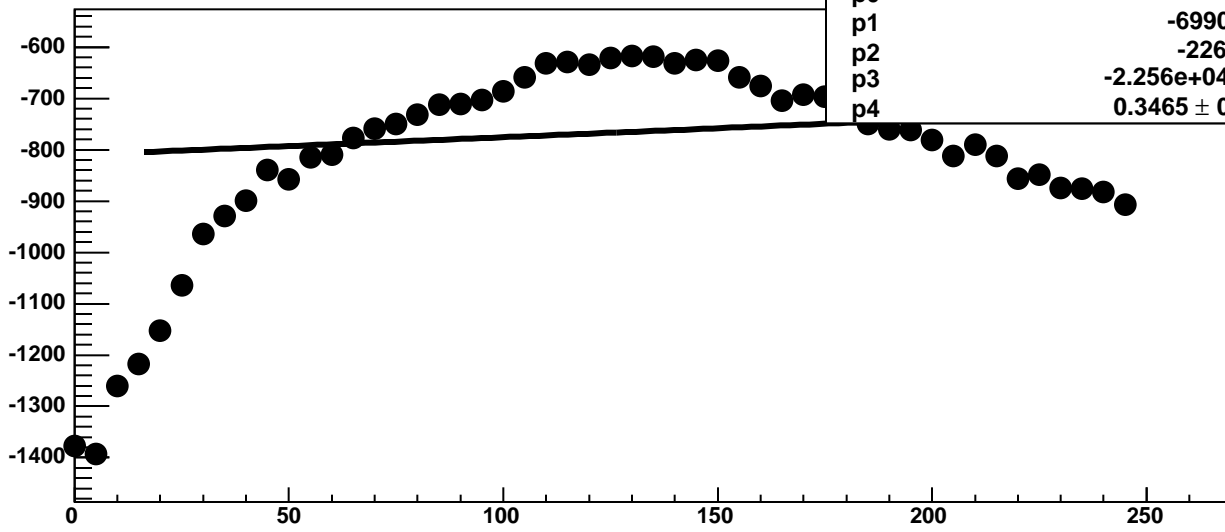
Chip 6, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold

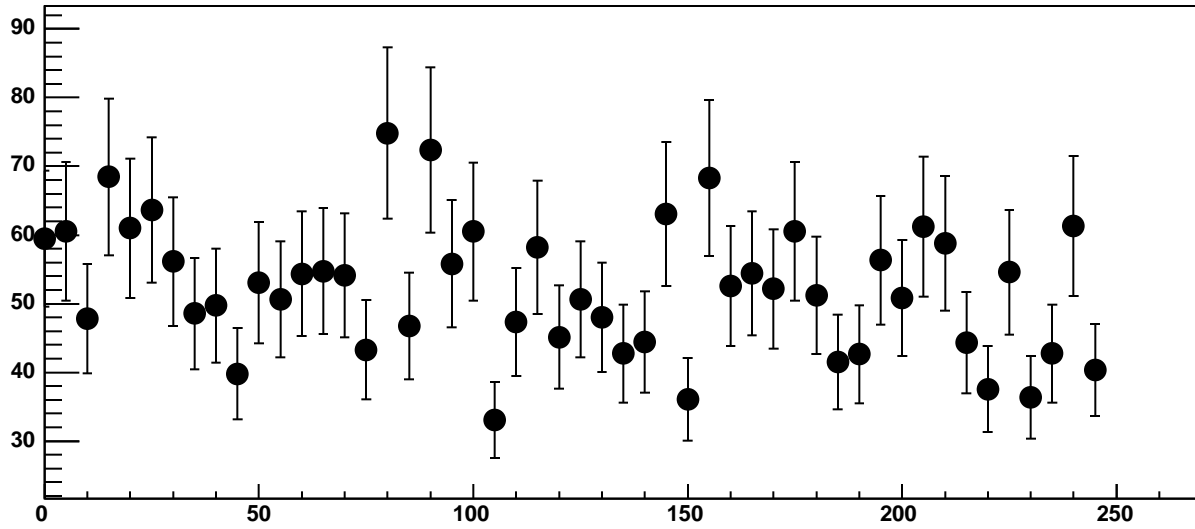


Chip 6, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

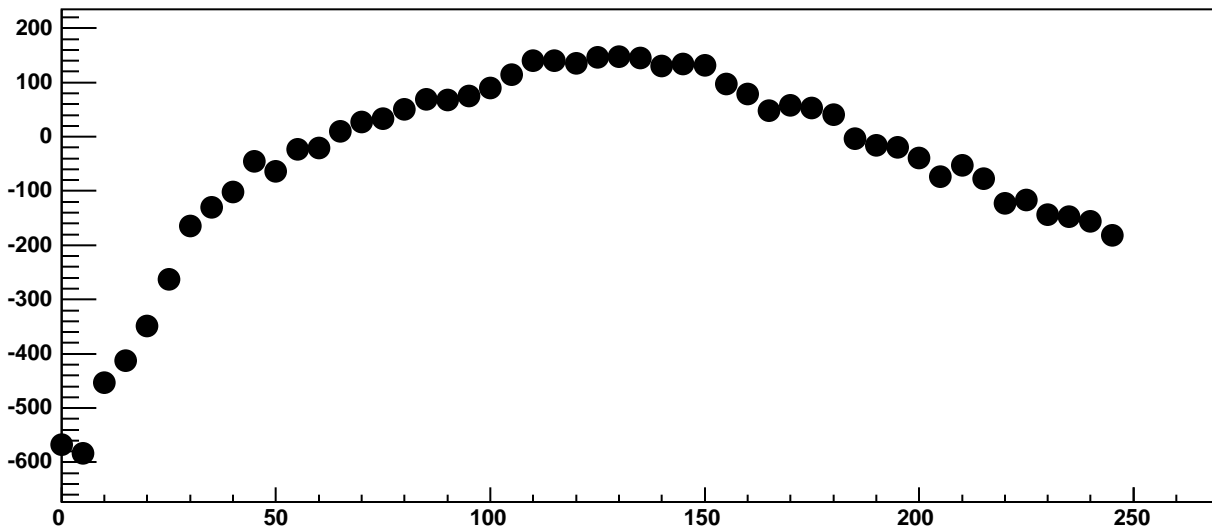


$\chi^2 / \text{ndf}$	5168 / 41
p0	-971.3 $\pm$ 8.247
p1	-6990 $\pm$ 21.86
p2	-2261 $\pm$ 10.9
p3	-2.256e+04 $\pm$ 2049
p4	0.3465 $\pm$ 0.001158

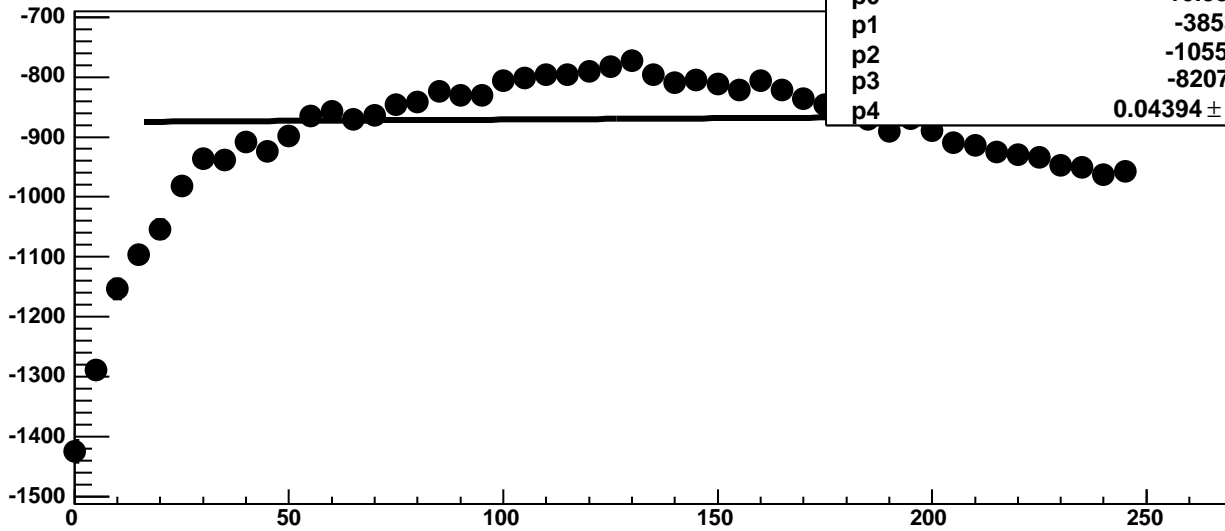
Chip 6, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

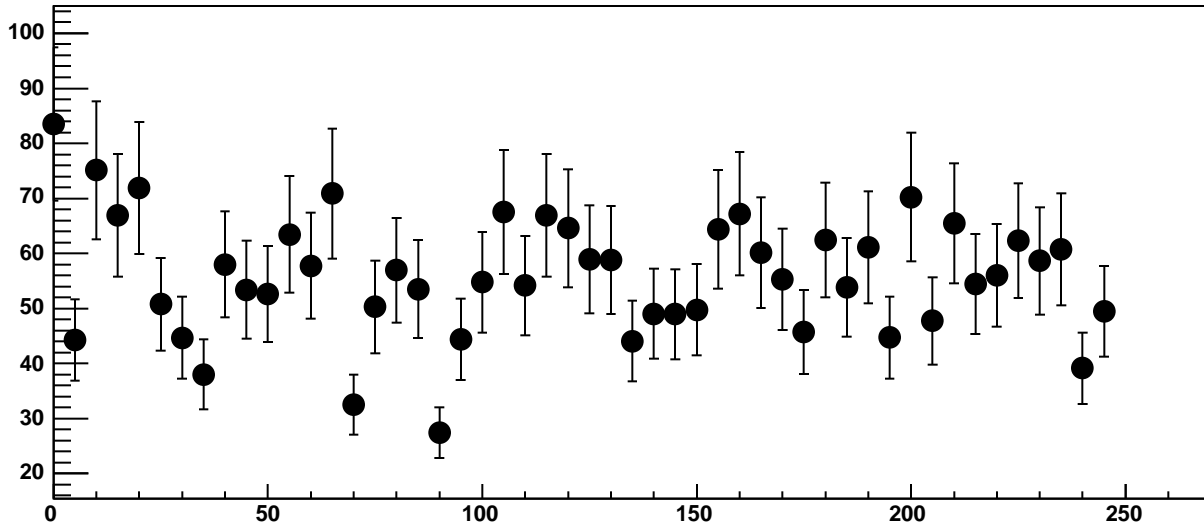


Chip 6, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

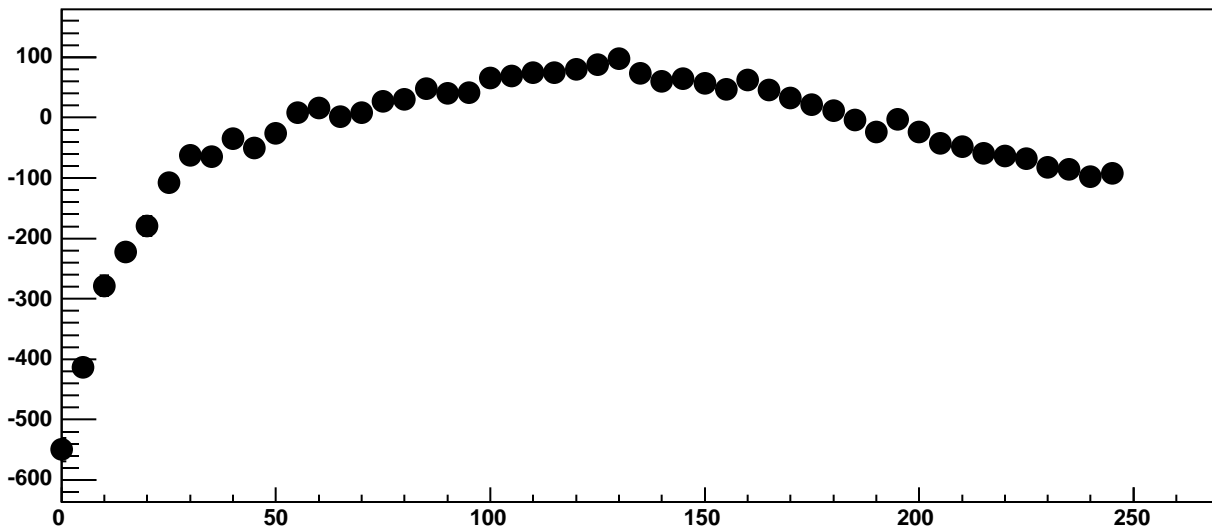


$\chi^2 / \text{ndf}$	1331 / 41
p0	$10.55 \pm 8.279$
p1	$-3853 \pm 324$
p2	$-1055 \pm 6.334$
p3	$-8207 \pm 1478$
p4	$0.04394 \pm 0.00208$

Chip 6, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

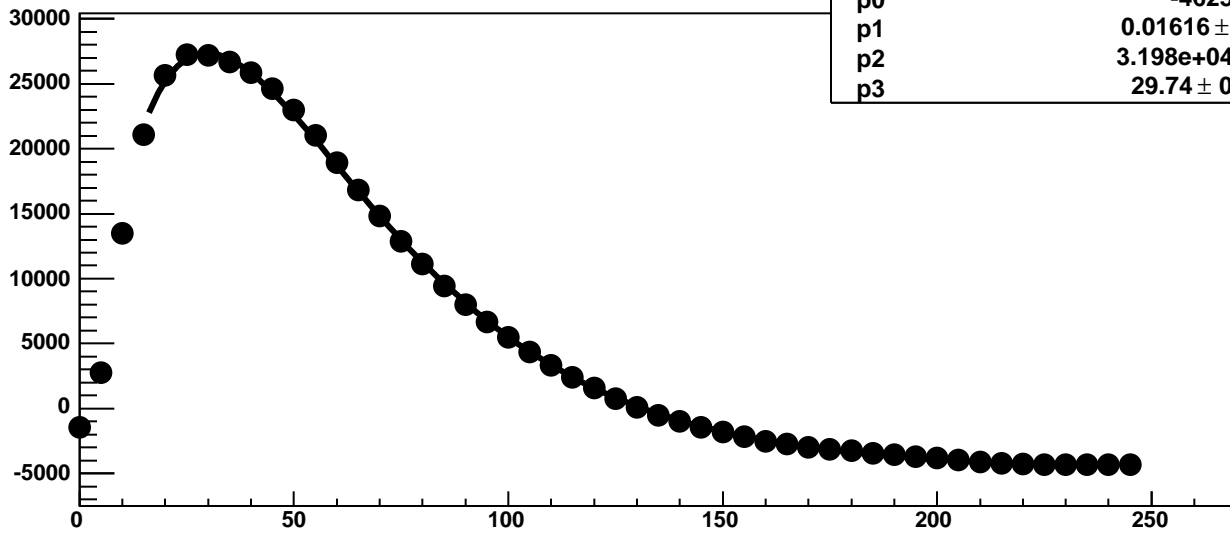


Chip 6, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

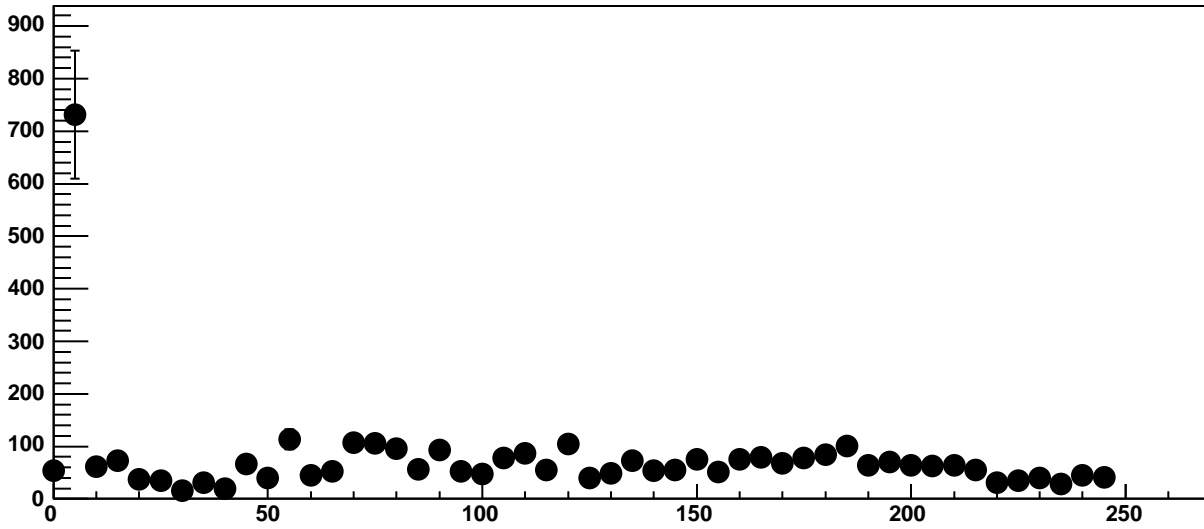




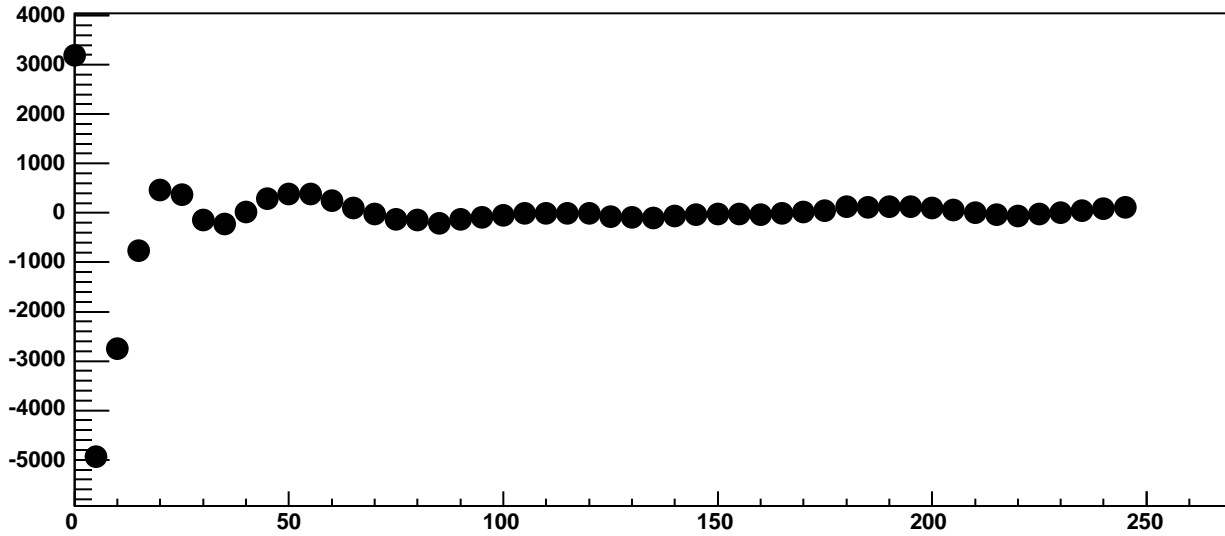
Chip 6, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold



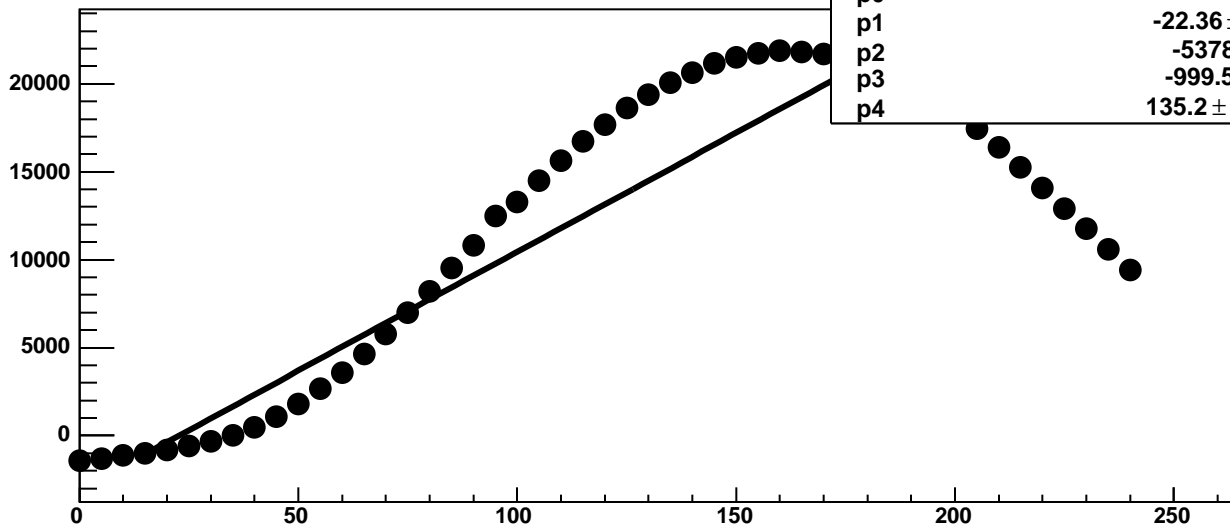
Chip 6, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold

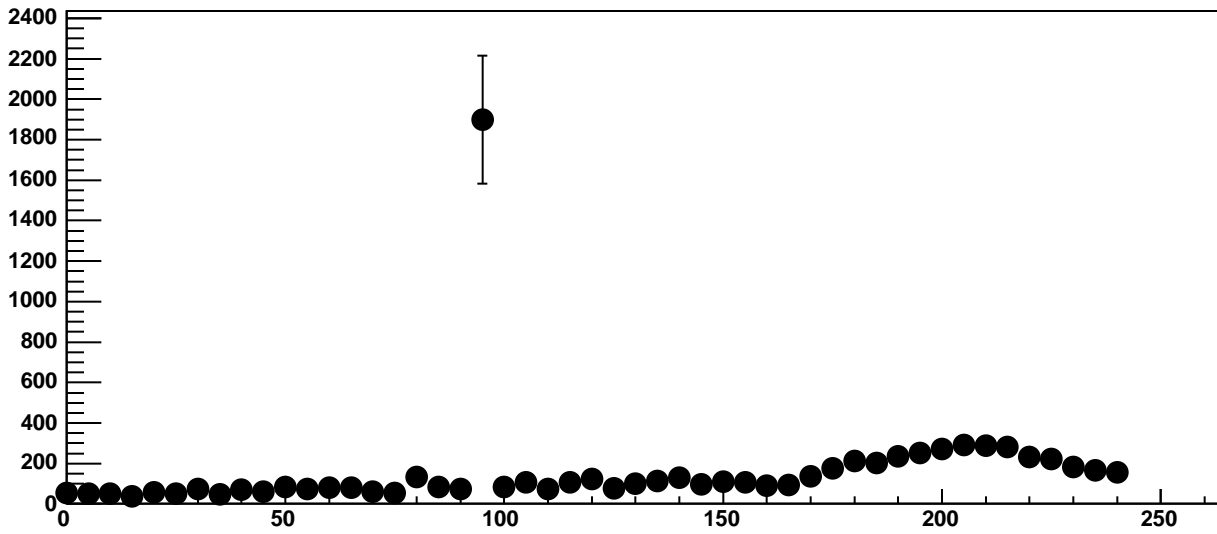


Chip 6, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

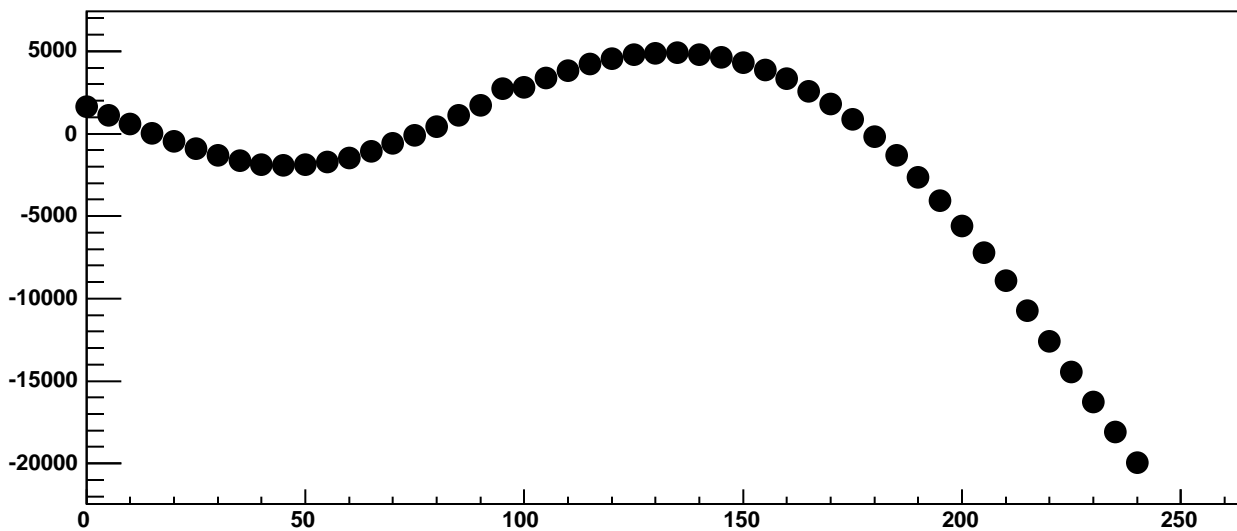


$\chi^2 / \text{ndf}$	1.474e+06 / 41
p0	-710.6 ± 18.1
p1	-22.36 ± 0.1125
p2	-5378 ± 19.09
p3	-999.5 ± 13.18
p4	135.2 ± 0.09697

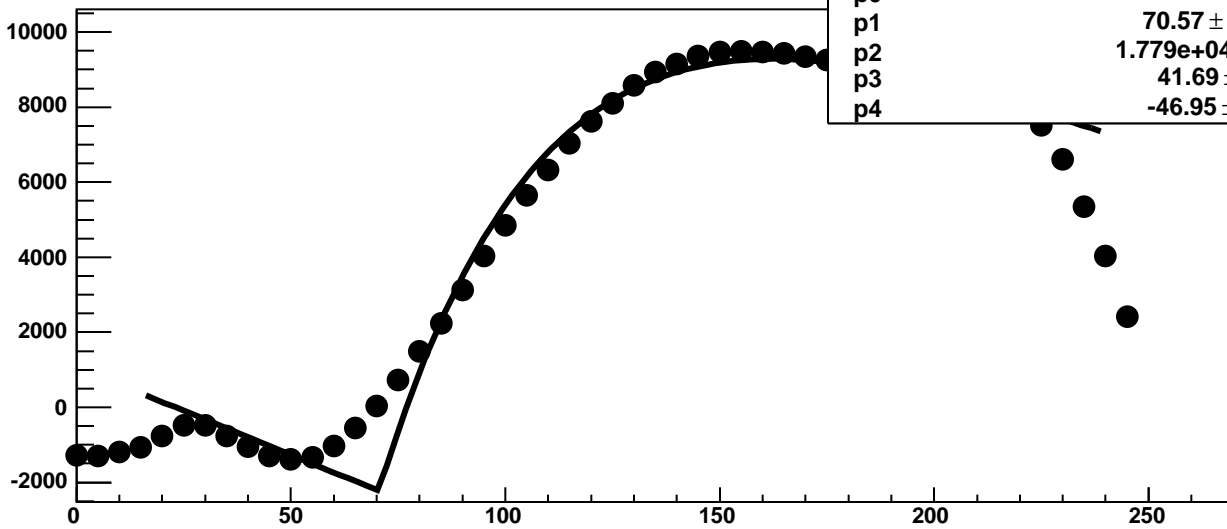
Chip 6, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

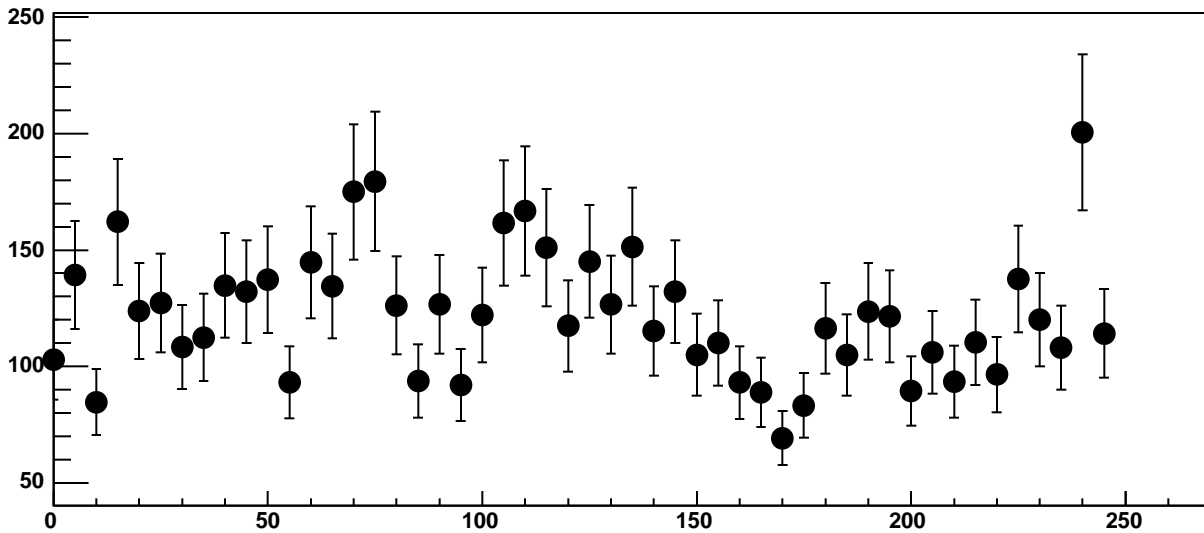


Chip 6, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

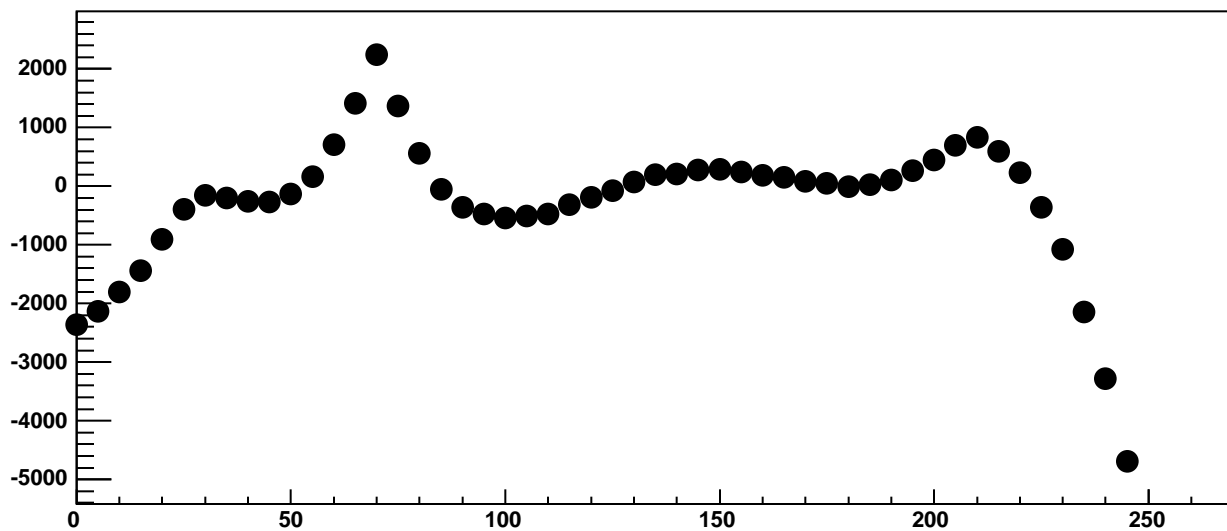


$\chi^2 / \text{ndf}$	3.015e+04 / 41
p0	-2230 ± 11.06
p1	70.57 ± 0.07047
p2	1.779e+04 ± 66.81
p3	41.69 ± 0.1948
p4	-46.95 ± 0.3406

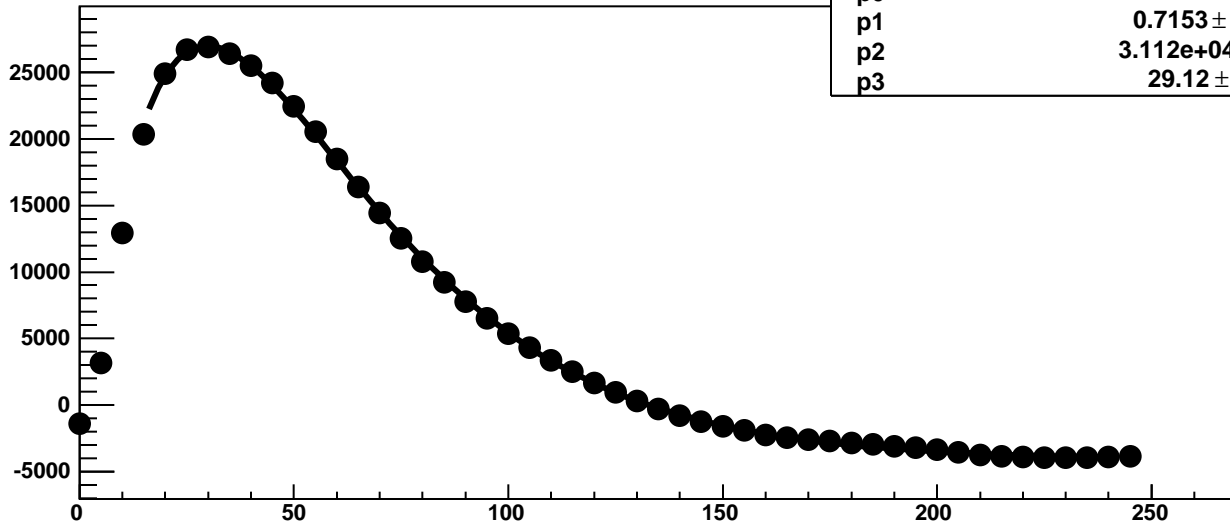
Chip 6, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

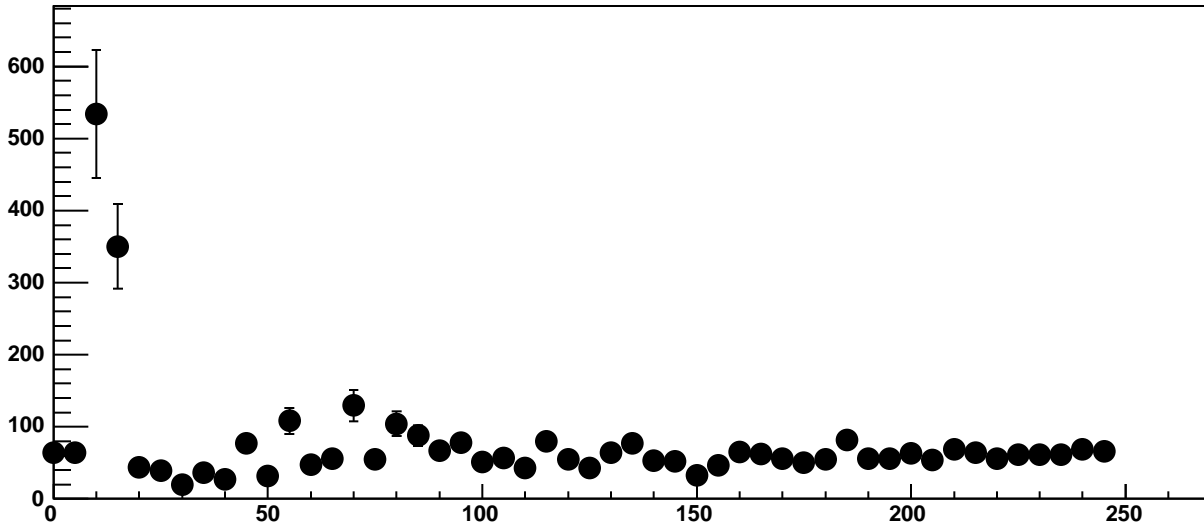


Chip 6, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold

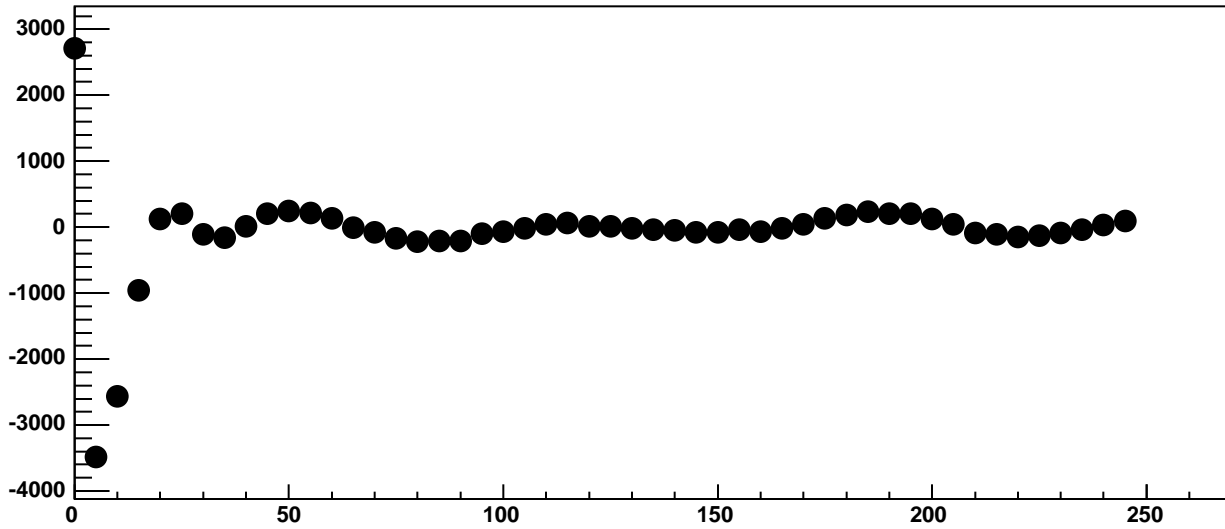


$\chi^2 / \text{ndf}$	5510 / 42
p0	-4119 ± 3.927
p1	0.7153 ± 0.02026
p2	3.112e+04 ± 4.534
p3	29.12 ± 0.01168

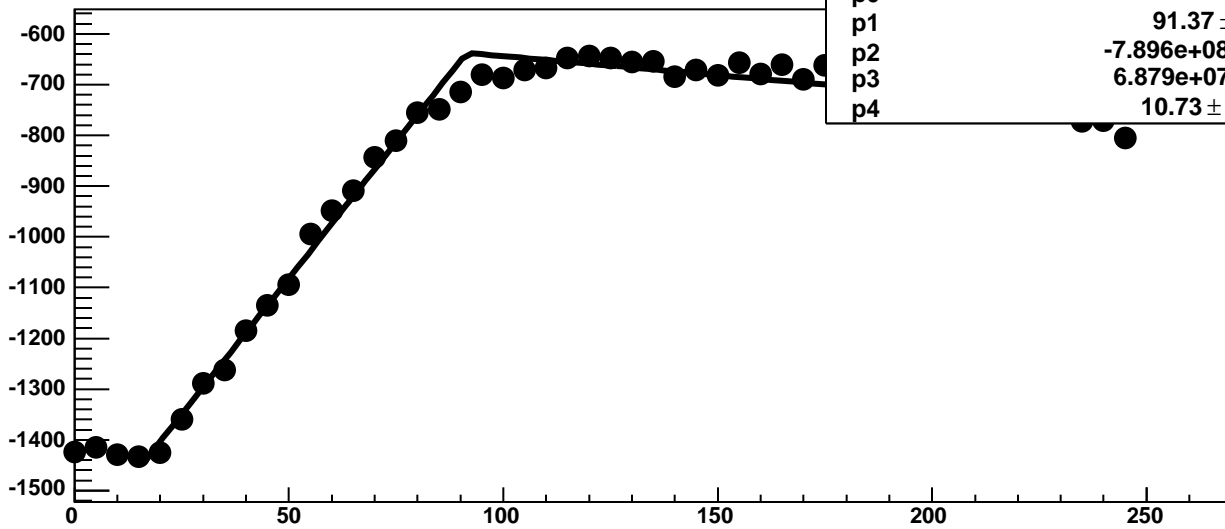
Chip 6, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

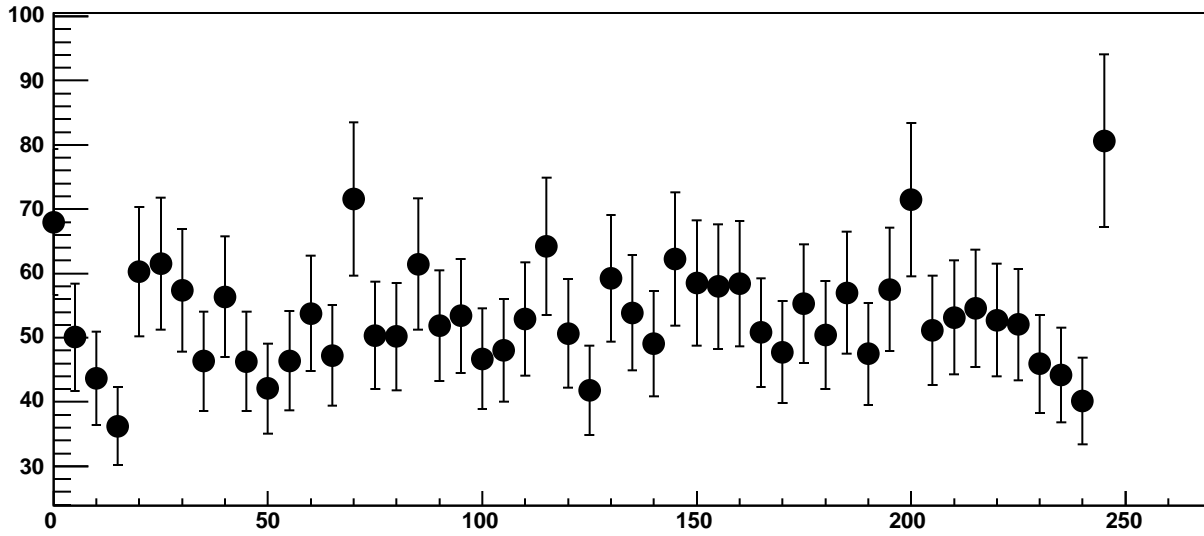


Chip 6, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

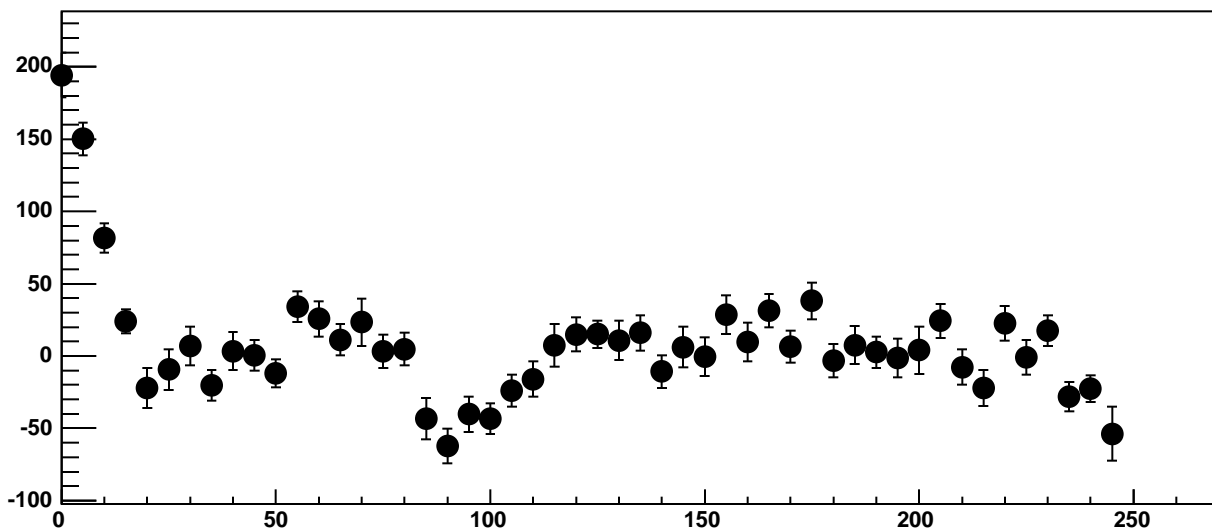


$\chi^2 / \text{ndf}$	162.9 / 41
p0	$-637.4 \pm 3.737$
p1	$91.37 \pm 0.5554$
p2	$-7.896e+08 \pm 1.414$
p3	$6.879e+07 \pm 1.414$
p4	$10.73 \pm 0.04453$

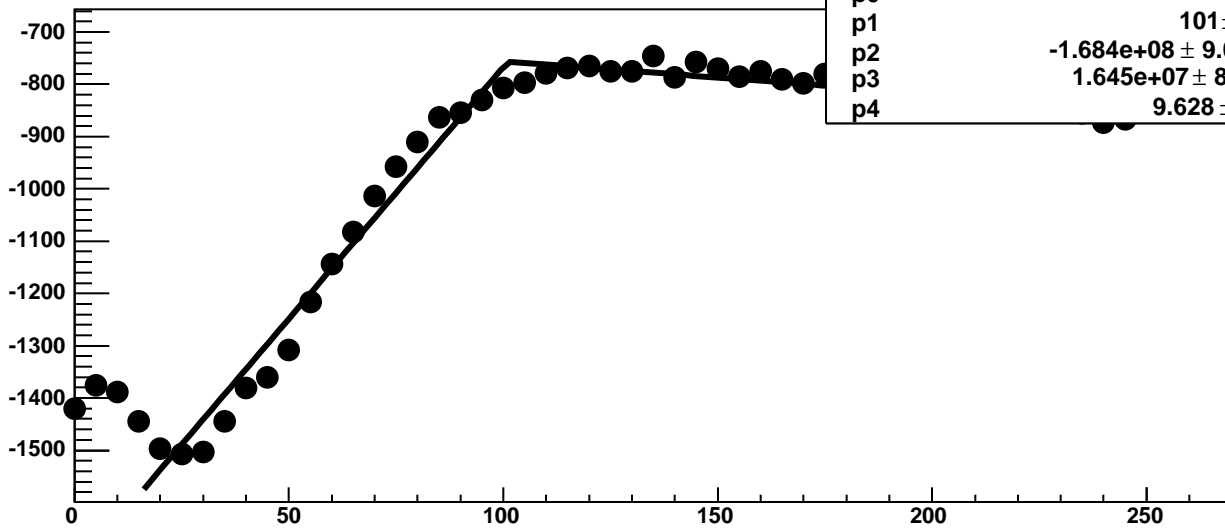
Chip 6, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

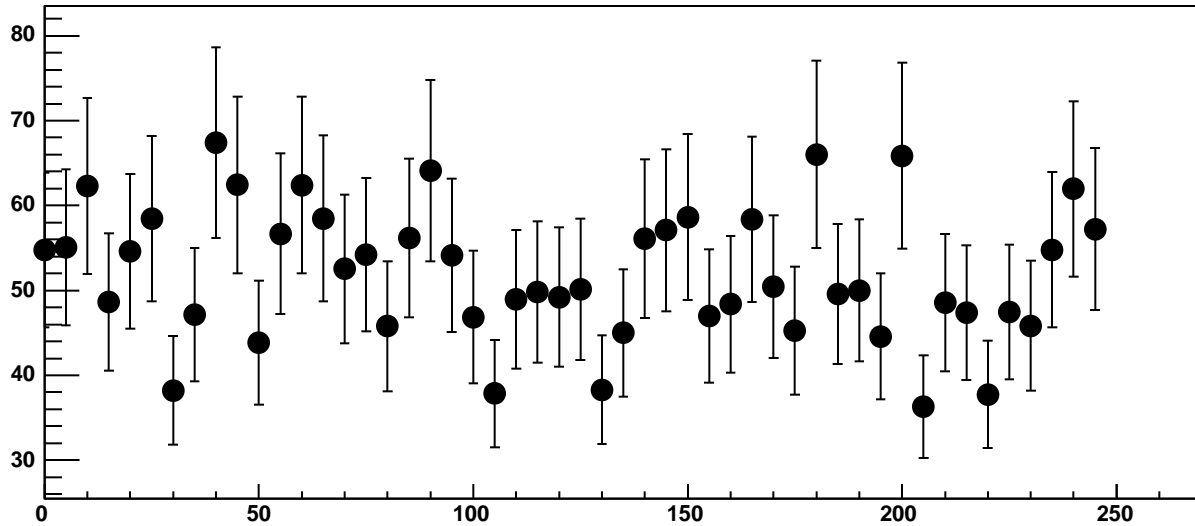


Chip 6, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

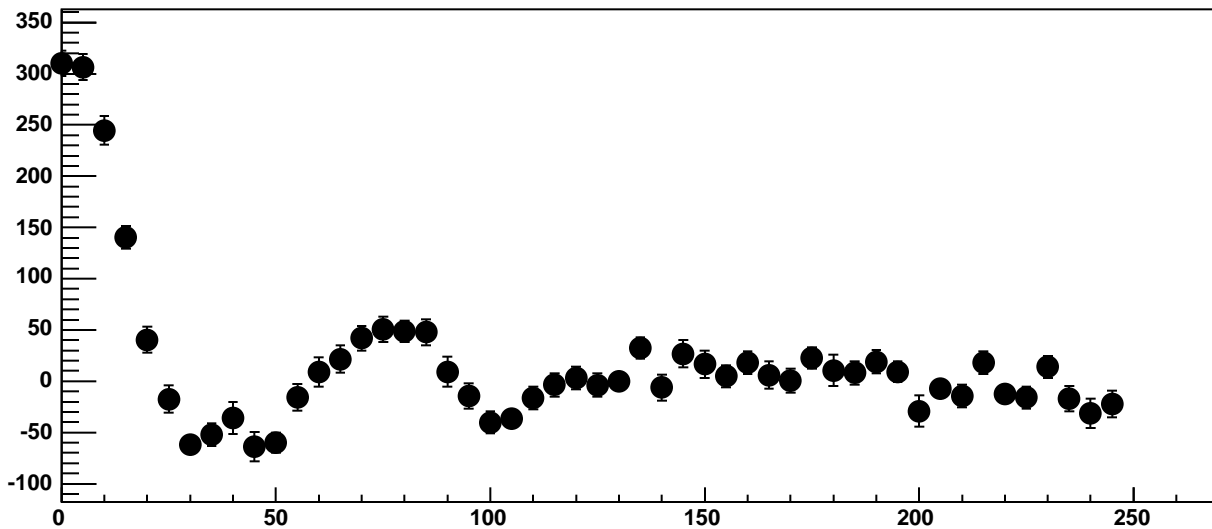


$\chi^2 / \text{ndf}$	458.3 / 41
p0	-757.1 ± 3.889
p1	101 ± 0.6752
p2	-1.684e+08 ± 9.088e+06
p3	1.645e+07 ± 8.64e+05
p4	9.628 ± 0.1066

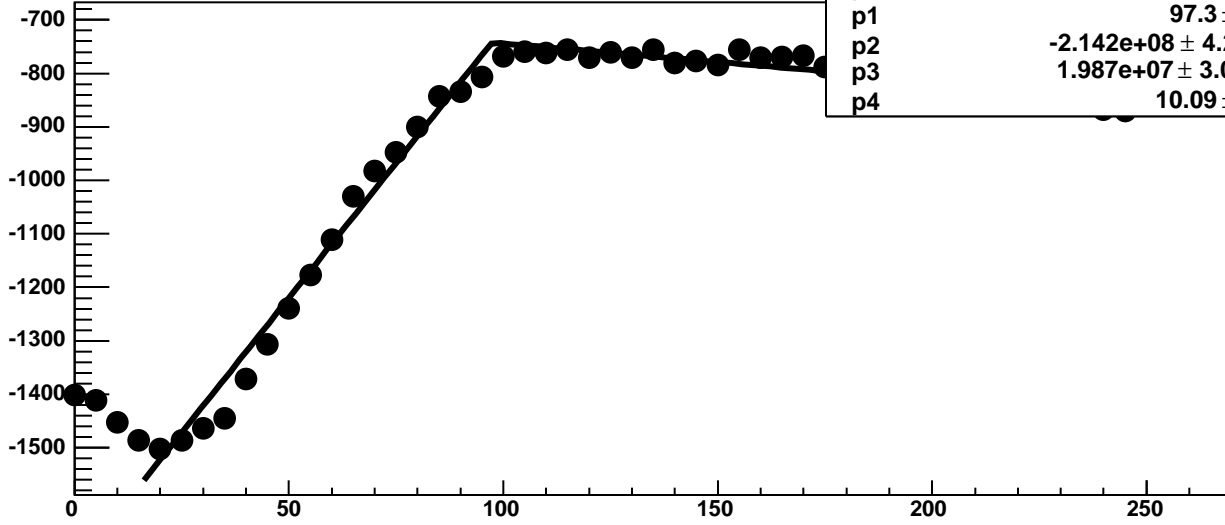
Chip 6, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

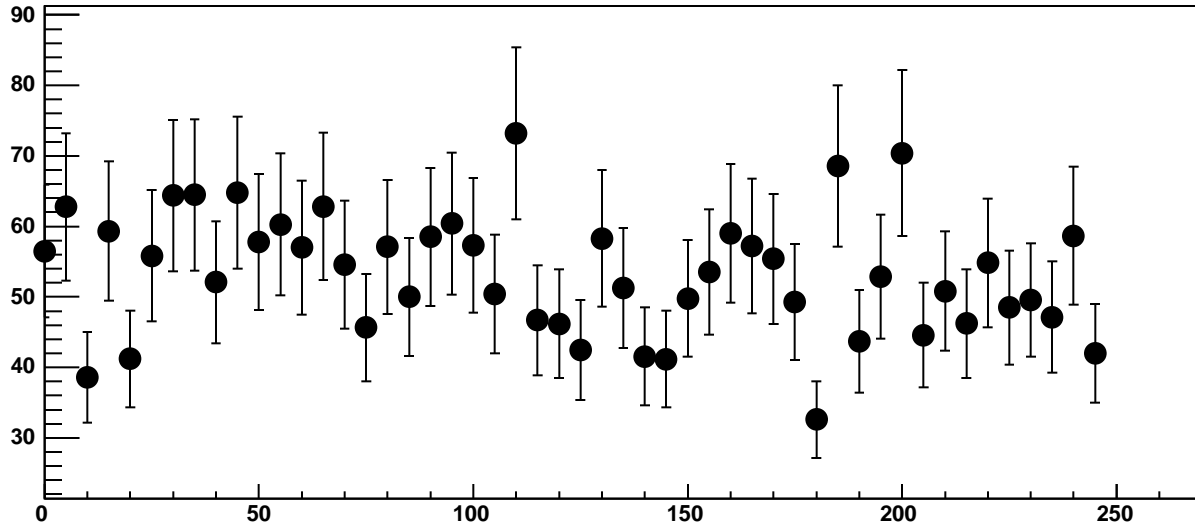


Chip 6, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold

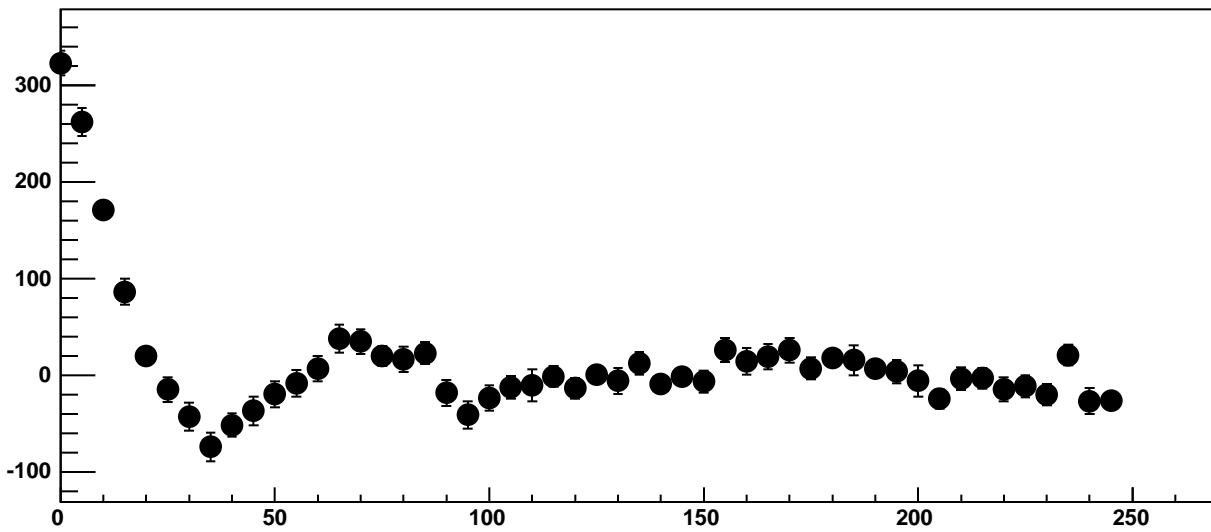


$\chi^2 / \text{ndf}$	189.5 / 41
p0	-742.3 ± 4.082
p1	97.3 ± 0.6947
p2	-2.142e+08 ± 4.263e+06
p3	1.987e+07 ± 3.062e+05
p4	10.09 ± 0.1232

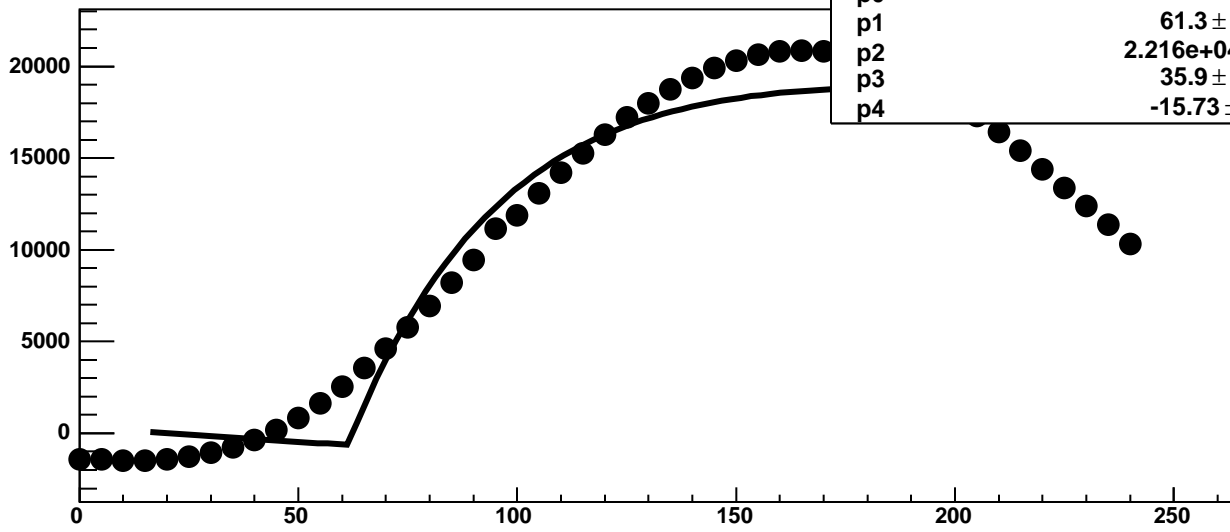
Chip 6, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

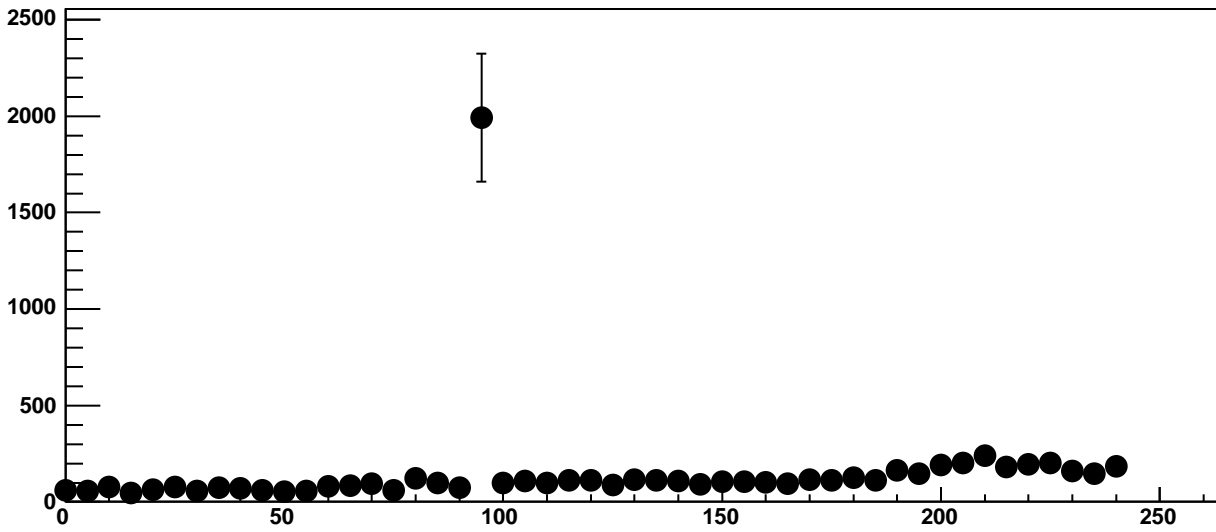


Chip 6, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

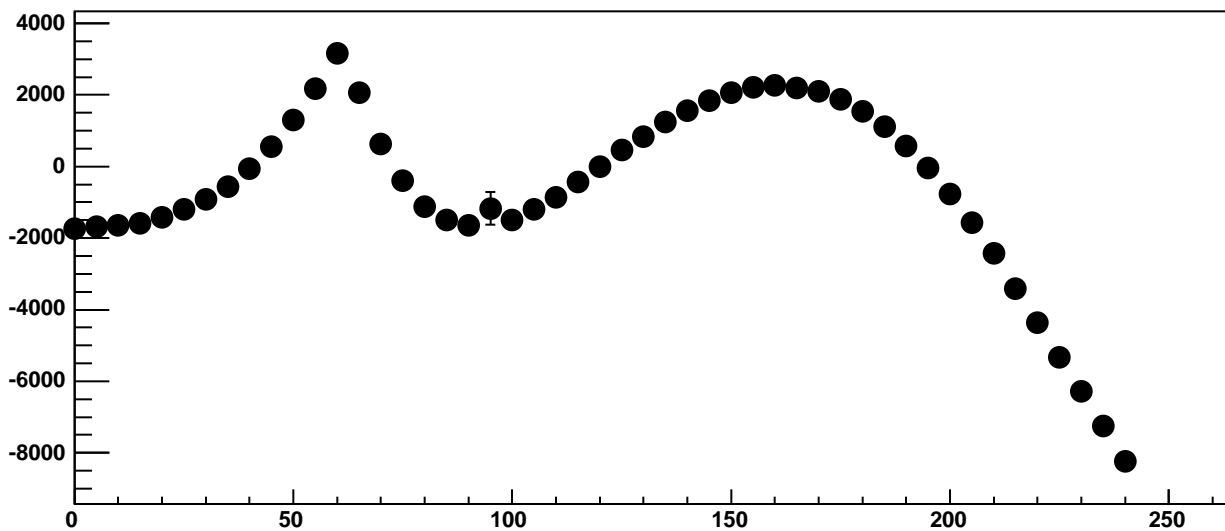


$\chi^2 / \text{ndf}$	3.61e+05 / 41
p0	-637.3 ± 6.634
p1	61.3 ± 0.02758
p2	2.216e+04 ± 34.2
p3	35.9 ± 0.06999
p4	-15.73 ± 0.2004

Chip 6, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

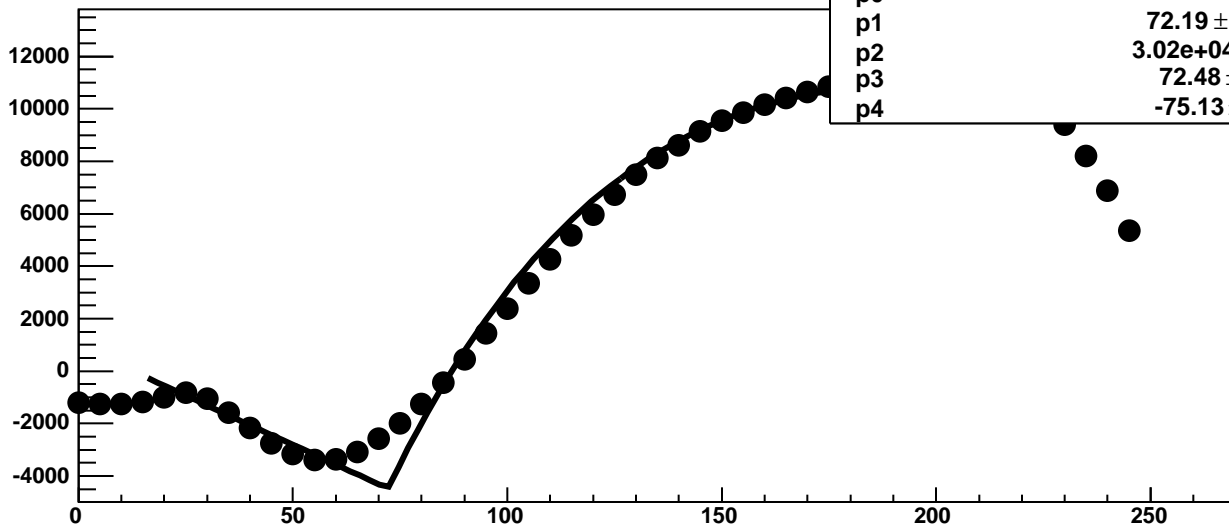


Chip 6, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold



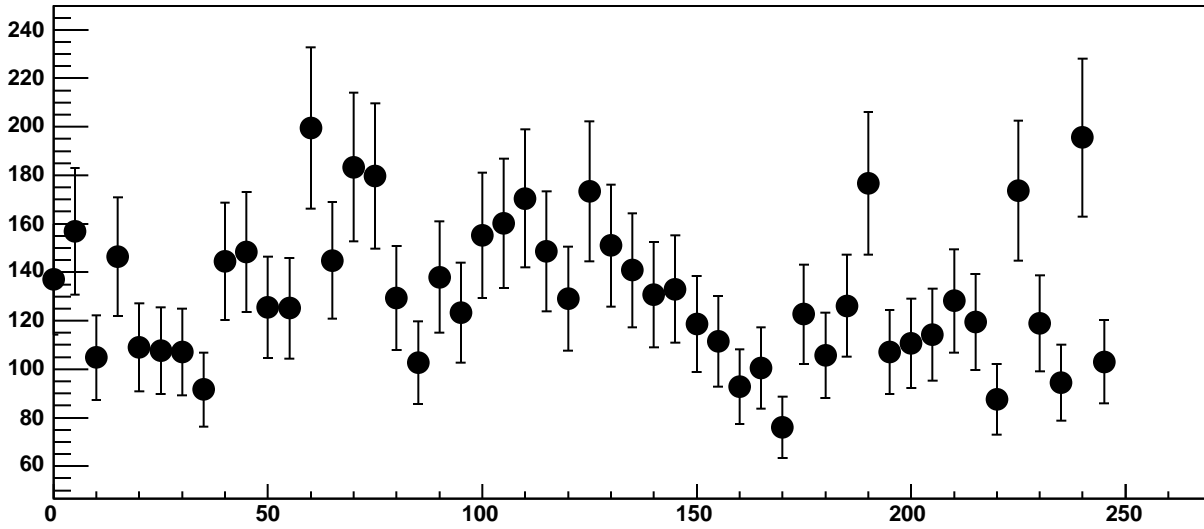


Chip 6, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

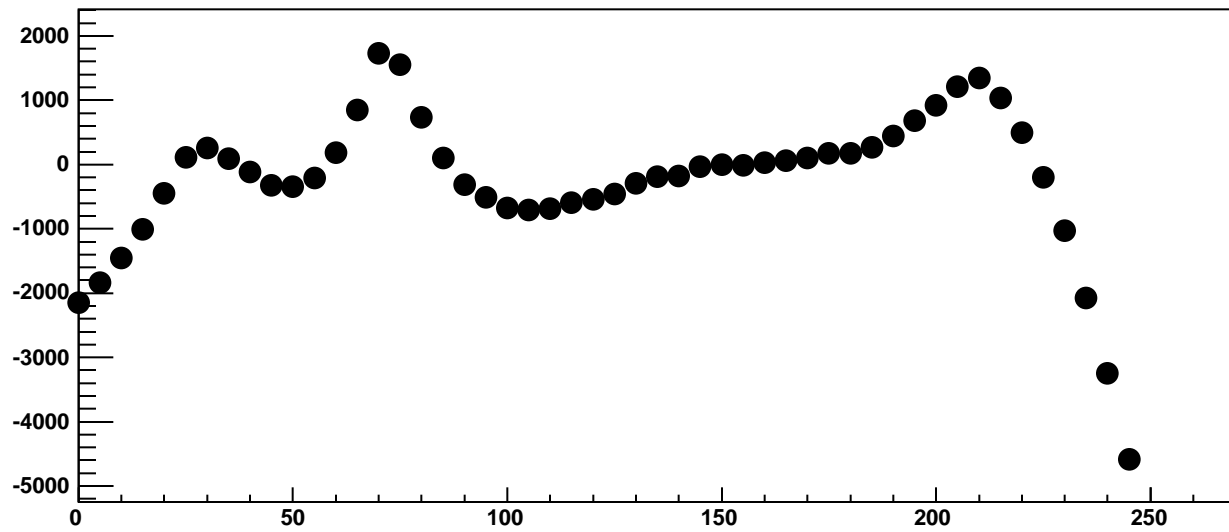


$\chi^2 / \text{ndf}$	3.308e+04 / 41
p0	-4479 ± 14.84
p1	72.19 ± 0.06791
p2	3.02e+04 ± 125.1
p3	72.48 ± 0.2778
p4	-75.13 ± 0.4711

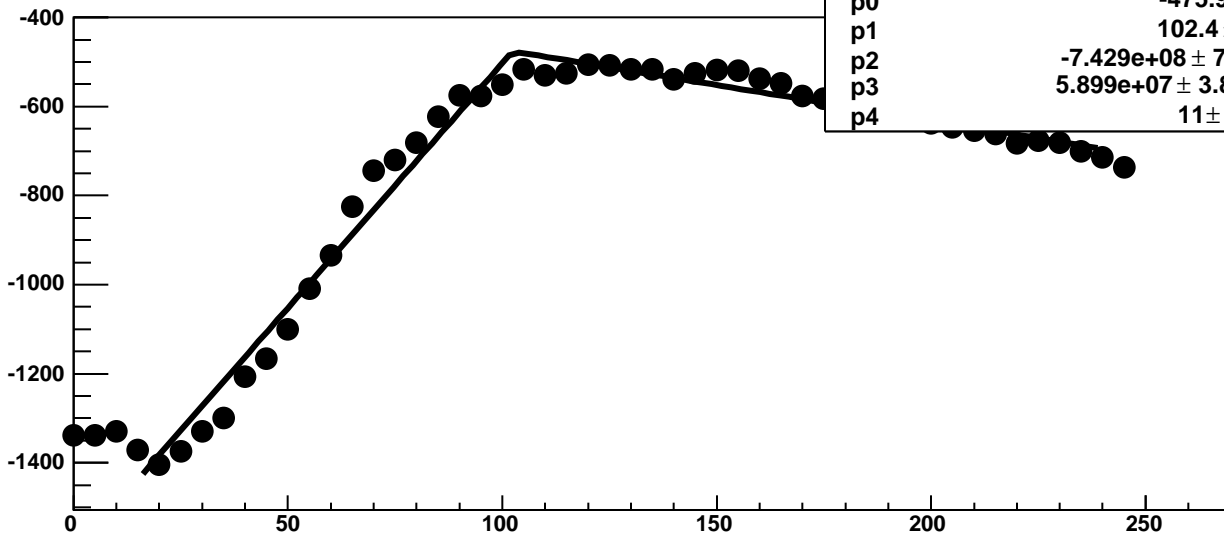
Chip 6, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

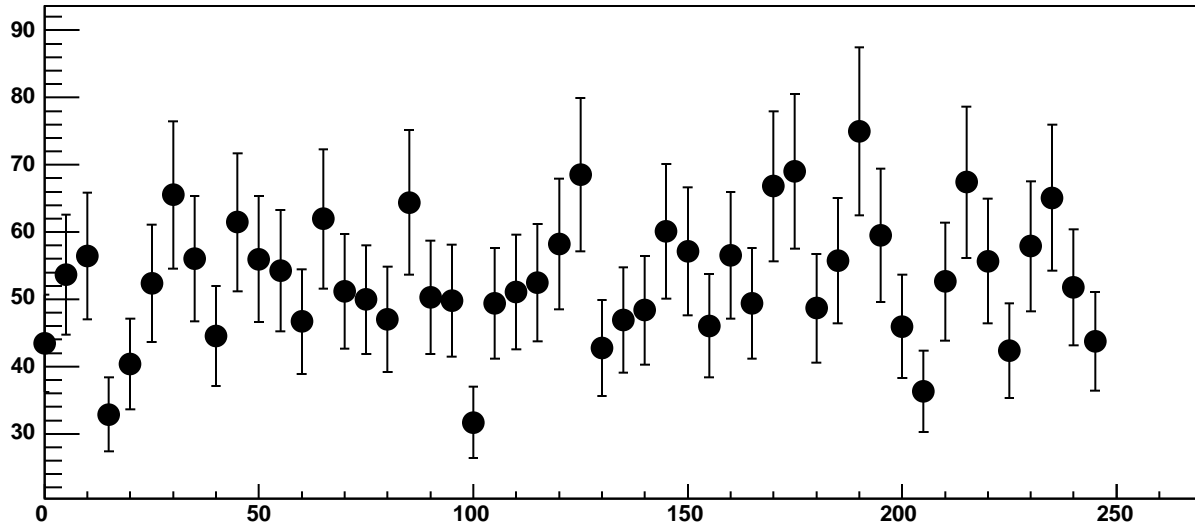


Chip 6, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

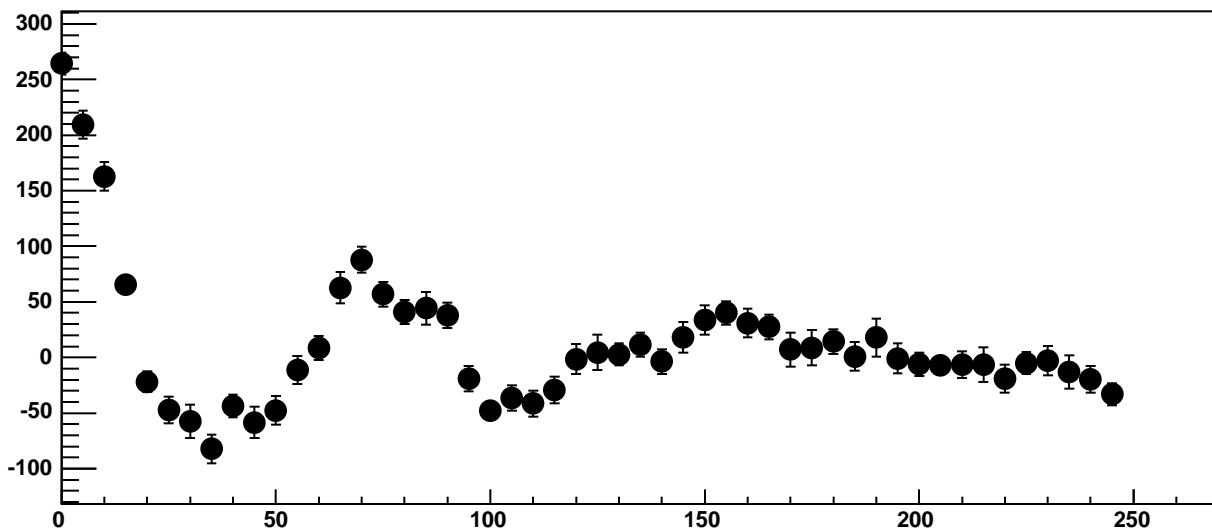


$\chi^2 / \text{ndf}$	459.8 / 41
p0	$-475.9 \pm 4.006$
p1	$102.4 \pm 0.5201$
p2	$-7.429\text{e}+08 \pm 7.82\text{e}+06$
p3	$5.899\text{e}+07 \pm 3.814\text{e}+05$
p4	$11 \pm 0.08753$

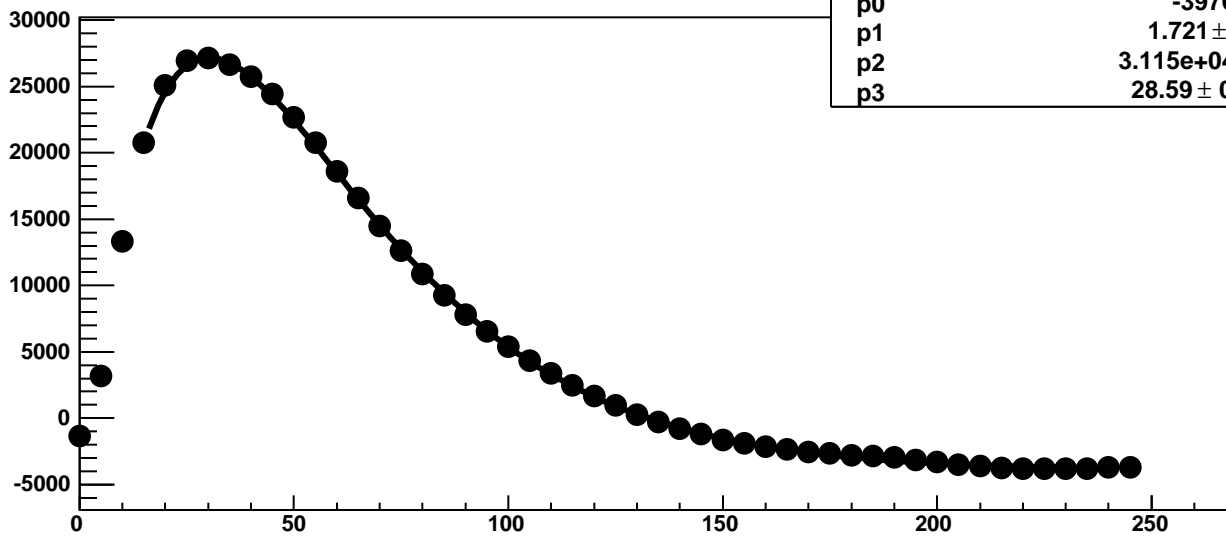
Chip 6, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold



Chip 6, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

5773 / 42

p0

$-3976 \pm 3.631$

p1

$1.721 \pm 0.01346$

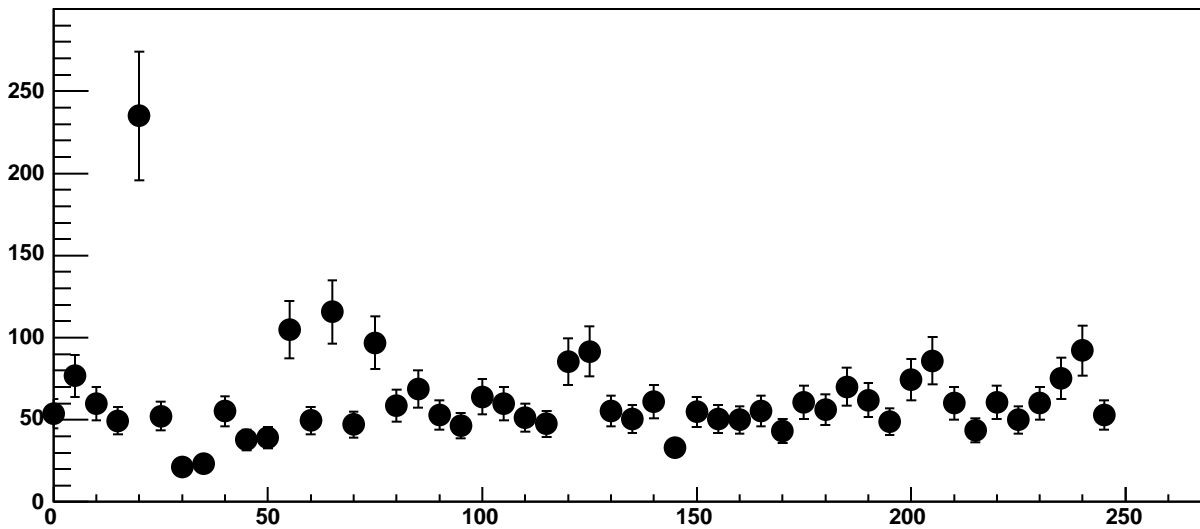
p2

$3.115 \times 10^4 \pm 4.338$

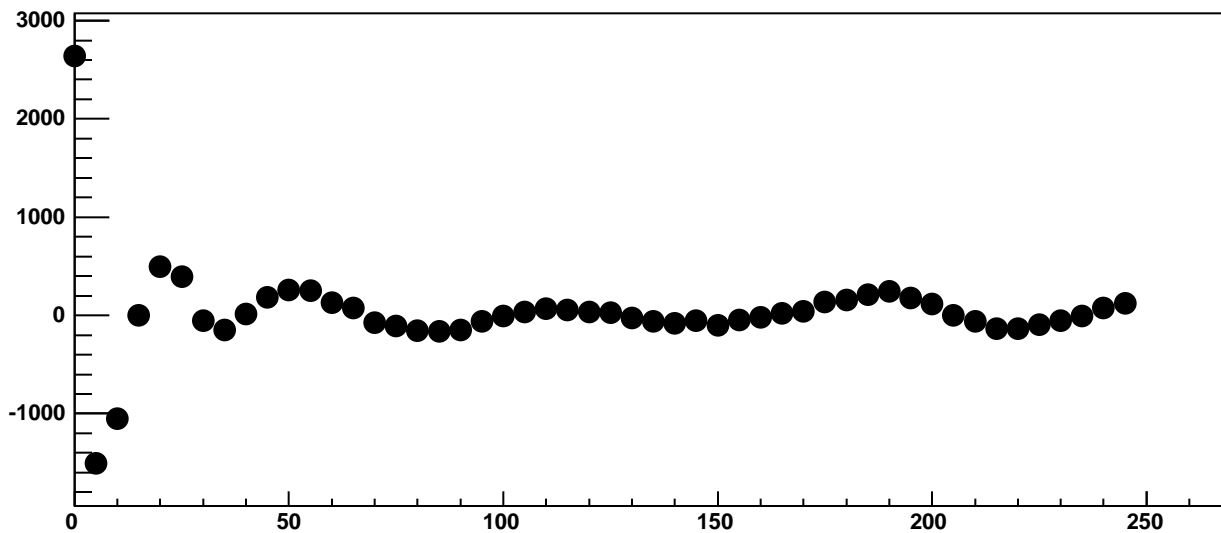
p3

$28.59 \pm 0.009095$

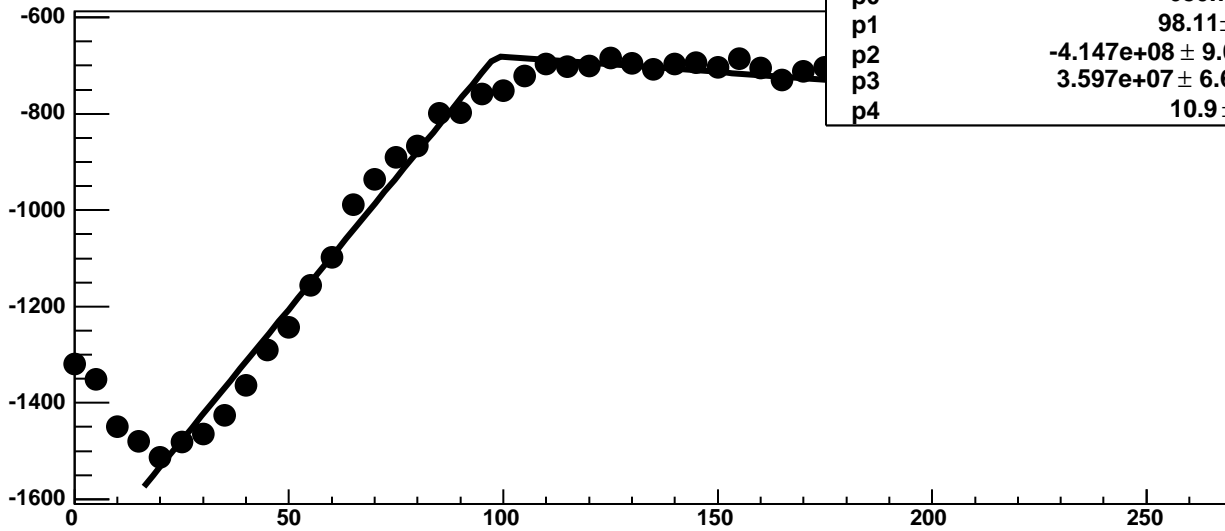
Chip 6, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

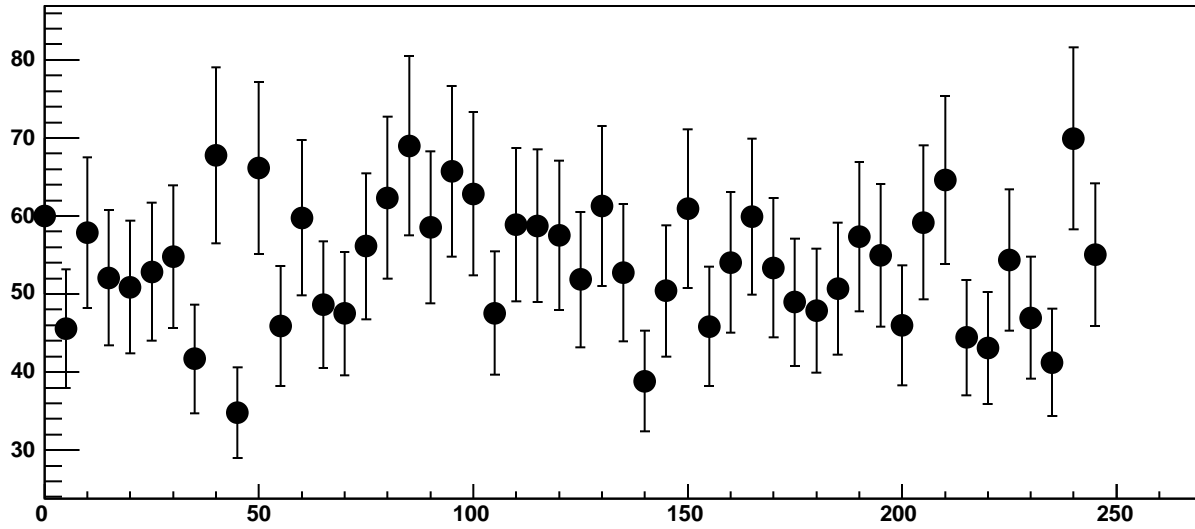


Chip 6, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

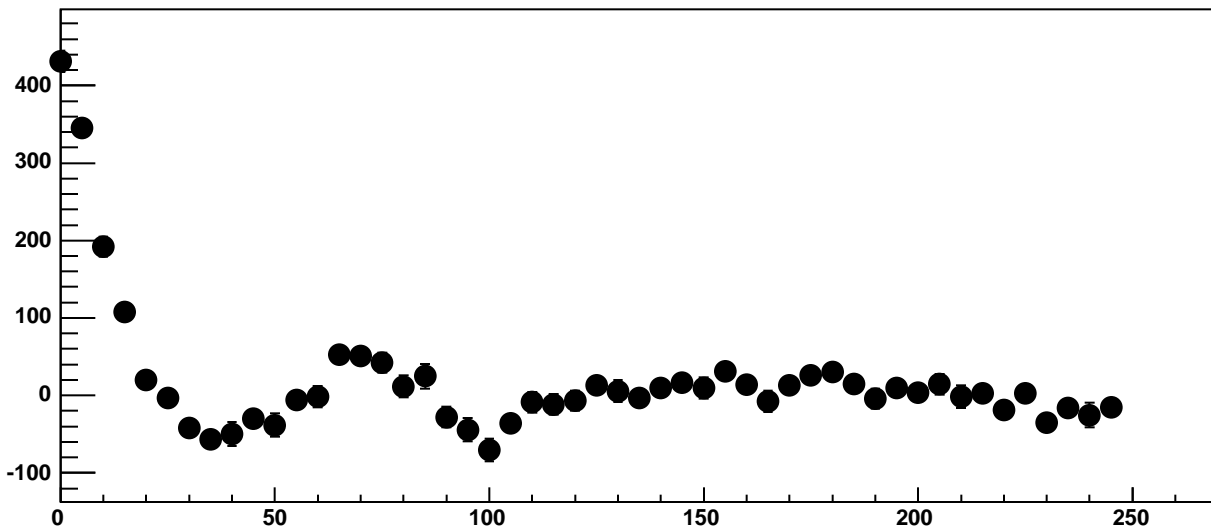


$\chi^2 / \text{ndf}$	321.3 / 41
p0	$-680.7 \pm 4.297$
p1	$98.11 \pm 0.6926$
p2	$-4.147\text{e}+08 \pm 9.086\text{e}+06$
p3	$3.597\text{e}+07 \pm 6.618\text{e}+05$
p4	$10.9 \pm 0.1272$

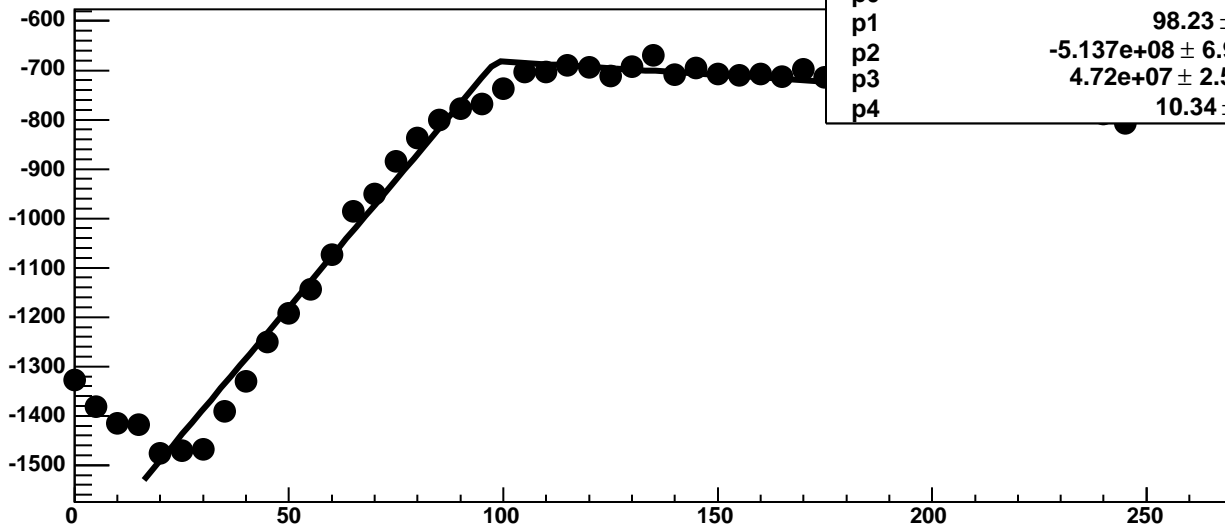
Chip 6, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

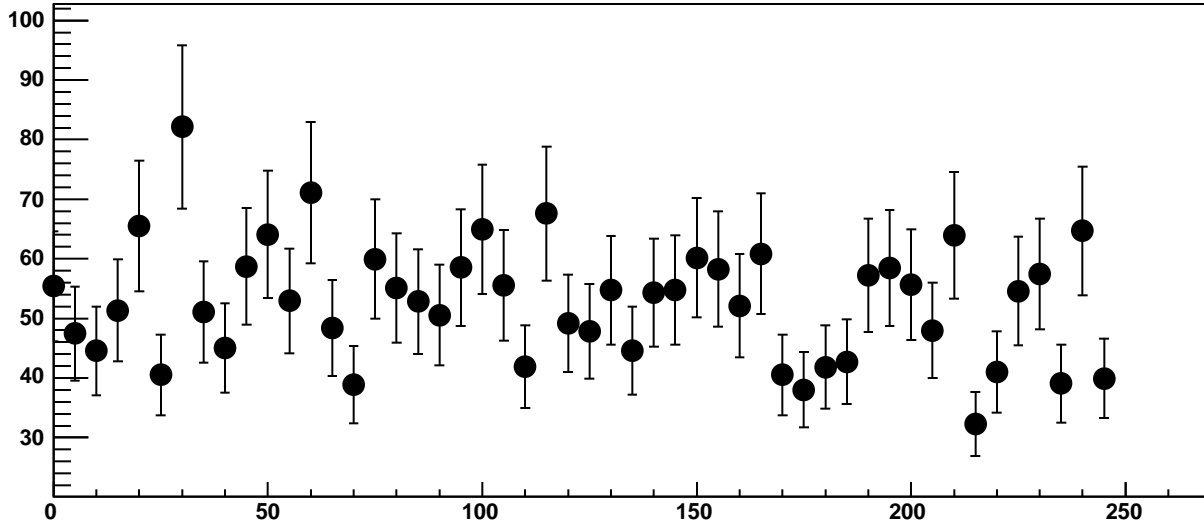


Chip 6, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

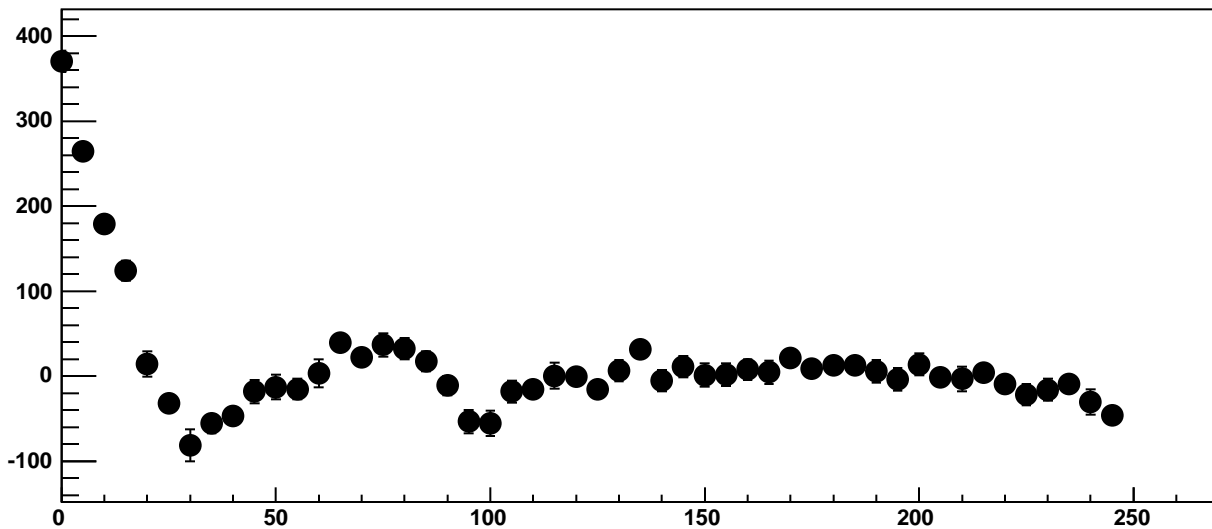


$\chi^2 / \text{ndf}$	295.5 / 41
p0	-681.1 ± 4.212
p1	98.23 ± 0.6834
p2	-5.137e+08 ± 6.992e+06
p3	4.72e+07 ± 2.591e+05
p4	10.34 ± 0.1208

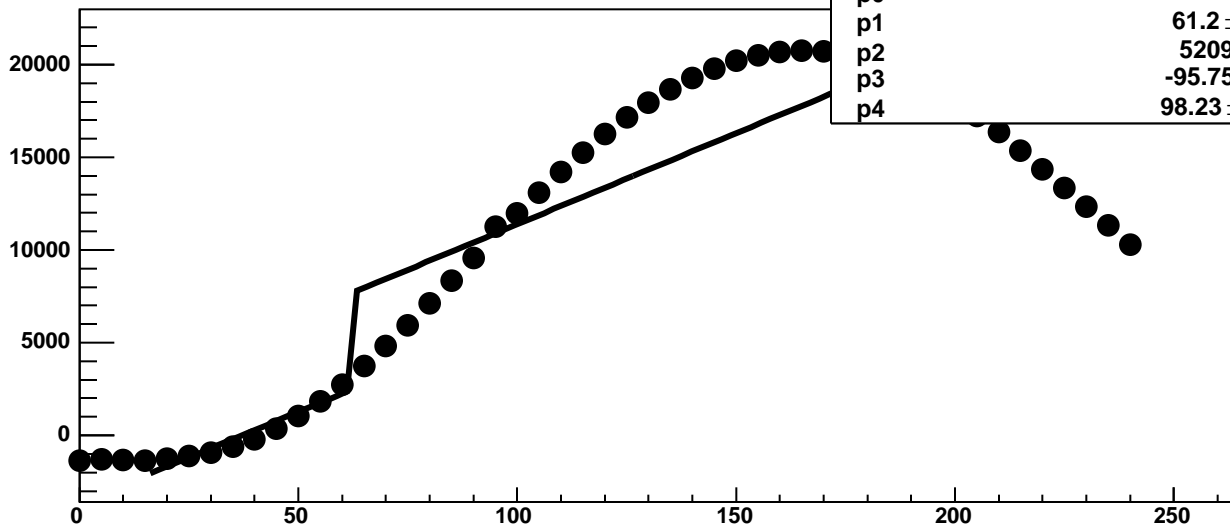
Chip 6, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

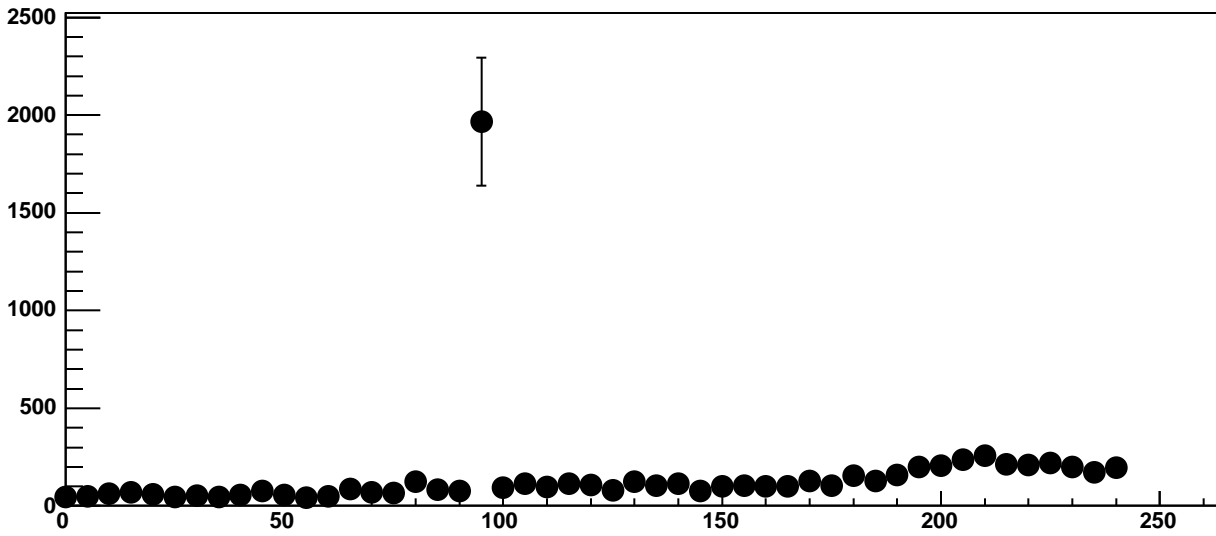


Chip 6, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

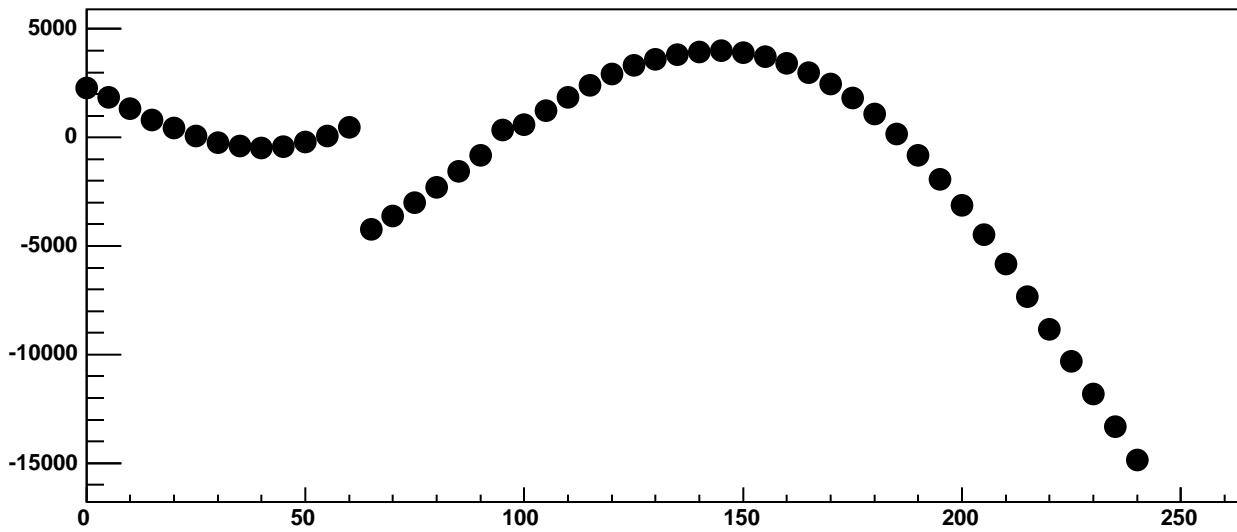


$\chi^2 / \text{ndf}$	8.545e+05 / 41
p0	2370 ± 11.37
p1	61.2 ± 0.1706
p2	5209 ± 28.45
p3	-95.75 ± 6.902
p4	98.23 ± 0.4047

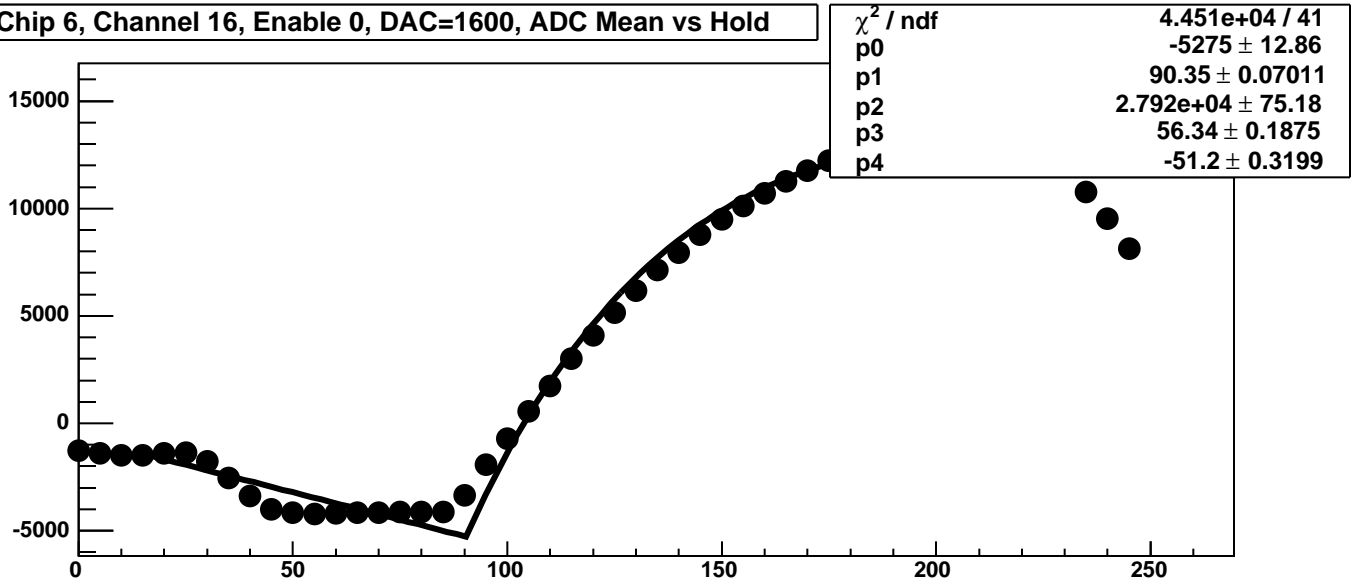
Chip 6, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



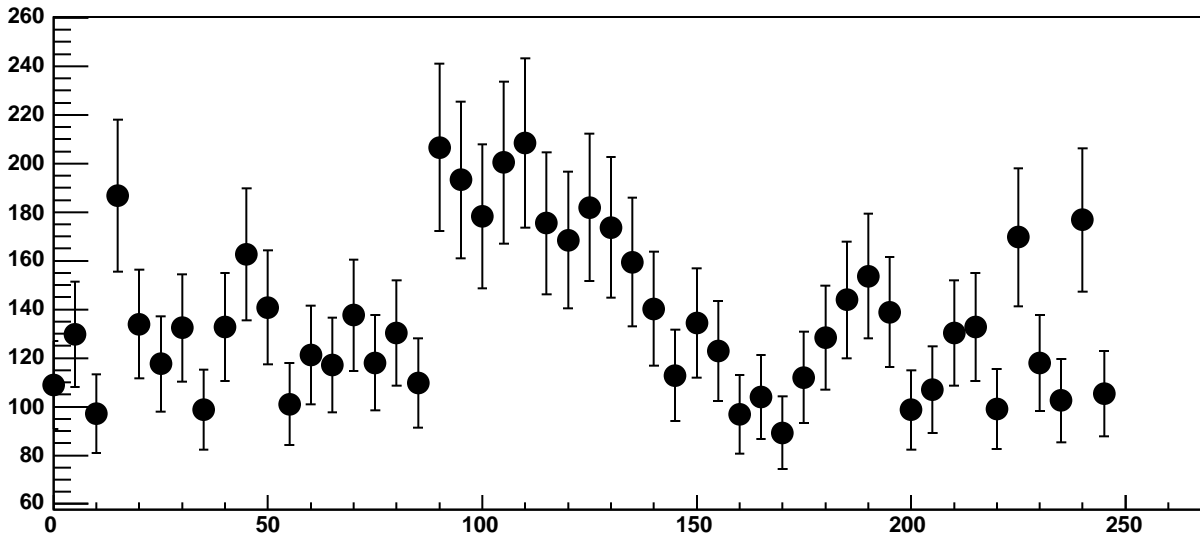
Chip 6, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold



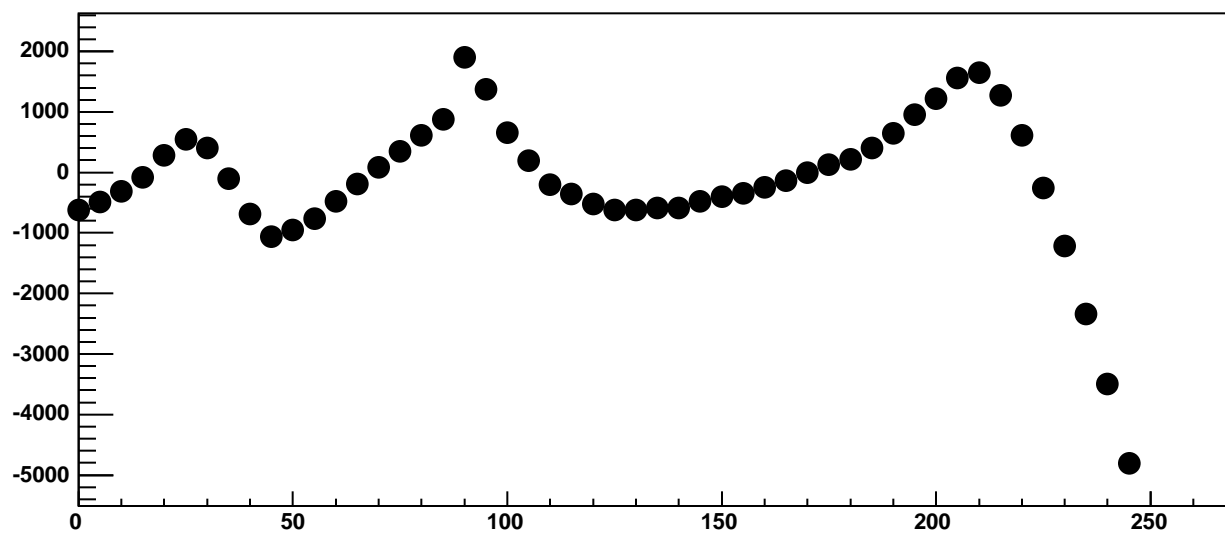
Chip 6, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold



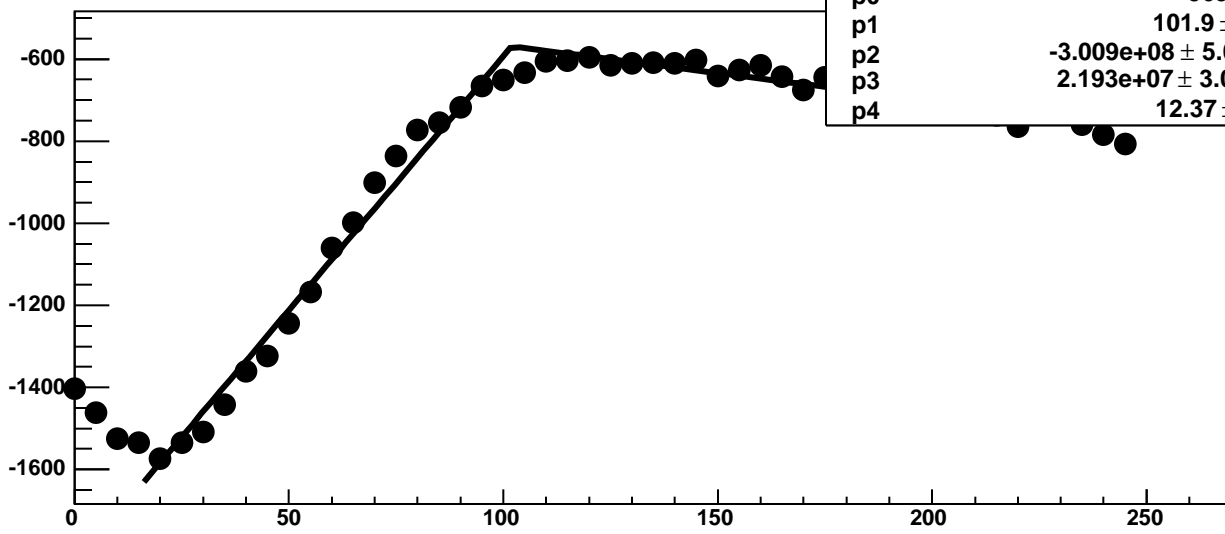
Chip 6, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

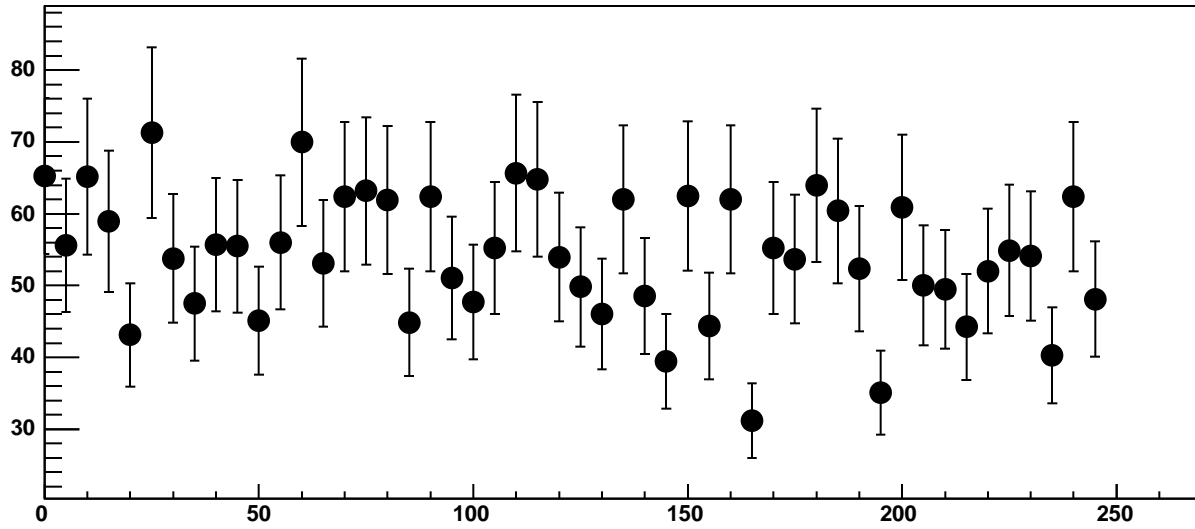


Chip 6, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

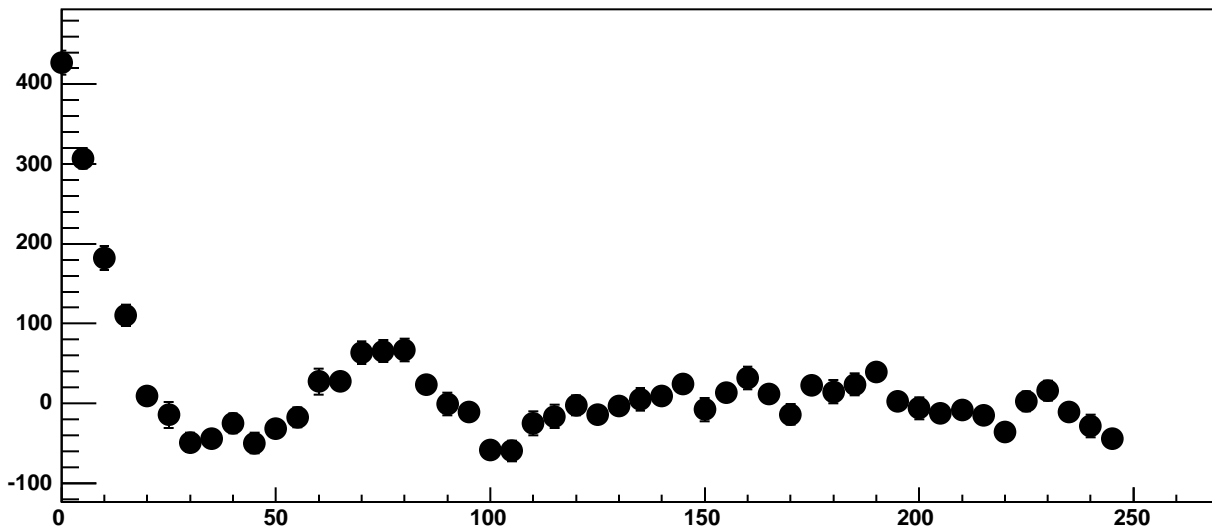


$\chi^2 / \text{ndf}$	322 / 41
p0	-569 ± 4.207
p1	101.9 ± 0.5334
p2	-3.009e+08 ± 5.066e+06
p3	2.193e+07 ± 3.031e+05
p4	12.37 ± 0.1093

Chip 6, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

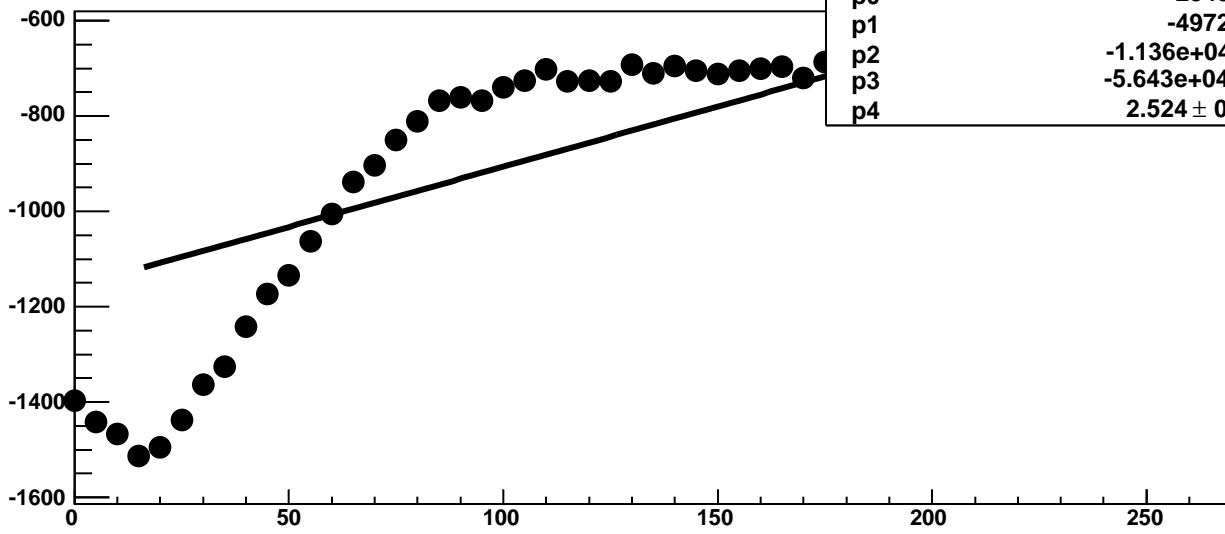


Chip 6, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold

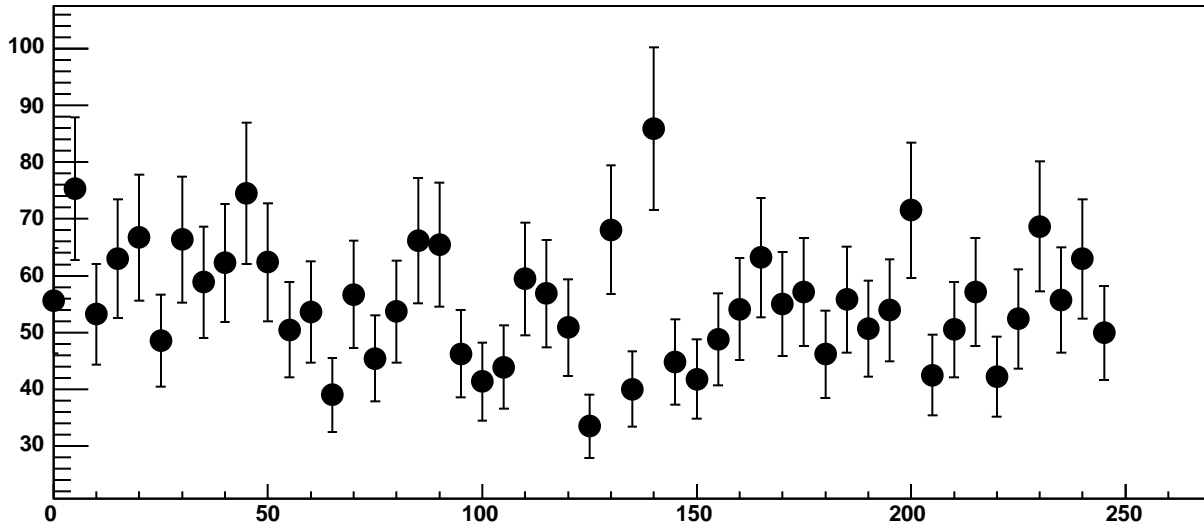




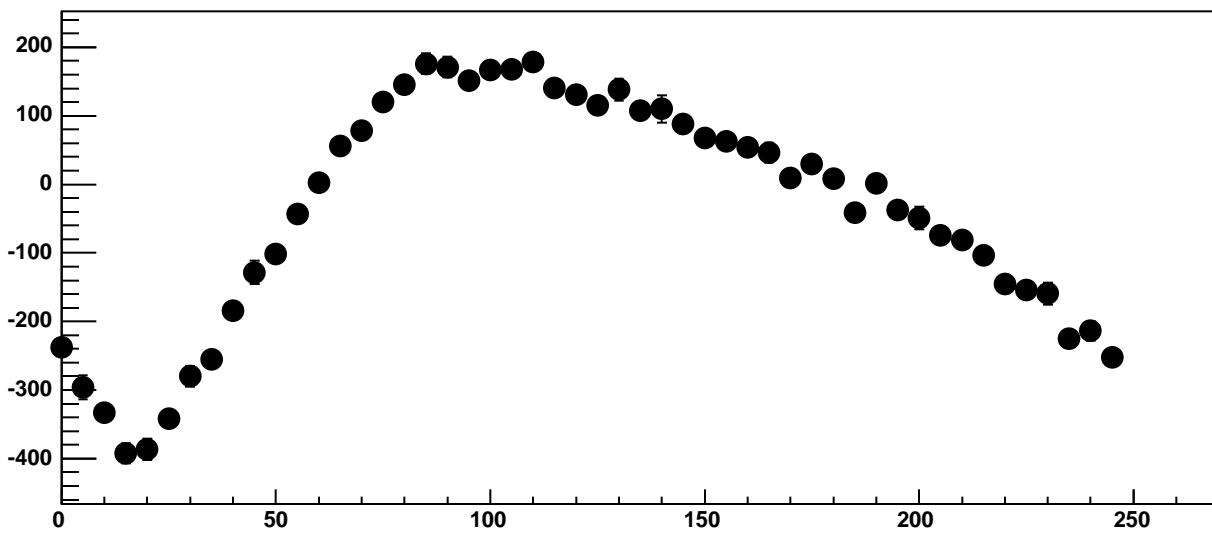
Chip 6, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold



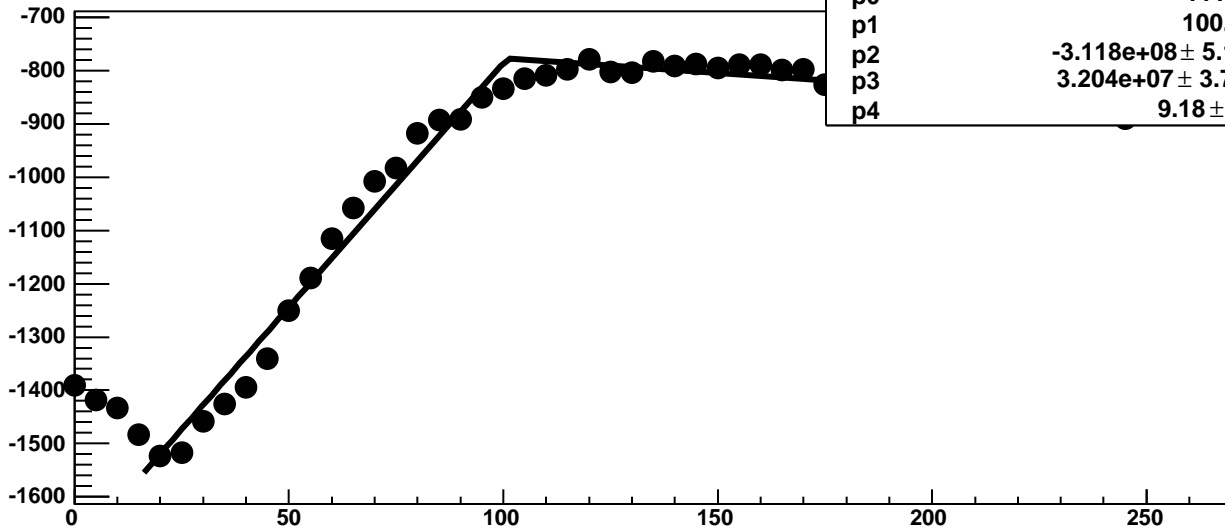
Chip 6, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

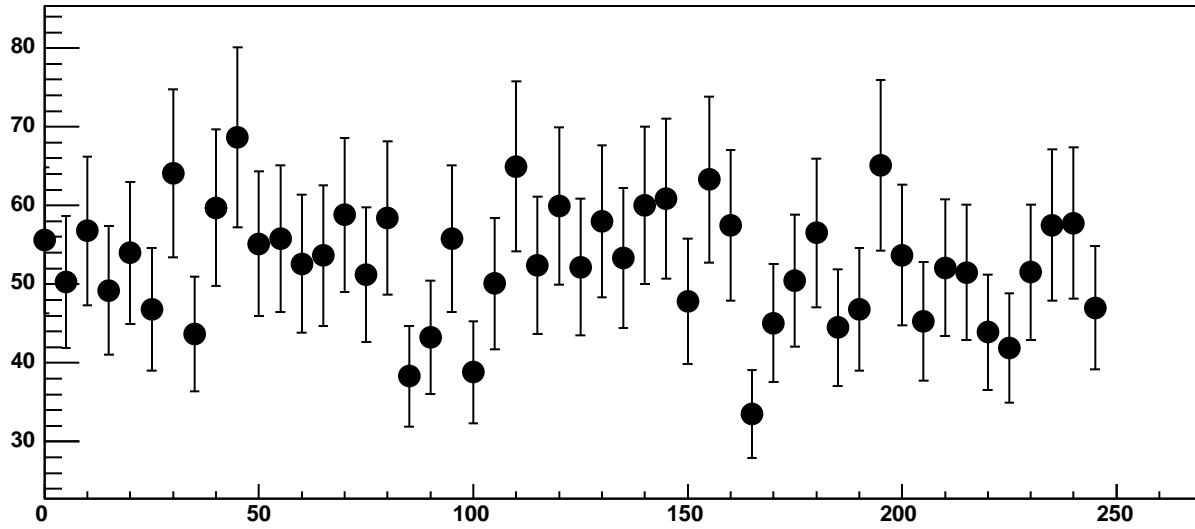


Chip 6, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

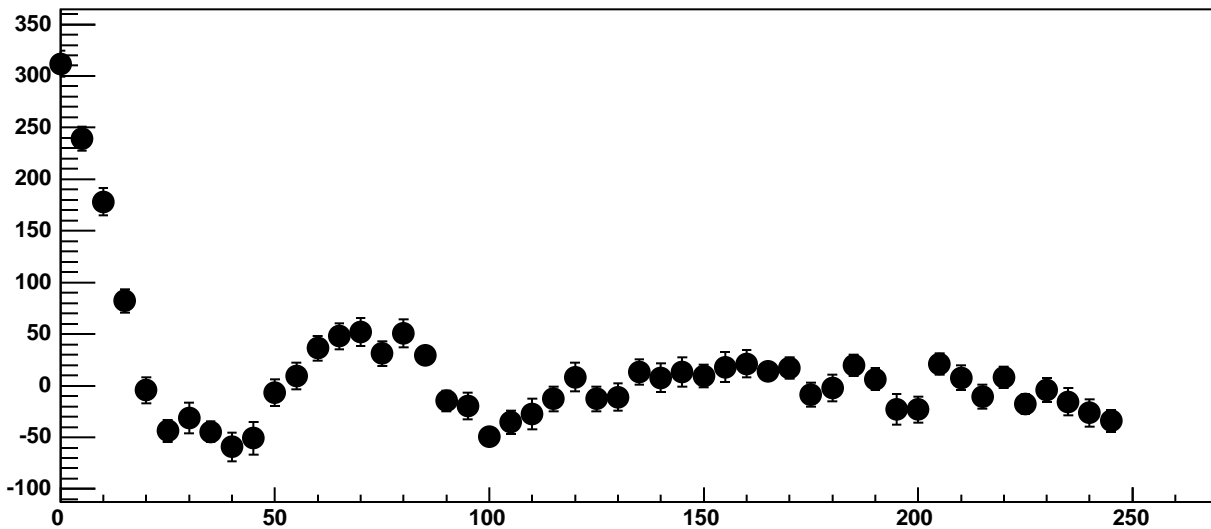


$\chi^2 / \text{ndf}$	285.2 / 41
p0	$-777 \pm 4.518$
p1	$100.9 \pm 0.7$
p2	$-3.118\text{e}+08 \pm 5.143\text{e}+06$
p3	$3.204\text{e}+07 \pm 3.704\text{e}+05$
p4	$9.18 \pm 0.0971$

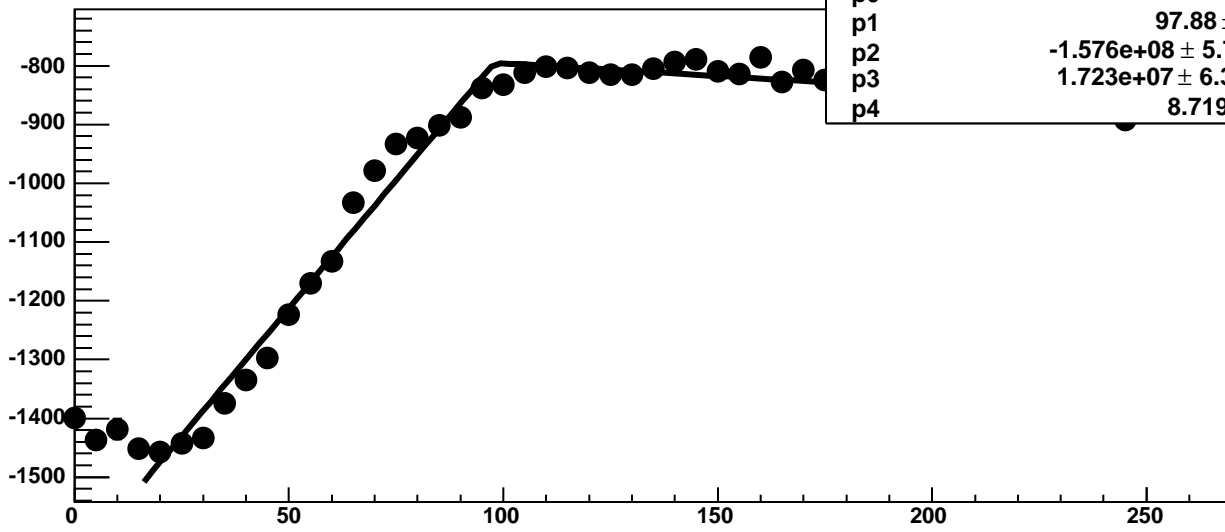
Chip 6, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

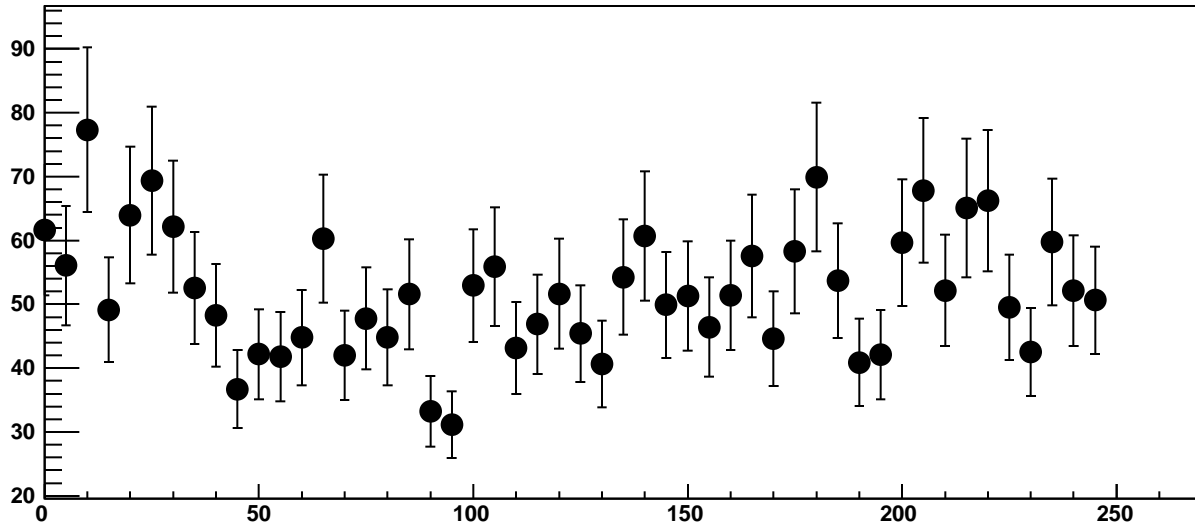


Chip 6, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

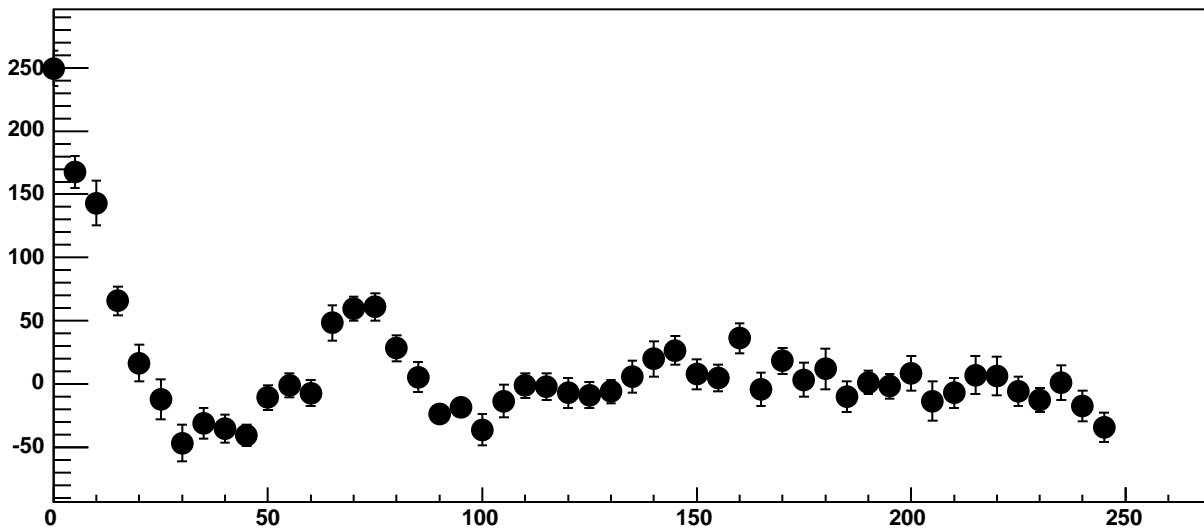


$\chi^2 / \text{ndf}$	233.9 / 41
p0	$-795.1 \pm 3.937$
p1	$97.88 \pm 0.6482$
p2	$-1.576\text{e}+08 \pm 5.712\text{e}+06$
p3	$1.723\text{e}+07 \pm 6.373\text{e}+05$
p4	$8.719 \pm 0.097$

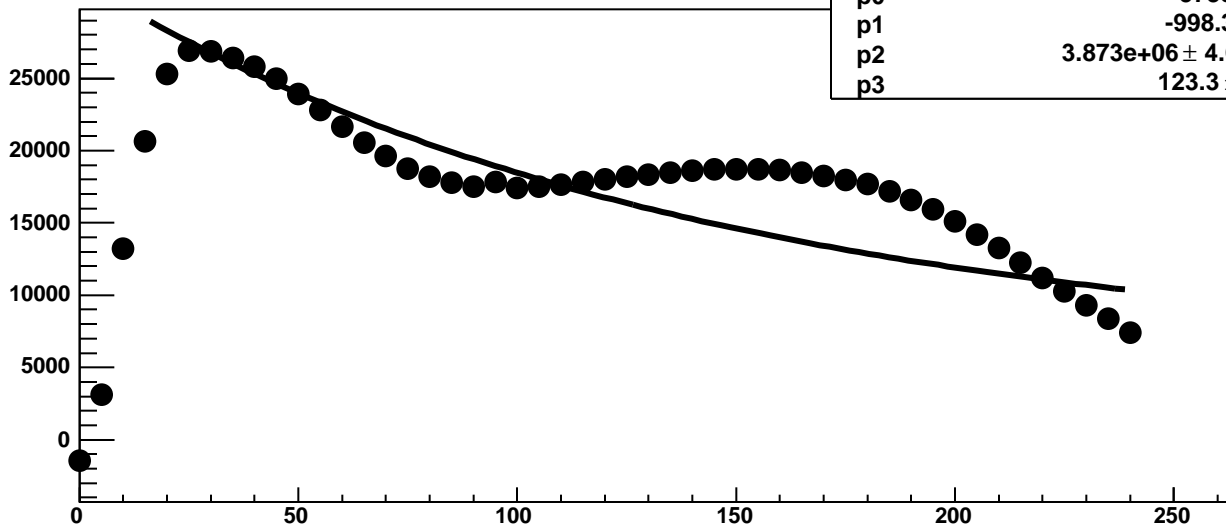
Chip 6, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

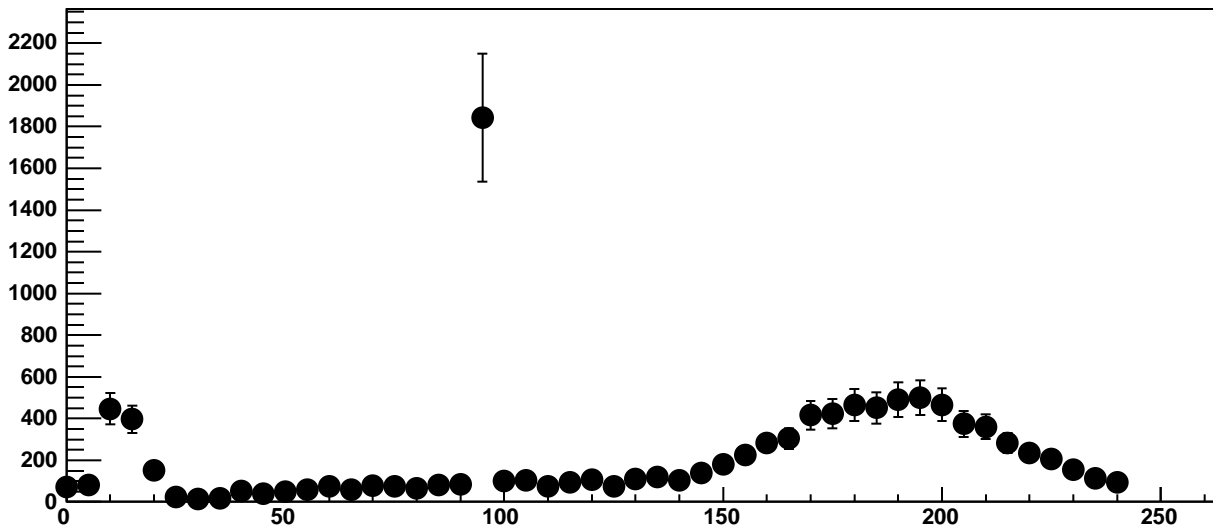


Chip 6, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

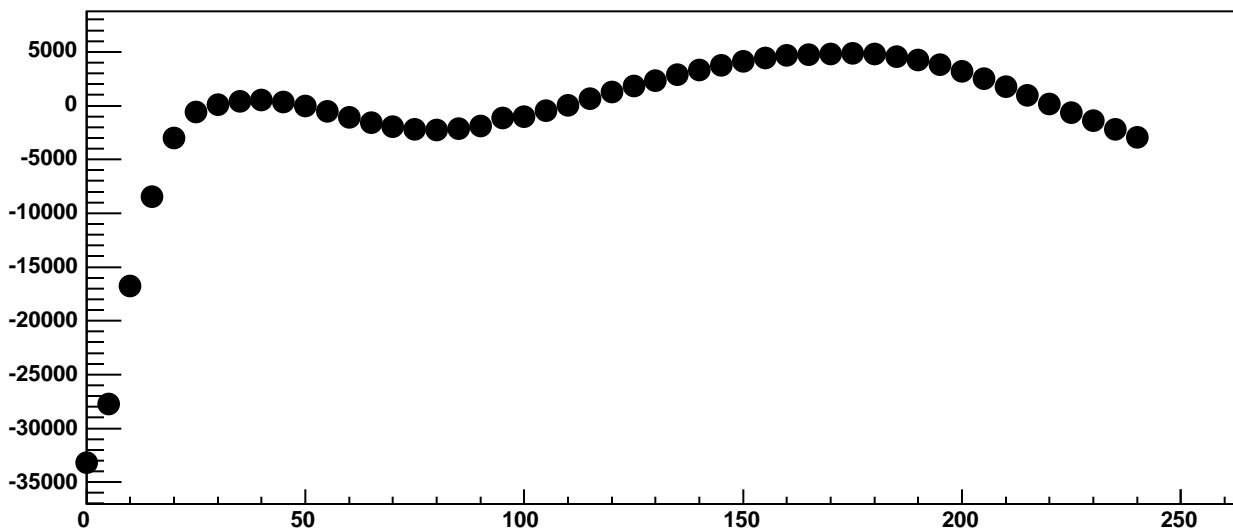


$\chi^2 / \text{ndf}$	2.706e+05 / 42
p0	5738 ± 46.32
p1	-998.3 ± 4.105
p2	3.873e+06 ± 4.678e+04
p3	123.3 ± 0.4155

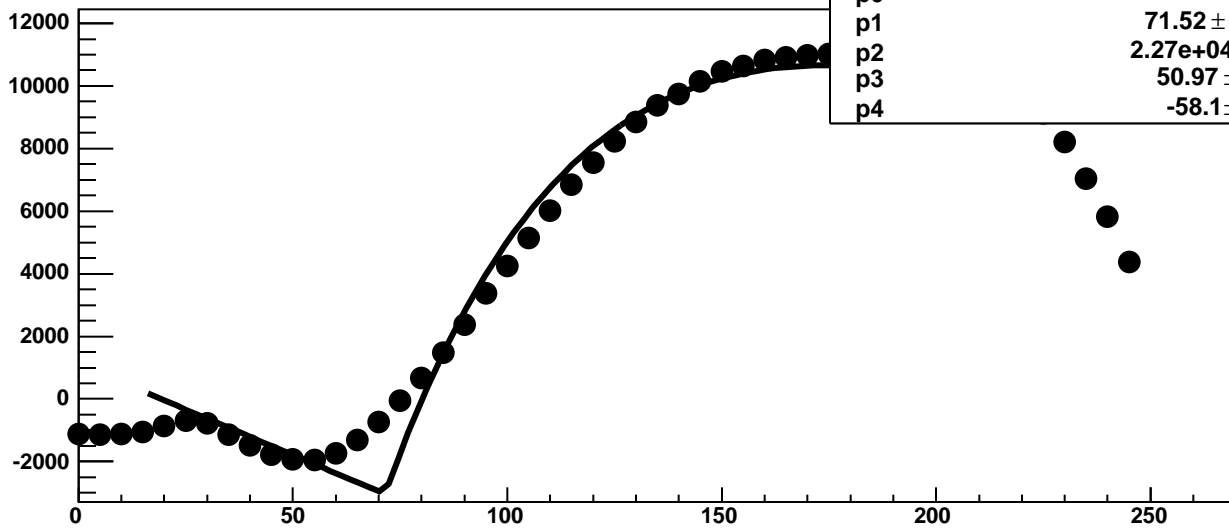
Chip 6, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

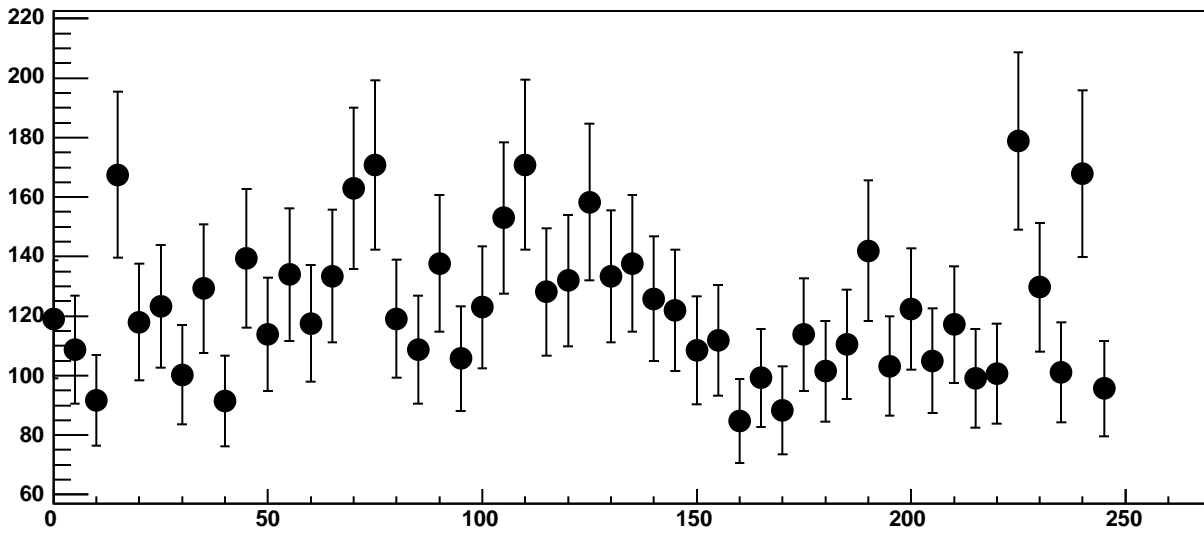


Chip 6, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

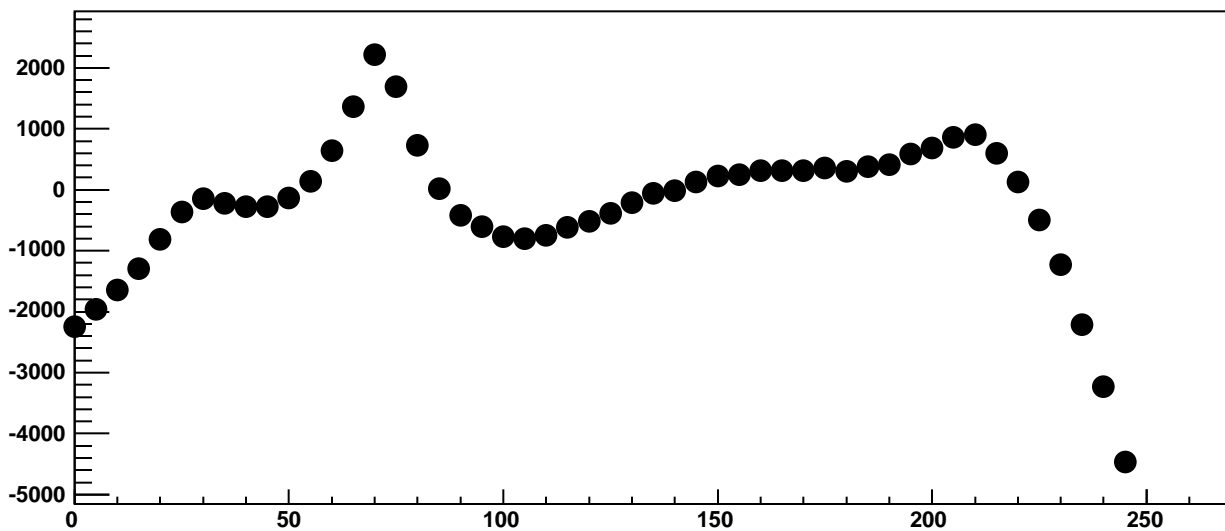


$\chi^2 / \text{ndf}$	3.852e+04 / 41
p0	-3039 ± 11.92
p1	71.52 ± 0.06116
p2	2.27e+04 ± 80.06
p3	50.97 ± 0.1945
p4	-58.1 ± 0.3726

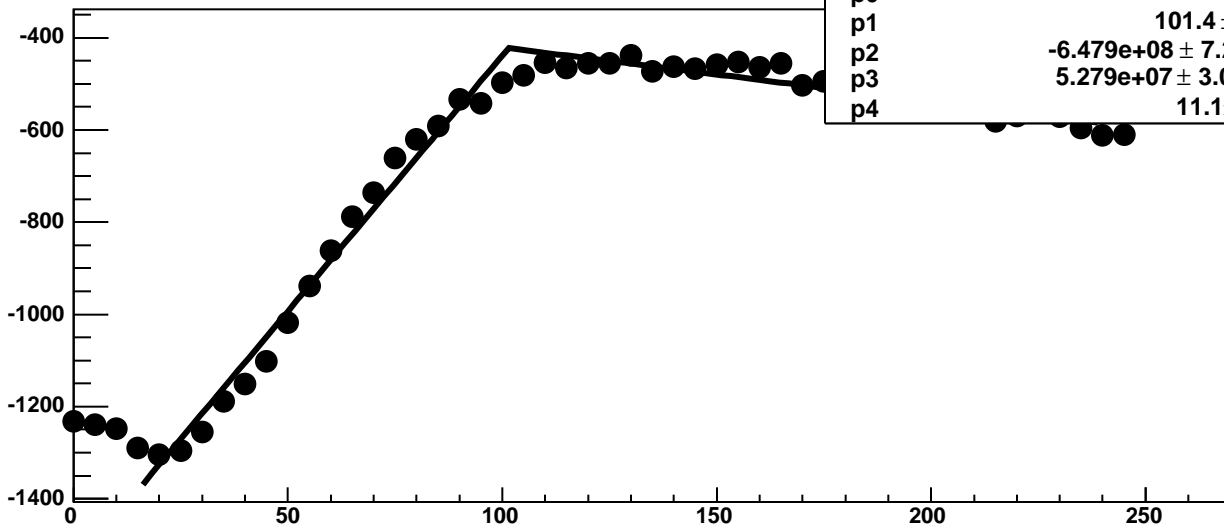
Chip 6, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

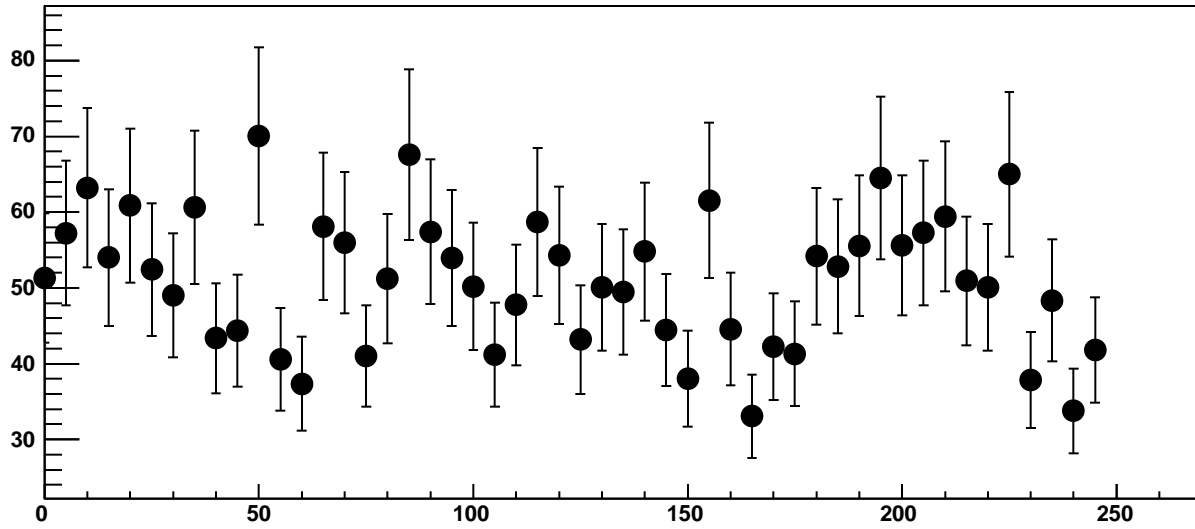


Chip 6, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

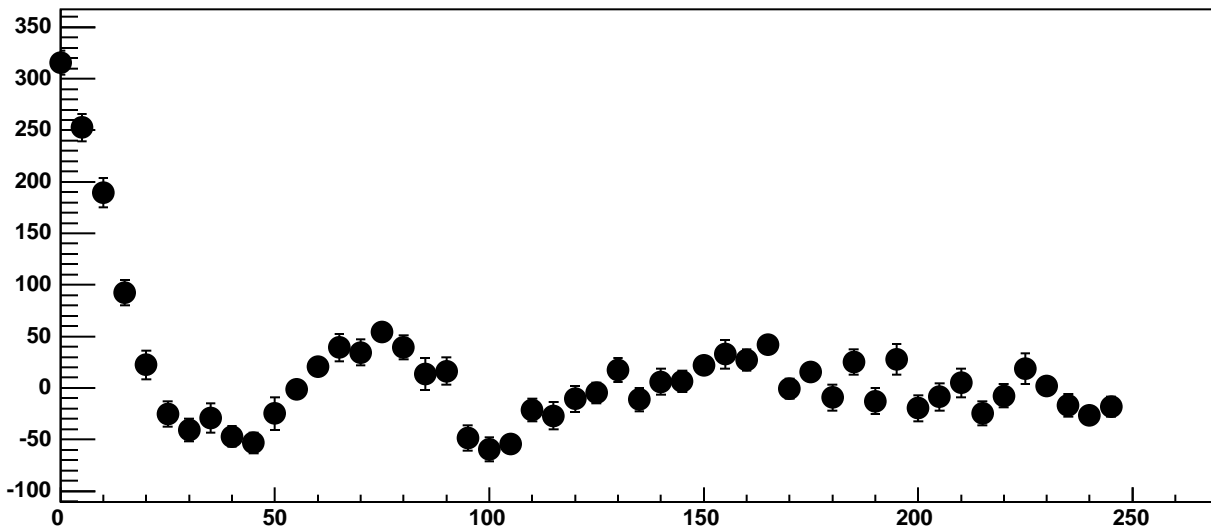


$\chi^2 / \text{ndf}$	376 / 41
p0	$-422.4 \pm 3.728$
p1	$101.4 \pm 0.5688$
p2	$-6.479\text{e}+08 \pm 7.232\text{e}+06$
p3	$5.279\text{e}+07 \pm 3.009\text{e}+05$
p4	$11.1 \pm 0.1116$

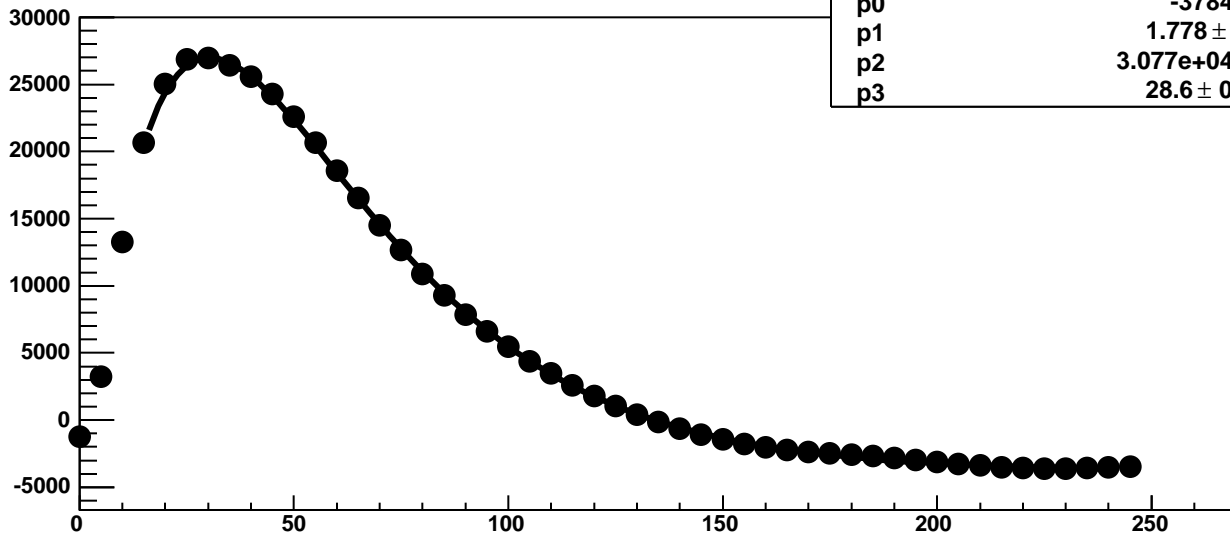
Chip 6, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

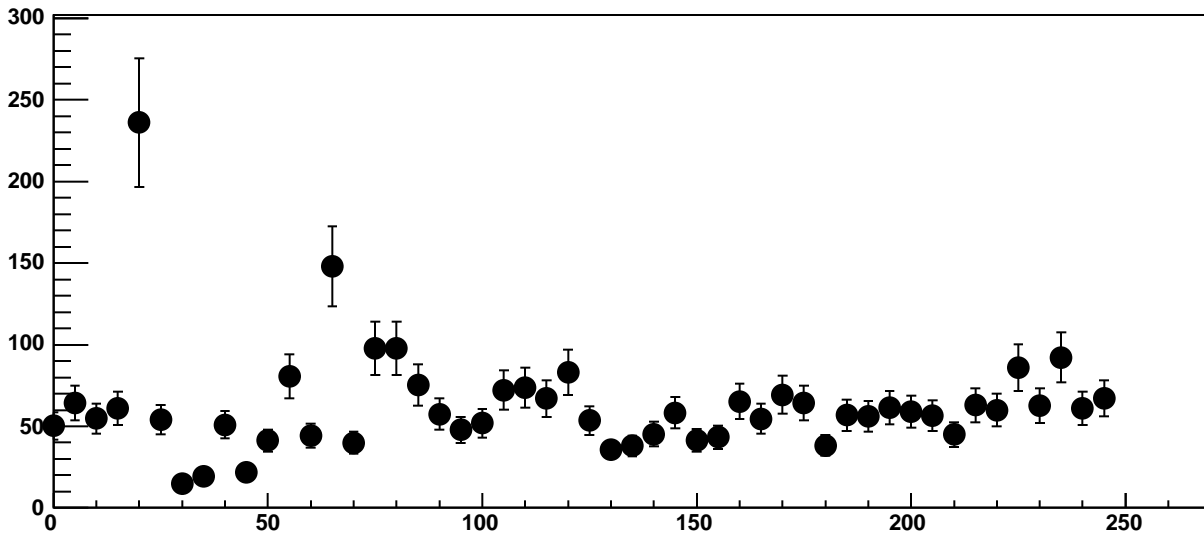


Chip 6, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

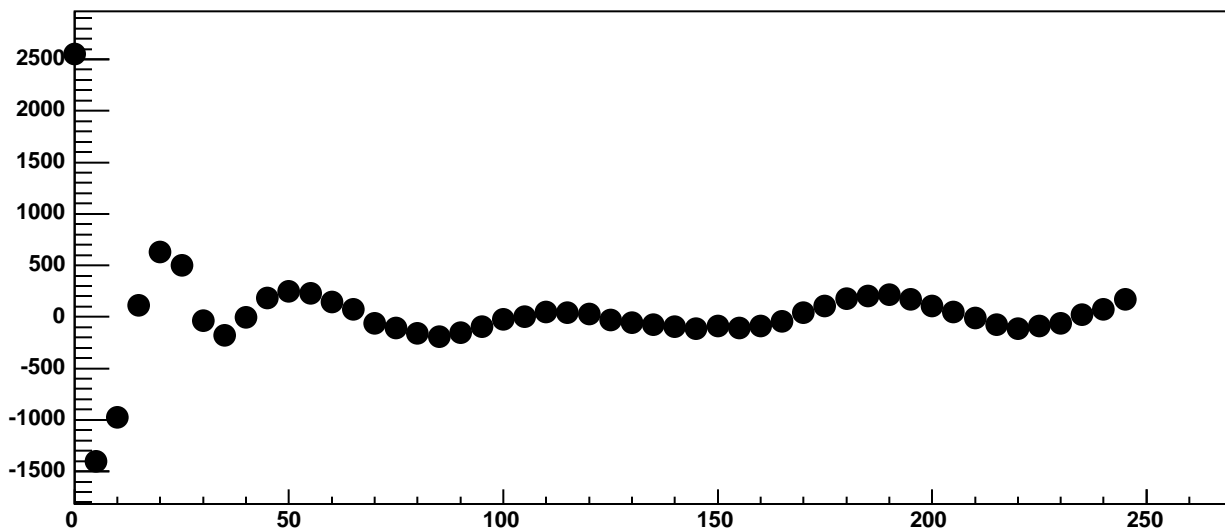


$\chi^2 / \text{ndf}$	8356 / 42
p0	-3784 ± 3.606
p1	1.778 ± 0.01512
p2	3.077e+04 ± 4.058
p3	28.6 ± 0.009509

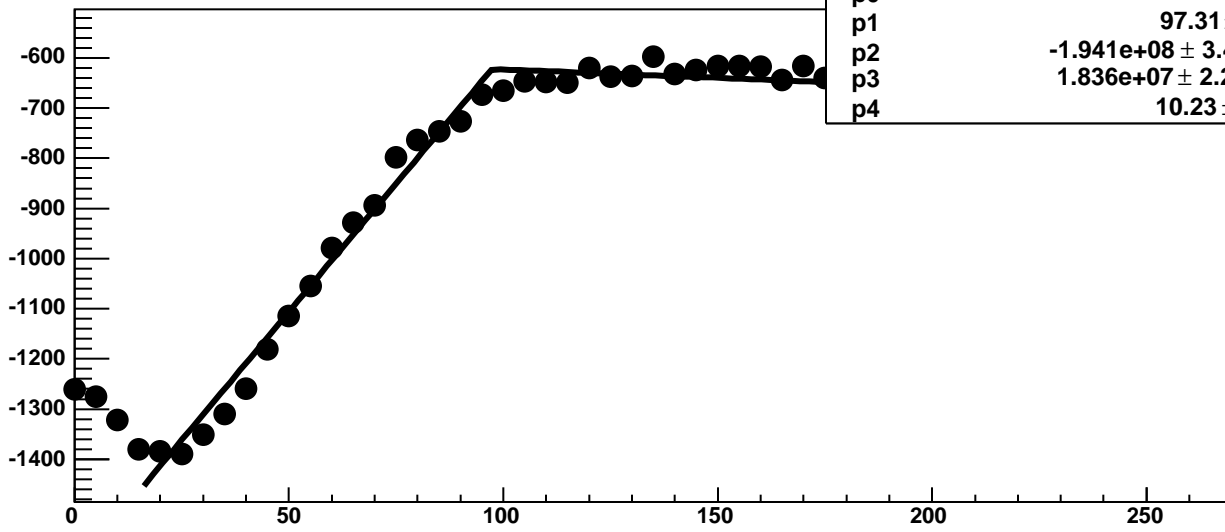
Chip 6, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

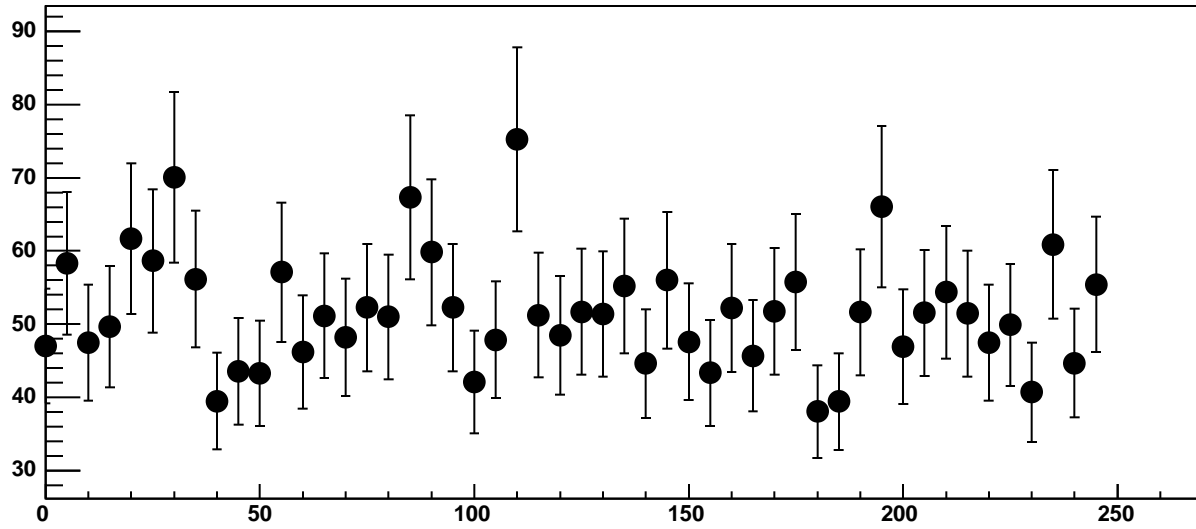


Chip 6, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

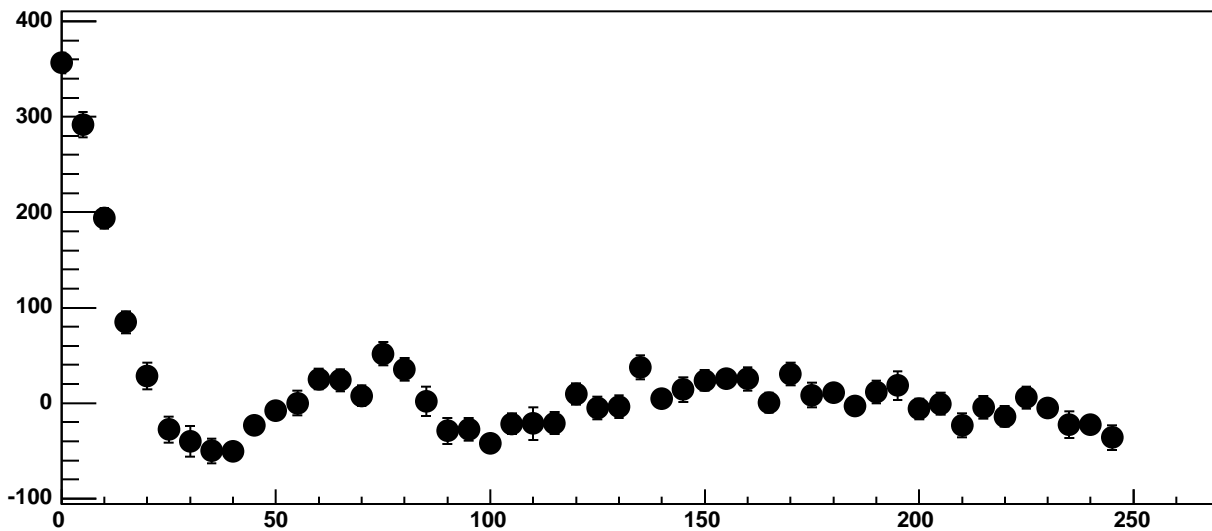


$\chi^2 / \text{ndf}$	249.1 / 41
p0	-622.1 ± 4.121
p1	97.31 ± 0.7011
p2	-1.941e+08 ± 3.447e+06
p3	1.836e+07 ± 2.257e+05
p4	10.23 ± 0.1252

Chip 6, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold

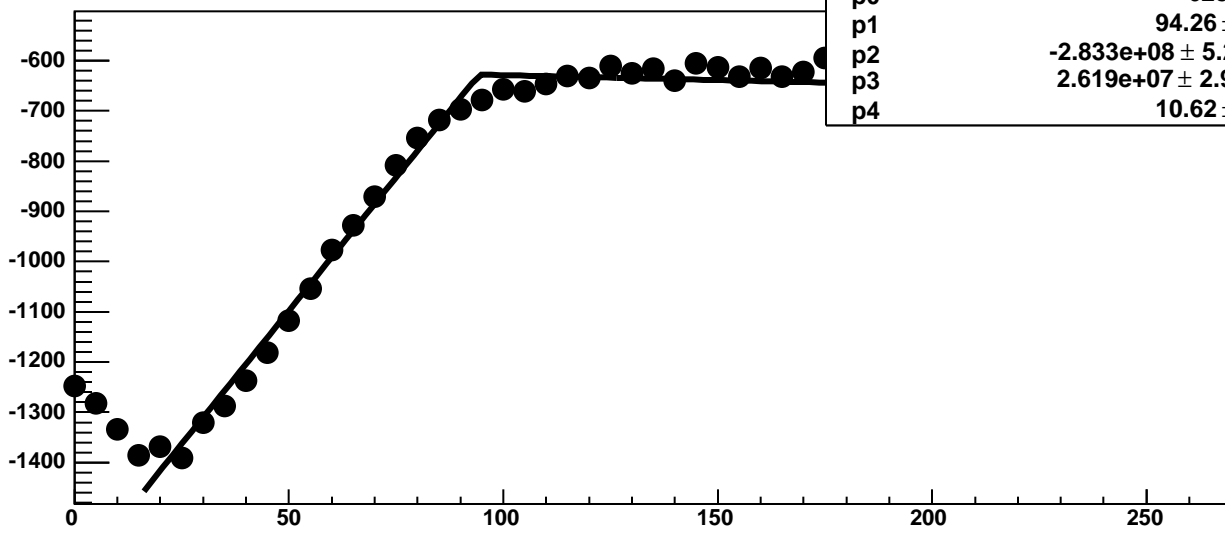


Chip 6, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



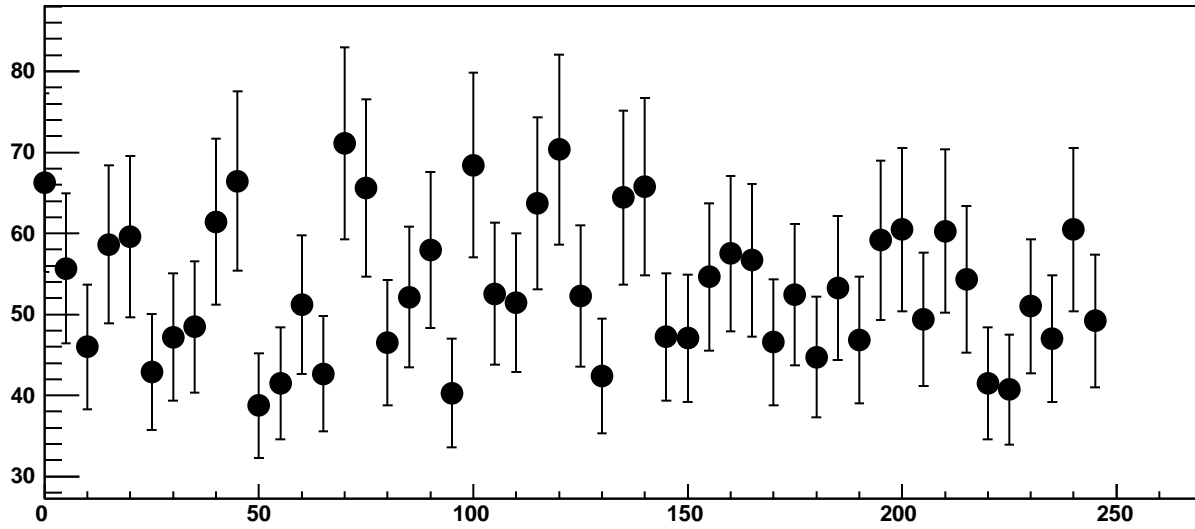


Chip 6, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

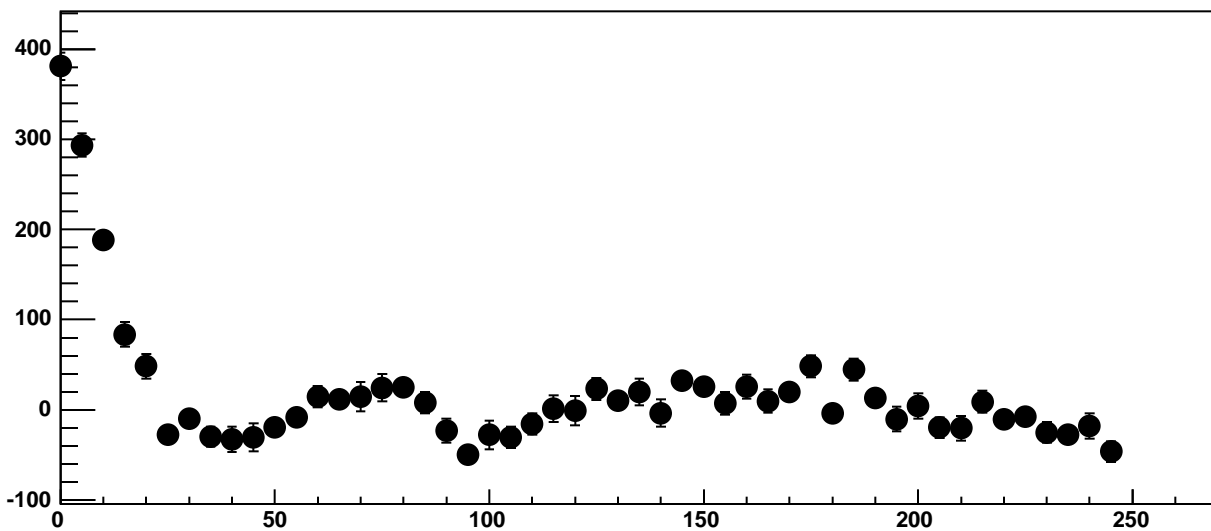


$\chi^2 / \text{ndf}$	219.1 / 41
p0	-628 ± 4.225
p1	94.26 ± 0.7073
p2	-2.833e+08 ± 5.217e+06
p3	2.619e+07 ± 2.906e+05
p4	10.62 ± 0.1332

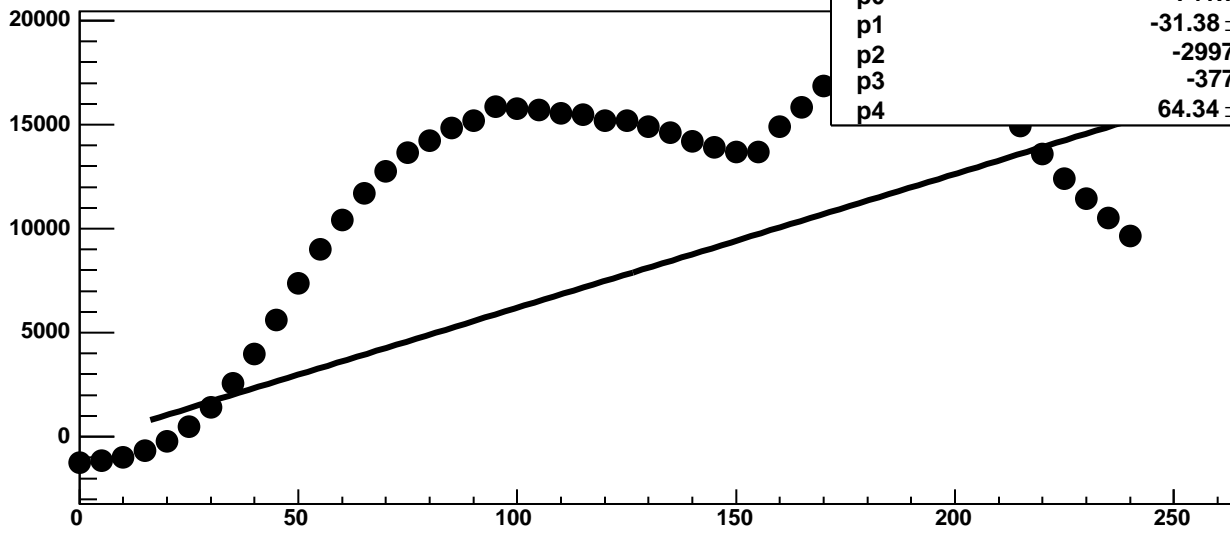
Chip 6, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 6, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

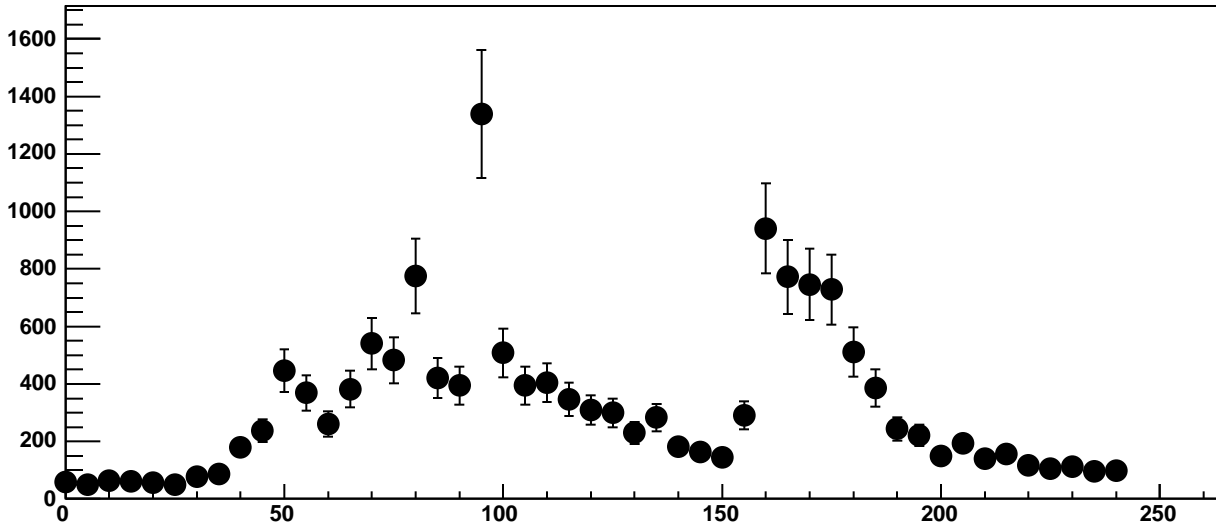


Chip 6, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold

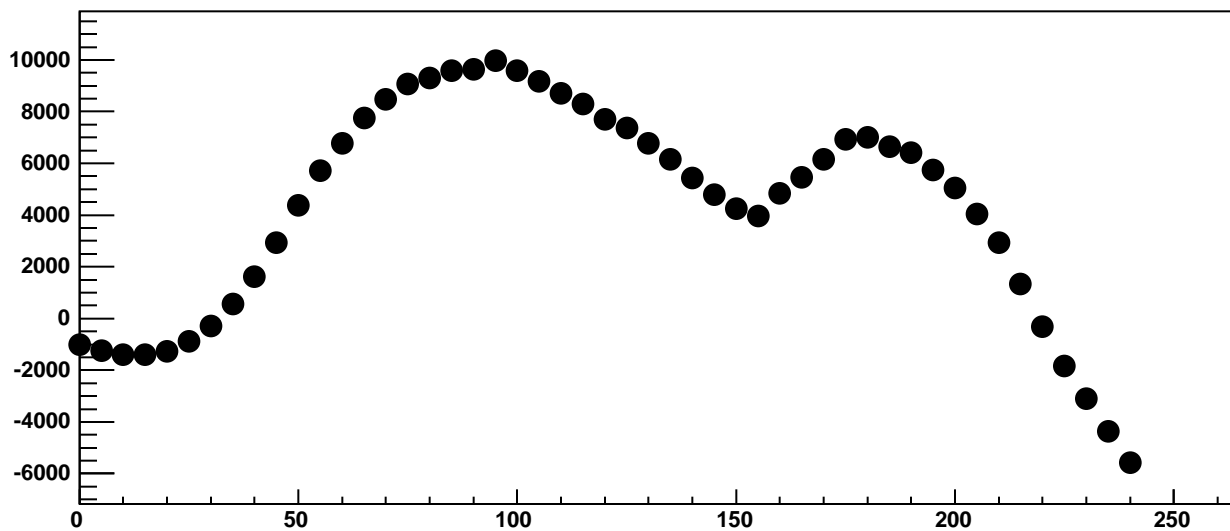


$\chi^2 / \text{ndf}$	4.313e+05 / 41
p0	741.7 ± 28.71
p1	-31.38 ± 0.4174
p2	-2997 ± 31.79
p3	-377 ± 43.21
p4	64.34 ± 0.1044

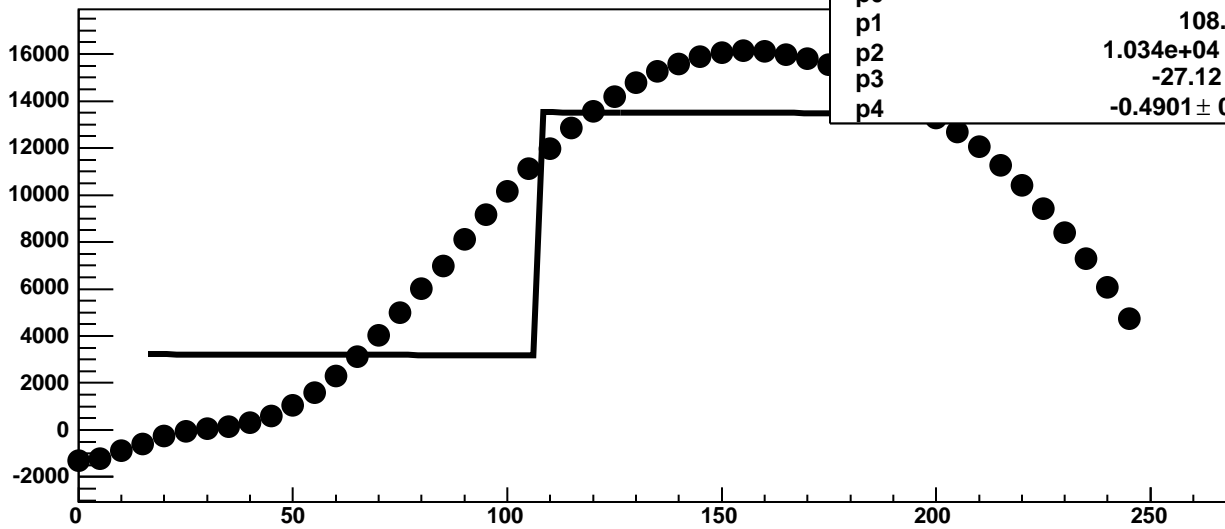
Chip 6, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



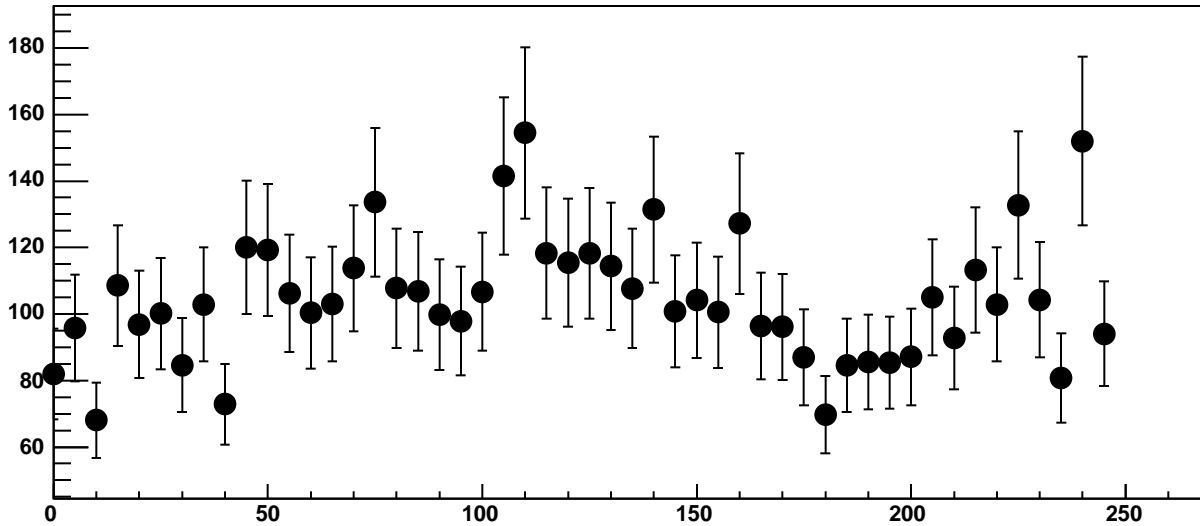
Chip 6, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold



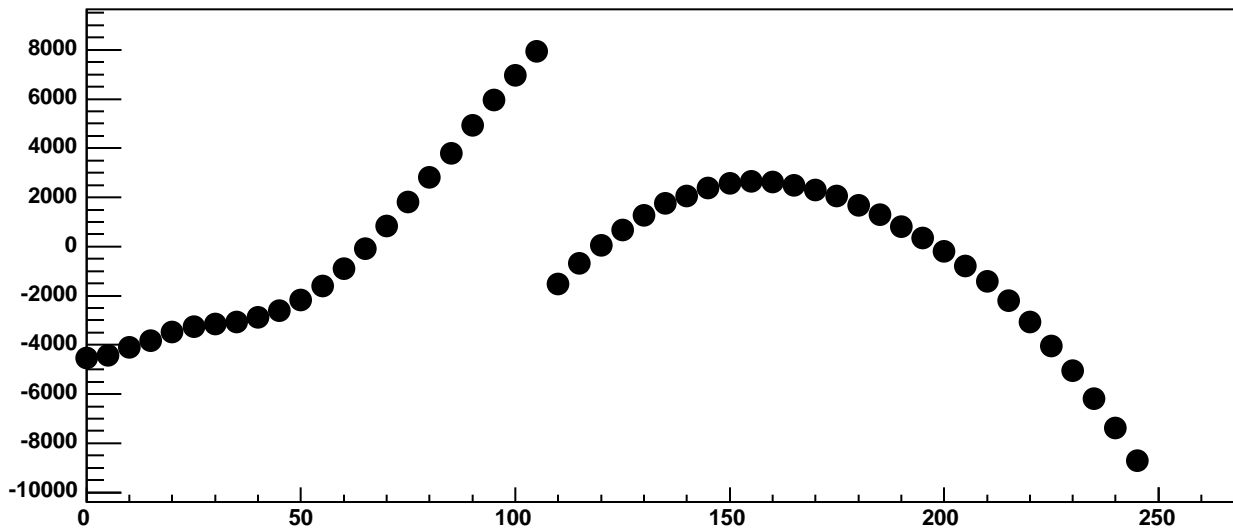
Chip 7, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold



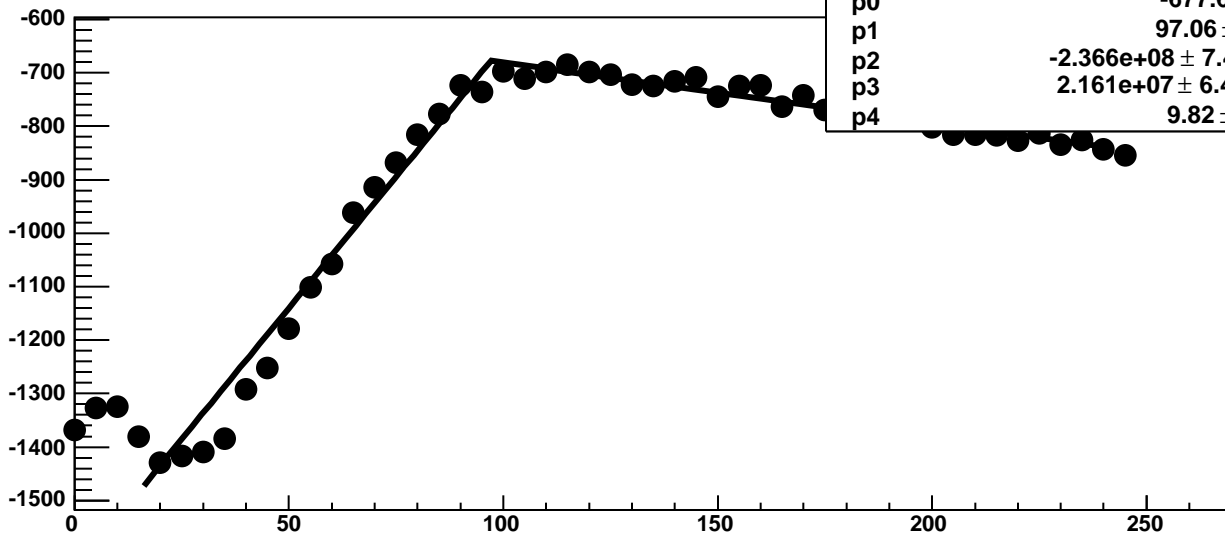
Chip 7, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold

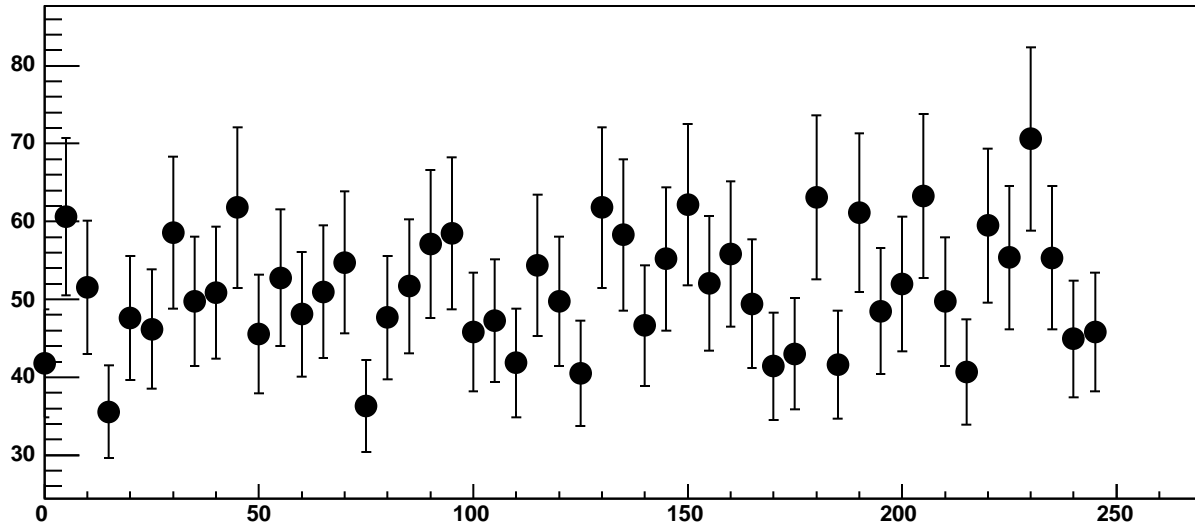


Chip 7, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

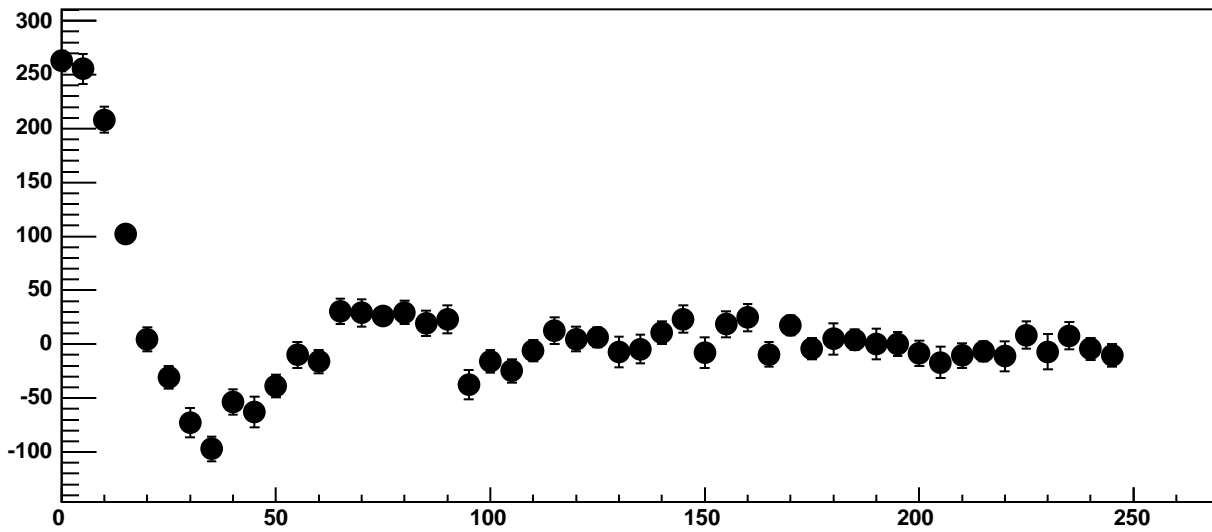


$\chi^2 / \text{ndf}$	398.6 / 41
p0	-677.6 ± 3.784
p1	97.06 ± 0.6278
p2	-2.366e+08 ± 7.491e+06
p3	2.161e+07 ± 6.443e+05
p4	9.82 ± 0.1074

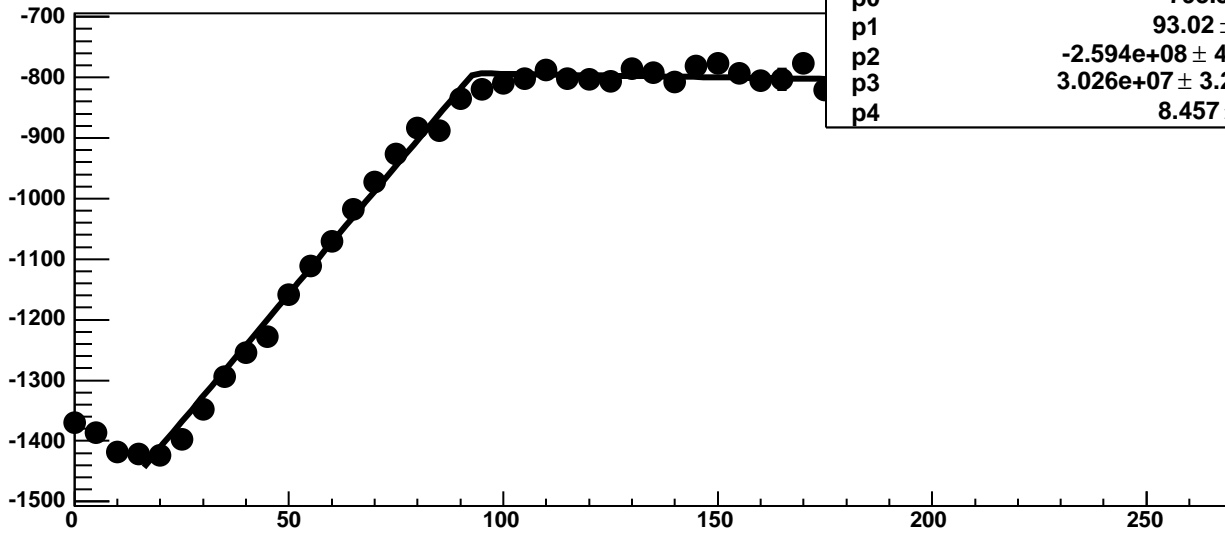
Chip 7, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold

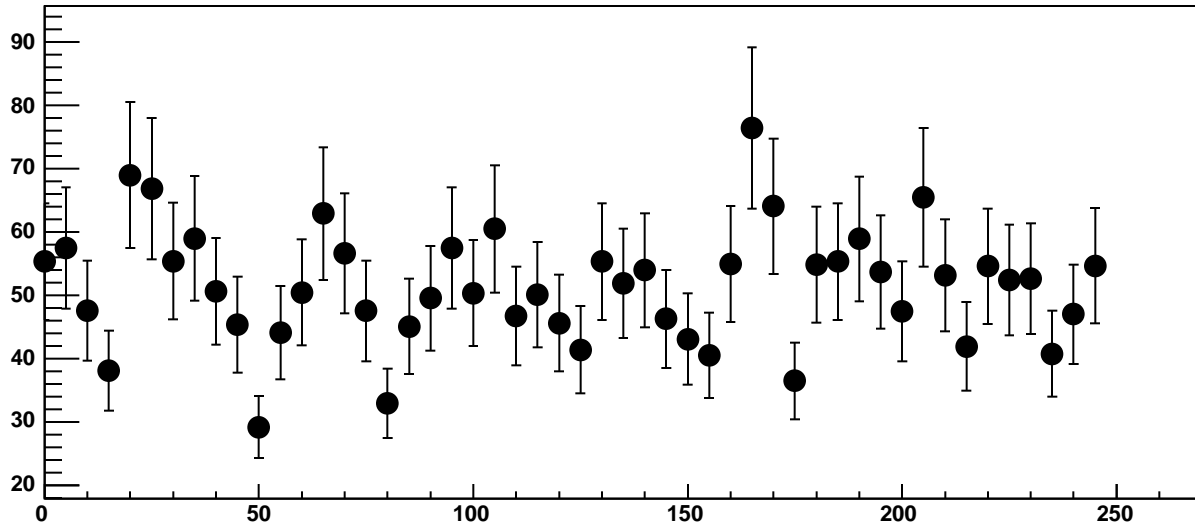


Chip 7, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

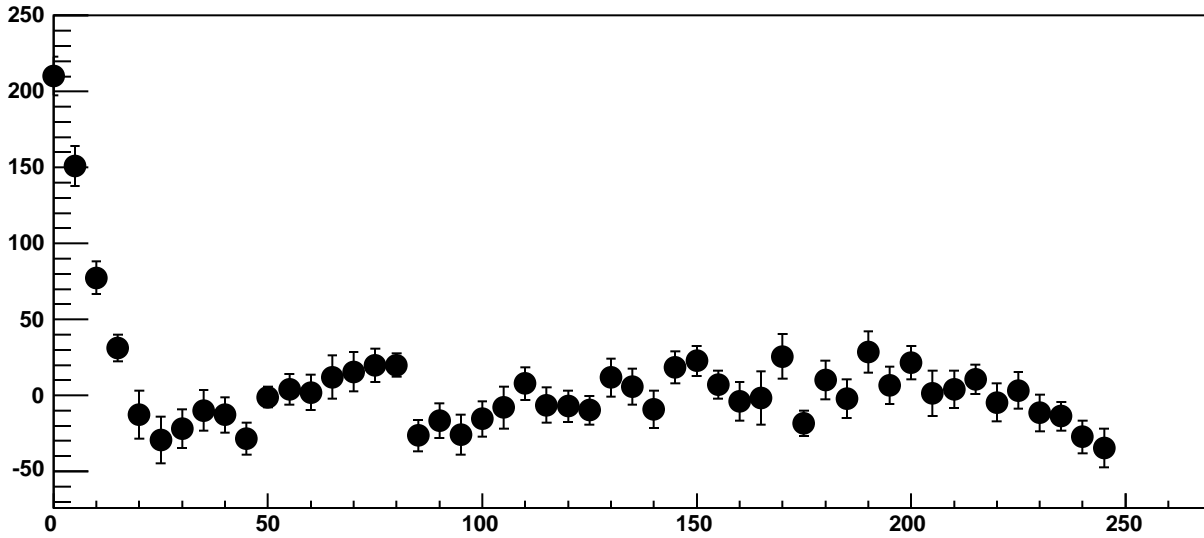


$\chi^2 / \text{ndf}$	97.19 / 41
p0	$-793.3 \pm 4.128$
p1	$93.02 \pm 0.7796$
p2	$-2.594\text{e}+08 \pm 4.74\text{e}+06$
p3	$3.026\text{e}+07 \pm 3.204\text{e}+05$
p4	$8.457 \pm 0.1171$

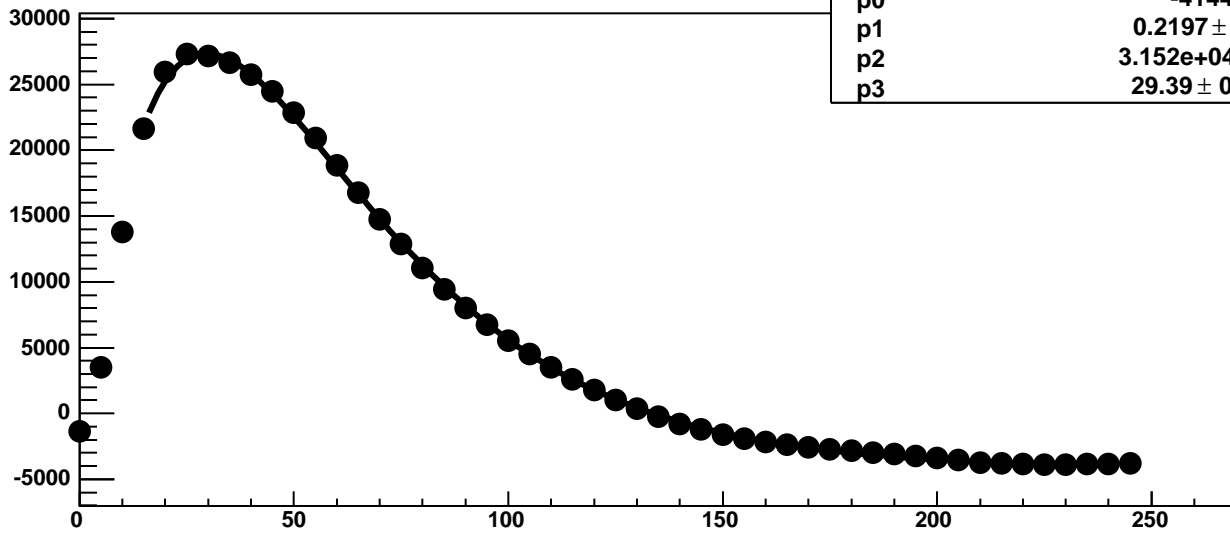
Chip 7, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold

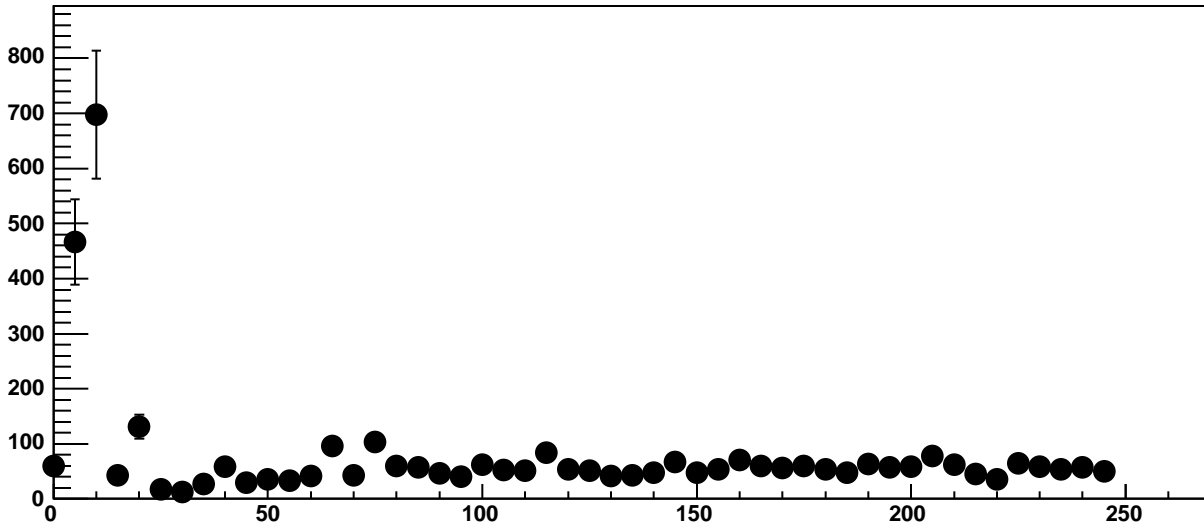


Chip 7, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold

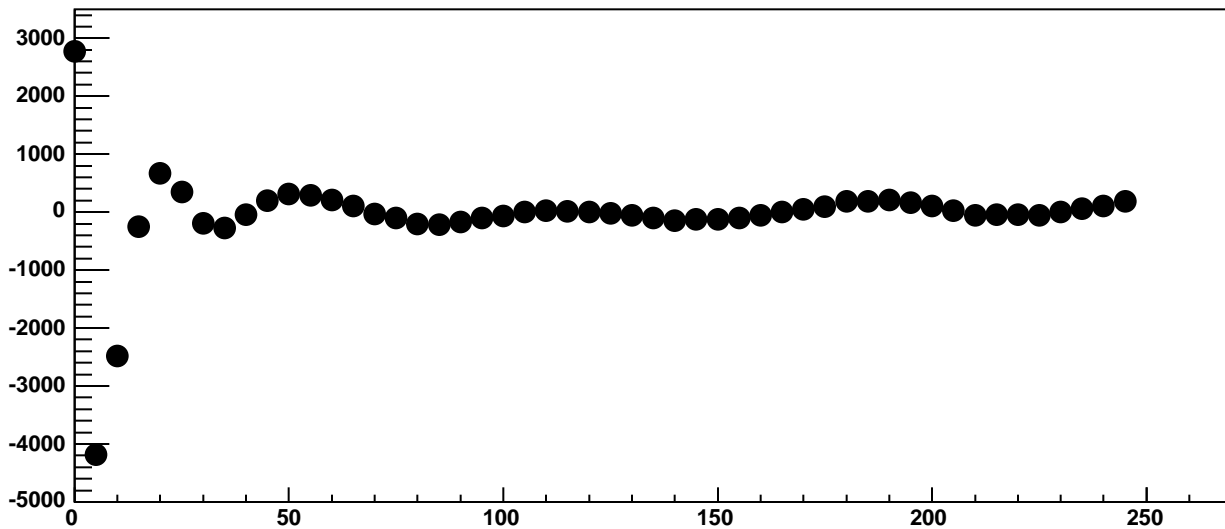


$\chi^2 / \text{ndf}$	2.271e+04 / 42
p0	-4144 ± 3.405
p1	0.2197 ± 0.01283
p2	3.152e+04 ± 3.691
p3	29.39 ± 0.008336

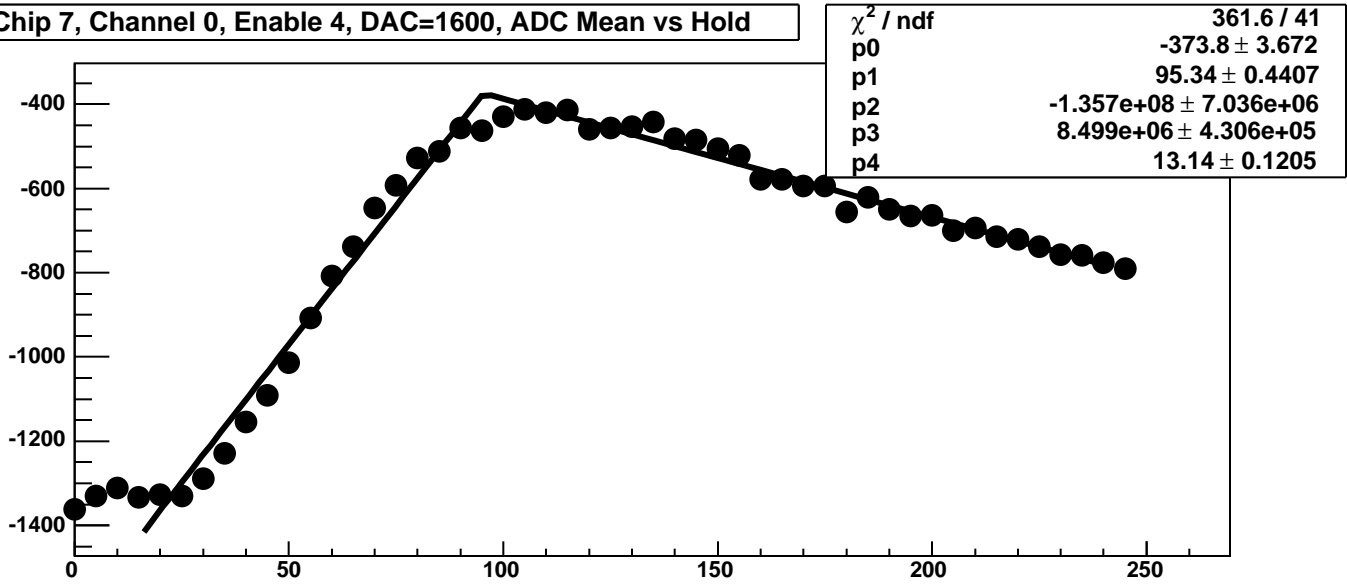
Chip 7, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



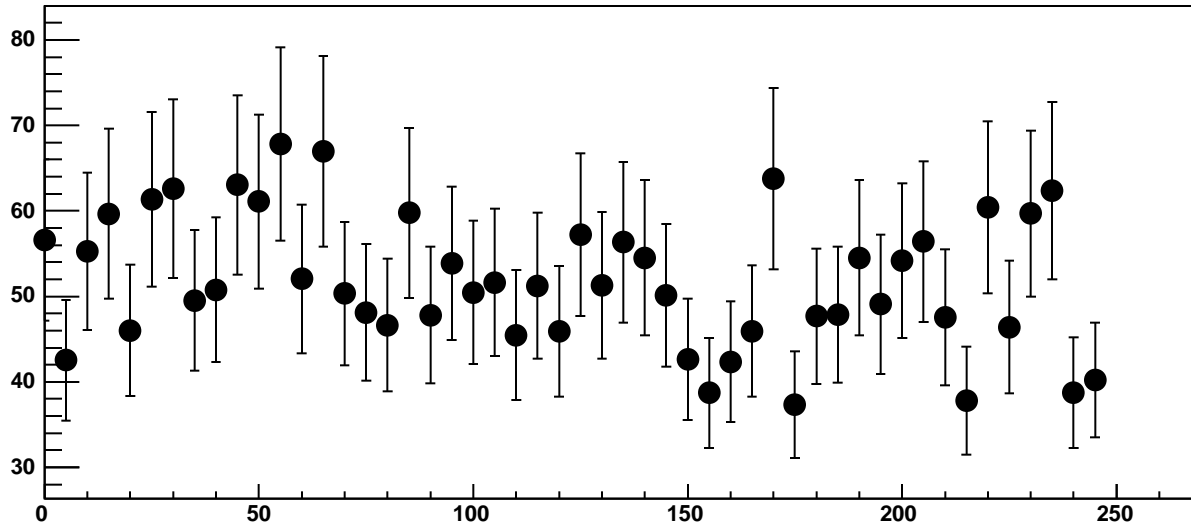
Chip 7, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold



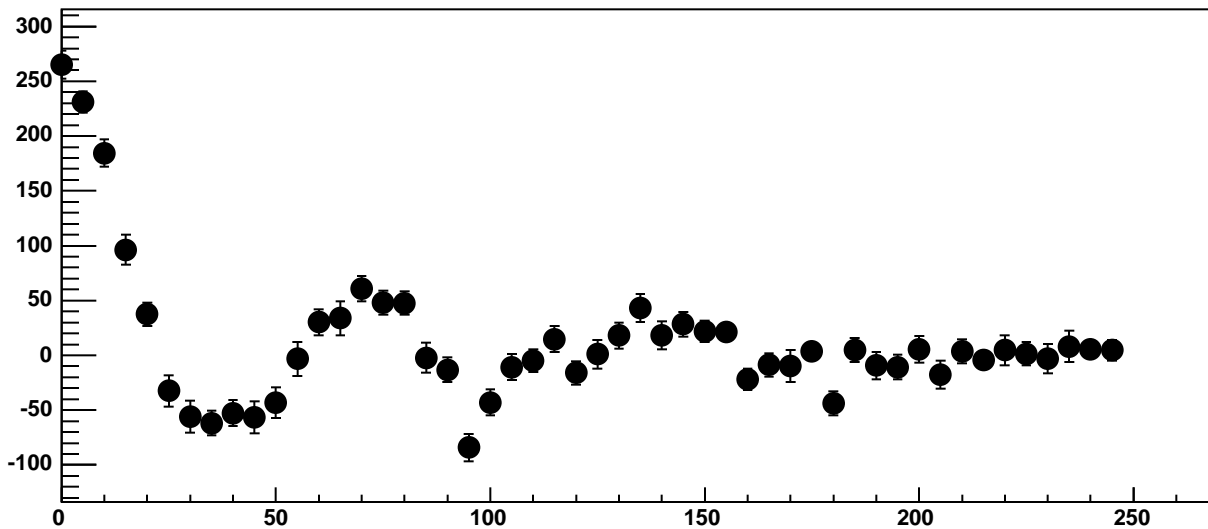
Chip 7, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold



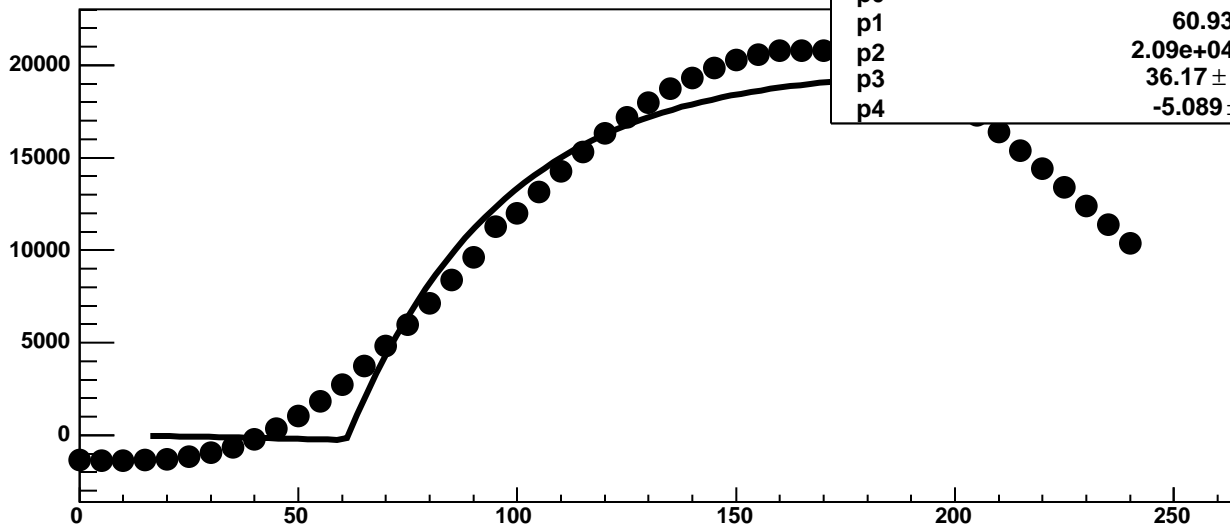
Chip 7, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

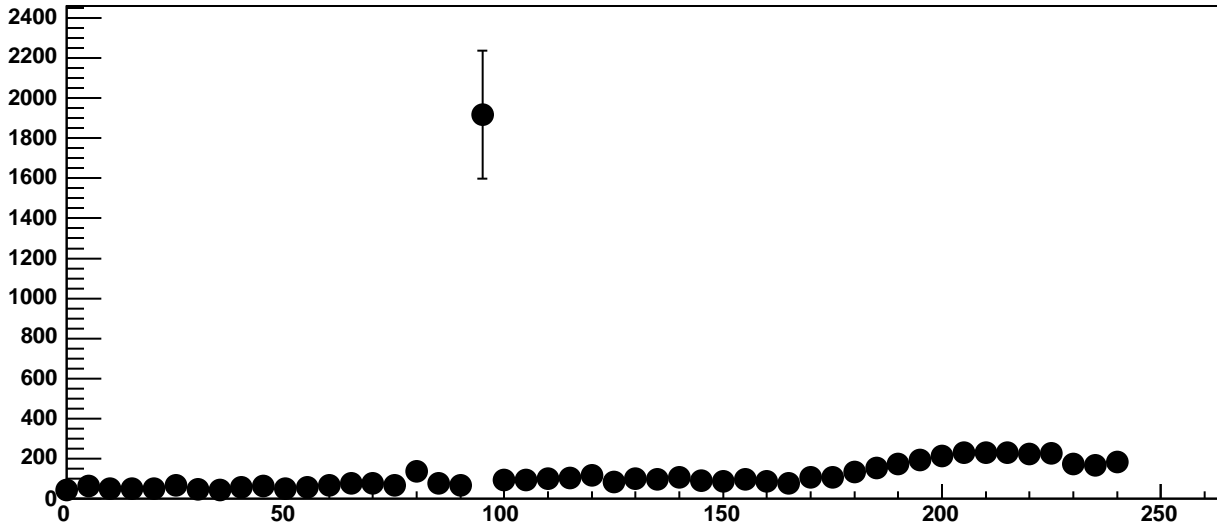


Chip 7, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

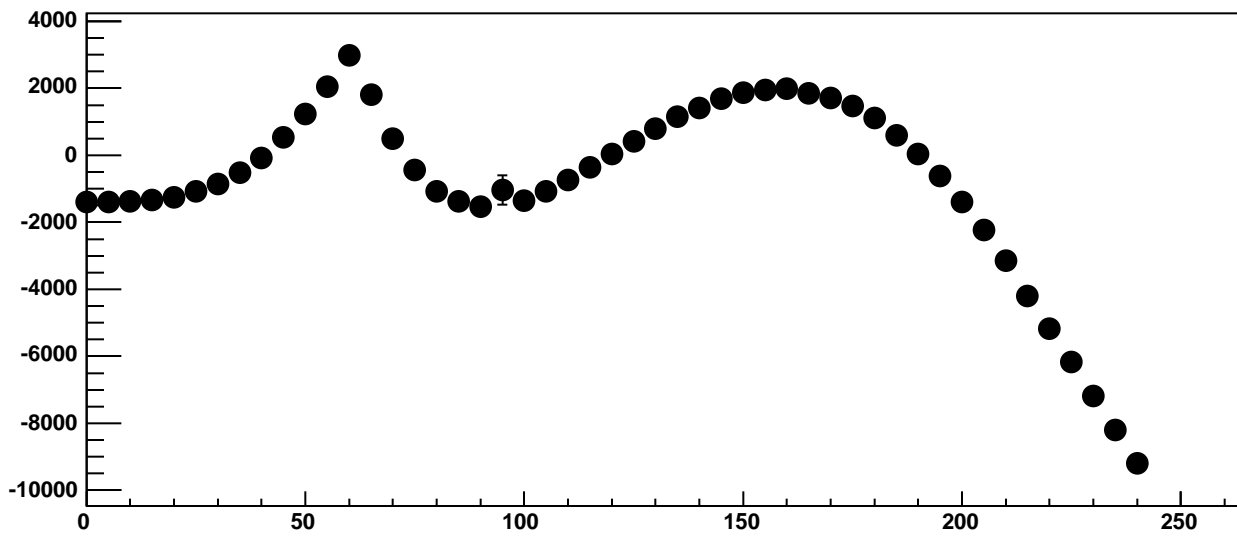


$\chi^2 / \text{ndf}$	3.668e+05 / 41
p0	-253.1 ± 6.253
p1	60.93 ± 0.028
p2	2.09e+04 ± 32.53
p3	36.17 ± 0.07128
p4	-5.089 ± 0.1957

Chip 7, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

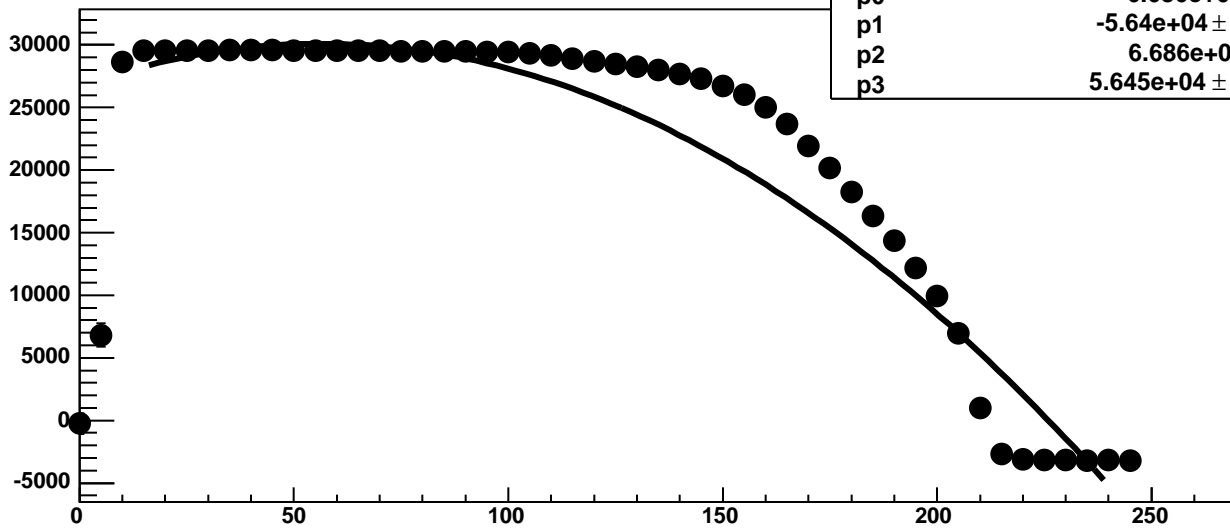


Chip 7, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold



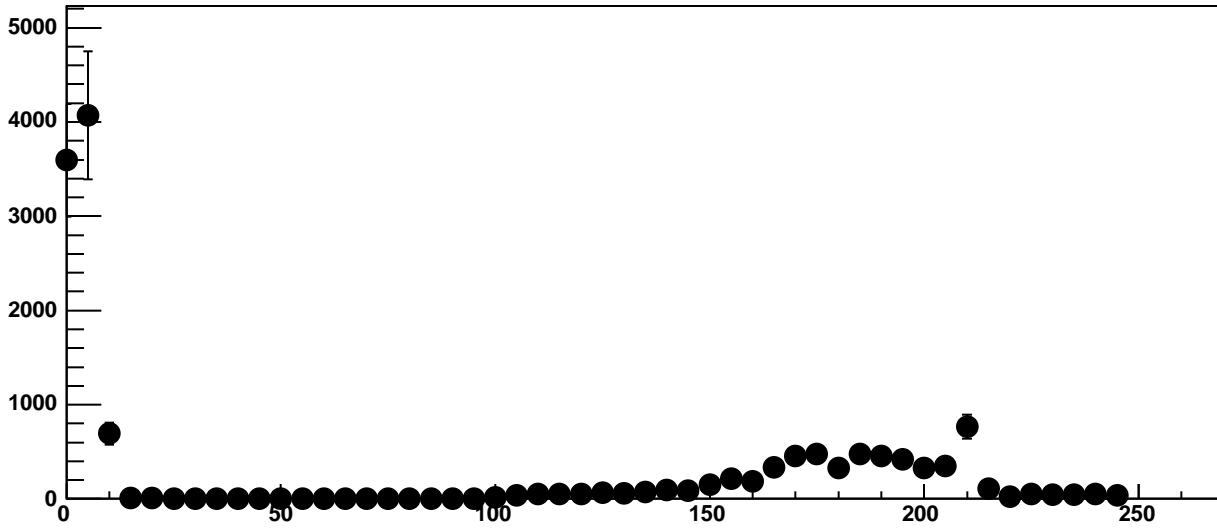


Chip 7, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold

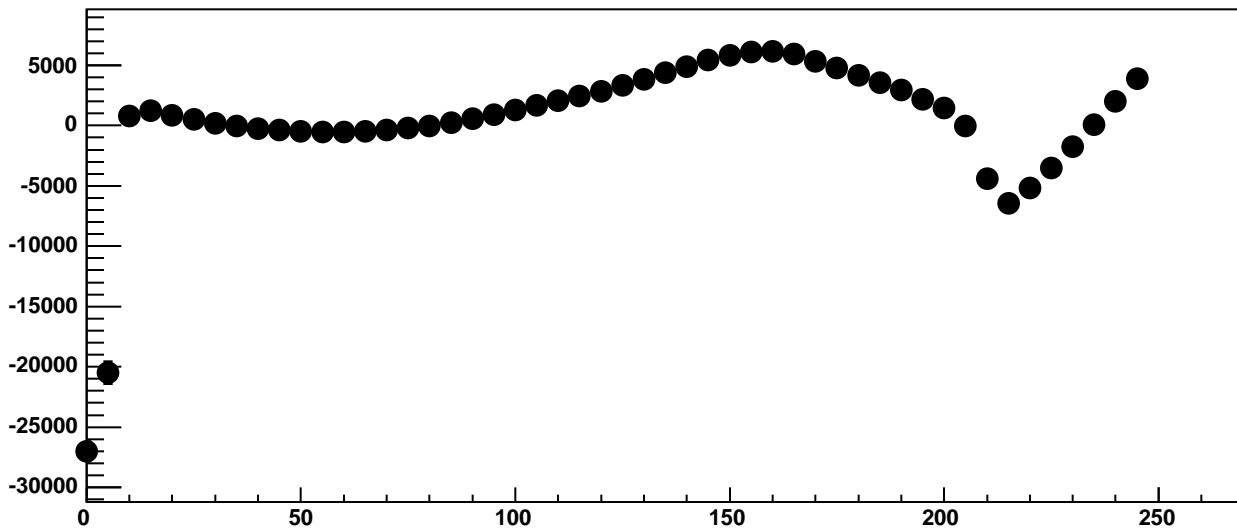


$\chi^2 / \text{ndf}$	5.356e+06 / 42
p0	-6.686e+09 ± 3.51
p1	-5.64e+04 ± 0.05798
p2	6.686e+09 ± 3.51
p3	5.645e+04 ± 0.05795

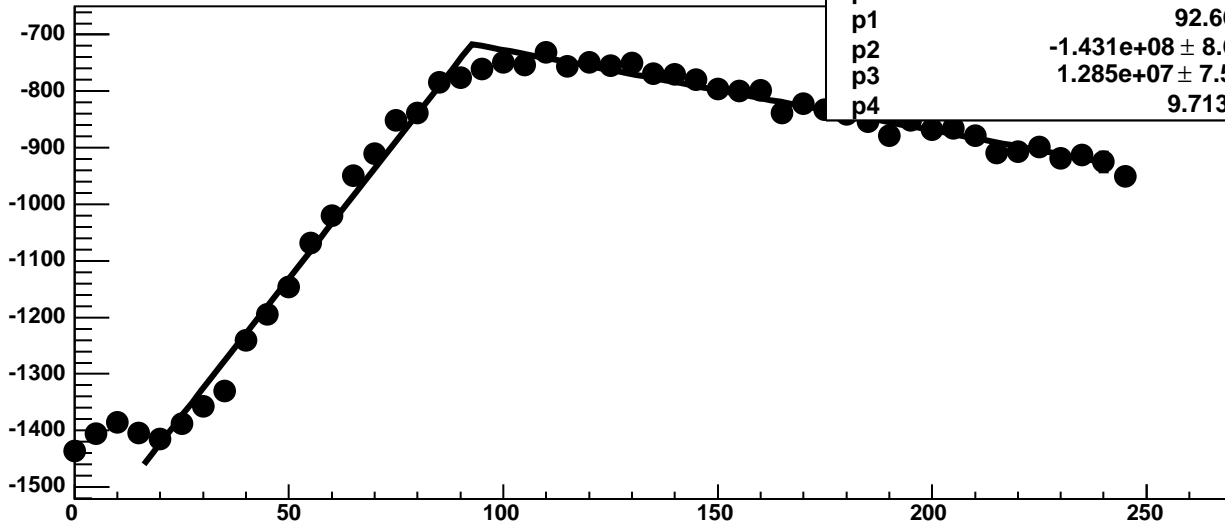
Chip 7, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold

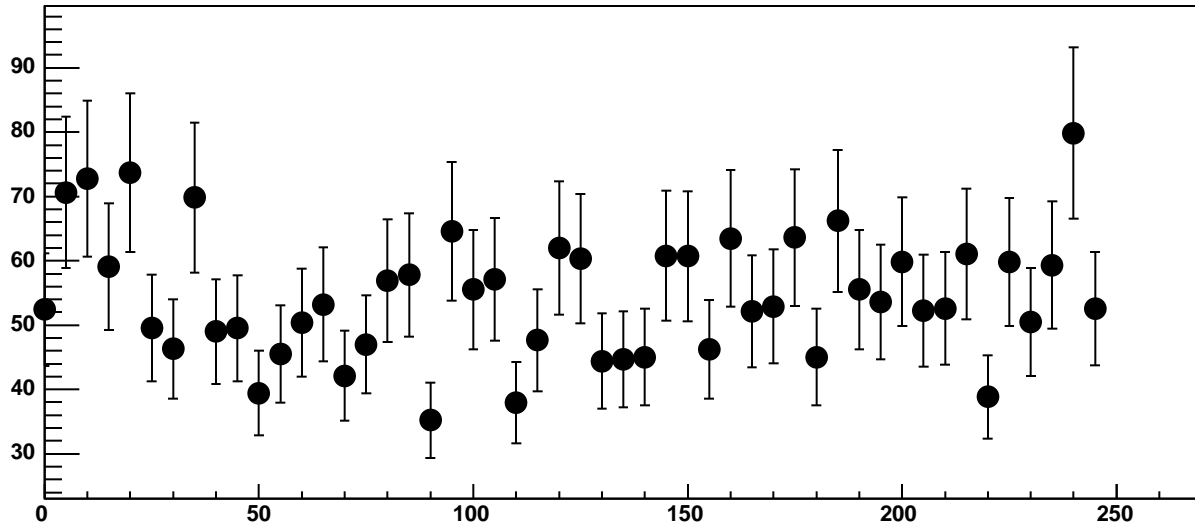


Chip 7, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

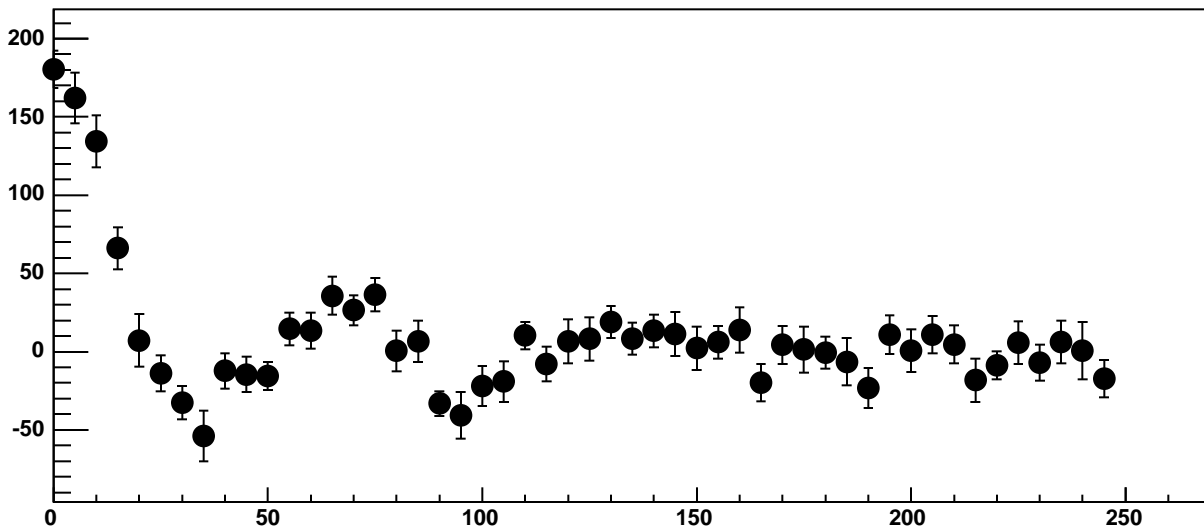


$\chi^2 / \text{ndf}$	134.7 / 41
p0	-716.6 ± 3.871
p1	92.66 ± 0.62
p2	-1.431e+08 ± 8.646e+06
p3	1.285e+07 ± 7.582e+05
p4	9.713 ± 0.125

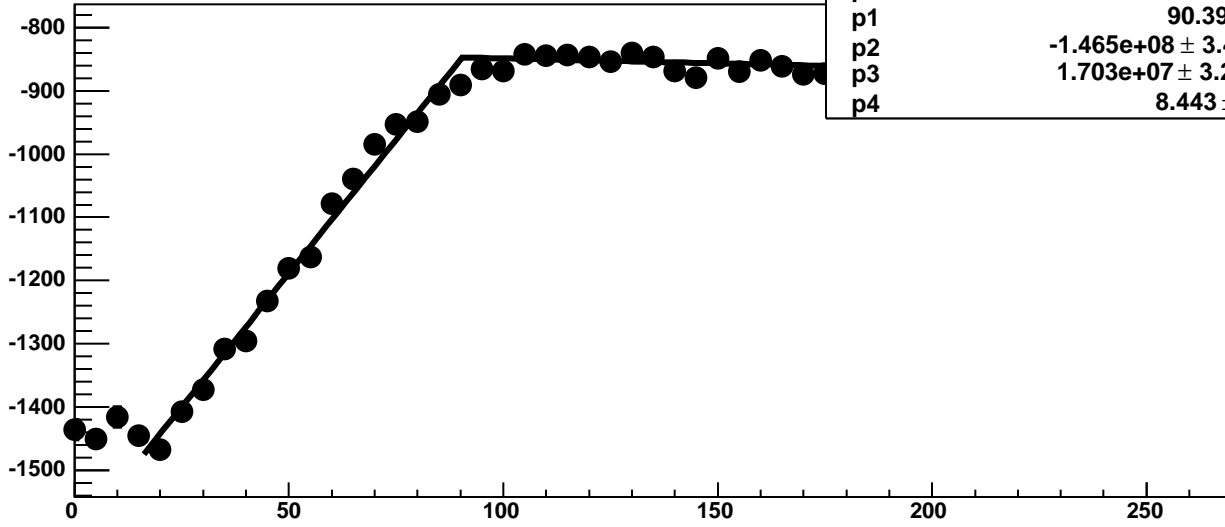
Chip 7, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

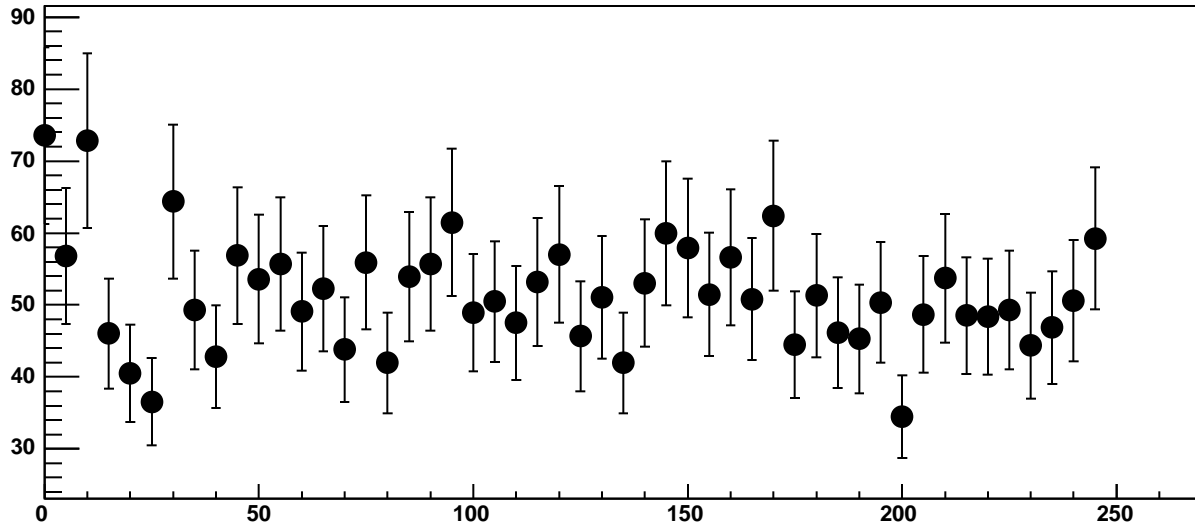


Chip 7, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

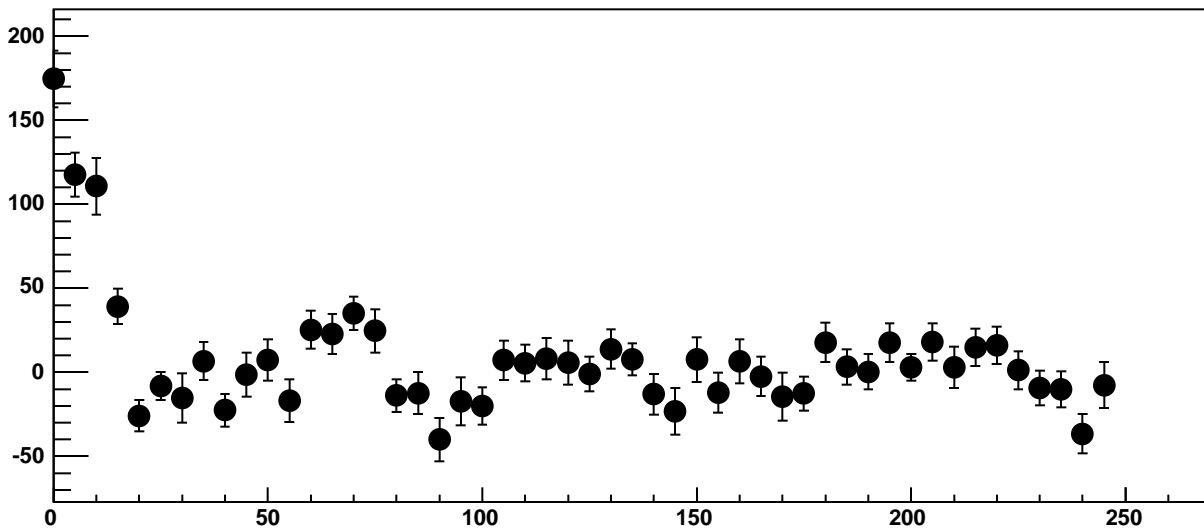


$\chi^2 / \text{ndf}$	108.1 / 41
p0	-847.4 ± 4.296
p1	90.39 ± 0.813
p2	-1.465e+08 ± 3.483e+06
p3	1.703e+07 ± 3.204e+05
p4	8.443 ± 0.1172

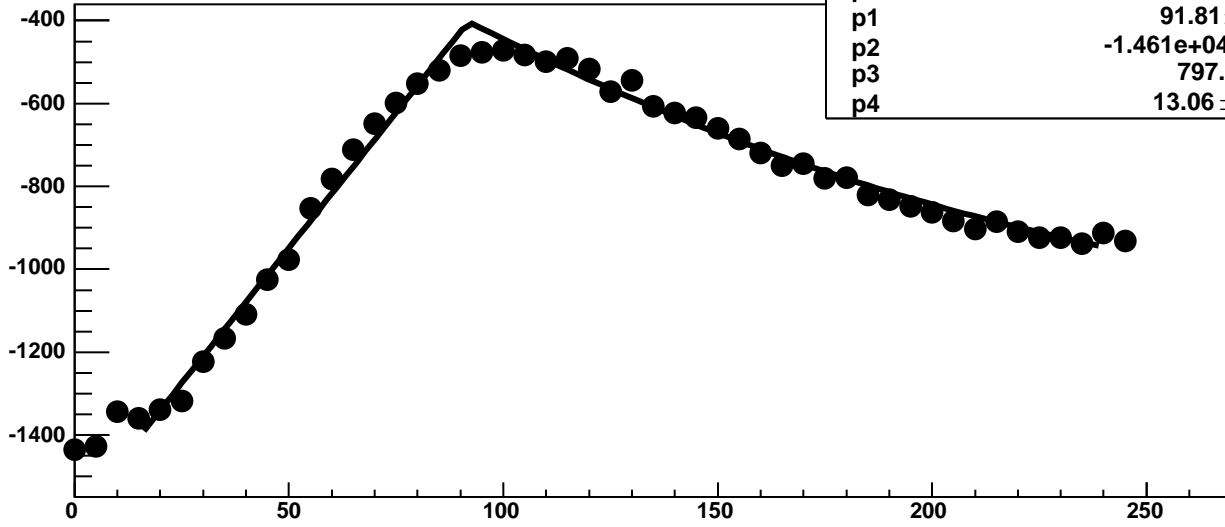
Chip 7, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

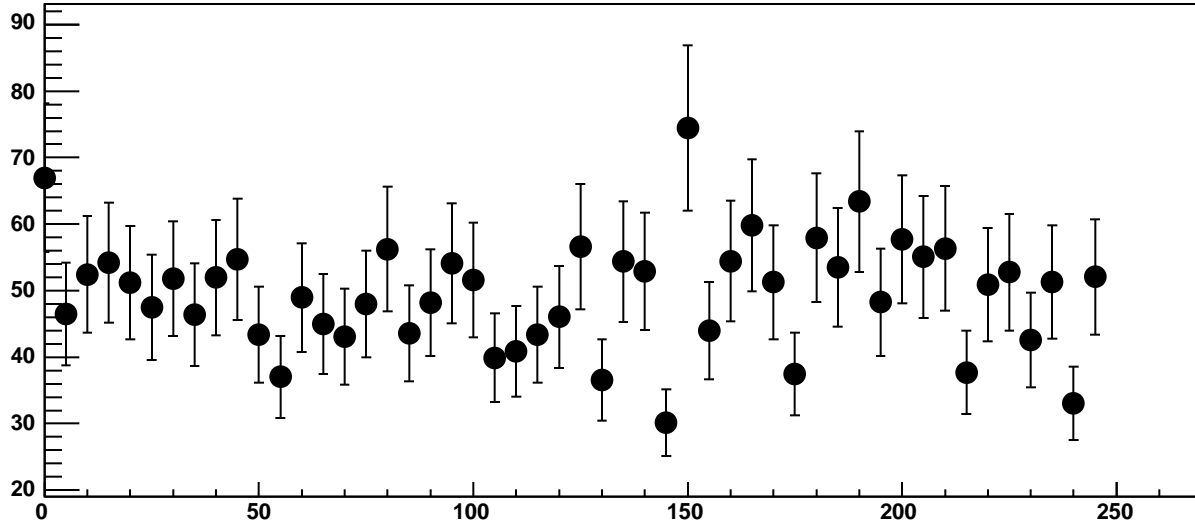


Chip 7, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold

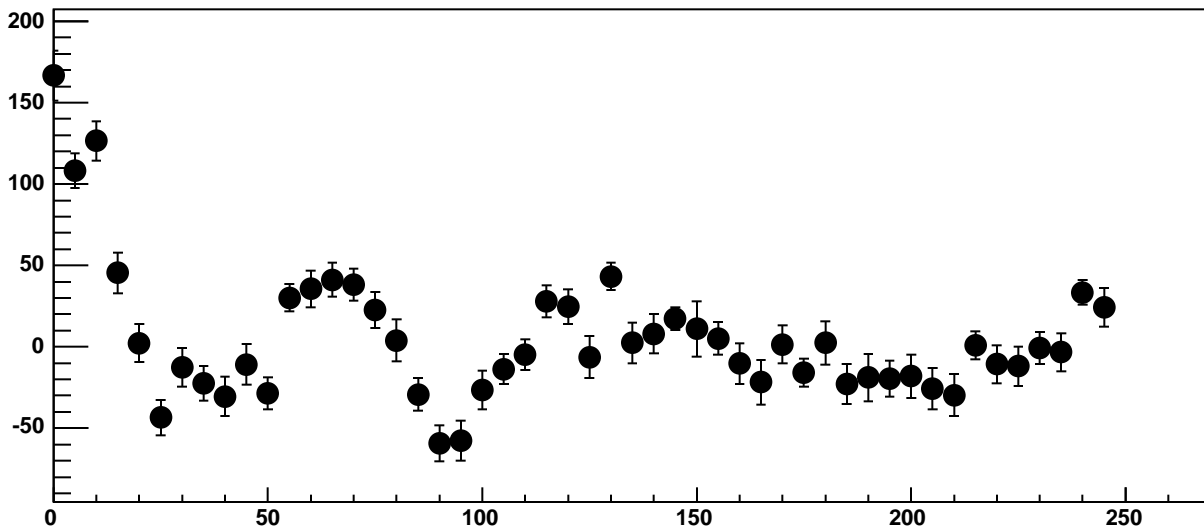


$\chi^2 / \text{ndf}$	269.9 / 41
p0	-402.4 ± 4.312
p1	91.81 ± 0.4201
p2	-1.461e+04 ± 1235
p3	797.1 ± 73.6
p4	13.06 ± 0.1224

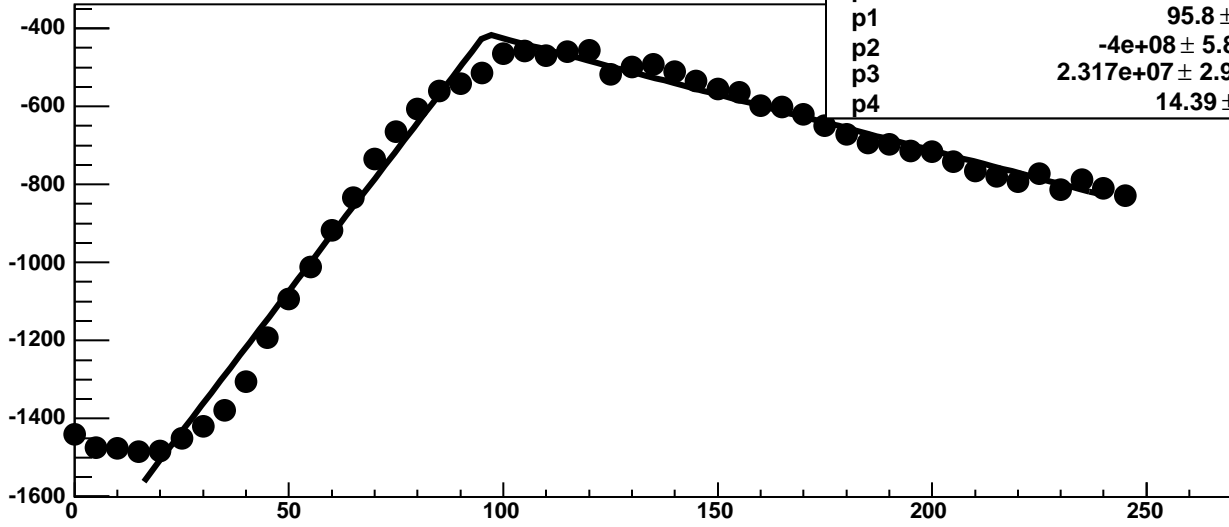
Chip 7, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold

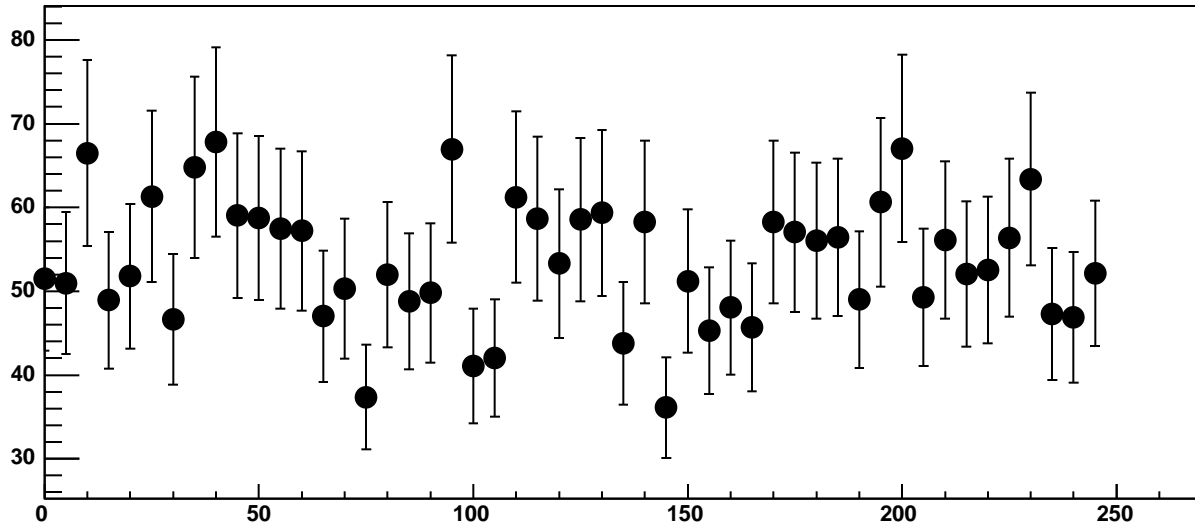


Chip 7, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

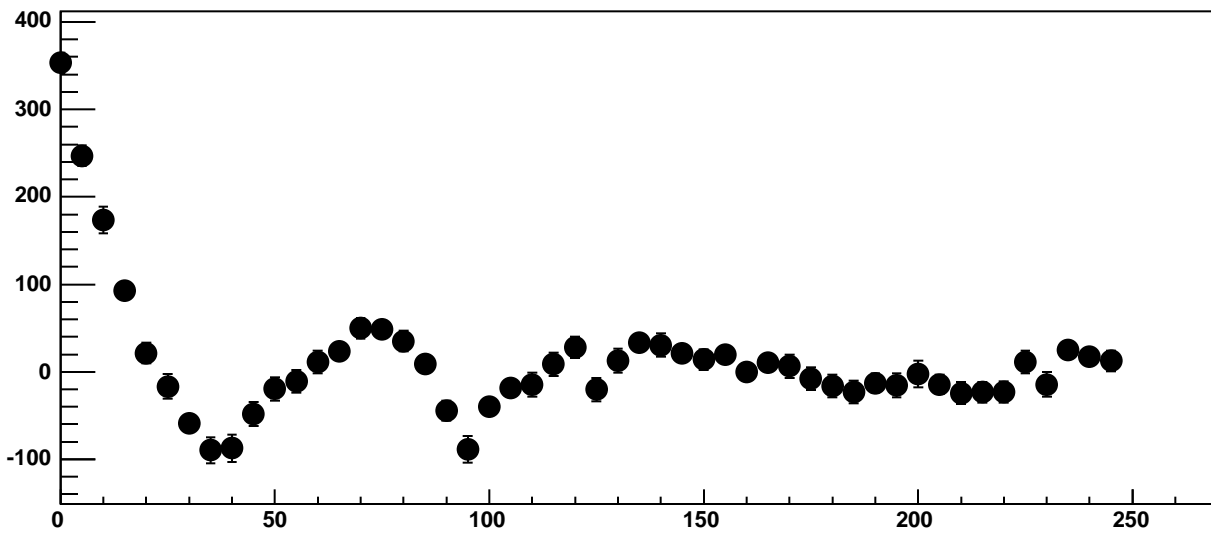


$\chi^2 / \text{ndf}$	390.7 / 41
p0	$-414.1 \pm 3.662$
p1	$95.8 \pm 0.4046$
p2	$-4e+08 \pm 5.832e+06$
p3	$2.317e+07 \pm 2.932e+05$
p4	$14.39 \pm 0.1192$

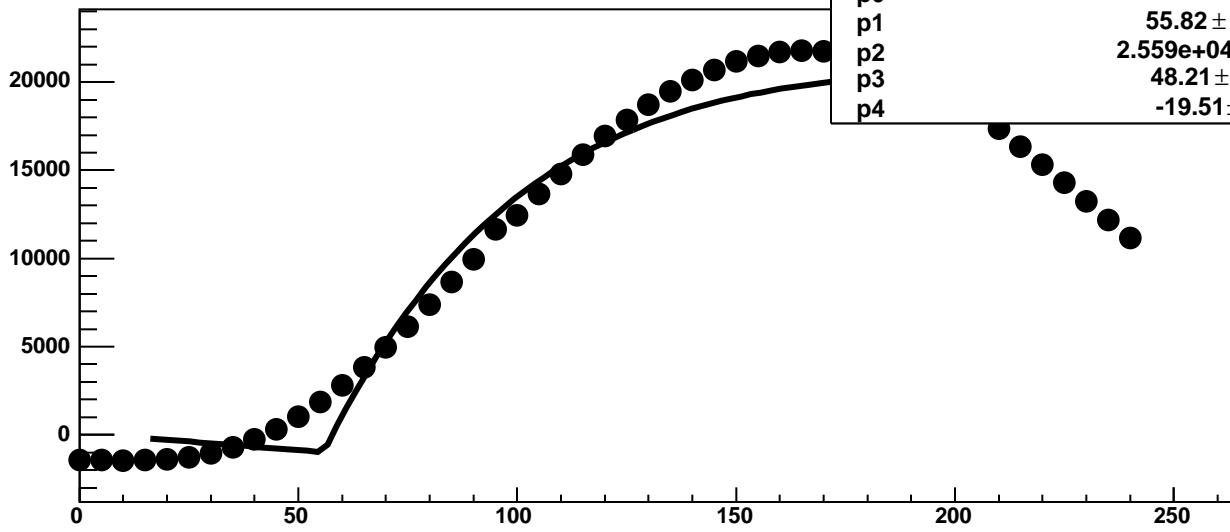
Chip 7, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

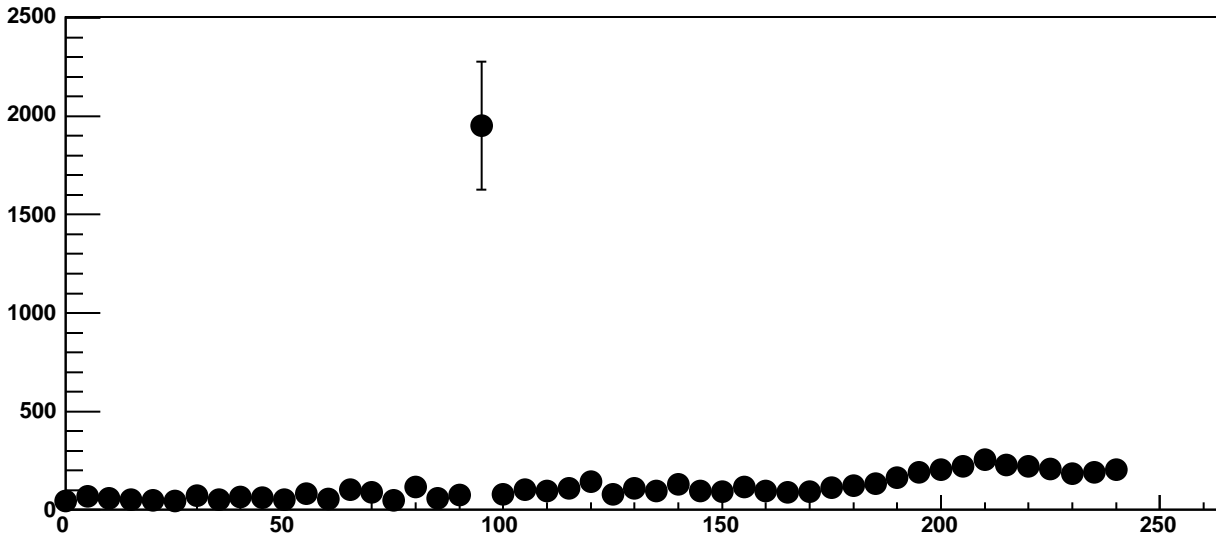


Chip 7, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

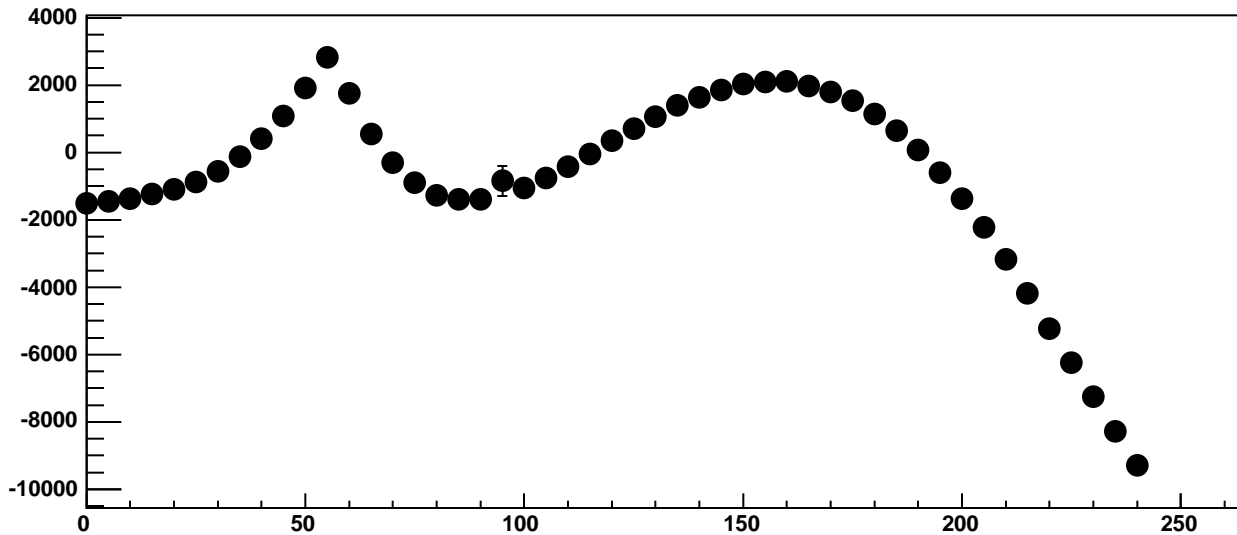


$\chi^2 / \text{ndf}$	3.379e+05 / 41
p0	-987.5 ± 6.962
p1	55.82 ± 0.02599
p2	2.559e+04 ± 46.37
p3	48.21 ± 0.08991
p4	-19.51 ± 0.2449

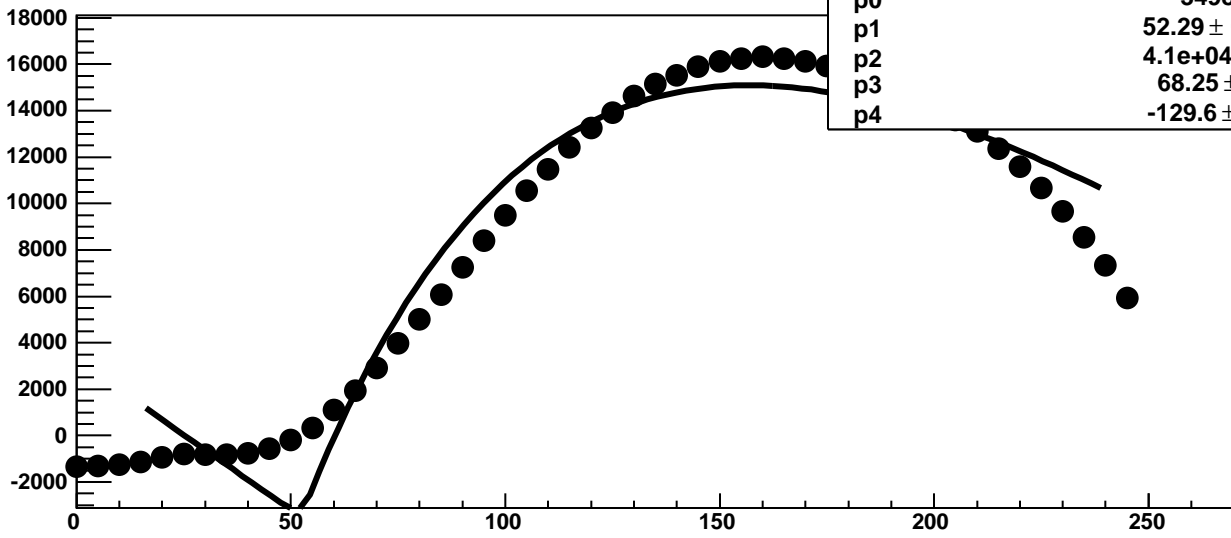
Chip 7, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



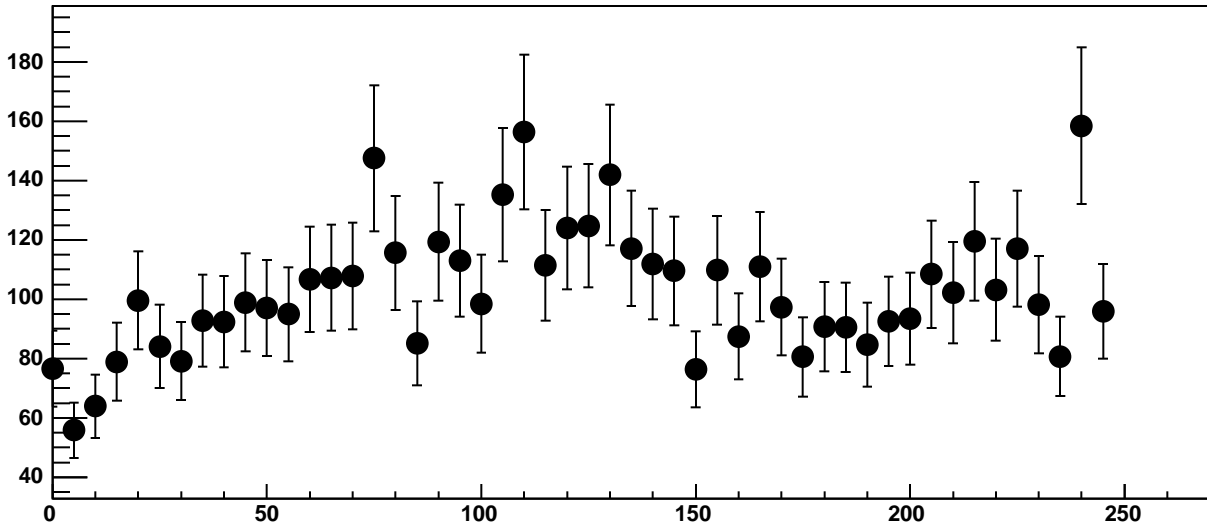
Chip 7, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold



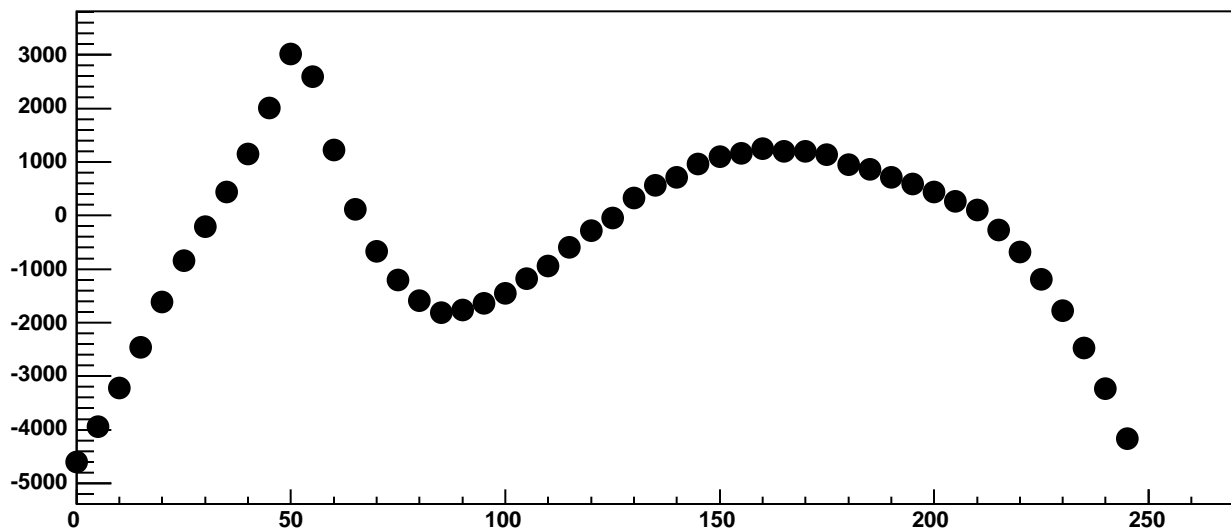
Chip 7, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold



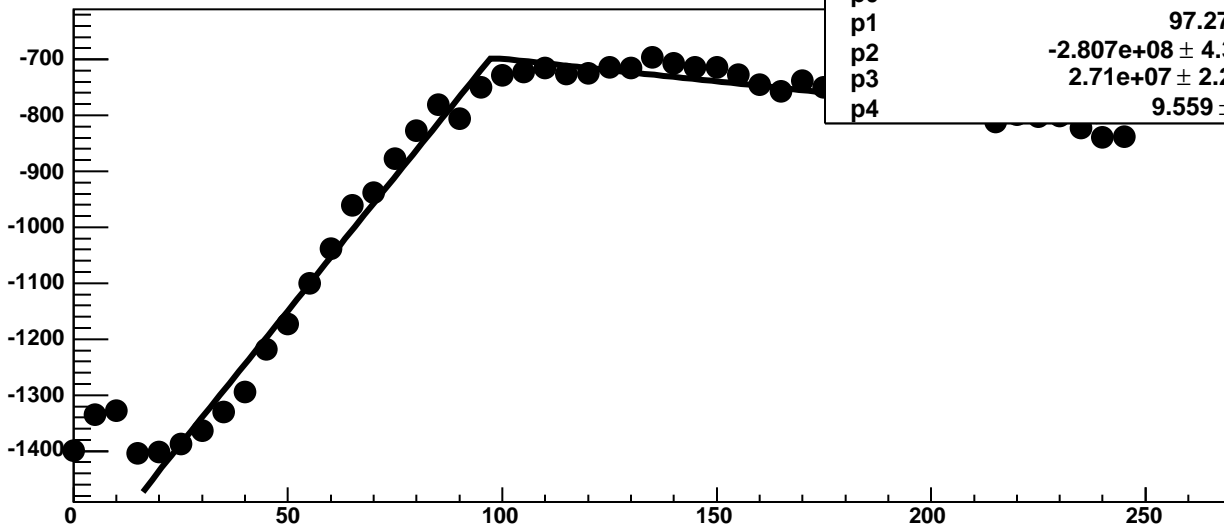
Chip 7, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

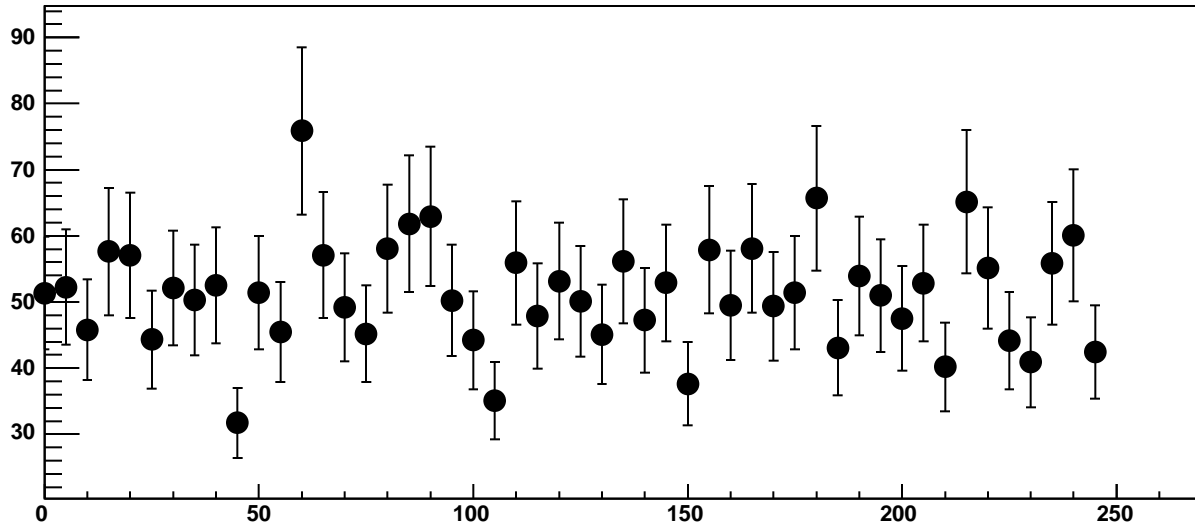


Chip 7, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

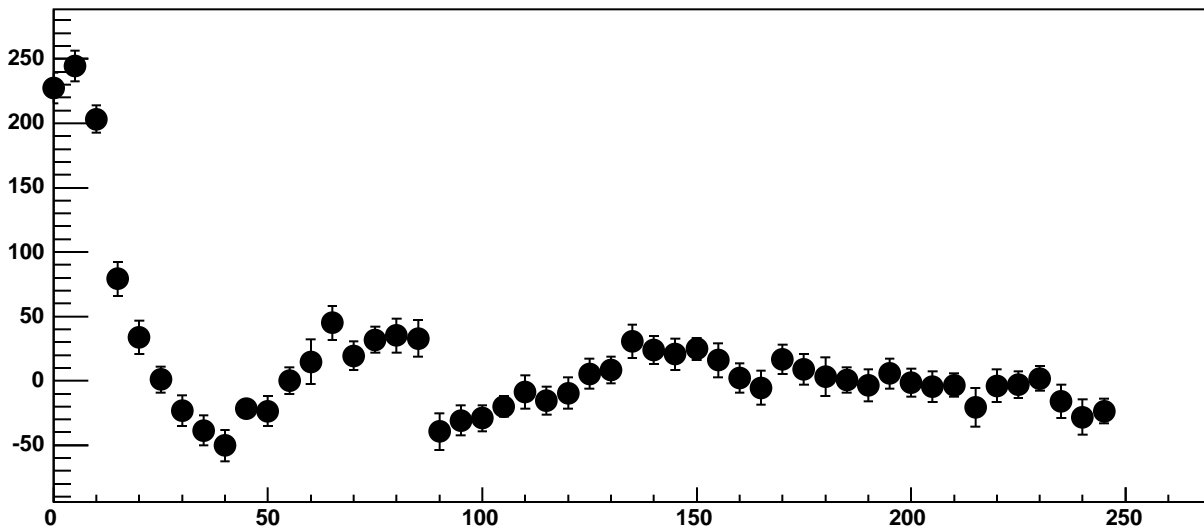


$\chi^2 / \text{ndf}$	192.8 / 41
p0	-697 ± 3.721
p1	97.27 ± 0.701
p2	-2.807e+08 ± 4.343e+06
p3	2.71e+07 ± 2.293e+05
p4	9.559 ± 0.1215

Chip 7, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

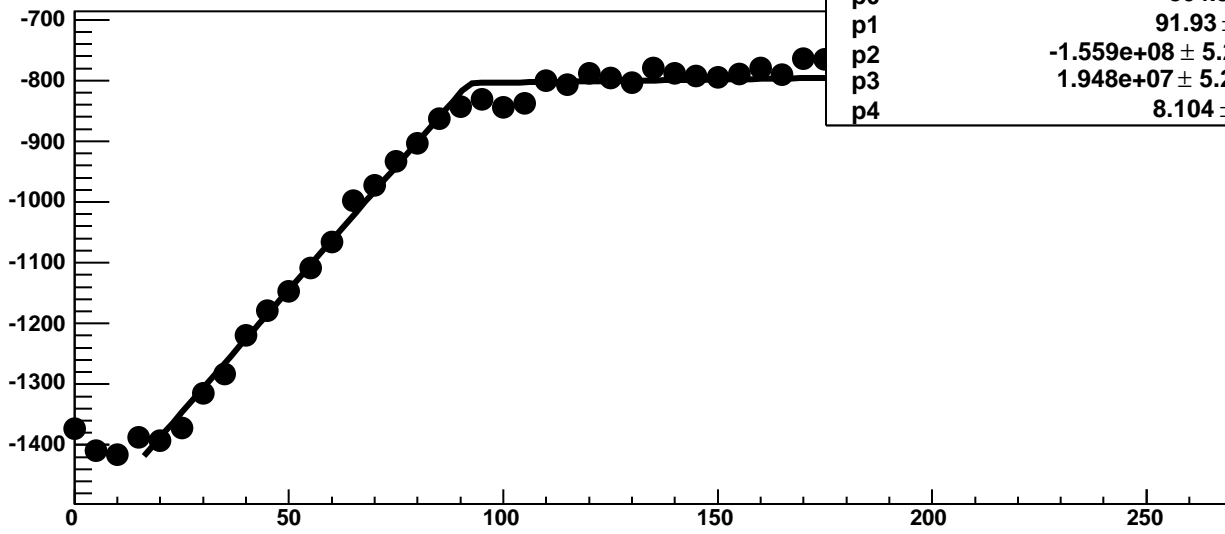


Chip 7, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



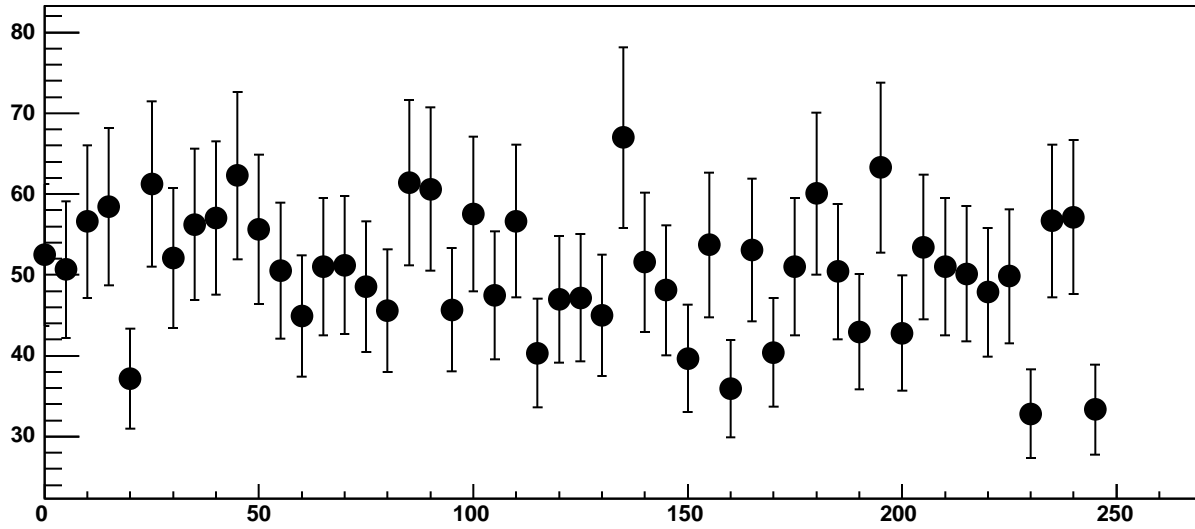


Chip 7, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

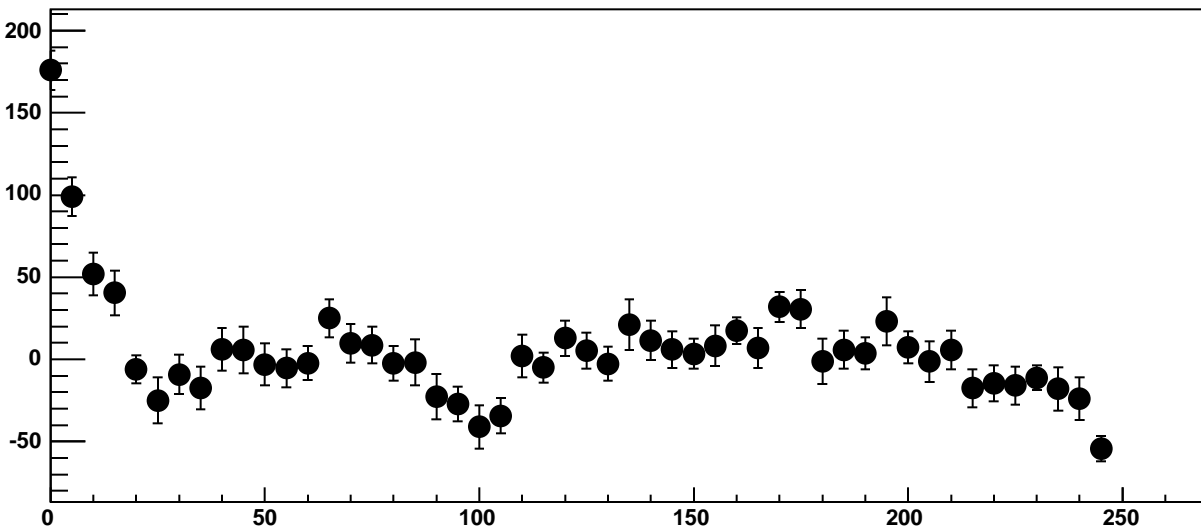


$\chi^2 / \text{ndf}$	97.29 / 41
p0	-804.3 ± 4.094
p1	91.93 ± 0.8913
p2	-1.559e+08 ± 5.278e+06
p3	1.948e+07 ± 5.258e+05
p4	8.104 ± 0.1276

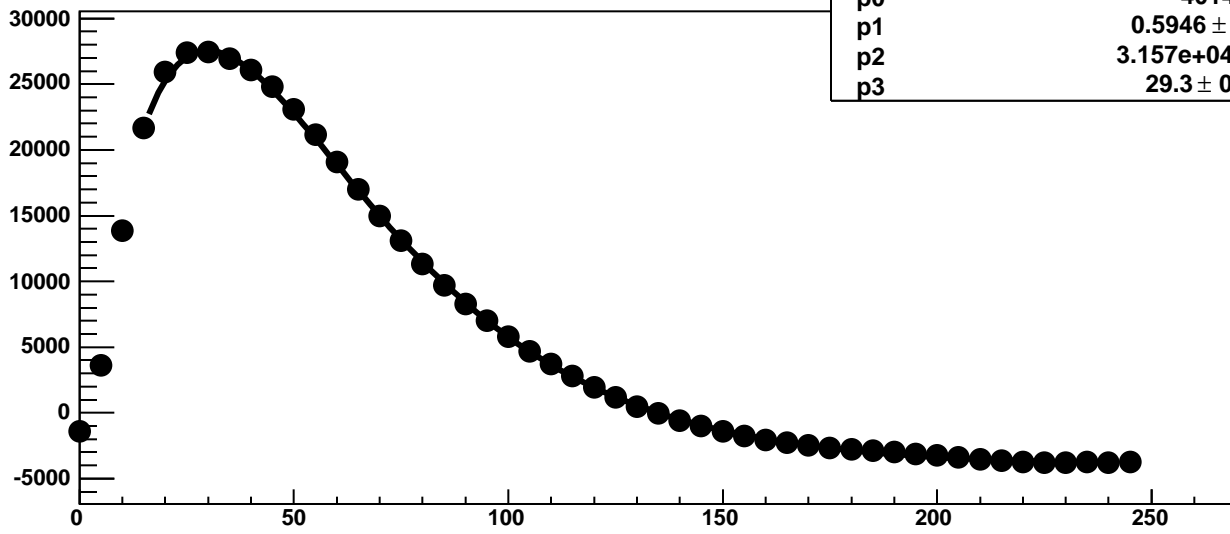
Chip 7, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

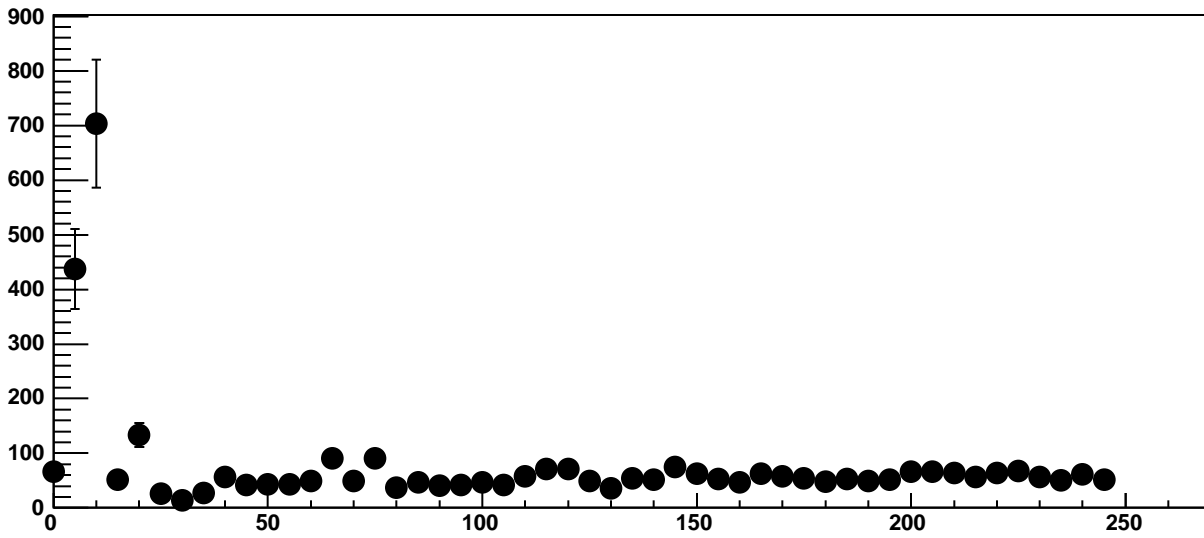


Chip 7, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

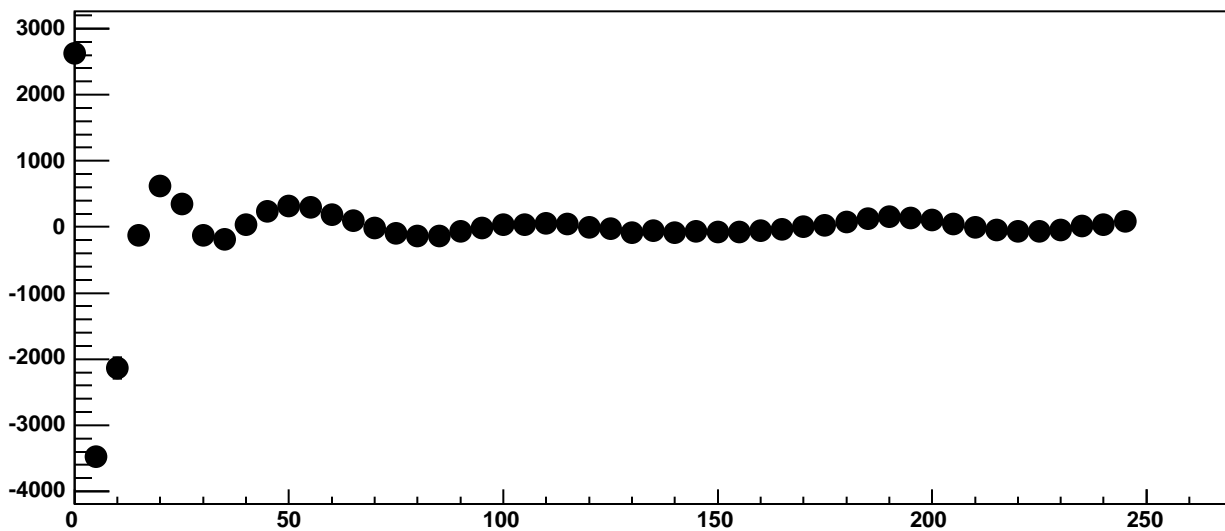


$\chi^2 / \text{ndf}$	1.06e+04 / 42
p0	-4014 ± 3.601
p1	0.5946 ± 0.01434
p2	3.157e+04 ± 4.042
p3	29.3 ± 0.008623

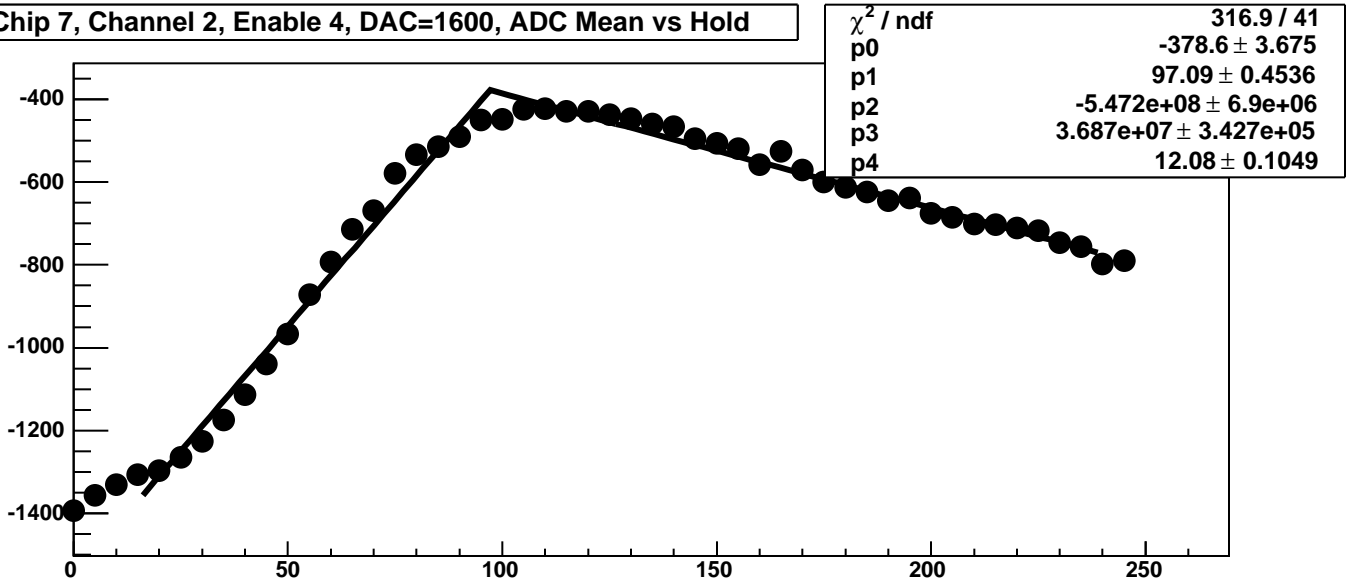
Chip 7, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



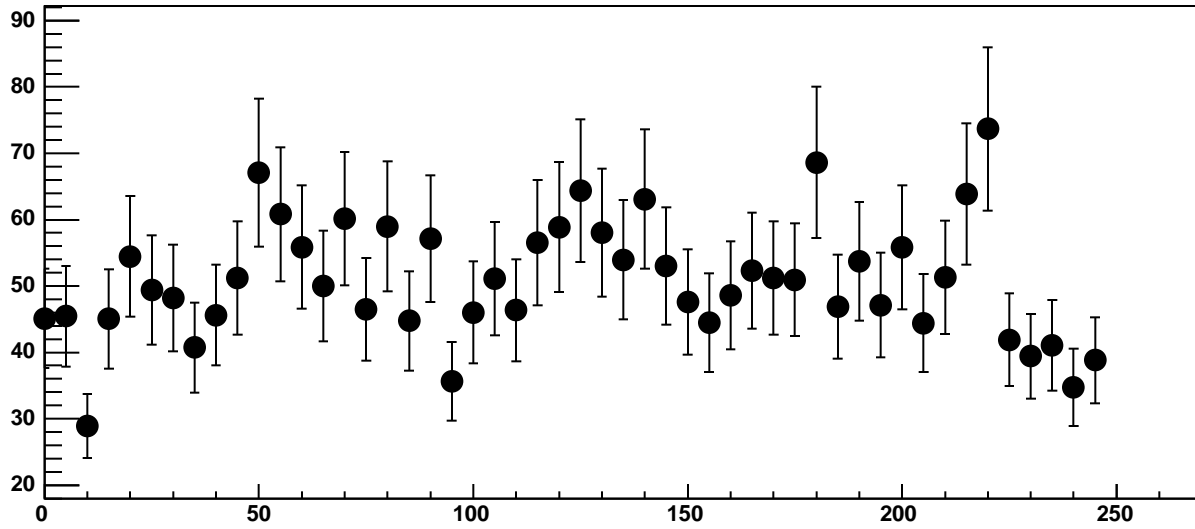
Chip 7, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold



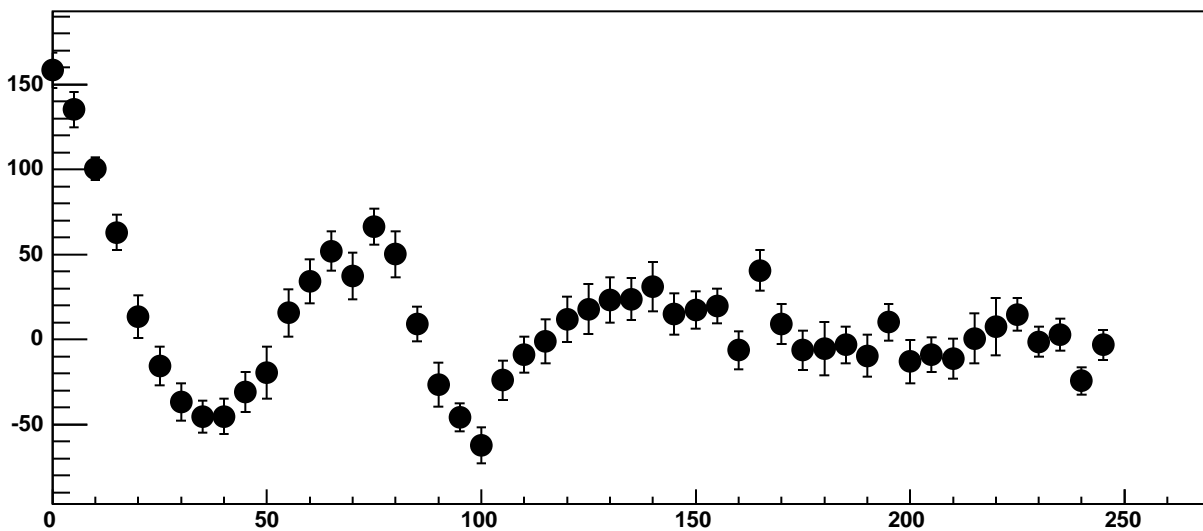
Chip 7, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold



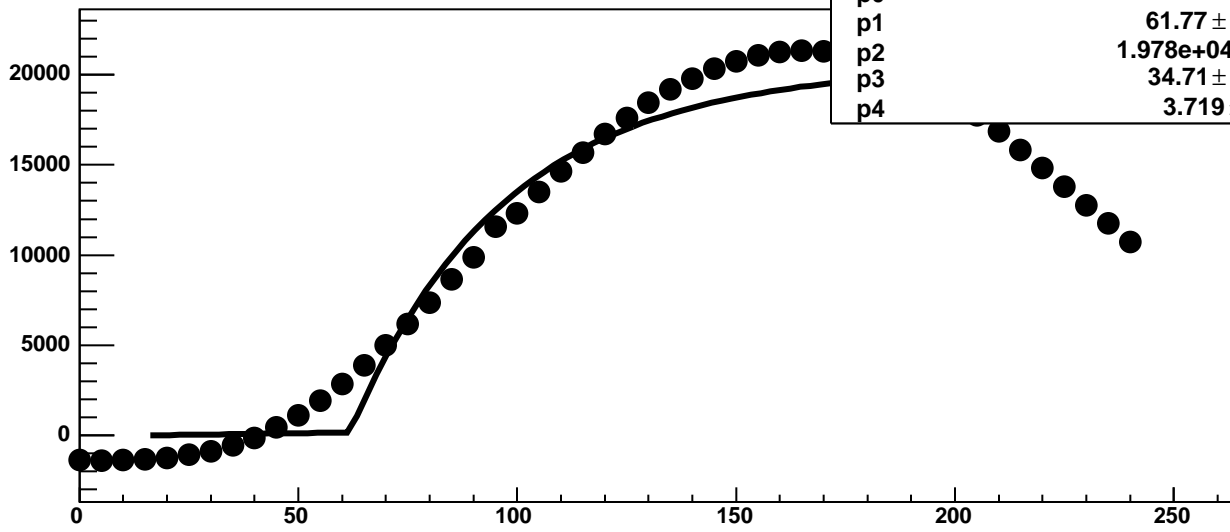
Chip 7, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



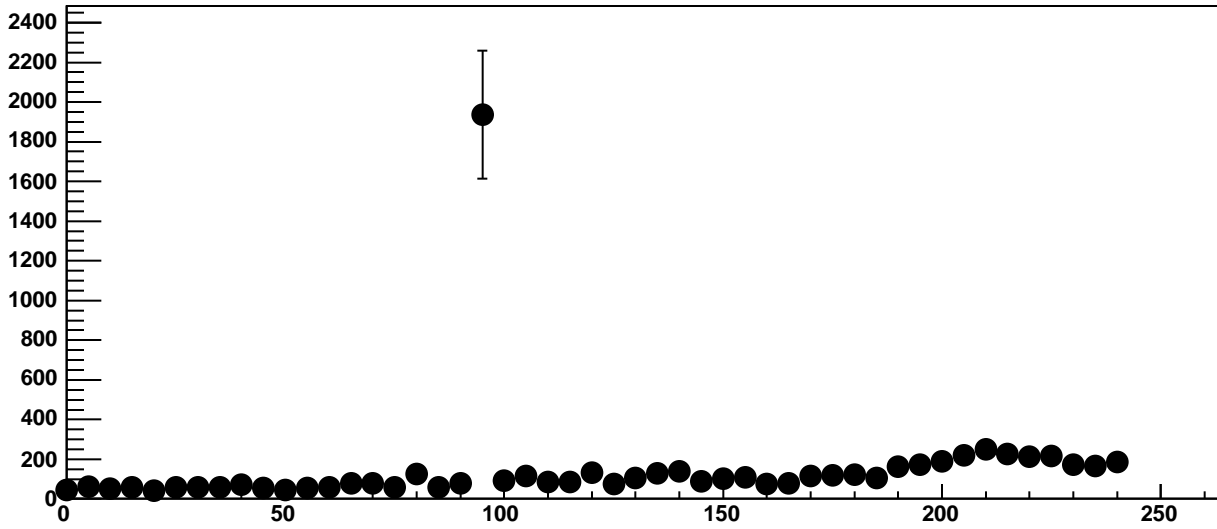
Chip 7, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold



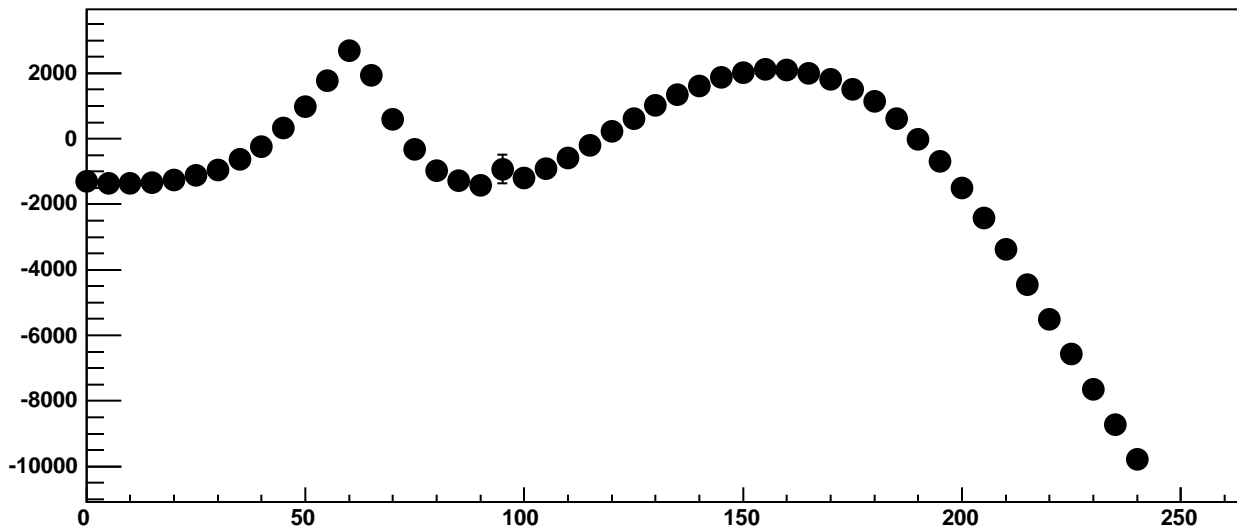
Chip 7, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold



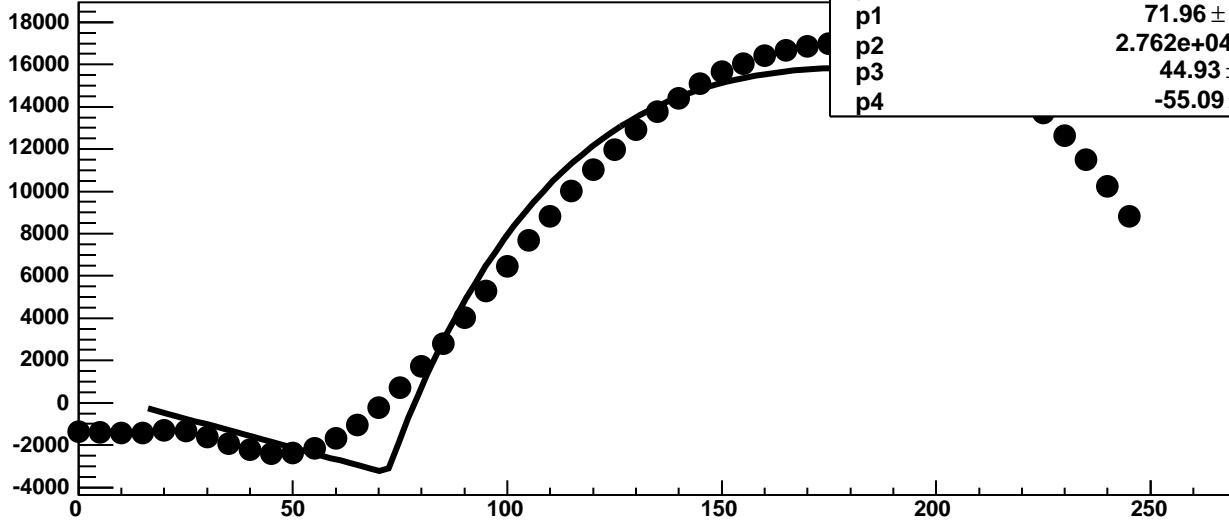
Chip 7, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

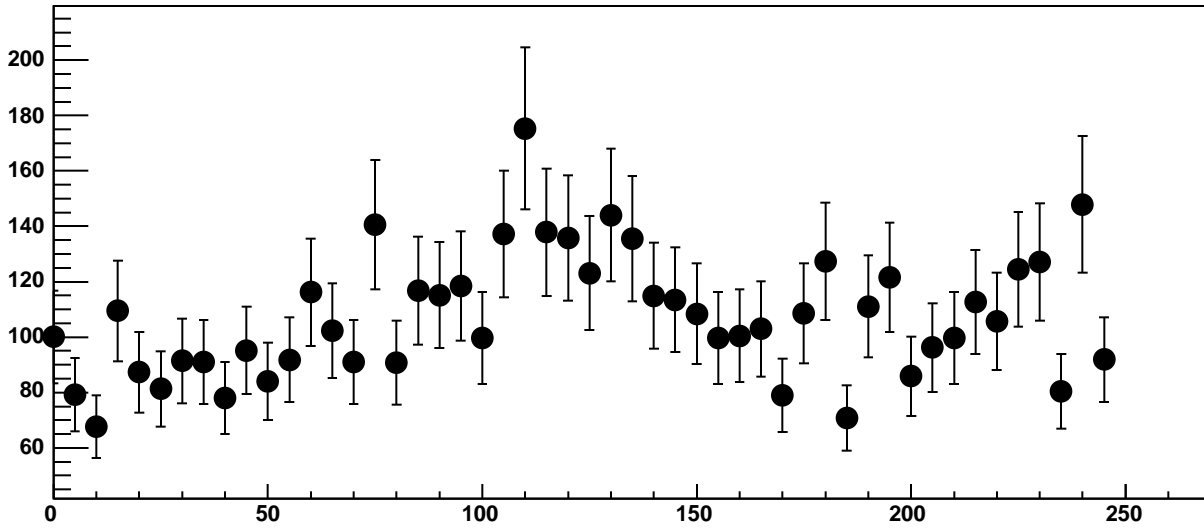


Chip 7, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

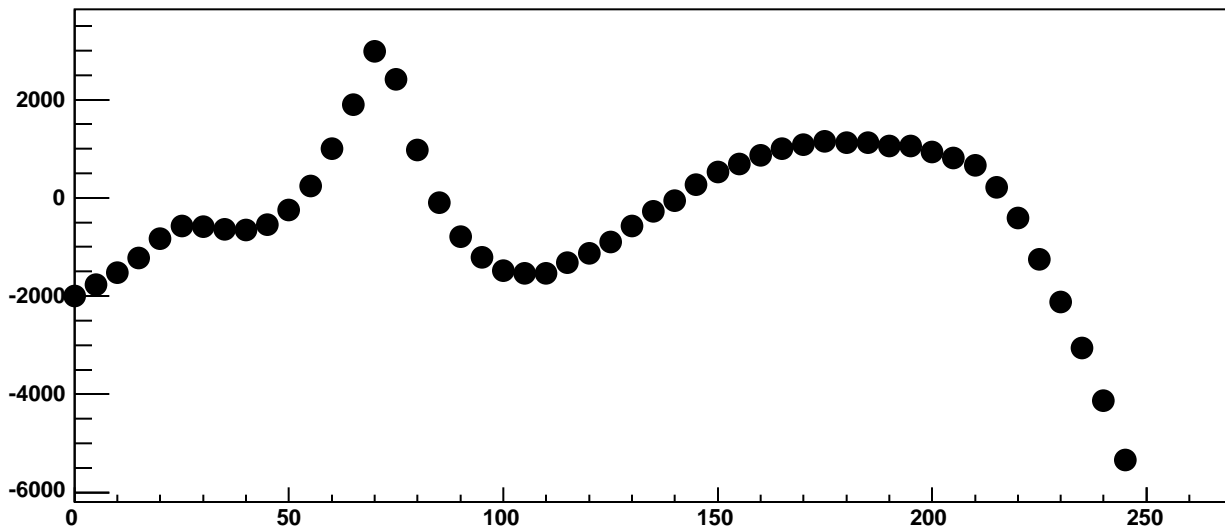


$\chi^2 / \text{ndf}$	1.349e+05 / 41
p0	-3333 ± 9.24
p1	71.96 ± 0.03576
p2	2.762e+04 ± 53.29
p3	44.93 ± 0.1013
p4	-55.09 ± 0.2651

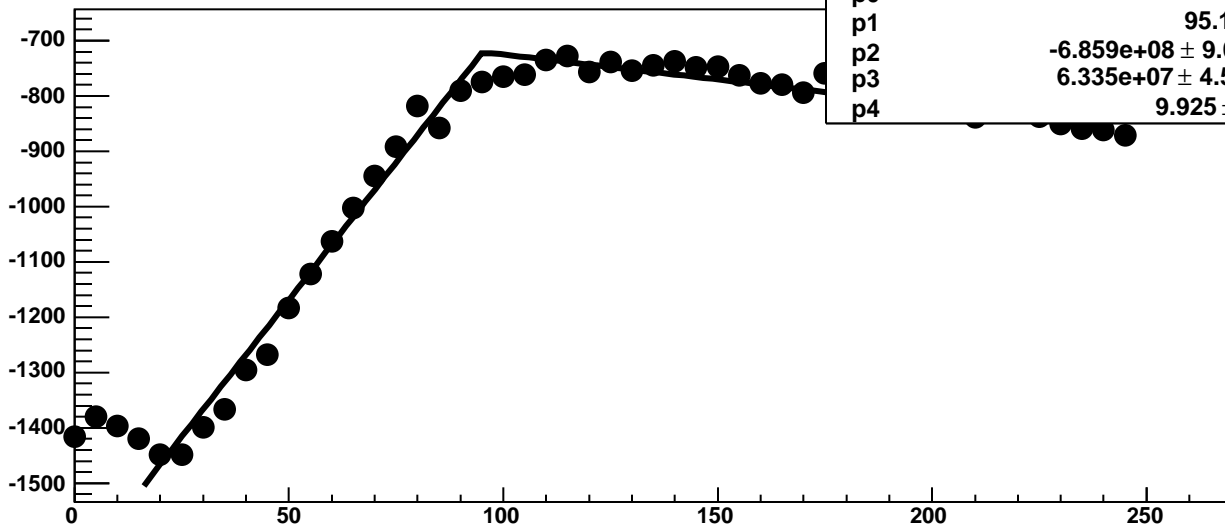
Chip 7, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

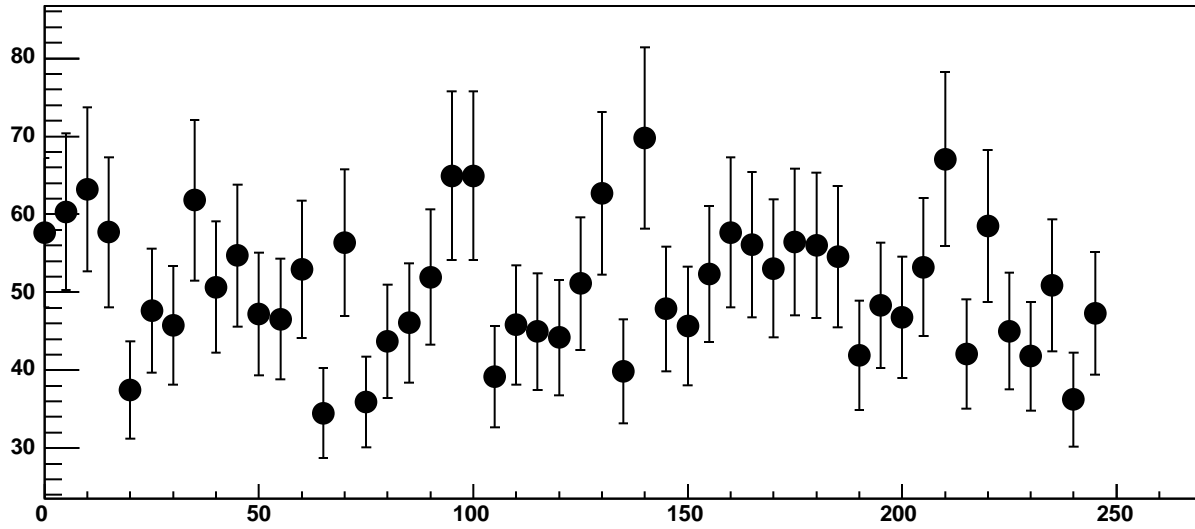


Chip 7, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

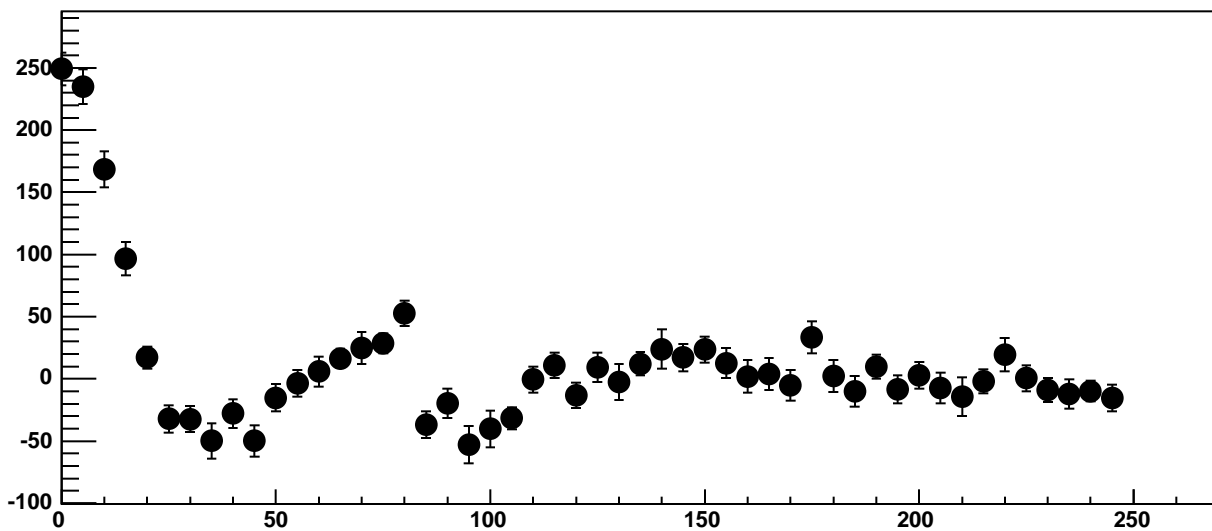


$\chi^2 / \text{ndf}$	239.1 / 41
p0	$-720.7 \pm 3.84$
p1	$95.1 \pm 0.607$
p2	$-6.859\text{e}+08 \pm 9.042\text{e}+06$
p3	$6.335\text{e}+07 \pm 4.598\text{e}+05$
p4	$9.925 \pm 0.1098$

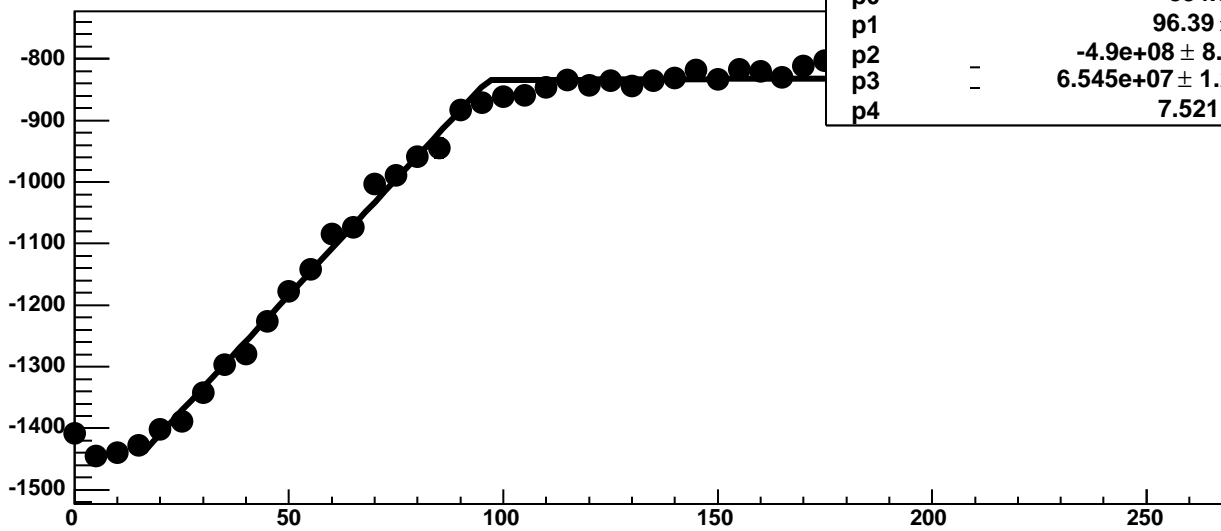
Chip 7, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold

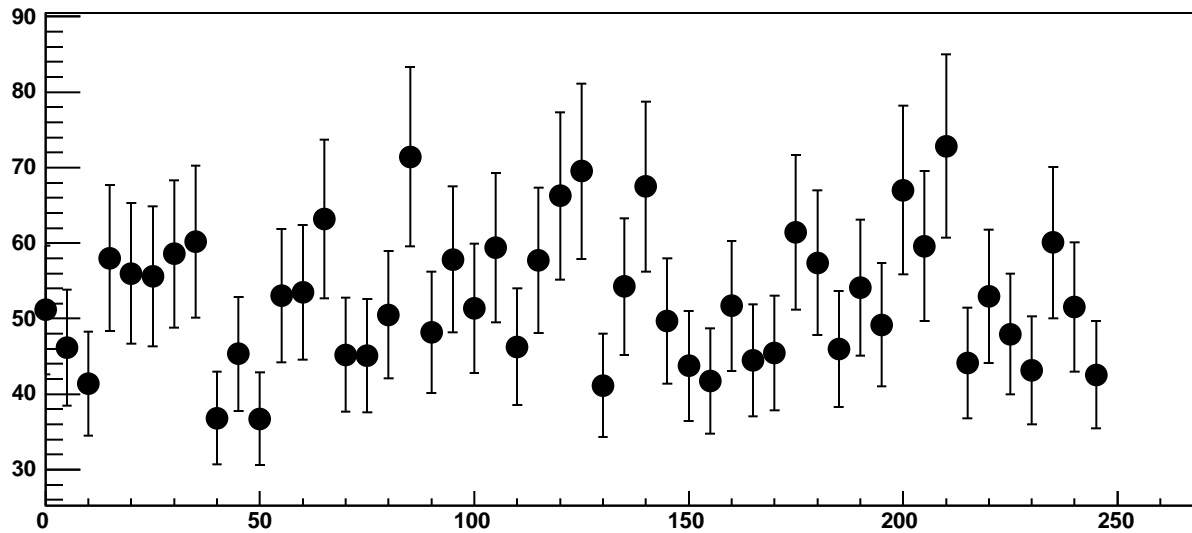


Chip 7, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

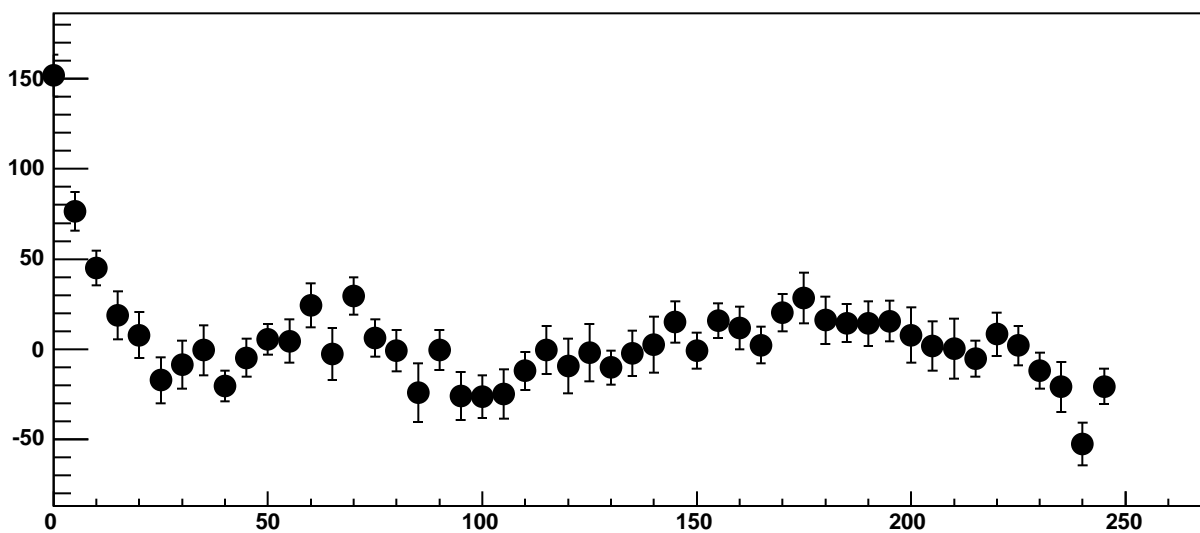


$\chi^2 / \text{ndf}$	85.39 / 41
p0	$-834.6 \pm 4.548$
p1	$96.39 \pm 0.9914$
p2	$-4.9\text{e}+08 \pm 8.831\text{e}+06$
p3	$6.545\text{e}+07 \pm 1.296\text{e}+05$
p4	$7.521 \pm 0.1239$

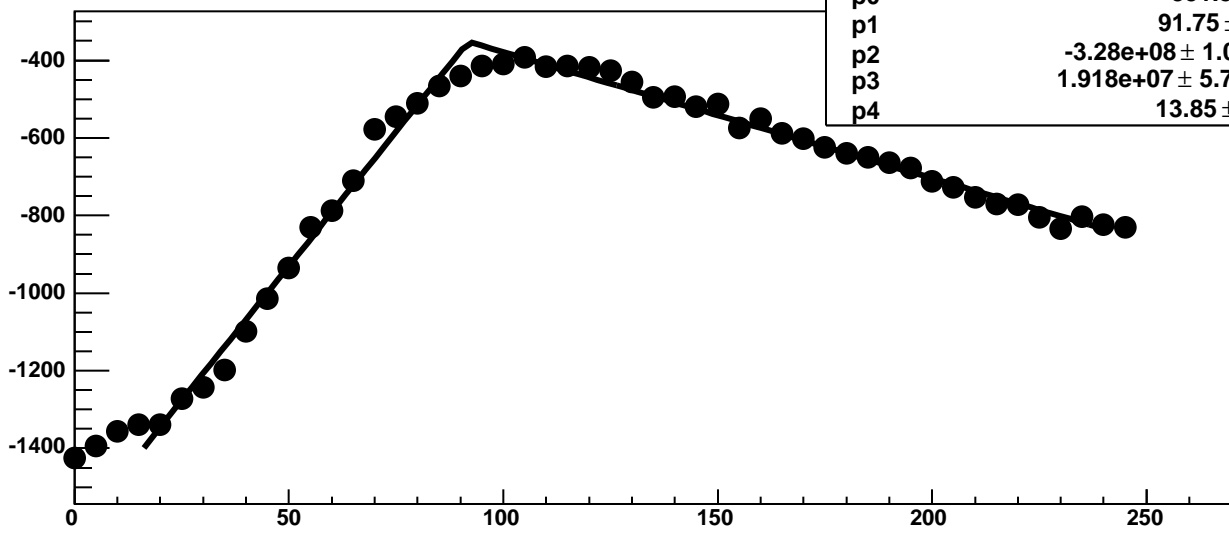
Chip 7, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

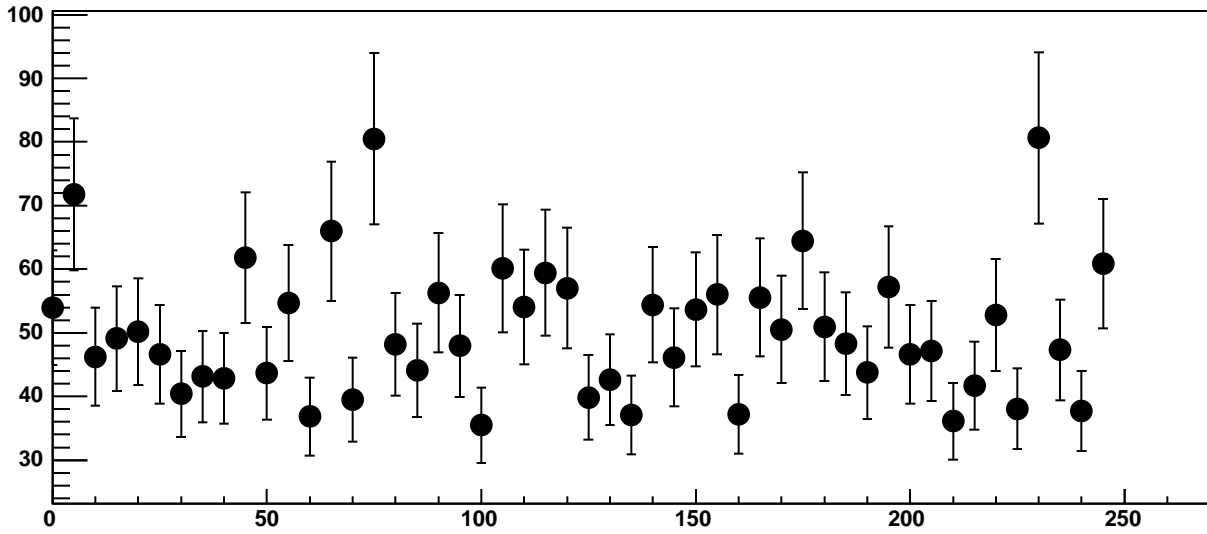


Chip 7, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

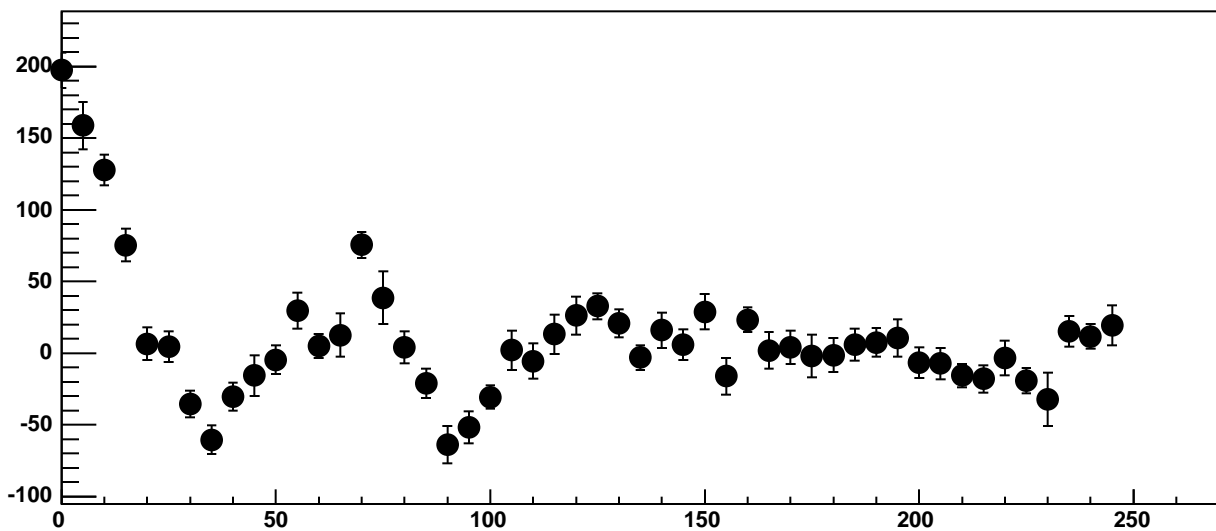


$\chi^2 / \text{ndf}$	314.4 / 41
p0	$-351.8 \pm 3.351$
p1	$91.75 \pm 0.4011$
p2	$-3.28\text{e}+08 \pm 1.006\text{e}+07$
p3	$1.918\text{e}+07 \pm 5.726\text{e}+05$
p4	$13.85 \pm 0.1212$

Chip 7, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

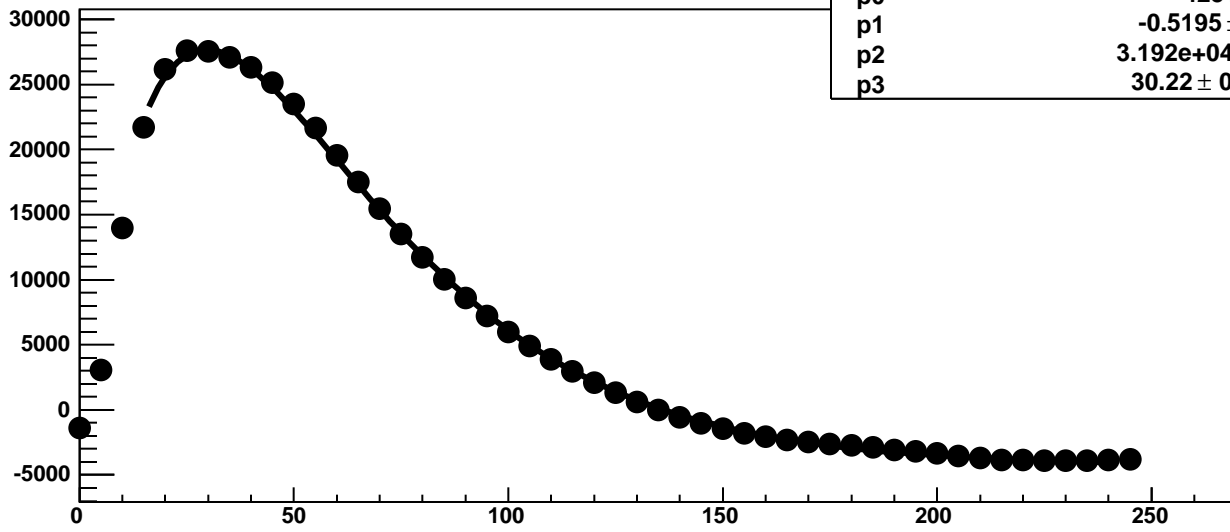


Chip 7, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



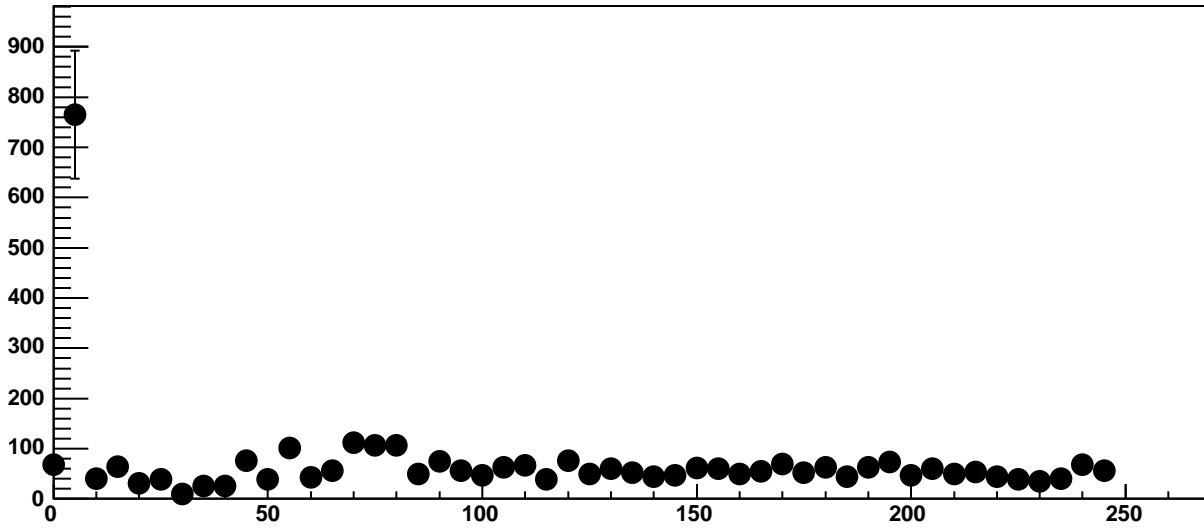


Chip 7, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold

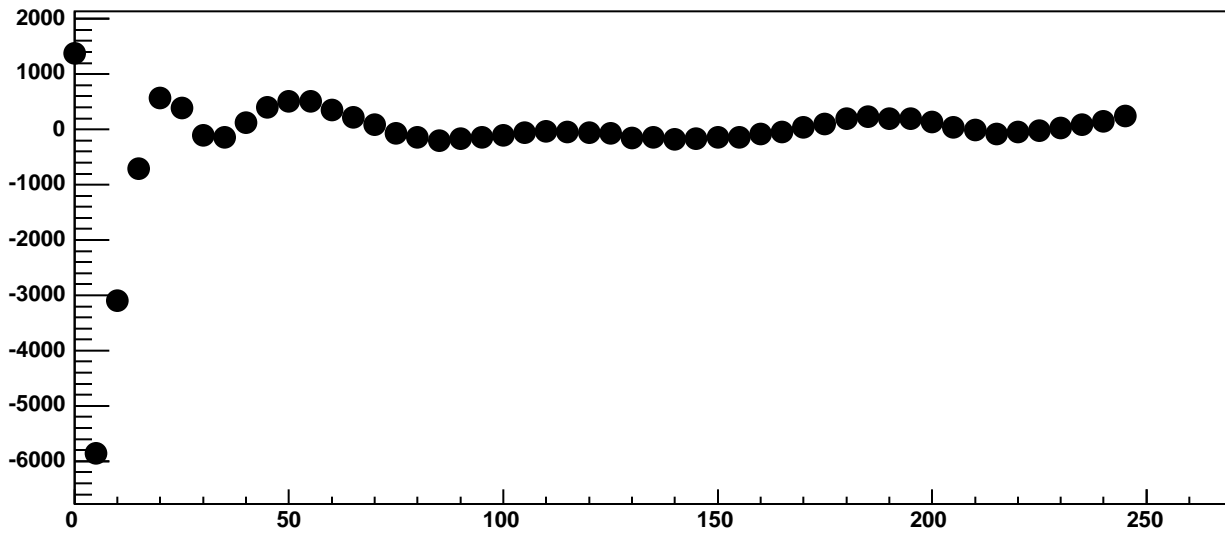


$\chi^2 / \text{ndf}$	2.271e+04 / 42
p0	-4251 ± 3.249
p1	-0.5195 ± 0.0142
p2	3.192e+04 ± 3.567
p3	30.22 ± 0.009086

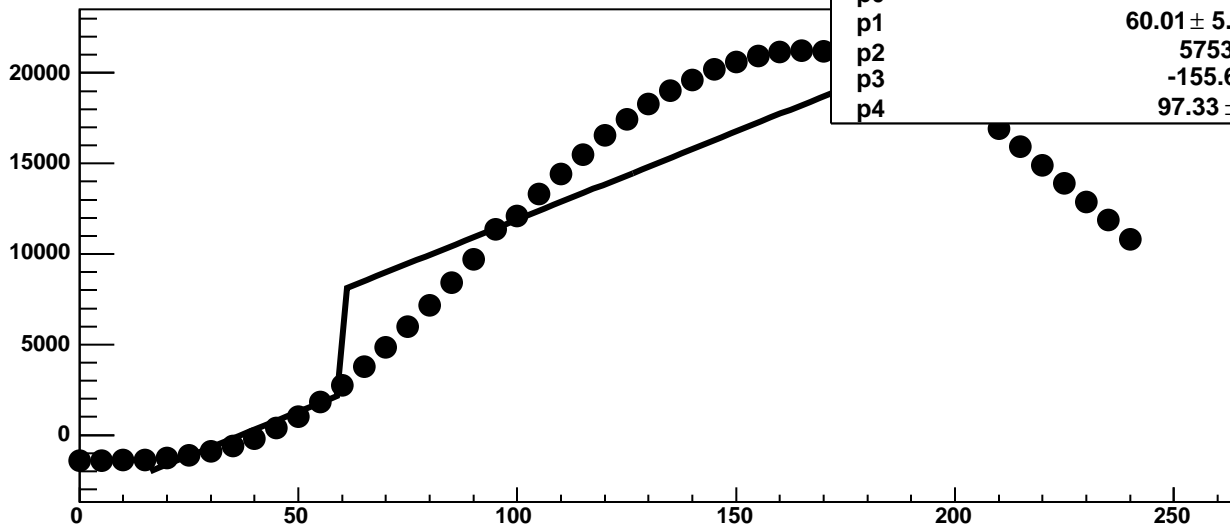
Chip 7, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



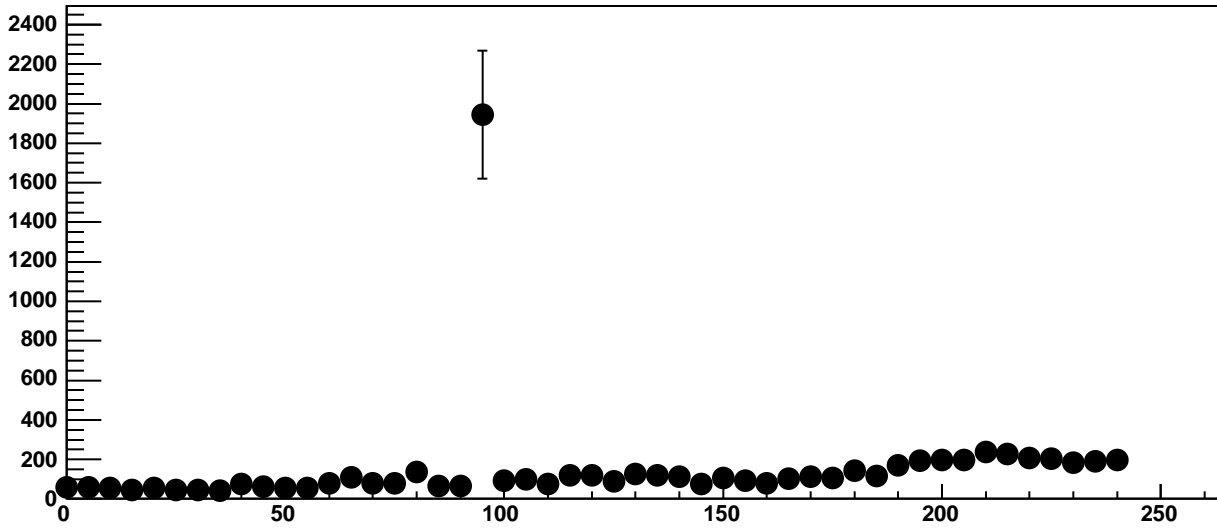
Chip 7, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold



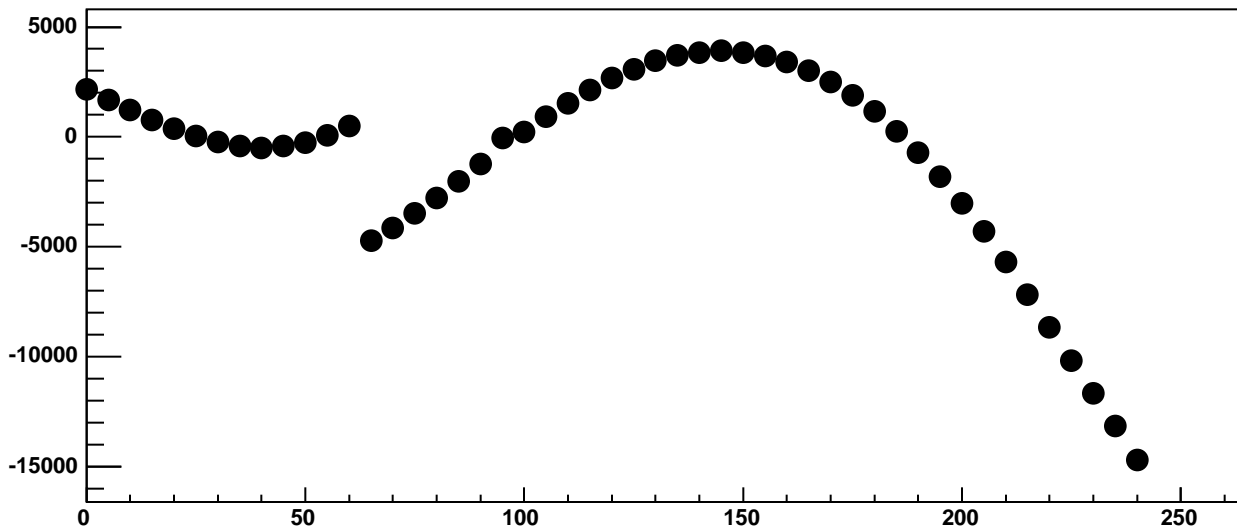
Chip 7, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold



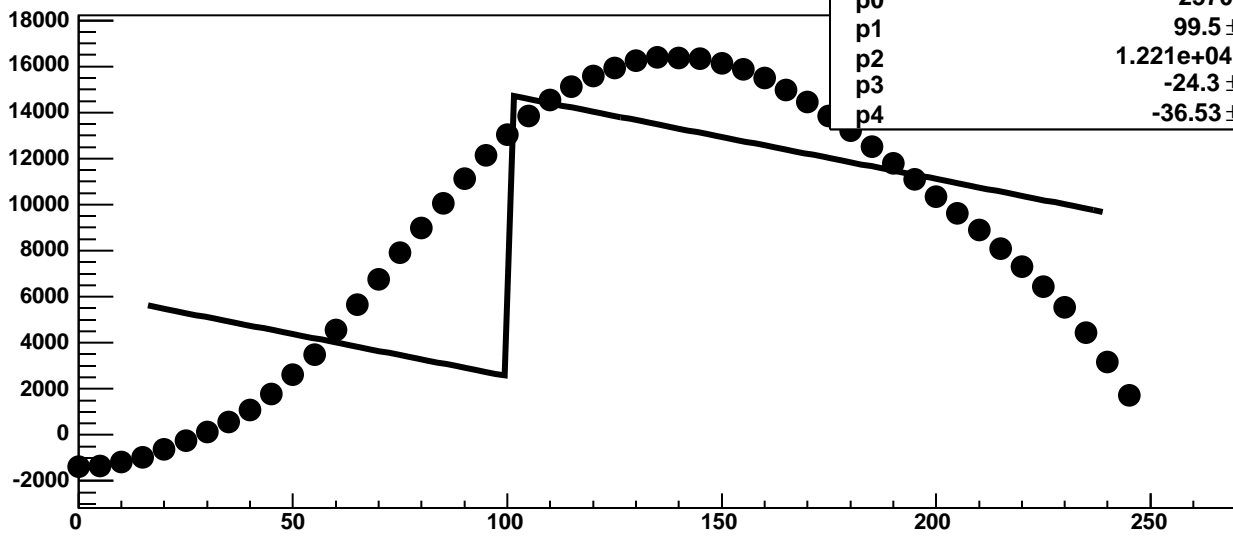
Chip 7, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



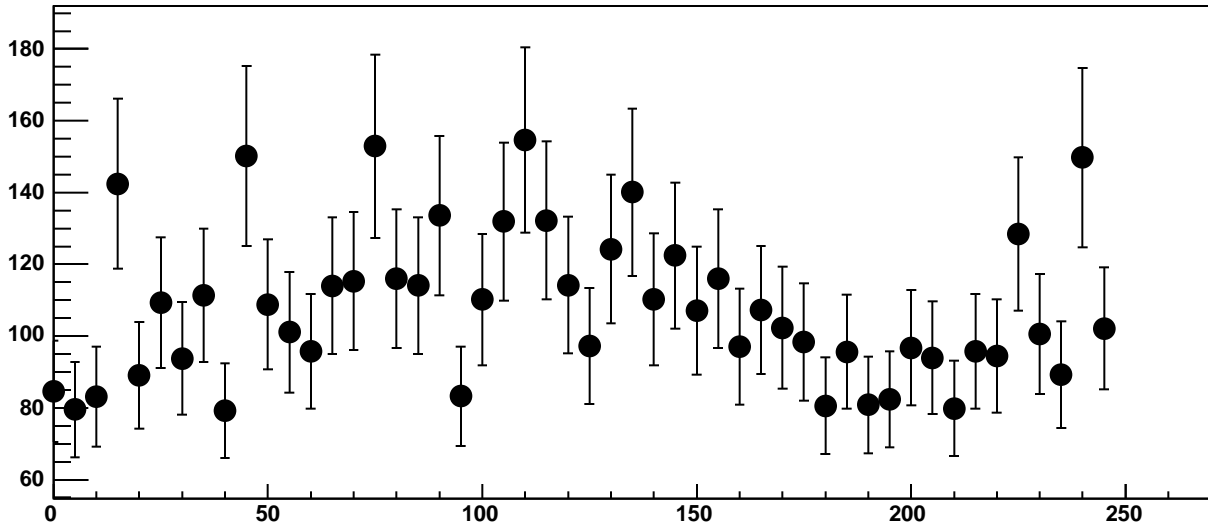
Chip 7, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold



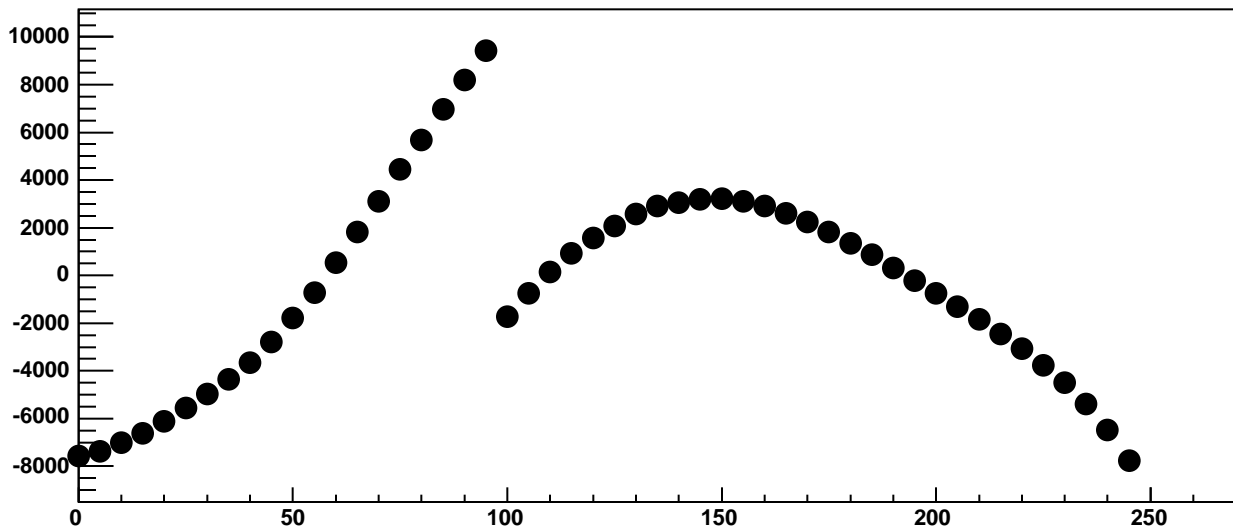
Chip 7, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold



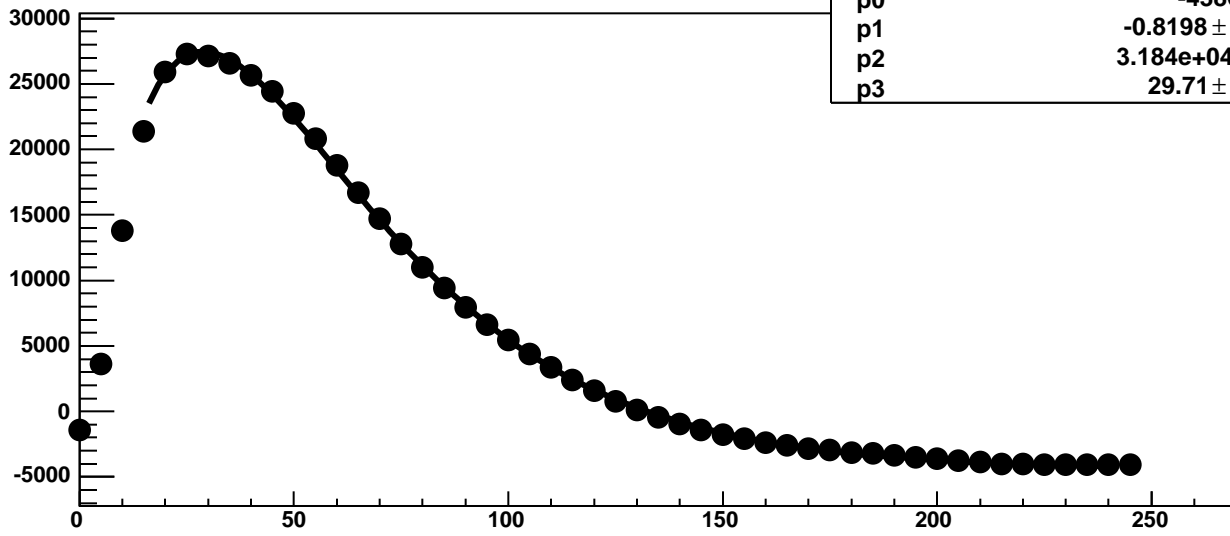
Chip 7, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

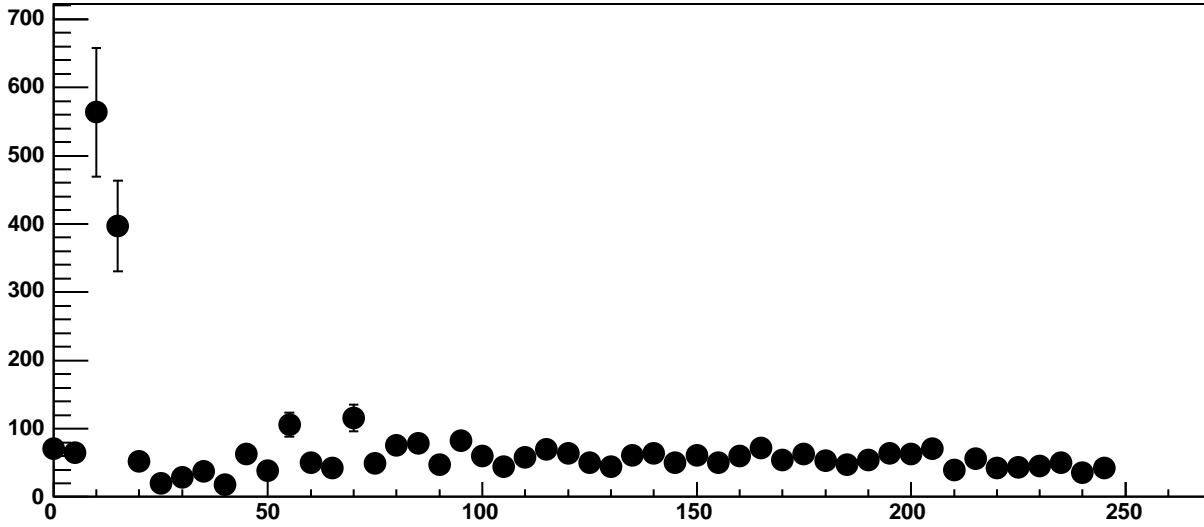


Chip 7, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold

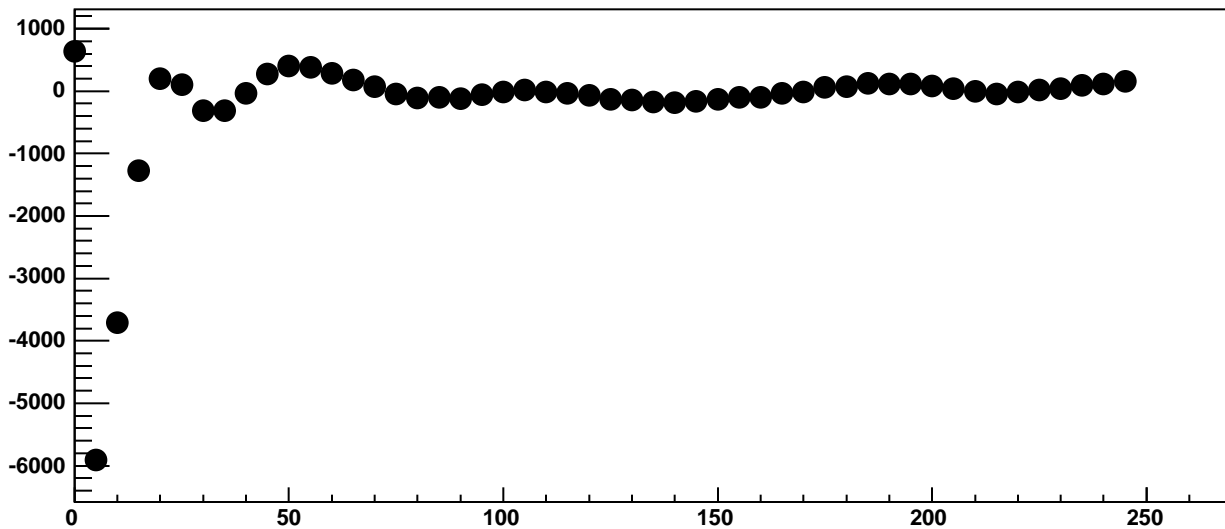


$\chi^2 / \text{ndf}$	1.017e+04 / 42
p0	-4386 ± 3.34
p1	-0.8198 ± 0.01968
p2	3.184e+04 ± 4.028
p3	29.71 ± 0.01086

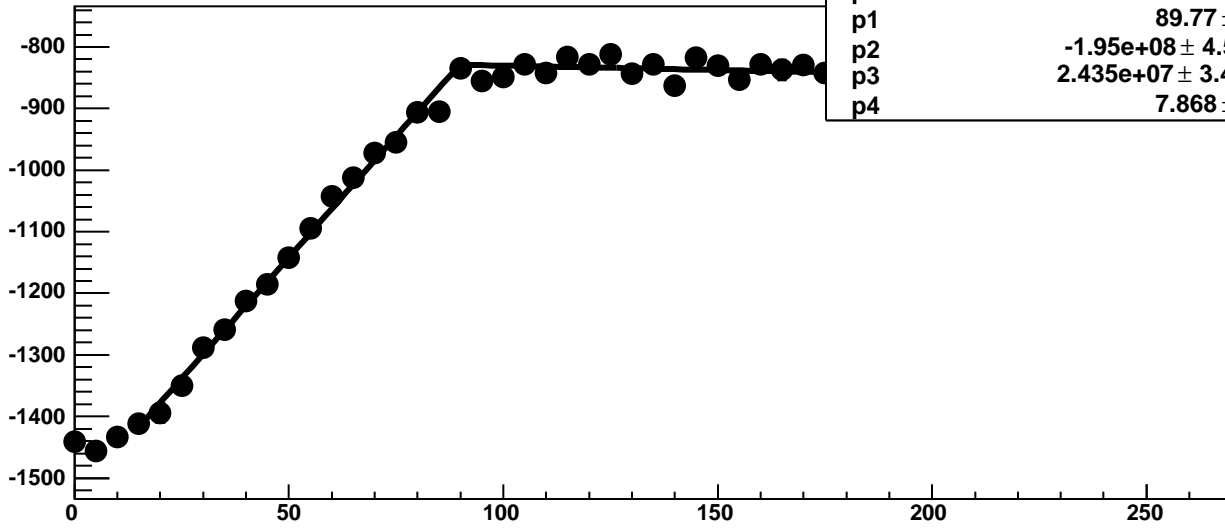
Chip 7, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold

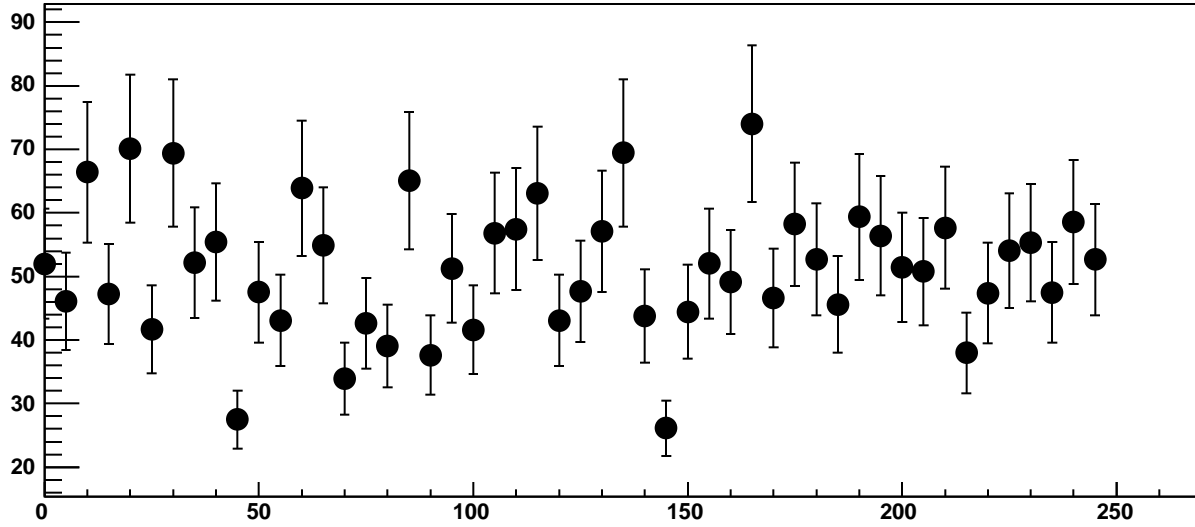


Chip 7, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

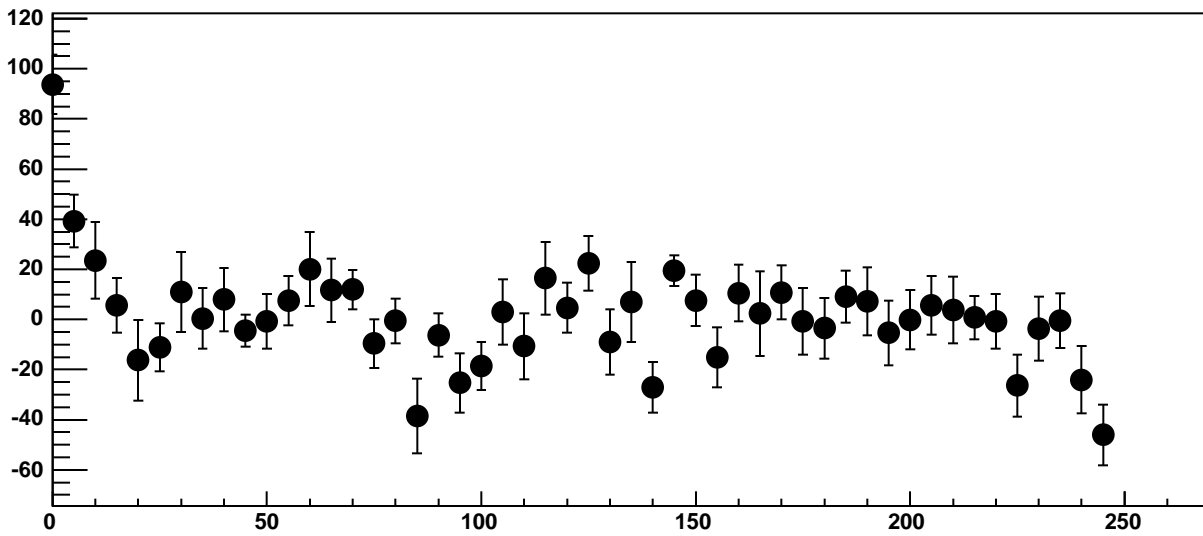


$\chi^2 / \text{ndf}$	64.68 / 41
p0	$-828.8 \pm 3.733$
p1	$89.77 \pm 0.8549$
p2	$-1.95\text{e}+08 \pm 4.551\text{e}+06$
p3	$2.435\text{e}+07 \pm 3.481\text{e}+05$
p4	$7.868 \pm 0.1329$

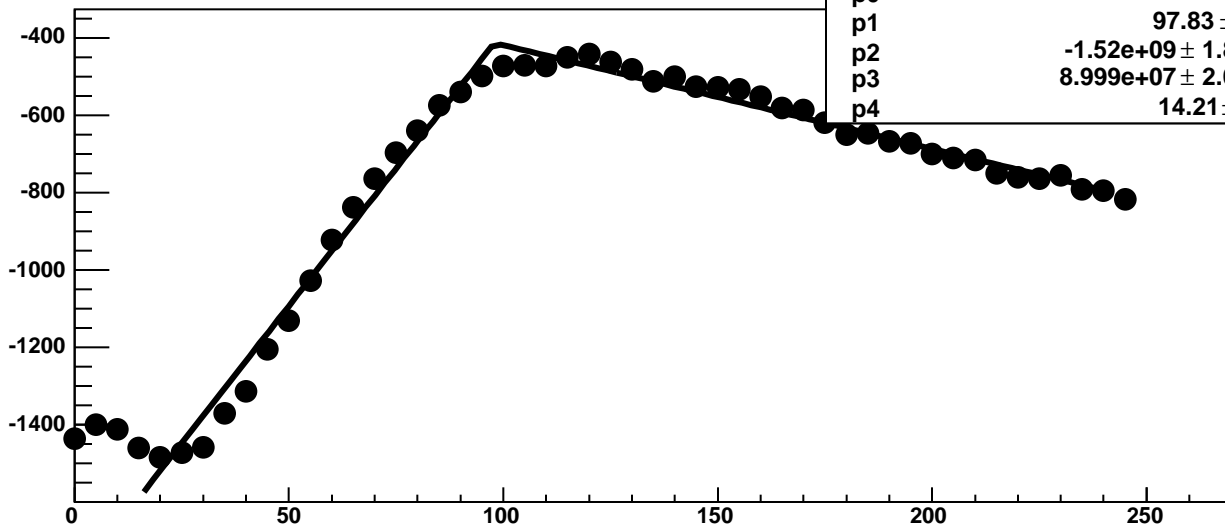
Chip 7, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

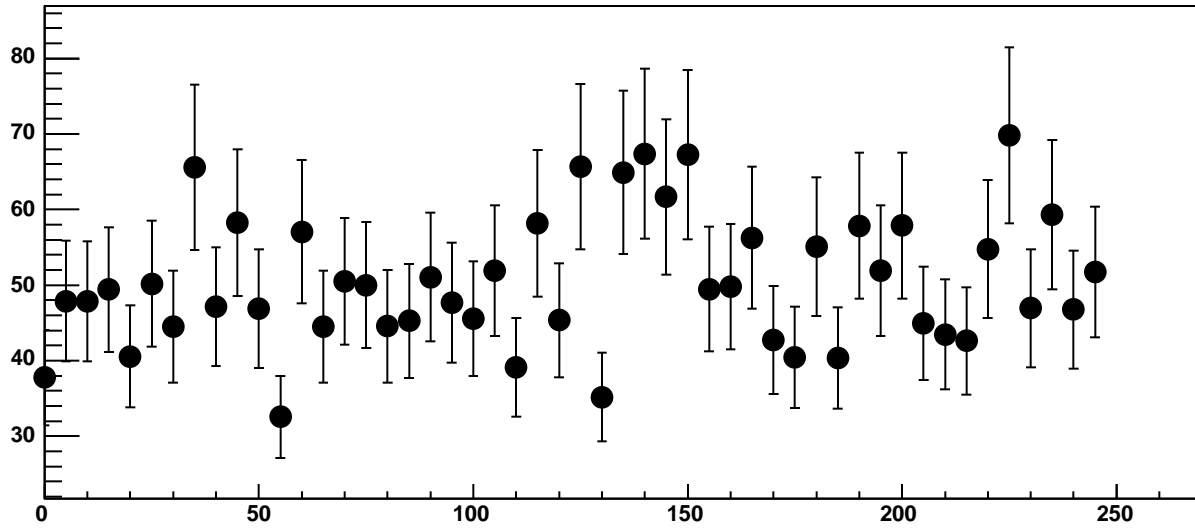


Chip 7, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

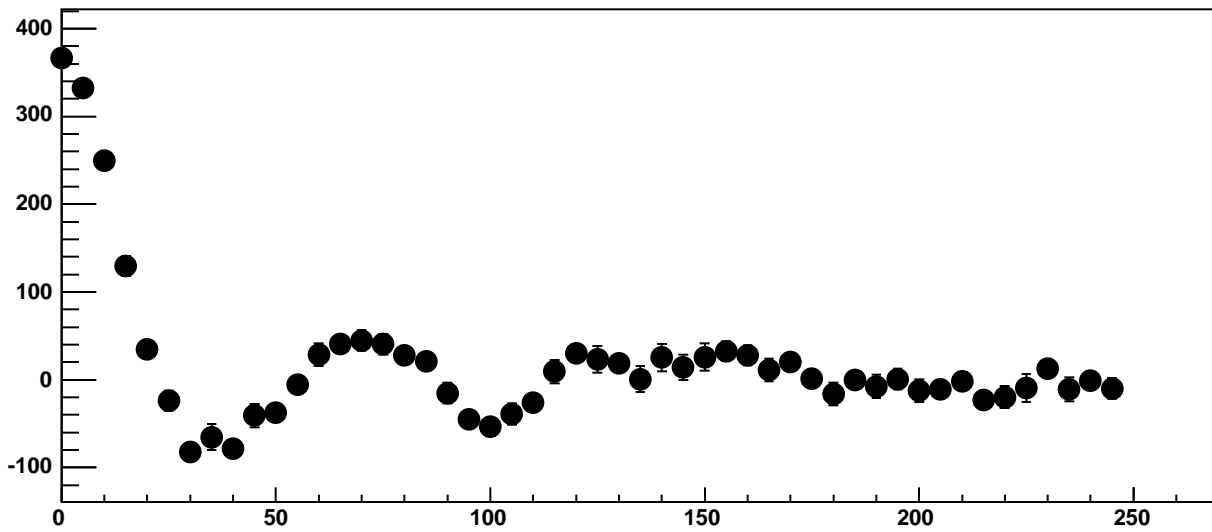


$\chi^2 / \text{ndf}$	488.1 / 41
p0	-412.7 ± 5.493
p1	97.83 ± 0.2525
p2	-1.52e+09 ± 1.835e+07
p3	8.999e+07 ± 2.093e+06
p4	14.21 ± 0.1194

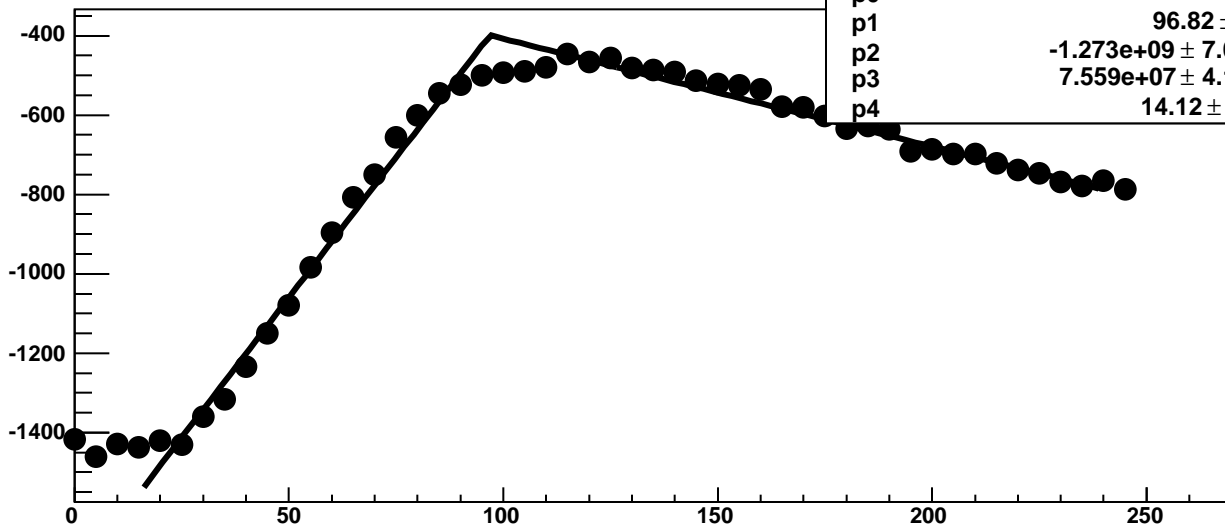
Chip 7, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

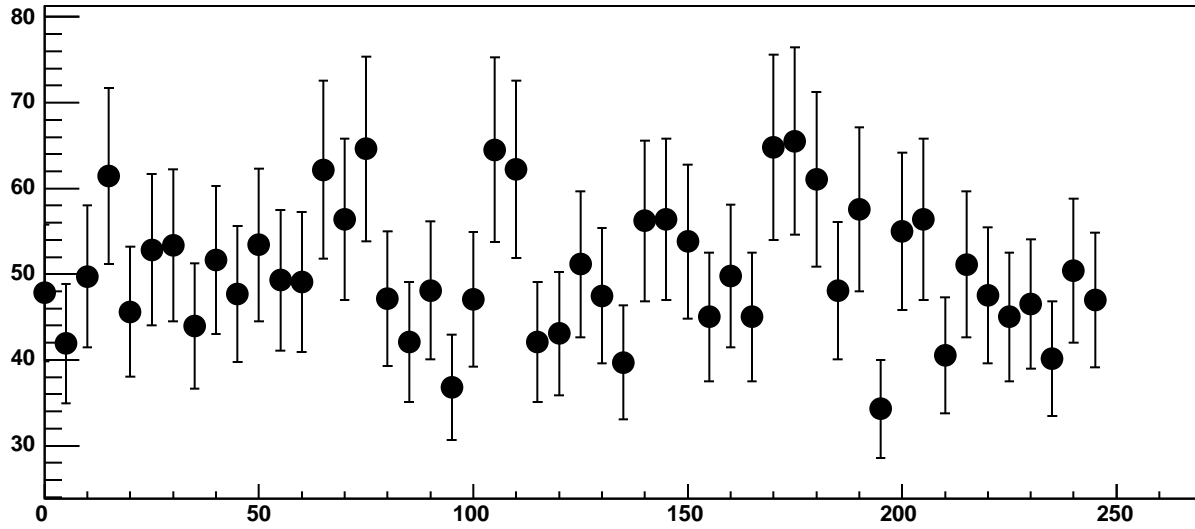


Chip 7, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold

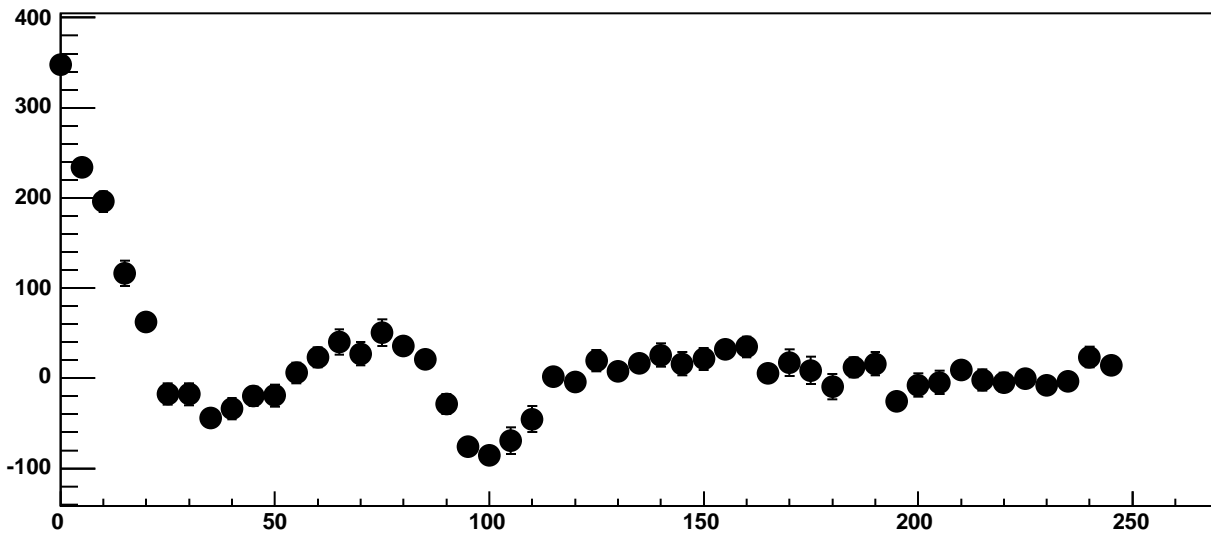


$\chi^2 / \text{ndf}$	424.3 / 41
p0	$-398.6 \pm 2.506$
p1	$96.82 \pm 0.3315$
p2	$-1.273\text{e}+09 \pm 7.046\text{e}+08$
p3	$7.559\text{e}+07 \pm 4.184\text{e}+07$
p4	$14.12 \pm 0.04205$

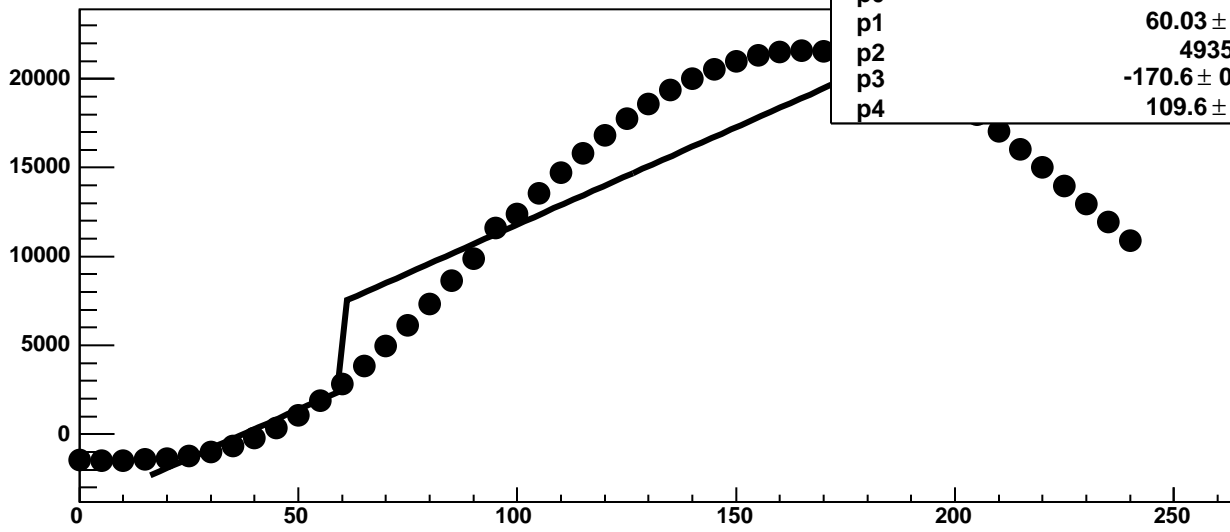
Chip 7, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



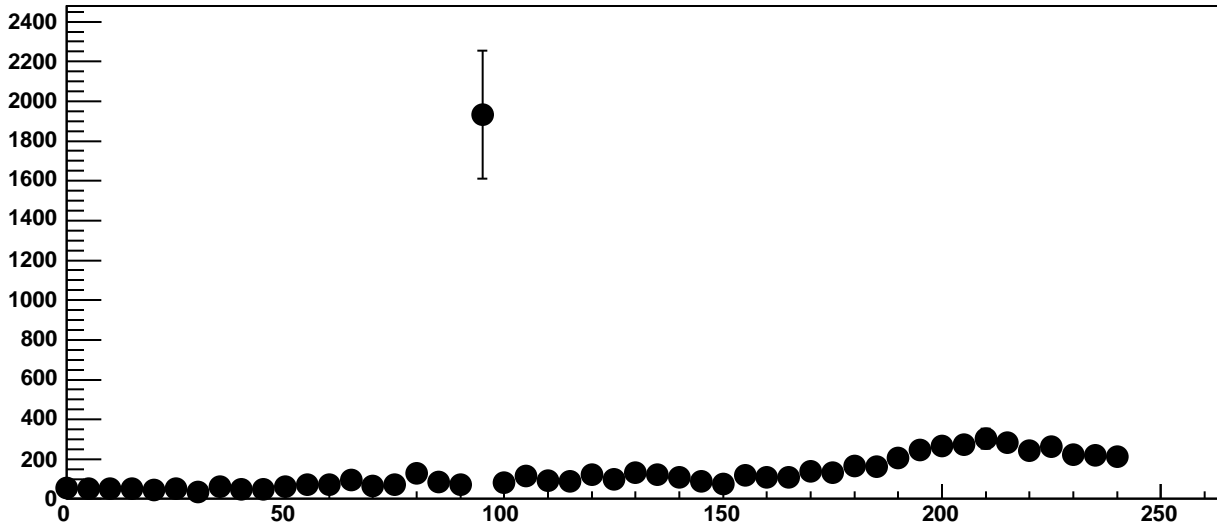
Chip 7, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold



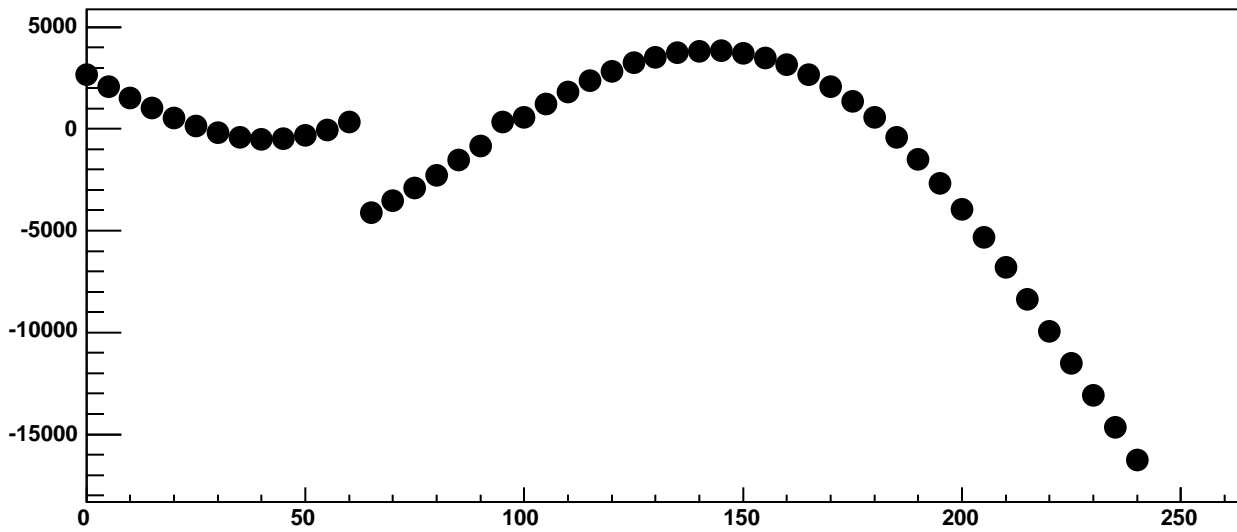
Chip 7, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 7, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

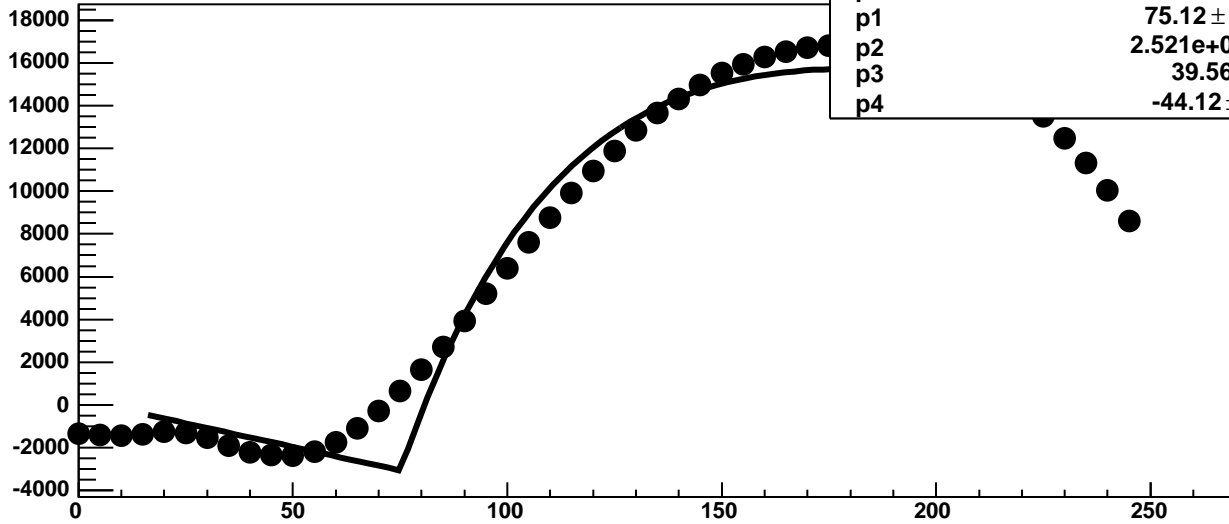


Chip 7, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



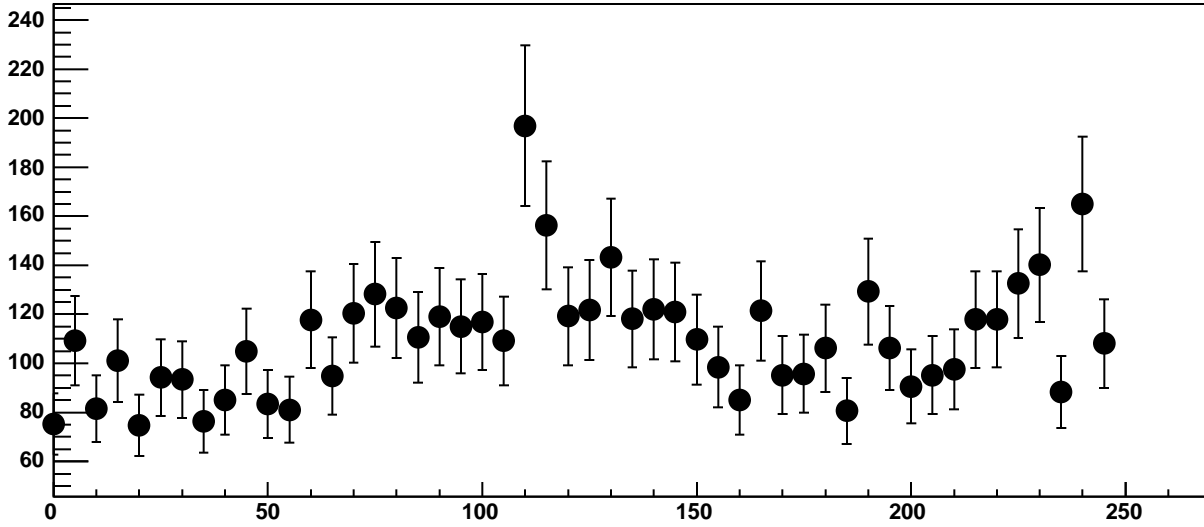


Chip 7, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

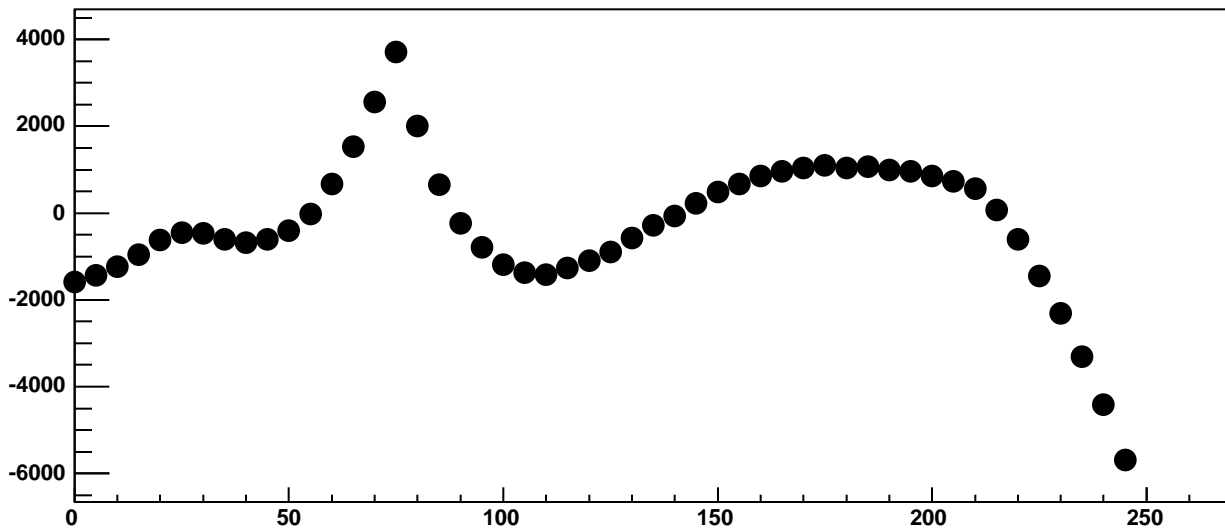


$\chi^2 / \text{ndf}$	1.233e+05 / 41
p0	-3073 ± 9.498
p1	75.12 ± 0.04015
p2	2.521e+04 ± 48
p3	39.56 ± 0.096
p4	-44.12 ± 0.2502

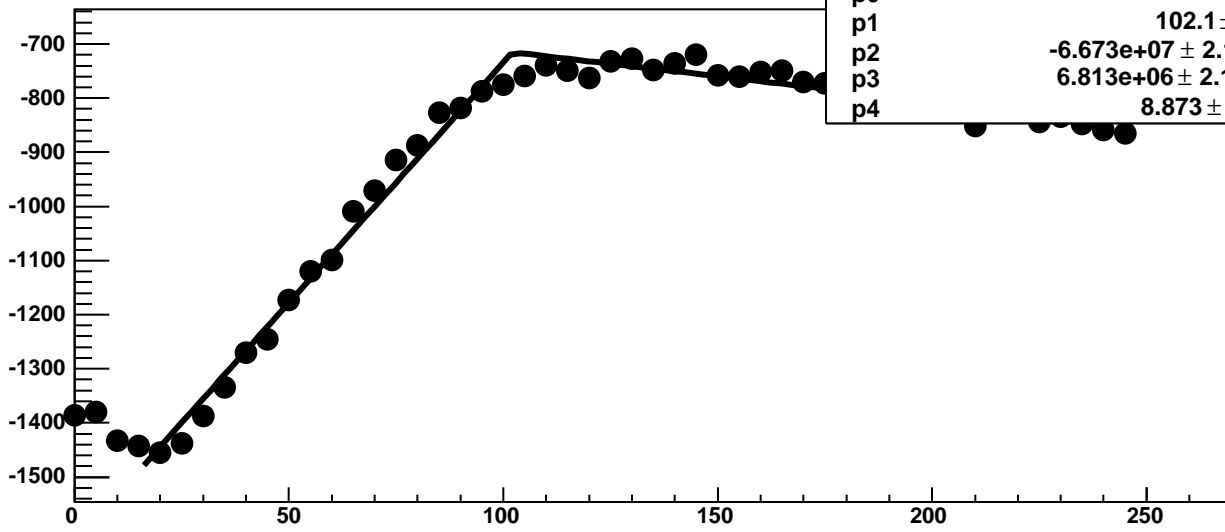
Chip 7, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

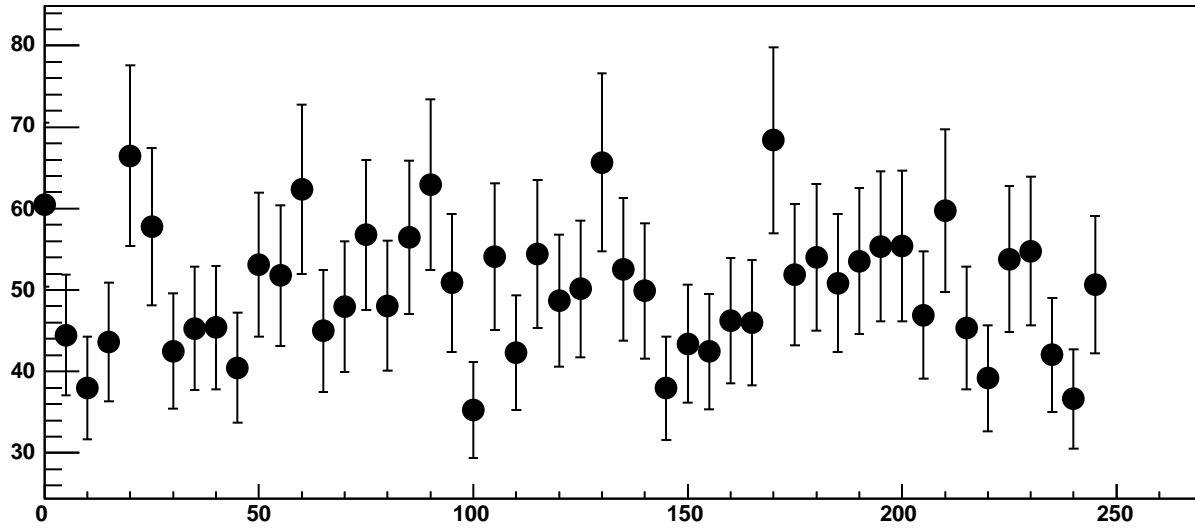


Chip 7, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

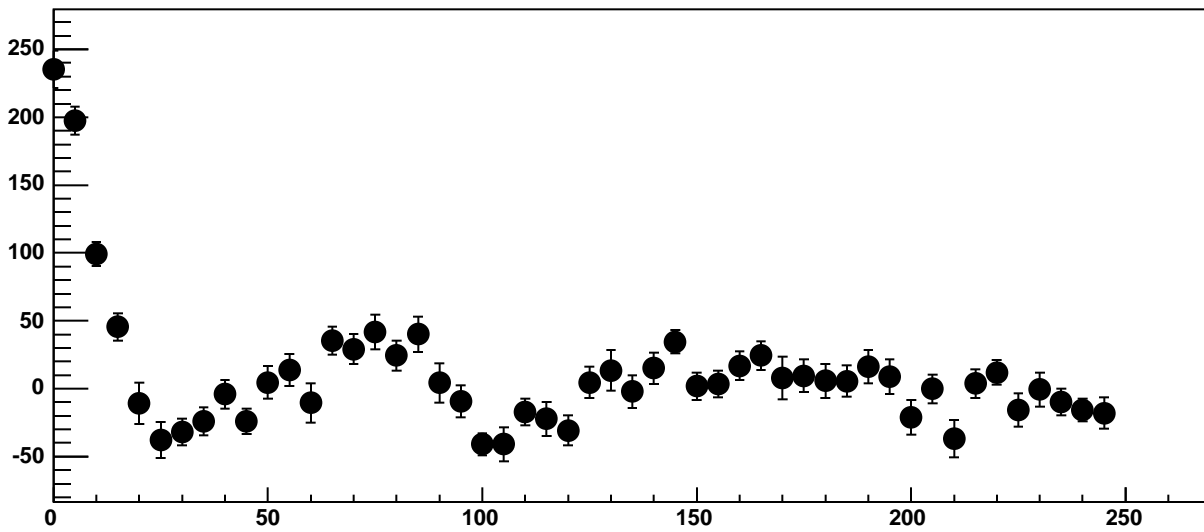


$\chi^2 / \text{ndf}$	197.9 / 41
p0	$-715.3 \pm 3.778$
p1	$102.1 \pm 0.6536$
p2	$-6.673\text{e}+07 \pm 2.121\text{e}+06$
p3	$6.813\text{e}+06 \pm 2.187\text{e}+05$
p4	$8.873 \pm 0.09353$

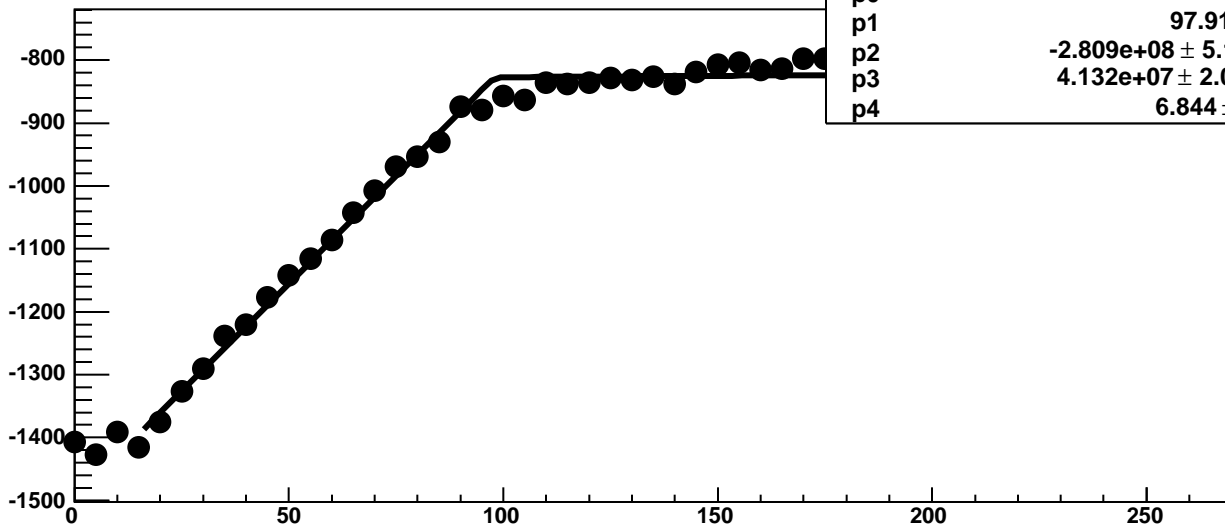
Chip 7, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold

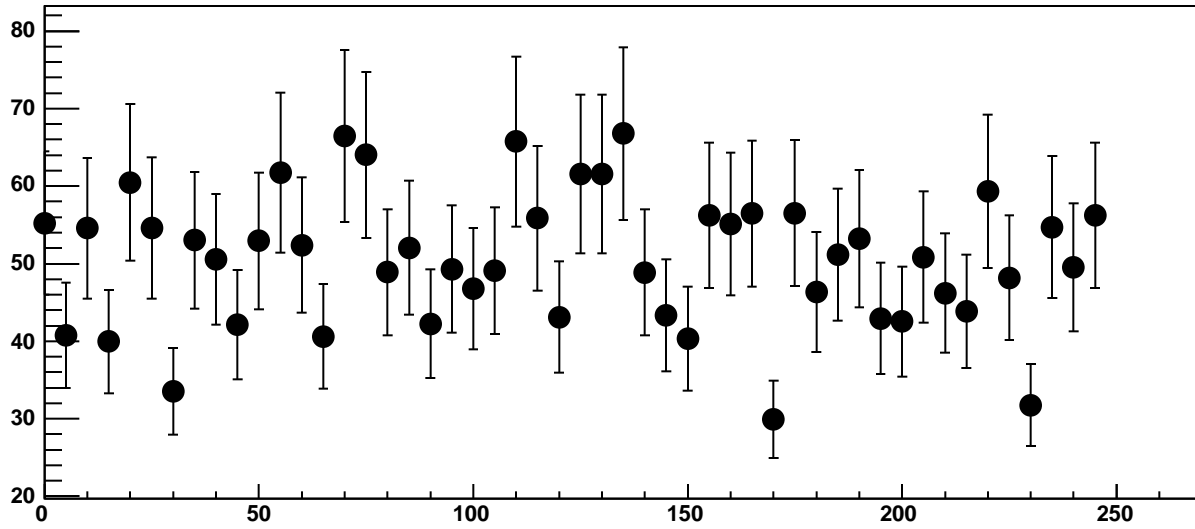


Chip 7, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

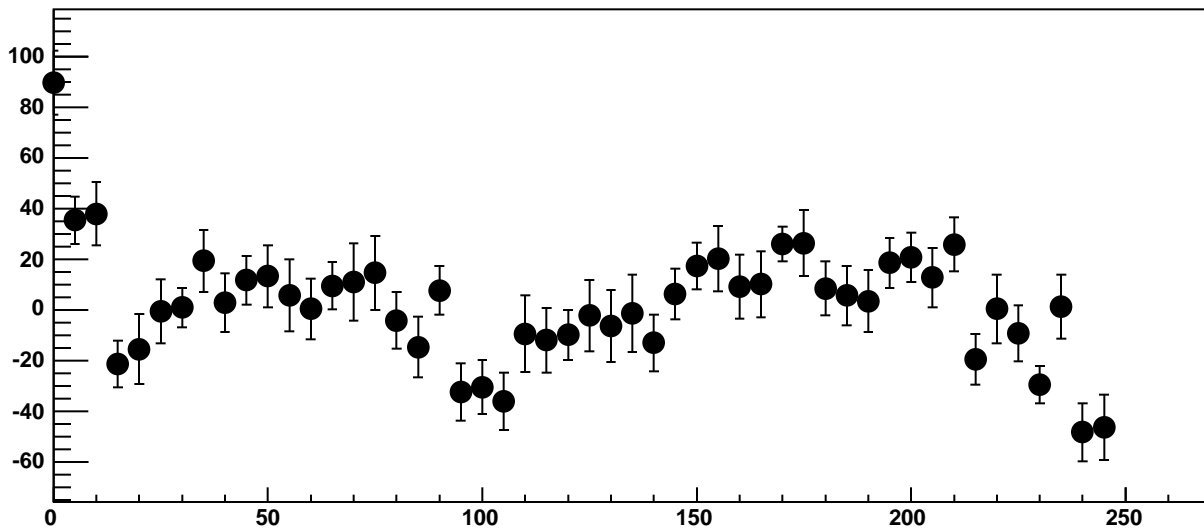


$\chi^2 / \text{ndf}$	128.4 / 41
p0	$-827.2 \pm 4.322$
p1	$97.91 \pm 1.024$
p2	$-2.809\text{e}+08 \pm 5.167\text{e}+06$
p3	$4.132\text{e}+07 \pm 2.088\text{e}+05$
p4	$6.844 \pm 0.1068$

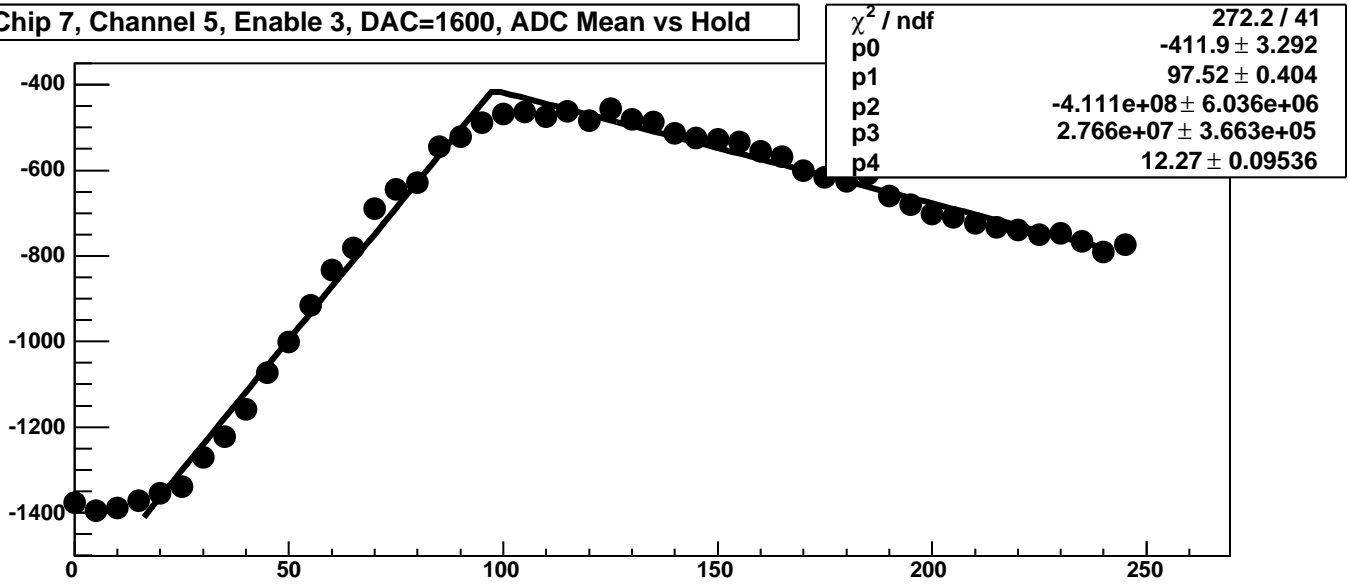
Chip 7, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



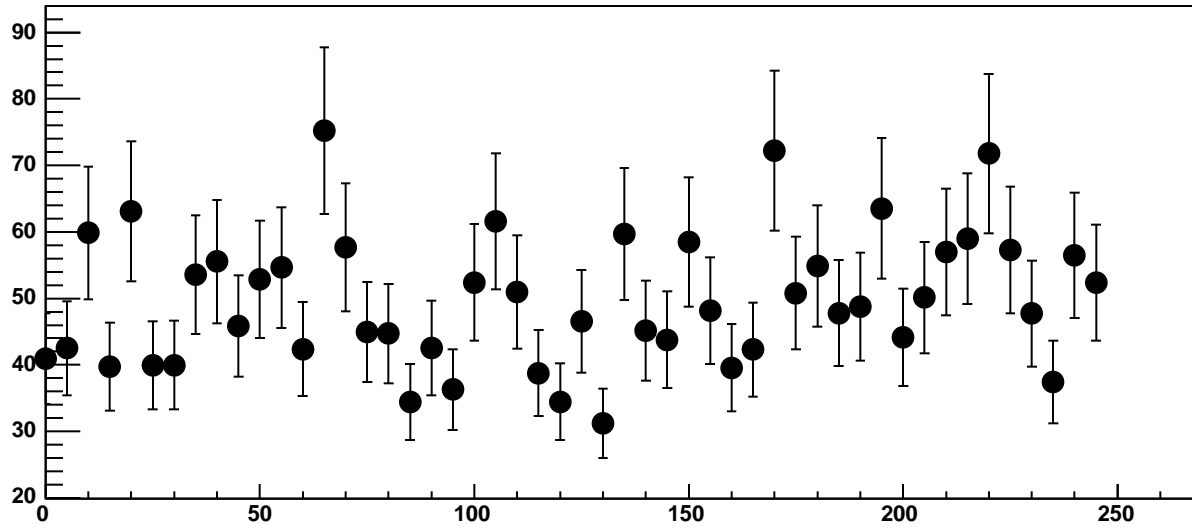
Chip 7, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold



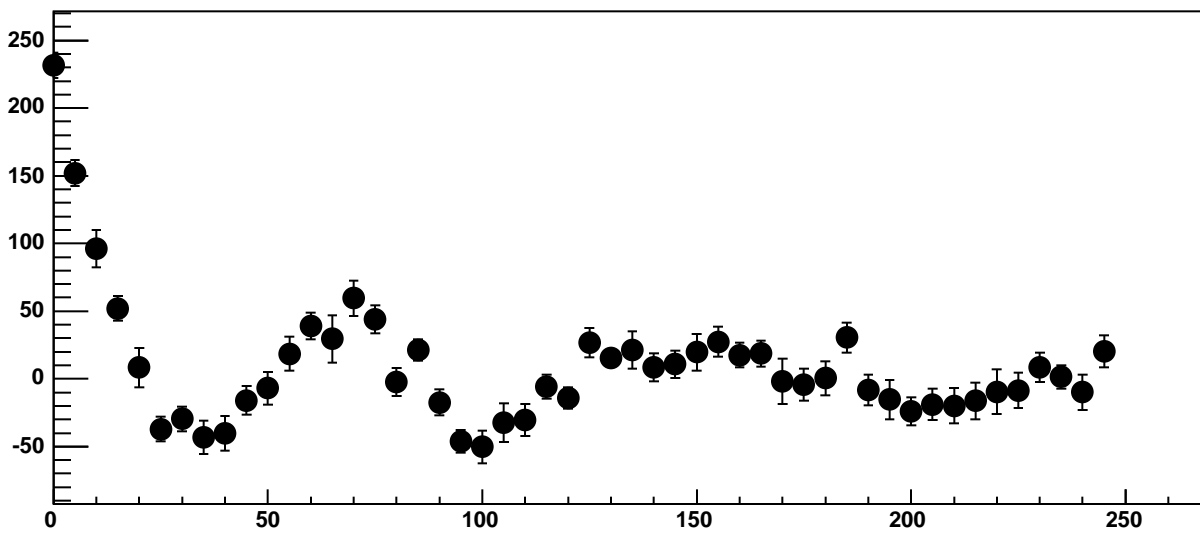
Chip 7, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold



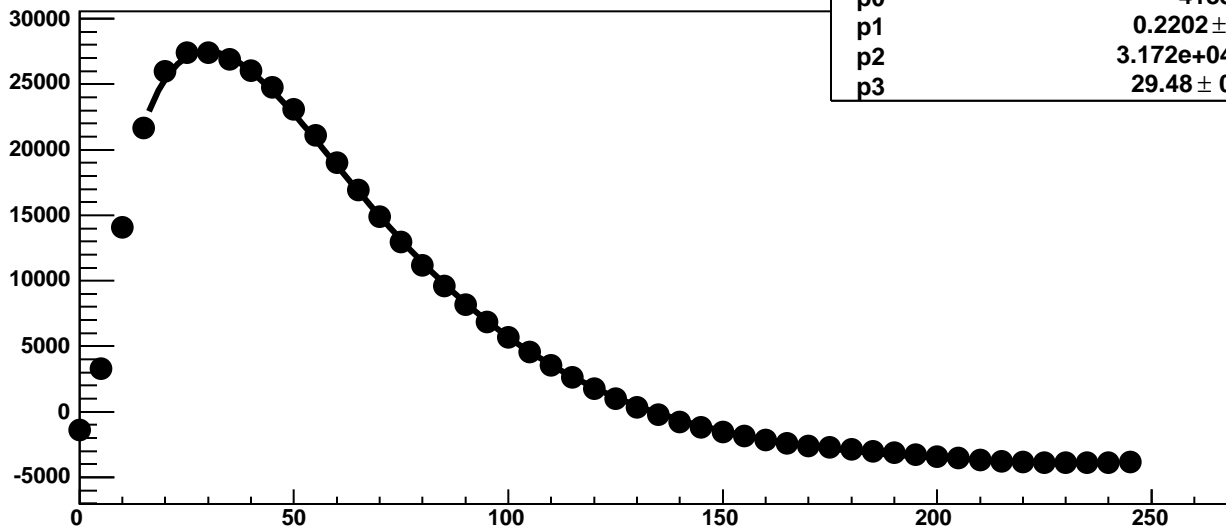
Chip 7, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

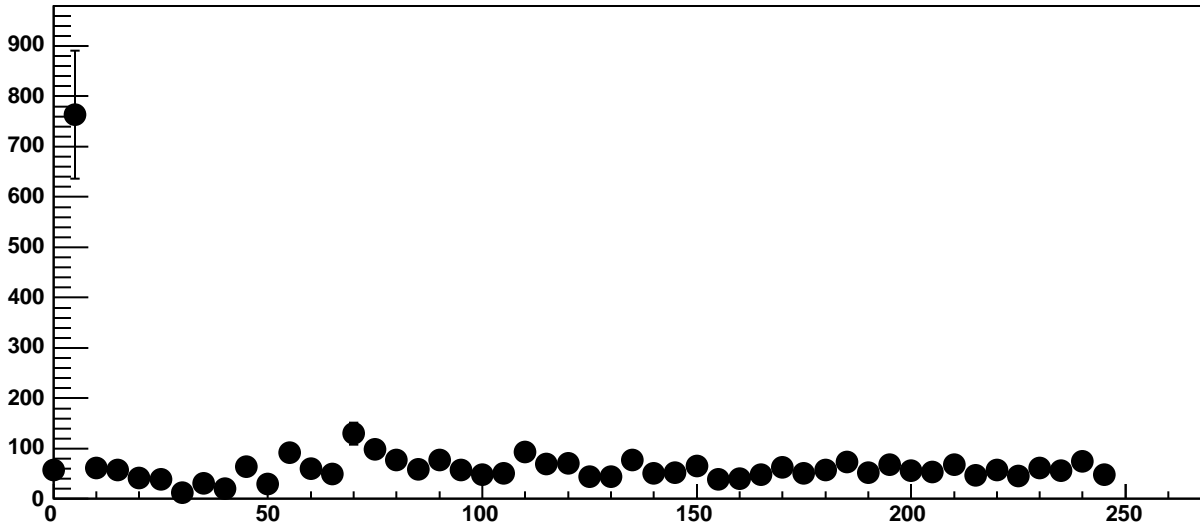


Chip 7, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

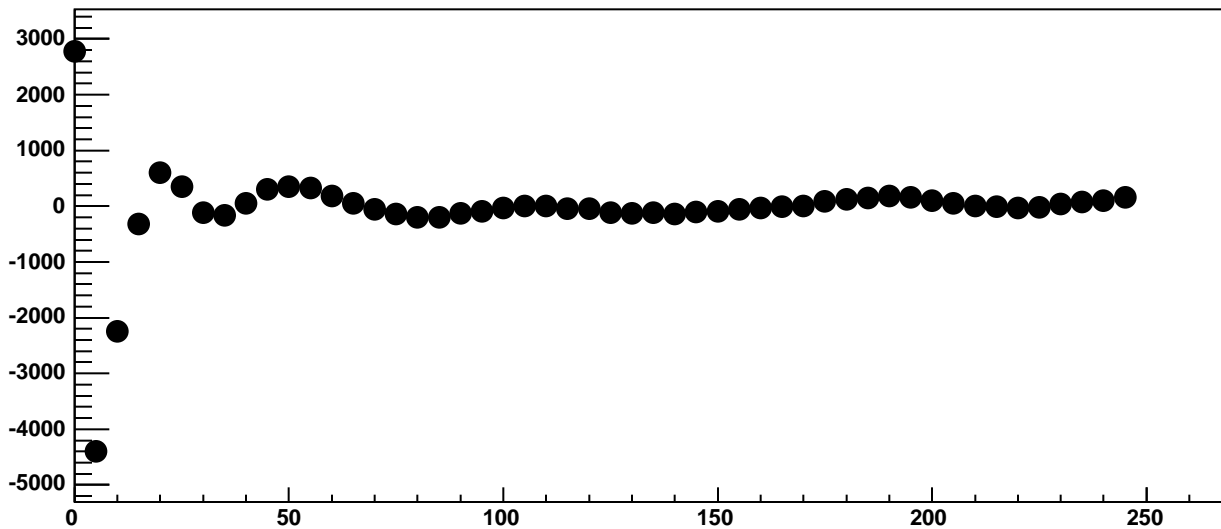


$\chi^2 / \text{ndf}$	1.354e+04 / 42
p0	-4185 ± 3.615
p1	0.2202 ± 0.01442
p2	3.172e+04 ± 3.944
p3	29.48 ± 0.009578

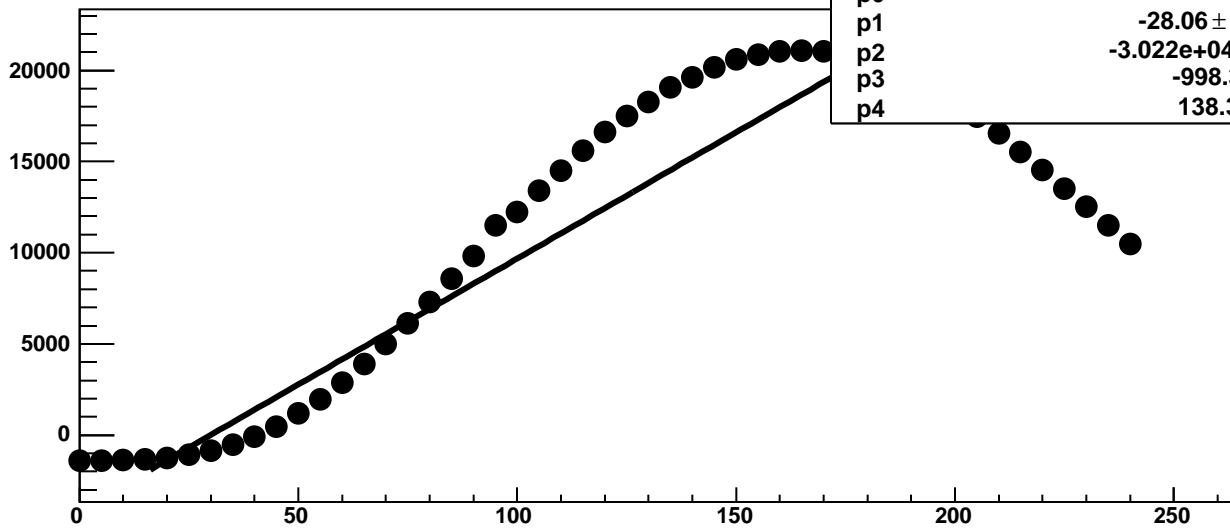
Chip 7, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold

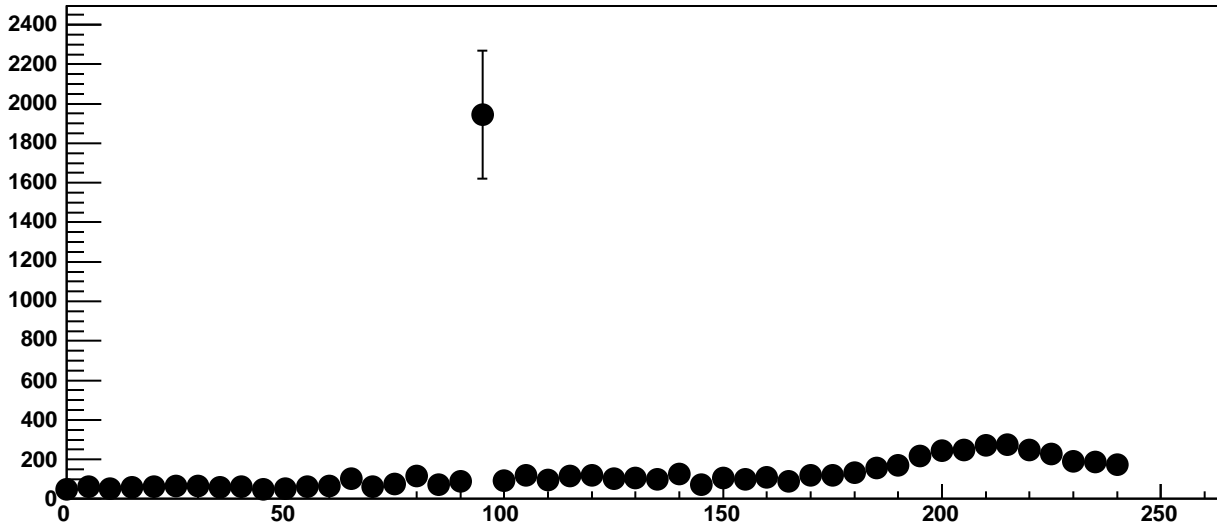


Chip 7, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

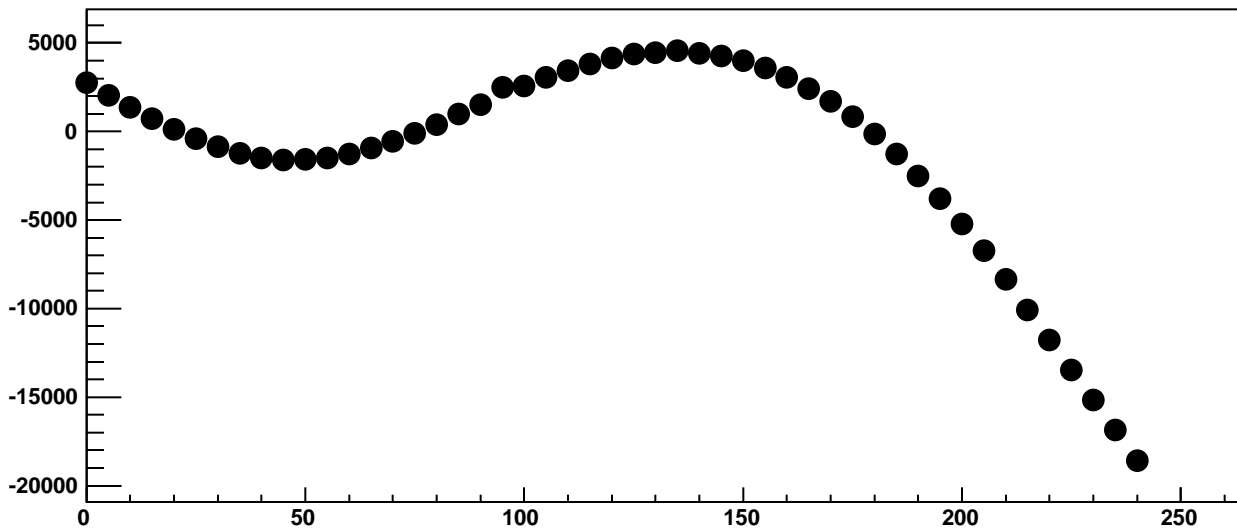


$\chi^2 / \text{ndf}$	1.145e+06 / 41
p0	2.22e+04 ± 19.33
p1	-28.06 ± 0.08789
p2	-3.022e+04 ± 20.58
p3	-998.3 ± 3.19
p4	138.3 ± 0.111

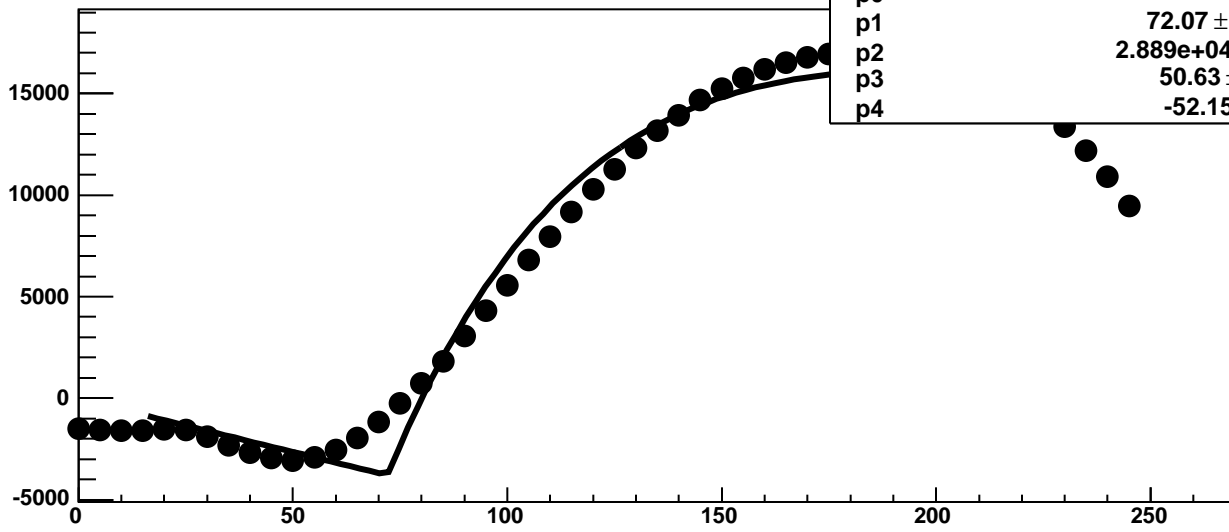
Chip 7, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

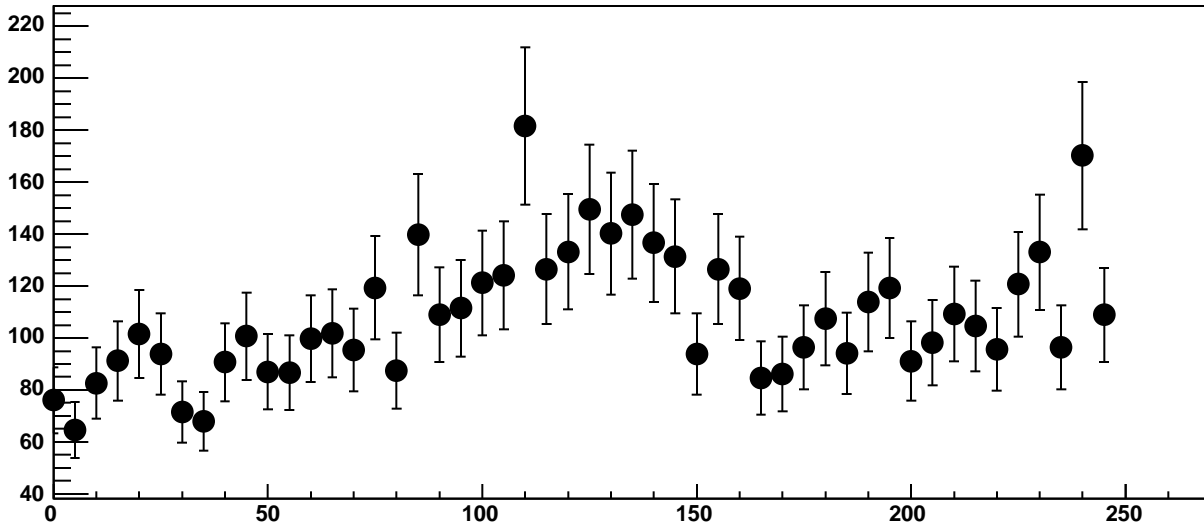


Chip 7, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

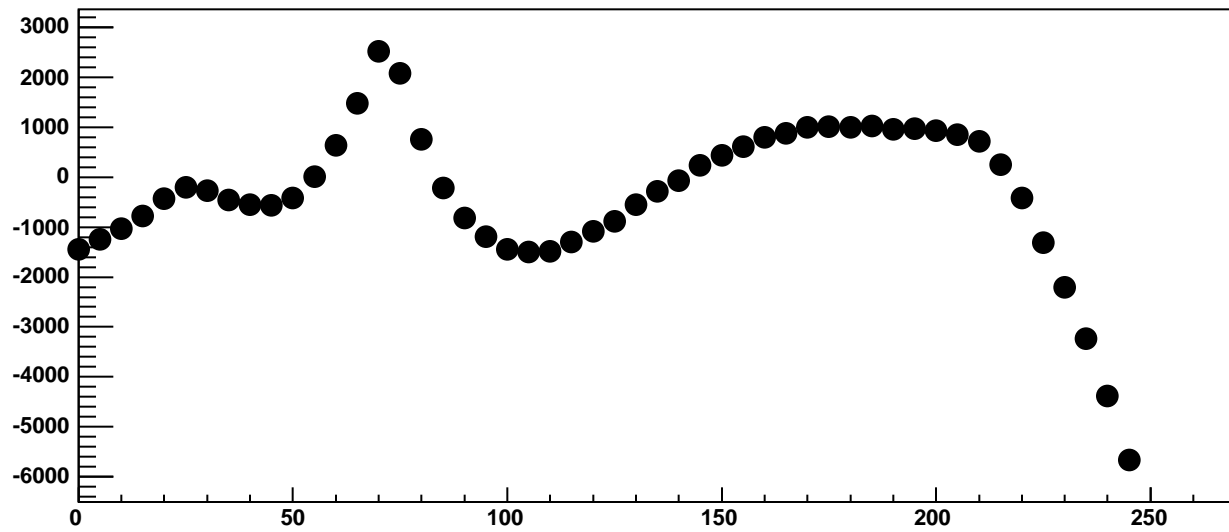


$\chi^2 / \text{ndf}$	1.055e+05 / 41
p0	-3804 ± 9.638
p1	72.07 ± 0.03691
p2	2.889e+04 ± 60.57
p3	50.63 ± 0.1178
p4	-52.15 ± 0.285

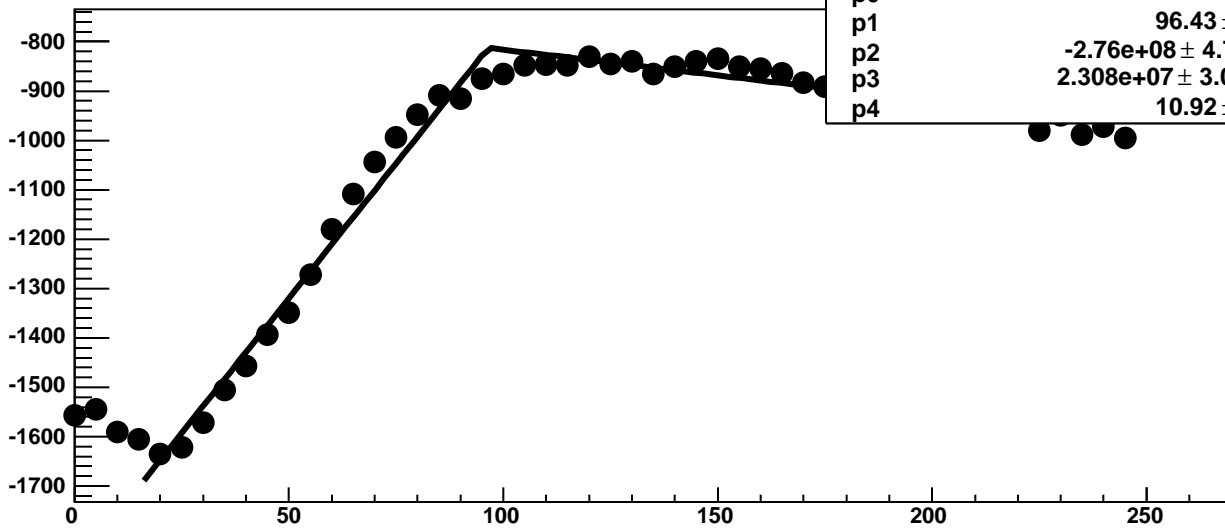
Chip 7, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

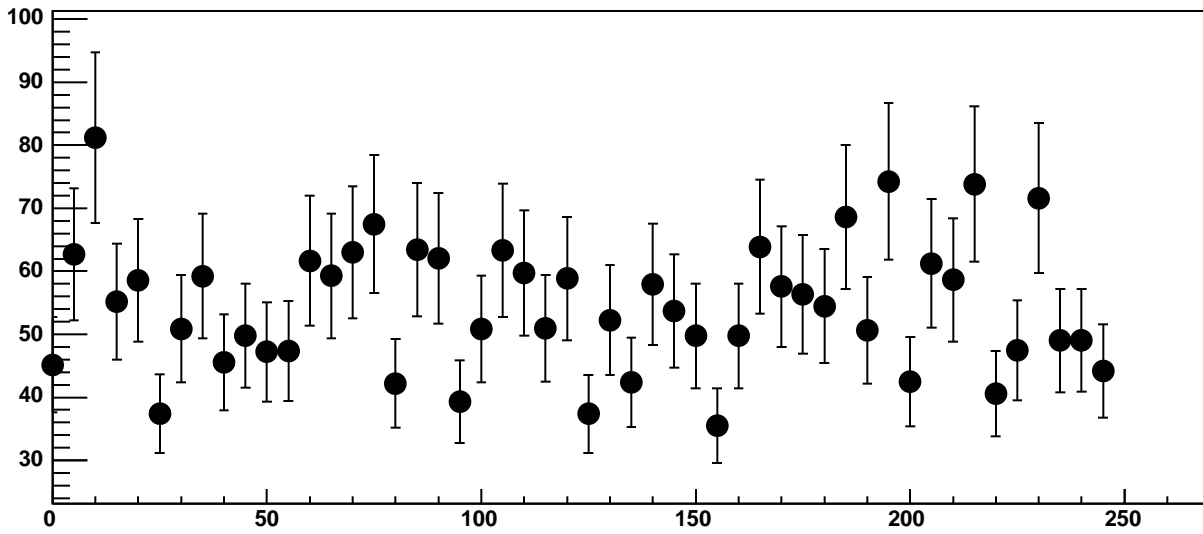


Chip 7, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

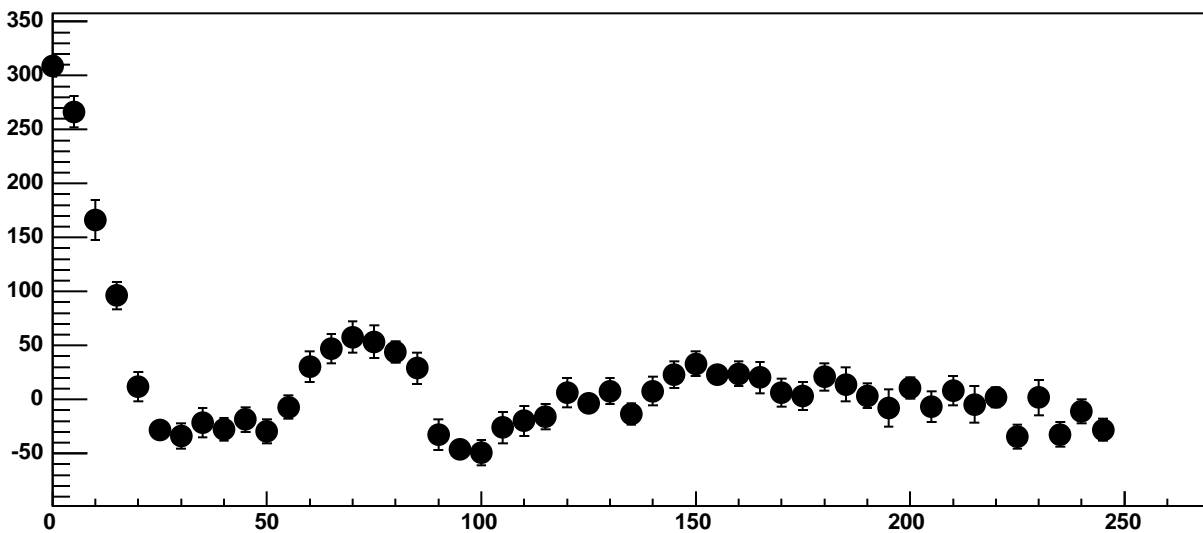


$\chi^2 / \text{ndf}$	278.5 / 41
p0	$-812.7 \pm 4.063$
p1	$96.43 \pm 0.5922$
p2	$-2.76\text{e}+08 \pm 4.724\text{e}+06$
p3	$2.308\text{e}+07 \pm 3.073\text{e}+05$
p4	$10.92 \pm 0.1127$

Chip 7, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

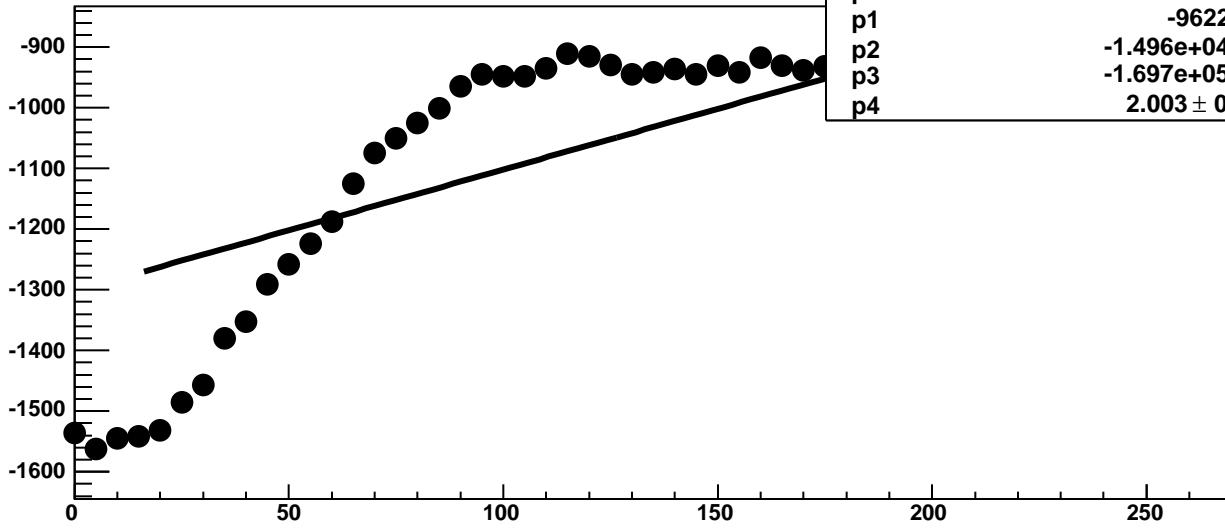


Chip 7, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



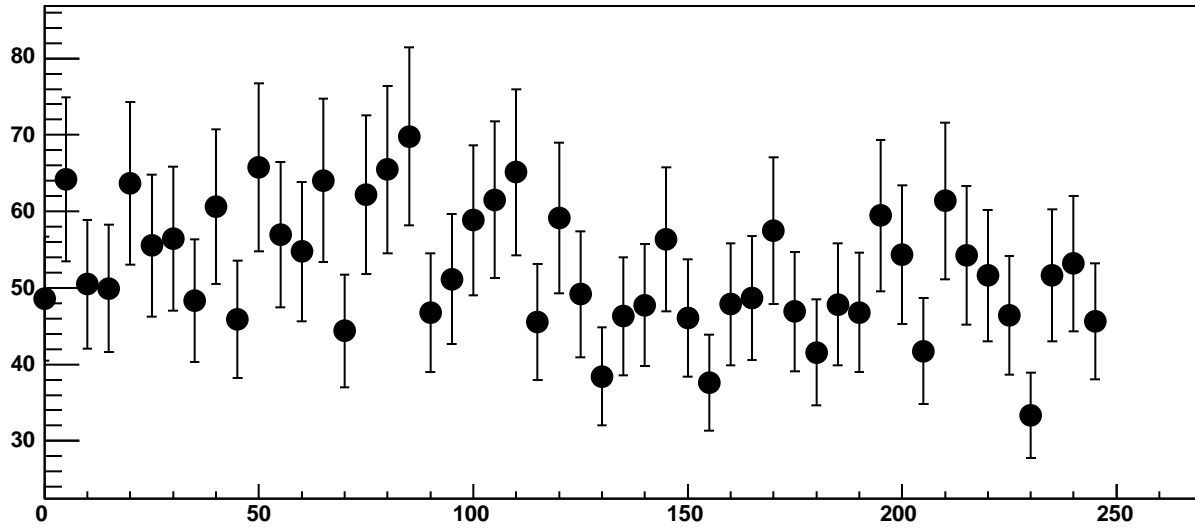


Chip 7, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold

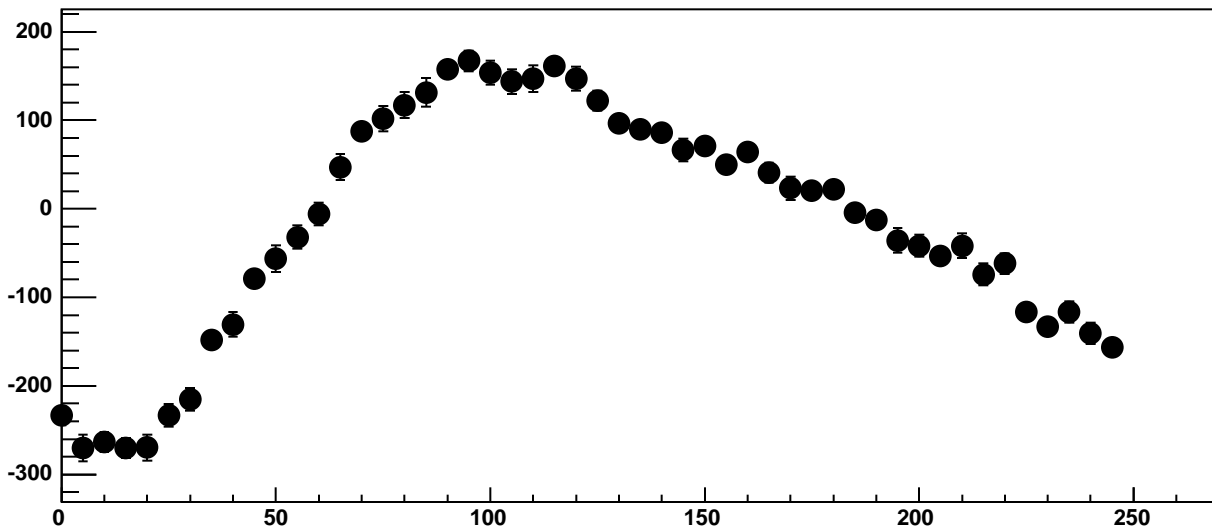


$\chi^2 / \text{ndf}$	4523 / 41
p0	-5616 ± 10.42
p1	-9622 ± 1.888
p2	-1.496e+04 ± 8.893
p3	-1.697e+05 ± 467.5
p4	2.003 ± 0.001067

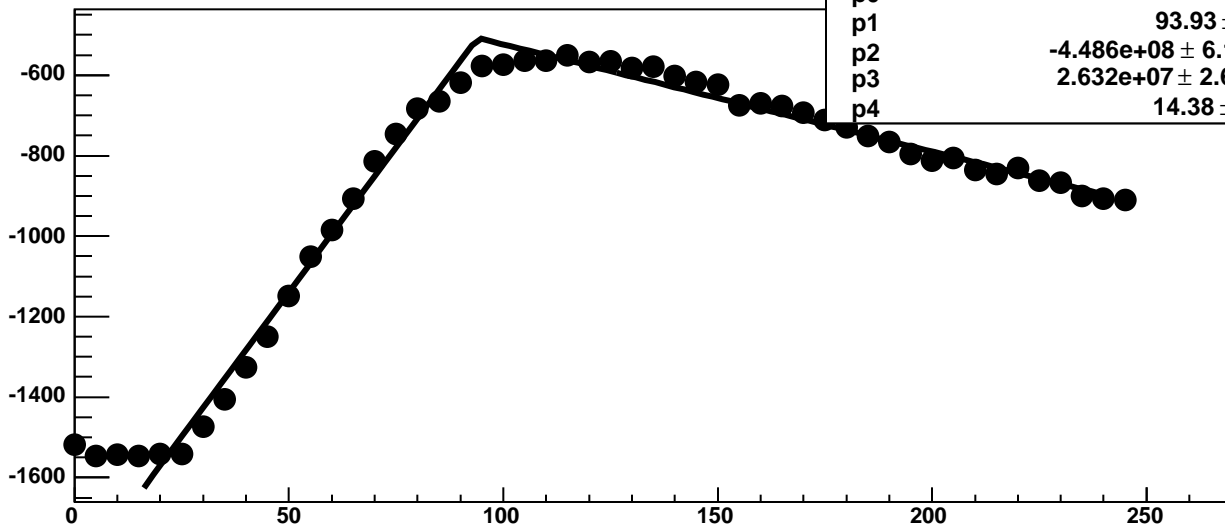
Chip 7, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold

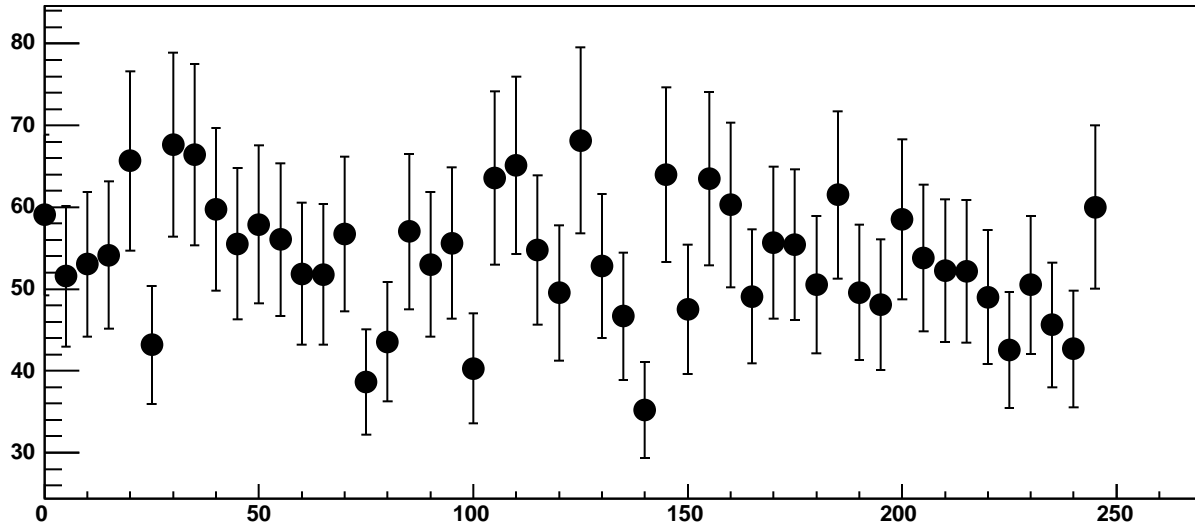


Chip 7, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

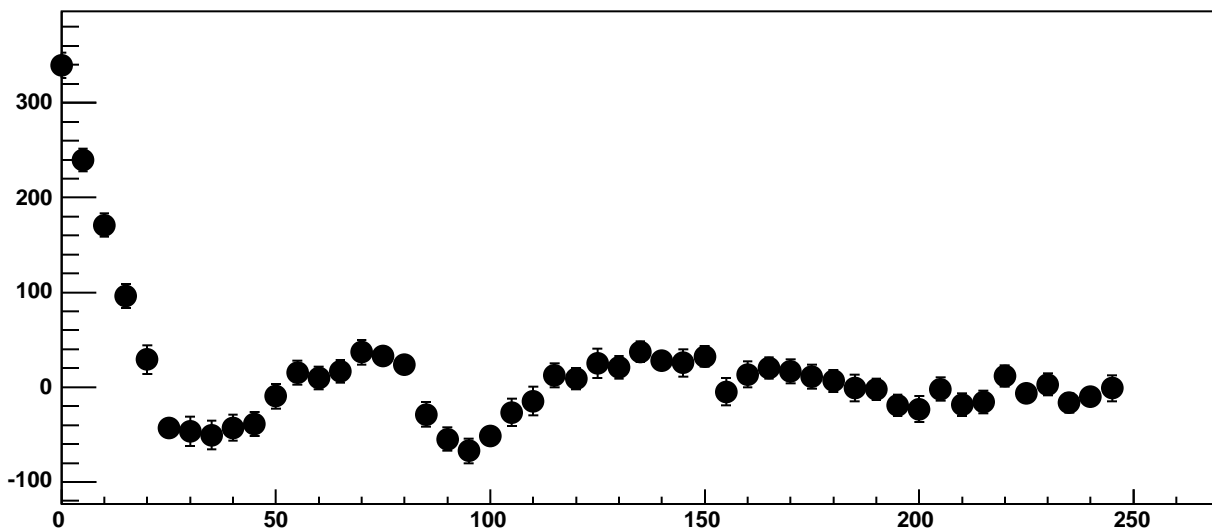


$\chi^2 / \text{ndf}$	307.2 / 41
p0	-507.1 ± 3.725
p1	93.93 ± 0.4268
p2	-4.486e+08 ± 6.193e+06
p3	2.632e+07 ± 2.639e+05
p4	14.38 ± 0.1314

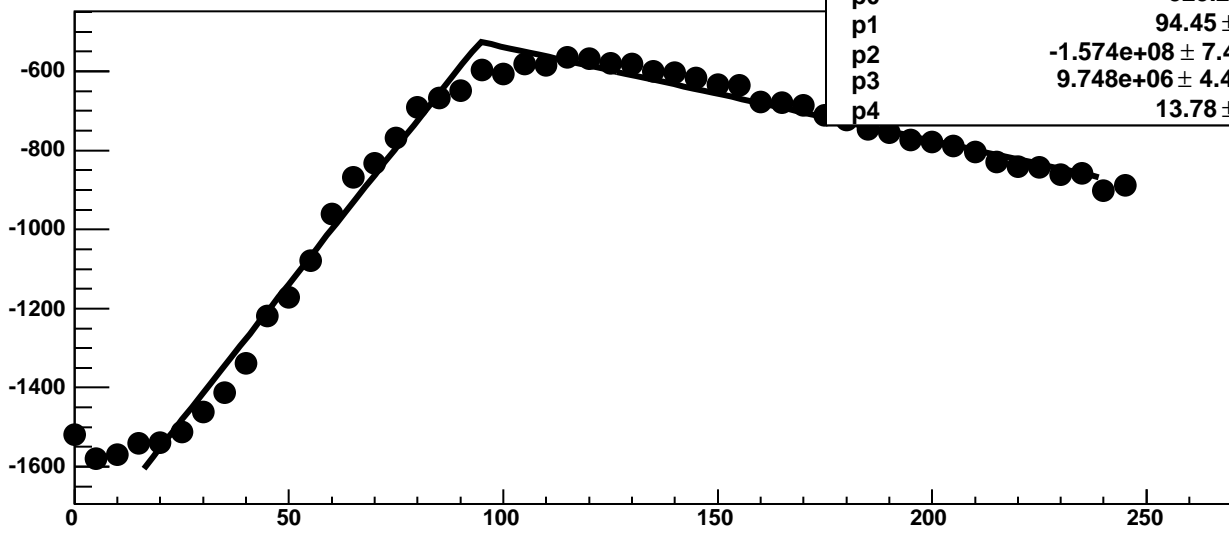
Chip 7, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

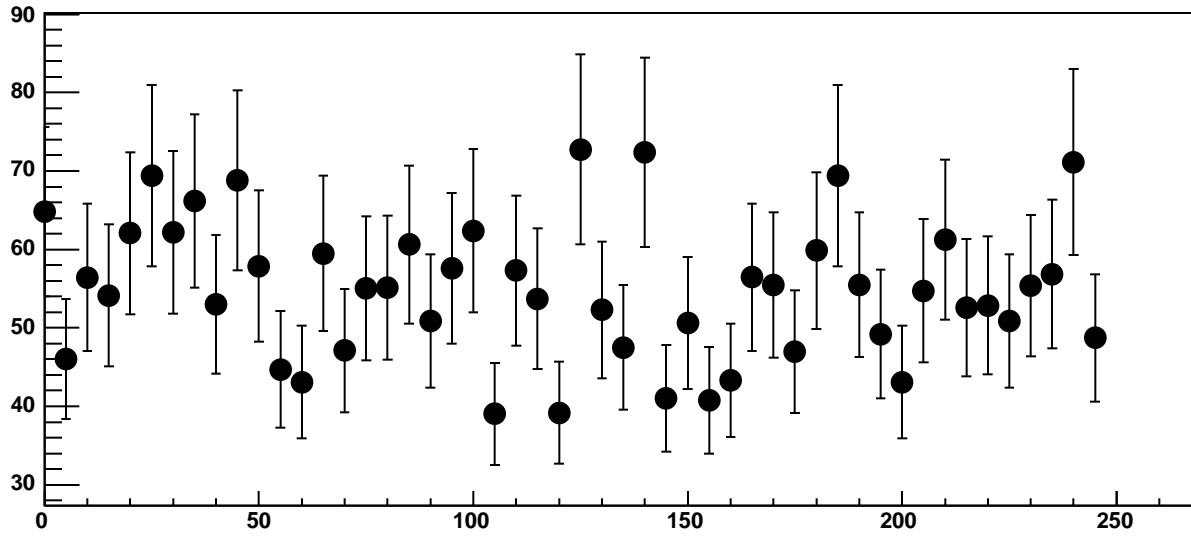


Chip 7, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

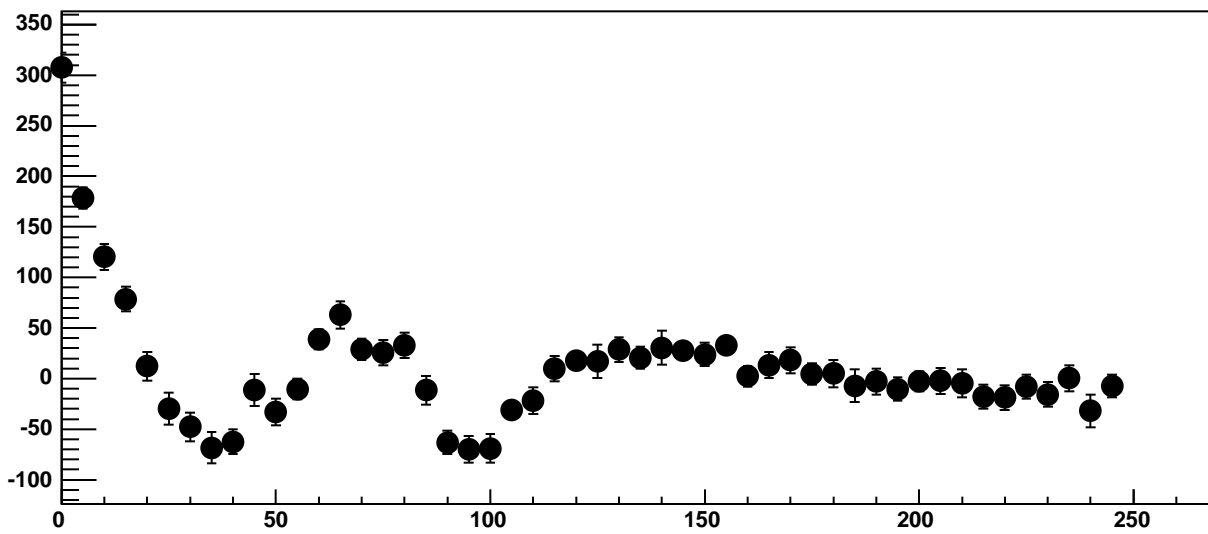


$\chi^2 / \text{ndf}$	319.1 / 41
p0	$-525.2 \pm 3.744$
p1	$94.45 \pm 0.4763$
p2	$-1.574\text{e}+08 \pm 7.416\text{e}+06$
p3	$9.748\text{e}+06 \pm 4.419\text{e}+05$
p4	$13.78 \pm 0.1418$

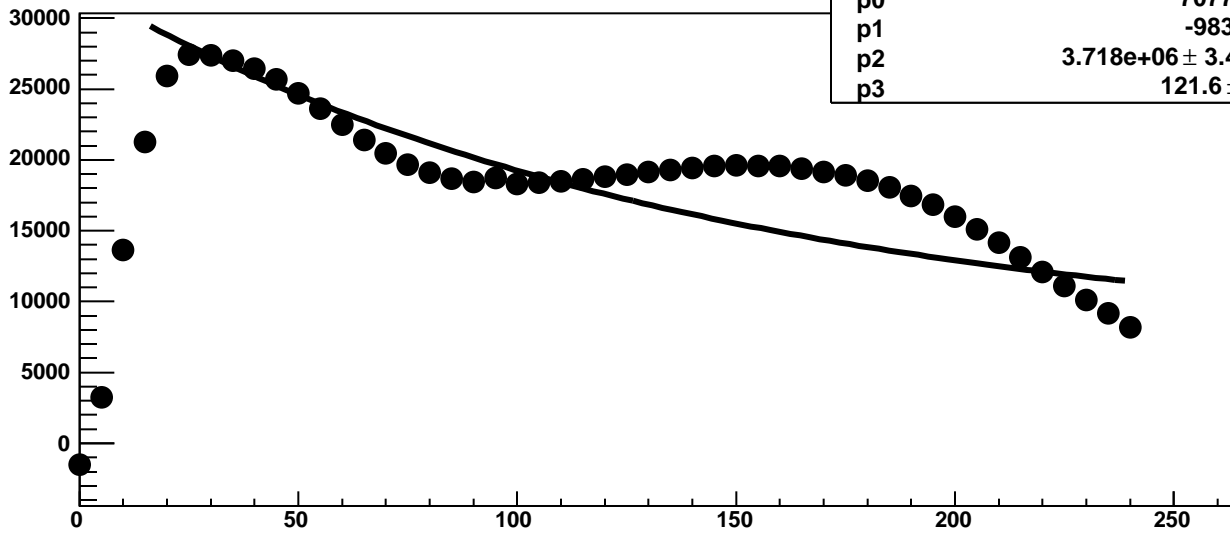
Chip 7, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

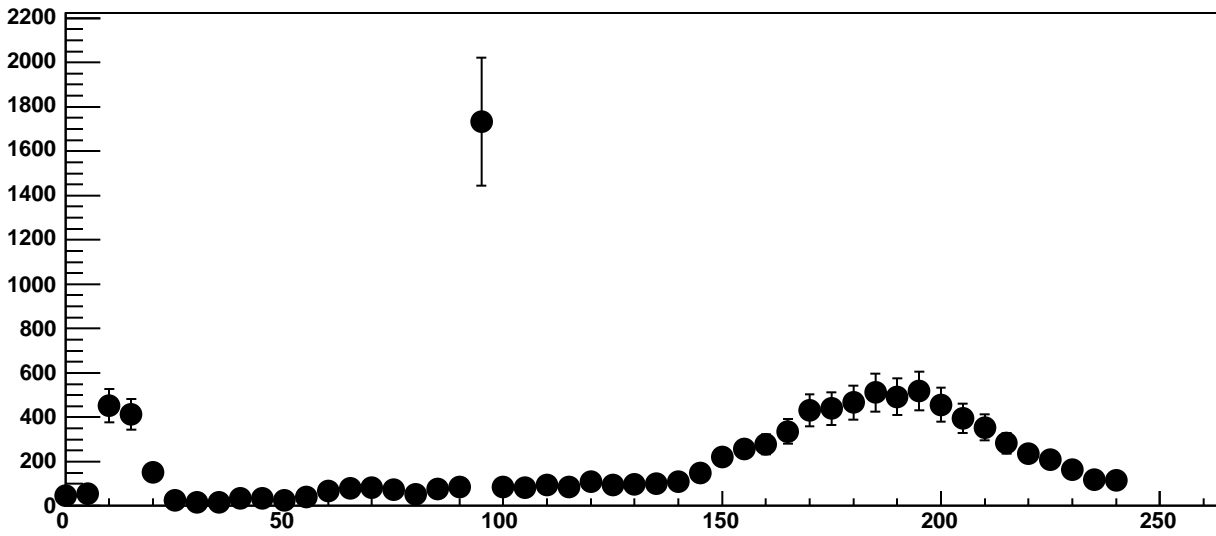


Chip 7, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

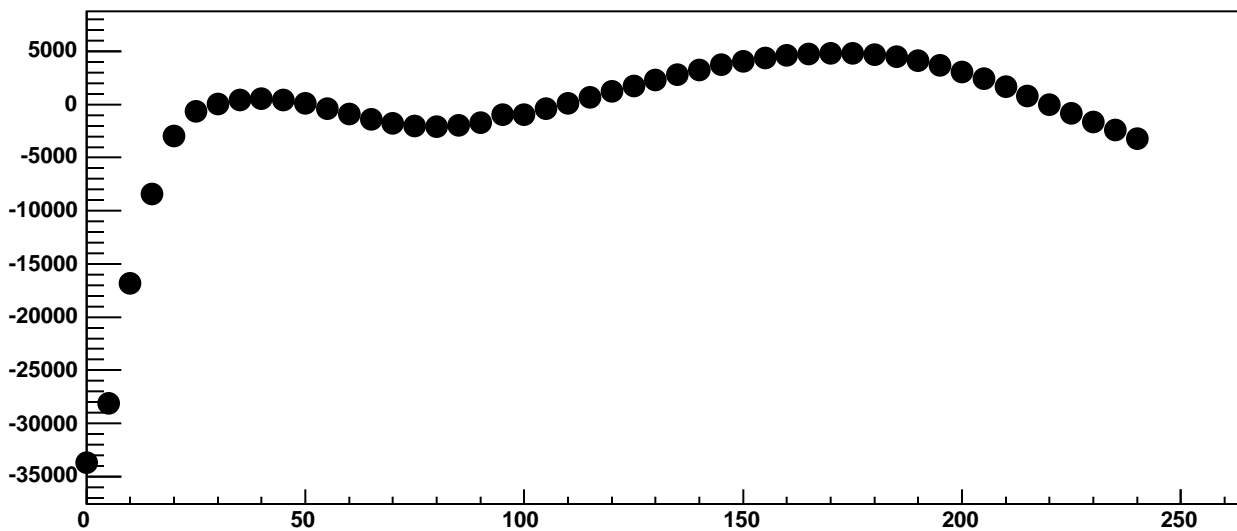


$\chi^2 / \text{ndf}$	2.535e+05 / 42
p0	7077 ± 43.03
p1	-983.5 ± 3
p2	3.718e+06 ± 3.405e+04
p3	121.6 ± 0.3739

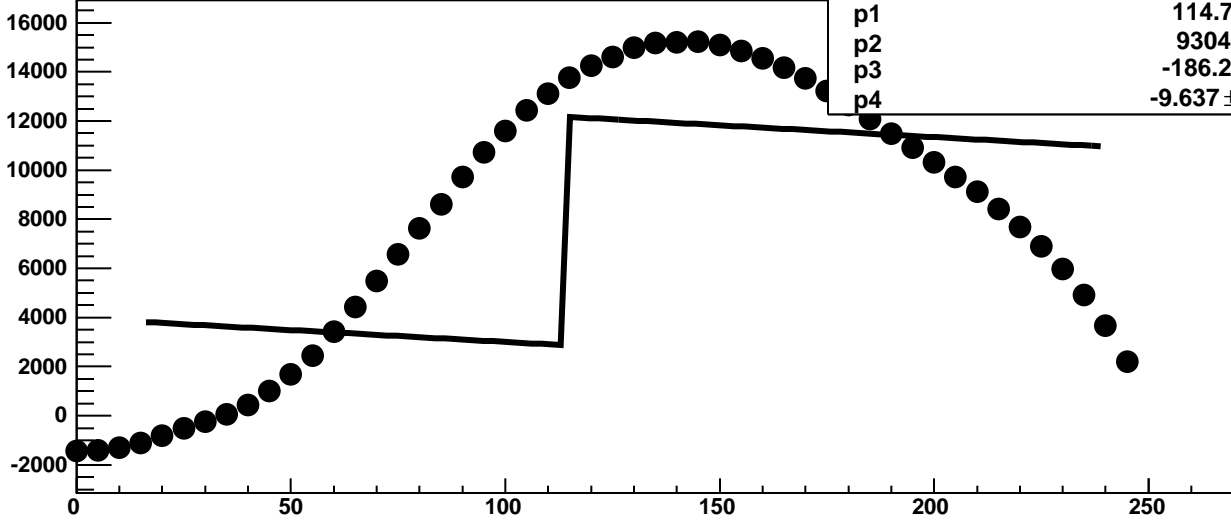
Chip 7, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



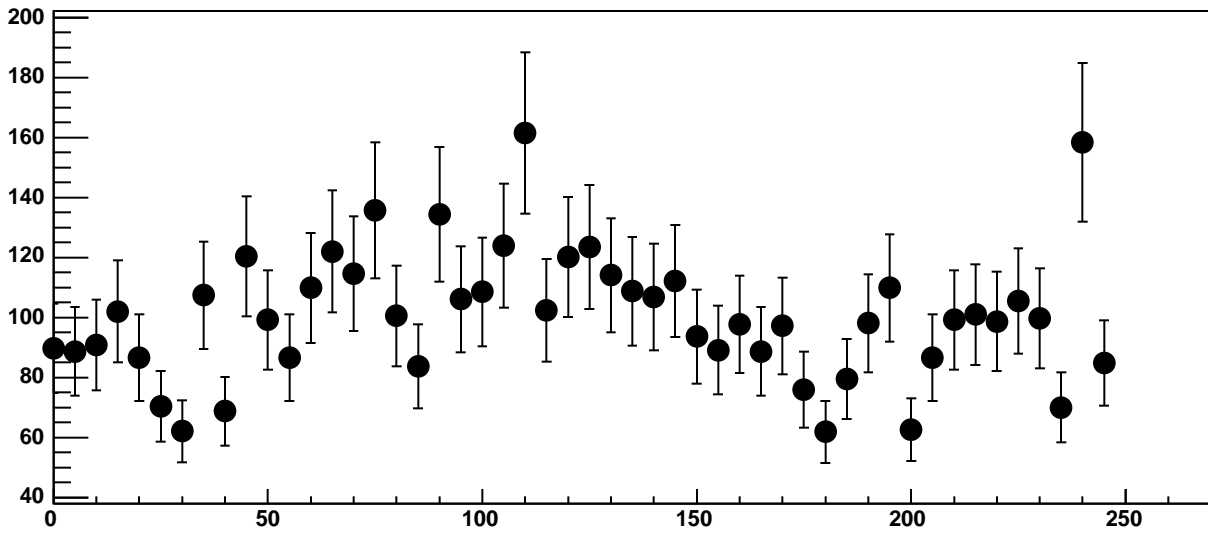
Chip 7, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold



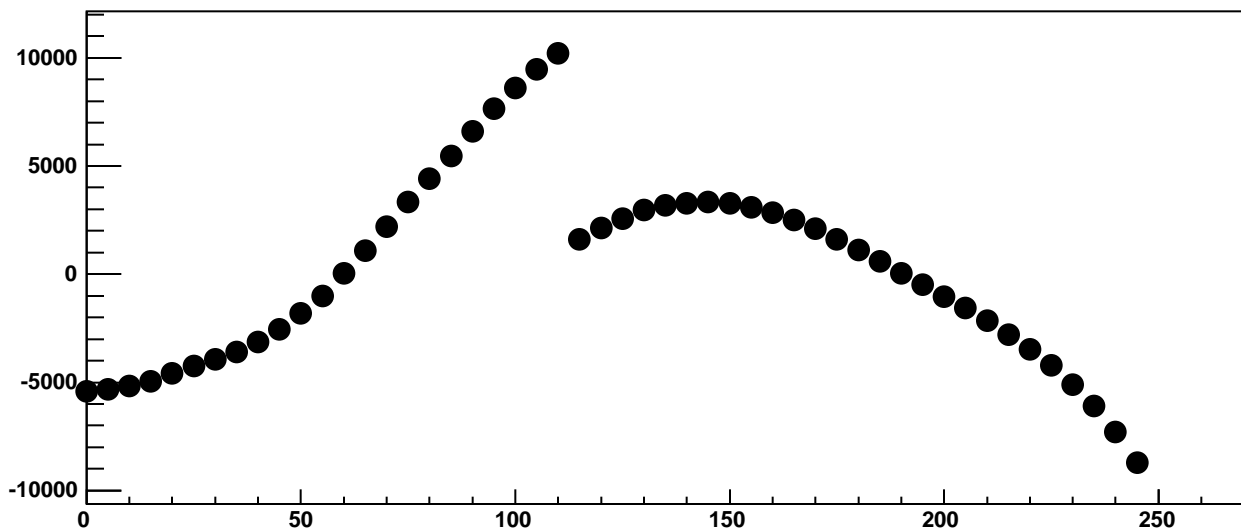
Chip 7, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold



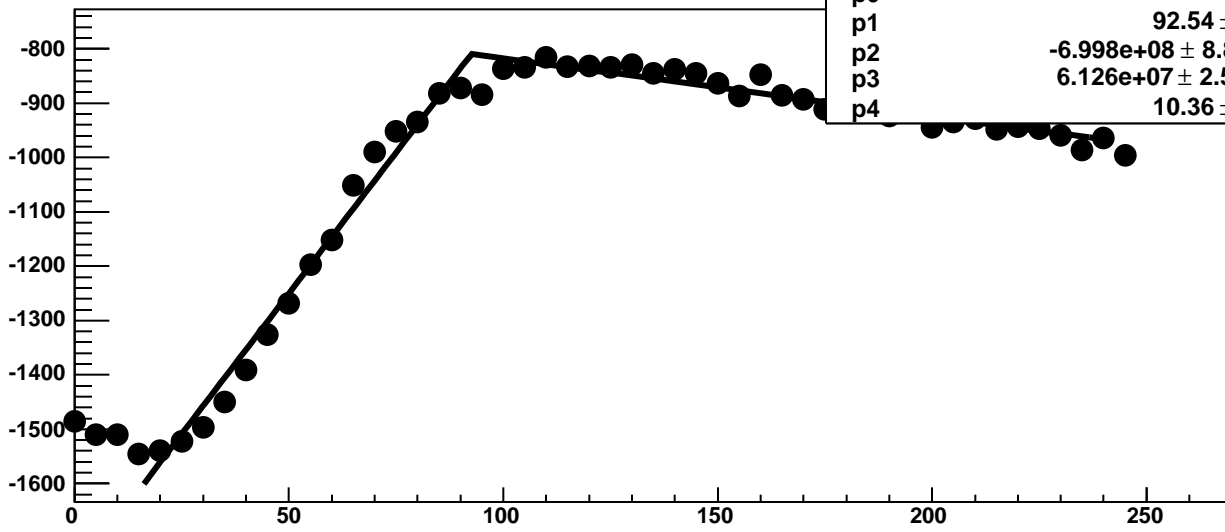
Chip 7, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

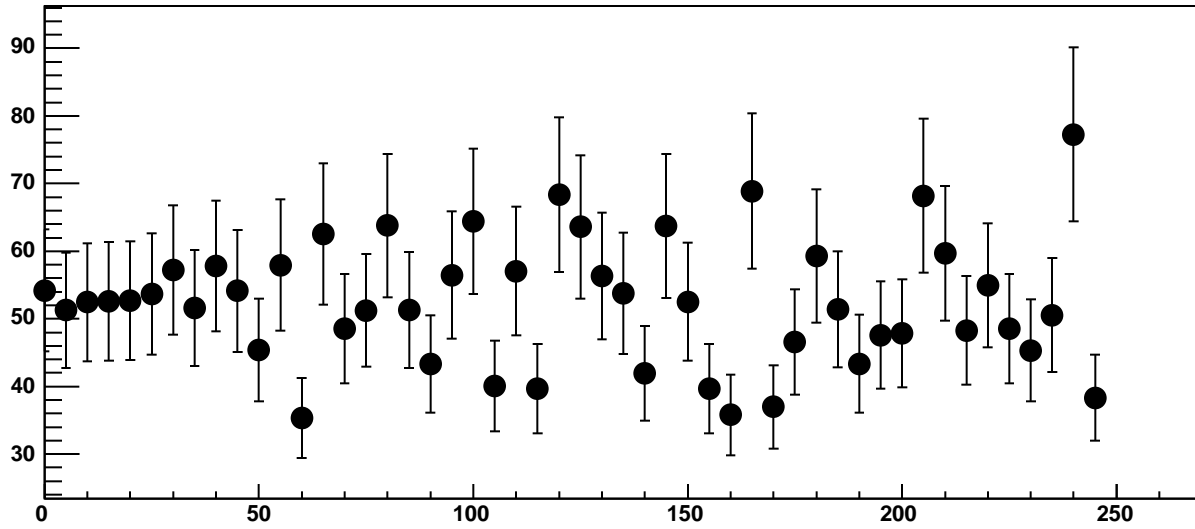


Chip 7, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

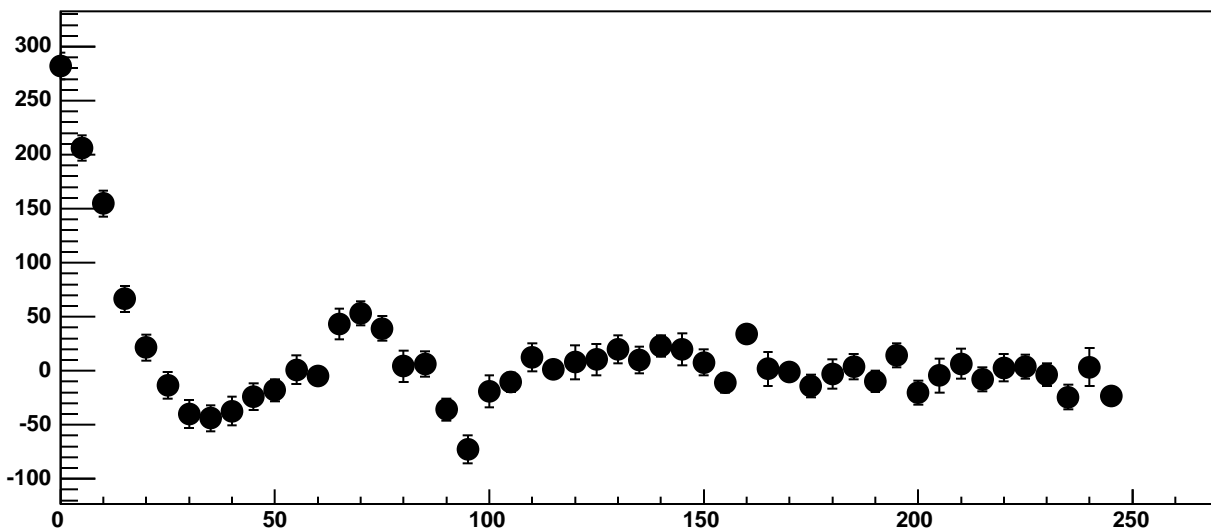


$\chi^2 / \text{ndf}$	209.2 / 41
p0	-809.5 ± 3.94
p1	92.54 ± 0.6254
p2	-6.998e+08 ± 8.897e+06
p3	6.126e+07 ± 2.531e+05
p4	10.36 ± 0.1276

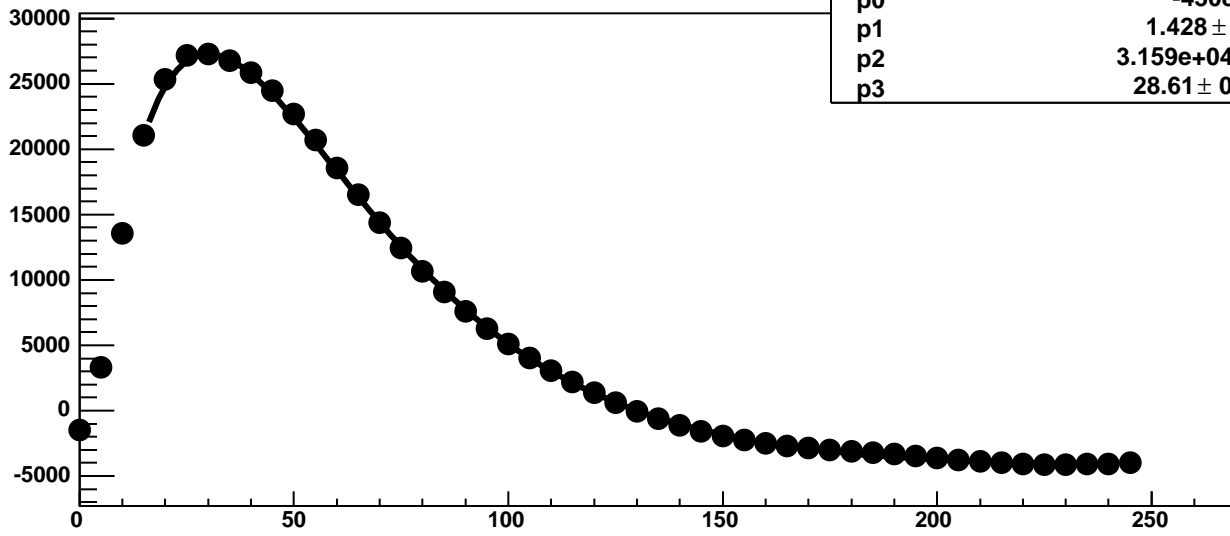
Chip 7, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

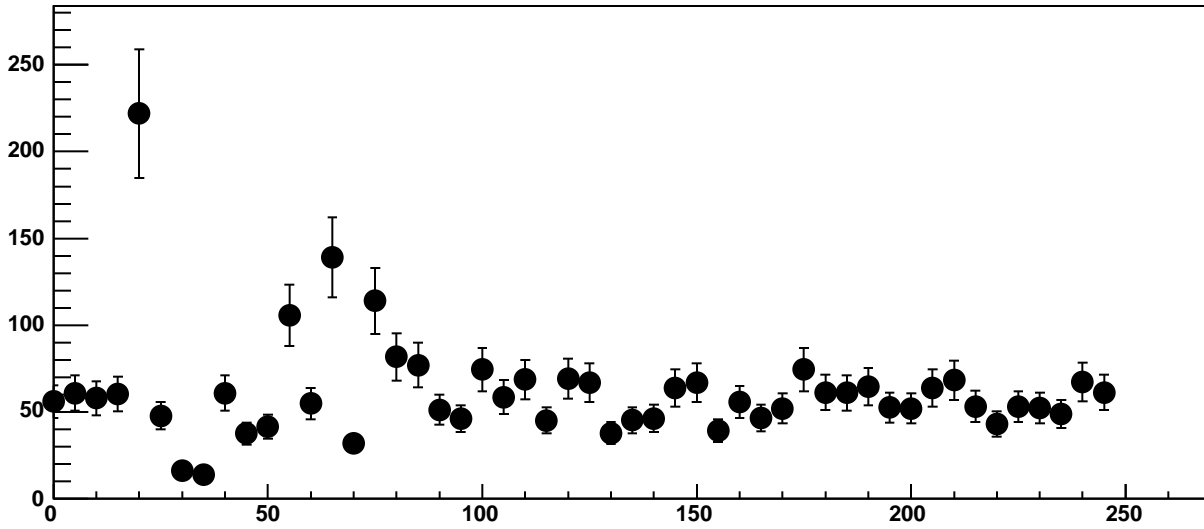


Chip 7, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold

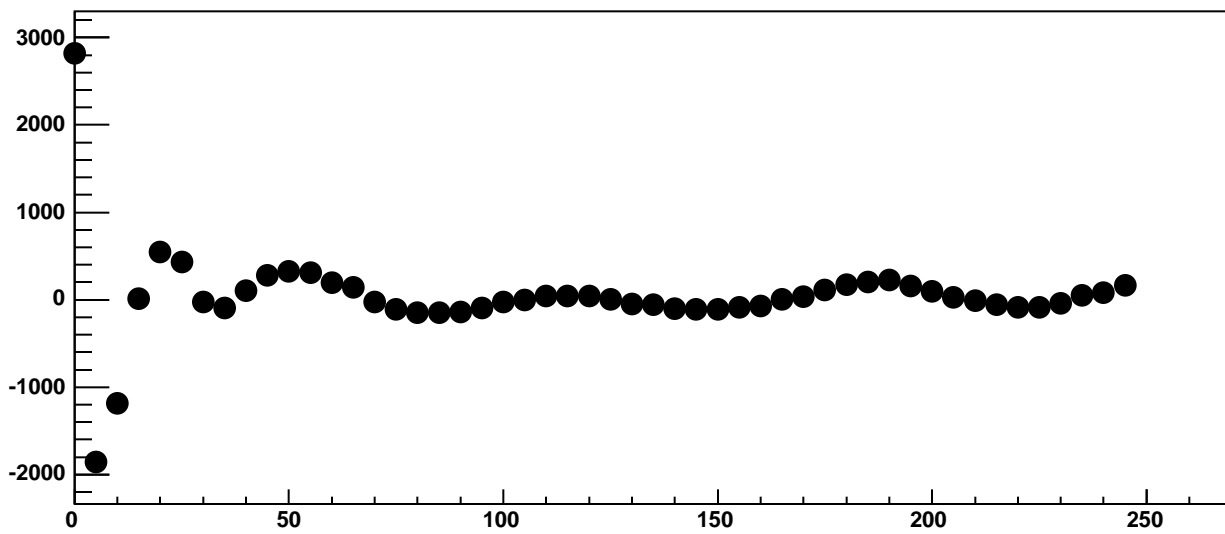


$\chi^2 / \text{ndf}$	7093 / 42
p0	$-4308 \pm 3.438$
p1	$1.428 \pm 0.01489$
p2	$3.159\text{e}+04 \pm 3.975$
p3	$28.61 \pm 0.008849$

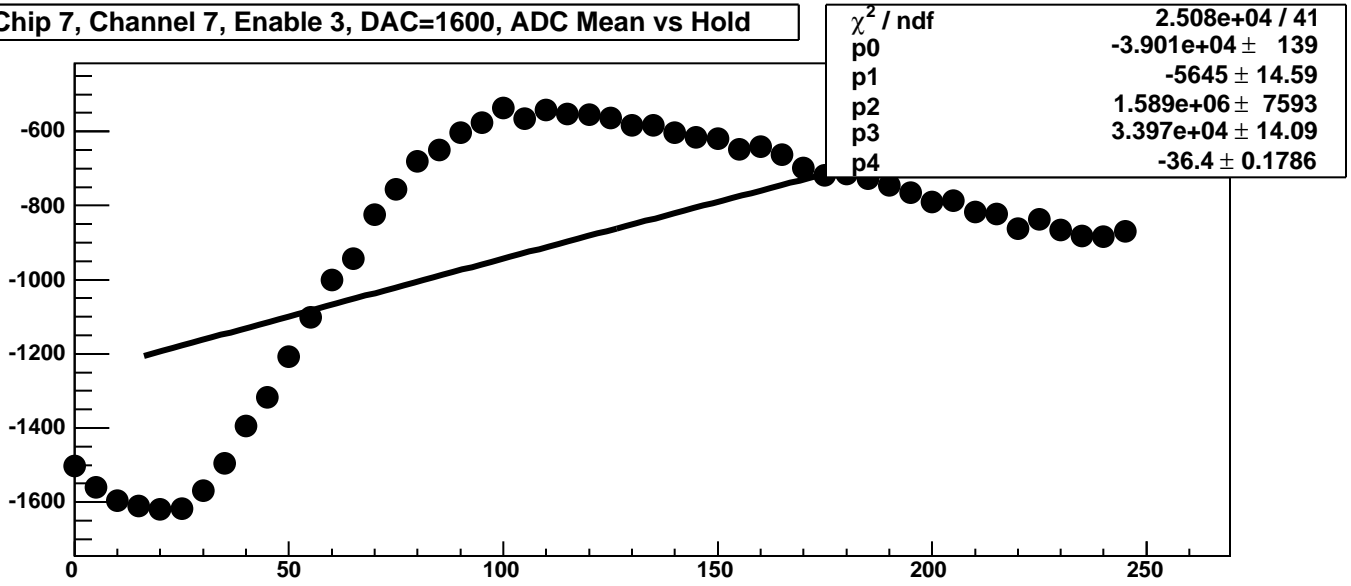
Chip 7, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



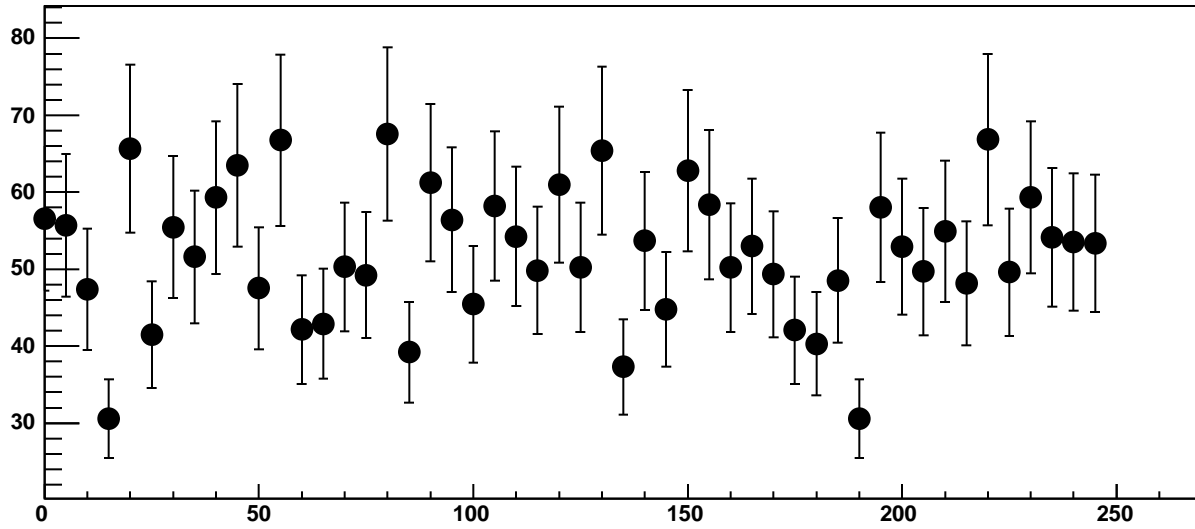
Chip 7, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold



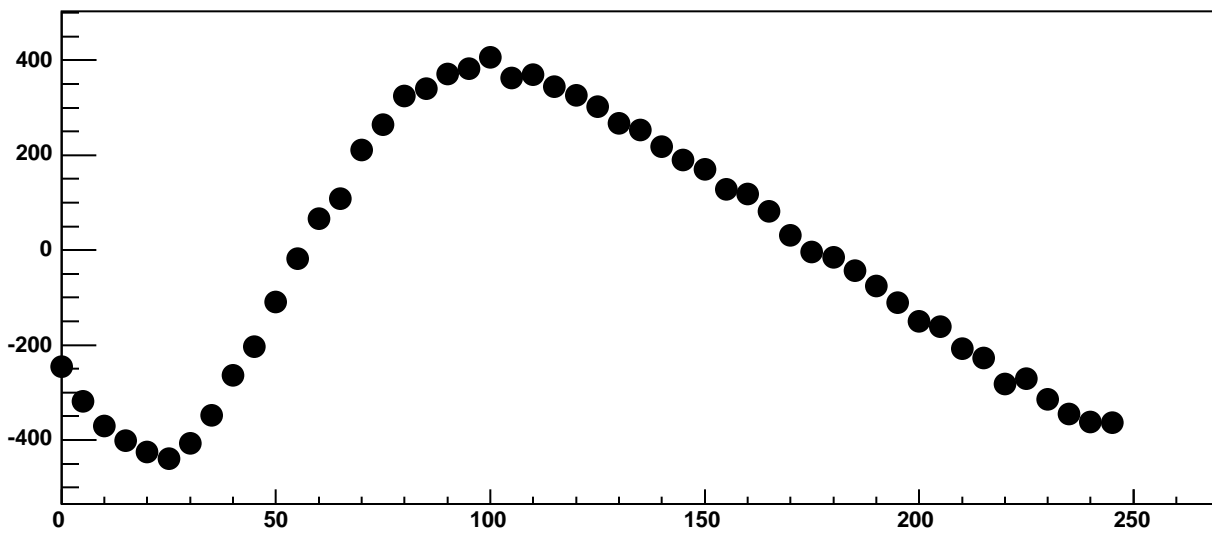
Chip 7, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold



Chip 7, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

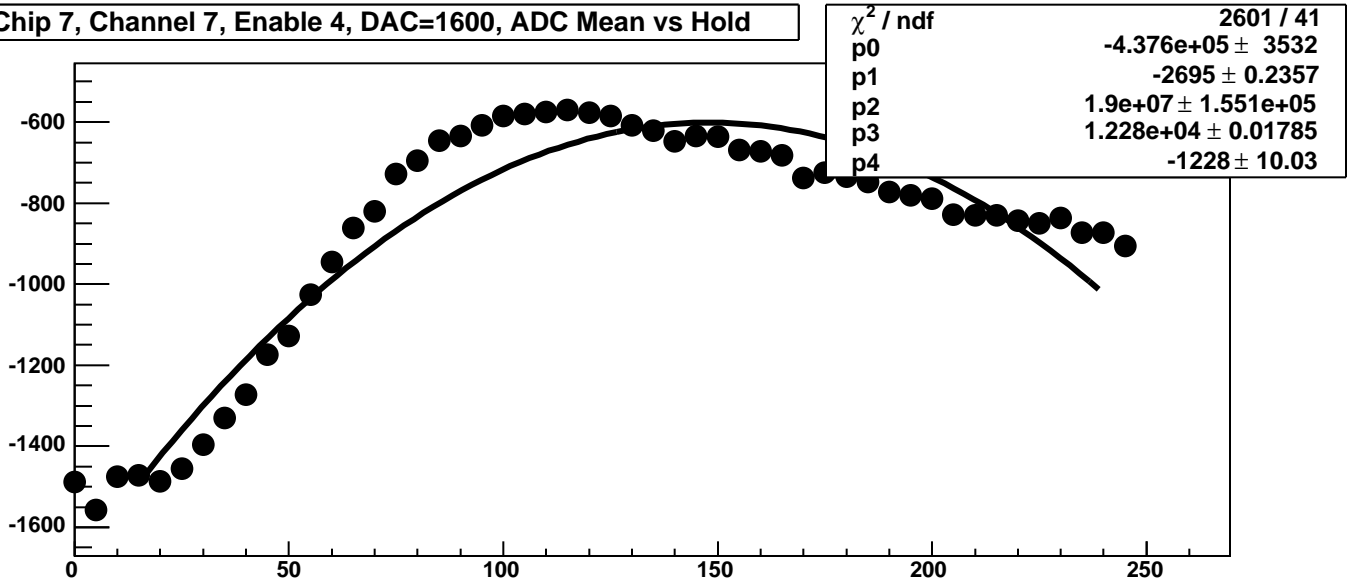


Chip 7, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

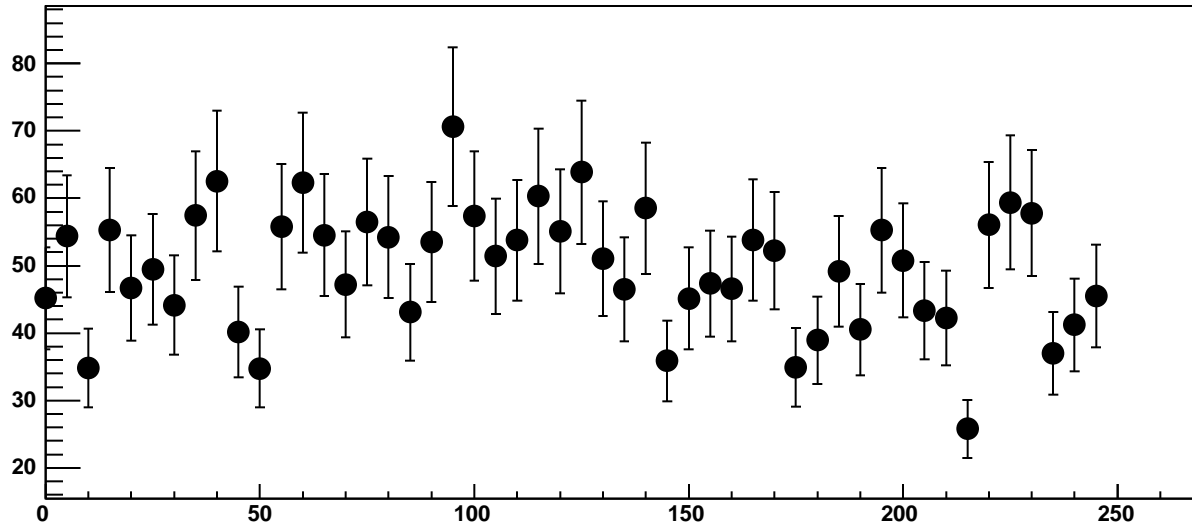




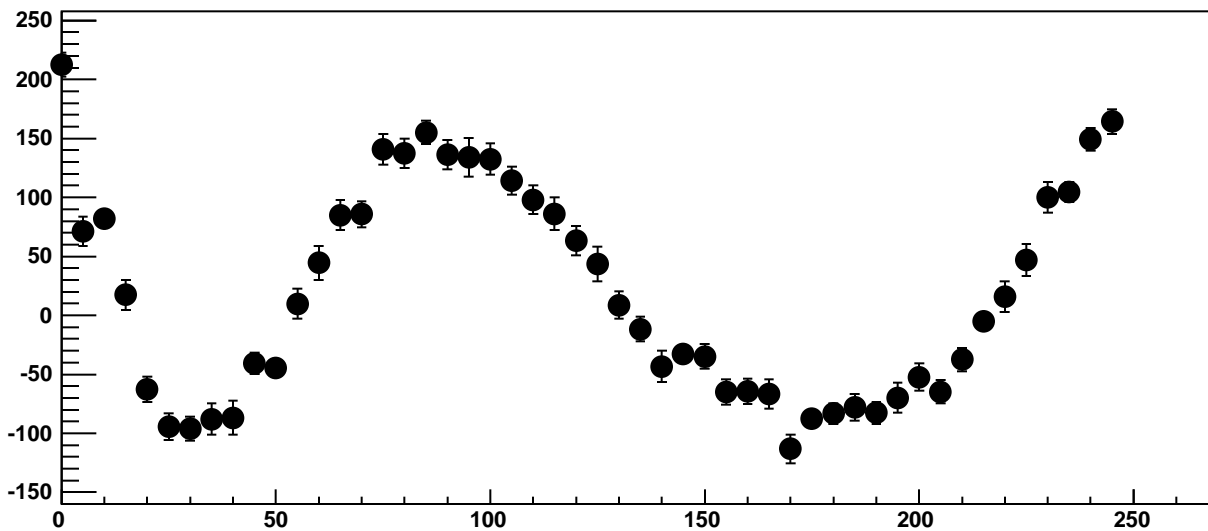
Chip 7, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold



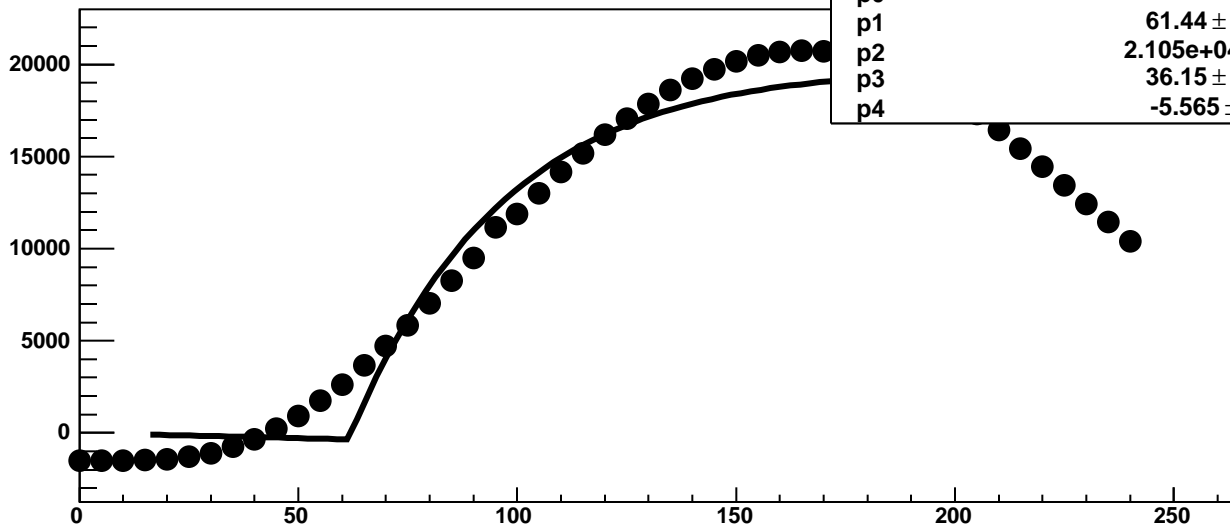
Chip 7, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

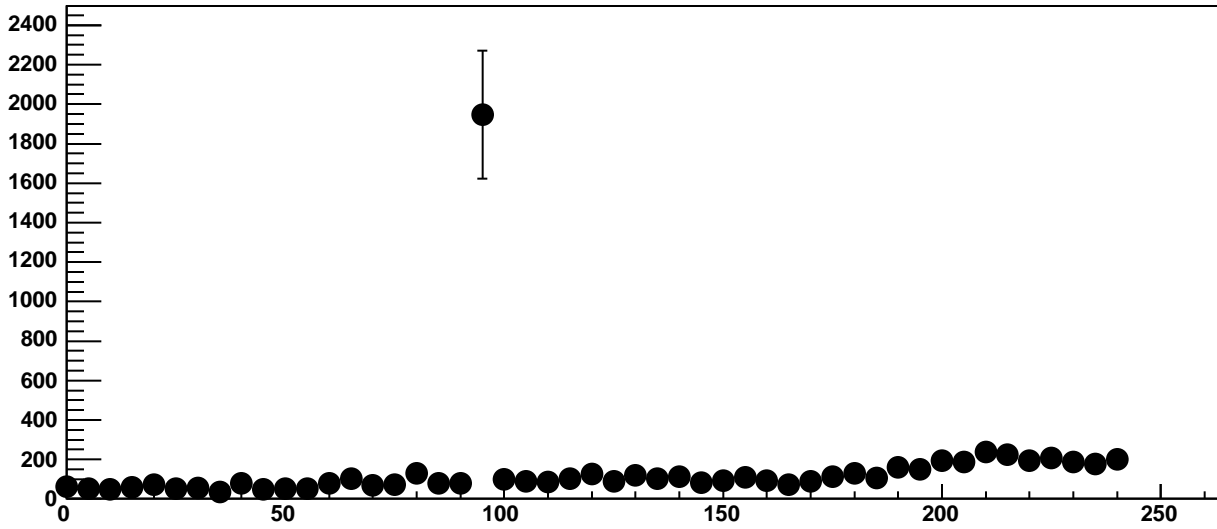


Chip 7, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold

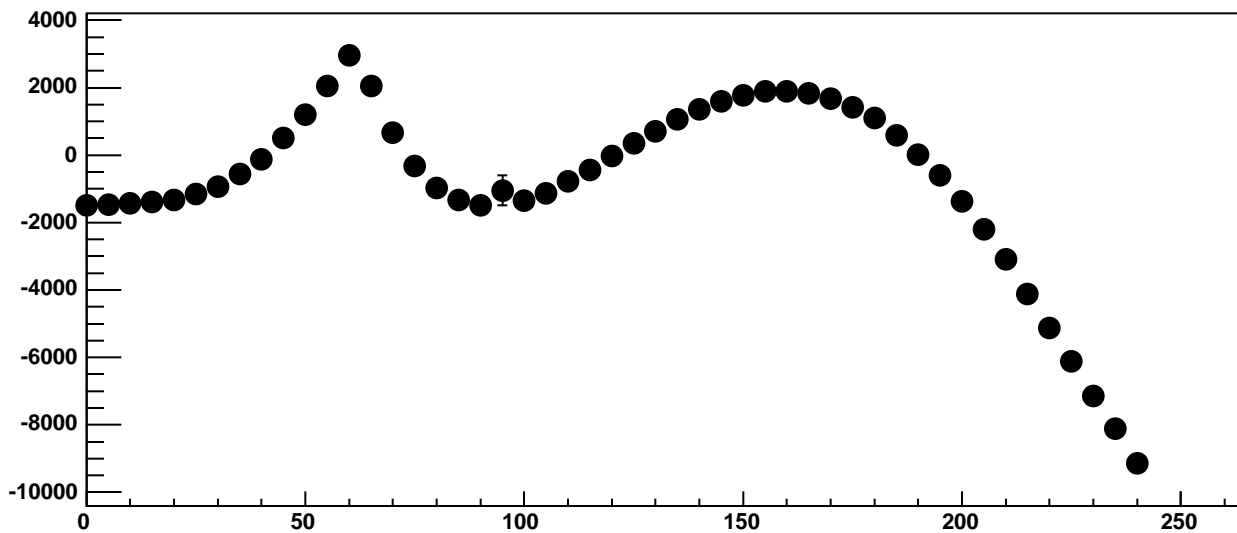


$\chi^2 / \text{ndf}$	3.419e+05 / 41
p0	-349.3 ± 6.336
p1	61.44 ± 0.02935
p2	2.105e+04 ± 34.7
p3	36.15 ± 0.07376
p4	-5.565 ± 0.2084

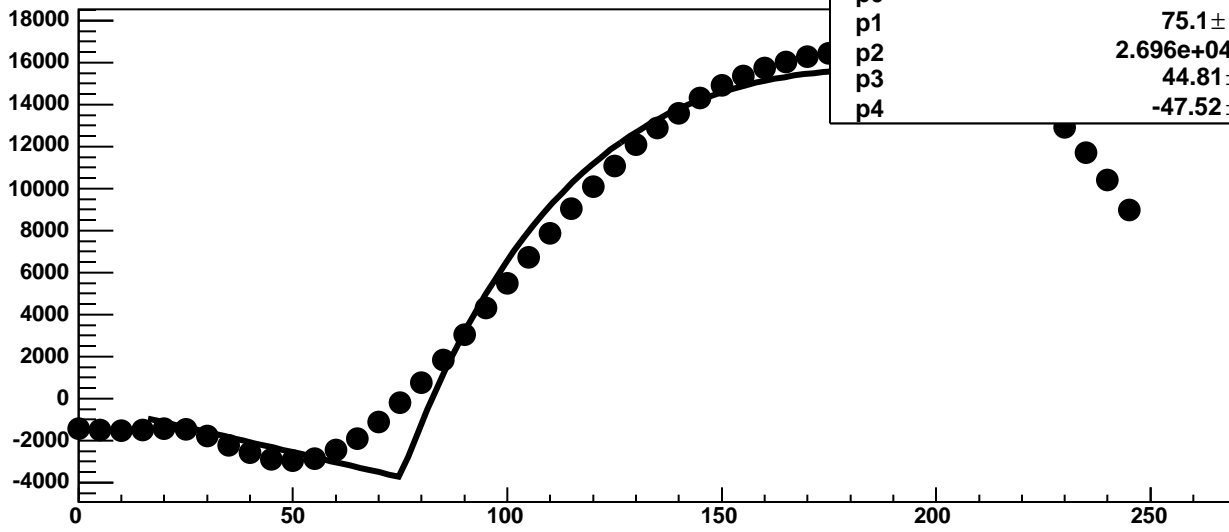
Chip 7, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold

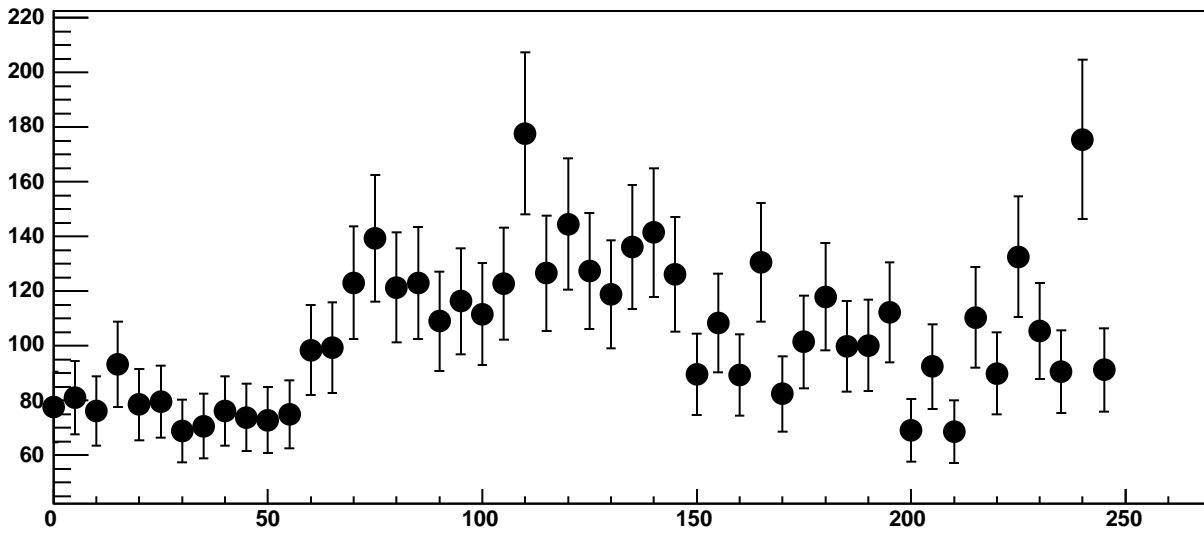


Chip 7, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

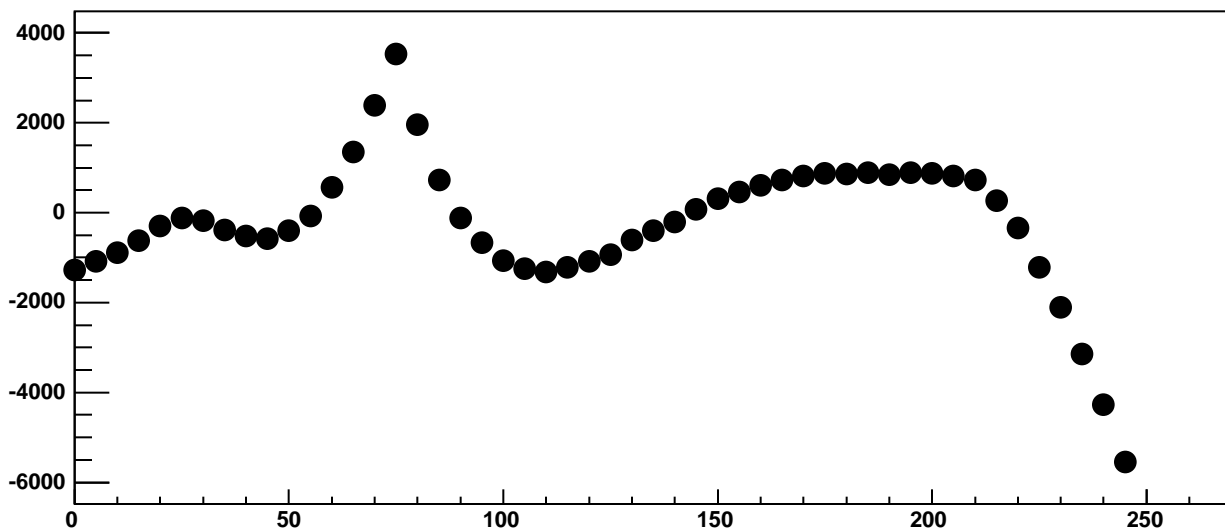


$\chi^2 / \text{ndf}$	1.043e+05 / 41
p0	-3745 ± 9.522
p1	75.1 ± 0.04148
p2	2.696e+04 ± 53.59
p3	44.81 ± 0.1083
p4	-47.52 ± 0.2617

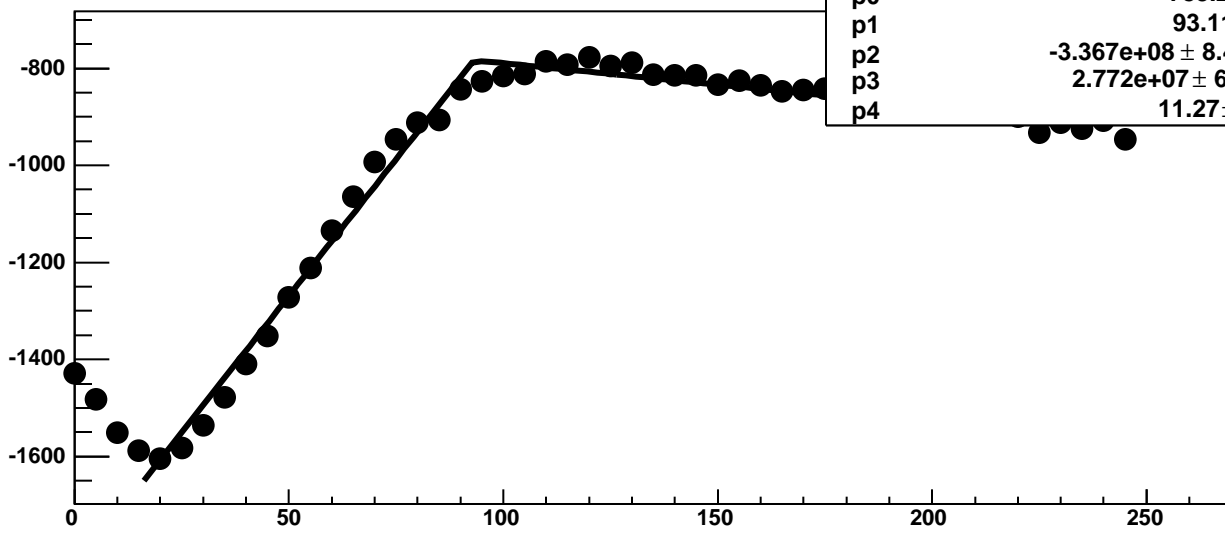
Chip 7, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

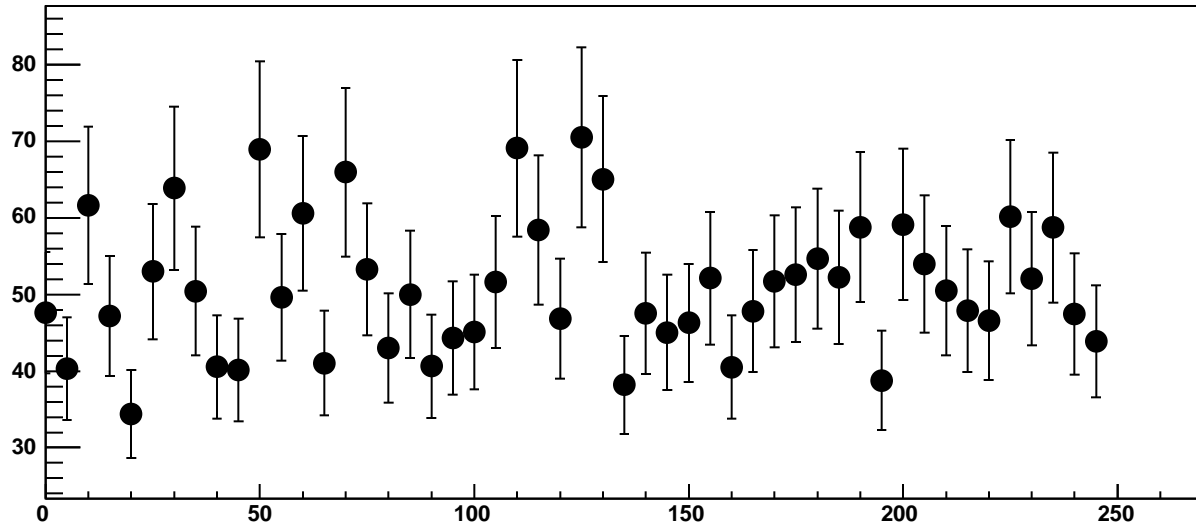


Chip 7, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

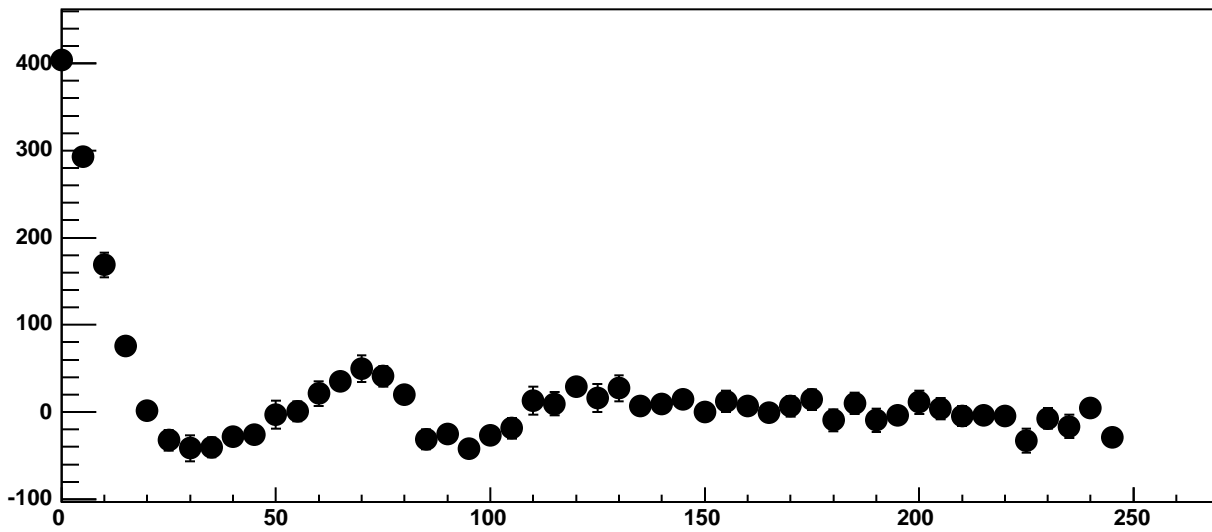


$\chi^2 / \text{ndf}$	208.5 / 41
p0	-783.2 ± 3.943
p1	93.11 ± 0.566
p2	-3.367e+08 ± 8.455e+06
p3	2.772e+07 ± 6.15e+05
p4	11.27 ± 0.1124

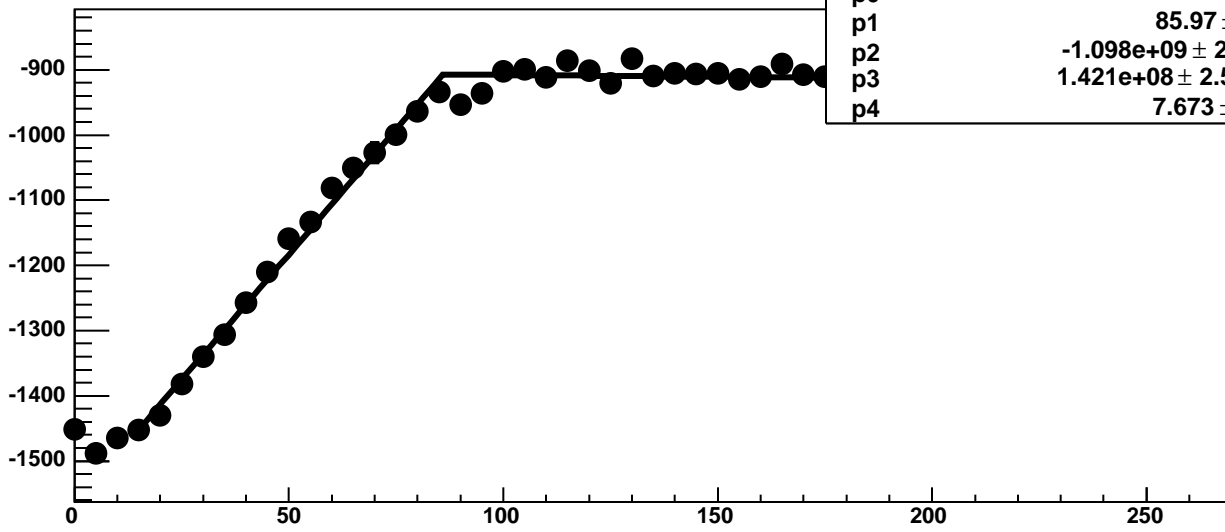
Chip 7, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

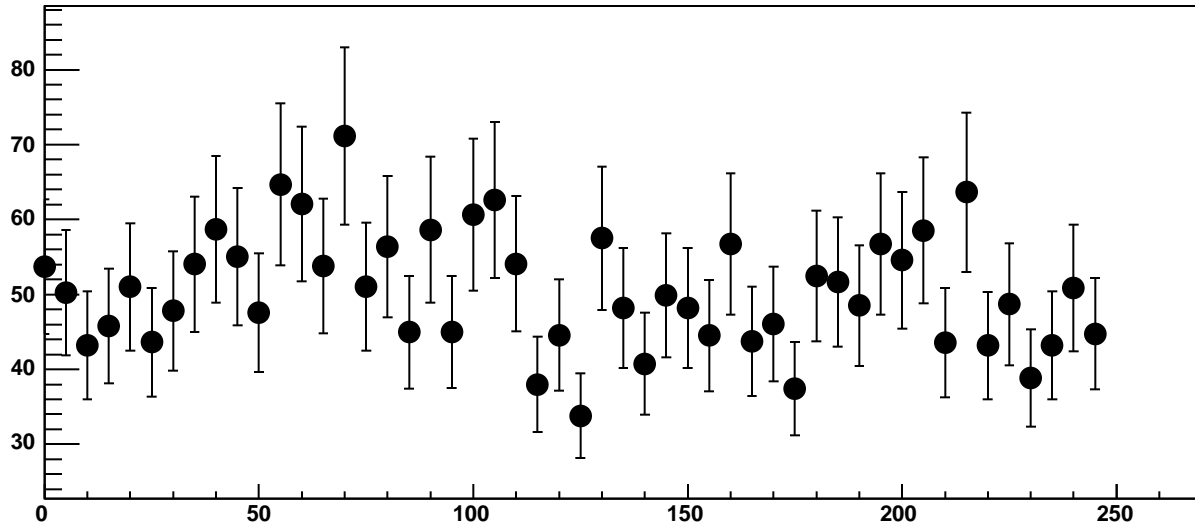


Chip 7, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold

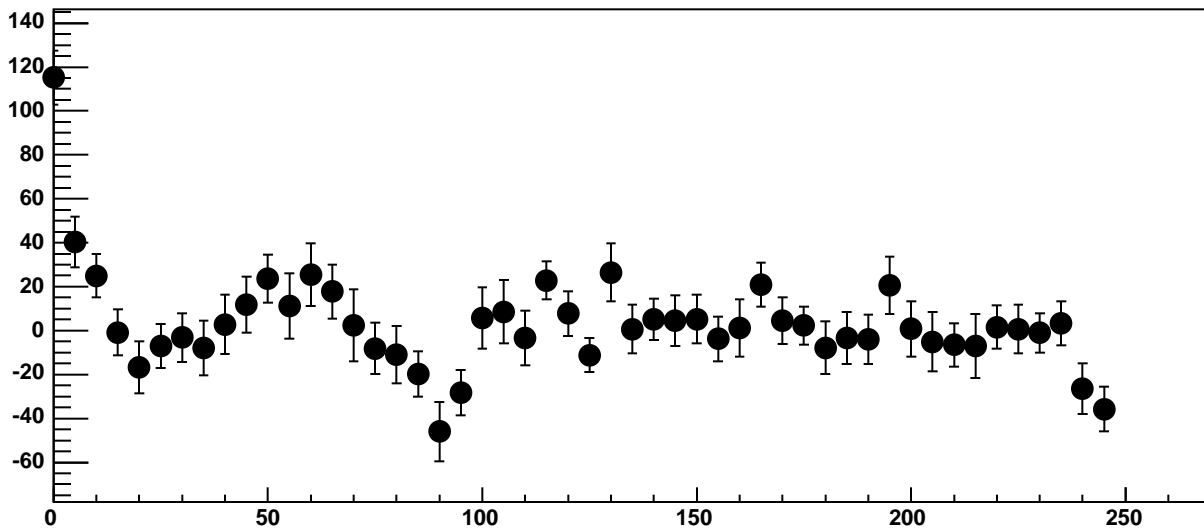


$\chi^2 / \text{ndf}$	67.41 / 41
p0	-907.2 ± 3.979
p1	85.97 ± 0.9277
p2	-1.098e+09 ± 2.03e+07
p3	1.421e+08 ± 2.578e+05
p4	7.673 ± 0.1354

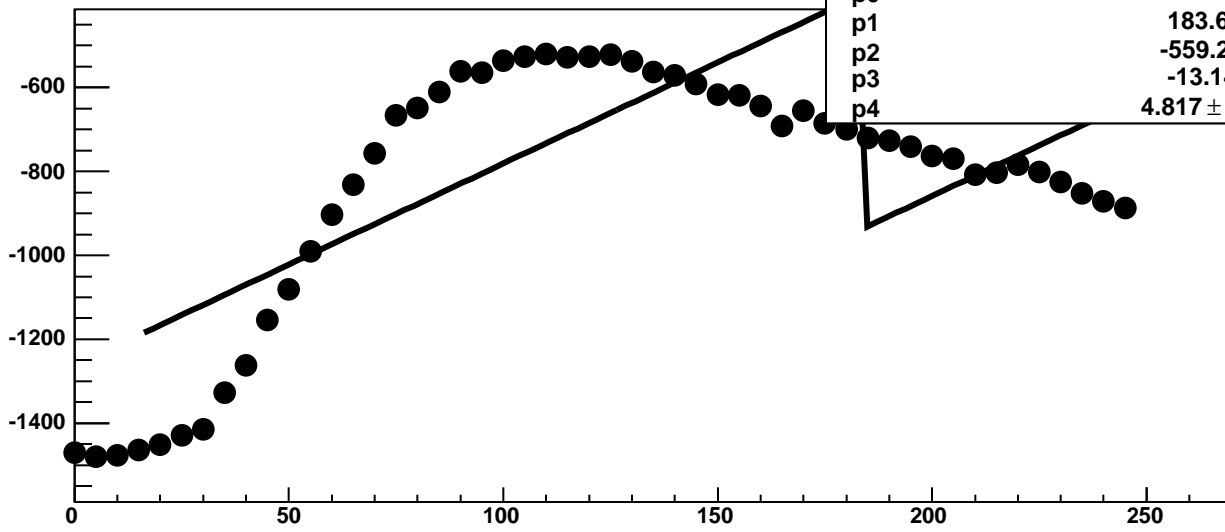
Chip 7, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



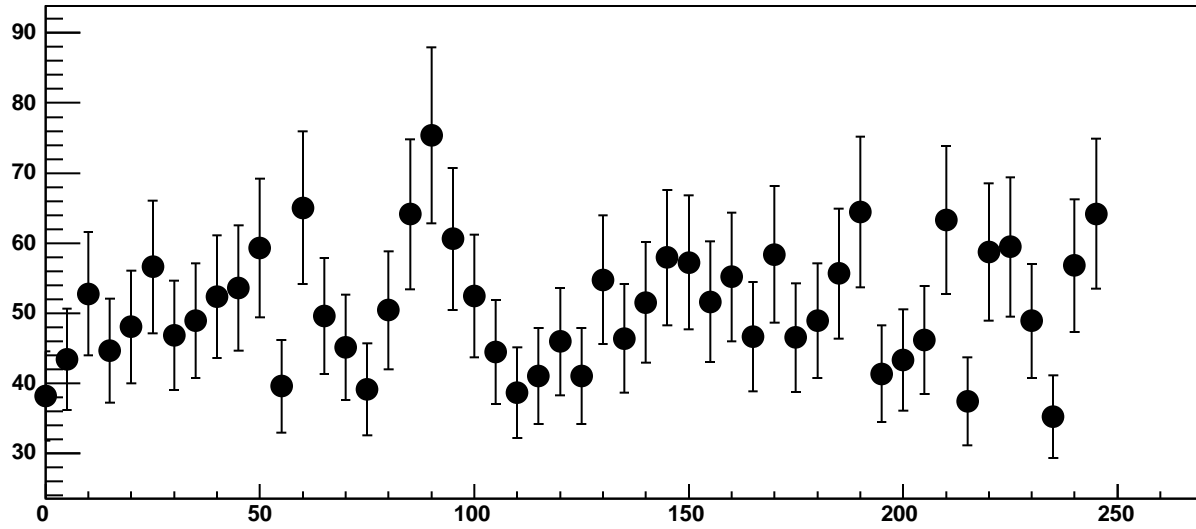
Chip 7, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold



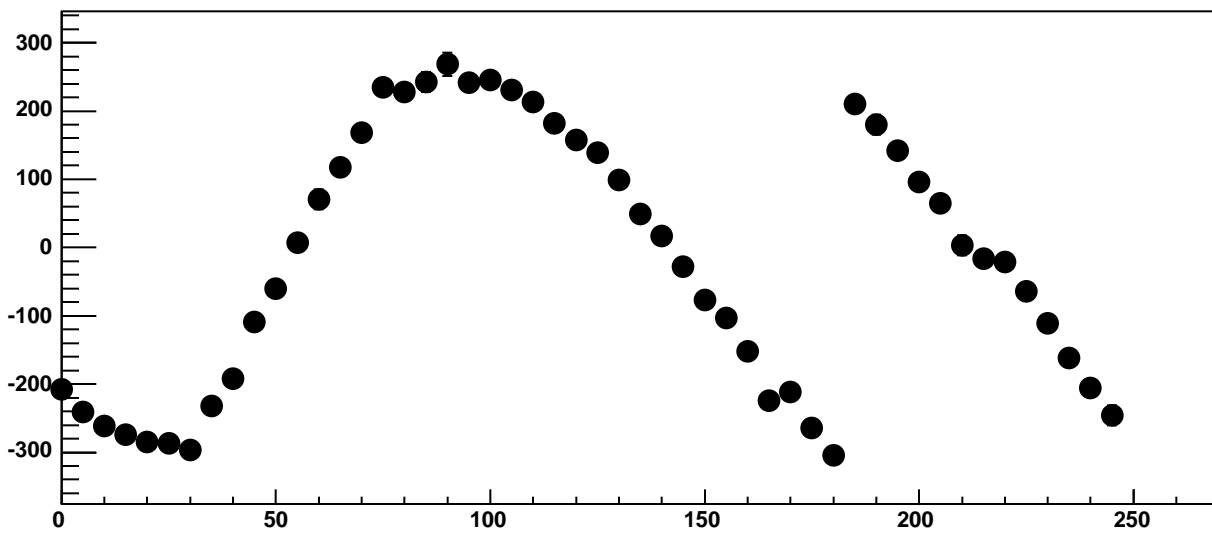
Chip 7, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold



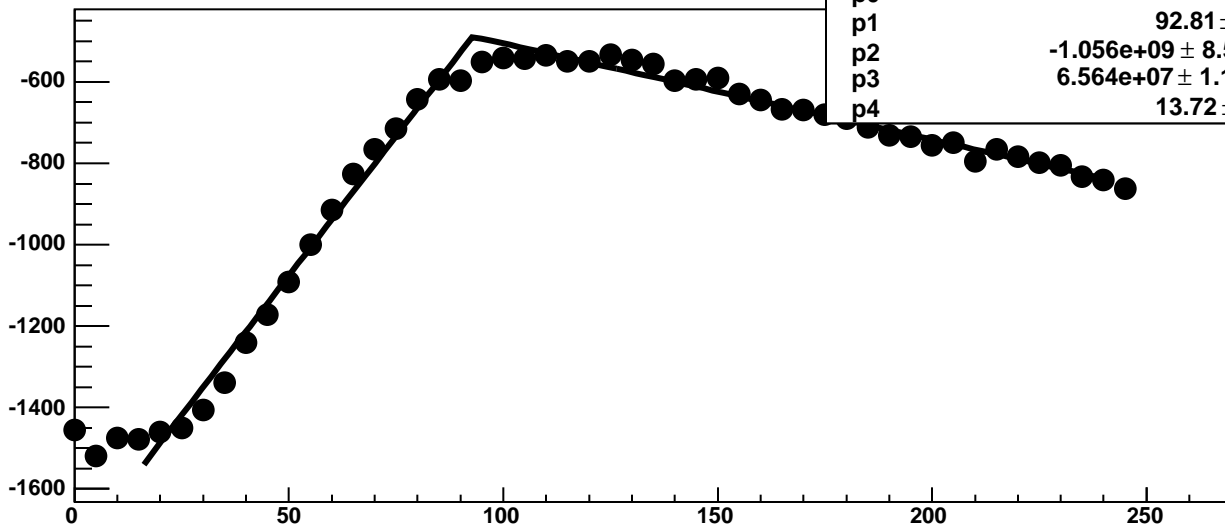
Chip 7, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

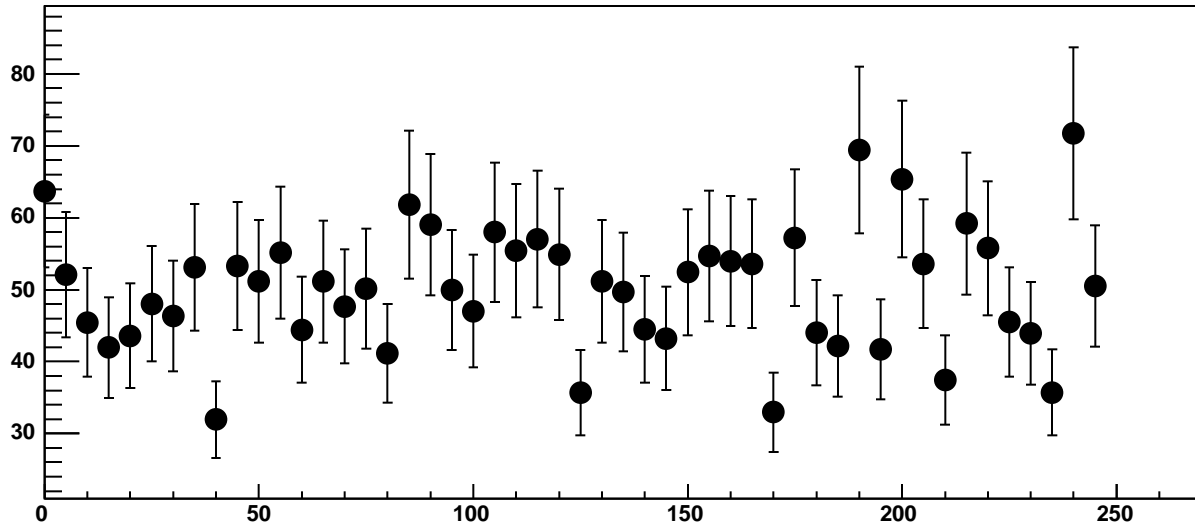


Chip 7, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

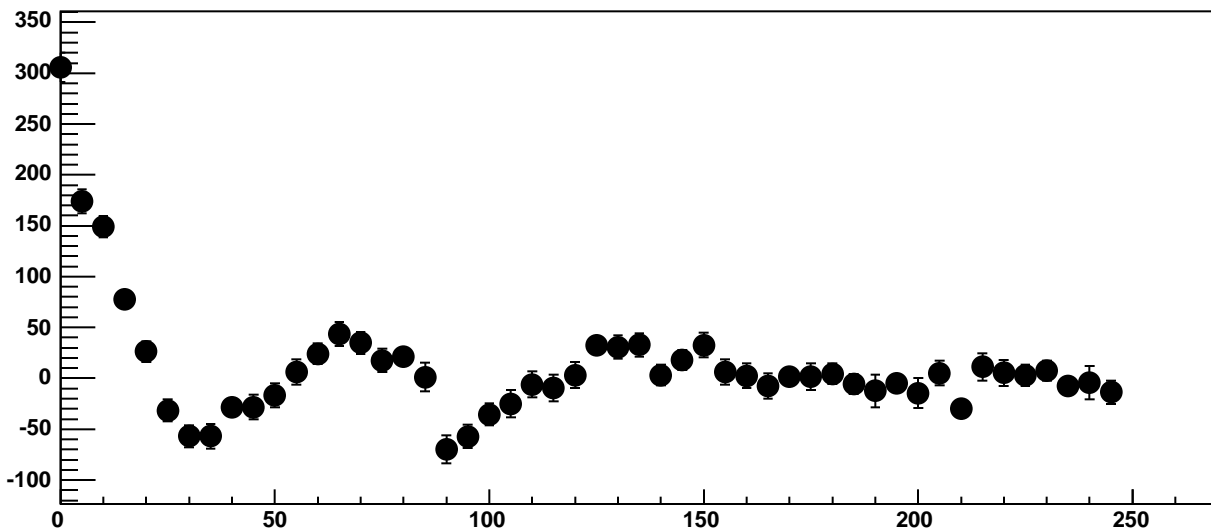


$\chi^2 / \text{ndf}$	315.7 / 41
p0	$-488.2 \pm 3.6$
p1	$92.81 \pm 0.4435$
p2	$-1.056e+09 \pm 8.588e+06$
p3	$6.564e+07 \pm 1.141e+05$
p4	$13.72 \pm 0.1196$

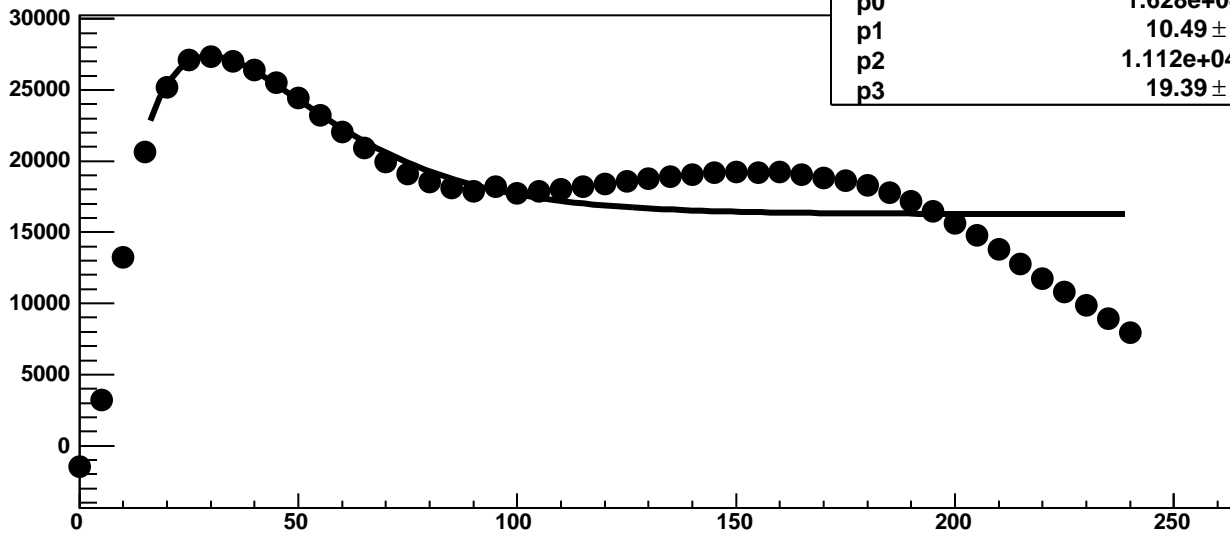
Chip 7, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

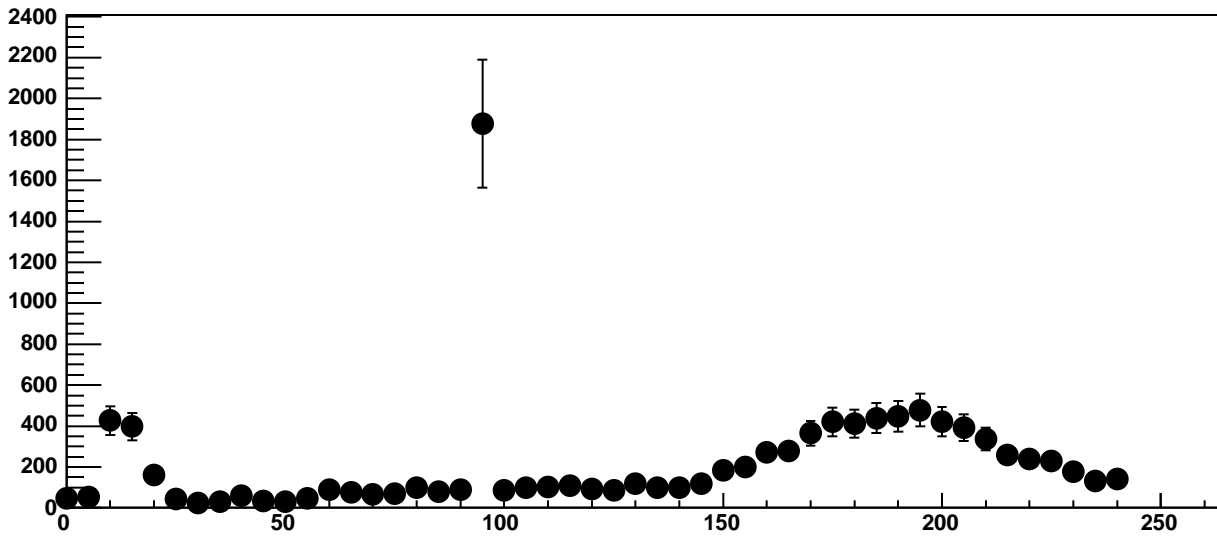


Chip 7, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold

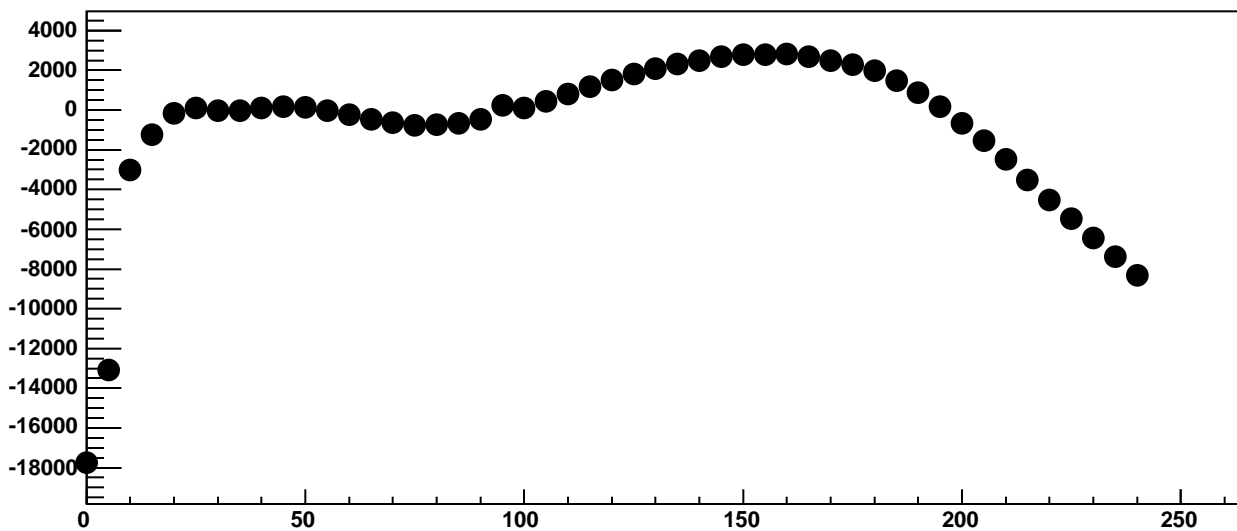


$\chi^2 / \text{ndf}$	2.525e+05 / 42
p0	1.628e+04 $\pm$ 8.51
p1	10.49 $\pm$ 0.05649
p2	1.112e+04 $\pm$ 8.581
p3	19.39 $\pm$ 0.03602

Chip 7, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

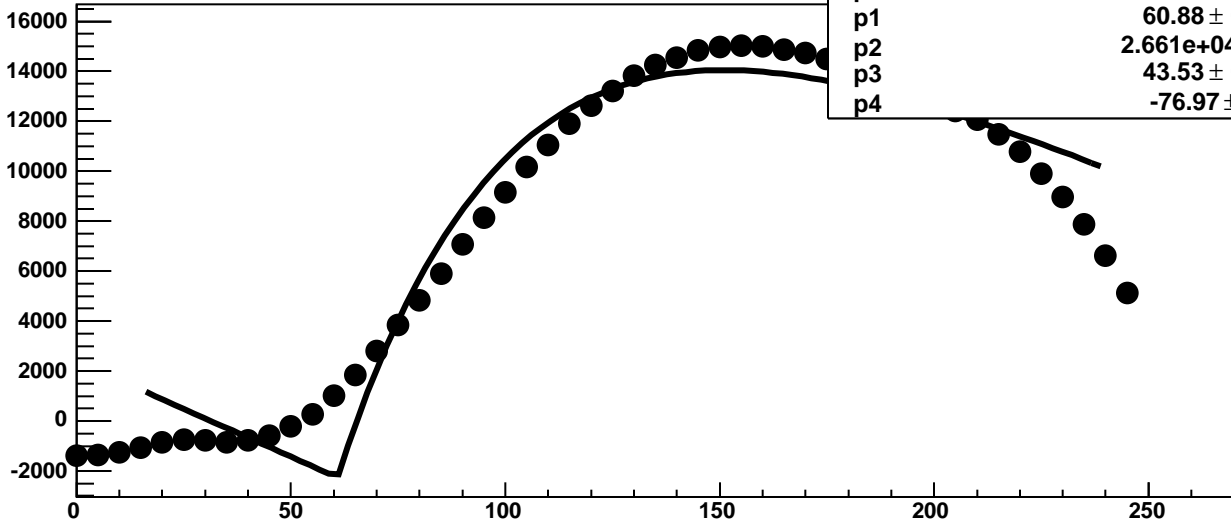


Chip 7, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold

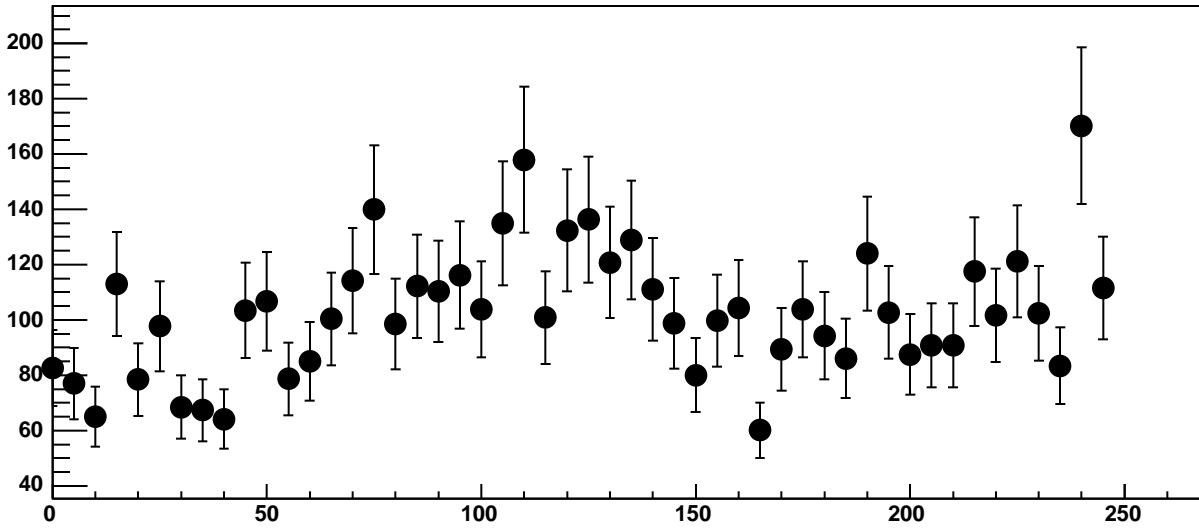




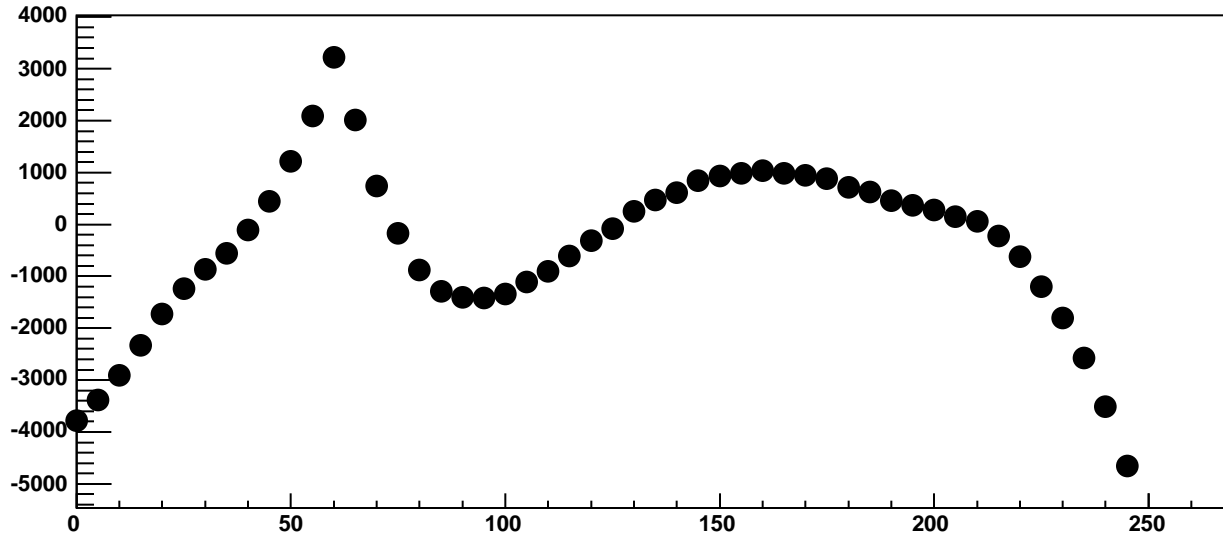
Chip 7, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold



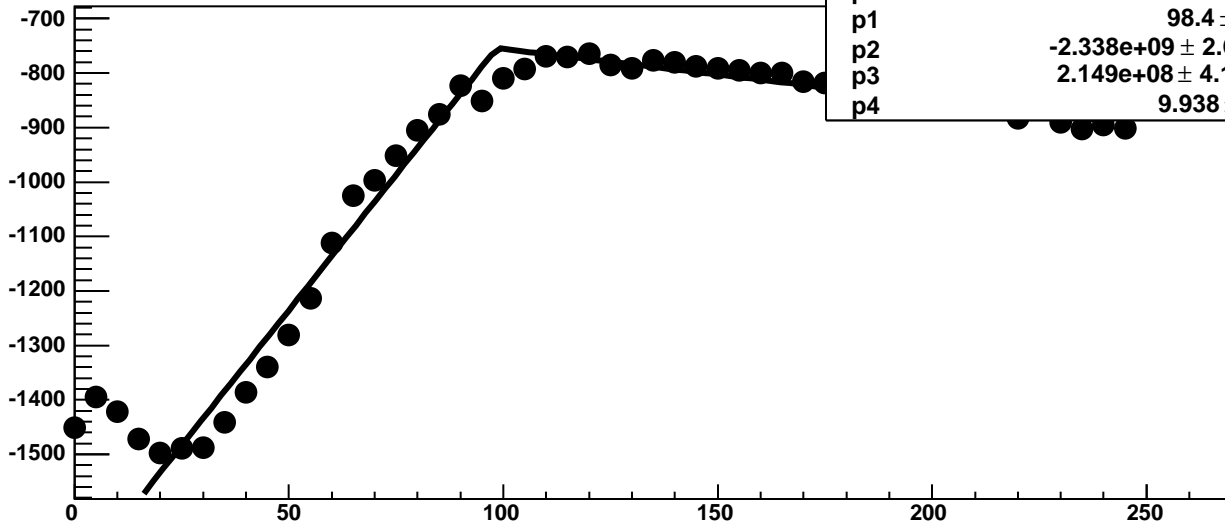
Chip 7, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold

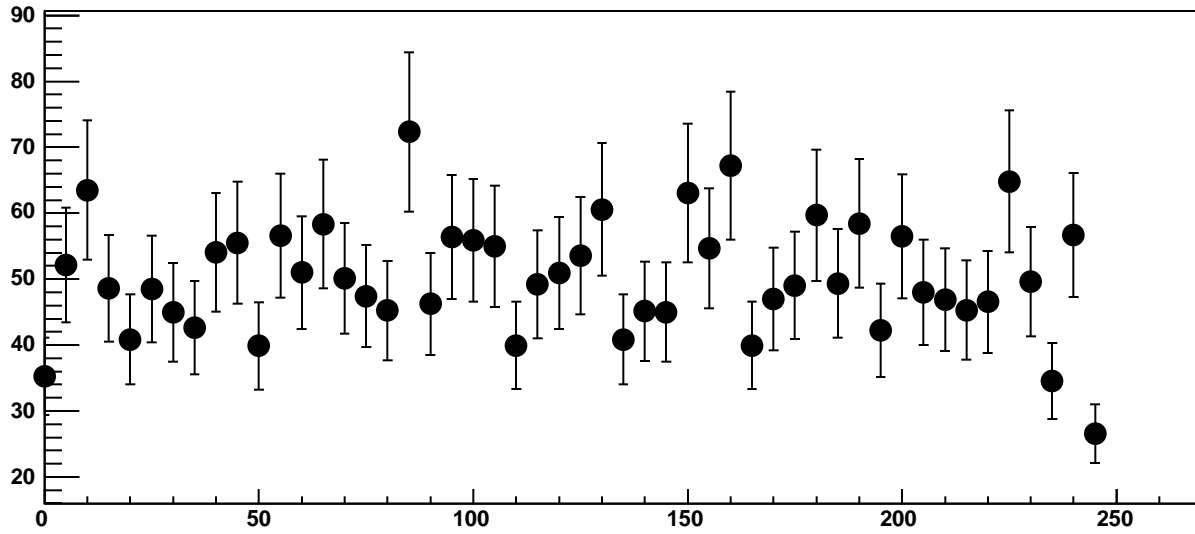


Chip 7, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

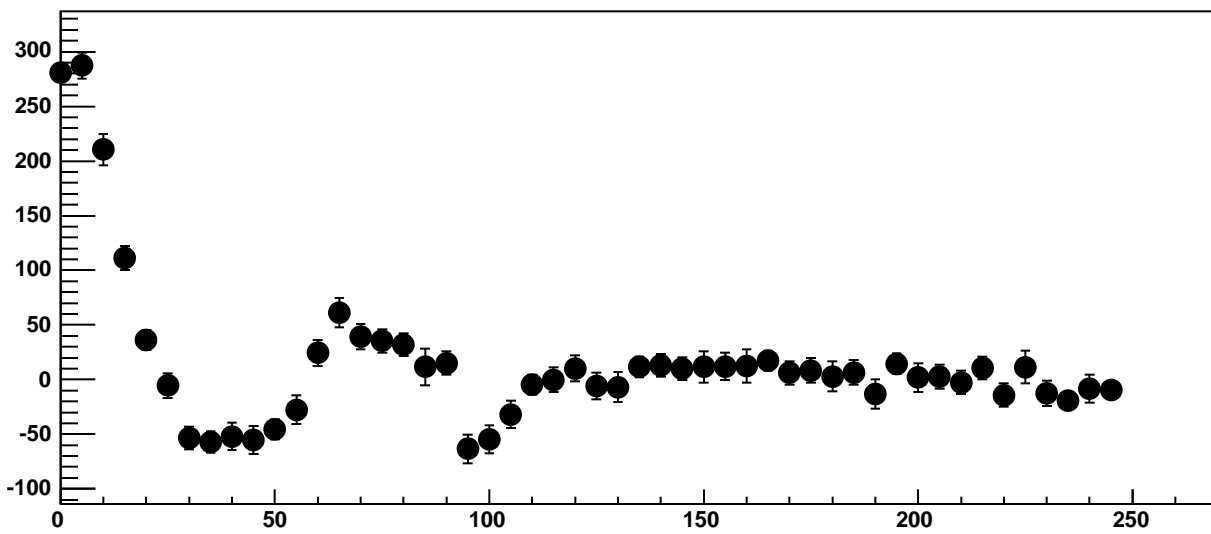


$\chi^2 / \text{ndf}$	377.2 / 41
p0	-754.2 ± 3.848
p1	98.4 ± 0.6566
p2	-2.338e+09 ± 2.625e+07
p3	2.149e+08 ± 4.123e+05
p4	9.938 ± 0.1113

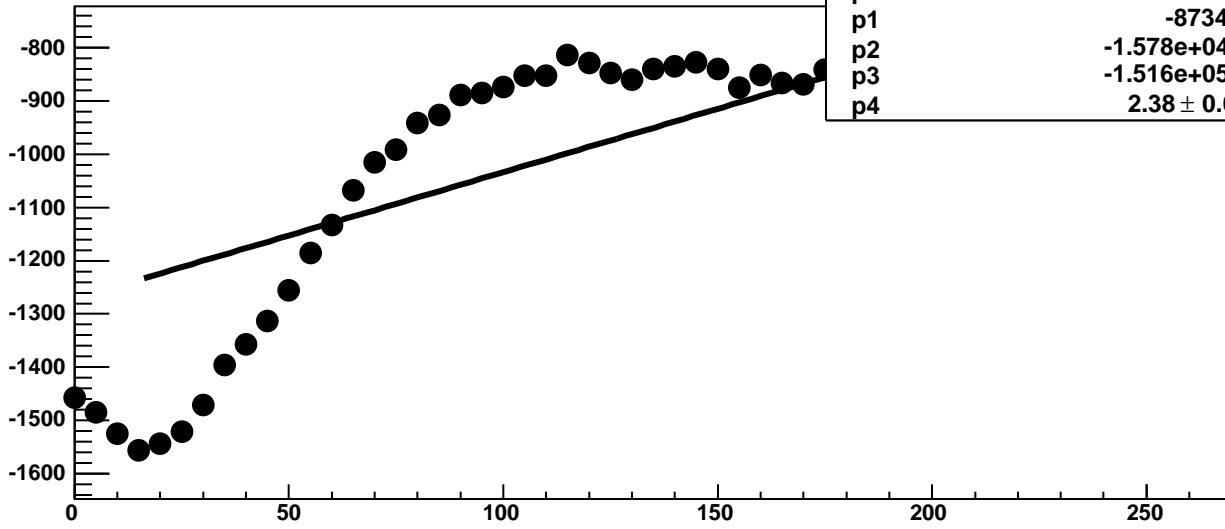
Chip 7, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

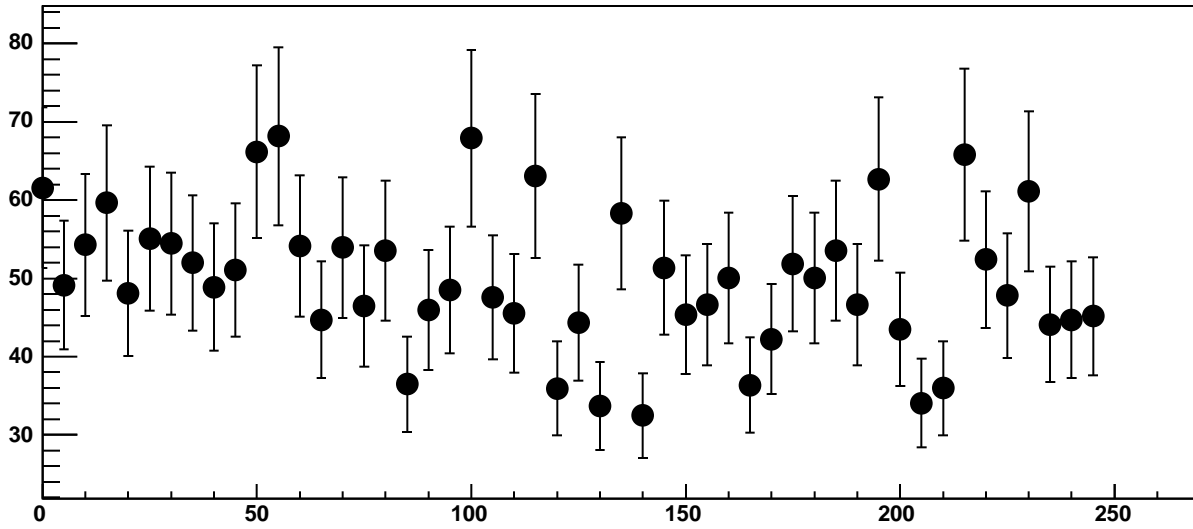


Chip 7, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

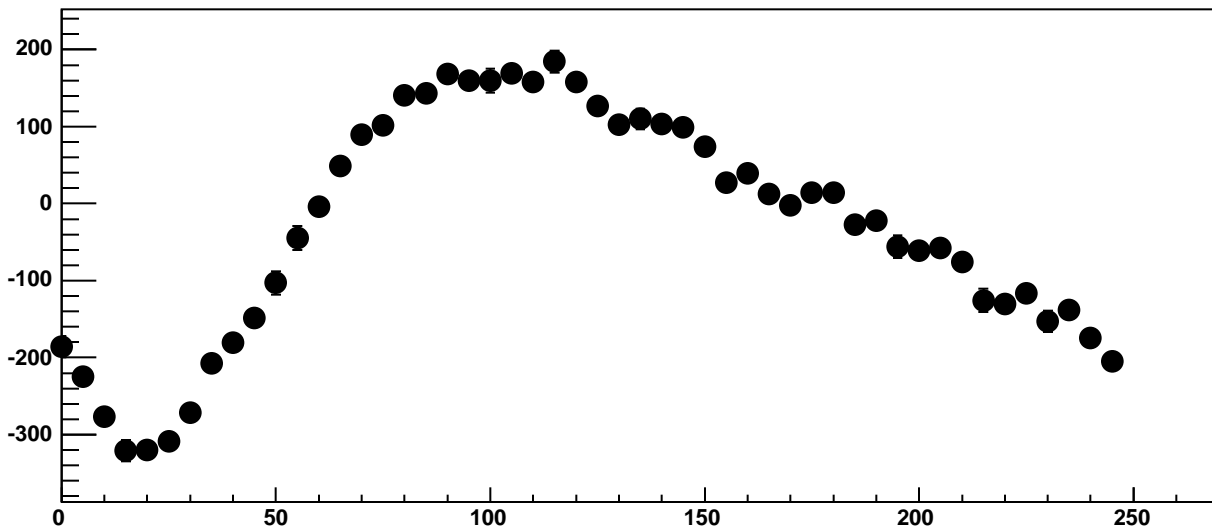


$\chi^2 / \text{ndf}$	7220 / 41
p0	$-6274 \pm 8.092$
p1	$-8734 \pm 2.844$
p2	$-1.578\text{e}+04 \pm 10.17$
p3	$-1.516\text{e}+05 \pm 350.4$
p4	$2.38 \pm 0.0009125$

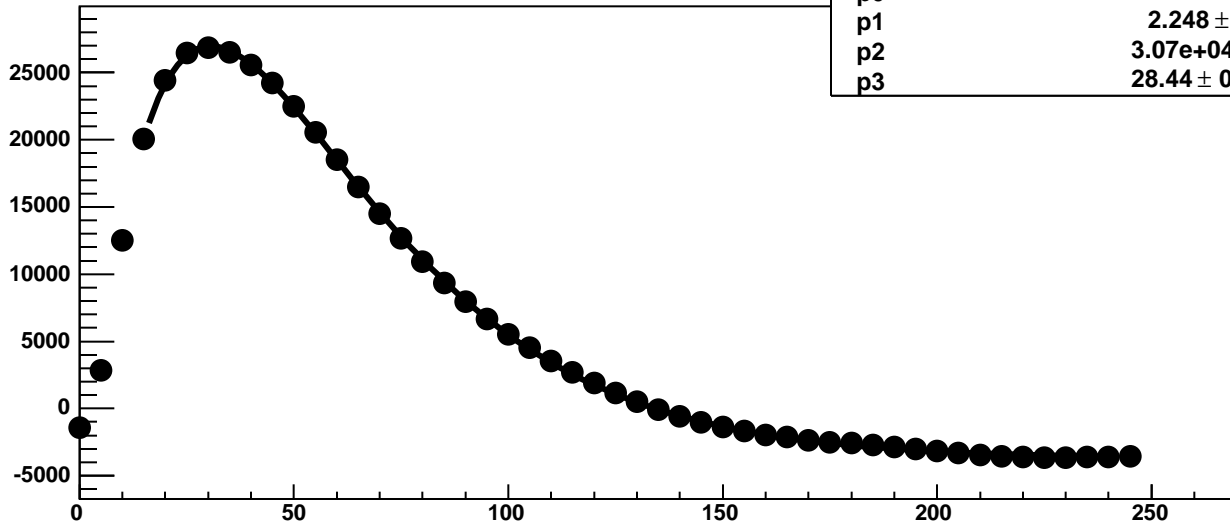
Chip 7, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

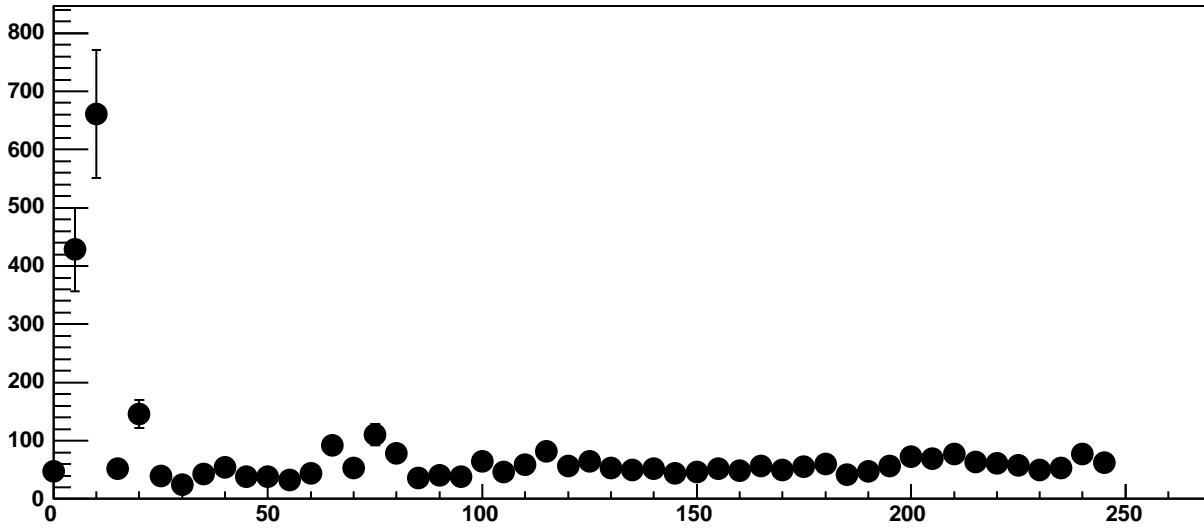


Chip 7, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold

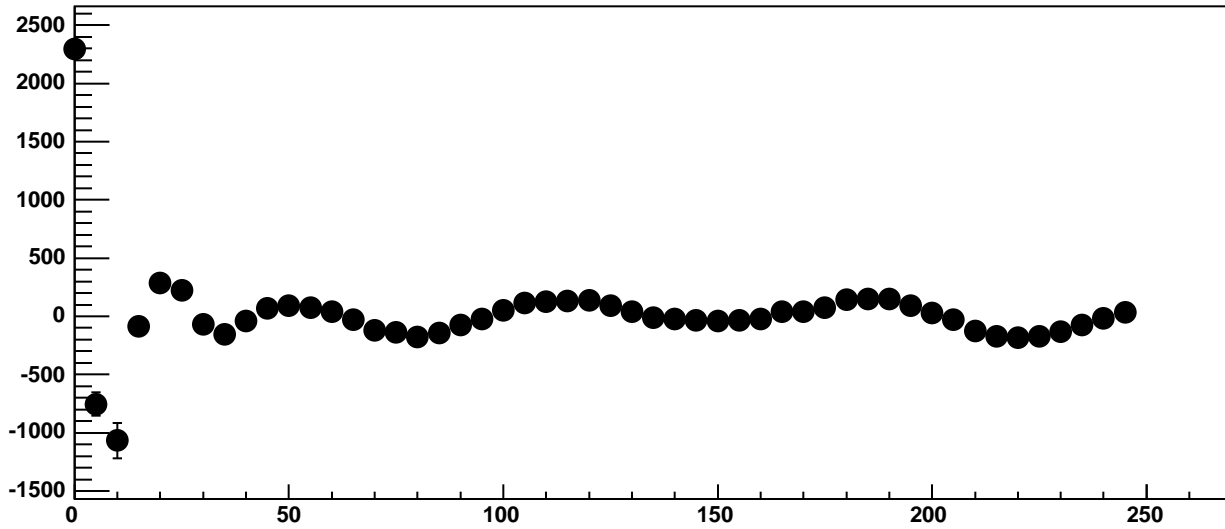


$\chi^2 / \text{ndf}$	3833 / 42
p0	-3741 ± 3.517
p1	2.248 ± 0.01341
p2	3.07e+04 ± 4.454
p3	28.44 ± 0.008898

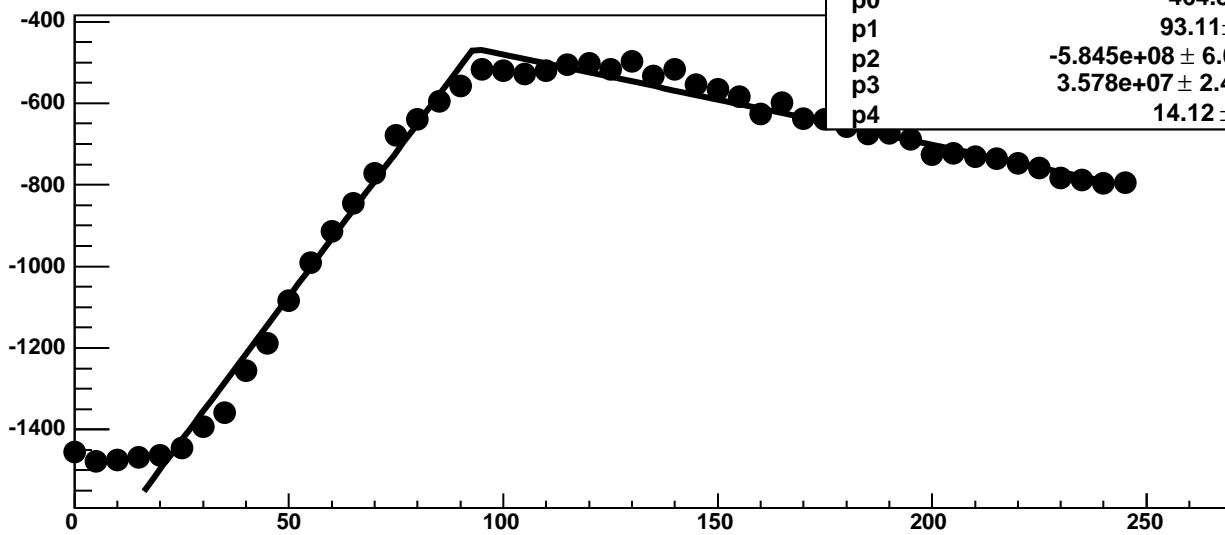
Chip 7, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold

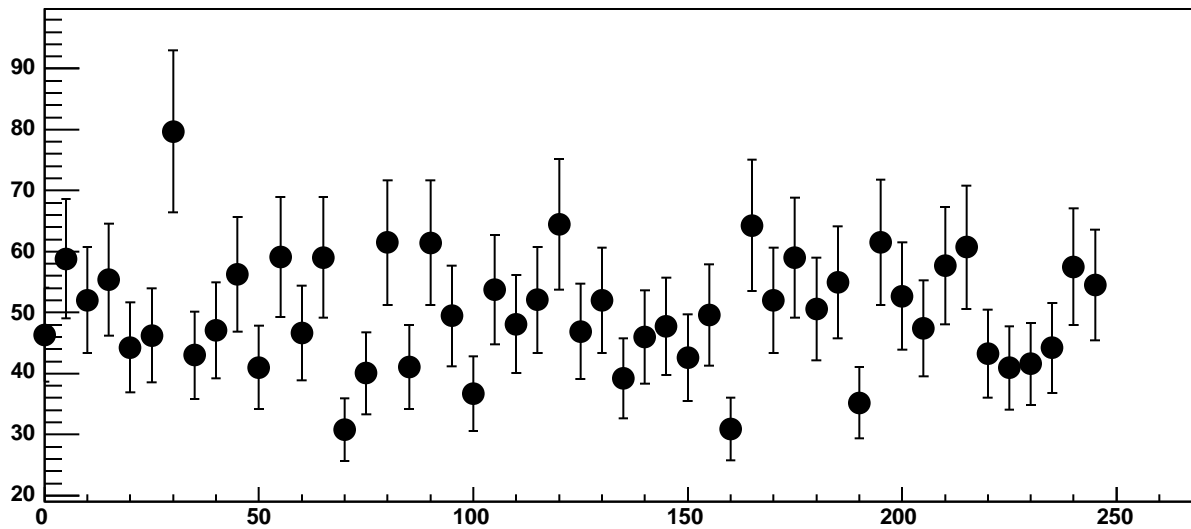


Chip 7, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

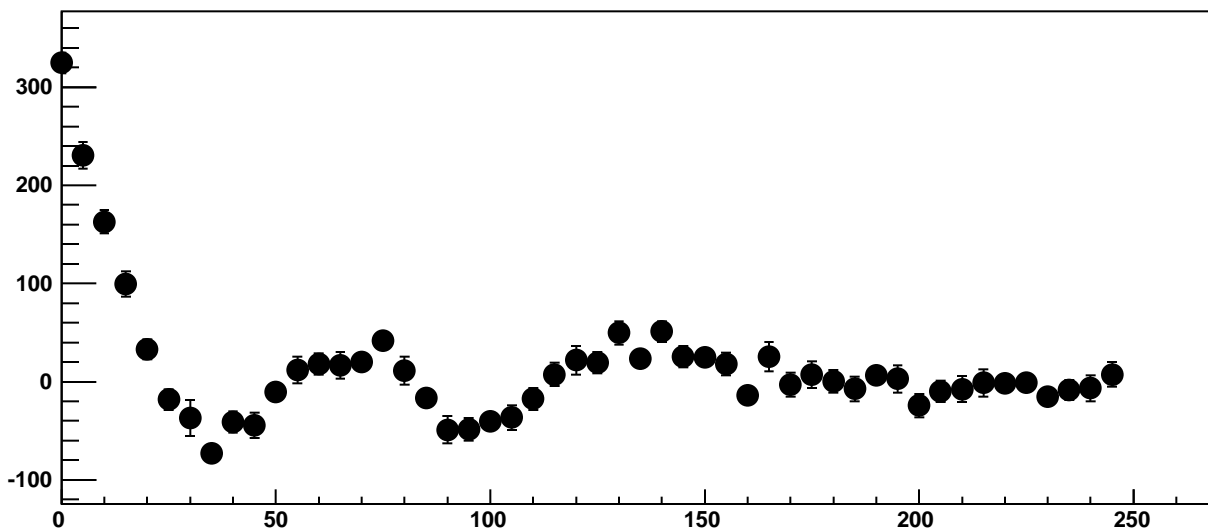


$\chi^2 / \text{ndf}$	348.3 / 41
p0	$-464.8 \pm 3.446$
p1	$93.11 \pm 0.4097$
p2	$-5.845e+08 \pm 6.078e+06$
p3	$3.578e+07 \pm 2.437e+05$
p4	$14.12 \pm 0.1214$

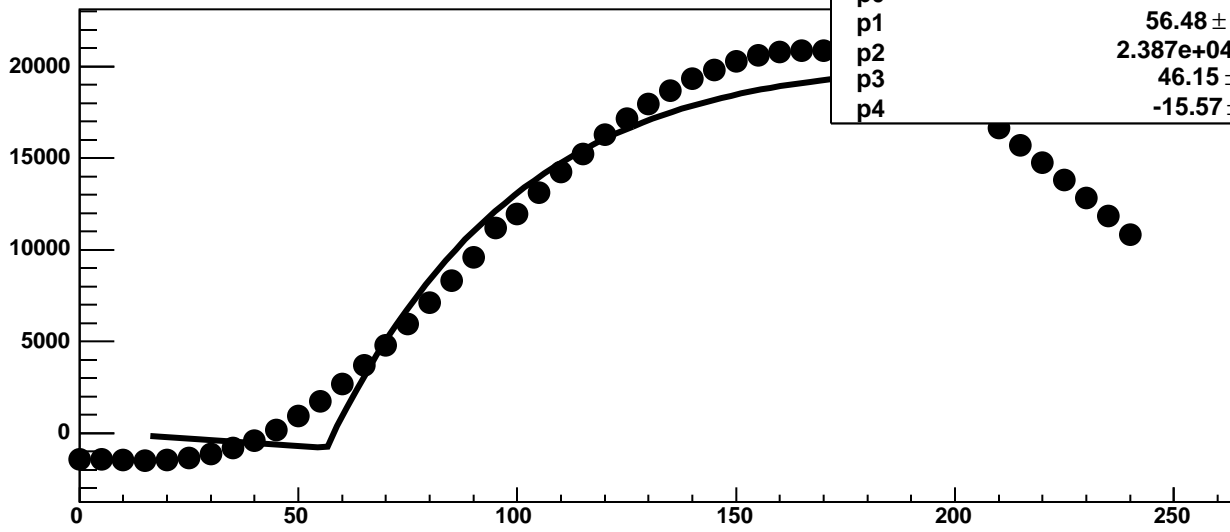
Chip 7, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

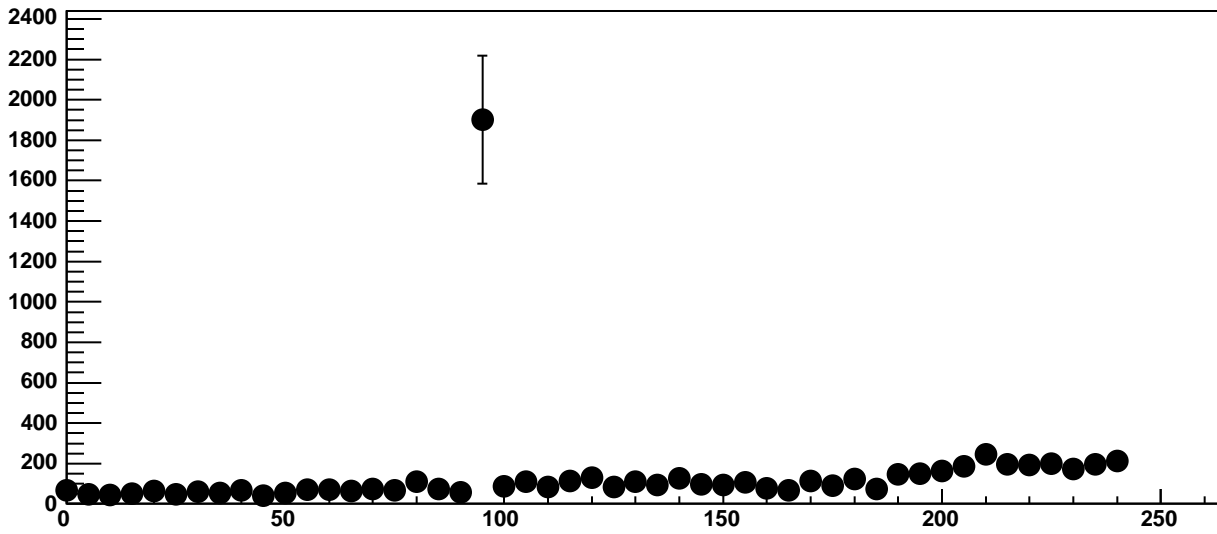


Chip 7, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

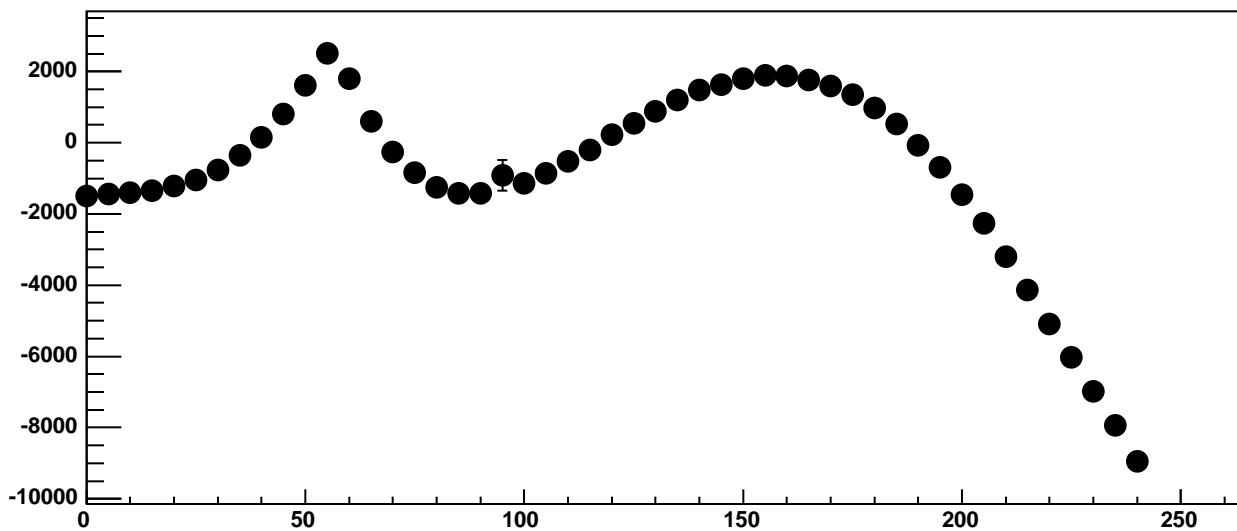


$\chi^2 / \text{ndf}$	3.262e+05 / 41
p0	-805 ± 6.369
p1	56.48 ± 0.02674
p2	2.387e+04 ± 42.89
p3	46.15 ± 0.0886
p4	-15.57 ± 0.2328

Chip 7, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold

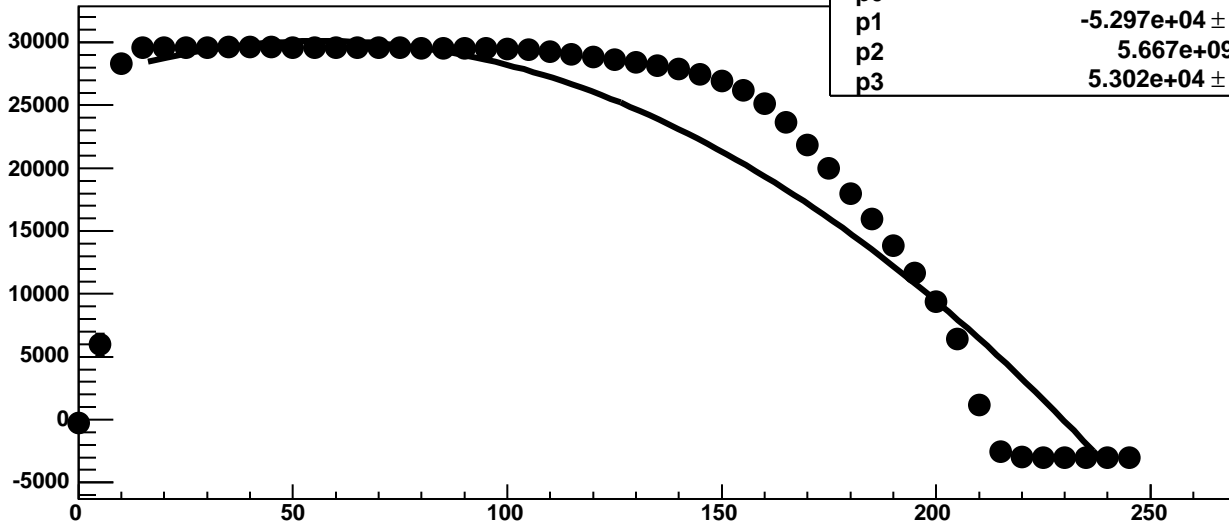


Chip 7, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

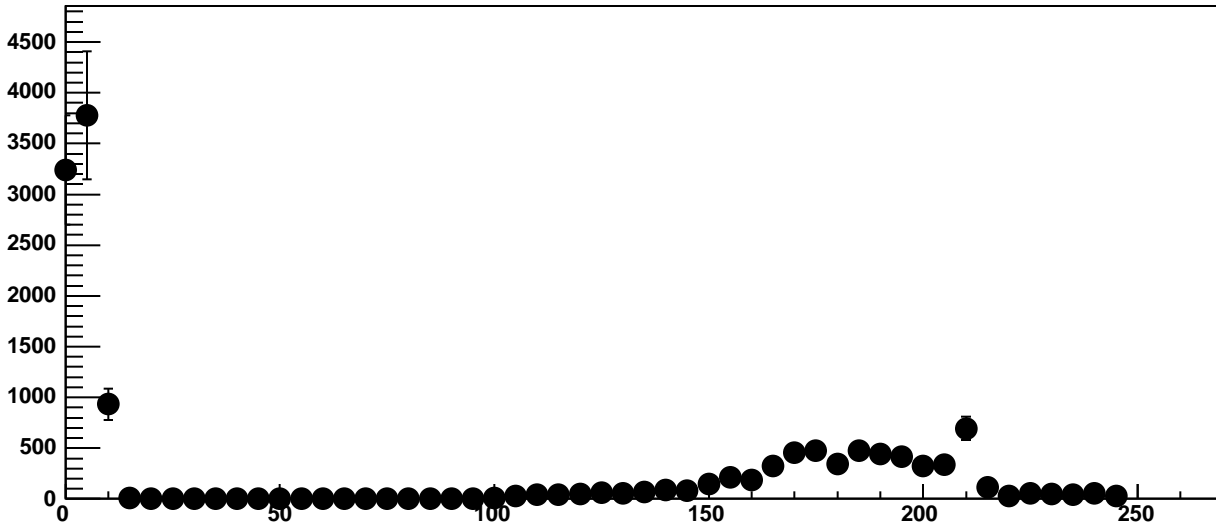


Chip 7, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

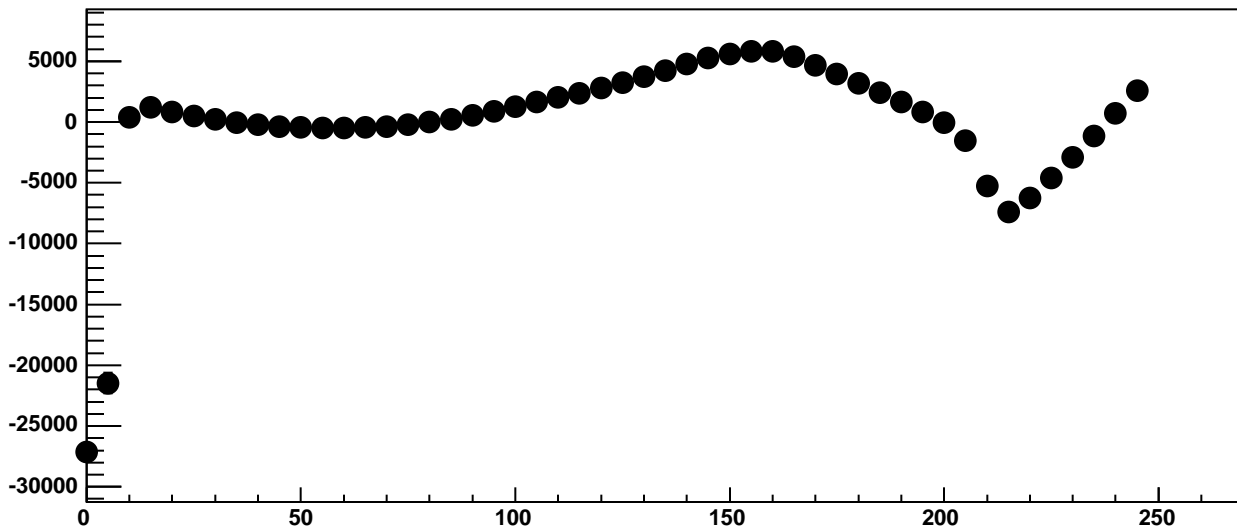
$\chi^2 / \text{ndf}$	6.943e+06 / 42
p0	-5.667e+09 $\pm$ 3.067
p1	-5.297e+04 $\pm$ 0.05376
p2	5.667e+09 $\pm$ 3.067
p3	5.302e+04 $\pm$ 0.05373



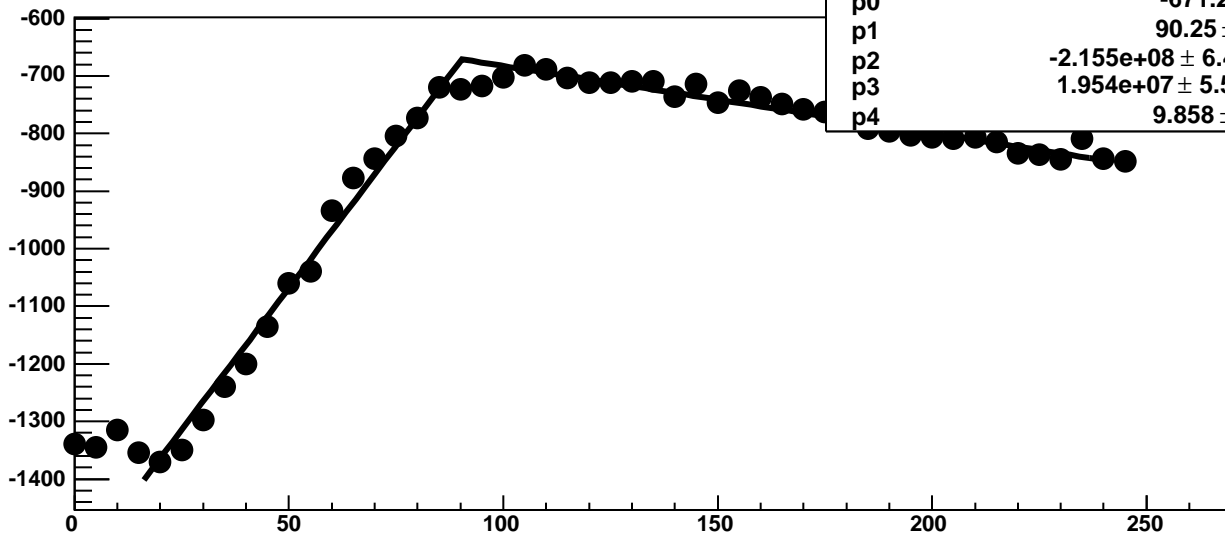
Chip 7, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

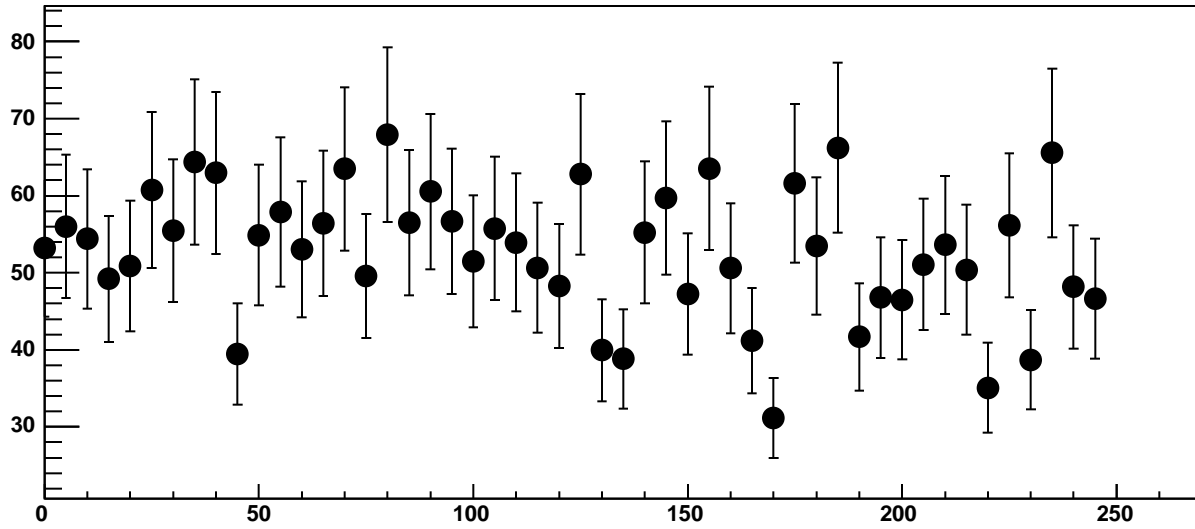


Chip 7, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

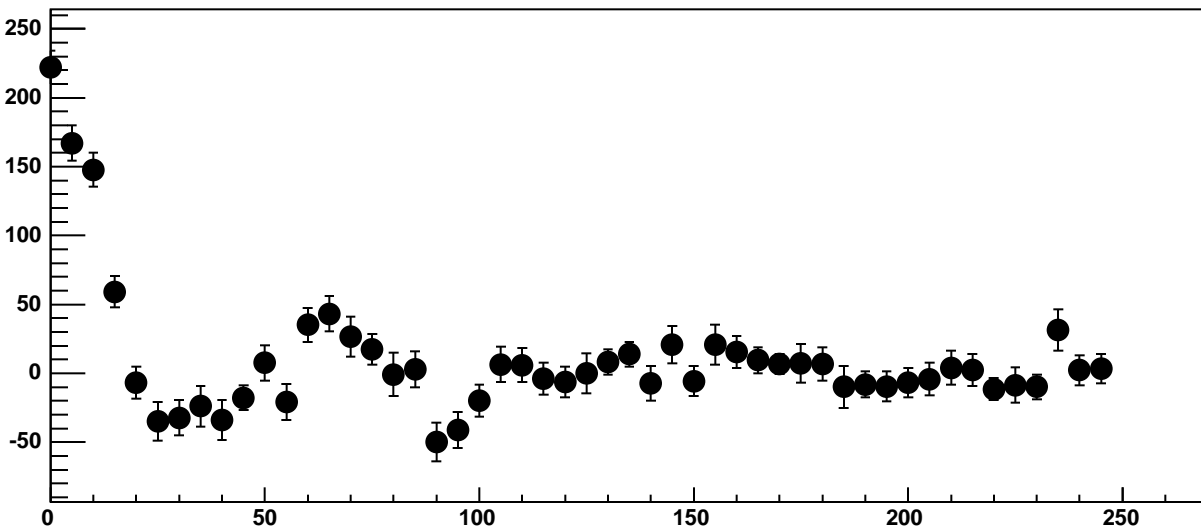


$\chi^2 / \text{ndf}$	130.4 / 41
p0	$-671.2 \pm 3.927$
p1	$90.25 \pm 0.6928$
p2	$-2.155\text{e}+08 \pm 6.427\text{e}+06$
p3	$1.954\text{e}+07 \pm 5.522\text{e}+05$
p4	$9.858 \pm 0.1385$

Chip 7, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold

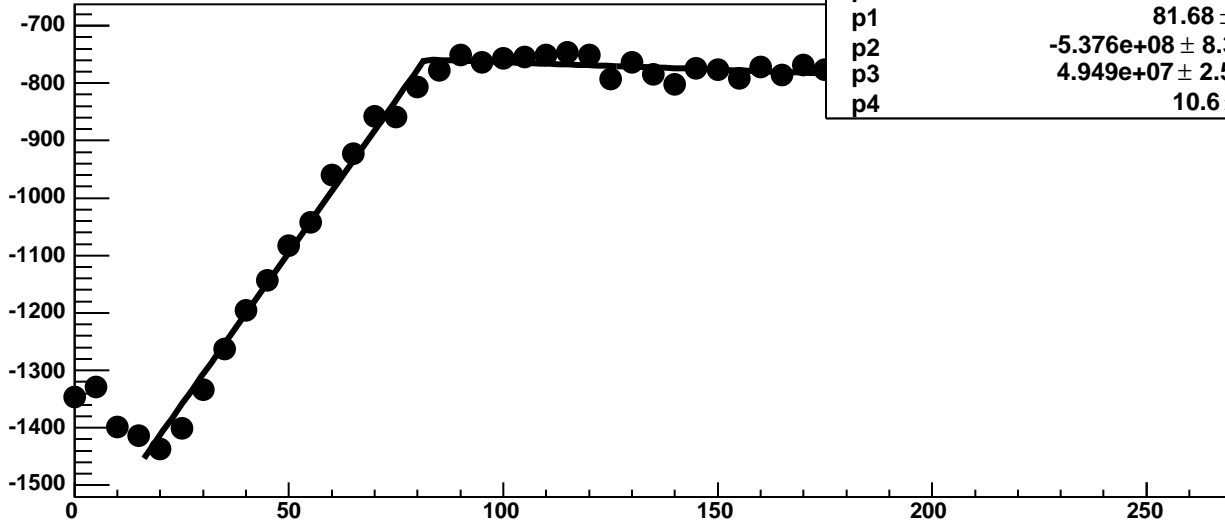


Chip 7, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold



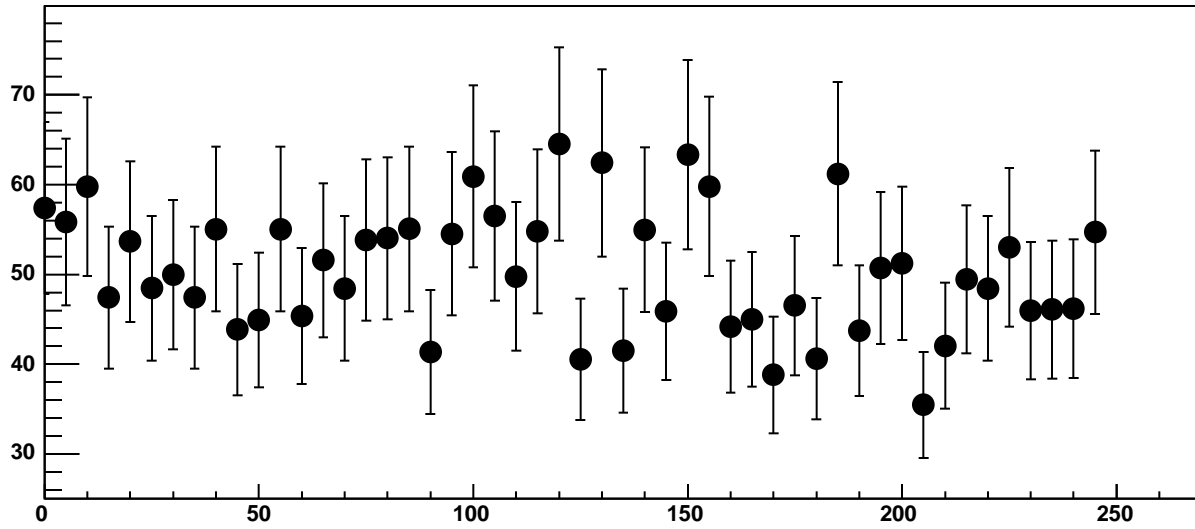


Chip 7, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

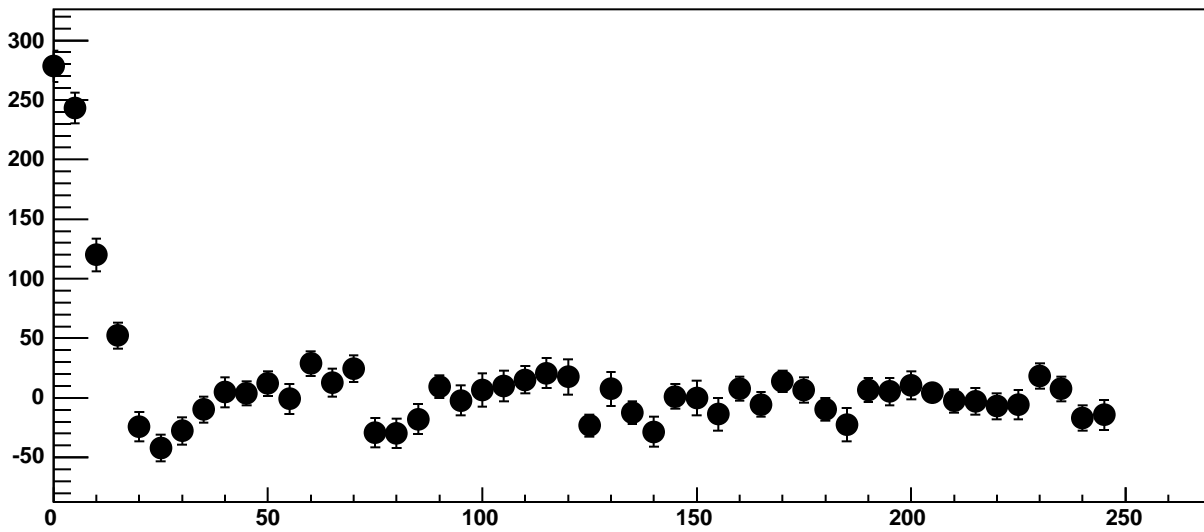


$\chi^2 / \text{ndf}$	114.2 / 41
p0	$-758.6 \pm 4.047$
p1	$81.68 \pm 0.6836$
p2	$-5.376\text{e}+08 \pm 8.312\text{e}+06$
p3	$4.949\text{e}+07 \pm 2.574\text{e}+05$
p4	$10.6 \pm 0.1541$

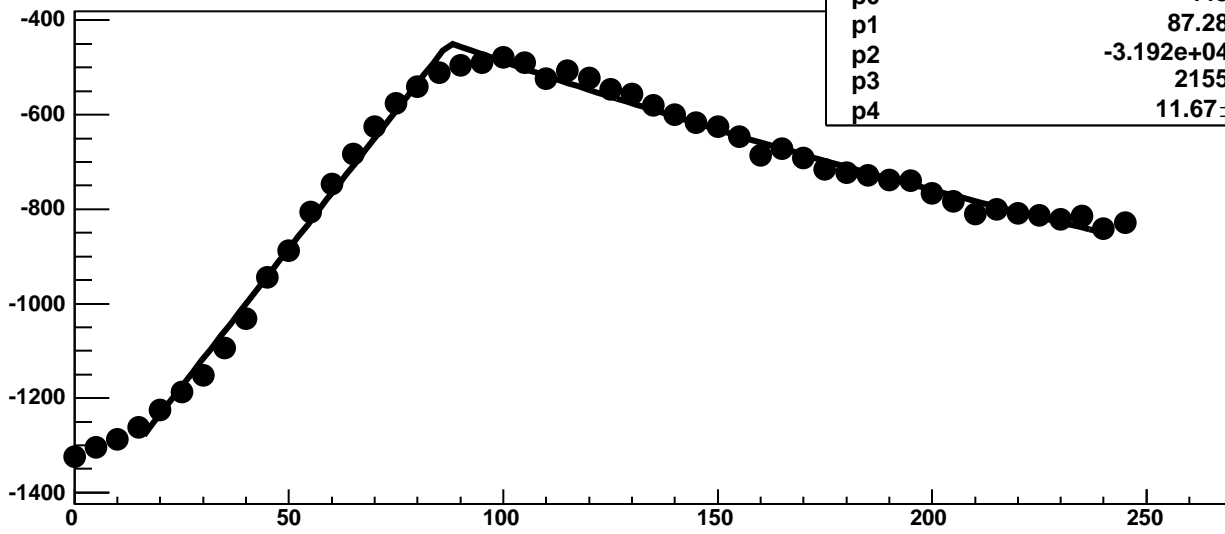
Chip 7, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

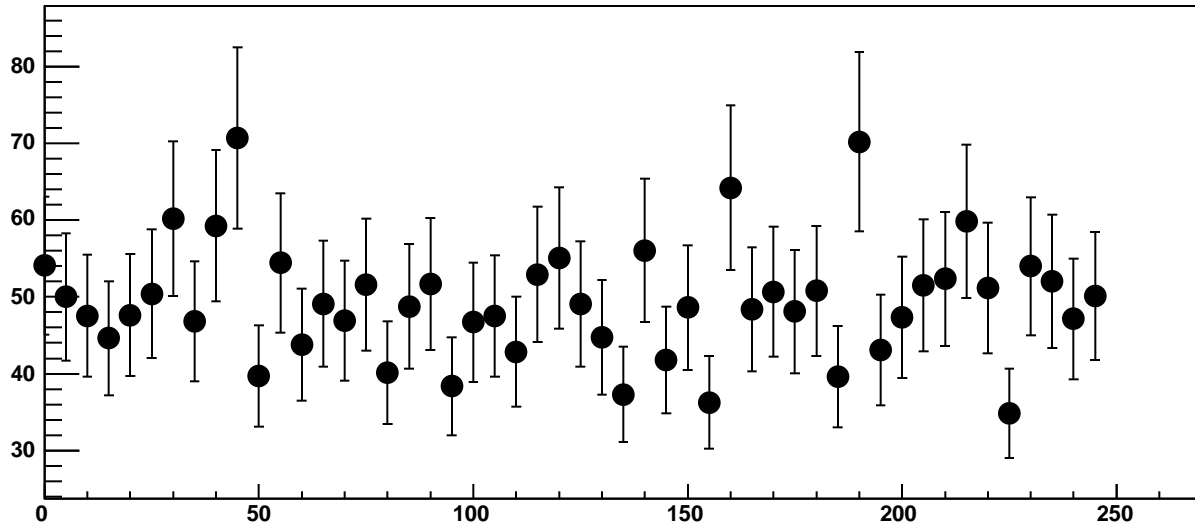


Chip 7, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold

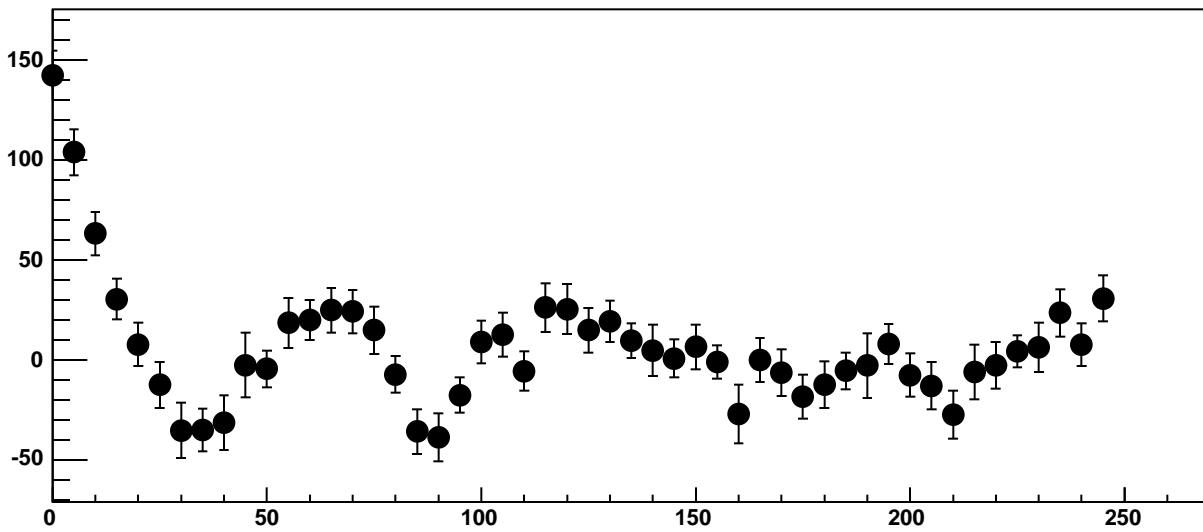


$\chi^2 / \text{ndf}$	115.3 / 41
p0	$-448 \pm 3.808$
p1	$87.28 \pm 0.477$
p2	$-3.192e+04 \pm 5710$
p3	$2155 \pm 398.9$
p4	$11.67 \pm 0.1295$

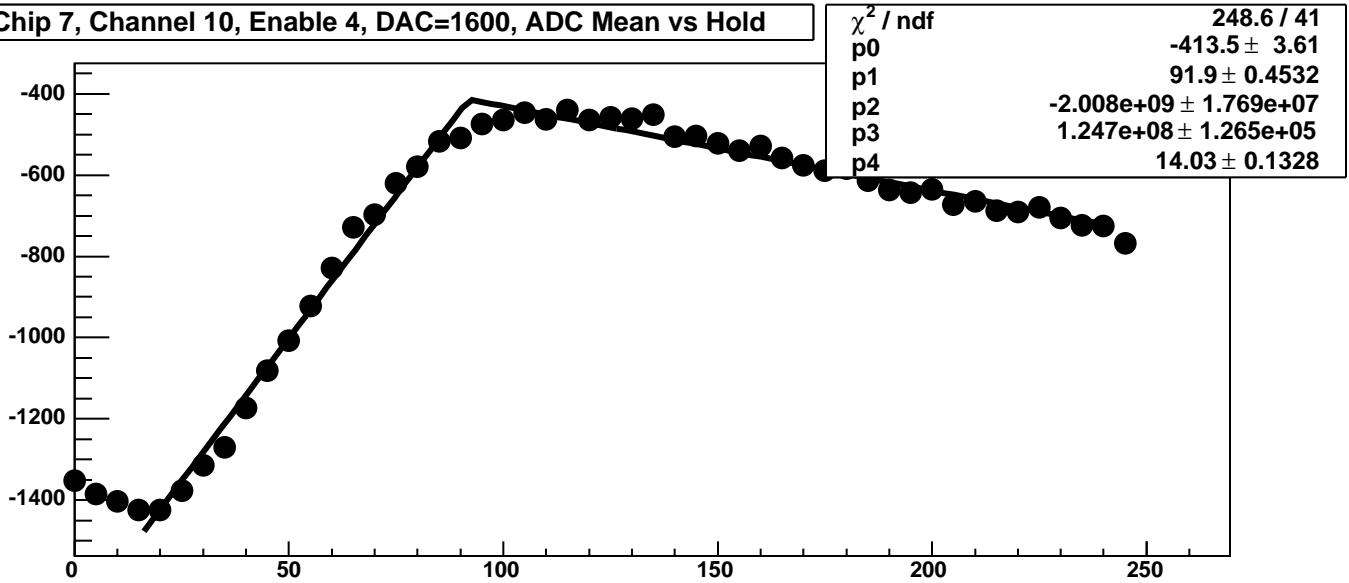
Chip 7, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



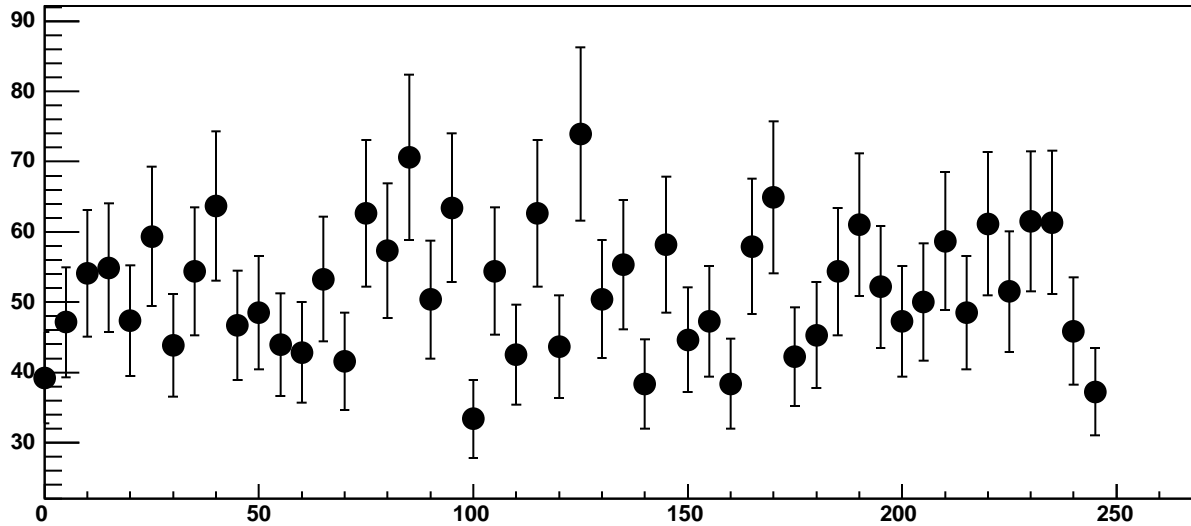
Chip 7, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold



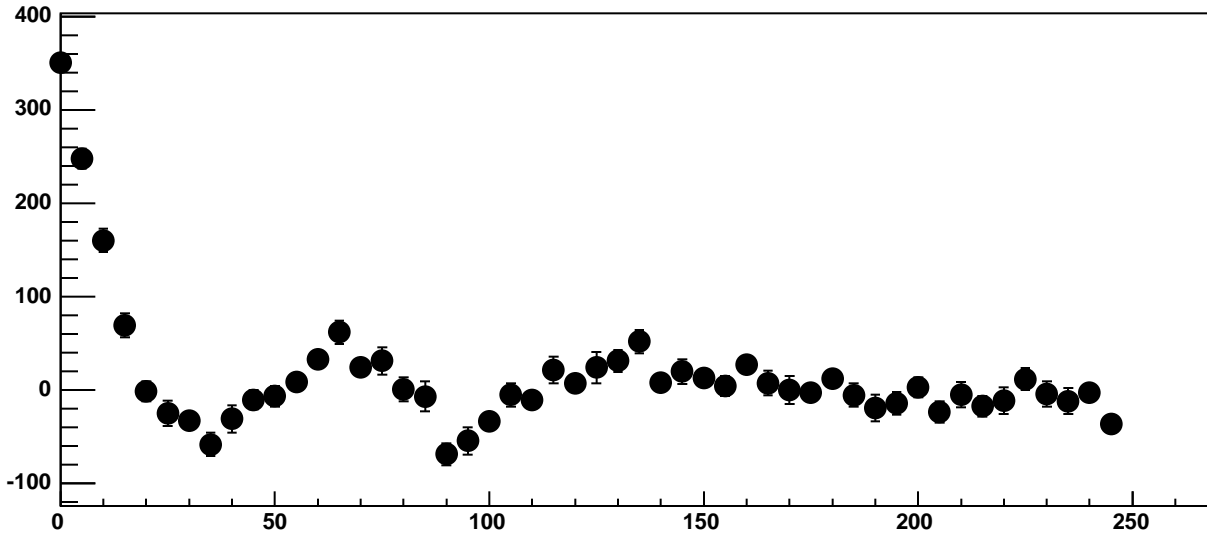
Chip 7, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold



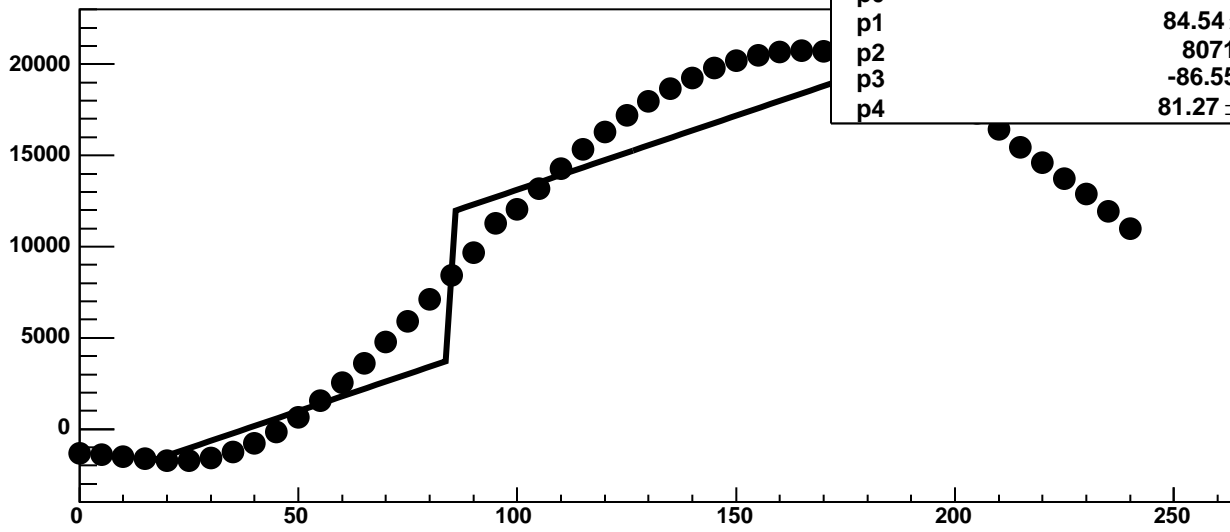
Chip 7, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

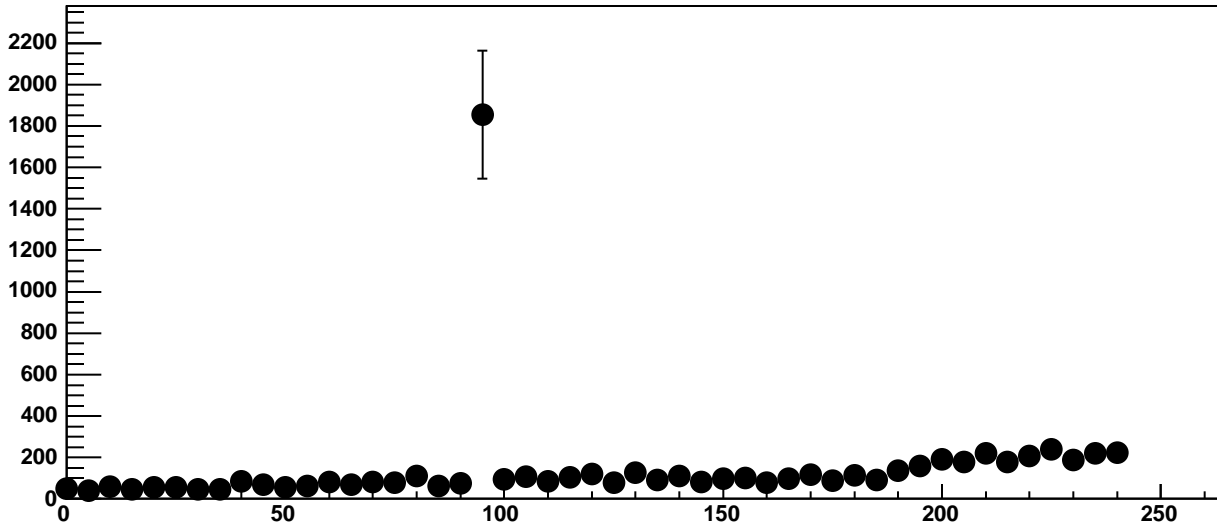


Chip 7, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

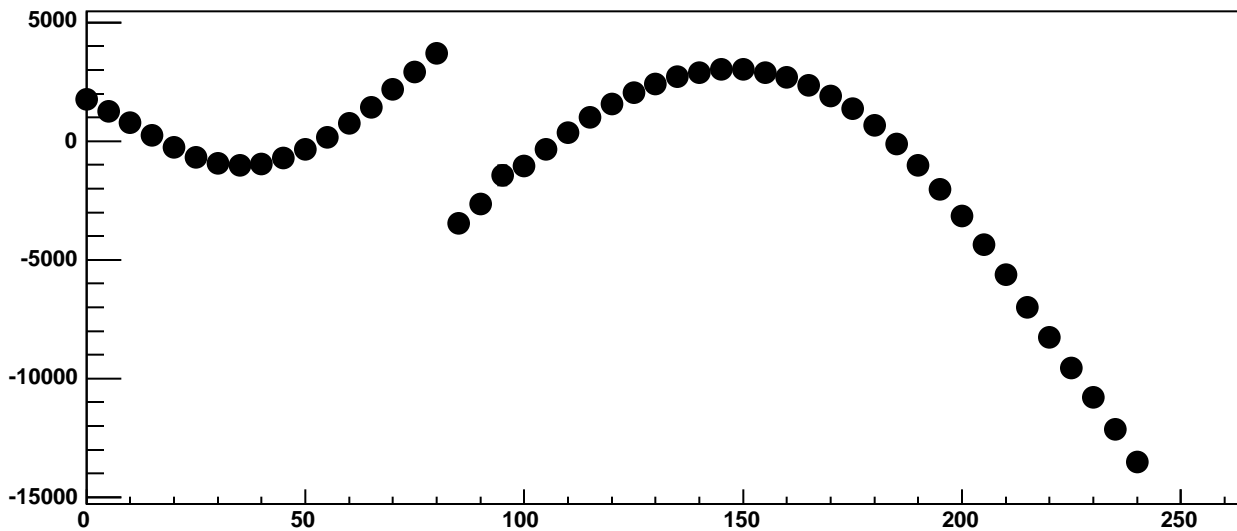


$\chi^2 / \text{ndf}$	6.489e+05 / 41
p0	3786 ± 10.54
p1	84.54 ± 0.2801
p2	8071 ± 27.37
p3	-86.55 ± 3.631
p4	81.27 ± 0.3856

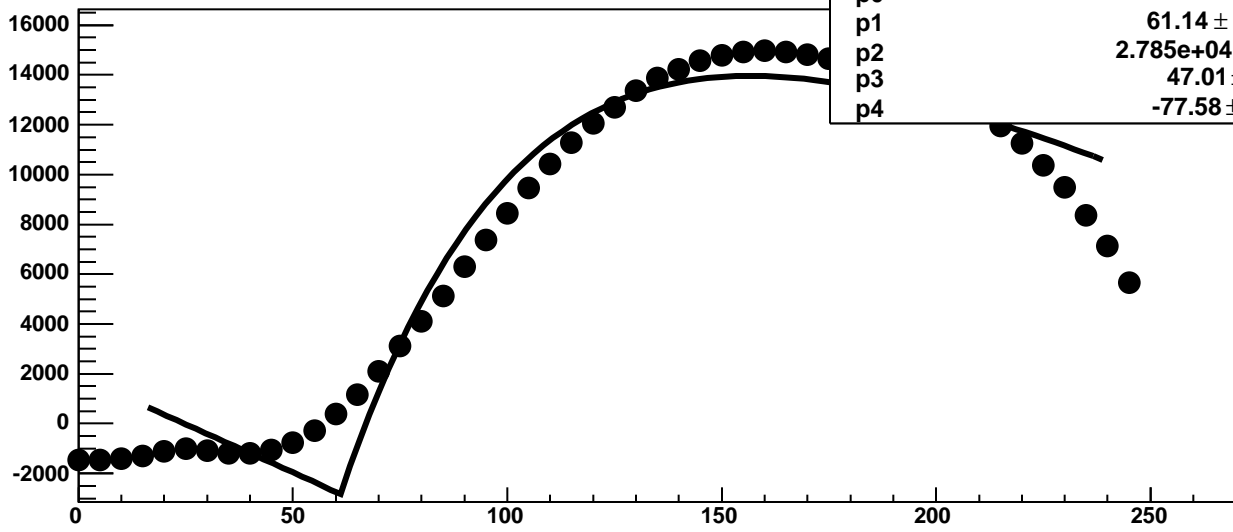
Chip 7, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold

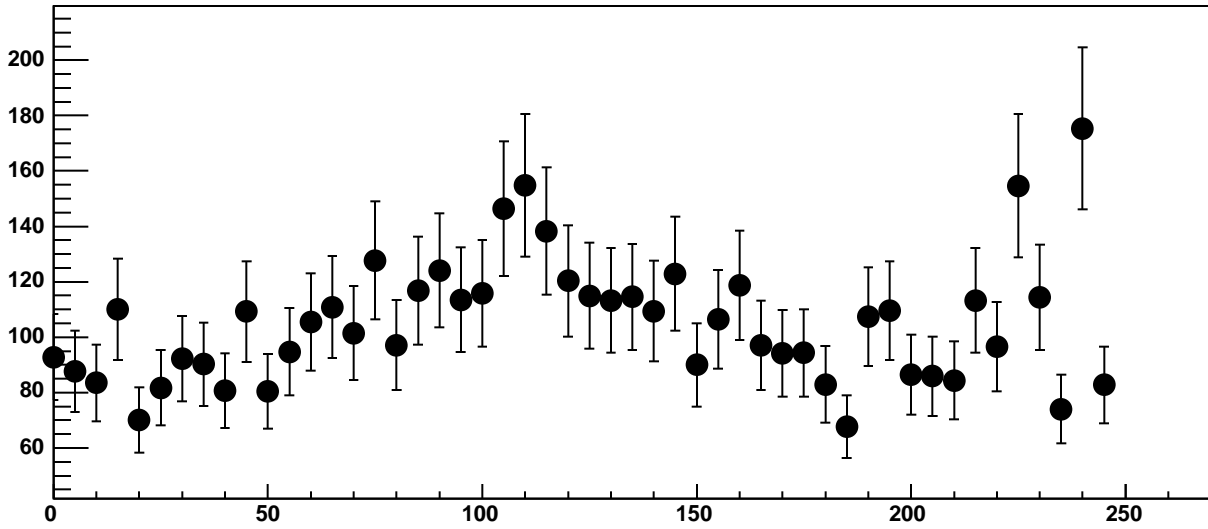


Chip 7, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold

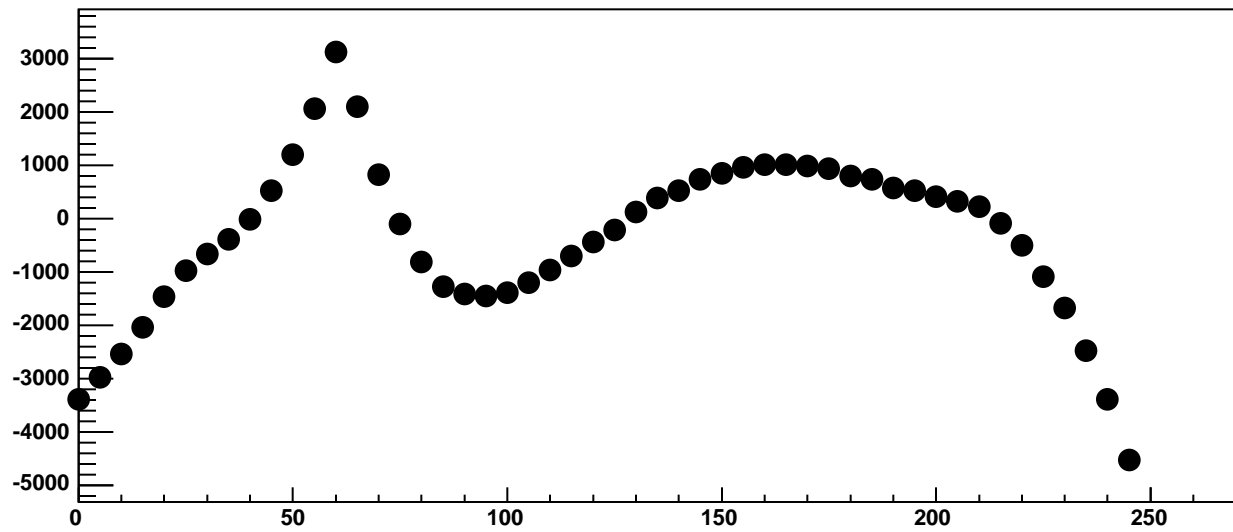


$\chi^2 / \text{ndf}$	1.24e+05 / 41
p0	-2827 ± 7.827
p1	61.14 ± 0.03651
p2	2.785e+04 ± 55.76
p3	47.01 ± 0.1111
p4	-77.58 ± 0.2738

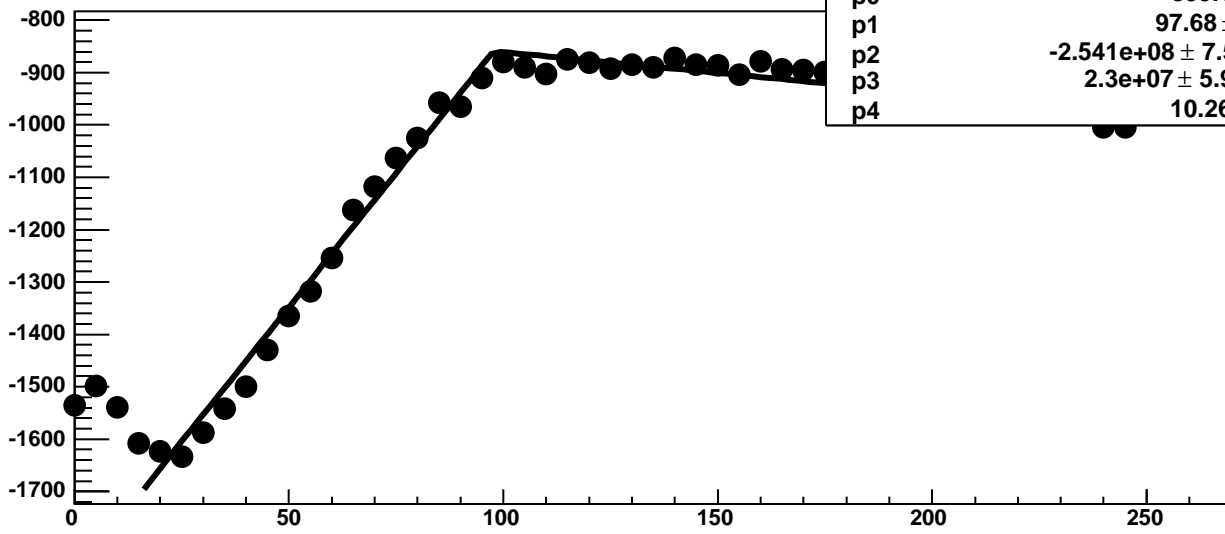
Chip 7, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold

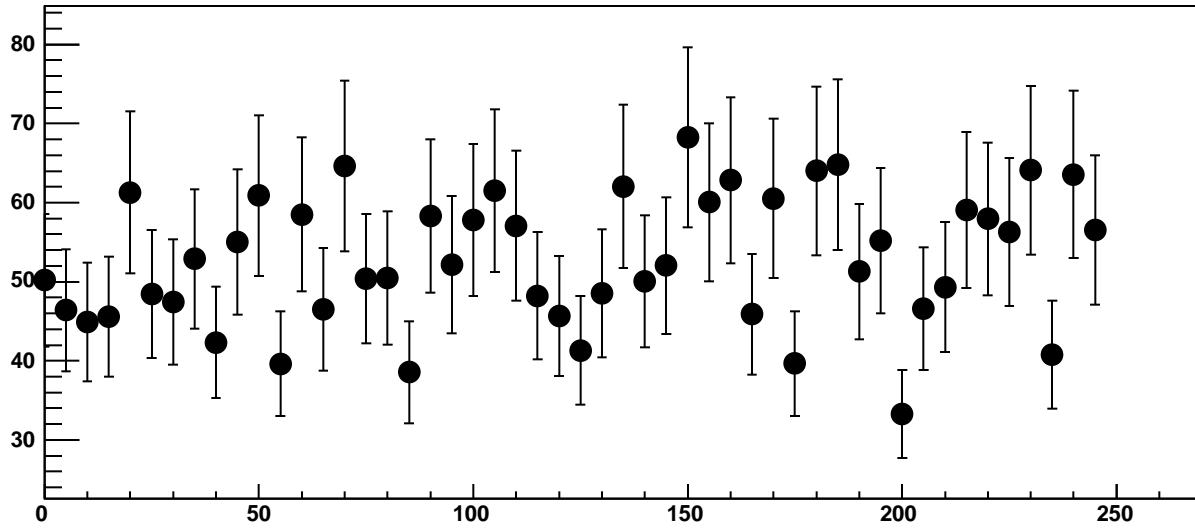


Chip 7, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

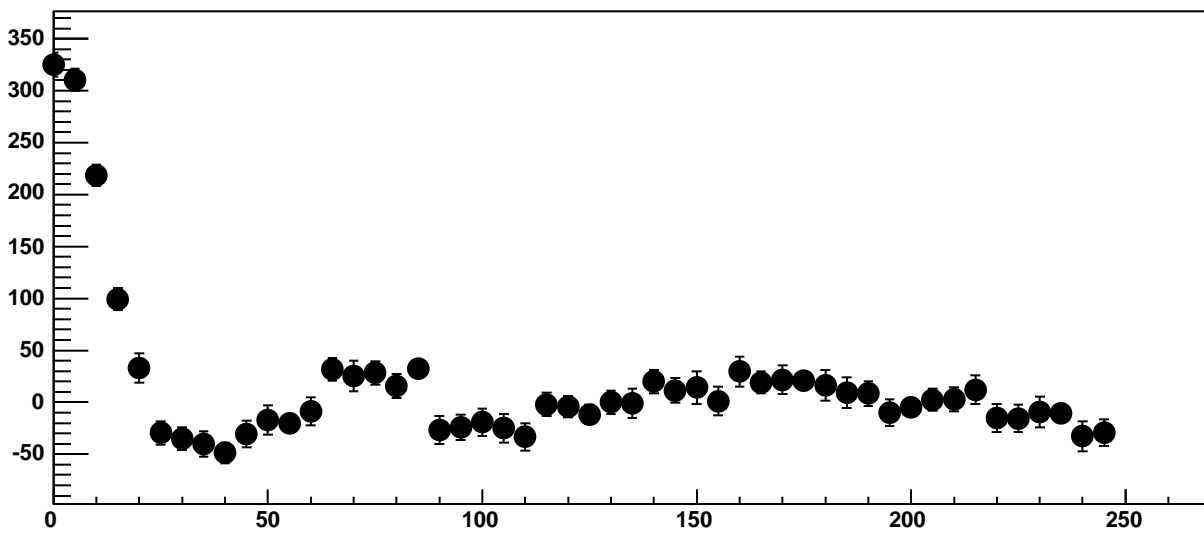


$\chi^2 / \text{ndf}$	250.1 / 41
p0	$-859.1 \pm 4.196$
p1	$97.68 \pm 0.6449$
p2	$-2.541\text{e}+08 \pm 7.527\text{e}+06$
p3	$2.3\text{e}+07 \pm 5.924\text{e}+05$
p4	$10.26 \pm 0.113$

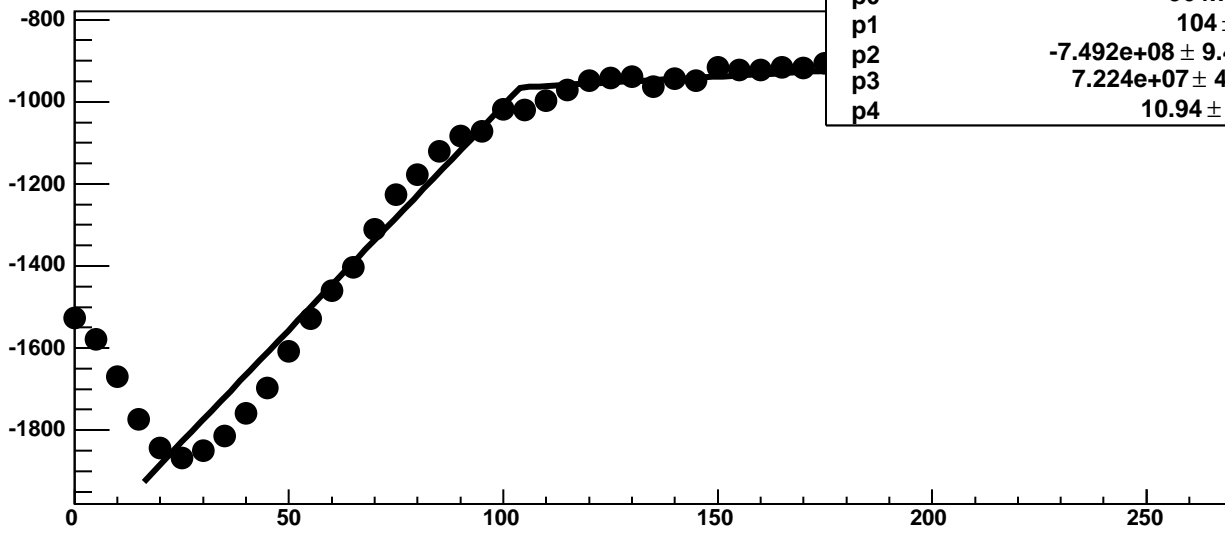
Chip 7, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

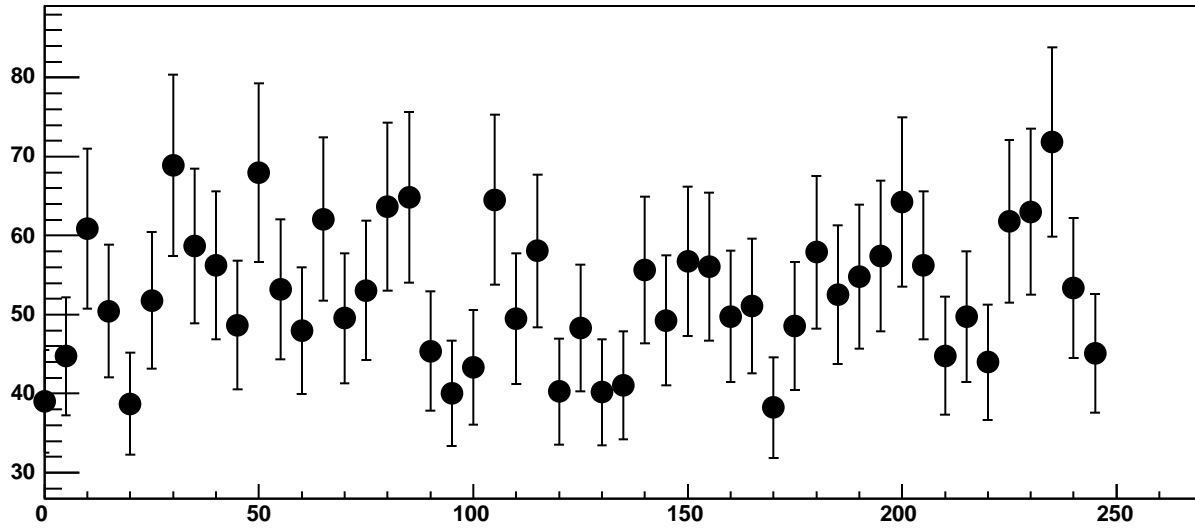


Chip 7, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

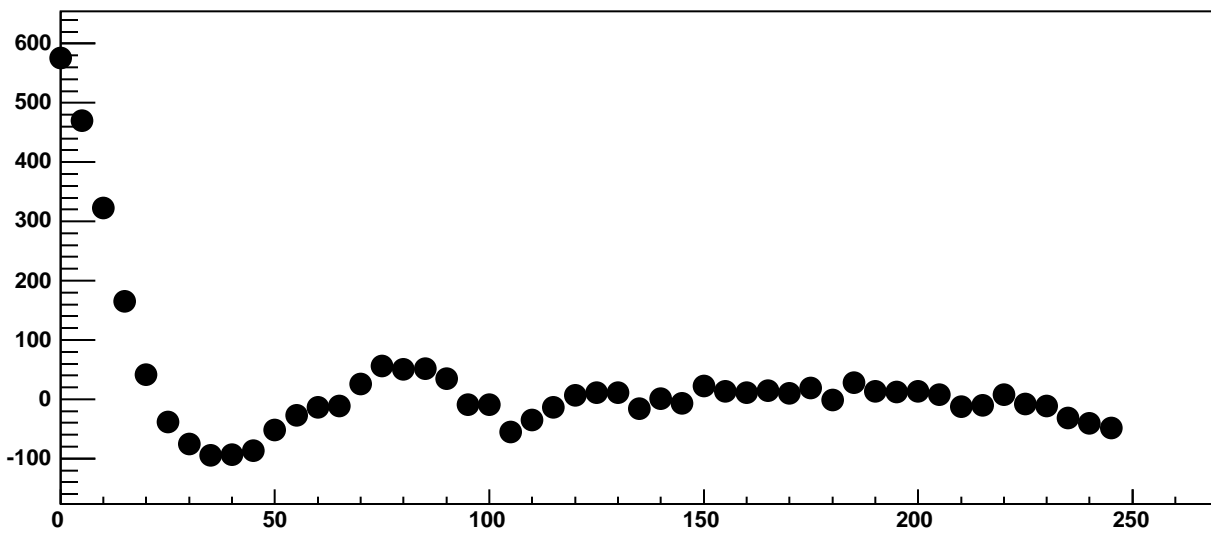


$\chi^2 / \text{ndf}$	568.2 / 41
p0	$-964.7 \pm 4.524$
p1	$104 \pm 0.6557$
p2	$-7.492\text{e}+08 \pm 9.493\text{e}+06$
p3	$7.224\text{e}+07 \pm 4.18\text{e}+05$
p4	$10.94 \pm 0.09916$

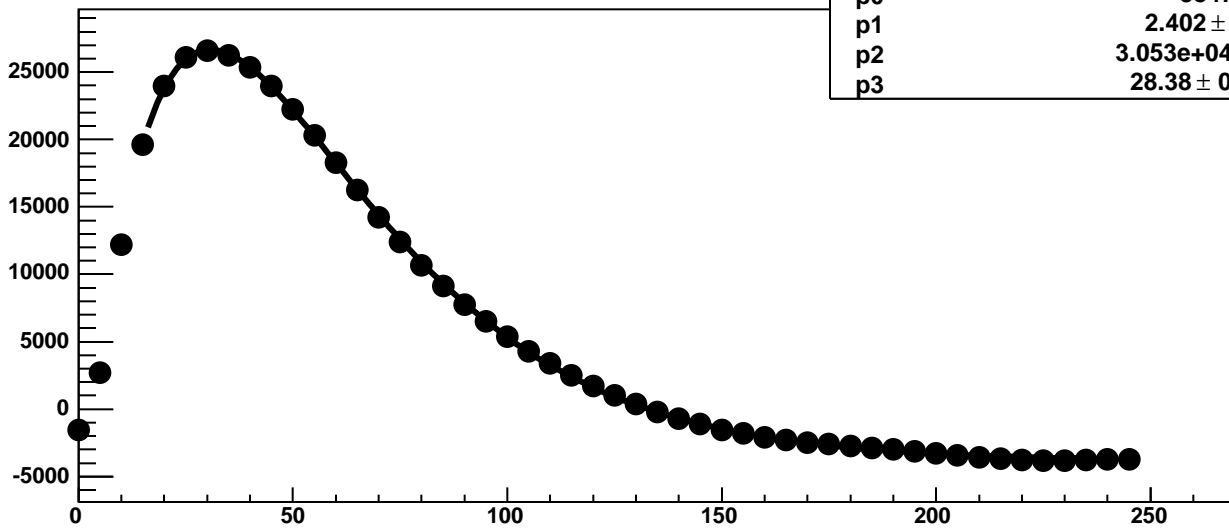
Chip 7, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

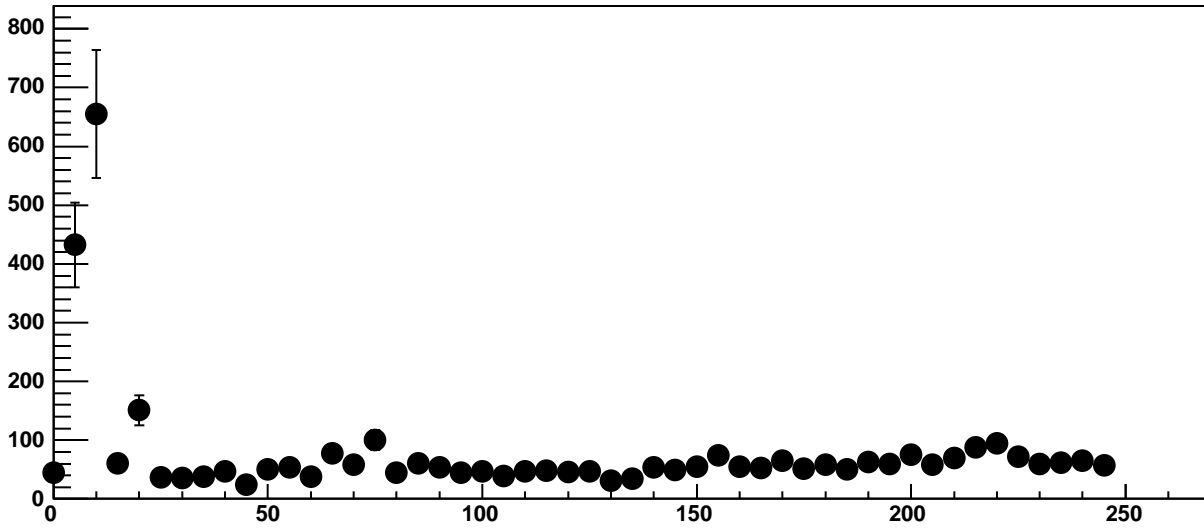


Chip 7, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

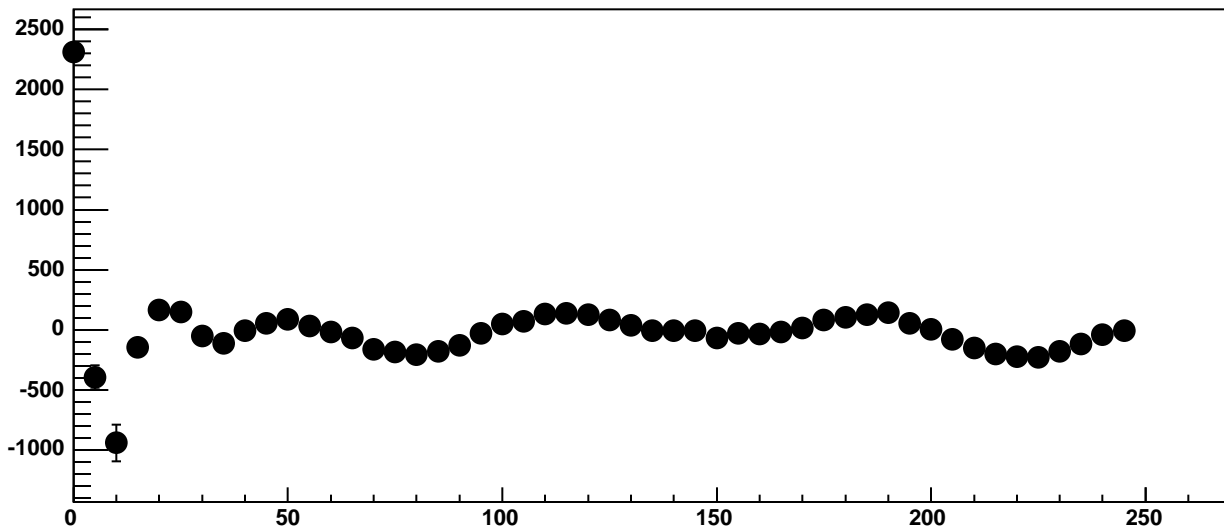


$\chi^2 / \text{ndf}$	3488 / 42
p0	-3847 ± 3.883
p1	2.402 ± 0.01427
p2	3.053e+04 ± 4.708
p3	28.38 ± 0.009403

Chip 7, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

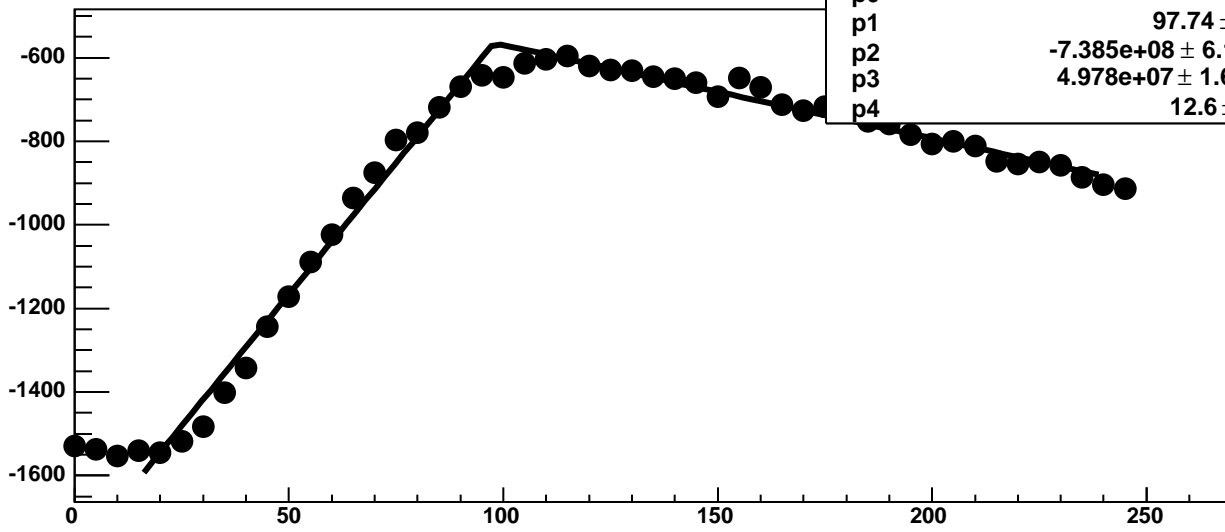


Chip 7, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold



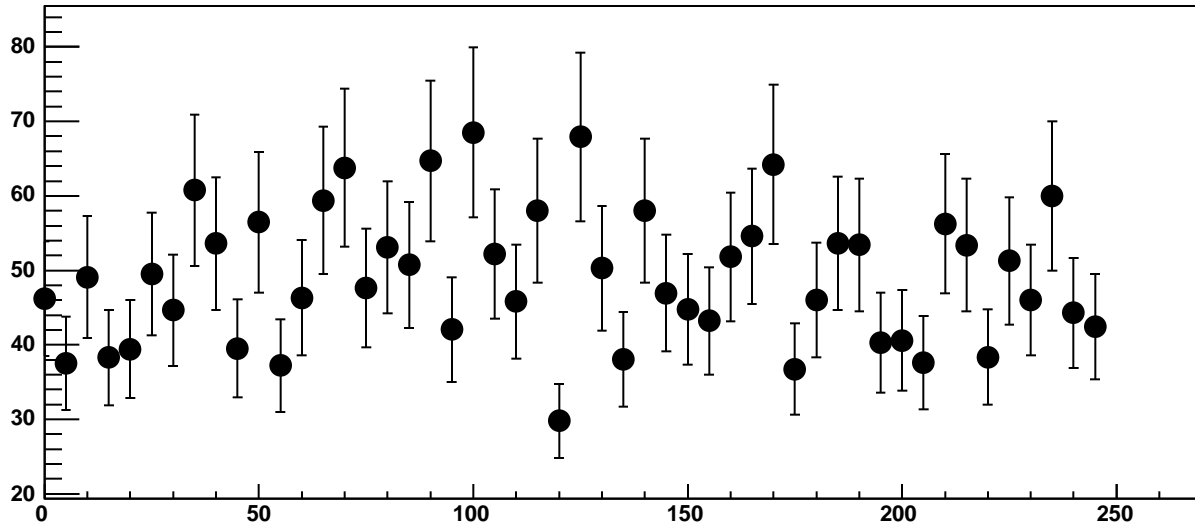


Chip 7, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

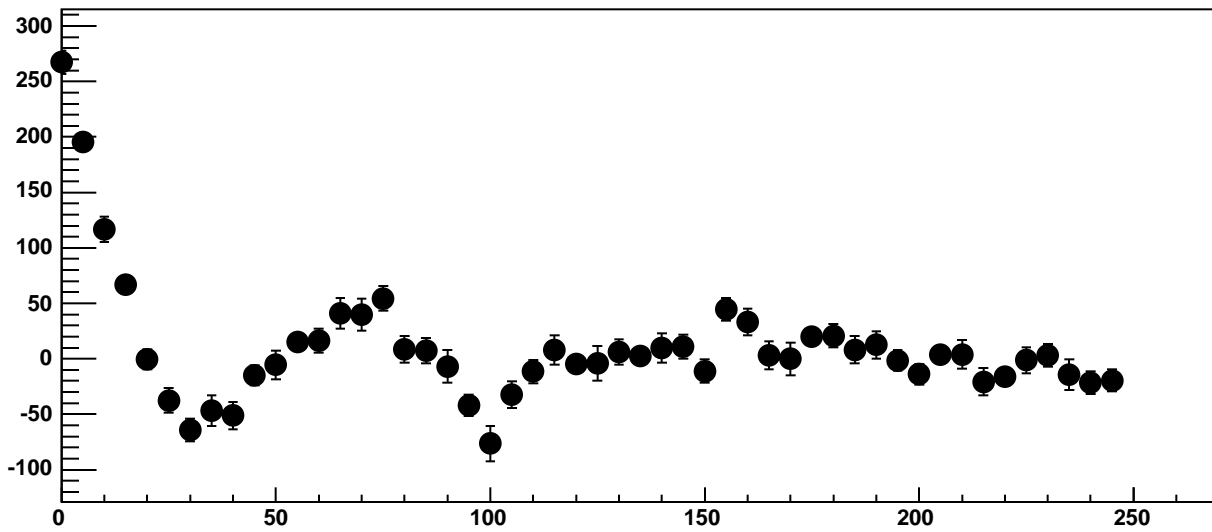


$\chi^2 / \text{ndf}$	296.2 / 41
p0	$-564.5 \pm 3.547$
p1	$97.74 \pm 0.4605$
p2	$-7.385\text{e}+08 \pm 6.193\text{e}+06$
p3	$4.978\text{e}+07 \pm 1.607\text{e}+05$
p4	$12.6 \pm 0.1049$

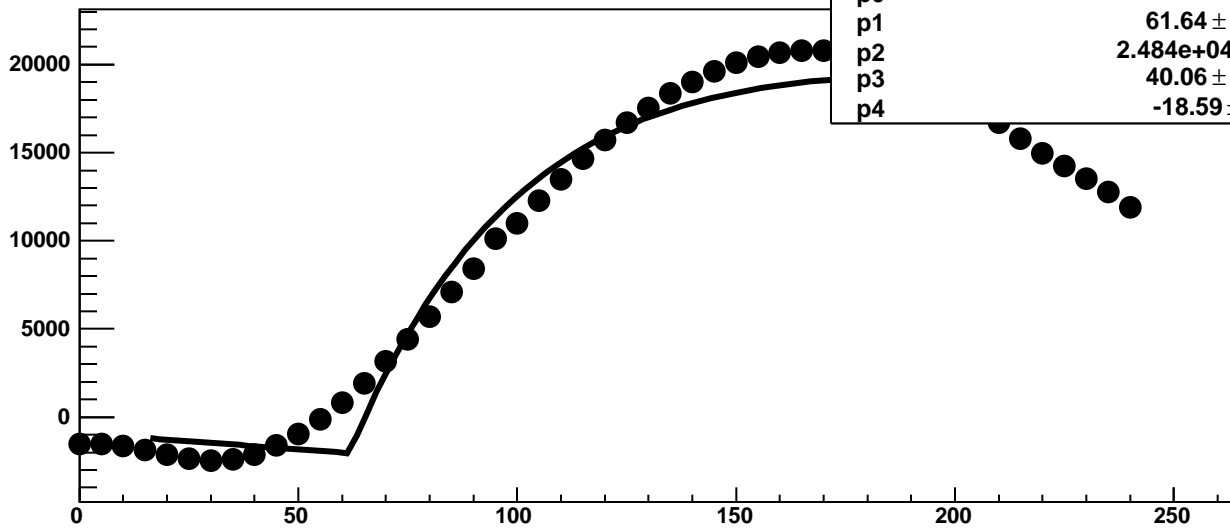
Chip 7, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

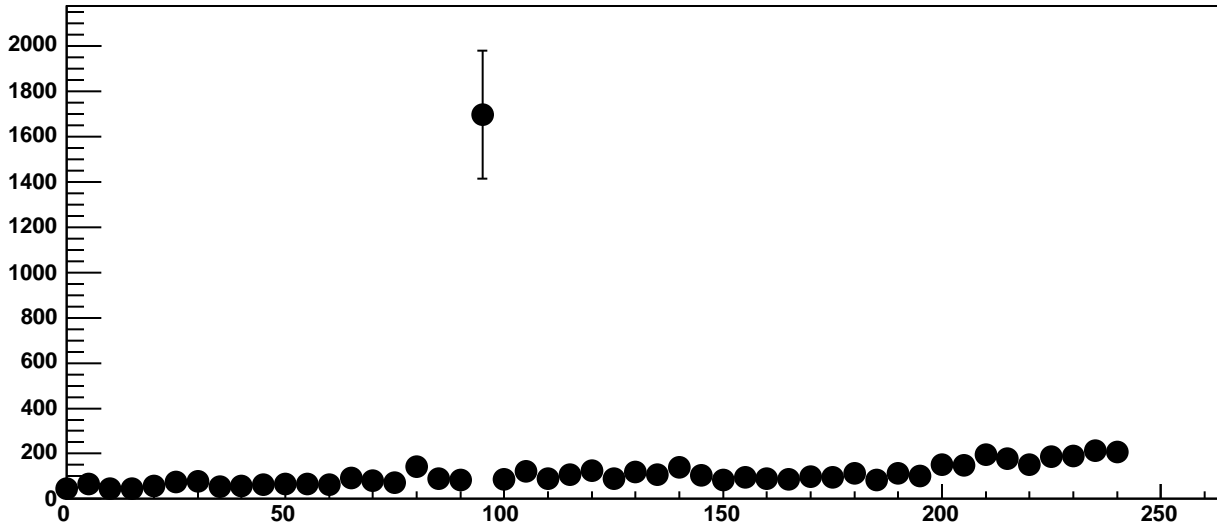


Chip 7, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

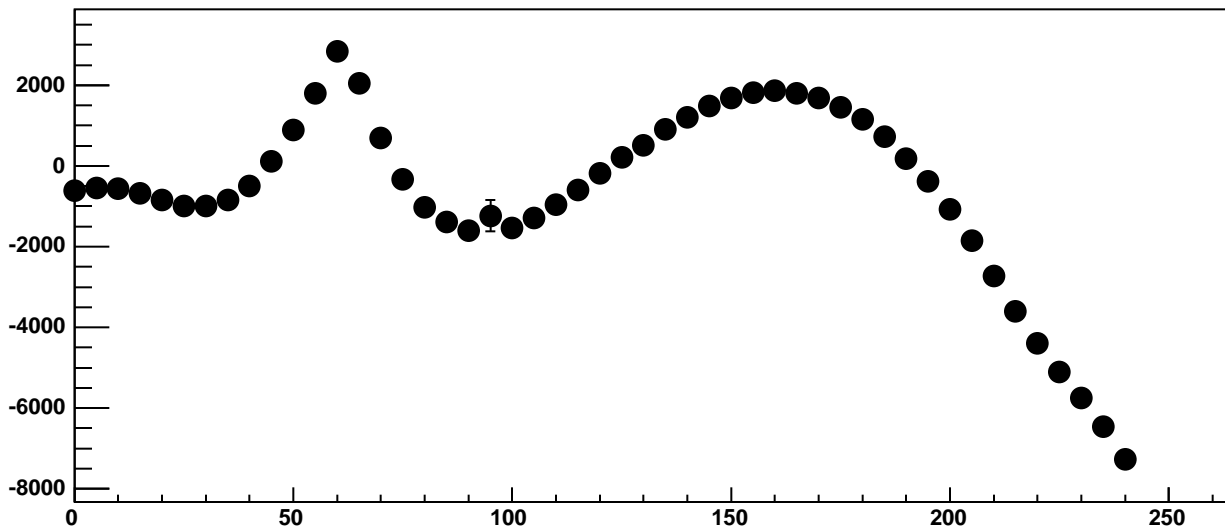


$\chi^2 / \text{ndf}$	2.658e+05 / 41
p0	-2050 ± 6.916
p1	61.64 ± 0.02802
p2	2.484e+04 ± 38.19
p3	40.06 ± 0.07575
p4	-18.59 ± 0.2129

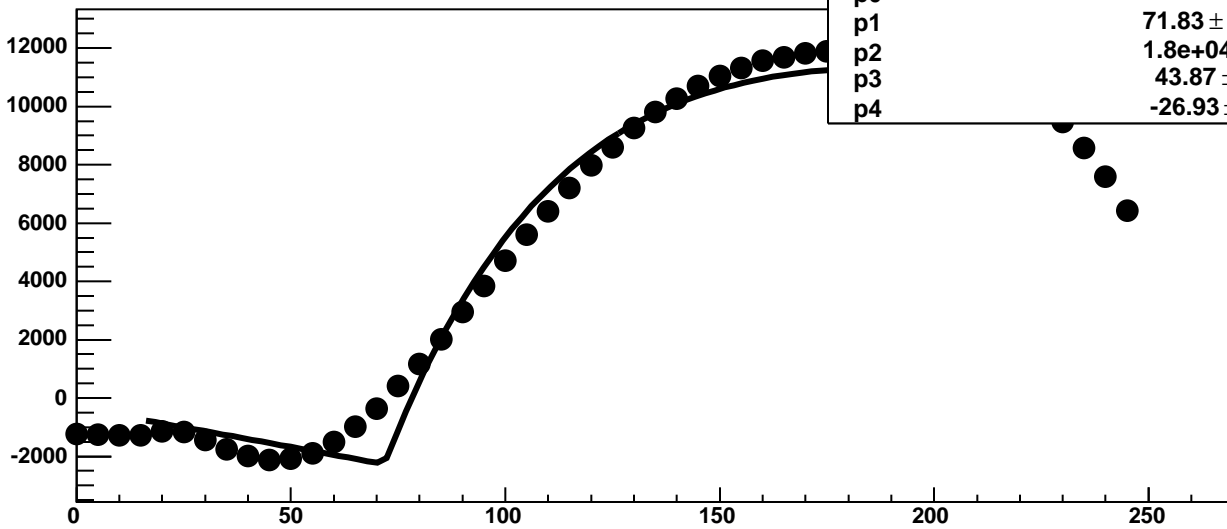
Chip 7, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

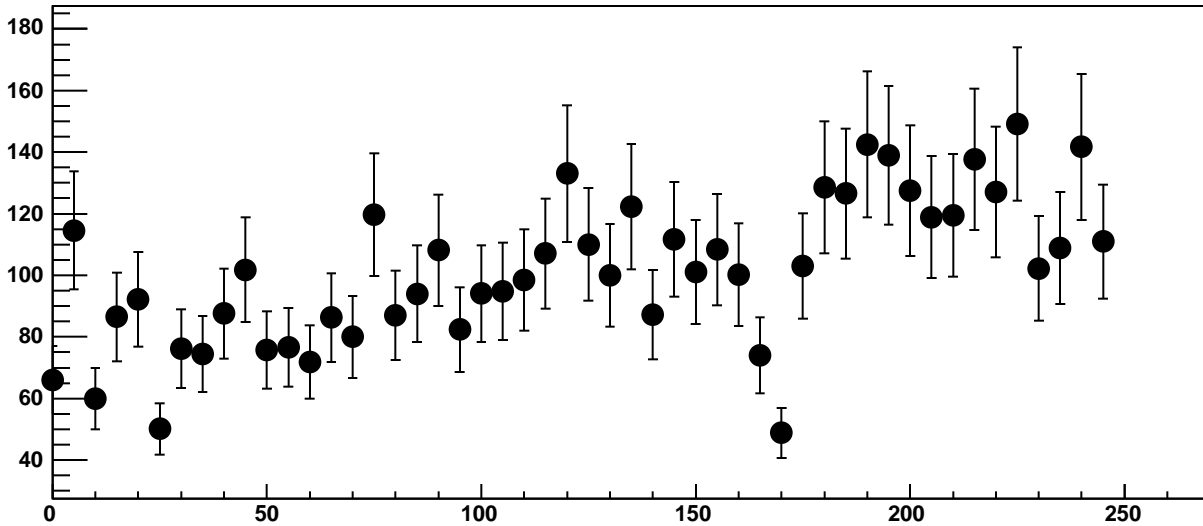


Chip 7, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold

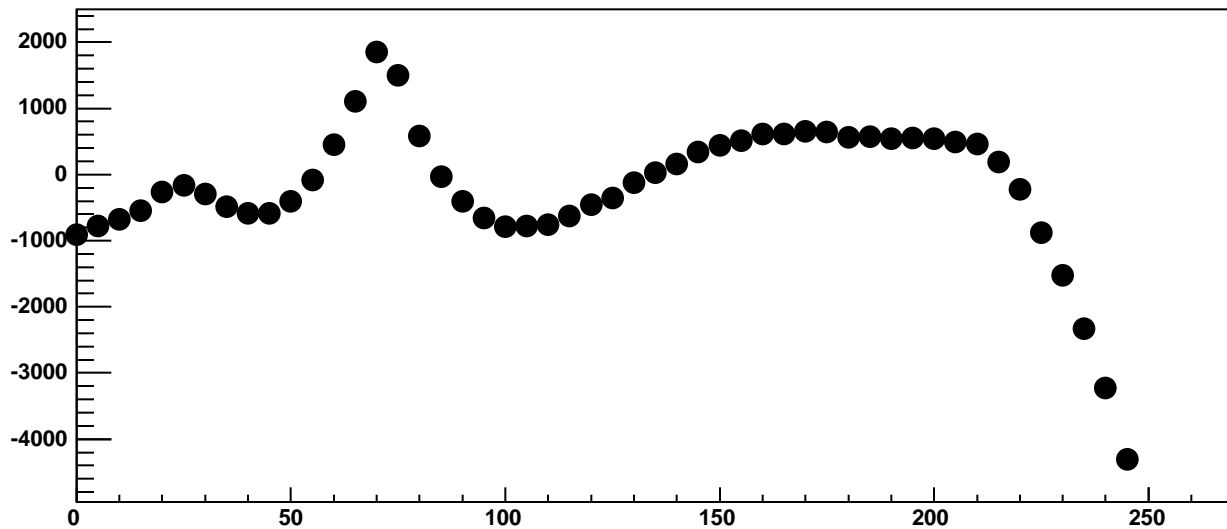


$\chi^2 / \text{ndf}$	6.166e+04 / 41
p0	-2265 ± 8.078
p1	71.83 ± 0.04852
p2	1.8e+04 ± 45.14
p3	43.87 ± 0.1335
p4	-26.93 ± 0.2288

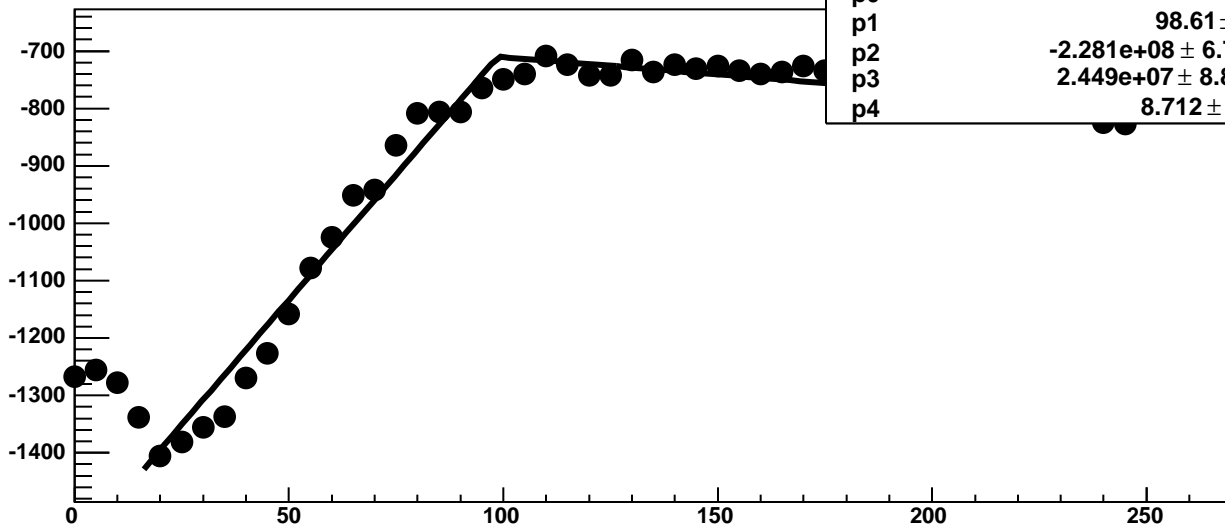
Chip 7, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

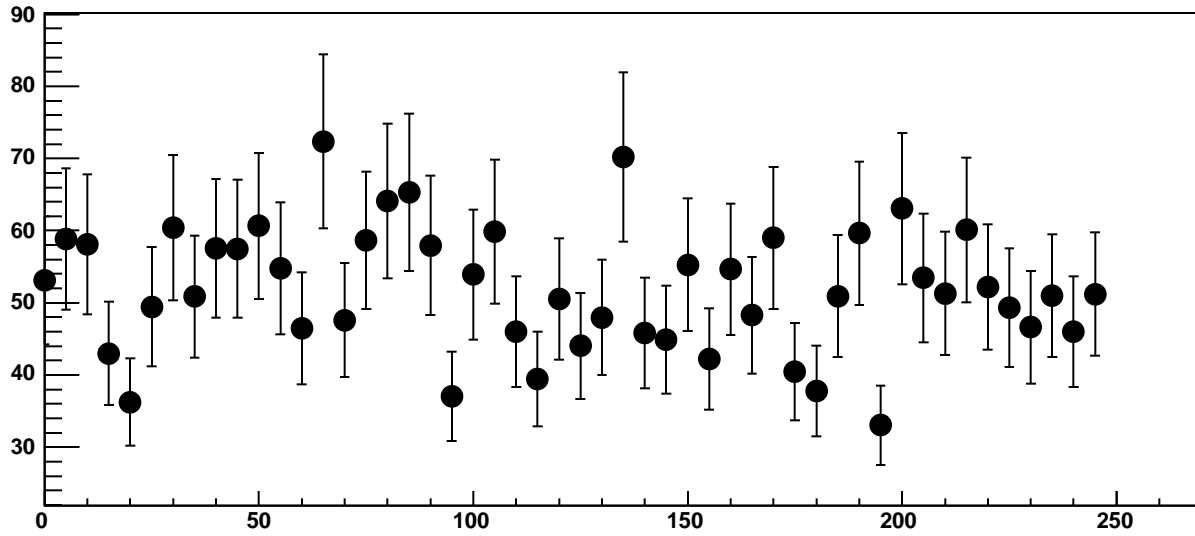


Chip 7, Channel 12, Enable 1, DAC=1600, ADC Mean vs Hold

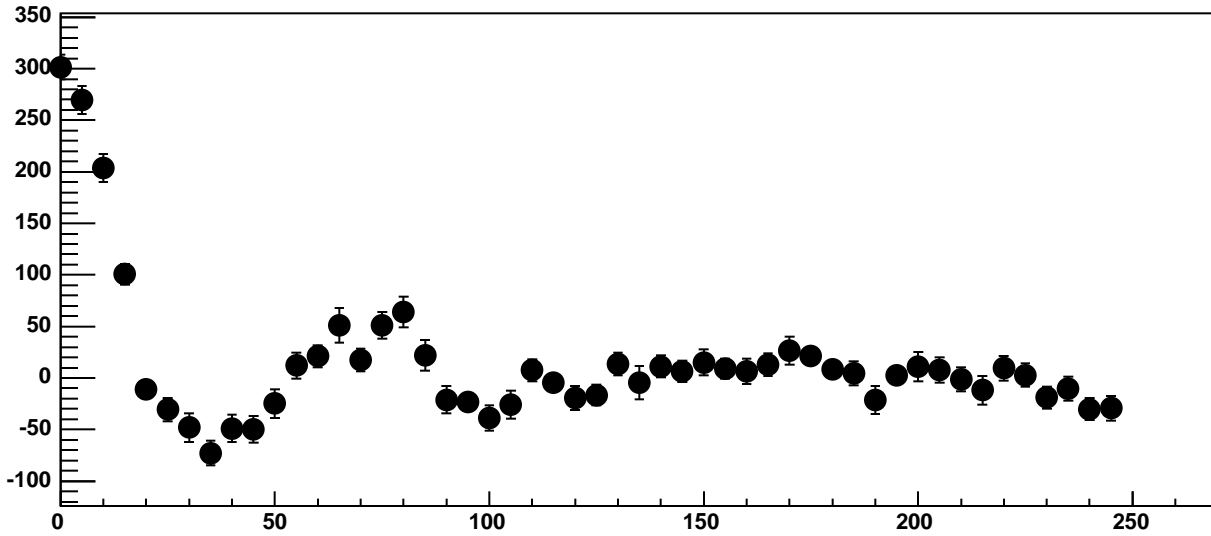


$\chi^2 / \text{ndf}$	311.8 / 41
p0	$-709.9 \pm 3.78$
p1	$98.61 \pm 0.6764$
p2	$-2.281\text{e}+08 \pm 6.787\text{e}+06$
p3	$2.449\text{e}+07 \pm 8.839\text{e}+05$
p4	$8.712 \pm 0.09947$

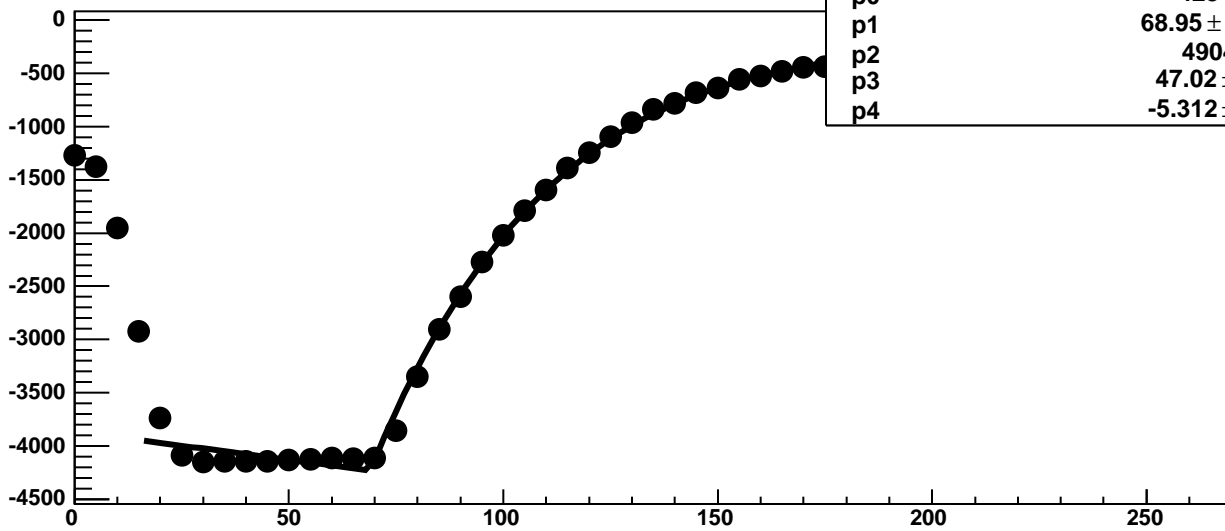
Chip 7, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold

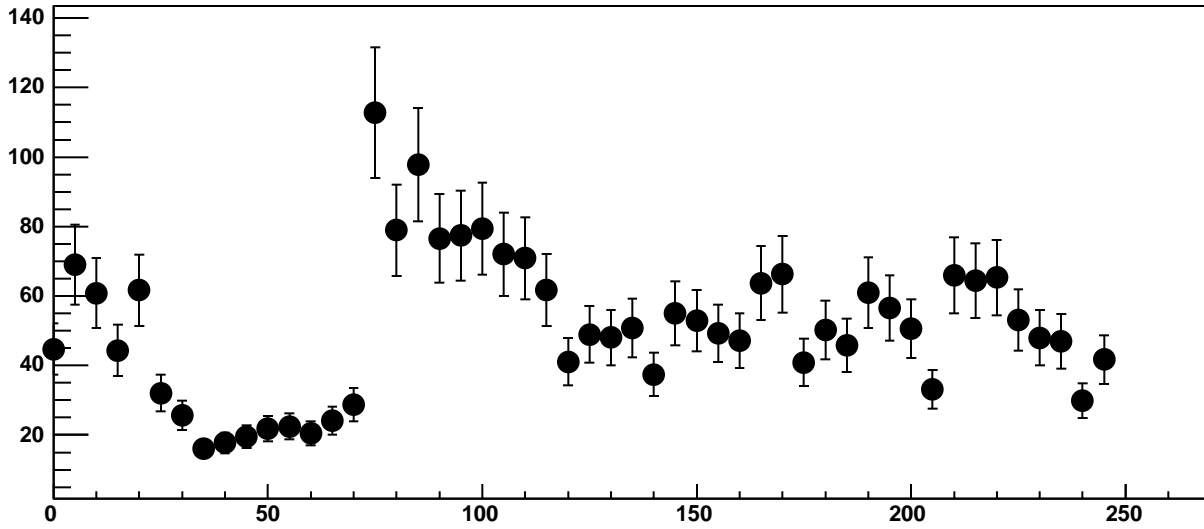


Chip 7, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

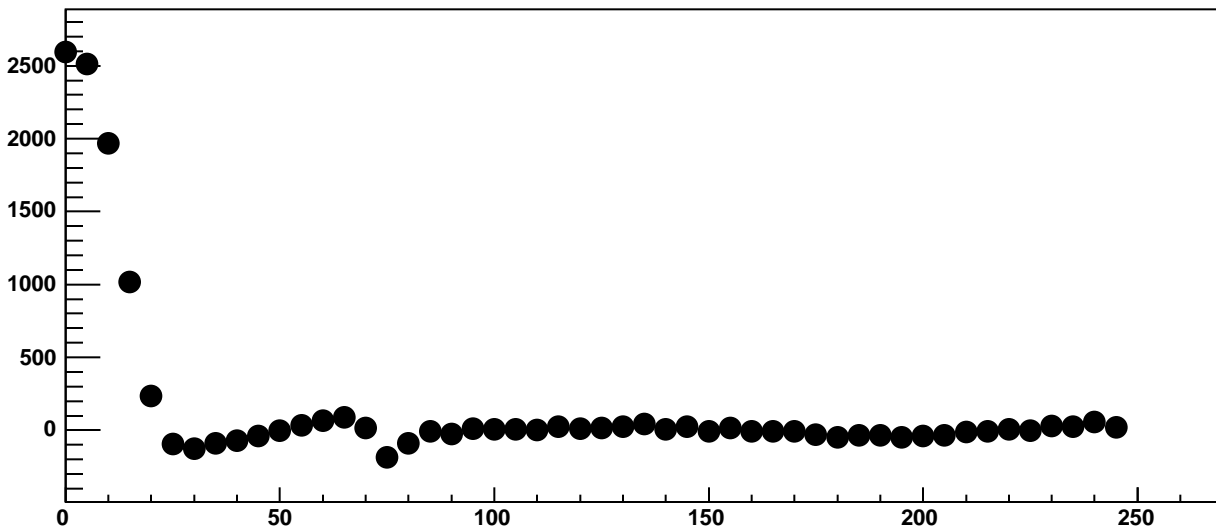


$\chi^2 / \text{ndf}$	1.273e+04 / 41
p0	-4231 ± 3.102
p1	68.95 ± 0.07274
p2	4904 ± 24.9
p3	47.02 ± 0.2989
p4	-5.312 ± 0.1164

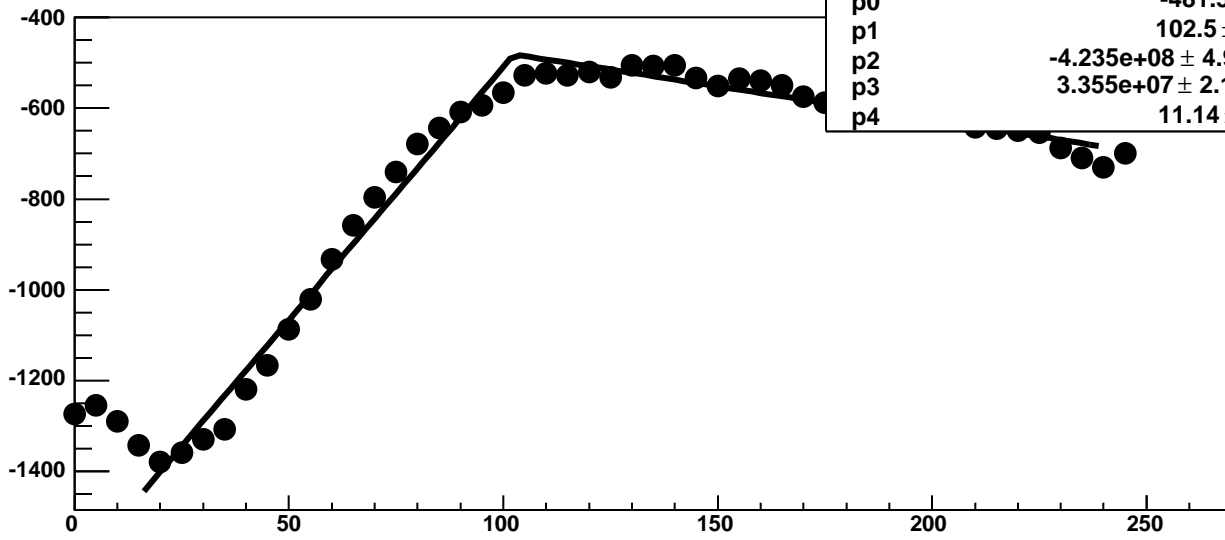
Chip 7, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

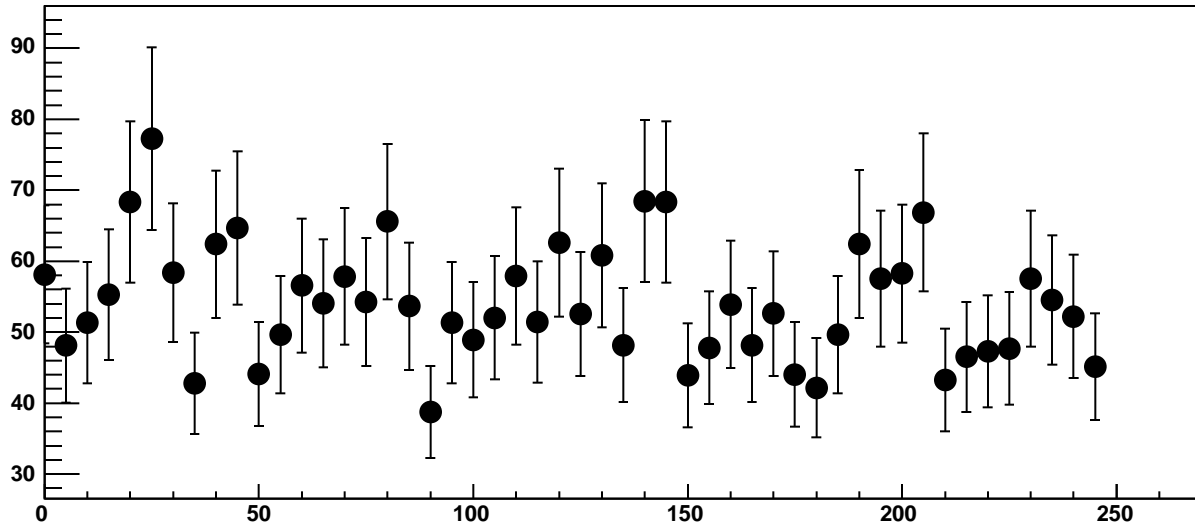


Chip 7, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

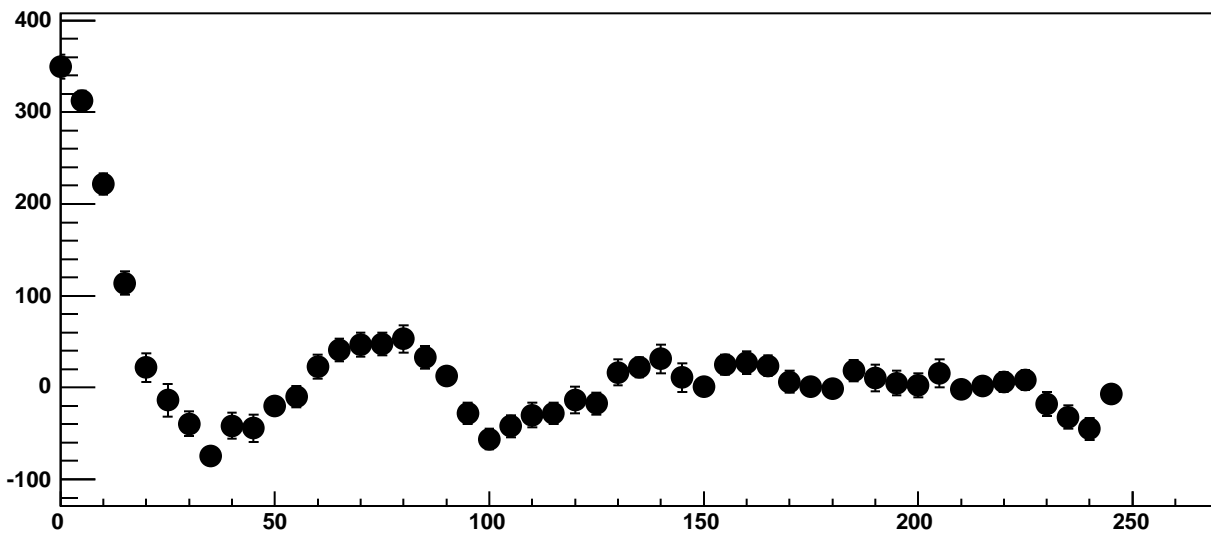


$\chi^2 / \text{ndf}$	342.9 / 41
p0	$-481.5 \pm 4.192$
p1	$102.5 \pm 0.5718$
p2	$-4.235e+08 \pm 4.989e+06$
p3	$3.355e+07 \pm 2.124e+05$
p4	$11.14 \pm 0.1121$

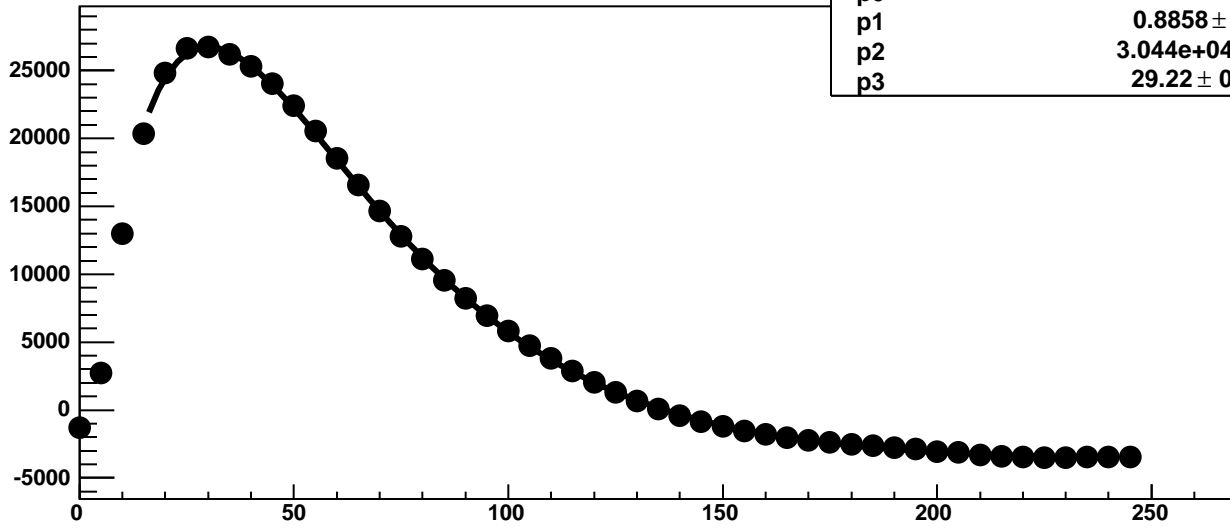
Chip 7, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

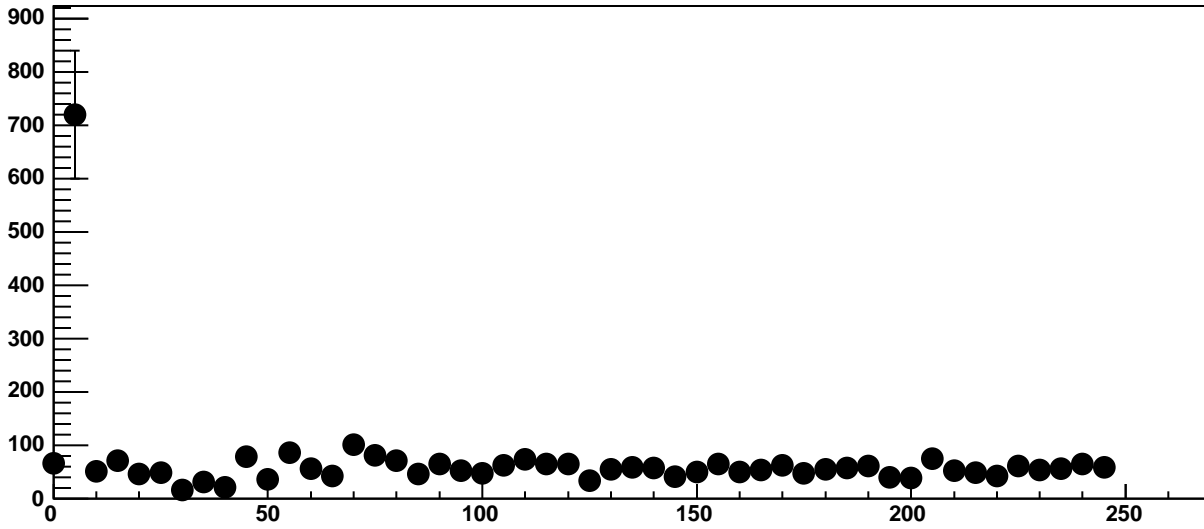


Chip 7, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold

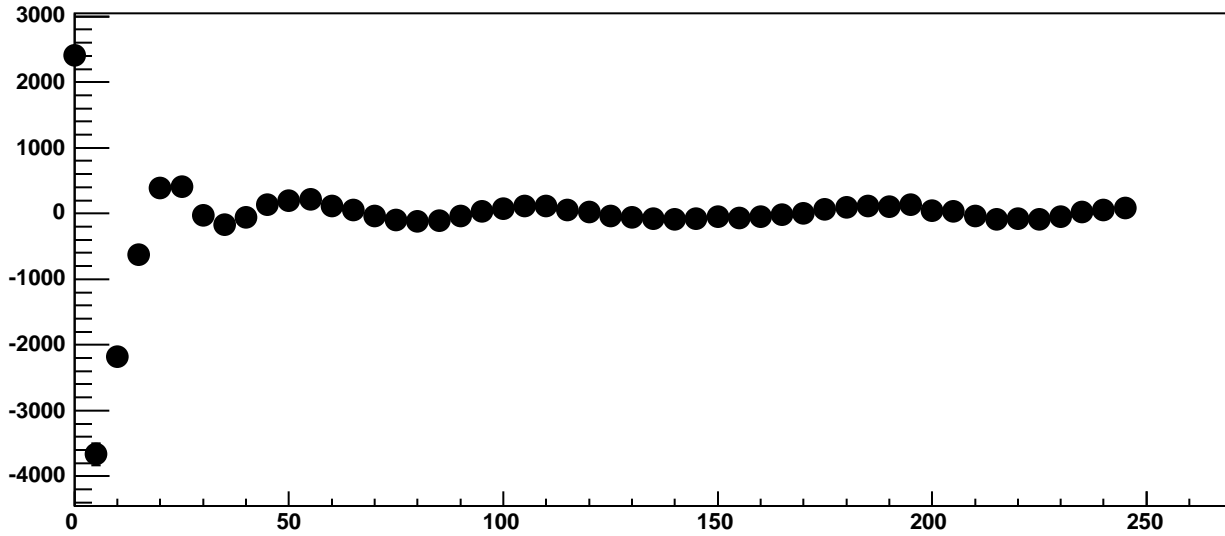


$\chi^2 / \text{ndf}$	6932 / 42
p0	-3706 ± 3.425
p1	0.8858 ± 0.01579
p2	3.044e+04 ± 3.993
p3	29.22 ± 0.009786

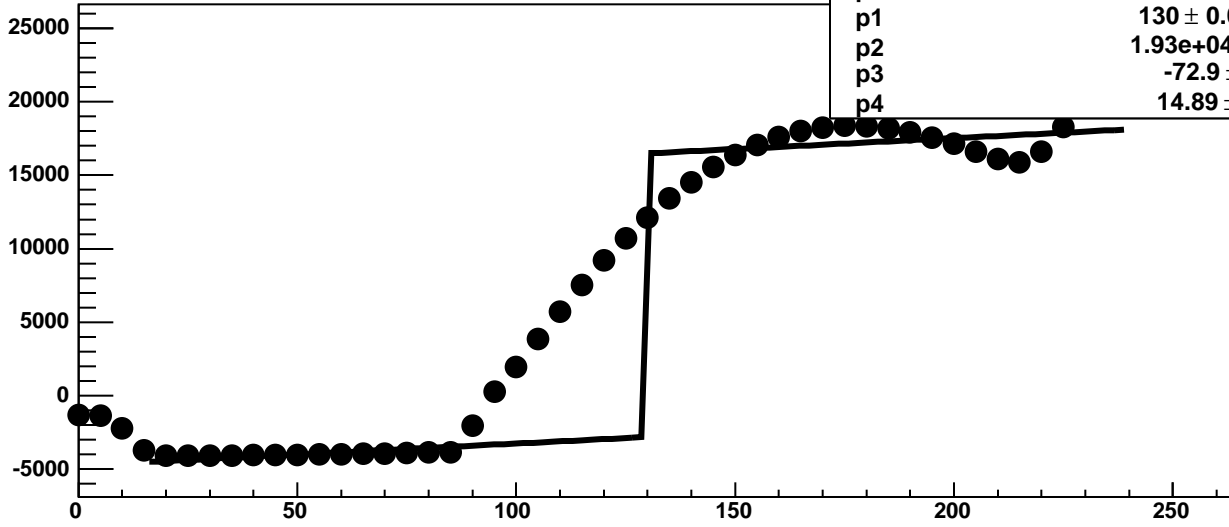
Chip 7, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



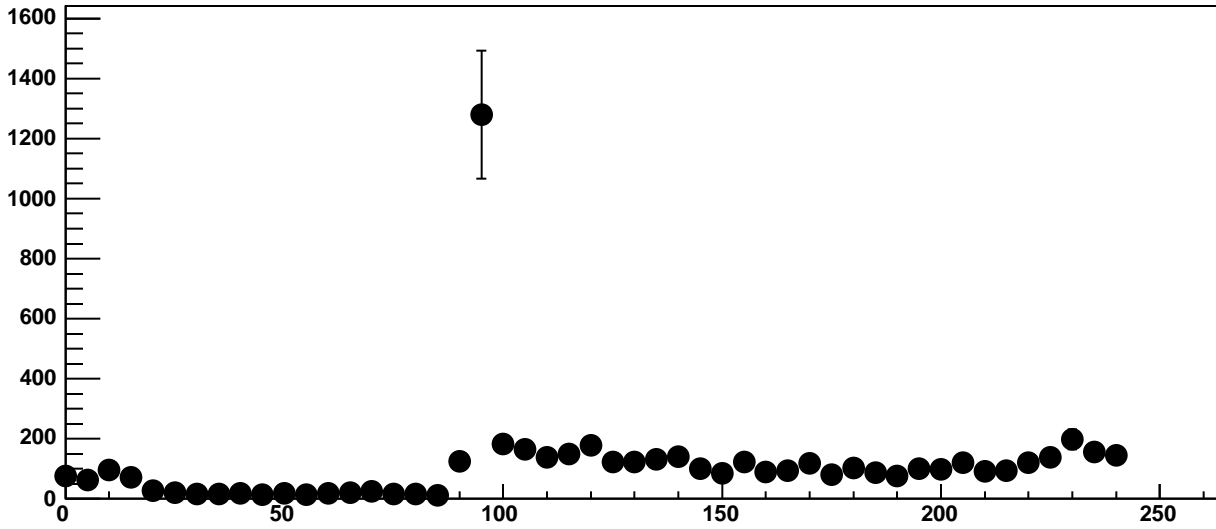
Chip 7, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold



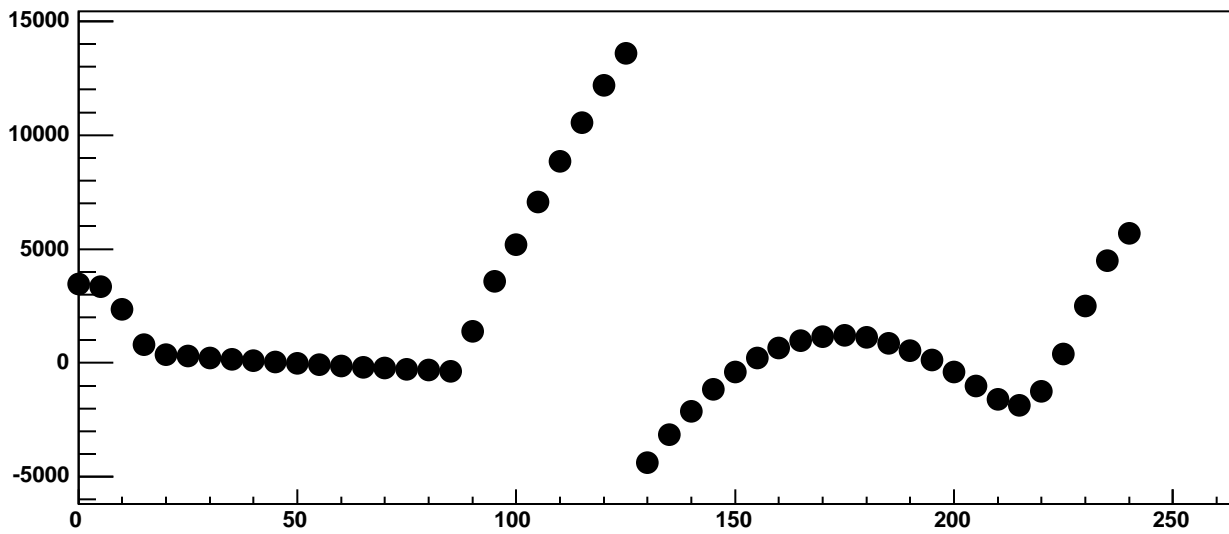
Chip 7, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 7, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

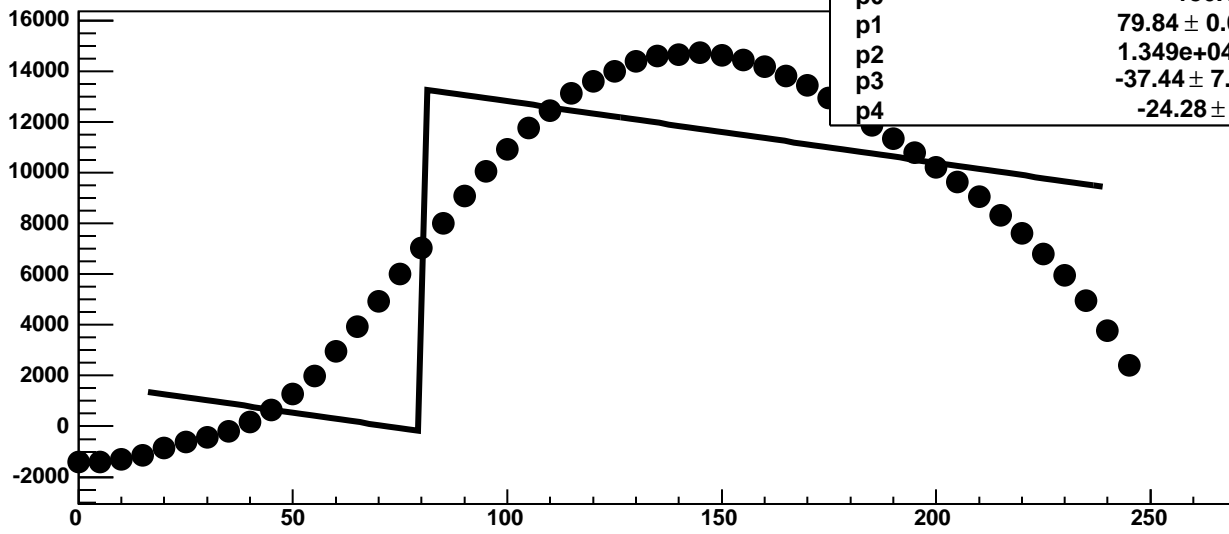


Chip 7, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



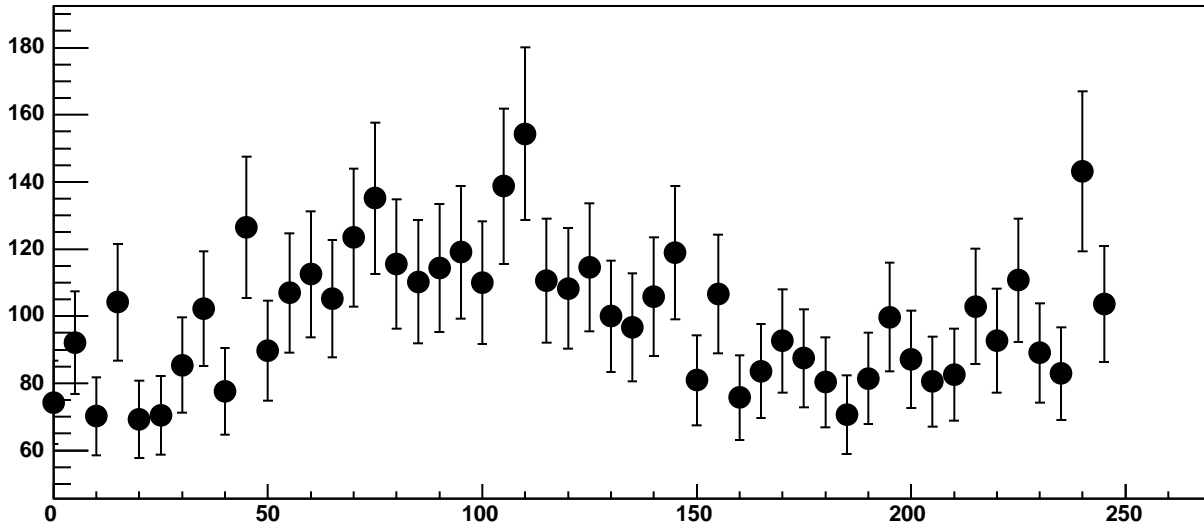


Chip 7, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

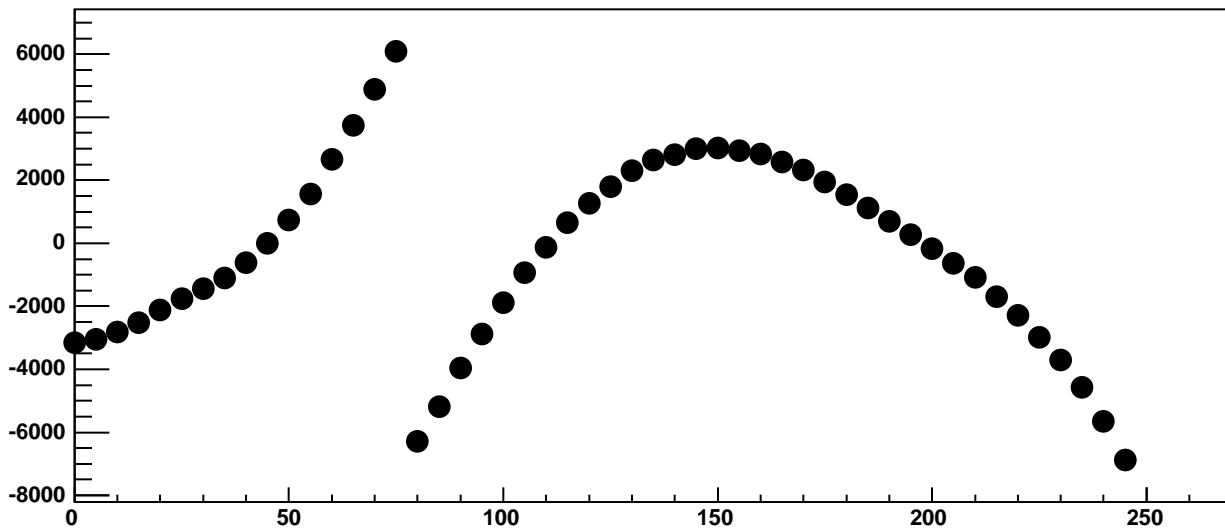


$\chi^2 / \text{ndf}$	6.298e+05 / 41
p0	-186.1 ± 7.649
p1	79.84 ± 0.0006898
p2	1.349e+04 ± 11.76
p3	-37.44 ± 7.894e-05
p4	-24.28 ± 0.07327

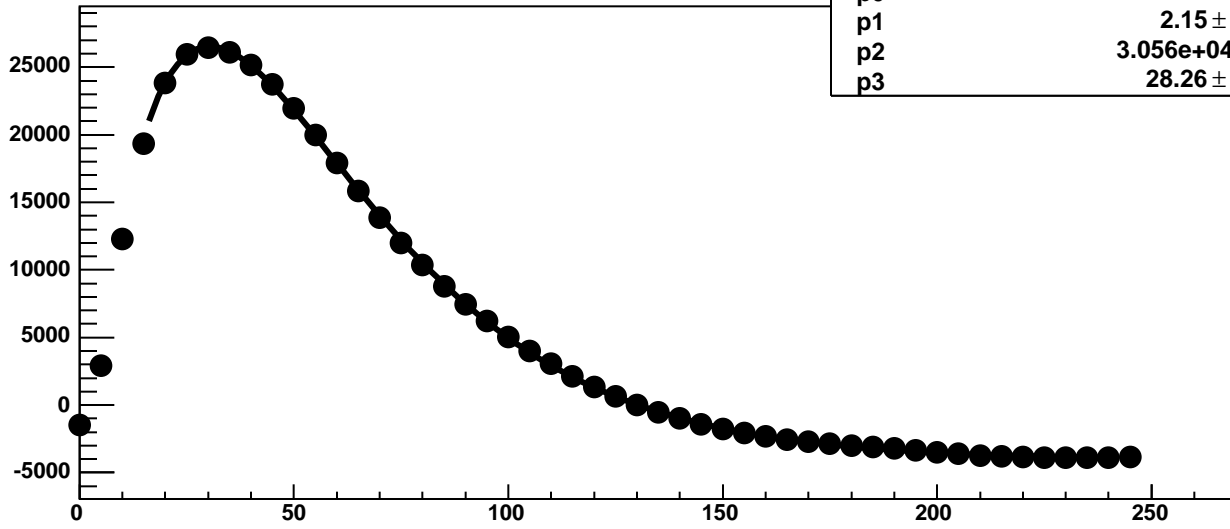
Chip 7, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

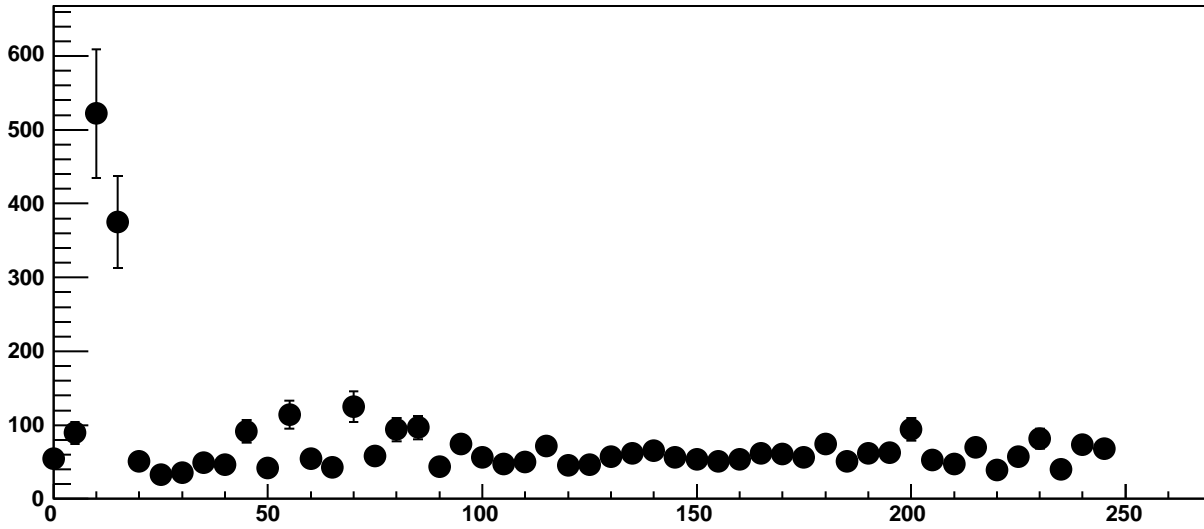


Chip 7, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold

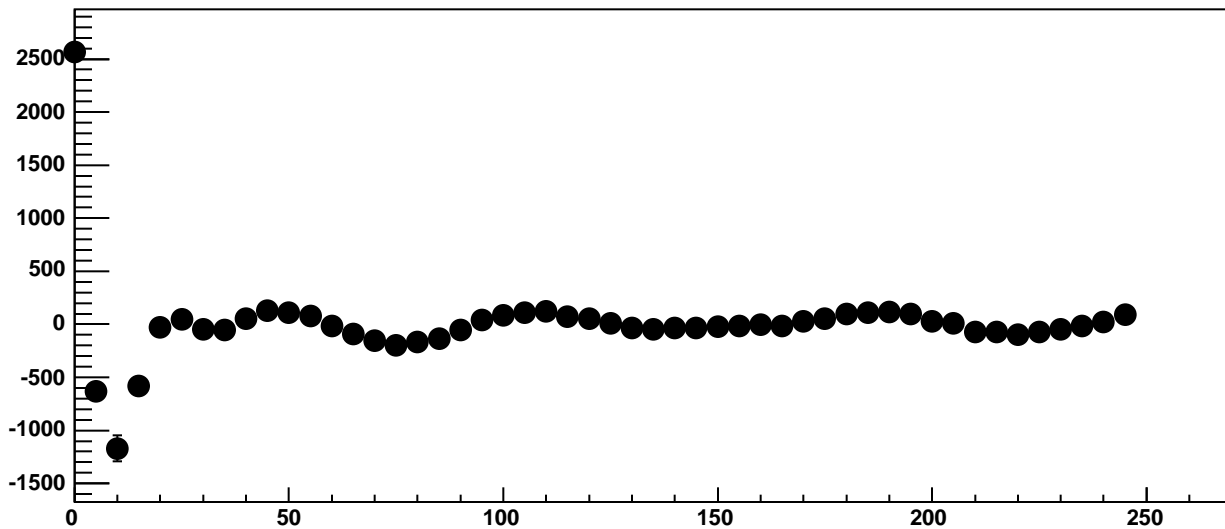


$\chi^2 / \text{ndf}$	1659 / 42
p0	-4046 ± 3.654
p1	2.15 ± 0.02097
p2	3.056e+04 ± 4.894
p3	28.26 ± 0.01175

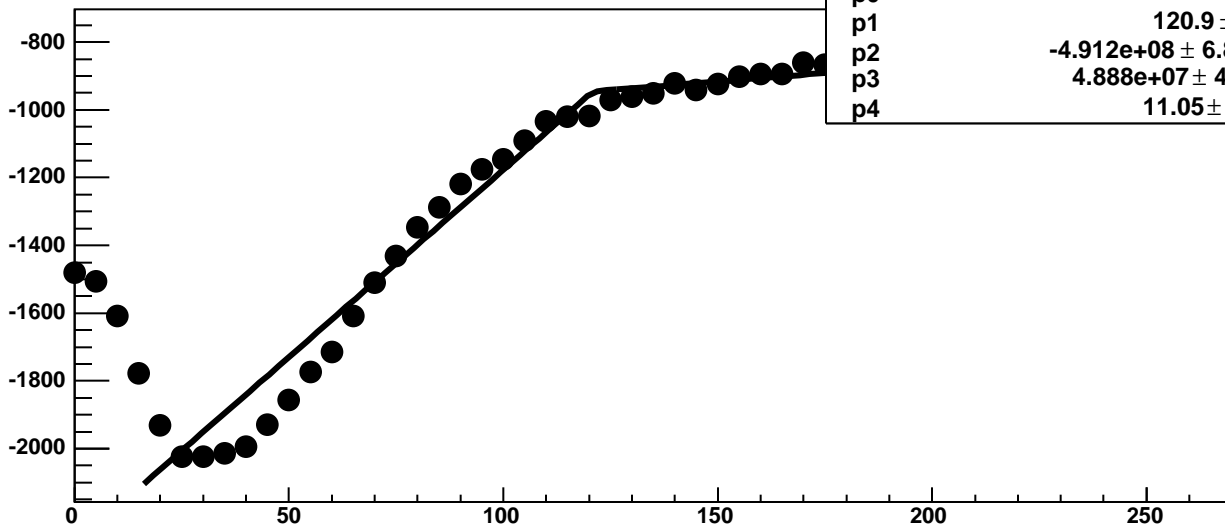
Chip 7, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

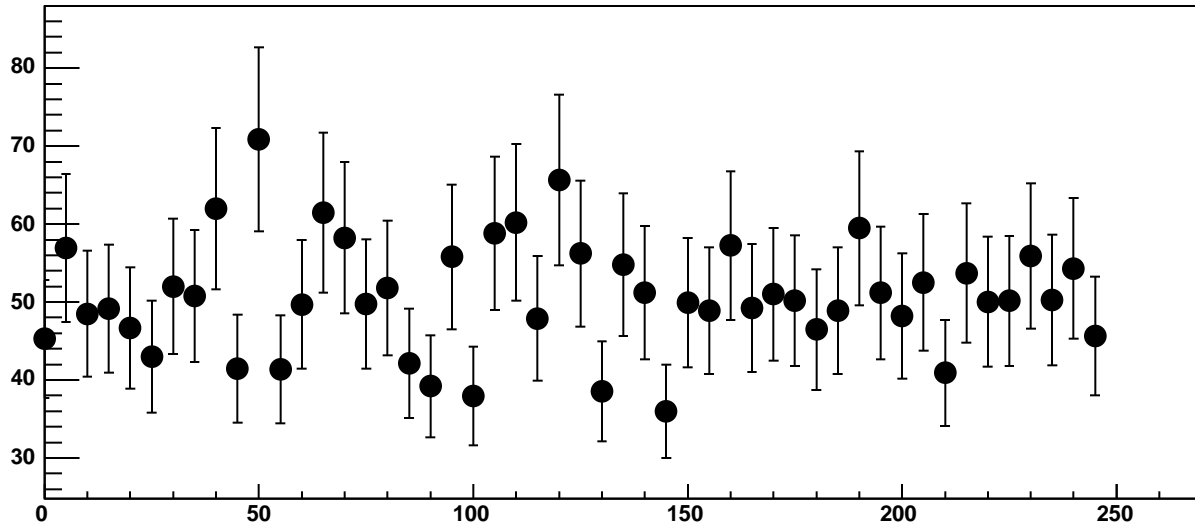


Chip 7, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

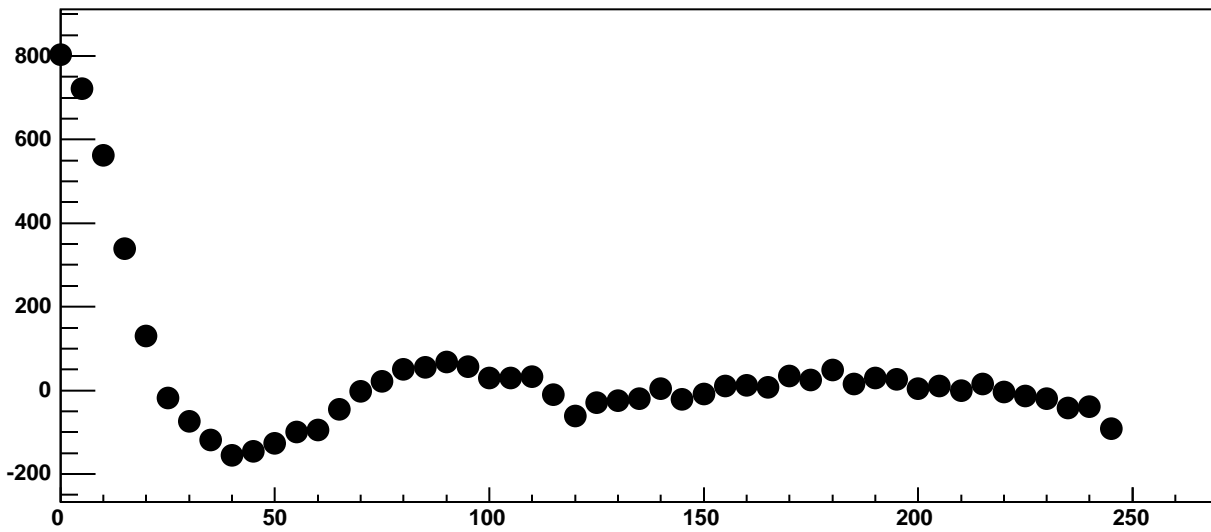


$\chi^2 / \text{ndf}$	2065 / 41
p0	-945.4 ± 5.034
p1	120.9 ± 0.6576
p2	-4.912e+08 ± 6.889e+06
p3	4.888e+07 ± 4.61e+05
p4	11.05 ± 0.07674

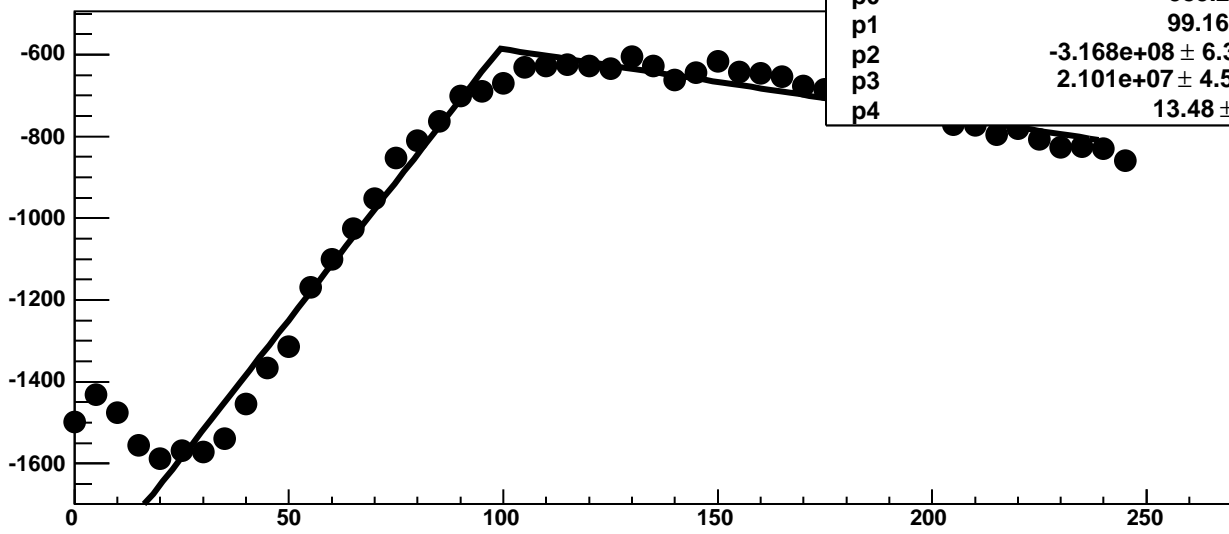
Chip 7, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

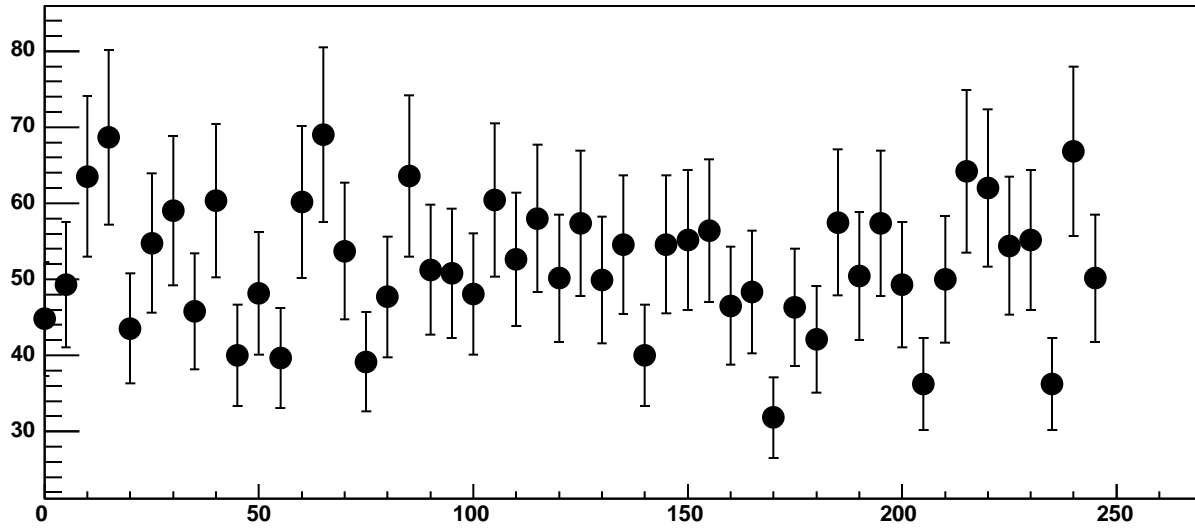


Chip 7, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

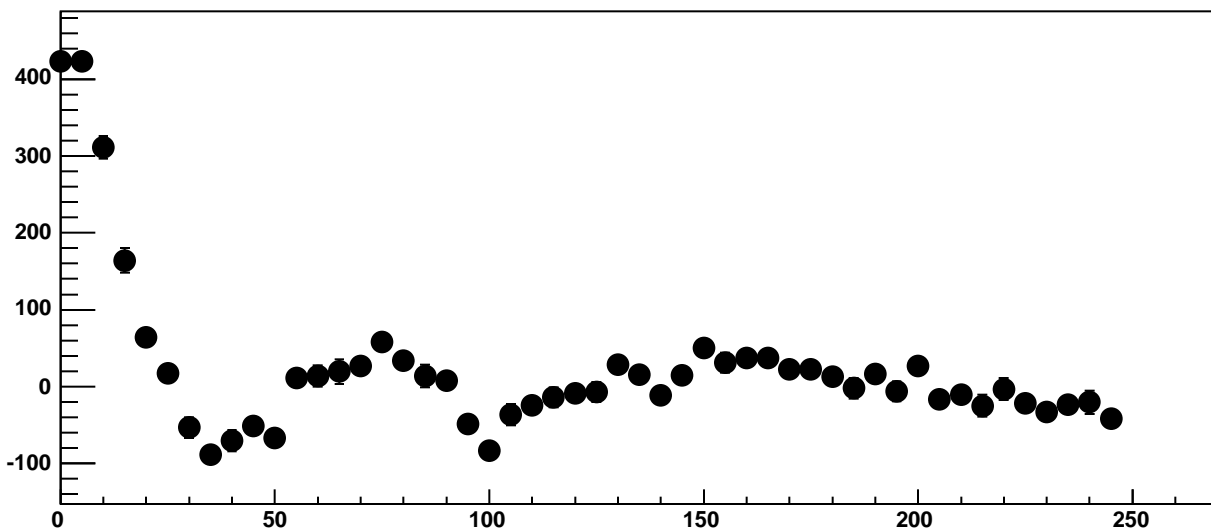


$\chi^2 / \text{ndf}$	588.6 / 41
p0	$-585.2 \pm 3.824$
p1	$99.16 \pm 0.453$
p2	$-3.168\text{e}+08 \pm 6.327\text{e}+06$
p3	$2.101\text{e}+07 \pm 4.531\text{e}+05$
p4	$13.48 \pm 0.1075$

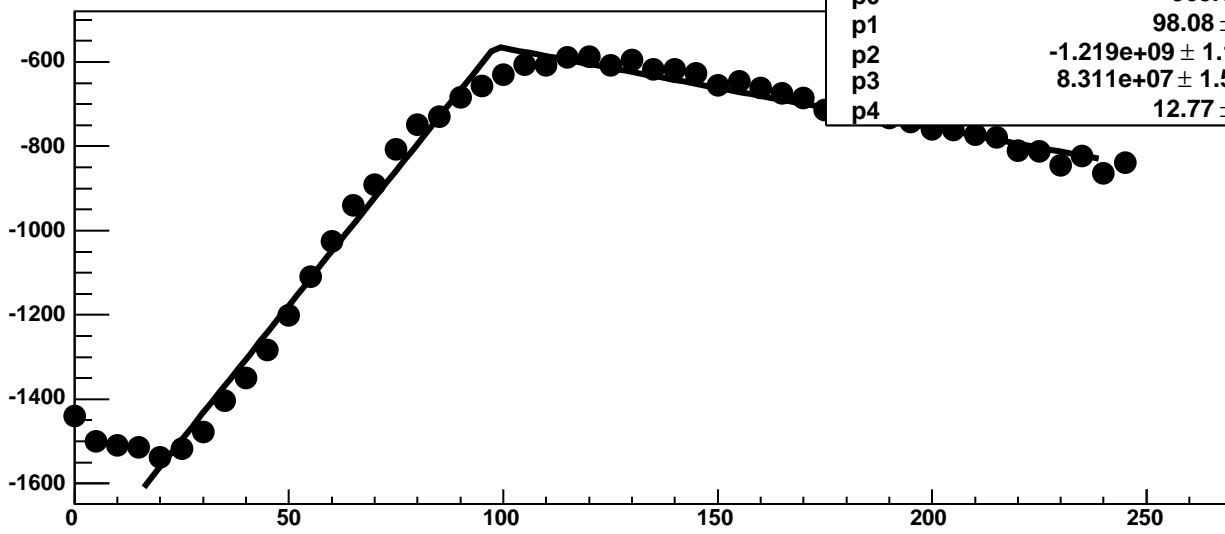
Chip 7, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

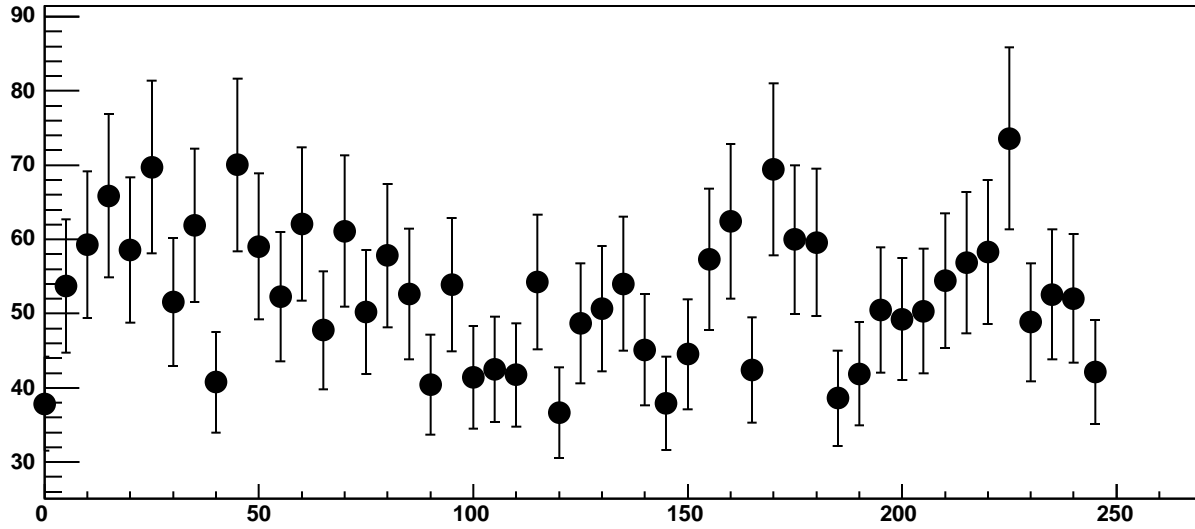


Chip 7, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold

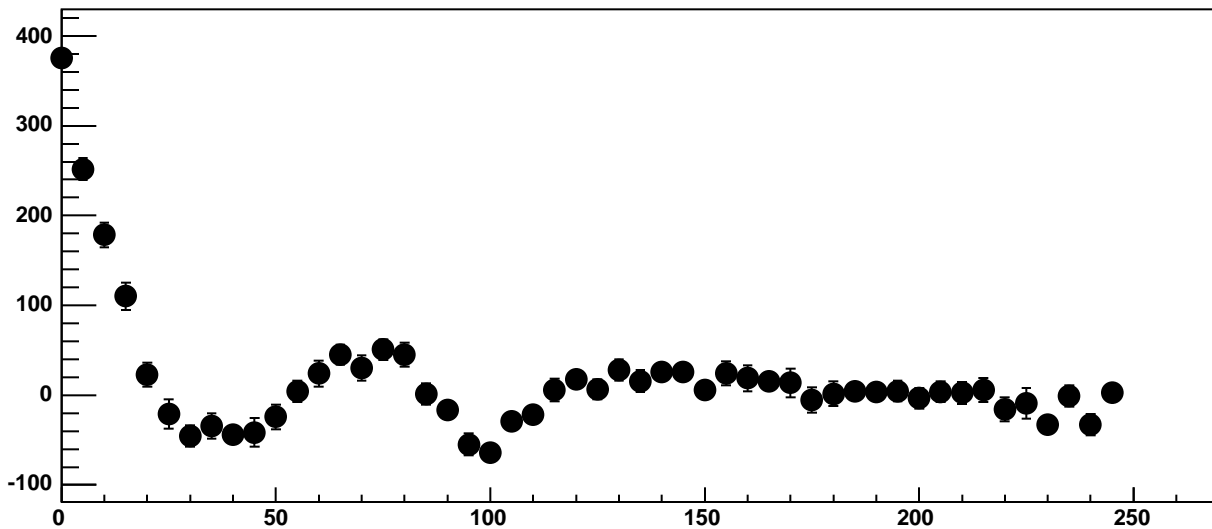


$\chi^2 / \text{ndf}$	304 / 41
p0	$-563.1 \pm 3.448$
p1	$98.08 \pm 0.4736$
p2	$-1.219\text{e}+09 \pm 1.122\text{e}+07$
p3	$8.311\text{e}+07 \pm 1.554\text{e}+05$
p4	$12.77 \pm 0.1234$

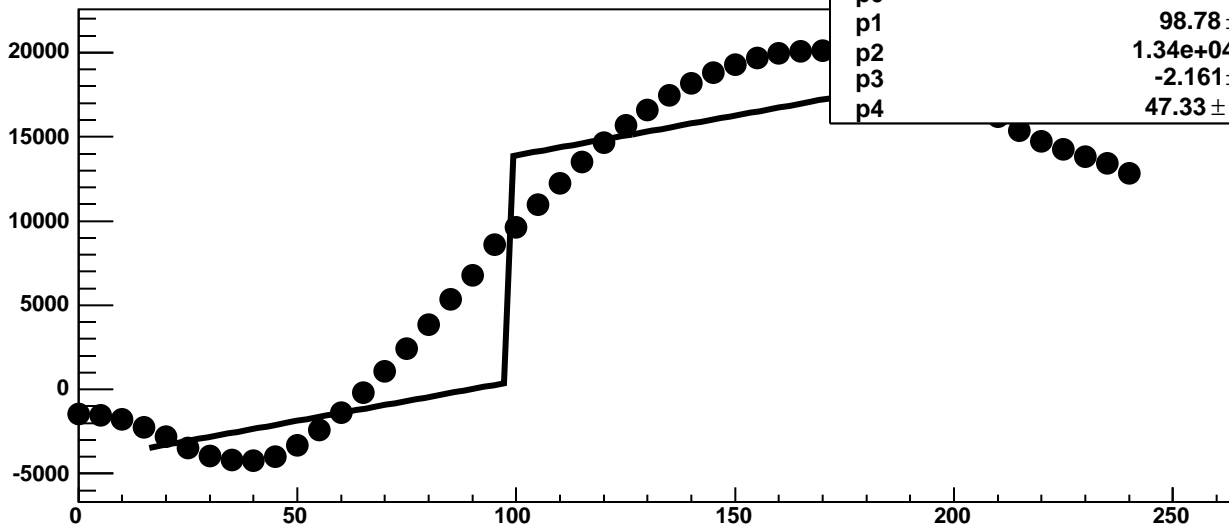
Chip 7, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

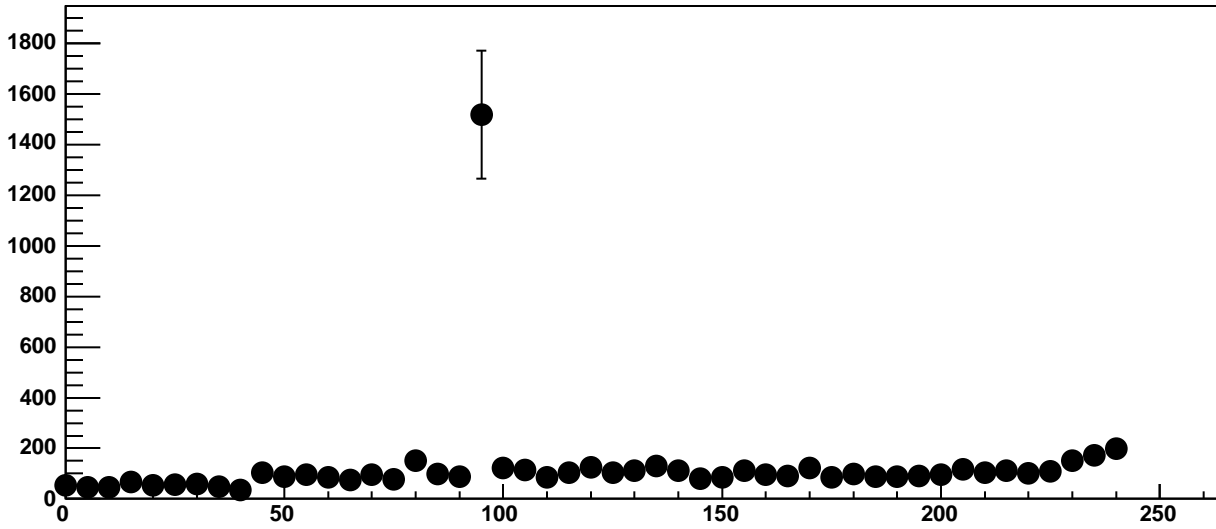


Chip 7, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

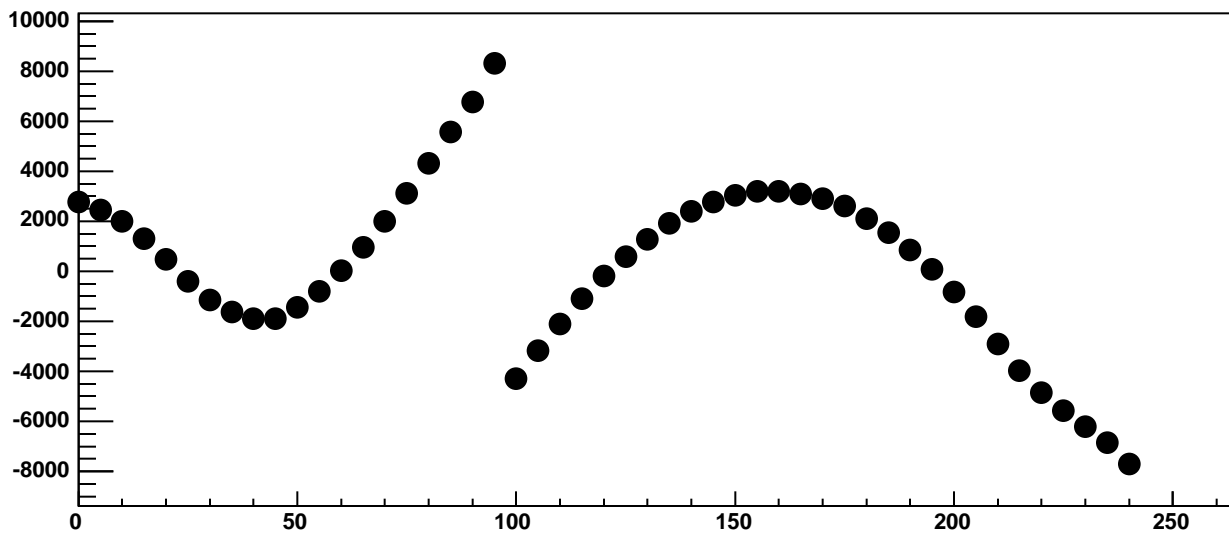


$\chi^2 / \text{ndf}$	7.8e+05 / 41
p0	441.1 ± 1.521
p1	98.78 ± 0.4792
p2	1.34e+04 ± 1.771
p3	-2.161 ± 0.4732
p4	47.33 ± 0.01767

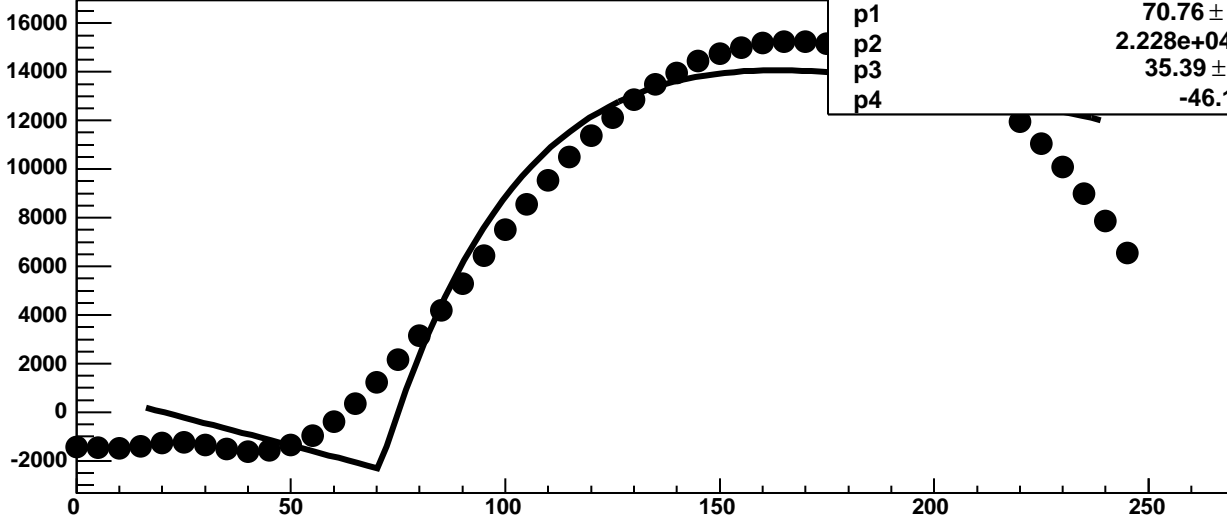
Chip 7, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

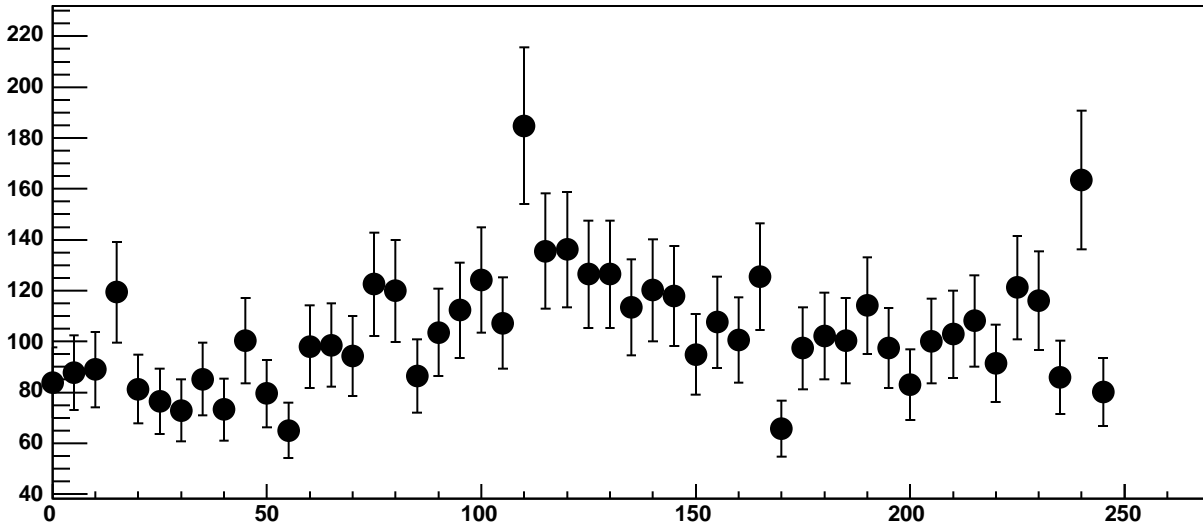


Chip 7, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

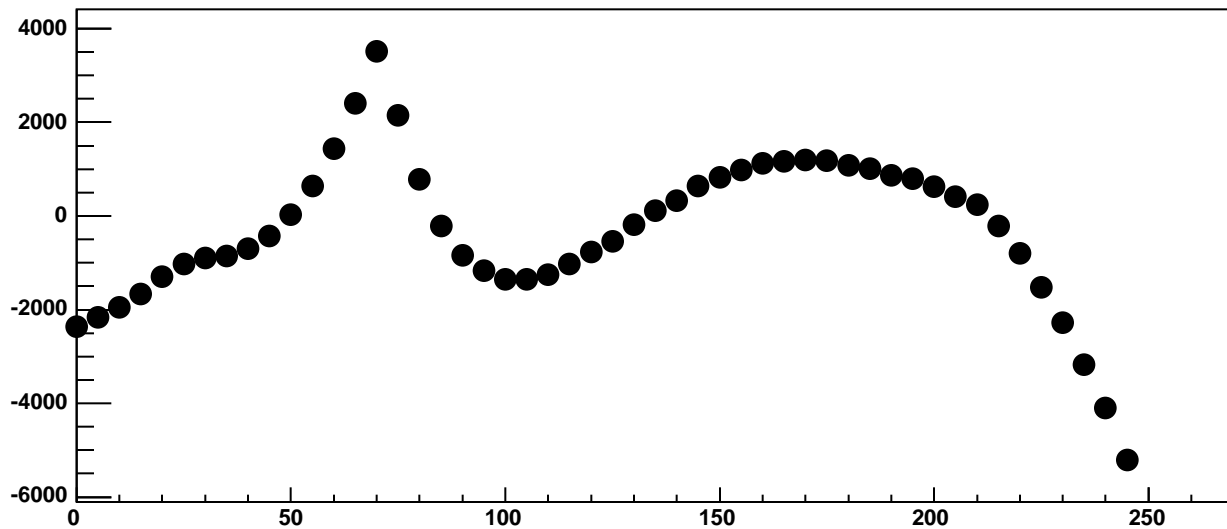


$\chi^2 / \text{ndf}$	1.553e+05 / 41
p0	-2323 $\pm$ 7.604
p1	70.76 $\pm$ 0.03805
p2	2.228e+04 $\pm$ 37.71
p3	35.39 $\pm$ 0.08621
p4	-46.1 $\pm$ 0.208

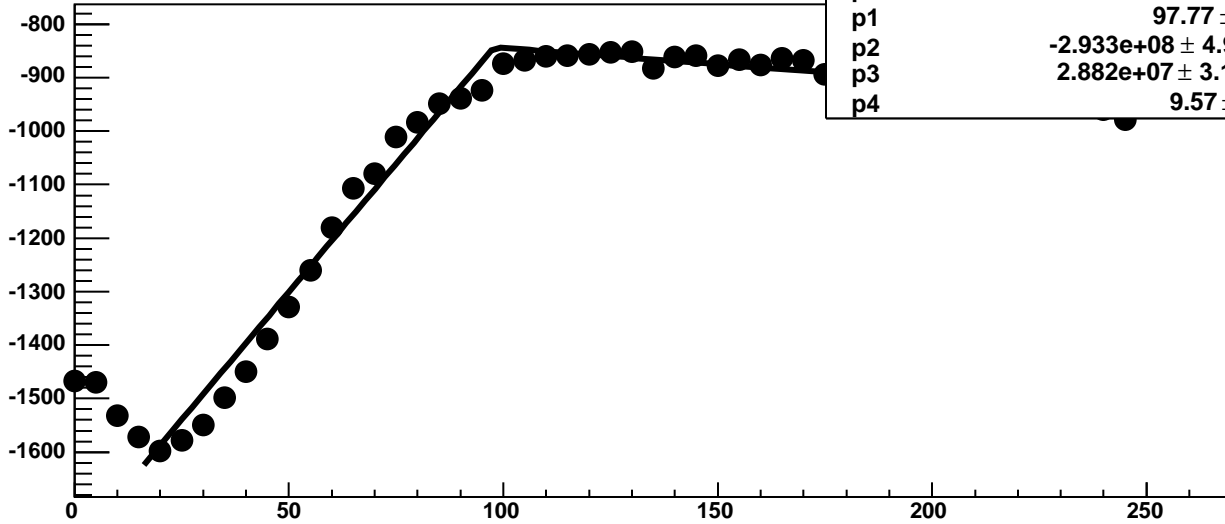
Chip 7, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

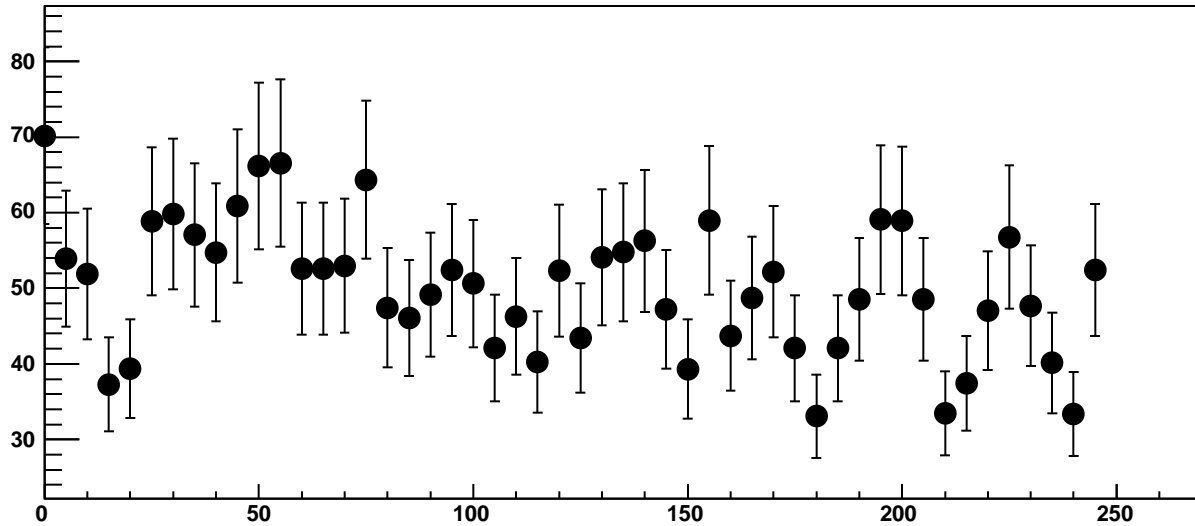


Chip 7, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold

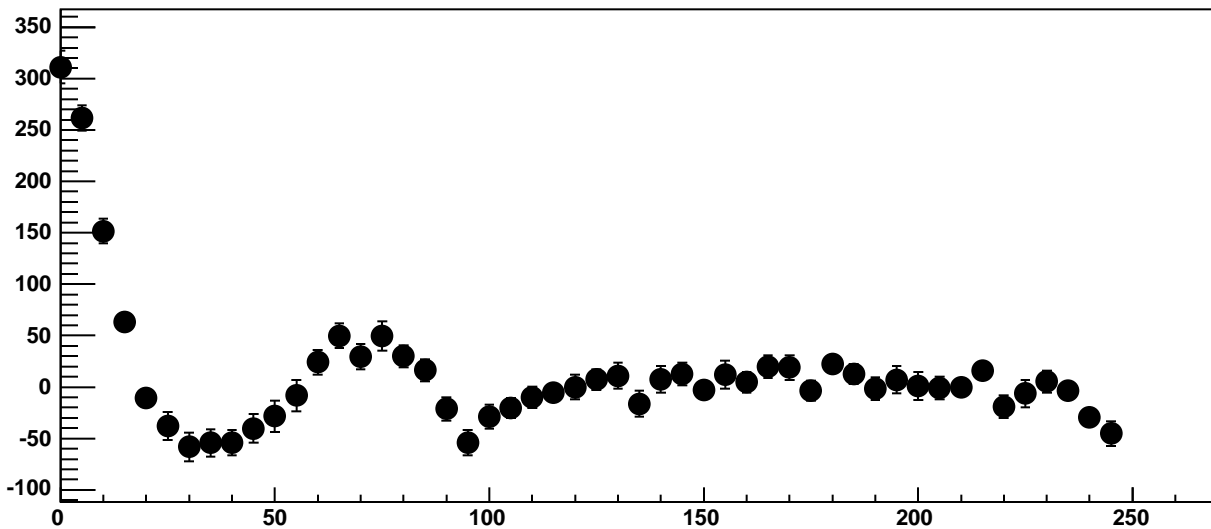


$\chi^2 / \text{ndf}$	259.4 / 41
p0	-843.2 ± 3.689
p1	97.77 ± 0.6696
p2	-2.933e+08 ± 4.914e+06
p3	2.882e+07 ± 3.172e+05
p4	9.57 ± 0.1069

Chip 7, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

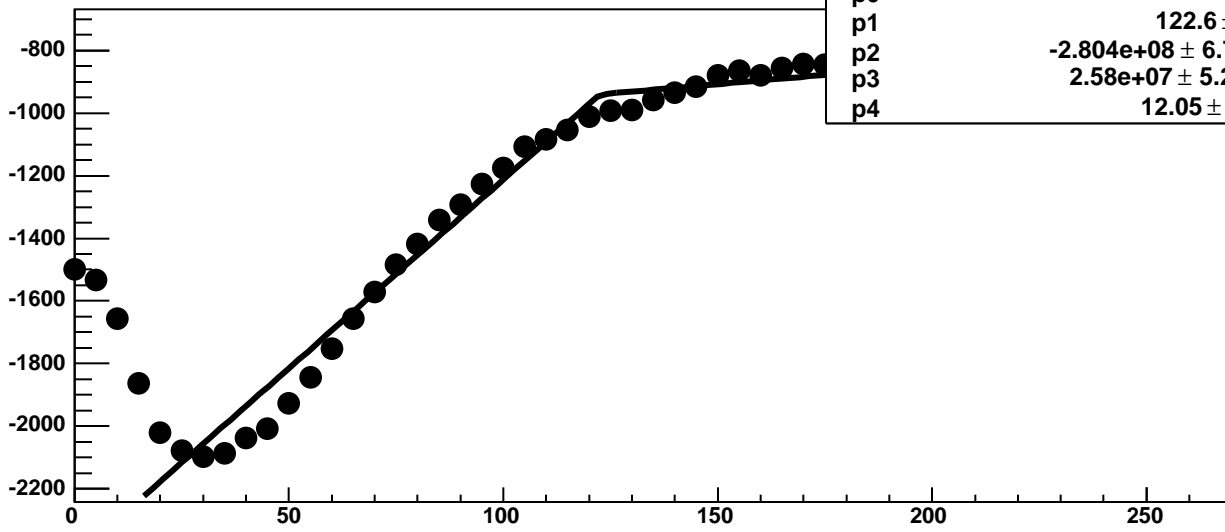


Chip 7, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold



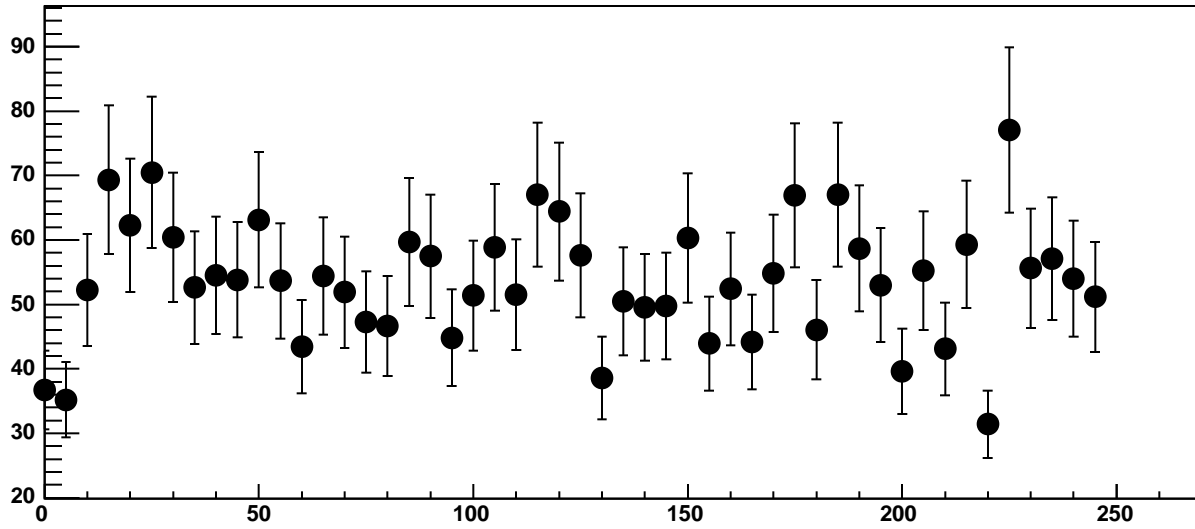


Chip 7, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

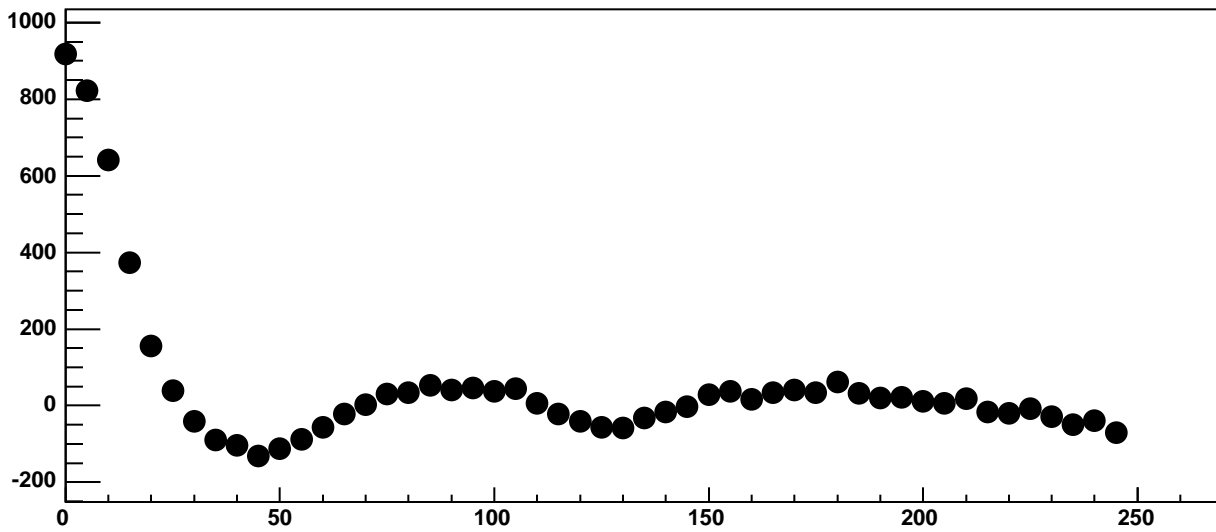


$\chi^2 / \text{ndf}$	1371 / 41
p0	-940.1 ± 5.191
p1	122.6 ± 0.6712
p2	-2.804e+08 ± 6.711e+06
p3	2.58e+07 ± 5.287e+05
p4	12.05 ± 0.09248

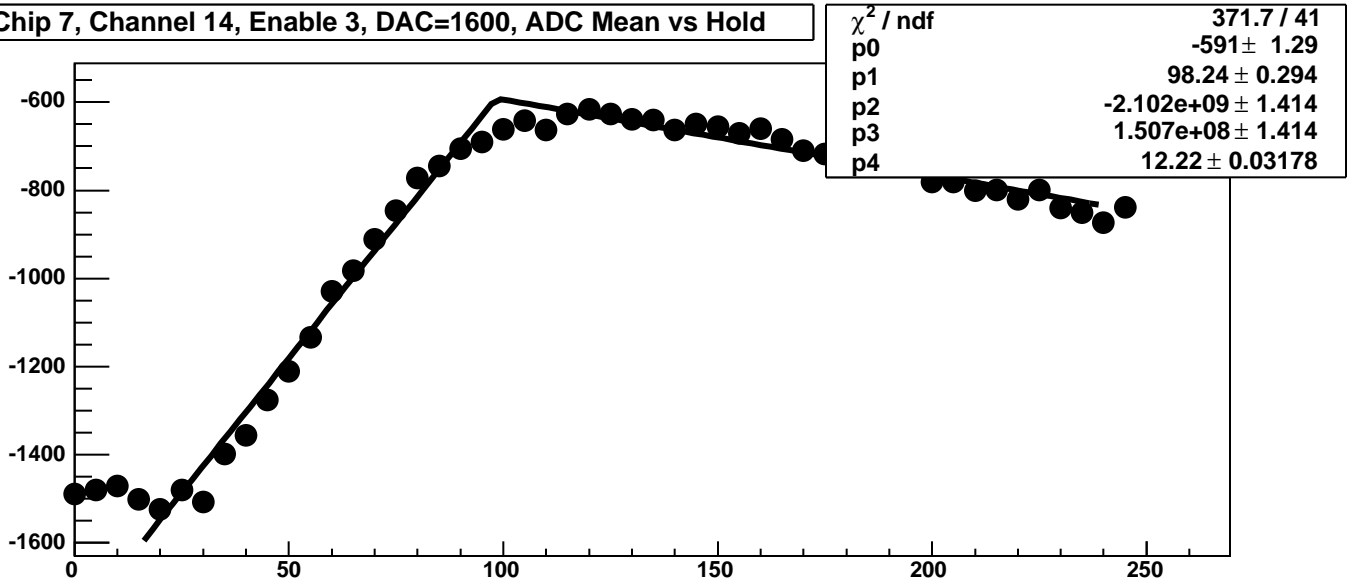
Chip 7, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



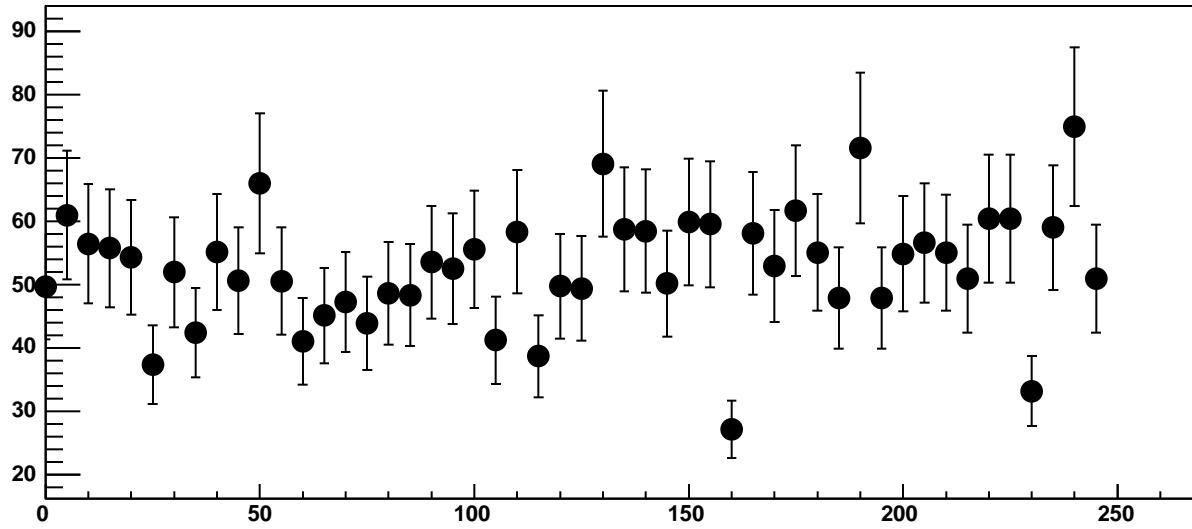
Chip 7, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold



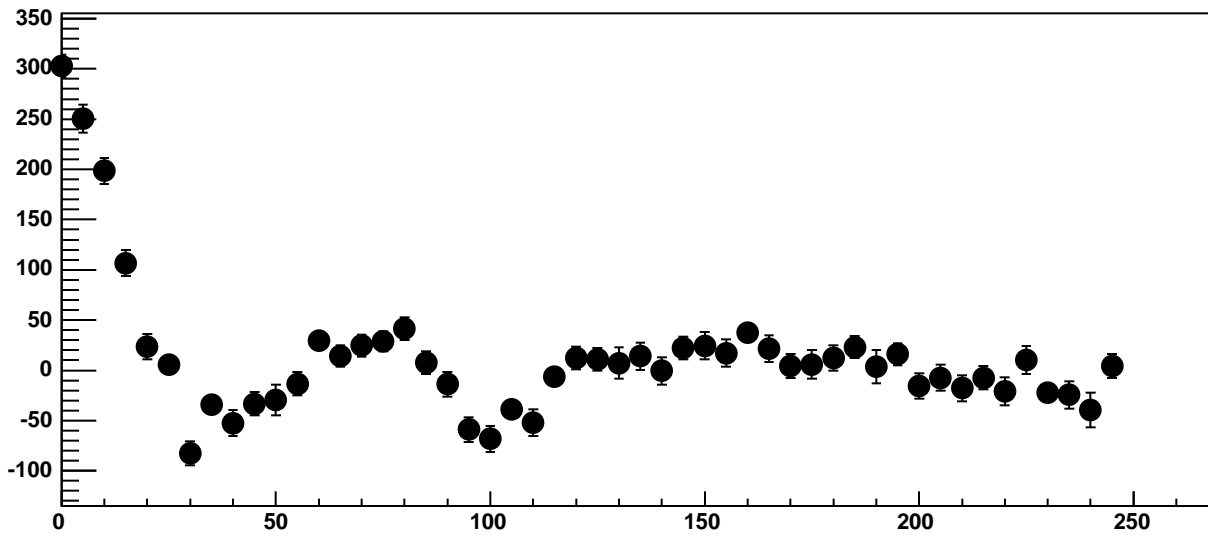
Chip 7, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold



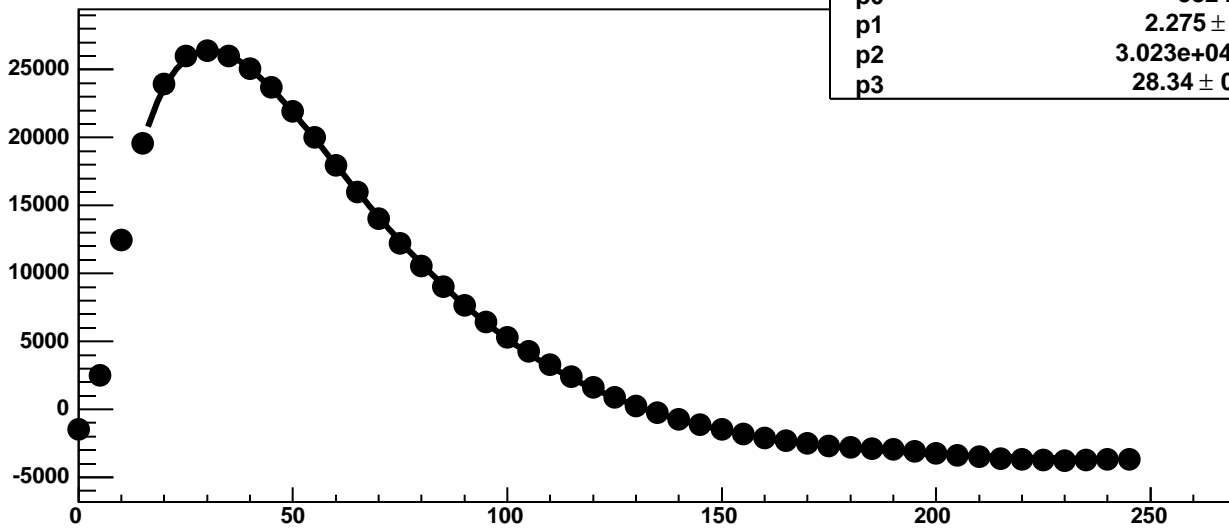
Chip 7, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

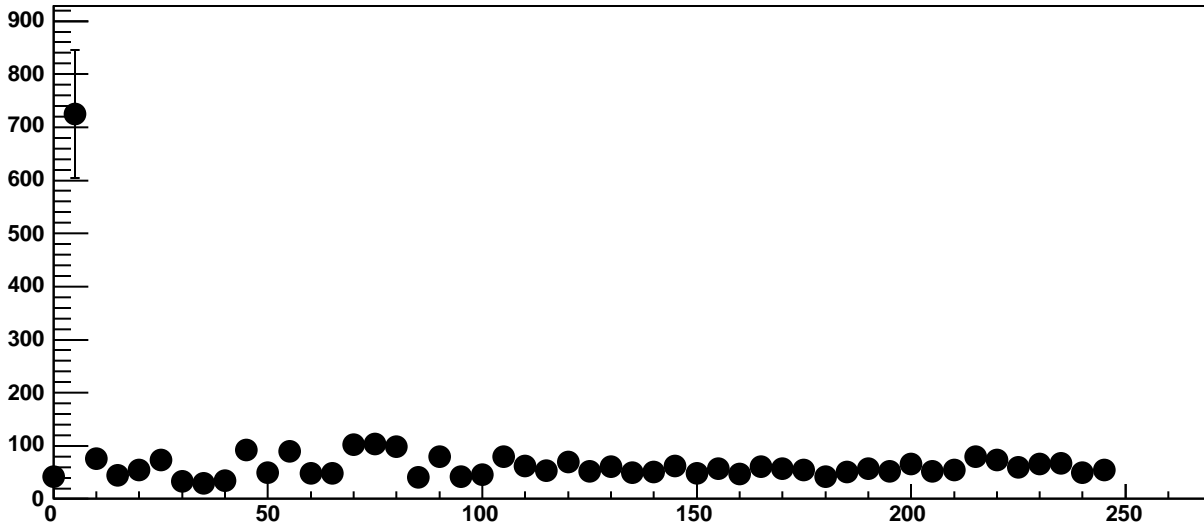


Chip 7, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold

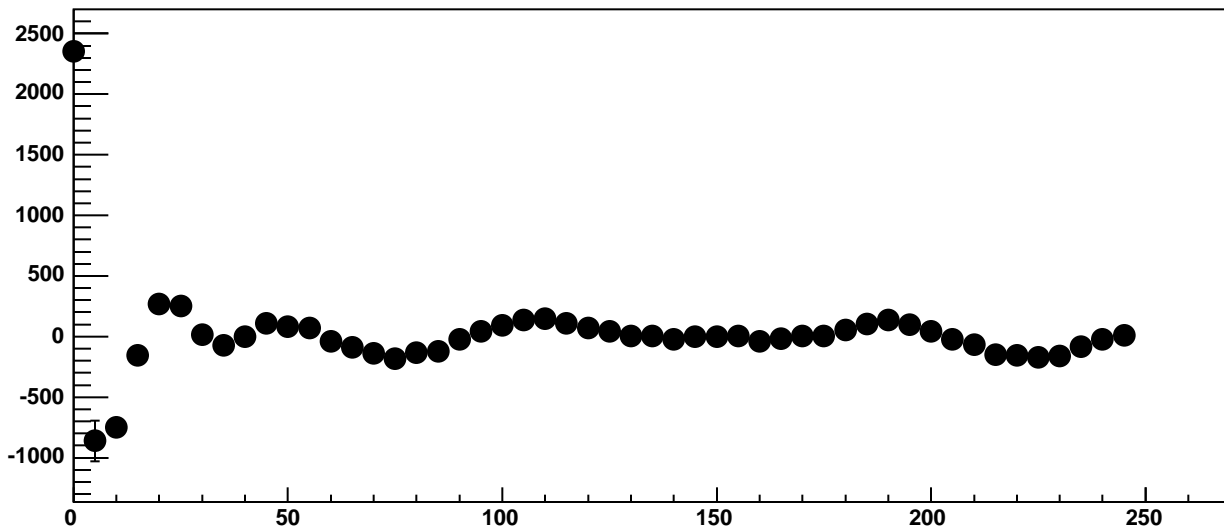


$\chi^2 / \text{ndf}$	2644 / 42
p0	-3824 ± 3.576
p1	2.275 ± 0.01225
p2	3.023e+04 ± 4.683
p3	28.34 ± 0.009262

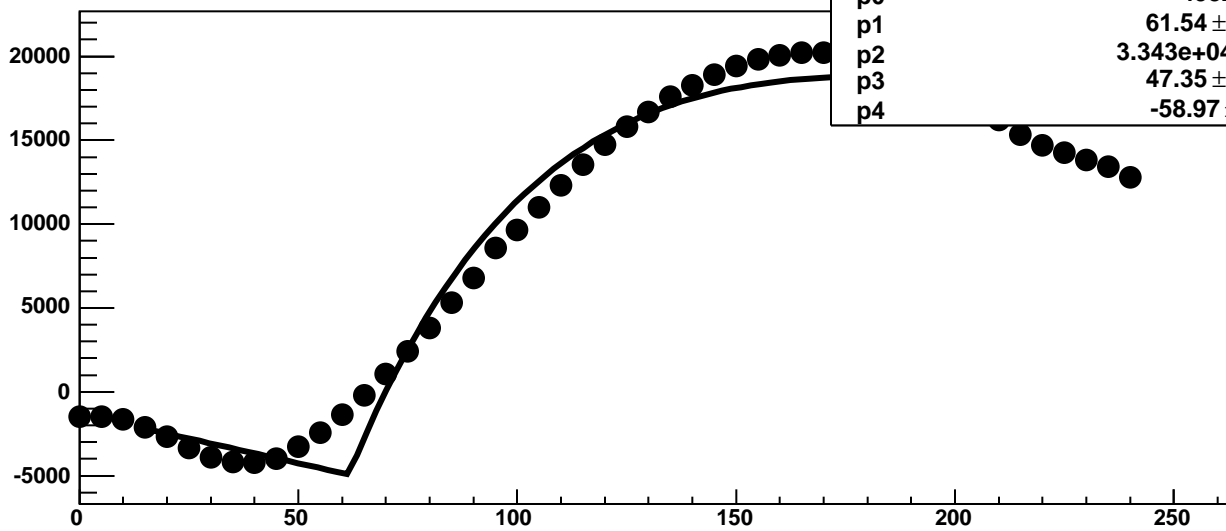
Chip 7, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold

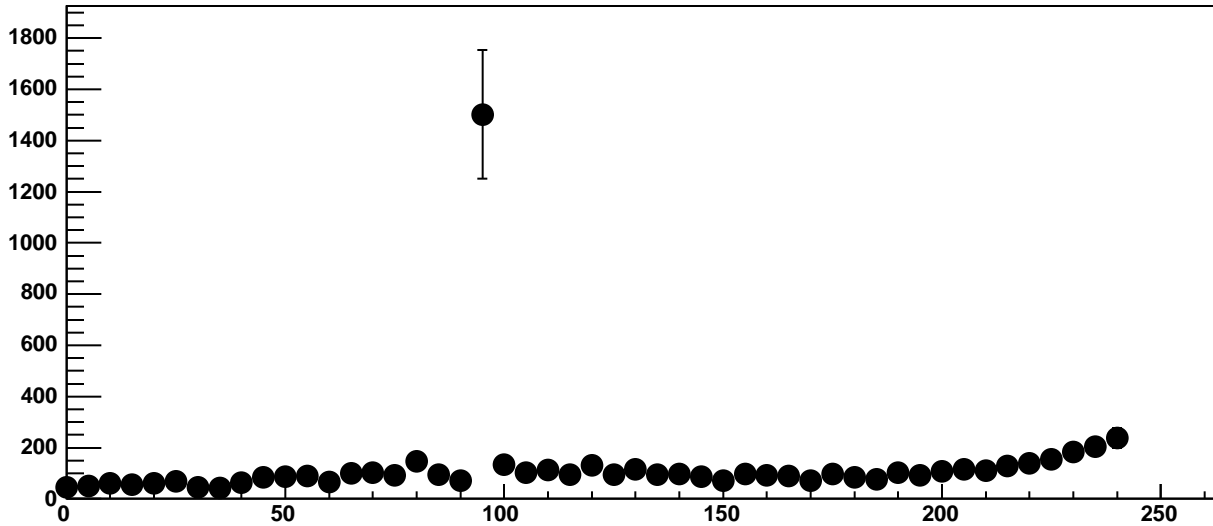


Chip 7, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

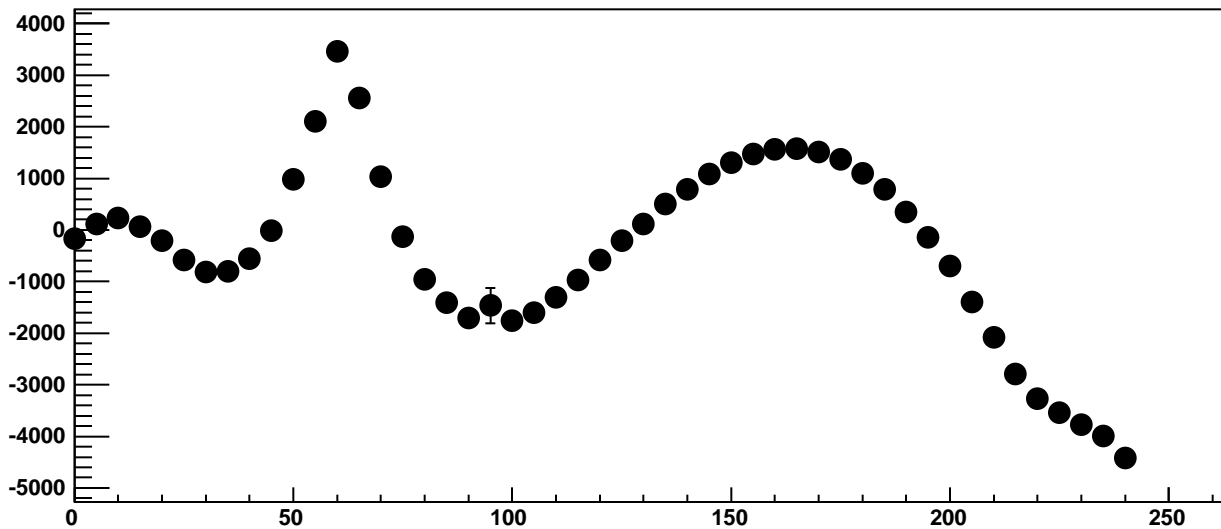


$\chi^2 / \text{ndf}$	2.278e+05 / 41
p0	-4932 ± 7.658
p1	61.54 ± 0.02715
p2	3.343e+04 ± 50.92
p3	47.35 ± 0.08174
p4	-58.97 ± 0.2554

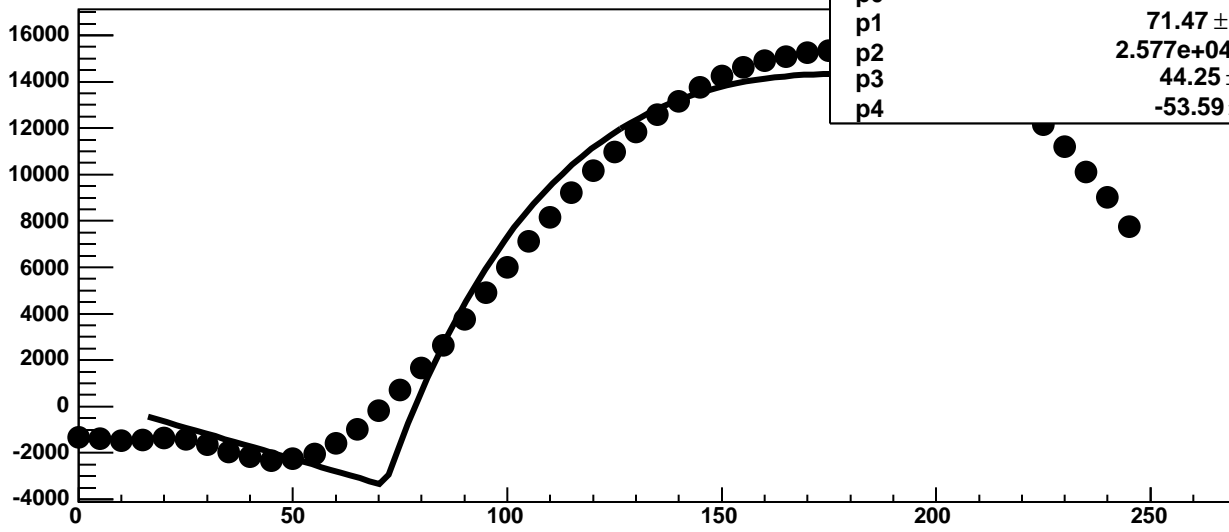
Chip 7, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

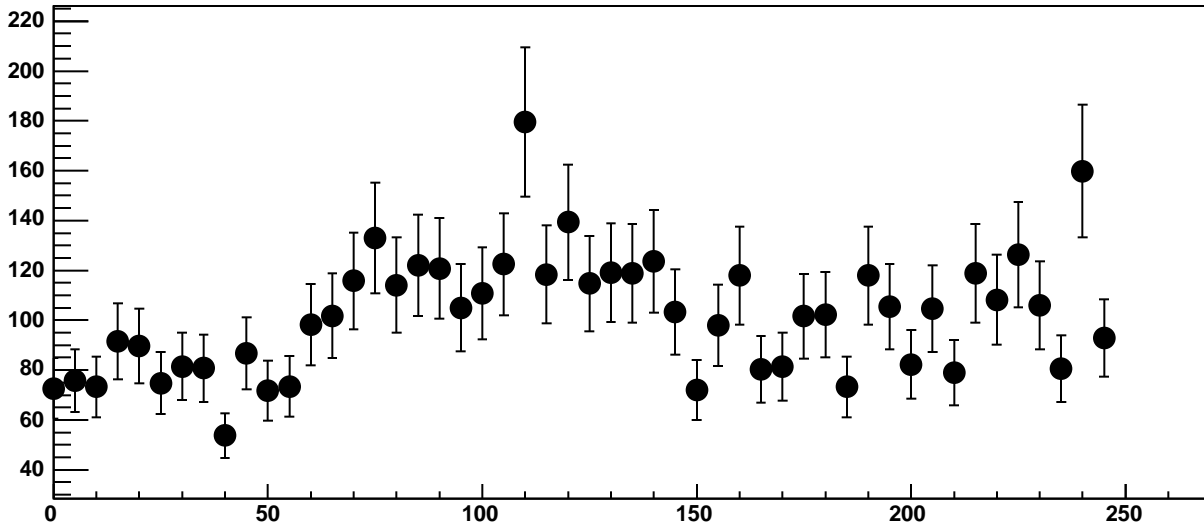


Chip 7, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

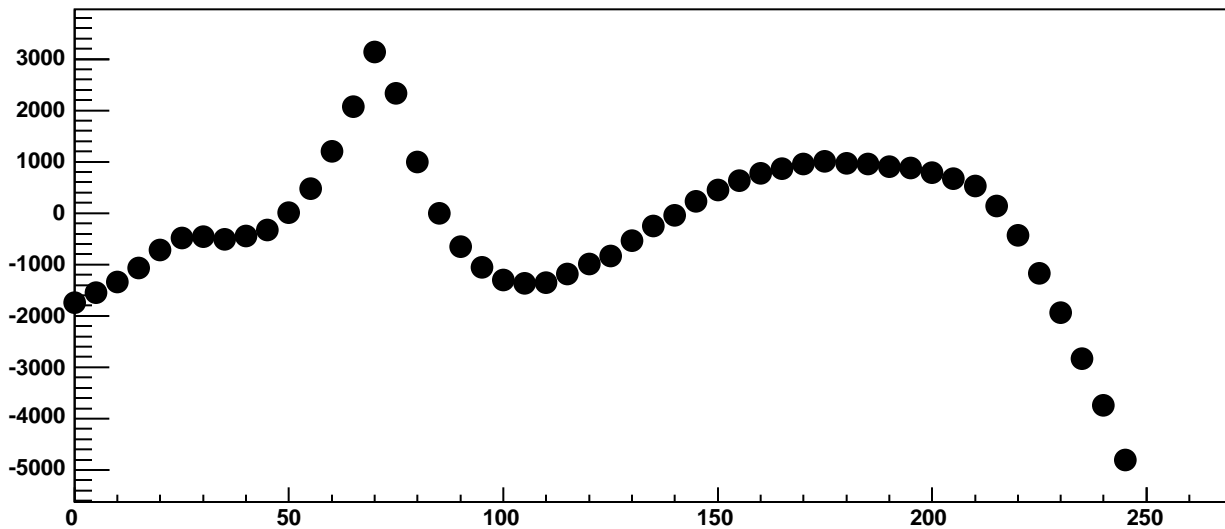


$\chi^2 / \text{ndf}$	1.154e+05 / 41
p0	-3405 ± 8.788
p1	71.47 ± 0.04041
p2	2.577e+04 ± 52.49
p3	44.25 ± 0.1078
p4	-53.59 ± 0.2621

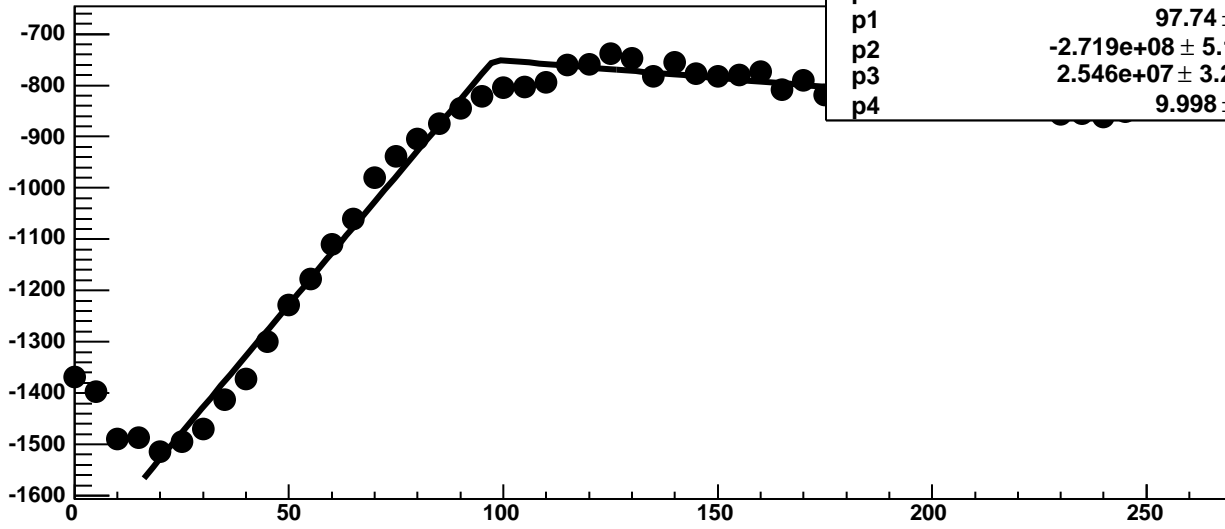
Chip 7, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

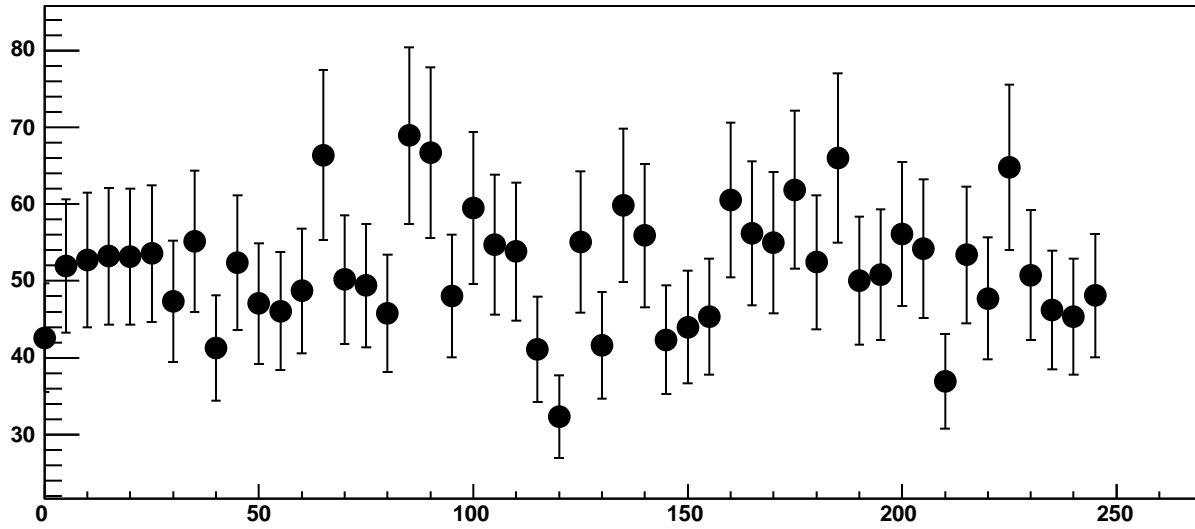


Chip 7, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

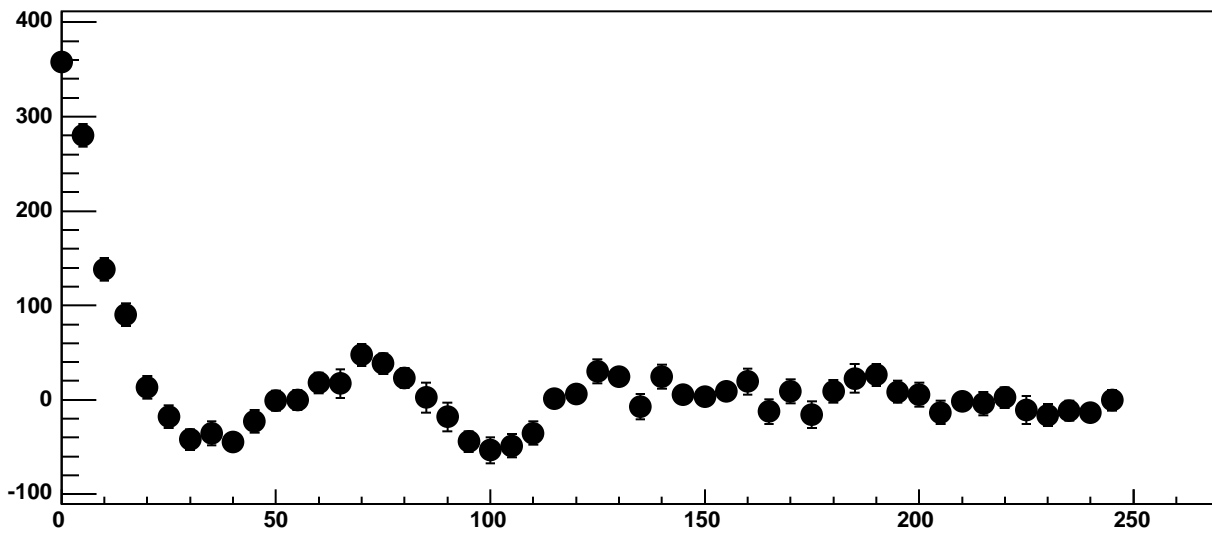


$\chi^2 / \text{ndf}$	238.7 / 41
p0	$-750 \pm 3.93$
p1	$97.74 \pm 0.6779$
p2	$-2.719\text{e}+08 \pm 5.151\text{e}+06$
p3	$2.546\text{e}+07 \pm 3.255\text{e}+05$
p4	$9.998 \pm 0.1203$

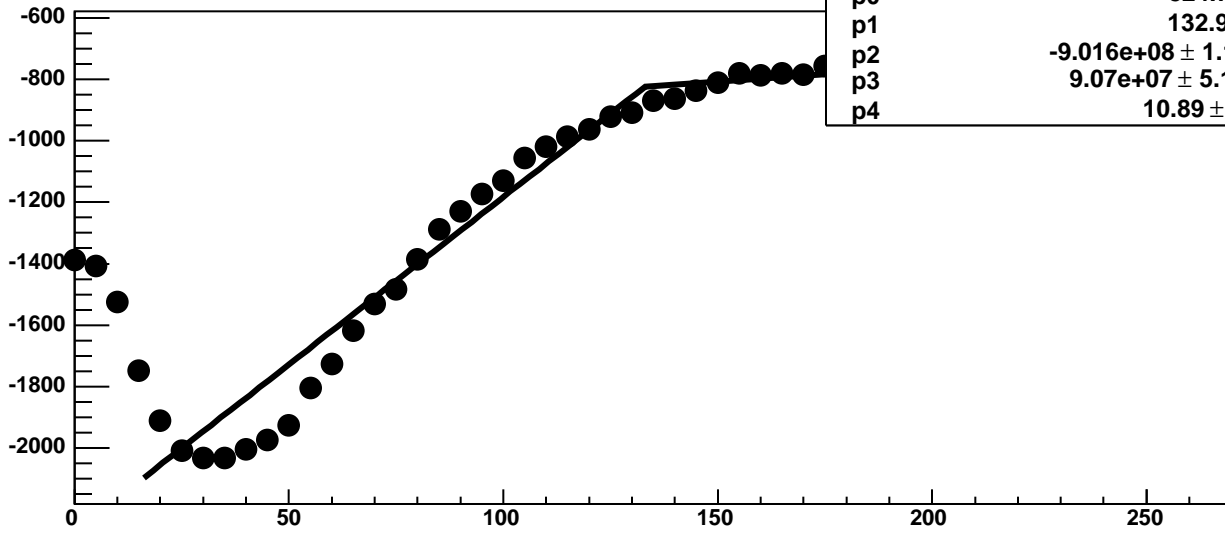
Chip 7, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

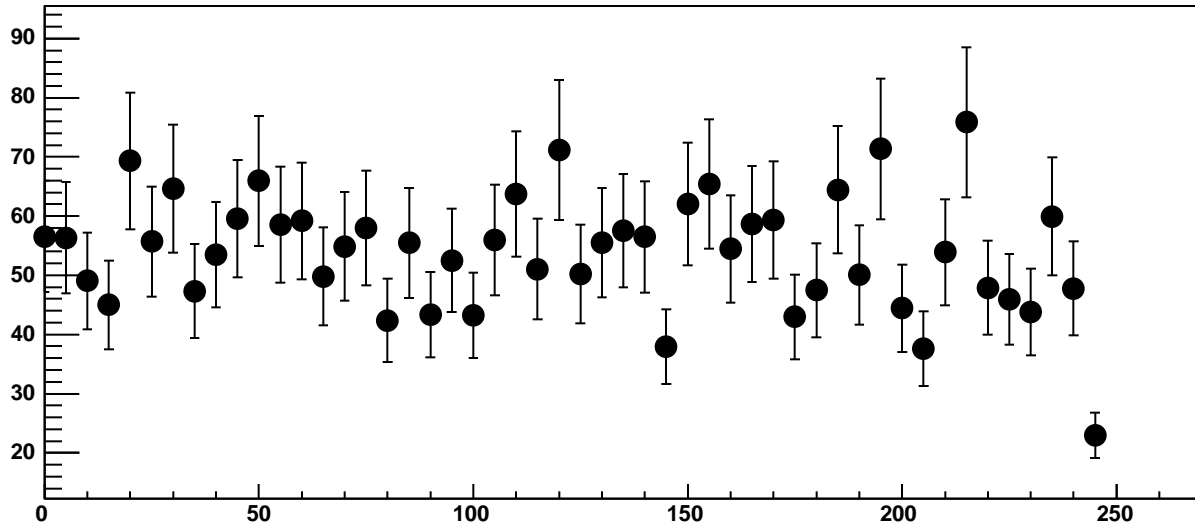


Chip 7, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

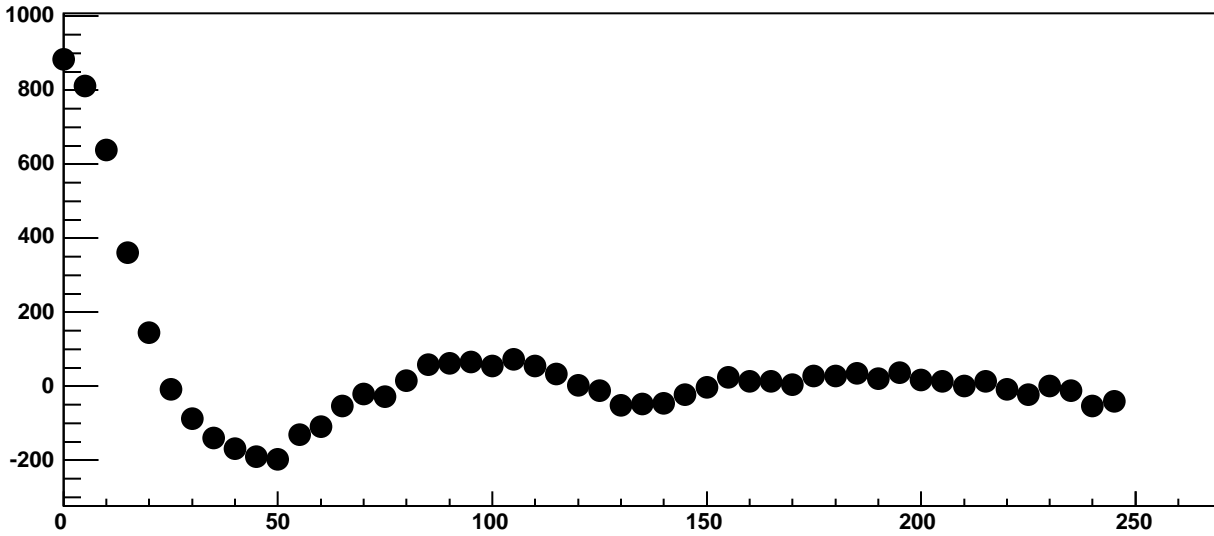


$\chi^2 / \text{ndf}$	2539 / 41
p0	$-824.7 \pm 5.598$
p1	$132.9 \pm 0.722$
p2	$-9.016\text{e}+08 \pm 1.106\text{e}+07$
p3	$9.07\text{e}+07 \pm 5.196\text{e}+05$
p4	$10.89 \pm 0.07381$

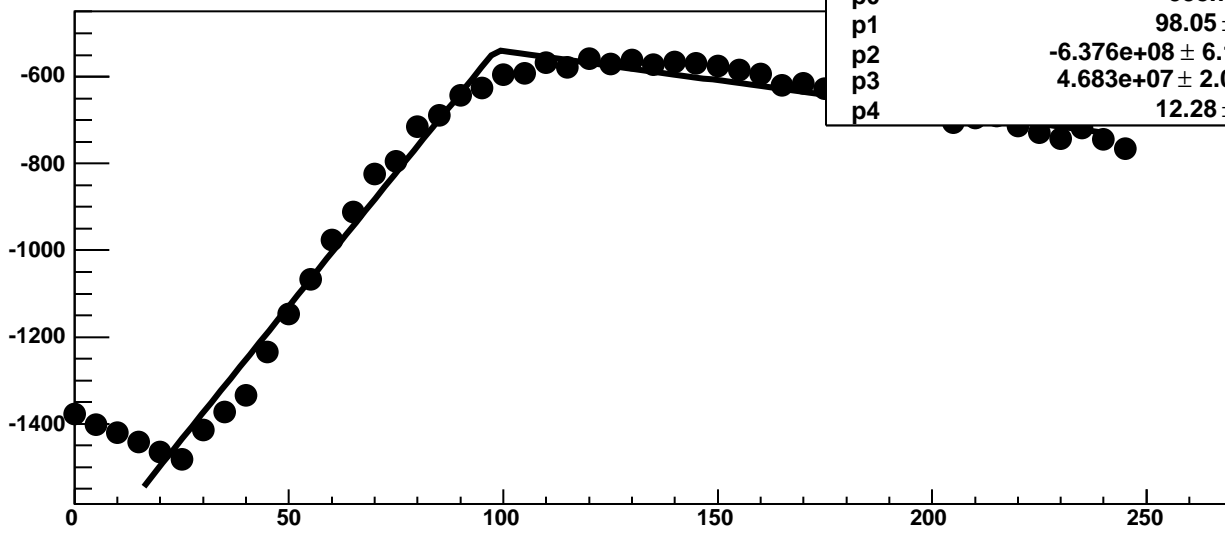
Chip 7, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold

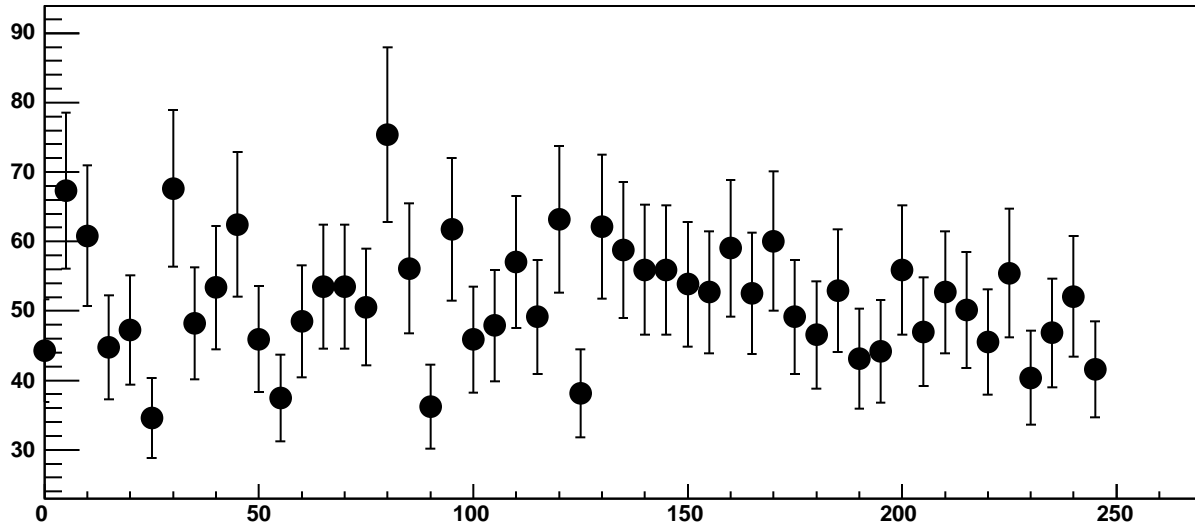


Chip 7, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

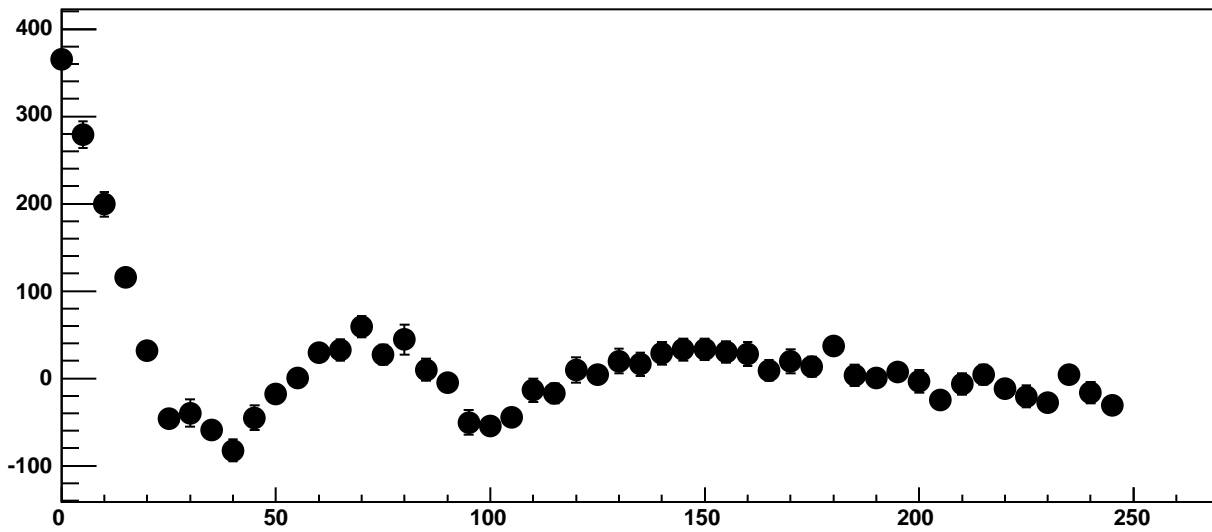


$\chi^2 / \text{ndf}$	443.1 / 41
p0	$-538.7 \pm 3.906$
p1	$98.05 \pm 0.5162$
p2	$-6.376e+08 \pm 6.192e+06$
p3	$4.683e+07 \pm 2.083e+05$
p4	$12.28 \pm 0.1079$

Chip 7, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

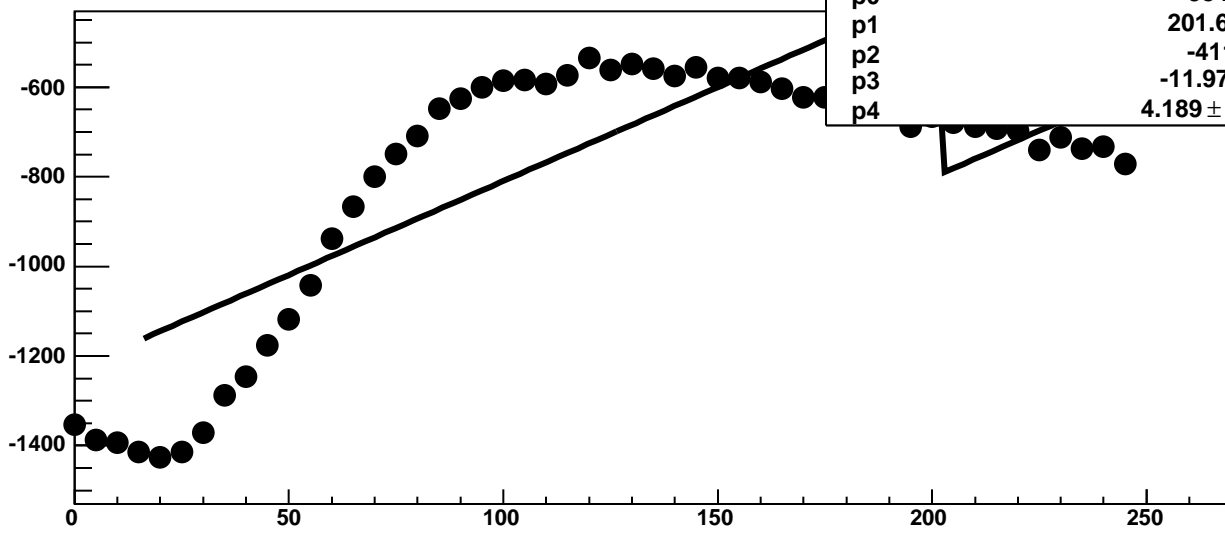


Chip 7, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold



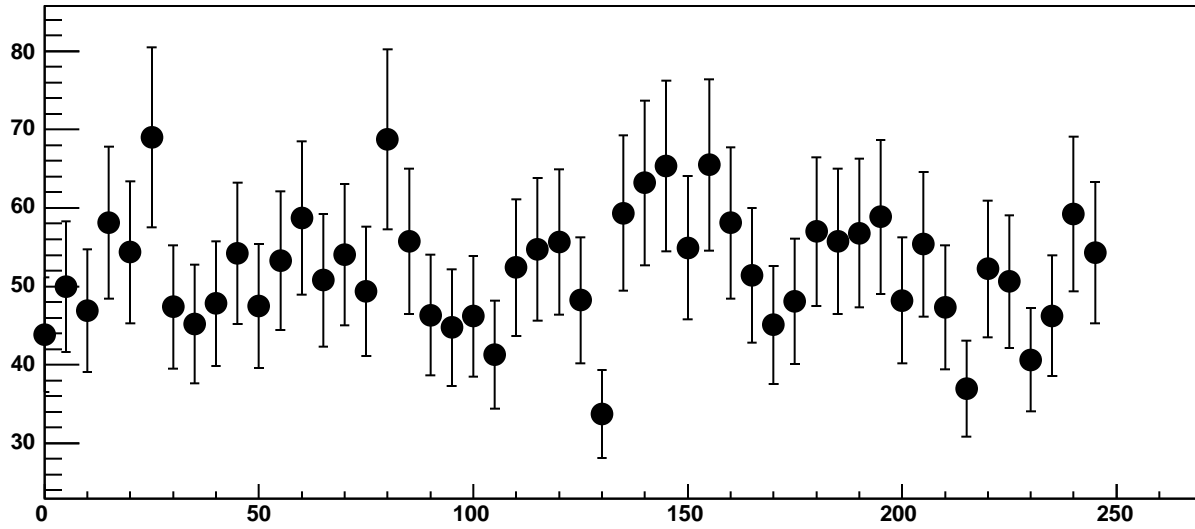


Chip 7, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

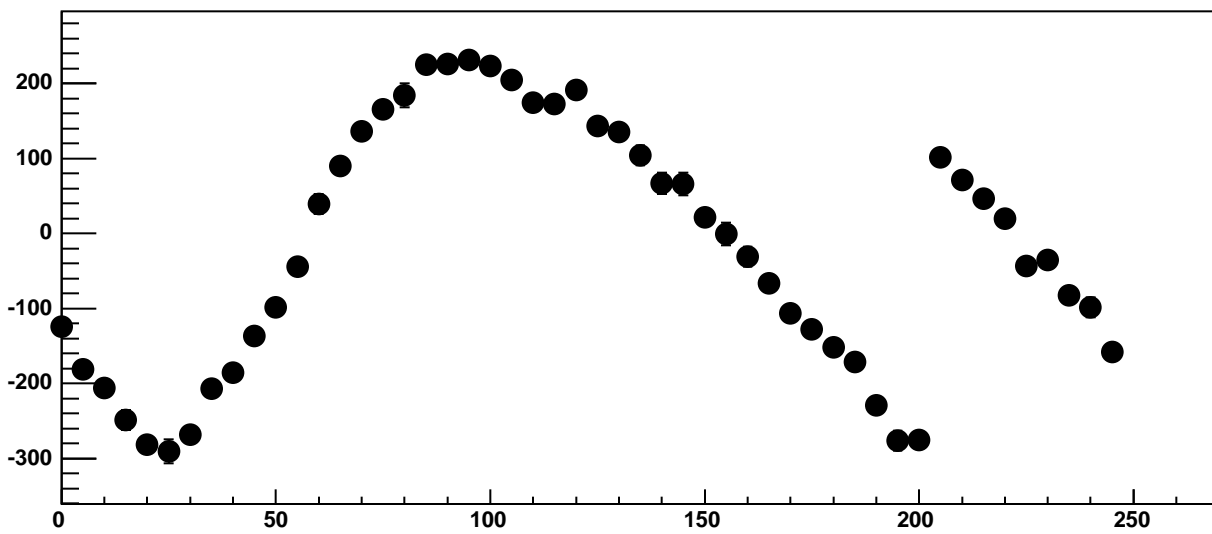


$\chi^2 / \text{ndf}$	8841 / 41
p0	$-384 \pm 17.26$
p1	$201.6 \pm 4.633$
p2	$-411 \pm 18.31$
p3	$-11.97 \pm 10.82$
p4	$4.189 \pm 0.01708$

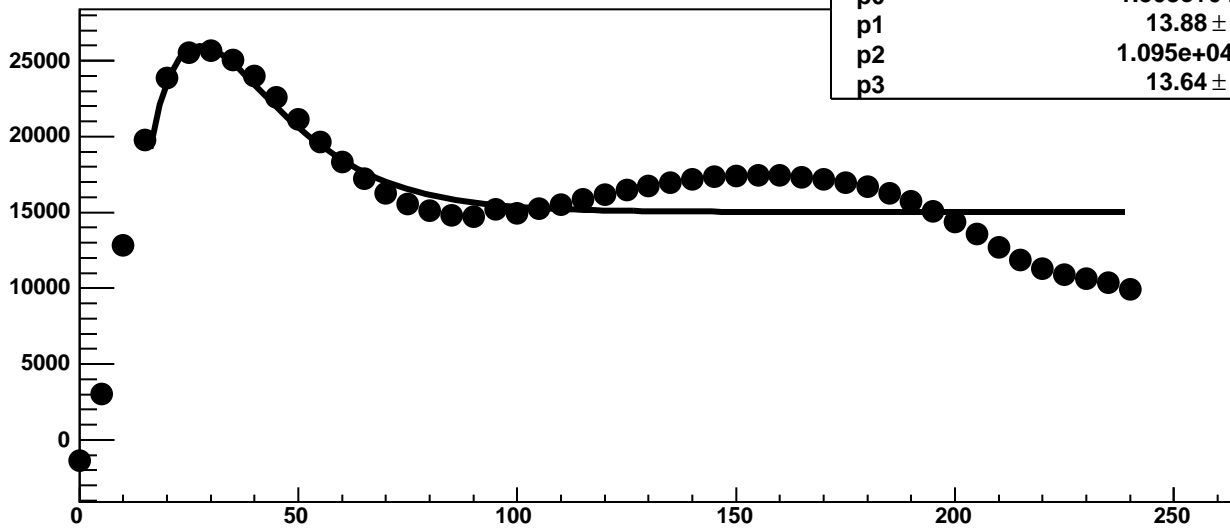
Chip 7, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

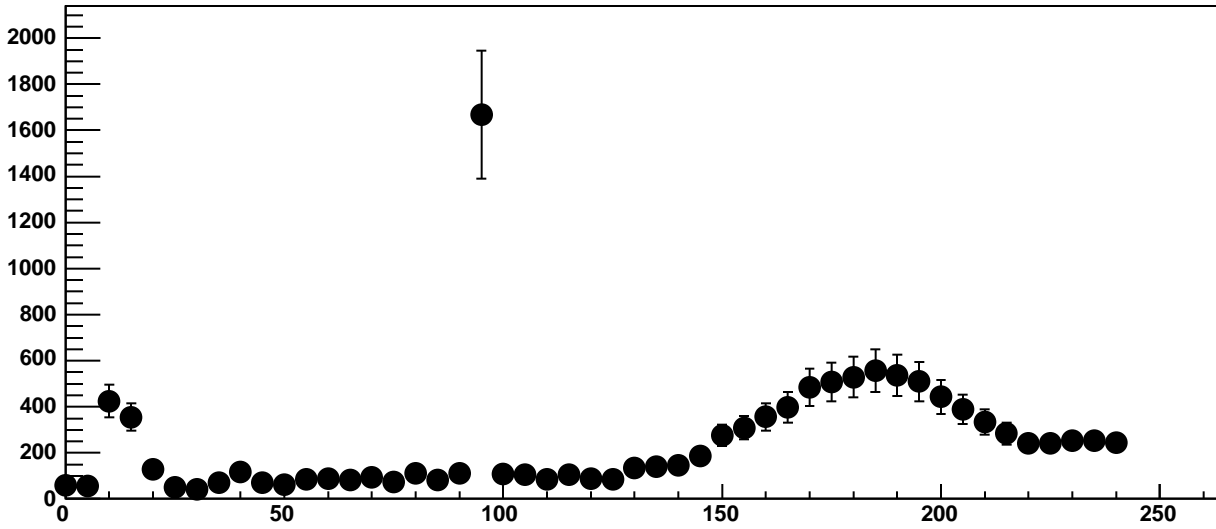


Chip 7, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold

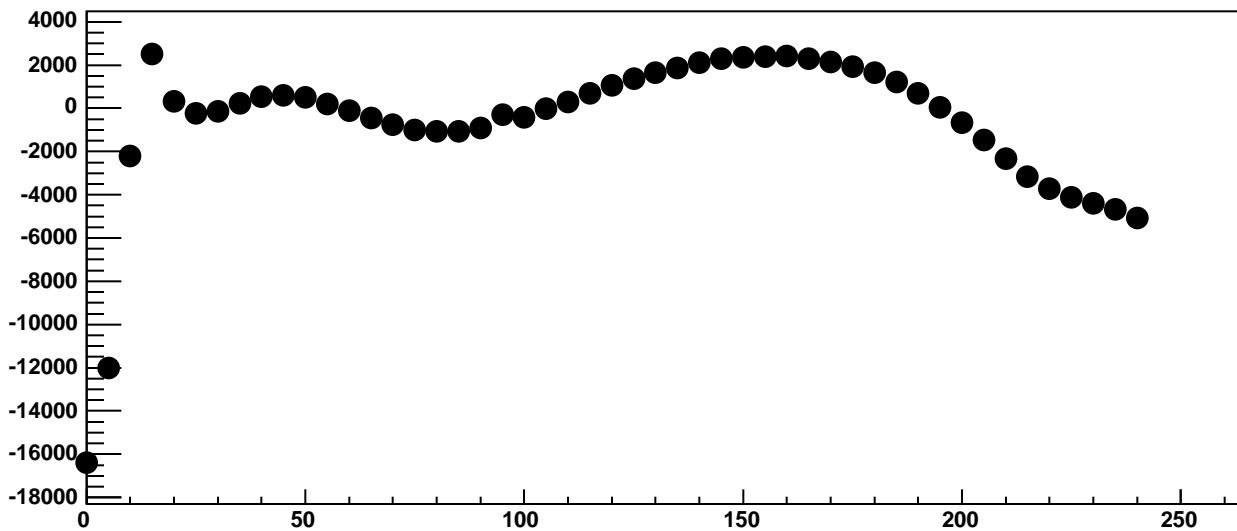


$\chi^2 / \text{ndf}$	7.796e+04 / 42
p0	1.503e+04 $\pm$ 6.831
p1	13.88 $\pm$ 0.02925
p2	1.095e+04 $\pm$ 9.447
p3	13.64 $\pm$ 0.01953

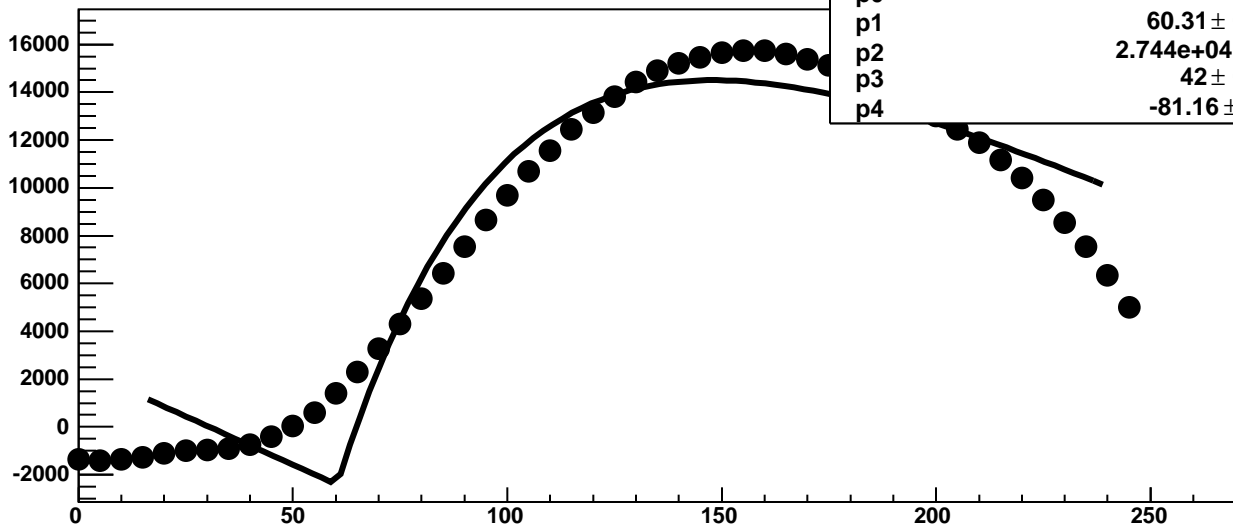
Chip 7, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

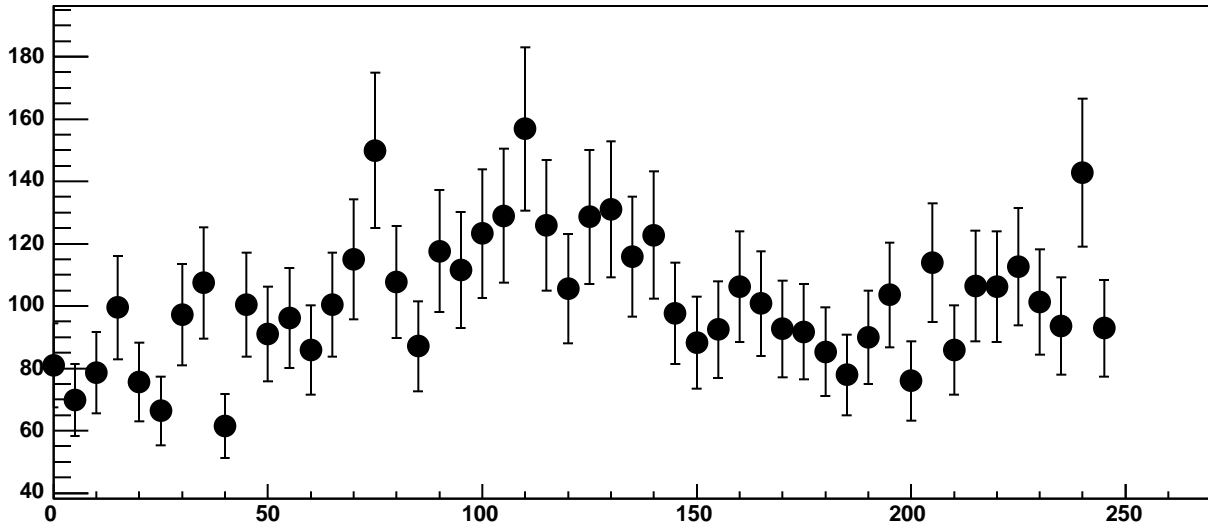


Chip 7, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

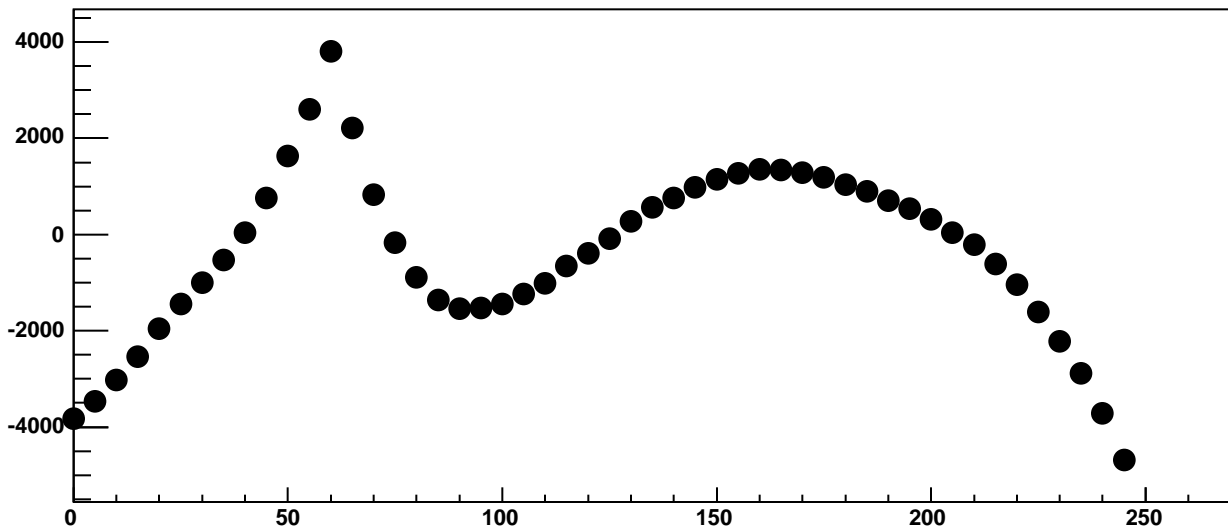


$\chi^2 / \text{ndf}$	2.008e+05 / 41
p0	-2420 ± 7.493
p1	60.31 ± 0.03342
p2	2.744e+04 ± 46.86
p3	42 ± 0.08886
p4	-81.16 ± 0.2426

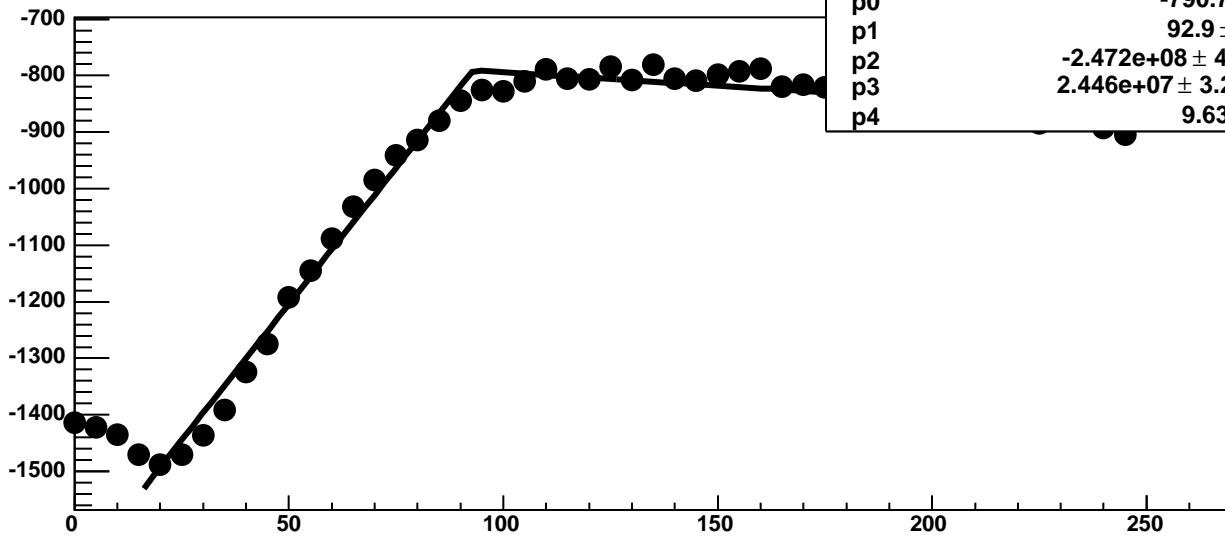
Chip 7, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

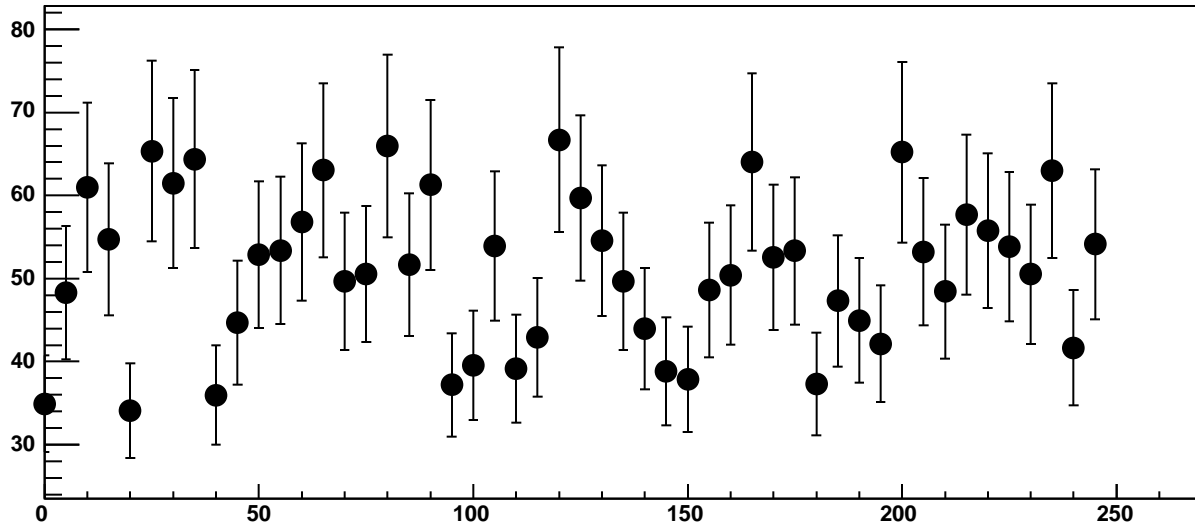


Chip 7, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

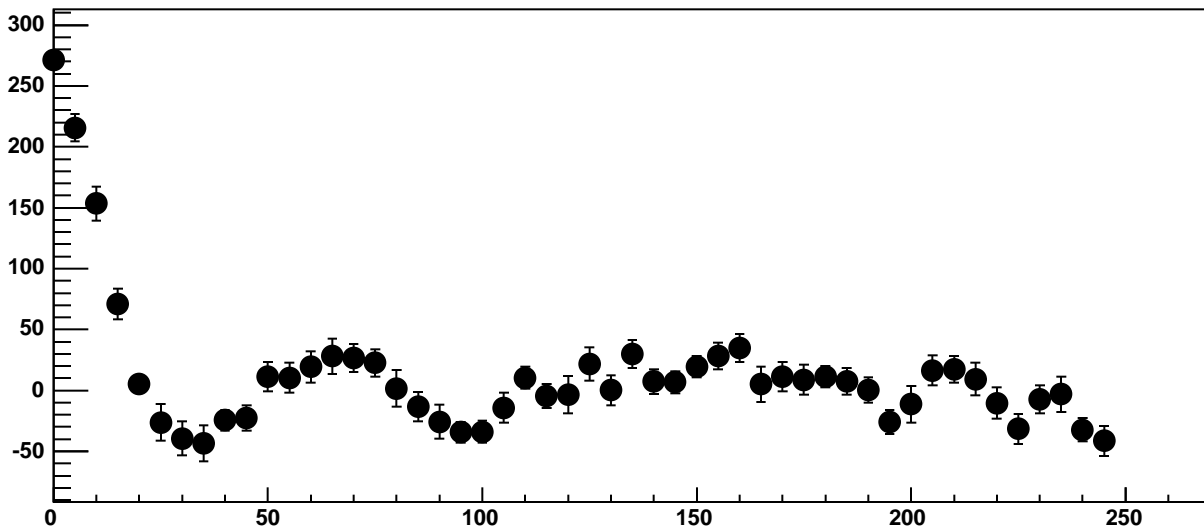


$\chi^2 / \text{ndf}$	186.4 / 41
p0	$-790.7 \pm 3.619$
p1	$92.9 \pm 0.7345$
p2	$-2.472\text{e}+08 \pm 4.59\text{e}+06$
p3	$2.446\text{e}+07 \pm 3.234\text{e}+05$
p4	$9.63 \pm 0.129$

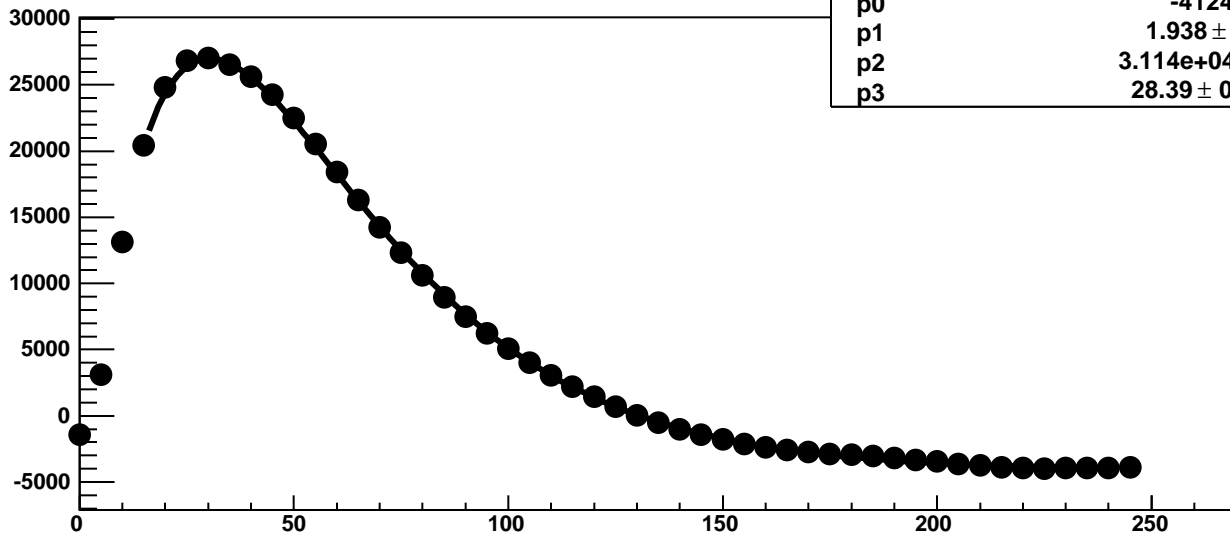
Chip 7, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



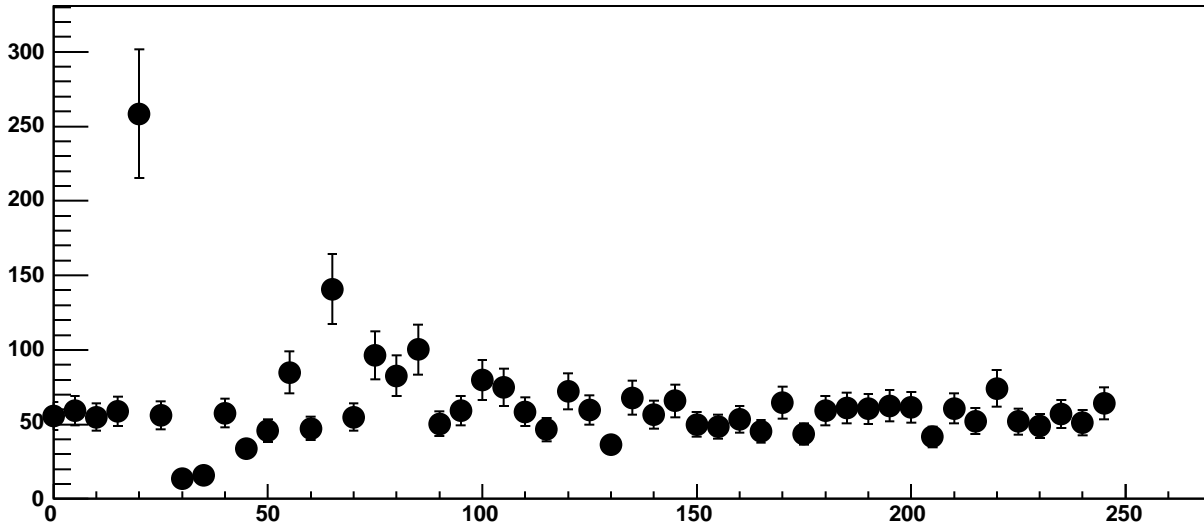
Chip 7, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



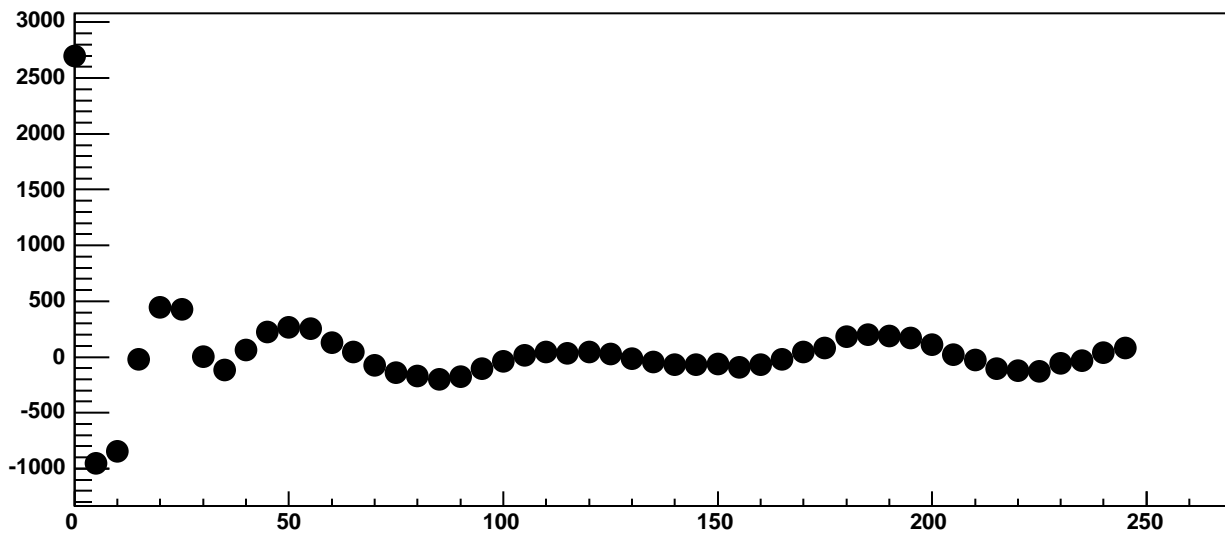
Chip 7, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold



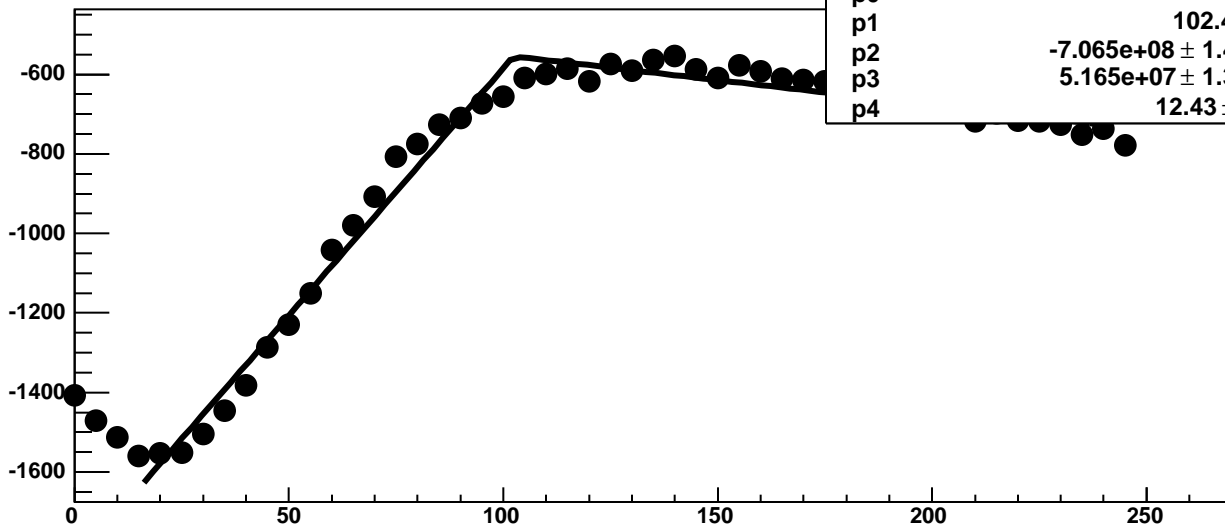
Chip 7, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold

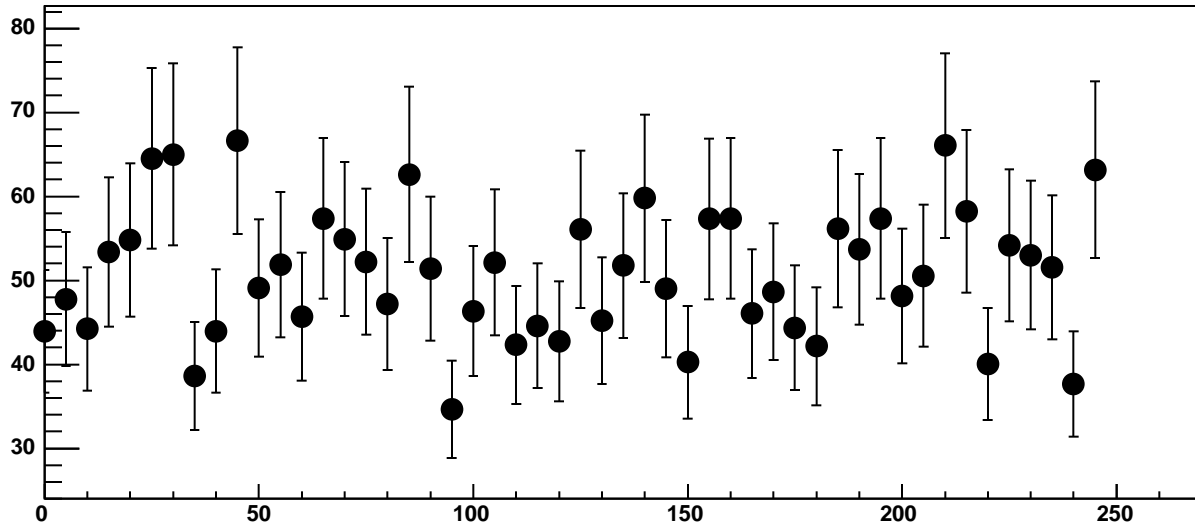


Chip 7, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

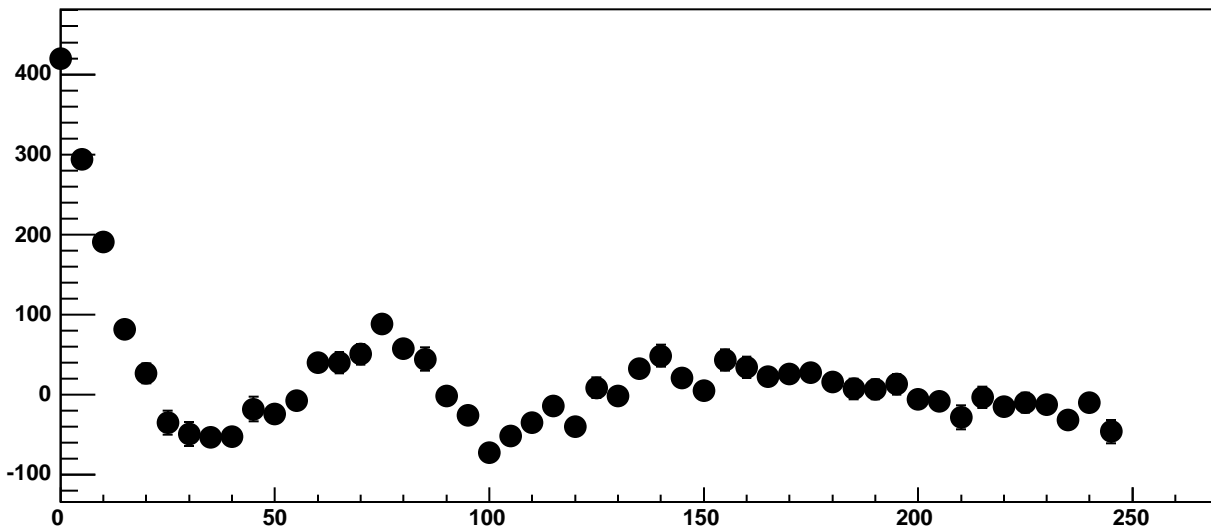


$\chi^2 / \text{ndf}$	452.8 / 41
p0	$-554.7 \pm 3.851$
p1	$102.4 \pm 0.411$
p2	$-7.065\text{e}+08 \pm 1.419\text{e}+07$
p3	$5.165\text{e}+07 \pm 1.372\text{e}+06$
p4	$12.43 \pm 0.1023$

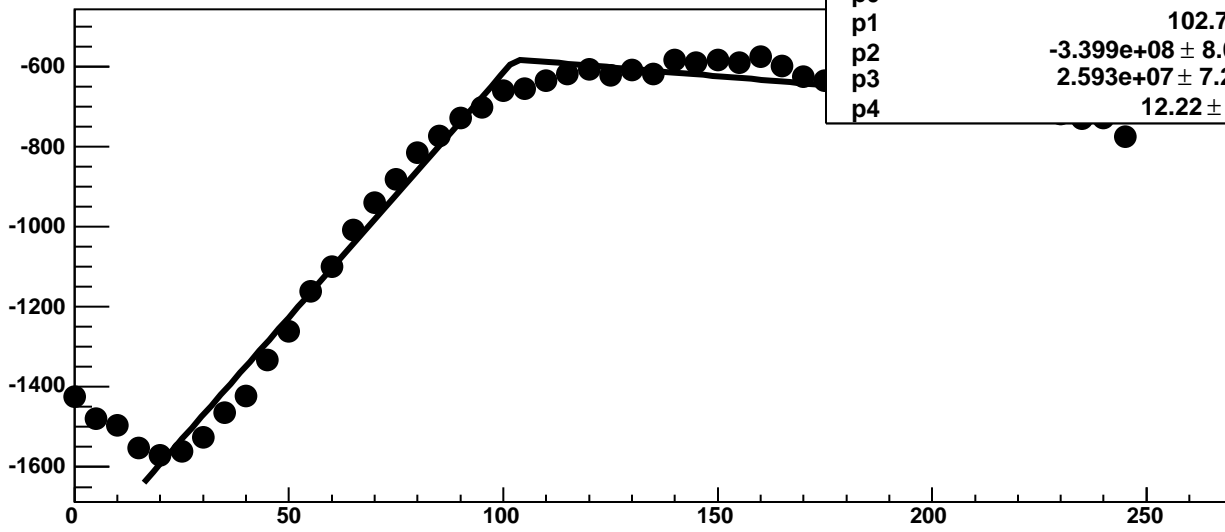
Chip 7, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

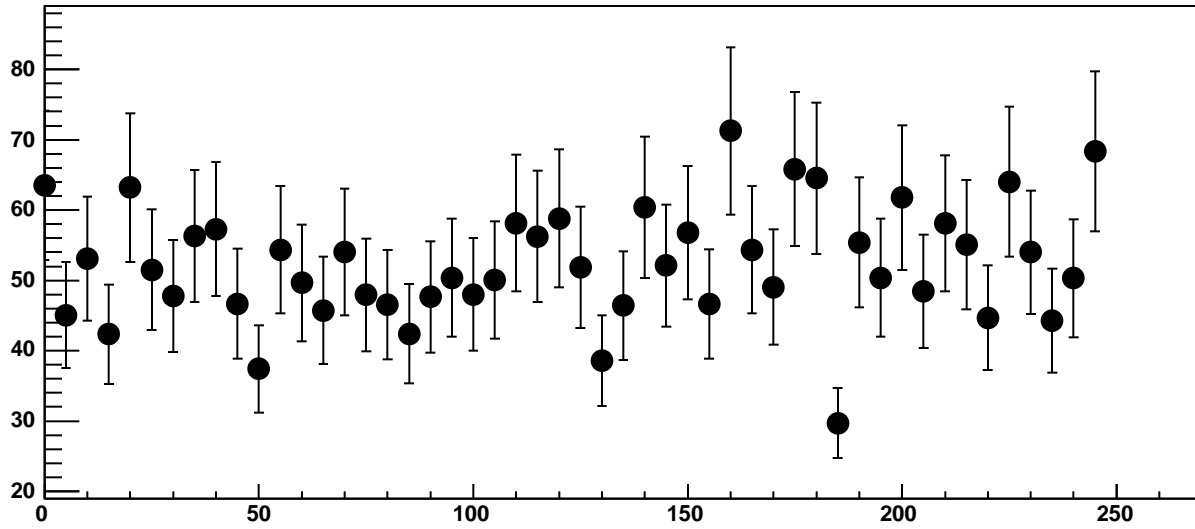


Chip 7, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

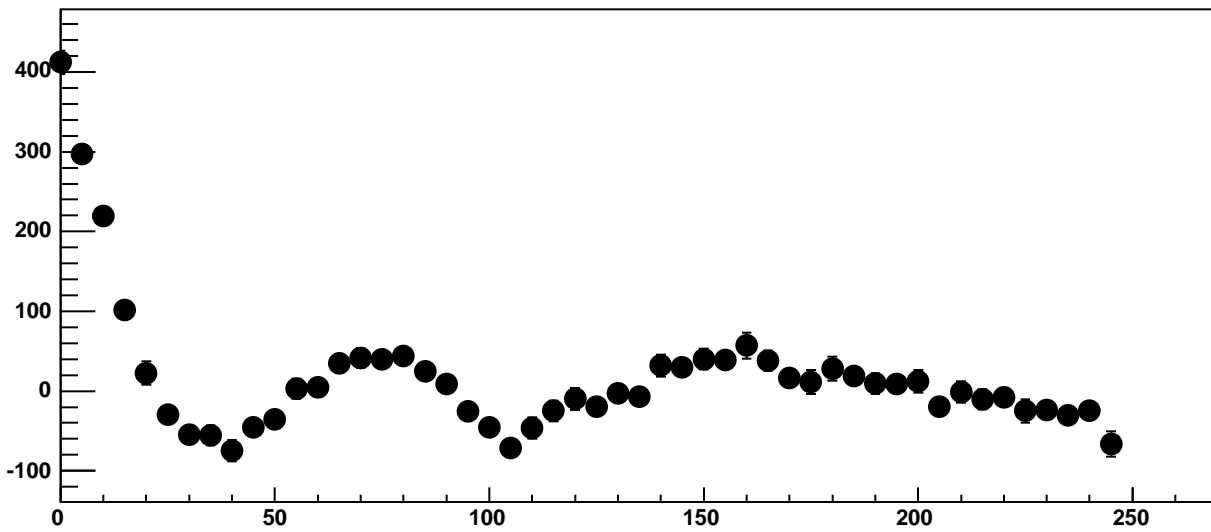


$\chi^2 / \text{ndf}$	464 / 41
p0	$-581.9 \pm 4.13$
p1	$102.7 \pm 0.466$
p2	$-3.399\text{e}+08 \pm 8.015\text{e}+06$
p3	$2.593\text{e}+07 \pm 7.249\text{e}+05$
p4	$12.22 \pm 0.09479$

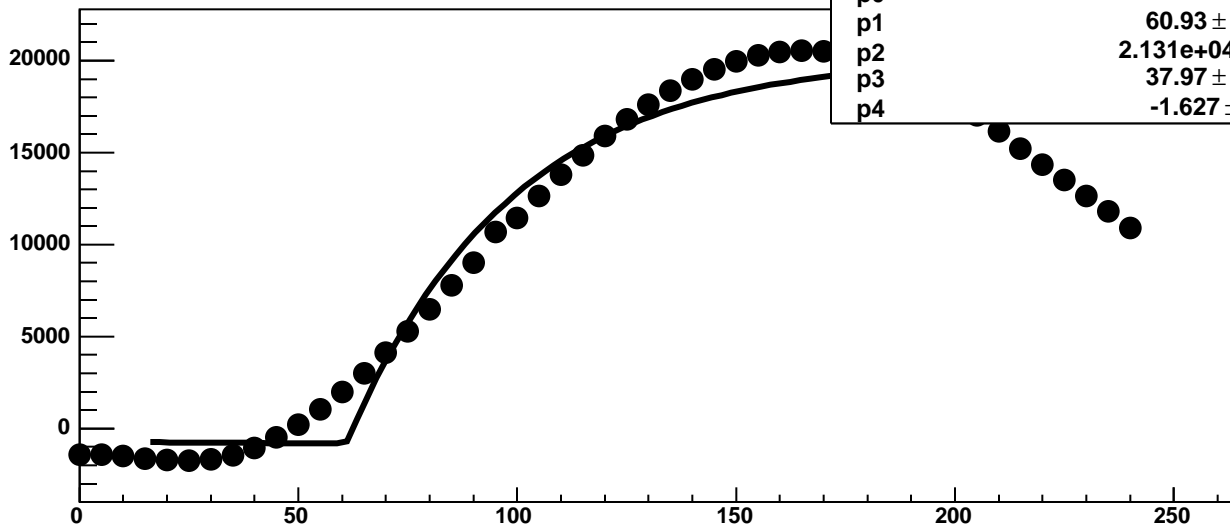
Chip 7, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

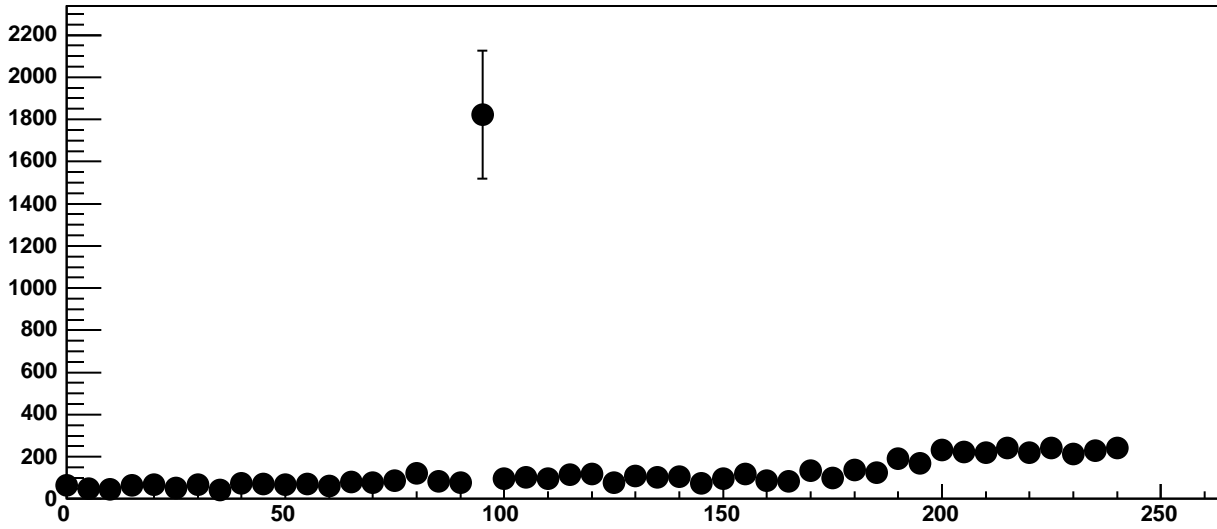


Chip 7, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold

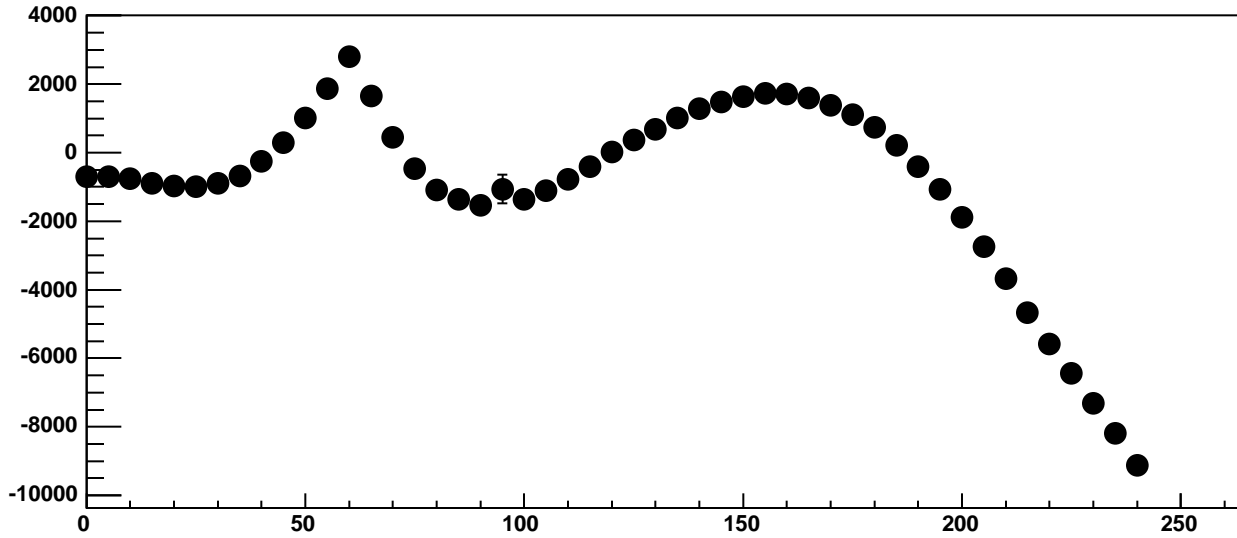


$\chi^2 / \text{ndf}$	2.694e+05 / 41
p0	-814.5 ± 7.137
p1	60.93 ± 0.03083
p2	2.131e+04 ± 38.61
p3	37.97 ± 0.08326
p4	-1.627 ± 0.2294

Chip 7, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold

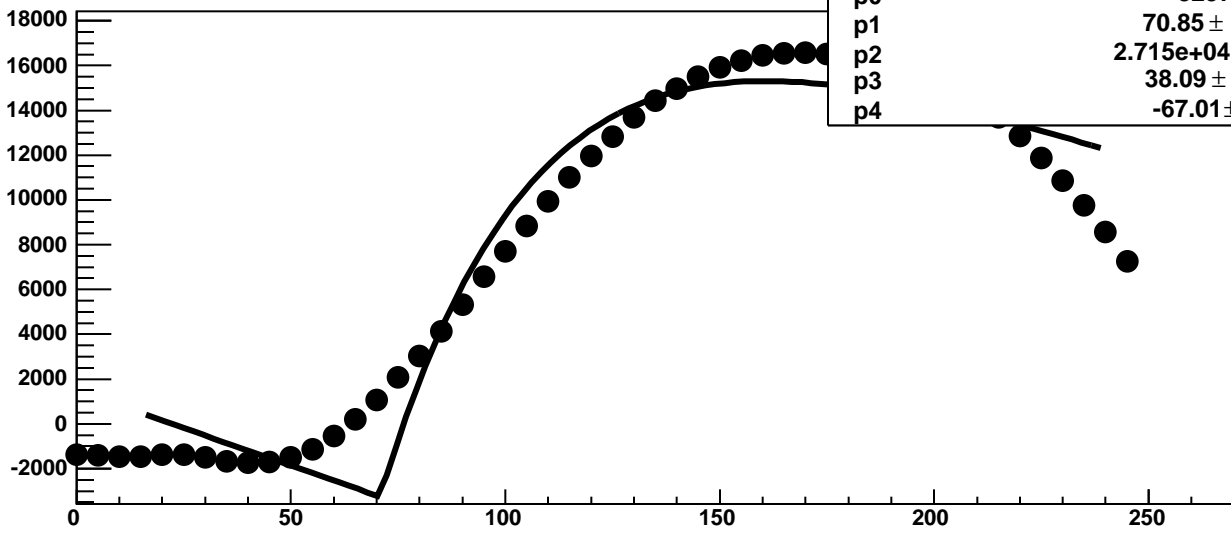


Chip 7, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold



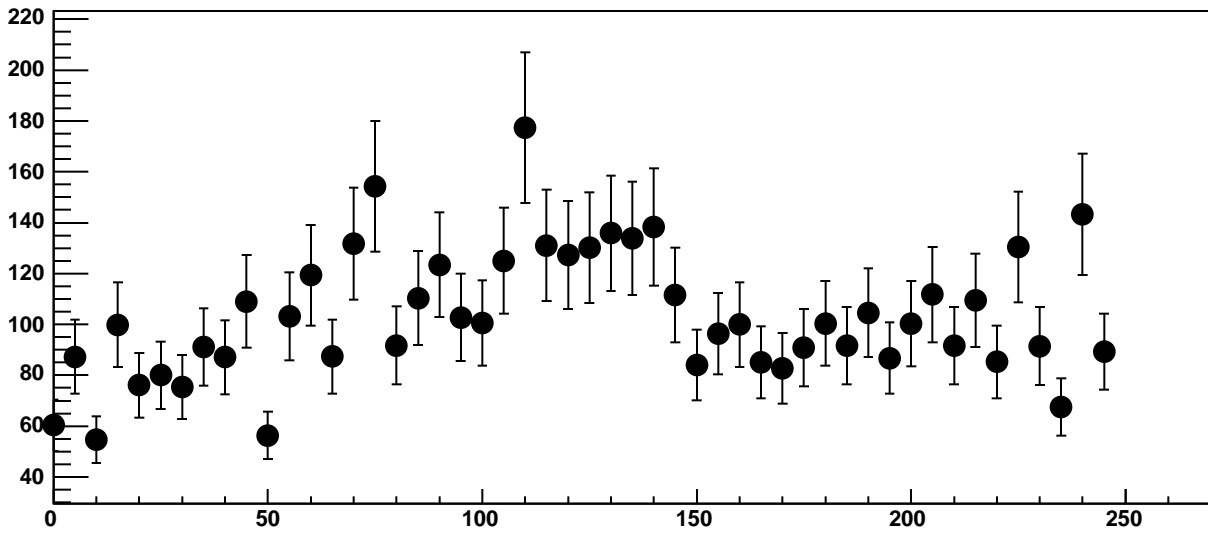


Chip 7, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

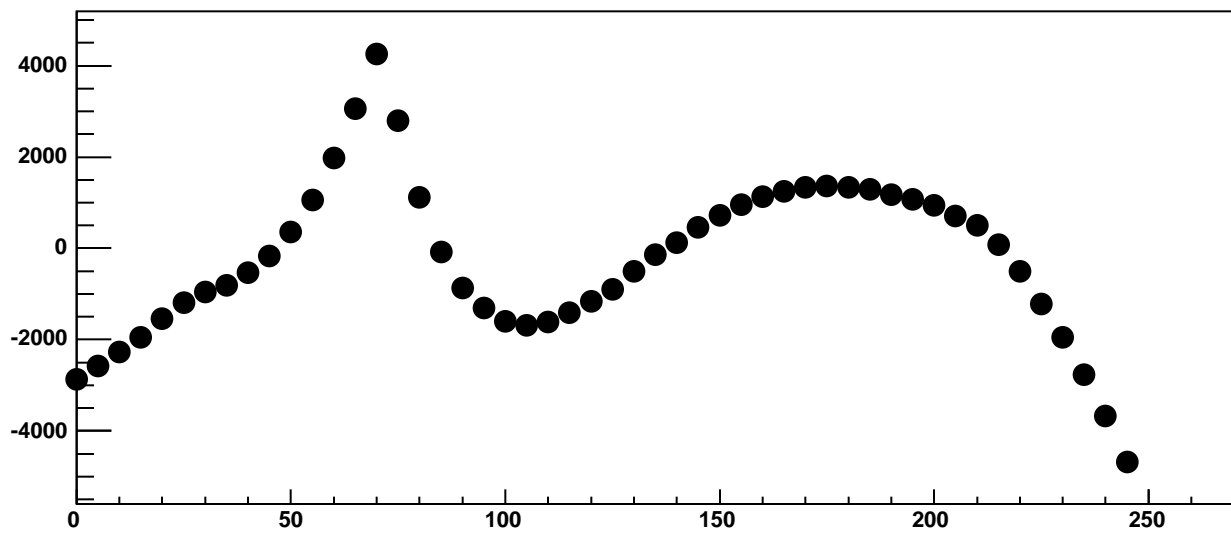


$\chi^2 / \text{ndf}$	1.94e+05 / 41
p0	-3257 ± 8.173
p1	70.85 ± 0.03402
p2	2.715e+04 ± 42.95
p3	38.09 ± 0.08071
p4	-67.01 ± 0.2252

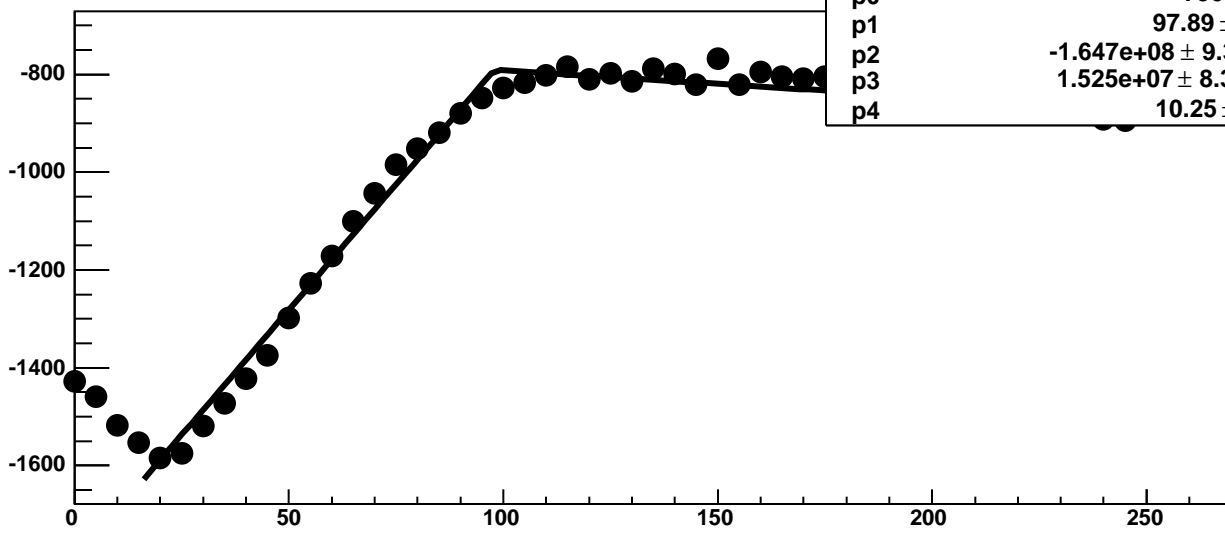
Chip 7, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

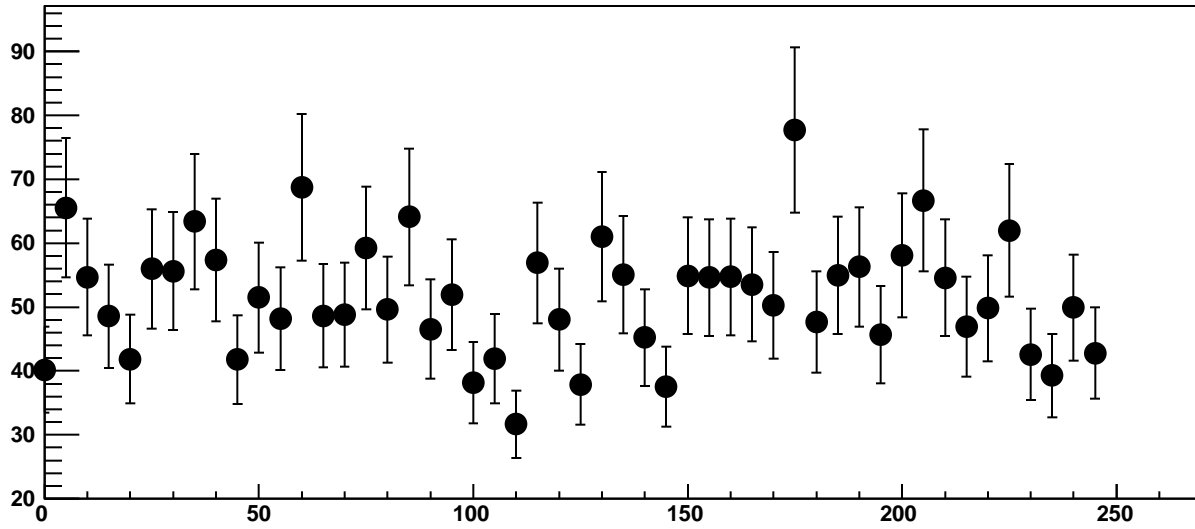


Chip 7, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

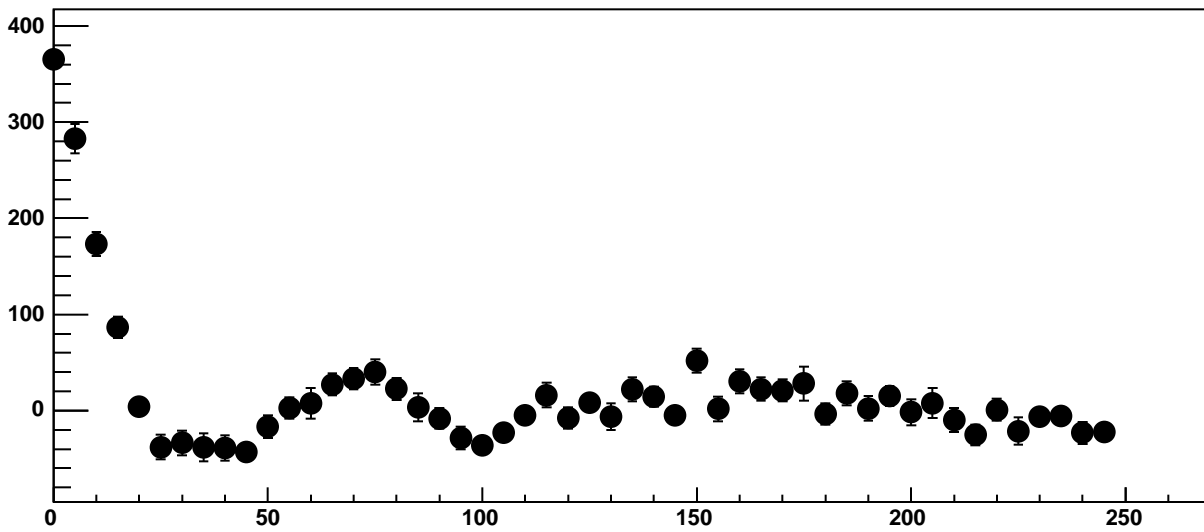


$\chi^2 / \text{ndf}$	230.2 / 41
p0	$-790.3 \pm 3.5$
p1	$97.89 \pm 0.6366$
p2	$-1.647\text{e}+08 \pm 9.313\text{e}+06$
p3	$1.525\text{e}+07 \pm 8.365\text{e}+05$
p4	$10.25 \pm 0.1154$

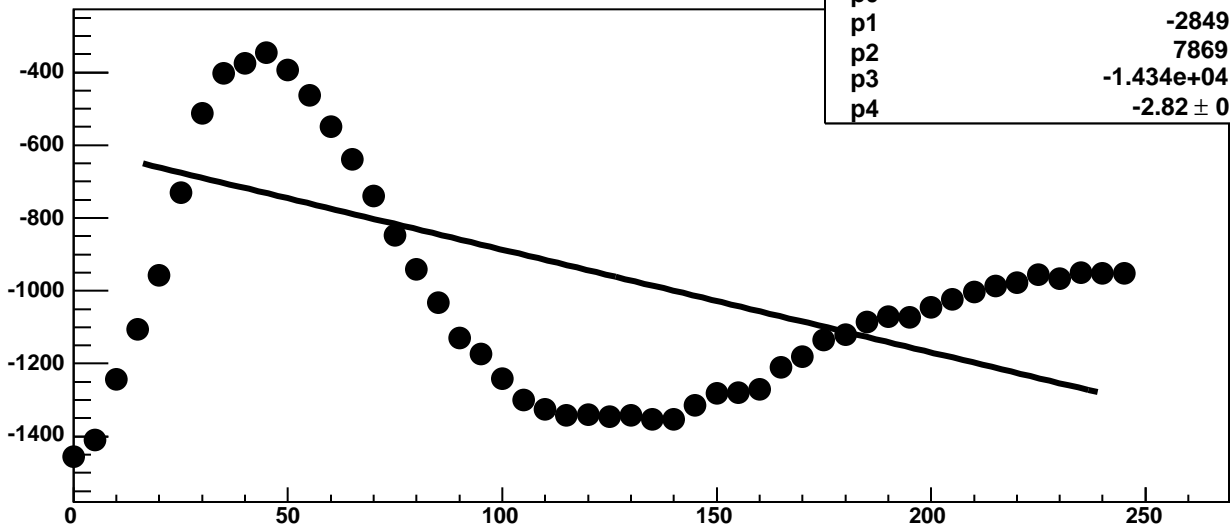
Chip 7, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

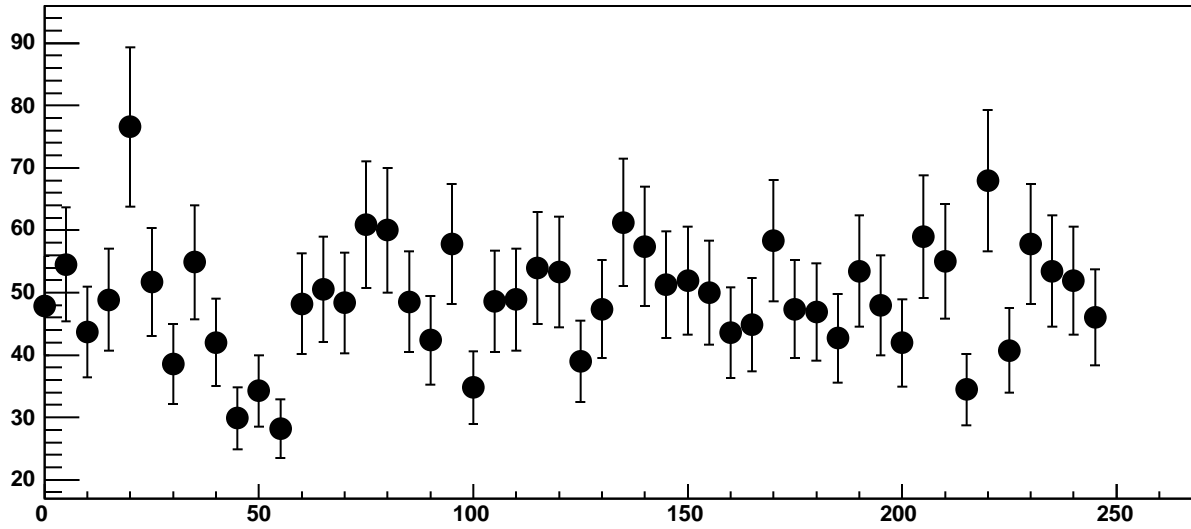


Chip 7, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold

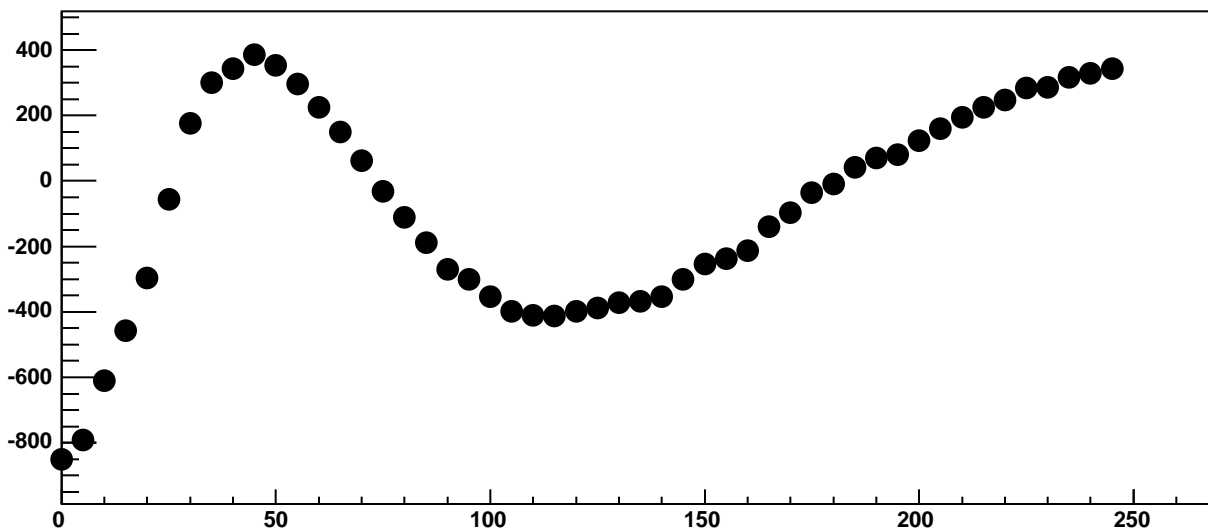


$\chi^2 / \text{ndf}$	3.17e+04 / 41
p0	-438.8 ± 7.976
p1	-2849 ± 2.346
p2	7869 ± 10.09
p3	-1.434e+04 ± 142.3
p4	-2.82 ± 0.002682

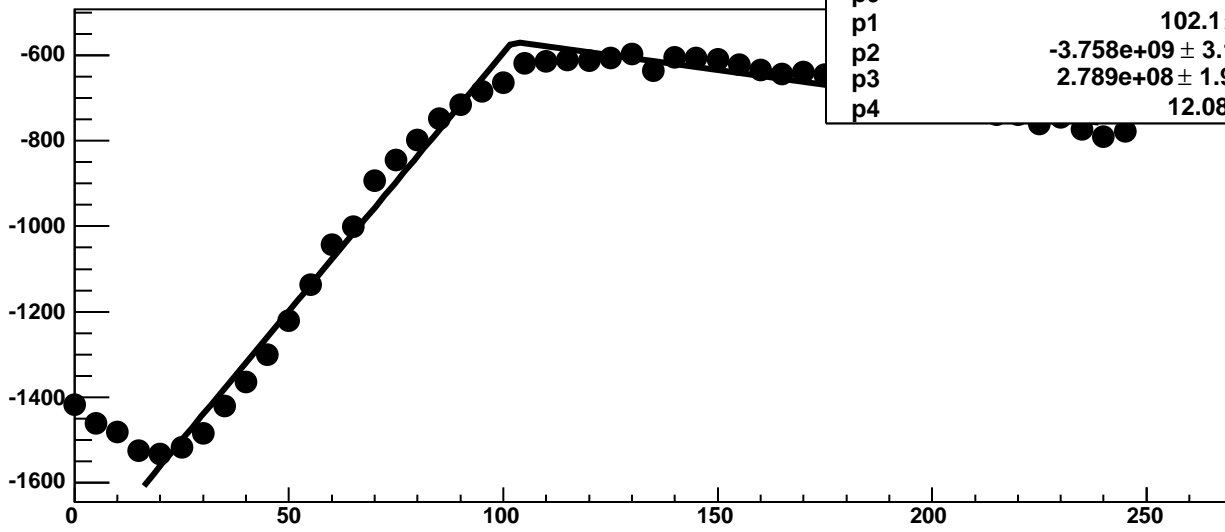
Chip 7, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

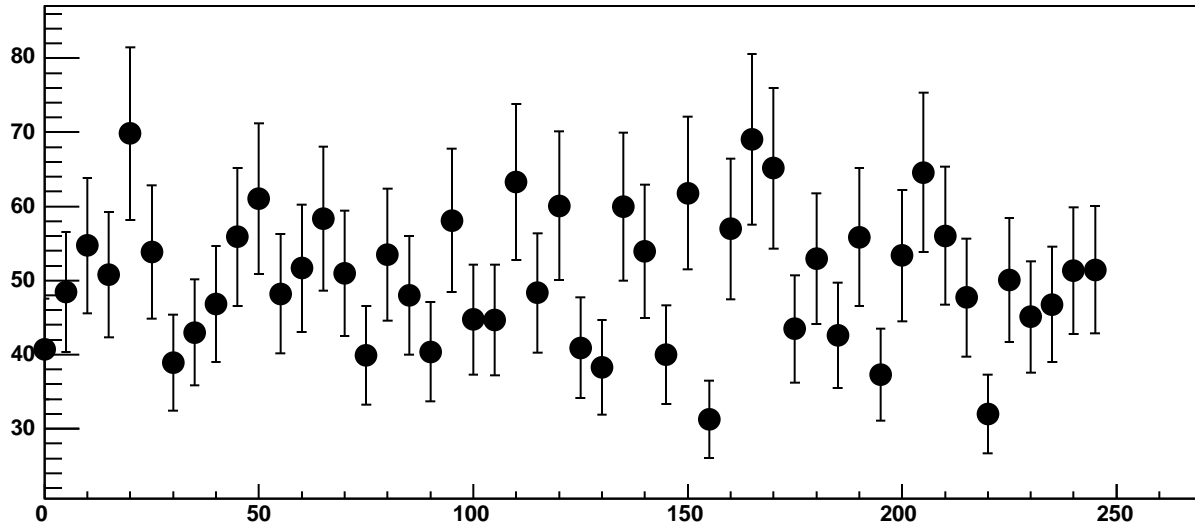


Chip 7, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

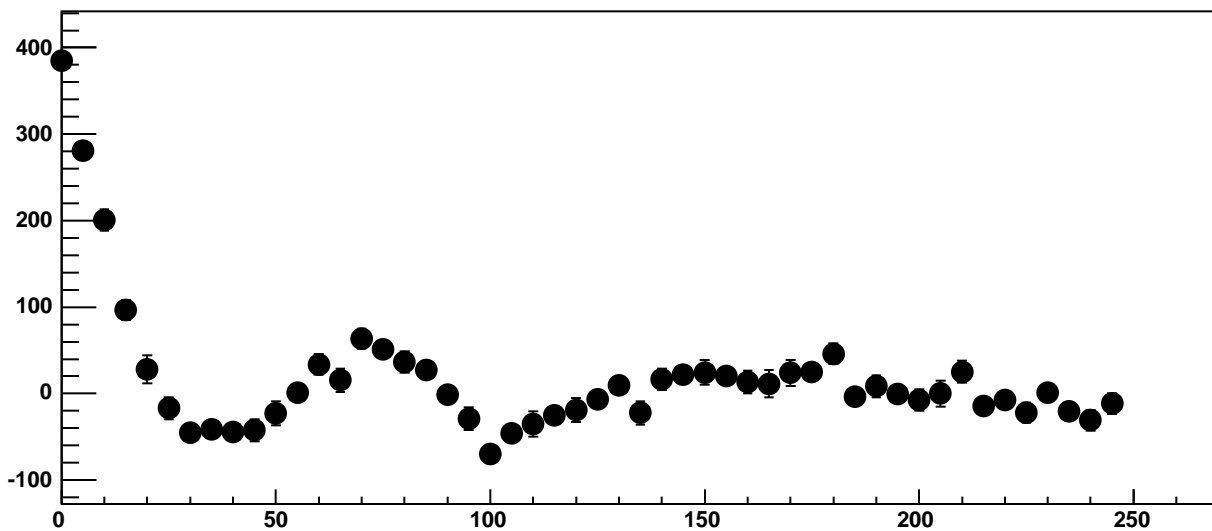


$\chi^2 / \text{ndf}$	387.6 / 41
p0	$-568.3 \pm 3.781$
p1	$102.1 \pm 0.4921$
p2	$-3.758e+09 \pm 3.181e+07$
p3	$2.789e+08 \pm 1.997e+05$
p4	$12.08 \pm 0.102$

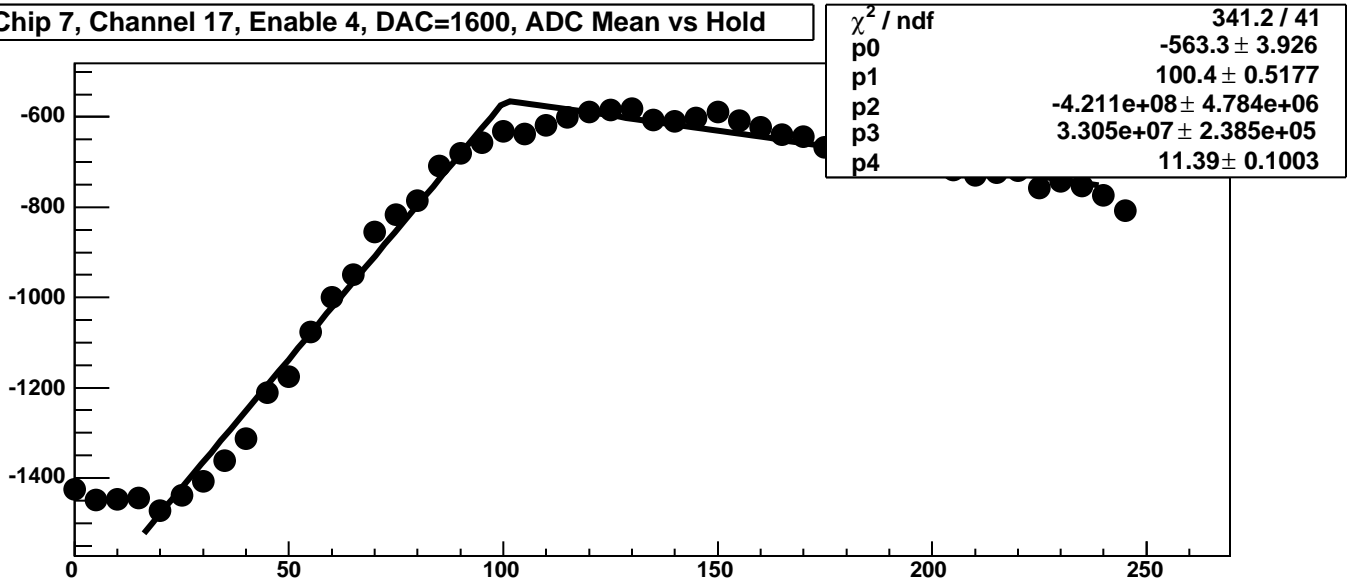
Chip 7, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



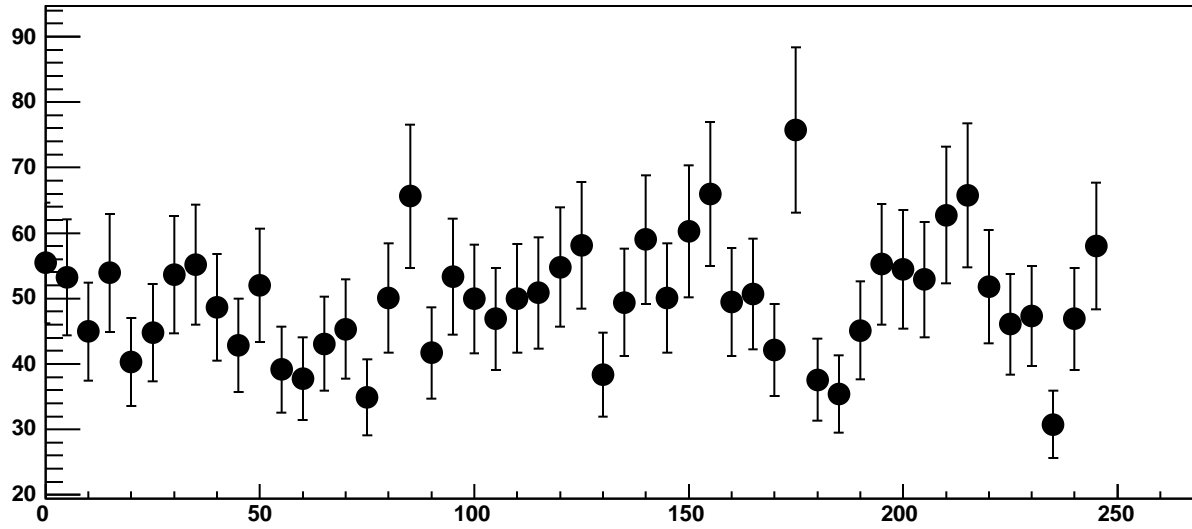
Chip 7, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



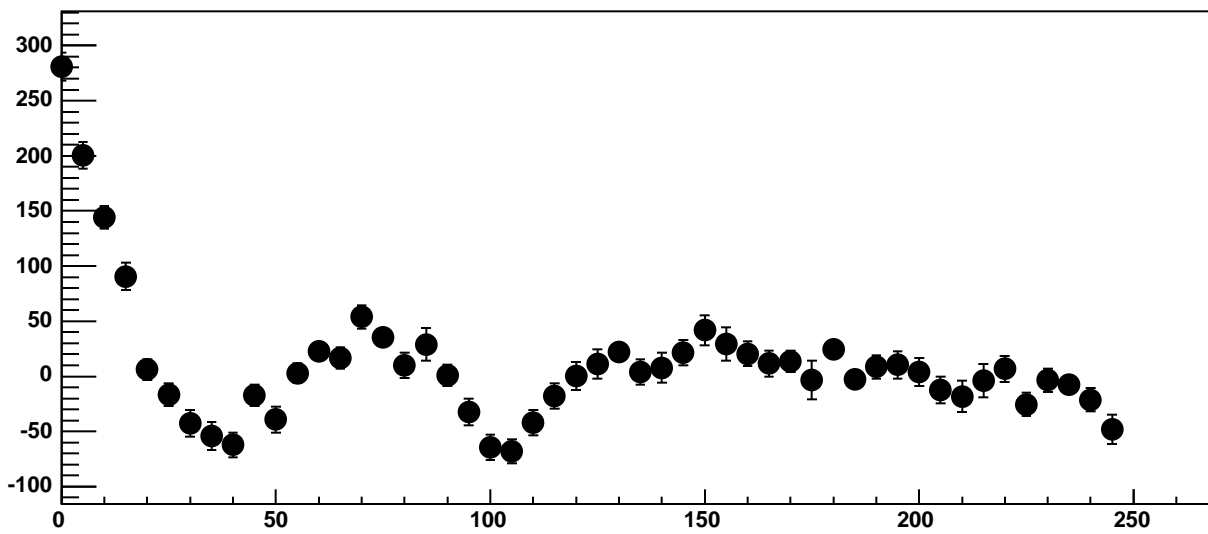
Chip 7, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold



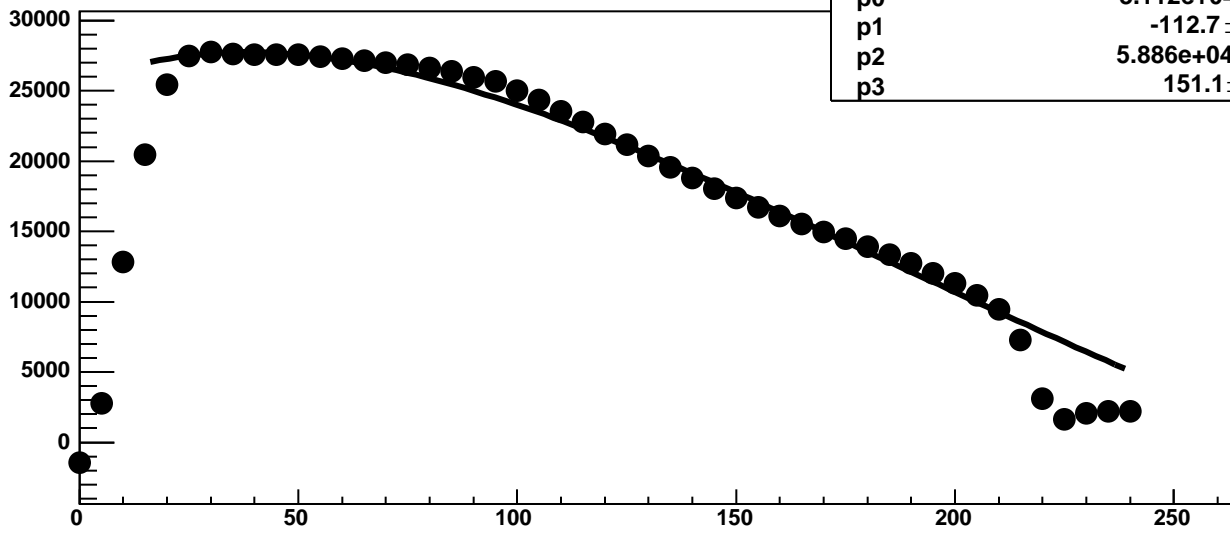
Chip 7, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 7, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

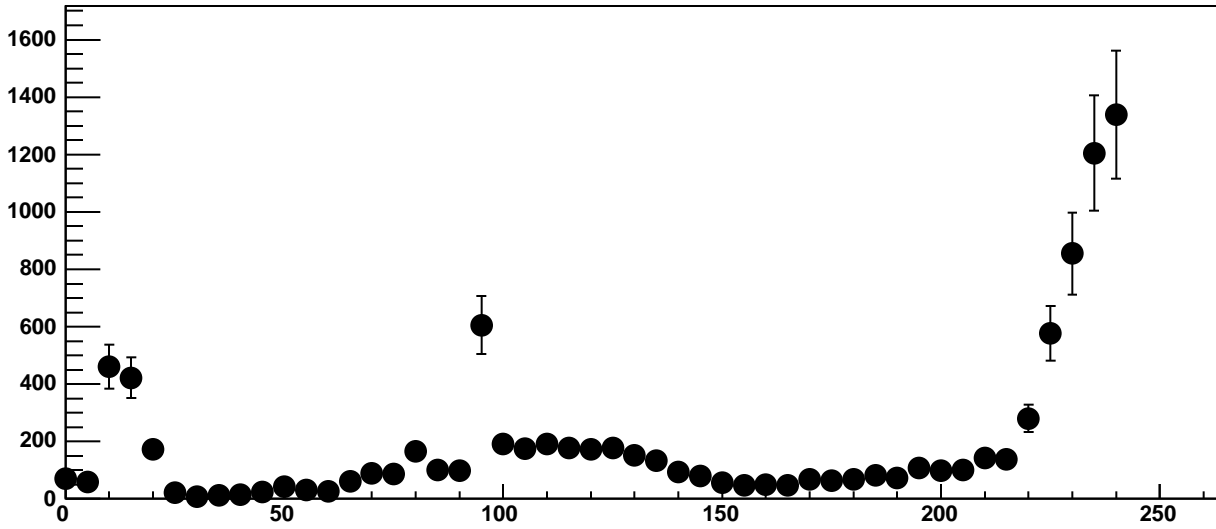


Chip 7, Channel 17, Enable 5!, DAC=1600, ADC Mean vs Hold

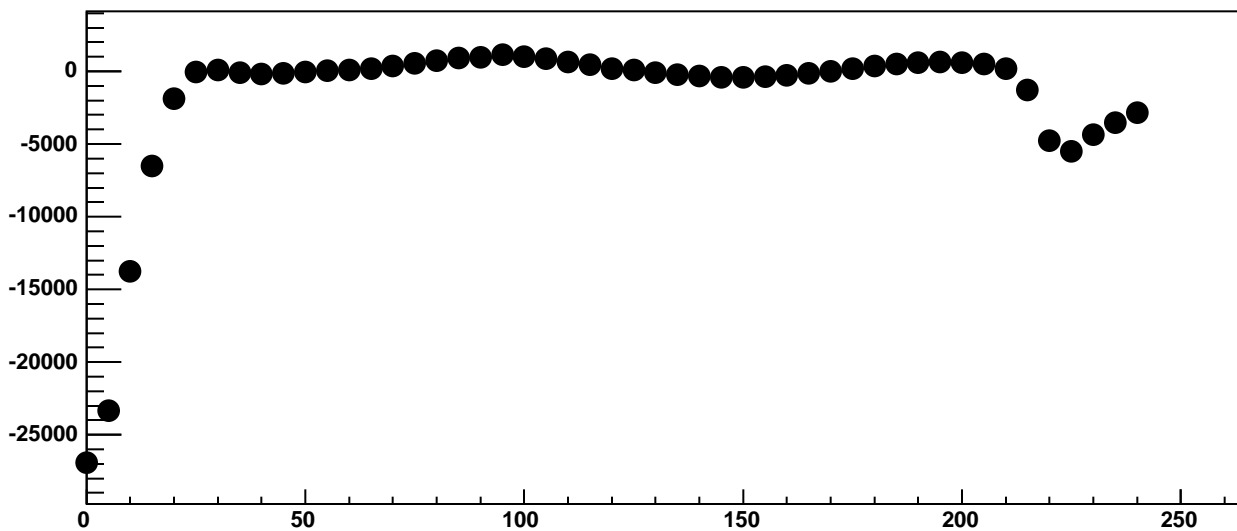


$\chi^2 / \text{ndf}$	3.667e+04 / 42
p0	-3.112e+04 ± 344.4
p1	-112.7 ± 0.6774
p2	5.886e+04 ± 343.9
p3	151.1 ± 0.6462

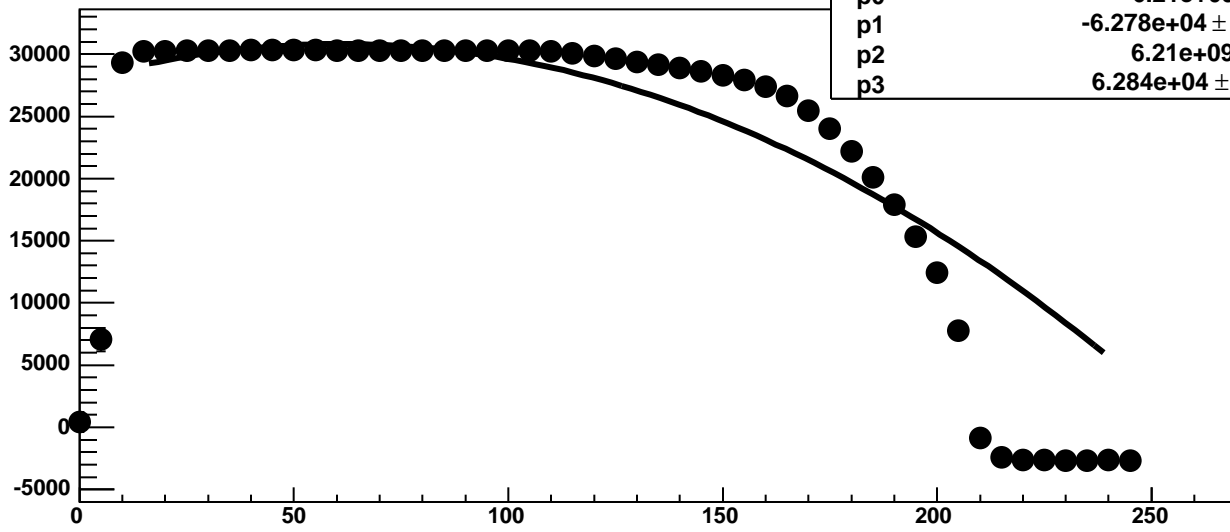
Chip 7, Channel 17, Enable 5!, DAC=1600, ADC Noise vs Hold



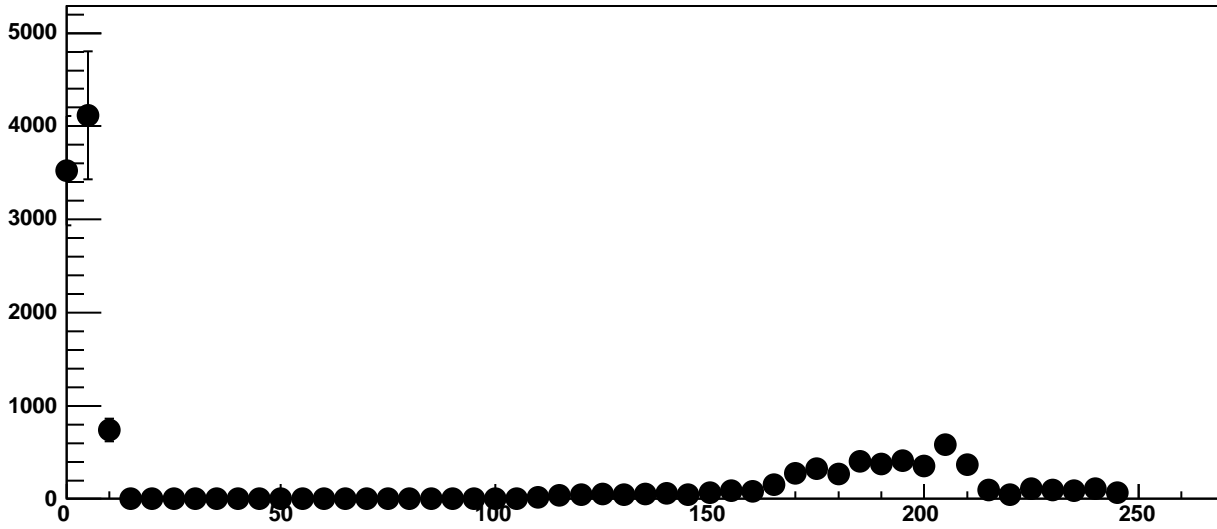
Chip 7, Channel 17, Enable 5!, DAC=1600, ADC Residuals vs Hold



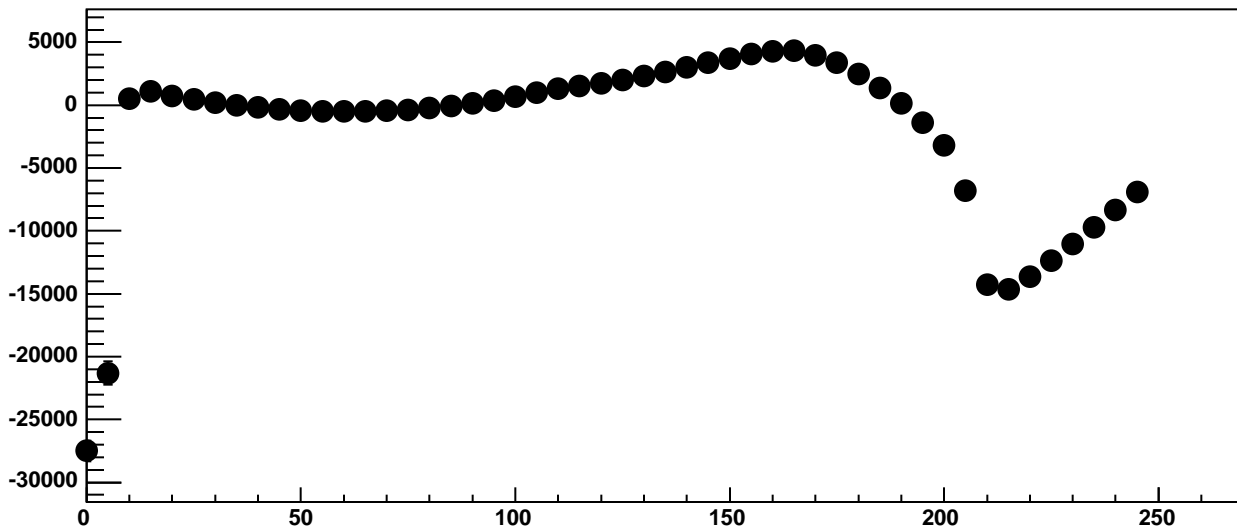
Chip 8, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold



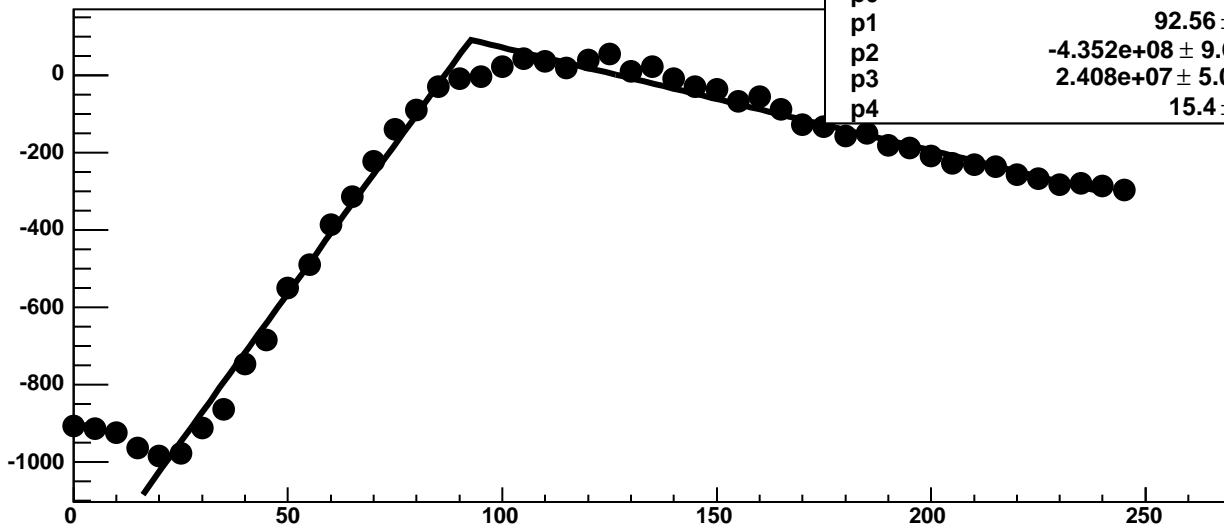
Chip 8, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold

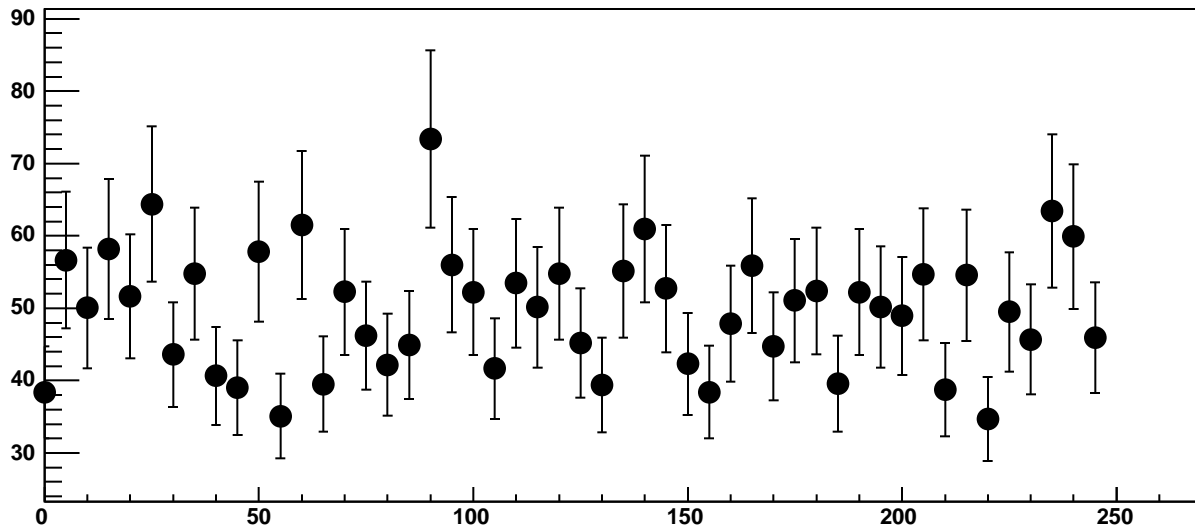


Chip 8, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

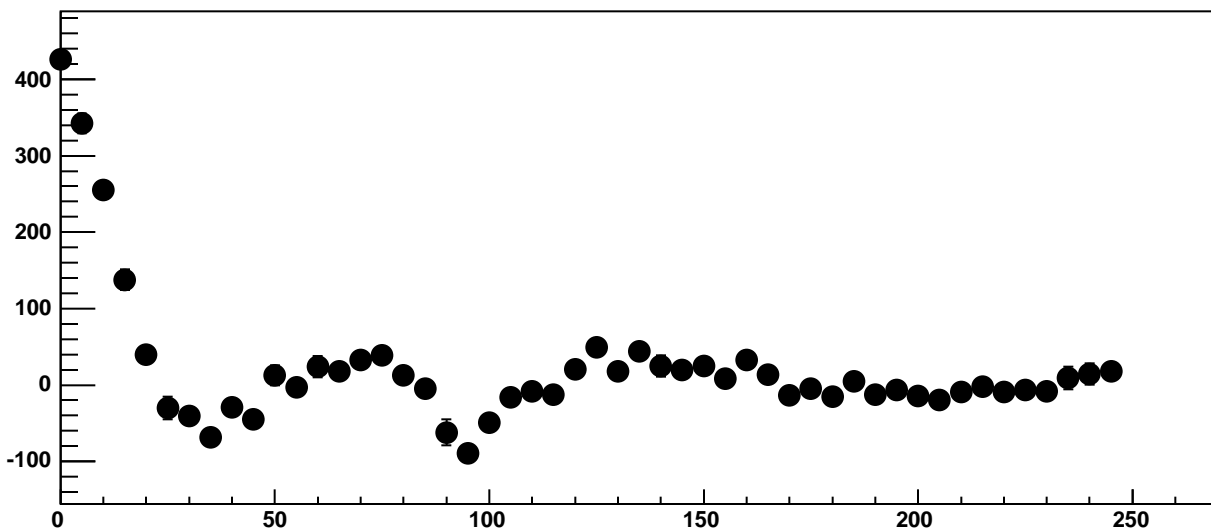


$\chi^2 / \text{ndf}$	396.1 / 41
p0	$91.65 \pm 3.618$
p1	$92.56 \pm 0.3908$
p2	$-4.352e+08 \pm 9.625e+06$
p3	$2.408e+07 \pm 5.071e+05$
p4	$15.4 \pm 0.1288$

Chip 8, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

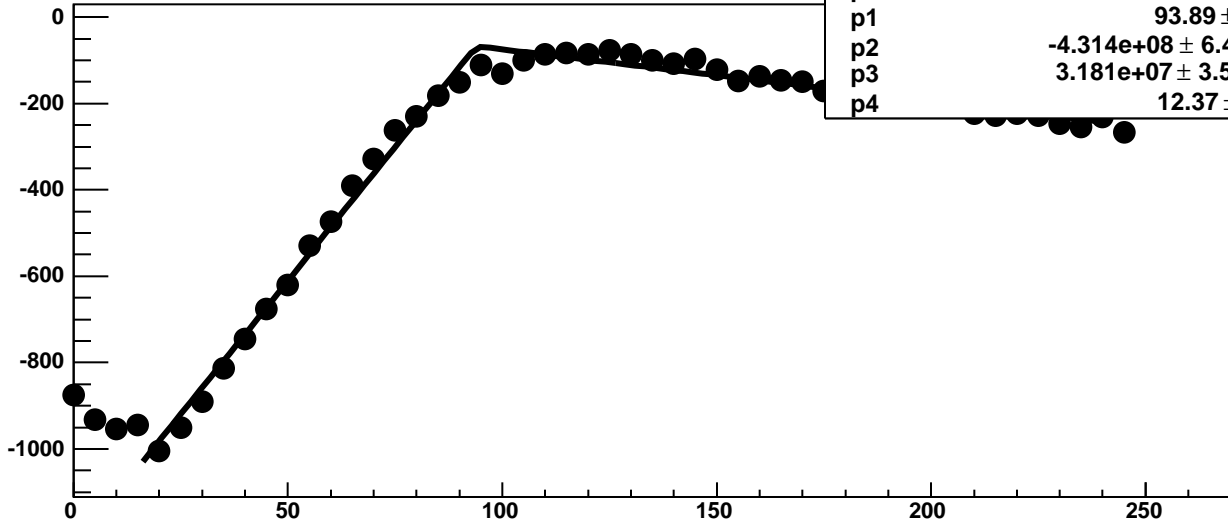


Chip 8, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



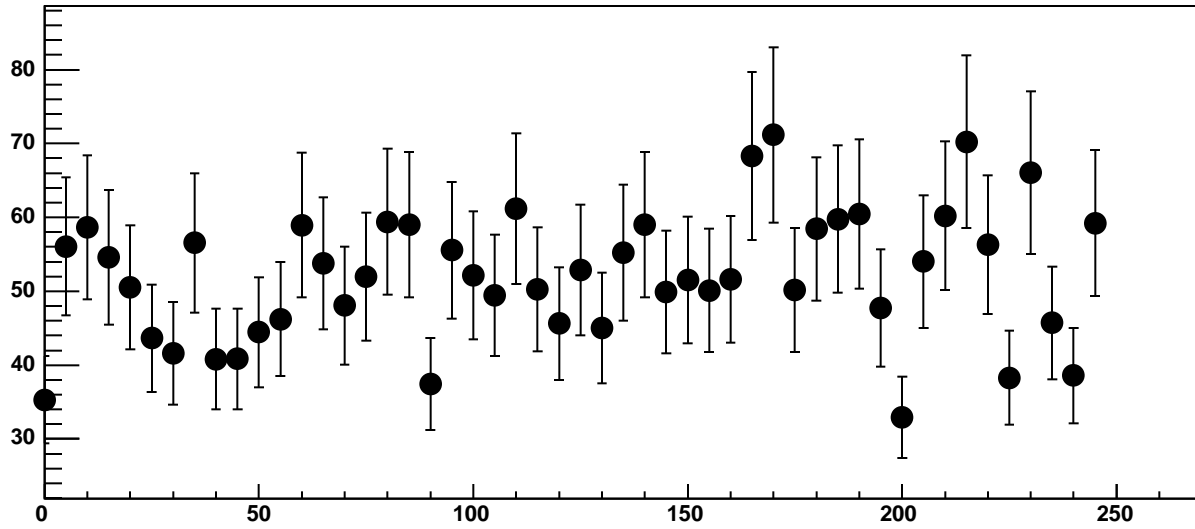


Chip 8, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

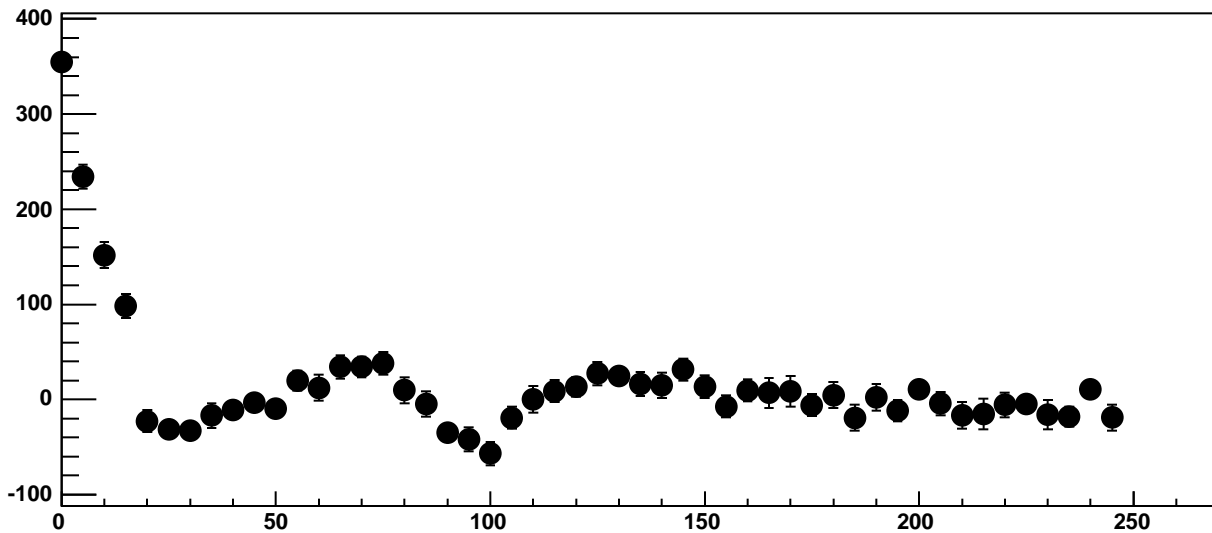


$\chi^2 / \text{ndf}$	216.8 / 41
p0	$-67.47 \pm 3.91$
p1	$93.89 \pm 0.5238$
p2	$-4.314\text{e}+08 \pm 6.434\text{e}+06$
p3	$3.181\text{e}+07 \pm 3.592\text{e}+05$
p4	$12.37 \pm 0.1191$

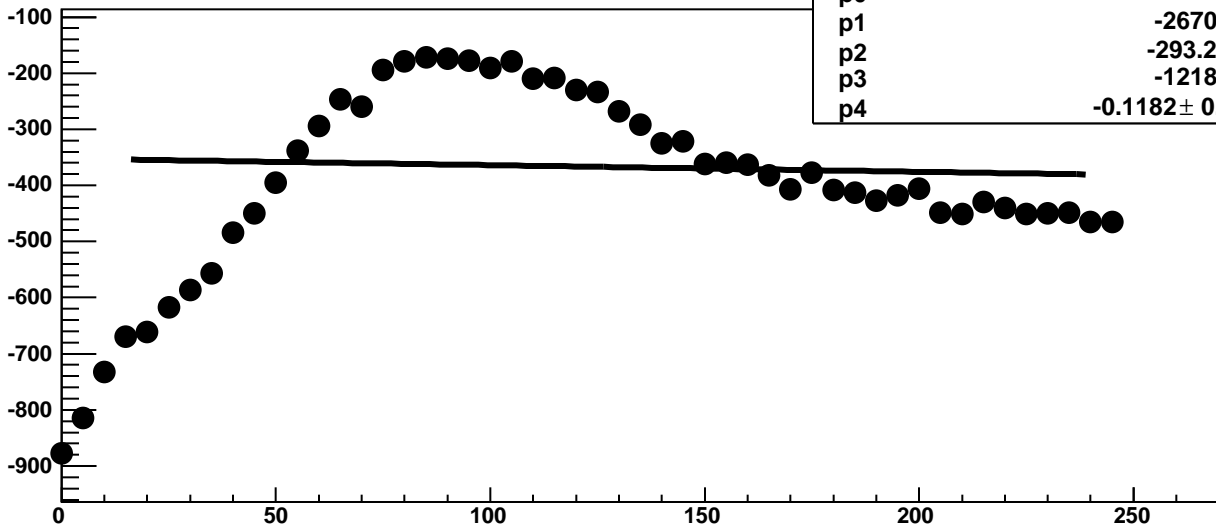
Chip 8, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



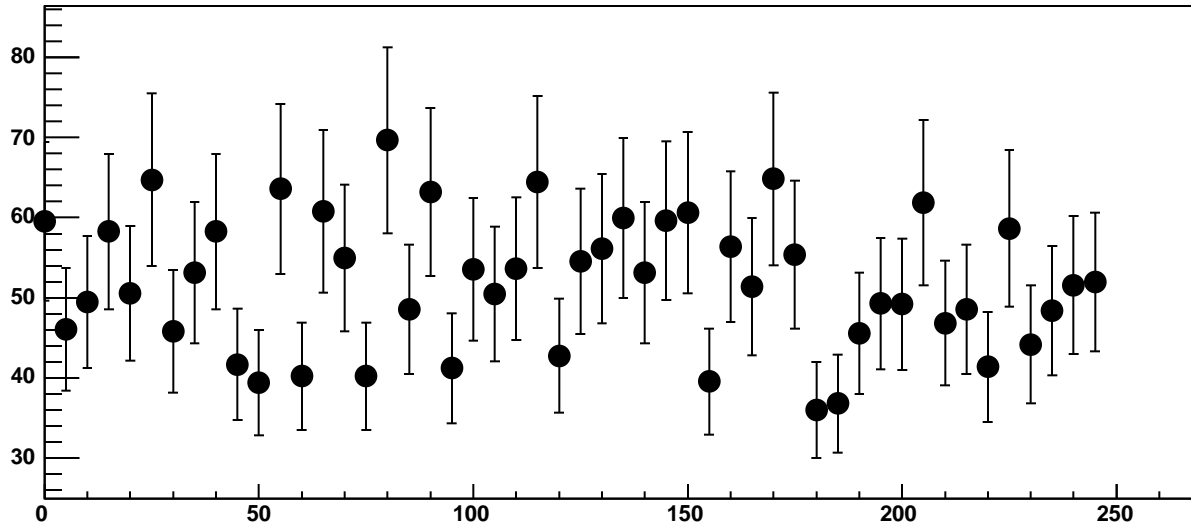
Chip 8, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



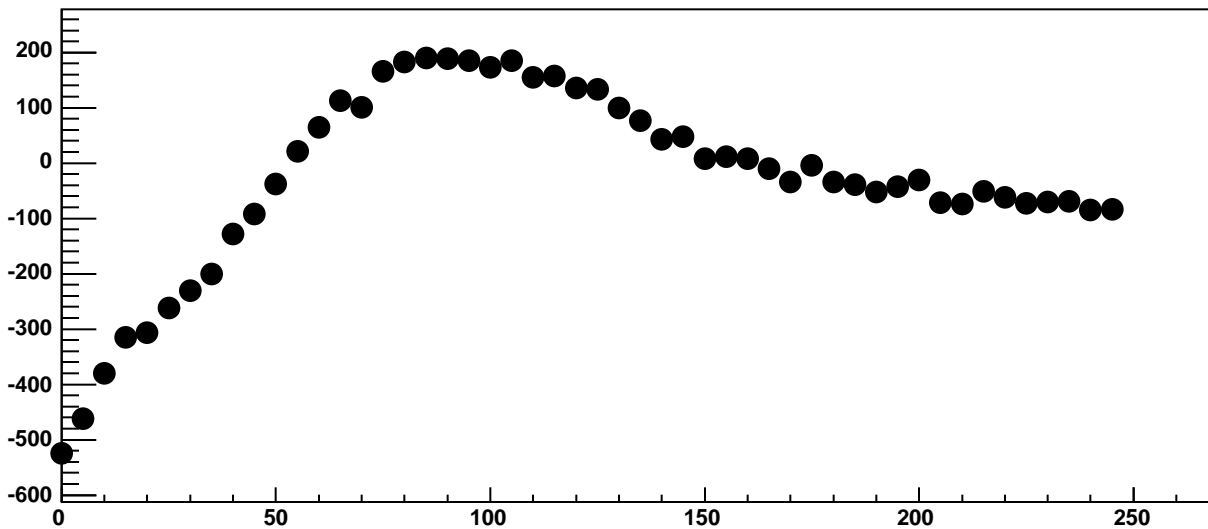
Chip 8, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold



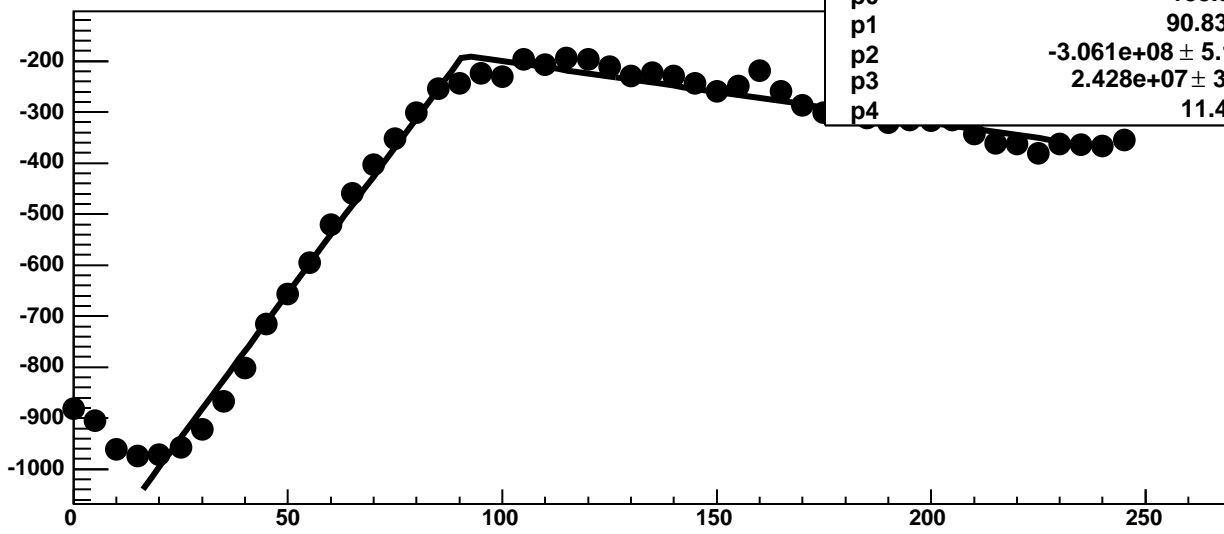
Chip 8, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold

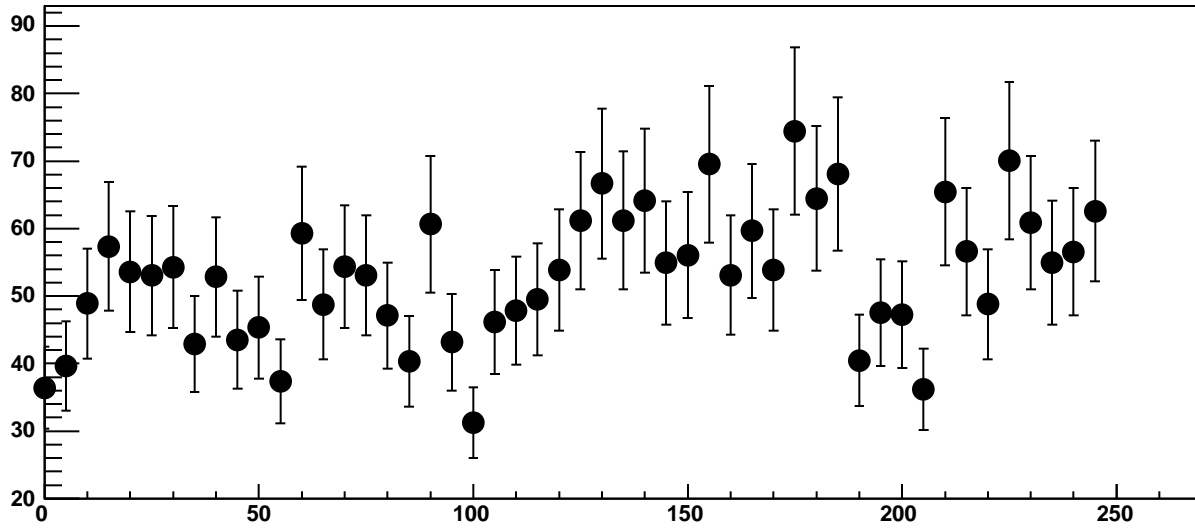


Chip 8, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

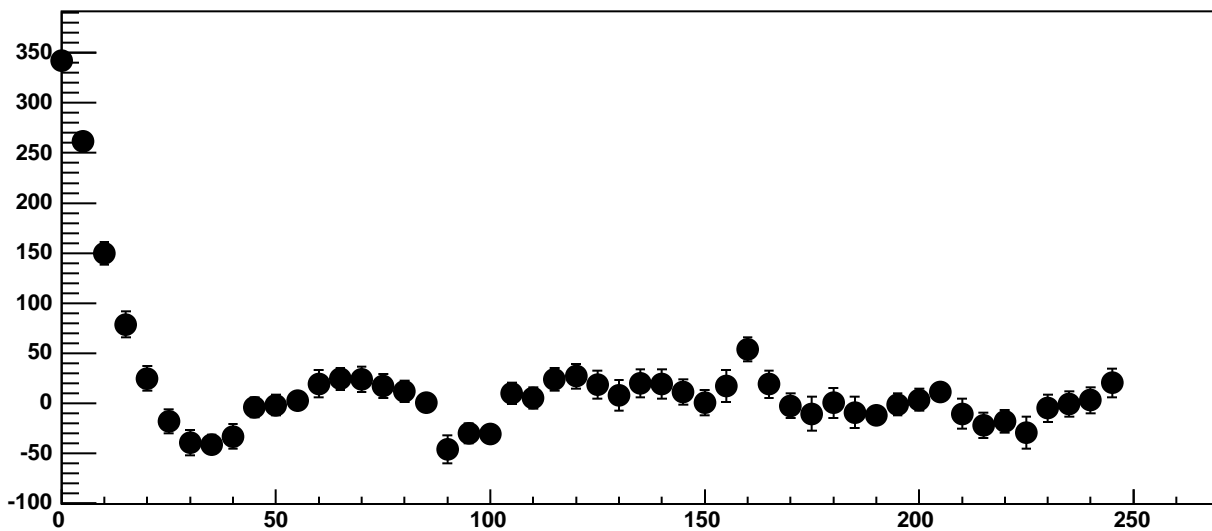


$\chi^2 / \text{ndf}$	183 / 41
p0	$-188.8 \pm 3.701$
p1	$90.83 \pm 0.543$
p2	$-3.061\text{e}+08 \pm 5.126\text{e}+06$
p3	$2.428\text{e}+07 \pm 3.43\text{e}+05$
p4	$11.4 \pm 0.128$

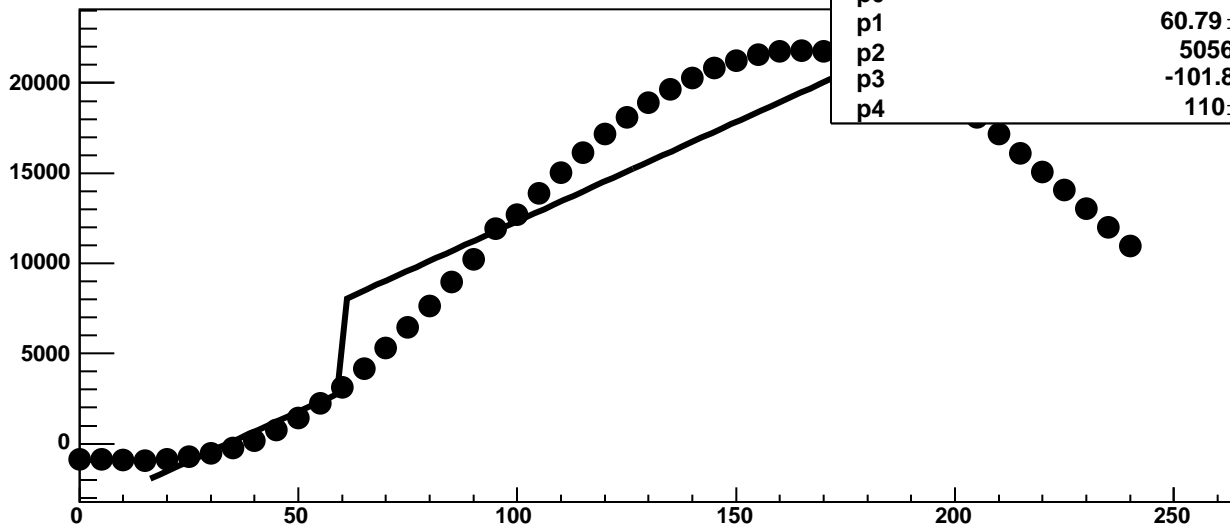
Chip 8, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

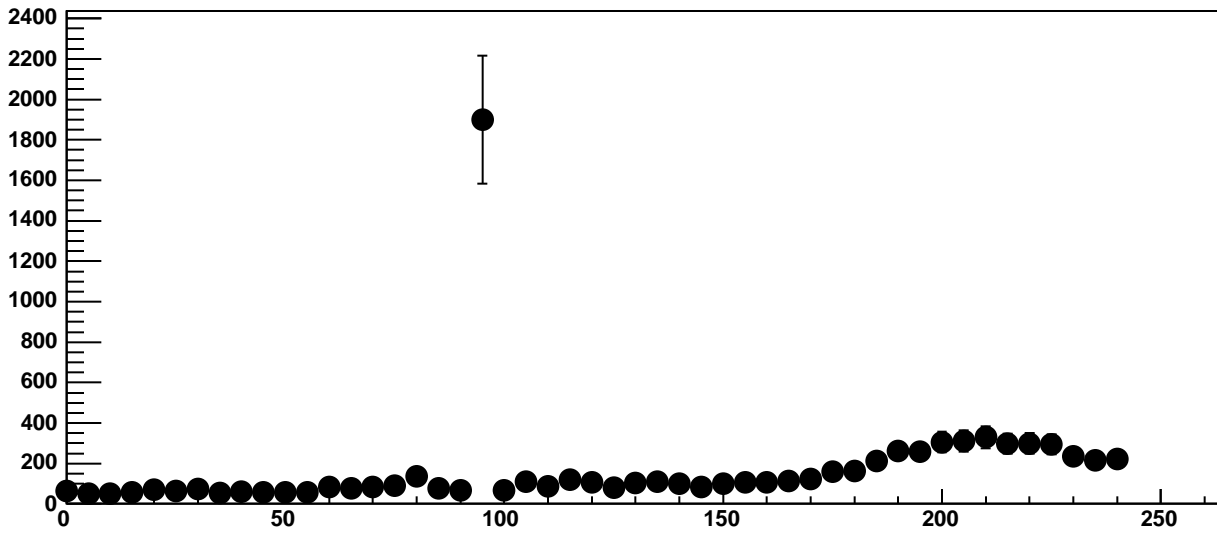


Chip 8, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

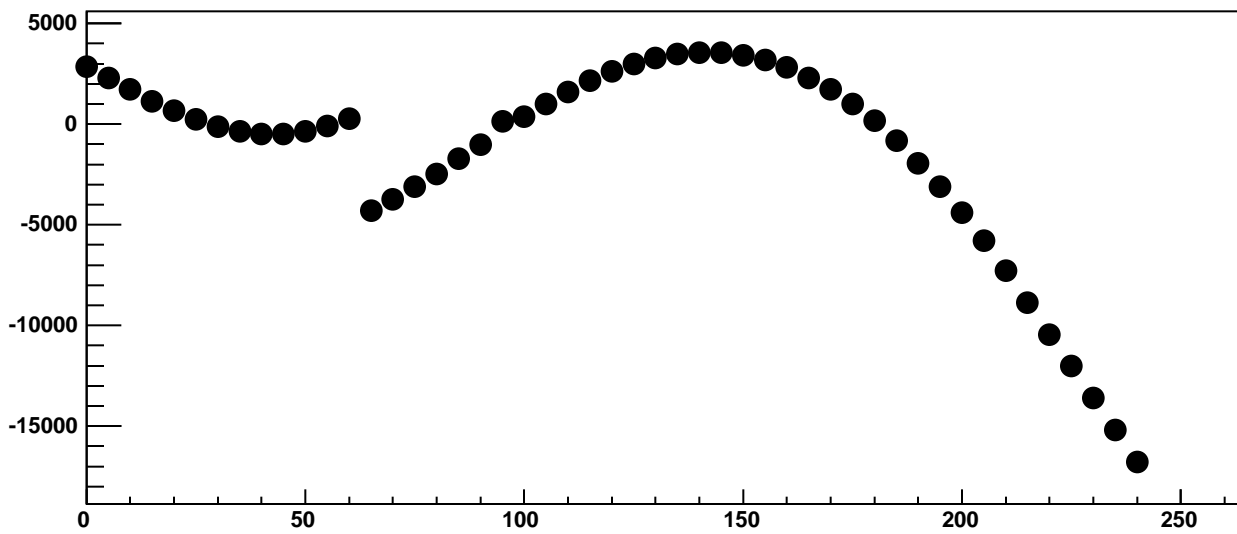


$\chi^2 / \text{ndf}$	7.273e+05 / 41
p0	2964 ± 13.82
p1	60.79 ± 0.1567
p2	5056 ± 30.15
p3	-101.8 ± 9.463
p4	110 ± 0.4368

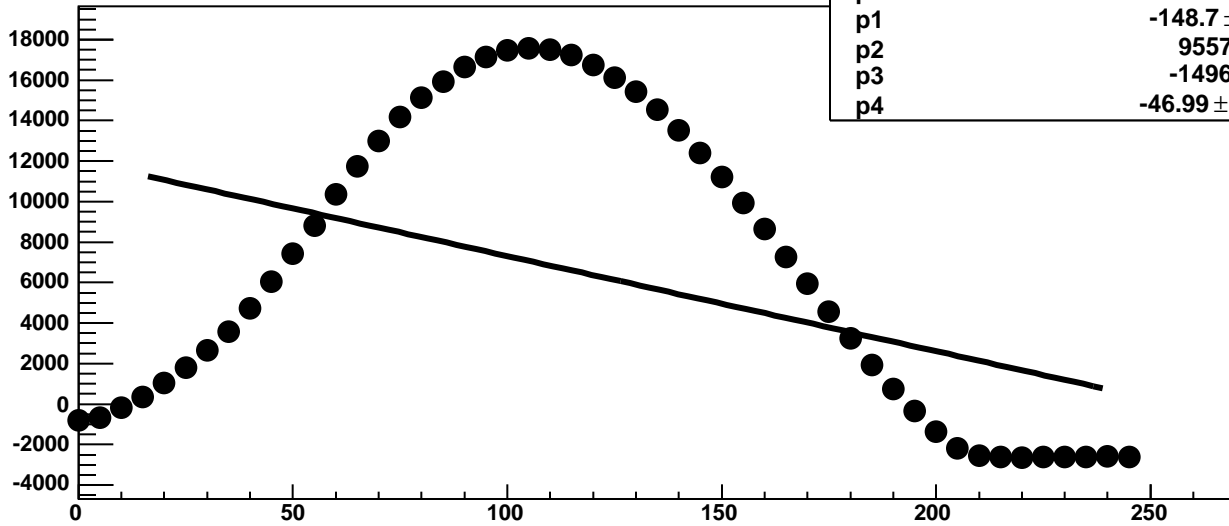
Chip 8, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

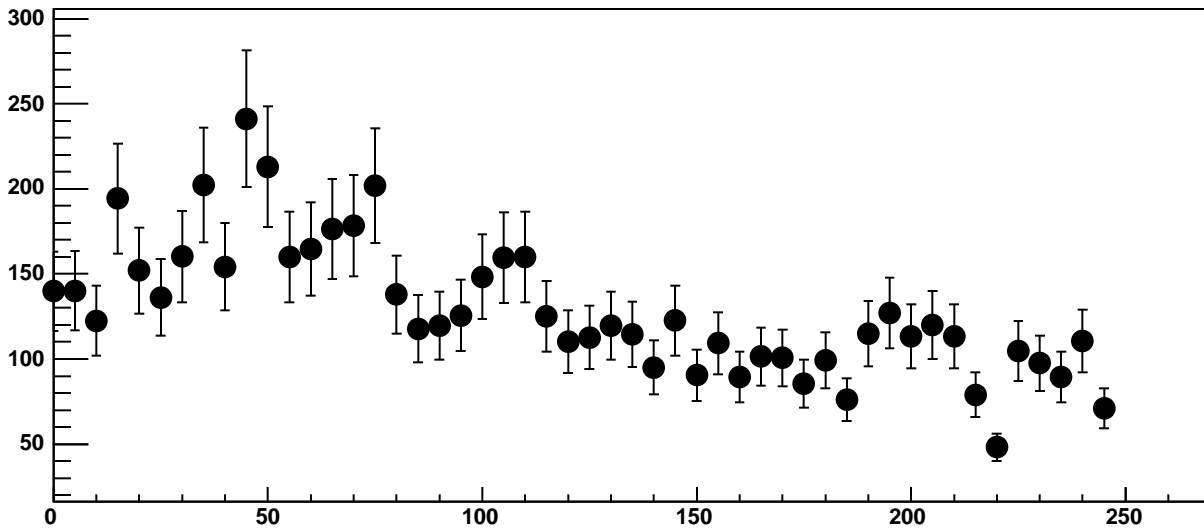


Chip 8, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

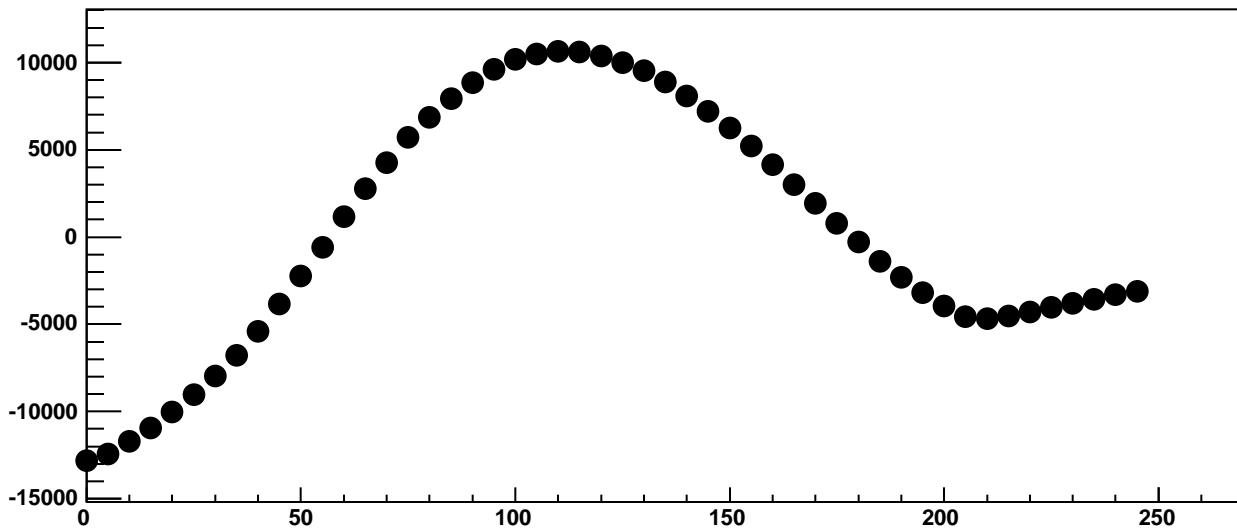


$\chi^2 / \text{ndf}$	2.486e+06 / 41
p0	9440 ± 20.32
p1	-148.7 ± 0.3394
p2	9557 ± 27.74
p3	-1496 ± 22.79
p4	-46.99 ± 0.05761

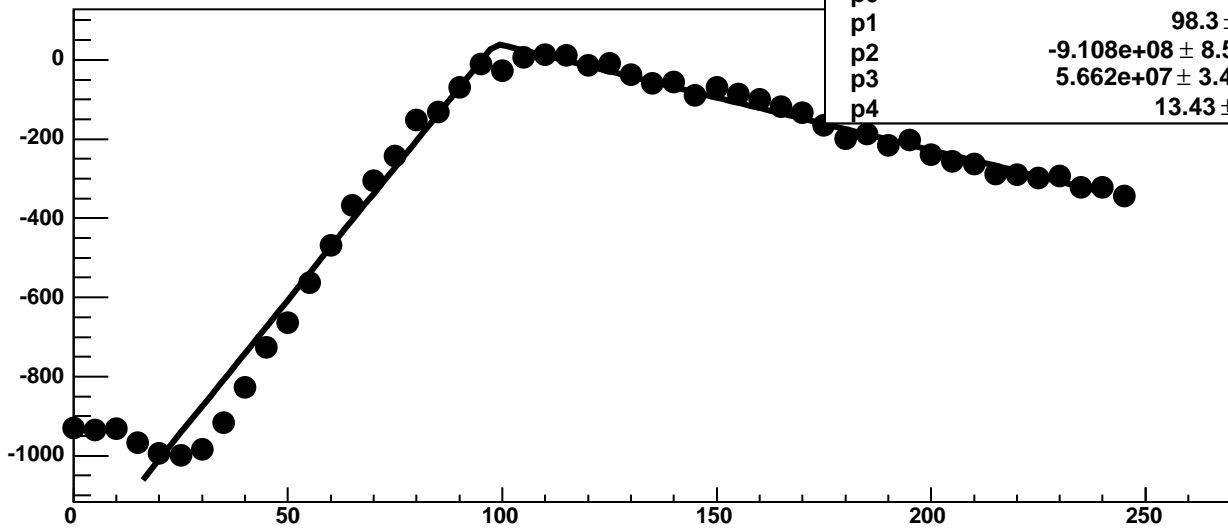
Chip 8, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold

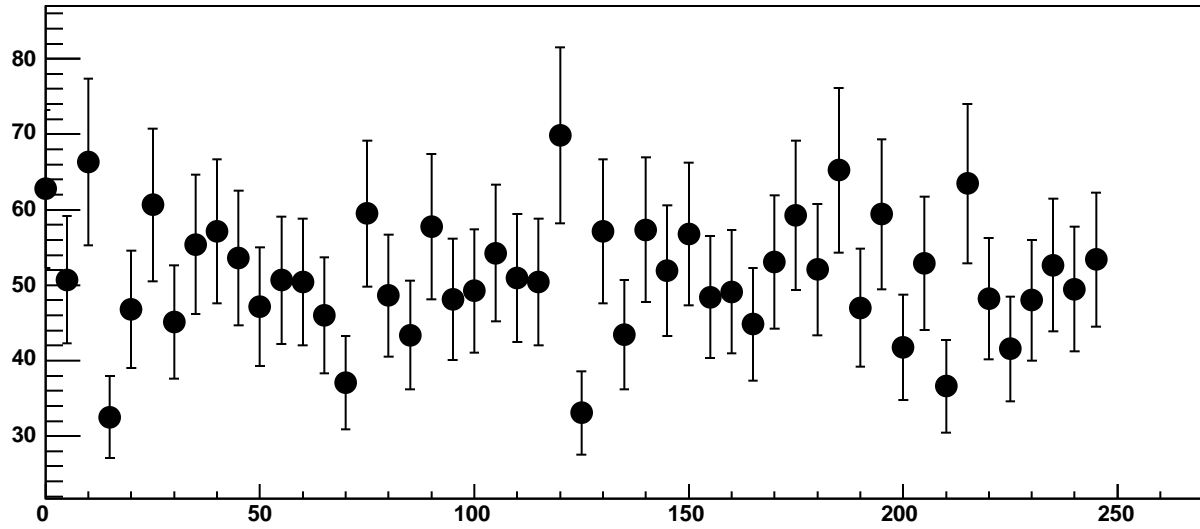


Chip 8, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

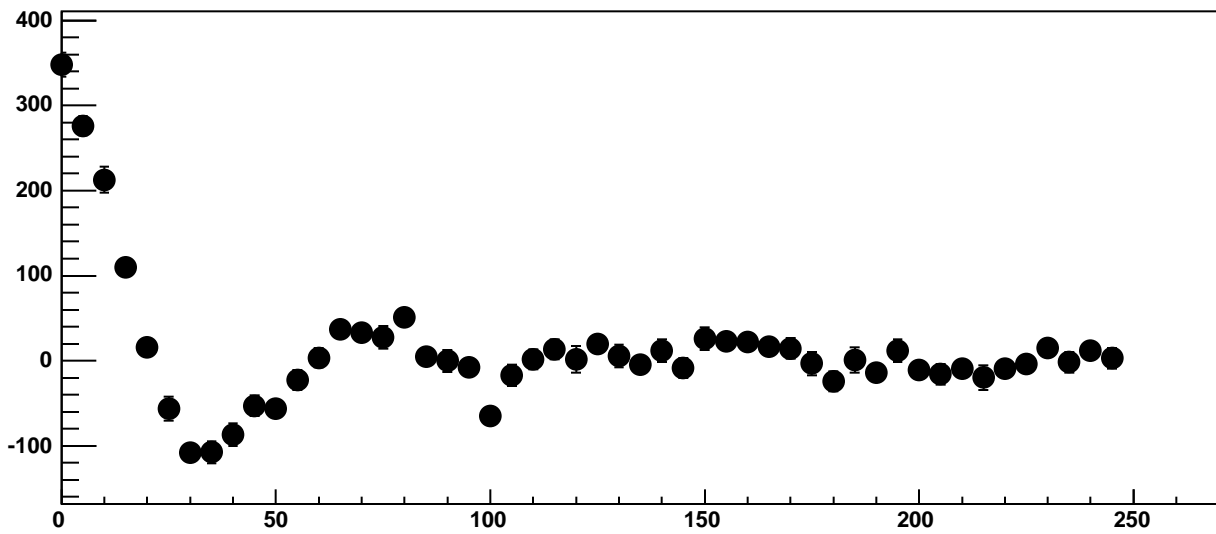


$\chi^2 / \text{ndf}$	641 / 41
p0	$42.13 \pm 3.602$
p1	$98.3 \pm 0.4211$
p2	$-9.108\text{e}+08 \pm 8.559\text{e}+06$
p3	$5.662\text{e}+07 \pm 3.413\text{e}+05$
p4	$13.43 \pm 0.1027$

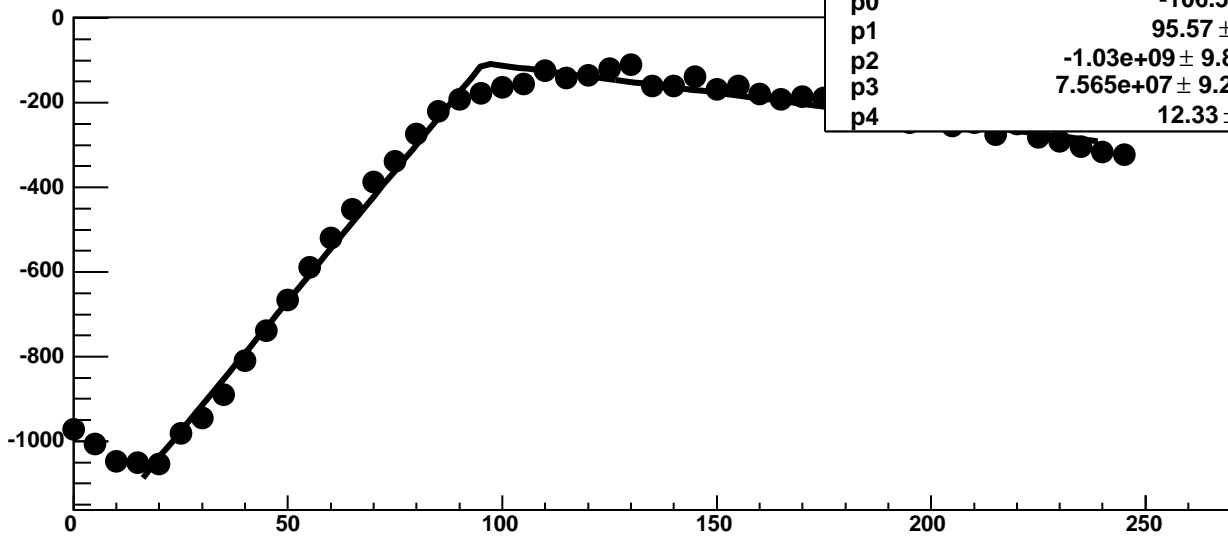
Chip 8, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

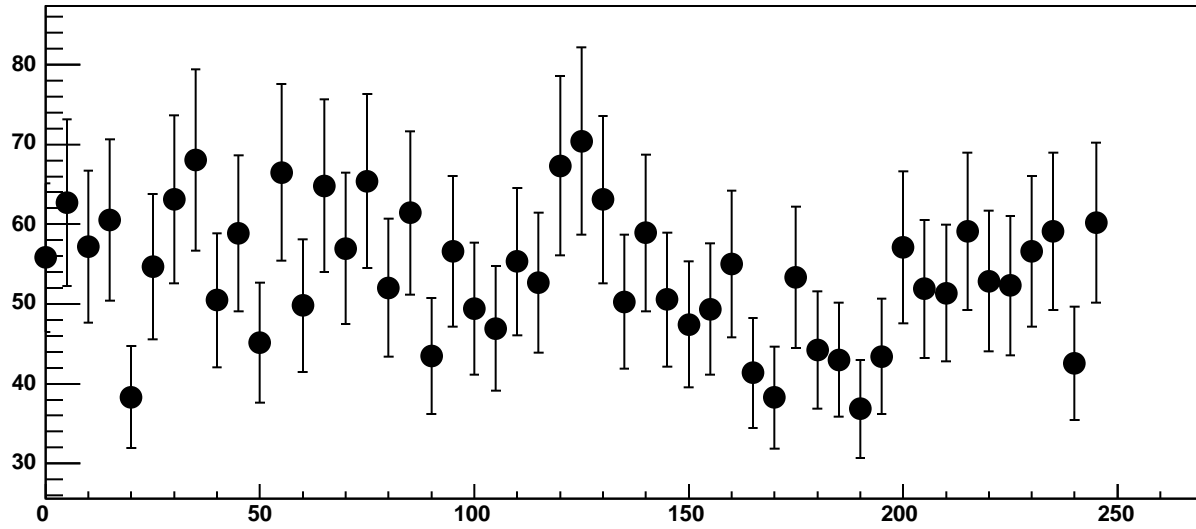


Chip 8, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

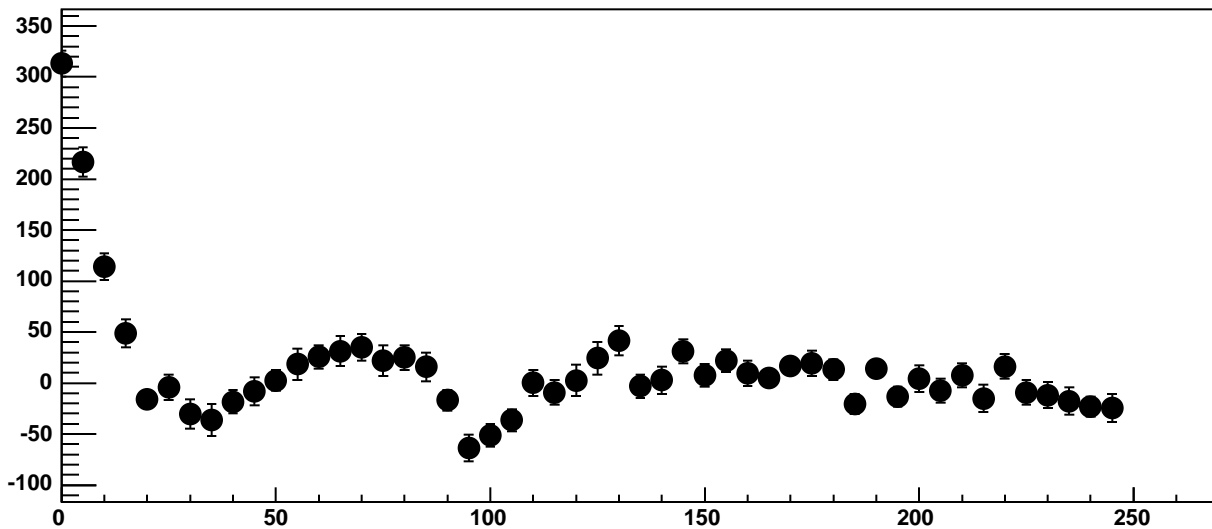


$\chi^2 / \text{ndf}$	165.8 / 41
p0	$-106.5 \pm 4.195$
p1	$95.57 \pm 0.5375$
p2	$-1.03\text{e}+09 \pm 9.873\text{e}+06$
p3	$7.565\text{e}+07 \pm 9.292\text{e}+04$
p4	$12.33 \pm 0.1181$

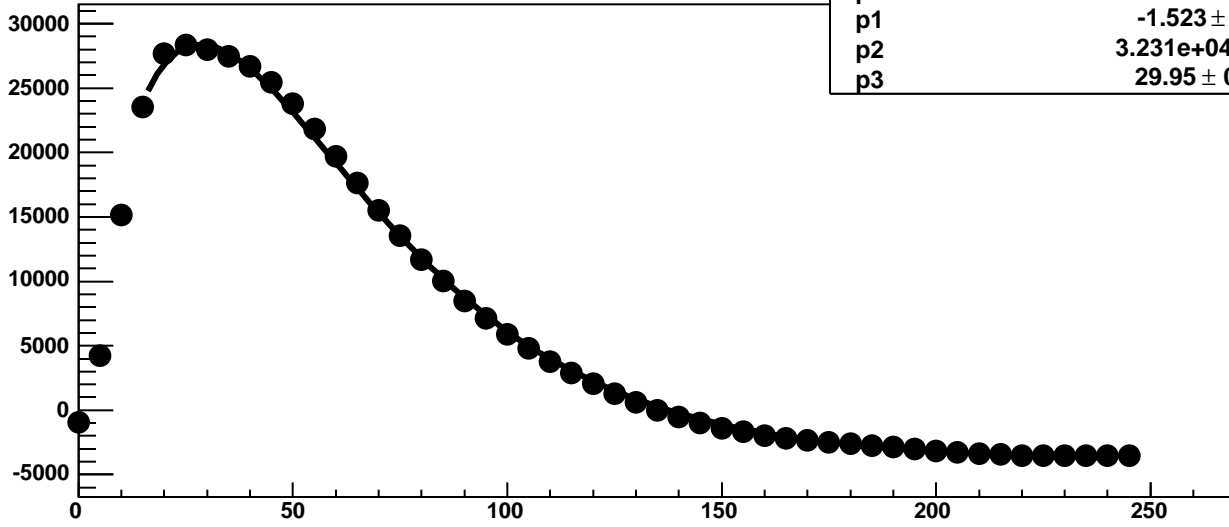
Chip 8, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

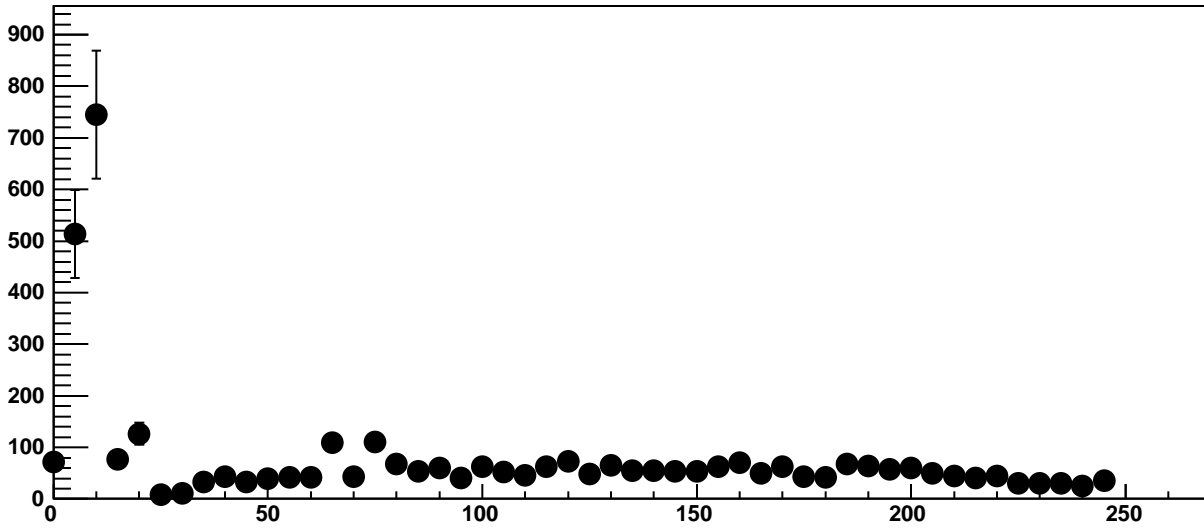


Chip 8, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

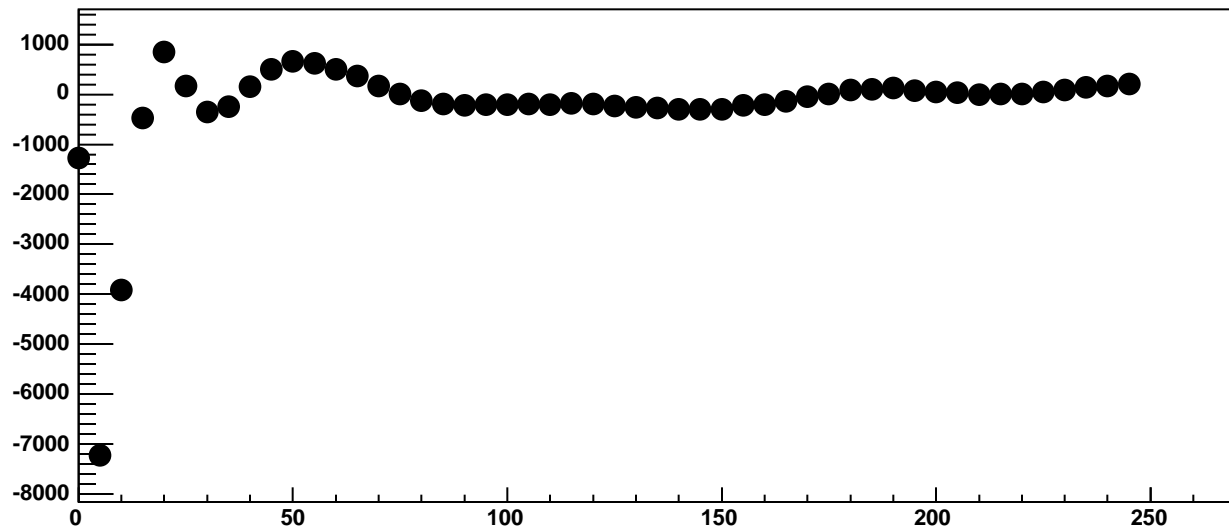


$\chi^2 / \text{ndf}$	5.388e+04 / 42
p0	-3920 ± 2.694
p1	-1.523 ± 0.01615
p2	3.231e+04 ± 2.906
p3	29.95 ± 0.009061

Chip 8, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

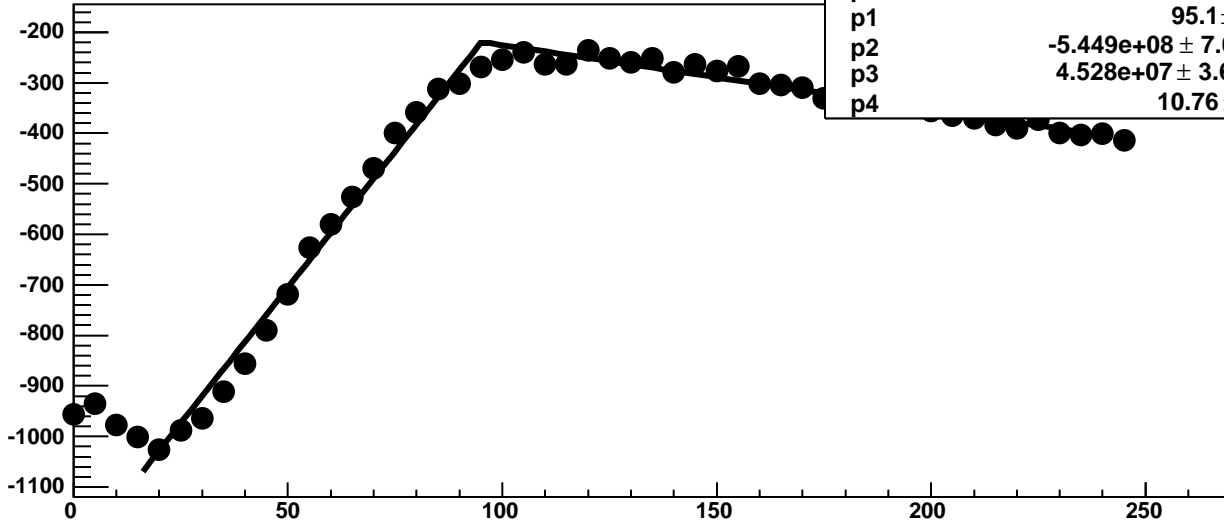


Chip 8, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold



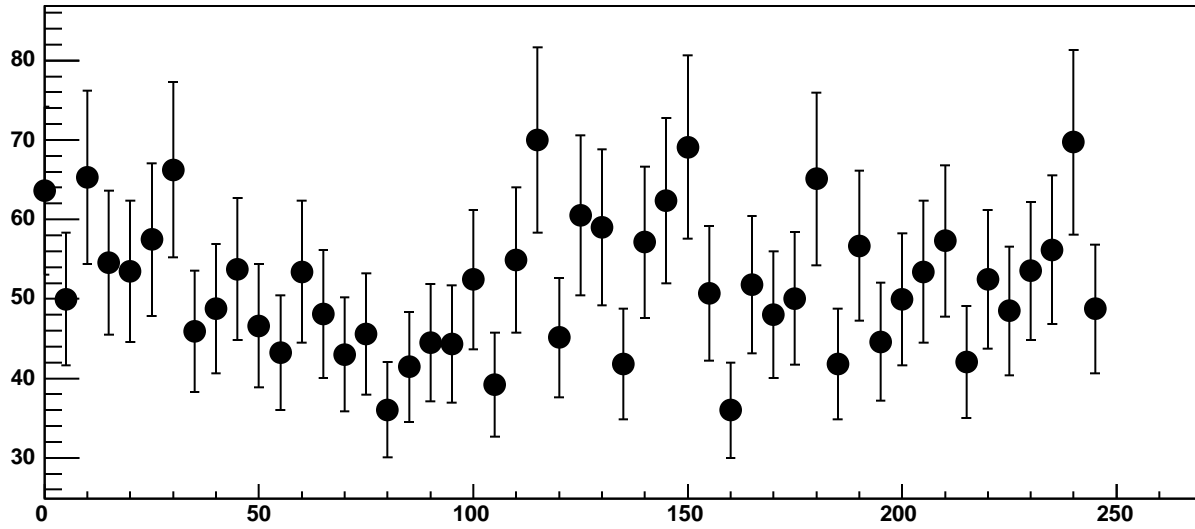


Chip 8, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

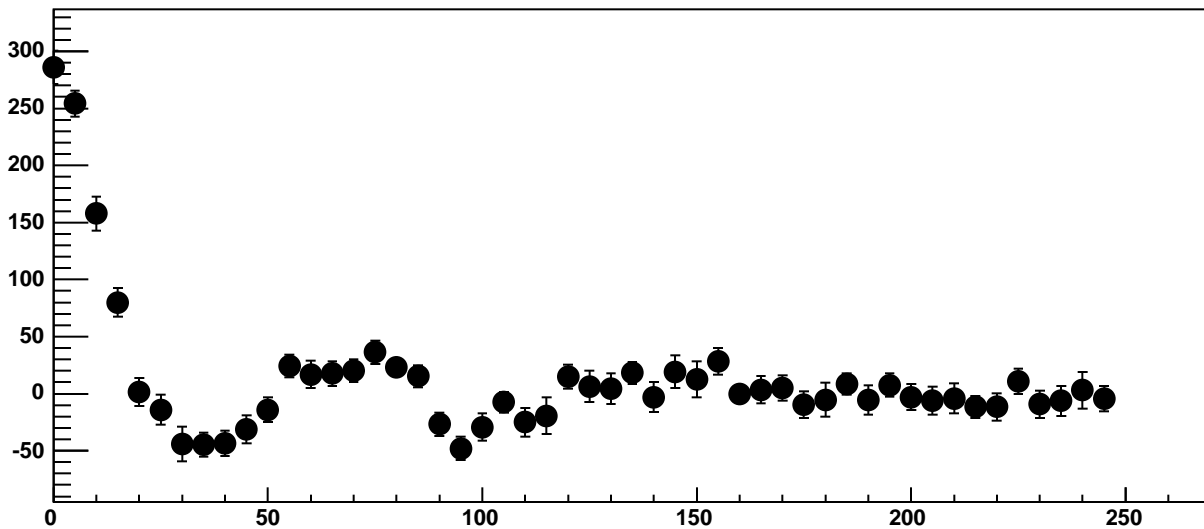


$\chi^2 / \text{ndf}$	191.3 / 41
p0	$-219.3 \pm 4.025$
p1	$95.1 \pm 0.5379$
p2	$-5.449\text{e}+08 \pm 7.015\text{e}+06$
p3	$4.528\text{e}+07 \pm 3.624\text{e}+05$
p4	$10.76 \pm 0.1101$

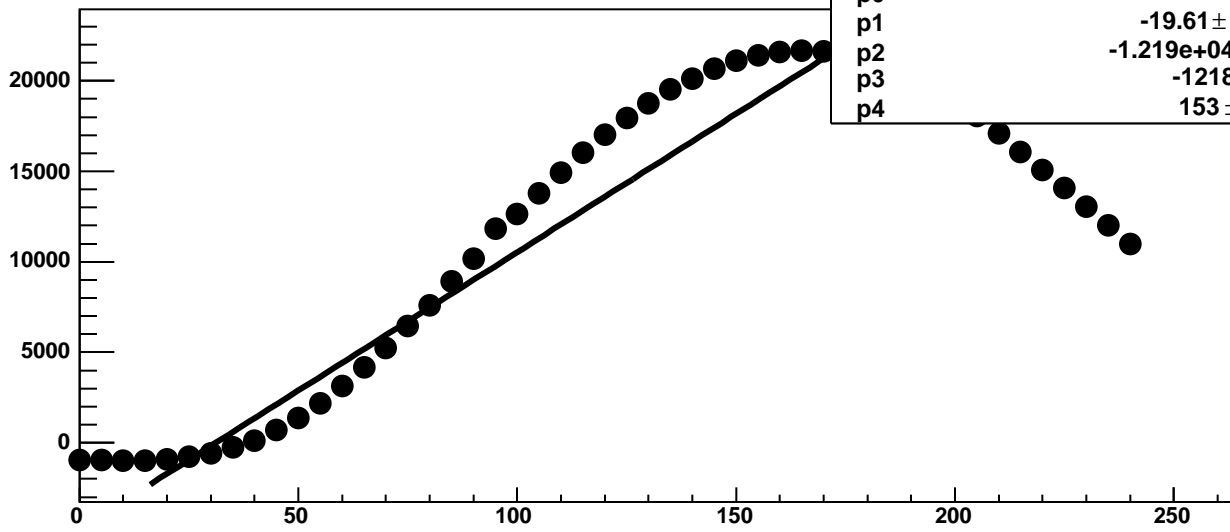
Chip 8, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



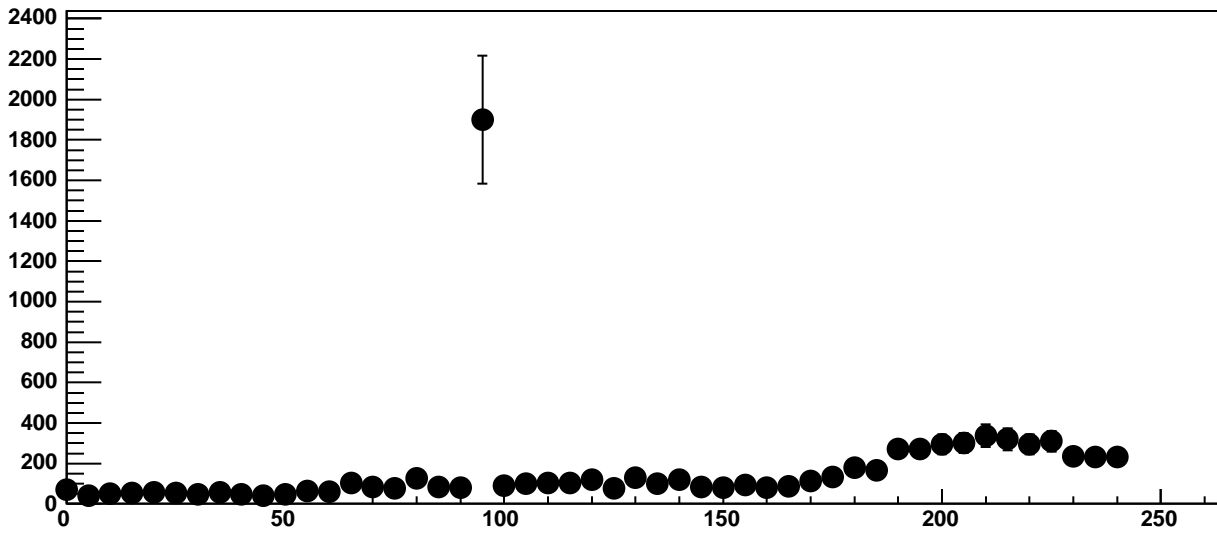
Chip 8, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold



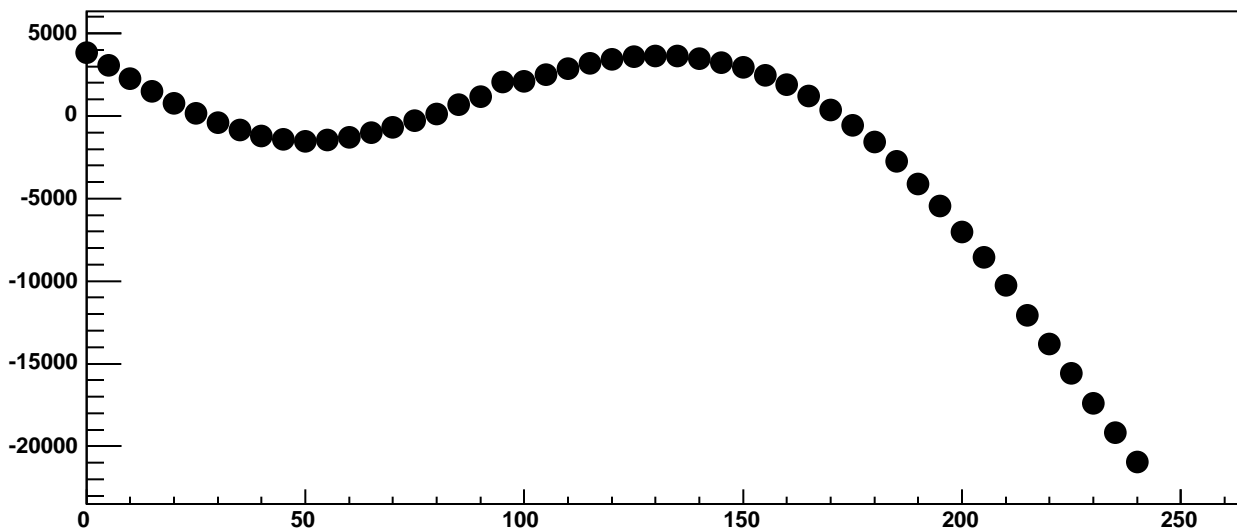
Chip 8, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold



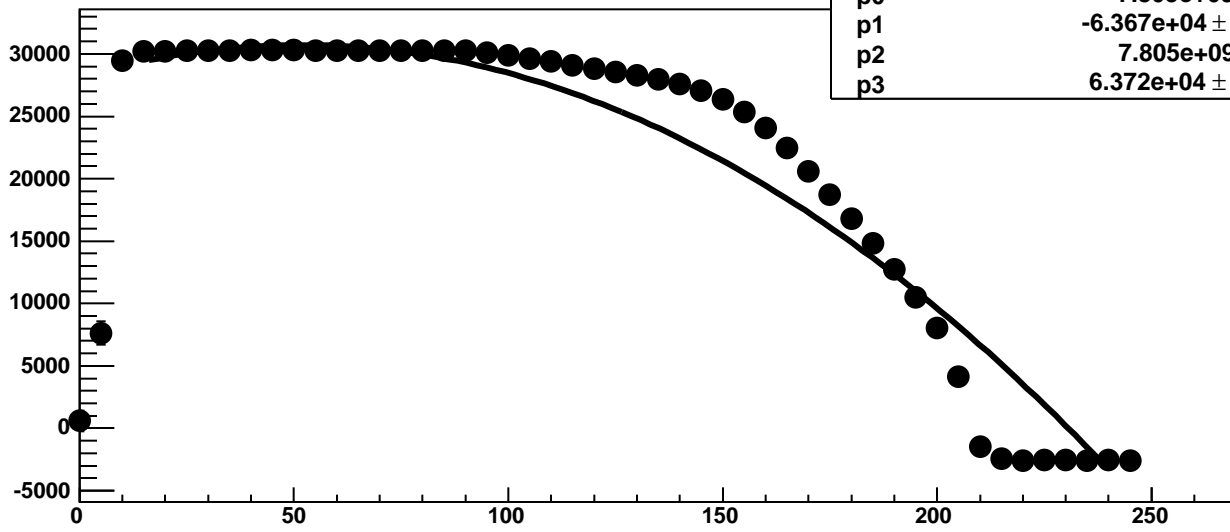
Chip 8, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

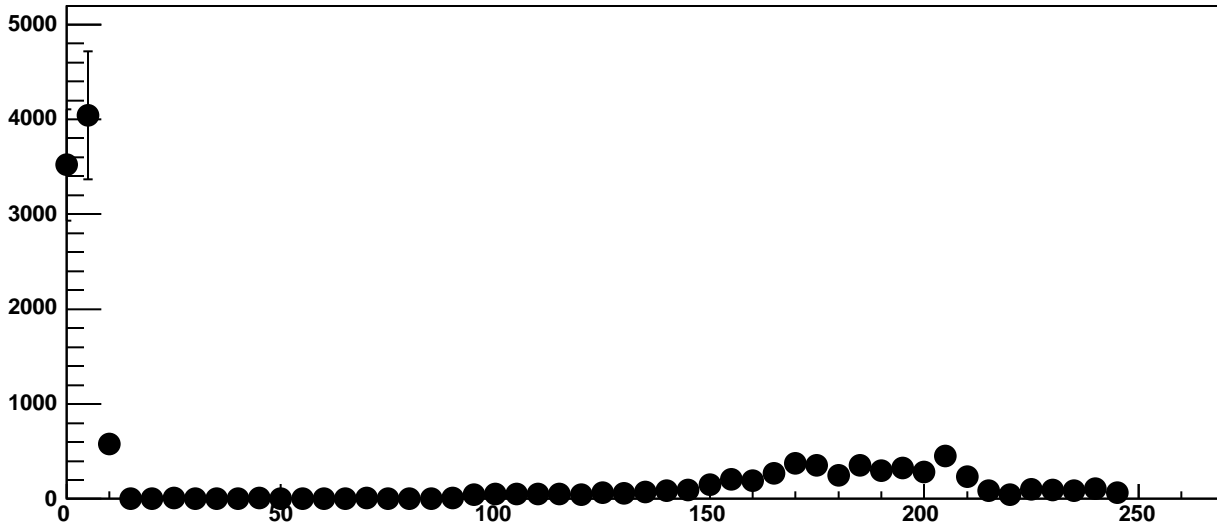


Chip 8, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold

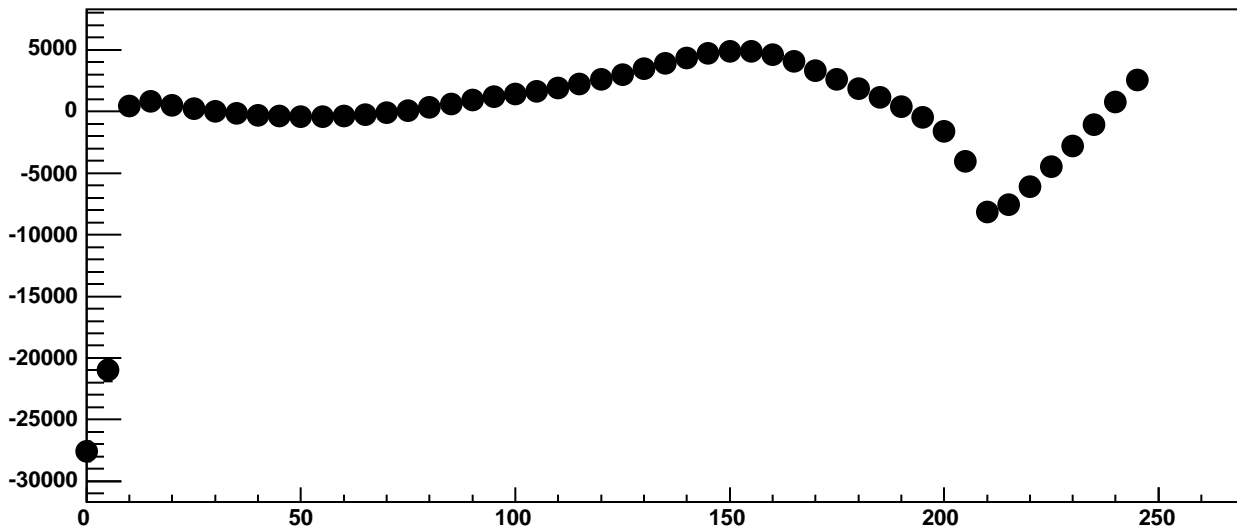


$\chi^2 / \text{ndf}$	2.756e+06 / 42
p0	-7.805e+09 ± 4.533
p1	-6.367e+04 ± 0.09418
p2	7.805e+09 ± 4.533
p3	6.372e+04 ± 0.09415

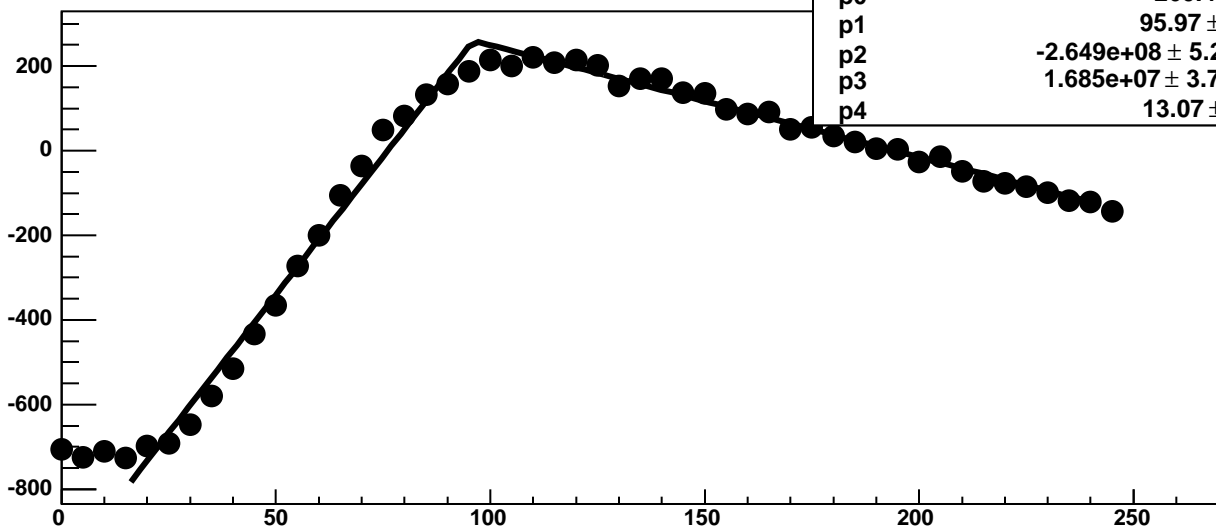
Chip 8, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



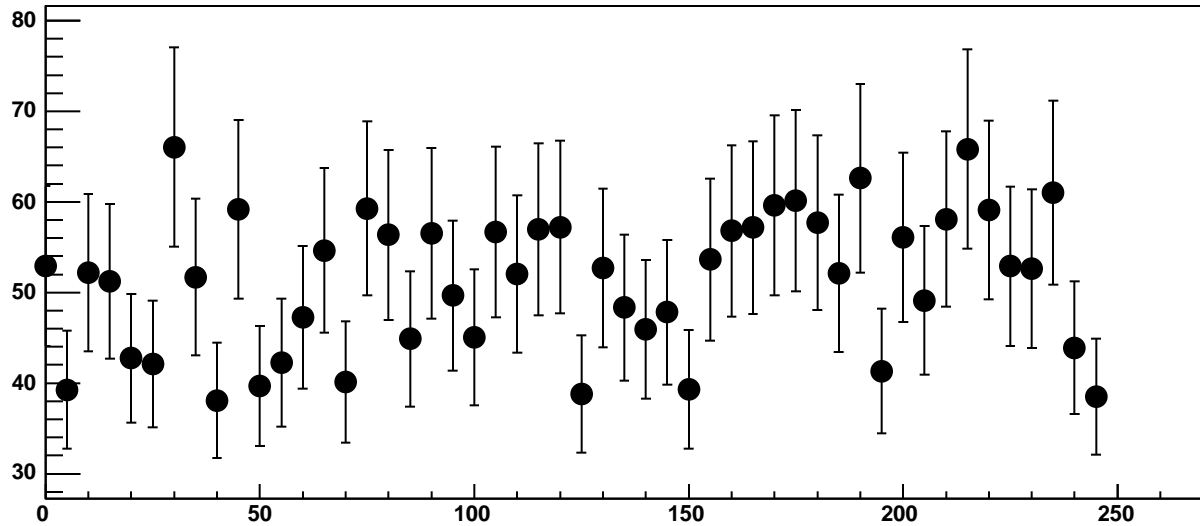
Chip 8, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold



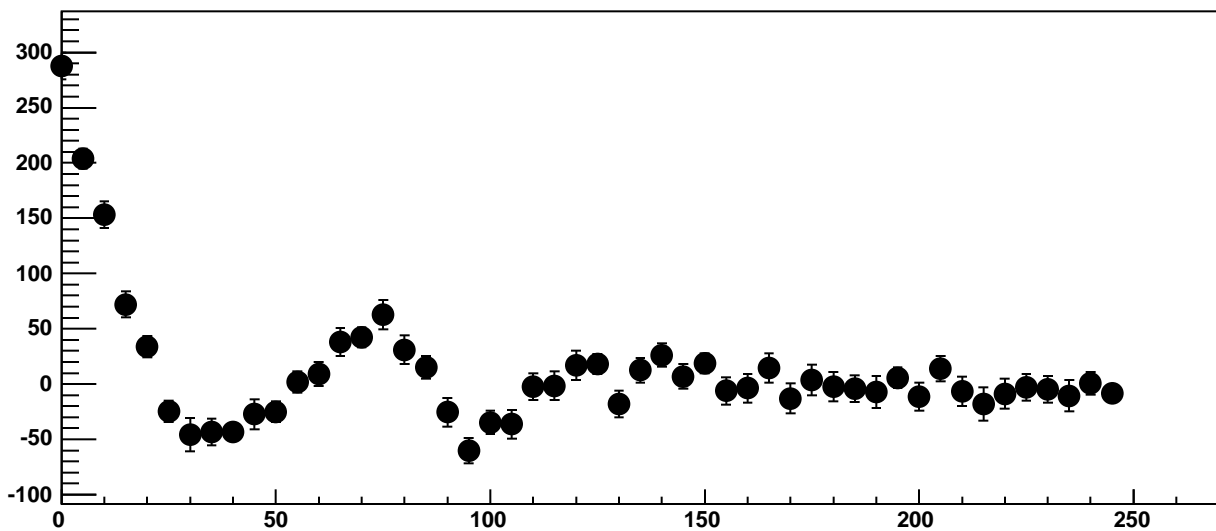
Chip 8, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold



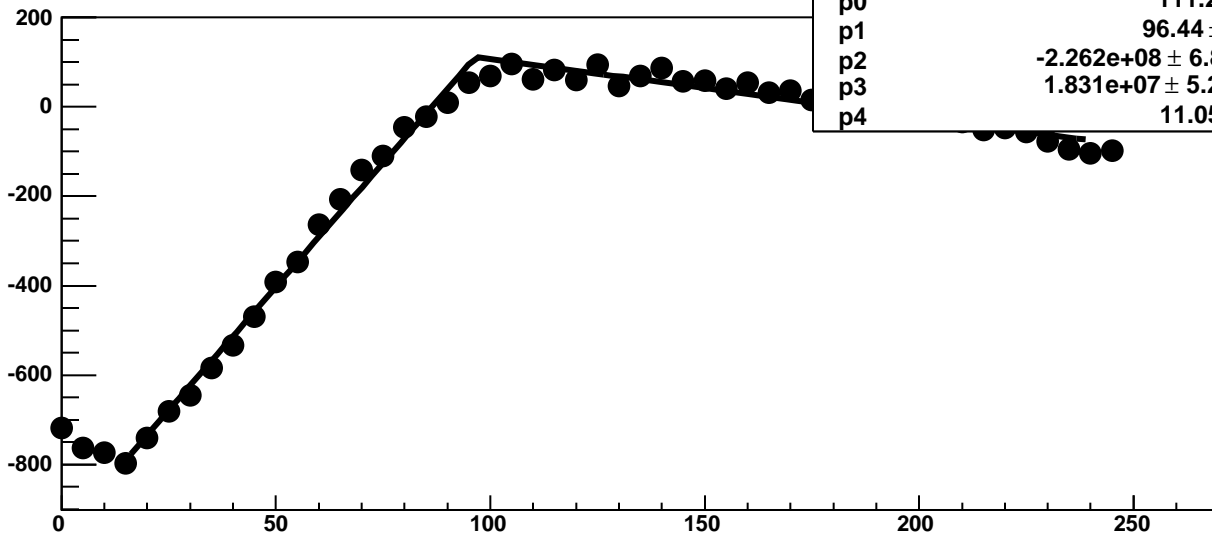
Chip 8, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold

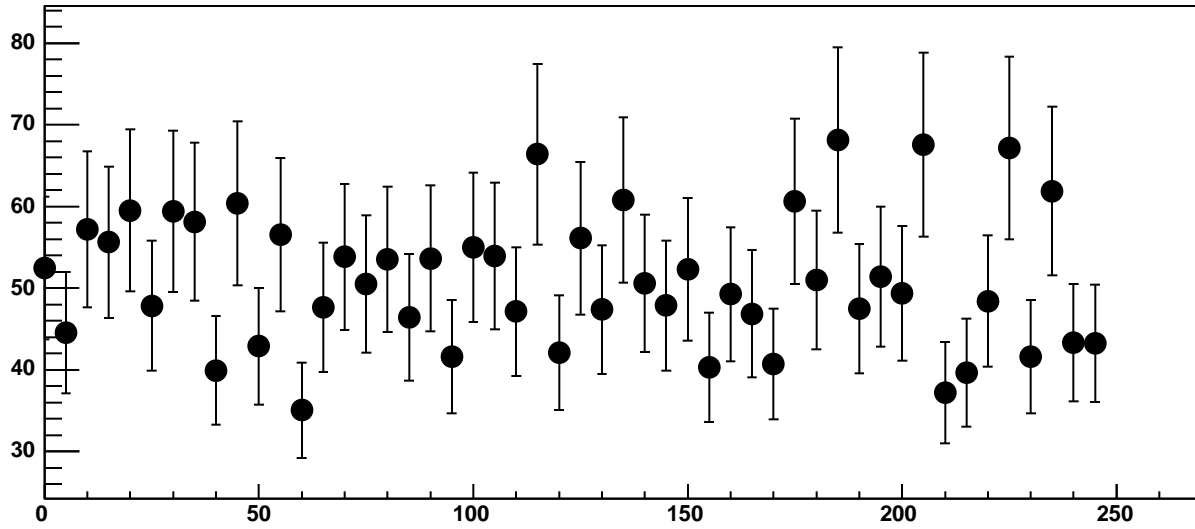


Chip 8, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

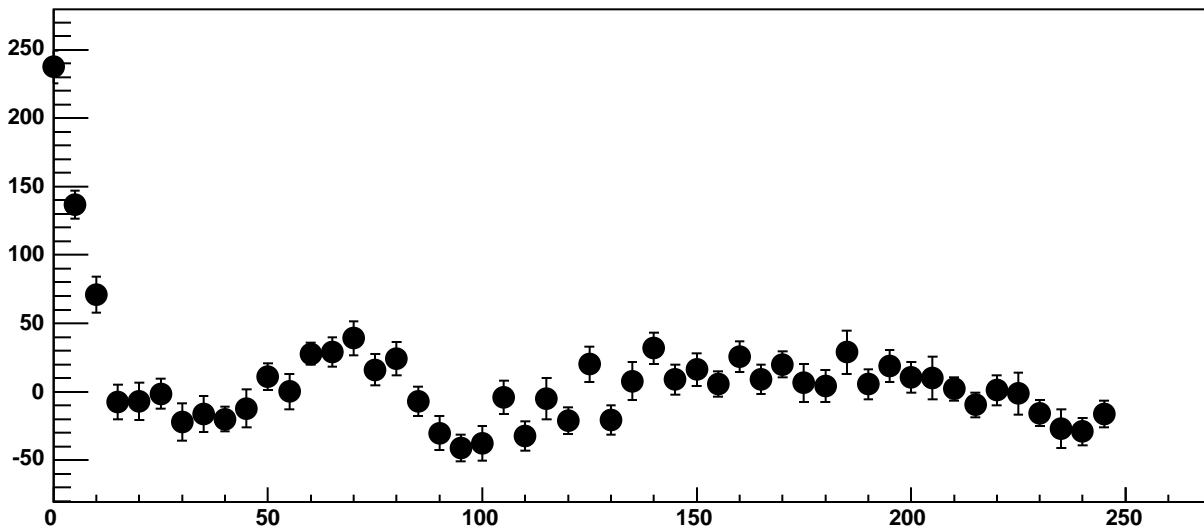


$\chi^2 / \text{ndf}$	145.4 / 41
p0	$111.2 \pm 3.956$
p1	$96.44 \pm 0.5549$
p2	$-2.262\text{e}+08 \pm 6.876\text{e}+06$
p3	$1.831\text{e}+07 \pm 5.265\text{e}+05$
p4	$11.05 \pm 0.115$

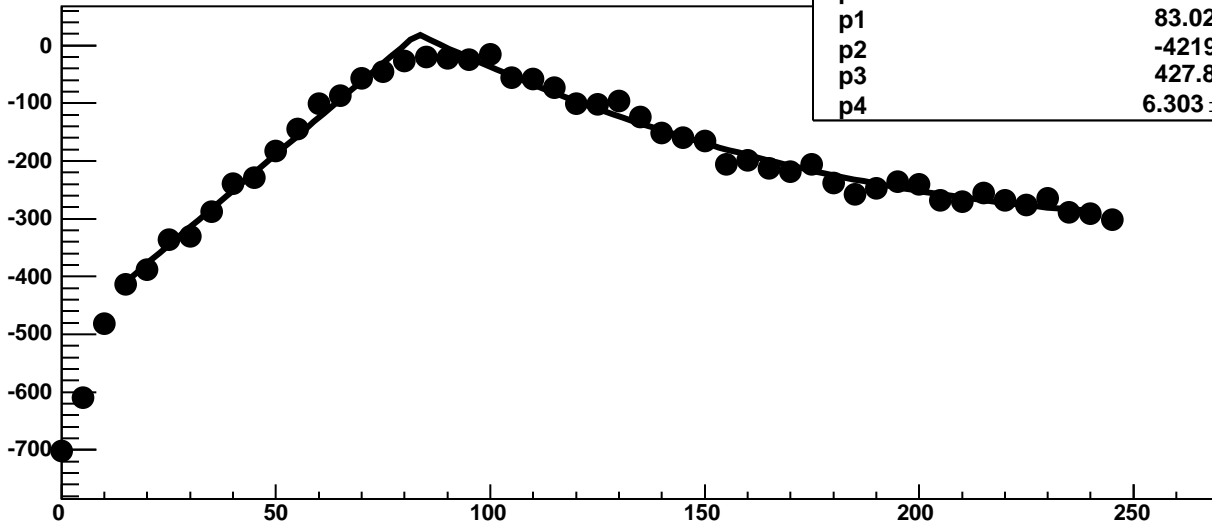
Chip 8, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

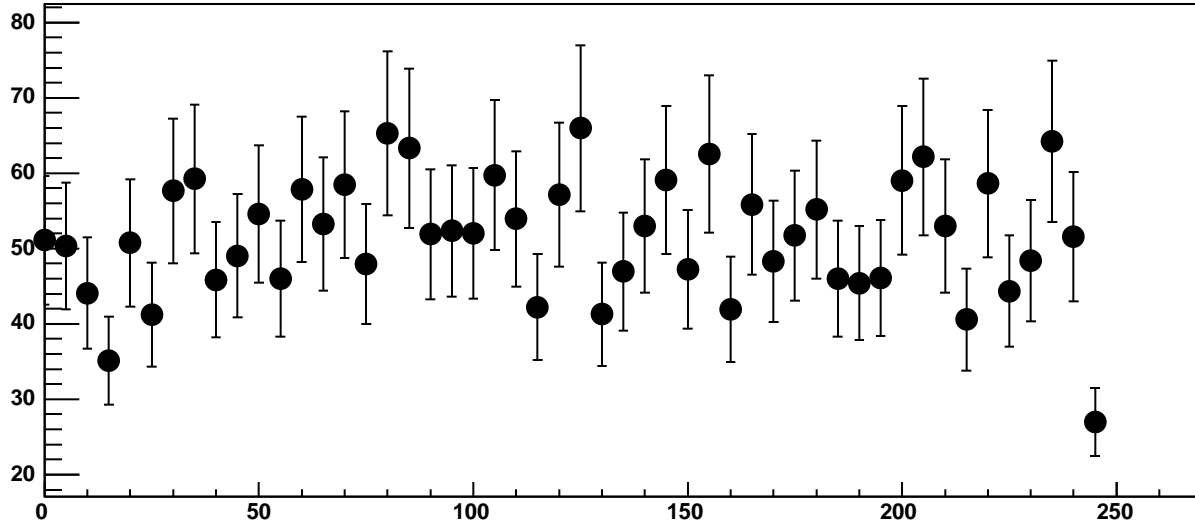


Chip 8, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

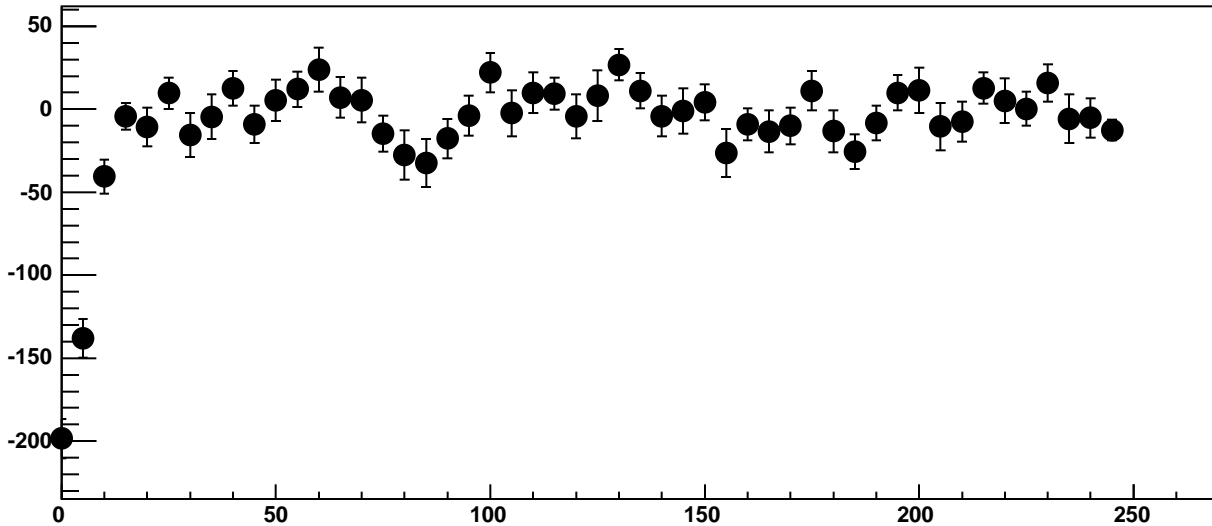


$\chi^2 / \text{ndf}$	59.94 / 41
p0	$19.85 \pm 4.947$
p1	$83.02 \pm 0.959$
p2	$-4219 \pm 430.9$
p3	$427.8 \pm 50.29$
p4	$6.303 \pm 0.1459$

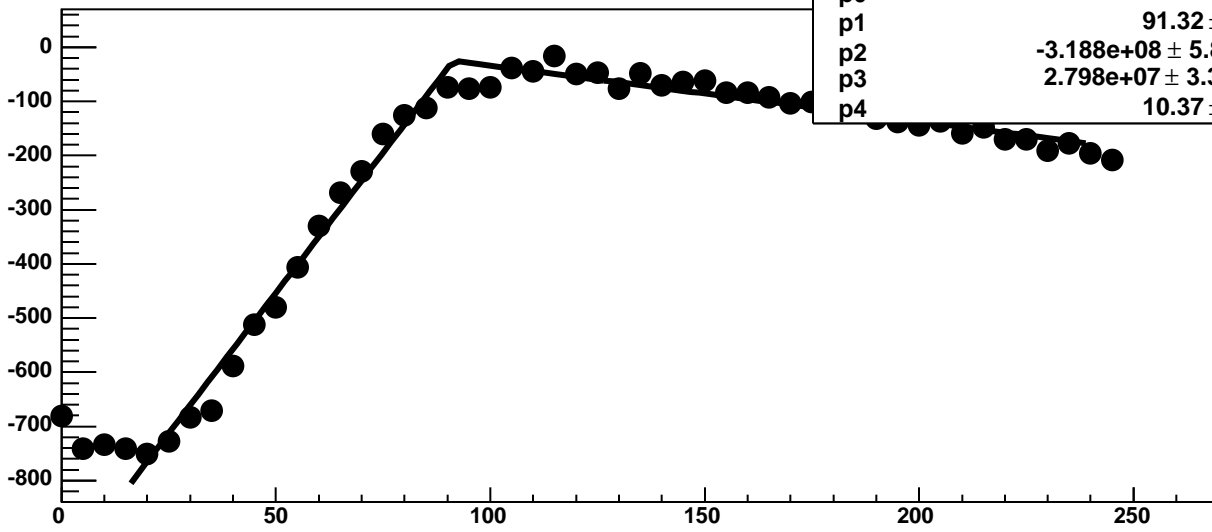
Chip 8, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold

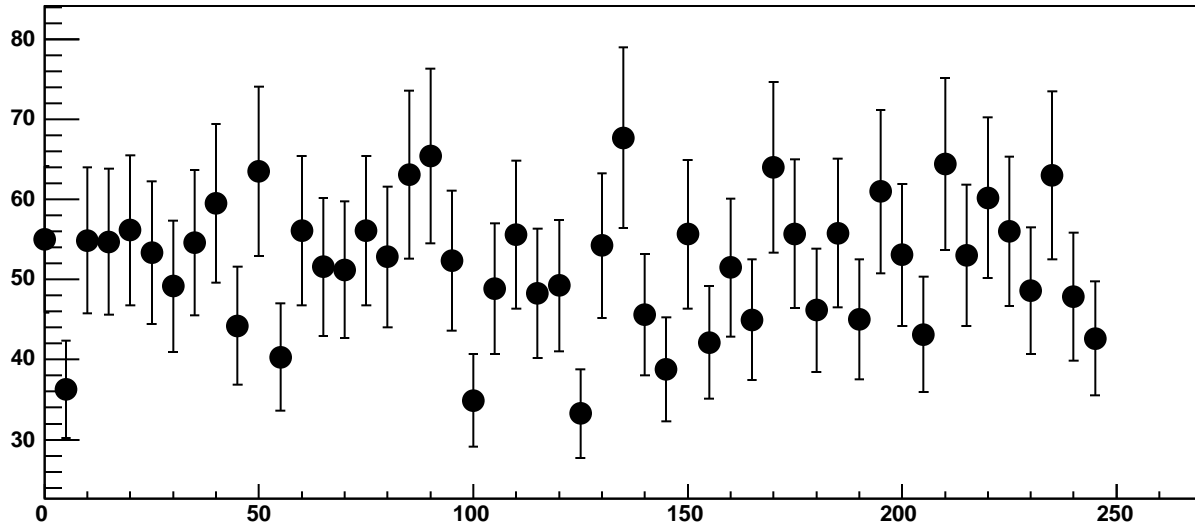


Chip 8, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

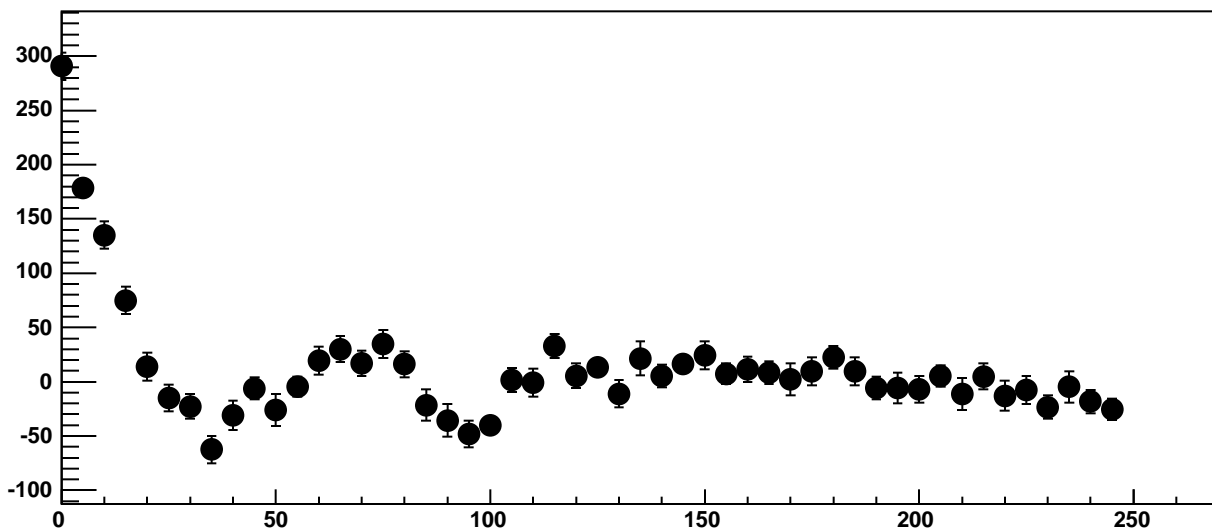


$\chi^2 / \text{ndf}$	185.3 / 41
p0	$-25.04 \pm 3.642$
p1	$91.32 \pm 0.6578$
p2	$-3.188\text{e}+08 \pm 5.892\text{e}+06$
p3	$2.798\text{e}+07 \pm 3.328\text{e}+05$
p4	$10.37 \pm 0.1407$

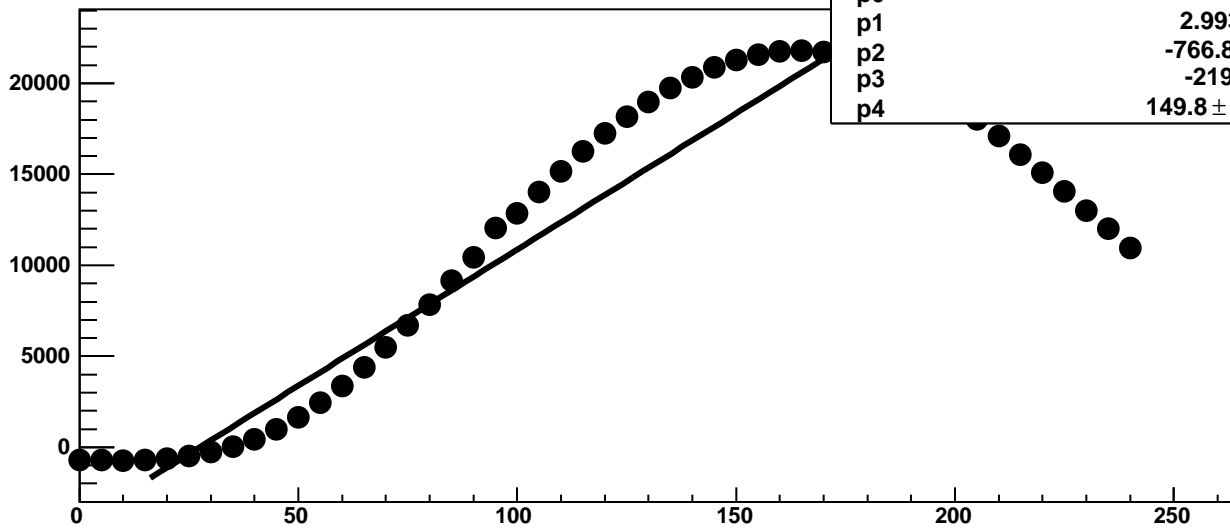
Chip 8, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

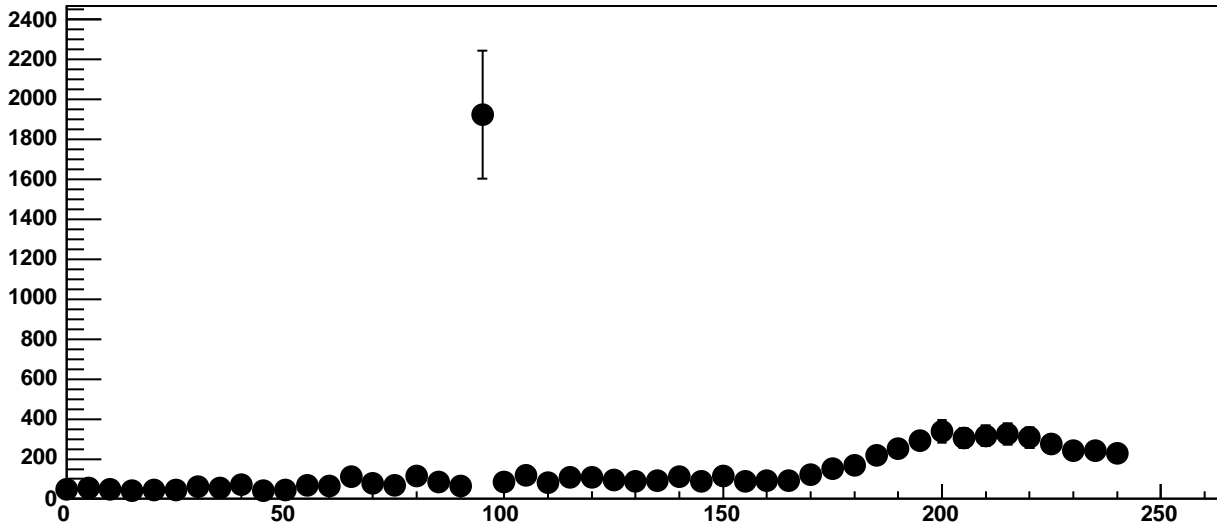


Chip 8, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

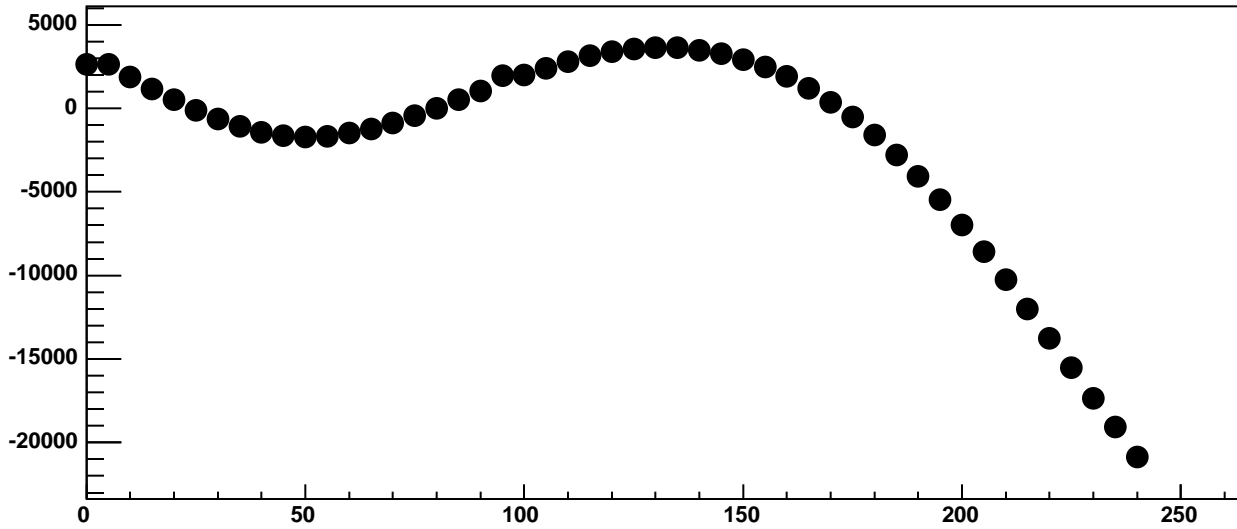


$\chi^2 / \text{ndf}$	9.295e+05 / 41
p0	-2898 ± 20.13
p1	2.993 ± 0.12
p2	-766.8 ± 22.24
p3	-219 ± 19.88
p4	149.8 ± 0.03917

Chip 8, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

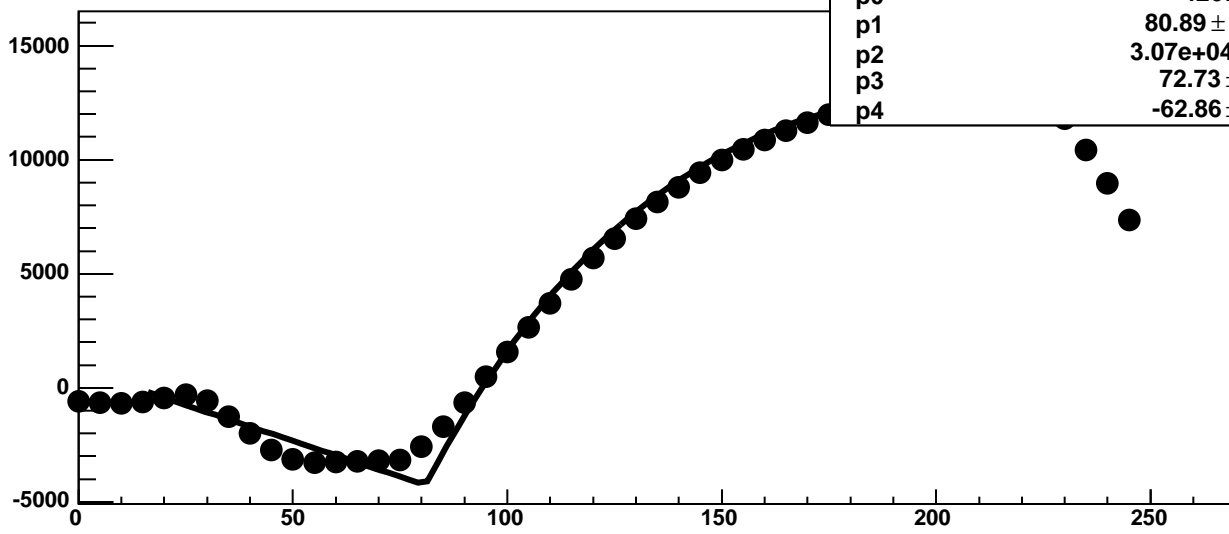


Chip 8, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



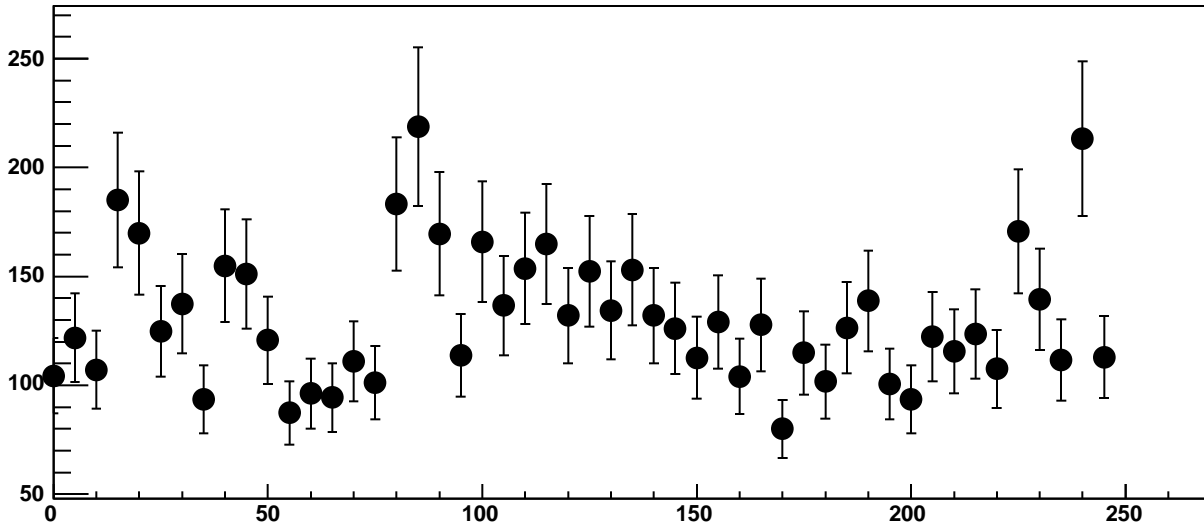


Chip 8, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

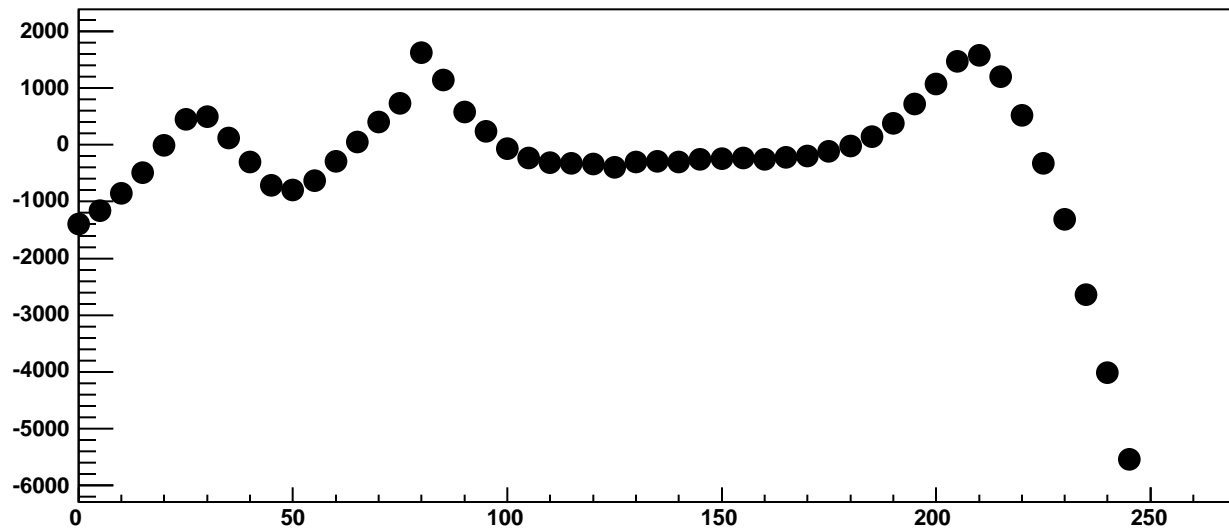


$\chi^2 / \text{ndf}$	3.925e+04 / 41
p0	-4267 ± 11.88
p1	80.89 ± 0.06902
p2	3.07e+04 ± 102.6
p3	72.73 ± 0.2679
p4	-62.86 ± 0.3867

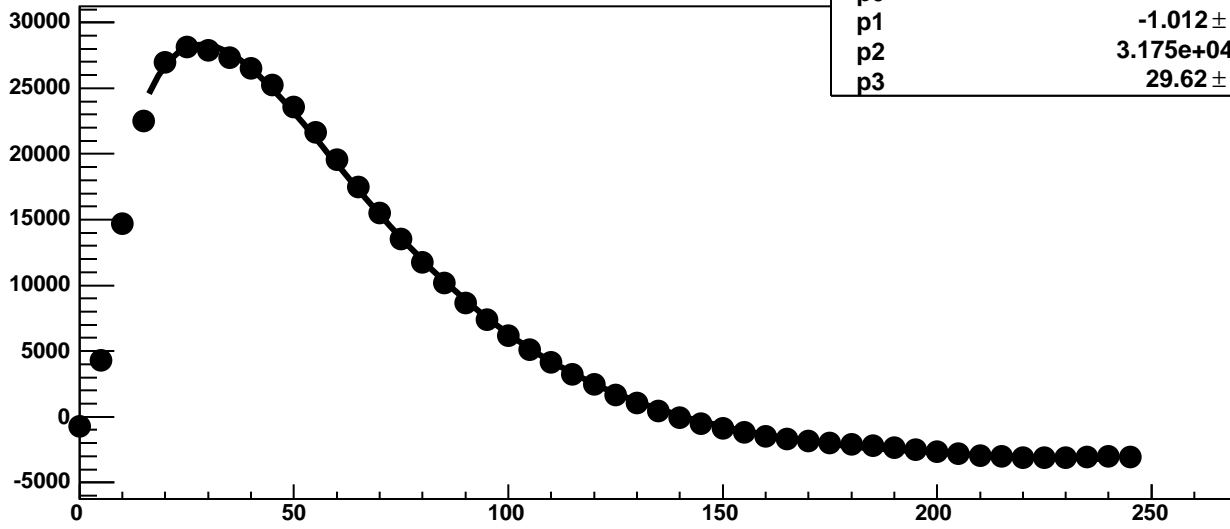
Chip 8, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

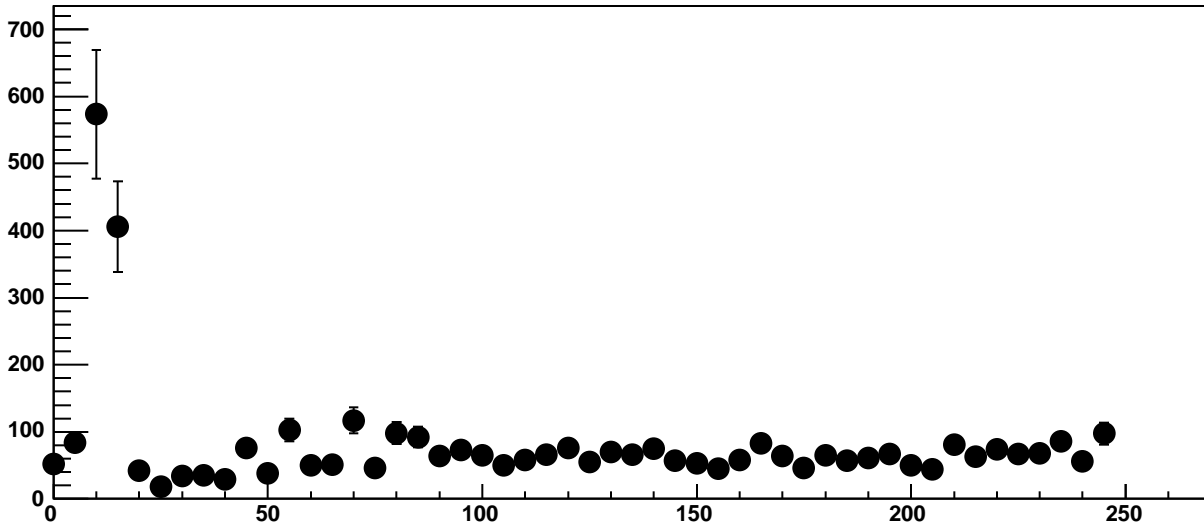


Chip 8, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold

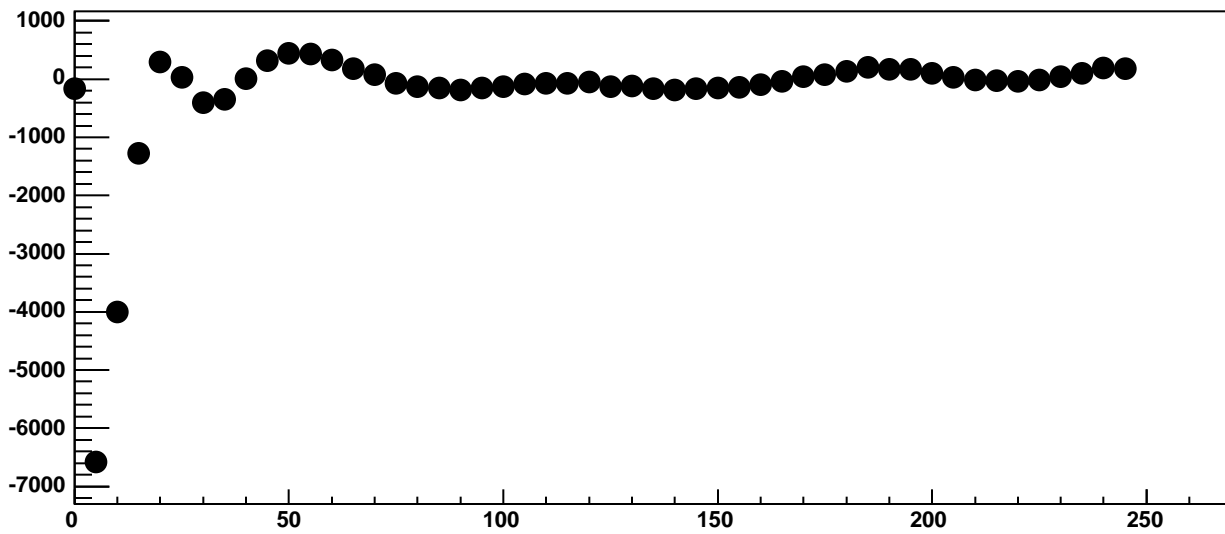


$\chi^2 / \text{ndf}$	1.265e+04 / 42
p0	-3414 ± 4.088
p1	-1.012 ± 0.02189
p2	3.175e+04 ± 4.518
p3	29.62 ± 0.01256

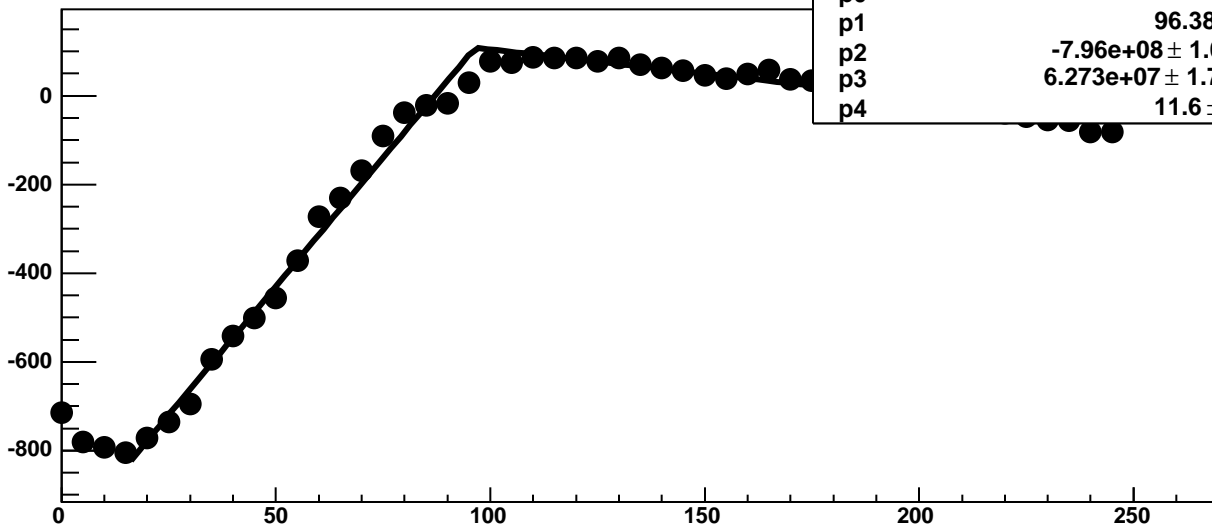
Chip 8, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold

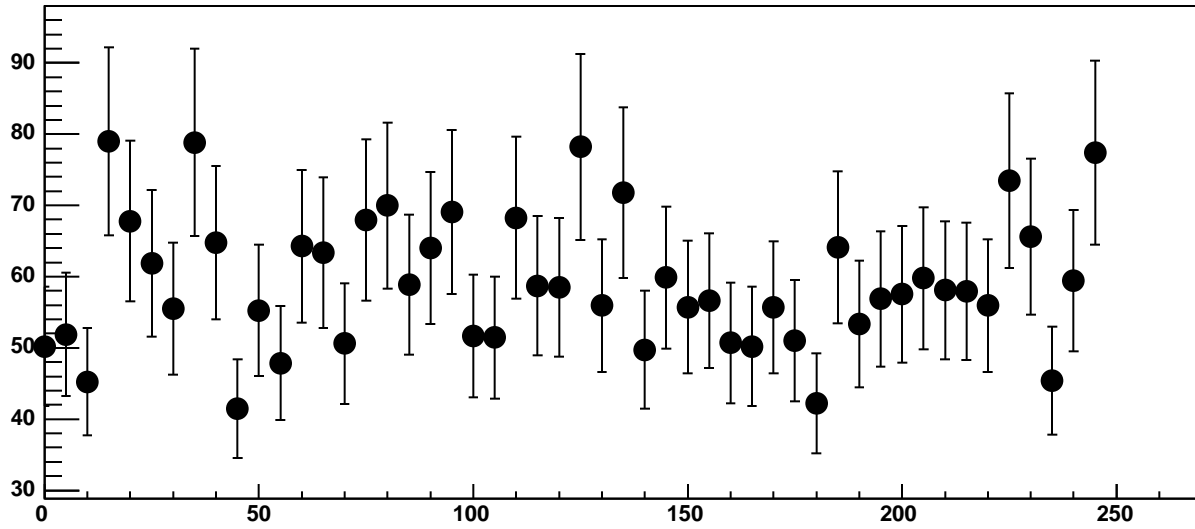


Chip 8, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

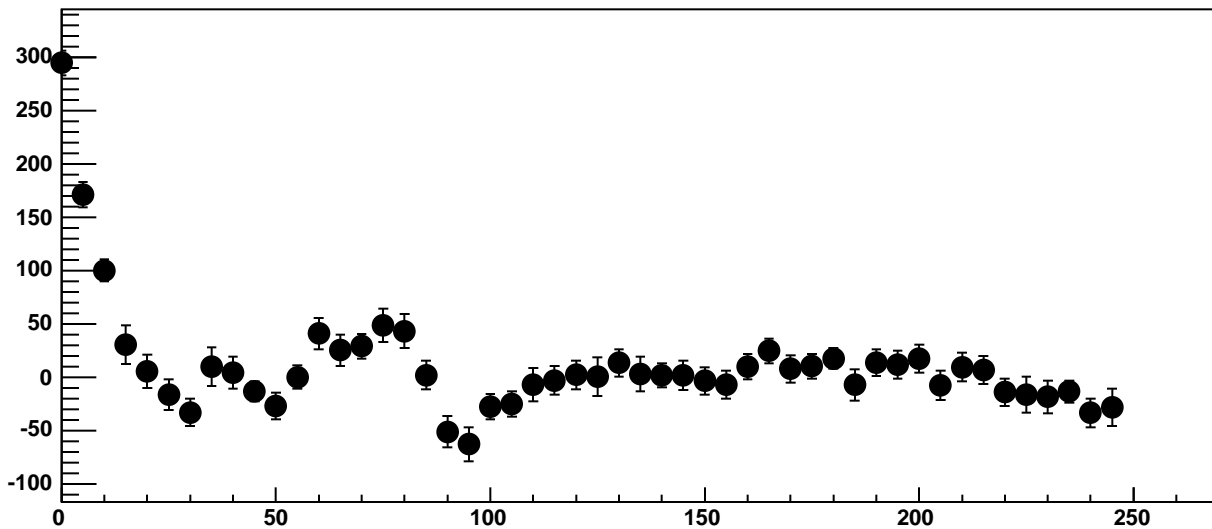


$\chi^2 / \text{ndf}$	117.8 / 41
p0	$108.5 \pm 4.567$
p1	$96.38 \pm 0.672$
p2	$-7.96\text{e}+08 \pm 1.031\text{e}+07$
p3	$6.273\text{e}+07 \pm 1.706\text{e}+05$
p4	$11.6 \pm 0.1484$

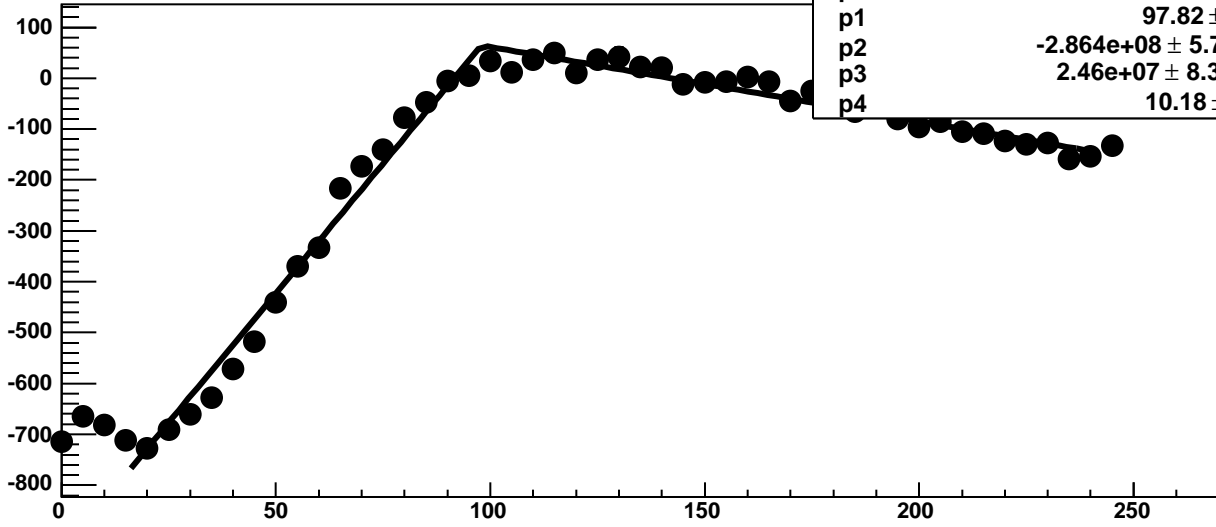
Chip 8, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

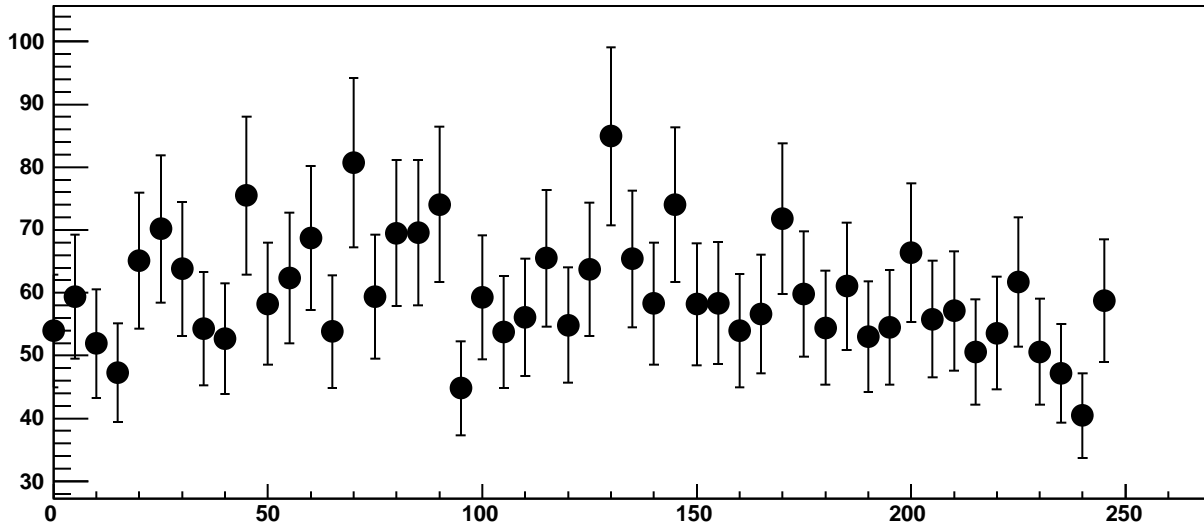


Chip 8, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

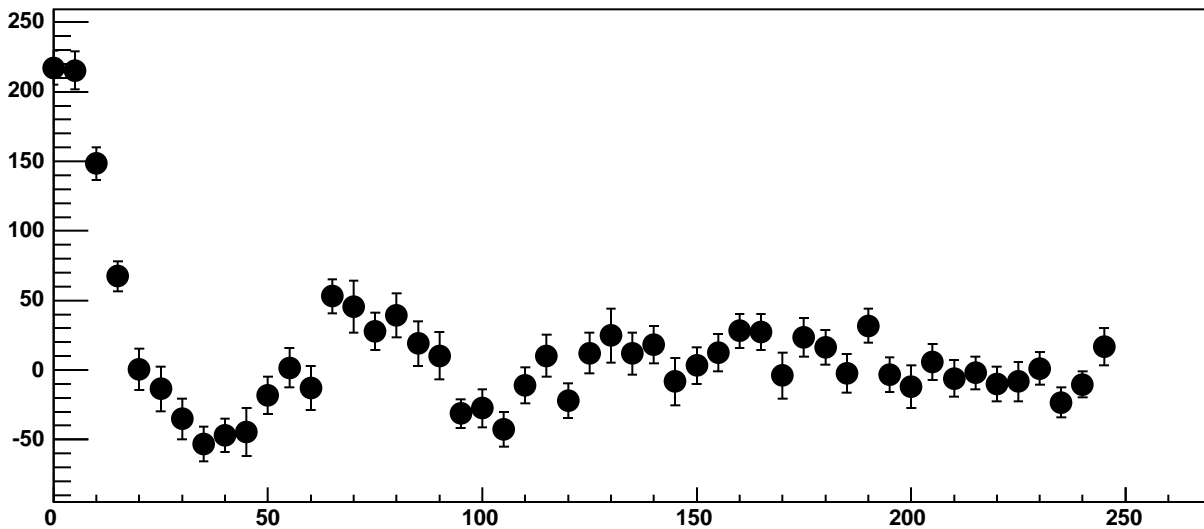


$\chi^2 / \text{ndf}$	188.6 / 41
p0	64.61 ± 5.238
p1	97.82 ± 0.5202
p2	-2.864e+08 ± 5.755e+06
p3	2.46e+07 ± 8.303e+05
p4	10.18 ± 0.1331

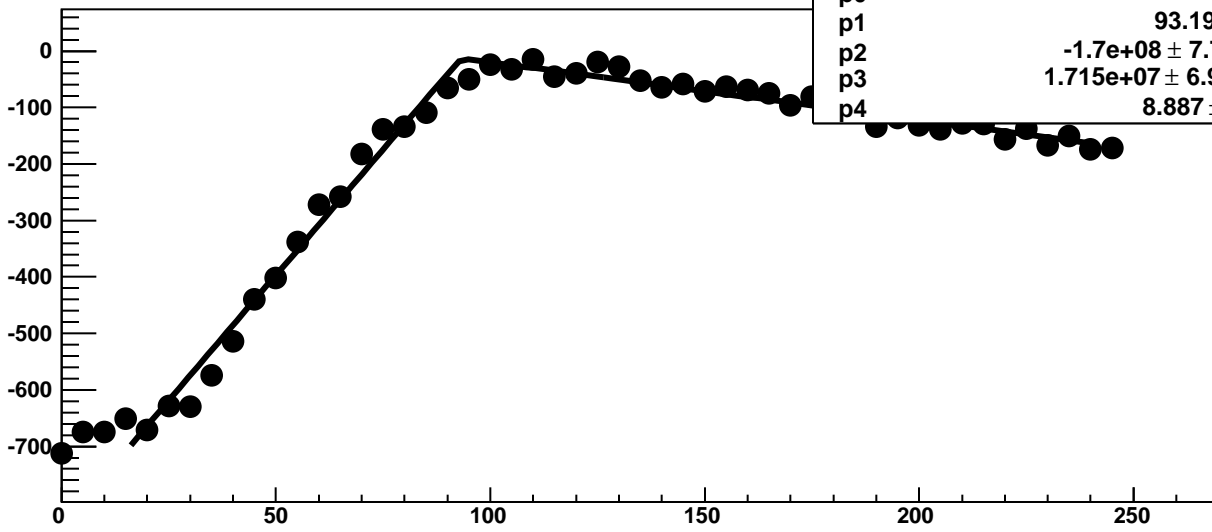
Chip 8, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

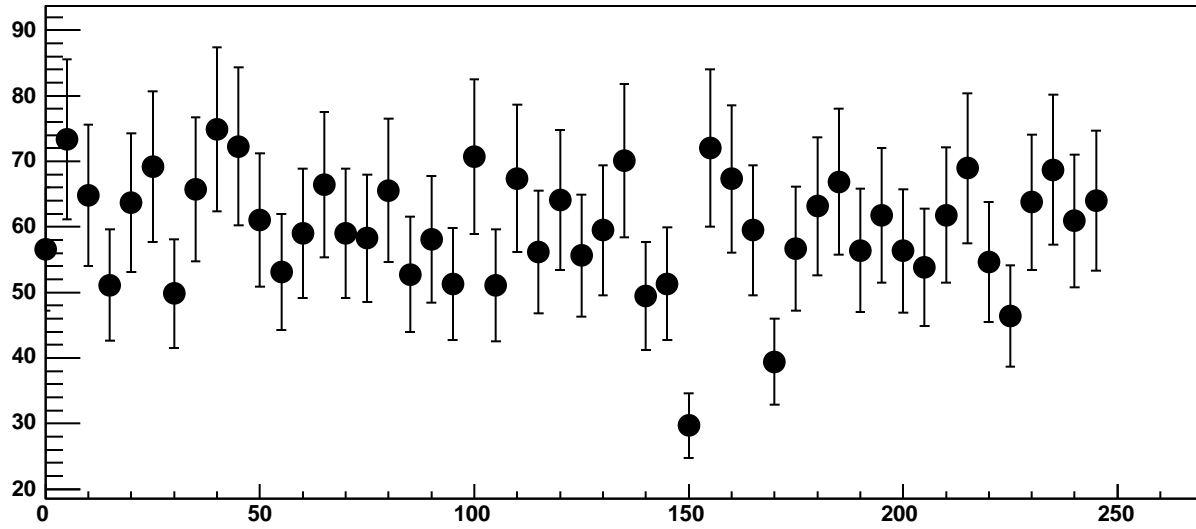


Chip 8, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold

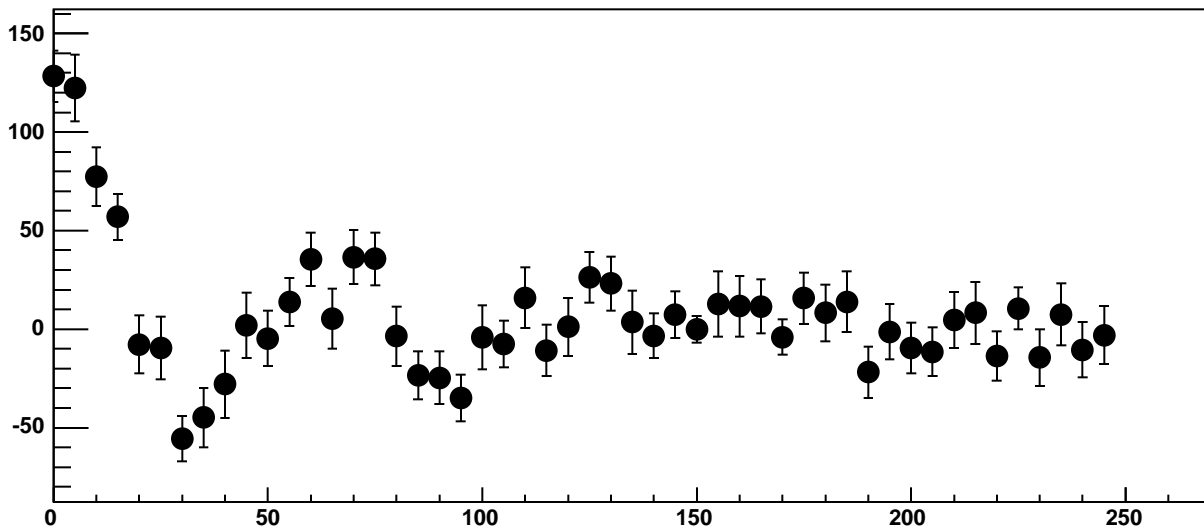


$\chi^2 / \text{ndf}$	121.5 / 41
p0	$-12.73 \pm 4.281$
p1	$93.19 \pm 0.829$
p2	$-1.7\text{e}+08 \pm 7.763\text{e}+06$
p3	$1.715\text{e}+07 \pm 6.979\text{e}+05$
p4	$8.887 \pm 0.1443$

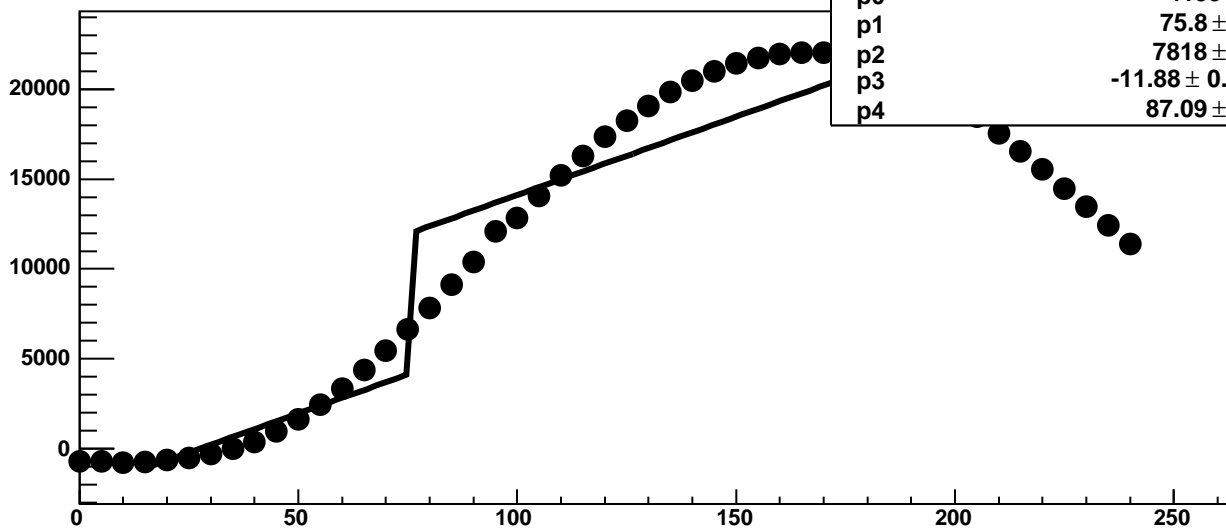
Chip 8, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold

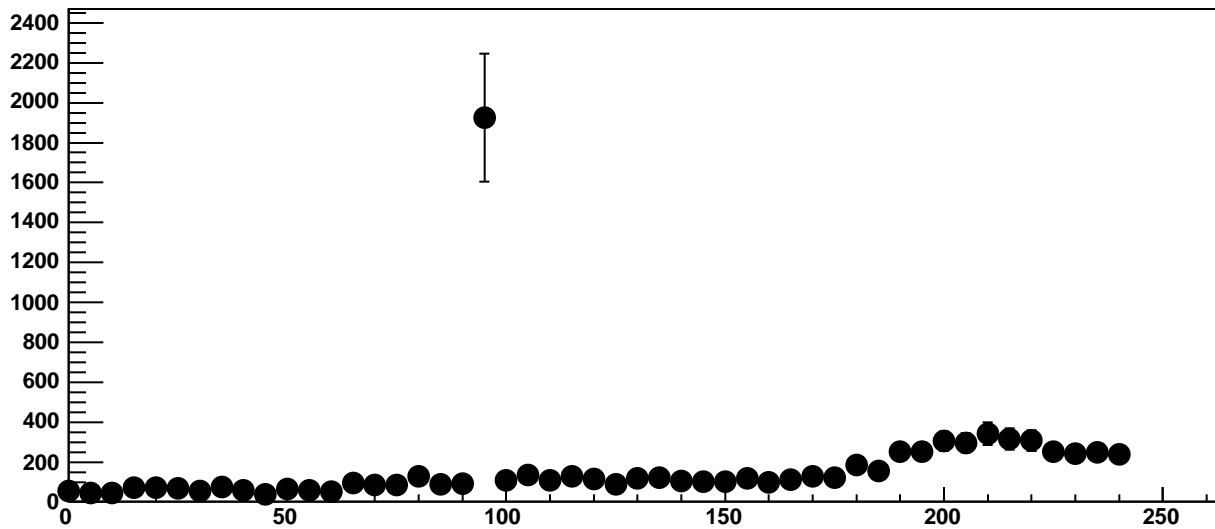


Chip 8, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

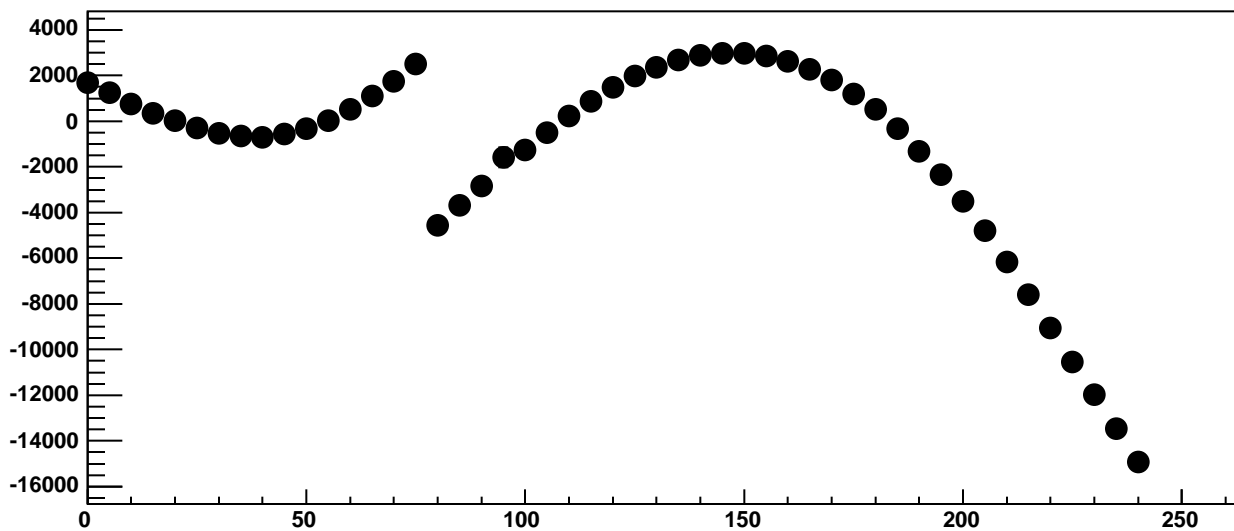


$\chi^2 / \text{ndf}$	4.885e+05 / 41
p0	4199 ± 0.0908
p1	75.8 ± 0.01313
p2	7818 ± 0.09502
p3	-11.88 ± 0.0003556
p4	87.09 ± 0.06272

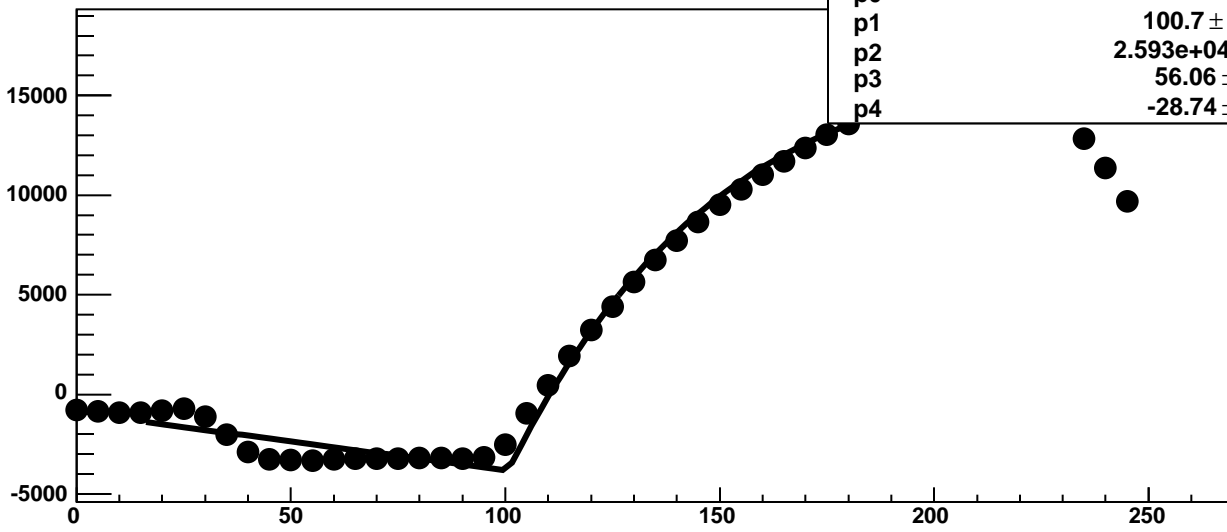
Chip 8, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



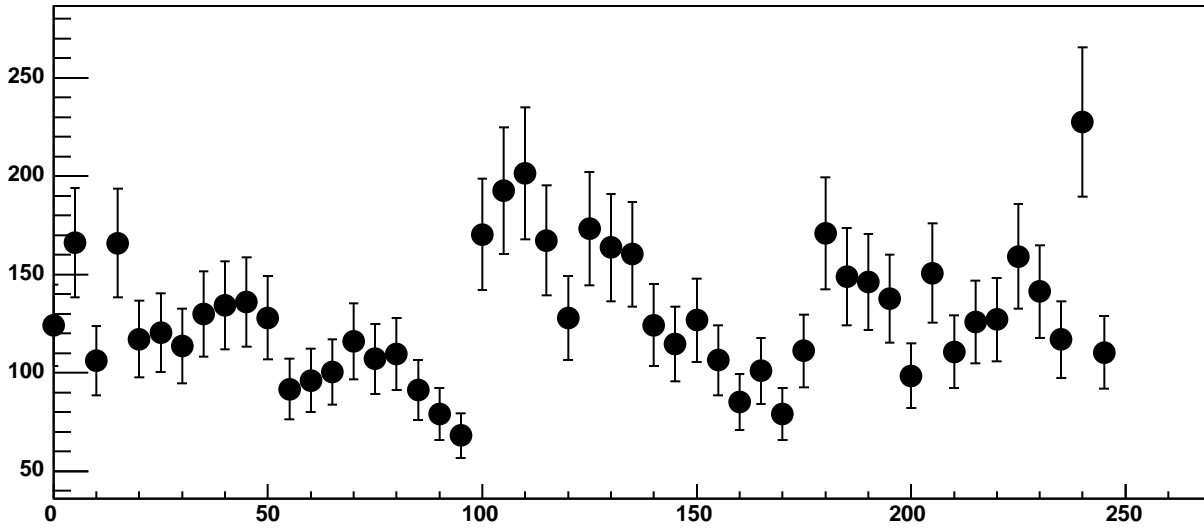
Chip 8, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold



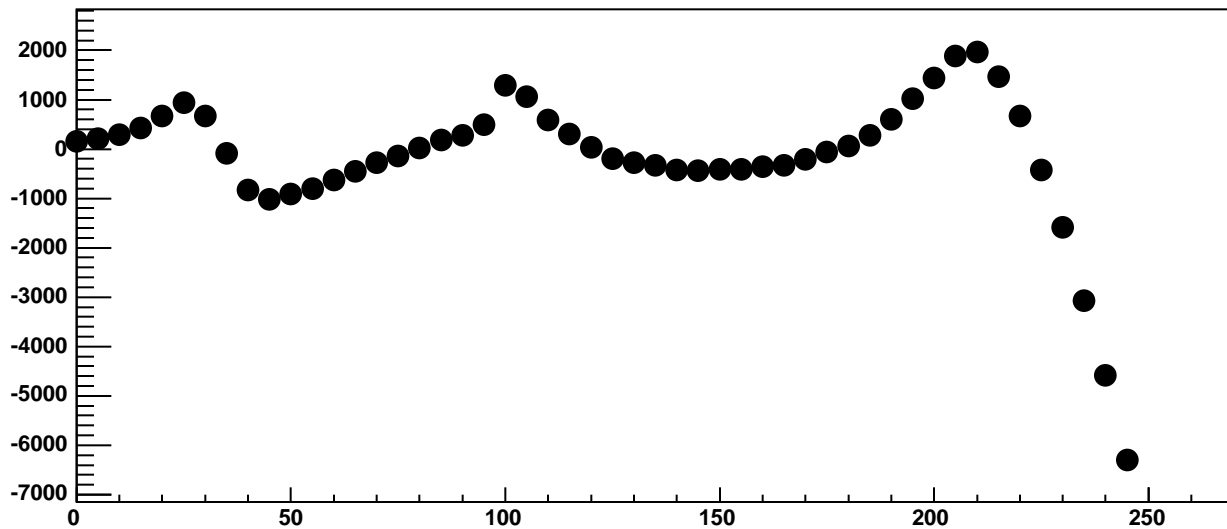
Chip 8, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold



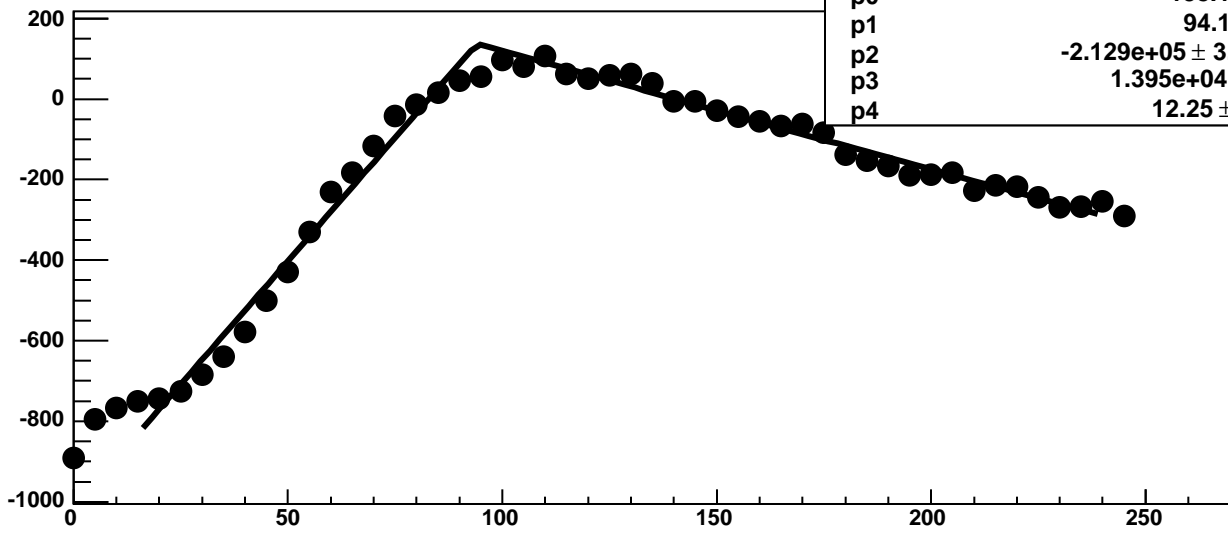
Chip 8, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



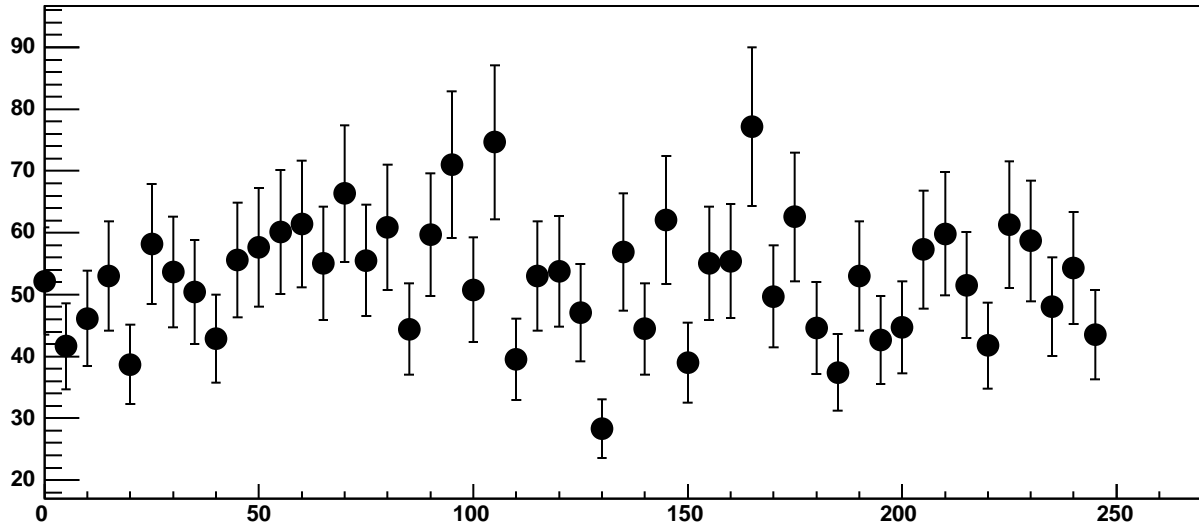
Chip 8, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



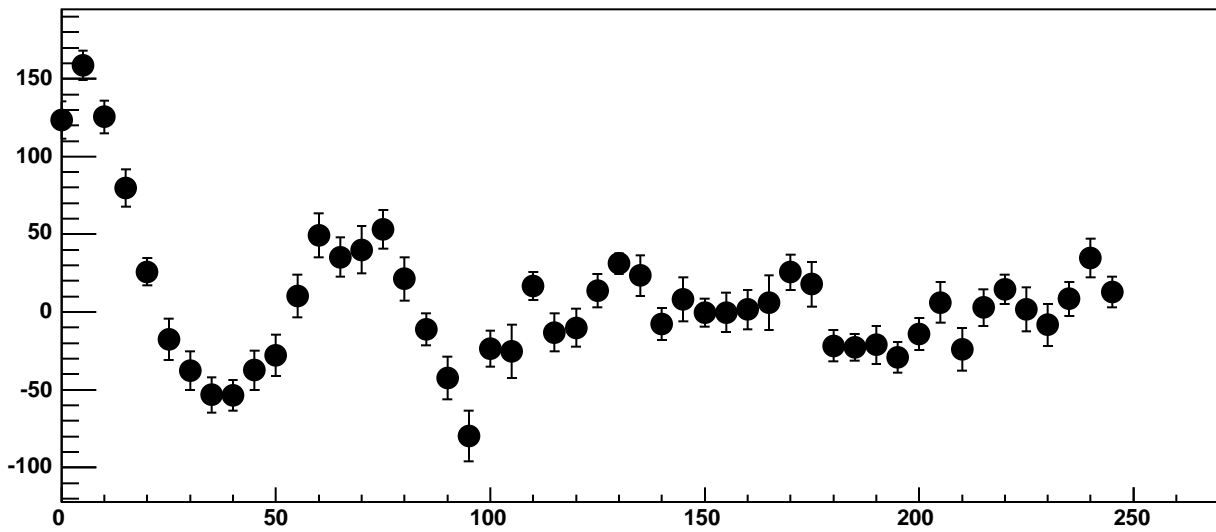
Chip 8, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 8, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

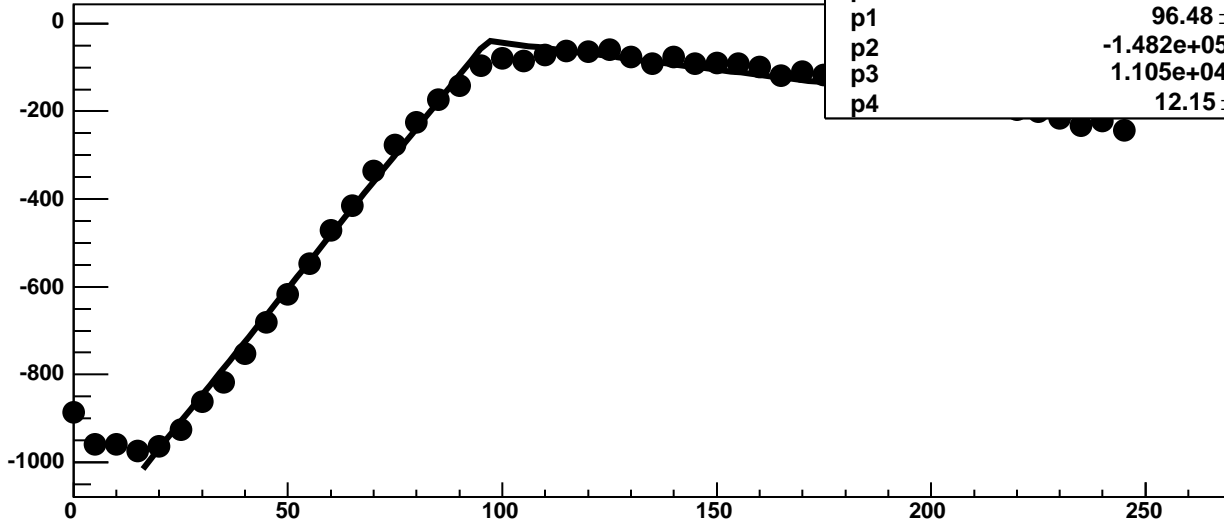


Chip 8, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold



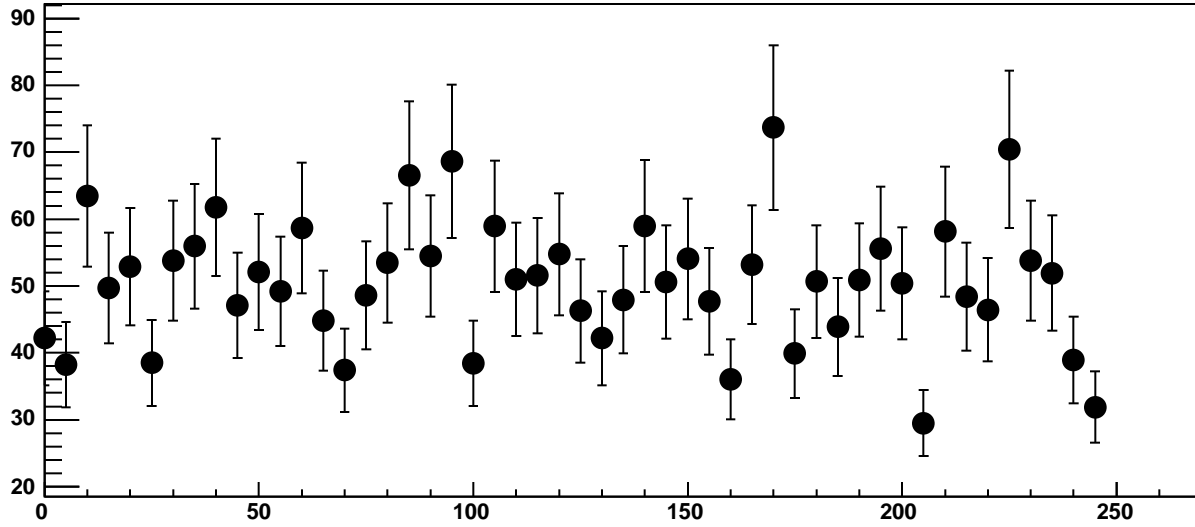


Chip 8, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

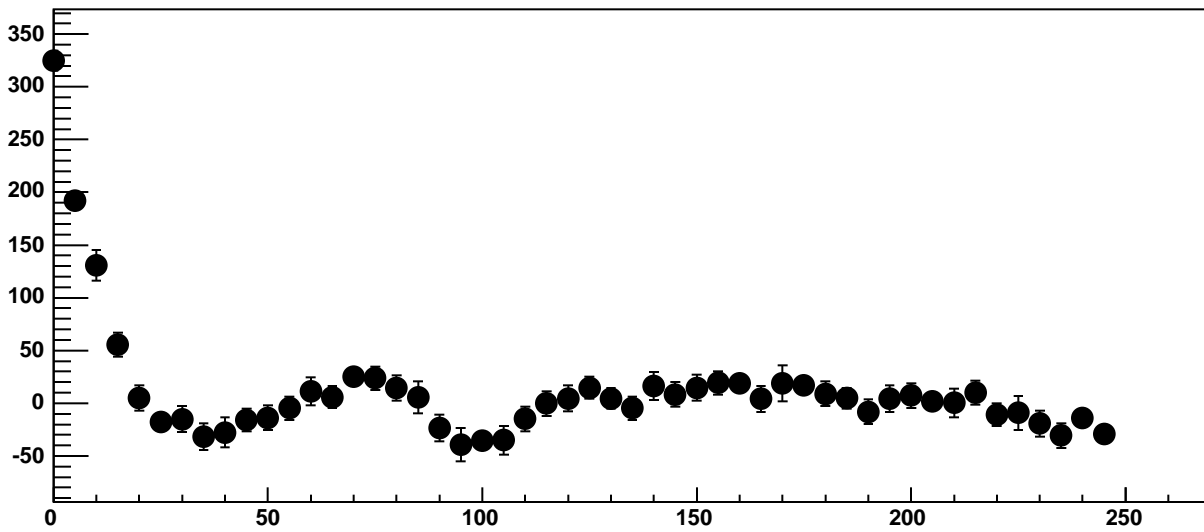


$\chi^2 / \text{ndf}$	126.8 / 41
p0	$-39.22 \pm 3.791$
p1	$96.48 \pm 0.5376$
p2	$-1.482e+05 \pm 1550$
p3	$1.105e+04 \pm 8.103$
p4	$12.15 \pm 0.1199$

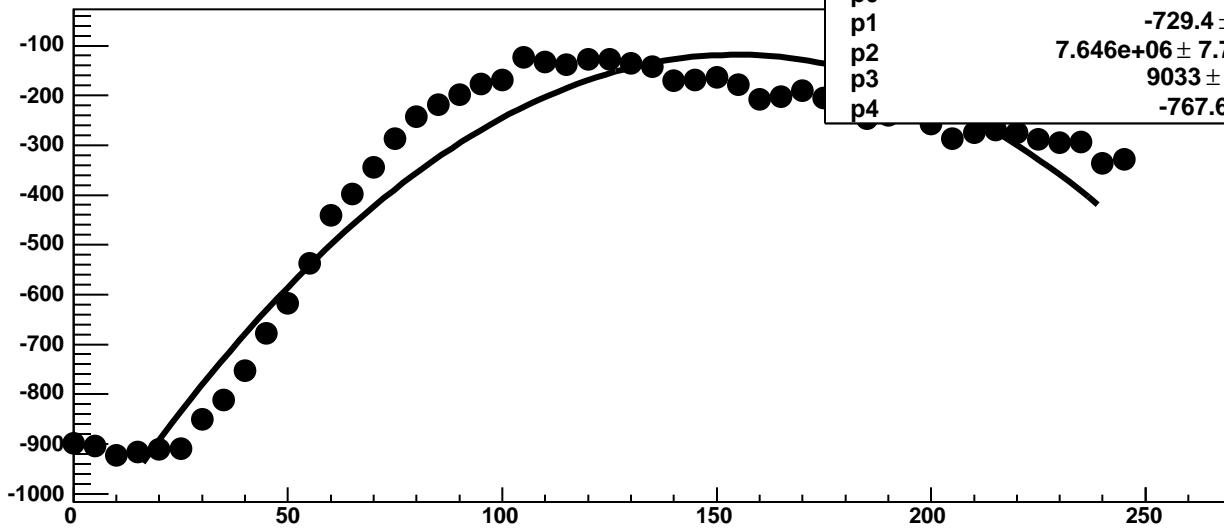
Chip 8, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

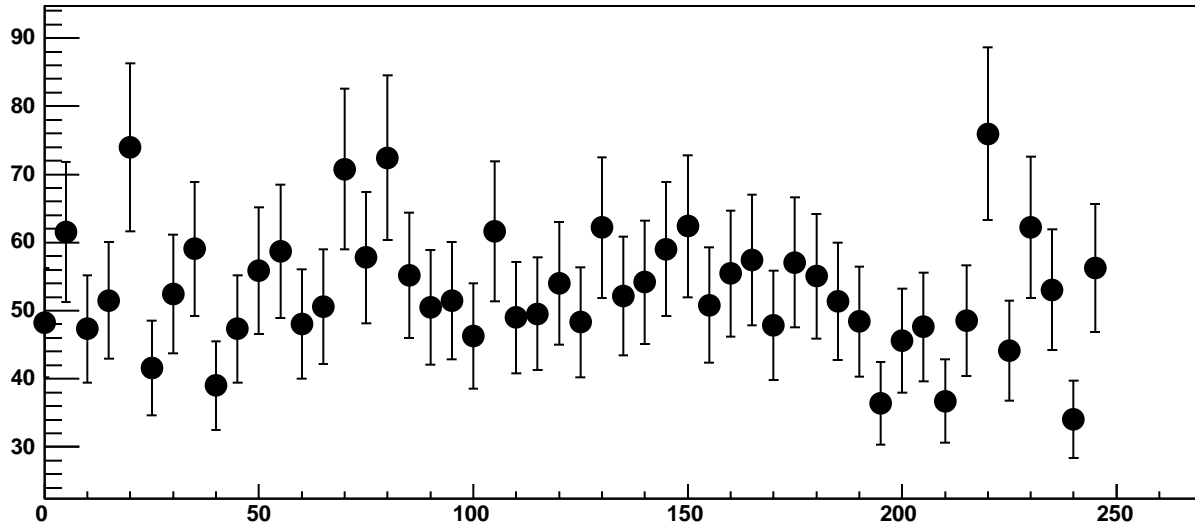


Chip 8, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

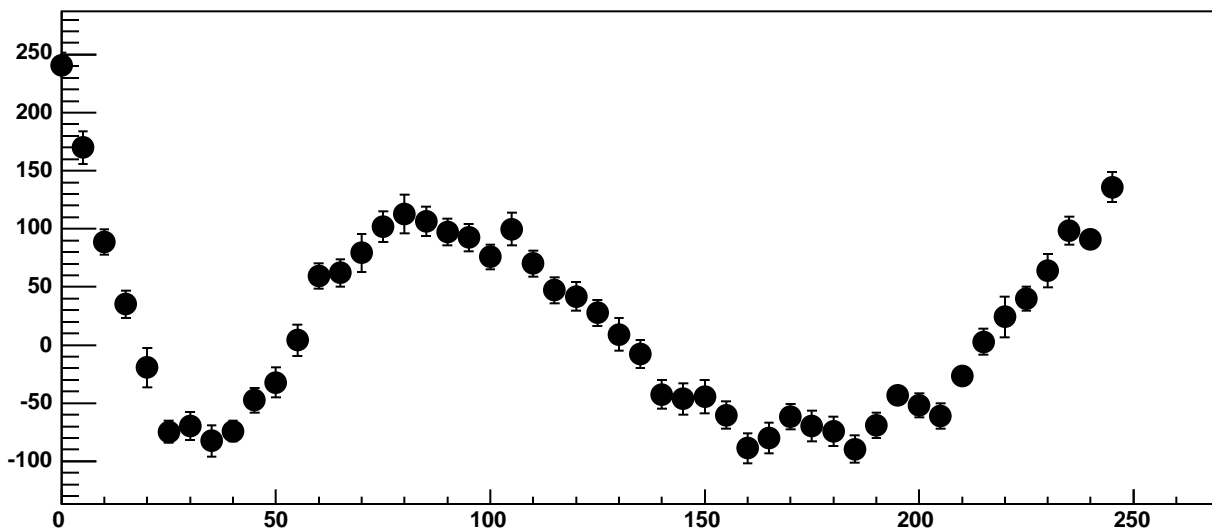


$\chi^2 / \text{ndf}$	1468 / 41
p0	$-3.443\text{e}+04 \pm 328.1$
p1	$-729.4 \pm 0.3016$
p2	$7.646\text{e}+06 \pm 7.775\text{e}+04$
p3	$9033 \pm 0.02562$
p4	$-767.6 \pm 7.826$

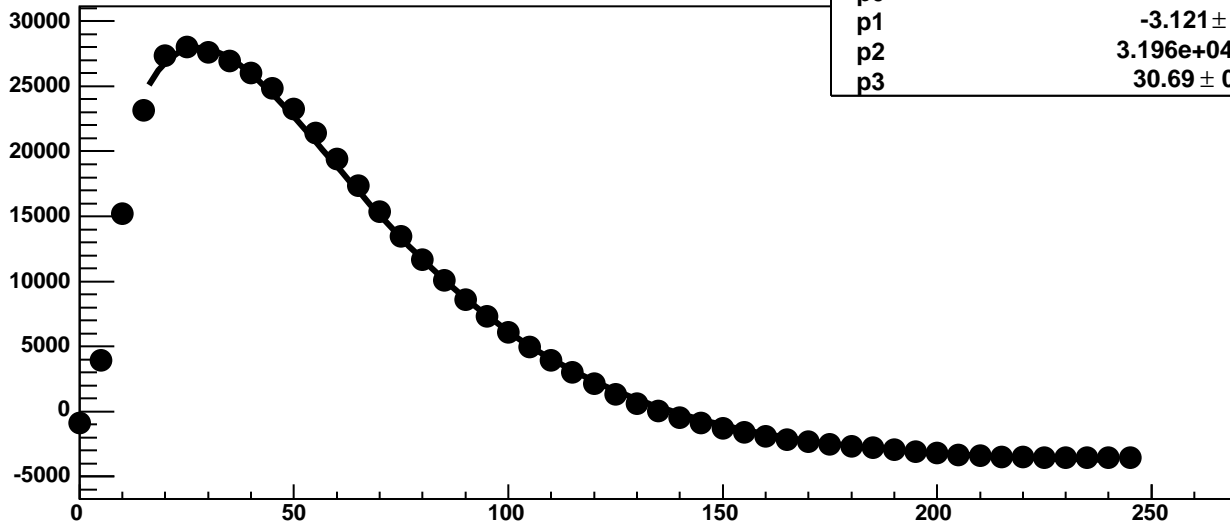
Chip 8, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

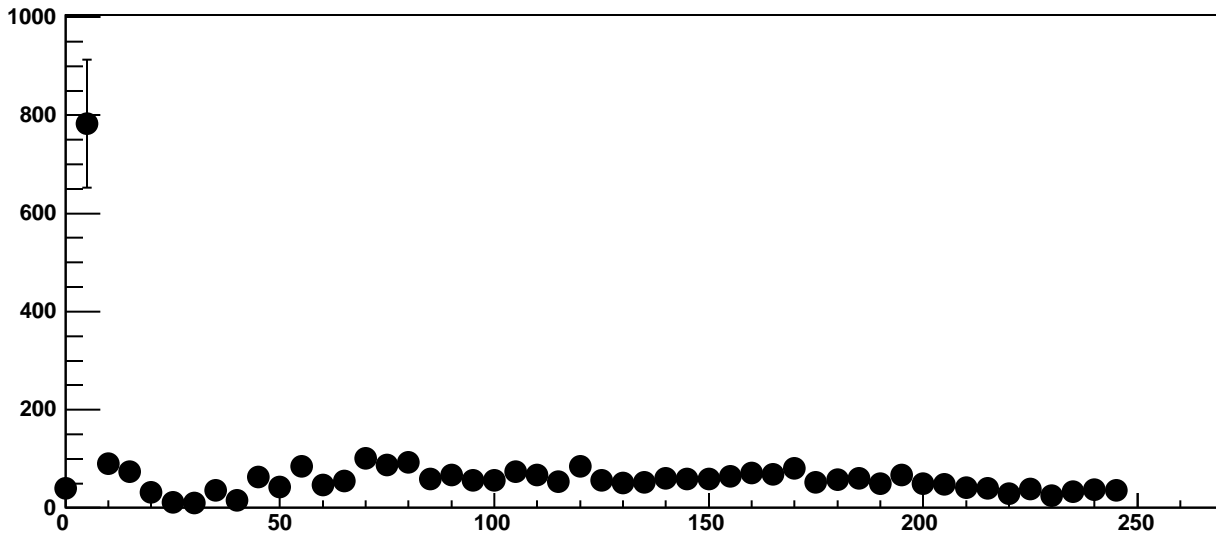


Chip 8, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

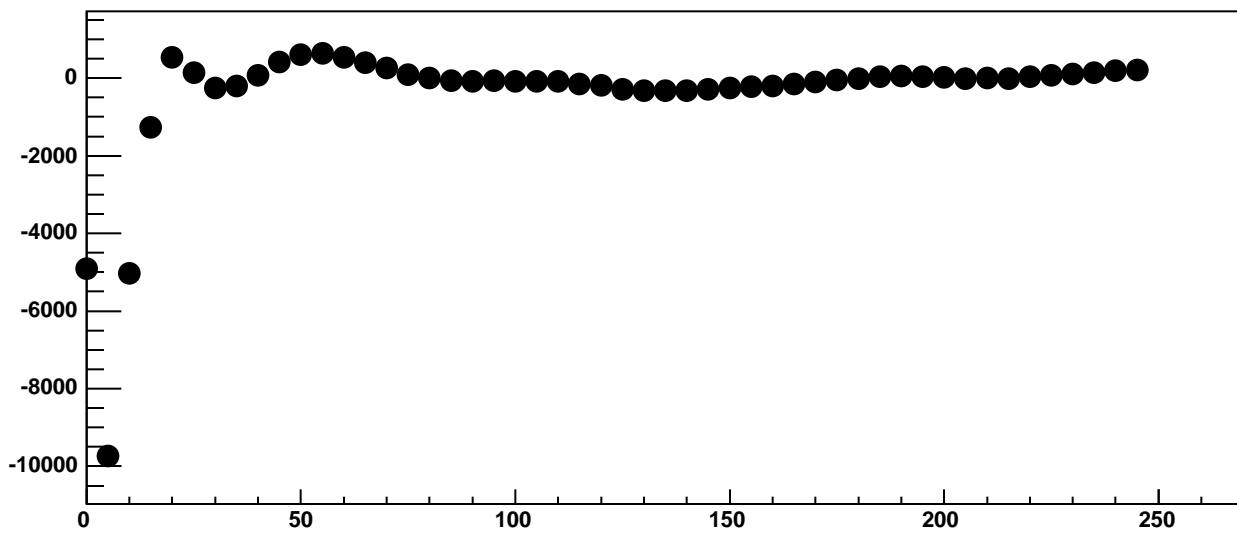


$\chi^2 / \text{ndf}$	4.122e+04 / 42
p0	-3992 ± 2.807
p1	-3.121 ± 0.01627
p2	3.196e+04 ± 3.079
p3	30.69 ± 0.009812

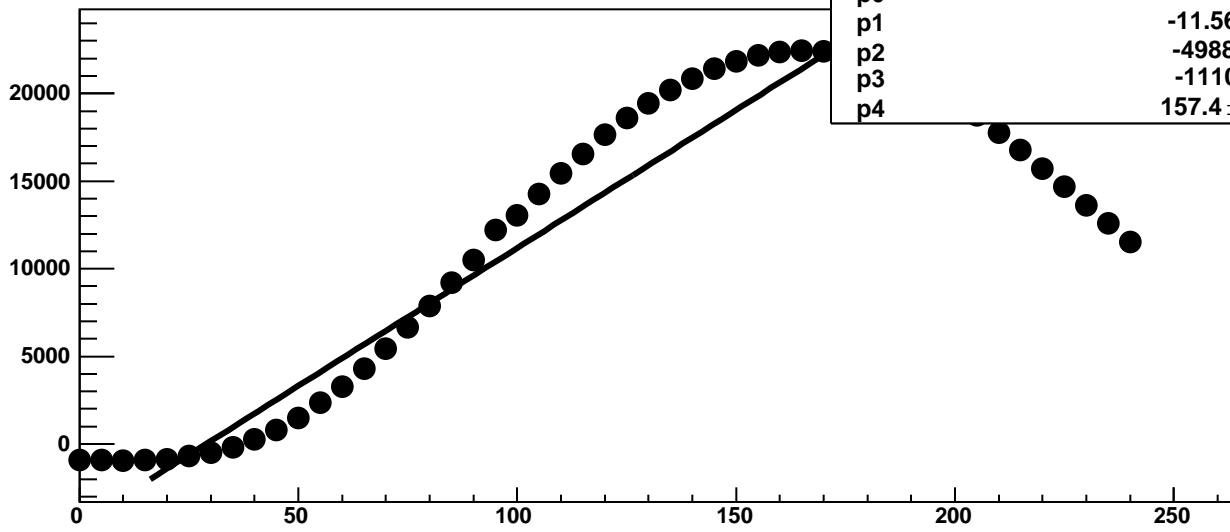
Chip 8, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

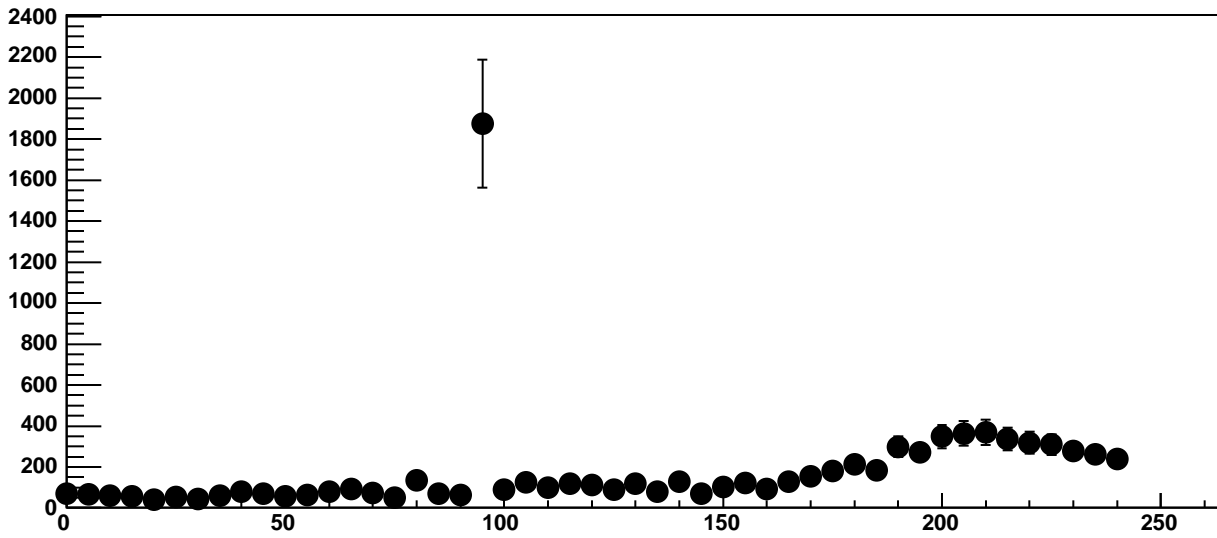


Chip 8, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

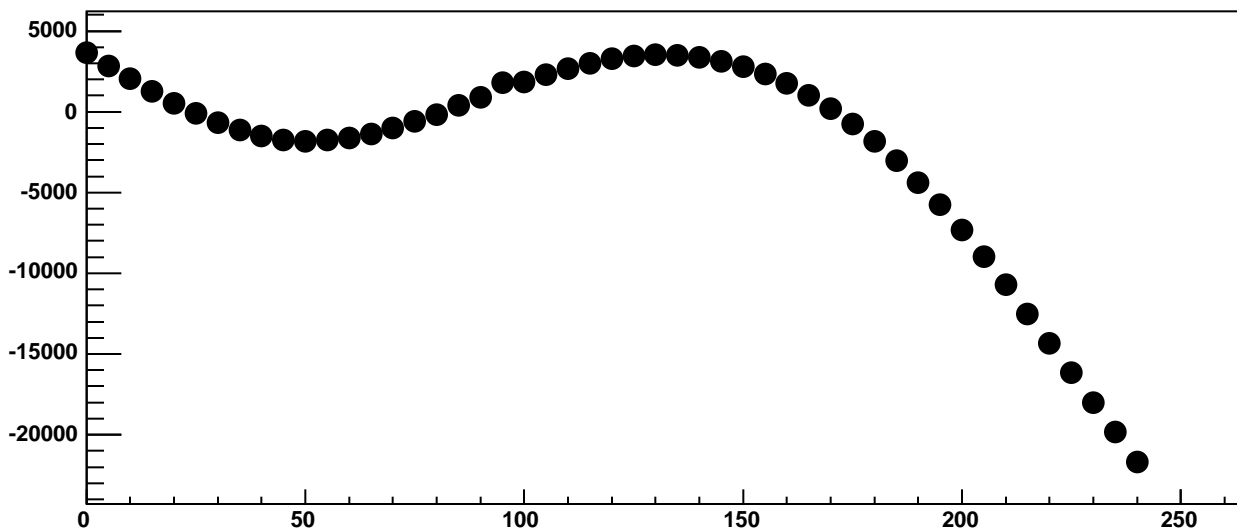


$\chi^2 / \text{ndf}$	8.367e+05 / 41
p0	-1388 ± 16.67
p1	-11.56 ± 0.101
p2	-4988 ± 19.45
p3	-1110 ± 21.55
p4	157.4 ± 0.1129

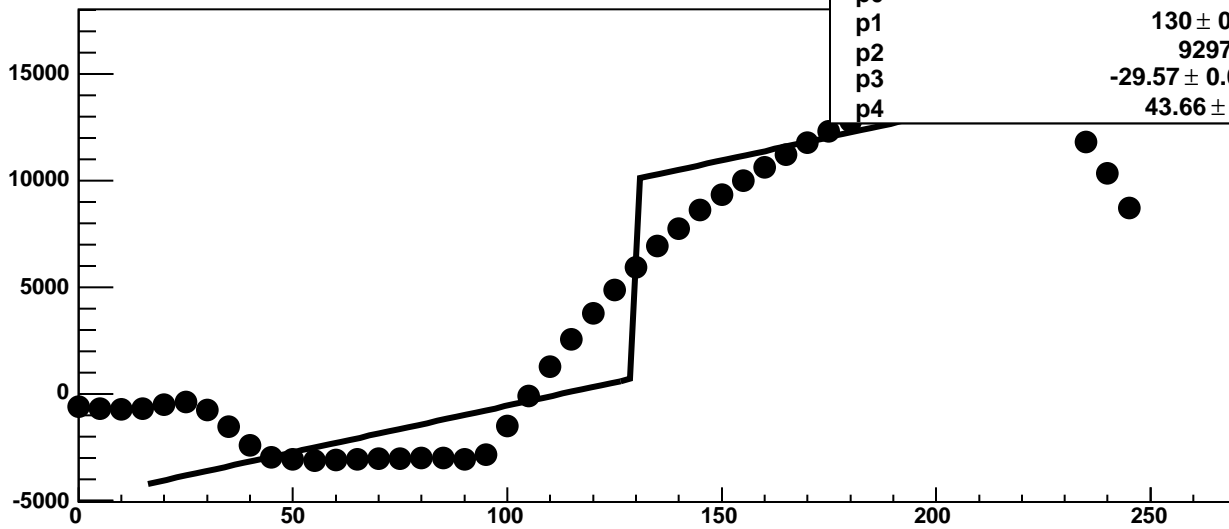
Chip 8, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



Chip 8, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

2.328e+05 / 41

p0

773.3 ± 2.888

p1

130 ± 0.003863

p2

9297 ± 7.425

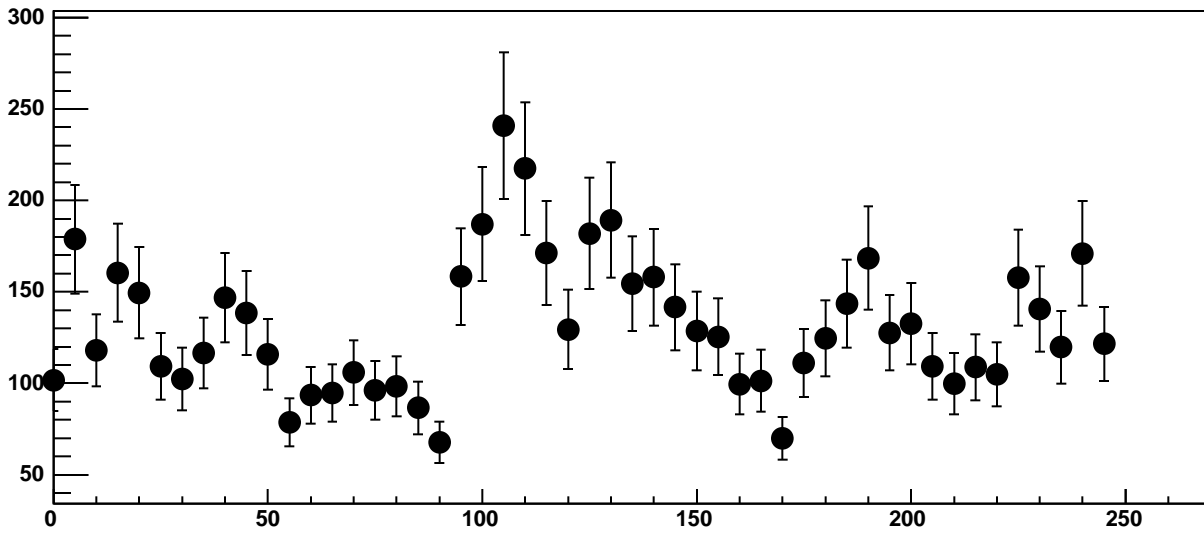
p3

-29.57 ± 0.0007566

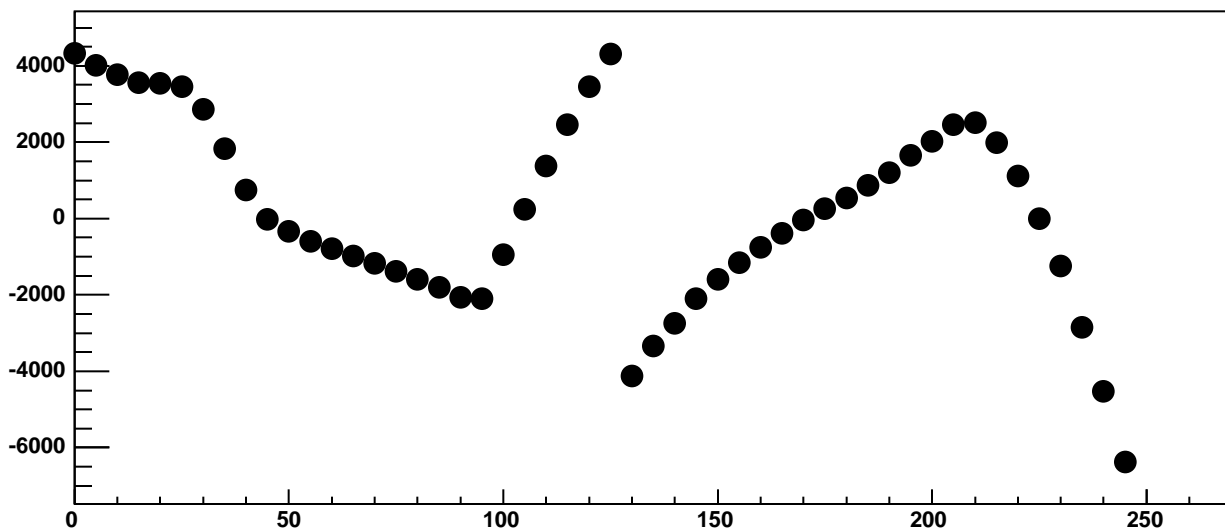
p4

43.66 ± 0.05083

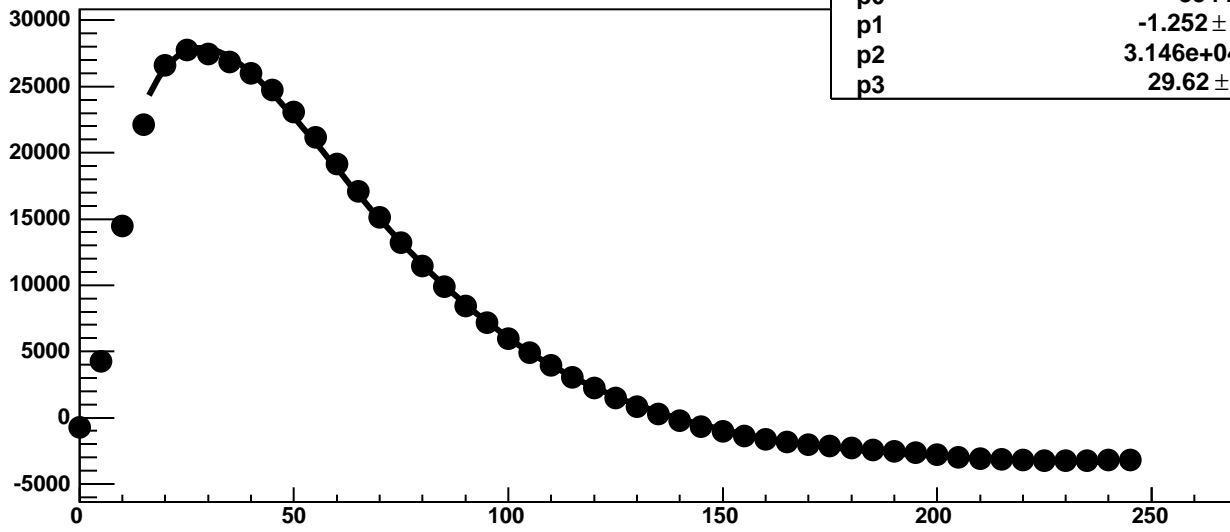
Chip 8, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

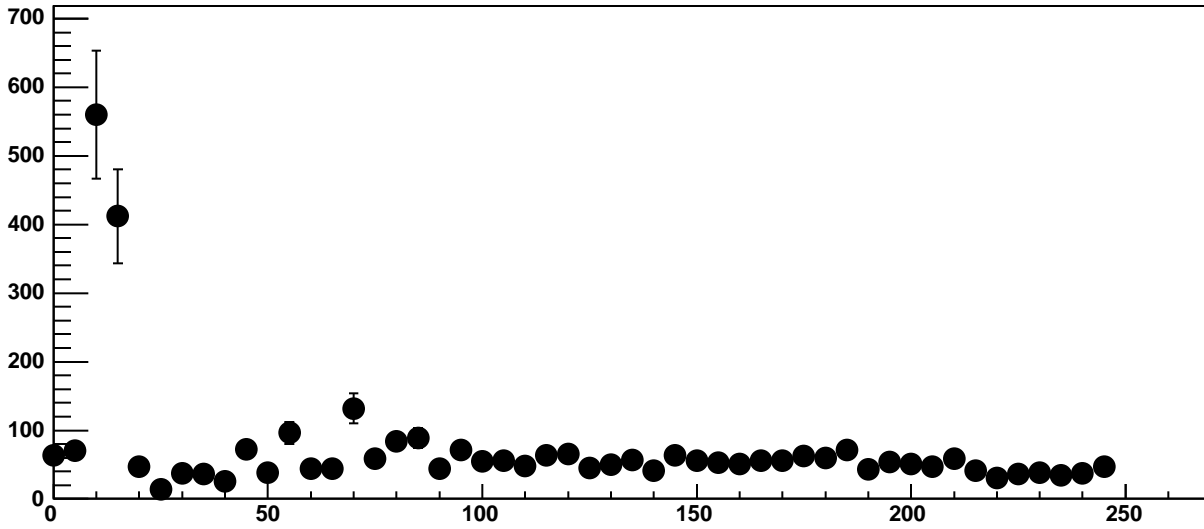


Chip 8, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold

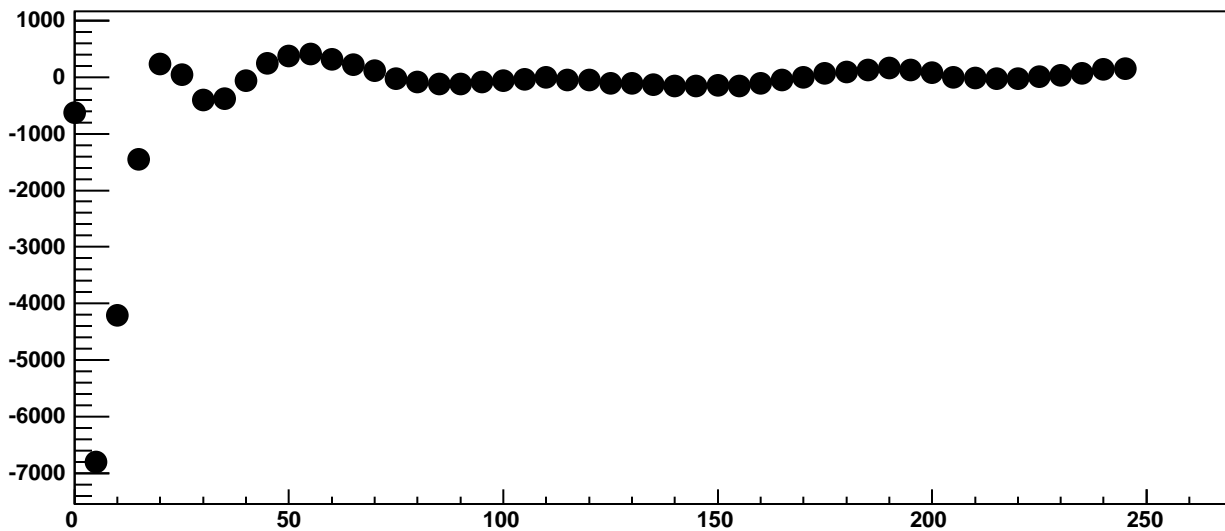


$\chi^2 / \text{ndf}$	1.145e+04 / 42
p0	-3544 ± 2.995
p1	-1.252 ± 0.02058
p2	3.146e+04 ± 3.58
p3	29.62 ± 0.01103

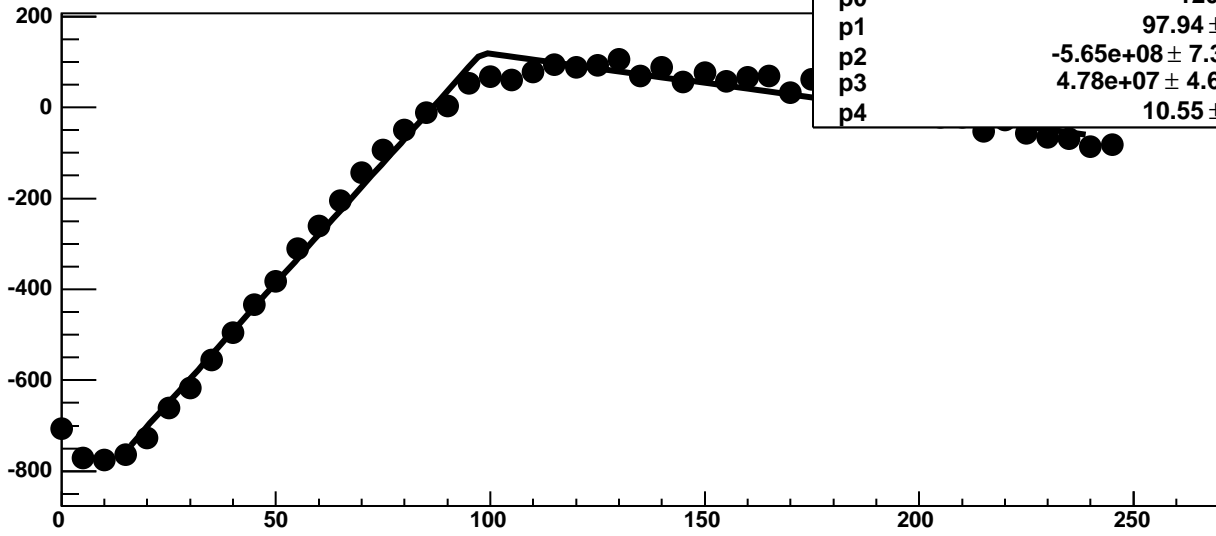
Chip 8, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

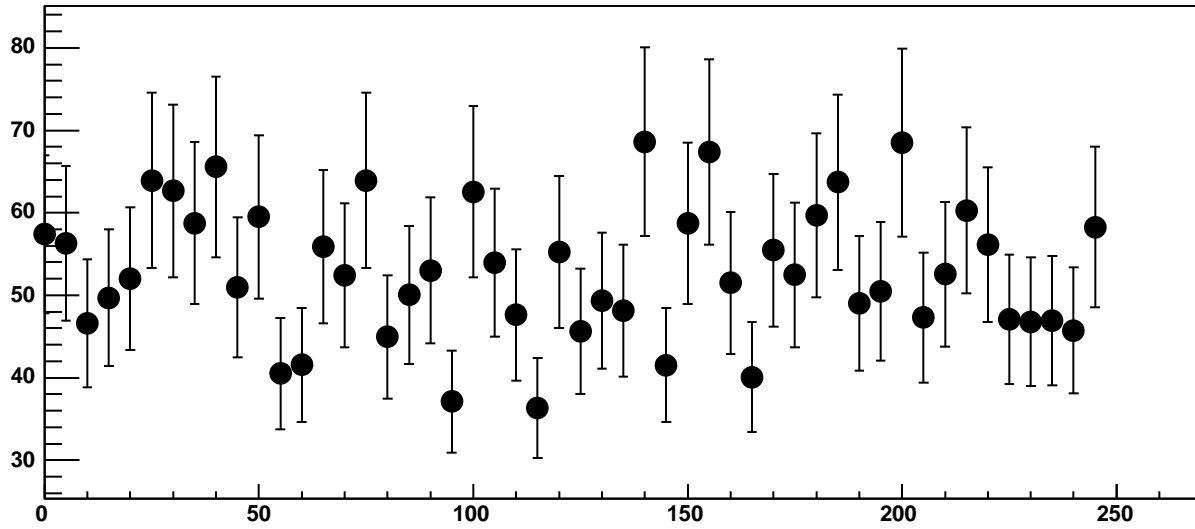


Chip 8, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

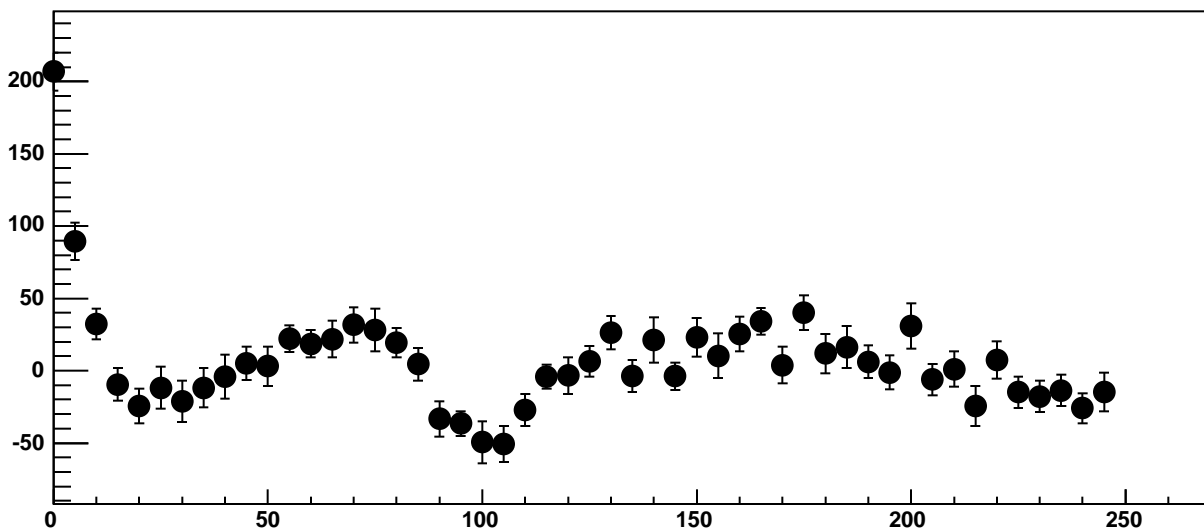


$\chi^2 / \text{ndf}$	159.8 / 41
p0	$120 \pm 3.771$
p1	$97.94 \pm 0.5698$
p2	$-5.65\text{e}+08 \pm 7.365\text{e}+06$
p3	$4.78\text{e}+07 \pm 4.617\text{e}+05$
p4	$10.55 \pm 0.1126$

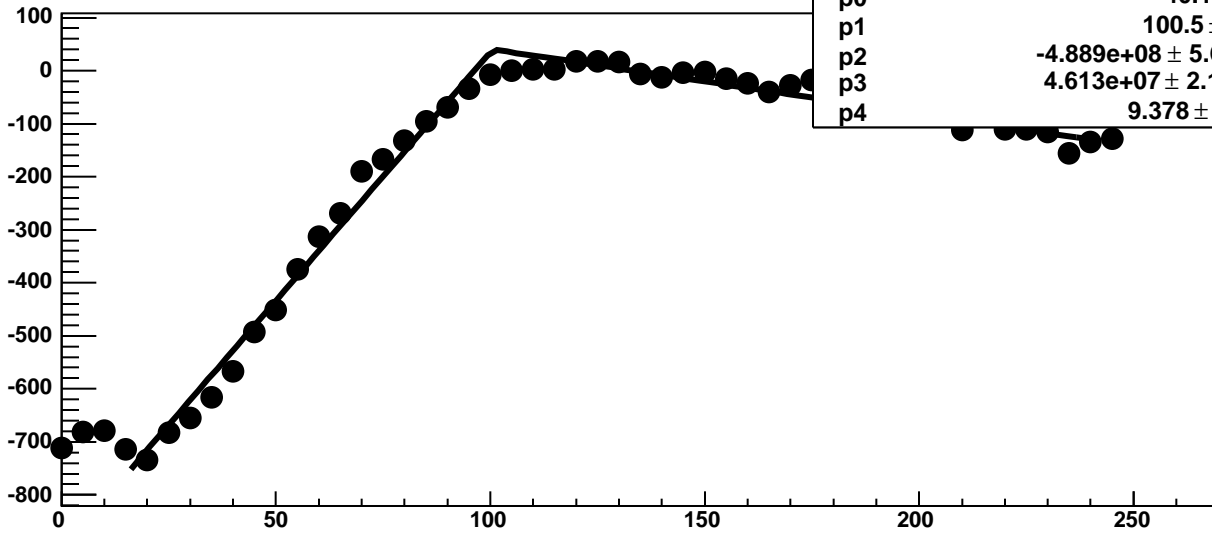
Chip 8, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

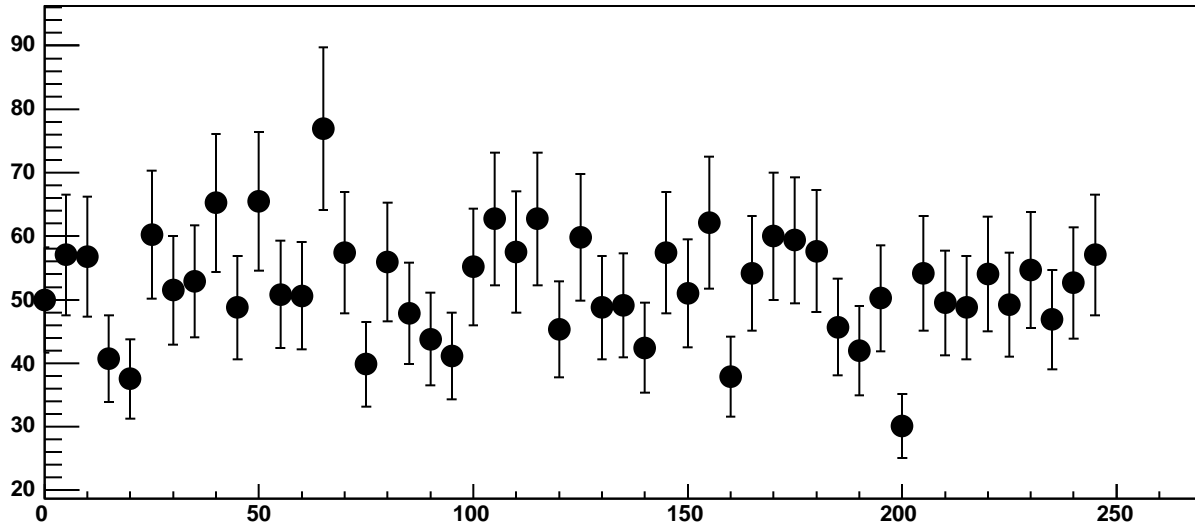


Chip 8, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

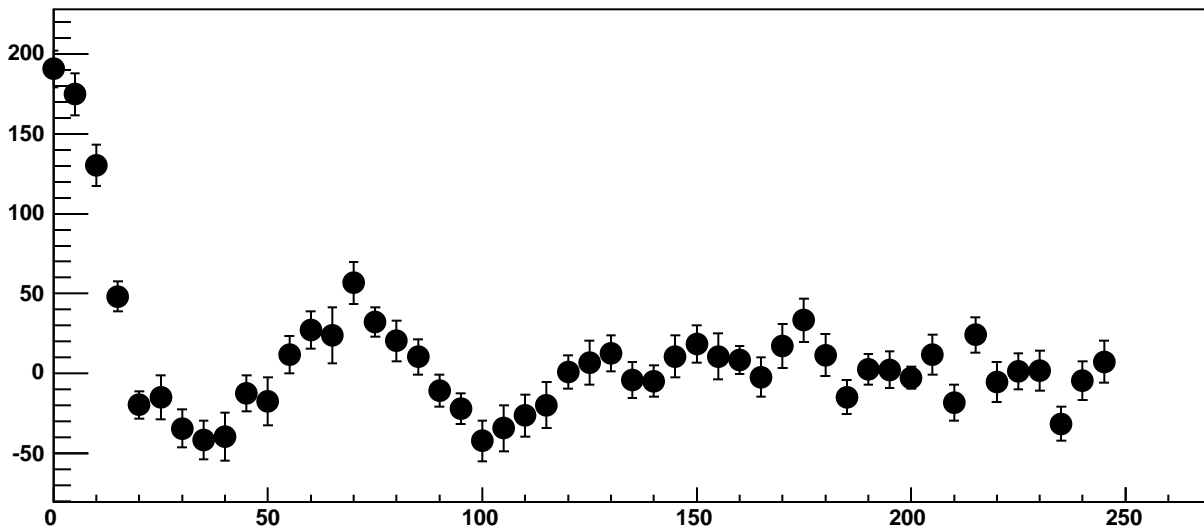


$\chi^2 / \text{ndf}$	168.7 / 41
p0	$40.18 \pm 4.21$
p1	$100.5 \pm 0.6447$
p2	$-4.889\text{e}+08 \pm 5.643\text{e}+06$
p3	$4.613\text{e}+07 \pm 2.171\text{e}+05$
p4	$9.378 \pm 0.09593$

Chip 8, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

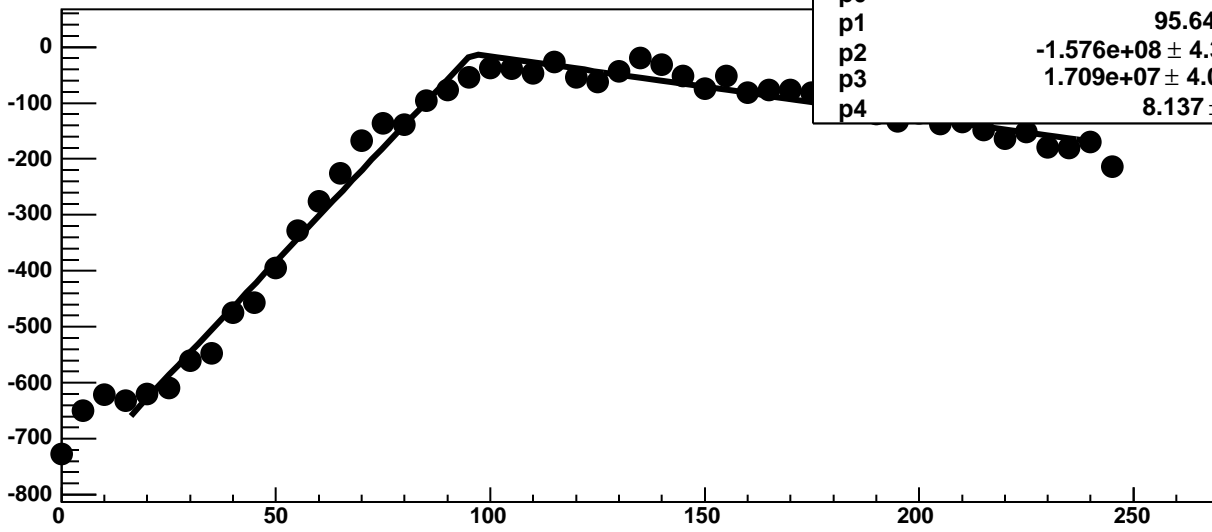


Chip 8, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold



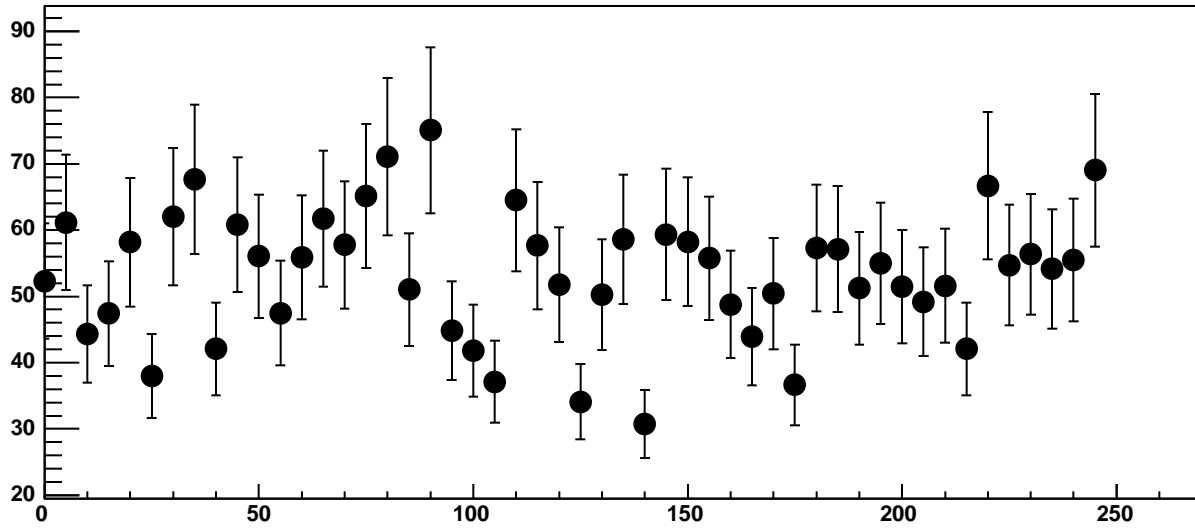


Chip 8, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold

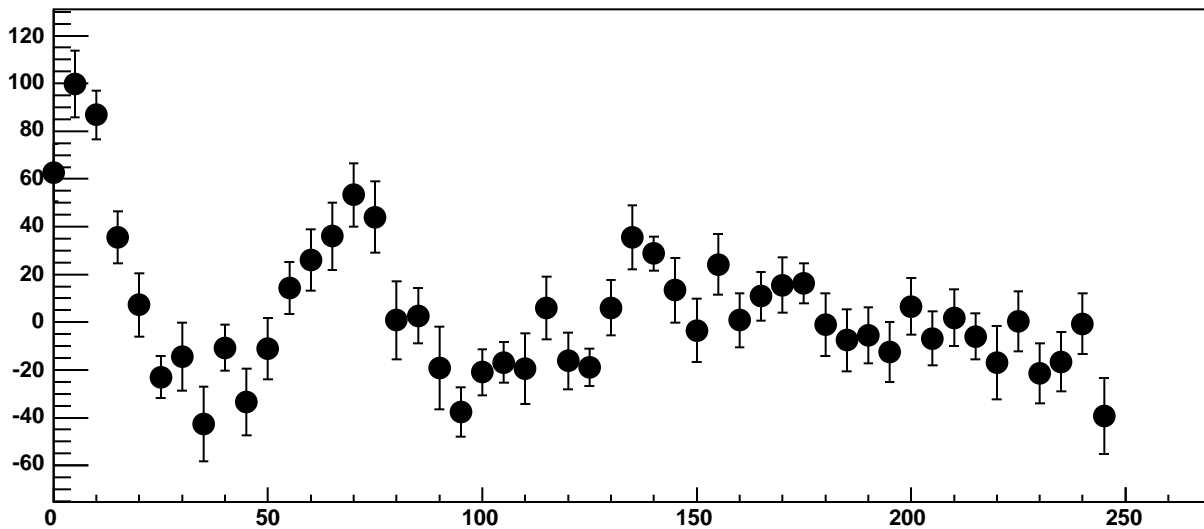


$\chi^2 / \text{ndf}$	148.3 / 41
p0	$-11.79 \pm 3.596$
p1	$95.64 \pm 0.778$
p2	$-1.576\text{e}+08 \pm 4.353\text{e}+06$
p3	$1.709\text{e}+07 \pm 4.077\text{e}+05$
p4	$8.137 \pm 0.1186$

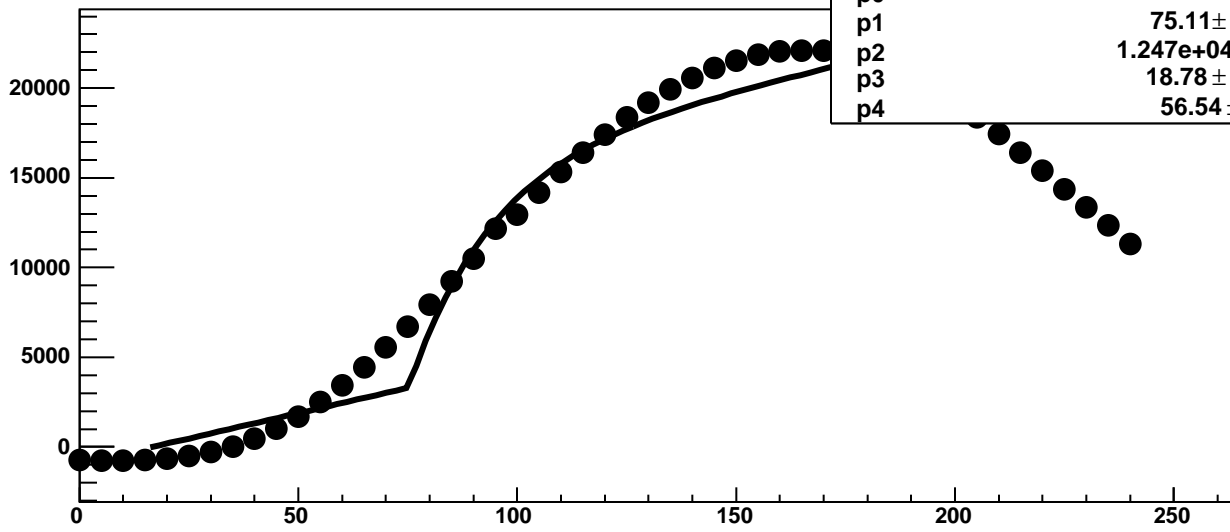
Chip 8, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold

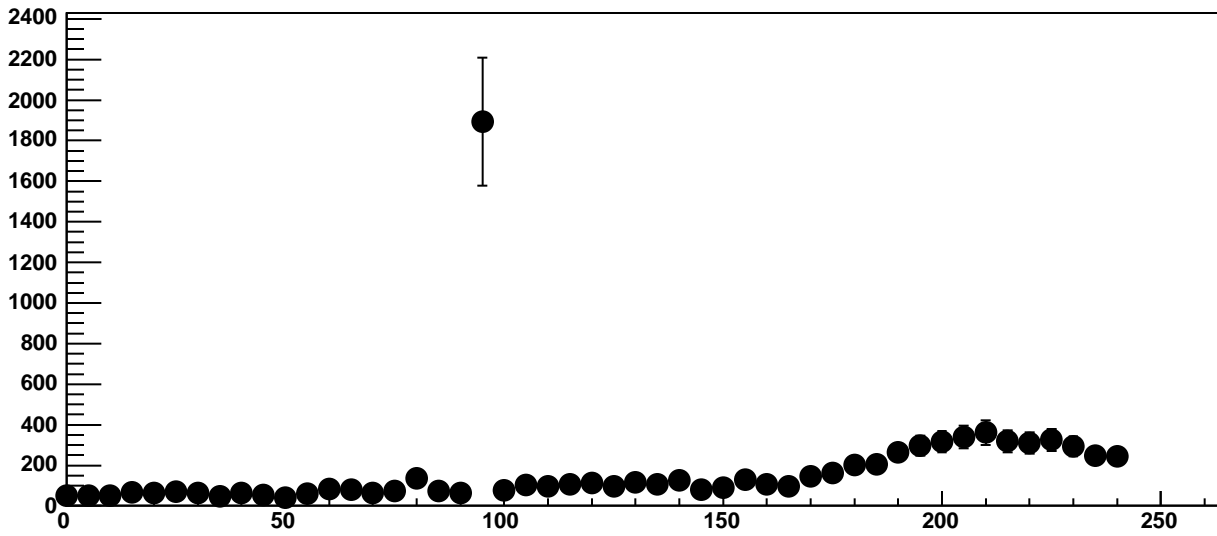


Chip 8, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

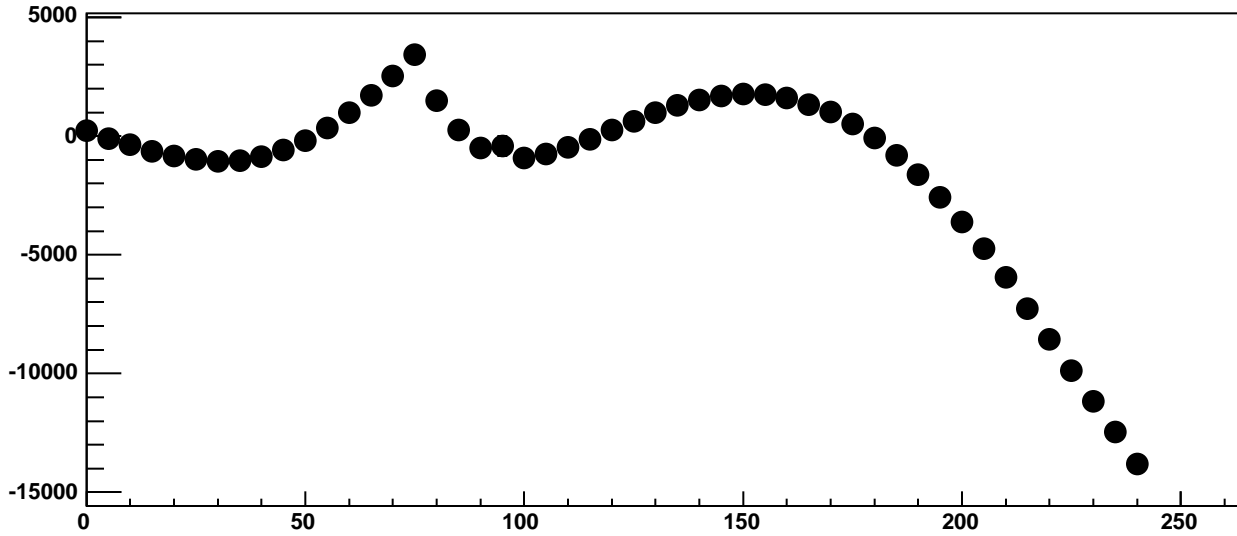


$\chi^2 / \text{ndf}$	3.461e+05 / 41
p0	3305 ± 7.668
p1	75.11 ± 0.04446
p2	1.247e+04 ± 22.77
p3	18.78 ± 0.06442
p4	56.54 ± 0.1753

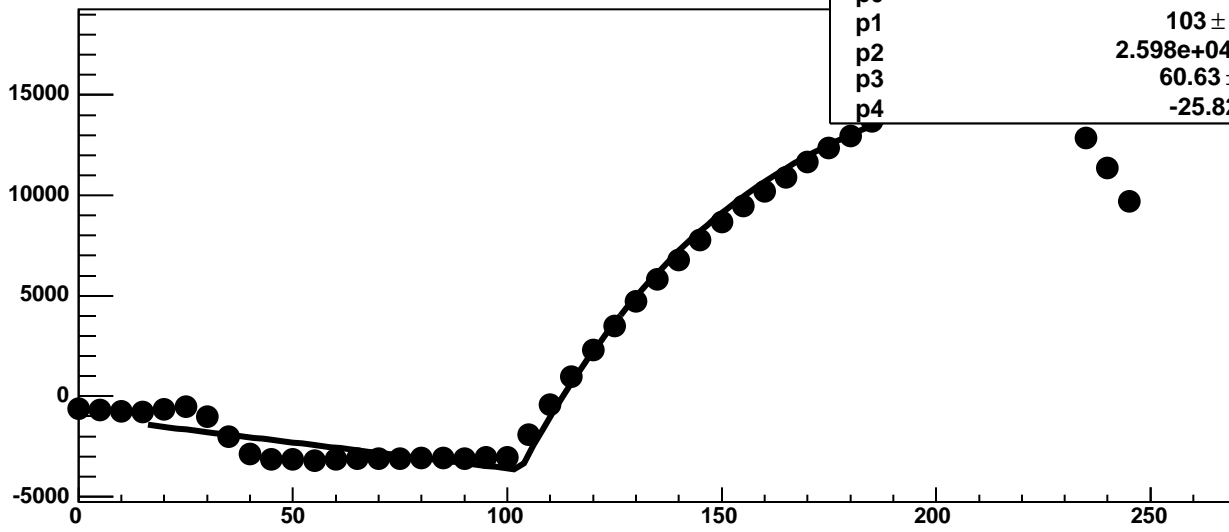
Chip 8, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



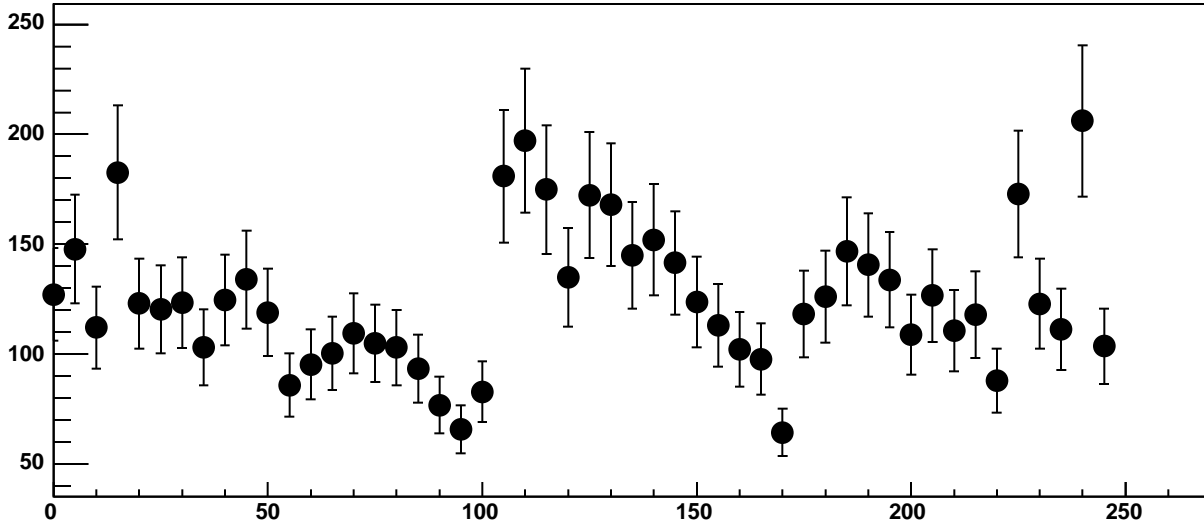
Chip 8, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold



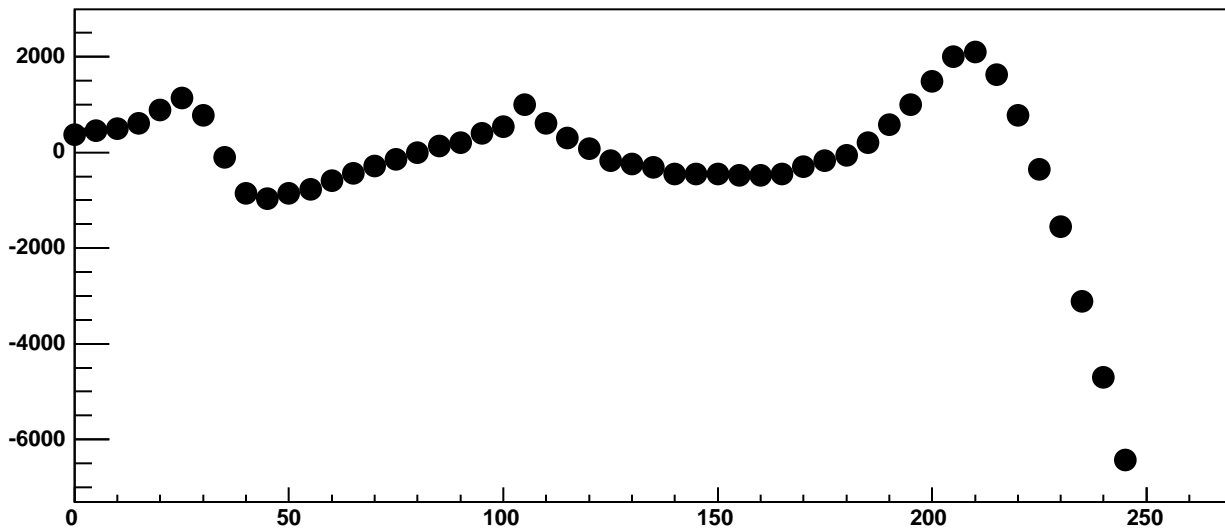
Chip 8, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold



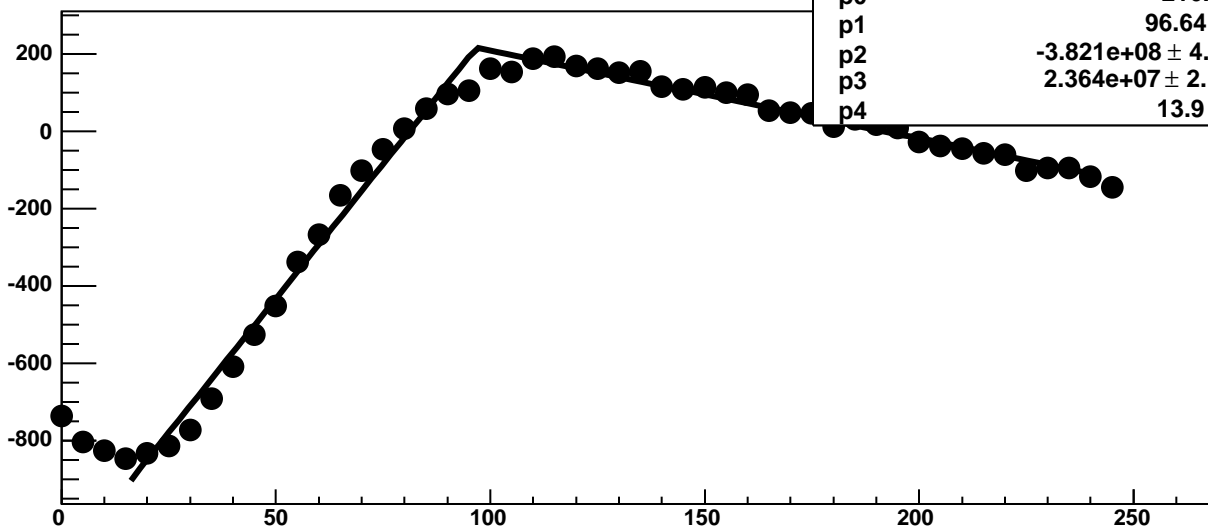
Chip 8, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

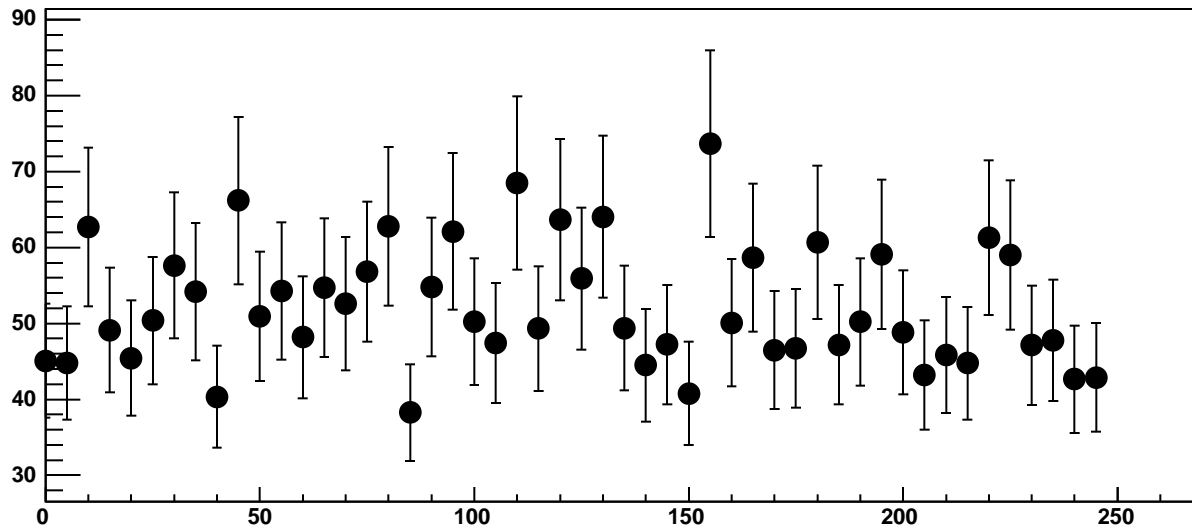


Chip 8, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

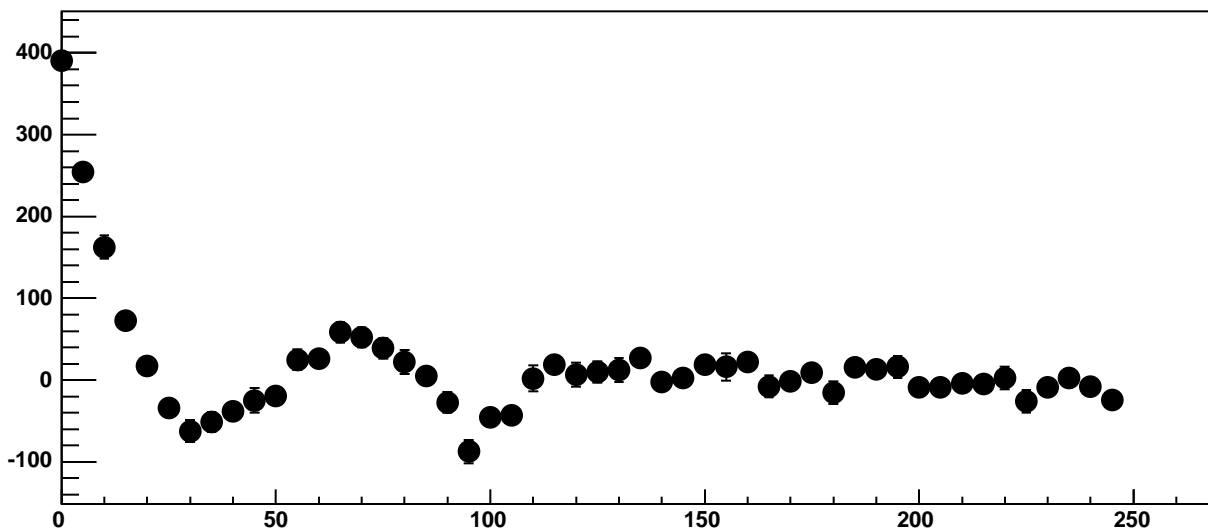


$\chi^2 / \text{ndf}$	283.3 / 41
p0	$216.4 \pm 3.93$
p1	$96.64 \pm 0.4491$
p2	$-3.821\text{e}+08 \pm 4.525\text{e}+06$
p3	$2.364\text{e}+07 \pm 2.109\text{e}+05$
p4	$13.9 \pm 0.1156$

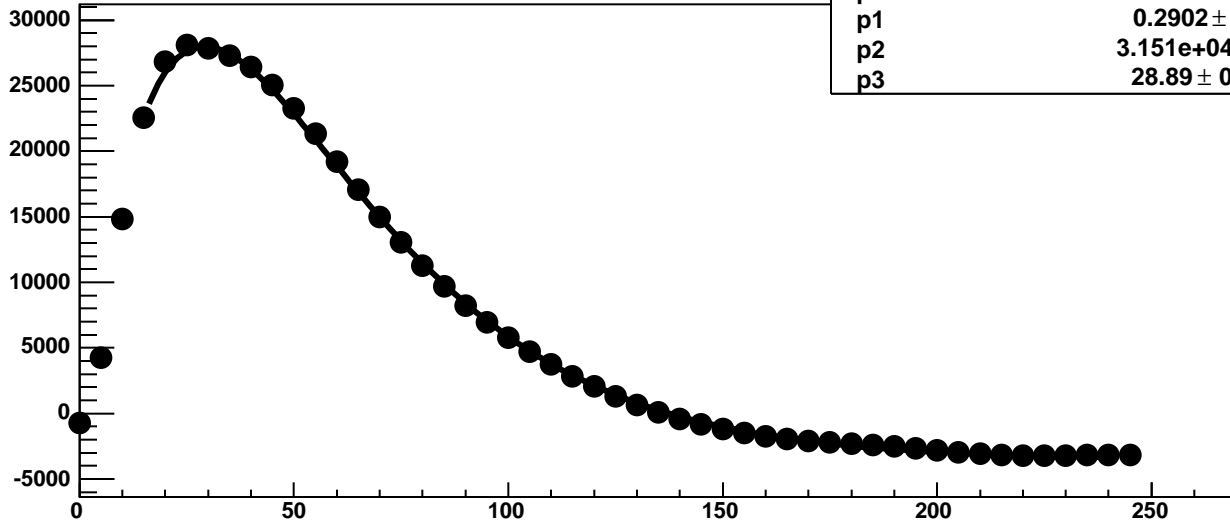
Chip 8, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

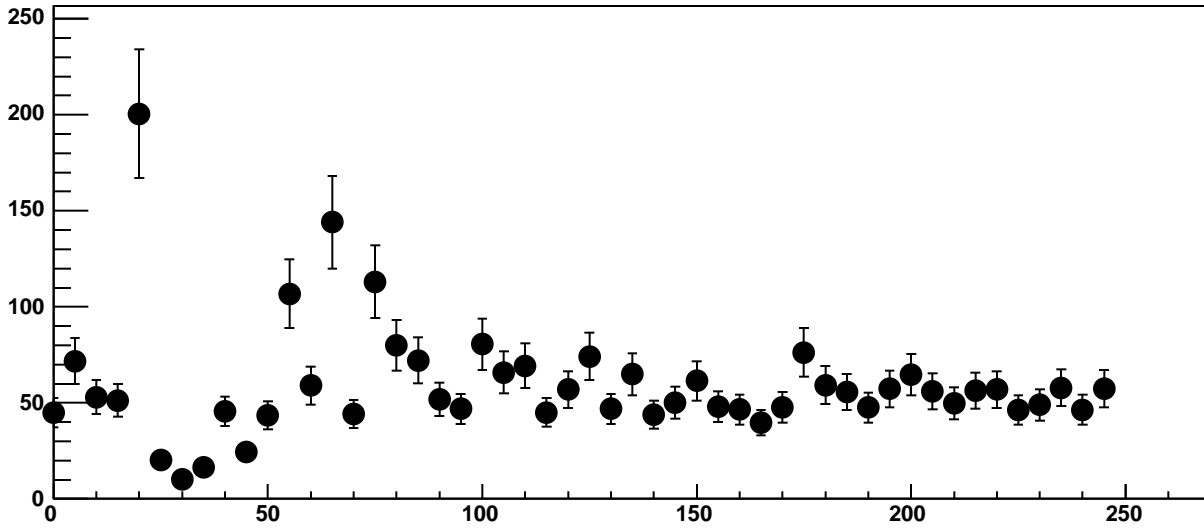


Chip 8, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold

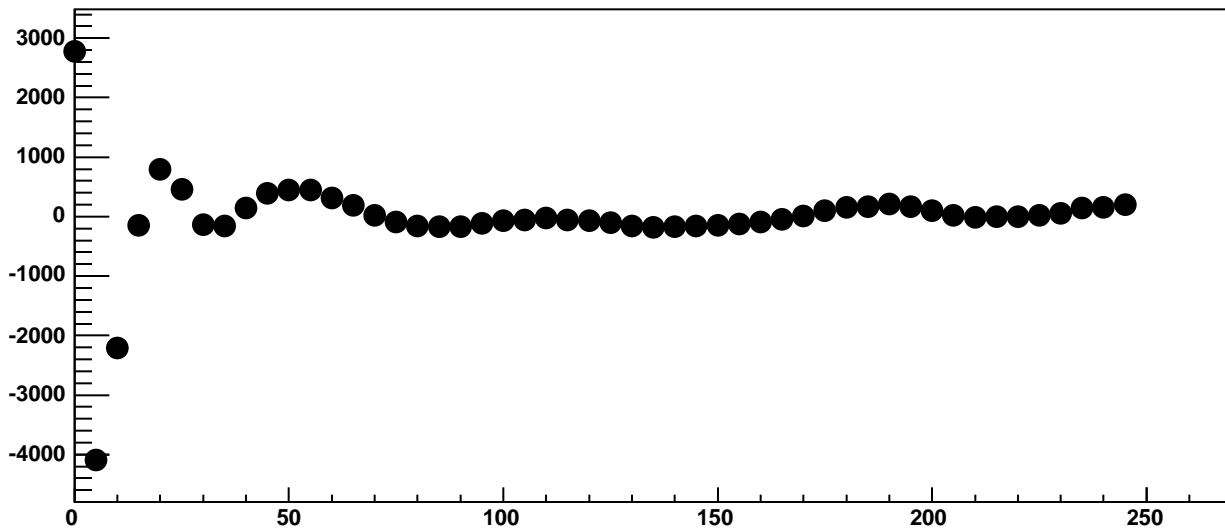


$\chi^2 / \text{ndf}$	2.589e+04 / 42
p0	-3518 ± 3.341
p1	0.2902 ± 0.01404
p2	3.151e+04 ± 3.605
p3	28.89 ± 0.008987

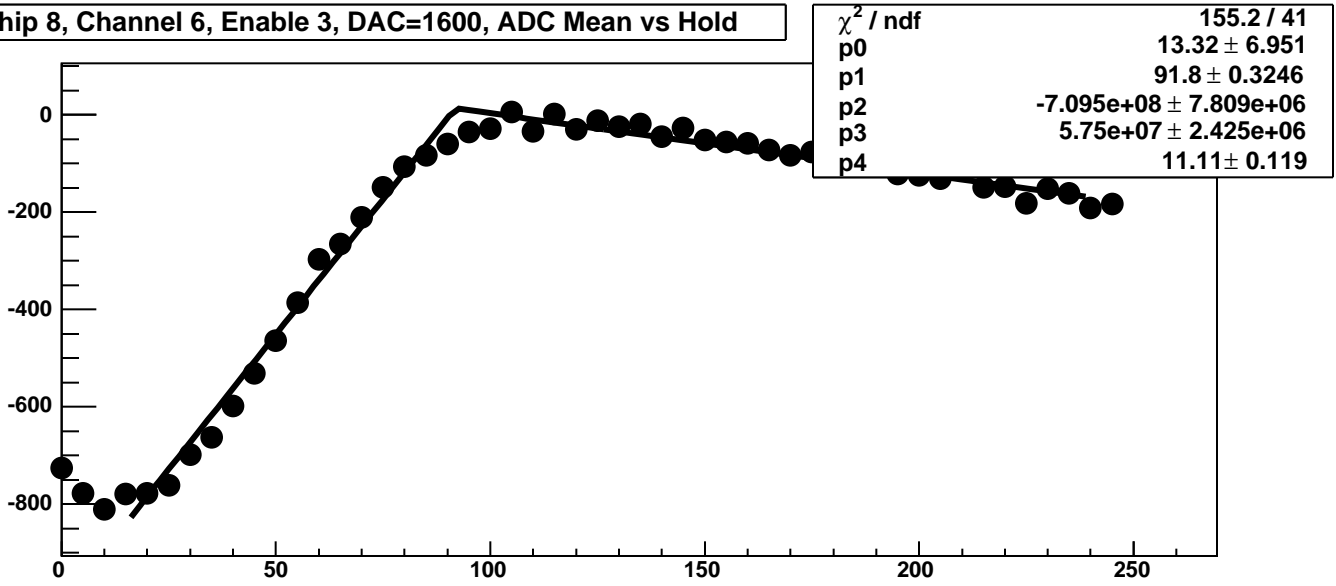
Chip 8, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



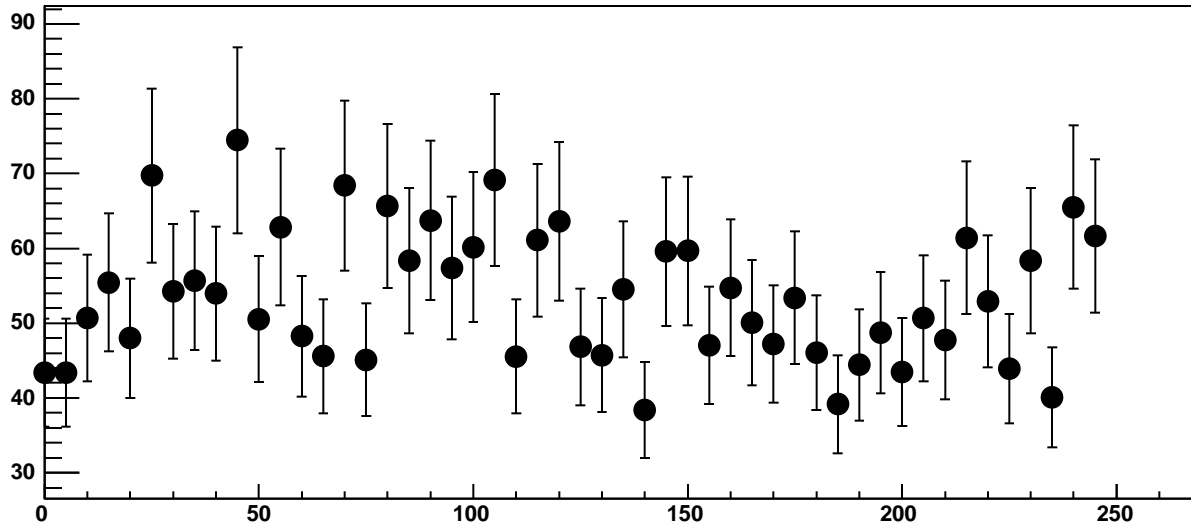
Chip 8, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold



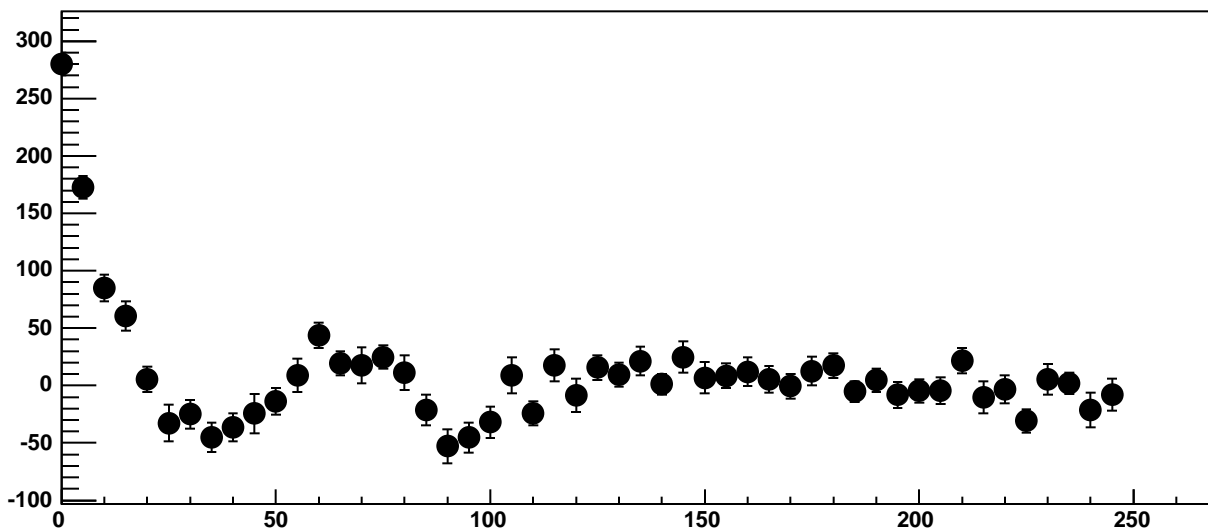
Chip 8, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold



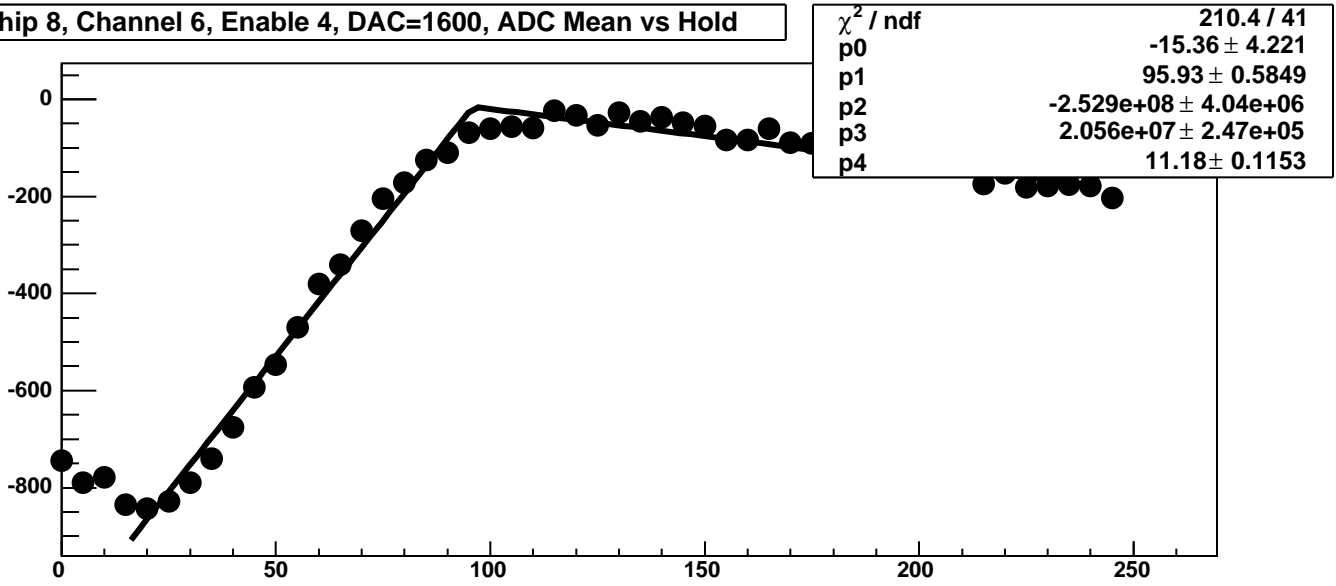
Chip 8, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



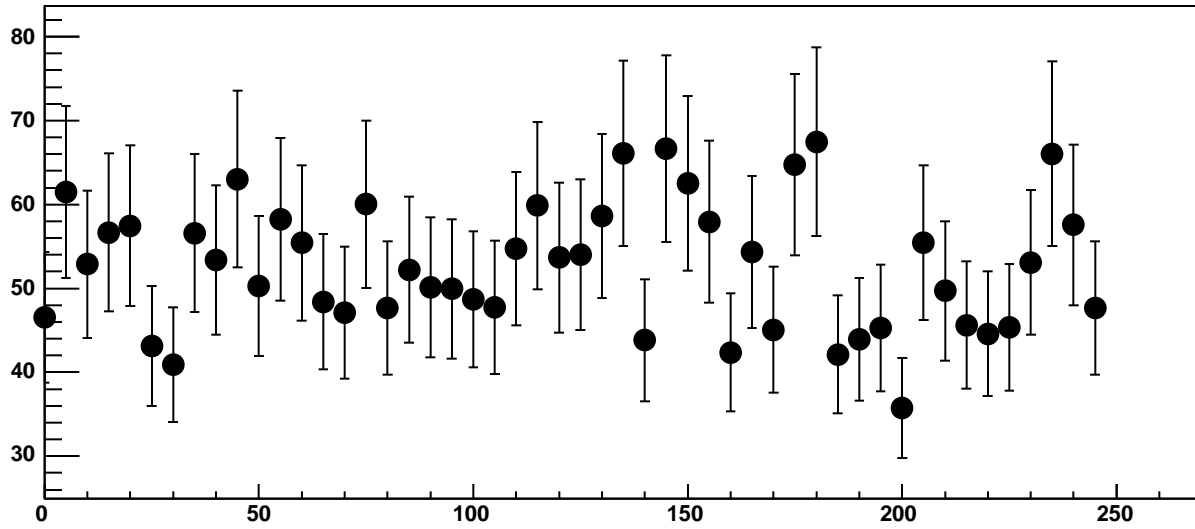
Chip 8, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold



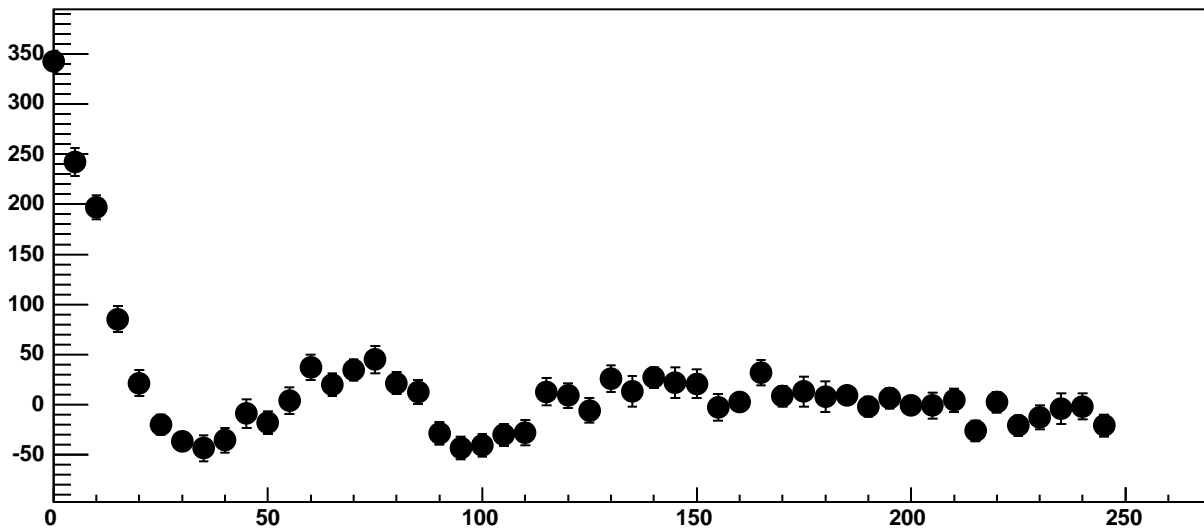
Chip 8, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold



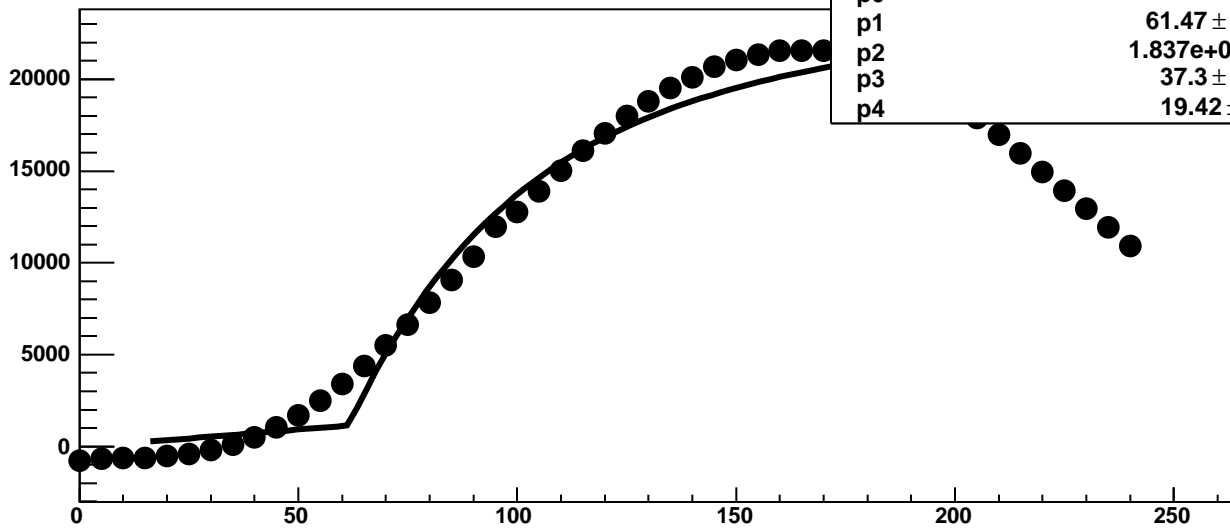
Chip 8, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



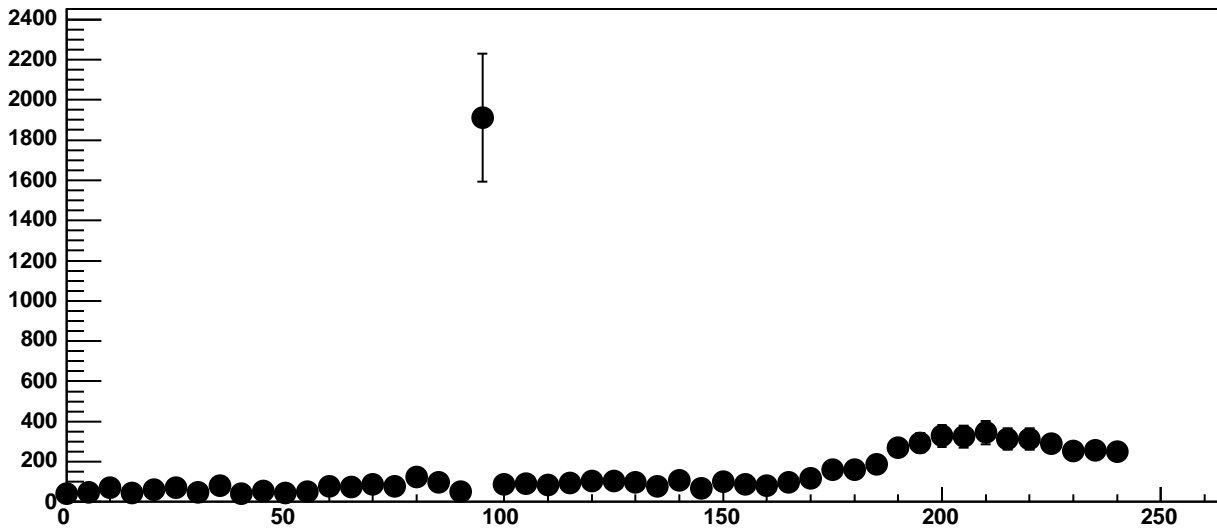
Chip 8, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold



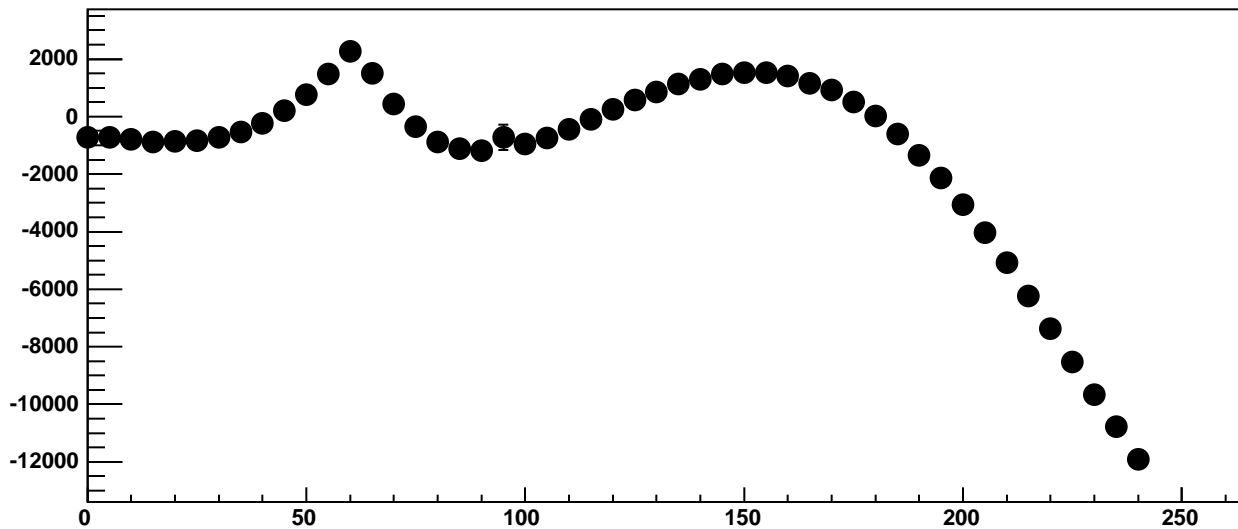
Chip 8, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 8, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

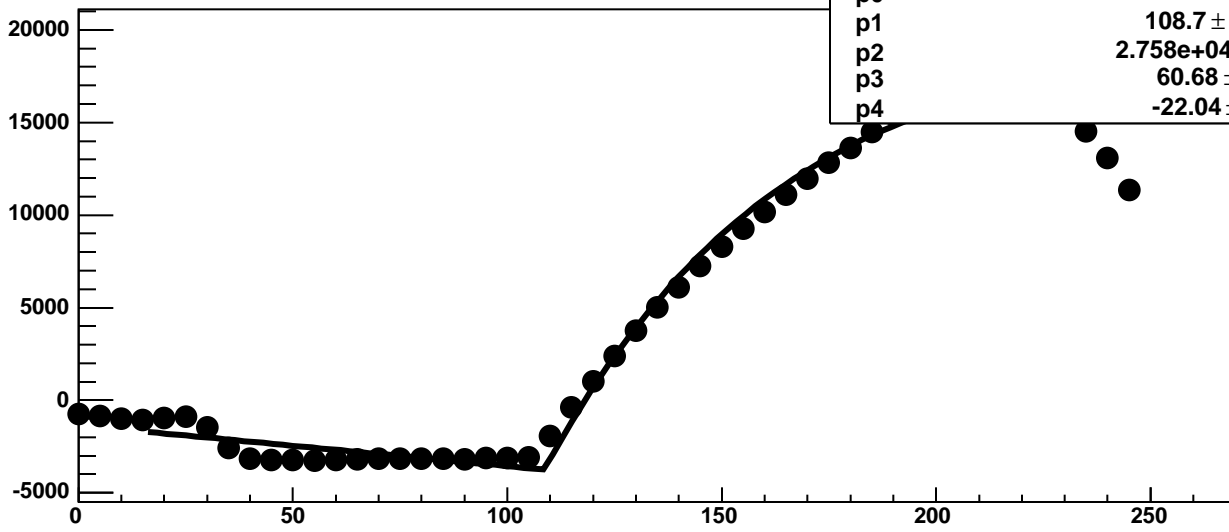


Chip 8, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold

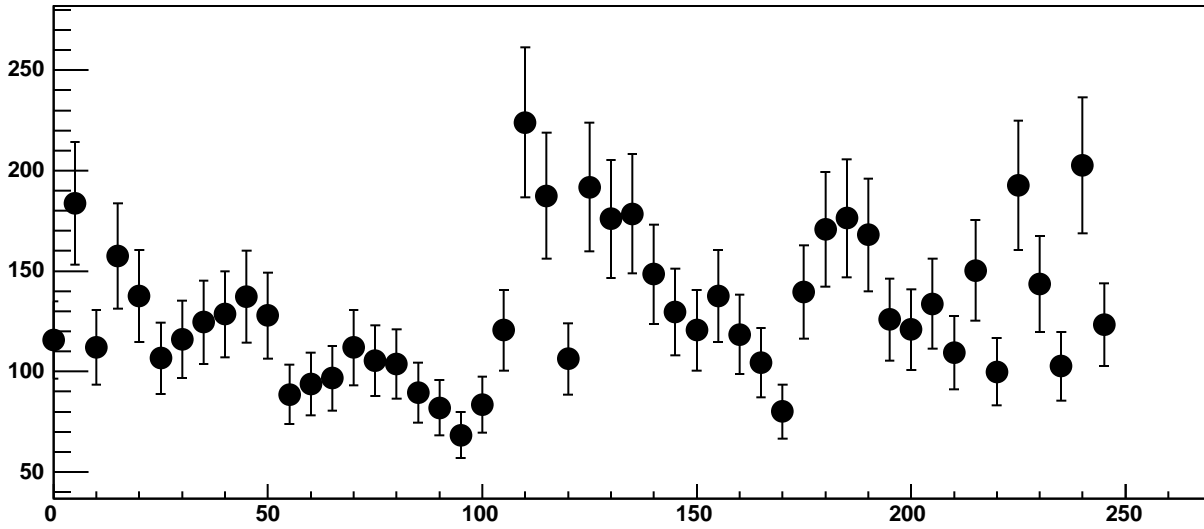




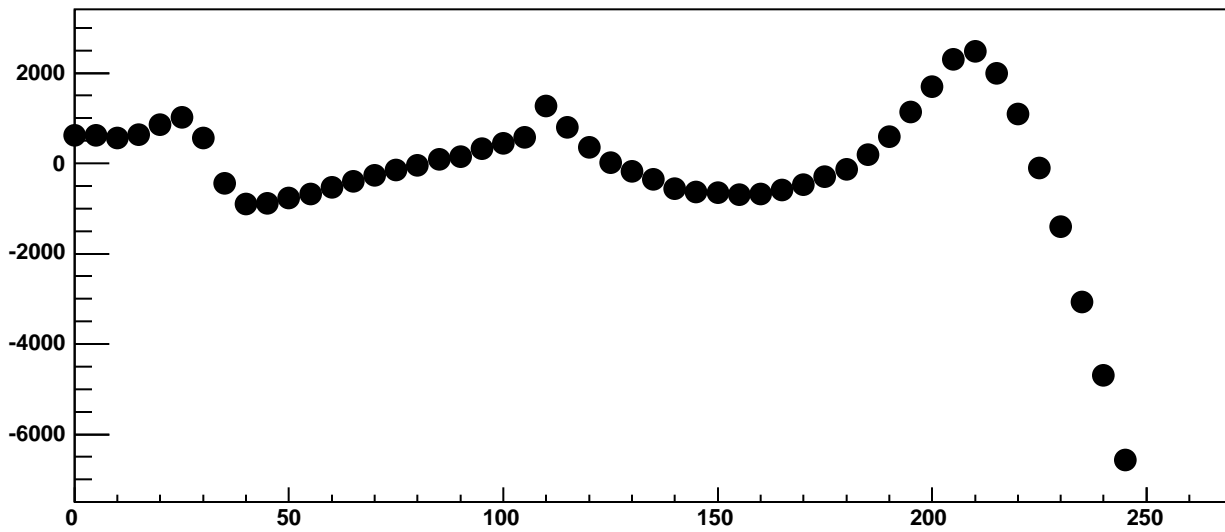
Chip 8, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold



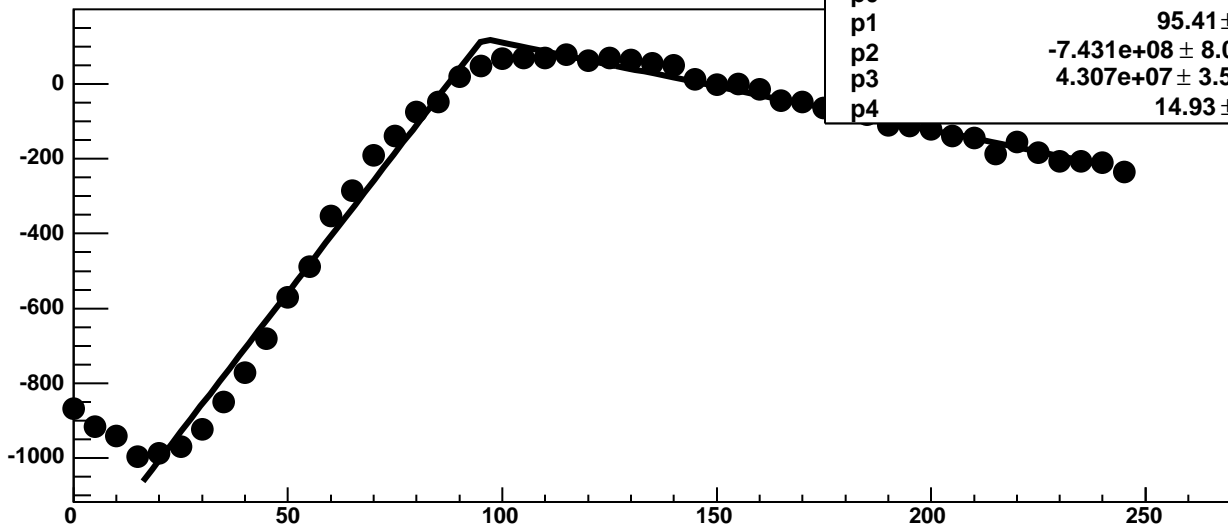
Chip 8, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

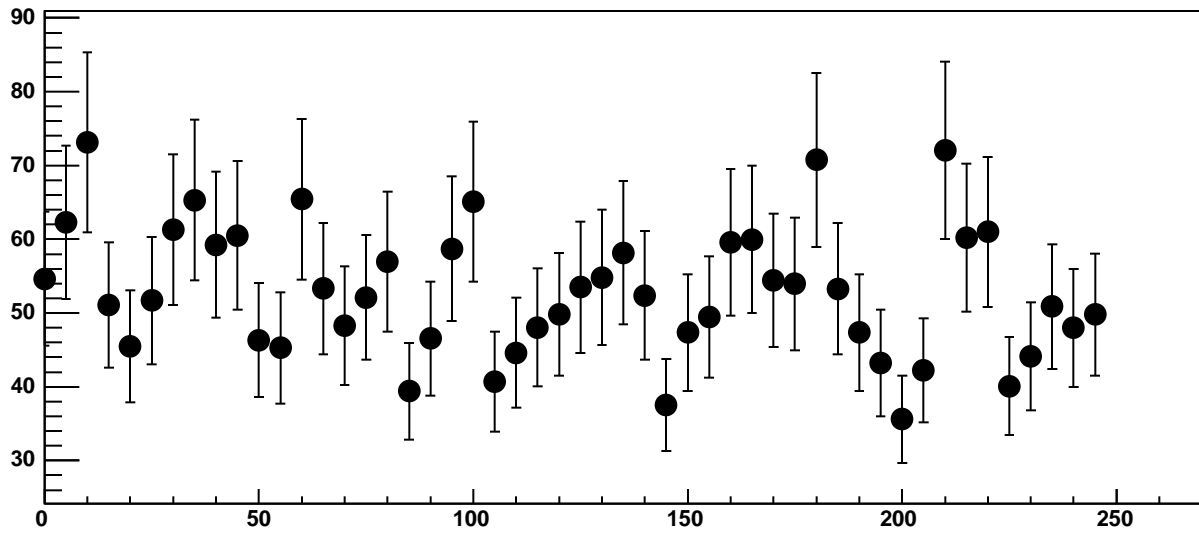


Chip 8, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

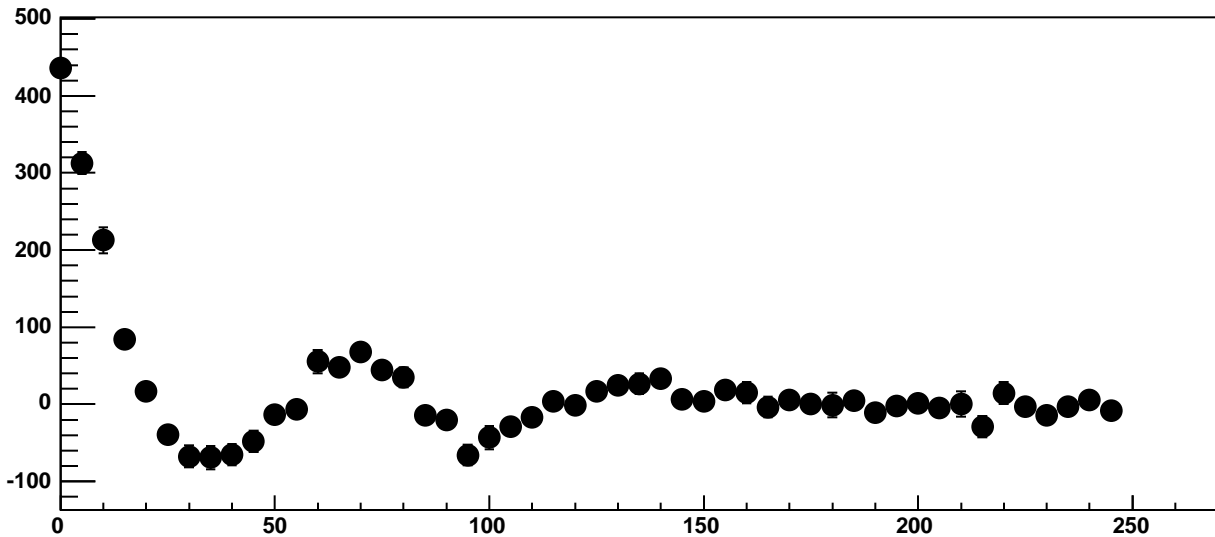


$\chi^2 / \text{ndf}$	317.9 / 41
p0	$120.6 \pm 3.775$
p1	$95.41 \pm 0.3952$
p2	$-7.431\text{e}+08 \pm 8.091\text{e}+06$
p3	$4.307\text{e}+07 \pm 3.516\text{e}+05$
p4	$14.93 \pm 0.1148$

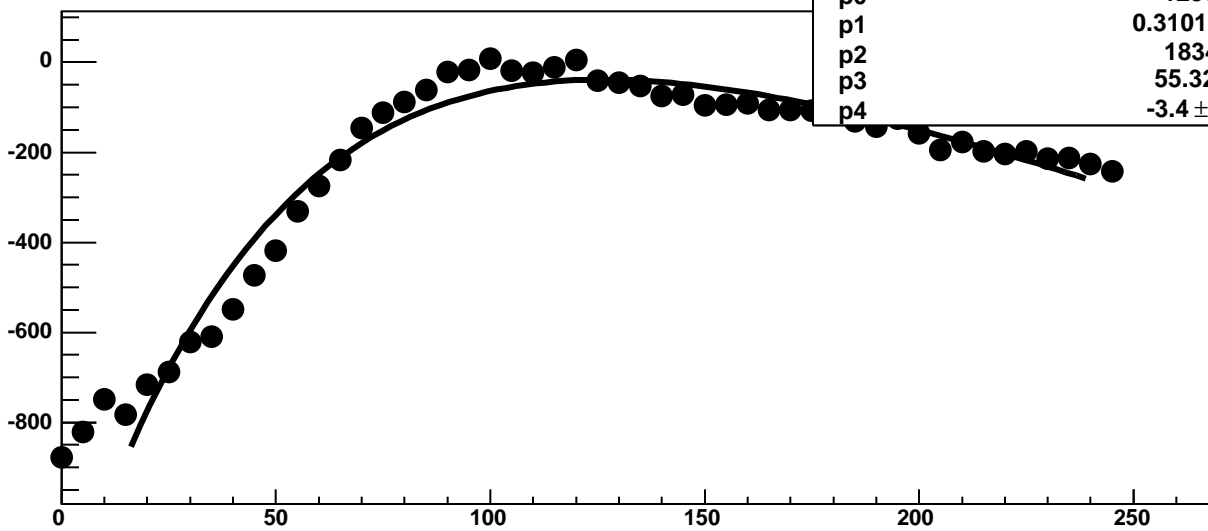
Chip 8, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

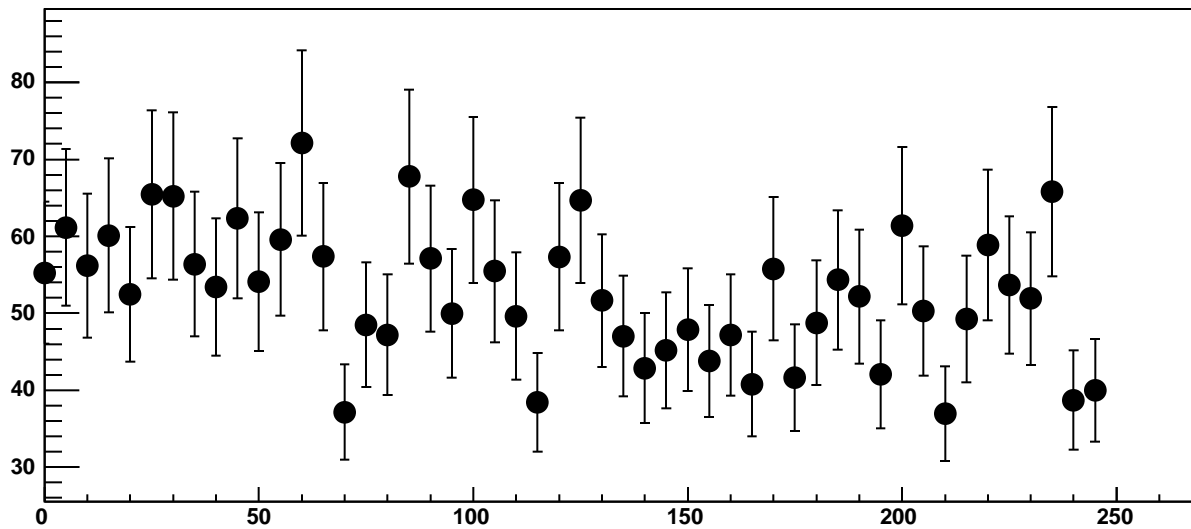


Chip 8, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold

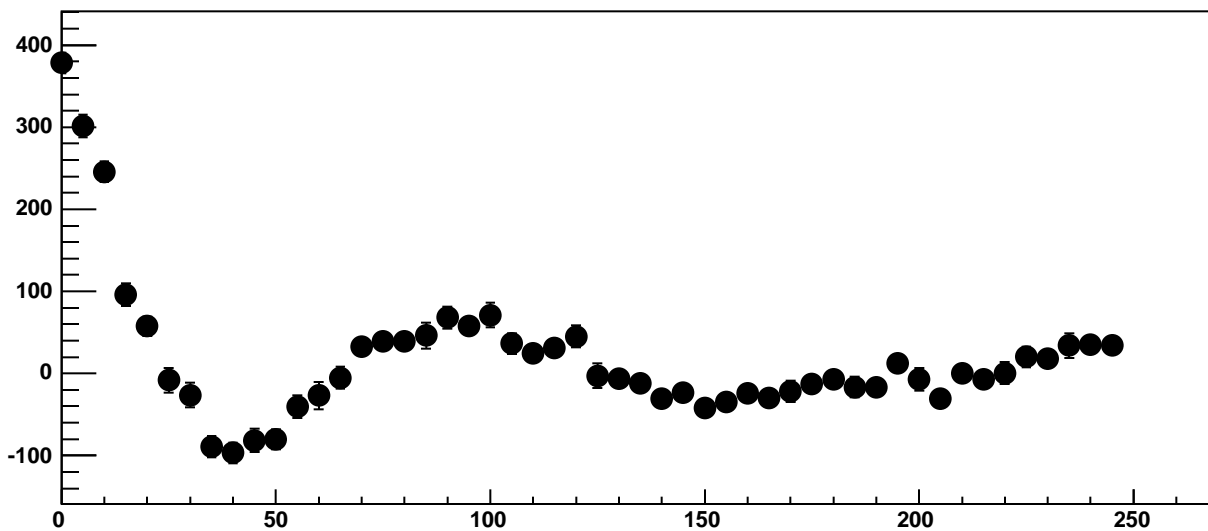


$\chi^2 / \text{ndf}$	534.4 / 41
p0	$-1256 \pm 22.41$
p1	$0.3101 \pm 0.8028$
p2	$1834 \pm 25.51$
p3	$55.32 \pm 1.148$
p4	$-3.4 \pm 0.09424$

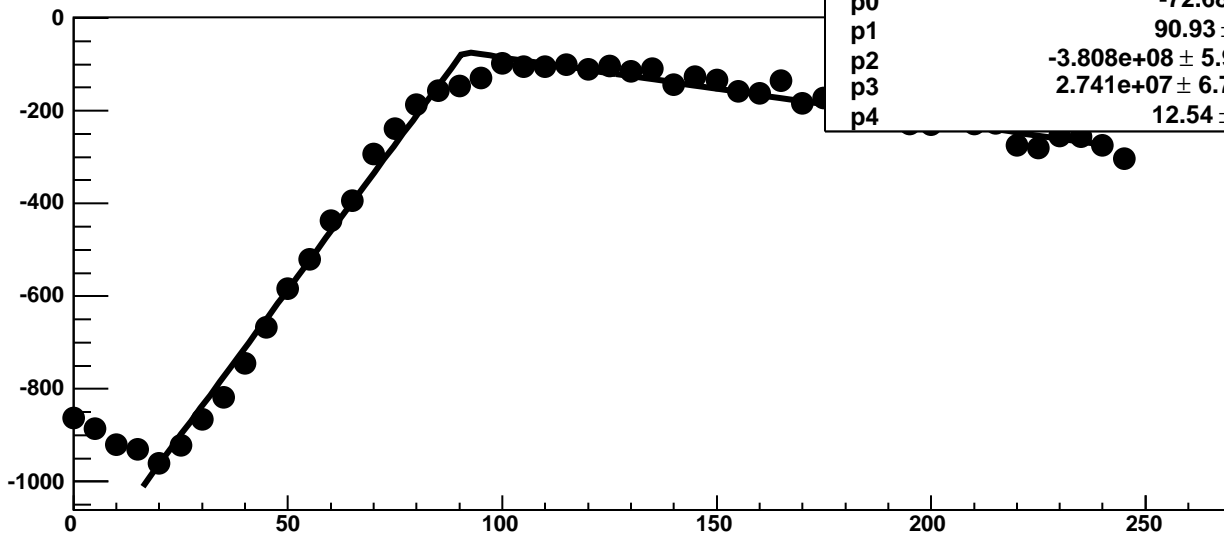
Chip 8, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold

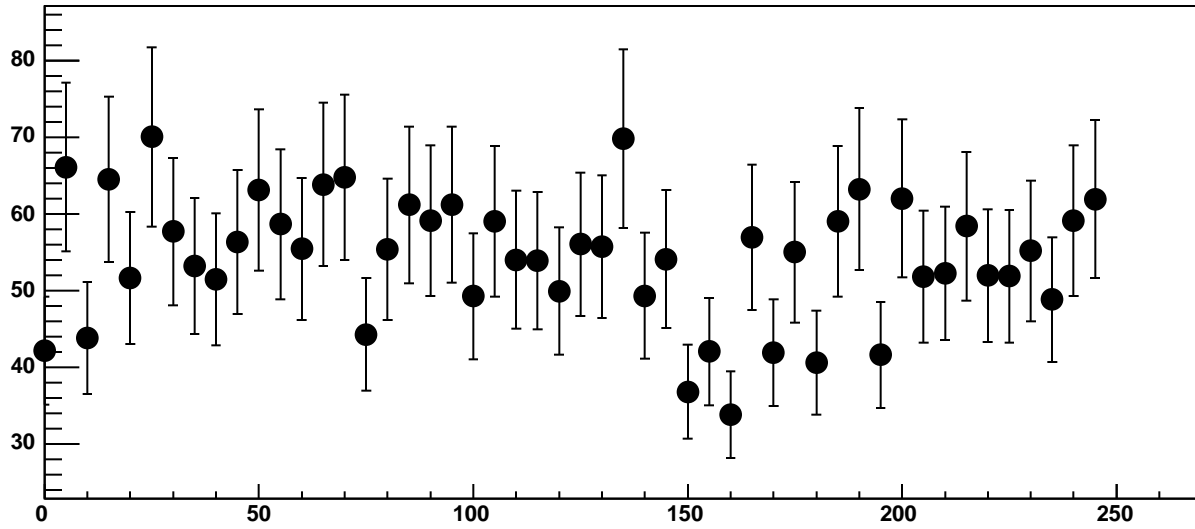


Chip 8, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

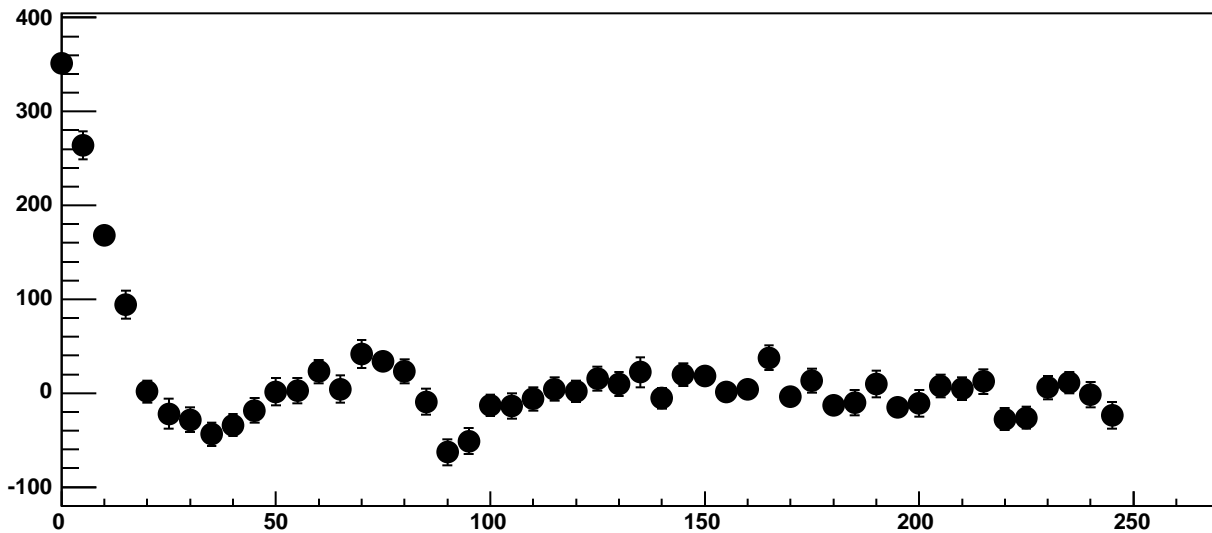


$\chi^2 / \text{ndf}$	173.9 / 41
p0	$-72.68 \pm 4.397$
p1	$90.93 \pm 0.4327$
p2	$-3.808\text{e}+08 \pm 5.944\text{e}+06$
p3	$2.741\text{e}+07 \pm 6.786\text{e}+05$
p4	$12.54 \pm 0.1286$

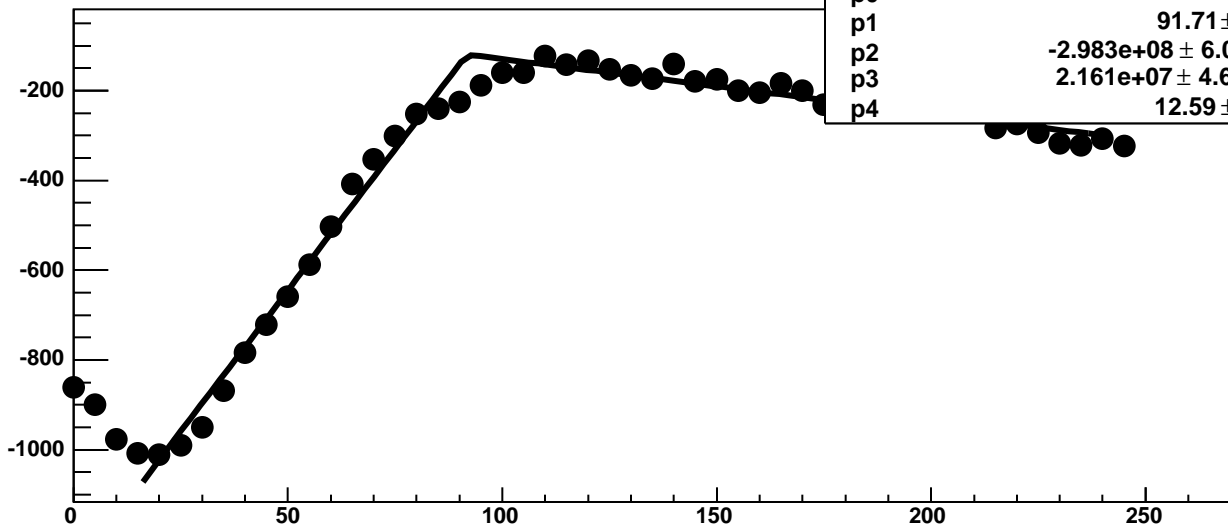
Chip 8, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

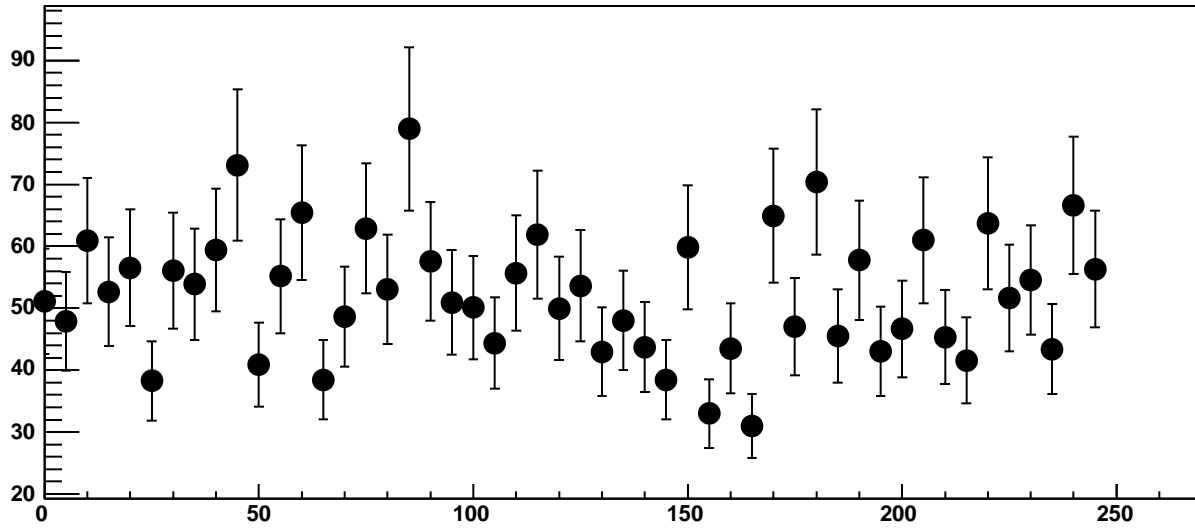


Chip 8, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

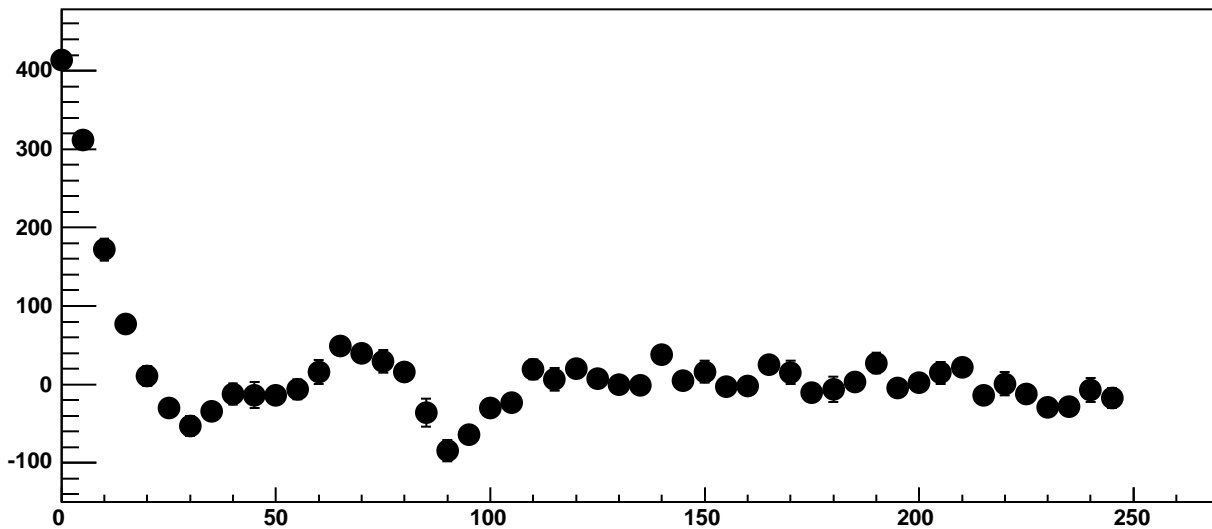


$\chi^2 / \text{ndf}$	284 / 41
p0	$-119.7 \pm 3.738$
p1	$91.71 \pm 0.5047$
p2	$-2.983\text{e}+08 \pm 6.027\text{e}+06$
p3	$2.161\text{e}+07 \pm 4.677\text{e}+05$
p4	$12.59 \pm 0.1182$

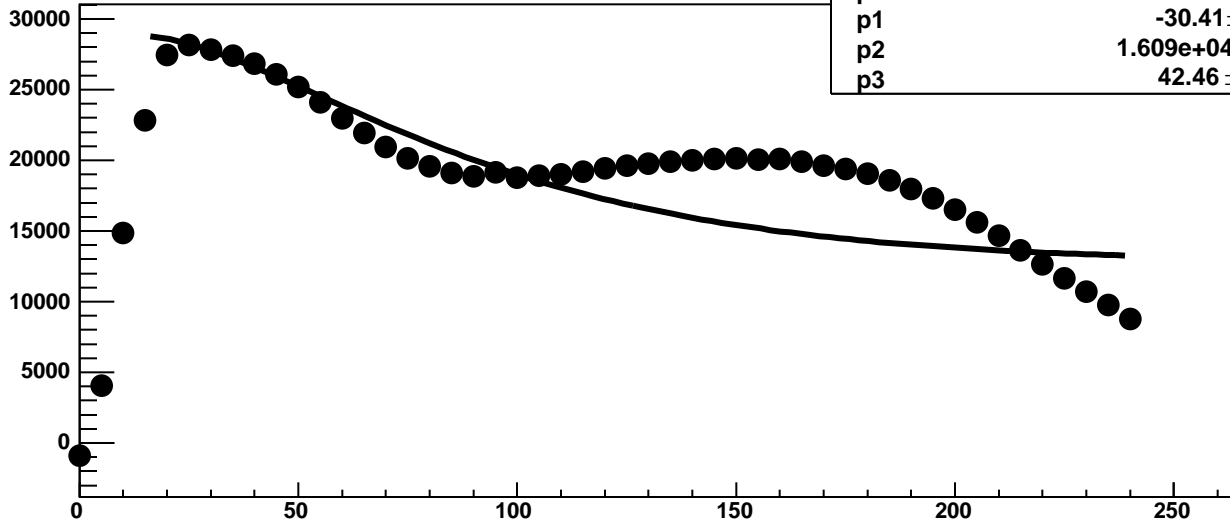
Chip 8, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



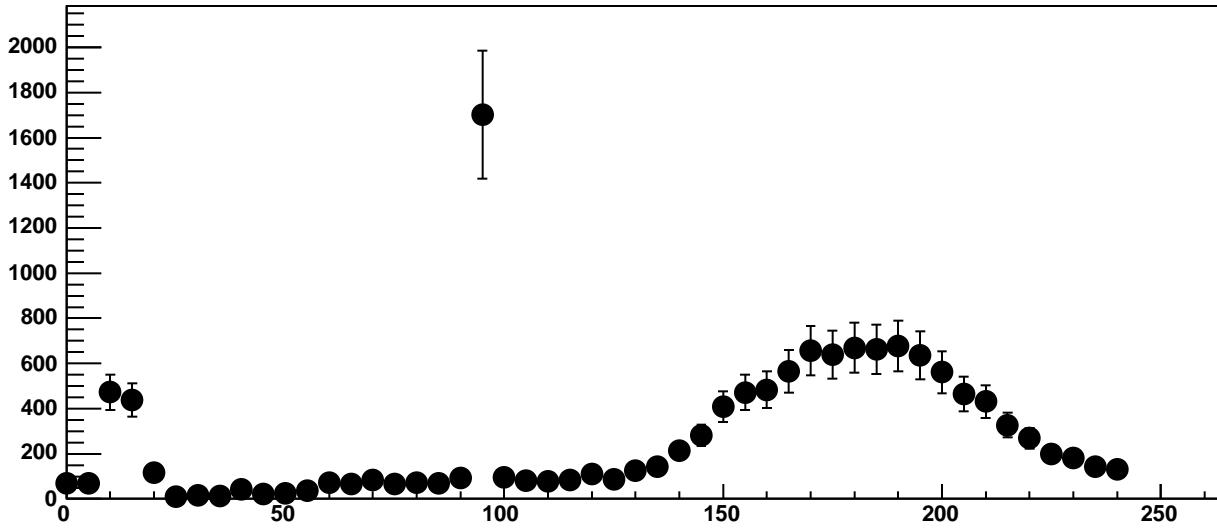
Chip 8, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold



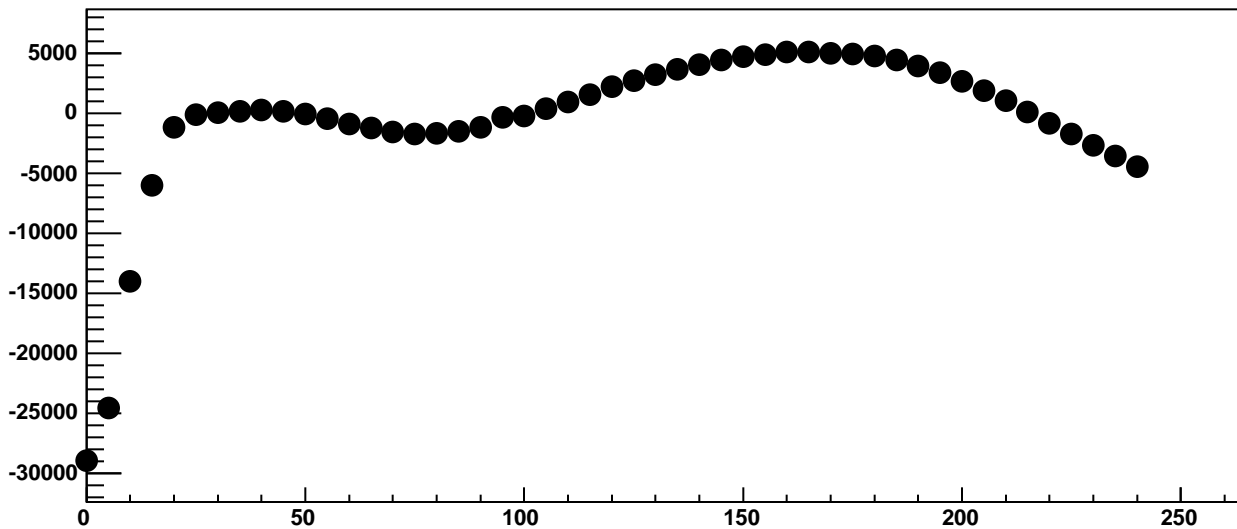
Chip 8, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold



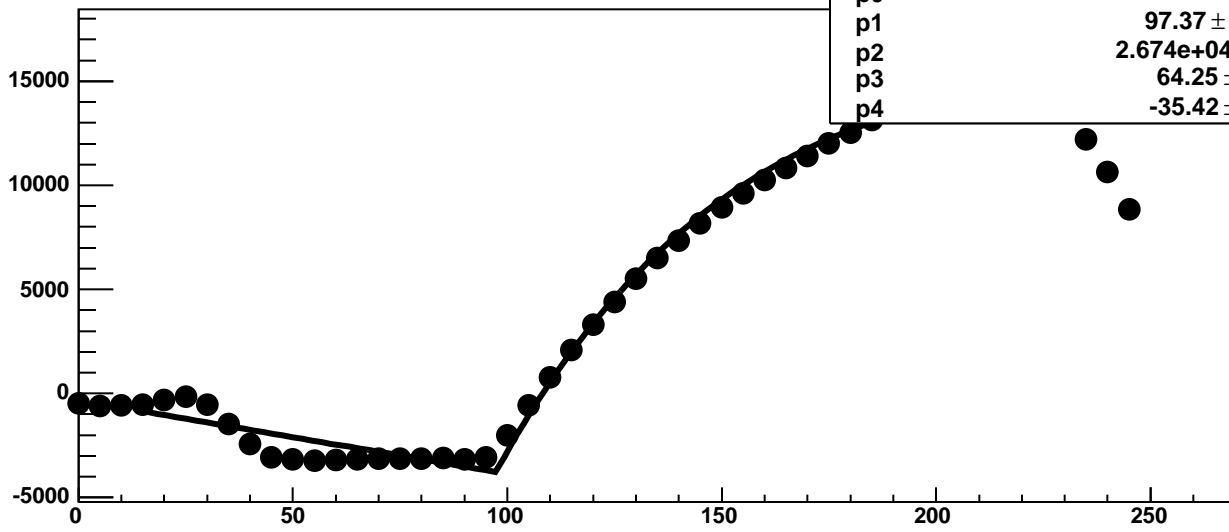
Chip 8, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold

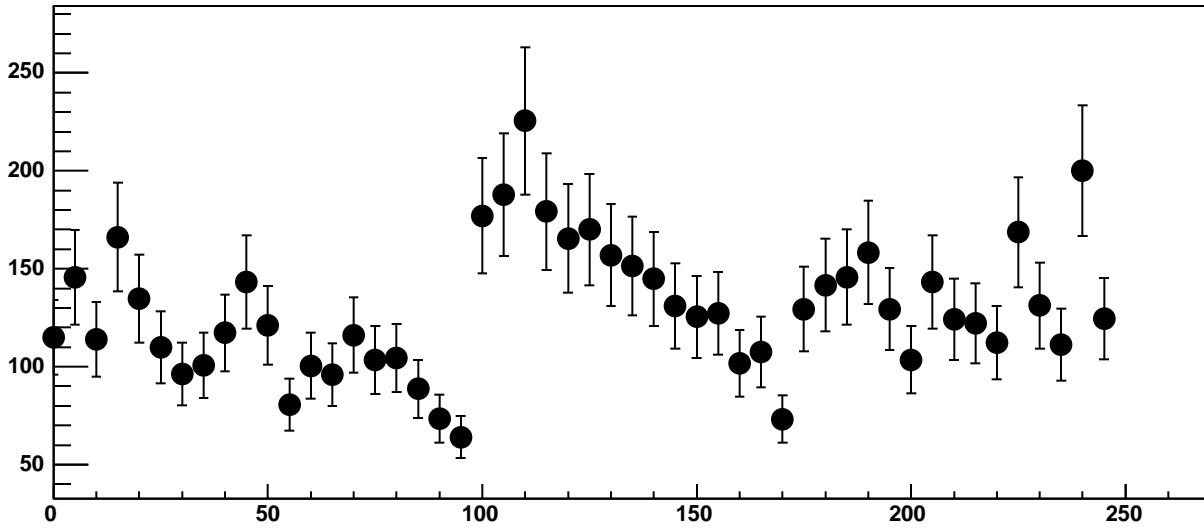


Chip 8, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

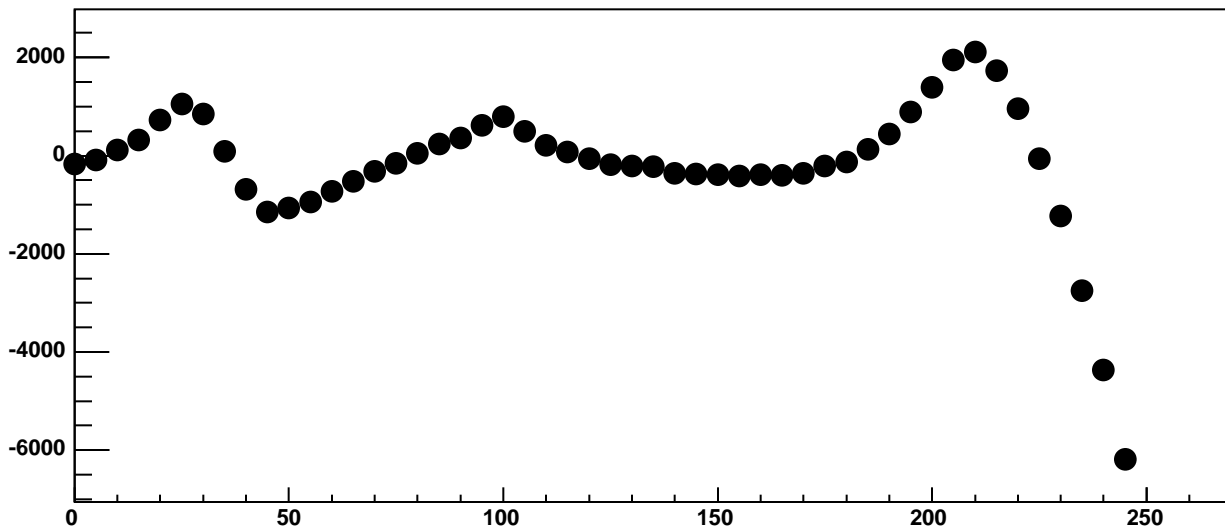


$\chi^2 / \text{ndf}$	5.75e+04 / 41
p0	-3774 ± 8.772
p1	97.37 ± 0.06902
p2	2.674e+04 ± 60.16
p3	64.25 ± 0.2236
p4	-35.42 ± 0.2194

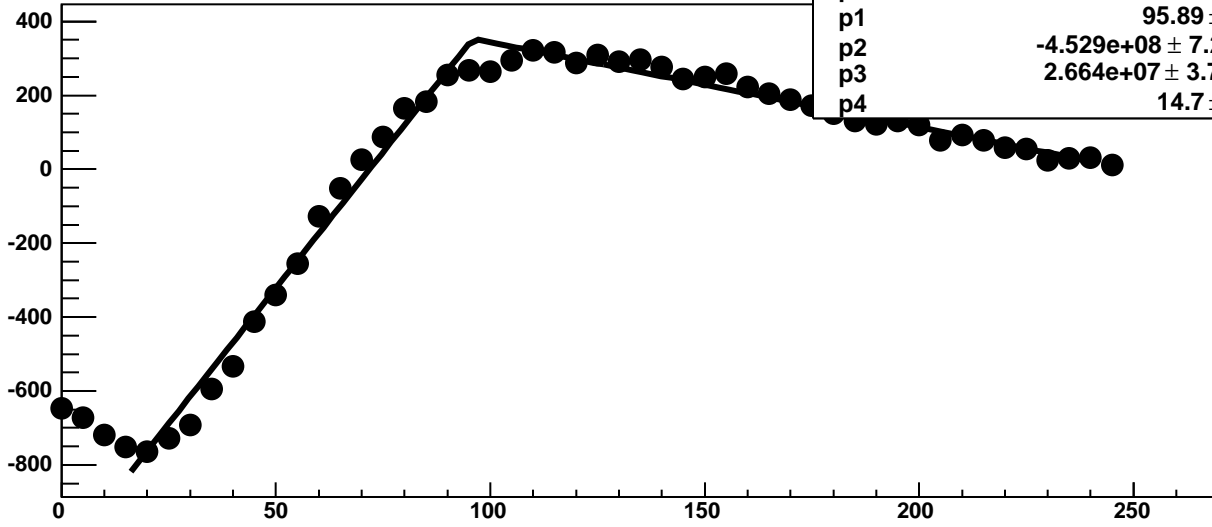
Chip 8, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

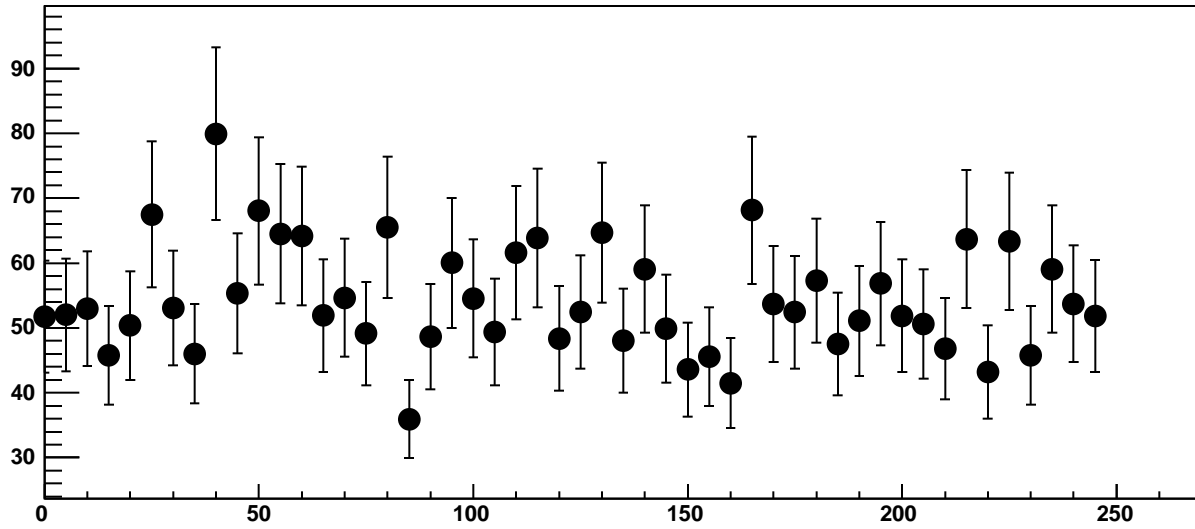


Chip 8, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

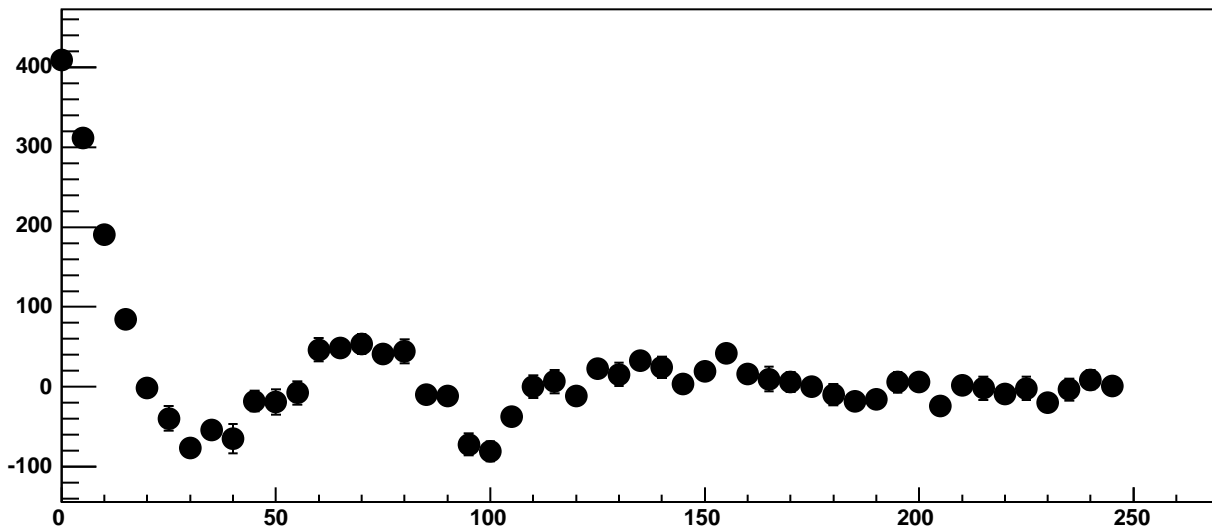


$\chi^2 / \text{ndf}$	359.1 / 41
p0	$353.4 \pm 4.061$
p1	$95.89 \pm 0.4177$
p2	$-4.529\text{e}+08 \pm 7.224\text{e}+06$
p3	$2.664\text{e}+07 \pm 3.762\text{e}+05$
p4	$14.7 \pm 0.1145$

Chip 8, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

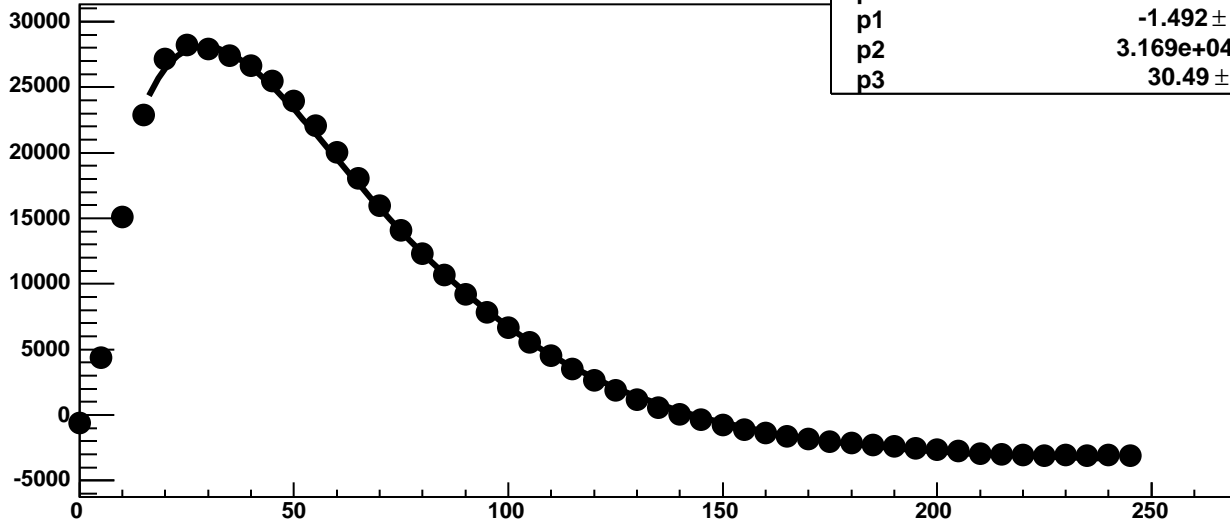


Chip 8, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



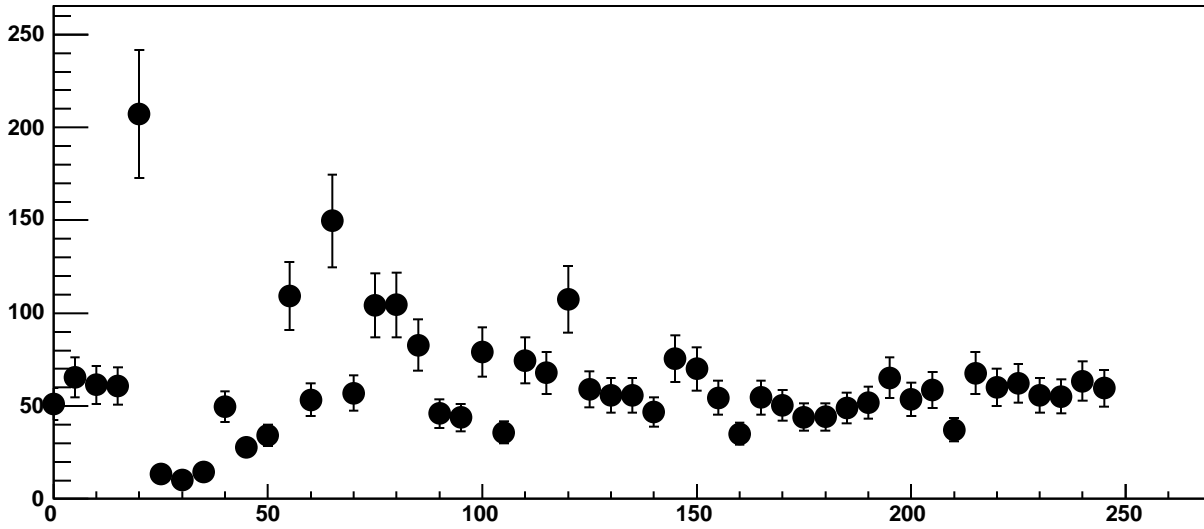


Chip 8, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold

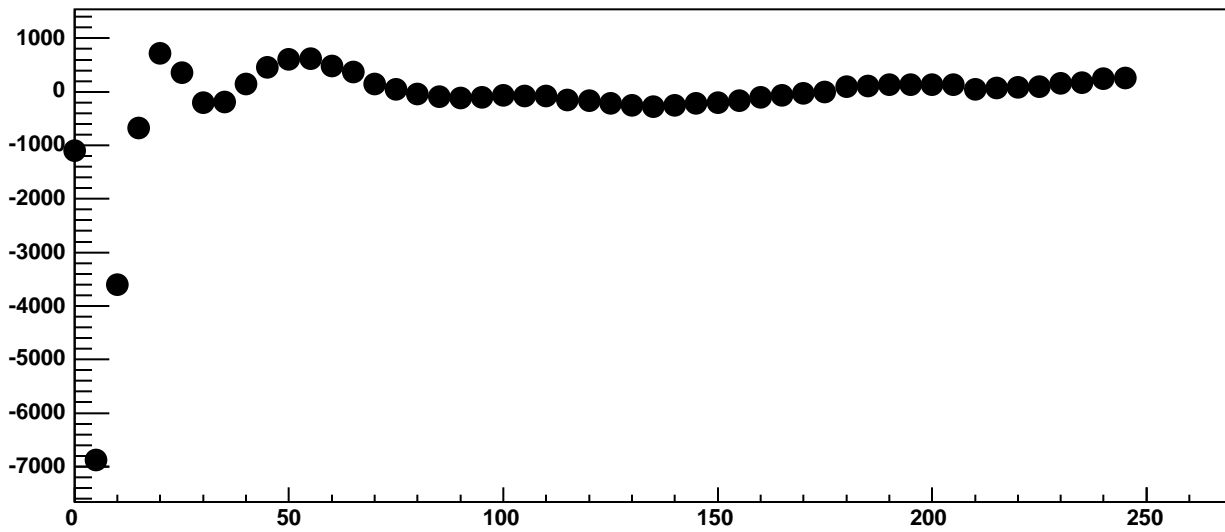


$\chi^2 / \text{ndf}$	4.486e+04 / 42
p0	-3551 ± 3.585
p1	-1.492 ± 0.01608
p2	3.169e+04 ± 3.758
p3	30.49 ± 0.01001

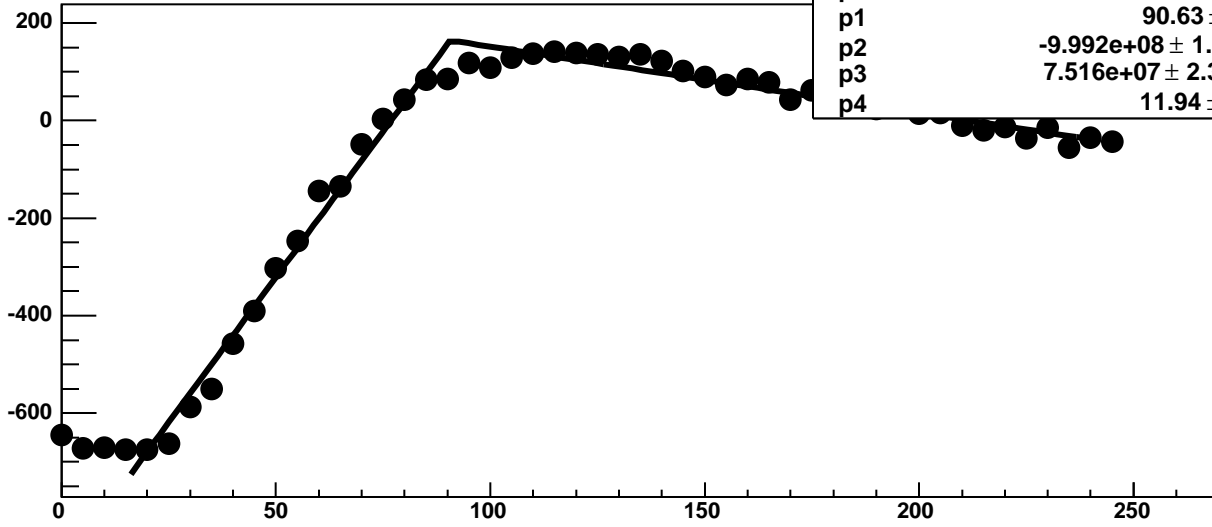
Chip 8, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold

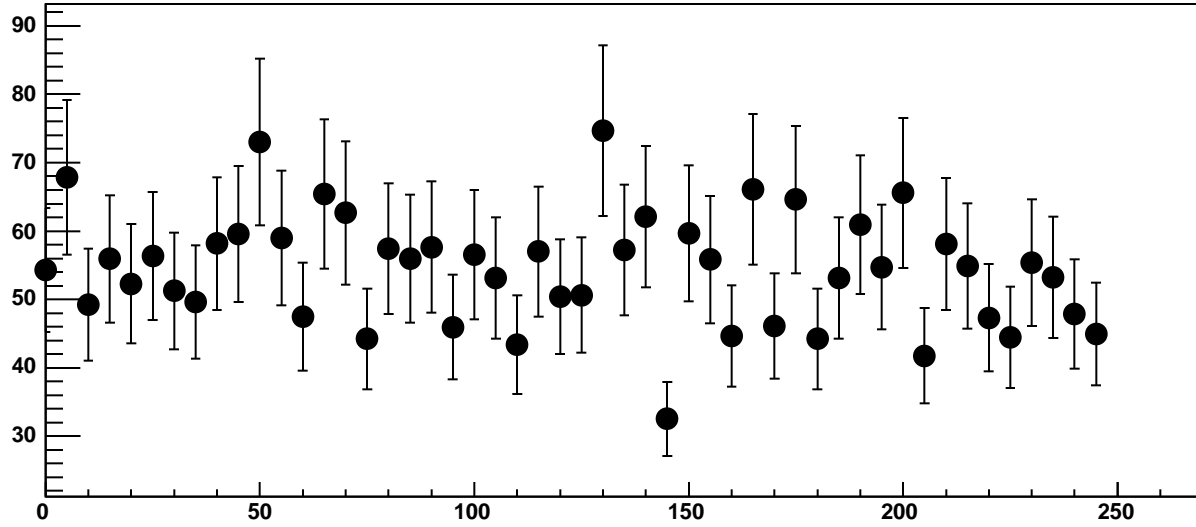


Chip 8, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

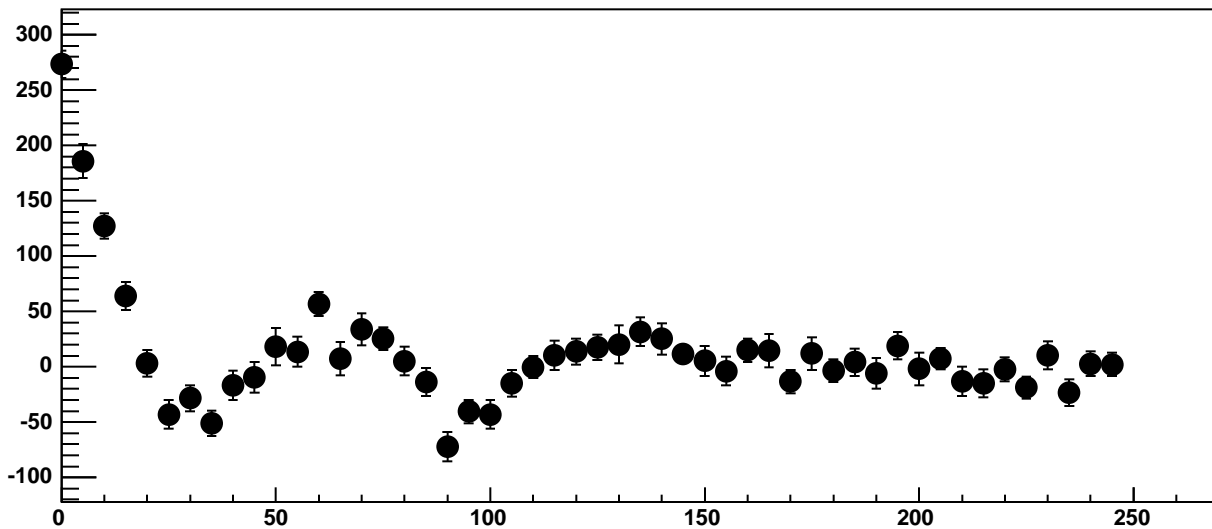


$\chi^2 / \text{ndf}$	199.7 / 41
p0	$164.4 \pm 3.932$
p1	$90.63 \pm 0.5637$
p2	$-9.992\text{e}+08 \pm 1.111\text{e}+07$
p3	$7.516\text{e}+07 \pm 2.384\text{e}+05$
p4	$11.94 \pm 0.1356$

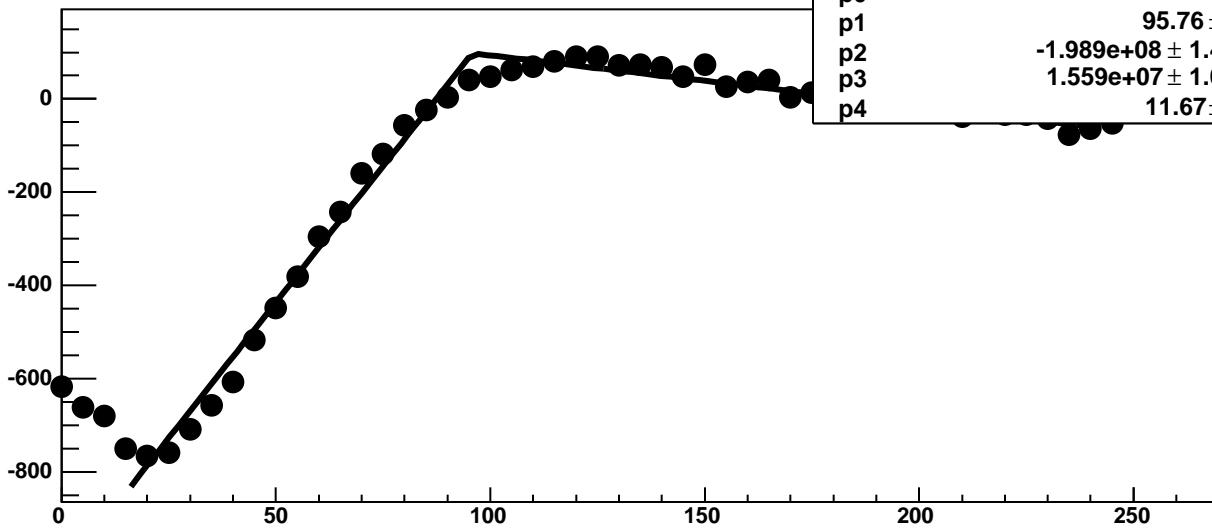
Chip 8, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

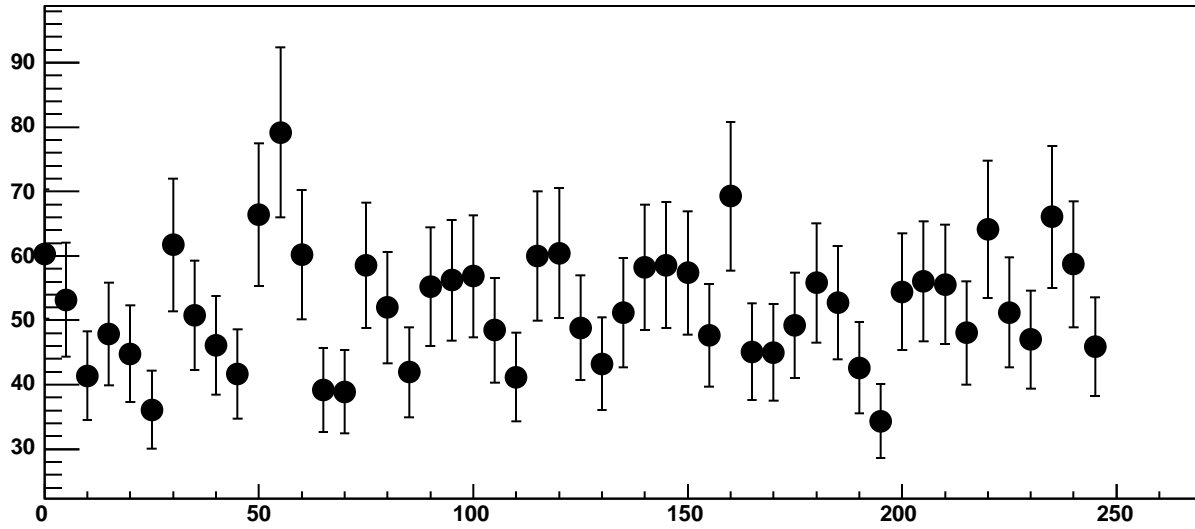


Chip 8, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

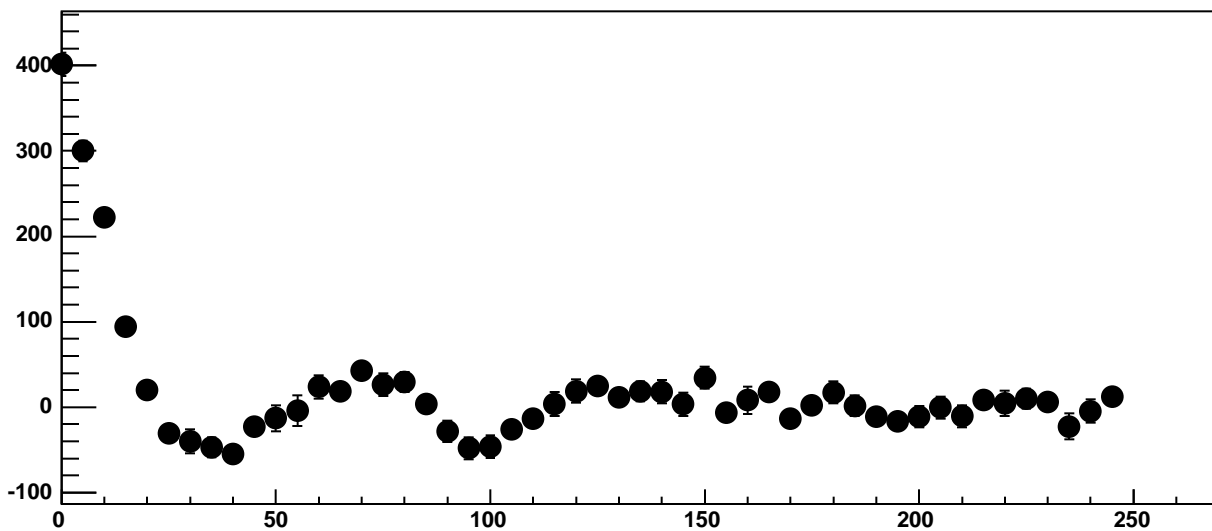


$\chi^2 / \text{ndf}$	266 / 41
p0	98.09 ± 4.113
p1	95.76 ± 0.5472
p2	-1.989e+08 ± 1.404e+07
p3	1.559e+07 ± 1.087e+06
p4	11.67 ± 0.1088

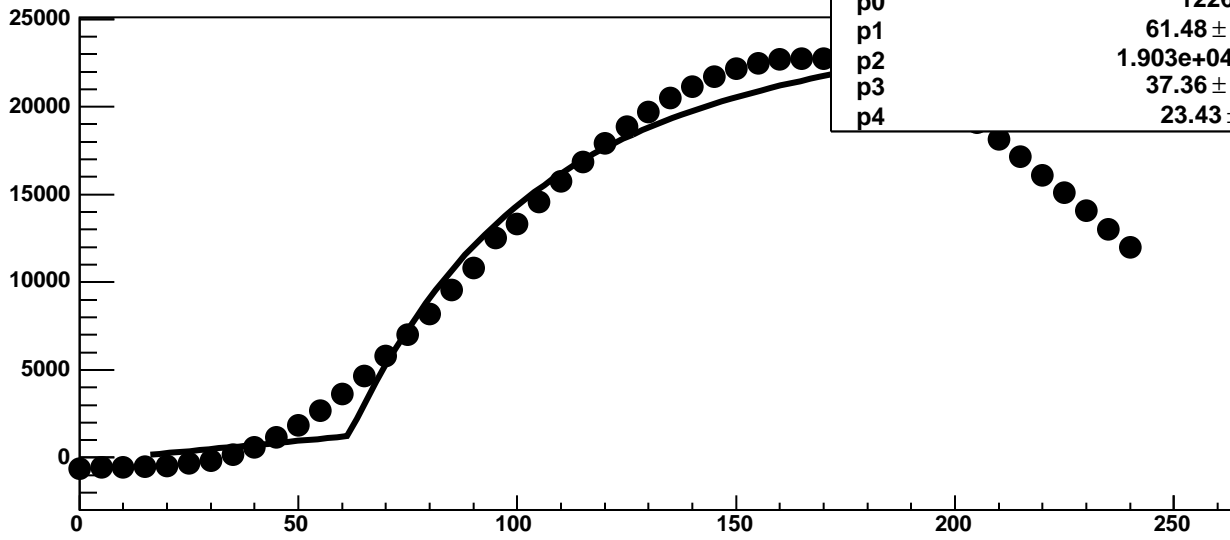
Chip 8, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



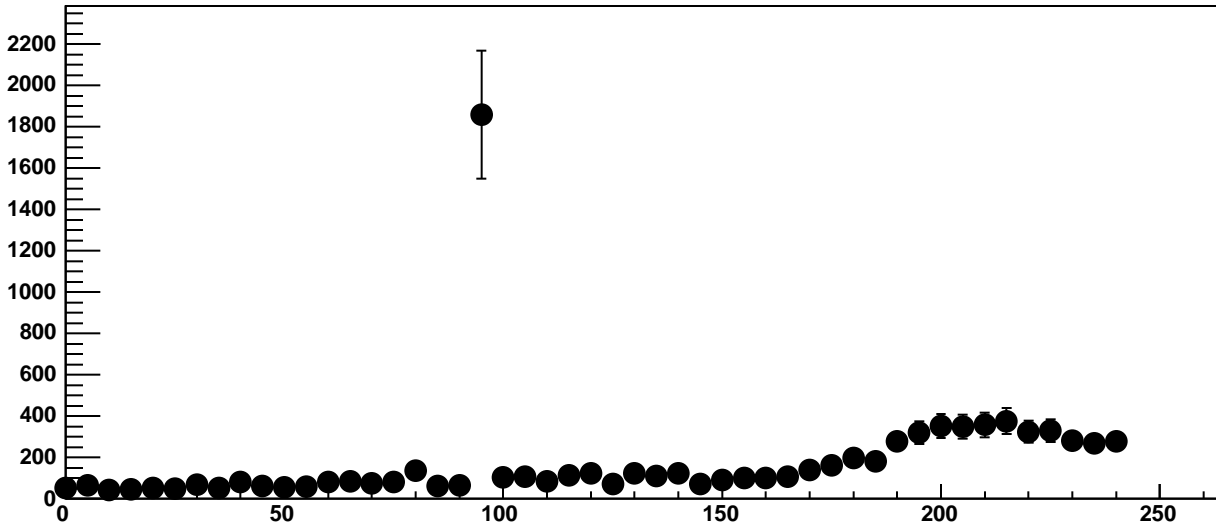
Chip 8, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold



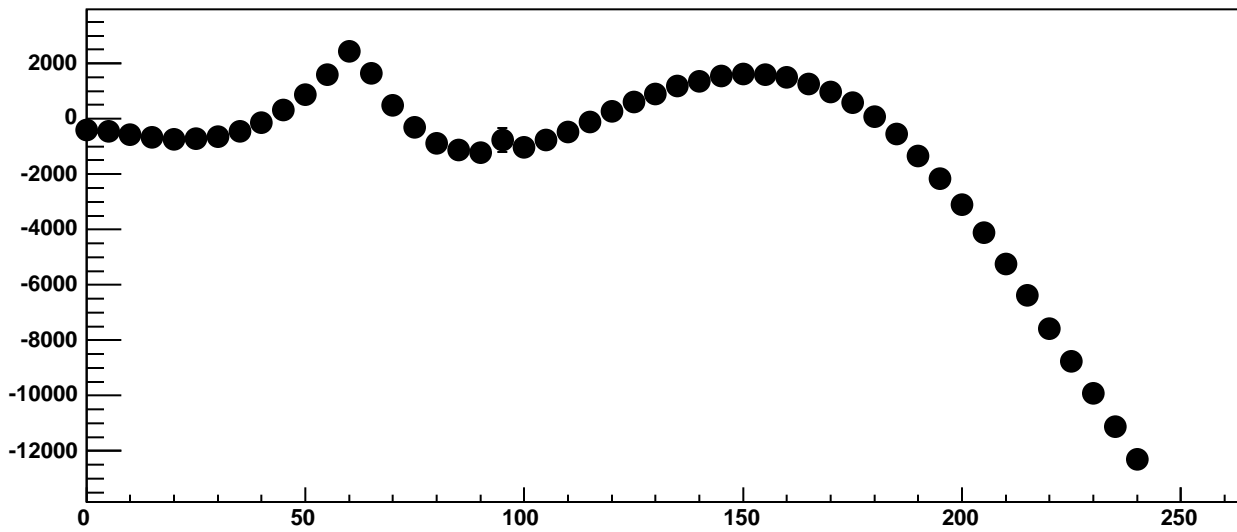
Chip 8, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold



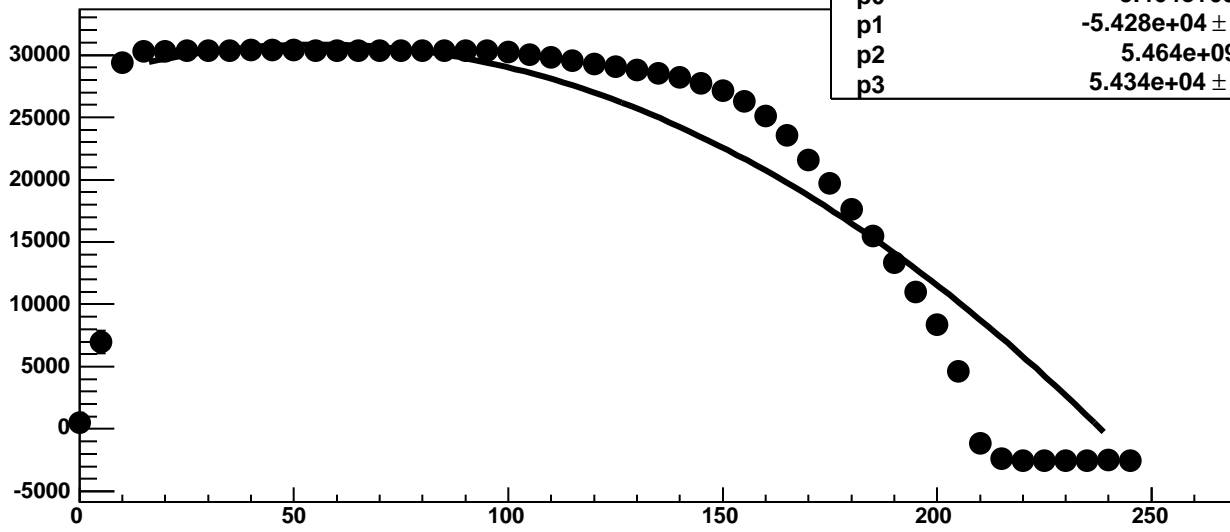
Chip 8, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold

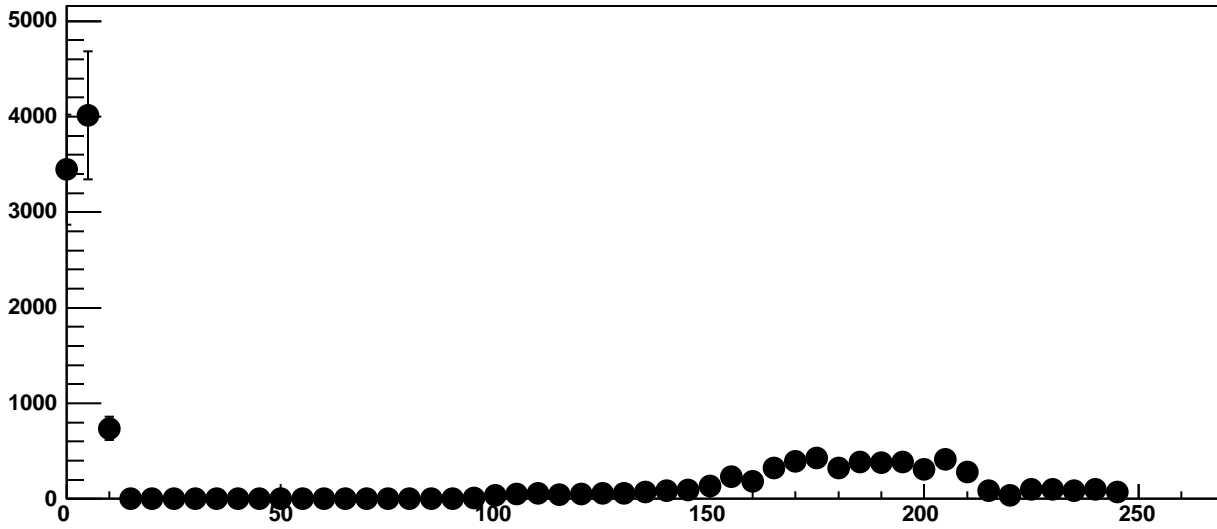


Chip 8, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold

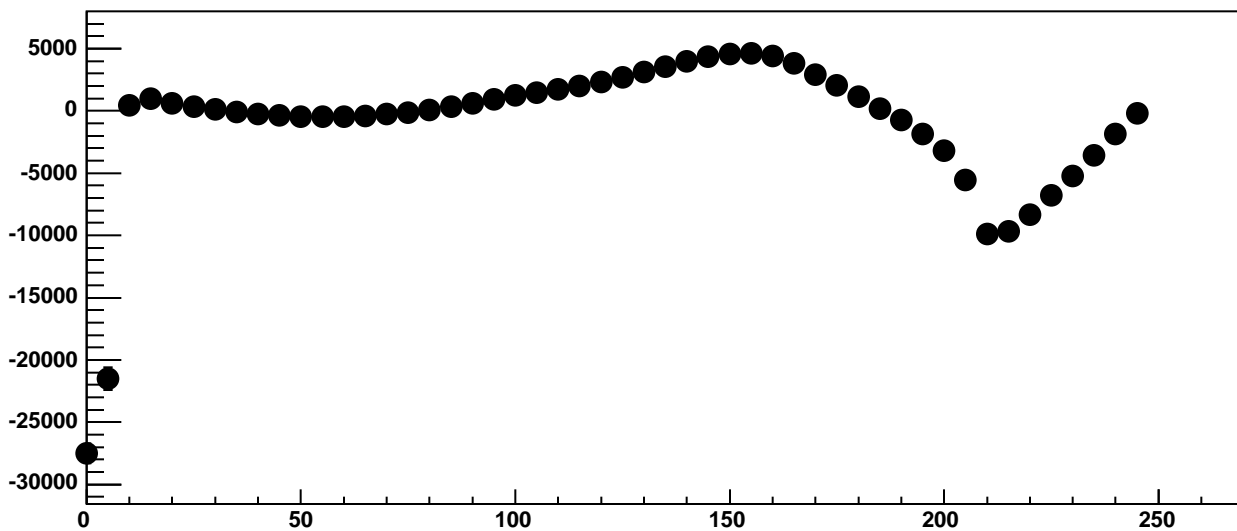


$\chi^2 / \text{ndf}$	4.83e+06 / 42
p0	-5.464e+09 ± 3.301
p1	-5.428e+04 ± 0.06518
p2	5.464e+09 ± 3.301
p3	5.434e+04 ± 0.06517

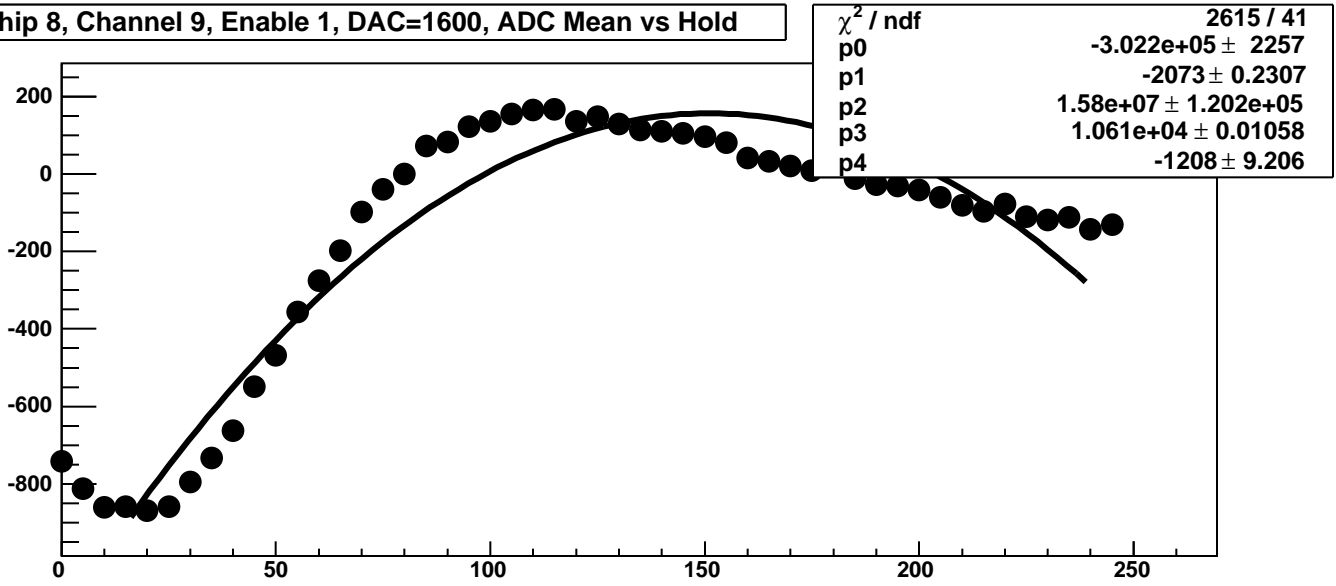
Chip 8, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



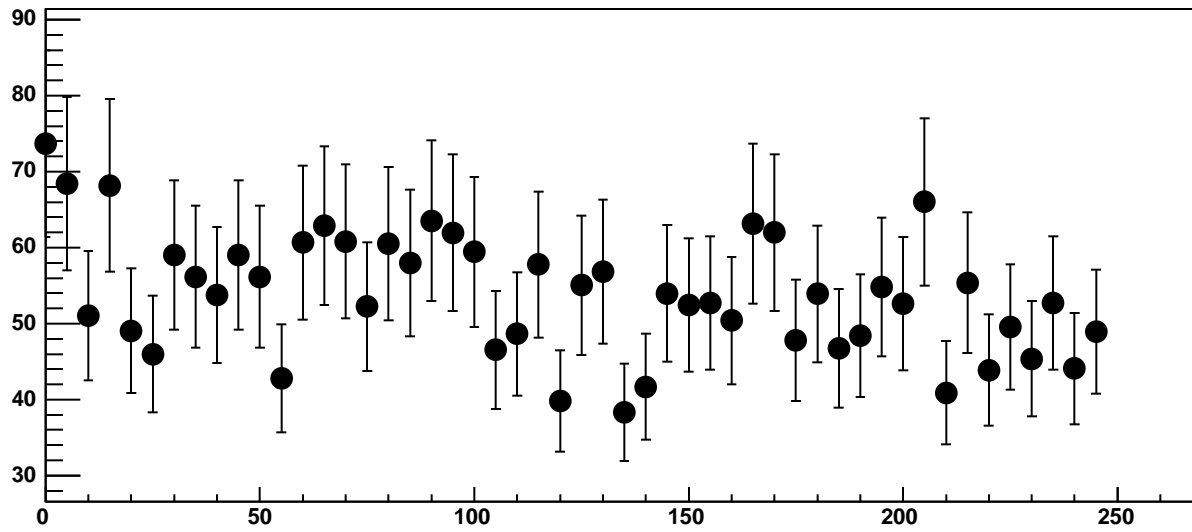
Chip 8, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold



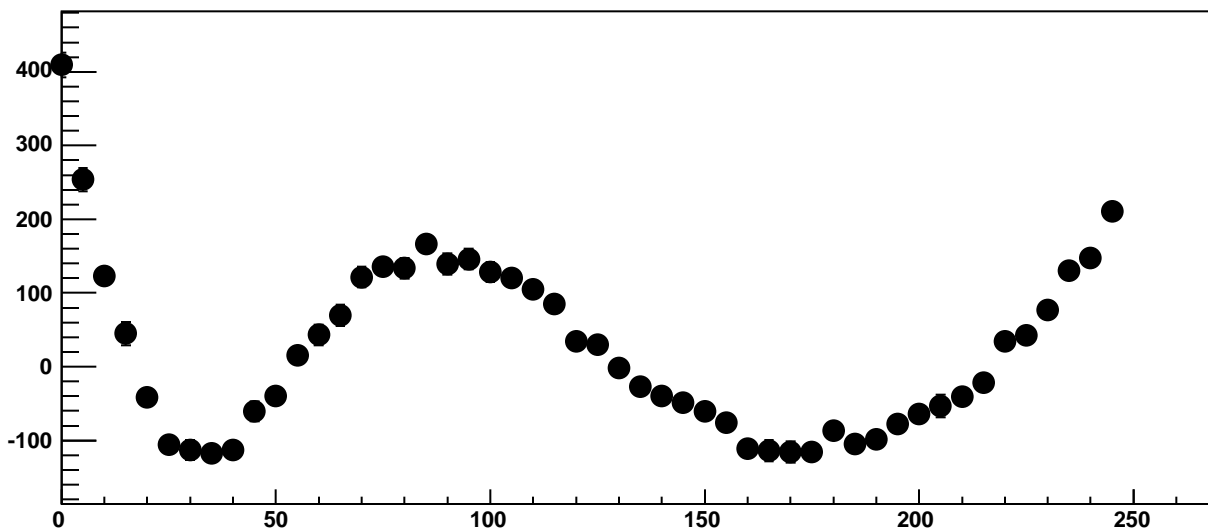
Chip 8, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold



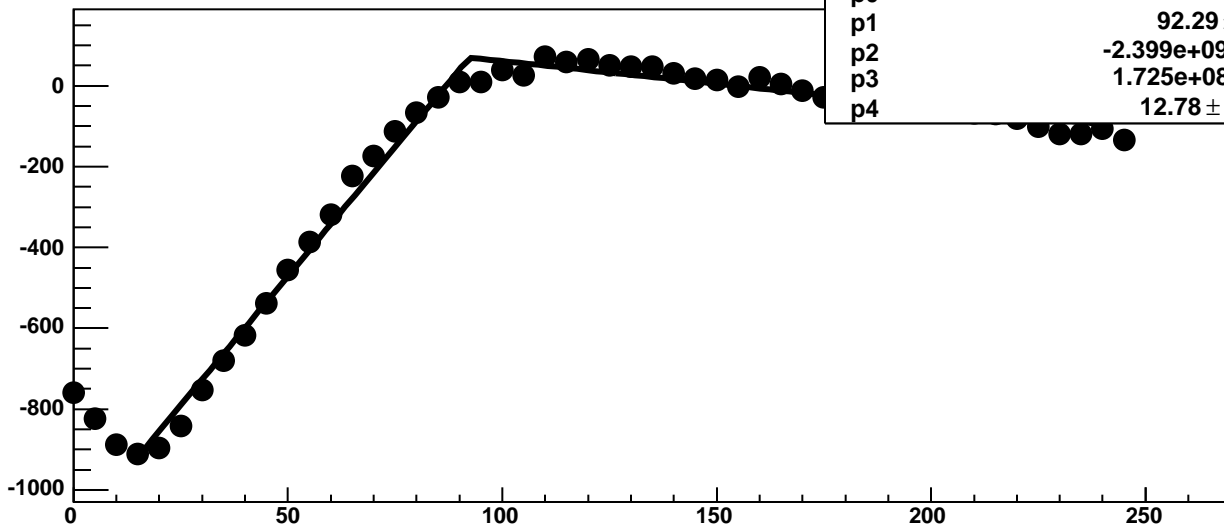
Chip 8, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

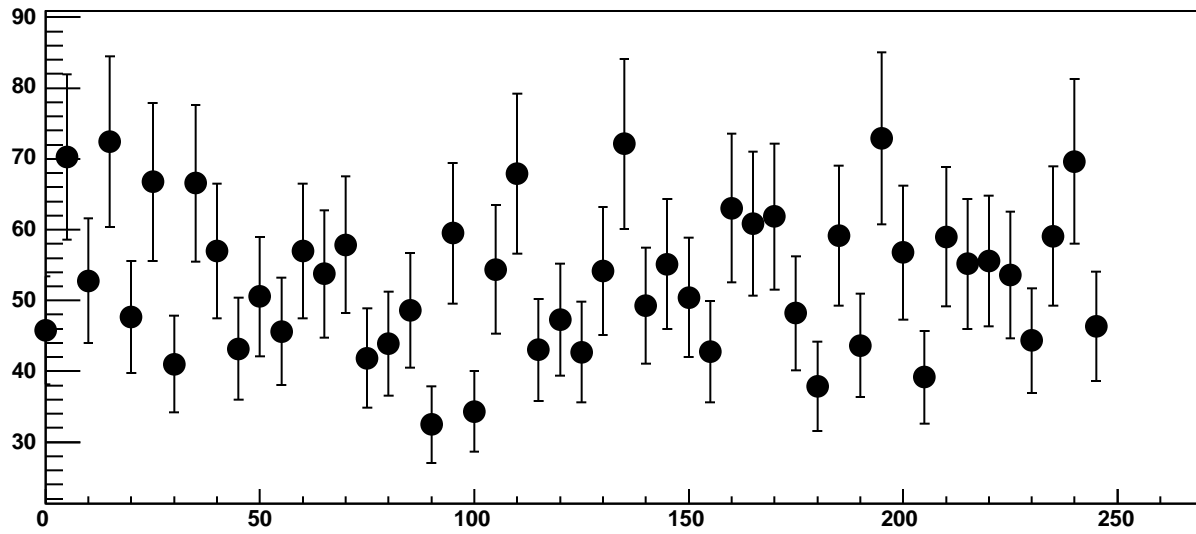


Chip 8, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

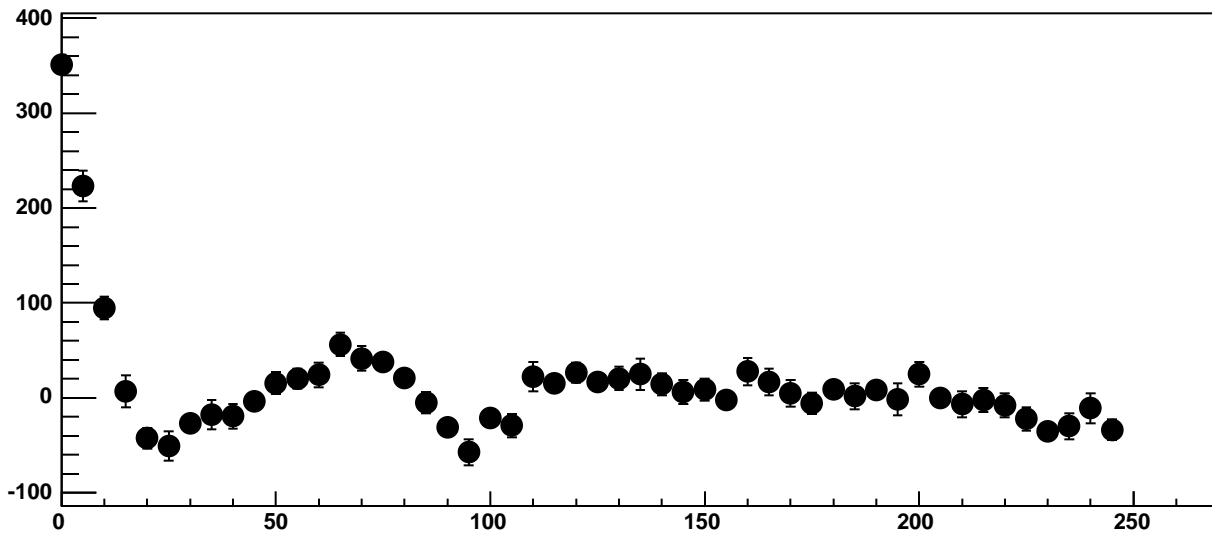


$\chi^2 / \text{ndf}$	198.1 / 41
p0	$69.85 \pm 3.487$
p1	$92.29 \pm 0.4281$
p2	$-2.399\text{e}+09 \pm 1.414$
p3	$1.725\text{e}+08 \pm 1.414$
p4	$12.78 \pm 0.04538$

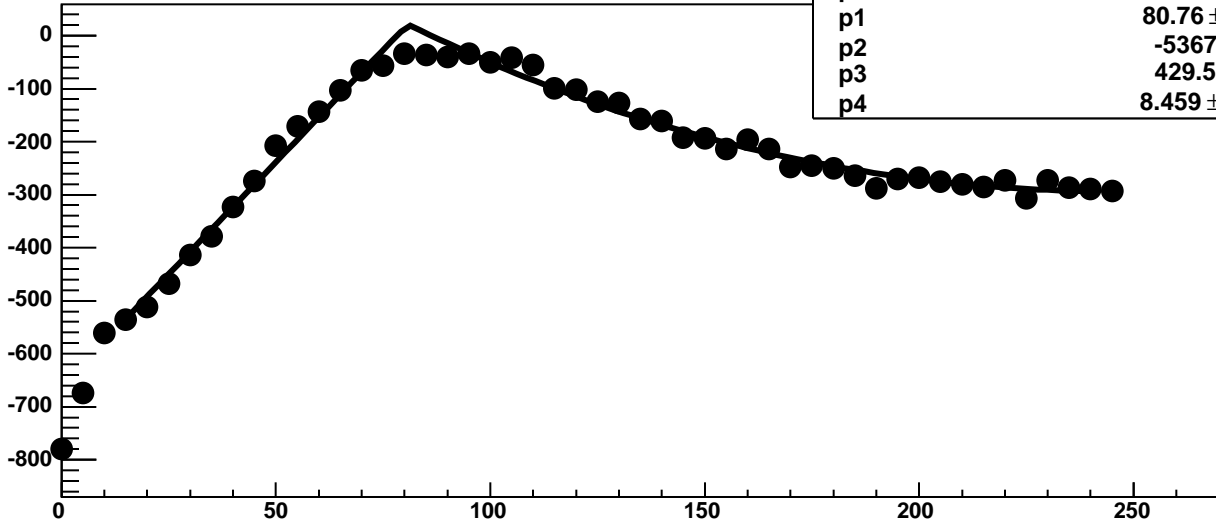
Chip 8, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

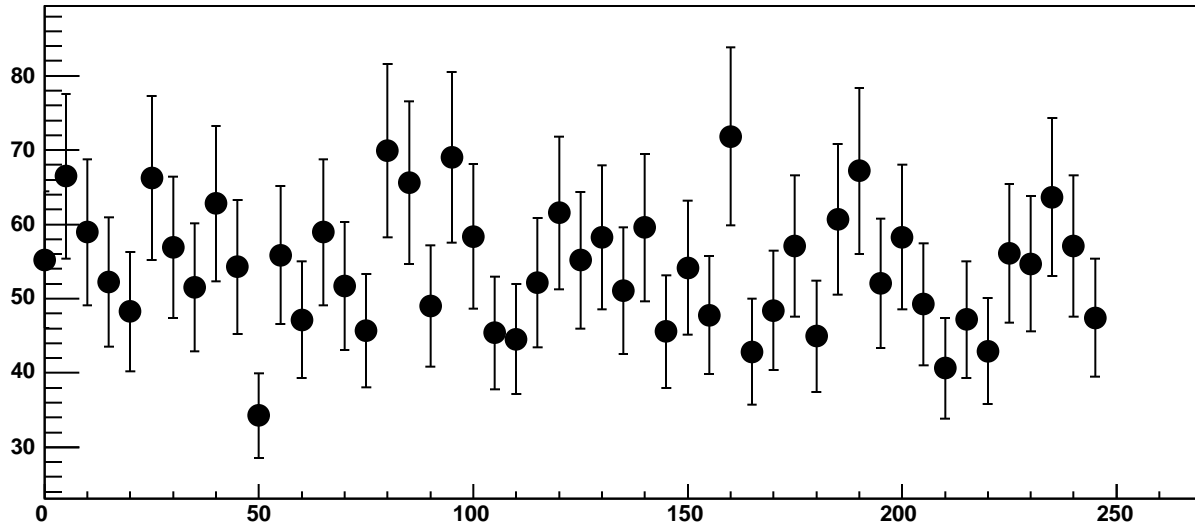


Chip 8, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold

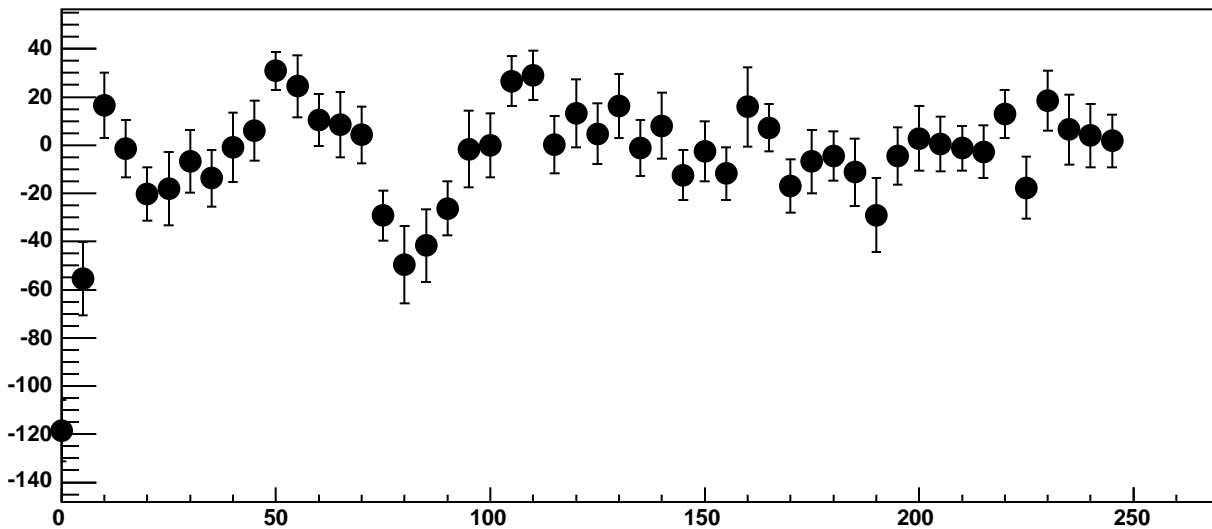


$\chi^2 / \text{ndf}$	92.49 / 41
p0	$21.89 \pm 5.37$
p1	$80.76 \pm 0.7638$
p2	$-5367 \pm 434.3$
p3	$429.5 \pm 39.94$
p4	$8.459 \pm 0.1636$

Chip 8, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

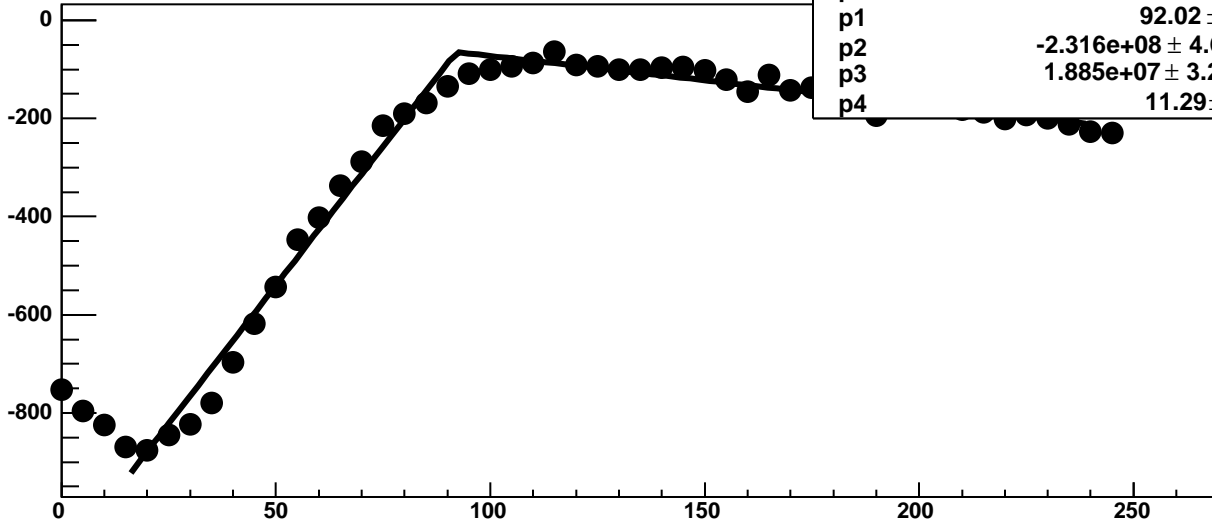


Chip 8, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold



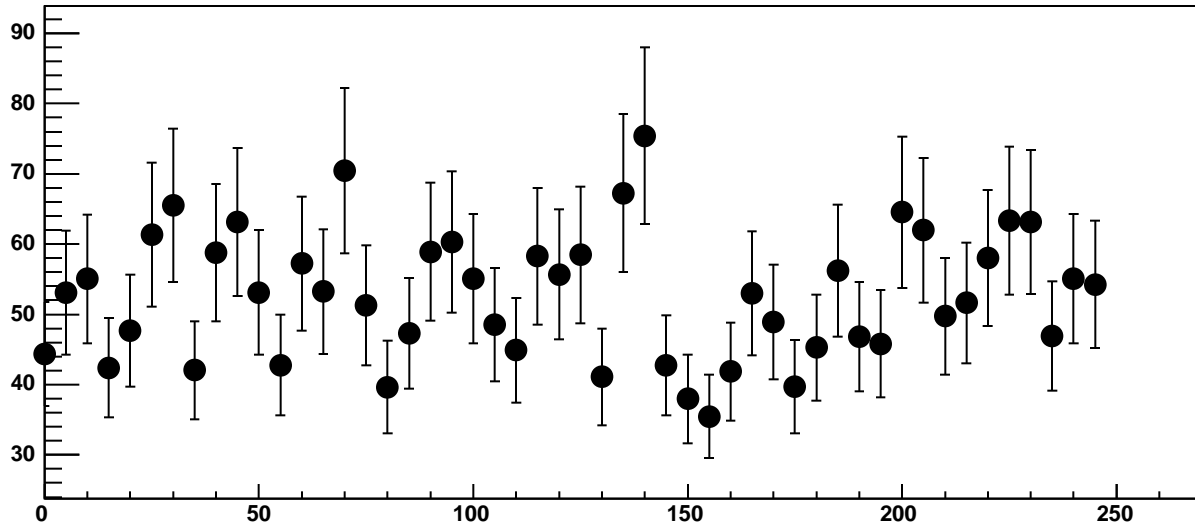


Chip 8, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

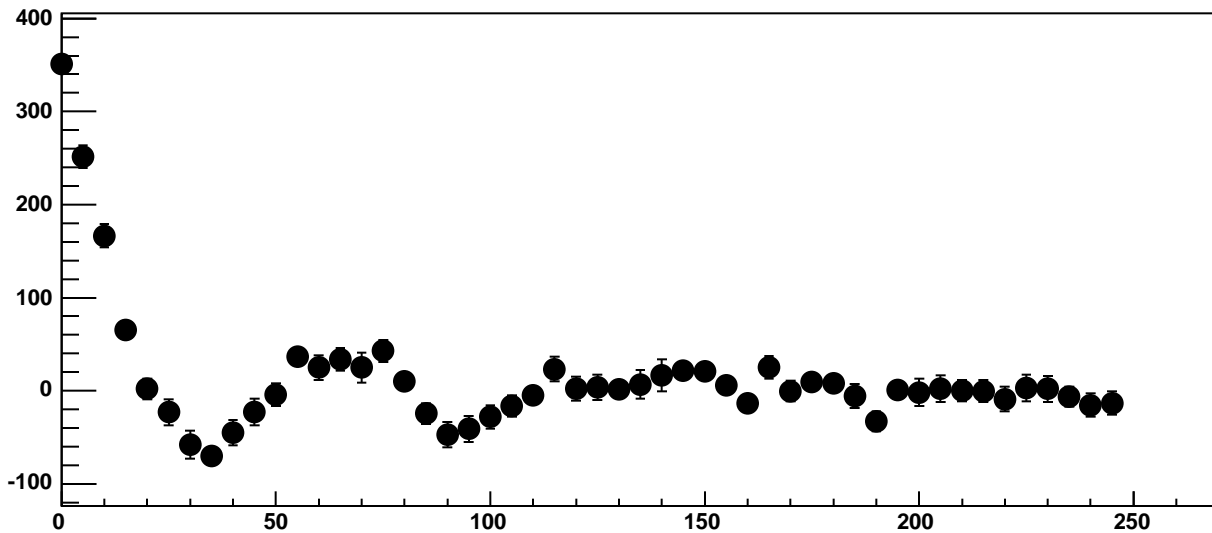


$\chi^2 / \text{ndf}$	239.4 / 41
p0	$-64.78 \pm 4.034$
p1	$92.02 \pm 0.5835$
p2	$-2.316\text{e}+08 \pm 4.648\text{e}+06$
p3	$1.885\text{e}+07 \pm 3.216\text{e}+05$
p4	$11.29 \pm 0.1228$

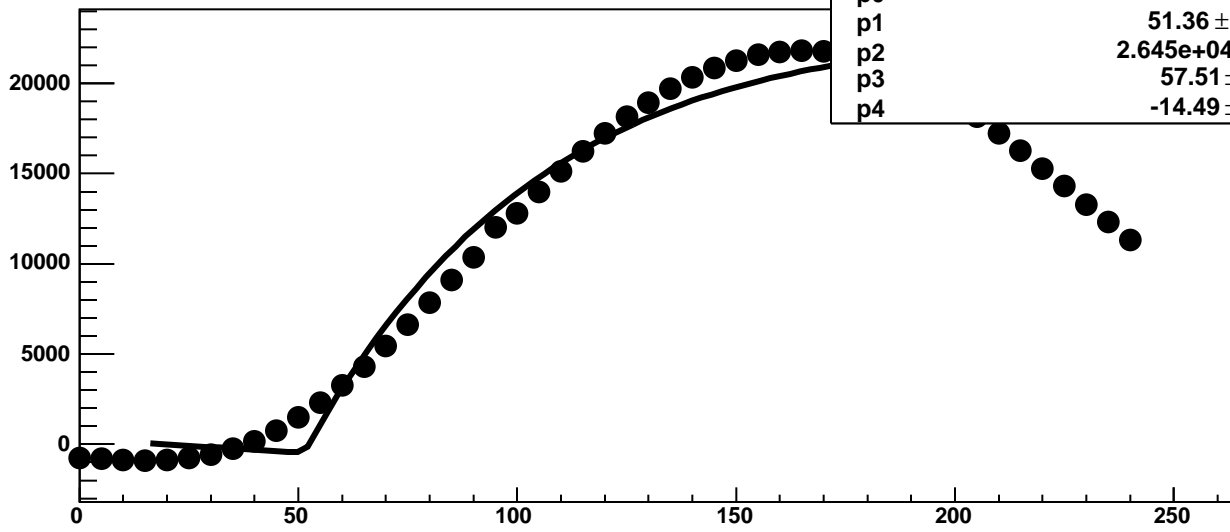
Chip 8, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

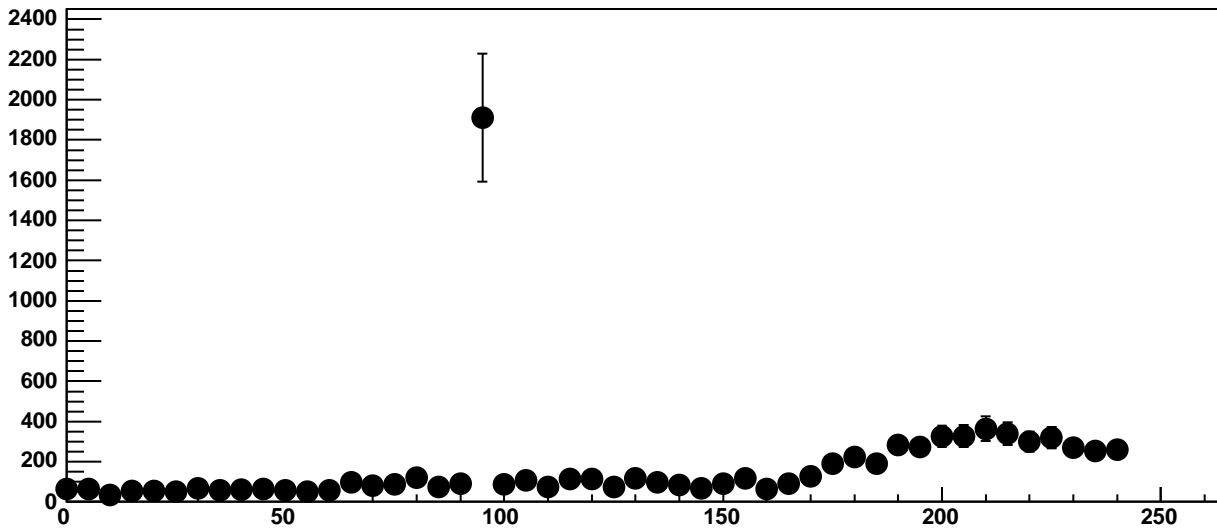


Chip 8, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

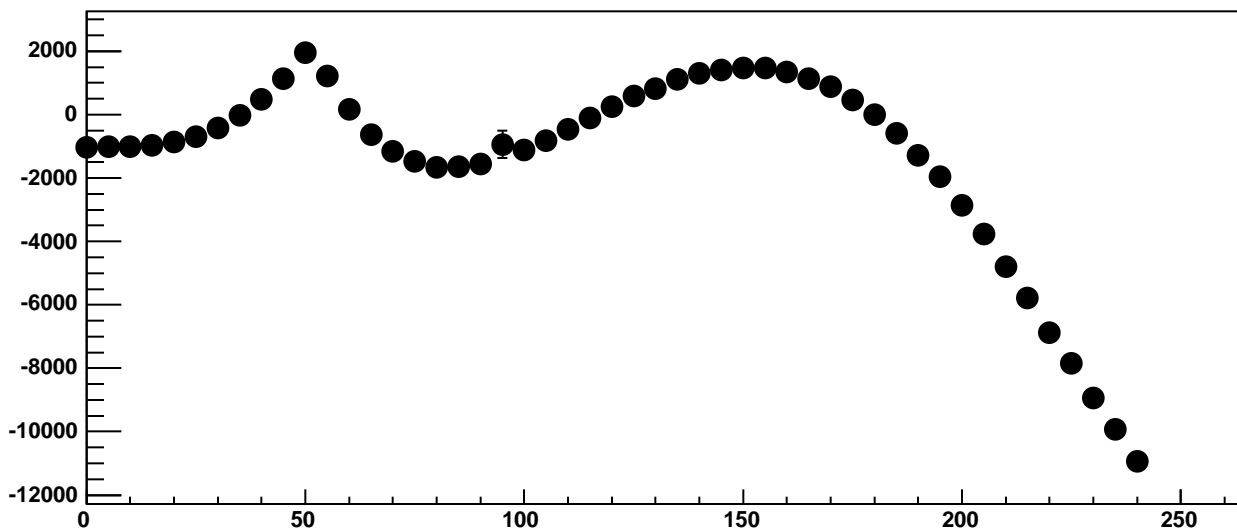


$\chi^2 / \text{ndf}$	2.445e+05 / 41
p0	-466.8 ± 7.496
p1	51.36 ± 0.02741
p2	2.645e+04 ± 60.58
p3	57.51 ± 0.1255
p4	-14.49 ± 0.3025

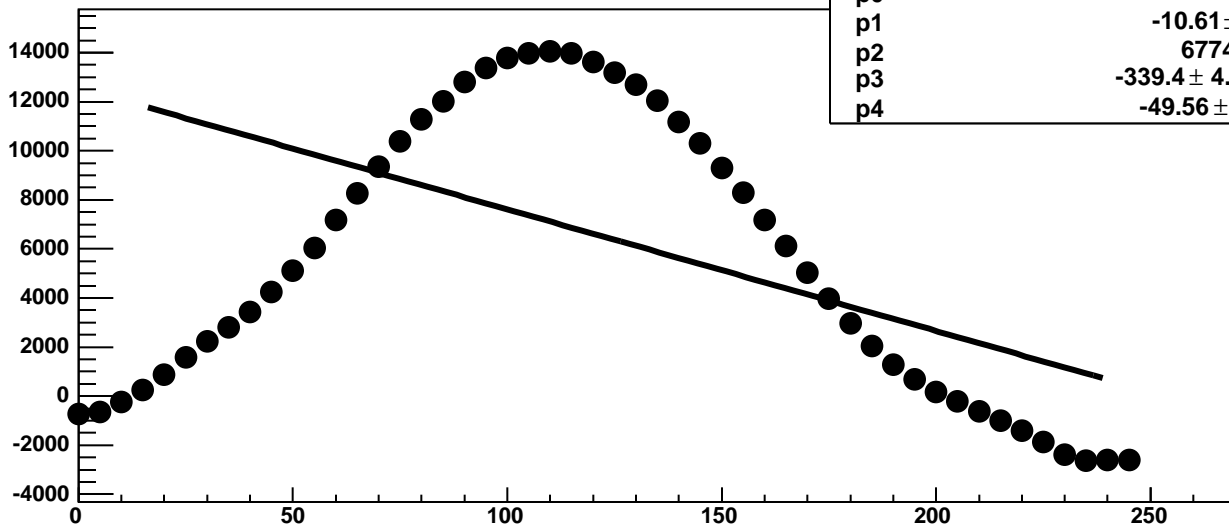
Chip 8, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

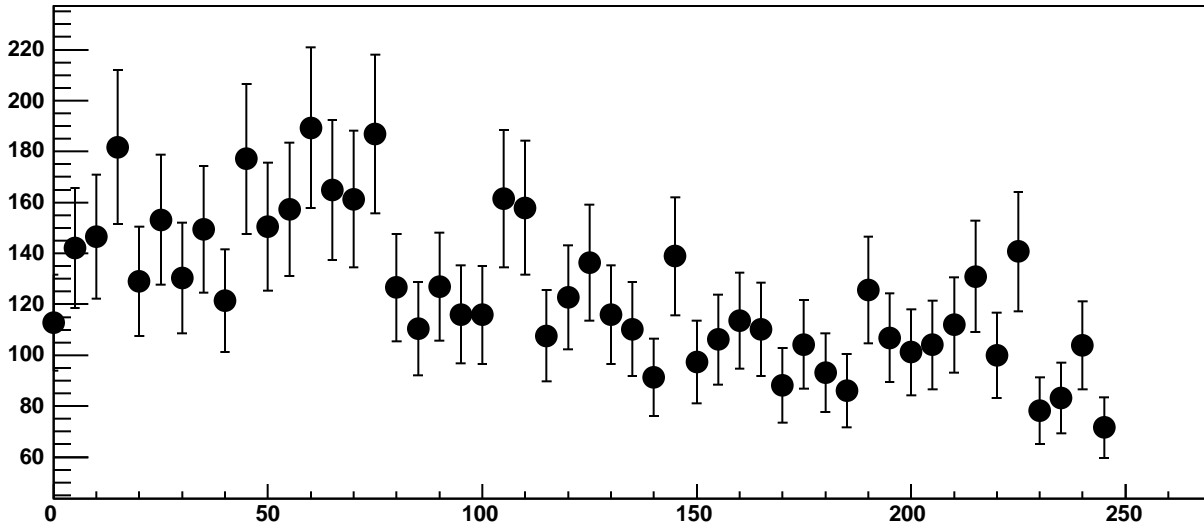


Chip 8, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold

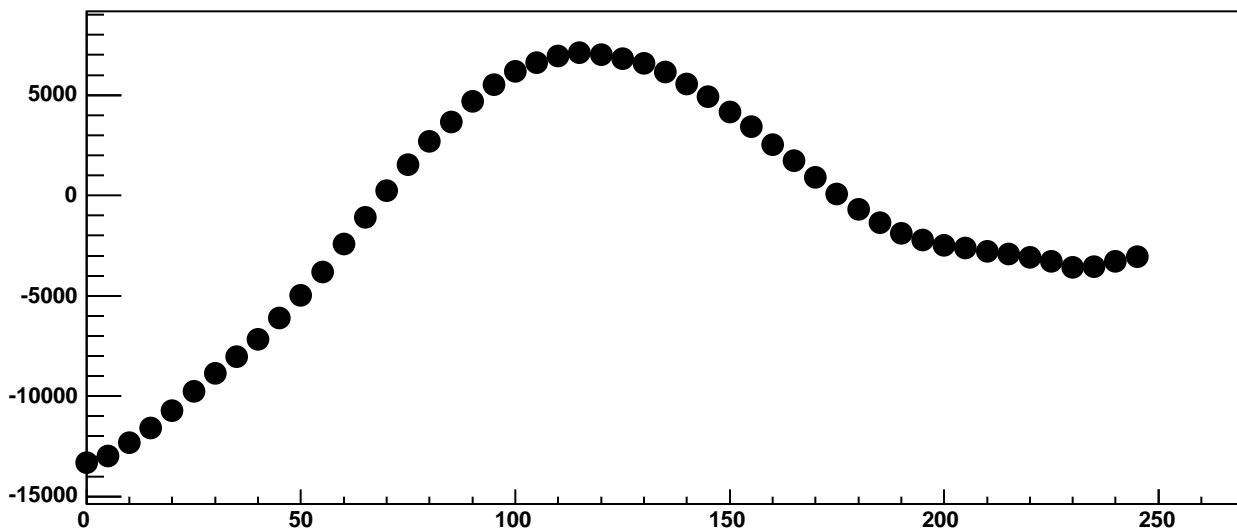


$\chi^2 / \text{ndf}$	1.436e+06 / 41
p0	6322 ± 4.724
p1	-10.61 ± 0.1206
p2	6774 ± 5.131
p3	-339.4 ± 4.845e-06
p4	-49.56 ± 0.06112

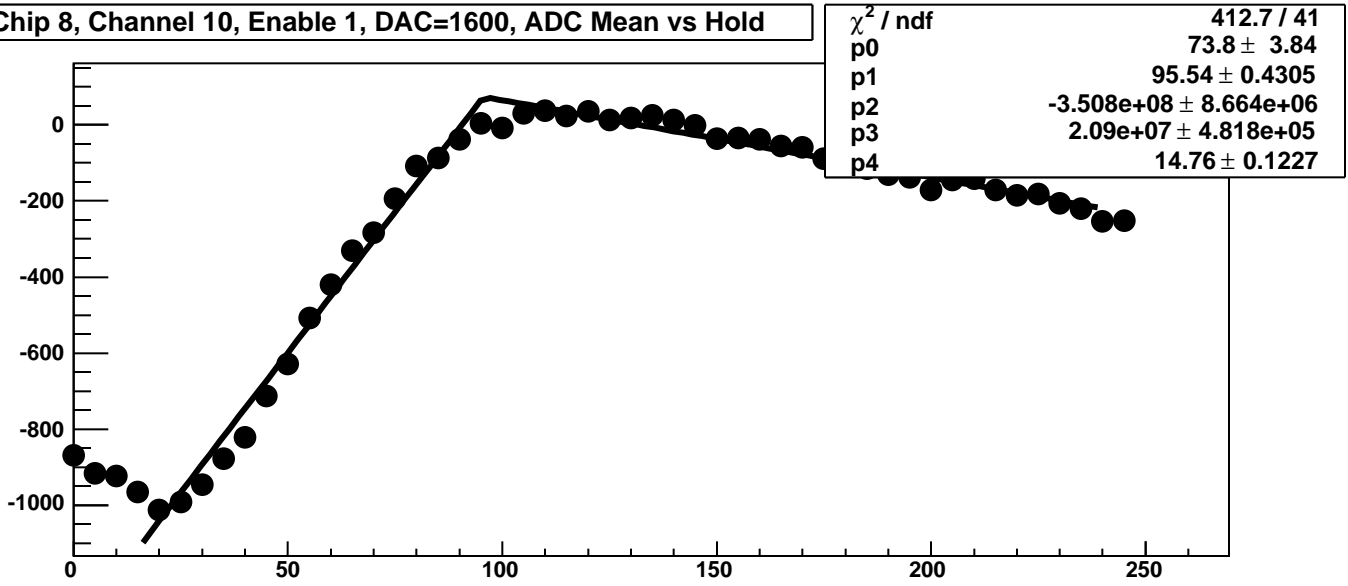
Chip 8, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



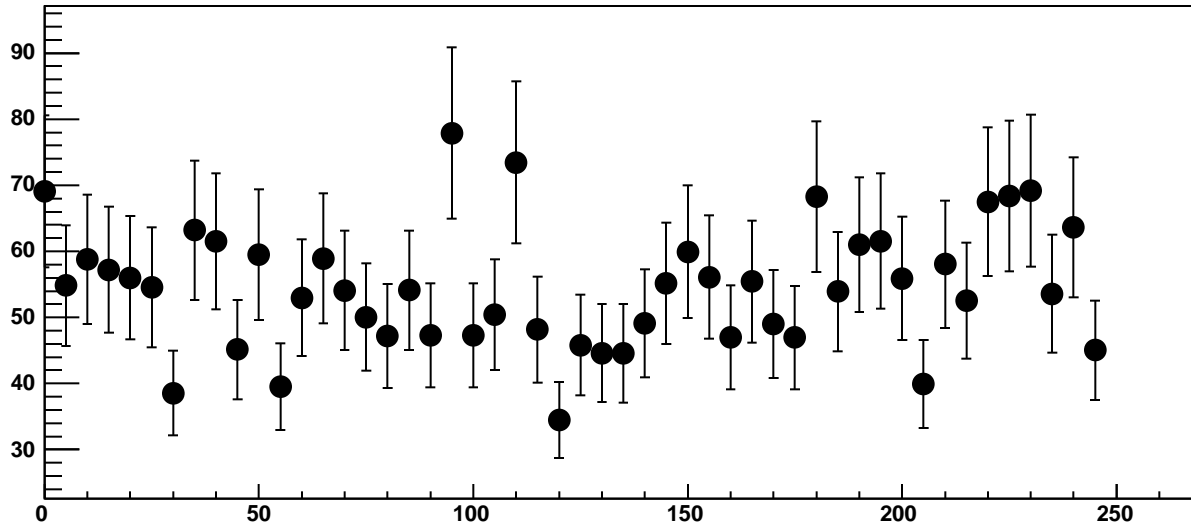
Chip 8, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold



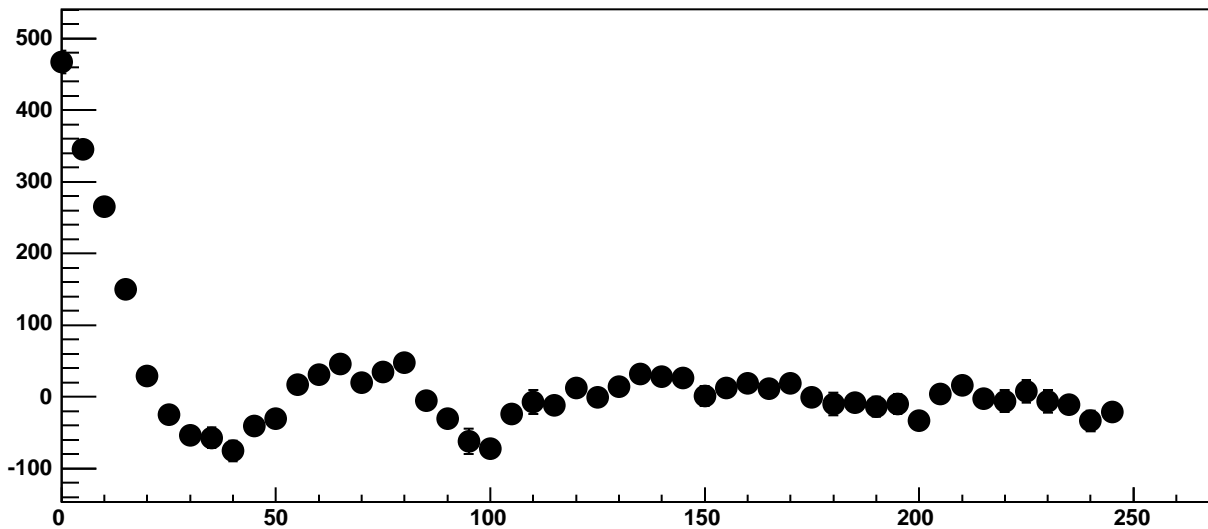
Chip 8, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold



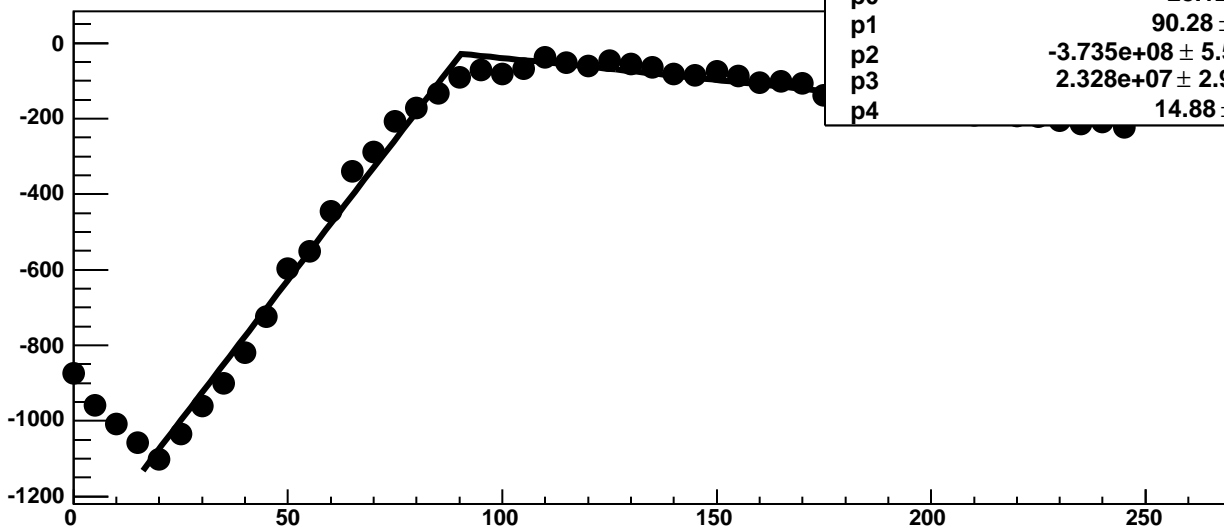
Chip 8, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

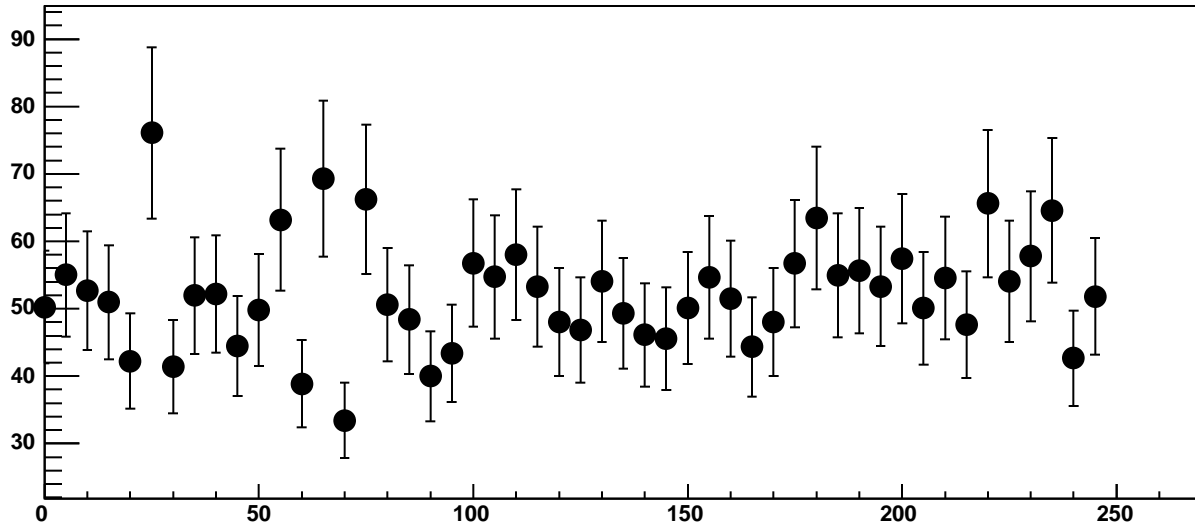


Chip 8, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

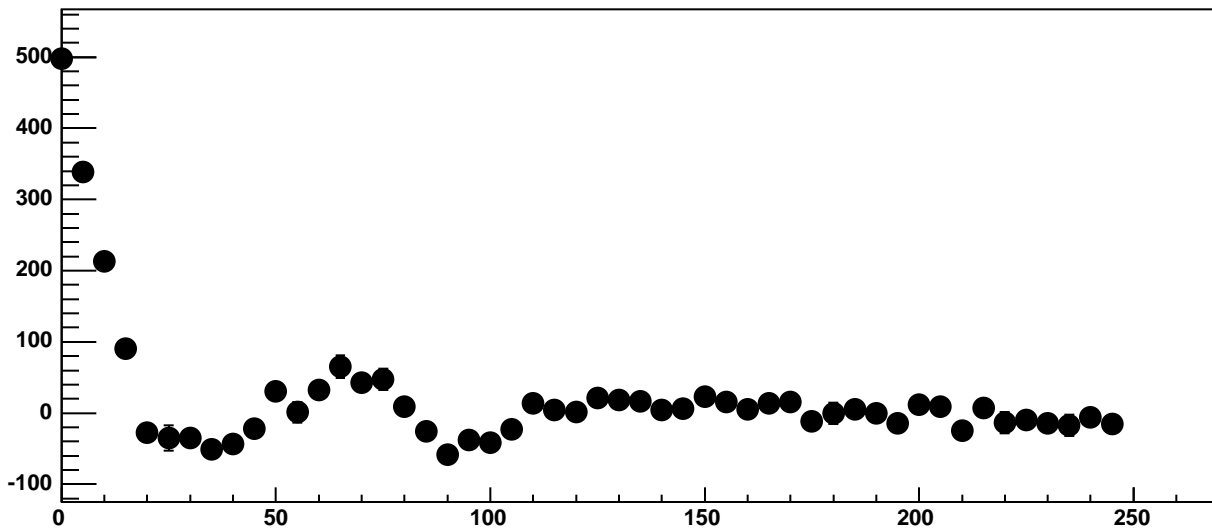


$\chi^2 / \text{ndf}$	305.4 / 41
p0	$-28.12 \pm 4.043$
p1	$90.28 \pm 0.4144$
p2	$-3.735e+08 \pm 5.563e+06$
p3	$2.328e+07 \pm 2.933e+05$
p4	$14.88 \pm 0.1172$

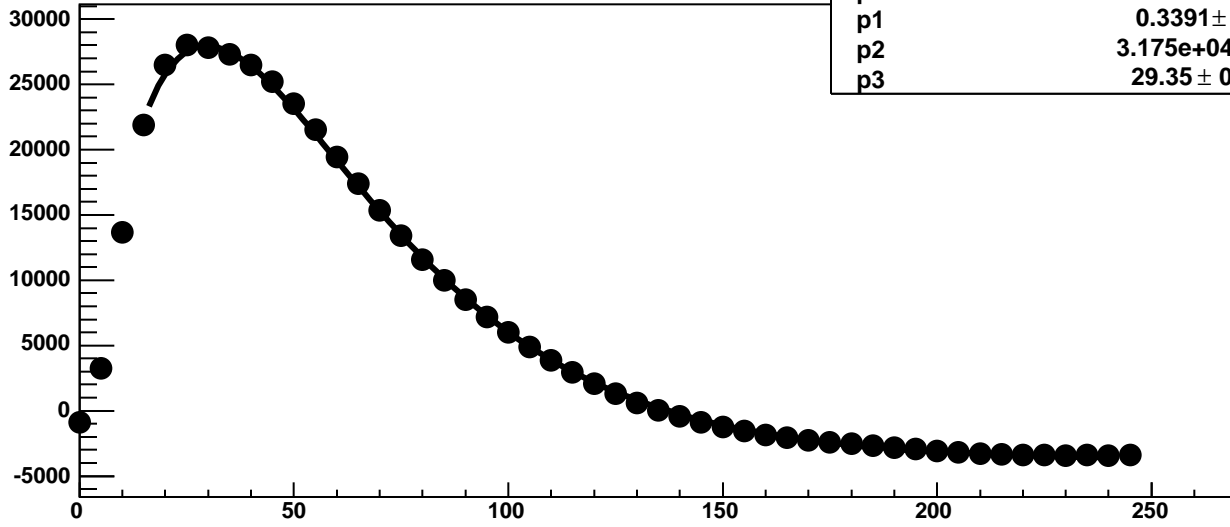
Chip 8, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

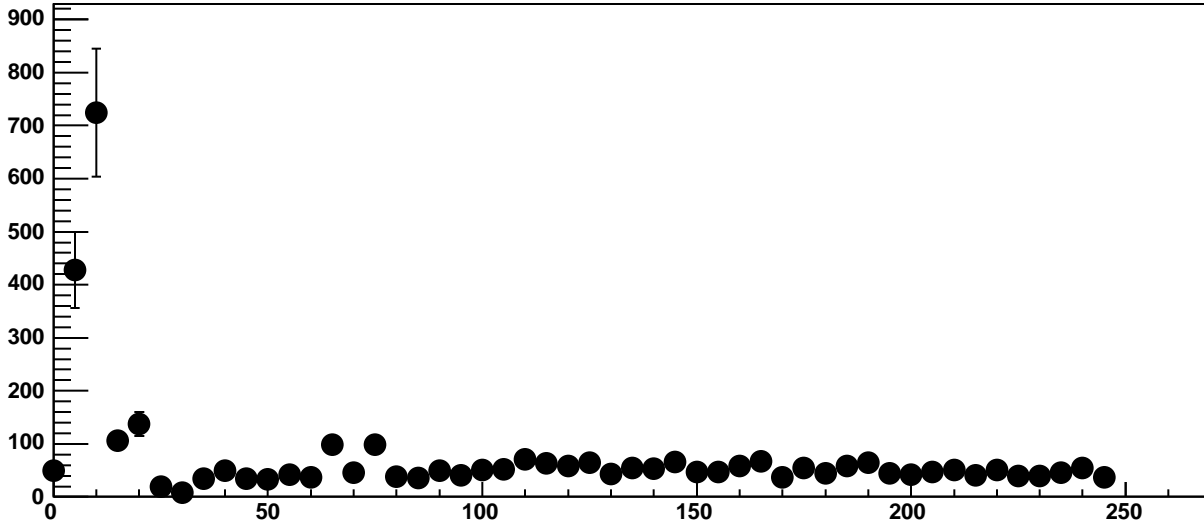


Chip 8, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold

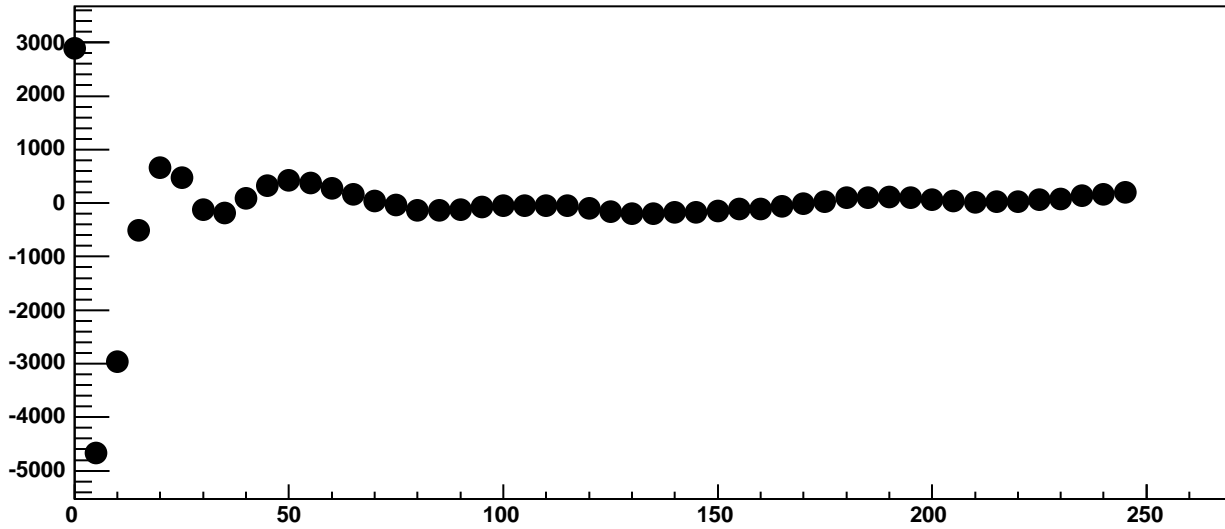


$\chi^2 / \text{ndf}$	2.785e+04 / 42
p0	-3787 ± 3.078
p1	0.3391 ± 0.01823
p2	3.175e+04 ± 3.356
p3	29.35 ± 0.009435

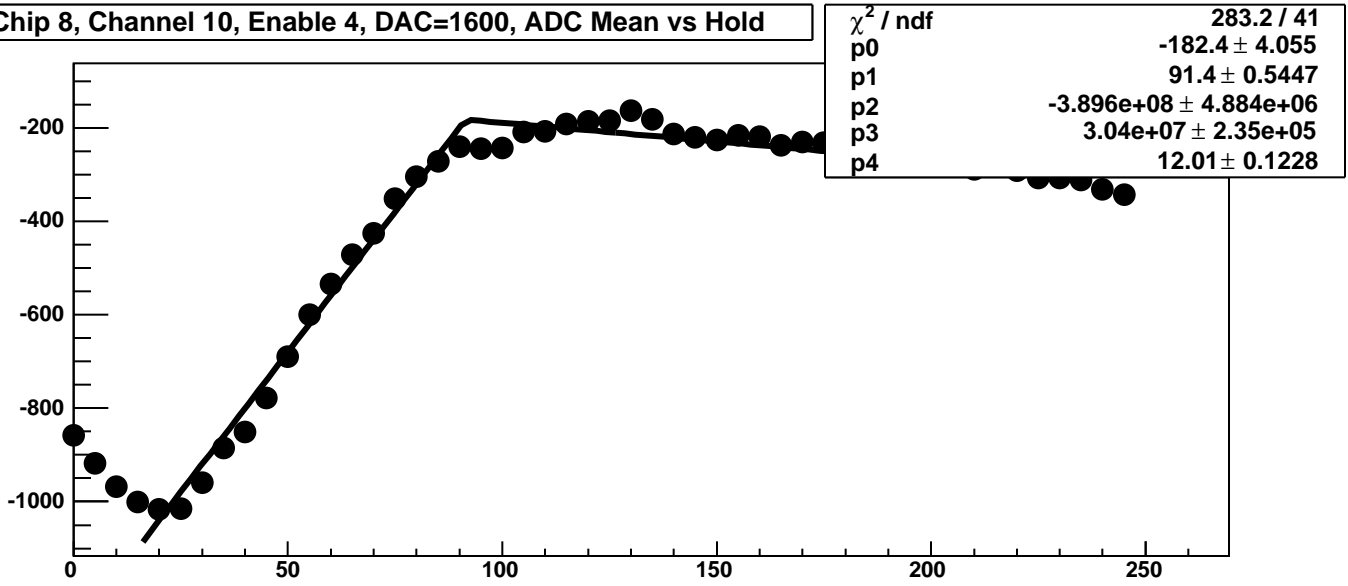
Chip 8, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



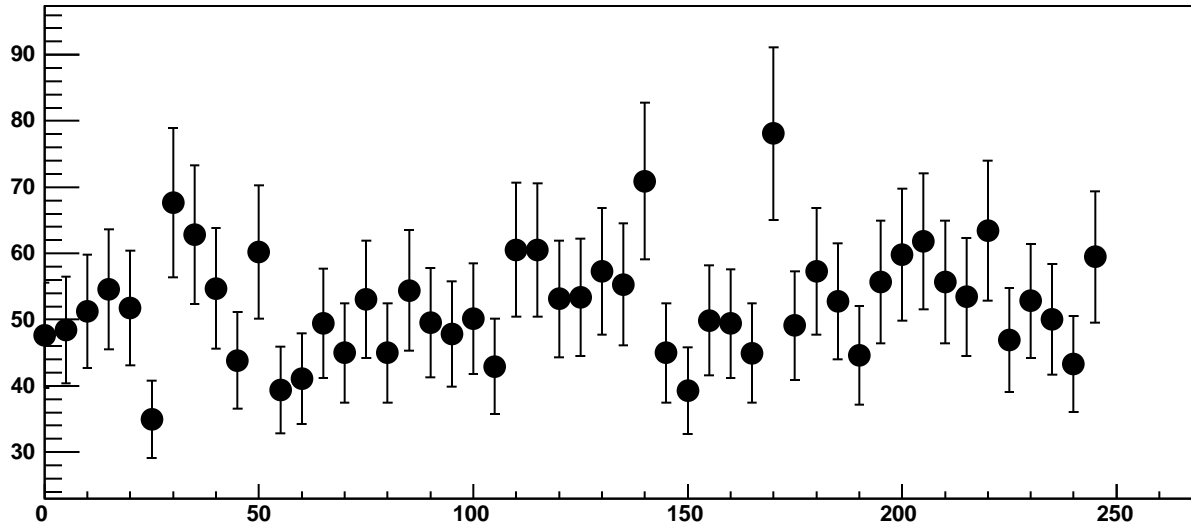
Chip 8, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold



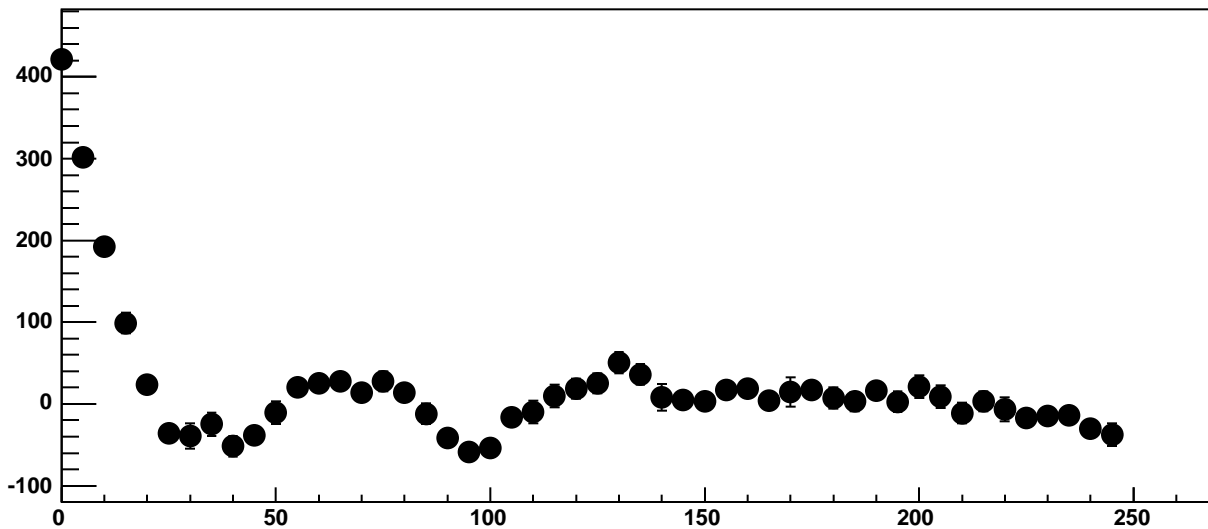
Chip 8, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold



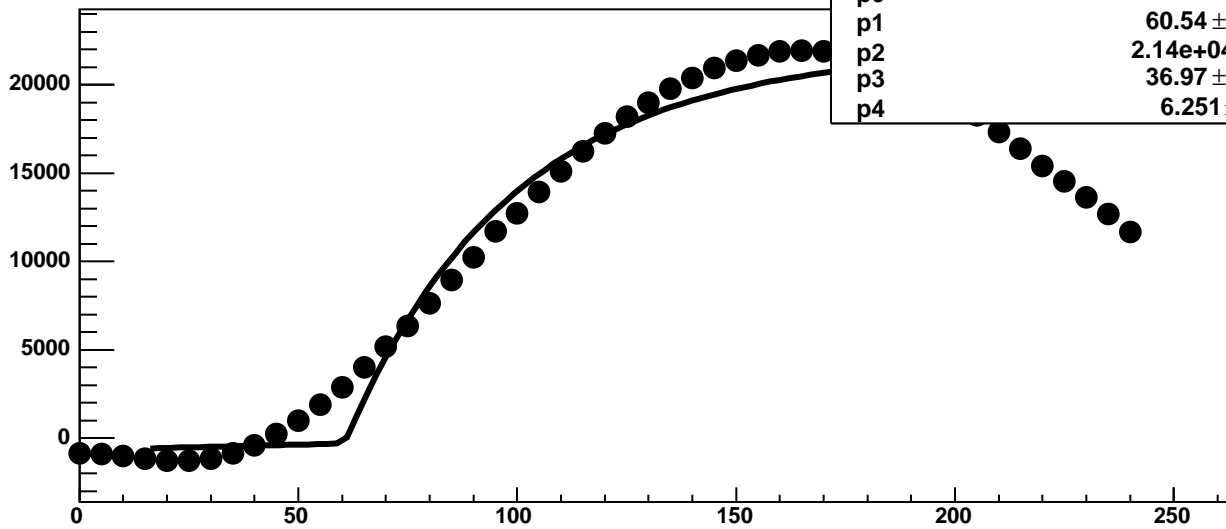
Chip 8, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

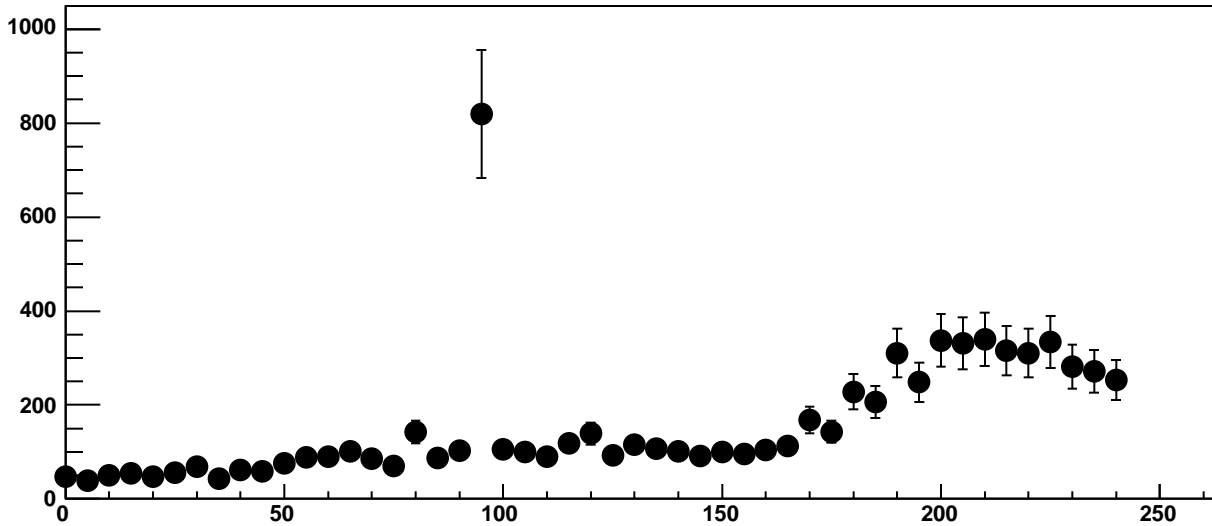


Chip 8, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

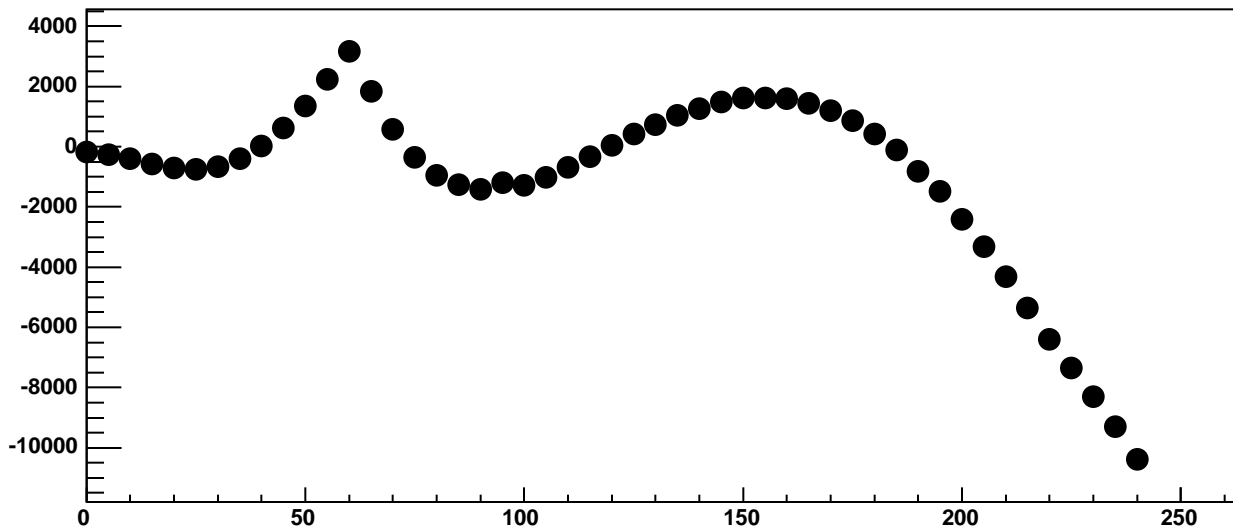


$\chi^2 / \text{ndf}$	2.095e+05 / 41
p0	-300.5 ± 8.228
p1	60.54 ± 0.03503
p2	2.14e+04 ± 42.15
p3	36.97 ± 0.09189
p4	6.251 ± 0.2524

Chip 8, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold

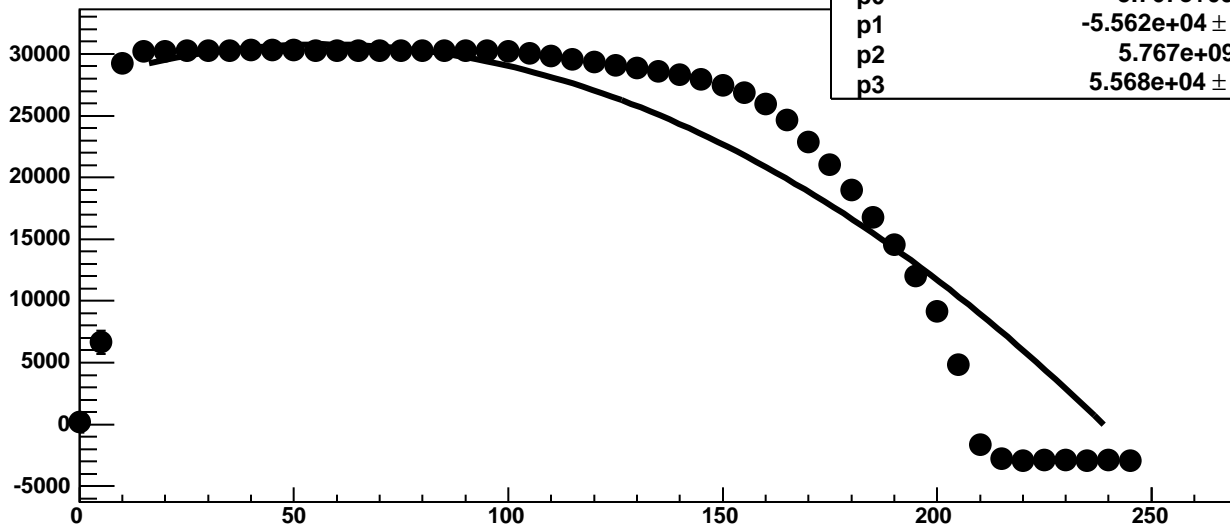


Chip 8, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



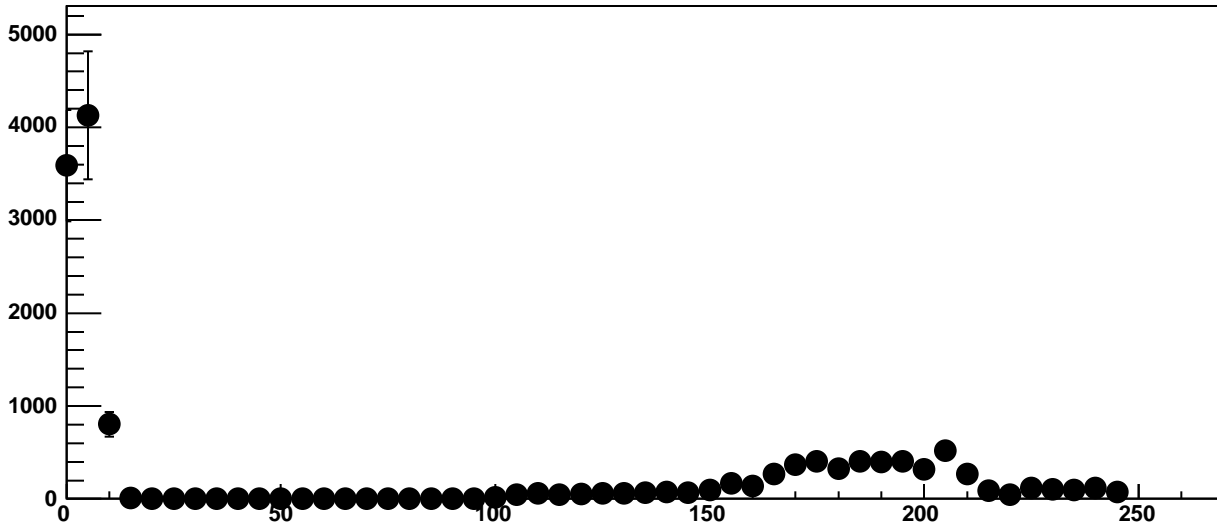


Chip 8, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold

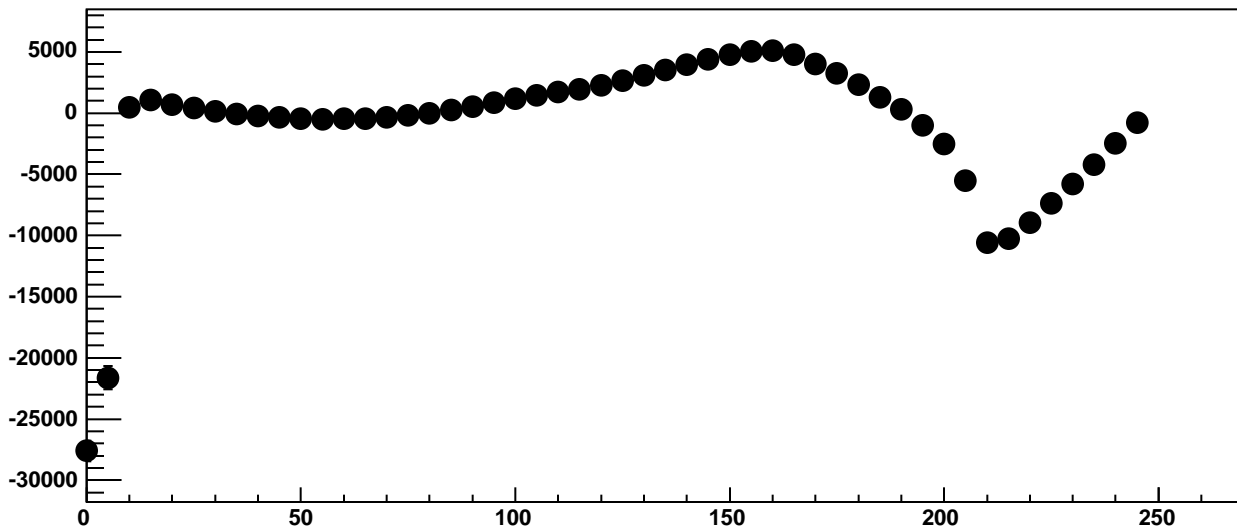


$\chi^2 / \text{ndf}$	4.198e+06 / 42
p0	-5.767e+09 $\pm$ 3.919
p1	-5.562e+04 $\pm$ 0.07845
p2	5.767e+09 $\pm$ 3.919
p3	5.568e+04 $\pm$ 0.07843

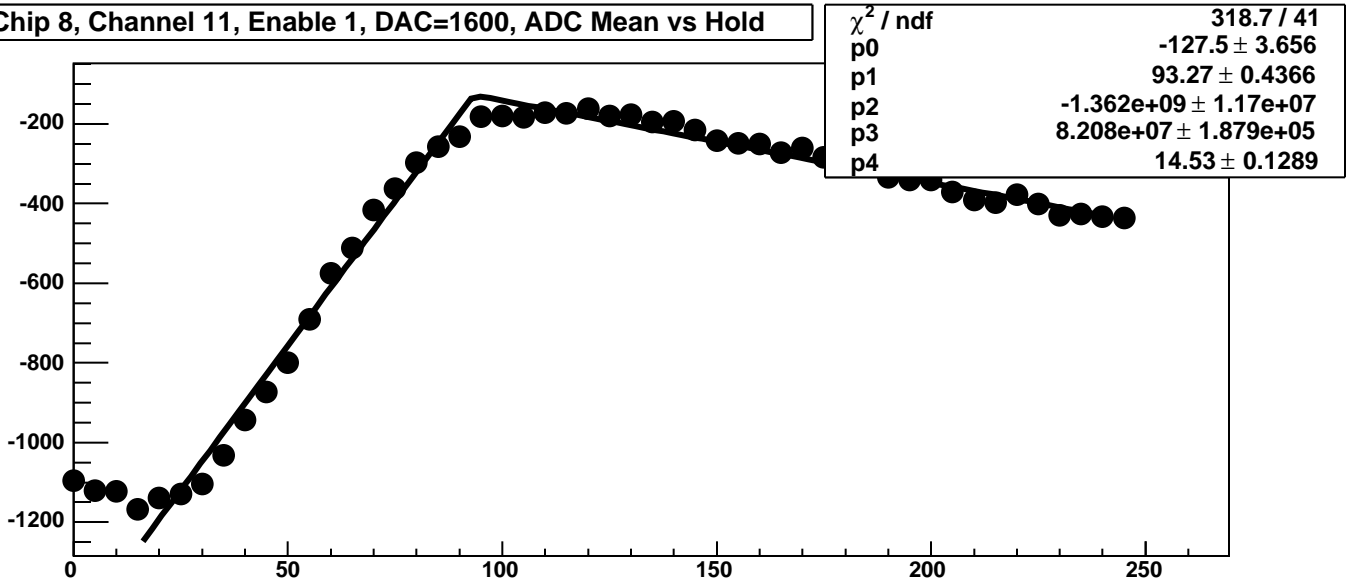
Chip 8, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



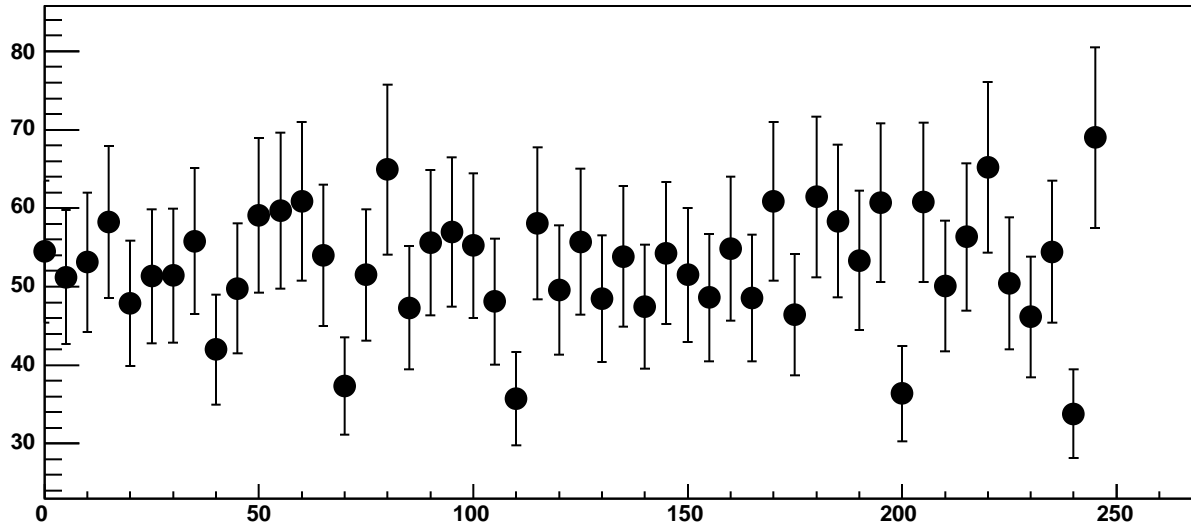
Chip 8, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold



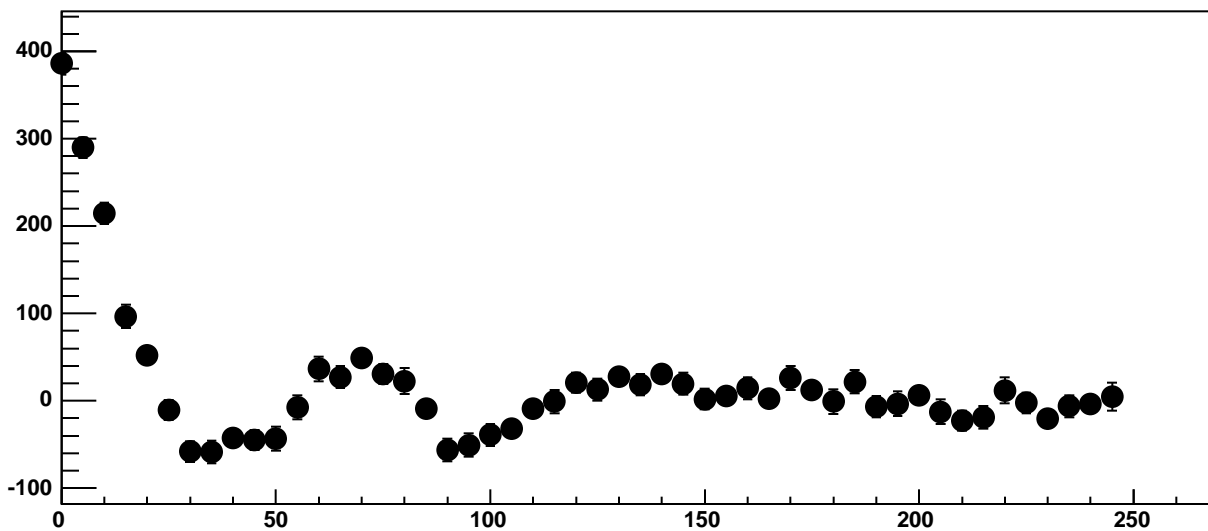
Chip 8, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold



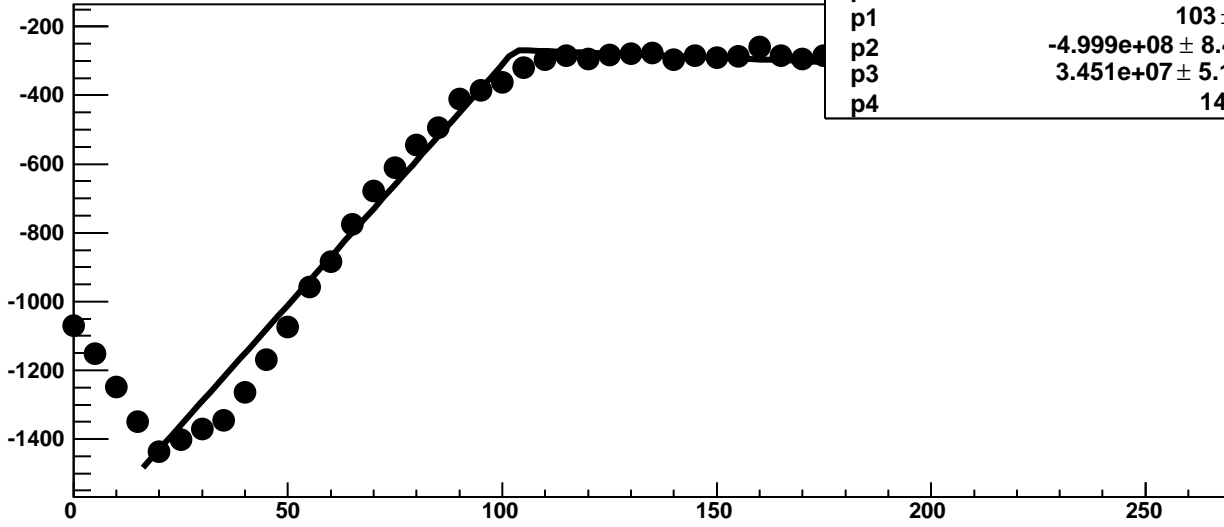
Chip 8, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

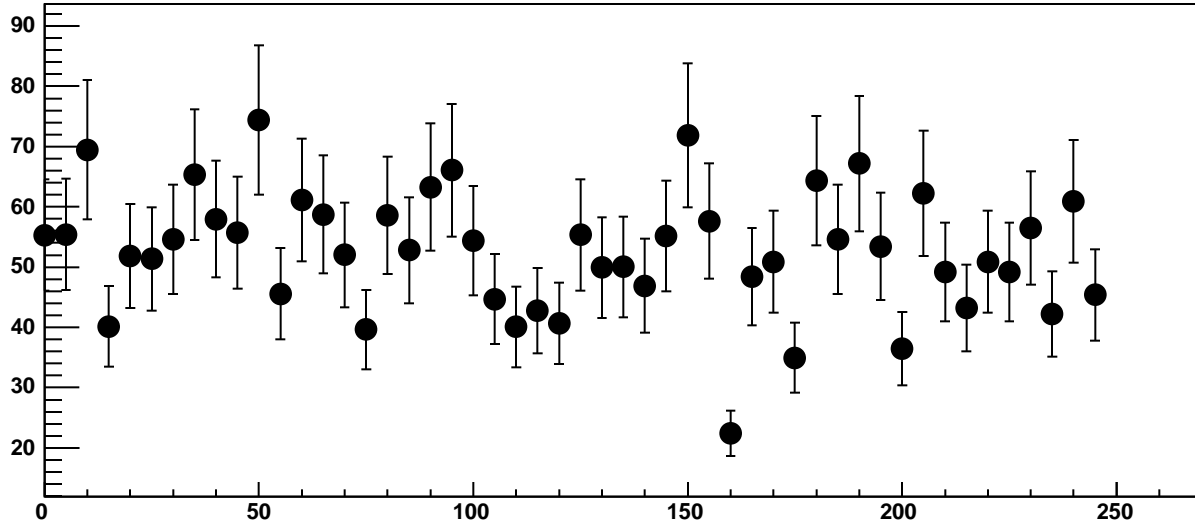


Chip 8, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

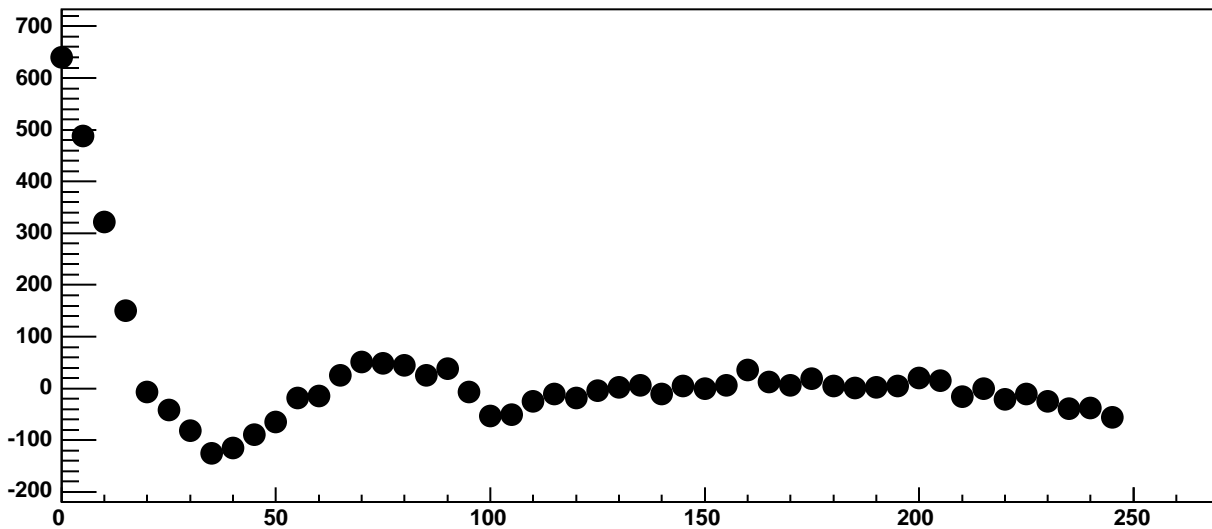


$\chi^2 / \text{ndf}$	760.3 / 41
p0	$-267.8 \pm 3.763$
p1	$103 \pm 0.4903$
p2	$-4.999\text{e}+08 \pm 8.443\text{e}+06$
p3	$3.451\text{e}+07 \pm 5.131\text{e}+05$
p4	$14 \pm 0.109$

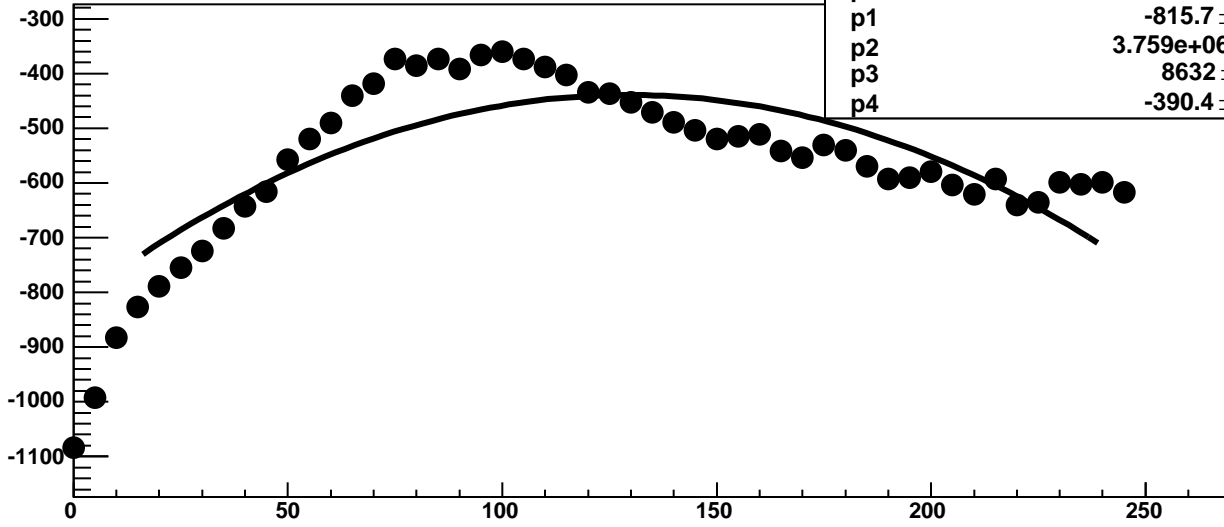
Chip 8, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



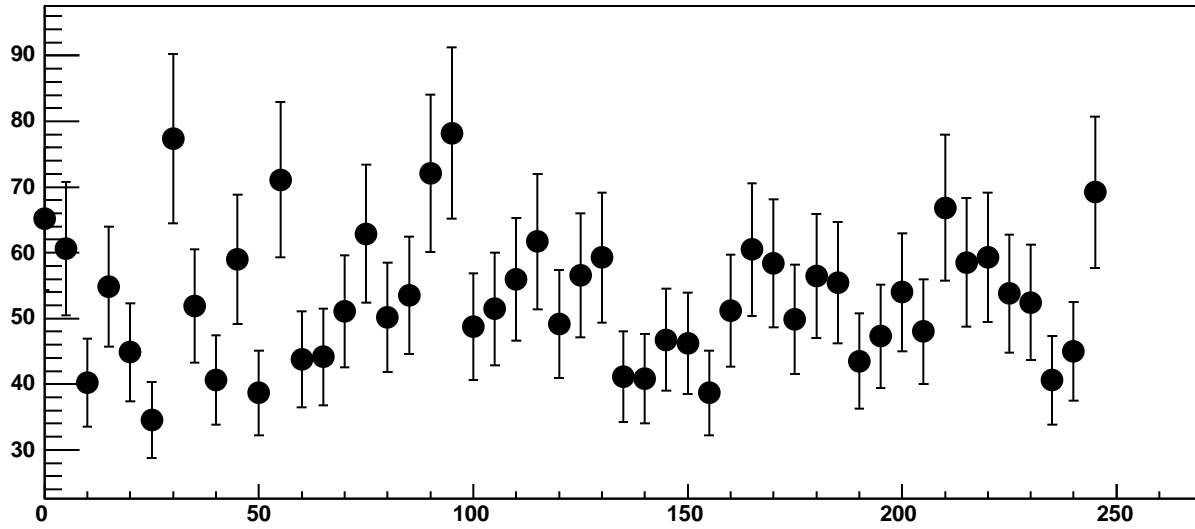
Chip 8, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold



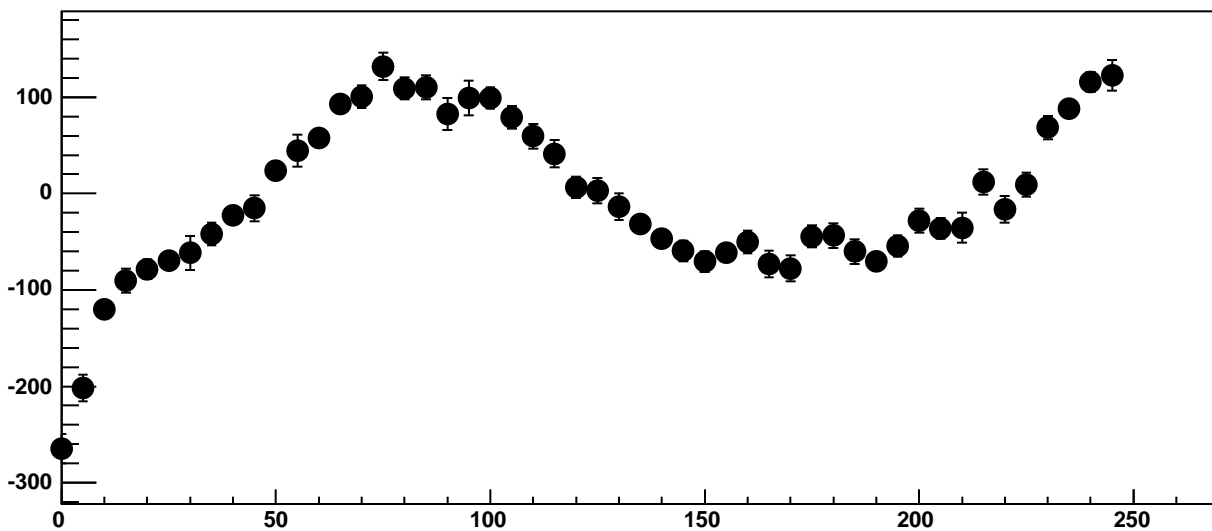
Chip 8, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold



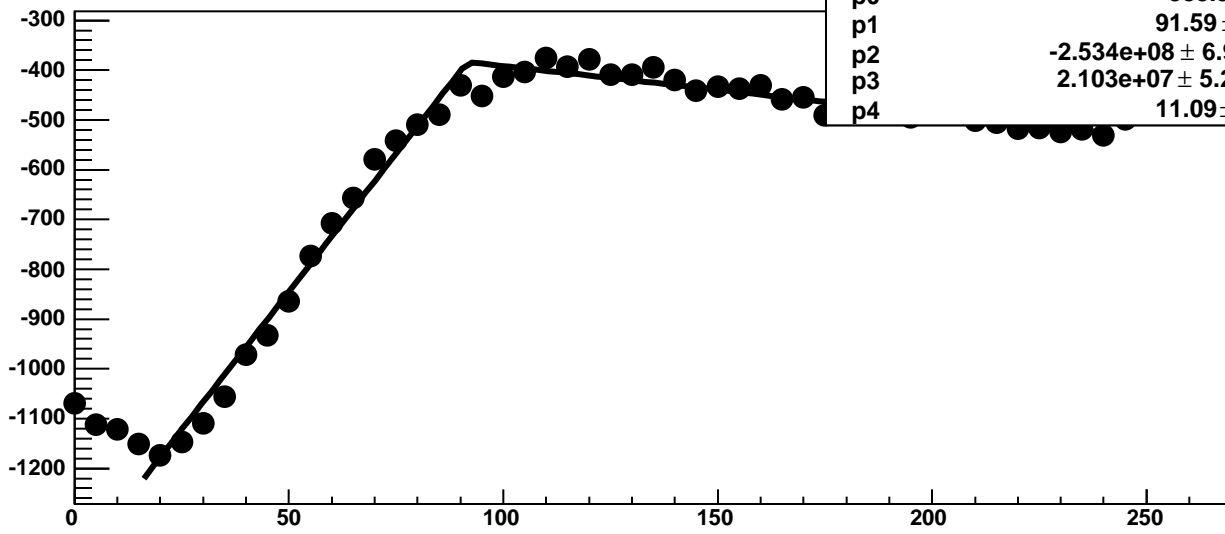
Chip 8, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

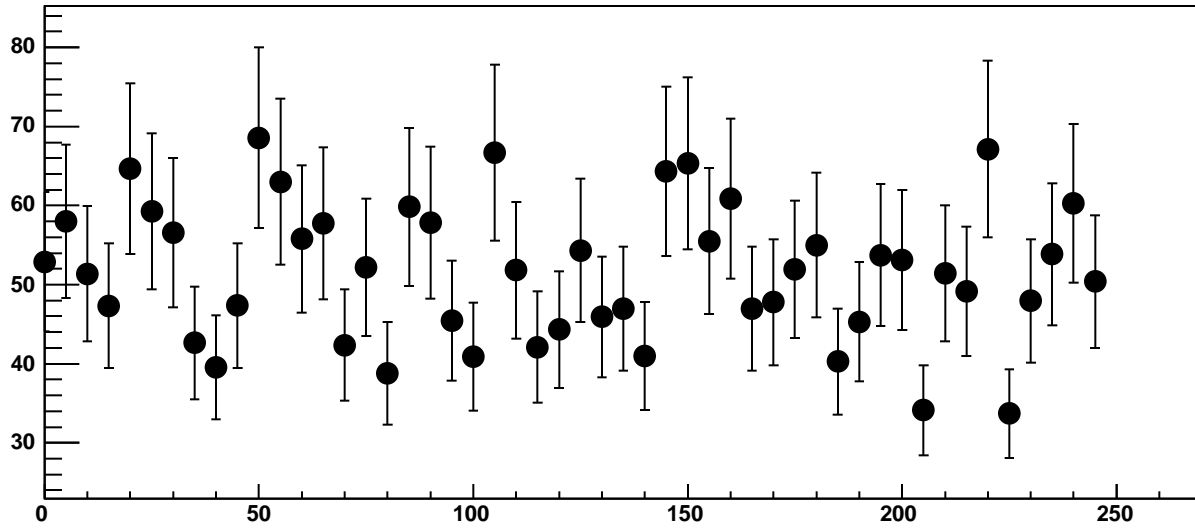


Chip 8, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

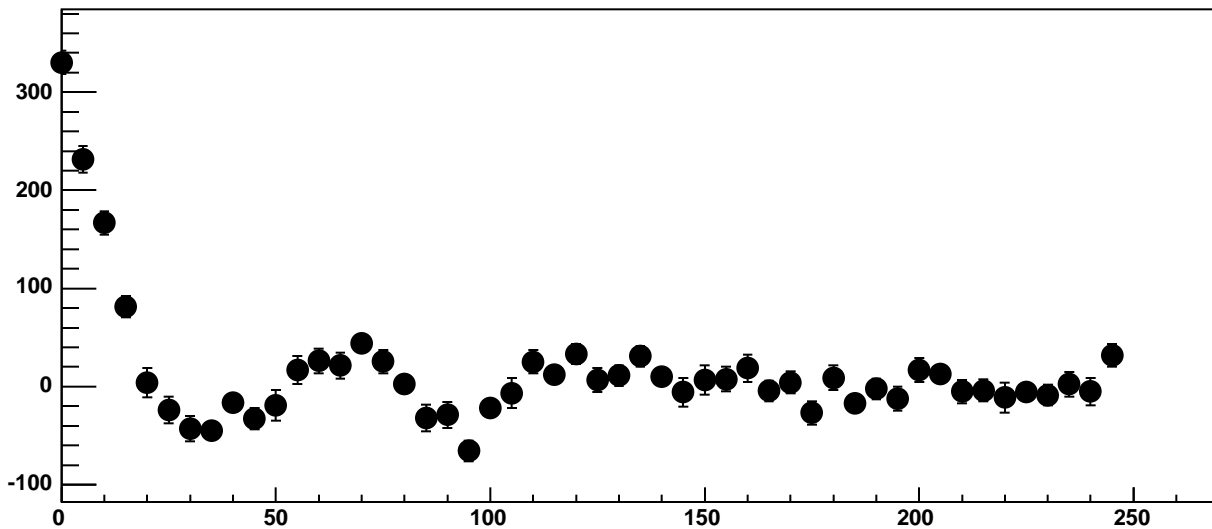


$\chi^2 / \text{ndf}$	241.4 / 41
p0	$-383.5 \pm 3.766$
p1	$91.59 \pm 0.5857$
p2	$-2.534\text{e}+08 \pm 6.948\text{e}+06$
p3	$2.103\text{e}+07 \pm 5.218\text{e}+05$
p4	$11.09 \pm 0.1285$

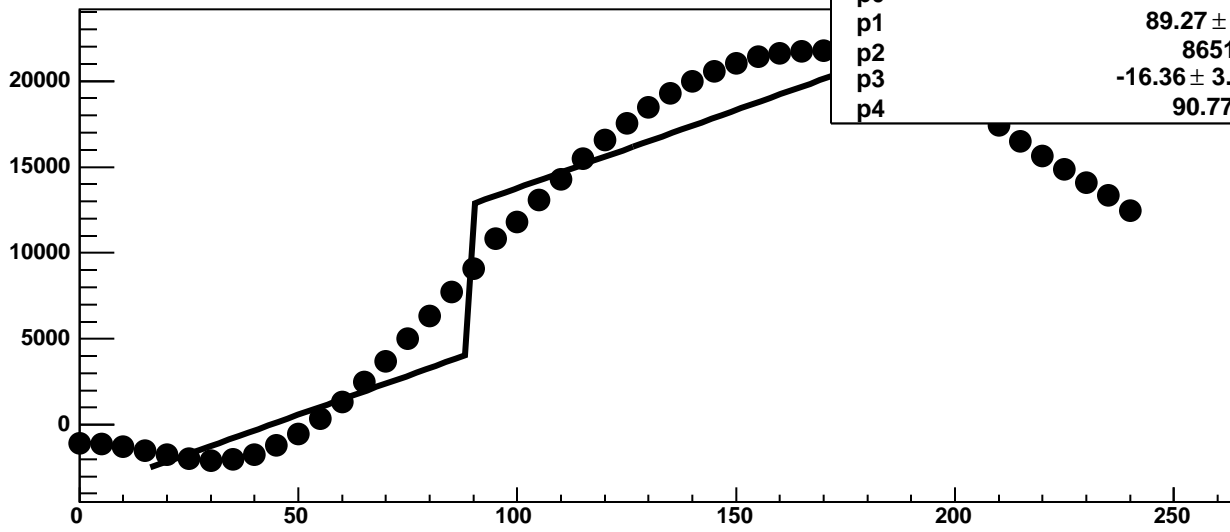
Chip 8, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

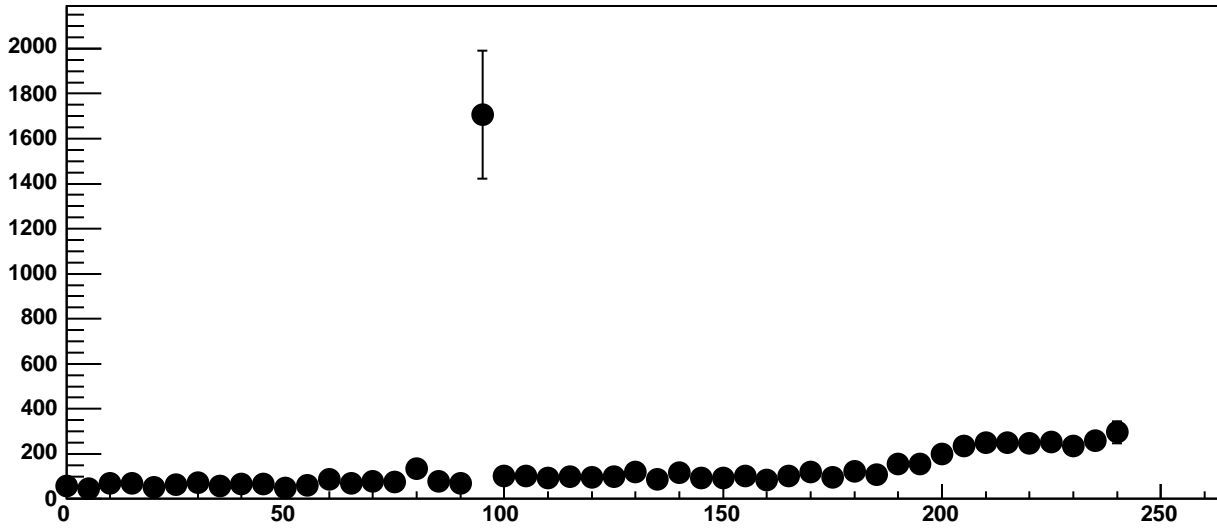


Chip 8, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

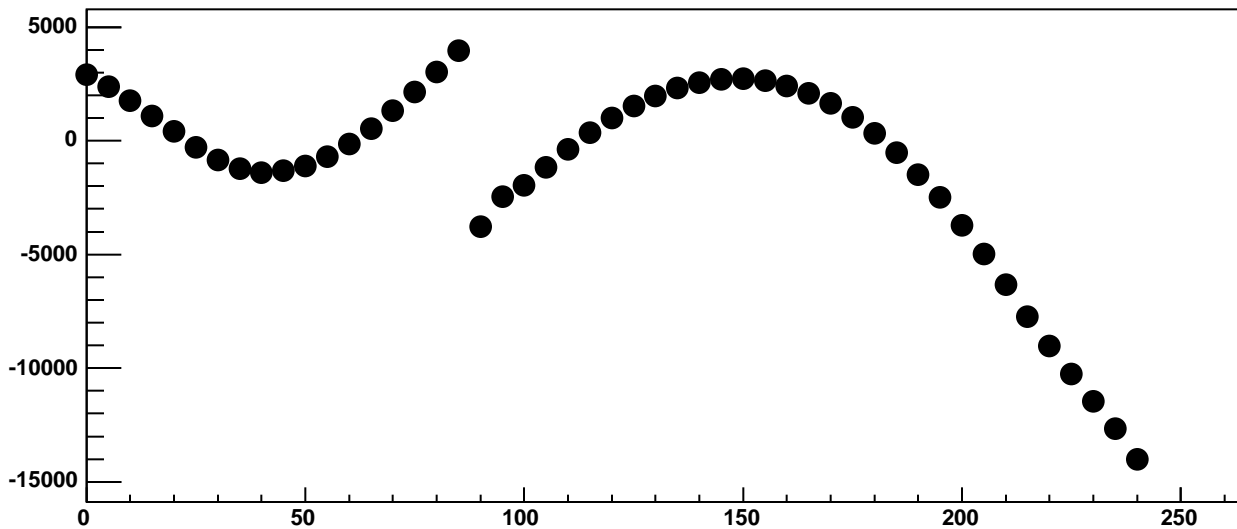


$\chi^2 / \text{ndf}$	5.41e+05 / 41
p0	4149 ± 6.254
p1	89.27 ± 0.06437
p2	8651 ± 15.04
p3	-16.36 ± 3.268e-05
p4	90.77 ± 0.125

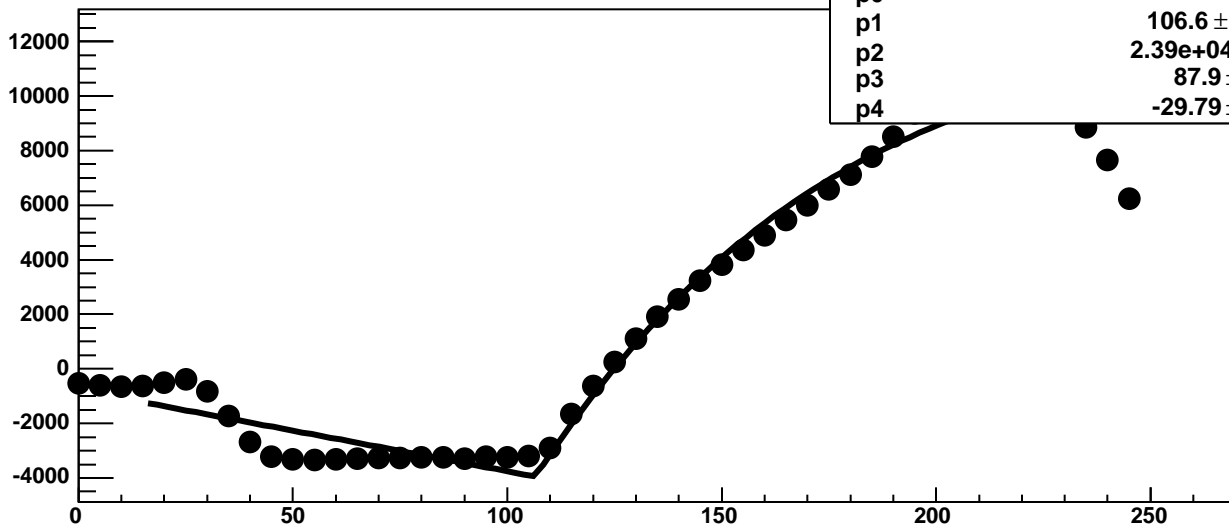
Chip 8, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



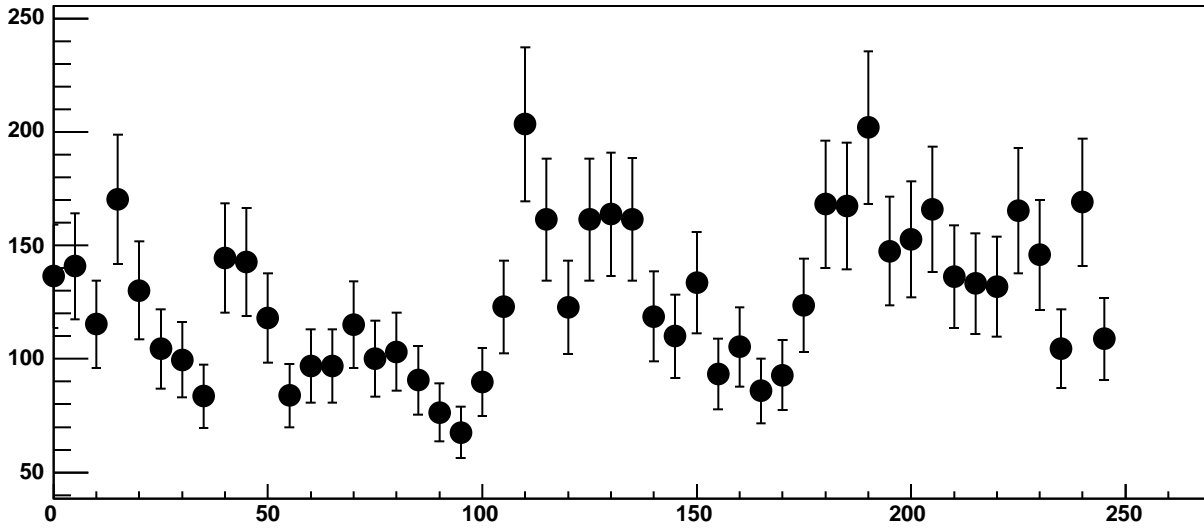
Chip 8, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



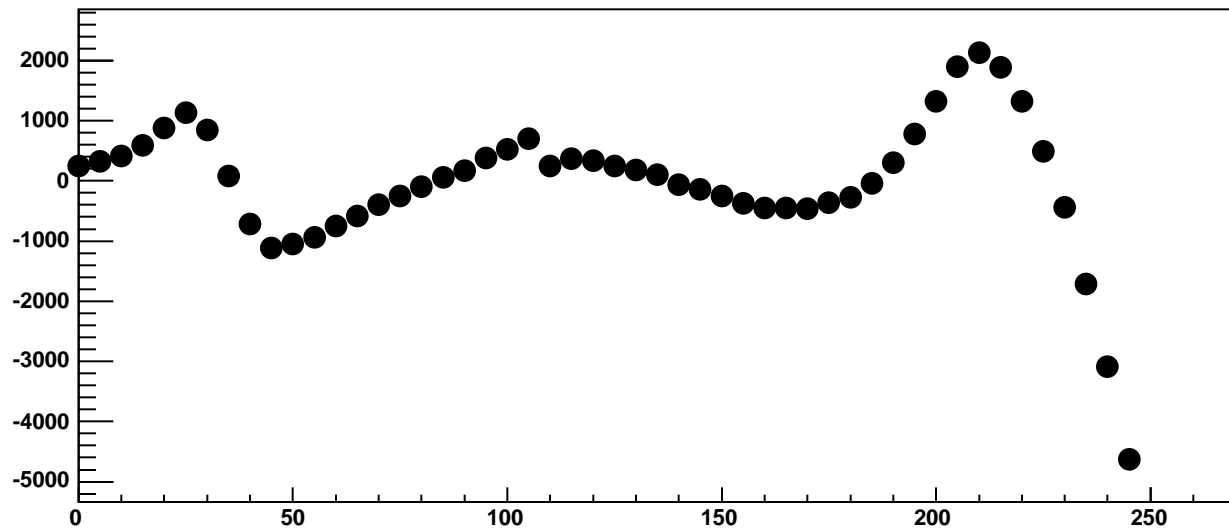
Chip 8, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



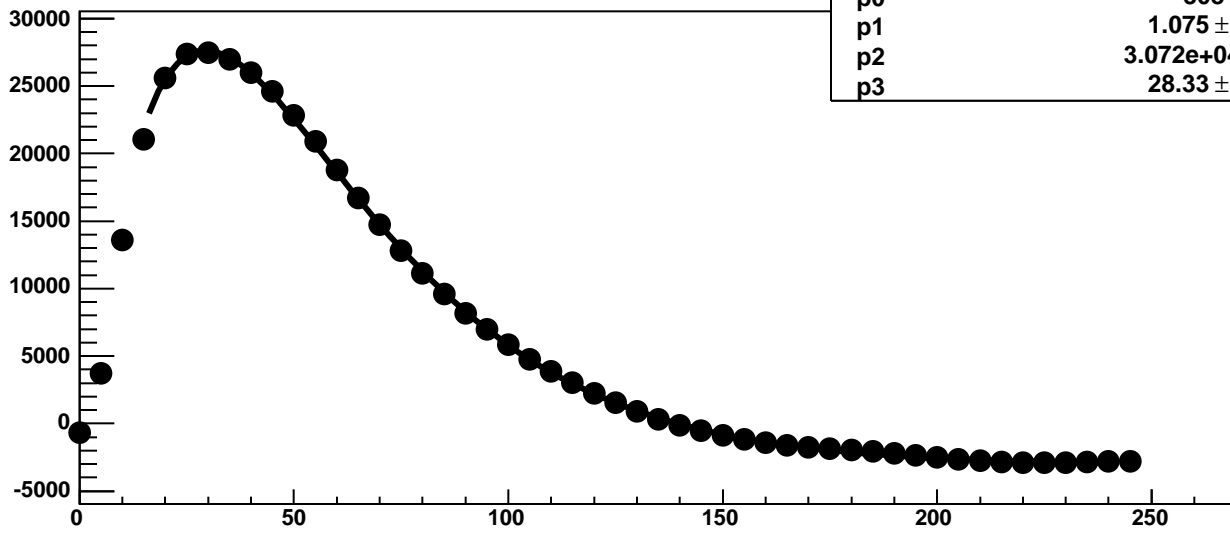
Chip 8, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

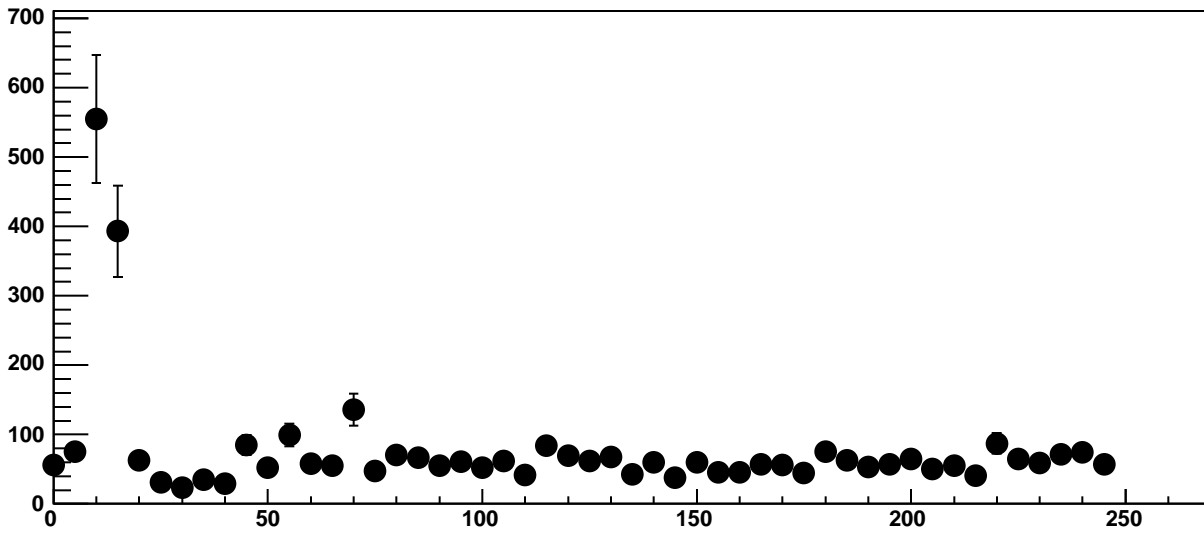


Chip 8, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

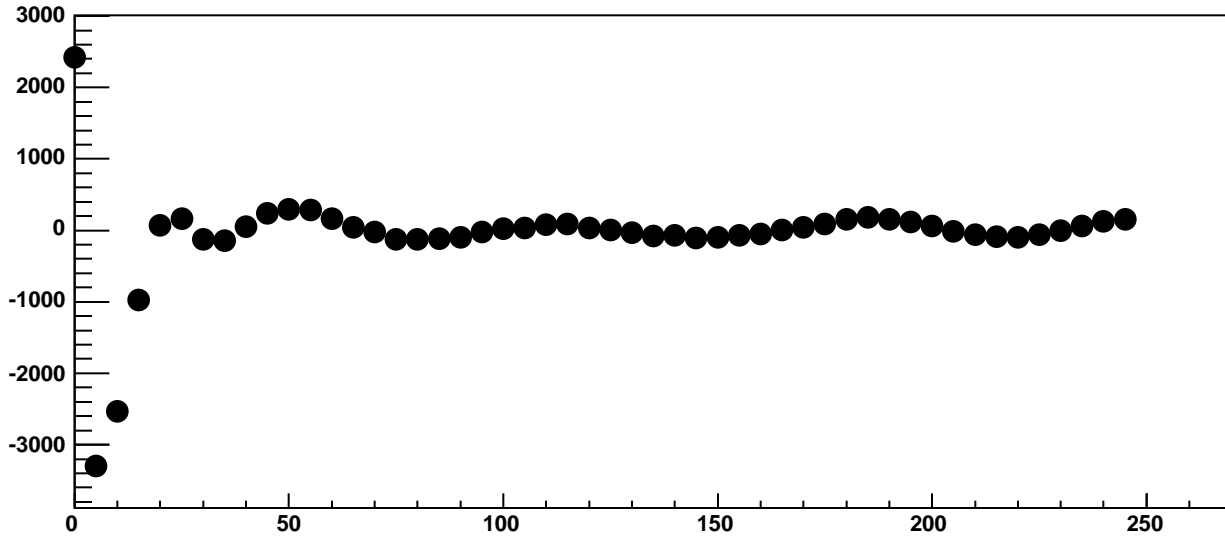


$\chi^2 / \text{ndf}$	4274 / 42
p0	-3081 ± 3.715
p1	1.075 ± 0.02301
p2	3.072e+04 ± 4.66
p3	28.33 ± 0.01188

Chip 8, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

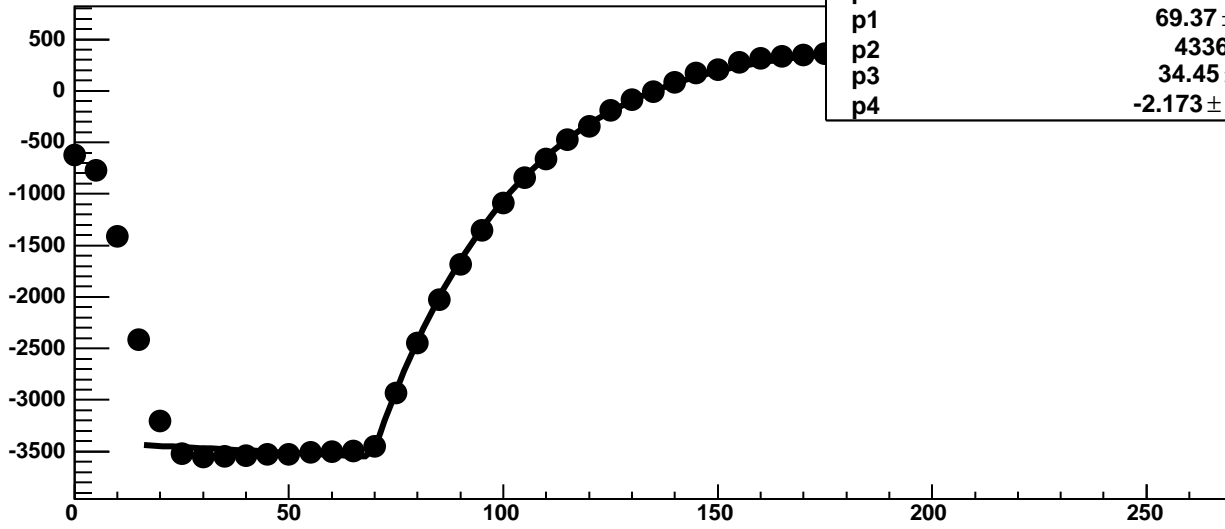


Chip 8, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



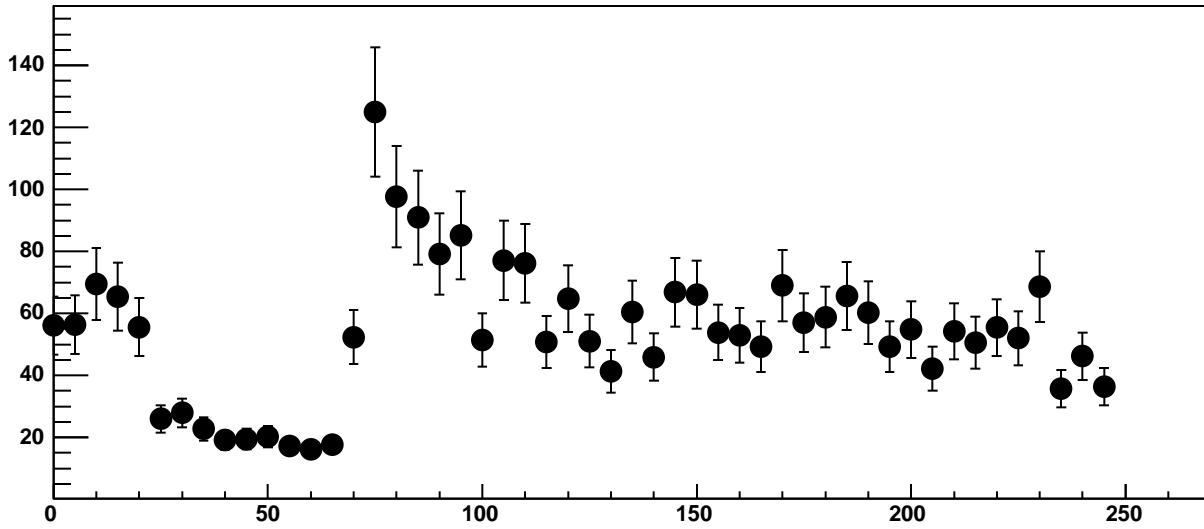


Chip 8, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

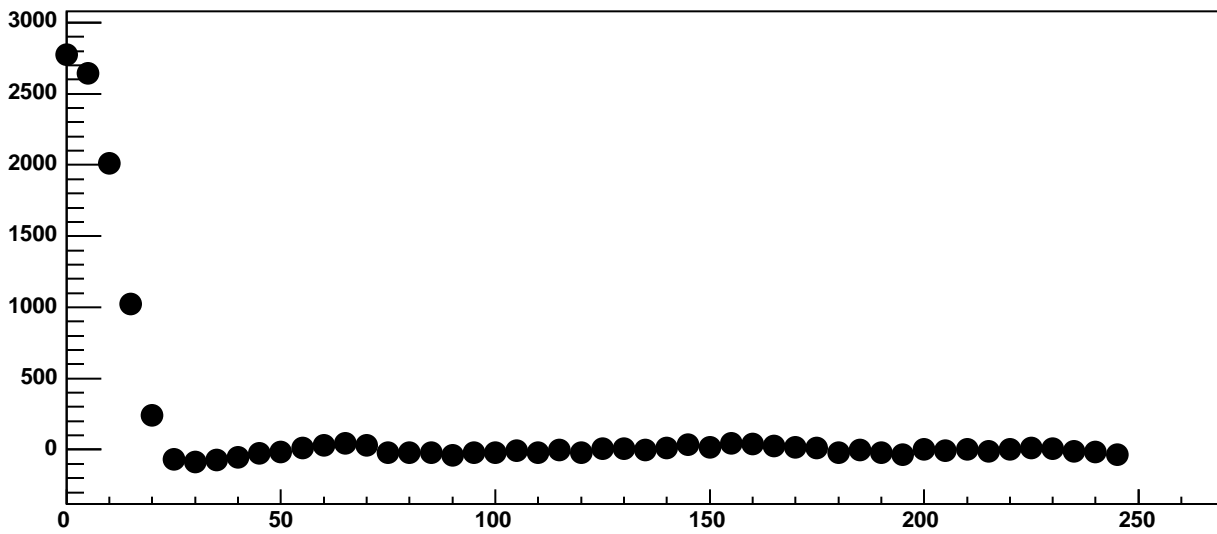


$\chi^2 / \text{ndf}$	5978 / 41
p0	$-3553 \pm 2.517$
p1	$69.37 \pm 0.0912$
p2	$4336 \pm 18.13$
p3	$34.45 \pm 0.2381$
p4	$-2.173 \pm 0.09828$

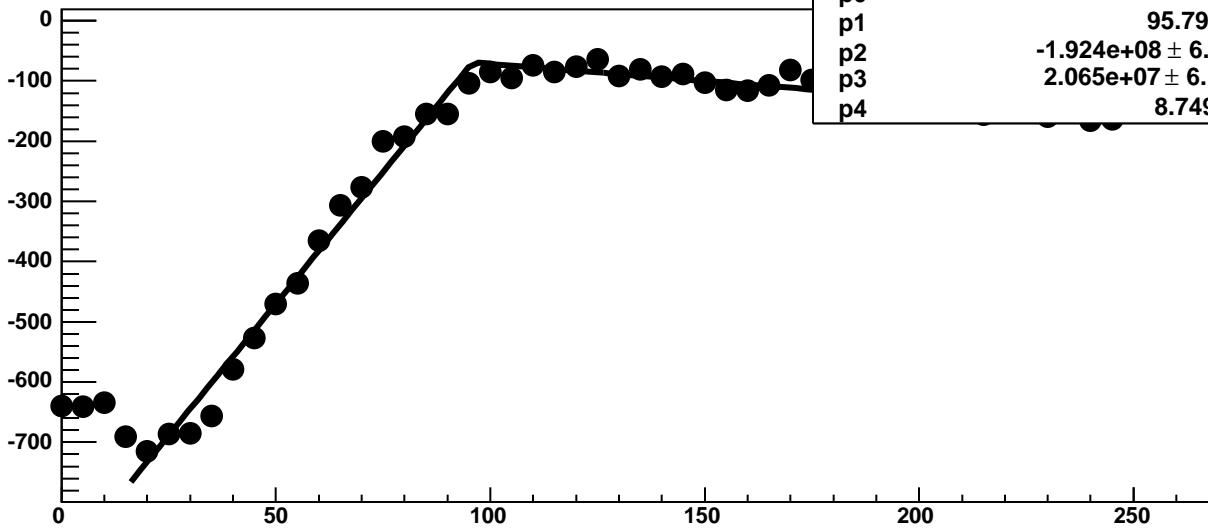
Chip 8, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

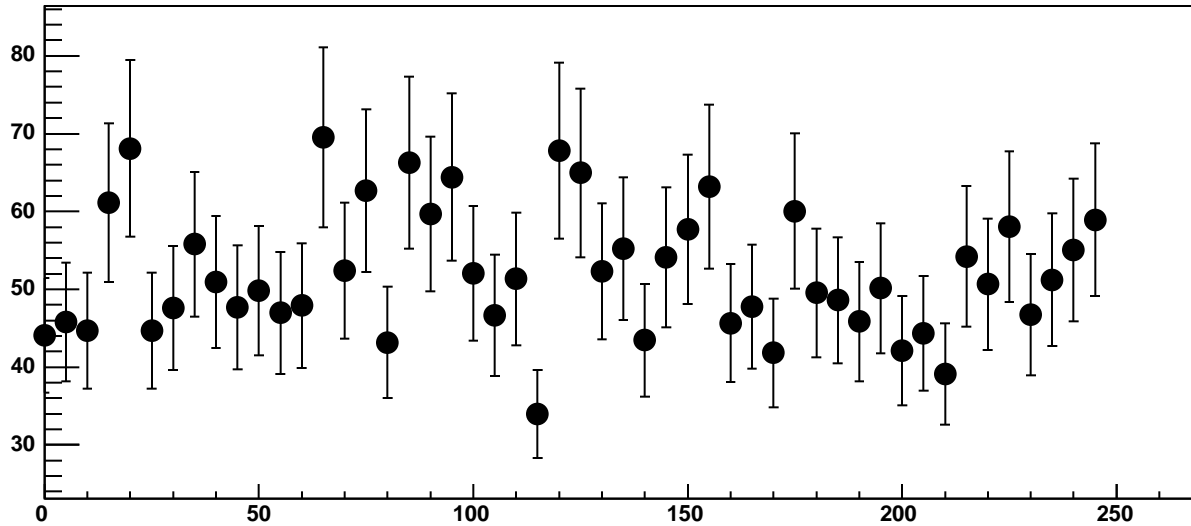


Chip 8, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

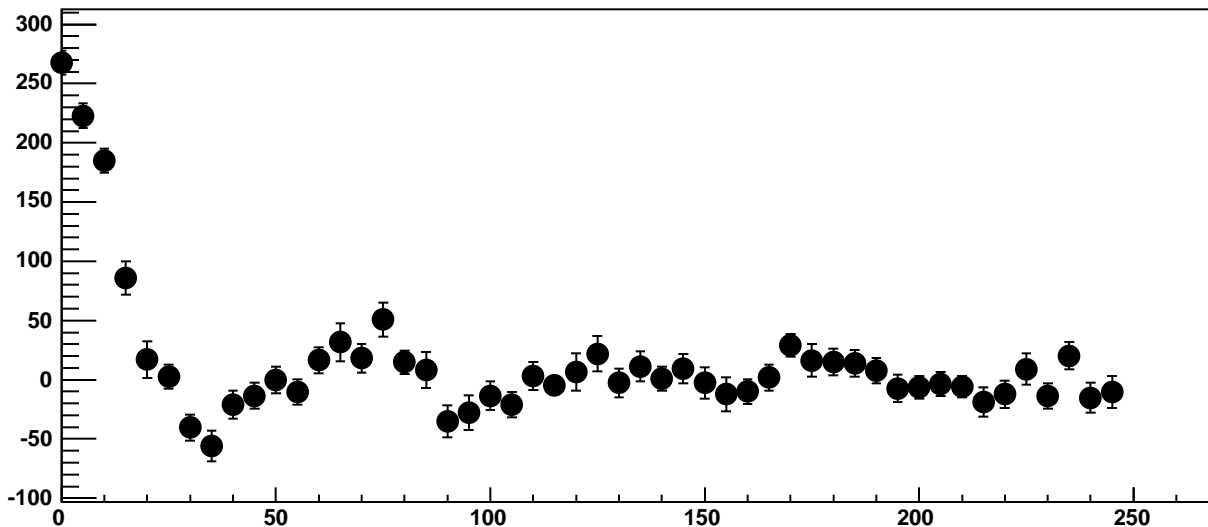


$\chi^2 / \text{ndf}$	147.6 / 41
p0	$-69.18 \pm 4.041$
p1	$95.79 \pm 0.8111$
p2	$-1.924\text{e}+08 \pm 6.435\text{e}+06$
p3	$2.065\text{e}+07 \pm 6.174\text{e}+05$
p4	$8.749 \pm 0.129$

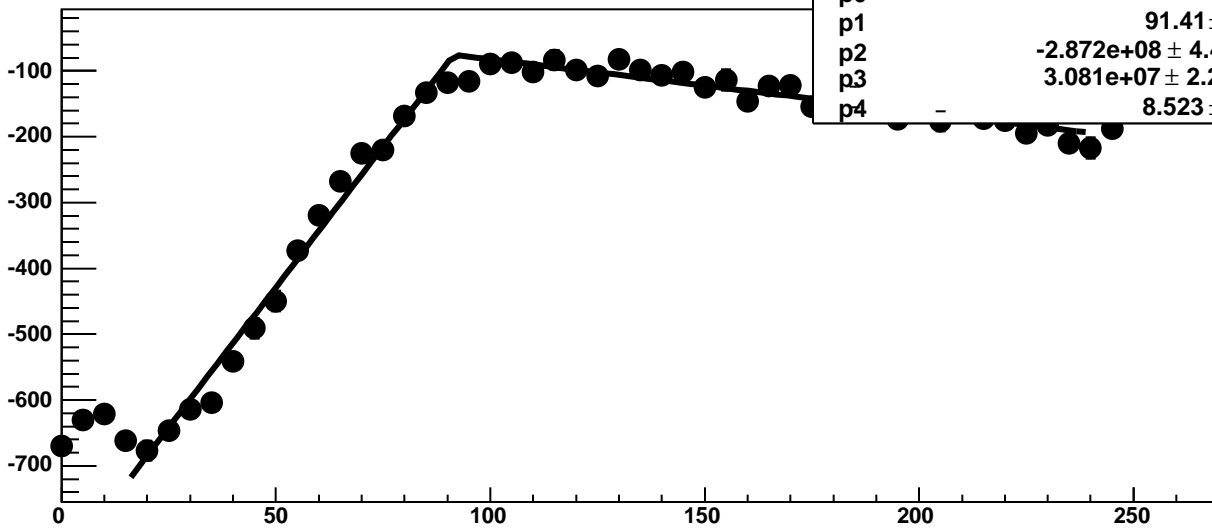
Chip 8, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

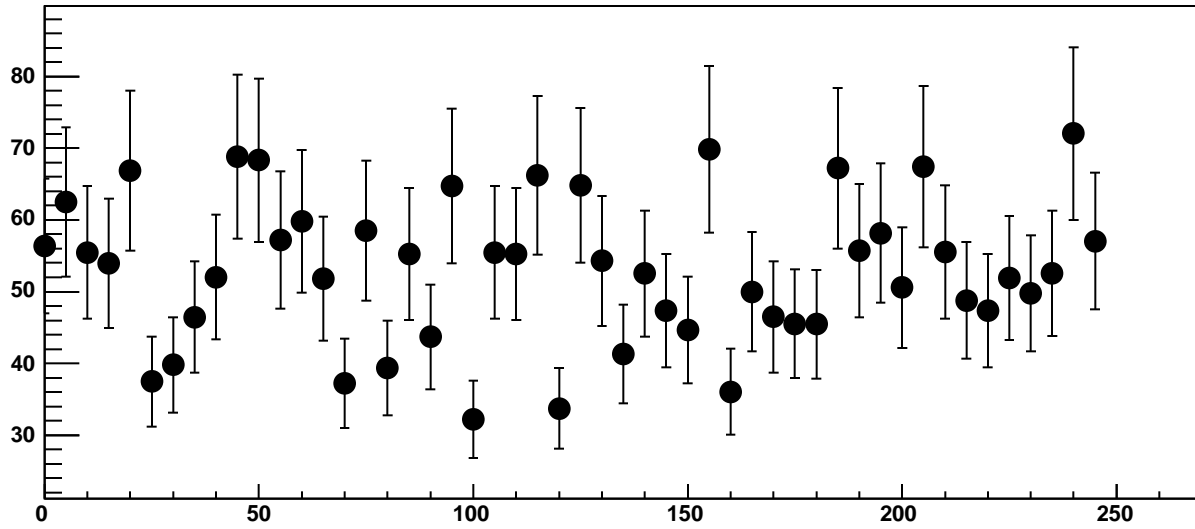


Chip 8, Channel 12, Enable 4, DAC=1600, ADC Mean vs Hold

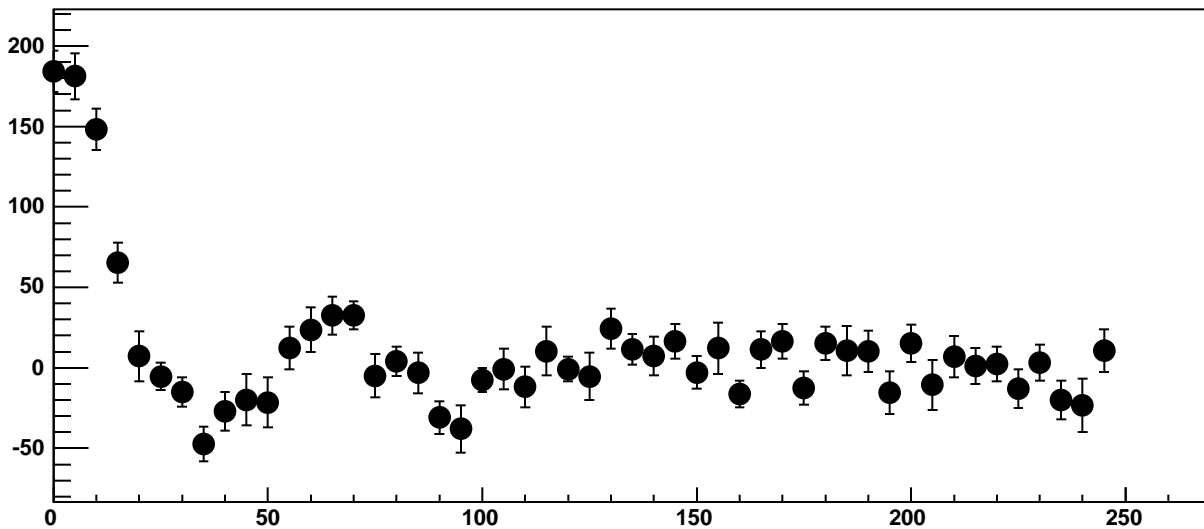


$\chi^2 / \text{ndf}$	134.8 / 41
p0	$-75.51 \pm 3.728$
p1	$91.41 \pm 0.7153$
p2	$-2.872\text{e}+08 \pm 4.495\text{e}+06$
p3	$3.081\text{e}+07 \pm 2.223\text{e}+05$
p4	$8.523 \pm 0.1178$

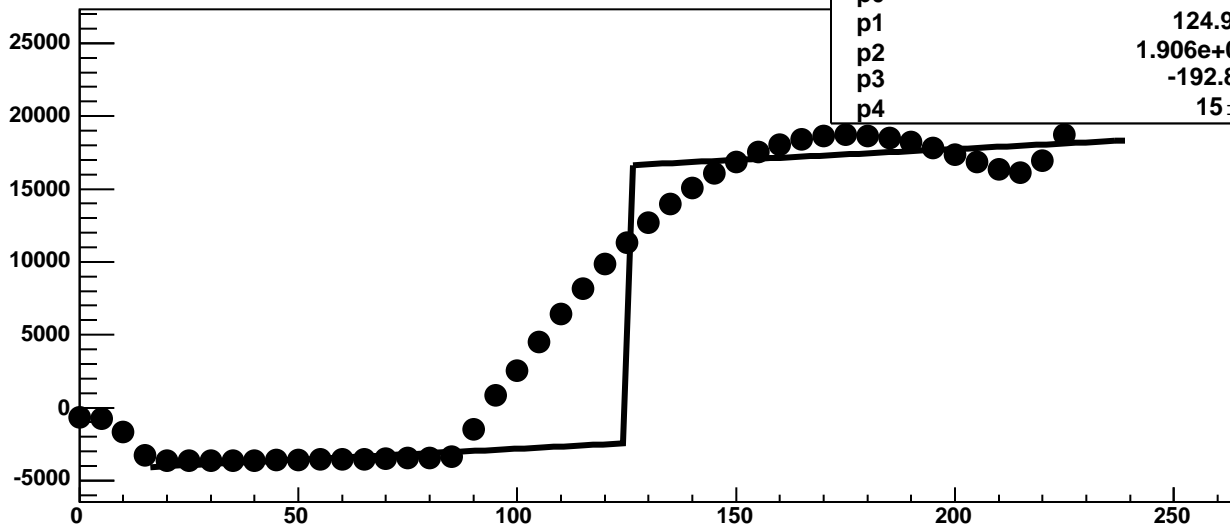
Chip 8, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold

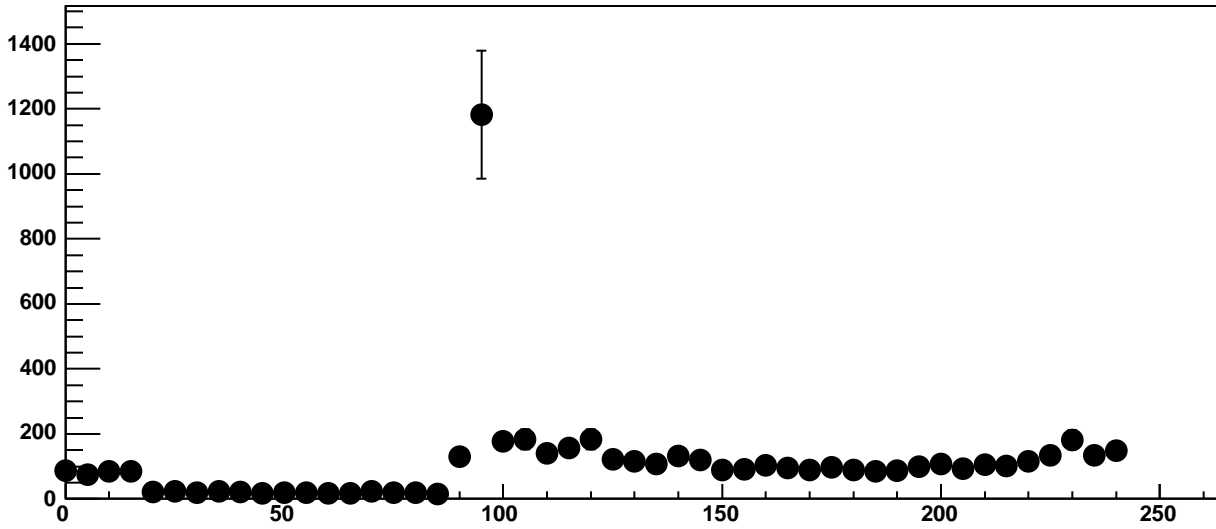


Chip 8, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

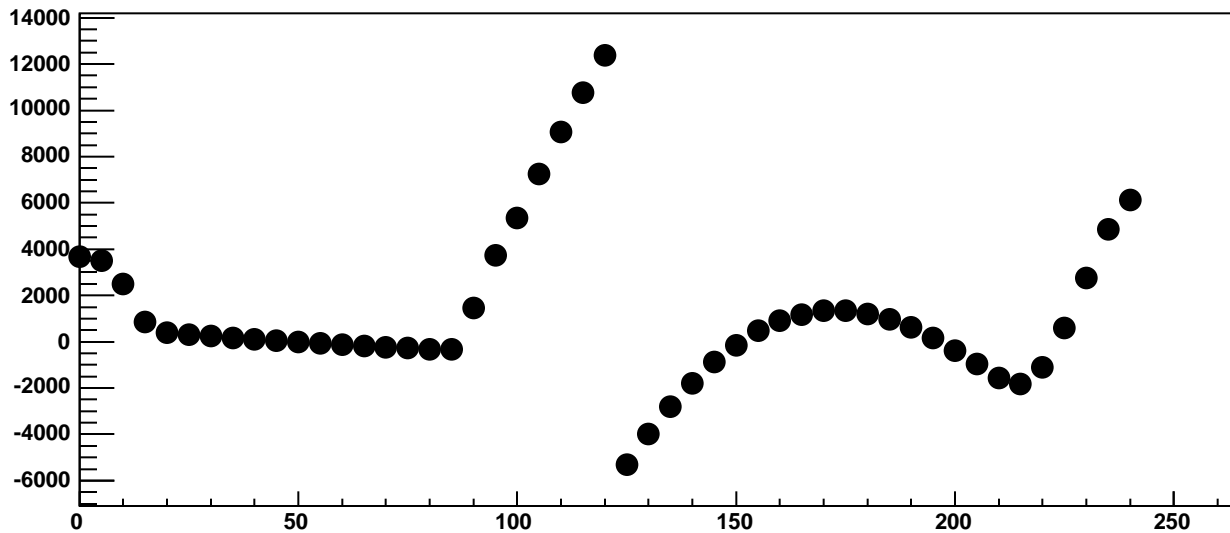


$\chi^2 / \text{ndf}$	5.128e+05 / 41
p0	-2443 ± 2.137
p1	124.9 ± 0.957
p2	1.906e+04 ± 6
p3	-192.8 ± 2.331
p4	15 ± 0.1093

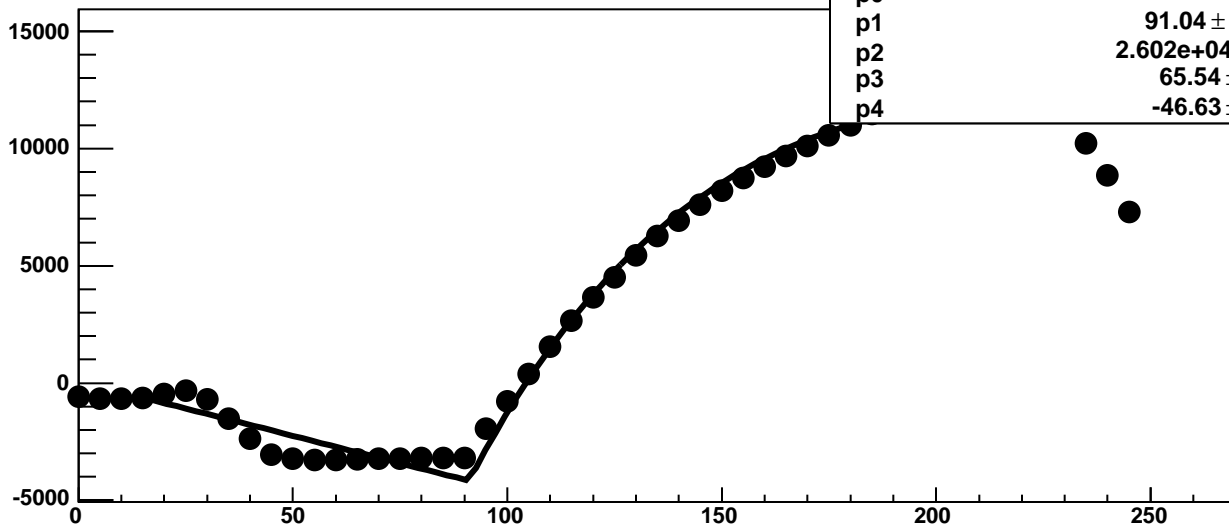
Chip 8, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold



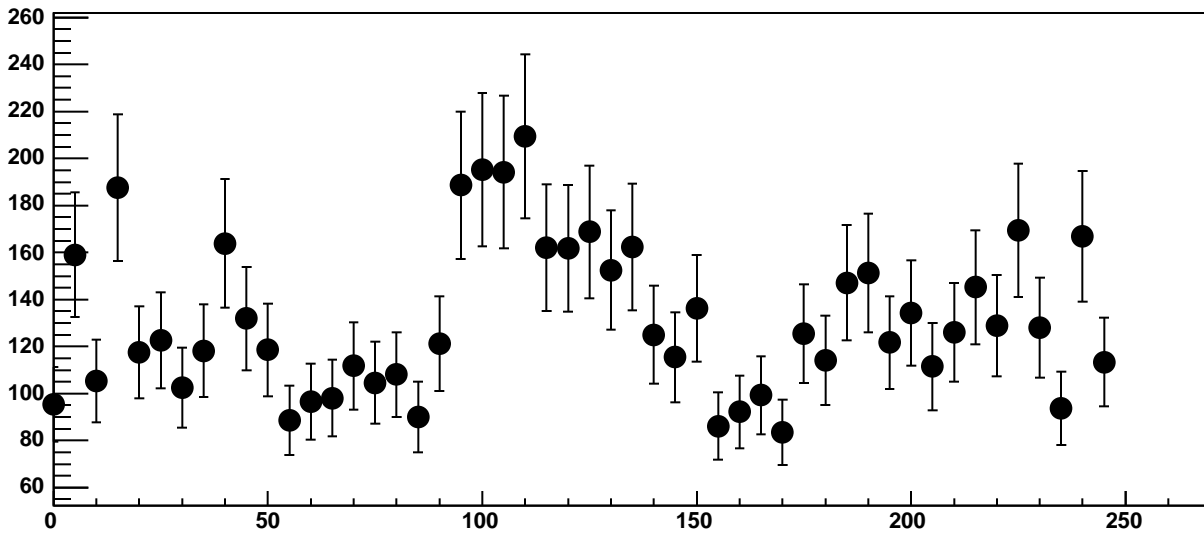
Chip 8, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



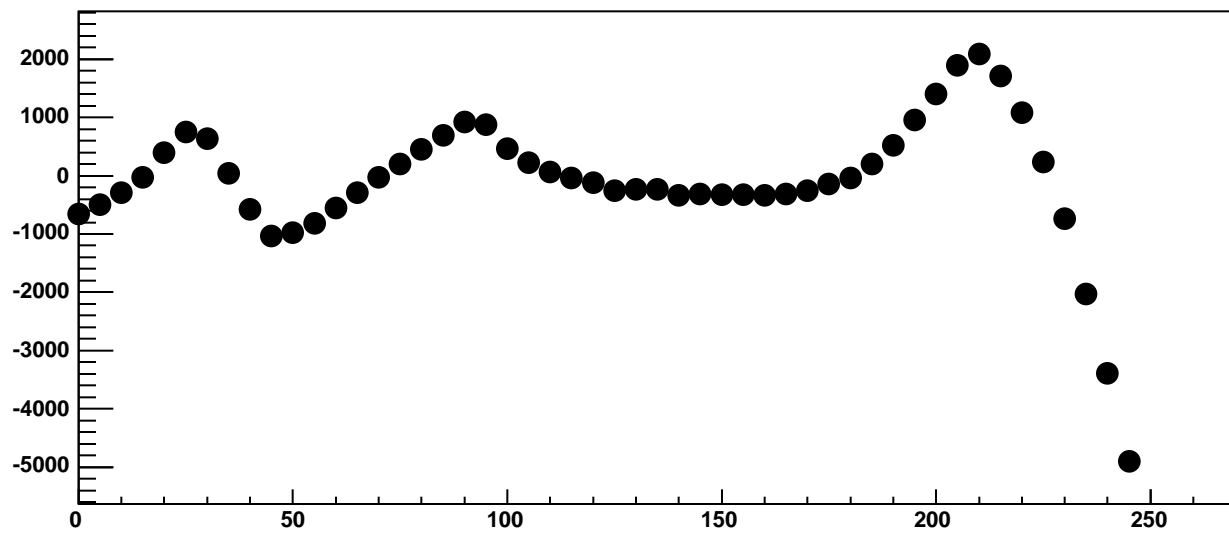
Chip 8, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold



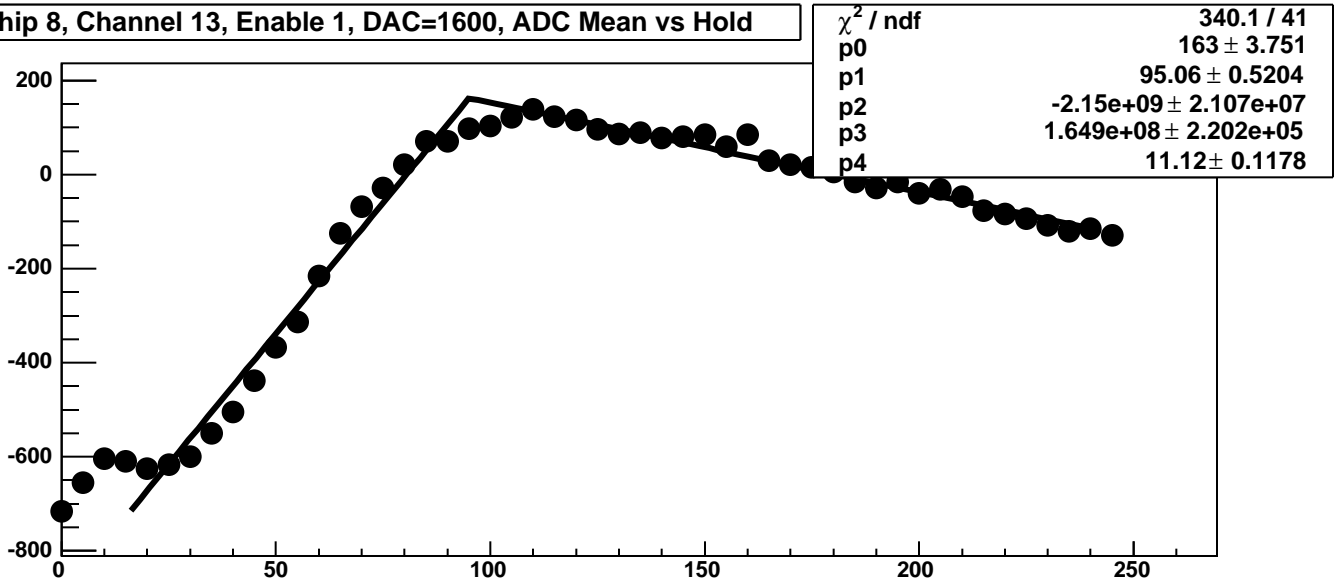
Chip 8, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



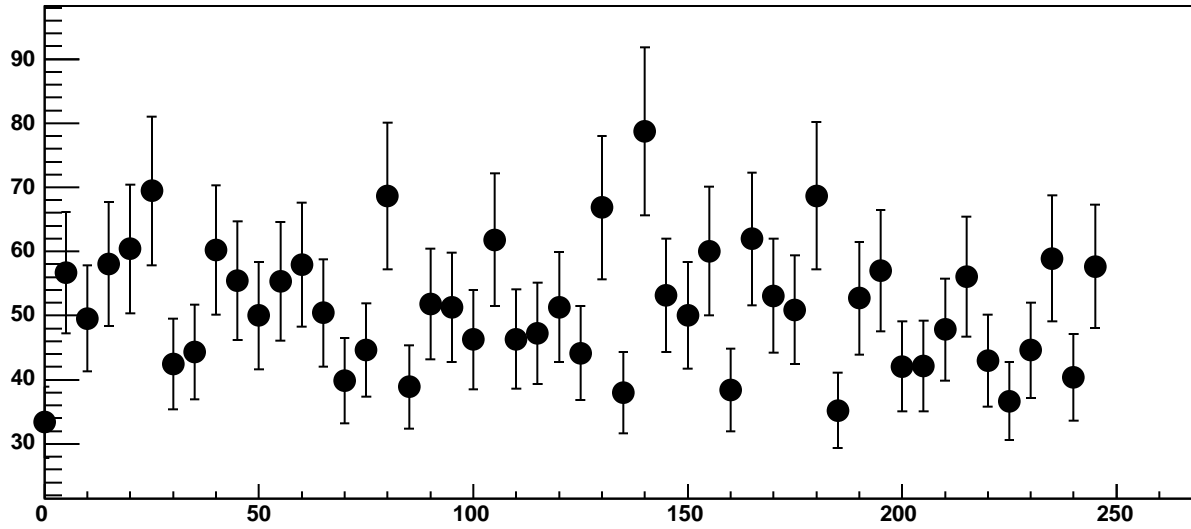
Chip 8, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold



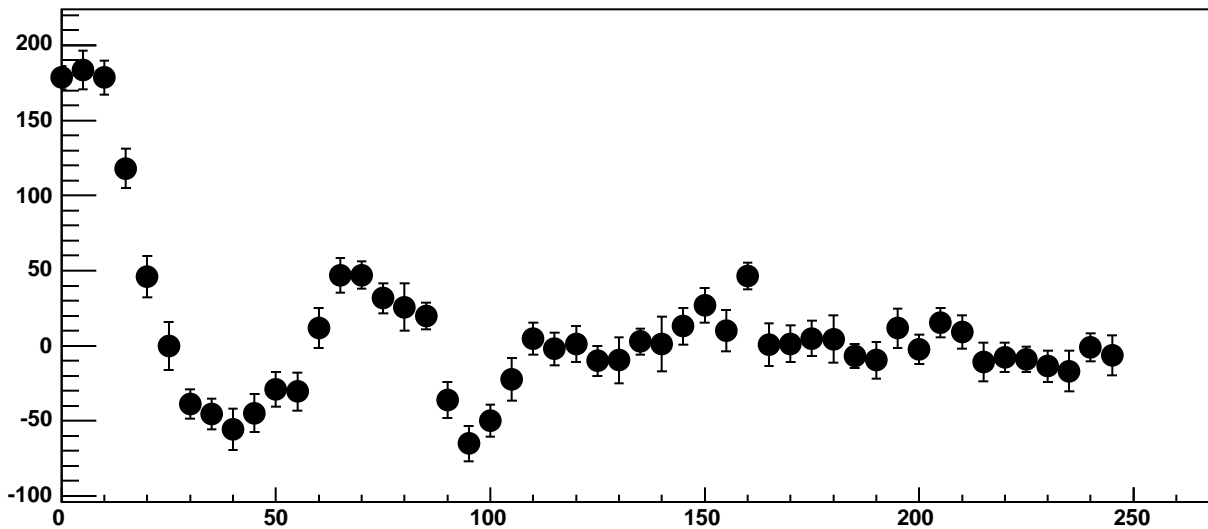
Chip 8, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold



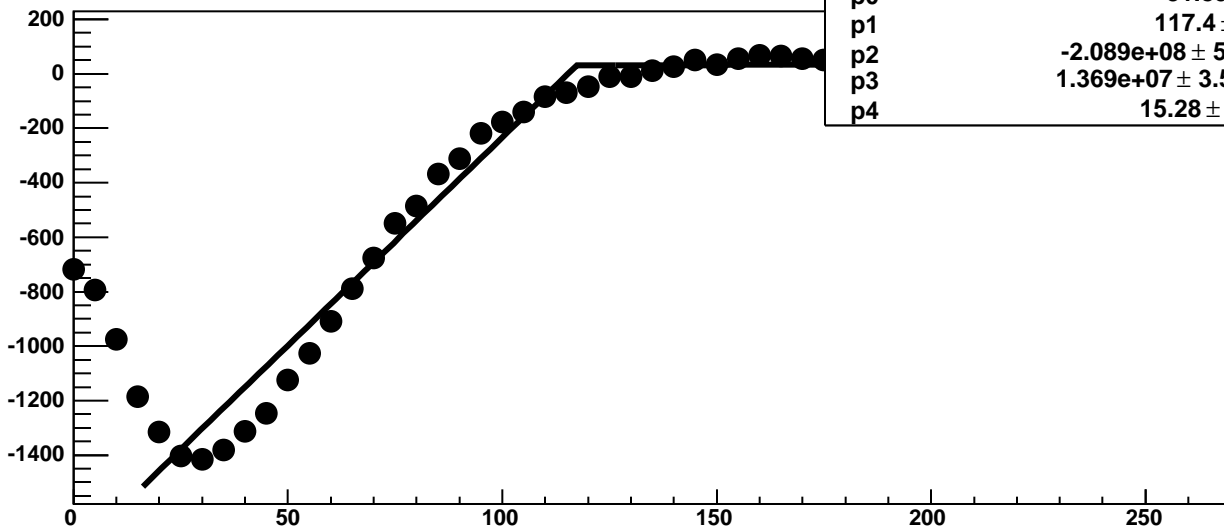
Chip 8, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold

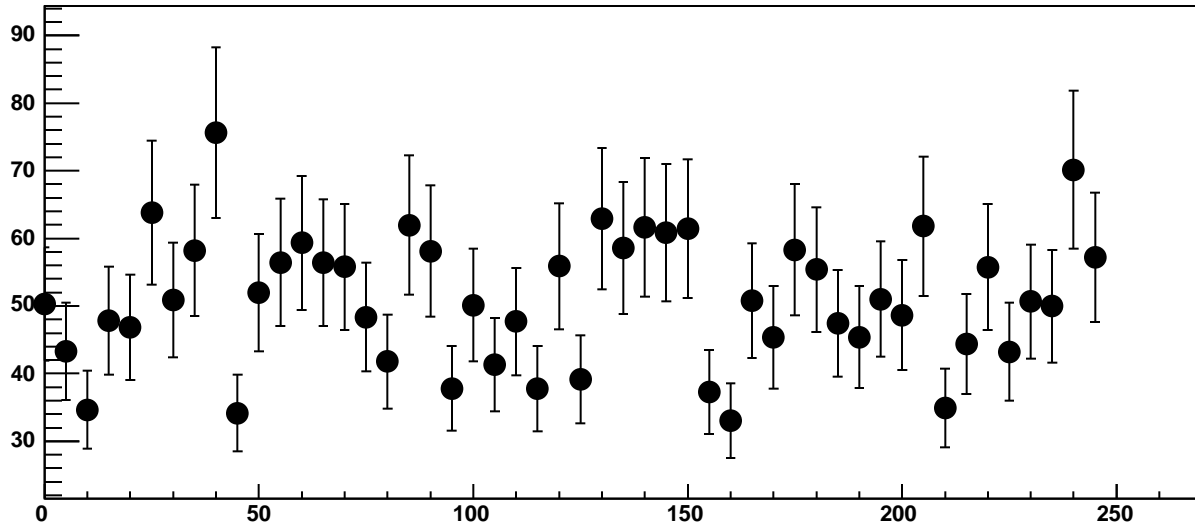


Chip 8, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

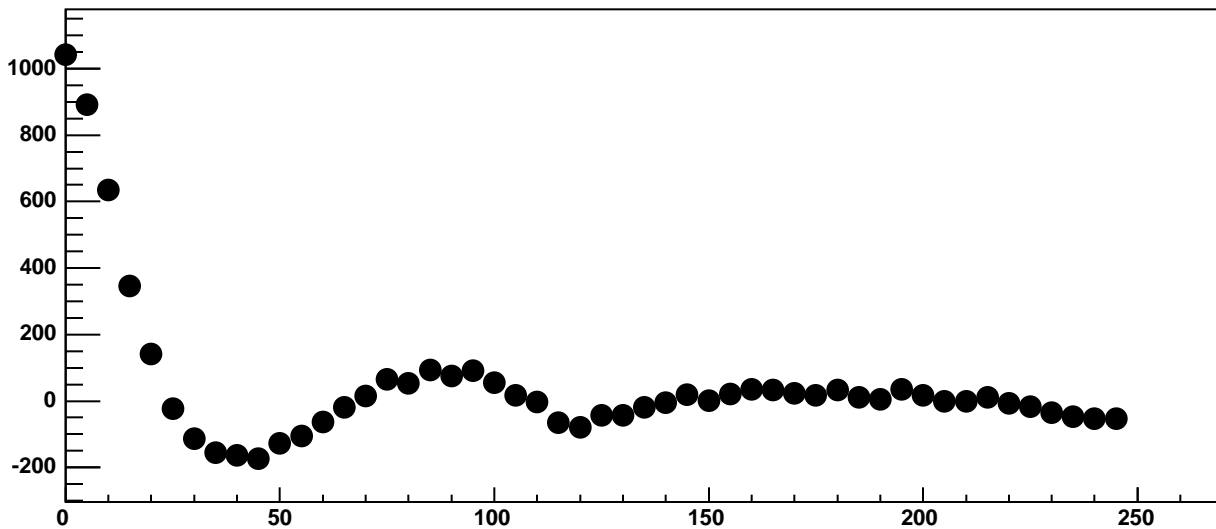


$\chi^2 / \text{ndf}$	2693 / 41
p0	$31.85 \pm 4.547$
p1	$117.4 \pm 0.4133$
p2	$-2.089\text{e}+08 \pm 5.42\text{e}+06$
p3	$1.369\text{e}+07 \pm 3.552\text{e}+05$
p4	$15.28 \pm 0.07577$

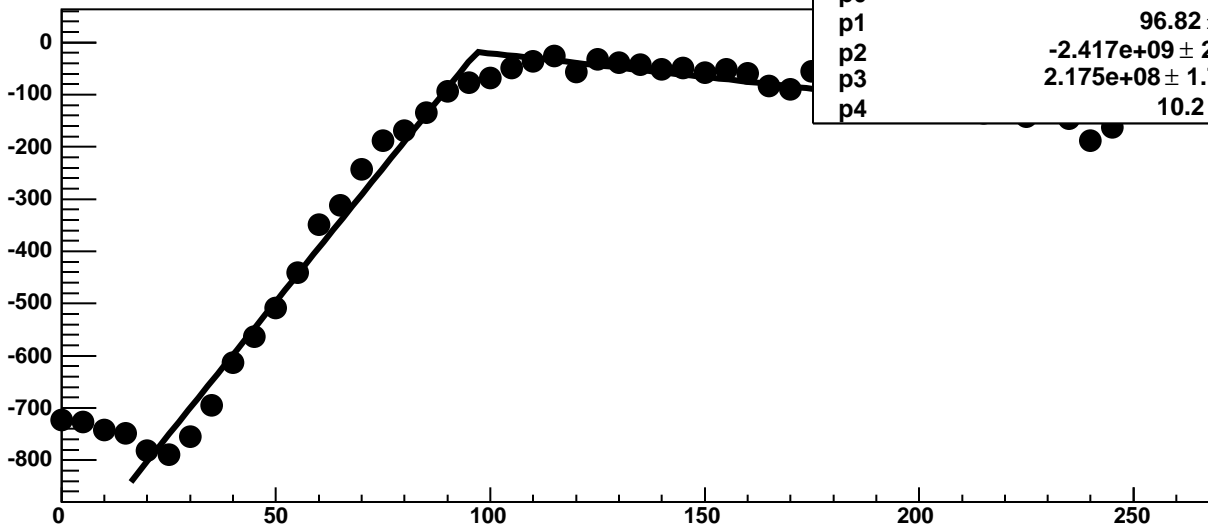
Chip 8, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

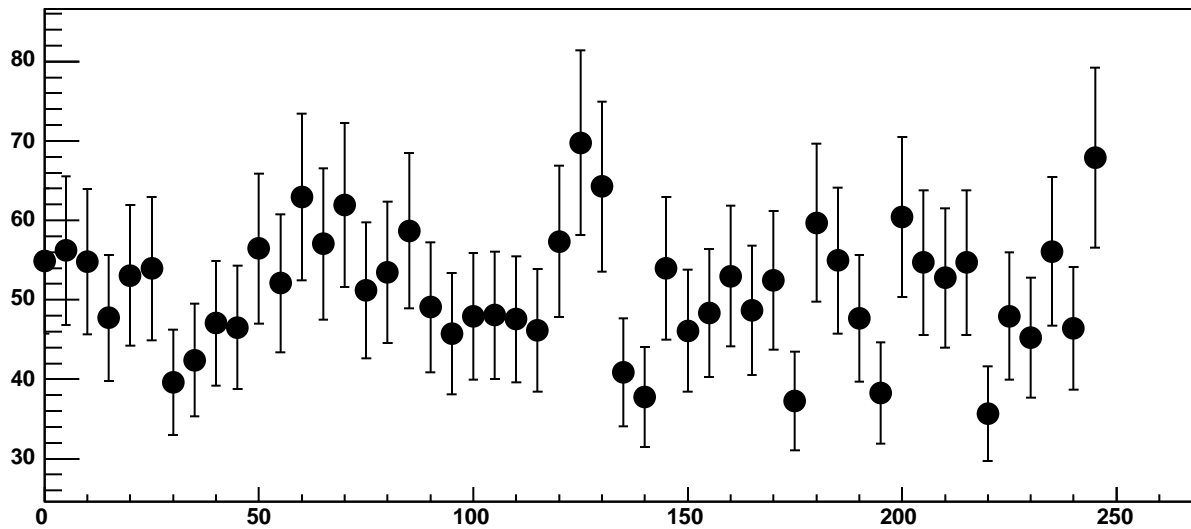


Chip 8, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

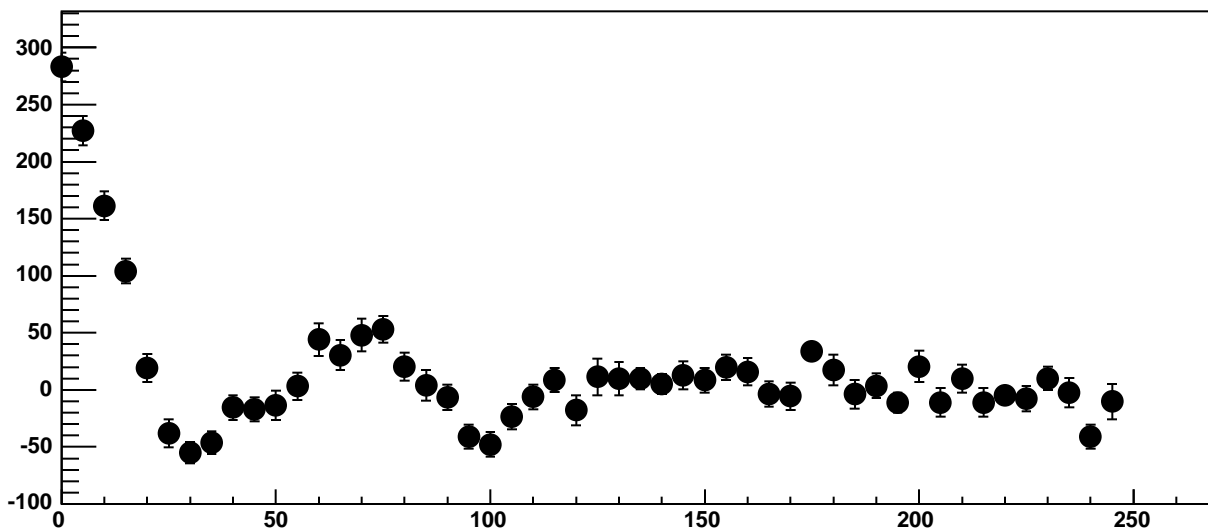


$\chi^2 / \text{ndf}$	308.2 / 41
p0	-17.84 ± 3.874
p1	96.82 ± 0.6406
p2	-2.417e+09 ± 2.67e+07
p3	2.175e+08 ± 1.749e+05
p4	10.2 ± 0.1127

Chip 8, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

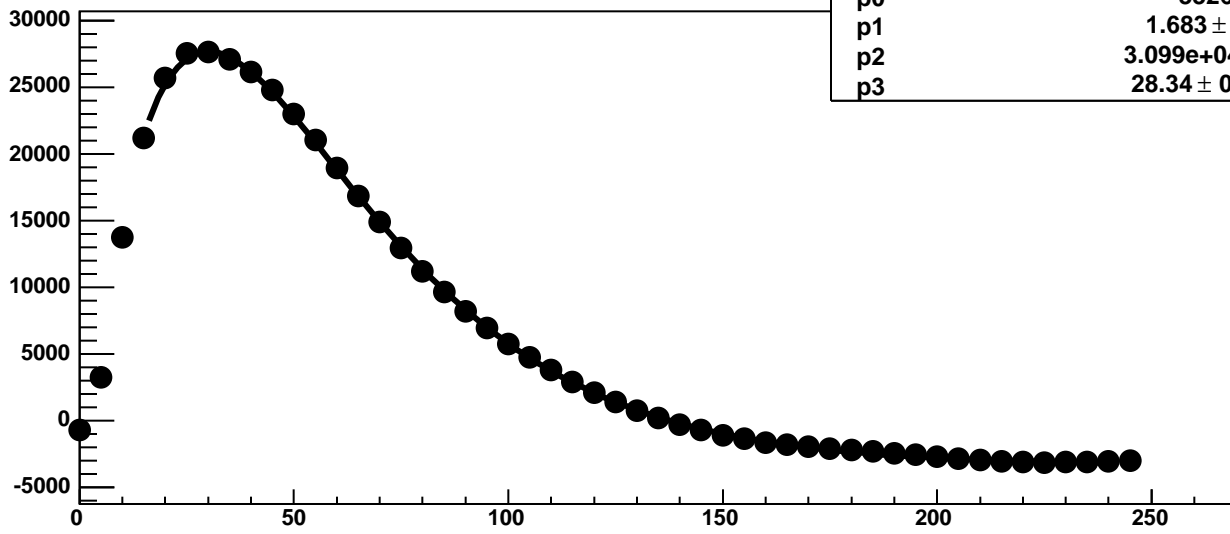


Chip 8, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold



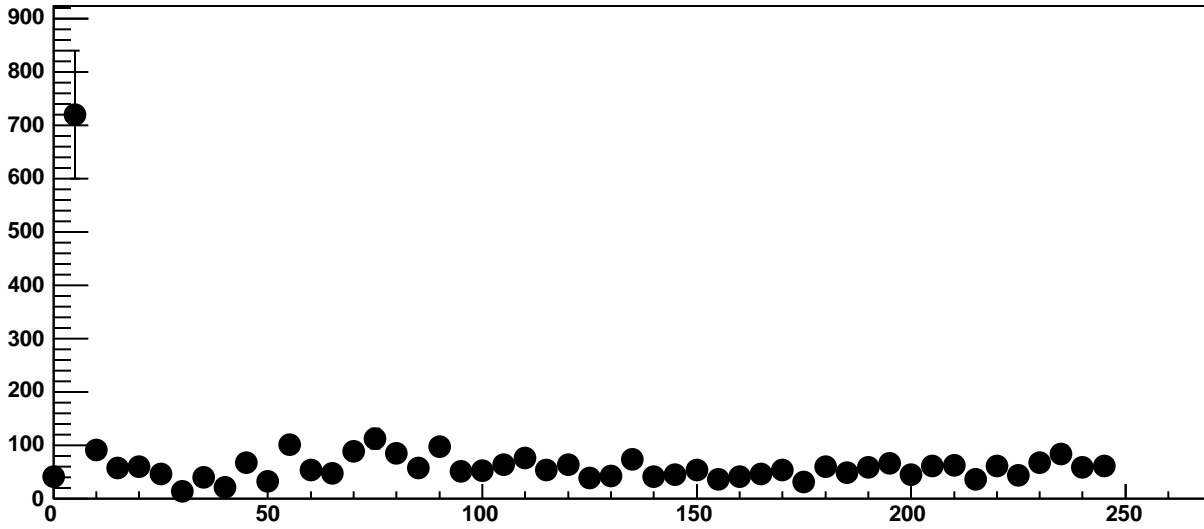


Chip 8, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold

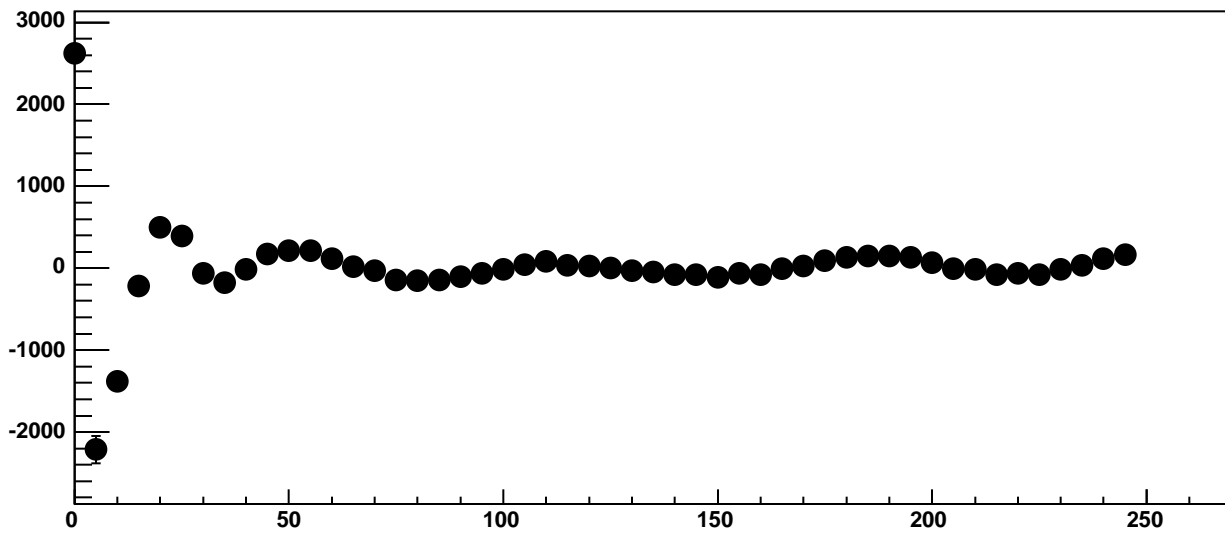


$\chi^2 / \text{ndf}$	6306 / 42
p0	-3326 ± 3.277
p1	1.683 ± 0.01398
p2	3.099e+04 ± 3.76
p3	28.34 ± 0.009214

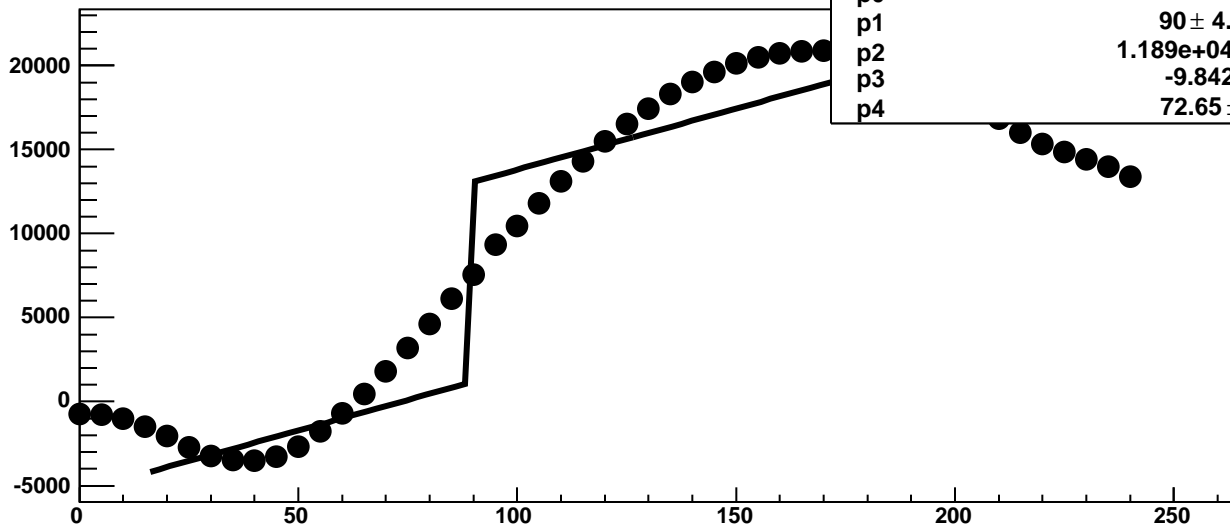
Chip 8, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold

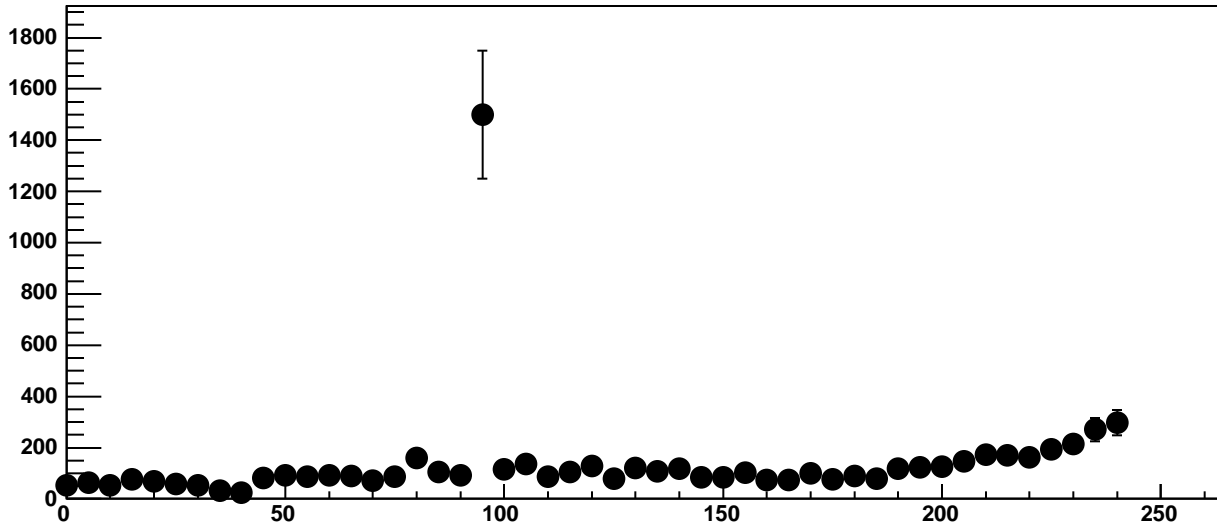


Chip 8, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

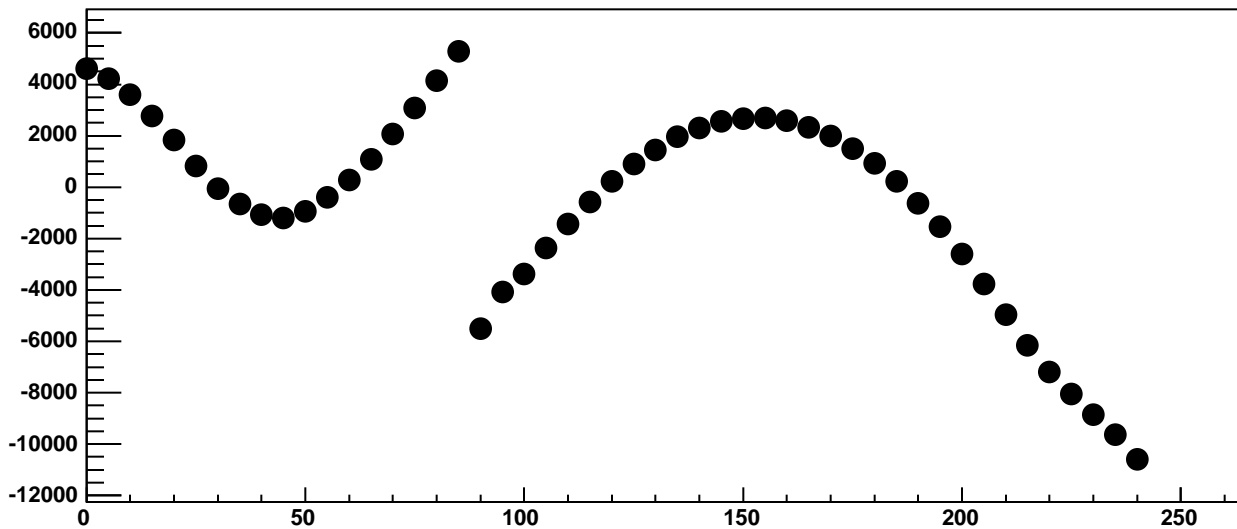


$\chi^2 / \text{ndf}$	6.342e+05 / 41
p0	1192 ± 20.33
p1	90 ± 4.594e-05
p2	1.189e+04 ± 26.14
p3	-9.842 ± 1.987
p4	72.65 ± 0.0653

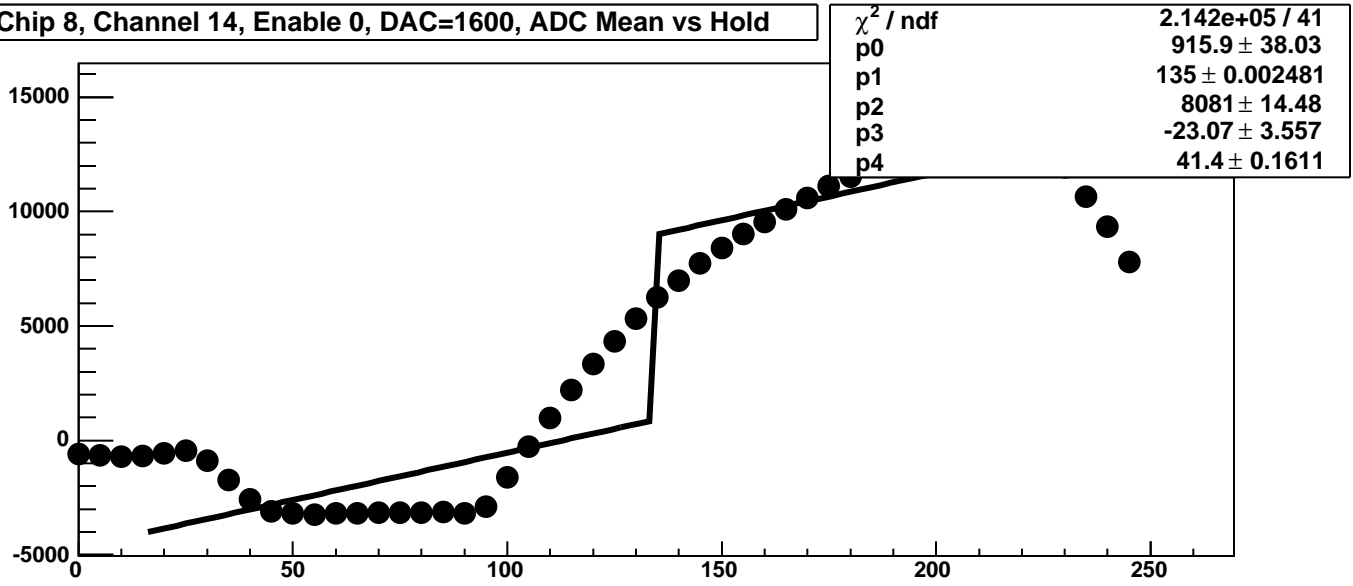
Chip 8, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



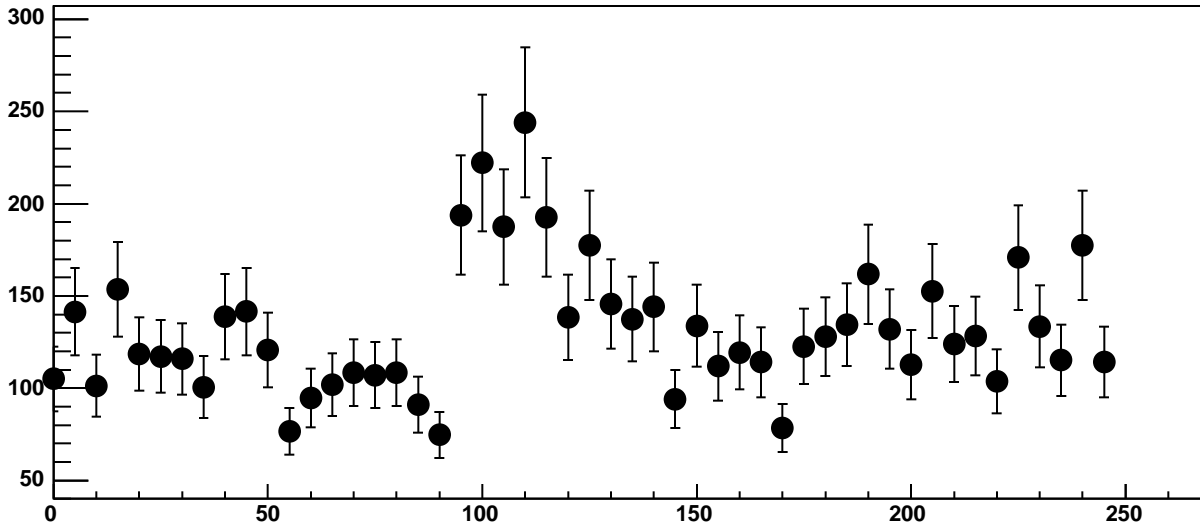
Chip 8, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold



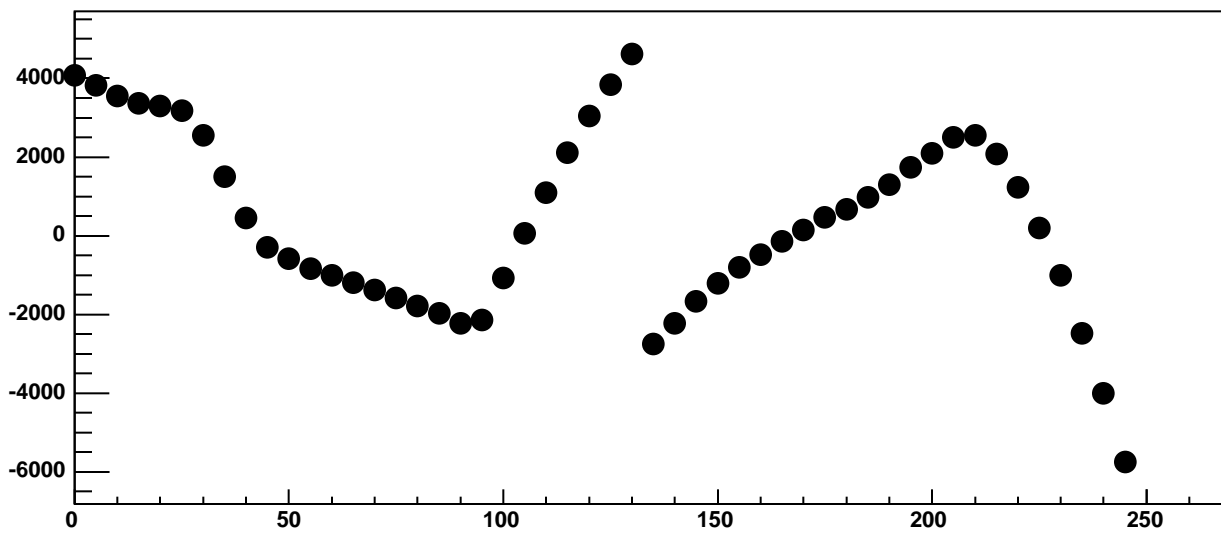
Chip 8, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold



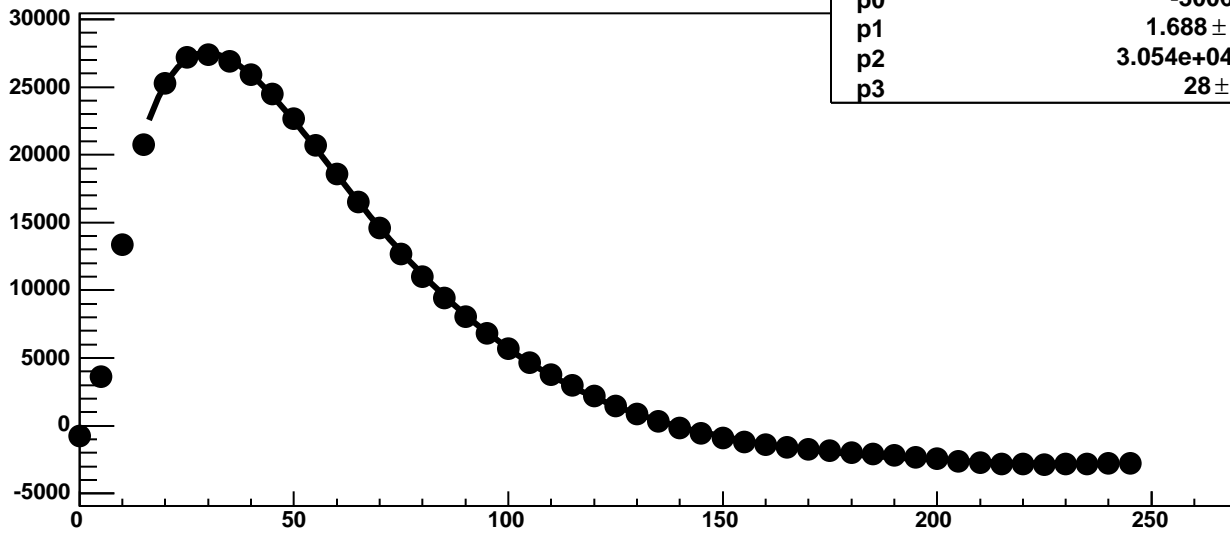
Chip 8, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

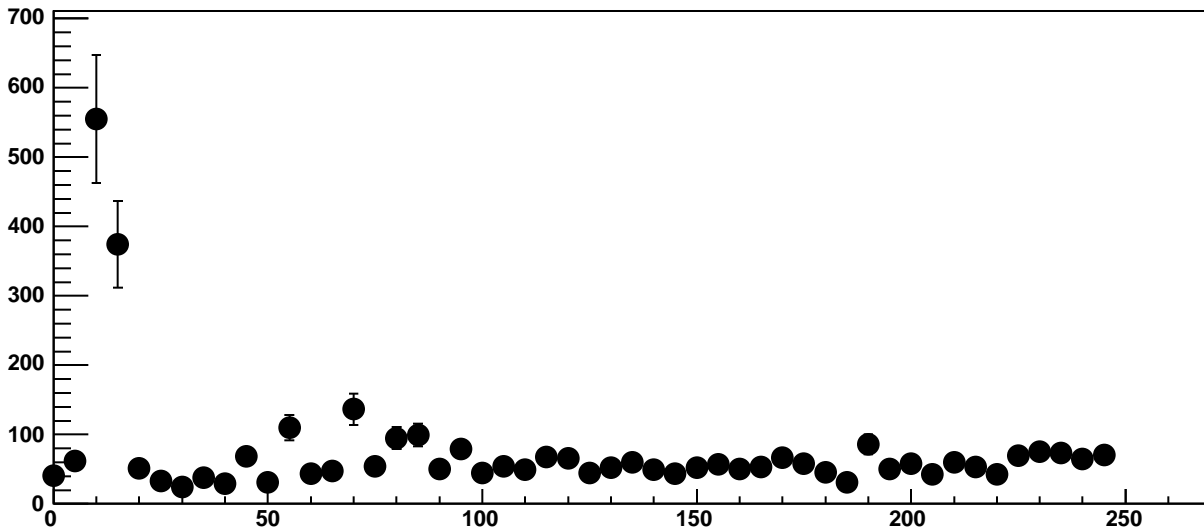


Chip 8, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold

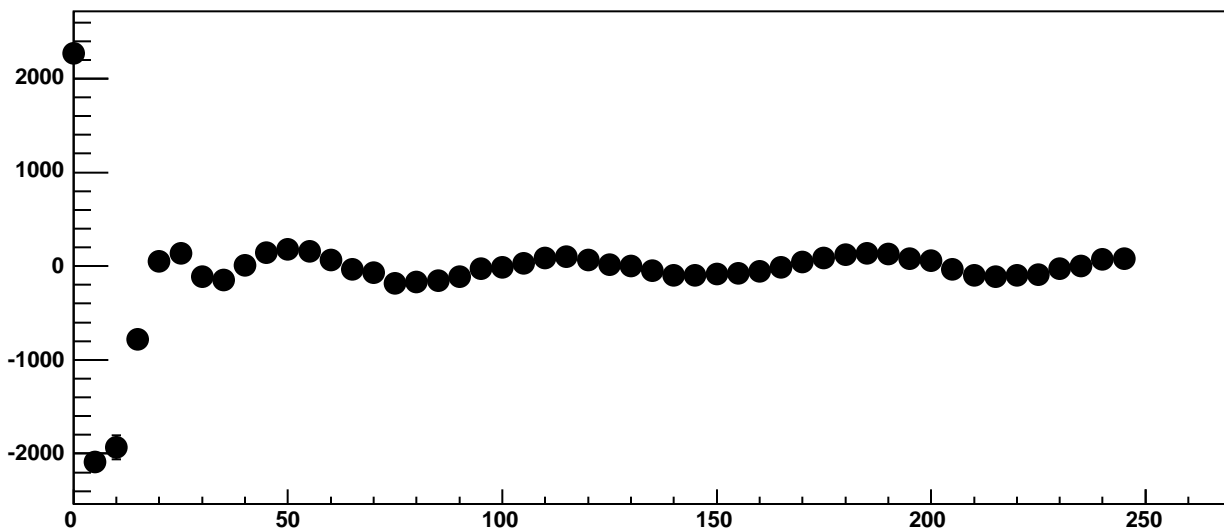


$\chi^2 / \text{ndf}$	3715 / 42
p0	-3006 ± 3.468
p1	1.688 ± 0.02023
p2	3.054e+04 ± 4.395
p3	28 ± 0.01122

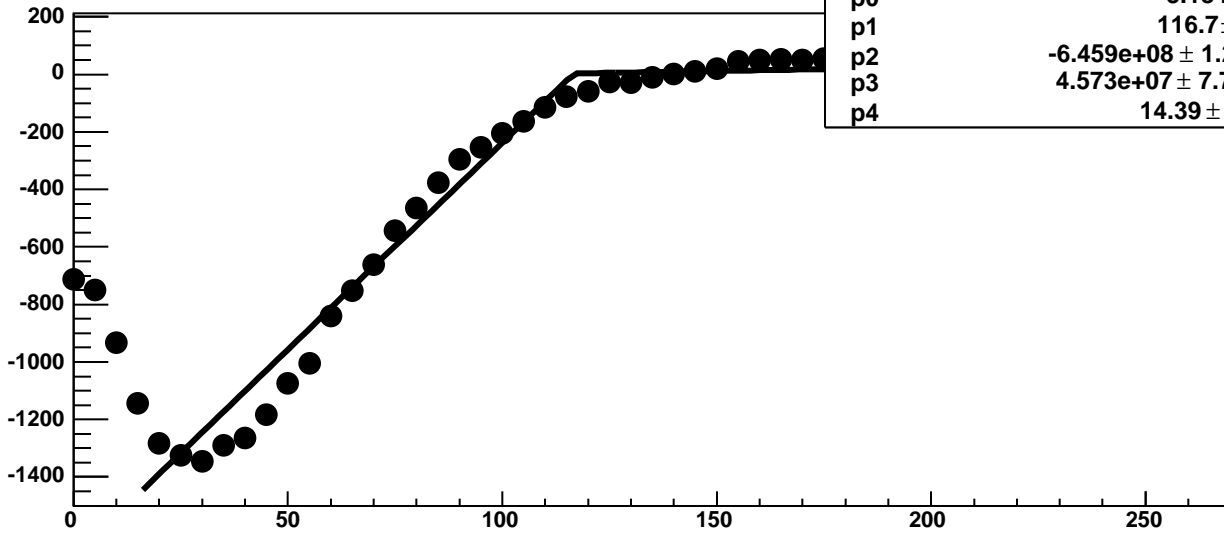
Chip 8, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

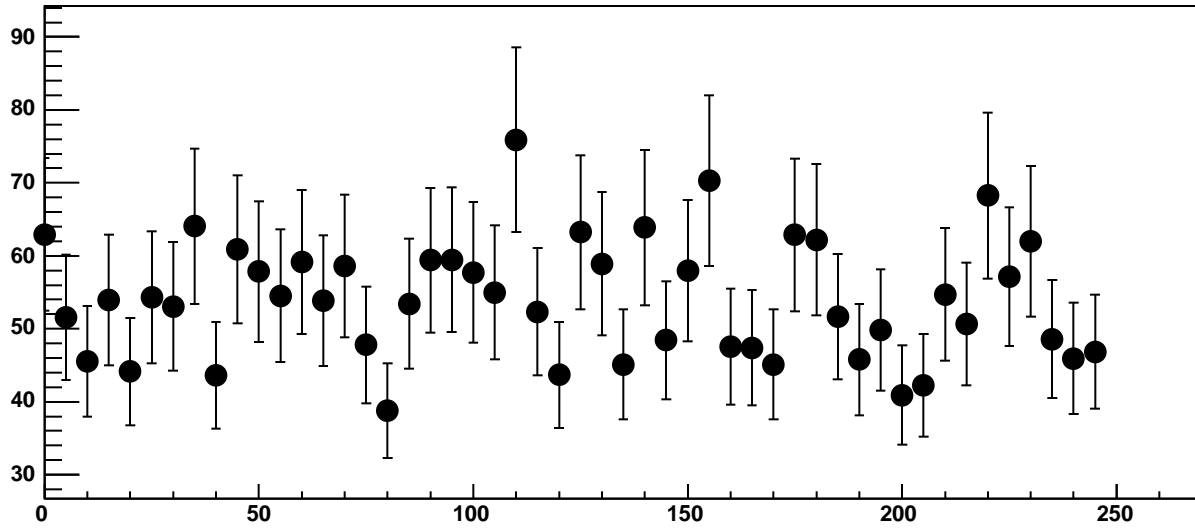


Chip 8, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

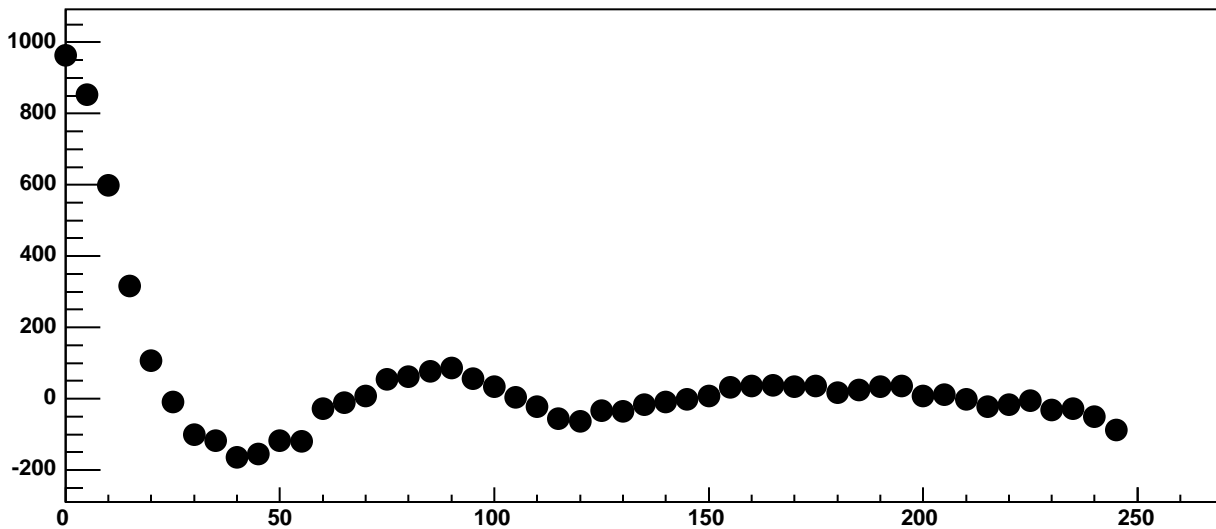


$\chi^2 / \text{ndf}$	1830 / 41
p0	$3.184 \pm 4.966$
p1	$116.7 \pm 0.5249$
p2	$-6.459\text{e}+08 \pm 1.248\text{e}+07$
p3	$4.573\text{e}+07 \pm 7.778\text{e}+05$
p4	$14.39 \pm 0.09053$

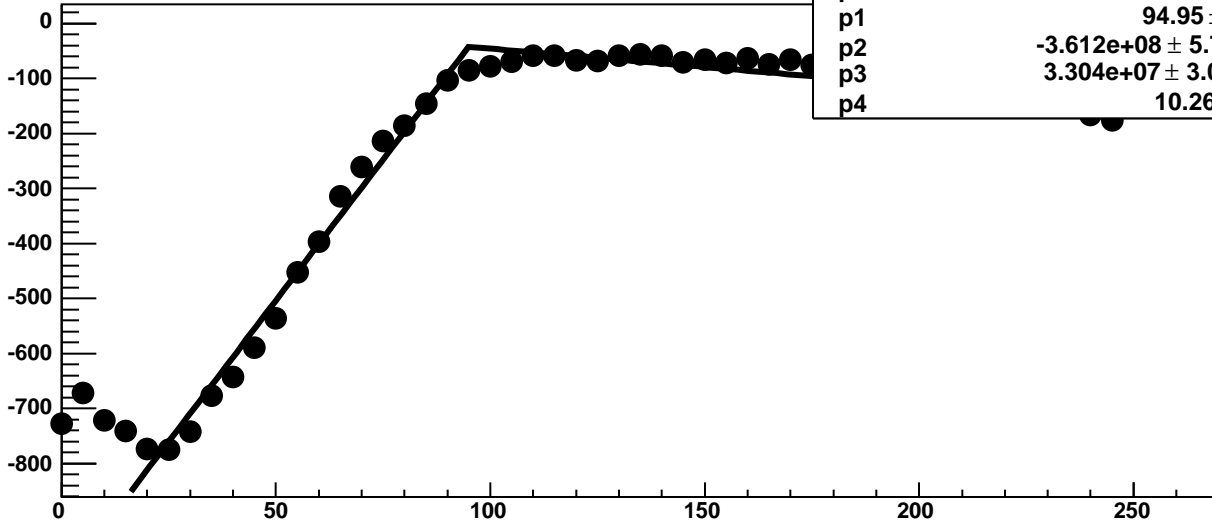
Chip 8, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

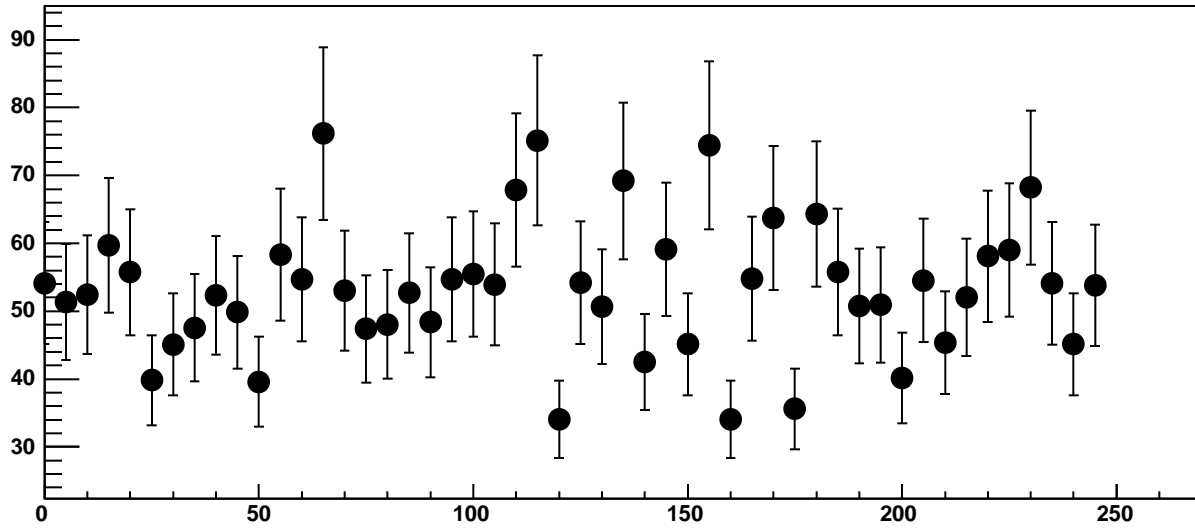


Chip 8, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

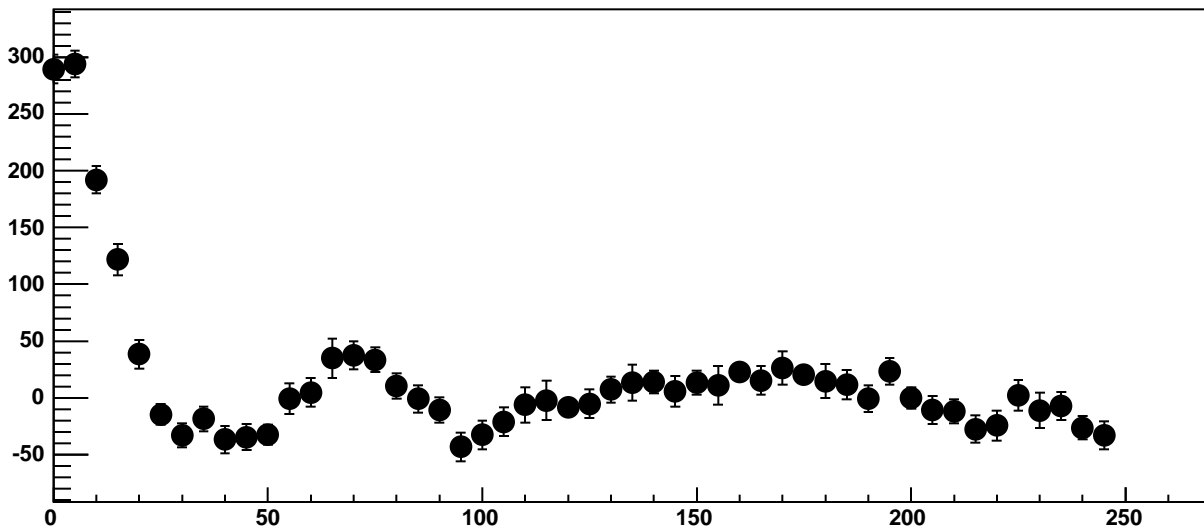


$\chi^2 / \text{ndf}$	231.5 / 41
p0	$-42.42 \pm 4.039$
p1	$94.95 \pm 0.6833$
p2	$-3.612\text{e}+08 \pm 5.754\text{e}+06$
p3	$3.304\text{e}+07 \pm 3.002\text{e}+05$
p4	$10.26 \pm 0.125$

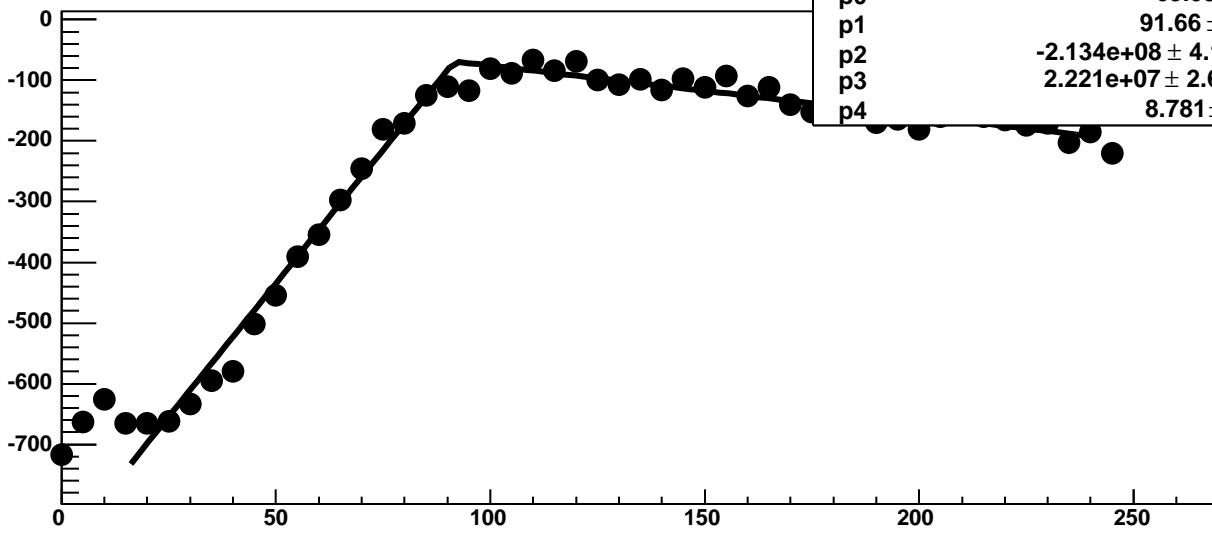
Chip 8, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

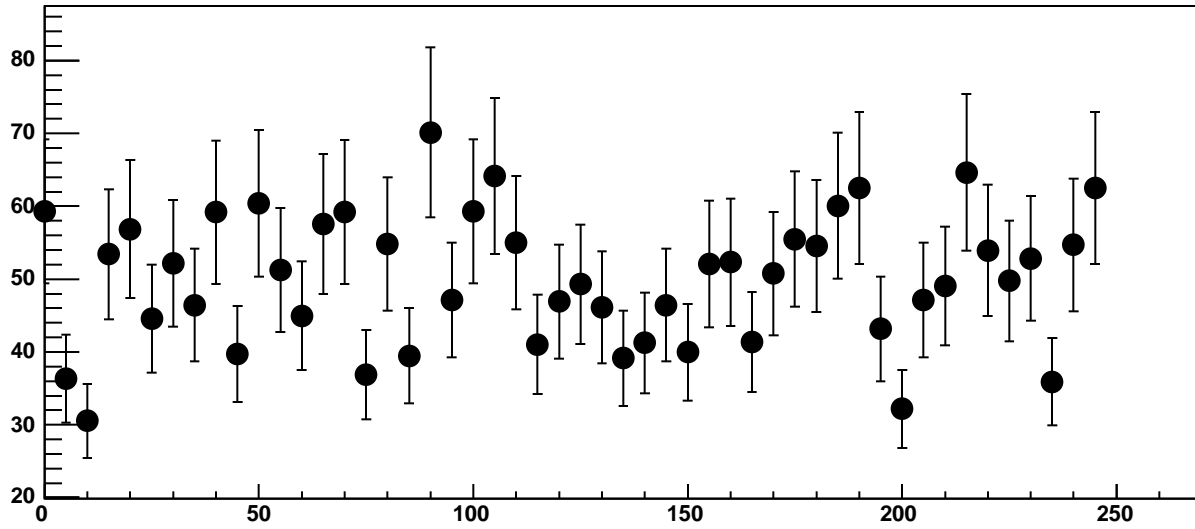


Chip 8, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold

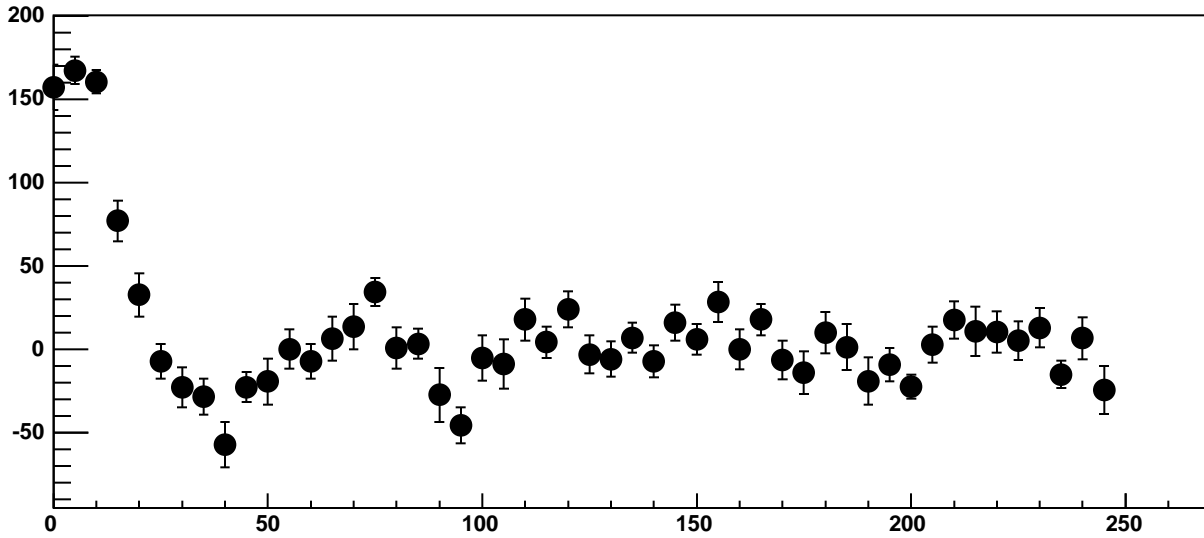


$\chi^2 / \text{ndf}$	165.9 / 41
p0	$-69.05 \pm 3.807$
p1	$91.66 \pm 0.7215$
p2	$-2.134\text{e}+08 \pm 4.124\text{e}+06$
p3	$2.221\text{e}+07 \pm 2.654\text{e}+05$
p4	$8.781 \pm 0.1253$

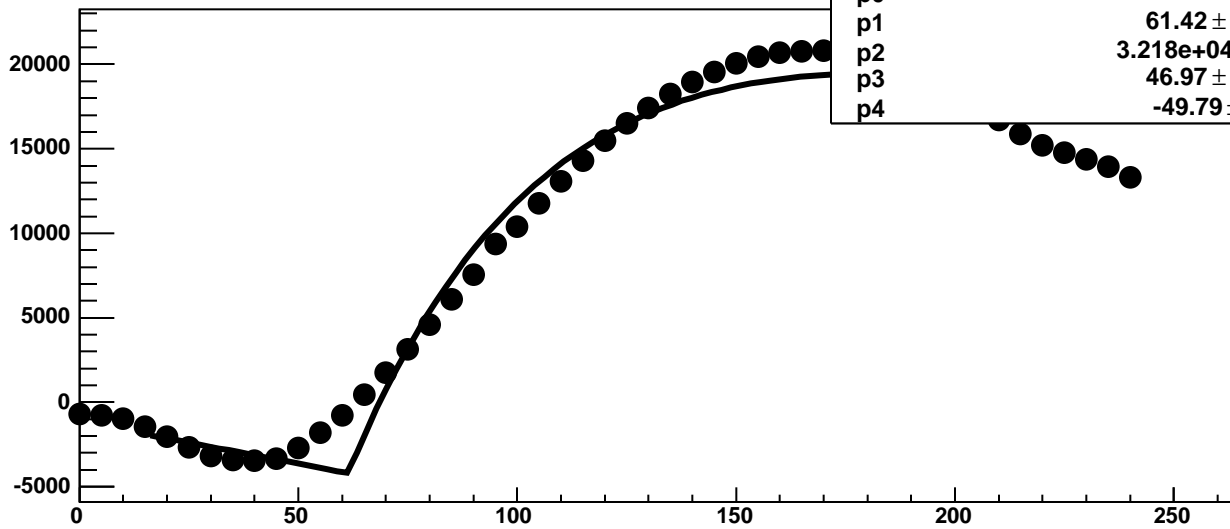
Chip 8, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

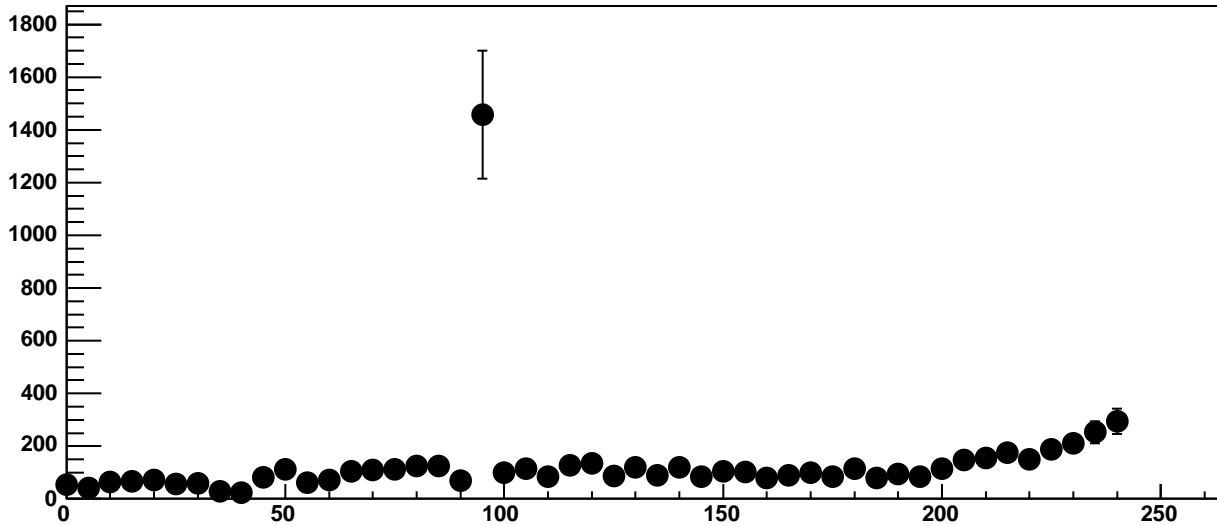


Chip 8, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

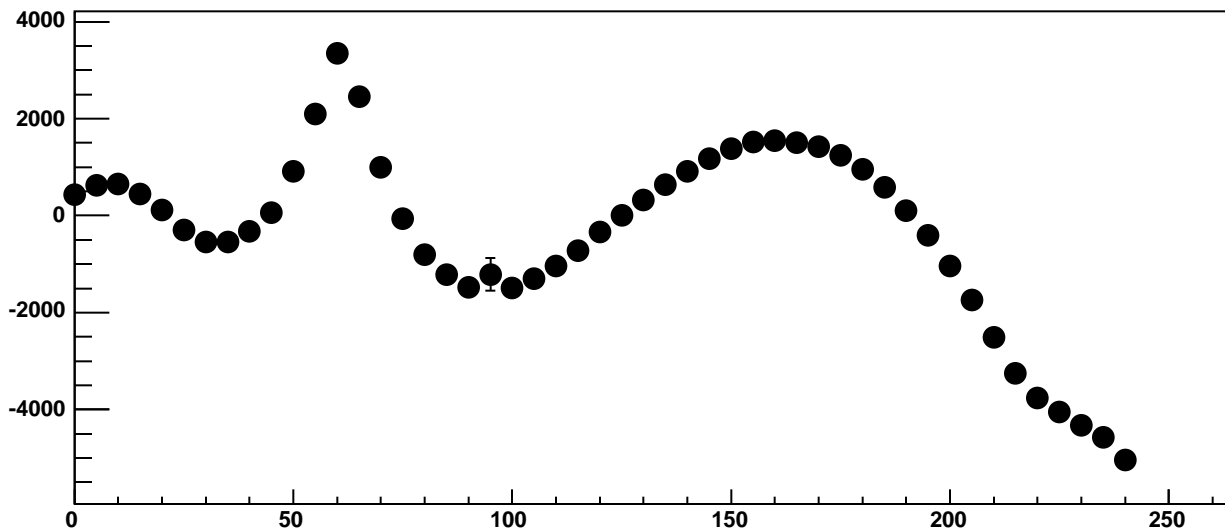


$\chi^2 / \text{ndf}$	2.023e+05 / 41
p0	-4199 ± 6.94
p1	61.42 ± 0.02935
p2	3.218e+04 ± 51.77
p3	46.97 ± 0.08724
p4	-49.79 ± 0.2672

Chip 8, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

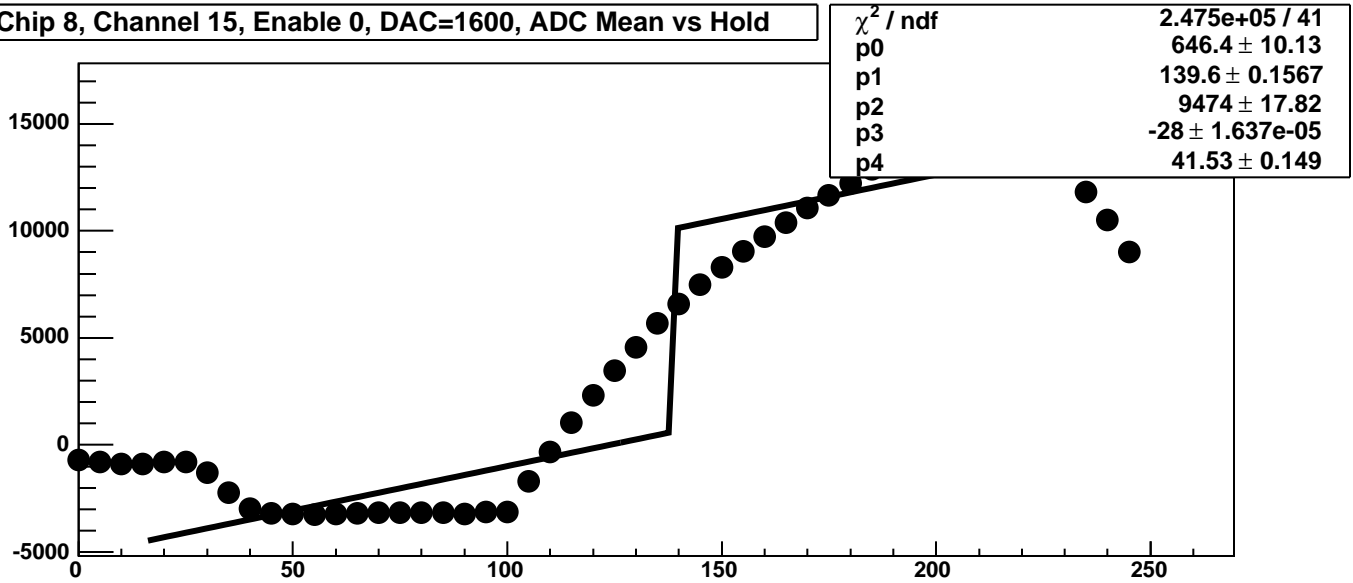


Chip 8, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

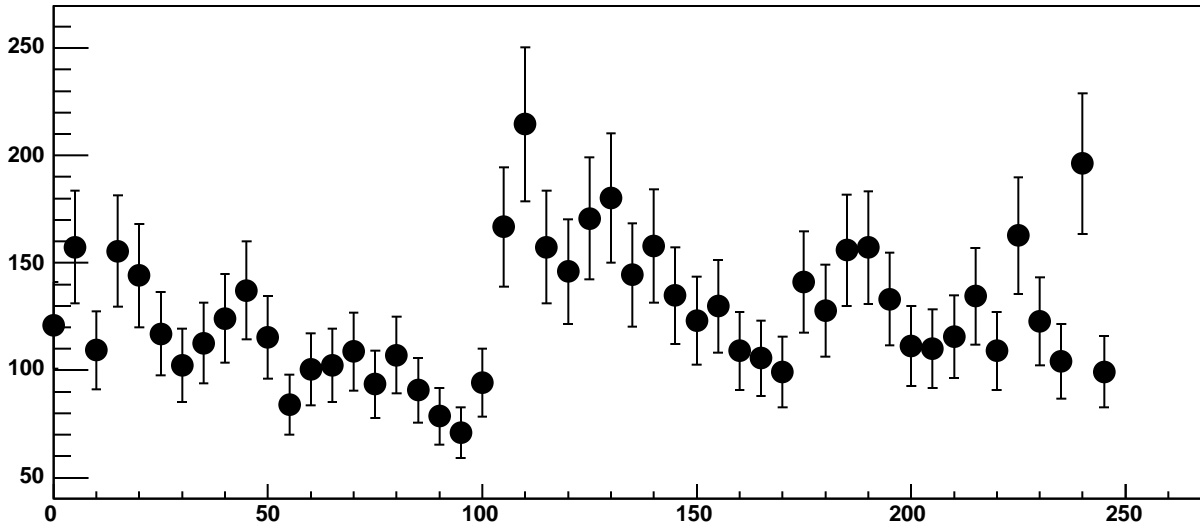




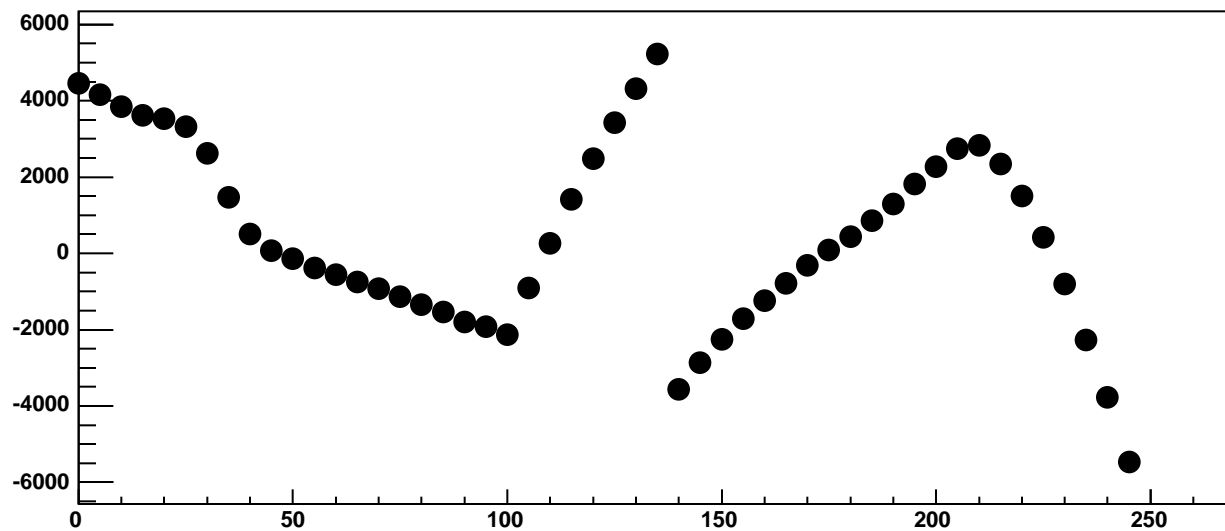
Chip 8, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold



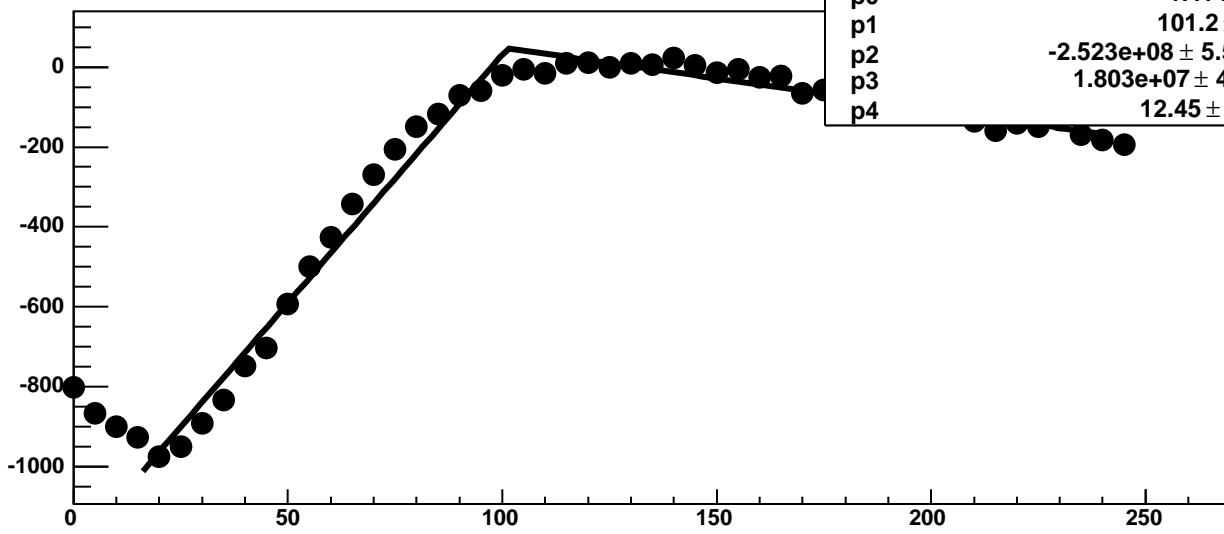
Chip 8, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

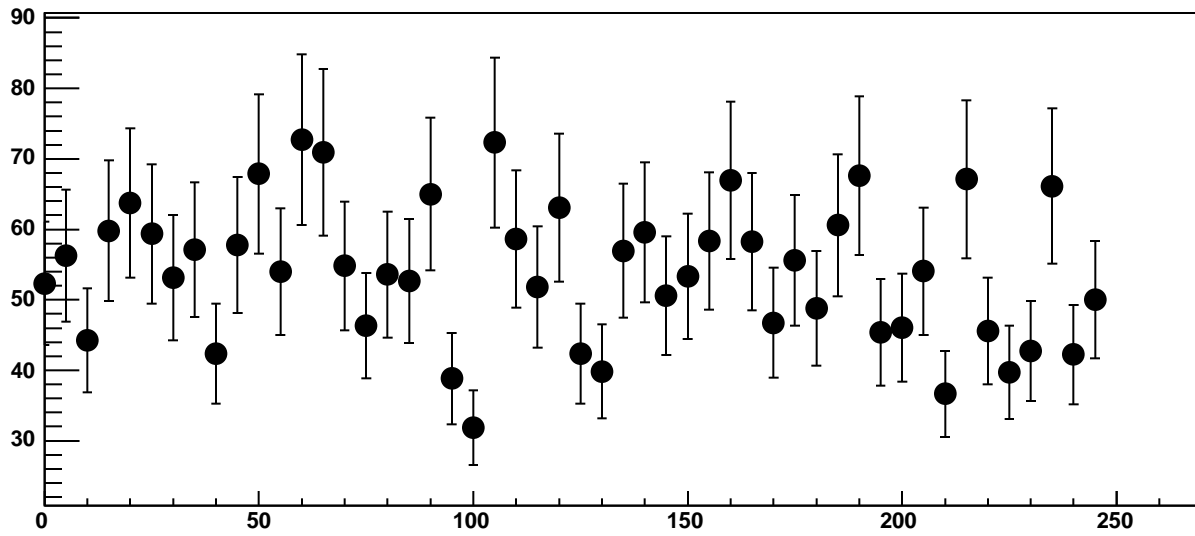


Chip 8, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

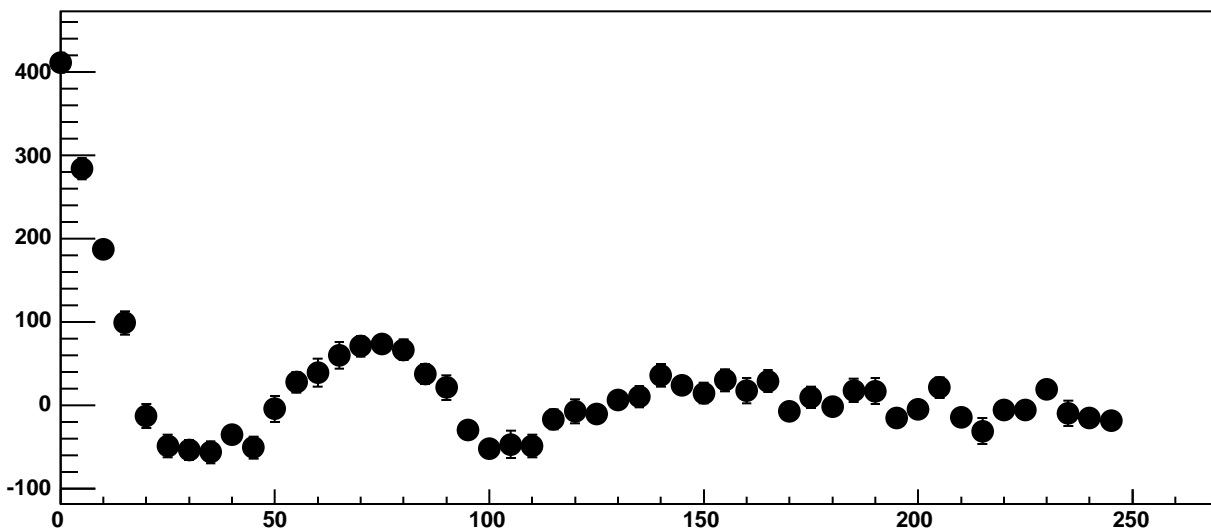


$\chi^2 / \text{ndf}$	413.6 / 41
p0	$47.14 \pm 4.099$
p1	$101.2 \pm 0.4581$
p2	$-2.523\text{e}+08 \pm 5.581\text{e}+06$
p3	$1.803\text{e}+07 \pm 4.11\text{e}+05$
p4	$12.45 \pm 0.09529$

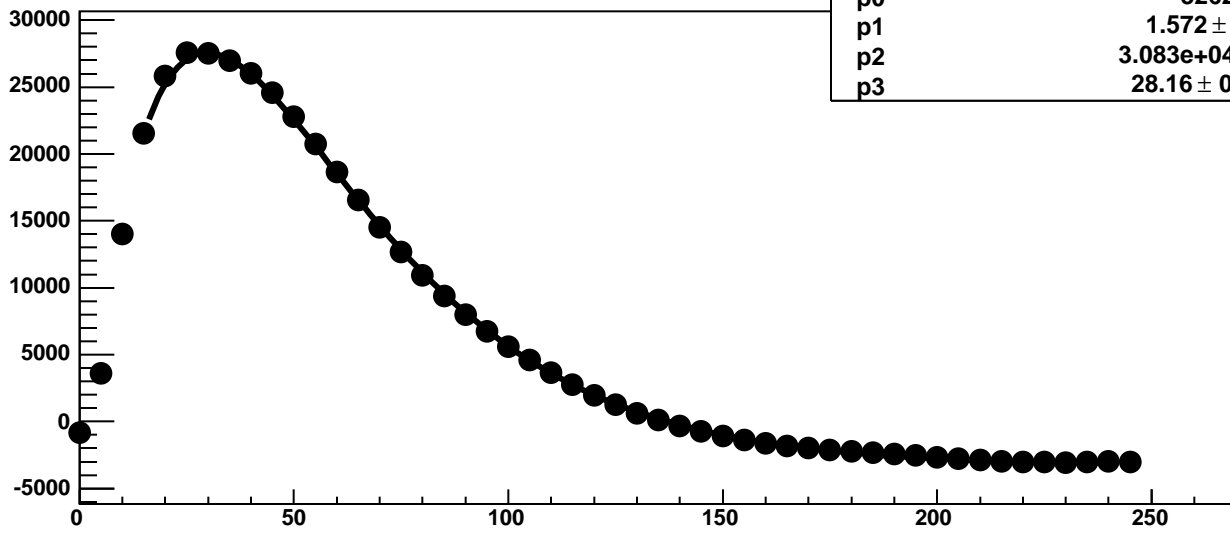
Chip 8, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

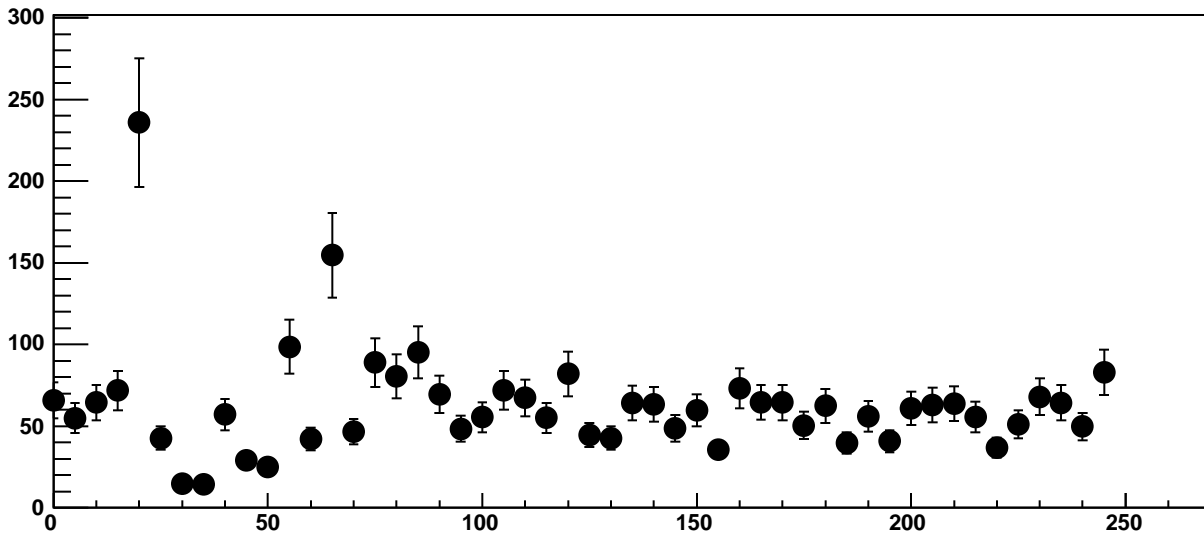


Chip 8, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold

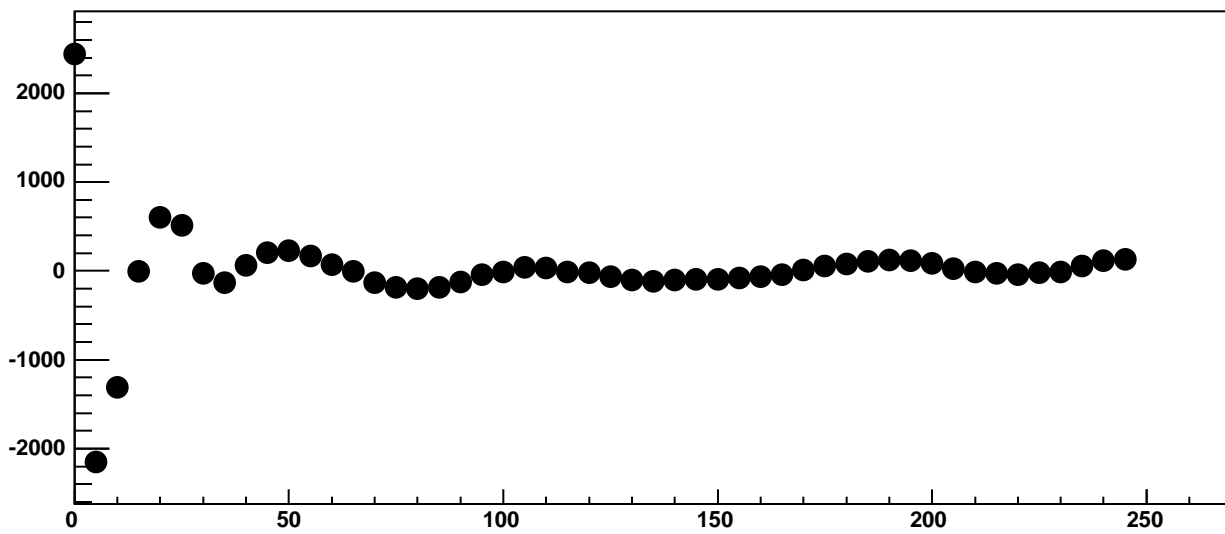


$\chi^2 / \text{ndf}$	8781 / 42
p0	-3262 ± 3.284
p1	1.572 ± 0.01652
p2	3.083e+04 ± 3.841
p3	28.16 ± 0.009614

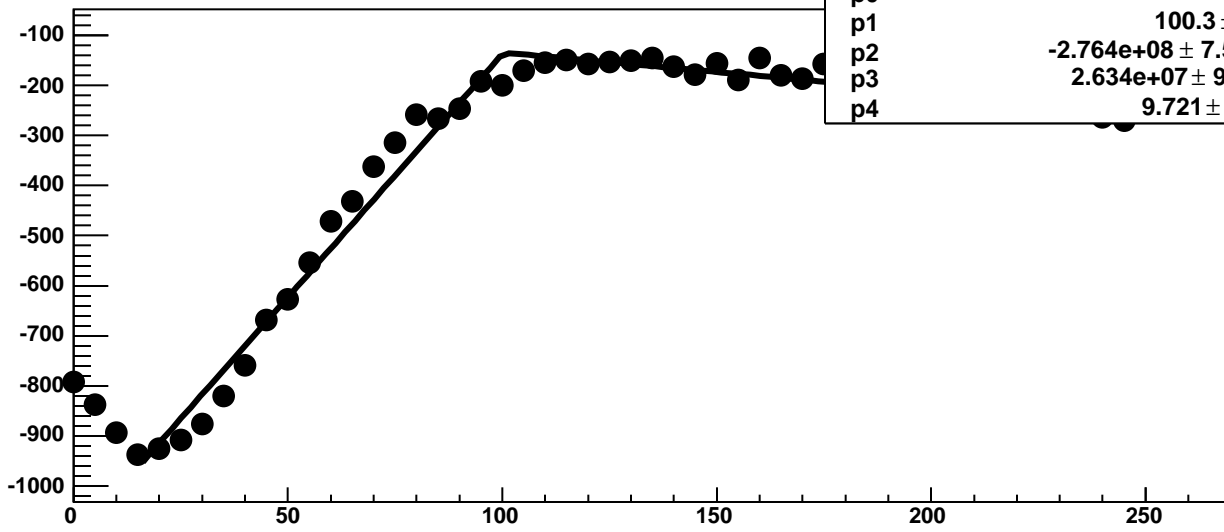
Chip 8, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

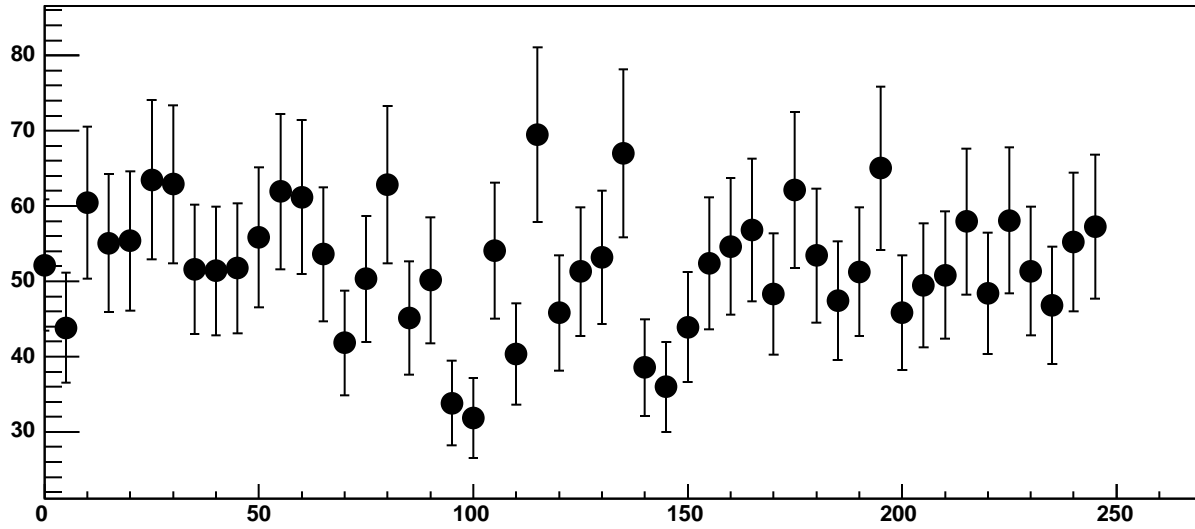


Chip 8, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

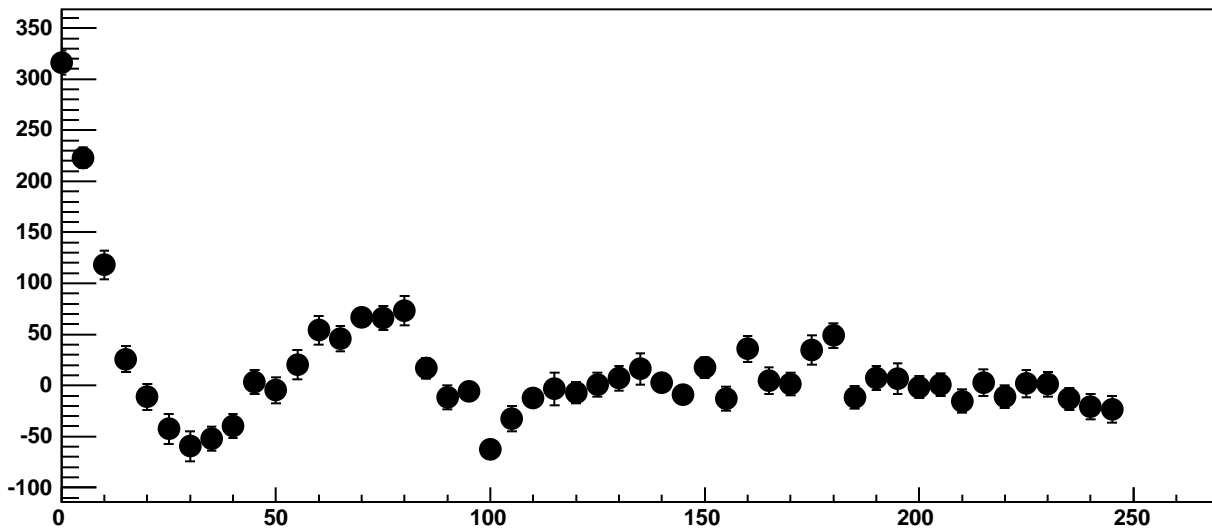


$\chi^2 / \text{ndf}$	331 / 41
p0	$-134.3 \pm 4.111$
p1	$100.3 \pm 0.5069$
p2	$-2.764\text{e}+08 \pm 7.529\text{e}+06$
p3	$2.634\text{e}+07 \pm 9.37\text{e}+05$
p4	$9.721 \pm 0.09915$

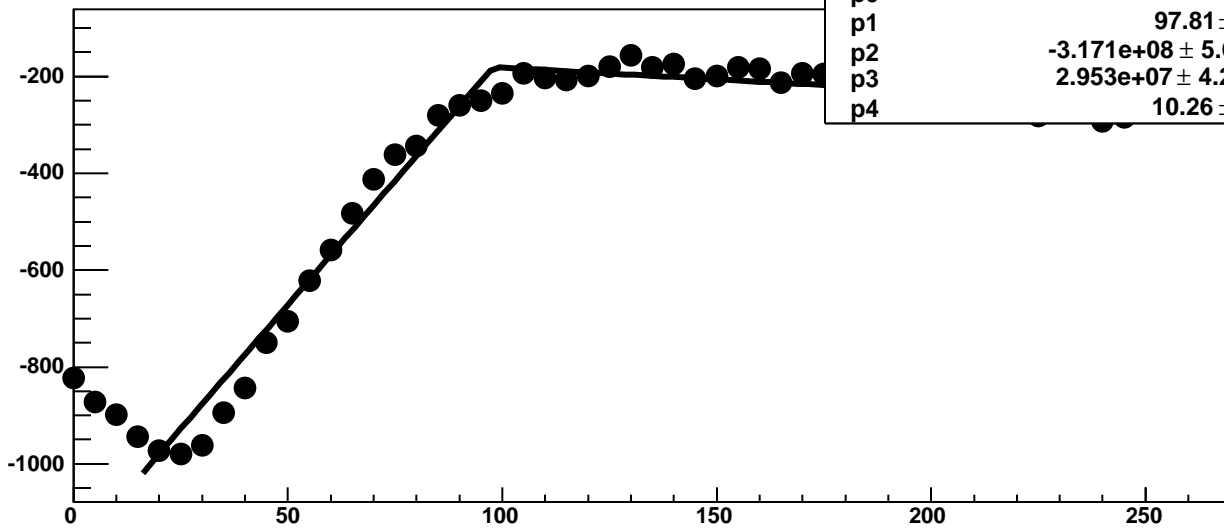
Chip 8, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

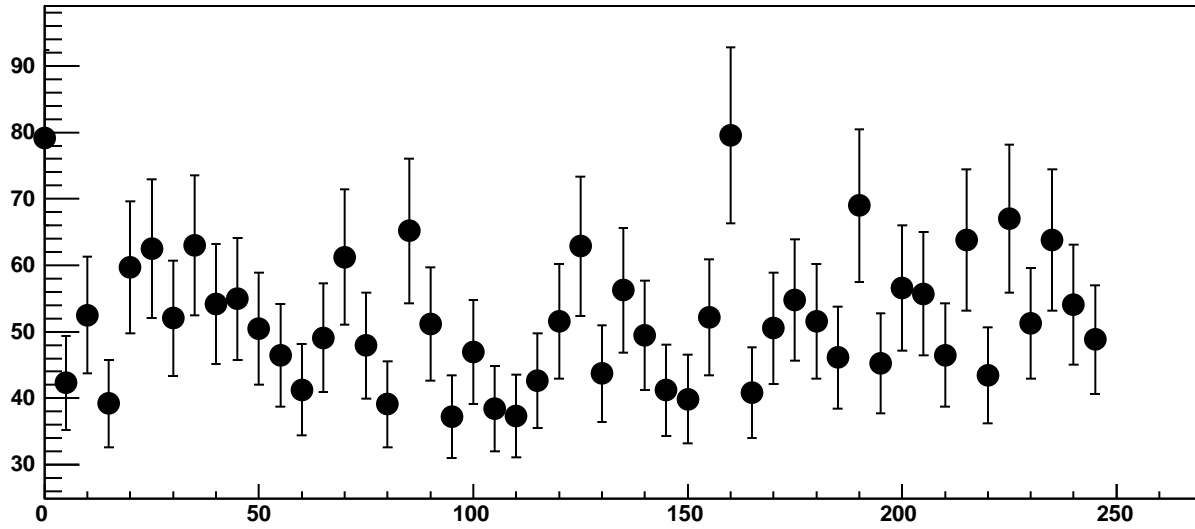


Chip 8, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

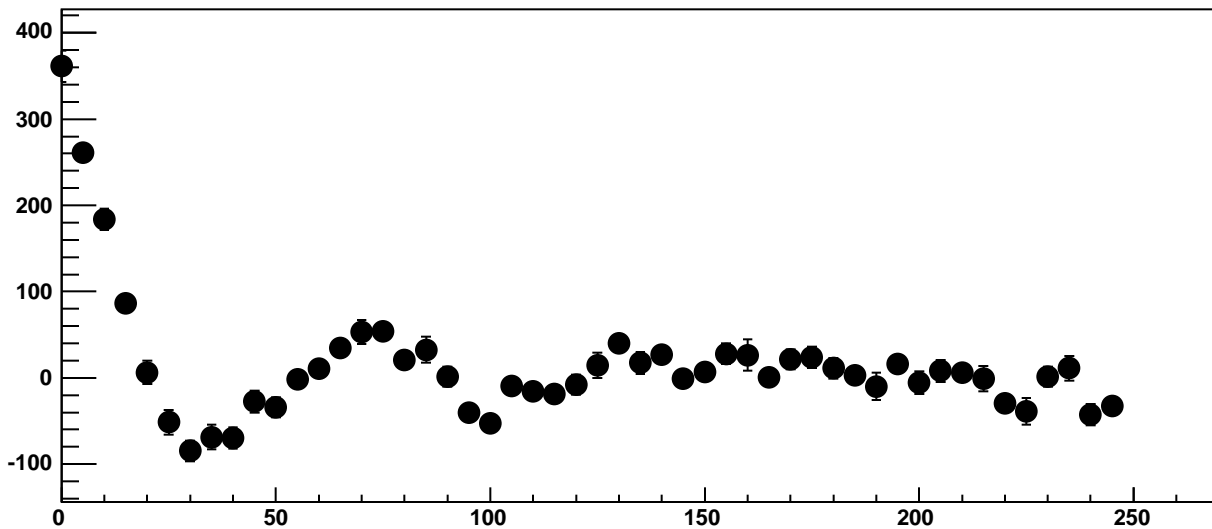


$\chi^2 / \text{ndf}$	408 / 41
p0	$-180.9 \pm 3.712$
p1	$97.81 \pm 0.5985$
p2	$-3.171\text{e}+08 \pm 5.651\text{e}+06$
p3	$2.953\text{e}+07 \pm 4.241\text{e}+05$
p4	$10.26 \pm 0.1074$

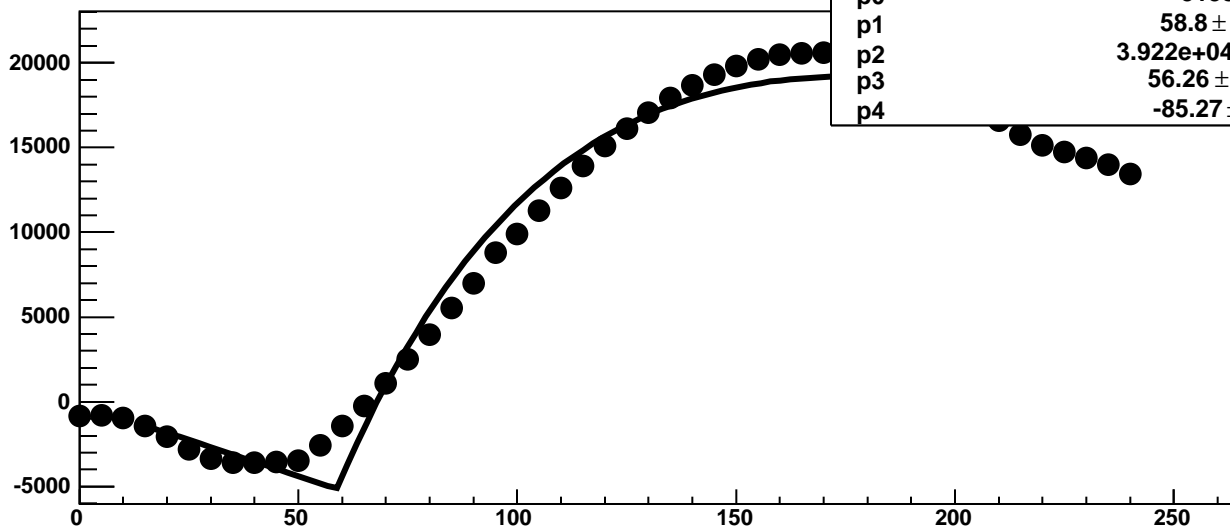
Chip 8, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

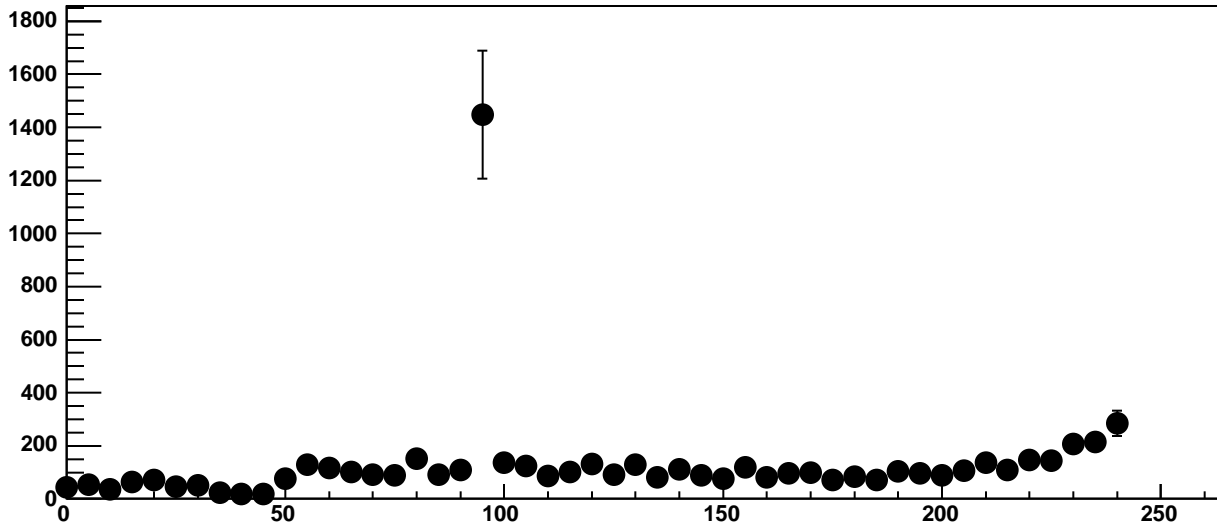


Chip 8, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

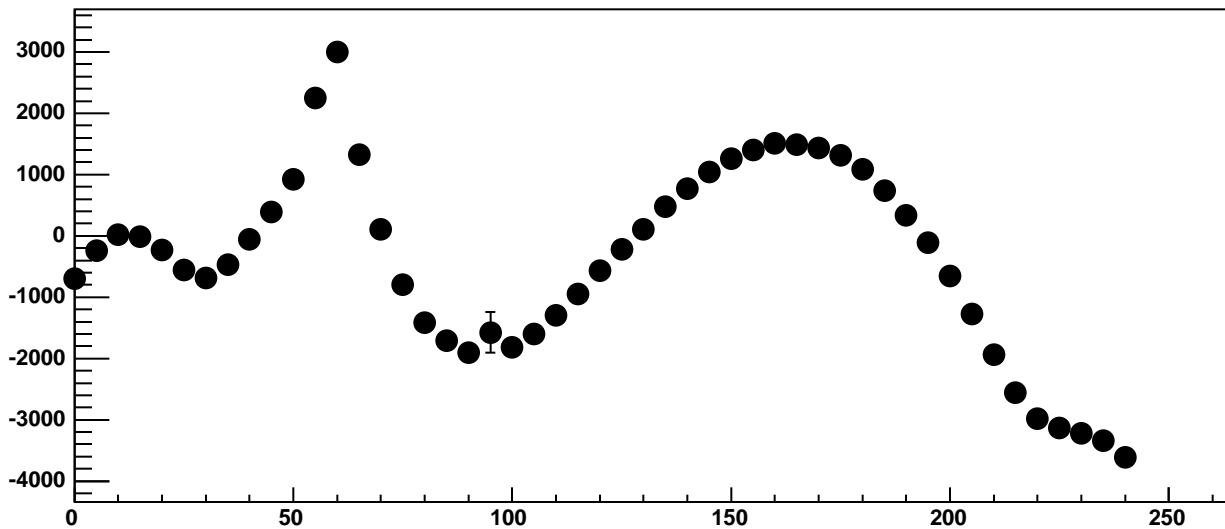


$\chi^2 / \text{ndf}$	1.601e+05 / 41
p0	-5138 ± 5.399
p1	58.8 ± 0.02376
p2	3.922e+04 ± 57.49
p3	56.26 ± 0.09151
p4	-85.27 ± 0.2703

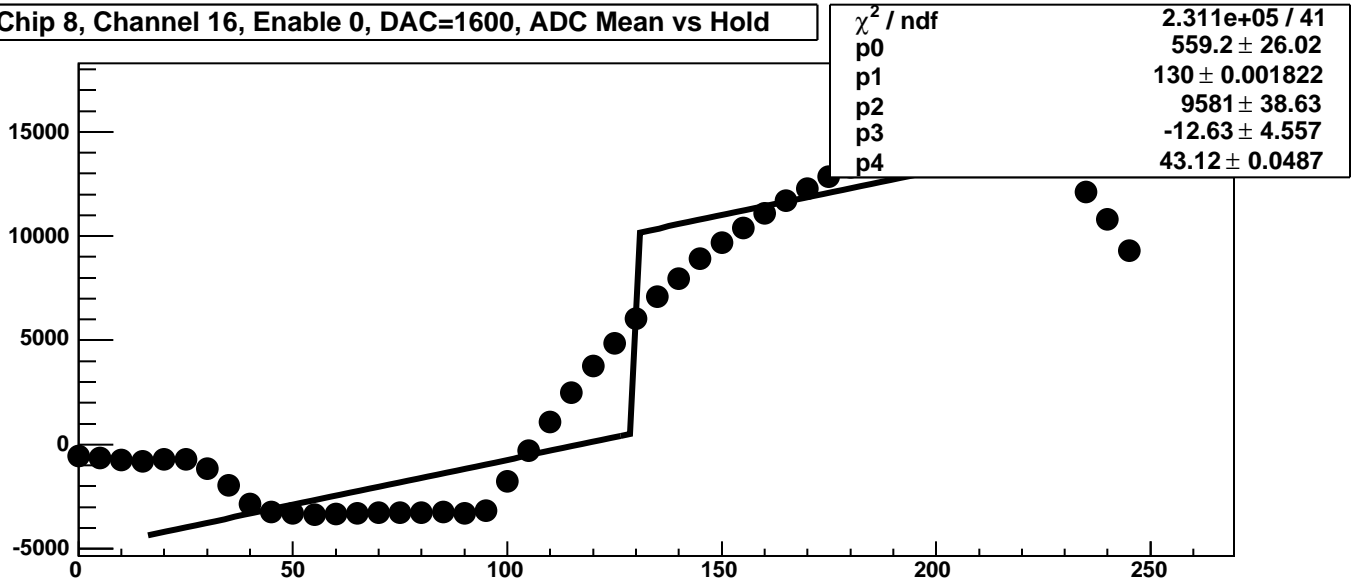
Chip 8, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



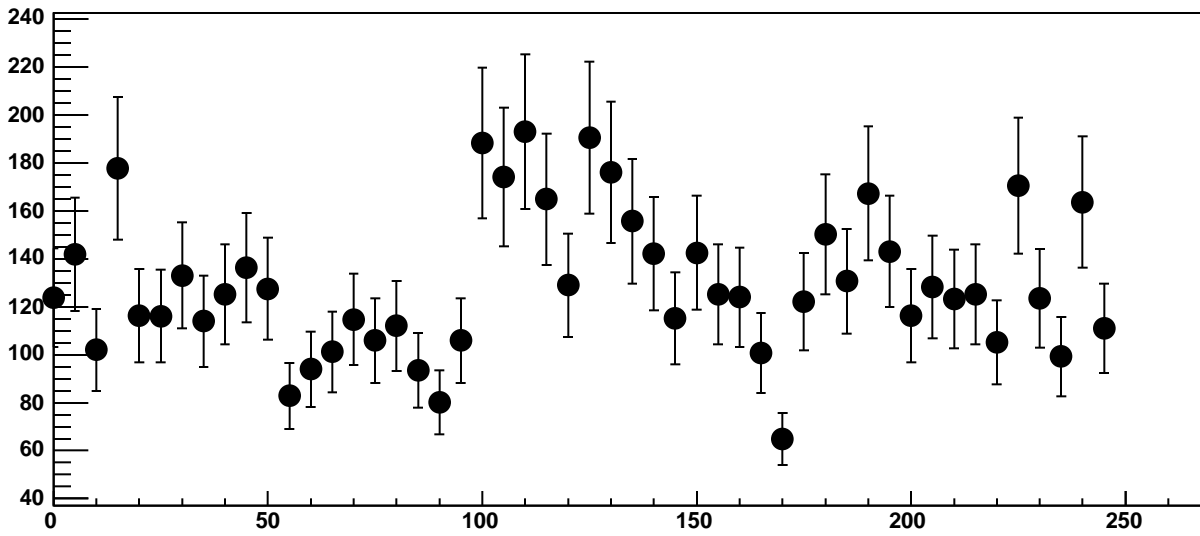
Chip 8, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold



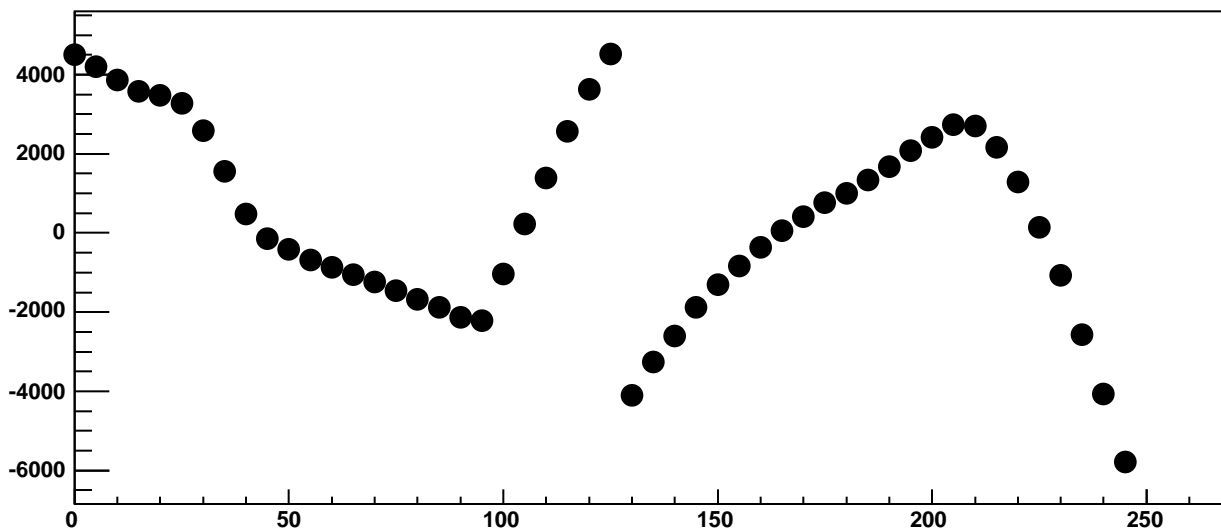
Chip 8, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold



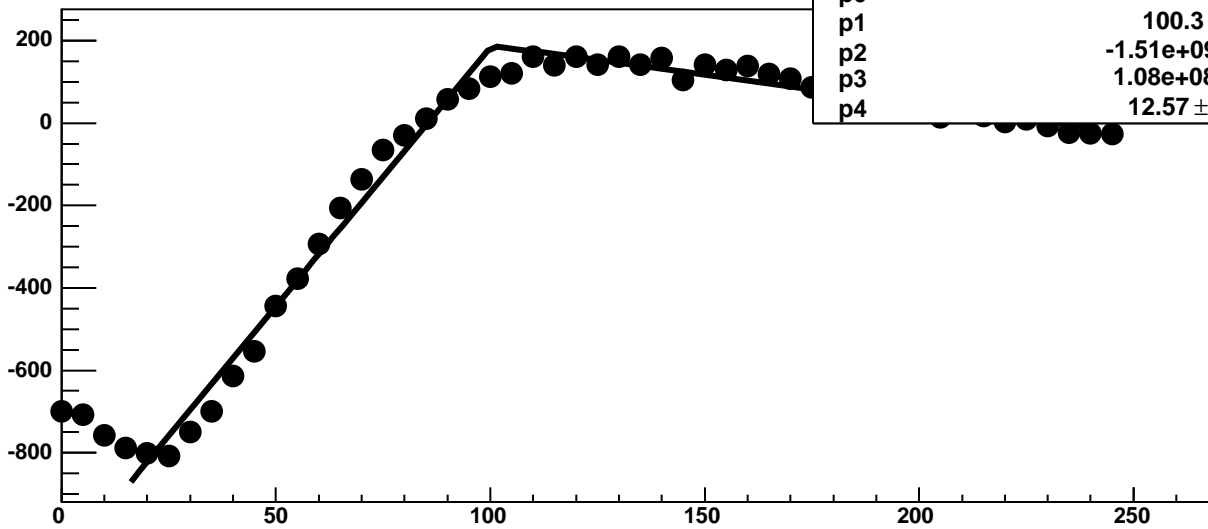
Chip 8, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

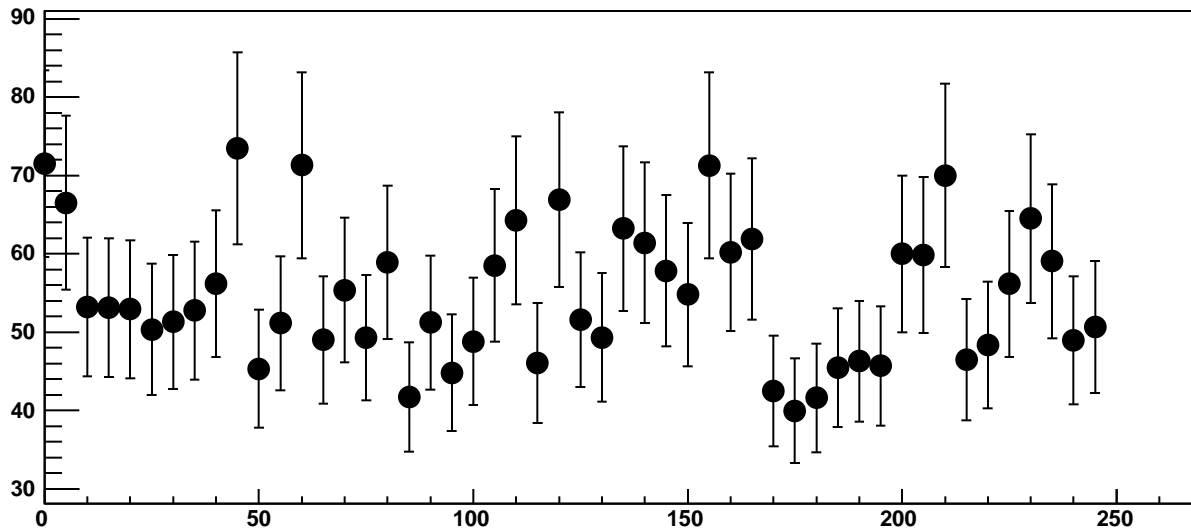


Chip 8, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

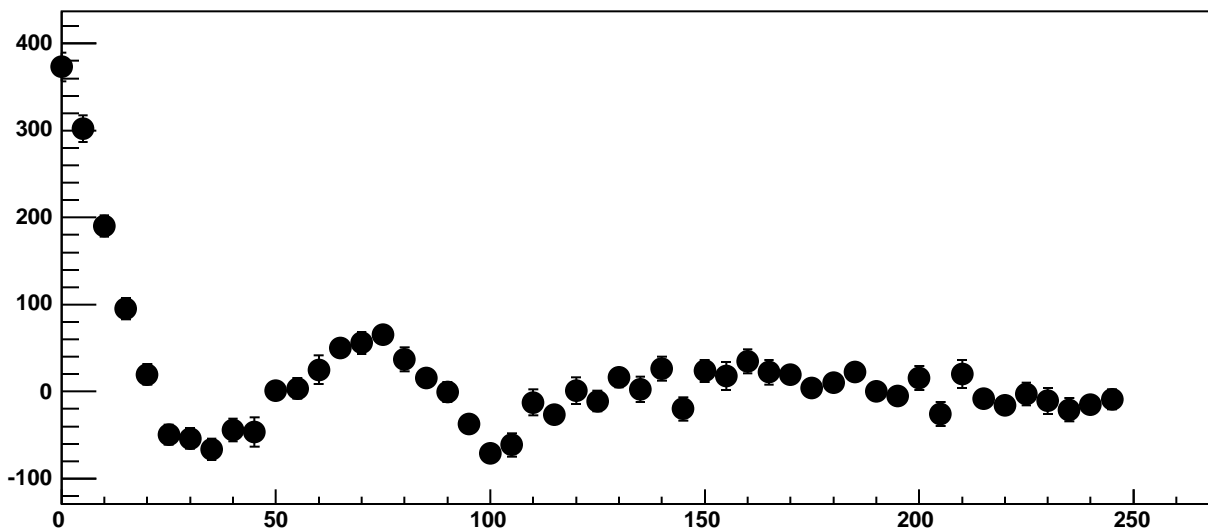


$\chi^2 / \text{ndf}$	366.8 / 41
p0	$188 \pm 1.321$
p1	$100.3 \pm 0.2843$
p2	$-1.51\text{e}+09 \pm 1.414$
p3	$1.08\text{e}+08 \pm 1.414$
p4	$12.57 \pm 0.03137$

Chip 8, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

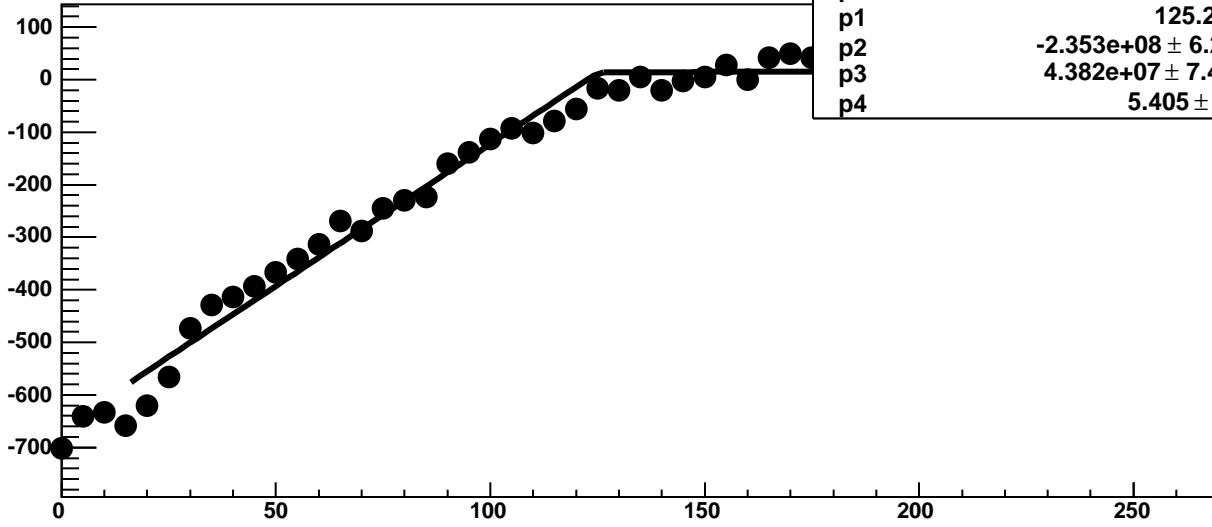


Chip 8, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



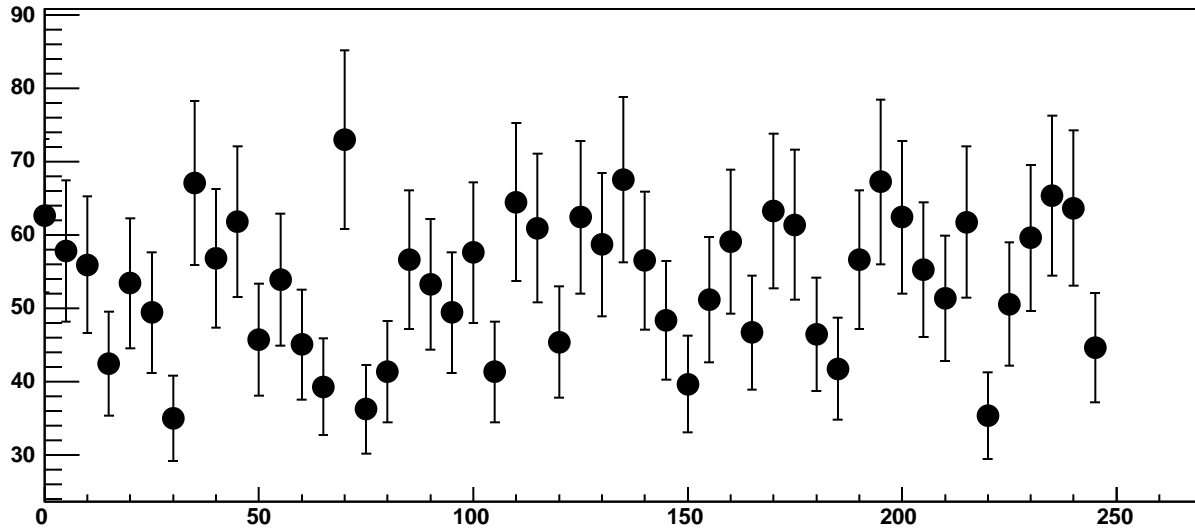


Chip 8, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold

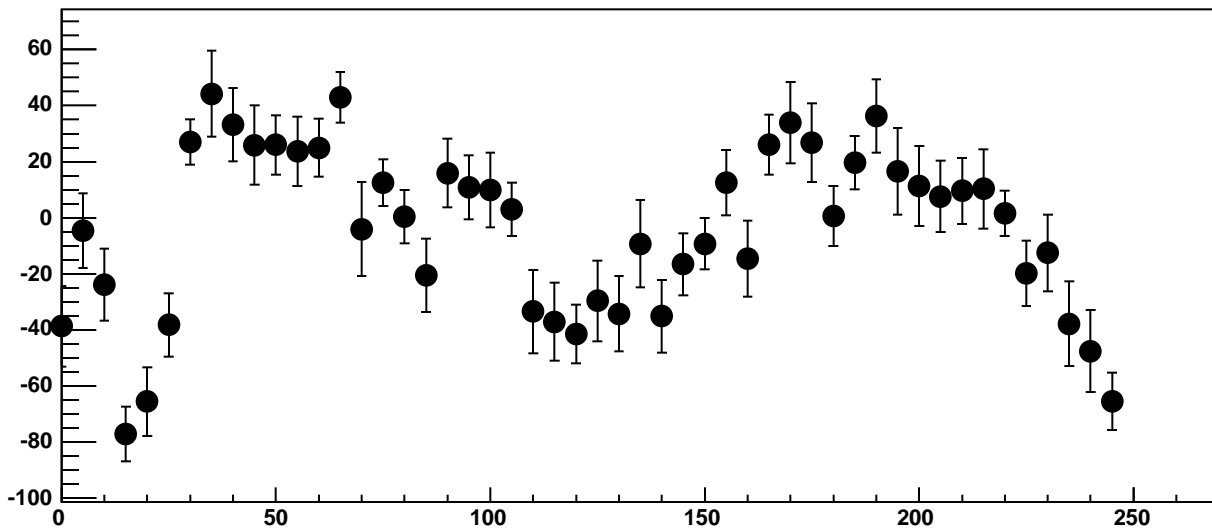


$\chi^2 / \text{ndf}$	281.3 / 41
p0	$13.82 \pm 5.348$
p1	$125.2 \pm 1.334$
p2	$-2.353\text{e}+08 \pm 6.224\text{e}+06$
p3	$4.382\text{e}+07 \pm 7.409\text{e}+05$
p4	$5.405 \pm 0.07238$

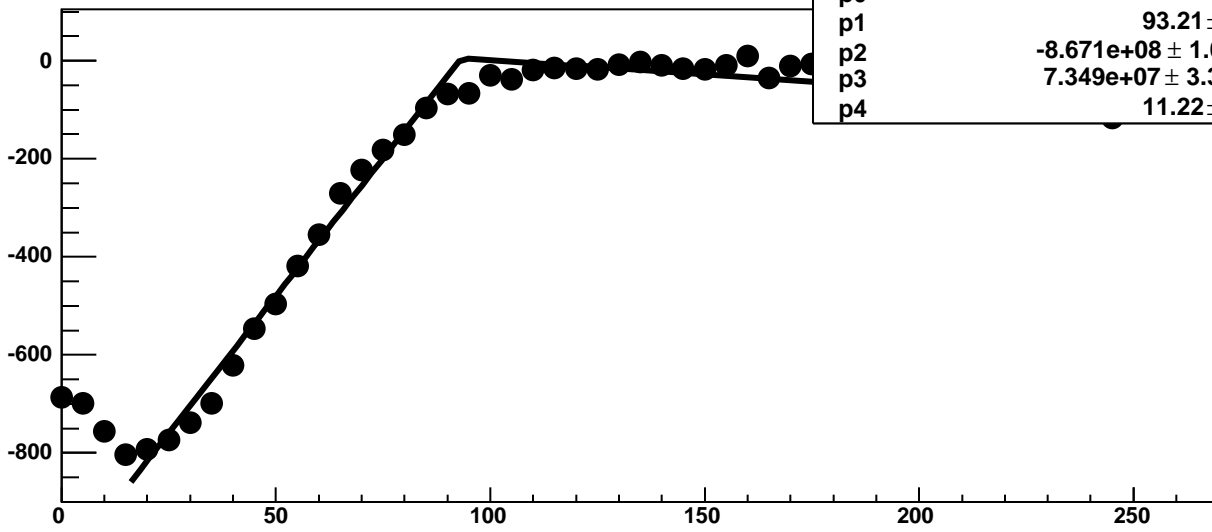
Chip 8, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

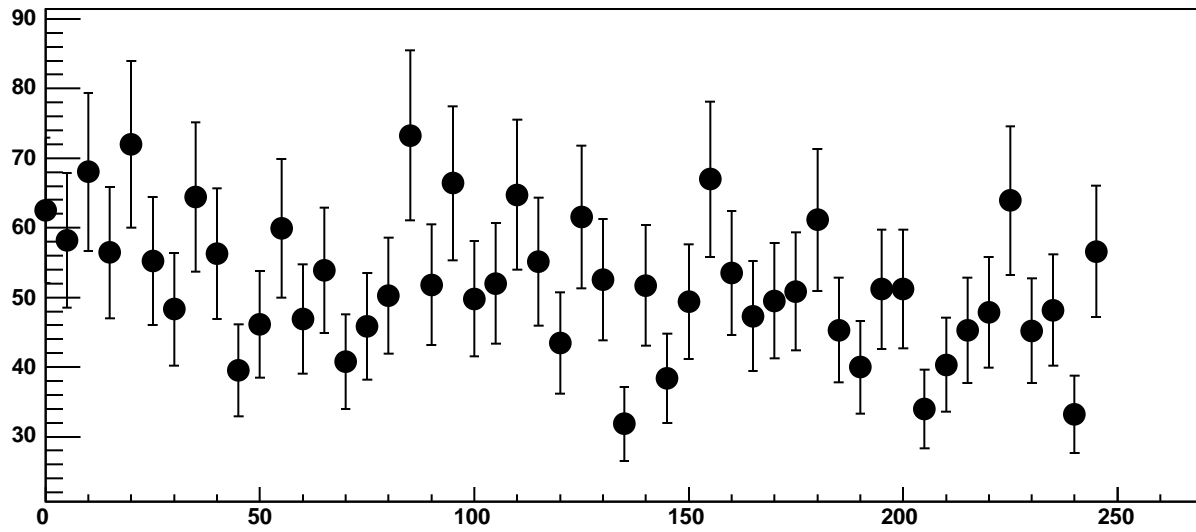


Chip 8, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

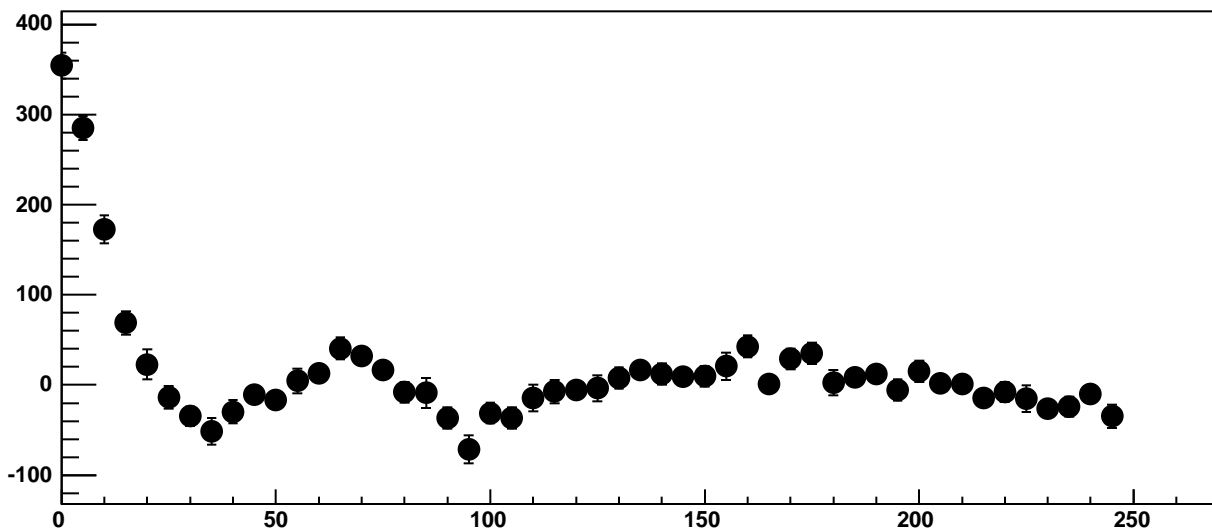


$\chi^2 / \text{ndf}$	198.9 / 41
p0	$5.402 \pm 3.982$
p1	$93.21 \pm 0.6245$
p2	$-8.671\text{e}+08 \pm 1.094\text{e}+07$
p3	$7.349\text{e}+07 \pm 3.383\text{e}+05$
p4	$11.22 \pm 0.1376$

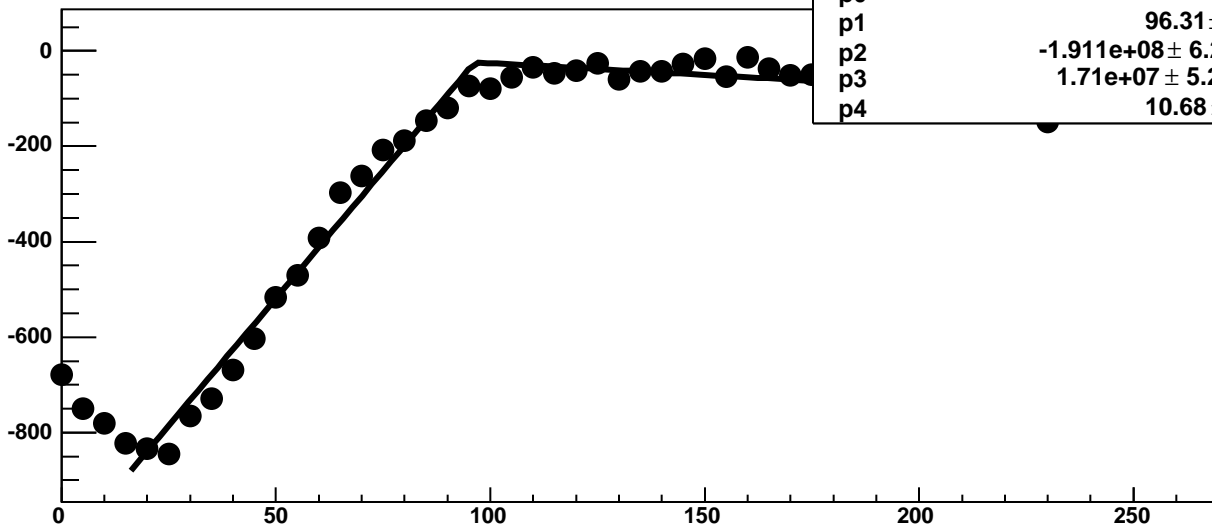
Chip 8, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold

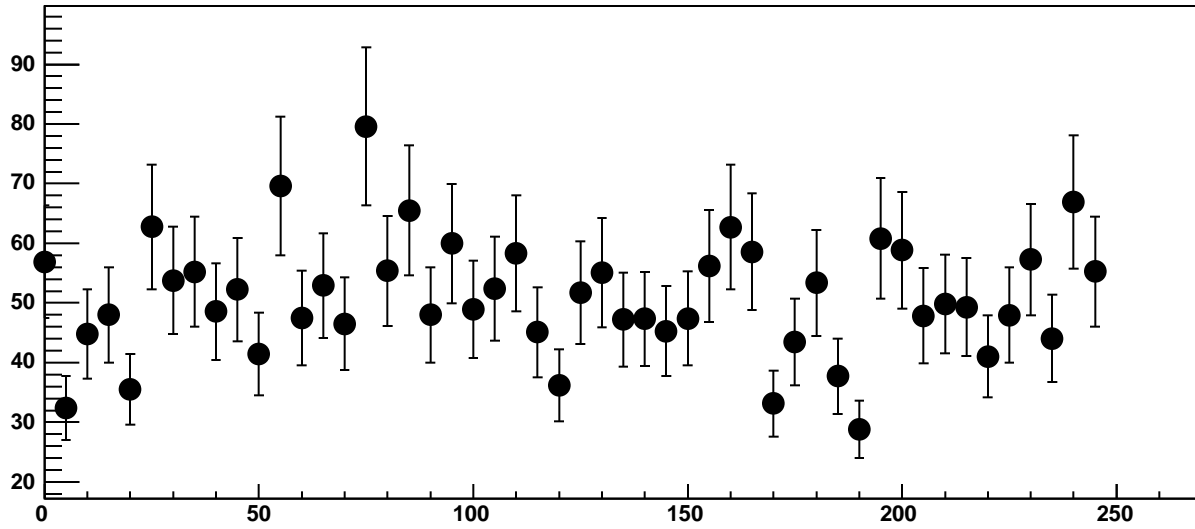


Chip 8, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

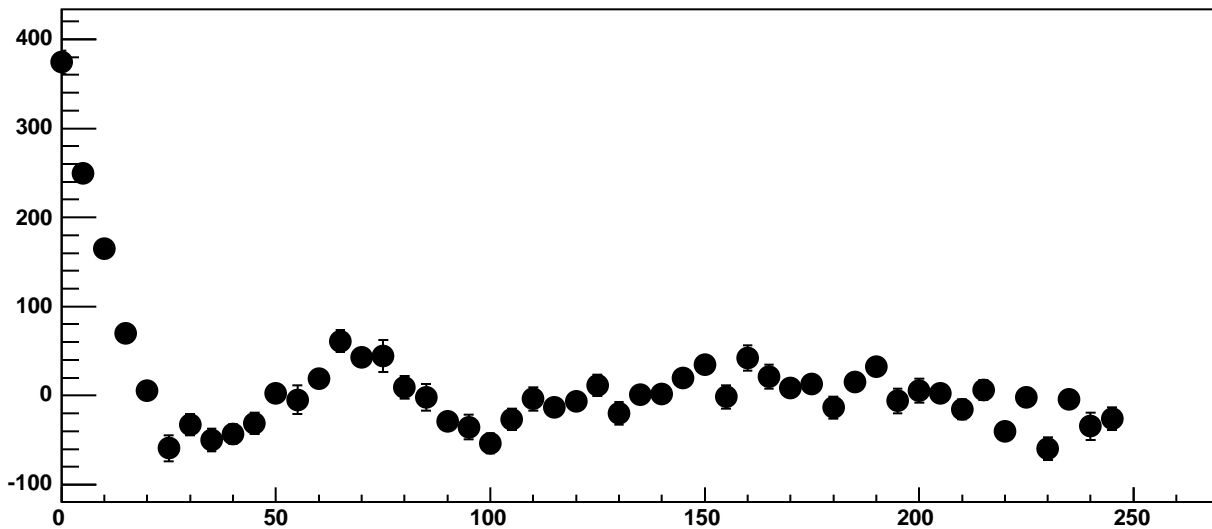


$\chi^2 / \text{ndf}$	304 / 41
p0	$-23.89 \pm 4.011$
p1	$96.31 \pm 0.6497$
p2	$-1.911\text{e}+08 \pm 6.251\text{e}+06$
p3	$1.71\text{e}+07 \pm 5.235\text{e}+05$
p4	$10.68 \pm 0.1161$

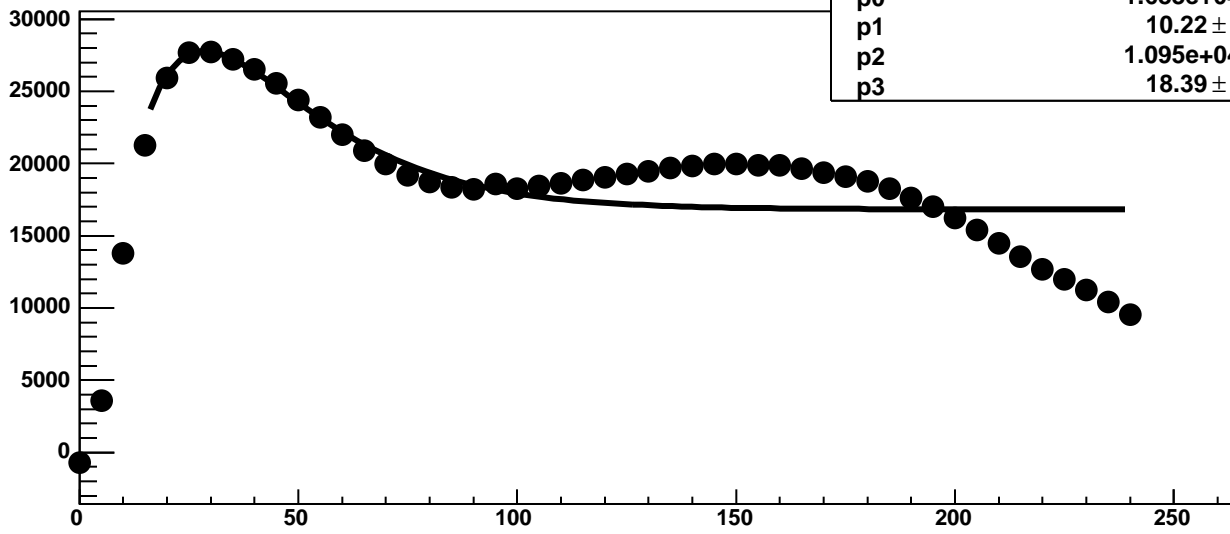
Chip 8, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

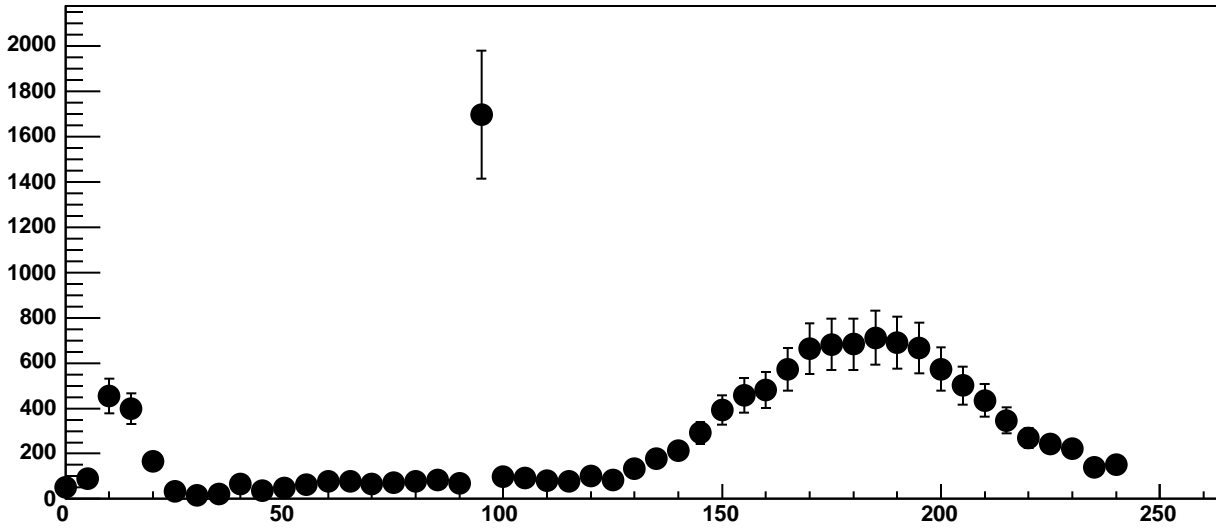


Chip 8, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

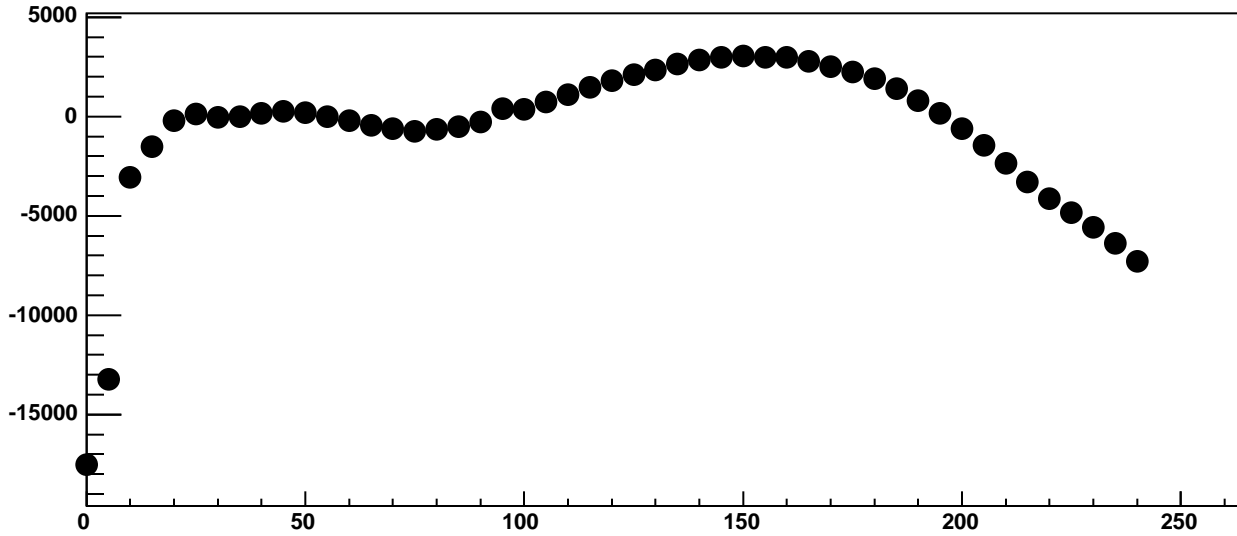


$\chi^2 / \text{ndf}$	1.684e+05 / 42
p0	1.683e+04 $\pm$ 9.27
p1	10.22 $\pm$ 0.05389
p2	1.095e+04 $\pm$ 9.39
p3	18.39 $\pm$ 0.03488

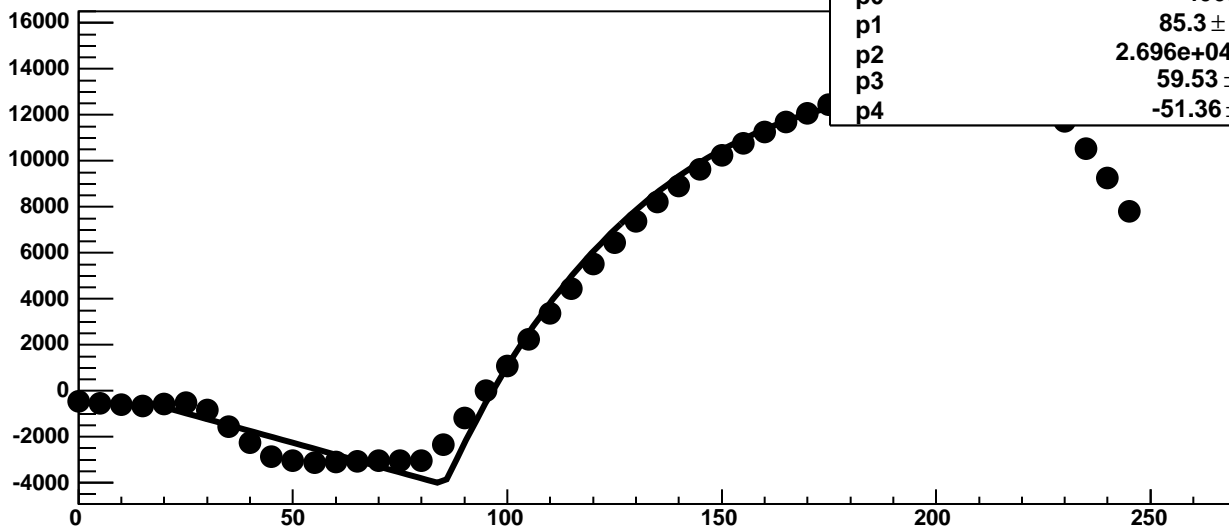
Chip 8, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

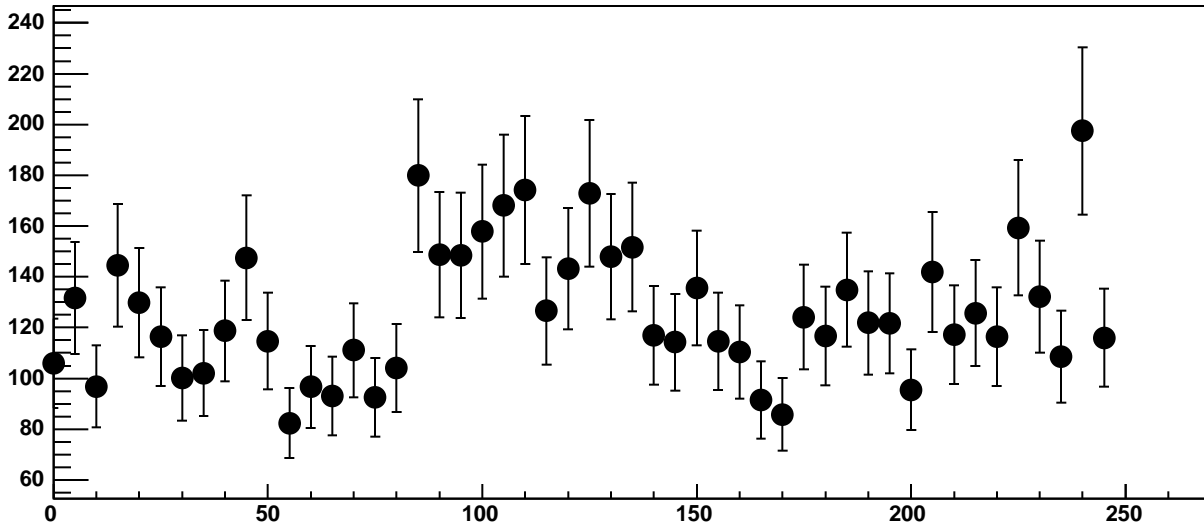


Chip 8, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

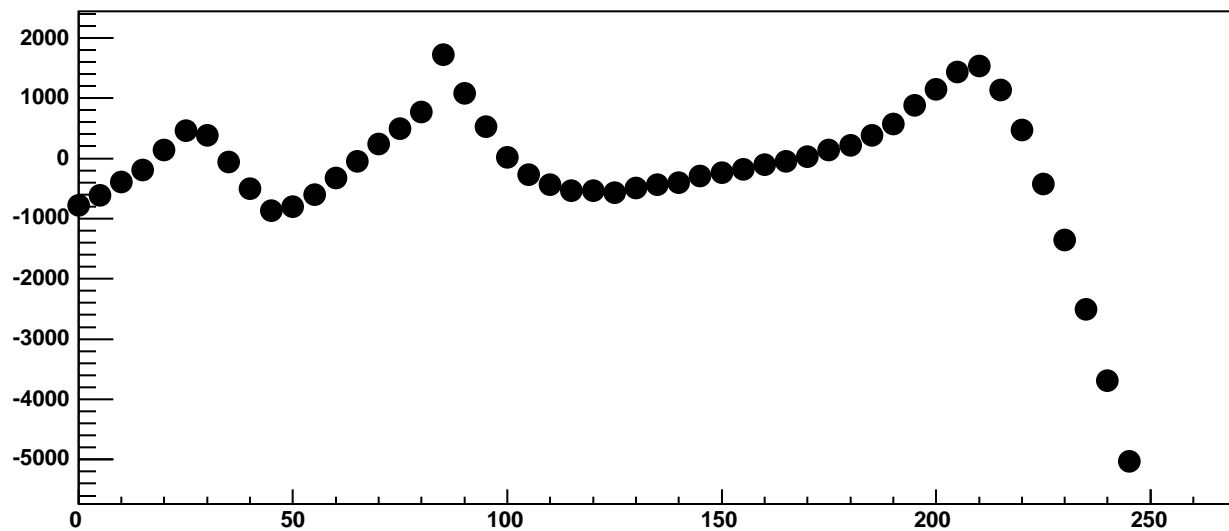


$\chi^2 / \text{ndf}$	4.063e+04 / 41
p0	-4067 ± 11.01
p1	85.3 ± 0.06276
p2	2.696e+04 ± 73.05
p3	59.53 ± 0.1944
p4	-51.36 ± 0.3083

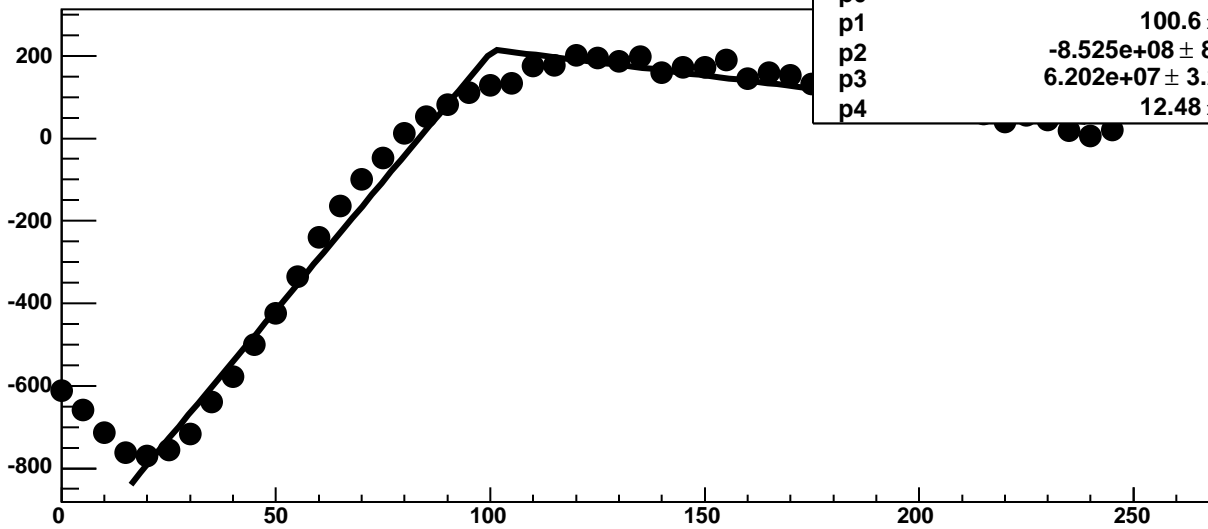
Chip 8, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

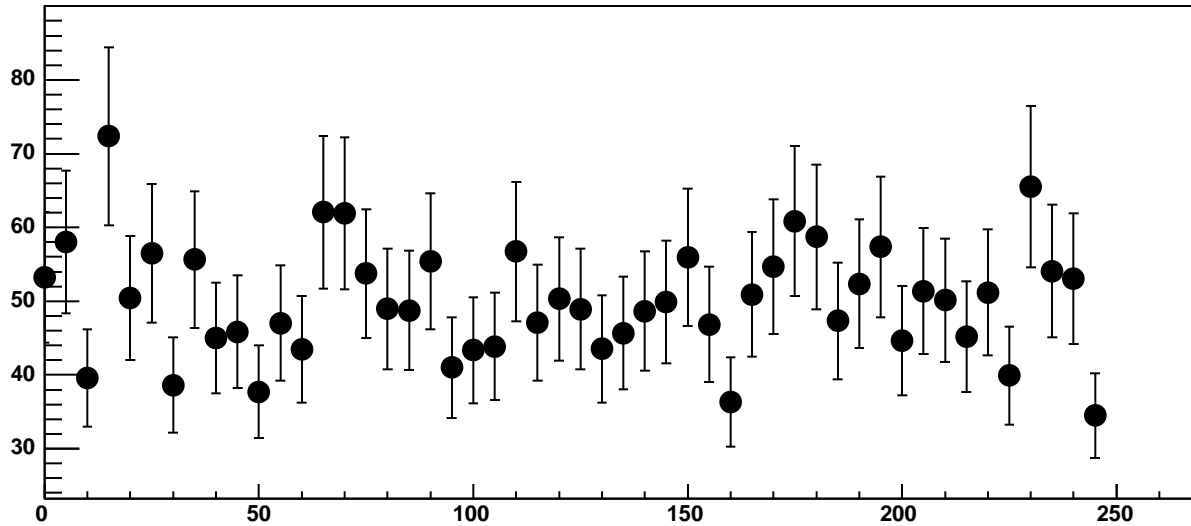


Chip 8, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

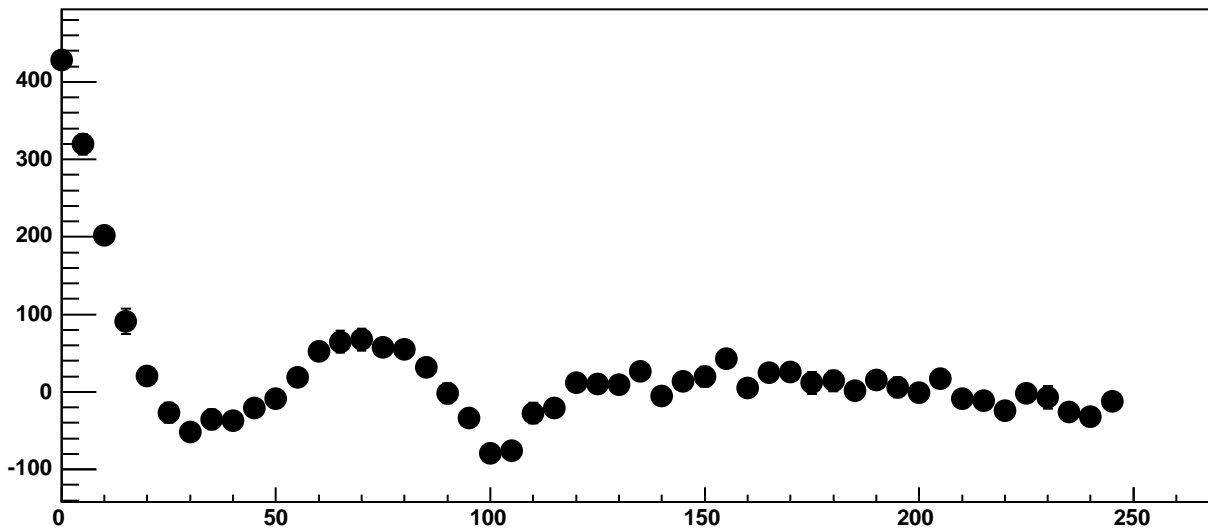


$\chi^2 / \text{ndf}$	428.8 / 41
p0	$215.1 \pm 3.907$
p1	$100.6 \pm 0.4795$
p2	$-8.525\text{e}+08 \pm 8.25\text{e}+06$
p3	$6.202\text{e}+07 \pm 3.221\text{e}+05$
p4	$12.48 \pm 0.1025$

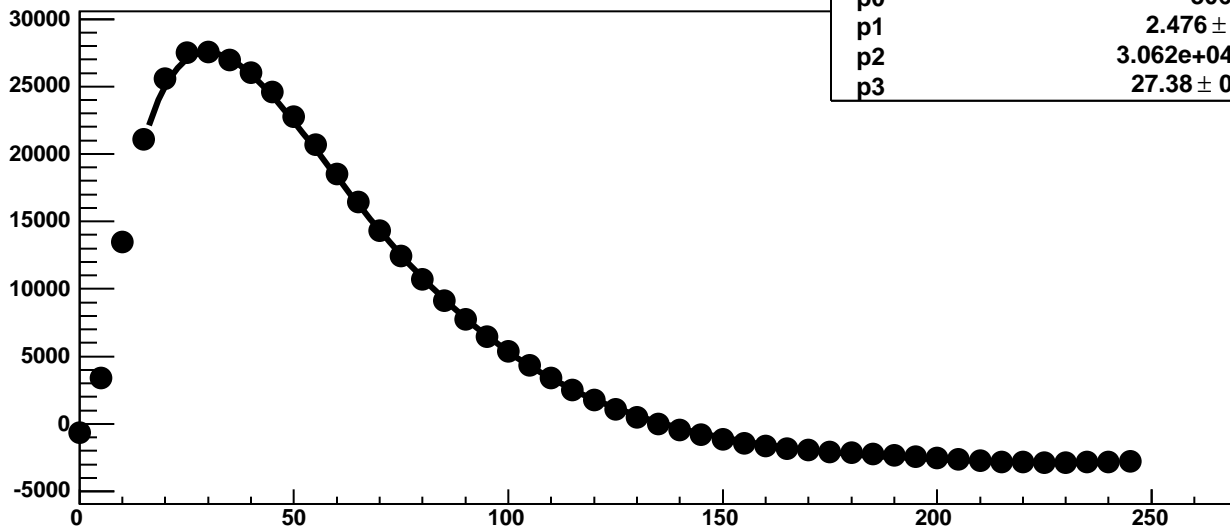
Chip 8, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

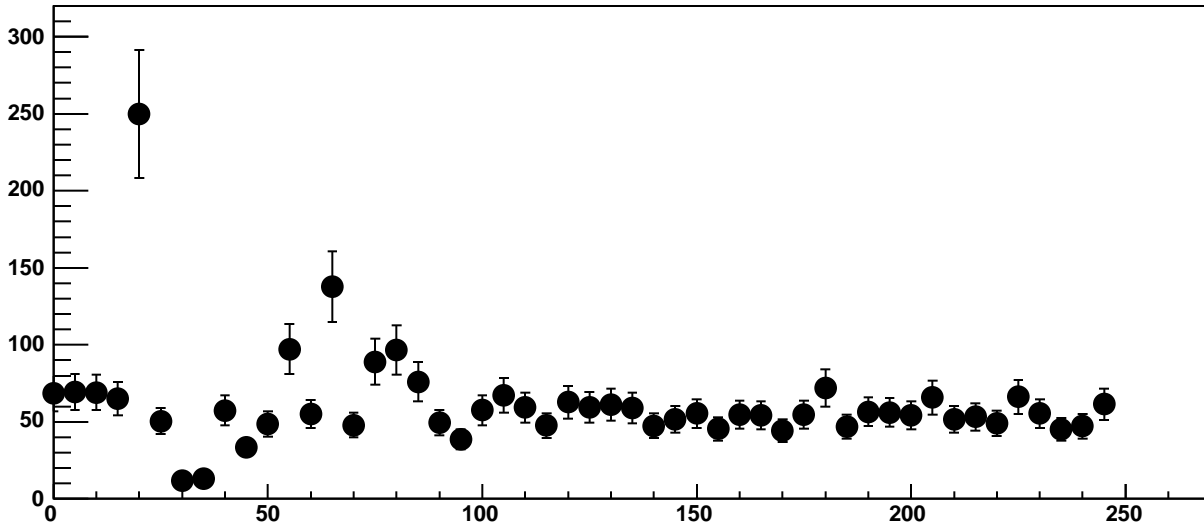


Chip 8, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

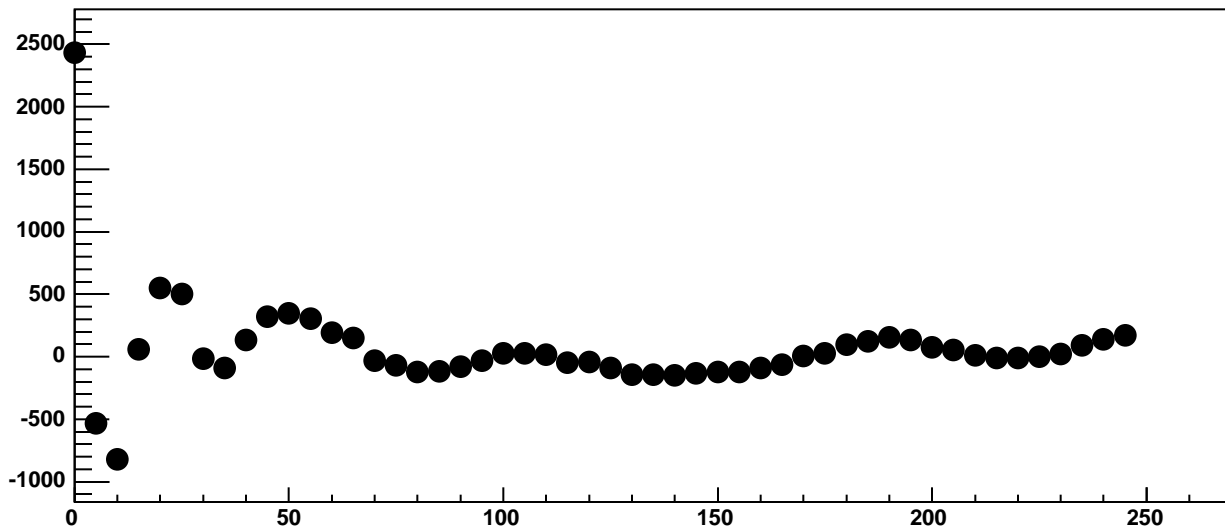


$\chi^2 / \text{ndf}$	7975 / 42
p0	-3068 ± 3.21
p1	2.476 ± 0.01455
p2	3.062e+04 ± 3.666
p3	27.38 ± 0.008634

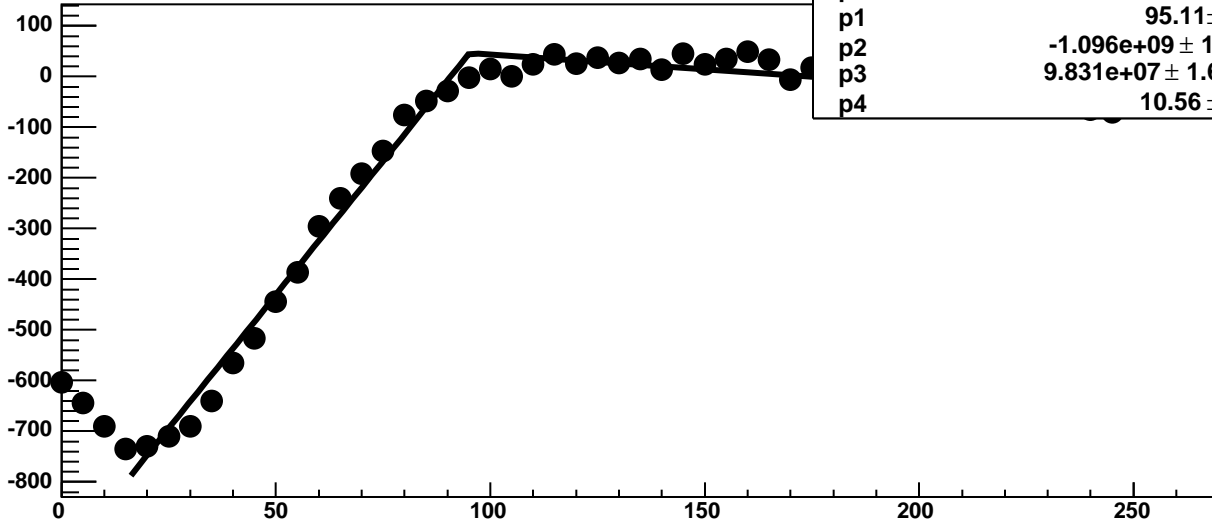
Chip 8, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

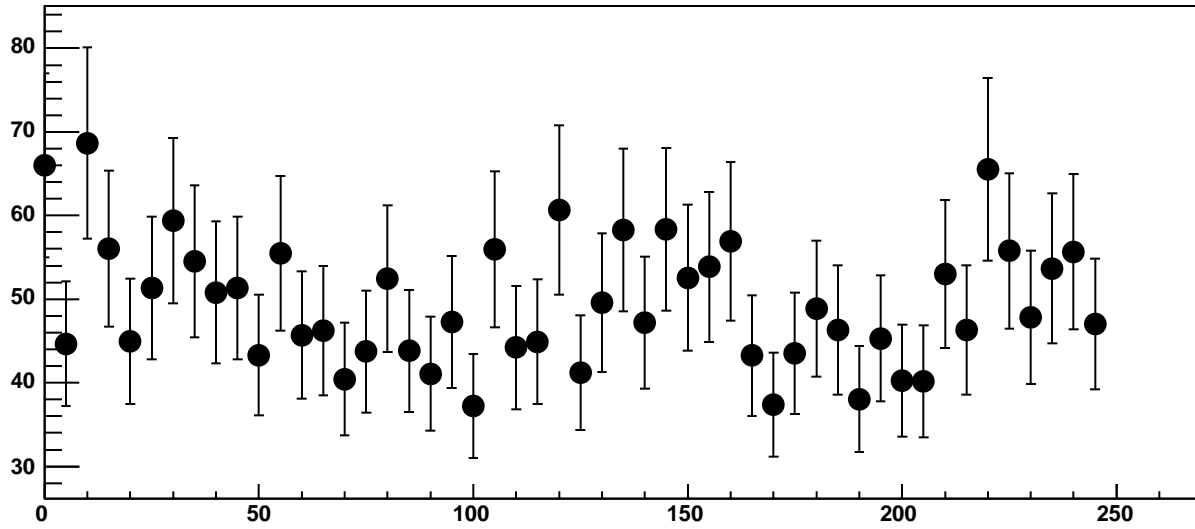


Chip 8, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

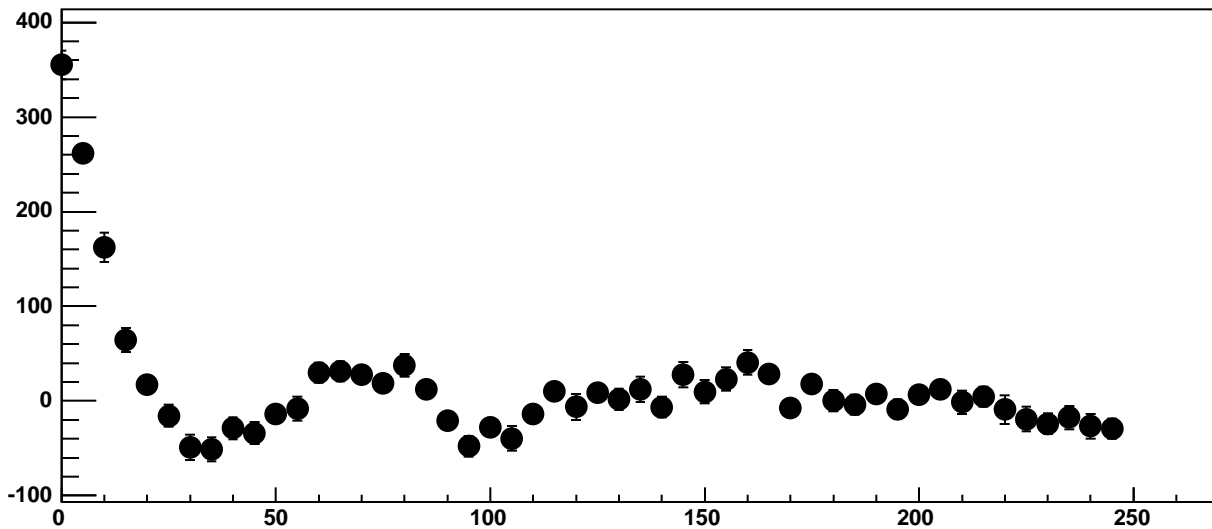


$\chi^2 / \text{ndf}$	214.4 / 41
p0	$46.12 \pm 3.933$
p1	$95.11 \pm 0.5736$
p2	$-1.096\text{e}+09 \pm 1.19\text{e}+07$
p3	$9.831\text{e}+07 \pm 1.665\text{e}+05$
p4	$10.56 \pm 0.1096$

Chip 8, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold

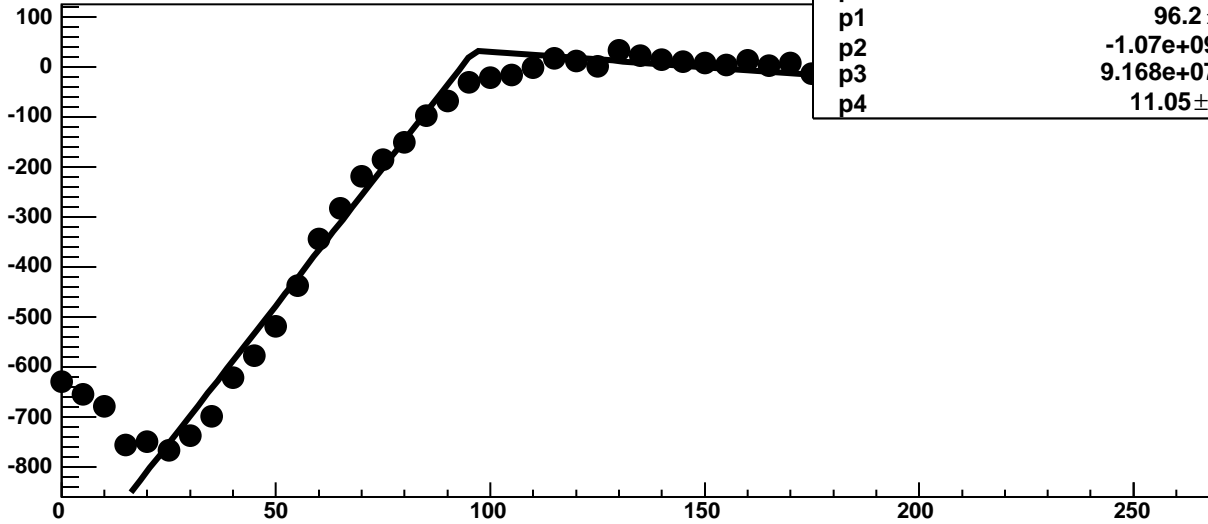


Chip 8, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold



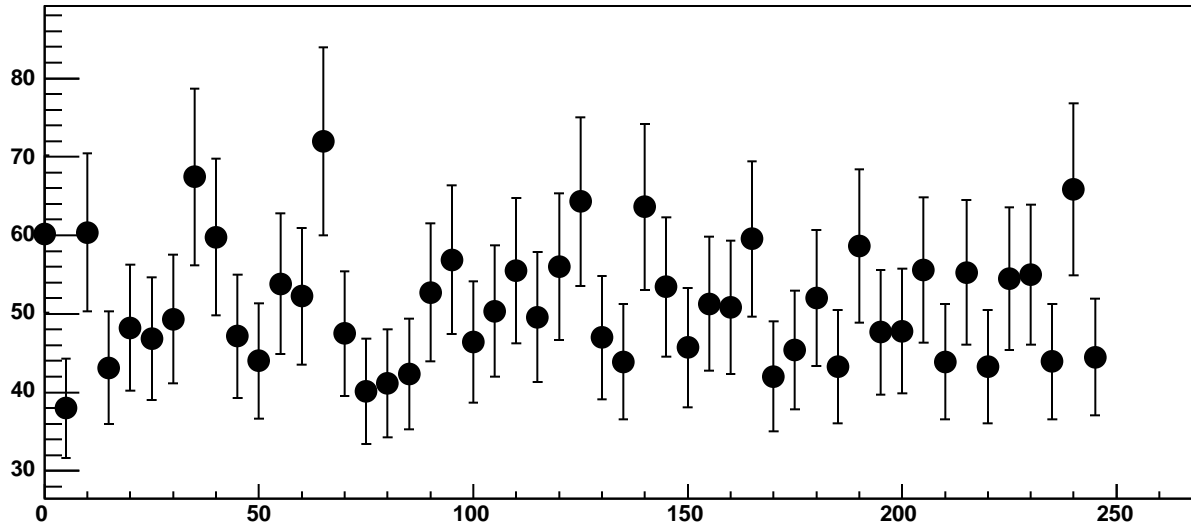


Chip 8, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

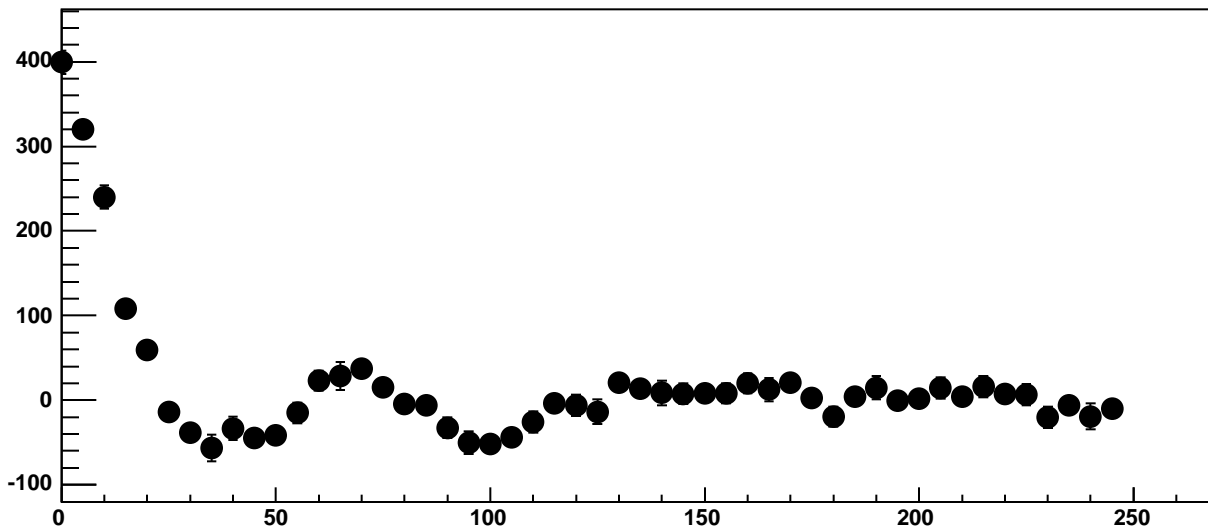


$\chi^2 / \text{ndf}$	331 / 41
p0	$32.77 \pm 3.785$
p1	$96.2 \pm 0.5466$
p2	$-1.07\text{e}+09 \pm 1.414$
p3	$9.168\text{e}+07 \pm 1.415$
p4	$11.05 \pm 0.04683$

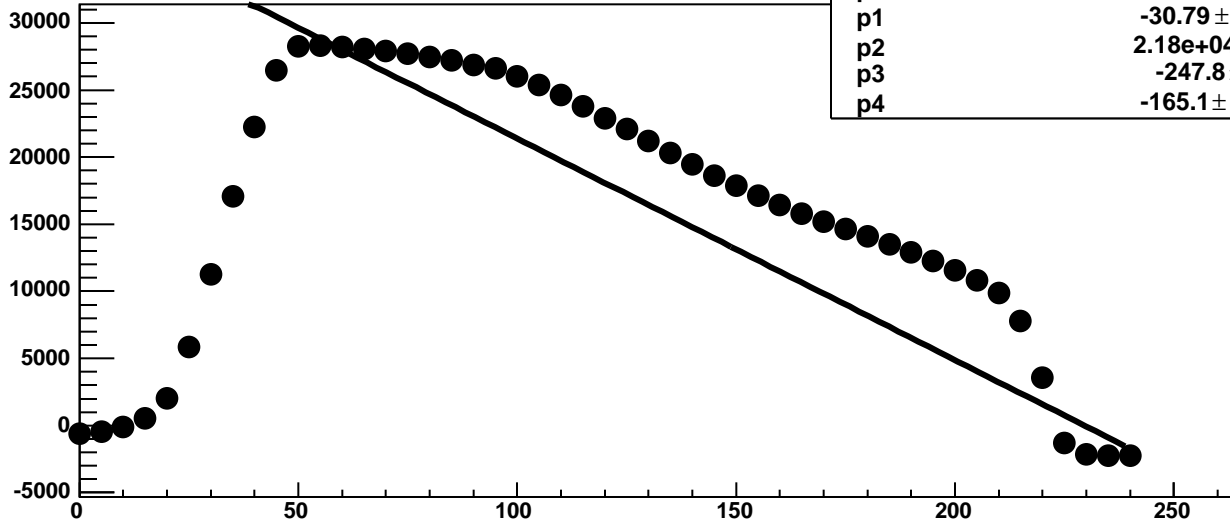
Chip 8, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

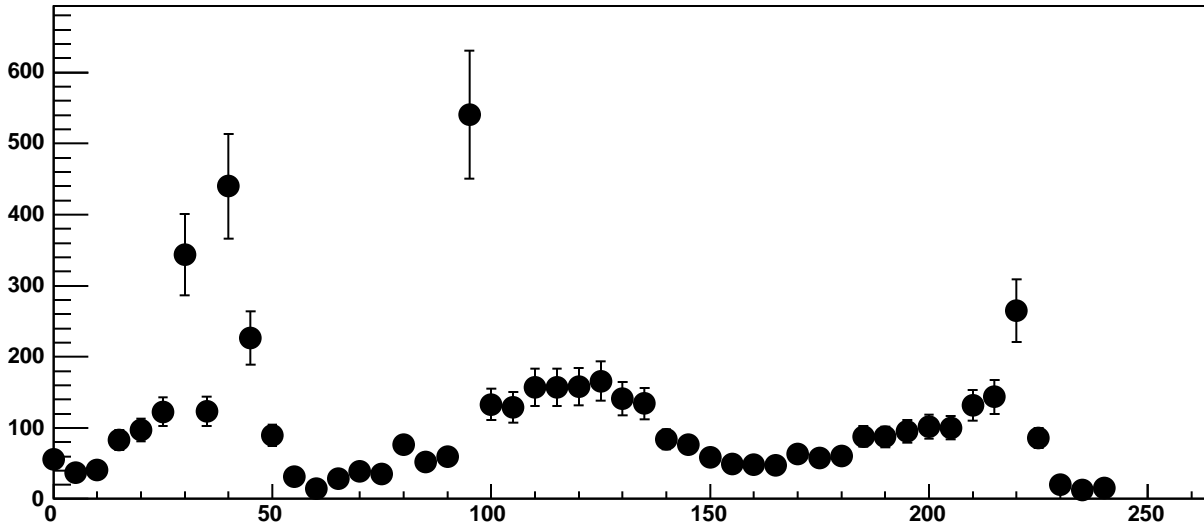


Chip 8, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold

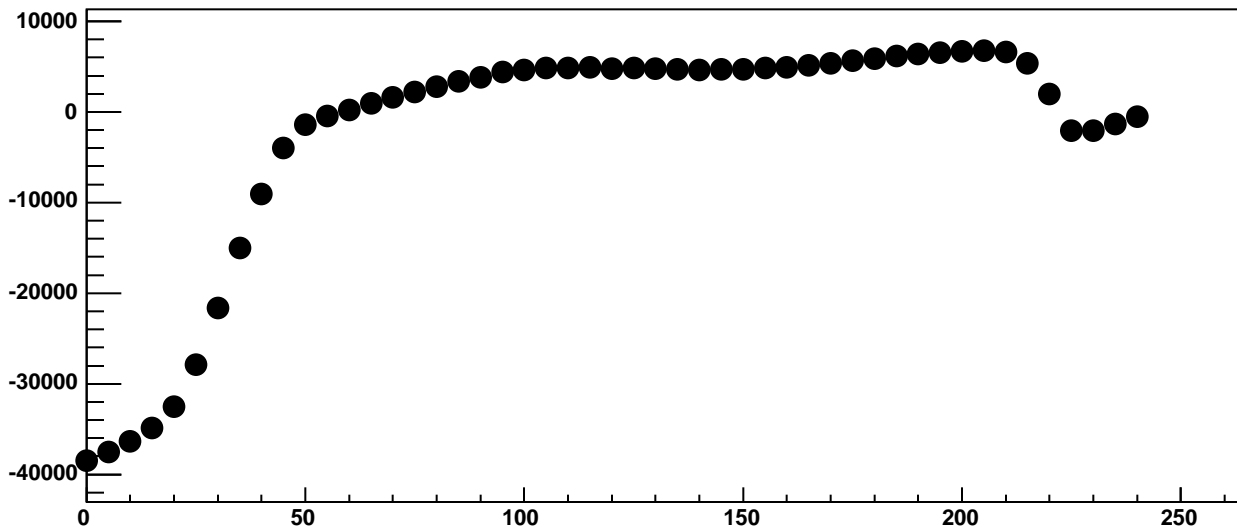


$\chi^2 / \text{ndf}$	9.65e+06 / 41
p0	2.118e+04 ± 13.67
p1	-30.79 ± 0.01167
p2	2.18e+04 ± 6.441
p3	-247.8 ± 0.8531
p4	-165.1 ± 0.02206

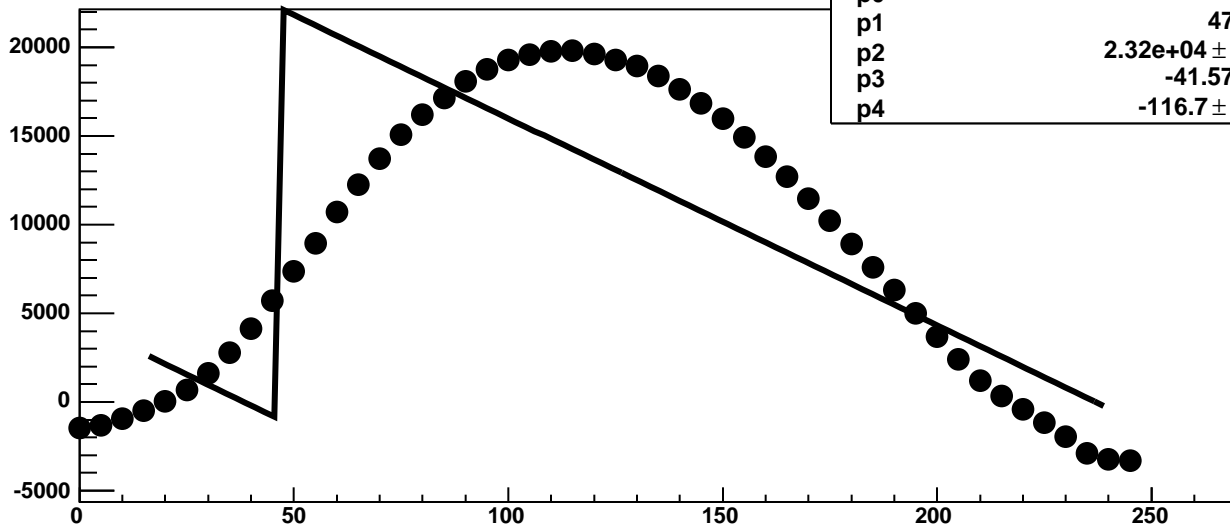
Chip 8, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 8, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold

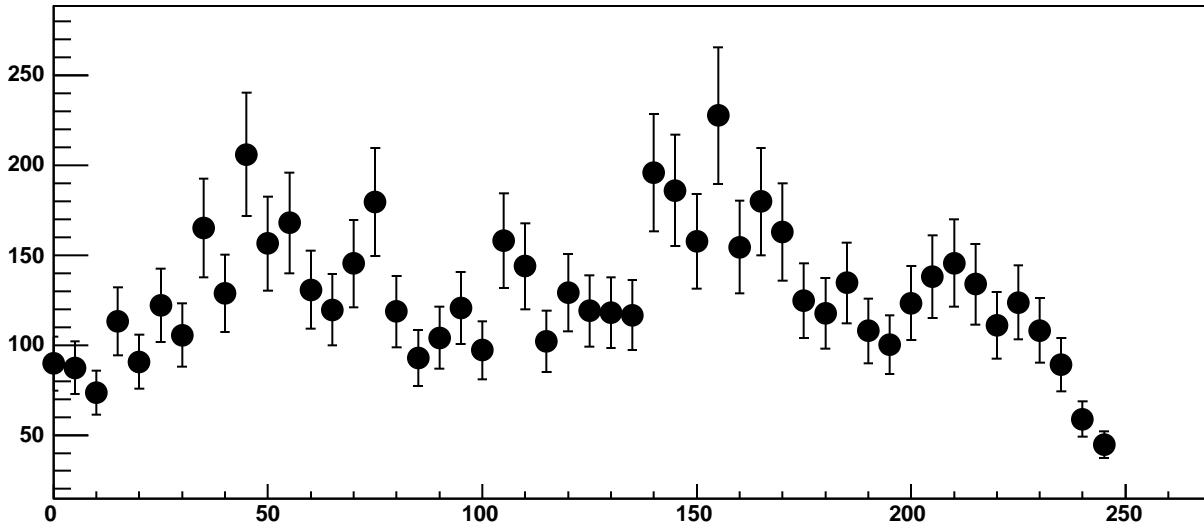


Chip 9, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold

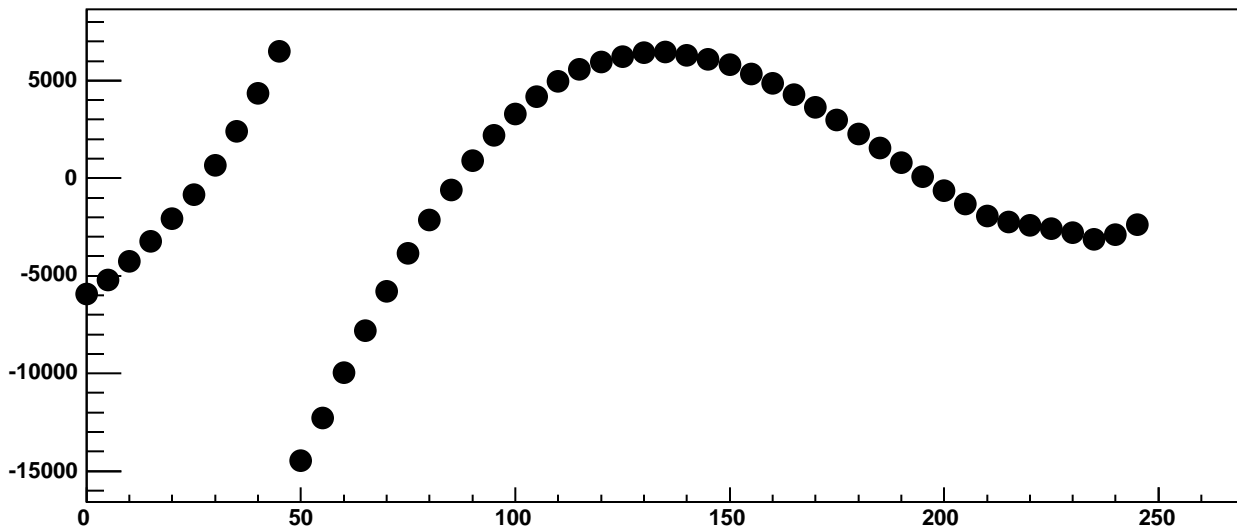


$\chi^2 / \text{ndf}$	1.148e+06 / 41
p0	-1021 ± 0.03418
p1	47 ± 0.213
p2	2.32e+04 ± 0.03428
p3	-41.57 ± 8.977
p4	-116.7 ± 0.01368

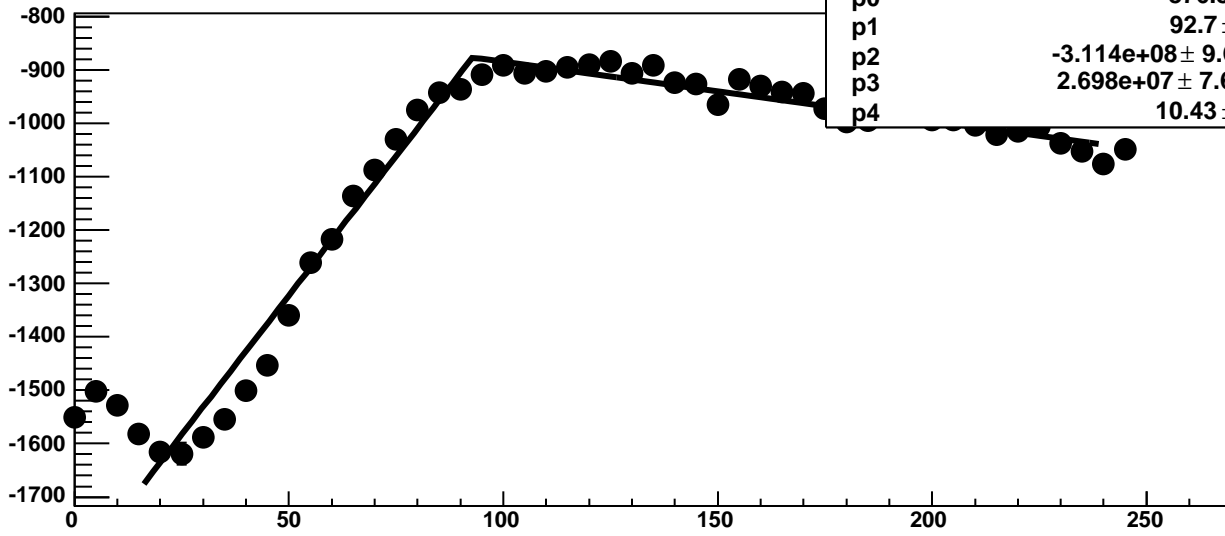
Chip 9, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold

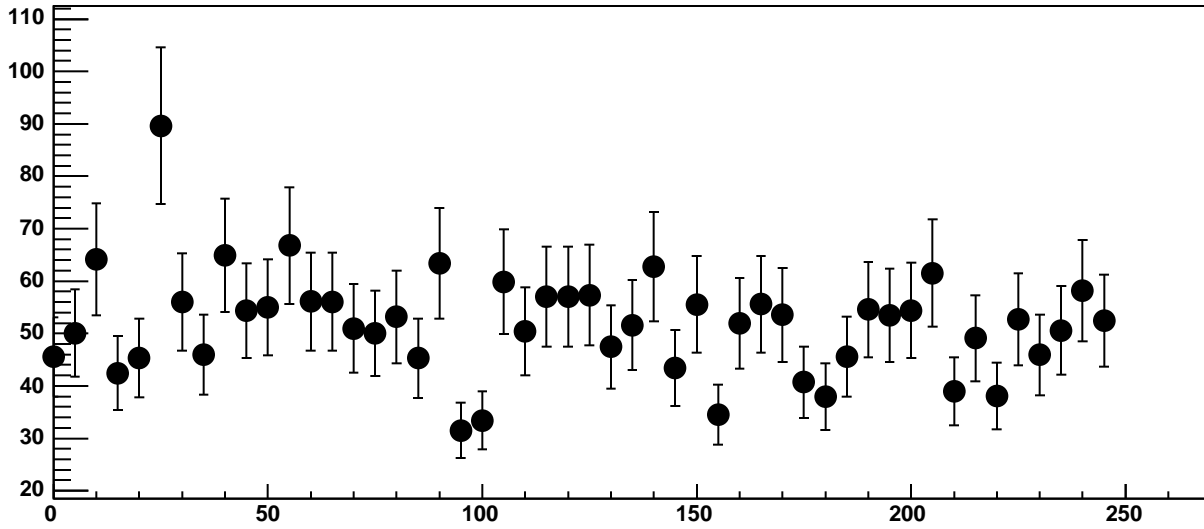


Chip 9, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

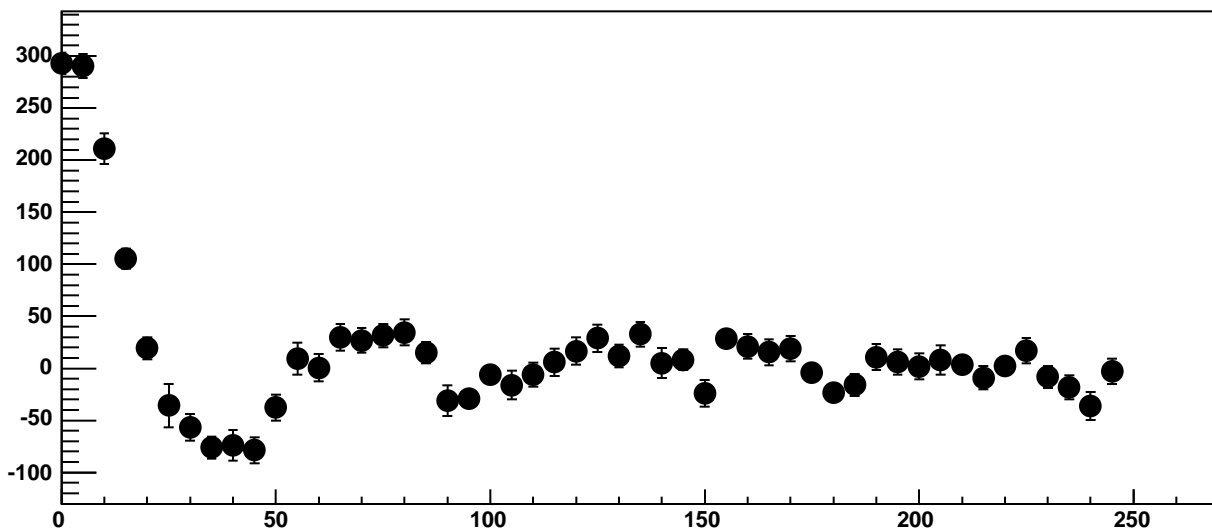


$\chi^2 / \text{ndf}$	384 / 41
p0	$-876.8 \pm 3.404$
p1	$92.7 \pm 0.6129$
p2	$-3.114\text{e}+08 \pm 9.664\text{e}+06$
p3	$2.698\text{e}+07 \pm 7.689\text{e}+05$
p4	$10.43 \pm 0.1267$

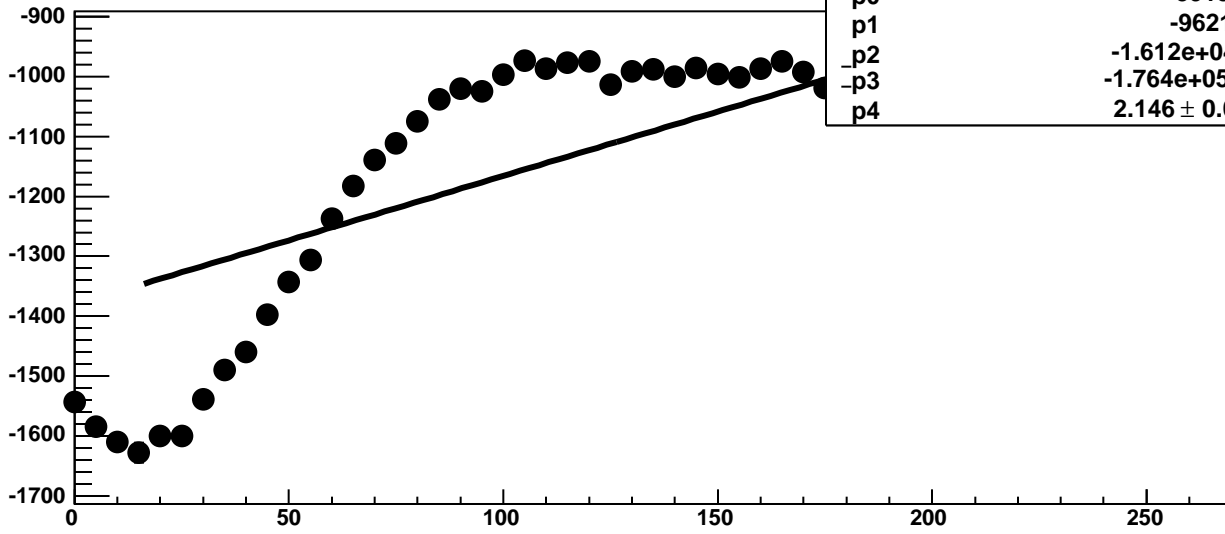
Chip 9, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



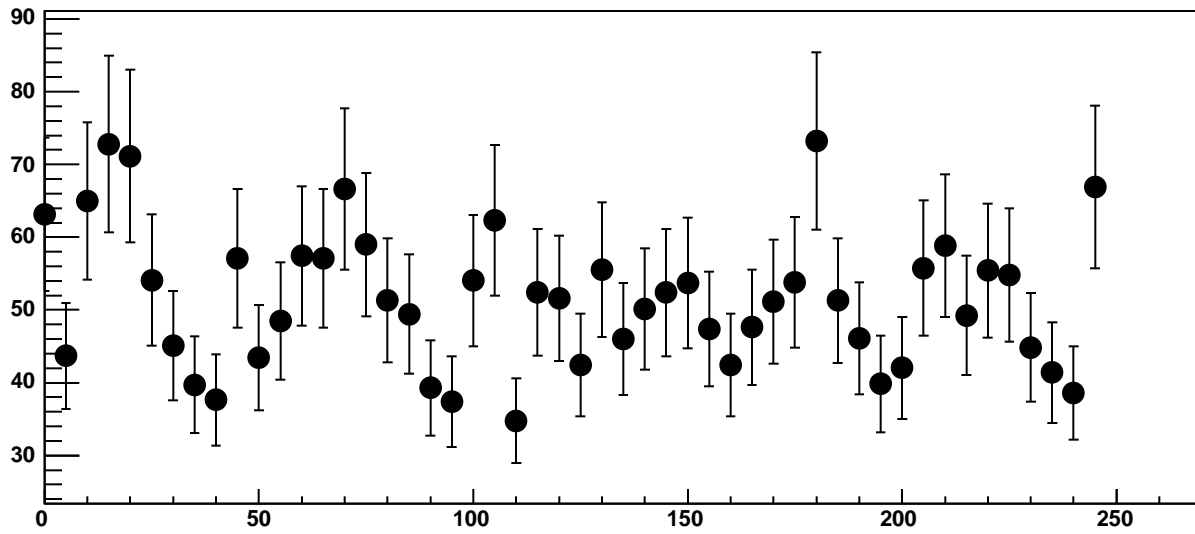
Chip 9, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



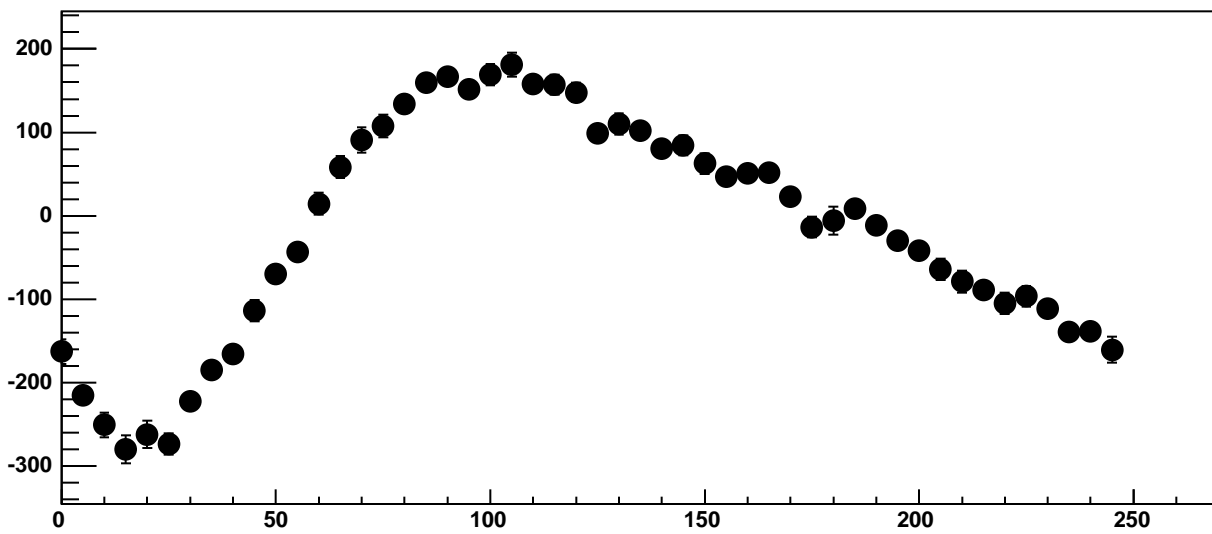
Chip 9, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold



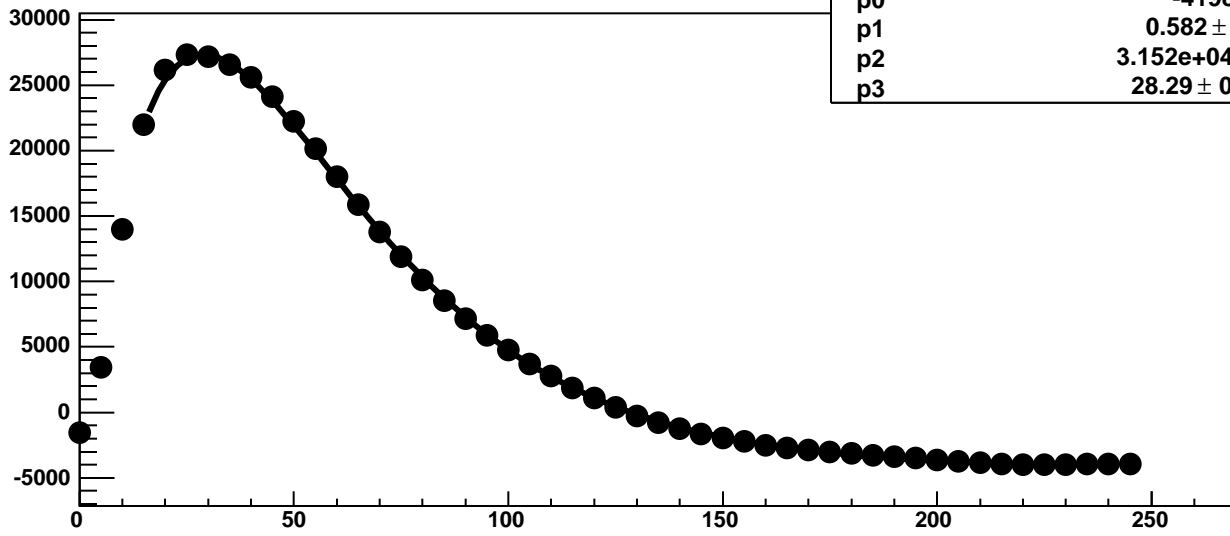
Chip 9, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold

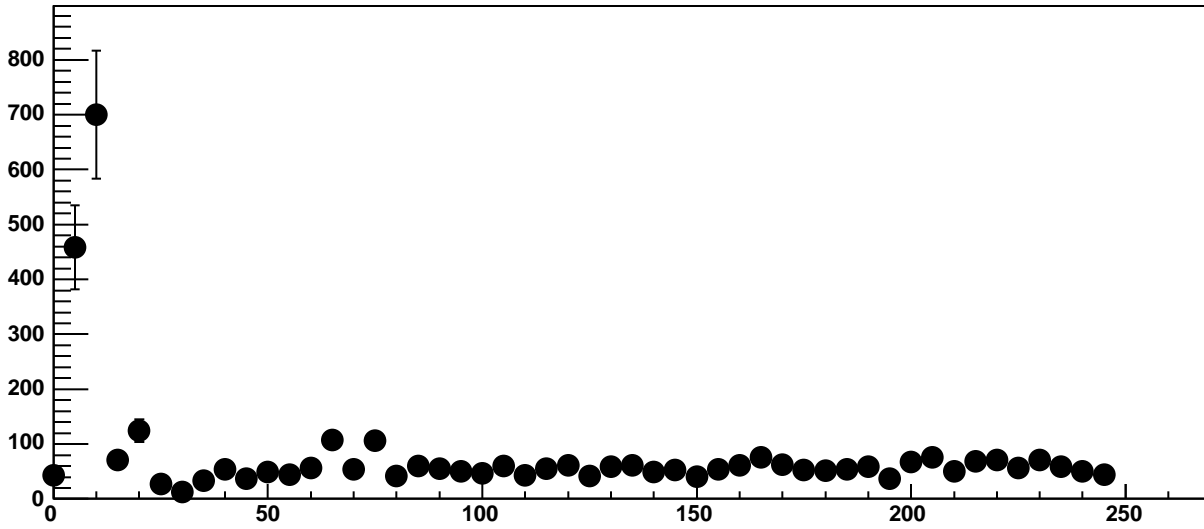


Chip 9, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold

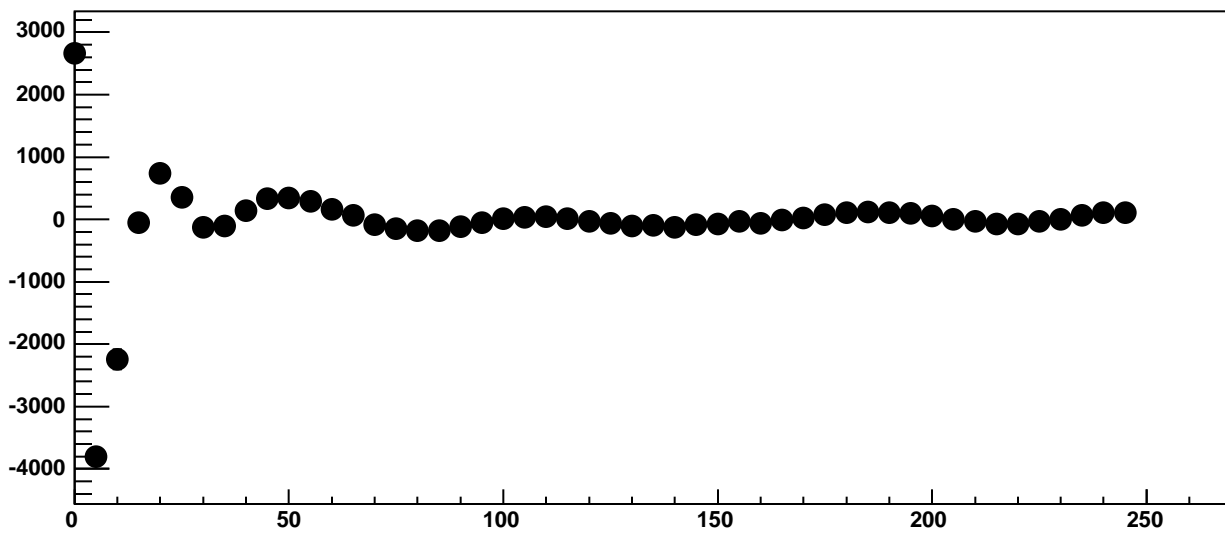


$\chi^2 / \text{ndf}$	1.128e+04 / 42
p0	-4198 ± 3.519
p1	0.582 ± 0.01738
p2	3.152e+04 ± 4.062
p3	28.29 ± 0.009448

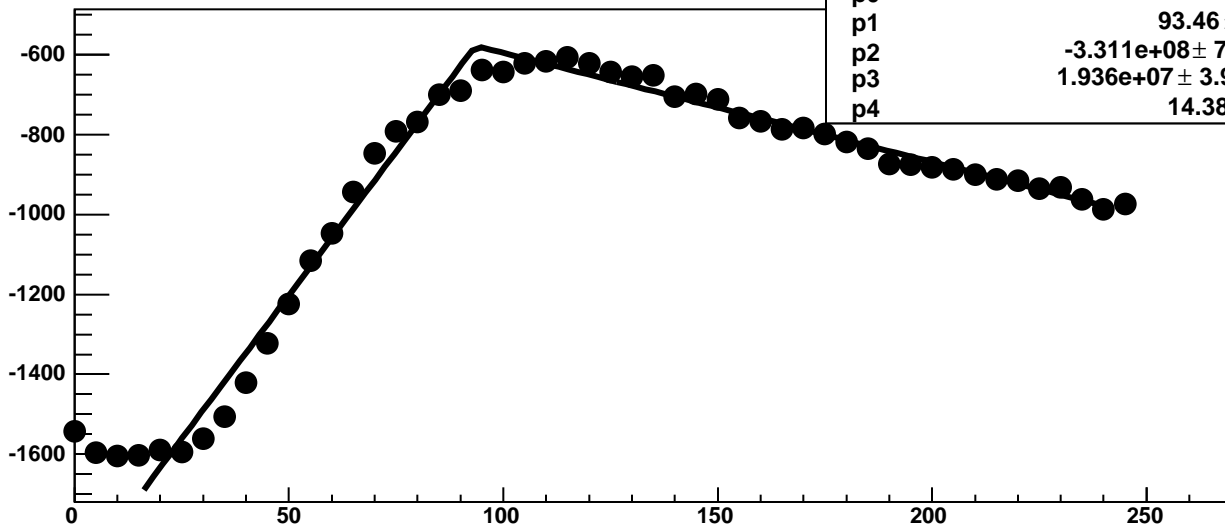
Chip 9, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold

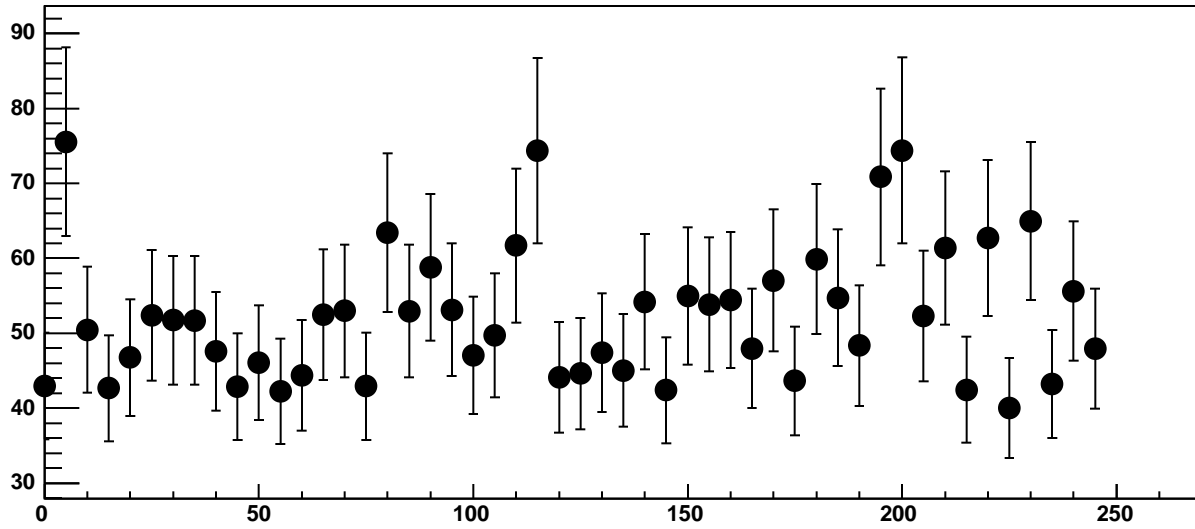


Chip 9, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold

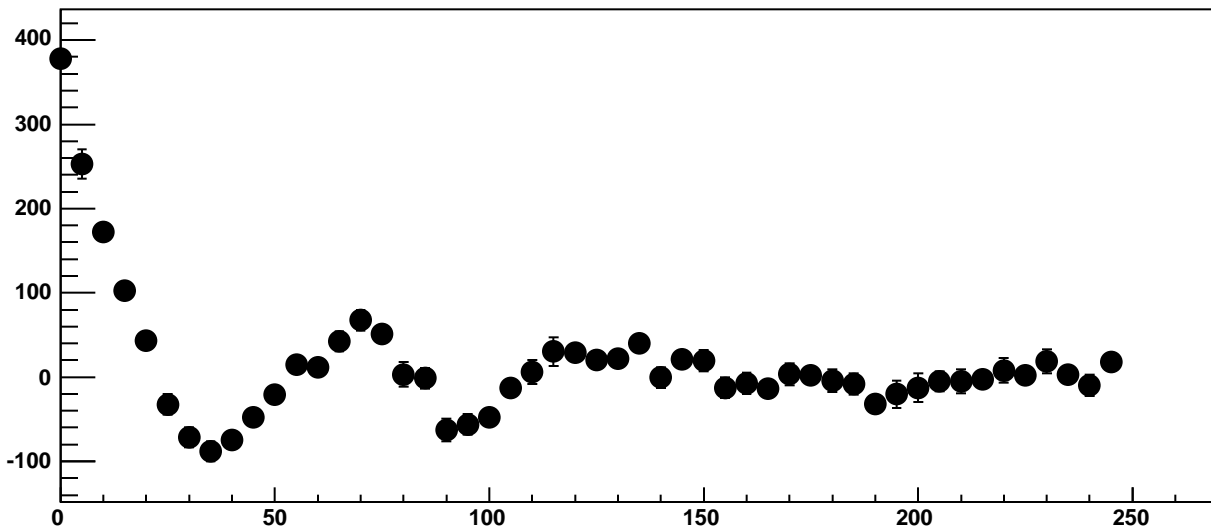


$\chi^2 / \text{ndf}$	497 / 41
p0	$-577.4 \pm 3.668$
p1	$93.46 \pm 0.4301$
p2	$-3.311\text{e}+08 \pm 7.31\text{e}+06$
p3	$1.936\text{e}+07 \pm 3.917\text{e}+05$
p4	$14.38 \pm 0.125$

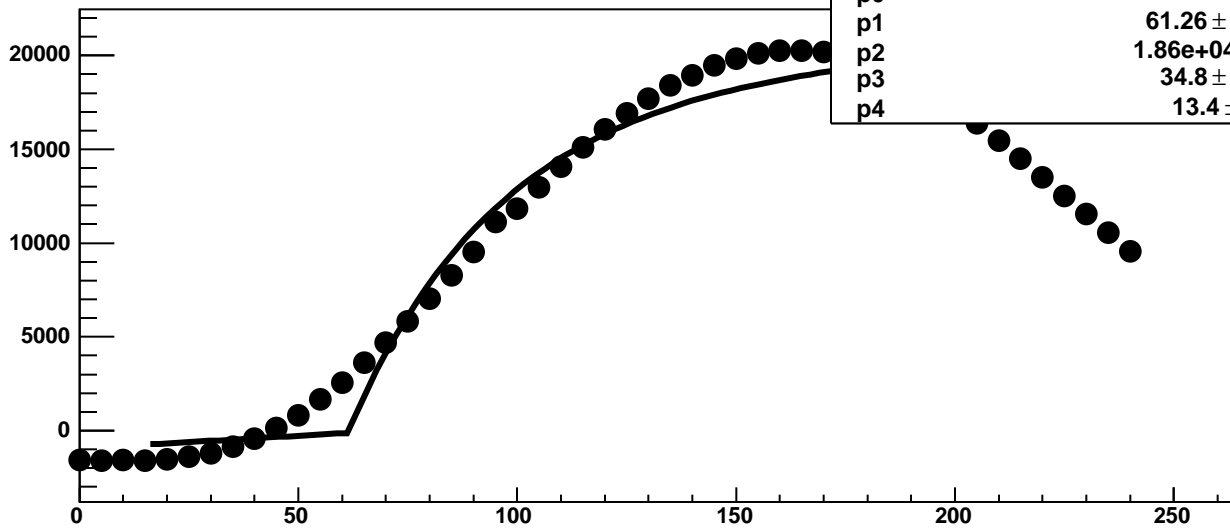
Chip 9, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



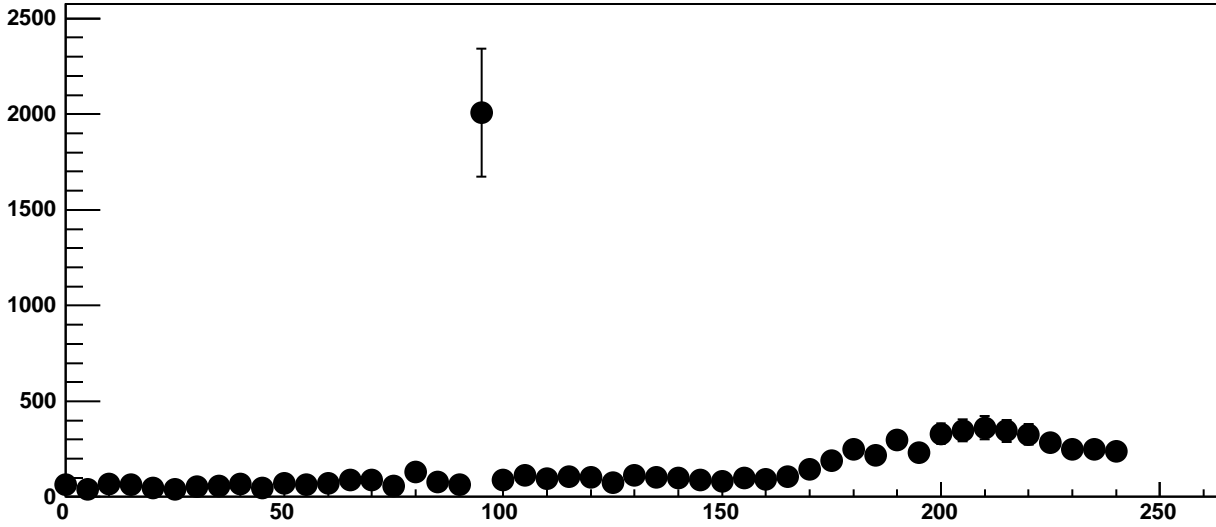
Chip 9, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold



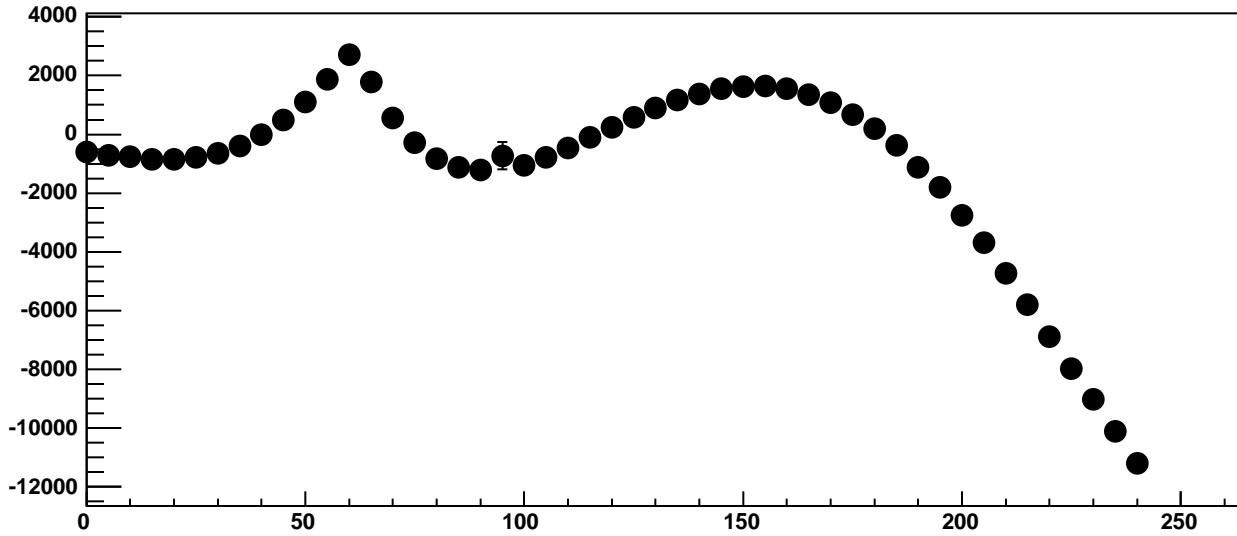
Chip 9, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 9, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

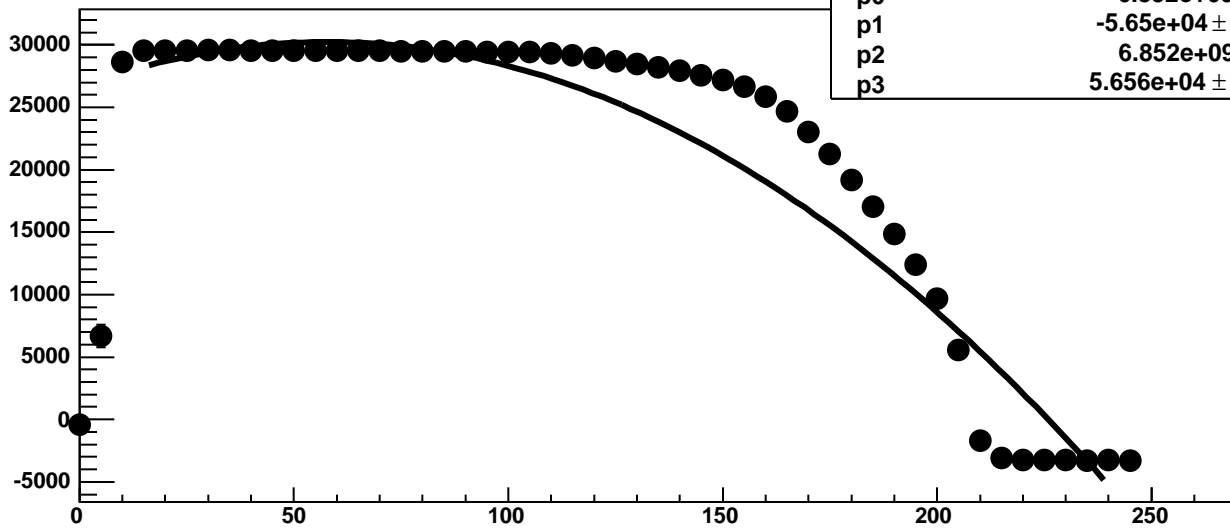


Chip 9, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

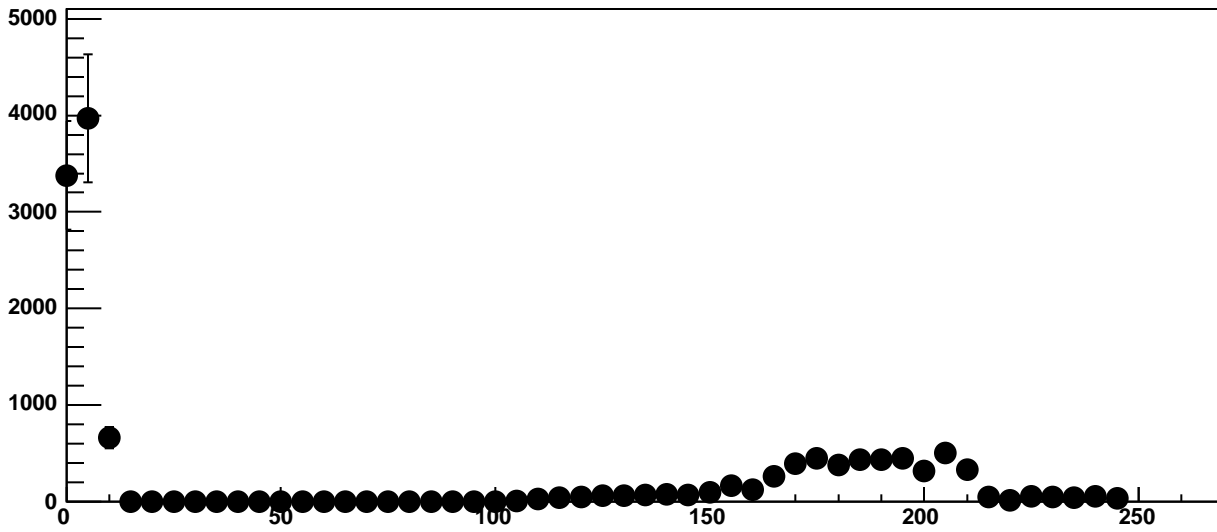




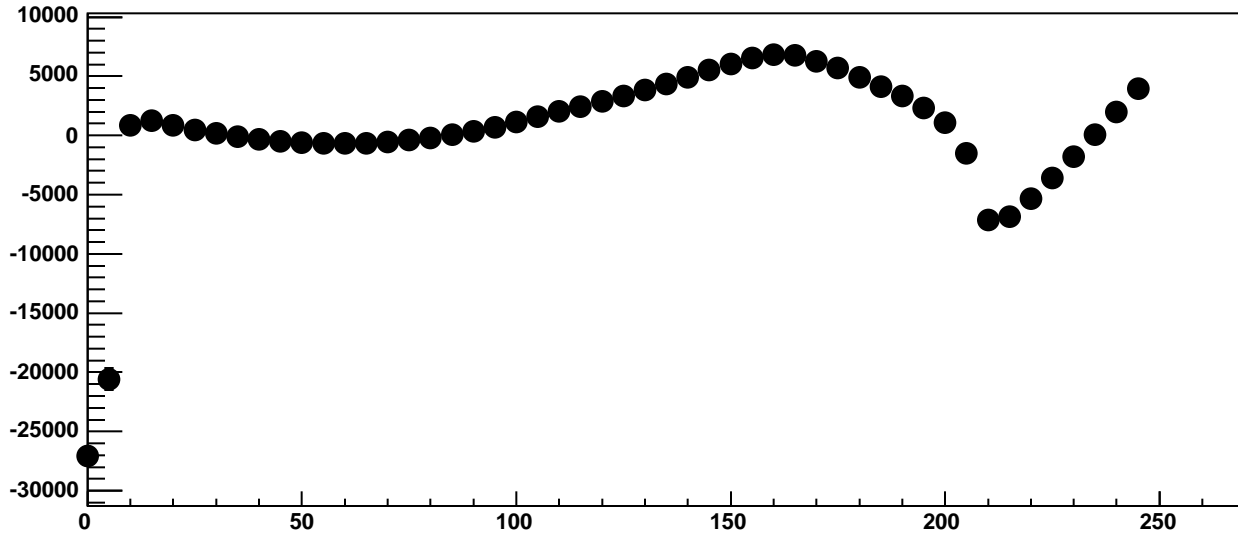
Chip 9, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold



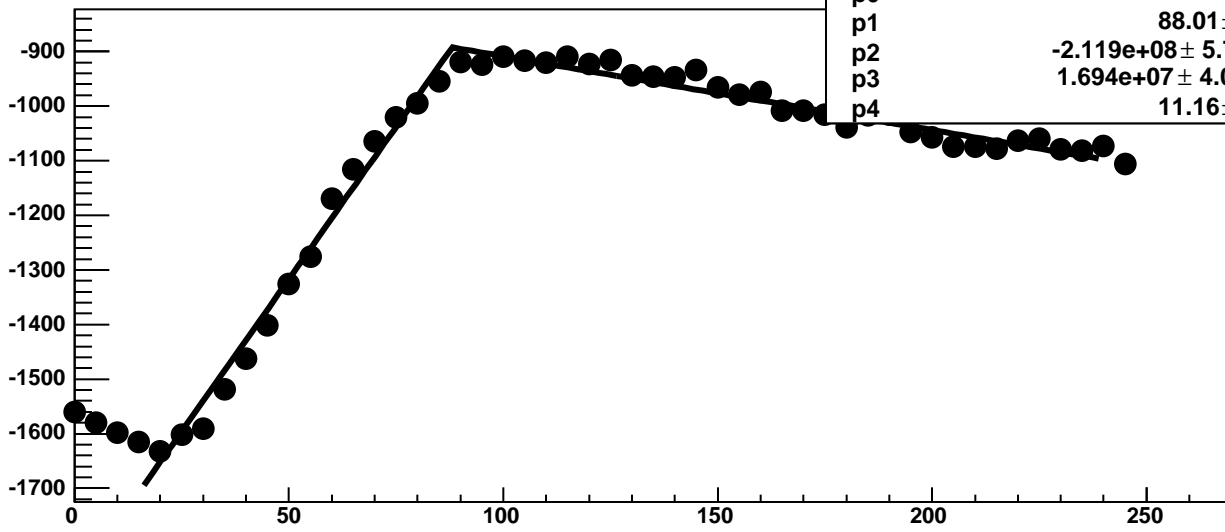
Chip 9, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold

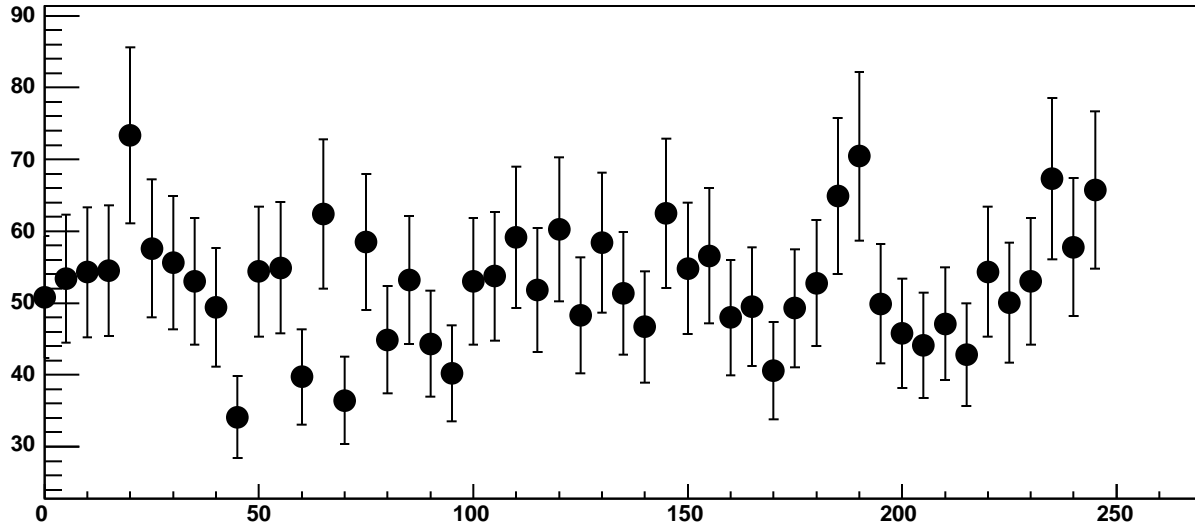


Chip 9, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

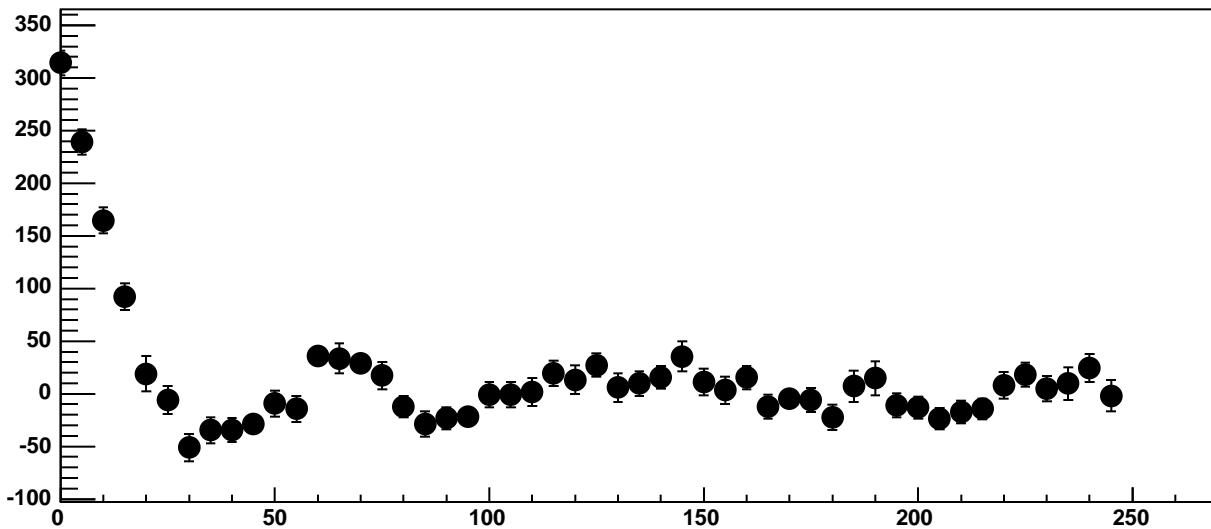


$\chi^2 / \text{ndf}$	204.4 / 41
p0	$-892.7 \pm 3.736$
p1	$88.01 \pm 0.5748$
p2	$-2.119\text{e}+08 \pm 5.709\text{e}+06$
p3	$1.694\text{e}+07 \pm 4.093\text{e}+05$
p4	$11.16 \pm 0.1452$

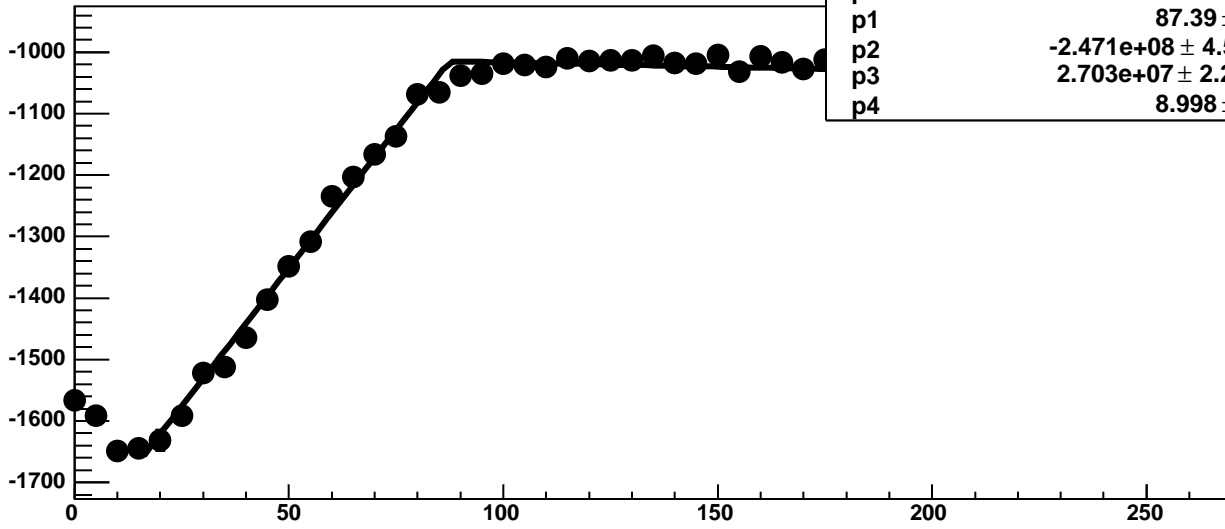
Chip 9, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

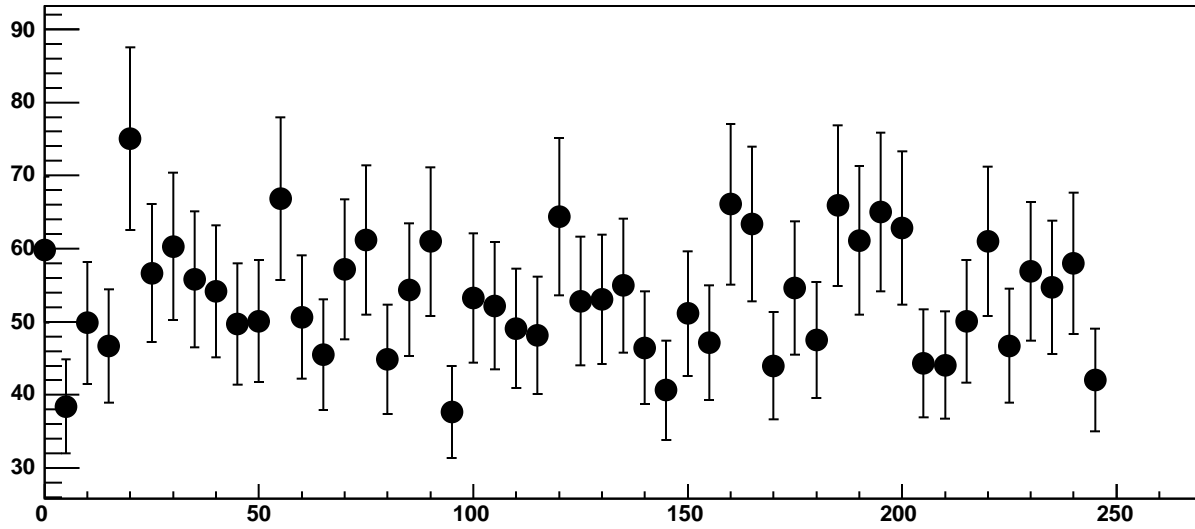


Chip 9, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

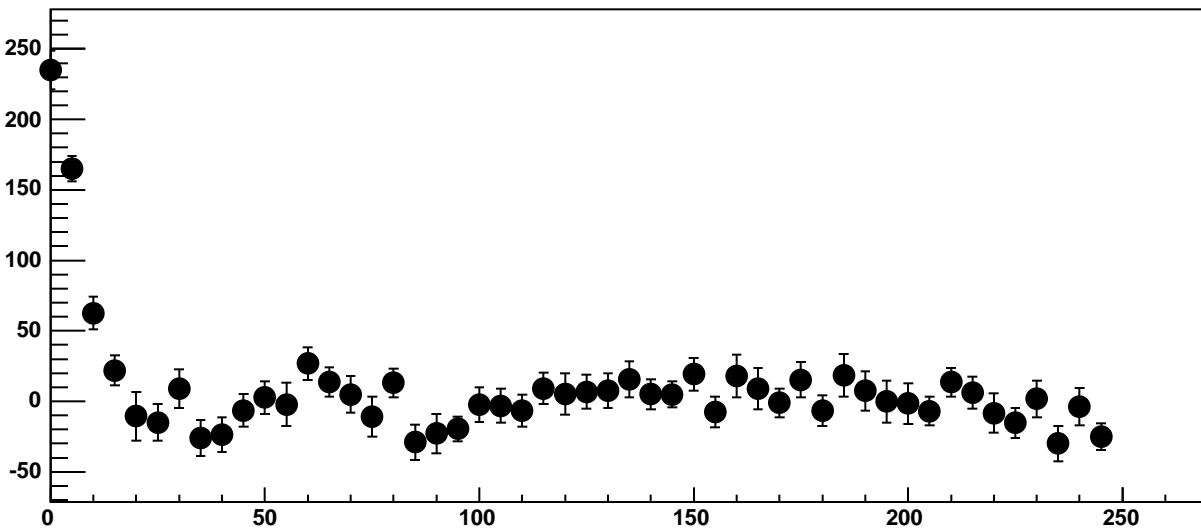


$\chi^2 / \text{ndf}$	60.25 / 41
p0	-1015 ± 4.083
p1	87.39 ± 0.8123
p2	-2.471e+08 ± 4.582e+06
p3	2.703e+07 ± 2.209e+05
p4	8.998 ± 0.1467

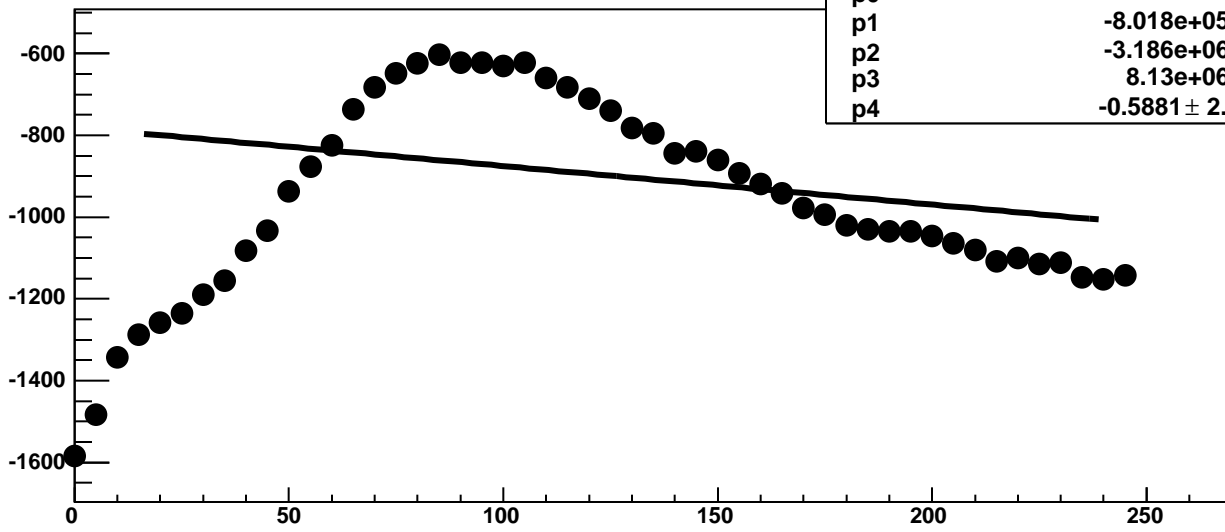
Chip 9, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

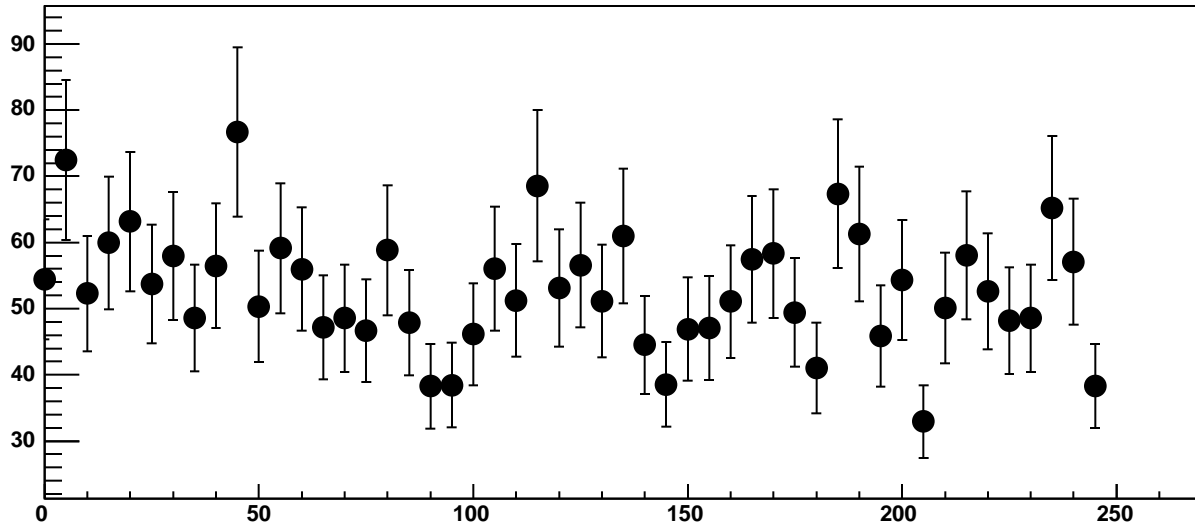


Chip 9, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold

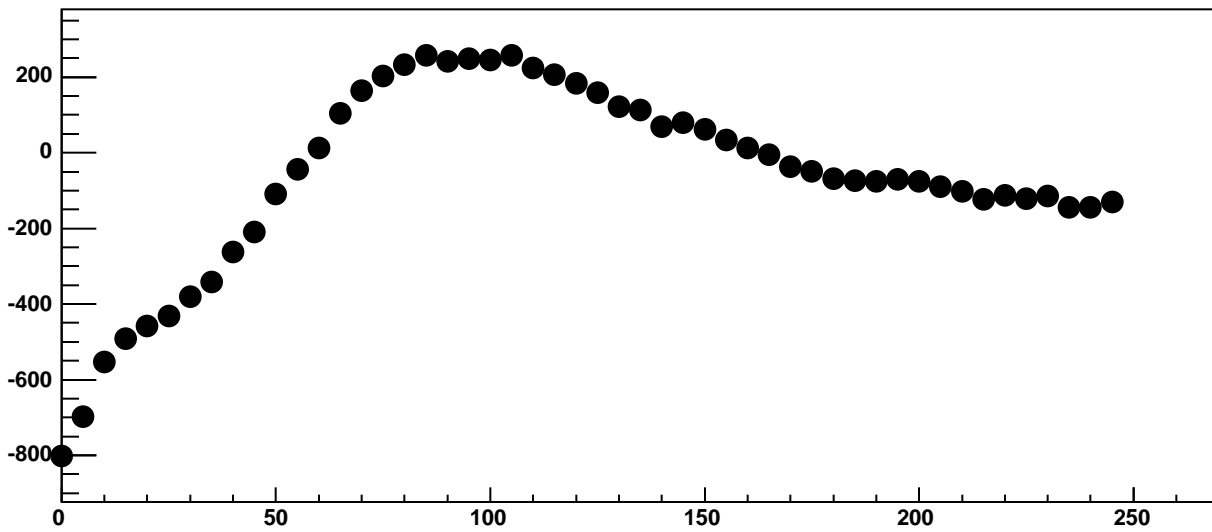


$\chi^2 / \text{ndf}$	1.223e+04 / 41
p0	7.699e+05 $\pm$ 21.67
p1	-8.018e+05 $\pm$ 22.97
p2	-3.186e+06 $\pm$ 230.7
p3	8.13e+06 $\pm$ 618.6
p4	-0.5881 $\pm$ 2.702e-05

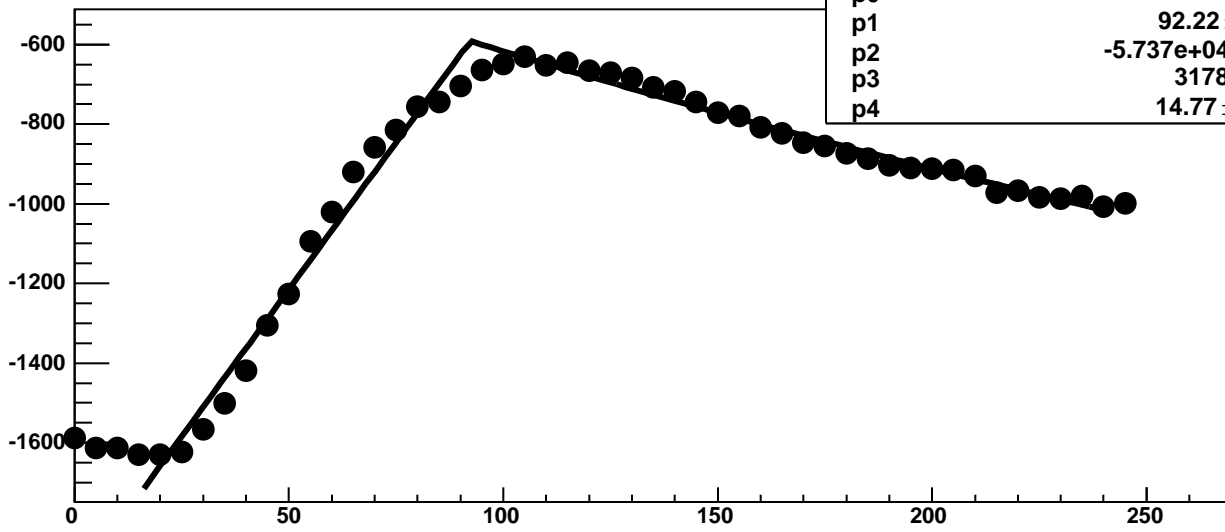
Chip 9, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



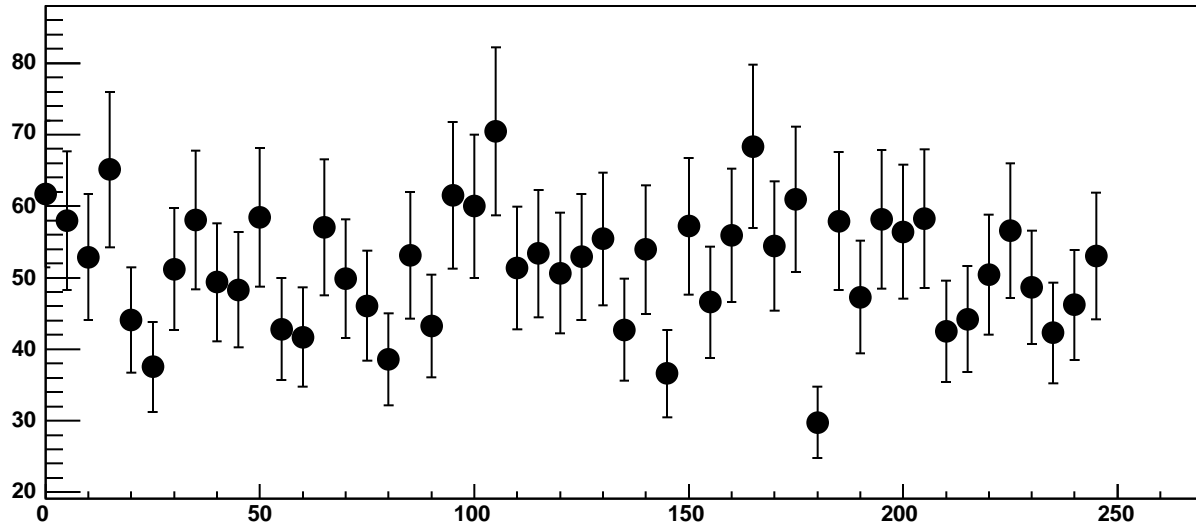
Chip 9, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold



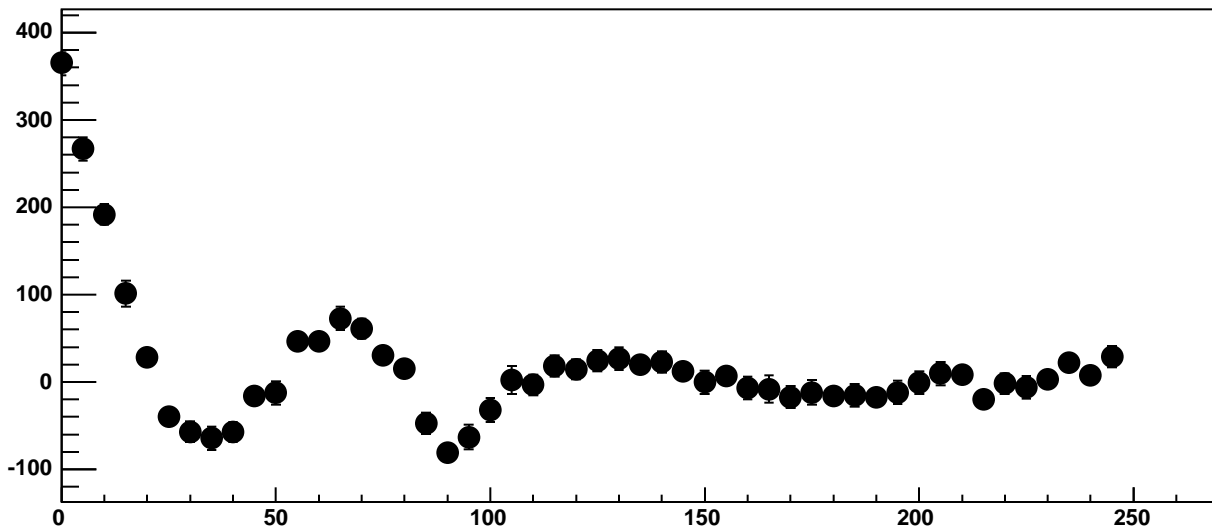
Chip 9, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold



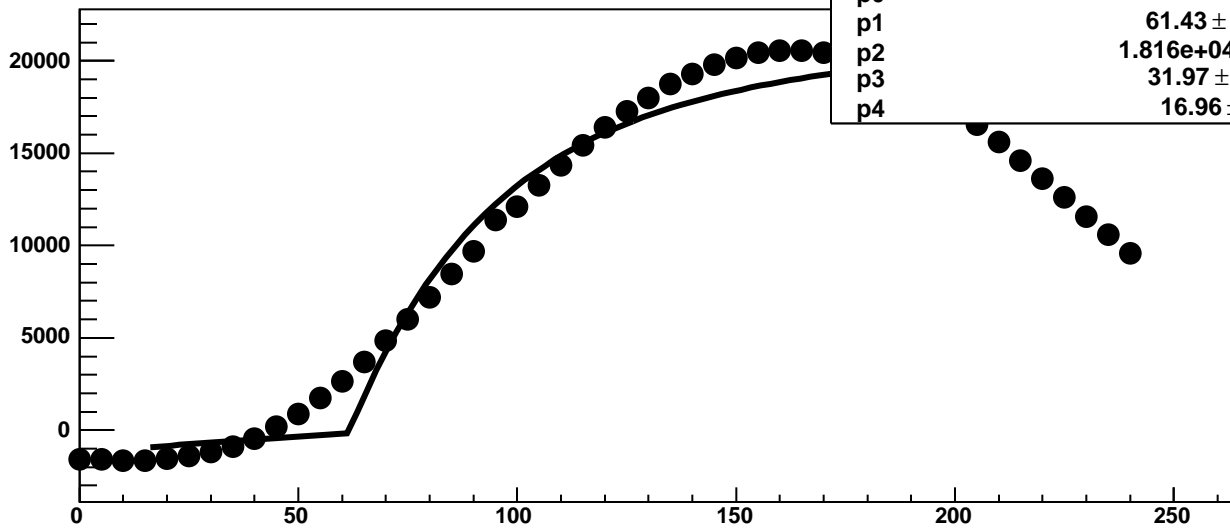
Chip 9, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

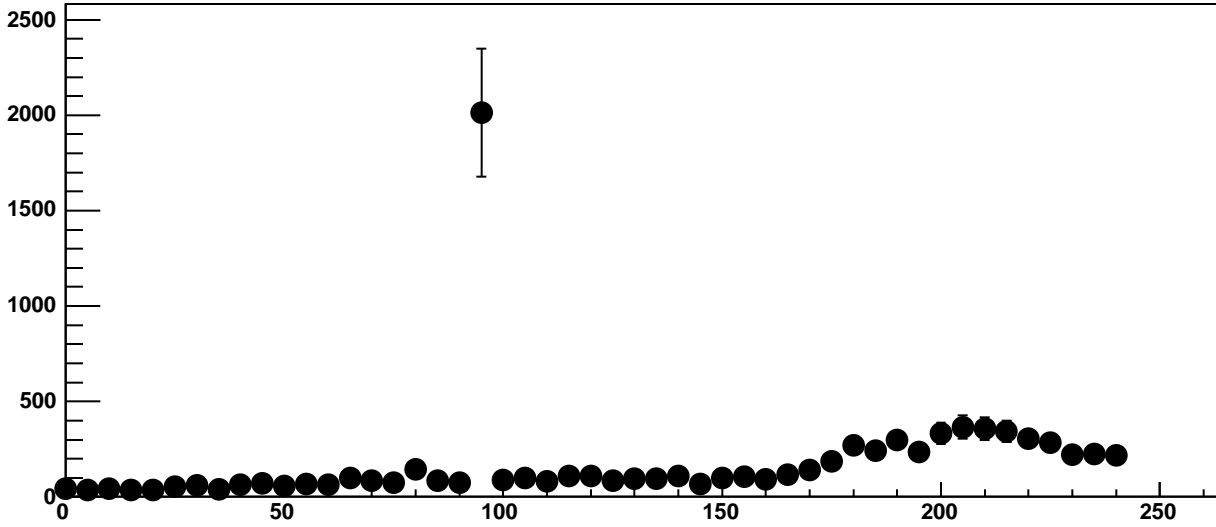


Chip 9, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

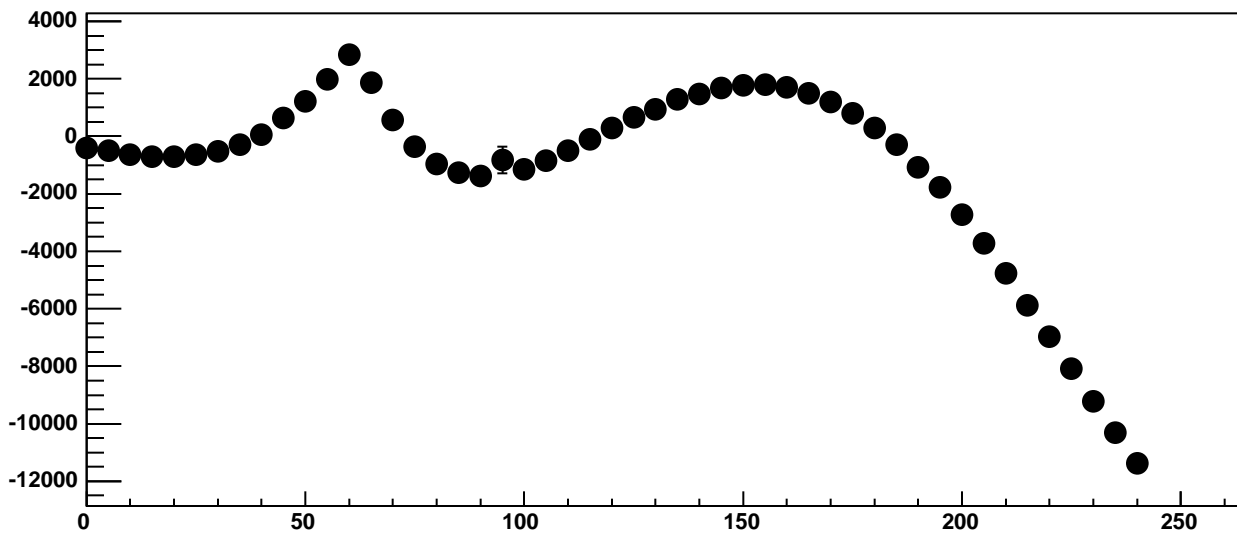


$\chi^2 / \text{ndf}$	3.142e+05 / 41
p0	-145.9 ± 7.011
p1	61.43 ± 0.03328
p2	1.816e+04 ± 30.51
p3	31.97 ± 0.07281
p4	16.96 ± 0.1932

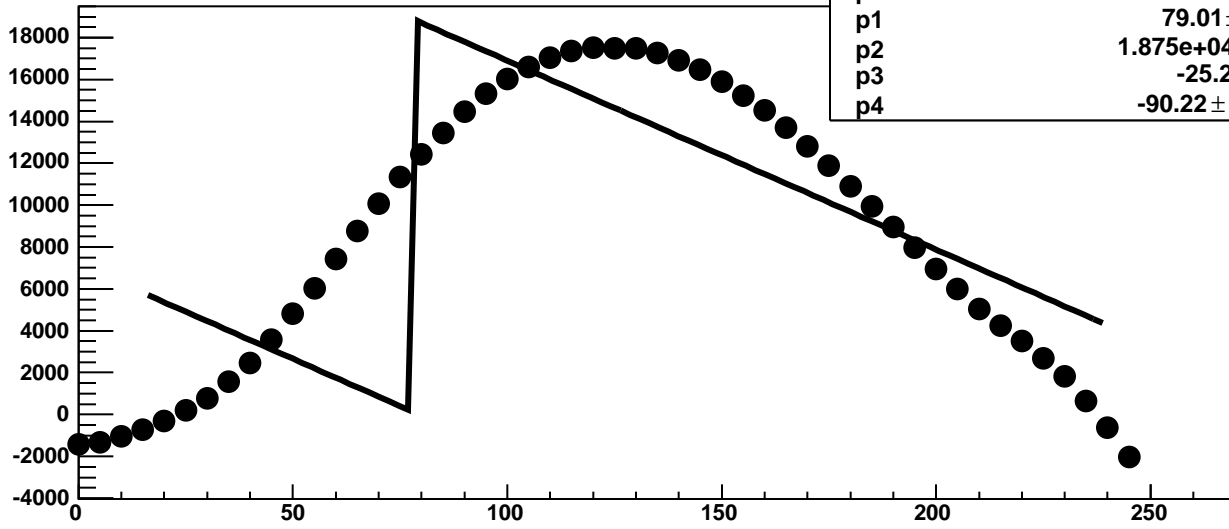
Chip 9, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

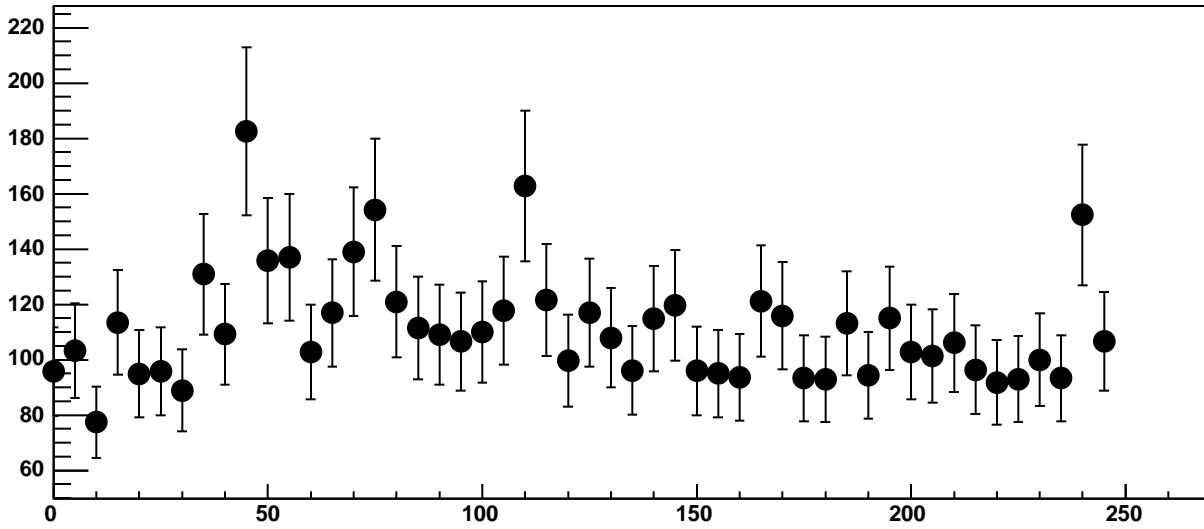


Chip 9, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold

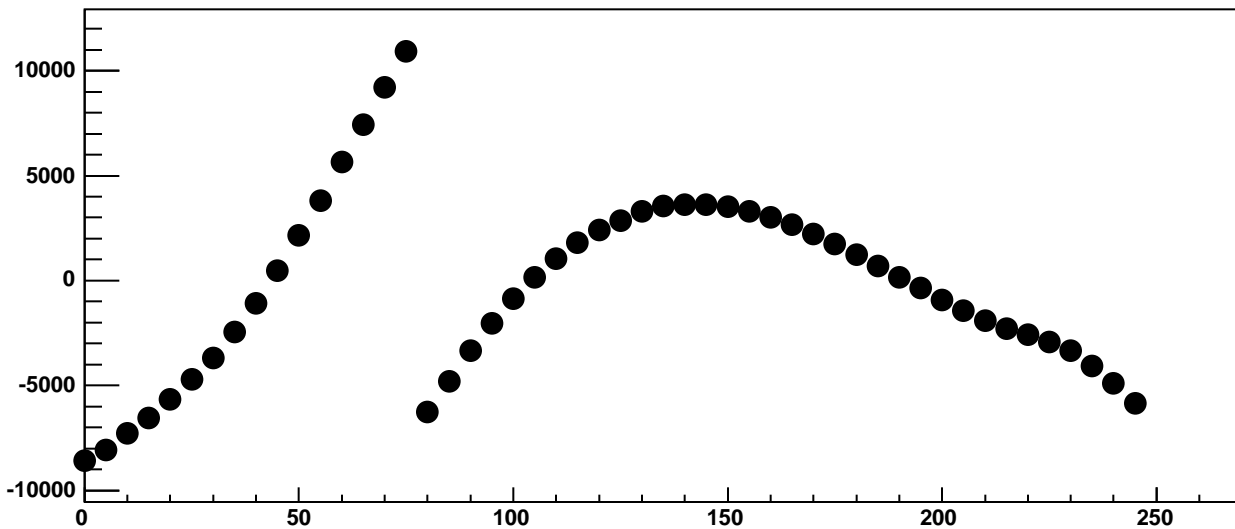


$\chi^2 / \text{ndf}$	1e+06 / 41
p0	43.13 ± 6.074
p1	79.01 ± 0.2928
p2	1.875e+04 ± 5.601
p3	-25.2 ± 1.487
p4	-90.22 ± 0.02083

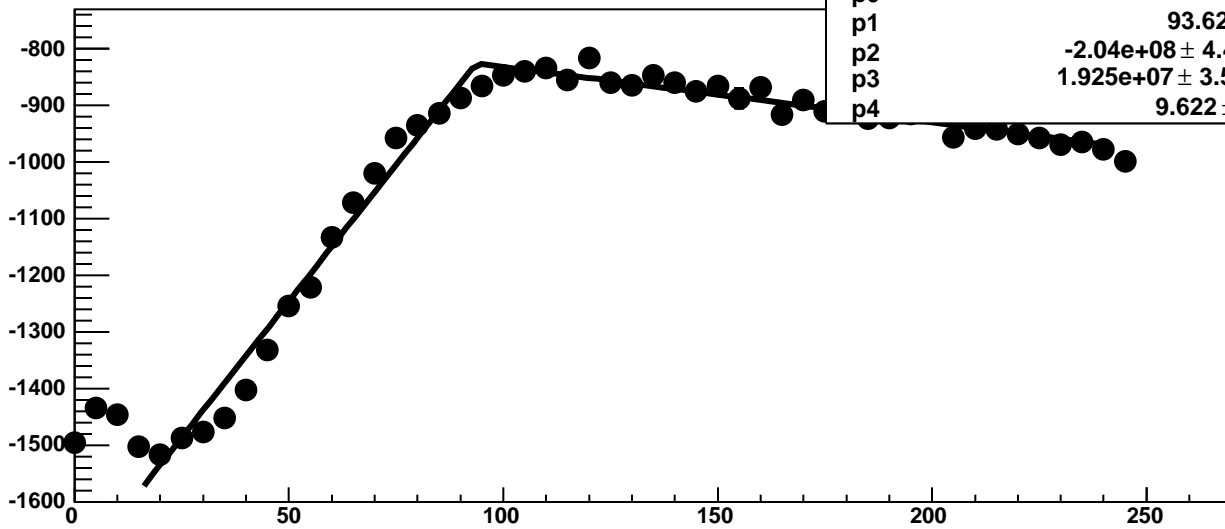
Chip 9, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

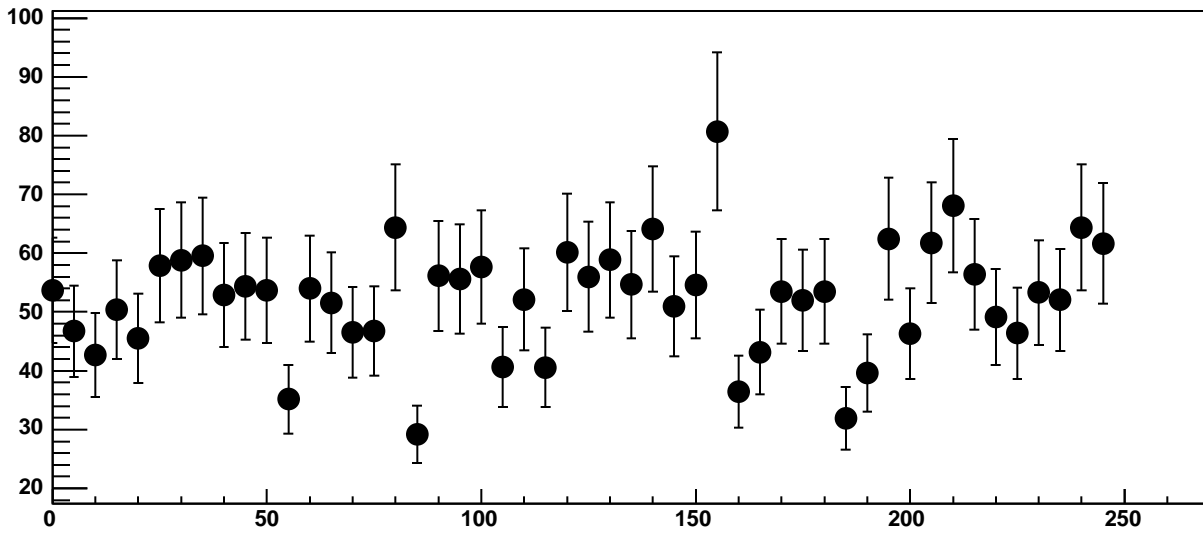


Chip 9, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

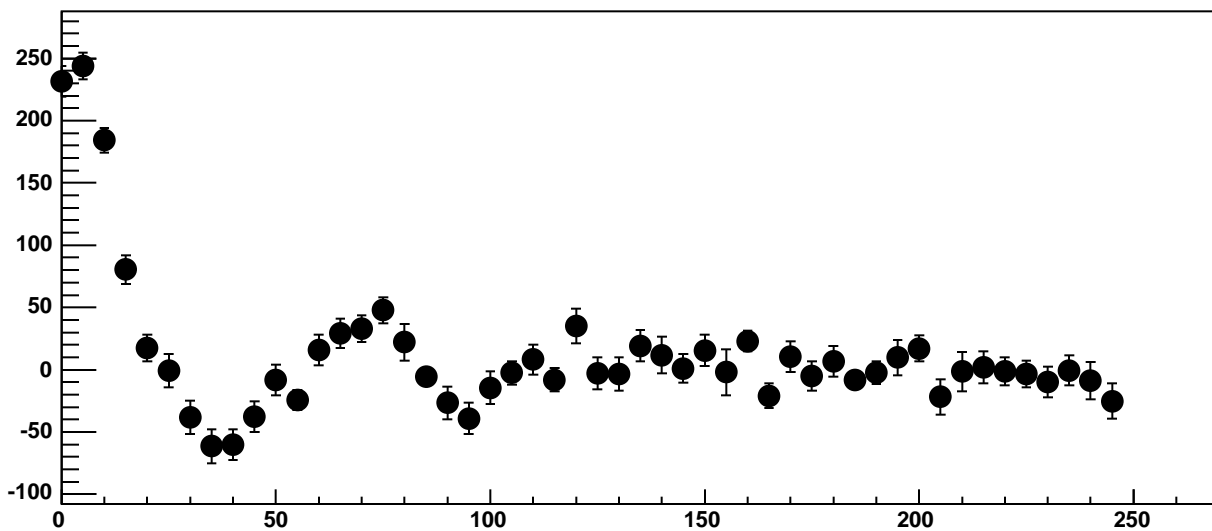


$\chi^2 / \text{ndf}$	212.2 / 41
p0	$-826.4 \pm 3.896$
p1	$93.62 \pm 0.633$
p2	$-2.04\text{e}+08 \pm 4.469\text{e}+06$
p3	$1.925\text{e}+07 \pm 3.549\text{e}+05$
p4	$9.622 \pm 0.1172$

Chip 9, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

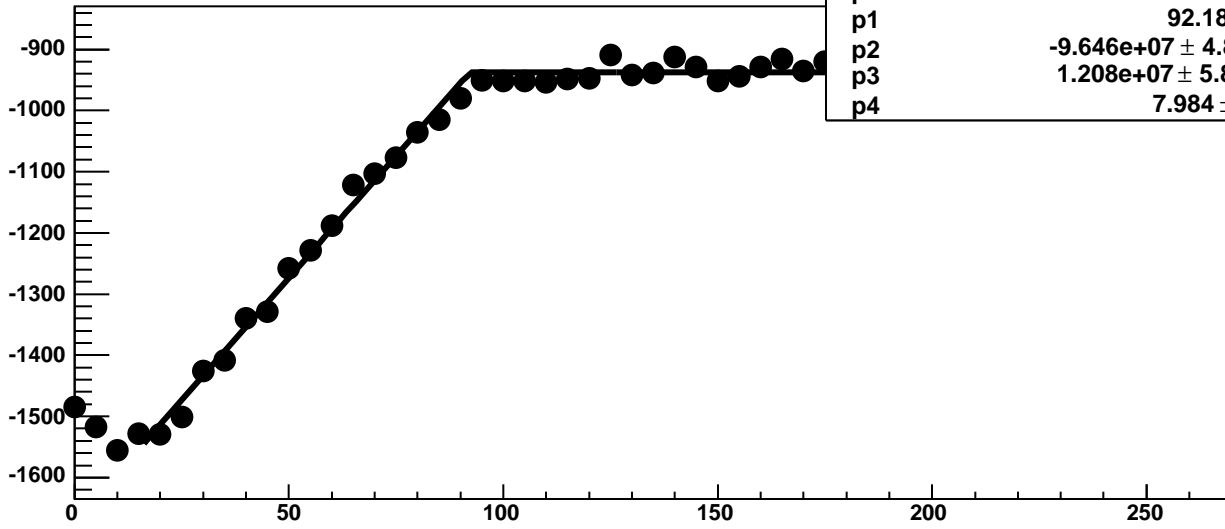


Chip 9, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



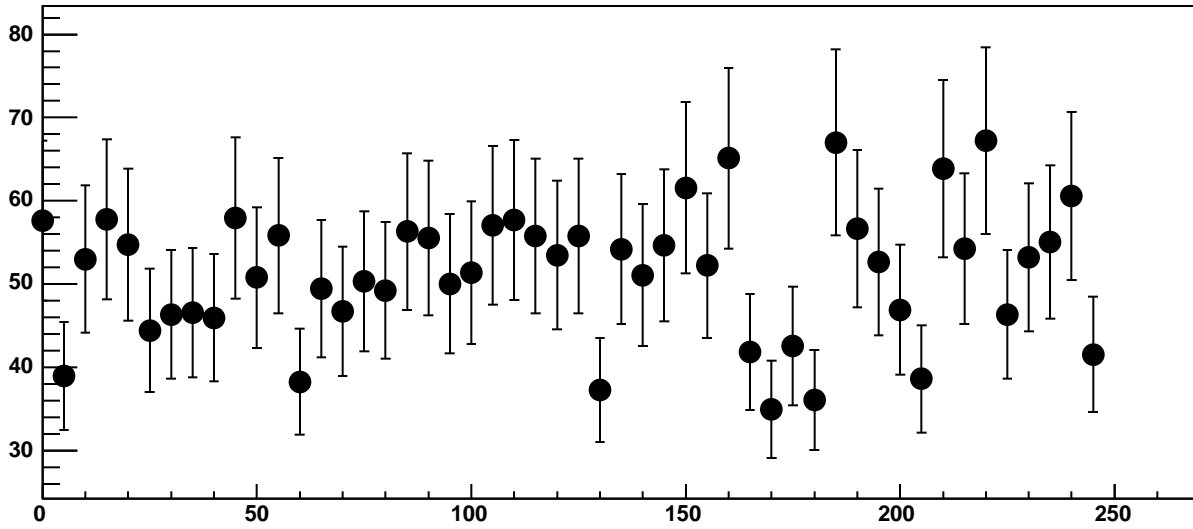


Chip 9, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

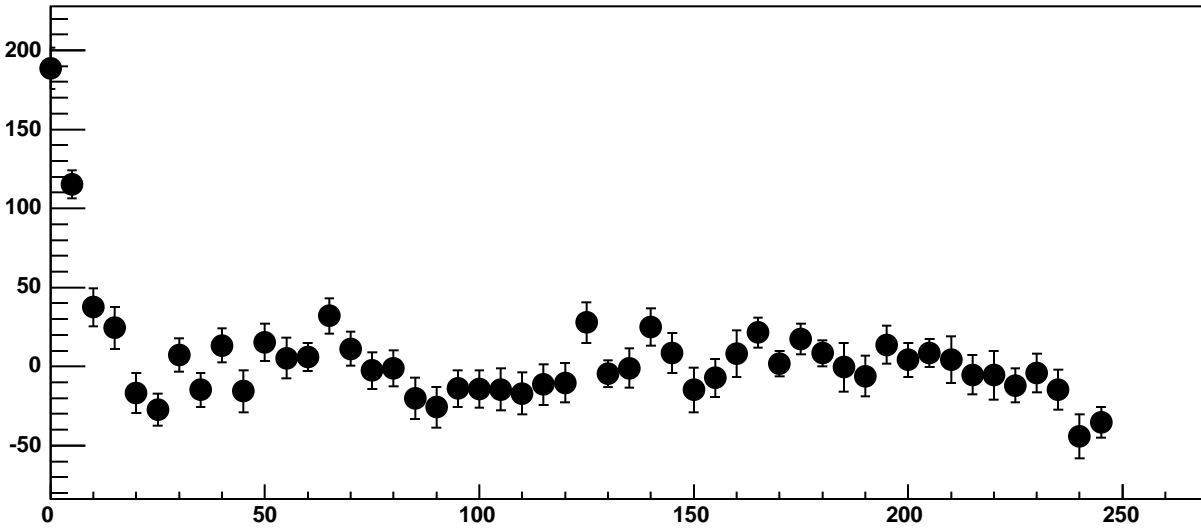


$\chi^2 / \text{ndf}$	79.57 / 41
p0	$-936.9 \pm 4.409$
p1	$92.18 \pm 0.937$
p2	$-9.646\text{e}+07 \pm 4.801\text{e}+06$
p3	$1.208\text{e}+07 \pm 5.825\text{e}+05$
p4	$7.984 \pm 0.1306$

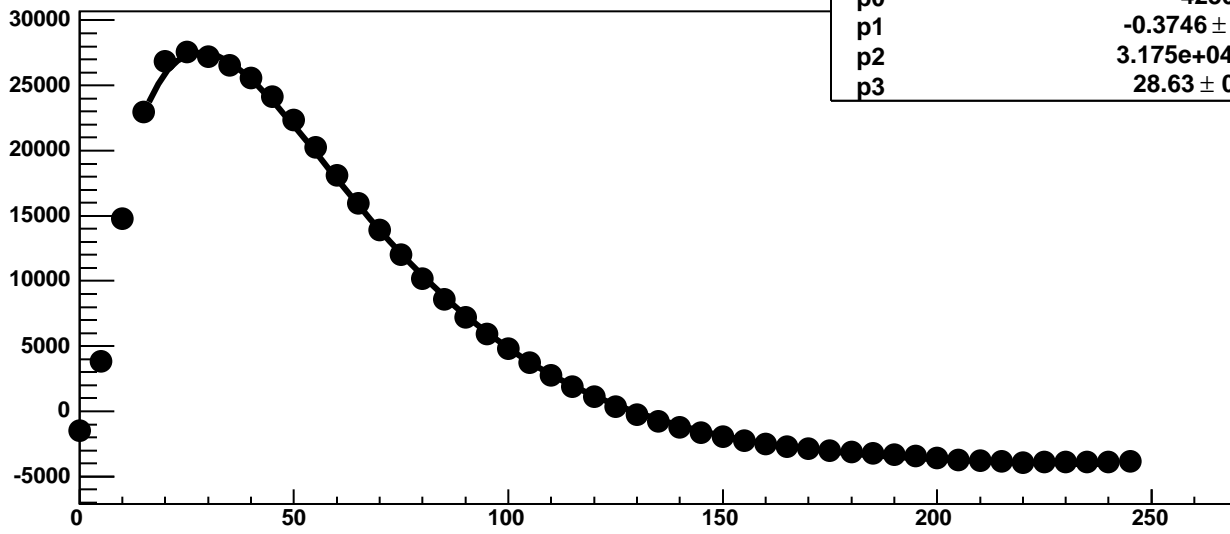
Chip 9, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

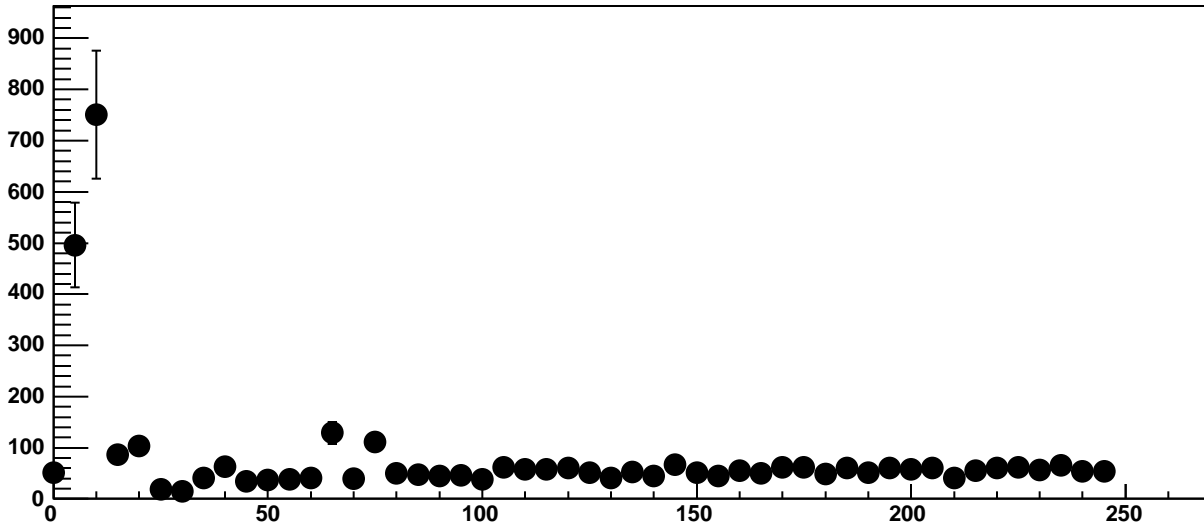


Chip 9, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

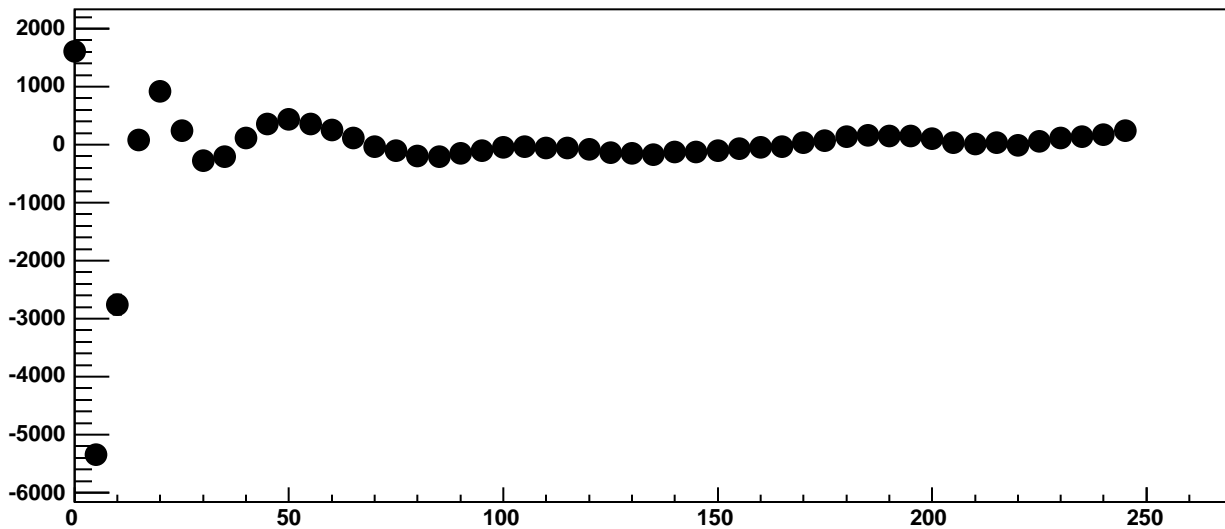


$\chi^2 / \text{ndf}$	2.219e+04 / 42
p0	-4230 ± 3.483
p1	-0.3746 ± 0.01878
p2	3.175e+04 ± 3.995
p3	28.63 ± 0.009812

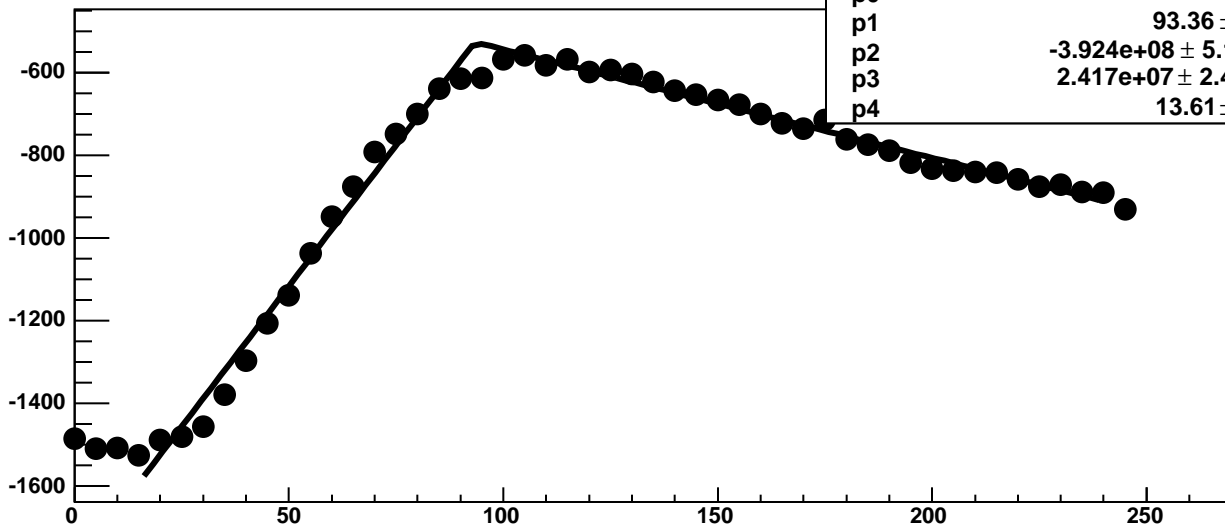
Chip 9, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold

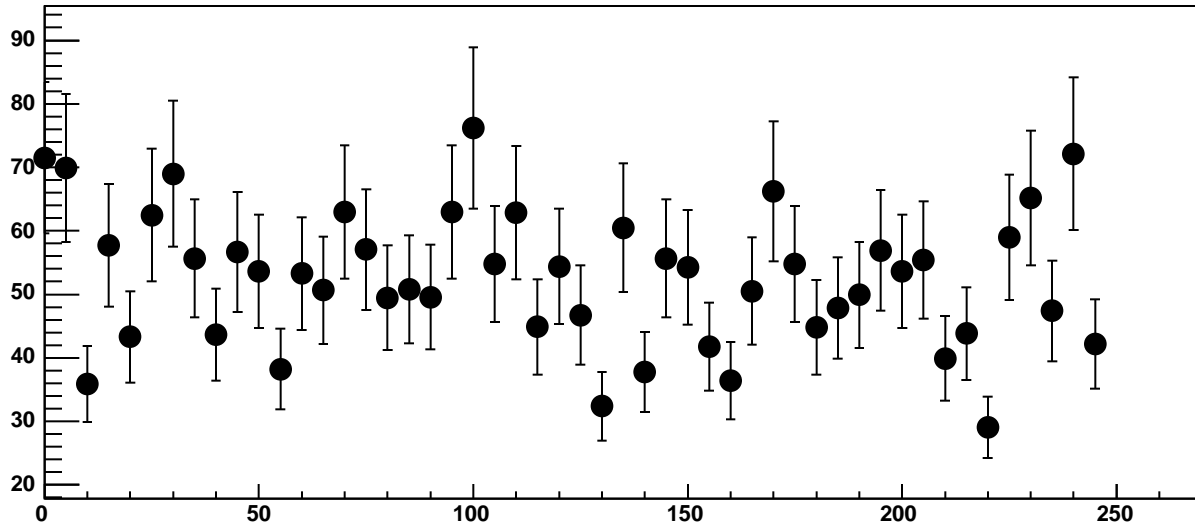


Chip 9, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

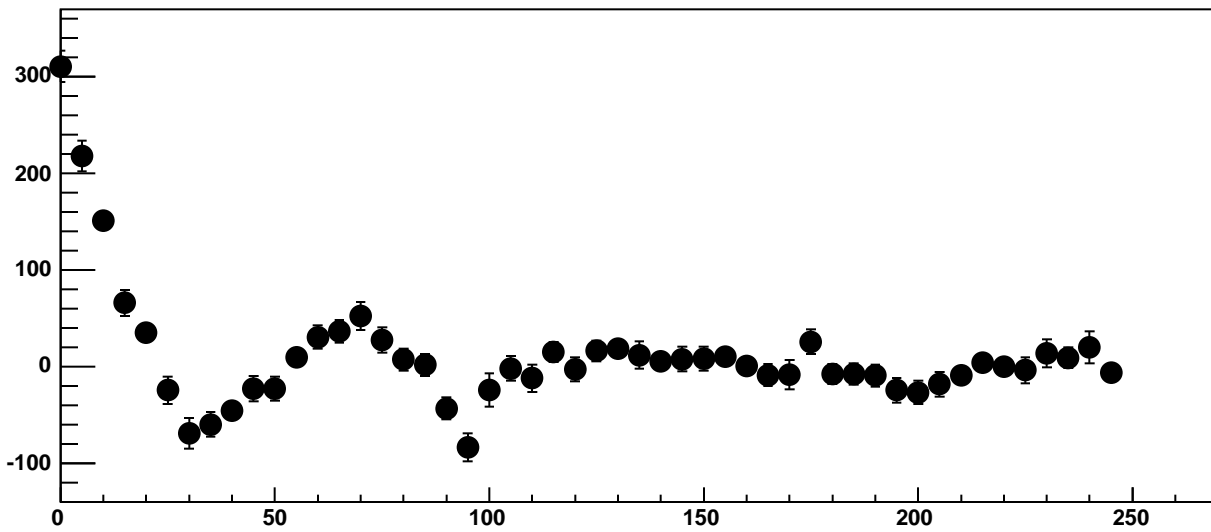


$\chi^2 / \text{ndf}$	228.8 / 41
p0	-525.9 ± 3.708
p1	93.36 ± 0.4536
p2	-3.924e+08 ± 5.136e+06
p3	2.417e+07 ± 2.422e+05
p4	13.61 ± 0.1305

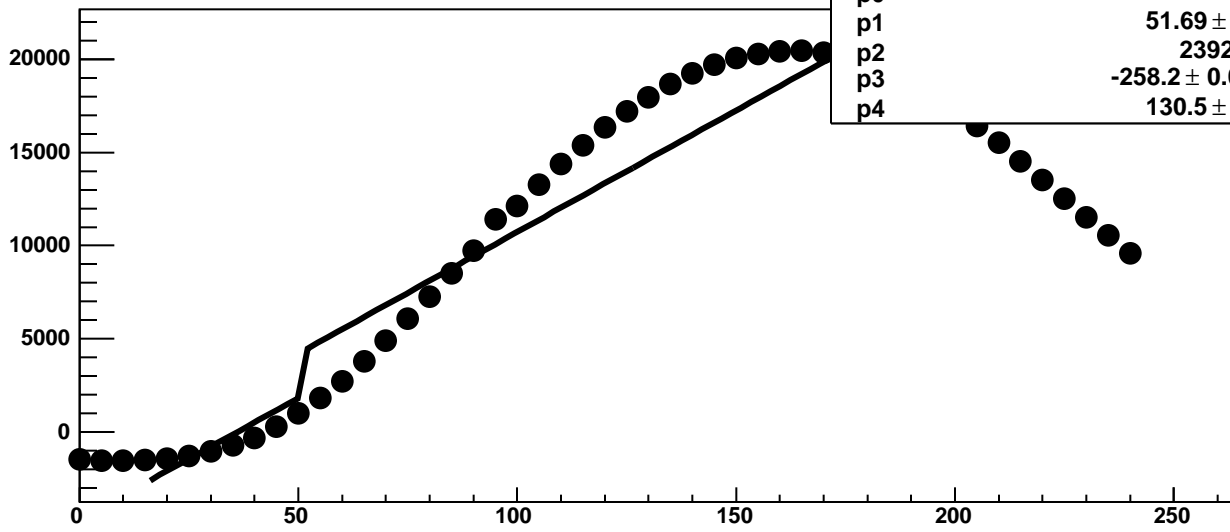
Chip 9, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

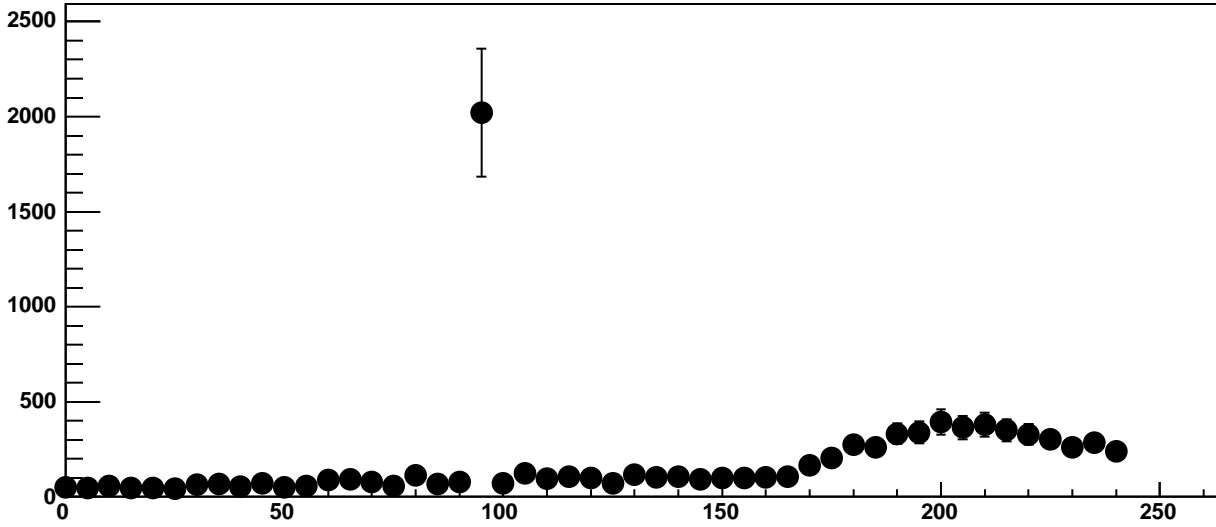


Chip 9, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

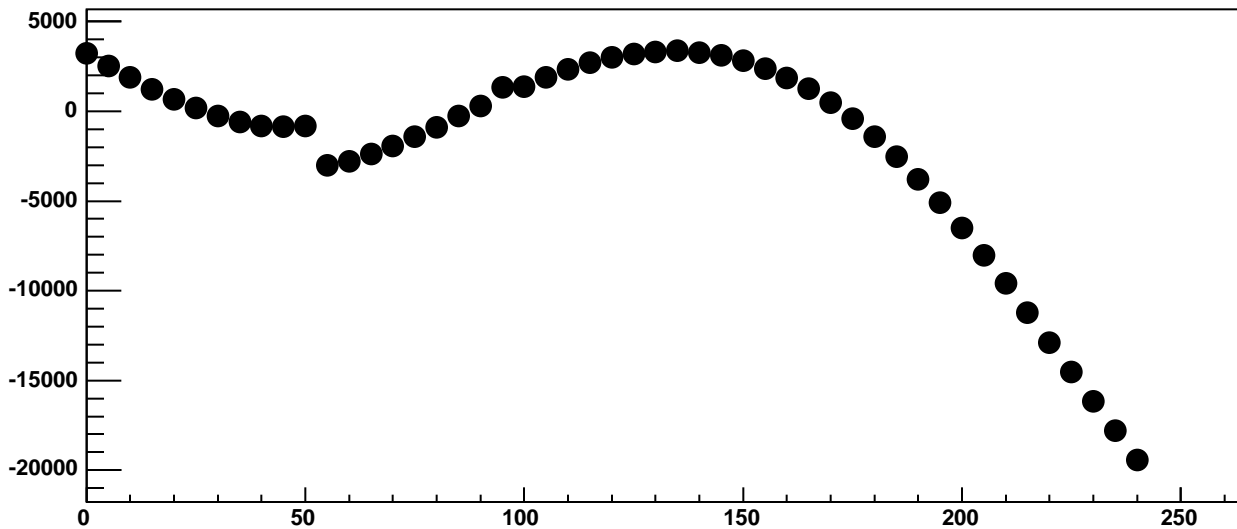


$\chi^2 / \text{ndf}$	7.364e+05 / 41
p0	2035 ± 4.007
p1	51.69 ± 0.03665
p2	2392 ± 9.502
p3	-258.2 ± 0.0003316
p4	130.5 ± 0.09195

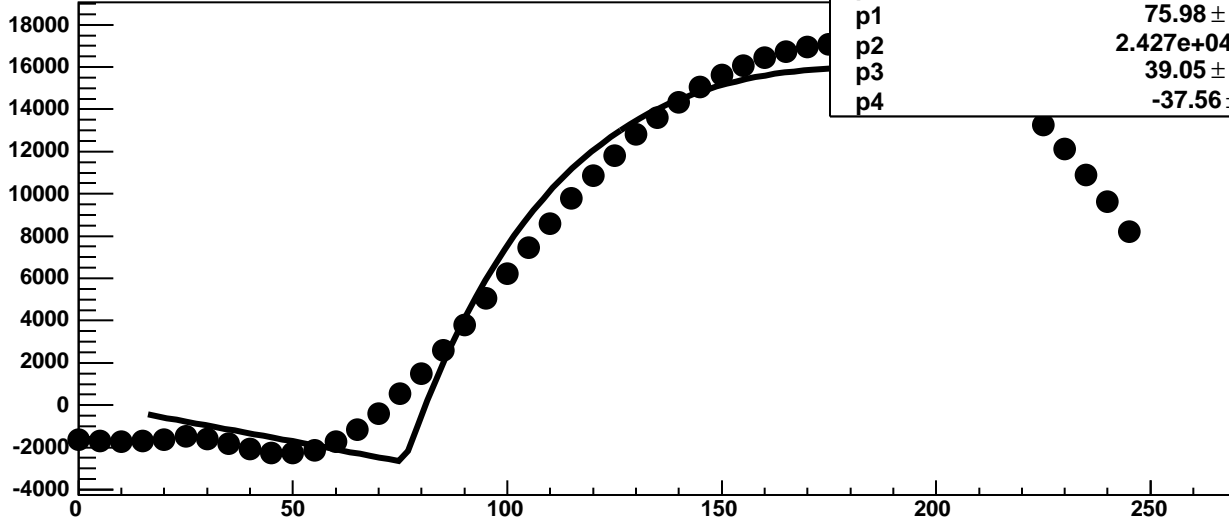
Chip 9, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold

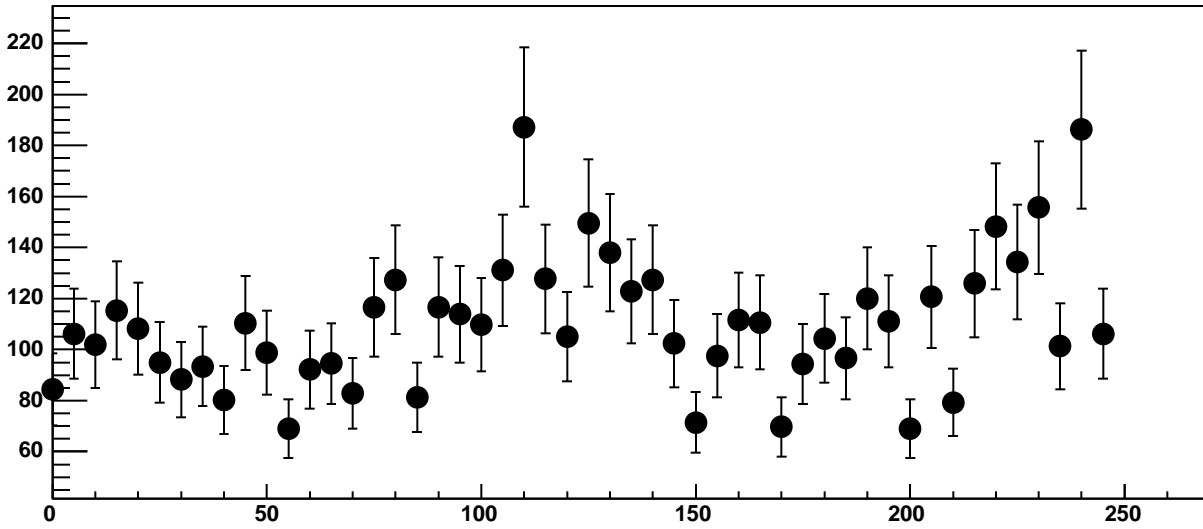


Chip 9, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

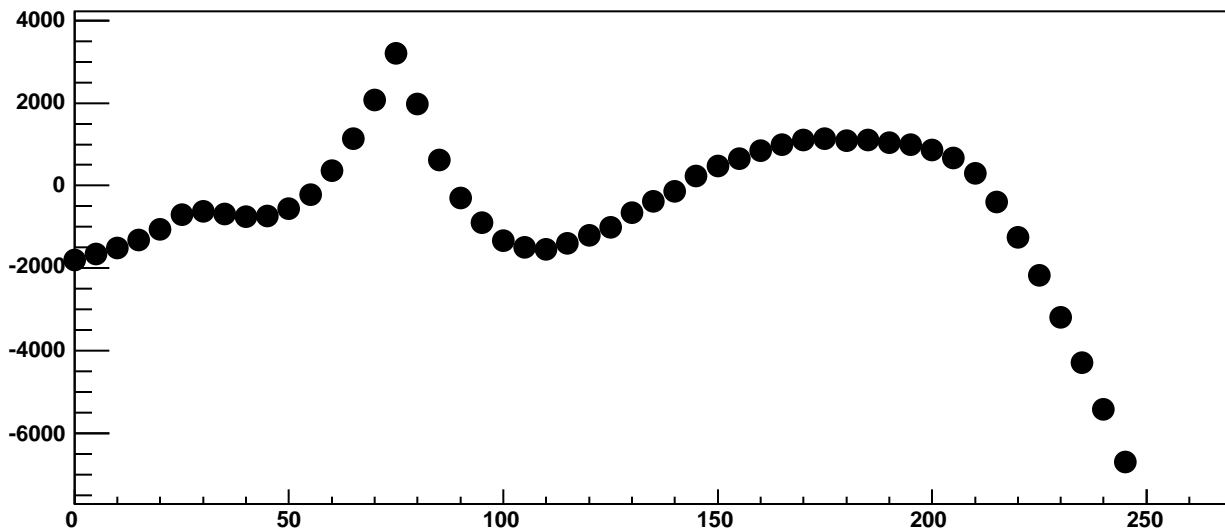


$\chi^2 / \text{ndf}$	1.479e+05 / 41
p0	-2691 ± 8.852
p1	75.98 ± 0.03622
p2	2.427e+04 ± 45.65
p3	39.05 ± 0.09303
p4	-37.56 ± 0.2473

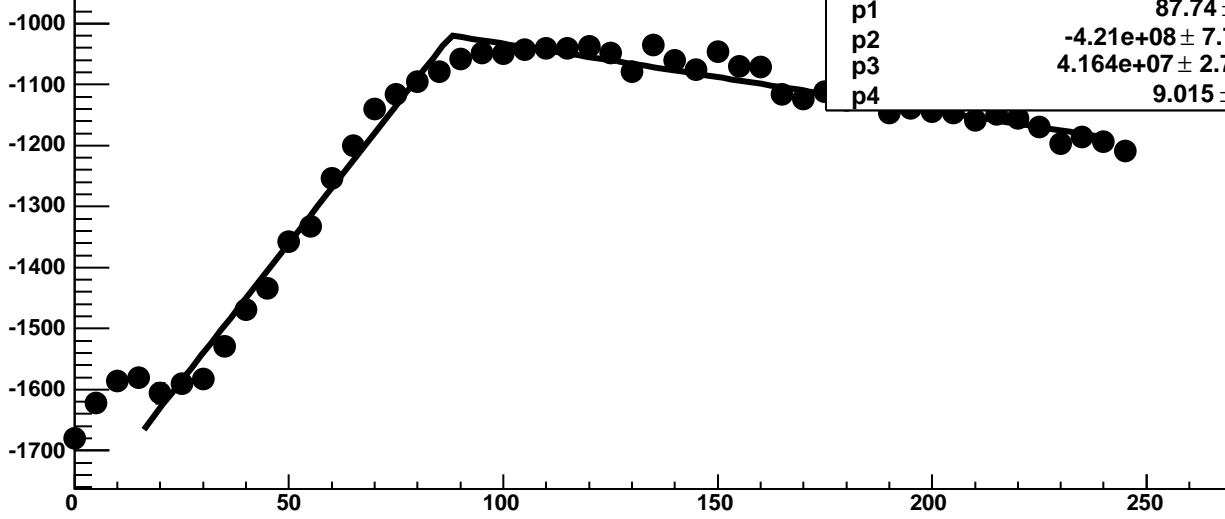
Chip 9, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

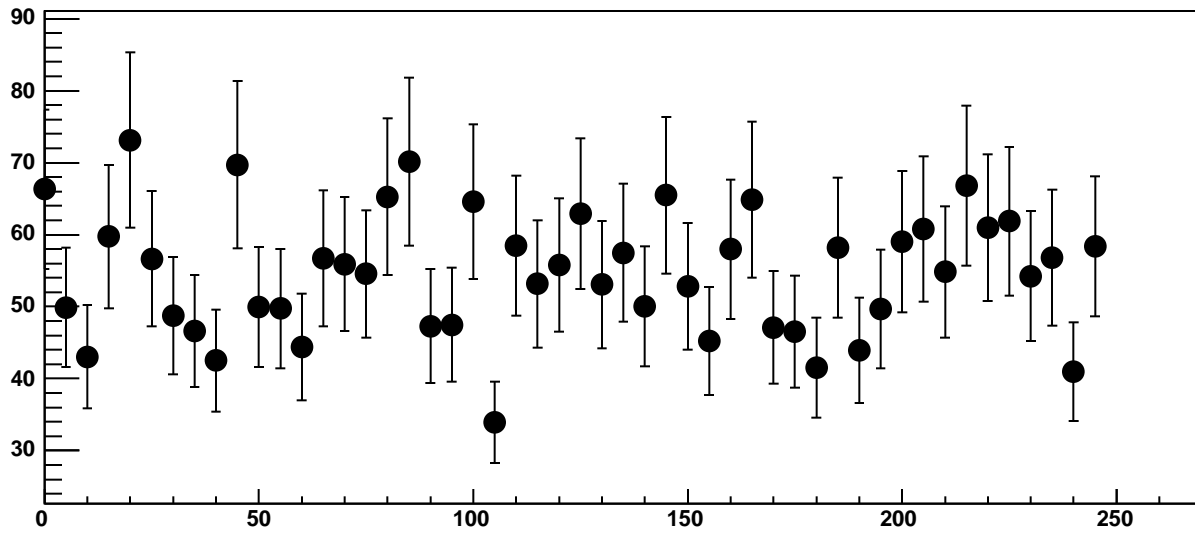


Chip 9, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

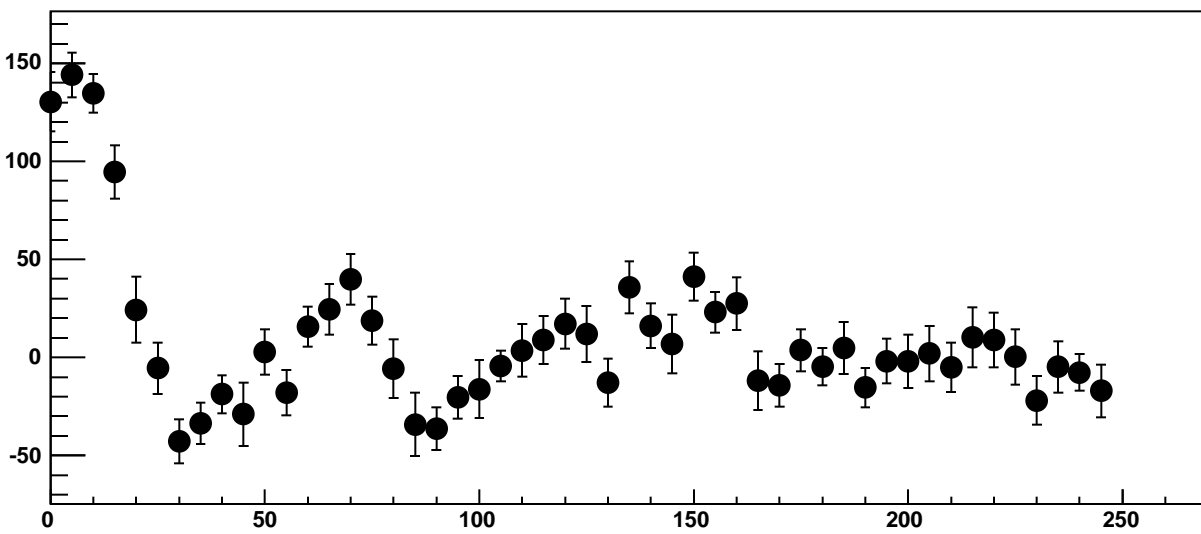


$\chi^2 / \text{ndf}$	167.4 / 41
p0	-1020 ± 3.774
p1	87.74 ± 0.8077
p2	-4.21e+08 ± 7.742e+06
p3	4.164e+07 ± 2.755e+05
p4	9.015 ± 0.1636

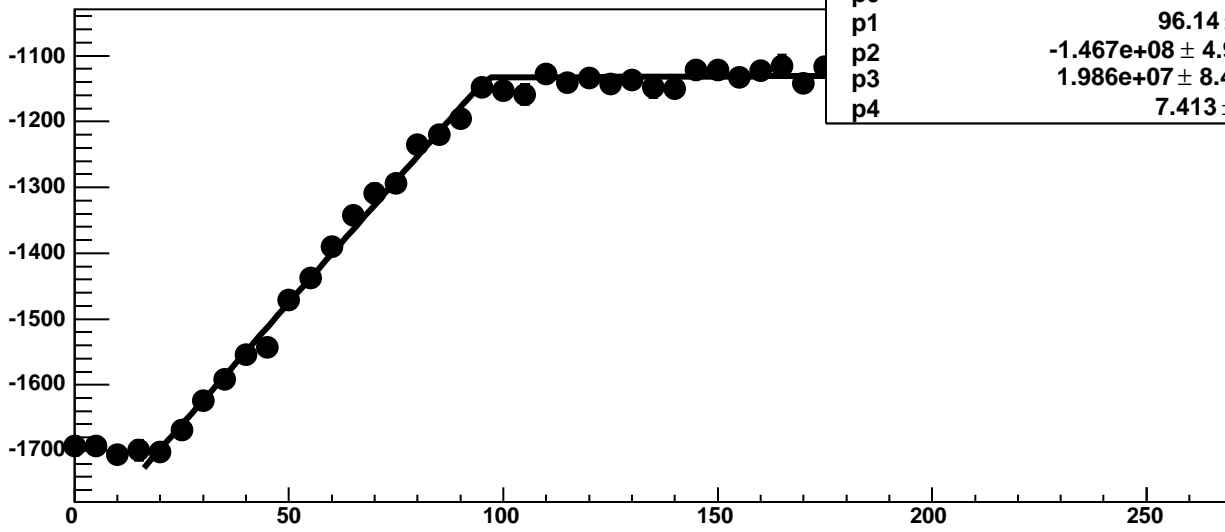
Chip 9, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold

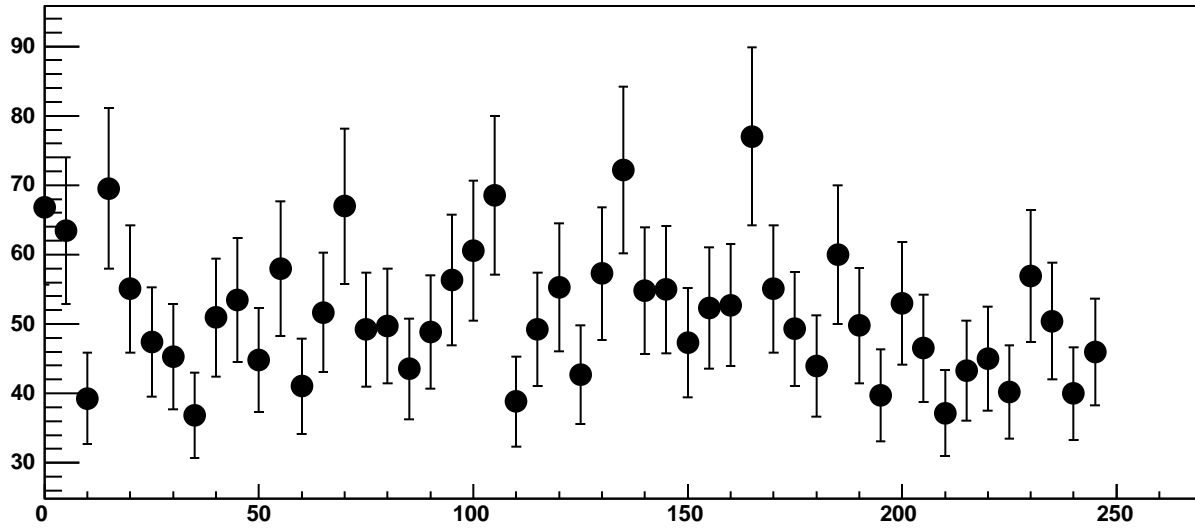


Chip 9, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

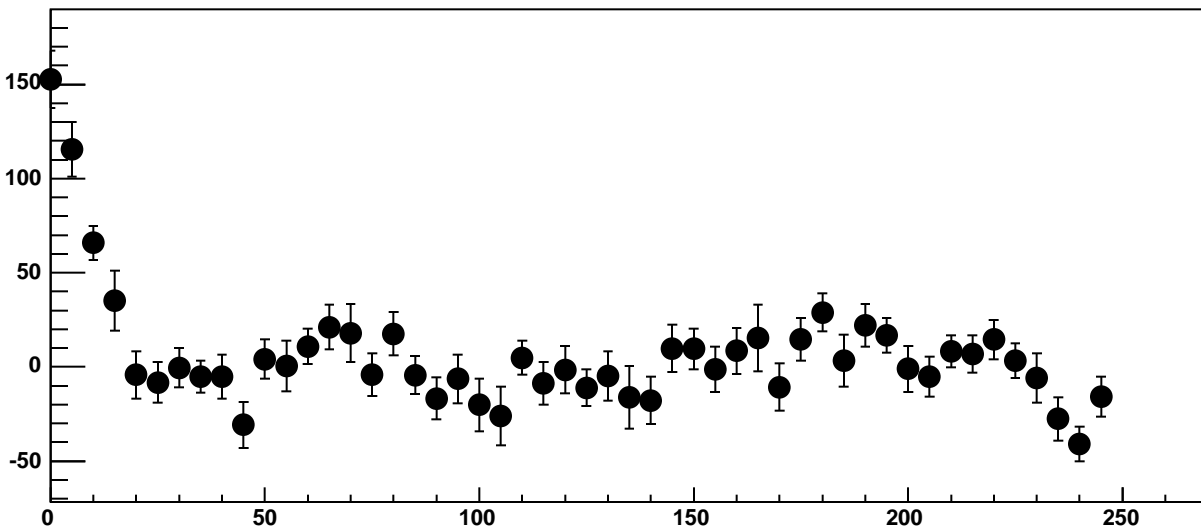


$\chi^2 / \text{ndf}$	83.57 / 41
p0	-1133 ± 4.302
p1	96.14 ± 0.8311
p2	-1.467e+08 ± 4.999e+06
p3	1.986e+07 ± 8.433e+05
p4	7.413 ± 0.1039

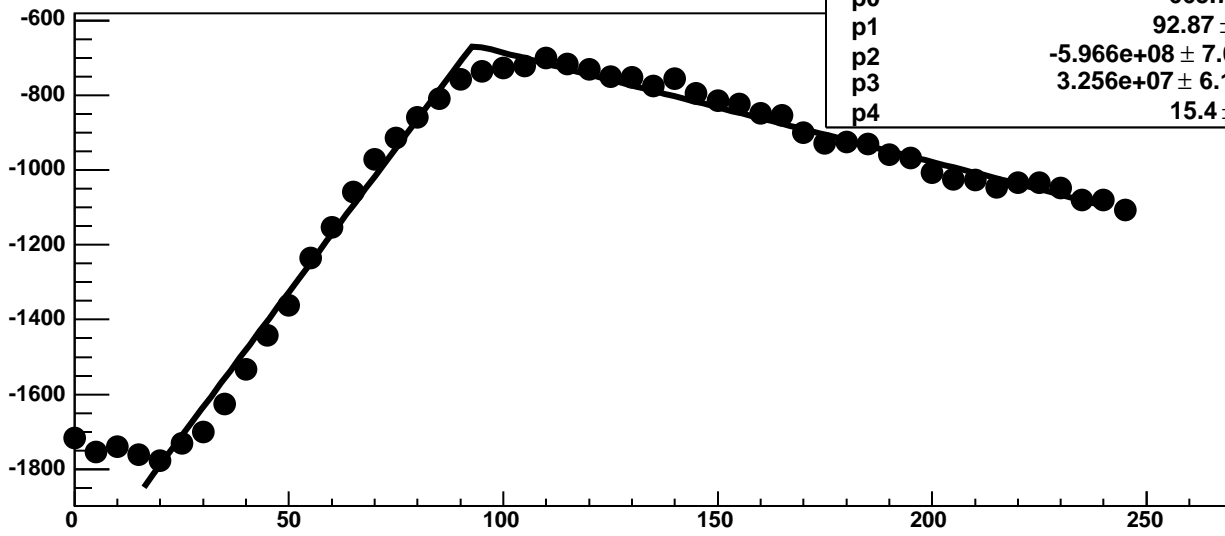
Chip 9, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

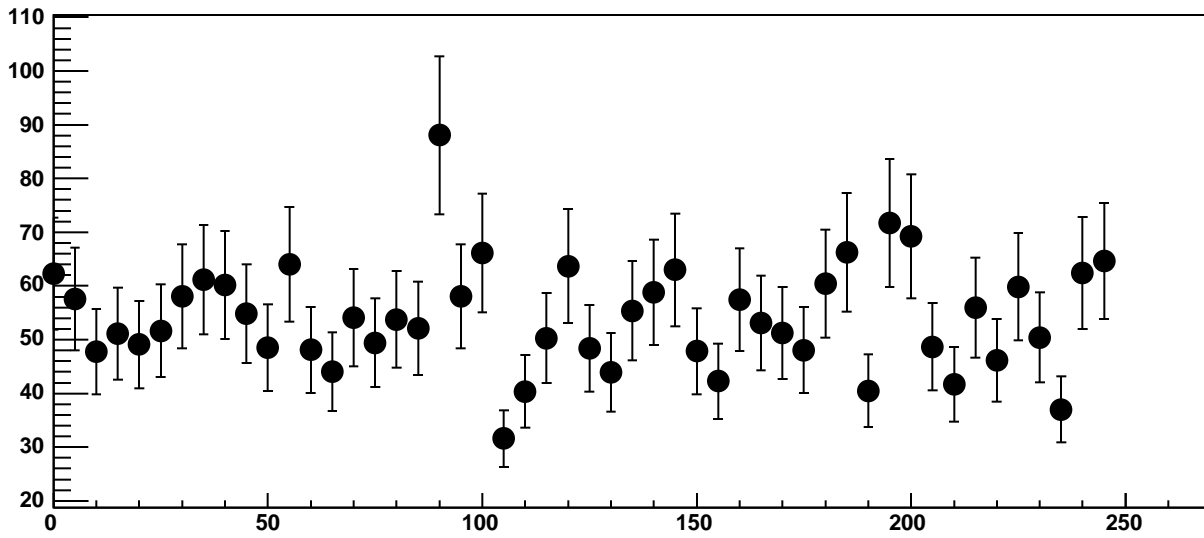


Chip 9, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

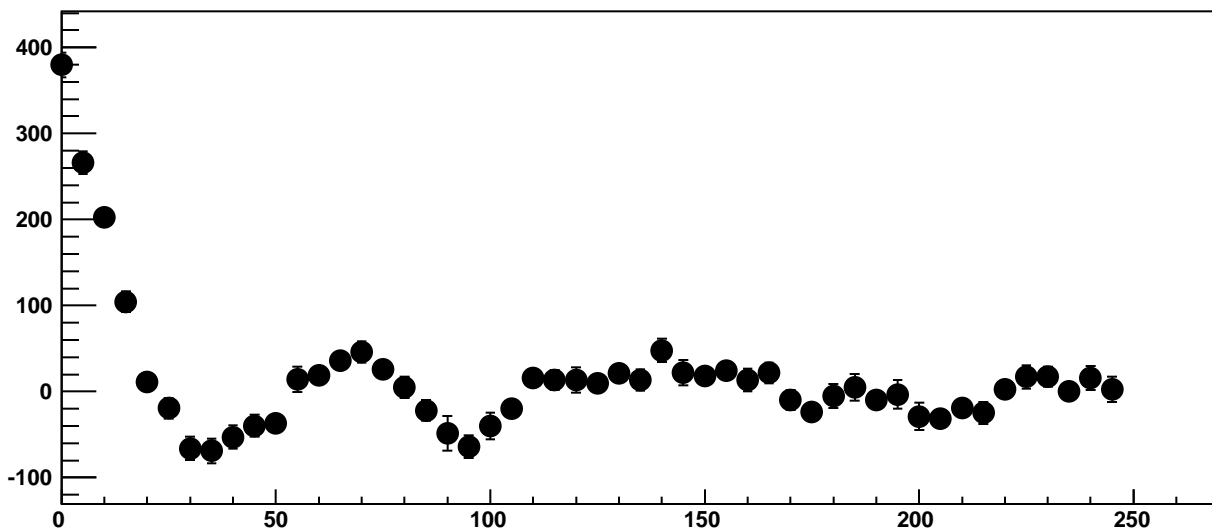


$\chi^2 / \text{ndf}$	319.7 / 41
p0	$-665.7 \pm 4.094$
p1	$92.87 \pm 0.3066$
p2	$-5.966\text{e}+08 \pm 7.014\text{e}+06$
p3	$3.256\text{e}+07 \pm 6.196\text{e}+05$
p4	$15.4 \pm 0.1249$

Chip 9, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

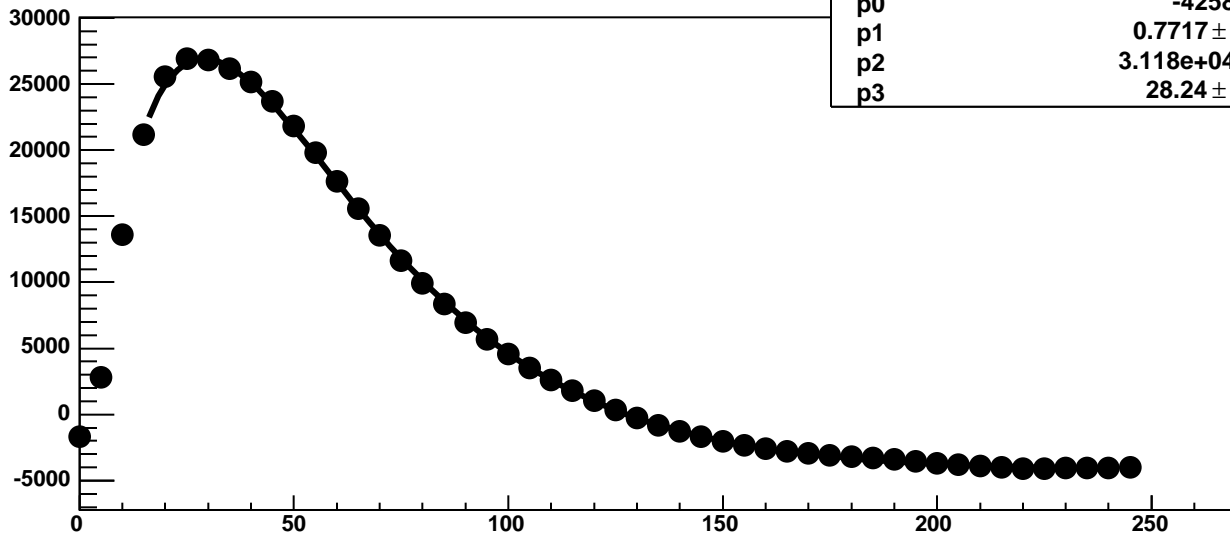


Chip 9, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



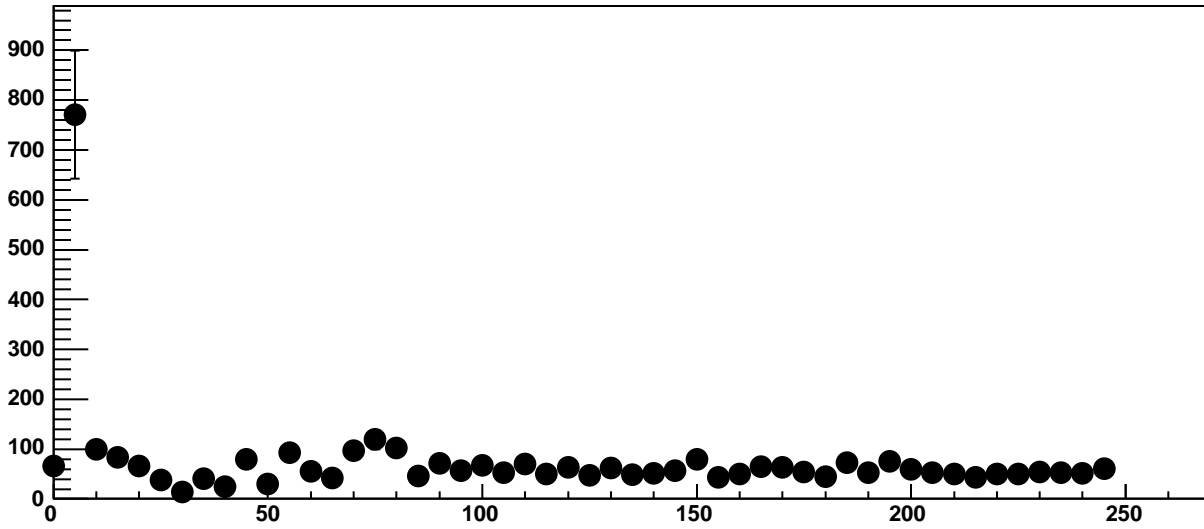


Chip 9, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold

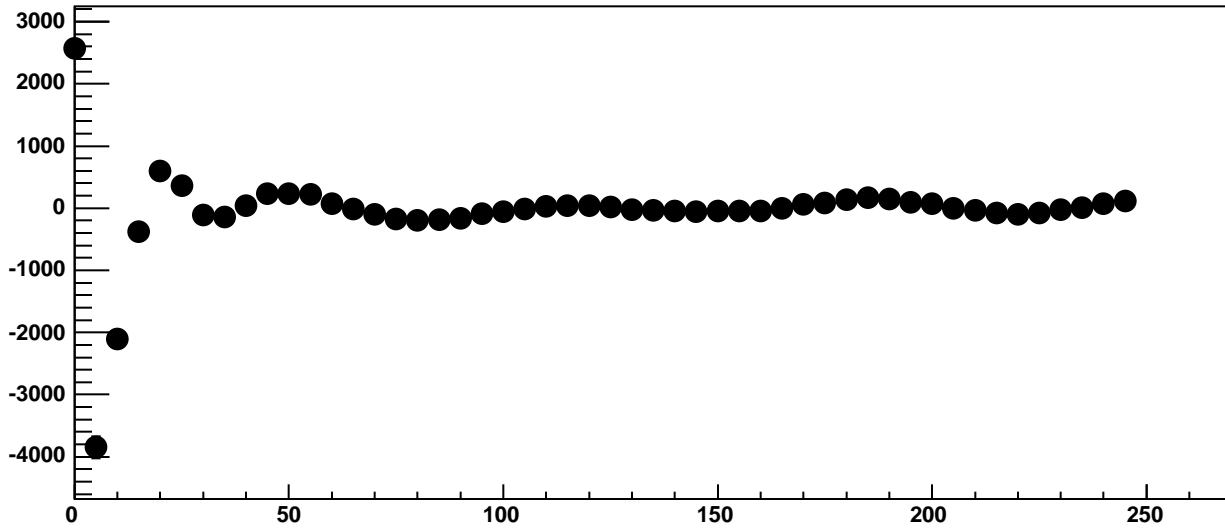


$\chi^2 / \text{ndf}$	7897 / 42
p0	-4258 ± 3.373
p1	0.7717 ± 0.01787
p2	3.118e+04 ± 4.063
p3	28.24 ± 0.01005

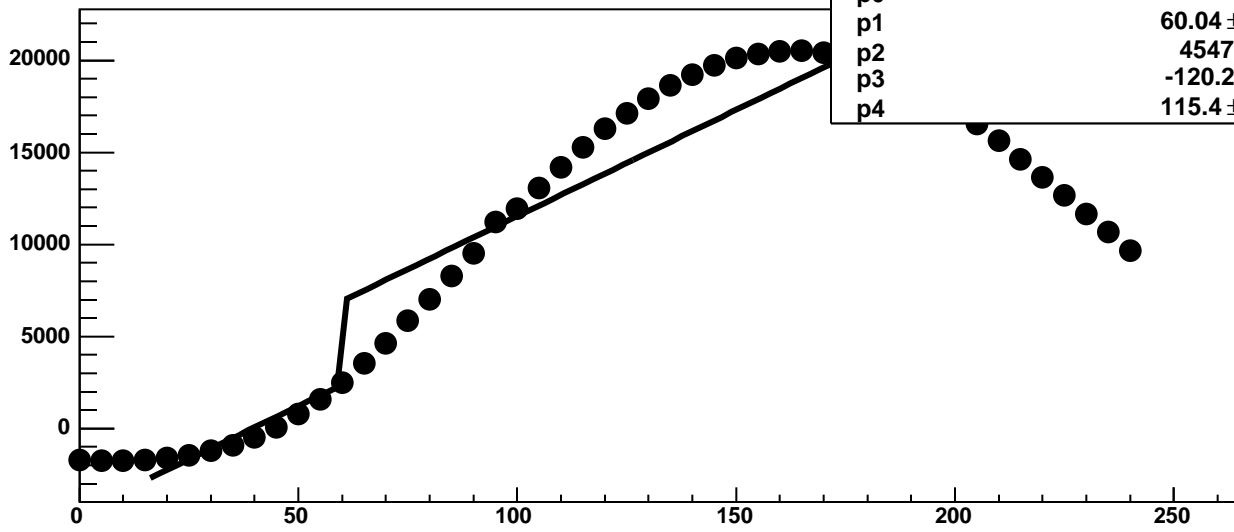
Chip 9, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold

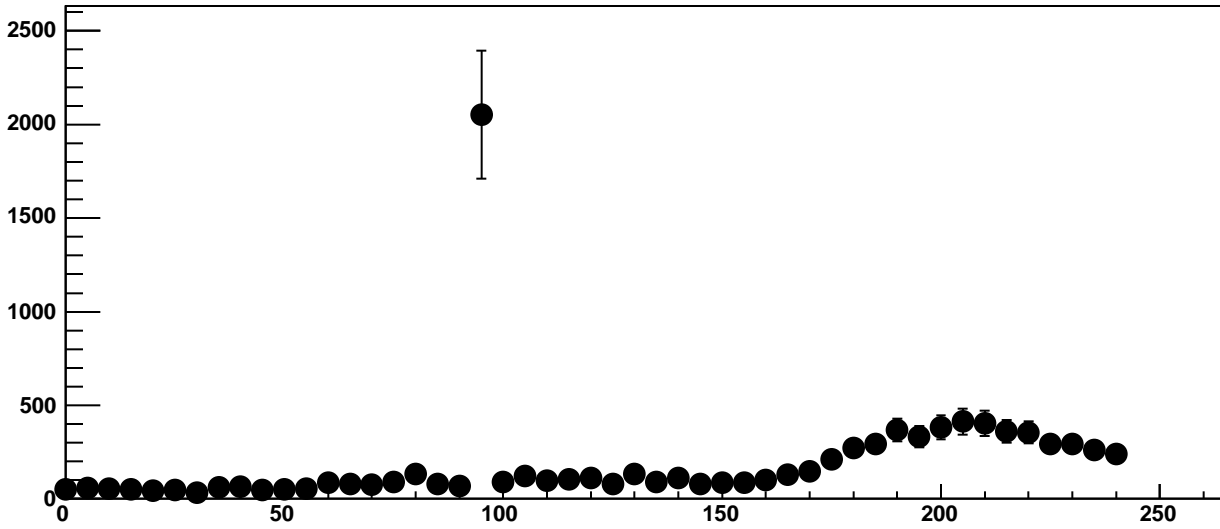


Chip 9, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

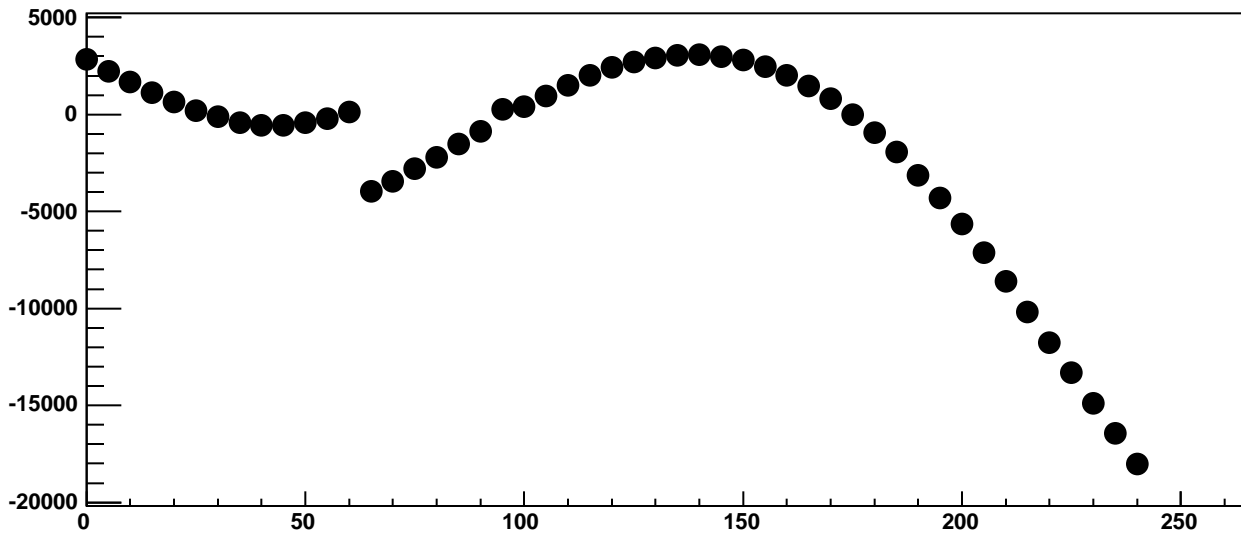


$\chi^2 / \text{ndf}$	6.281e+05 / 41
p0	2378 ± 12.76
p1	60.04 ± 0.1307
p2	4547 ± 31.96
p3	-120.2 ± 12.42
p4	115.4 ± 0.5109

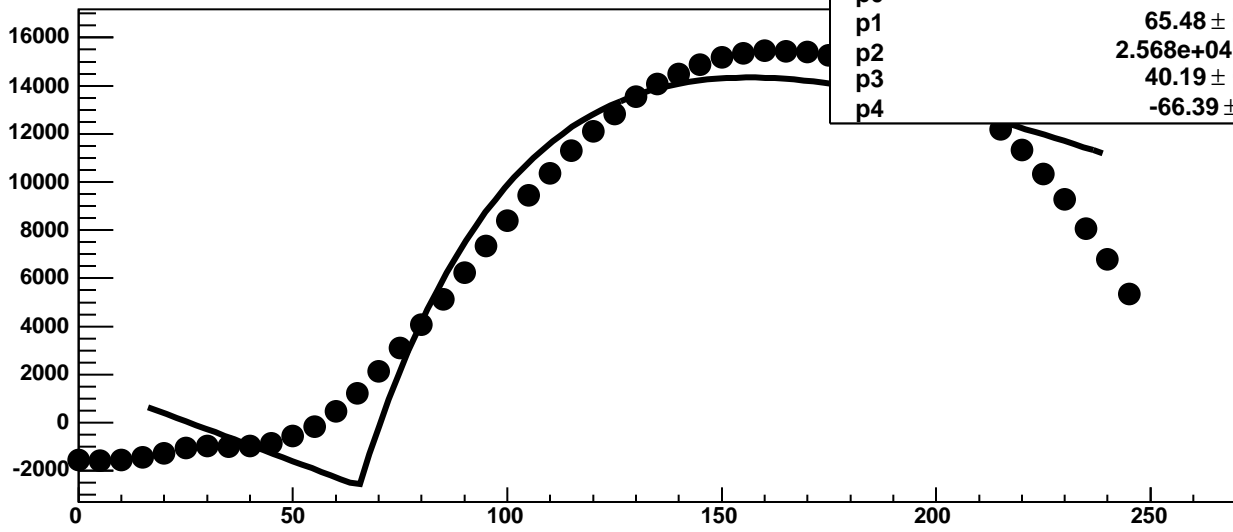
Chip 9, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

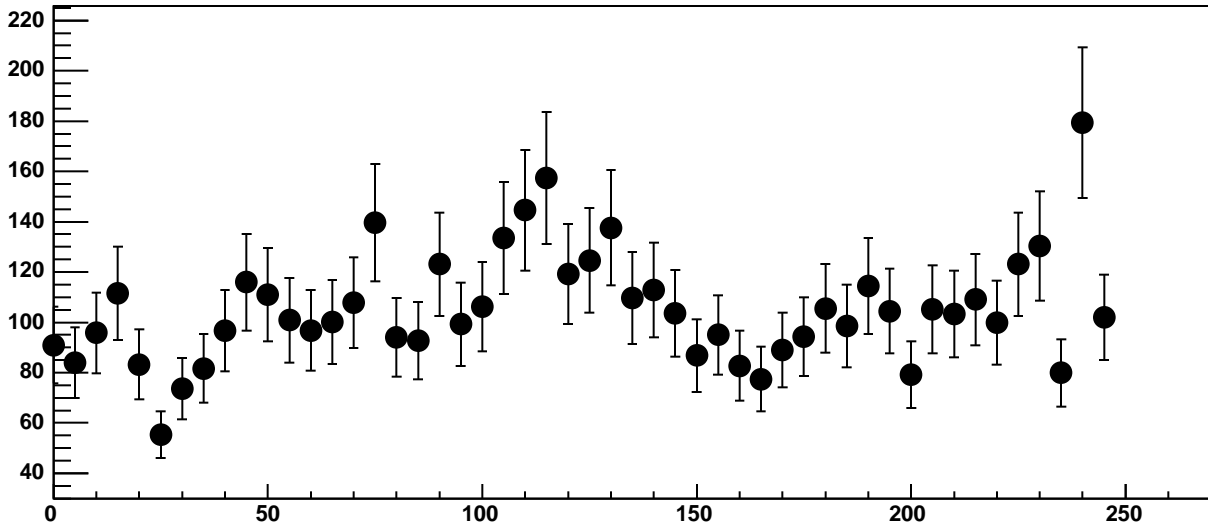


Chip 9, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

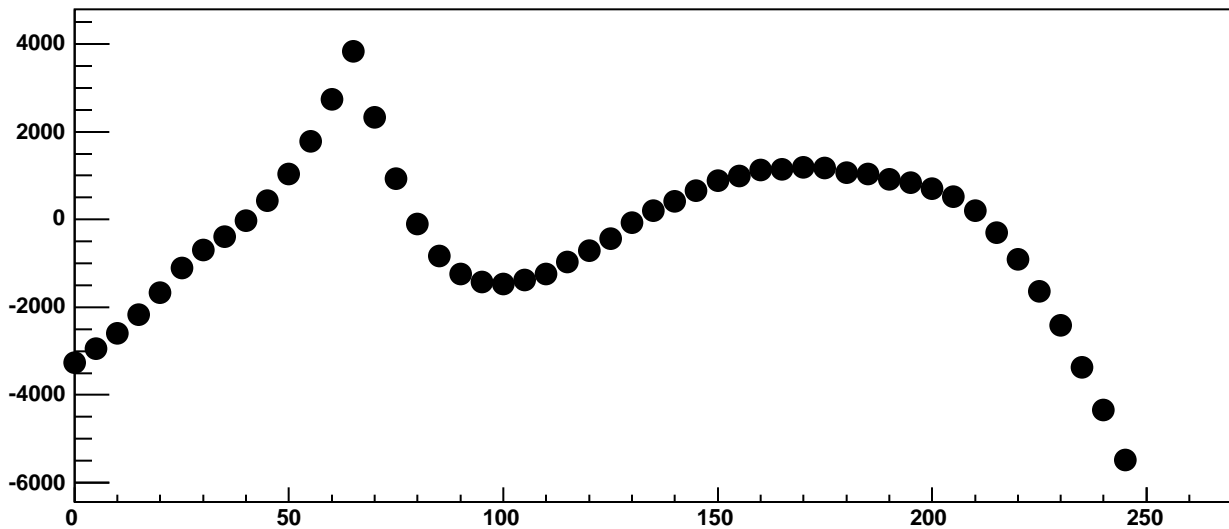


$\chi^2 / \text{ndf}$	1.852e+05 / 41
p0	-2631 ± 8.34
p1	65.48 ± 0.03494
p2	2.568e+04 ± 45.64
p3	40.19 ± 0.08856
p4	-66.39 ± 0.2374

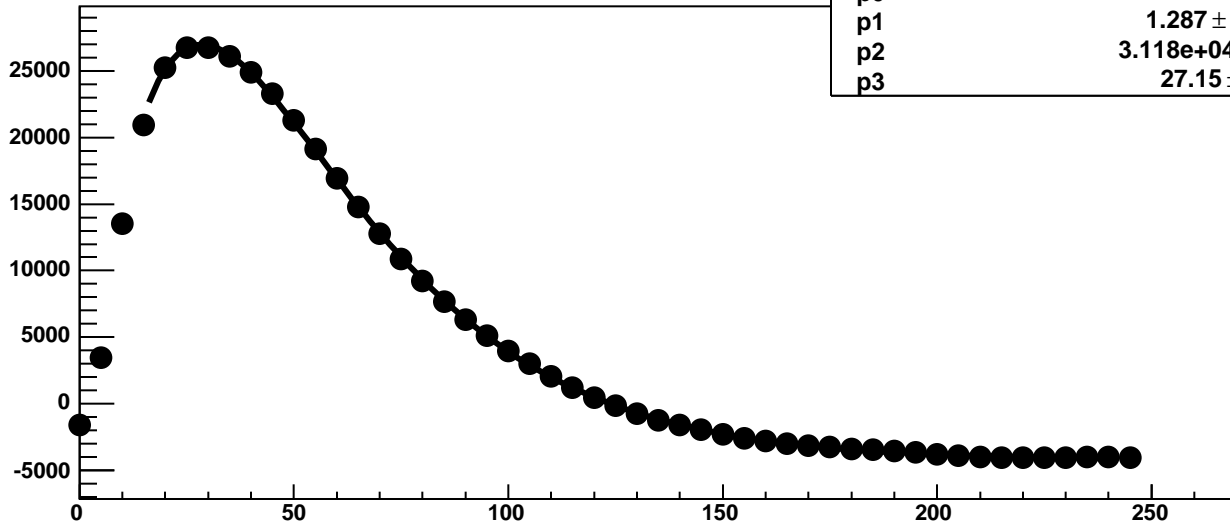
Chip 9, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold

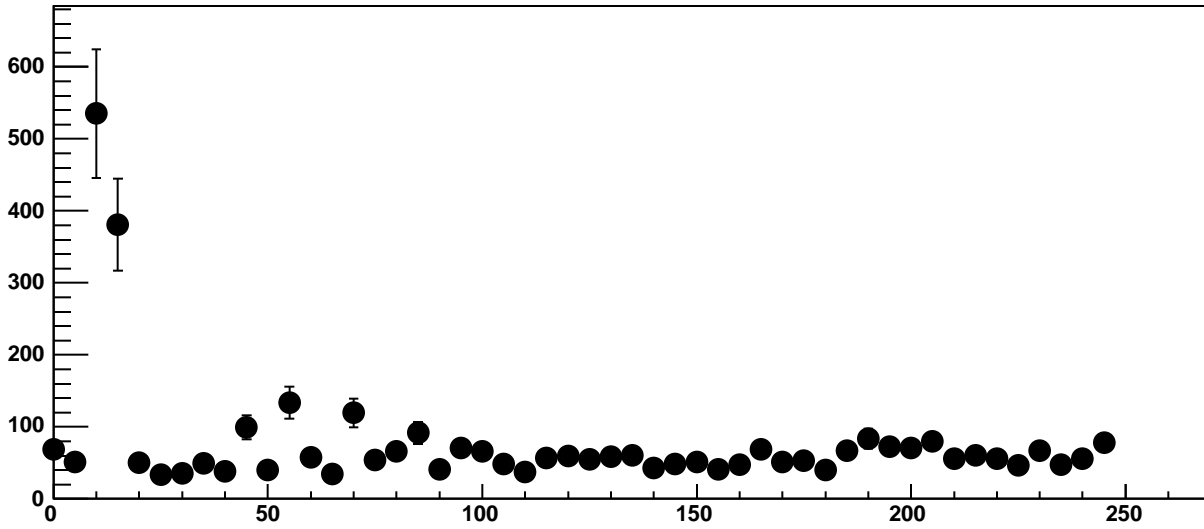


Chip 9, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold

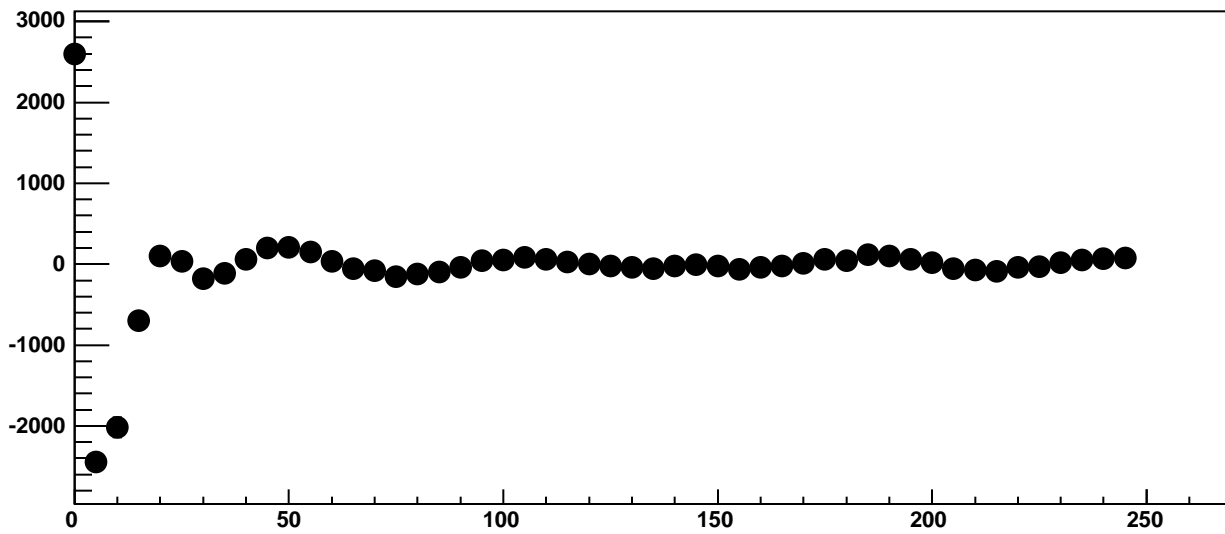


$\chi^2 / \text{ndf}$	2252 / 42
p0	-4196 ± 3.508
p1	1.287 ± 0.02212
p2	3.118e+04 ± 4.943
p3	27.15 ± 0.0113

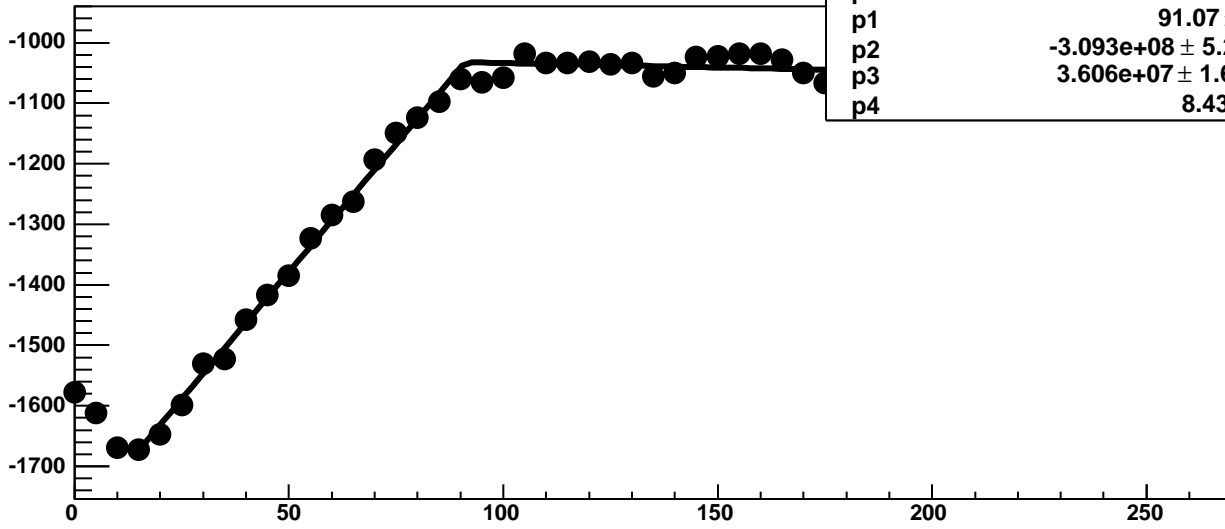
Chip 9, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold

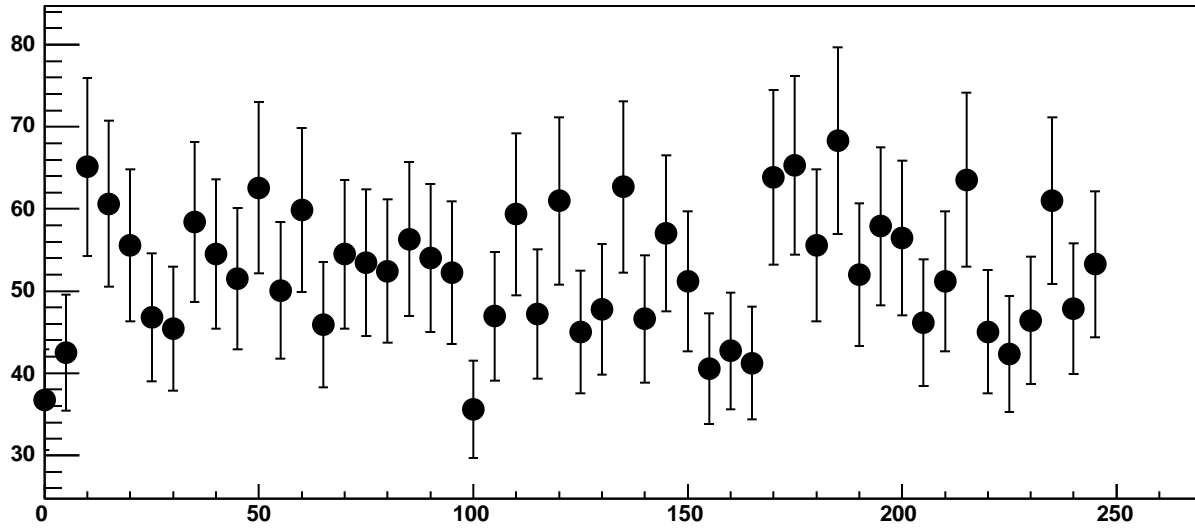


Chip 9, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

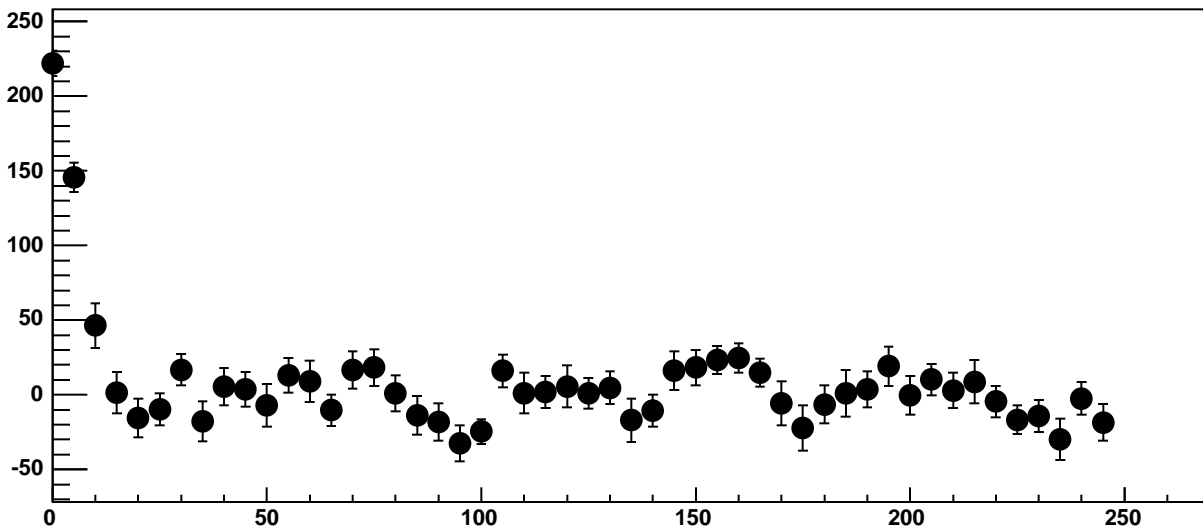


$\chi^2 / \text{ndf}$	72.97 / 41
p0	-1032 ± 4
p1	91.07 ± 0.8491
p2	-3.093e+08 ± 5.229e+06
p3	3.606e+07 ± 1.647e+05
p4	8.43 ± 0.134

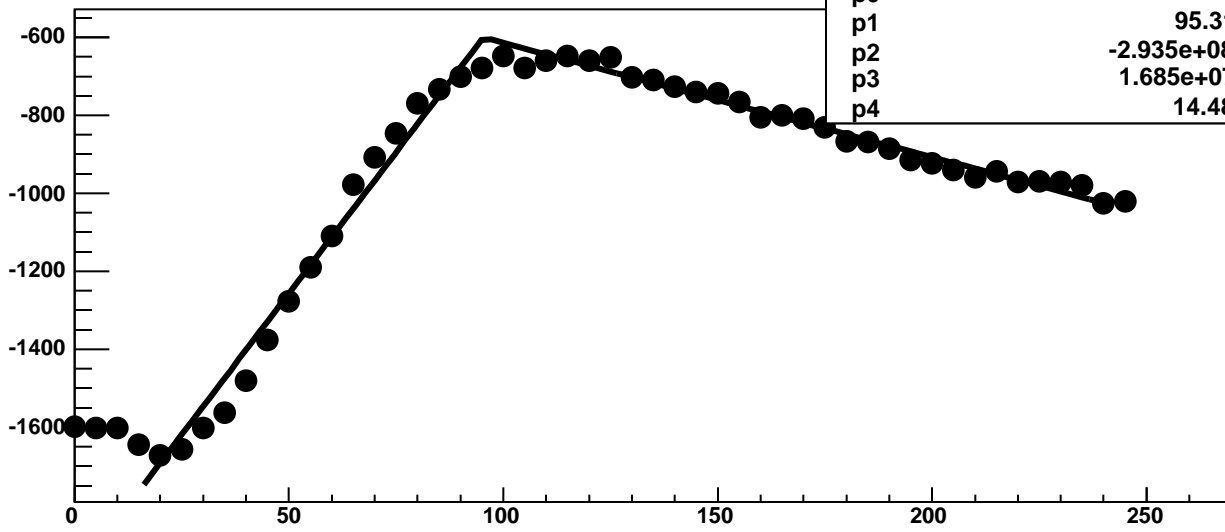
Chip 9, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold

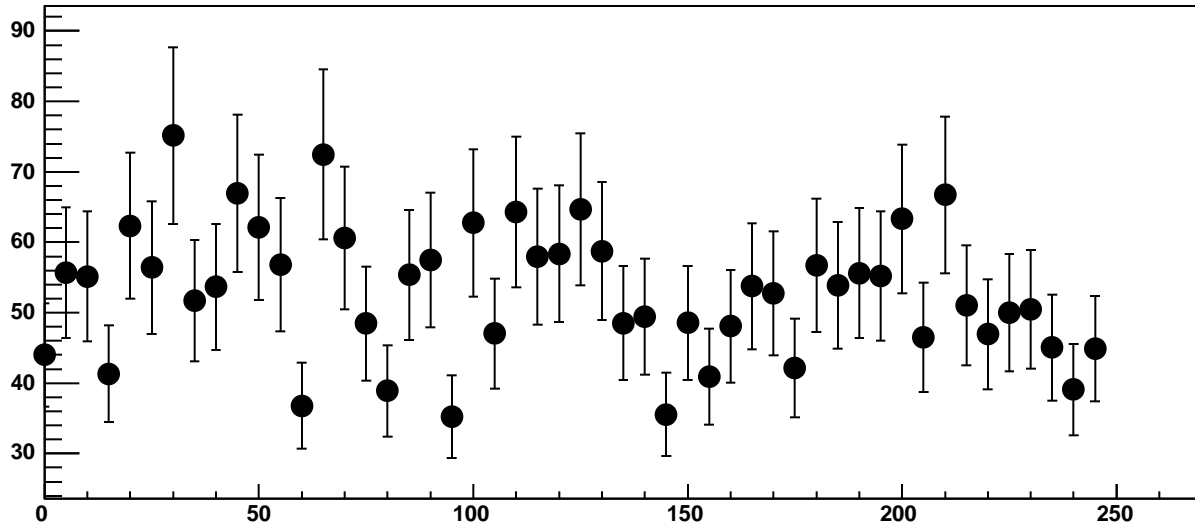


Chip 9, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold

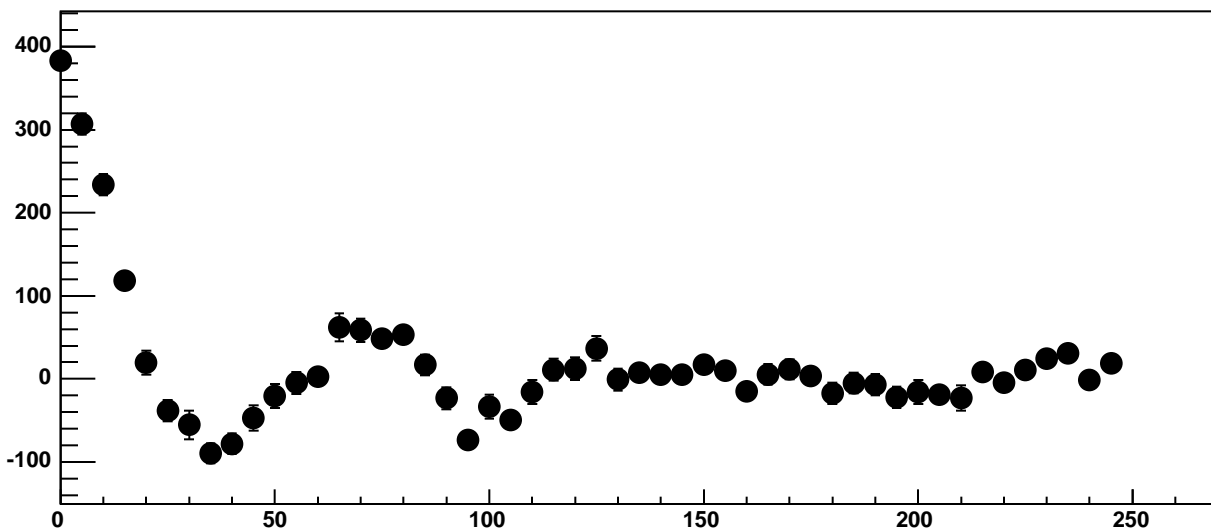


$\chi^2 / \text{ndf}$	529.6 / 41
p0	-600.4 ± nan
p1	95.31 ± nan
p2	-2.935e+08 ± nan
p3	1.685e+07 ± nan
p4	14.48 ± nan

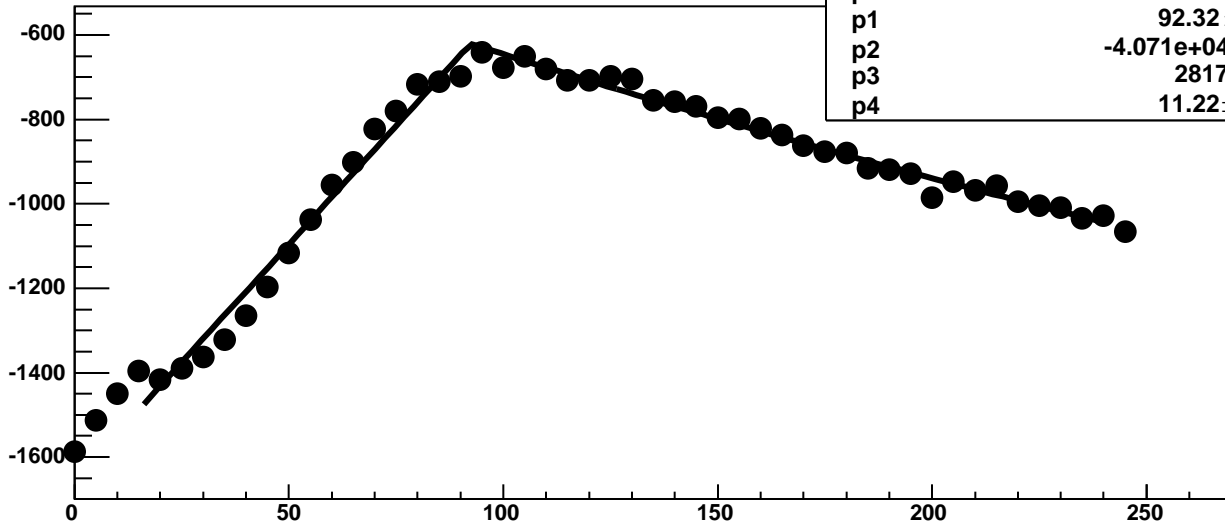
Chip 9, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

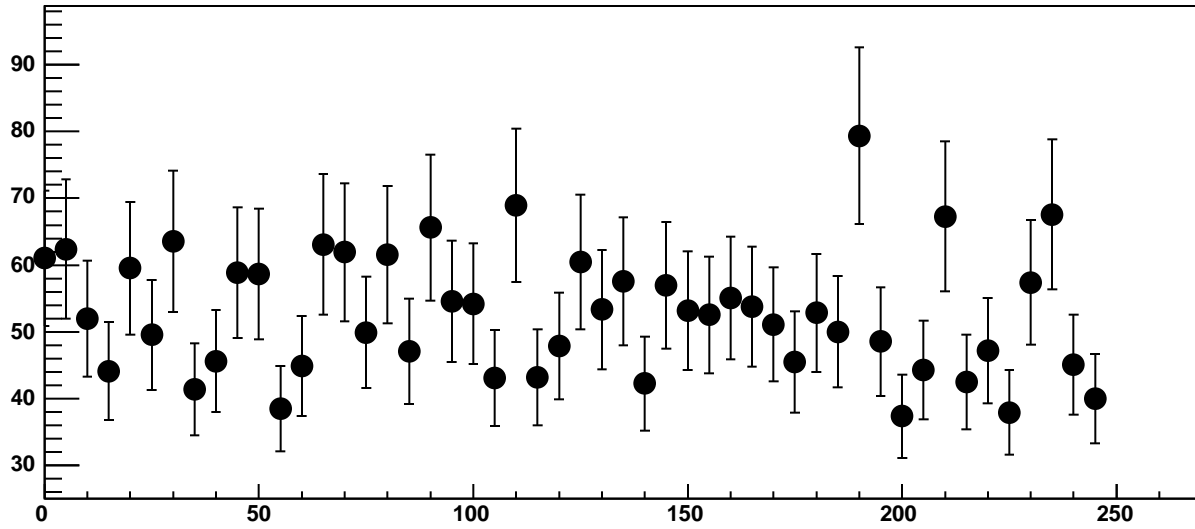


Chip 9, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold

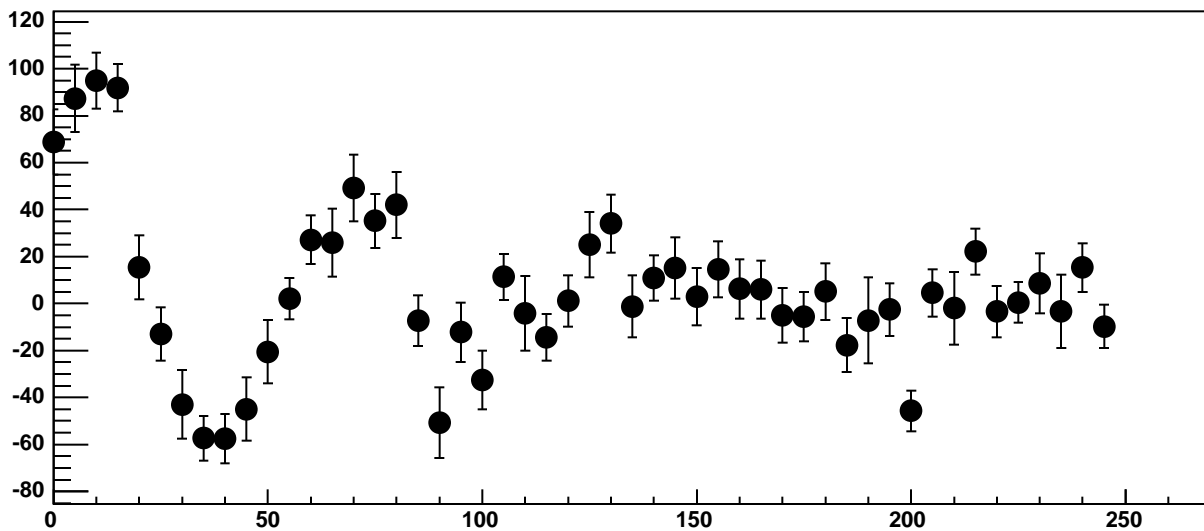


$\chi^2 / \text{ndf}$	292.7 / 41
p0	$-620.6 \pm 3.888$
p1	$92.32 \pm 0.5311$
p2	$-4.071\text{e}+04 \pm 6933$
p3	$2817 \pm 492.2$
p4	$11.22 \pm 0.1312$

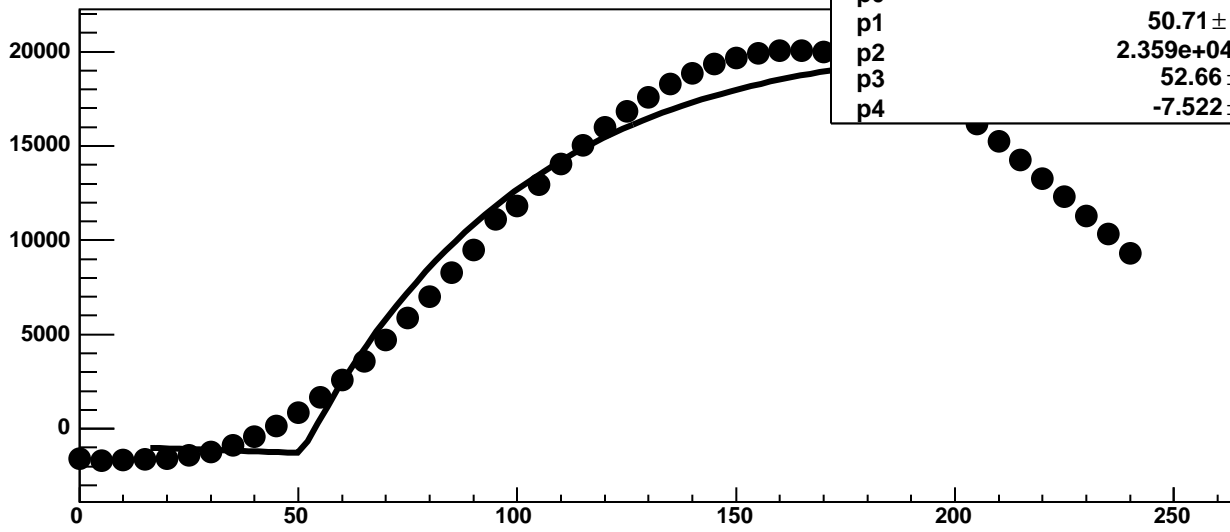
Chip 9, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



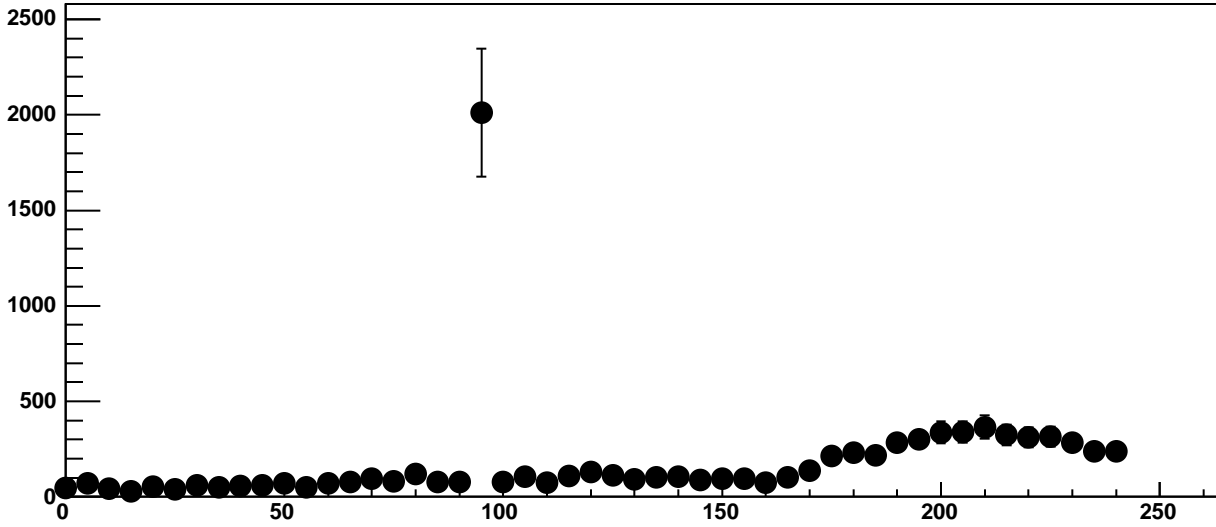
Chip 9, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold



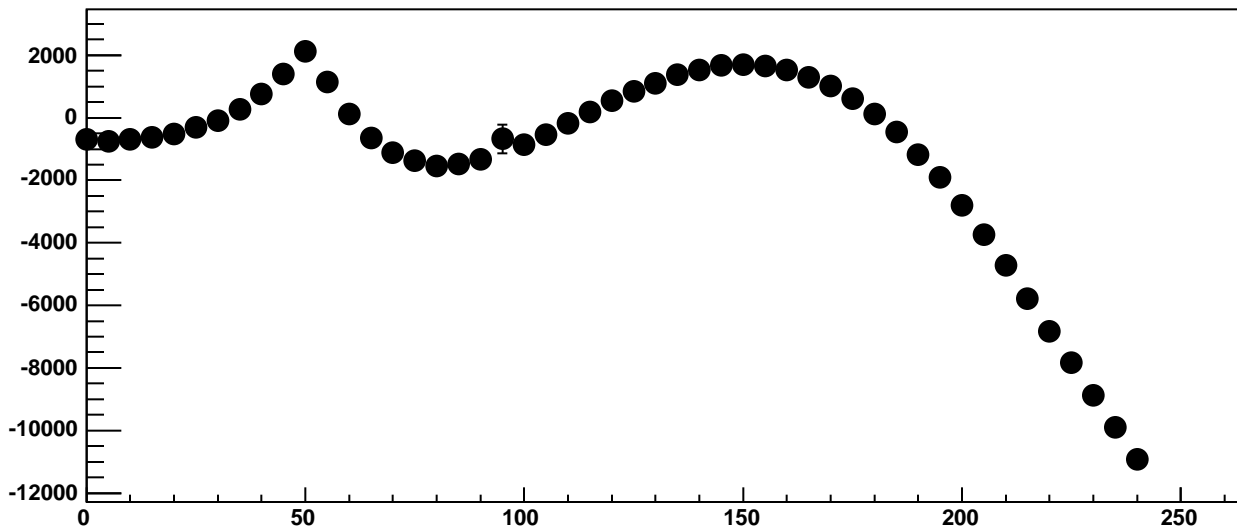
Chip 9, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold



Chip 9, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

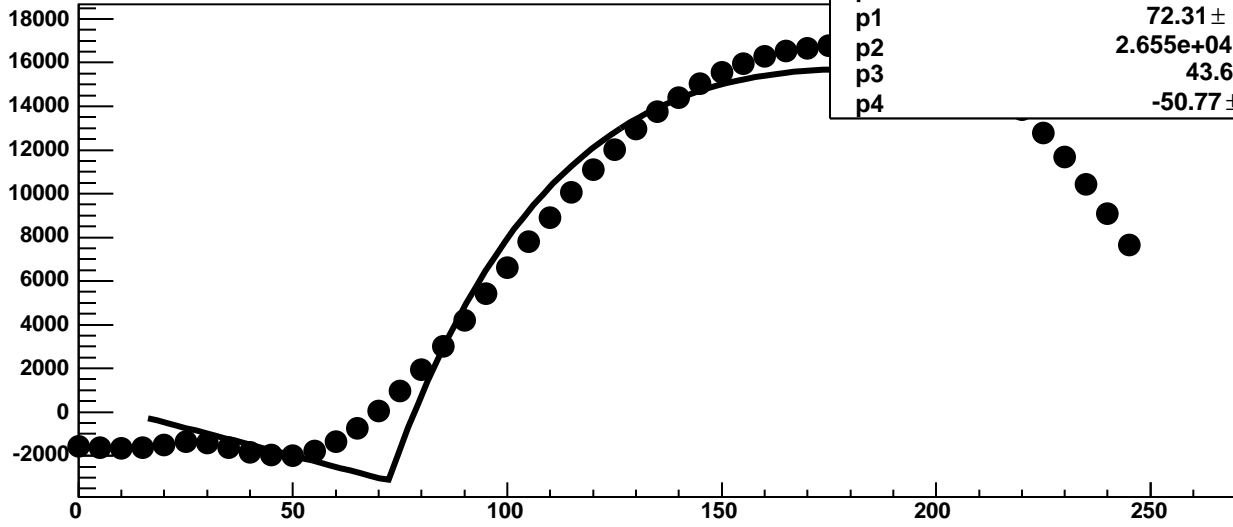


Chip 9, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



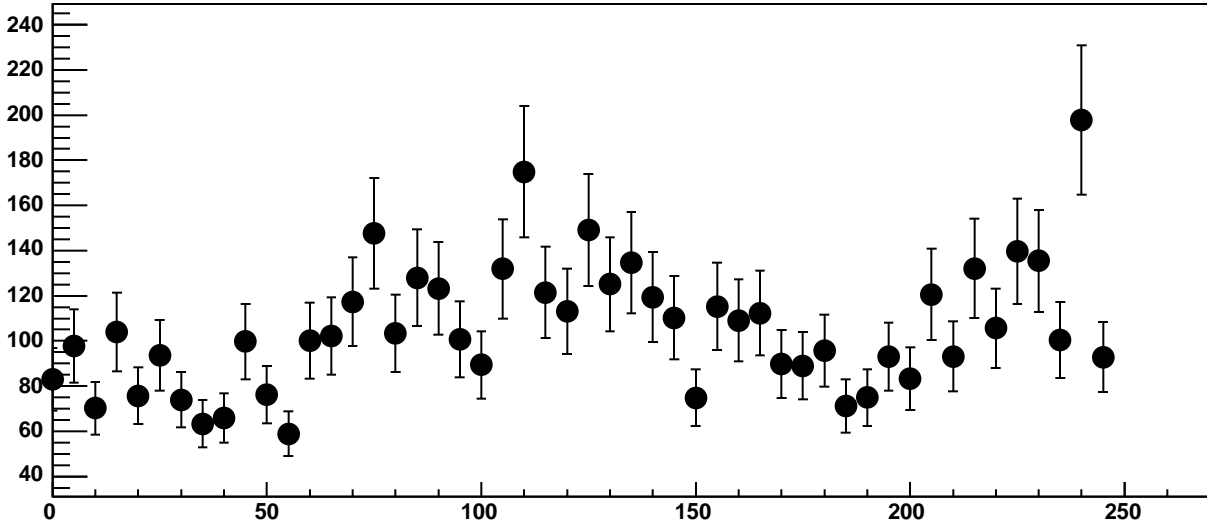


Chip 9, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

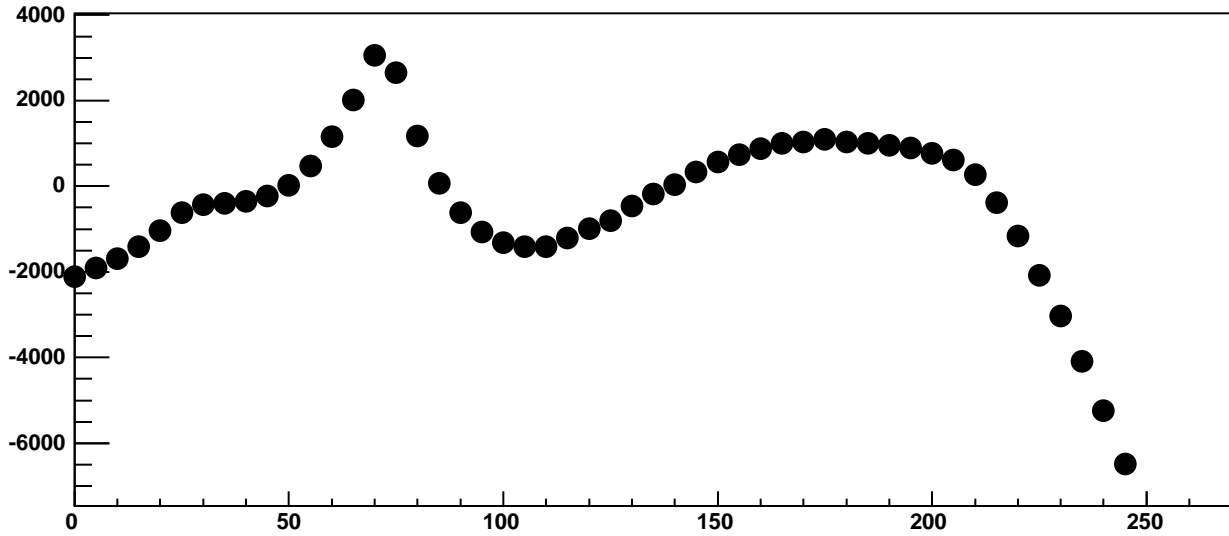


$\chi^2 / \text{ndf}$	1.413e+05 / 41
p0	-3131 ± 8.897
p1	72.31 ± 0.03727
p2	2.655e+04 ± 50.63
p3	43.6 ± 0.098
p4	-50.77 ± 0.2593

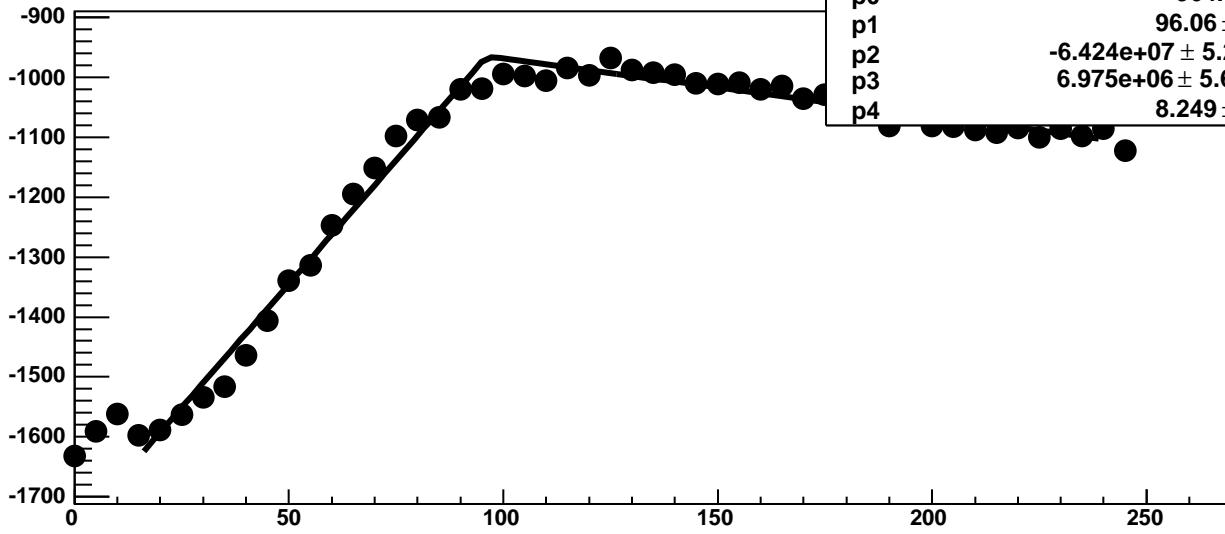
Chip 9, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

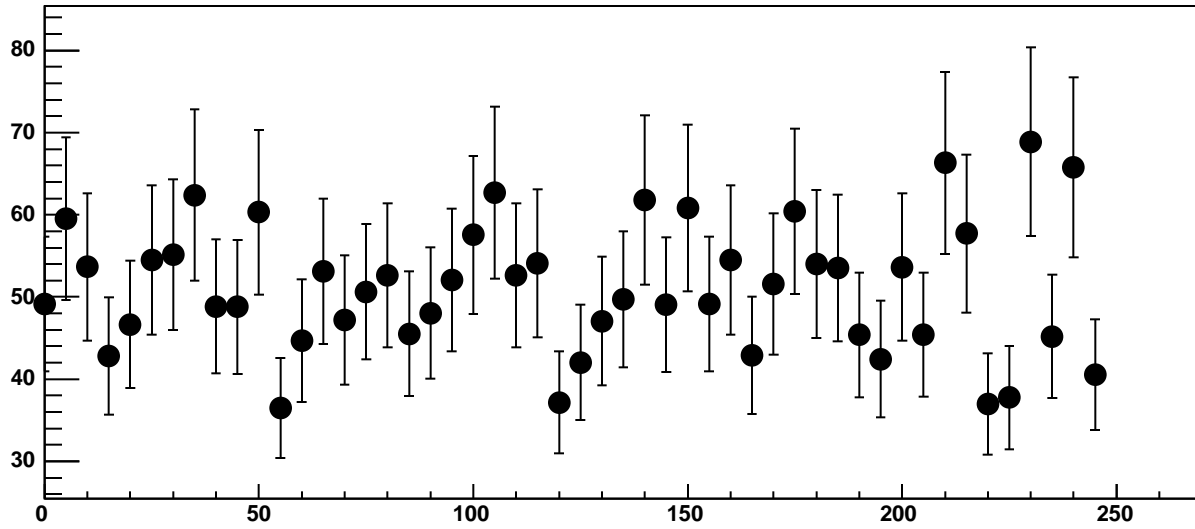


Chip 9, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

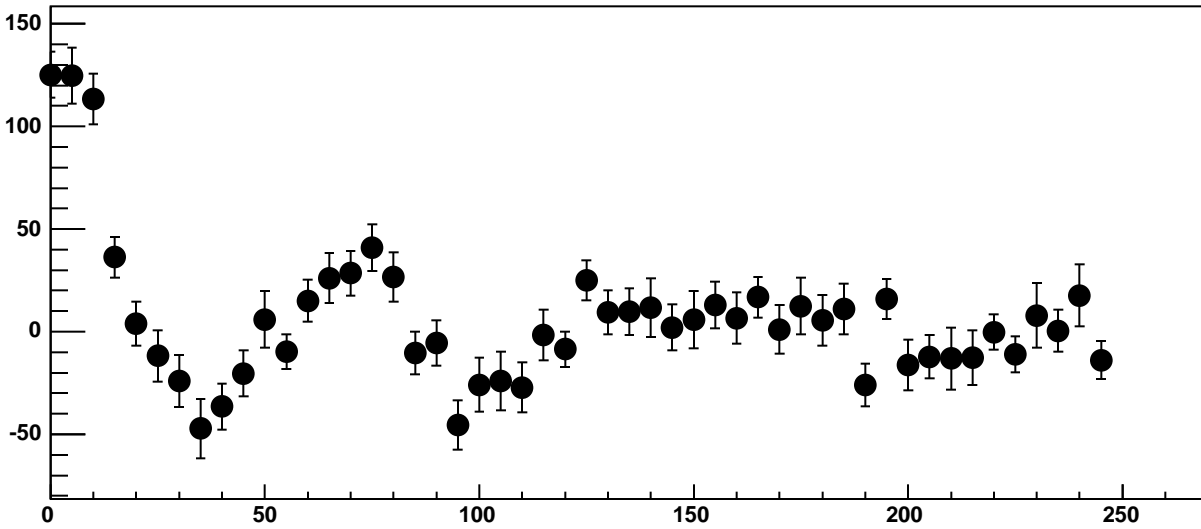


$\chi^2 / \text{ndf}$	136.8 / 41
p0	-964.9 ± 3.95
p1	96.06 ± 0.7439
p2	-6.424e+07 ± 5.287e+06
p3	6.975e+06 ± 5.666e+05
p4	8.249 ± 0.1108

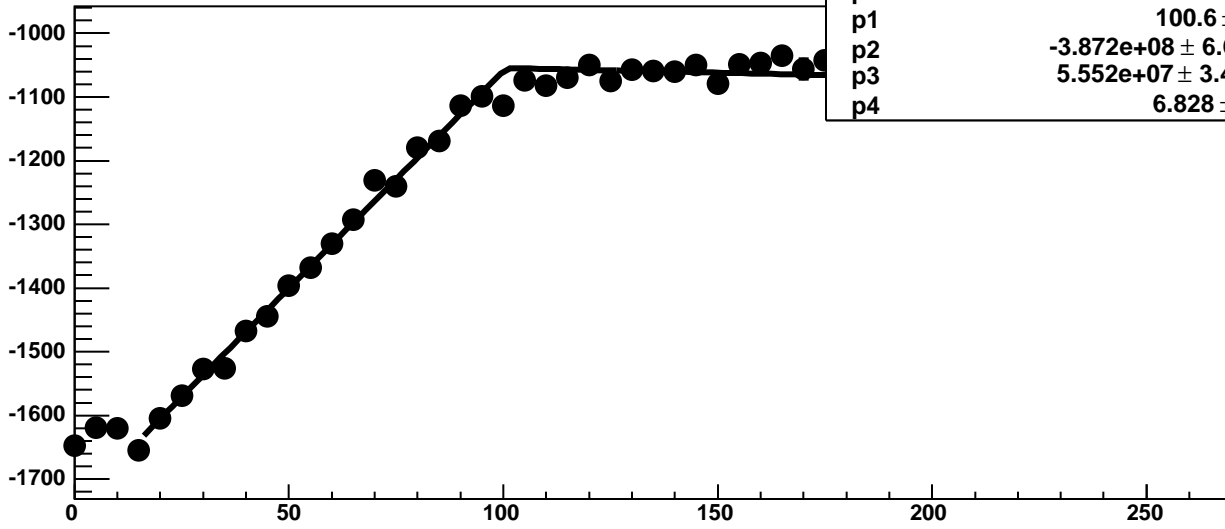
Chip 9, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold

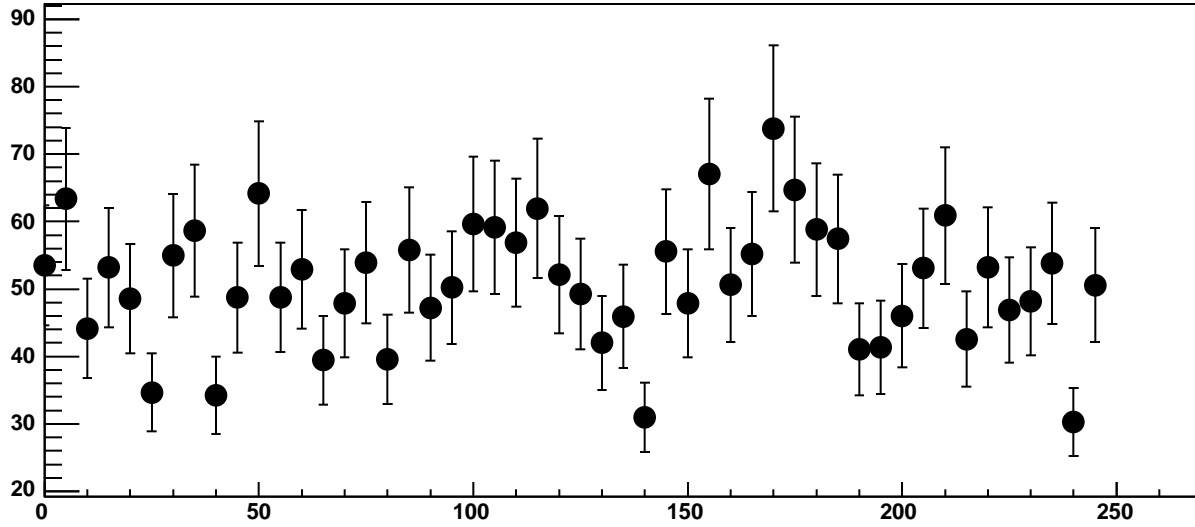


Chip 9, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

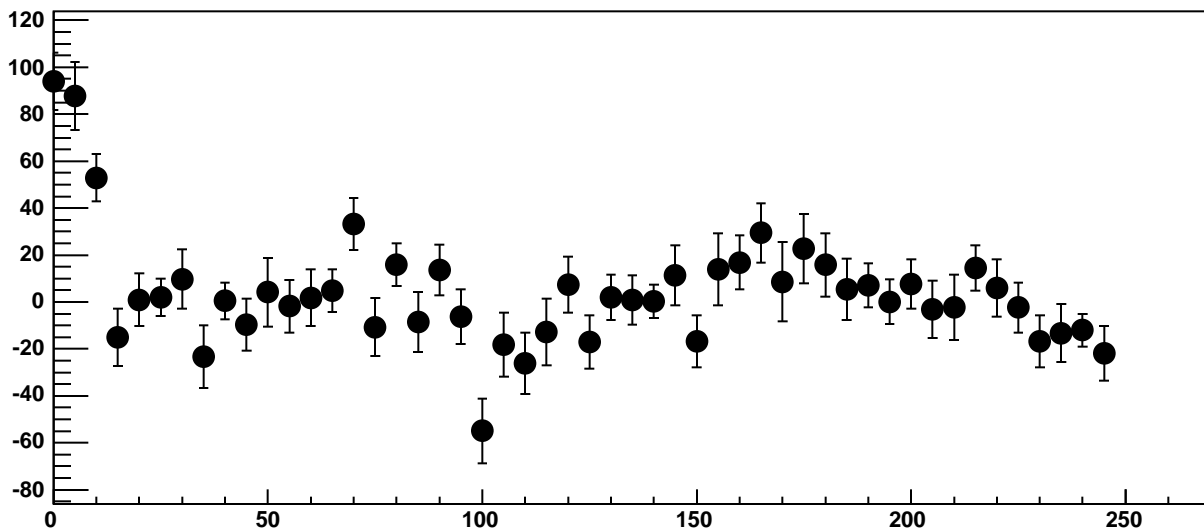


$\chi^2 / \text{ndf}$	72.87 / 41
p0	-1055 ± 4.272
p1	100.6 ± 0.9668
p2	-3.872e+08 ± 6.616e+06
p3	5.552e+07 ± 3.425e+05
p4	6.828 ± 0.1006

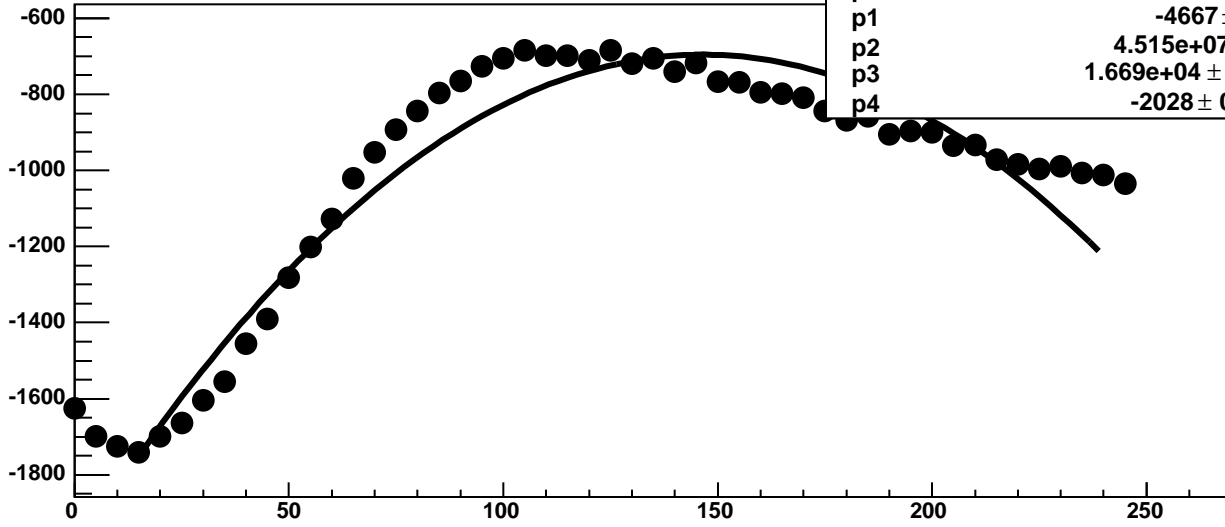
Chip 9, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

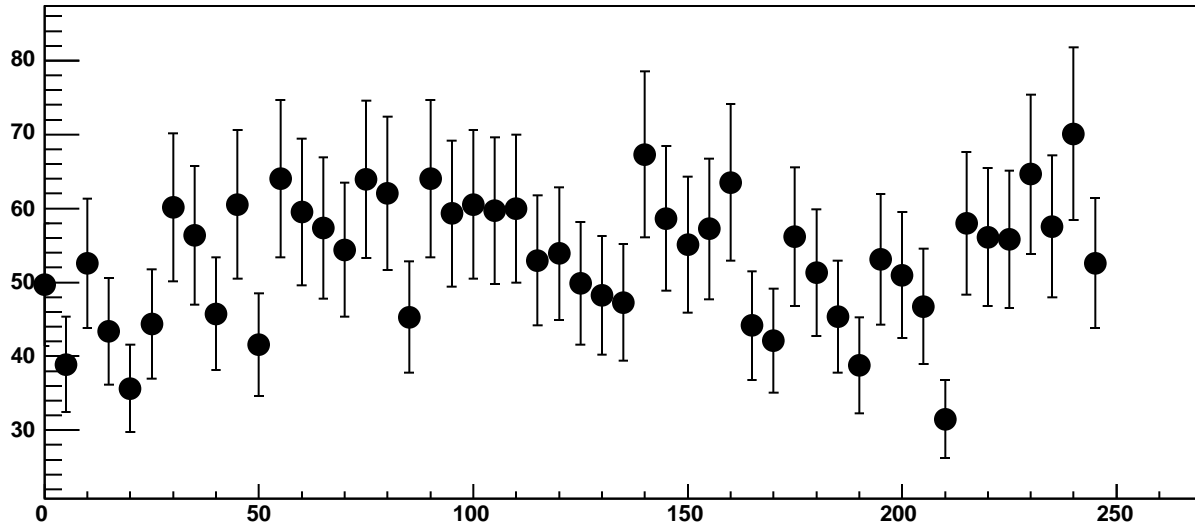


Chip 9, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

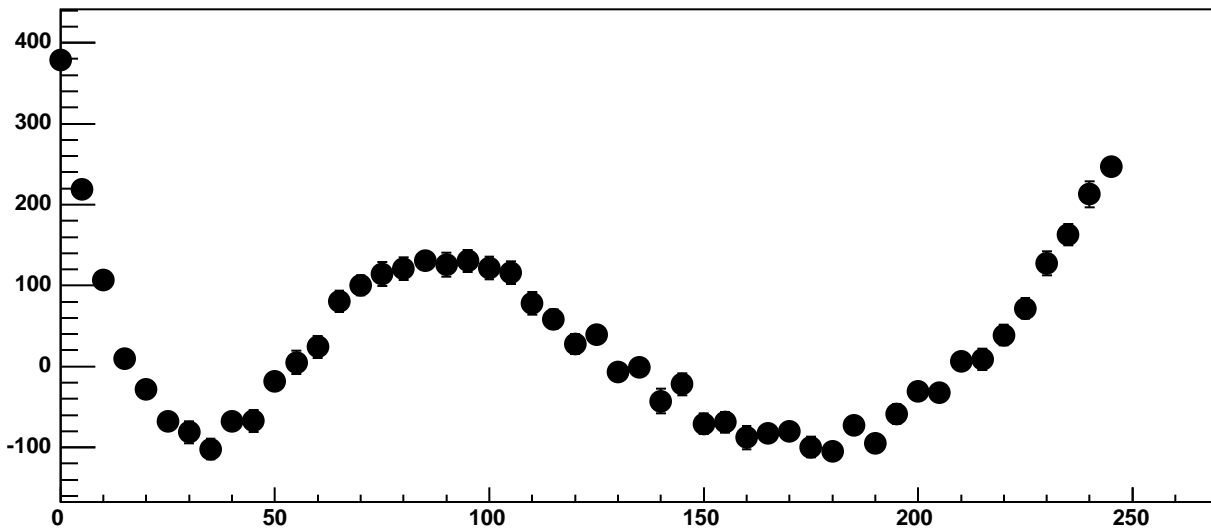


$\chi^2 / \text{ndf}$	2032 / 41
p0	$-1.554\text{e}+06 \pm 23.53$
p1	$-4667 \pm 0.2102$
p2	$4.515\text{e}+07 \pm 94.14$
p3	$1.669\text{e}+04 \pm 0.04032$
p4	$-2028 \pm 0.004901$

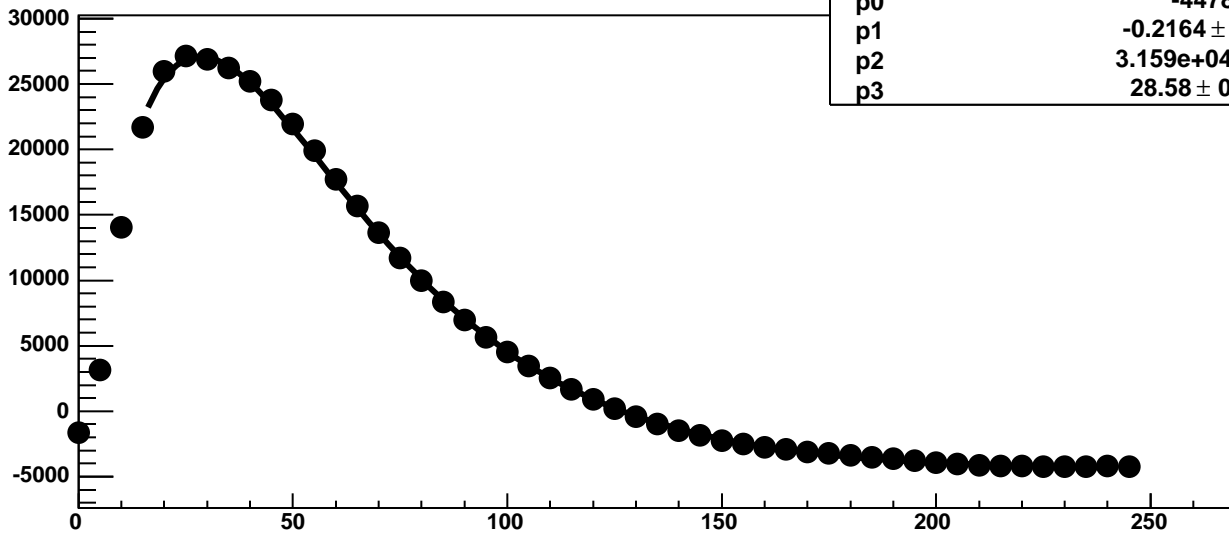
Chip 9, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

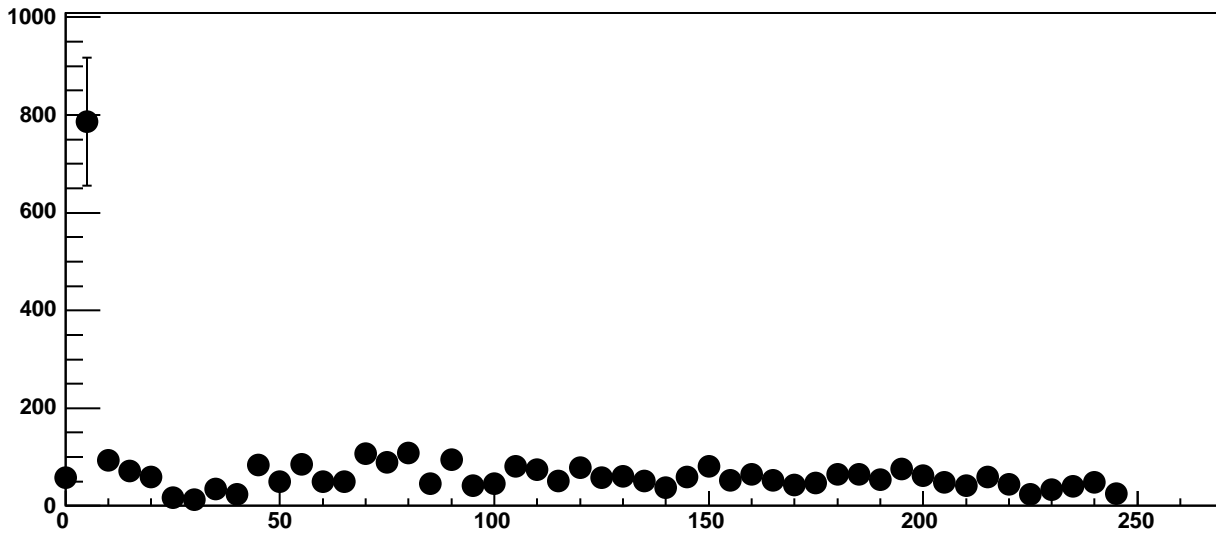


Chip 9, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

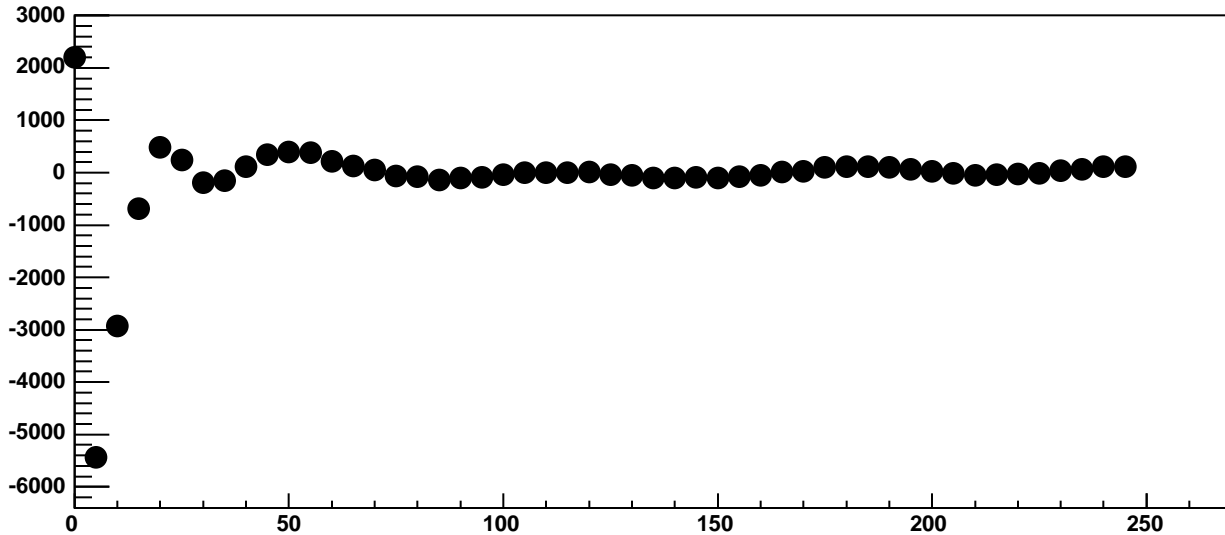


$\chi^2 / \text{ndf}$	1.52e+04 / 42
p0	-4478 ± 2.848
p1	-0.2164 ± 0.01642
p2	3.159e+04 ± 3.373
p3	28.58 ± 0.009268

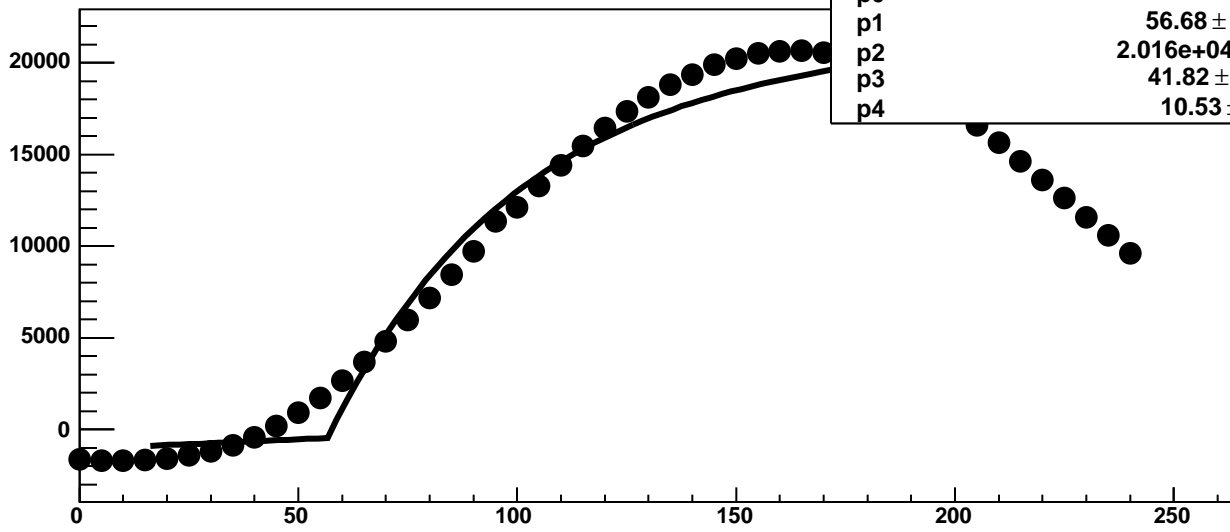
Chip 9, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



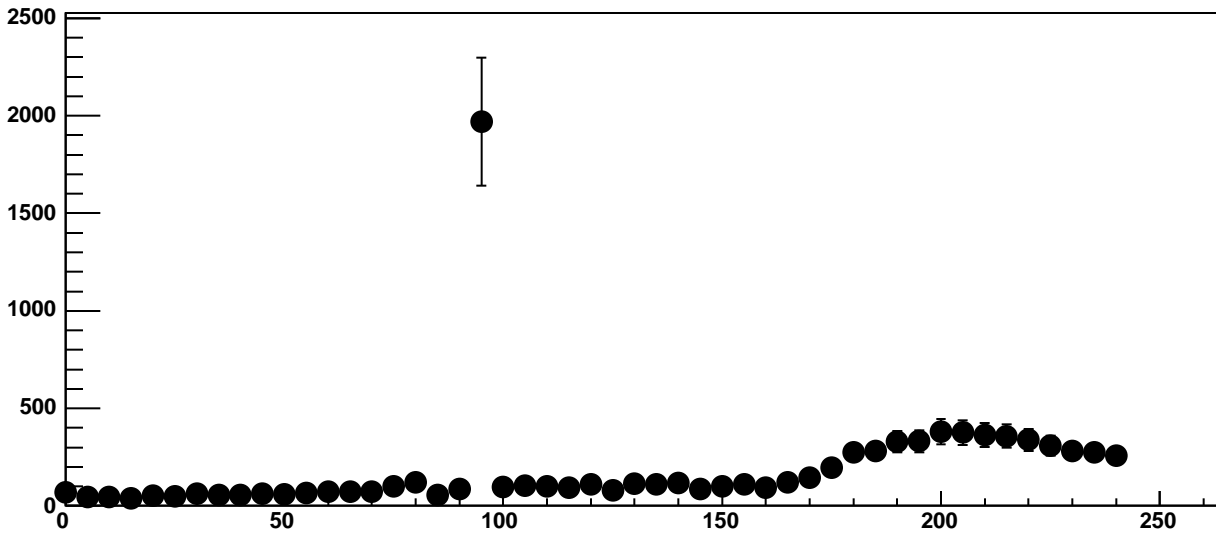
Chip 9, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold



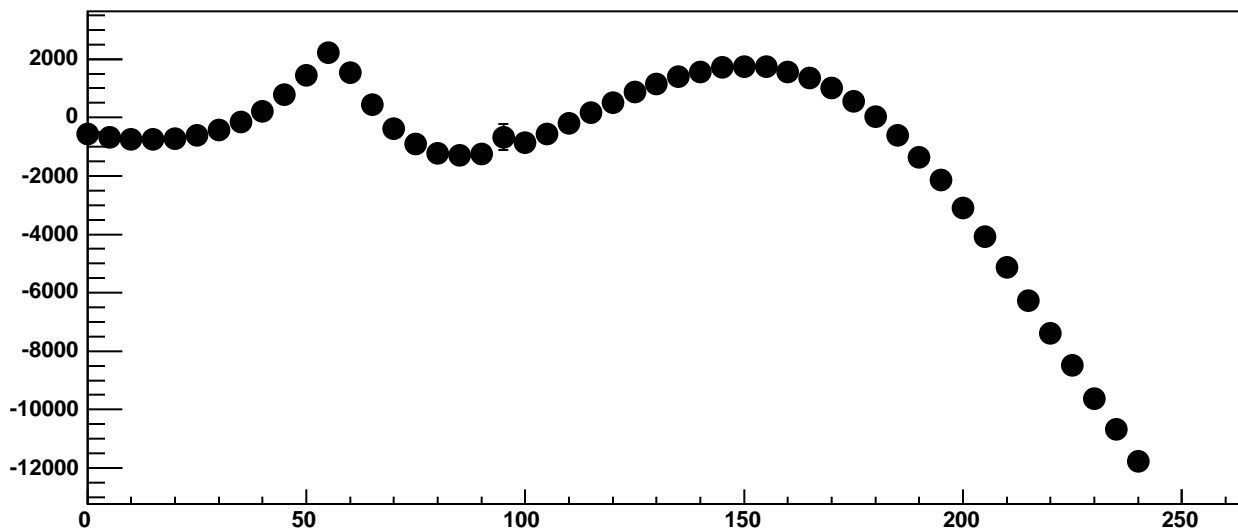
Chip 9, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold



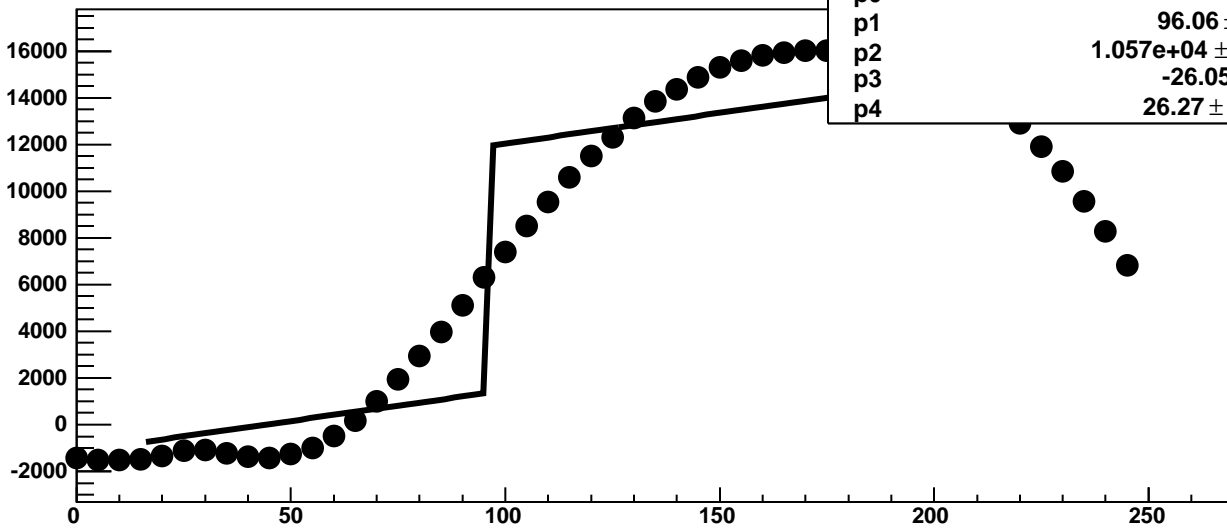
Chip 9, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



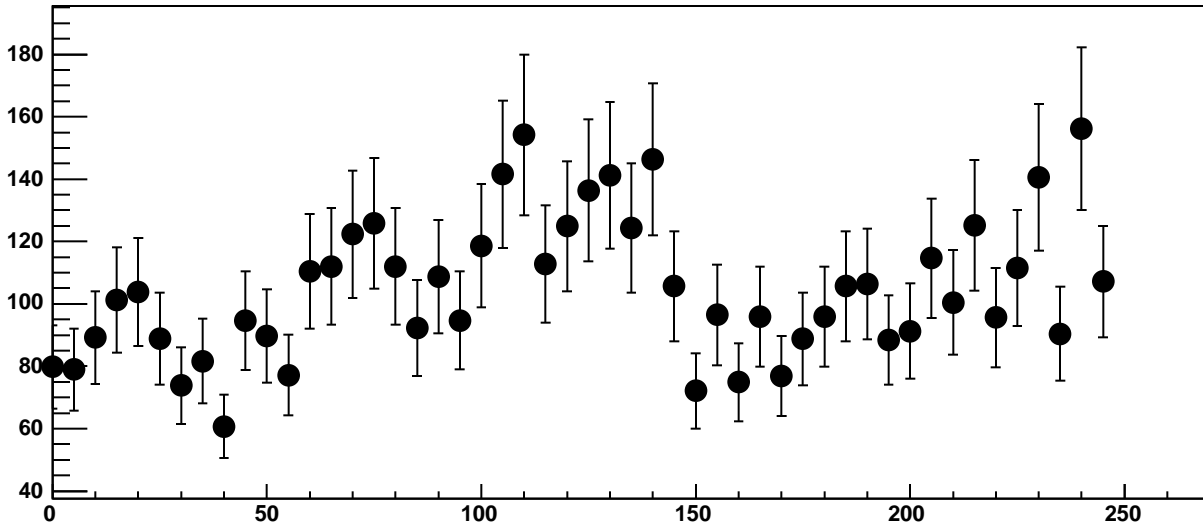
Chip 9, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold



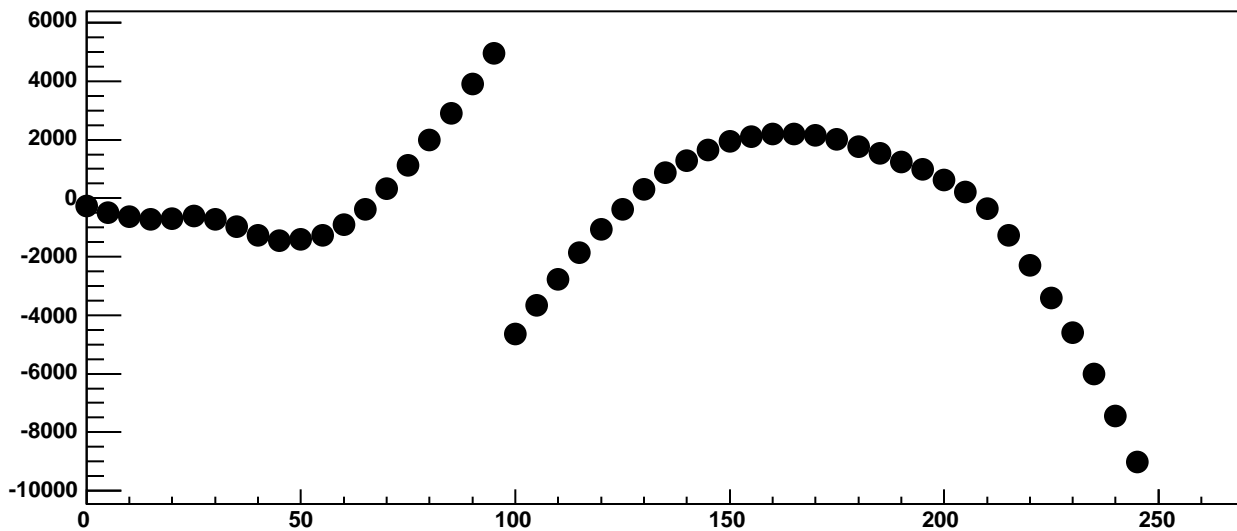
Chip 9, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold



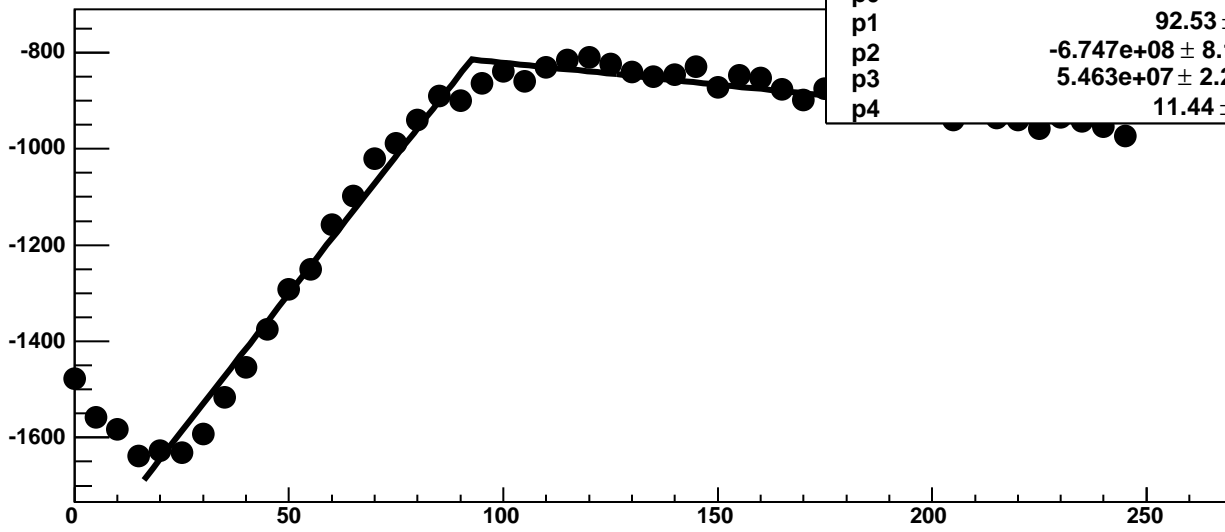
Chip 9, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold

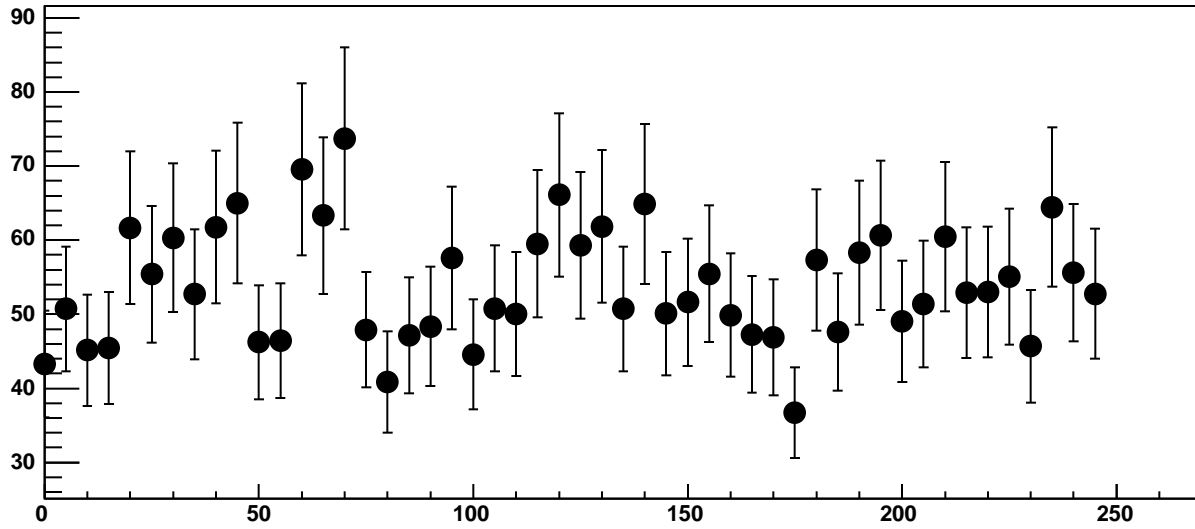


Chip 9, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold

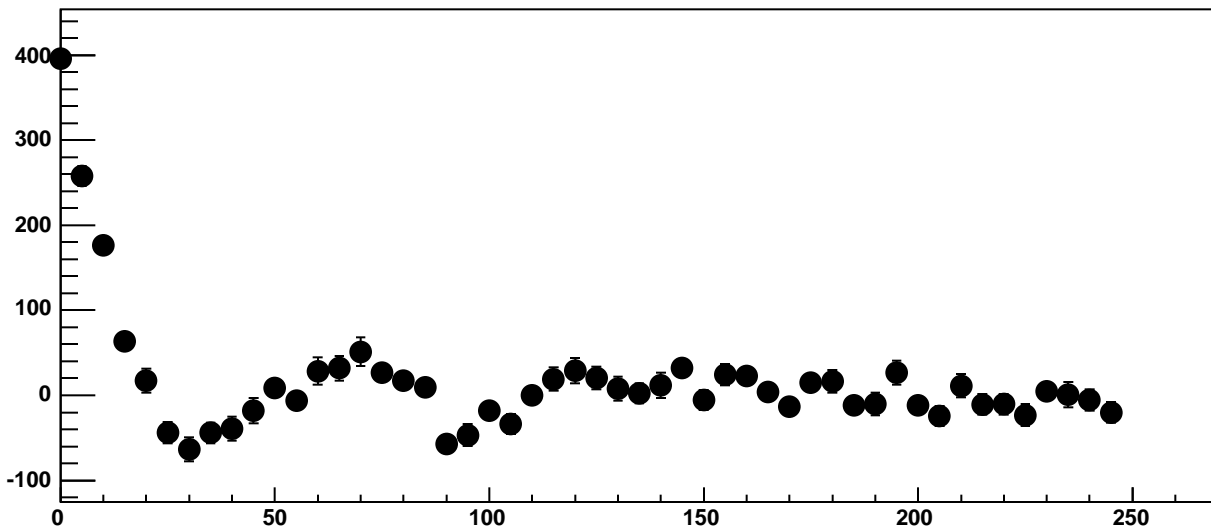


$\chi^2 / \text{ndf}$	220.2 / 41
p0	-814.2 ± 4.186
p1	92.53 ± 0.5828
p2	-6.747e+08 ± 8.144e+06
p3	5.463e+07 ± 2.201e+05
p4	11.44 ± 0.1254

Chip 9, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

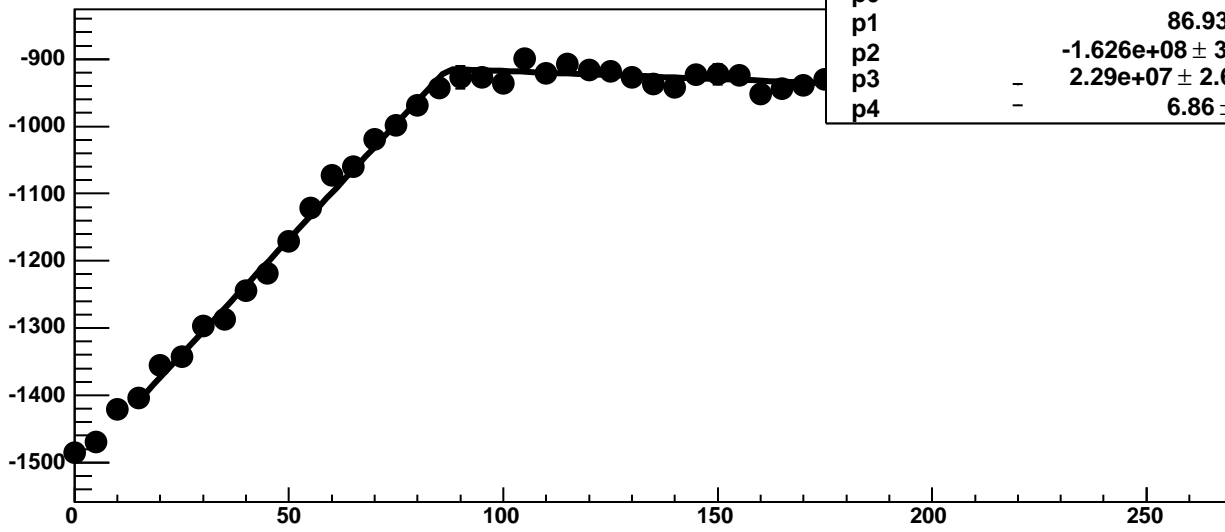


Chip 9, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



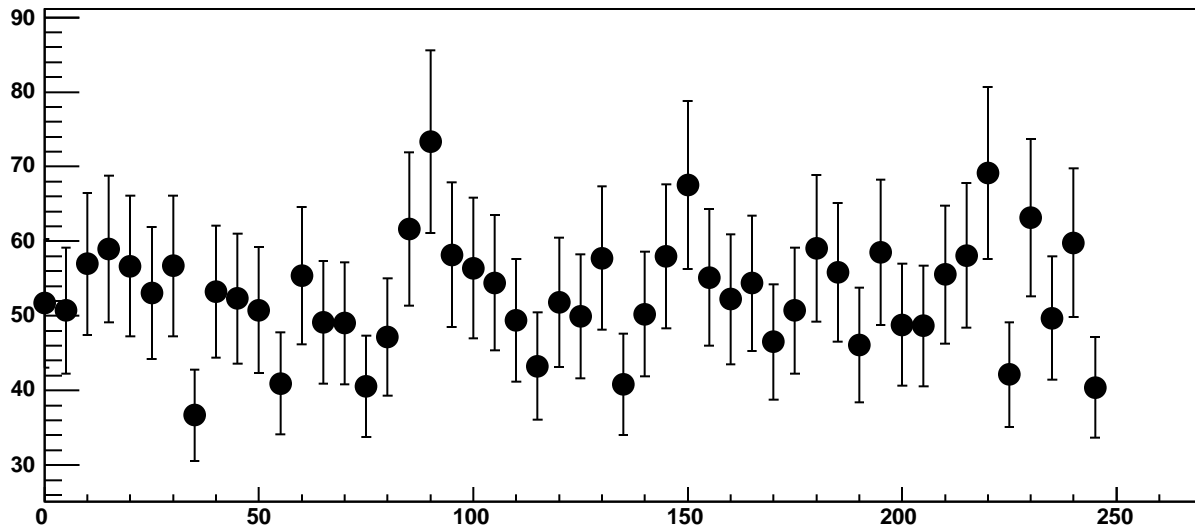


Chip 9, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold

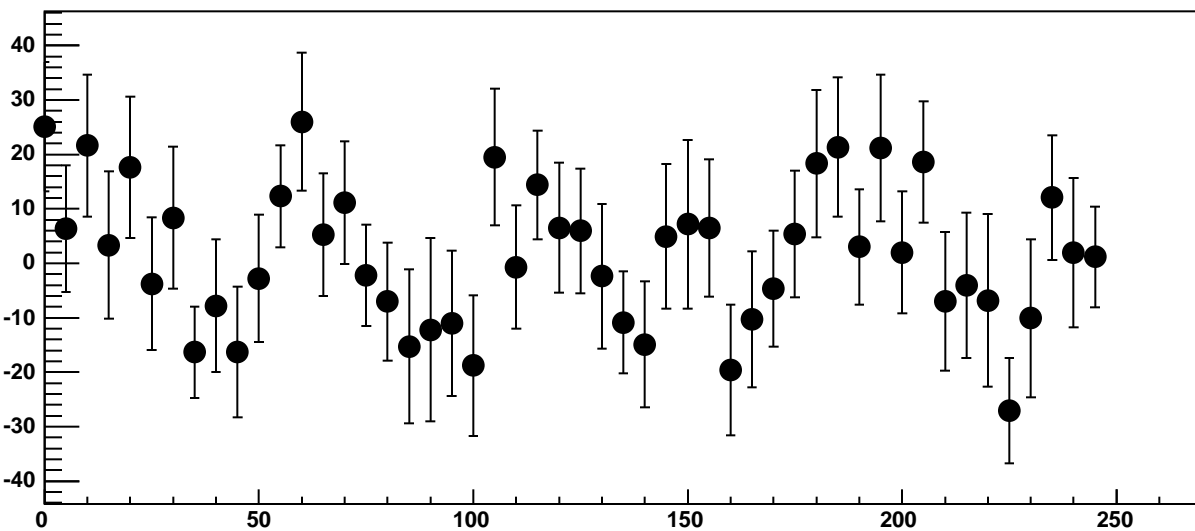


$\chi^2 / \text{ndf}$	53.09 / 41
p0	-914.4 ± 4.316
p1	86.93 ± 1.038
p2	-1.626e+08 ± 3.83e+06
p3	2.29e+07 ± 2.608e+05
p4	6.86 ± 0.1424

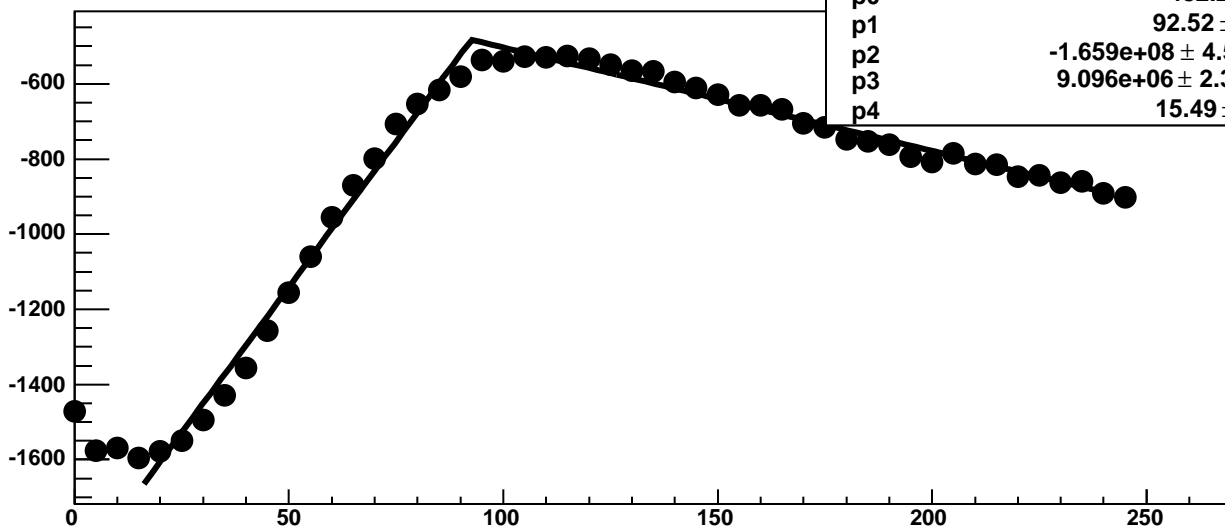
Chip 9, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold

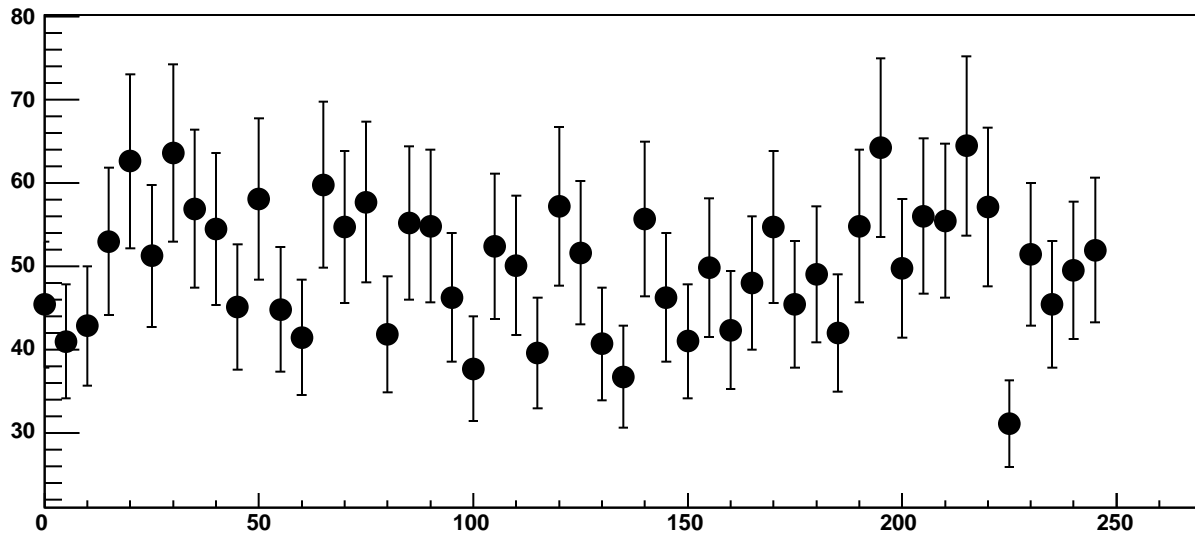


Chip 9, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

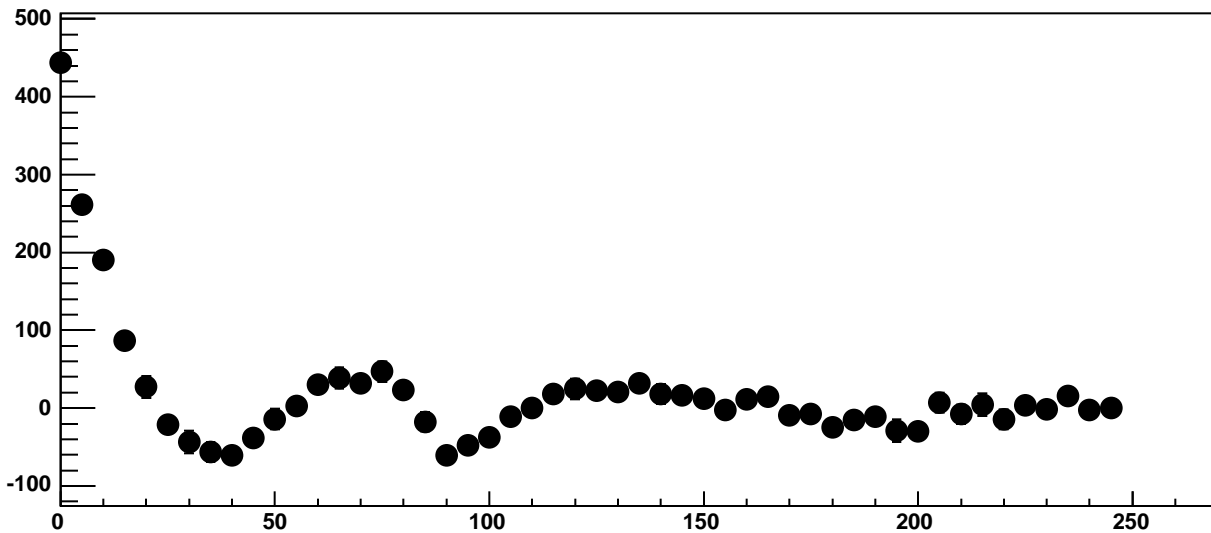


$\chi^2 / \text{ndf}$	295.4 / 41
p0	-482.2 ± 3.373
p1	92.52 ± 0.3874
p2	-1.659e+08 ± 4.555e+06
p3	9.096e+06 ± 2.319e+05
p4	15.49 ± 0.1338

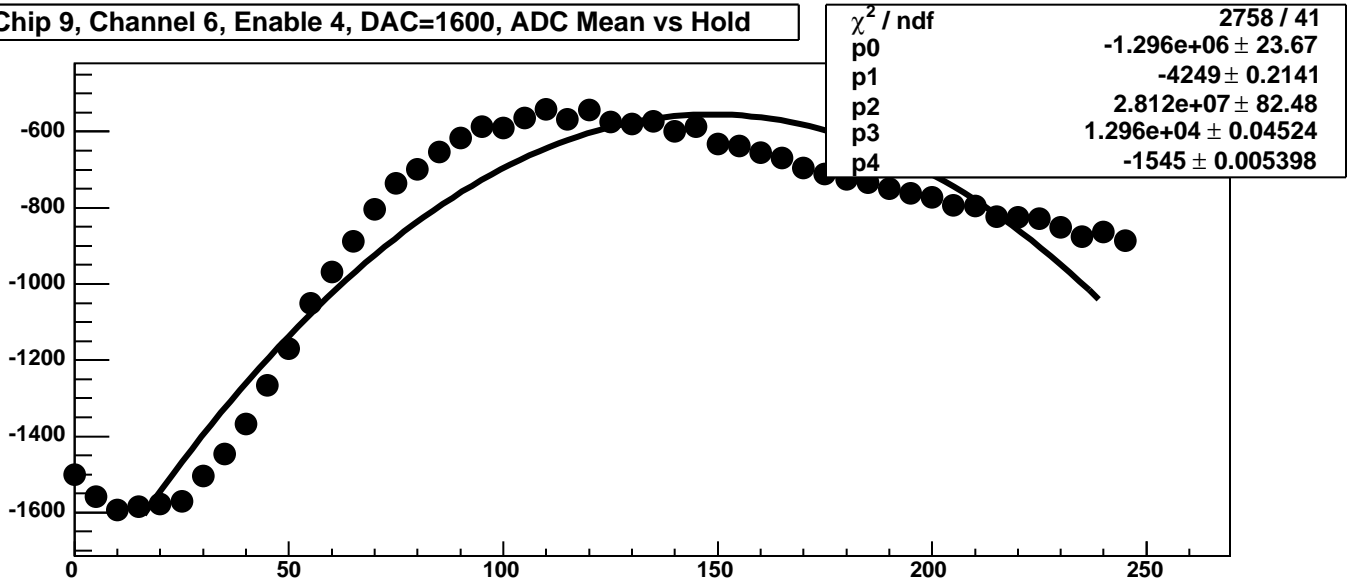
Chip 9, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



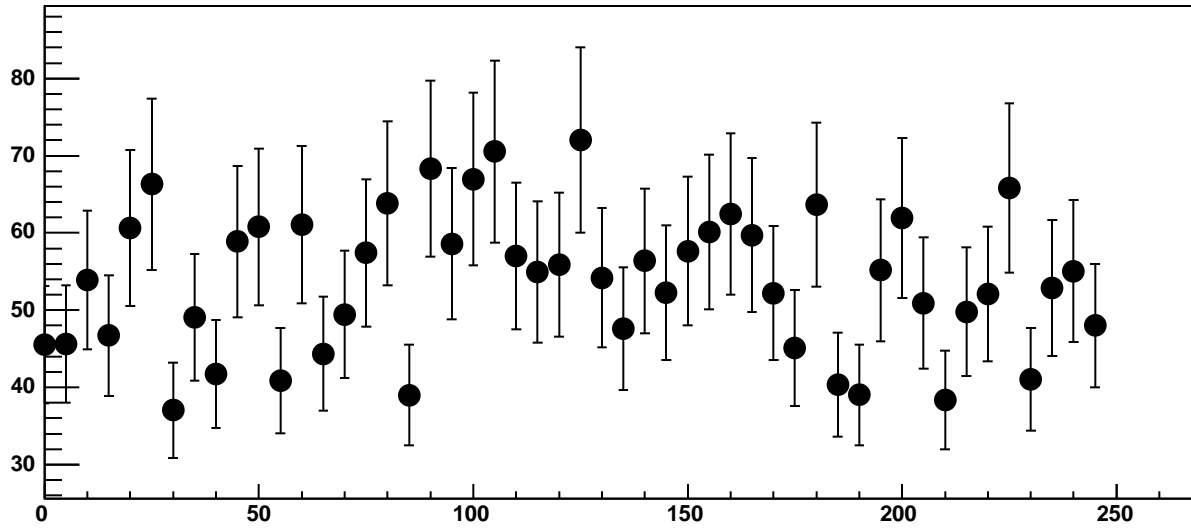
Chip 9, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold



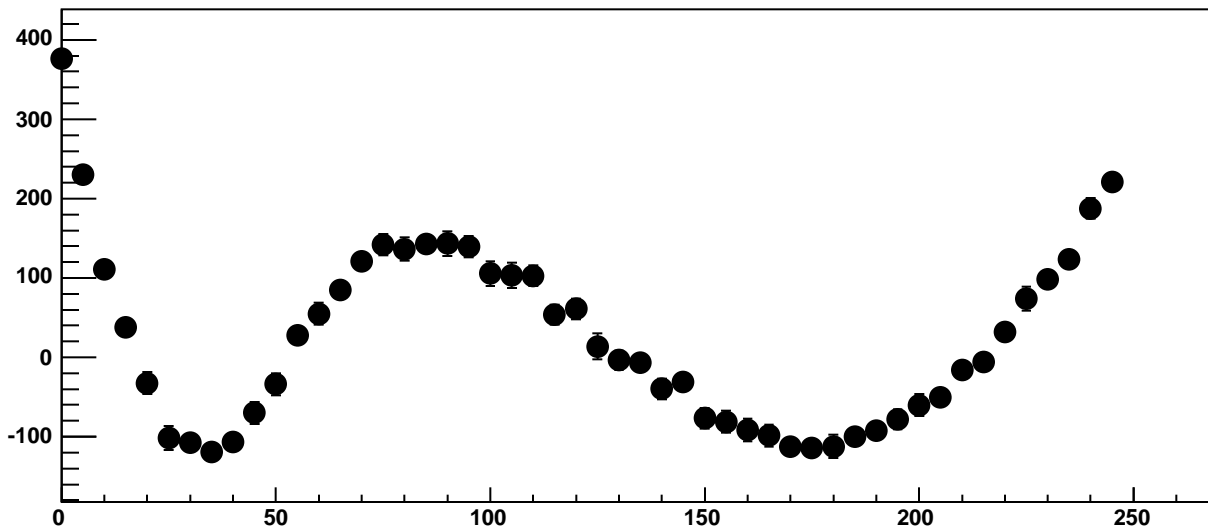
Chip 9, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold



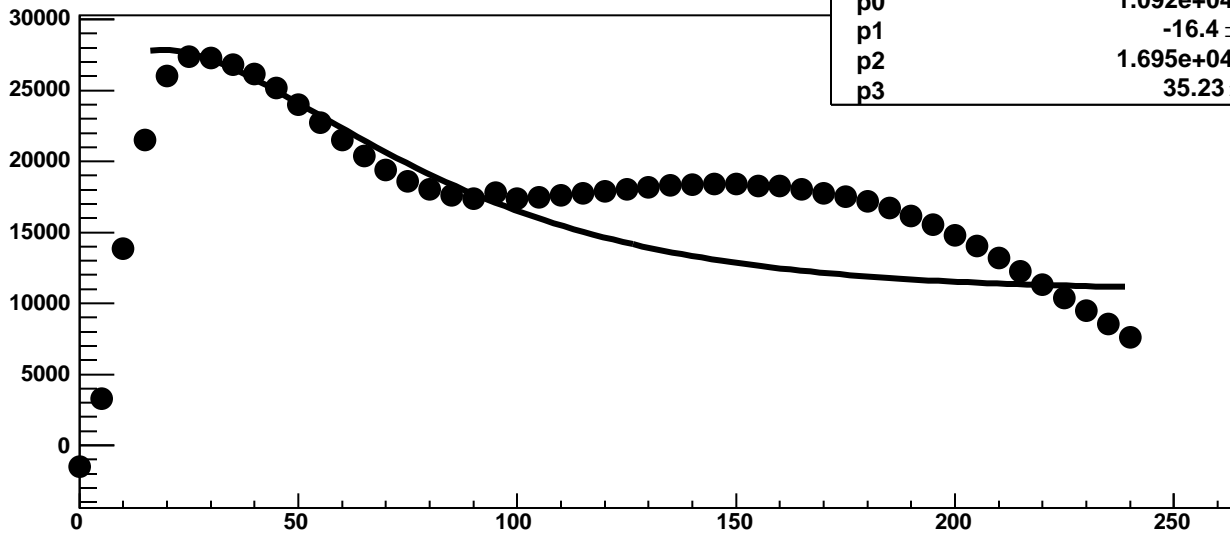
Chip 9, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

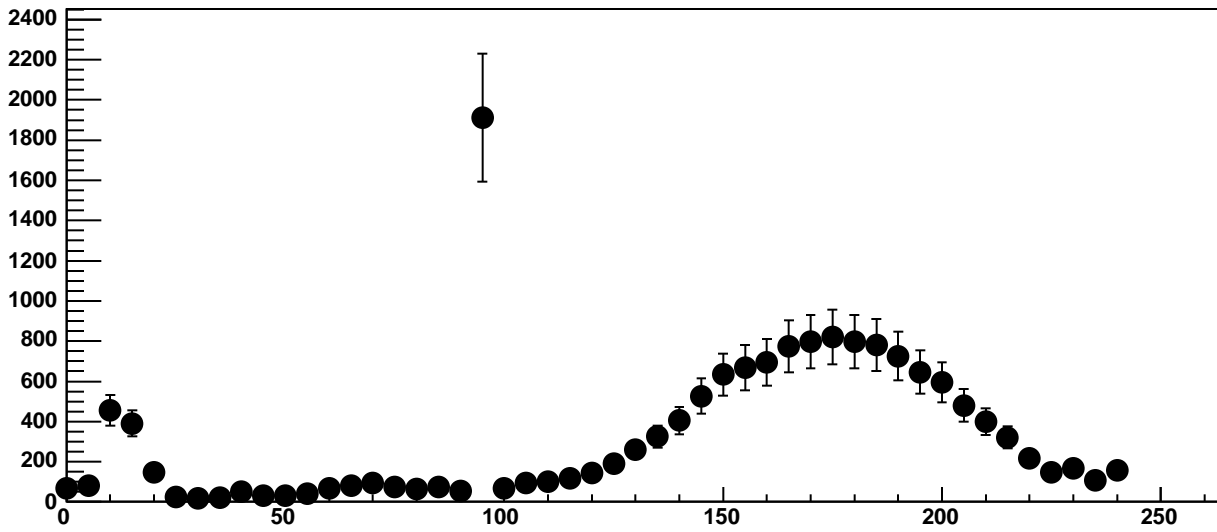


Chip 9, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

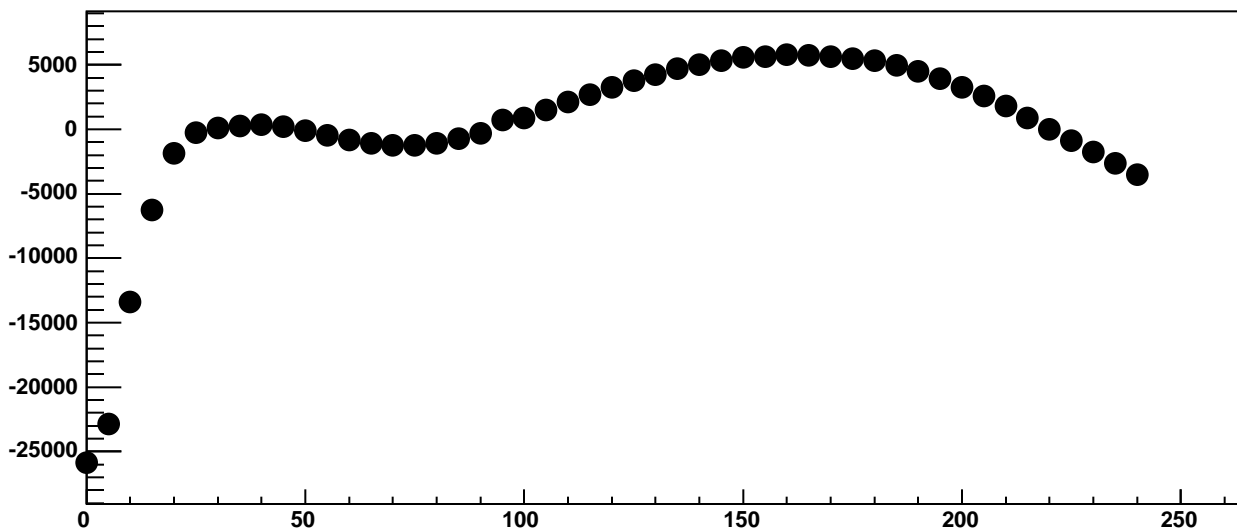


$\chi^2 / \text{ndf}$	1.341e+05 / 42
p0	1.092e+04 $\pm$ 20.34
p1	-16.4 $\pm$ 0.2236
p2	1.695e+04 $\pm$ 29.05
p3	35.23 $\pm$ 0.1021

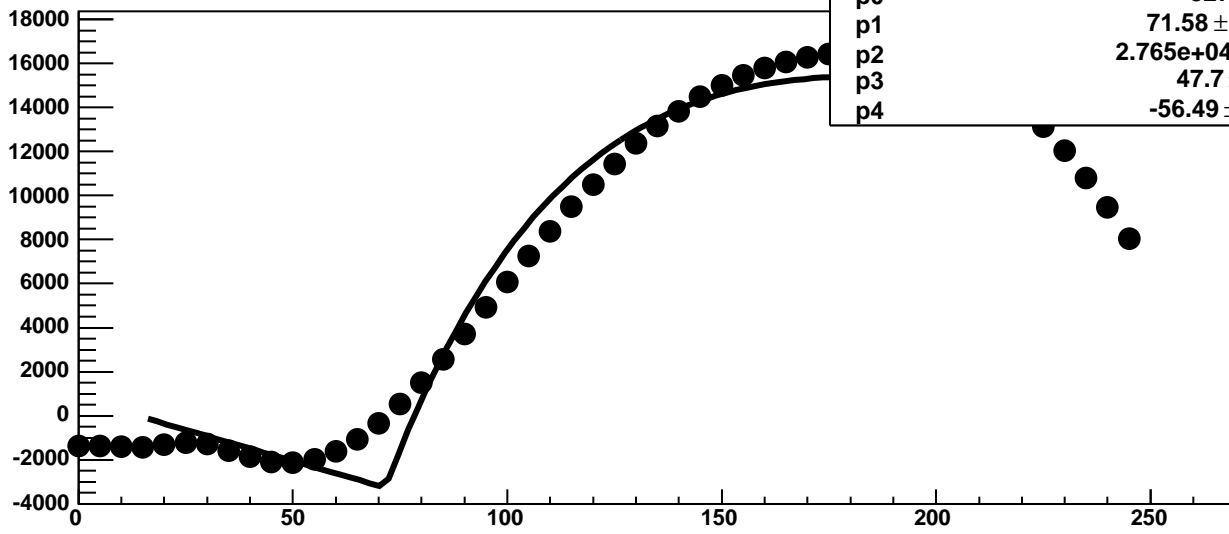
Chip 9, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold

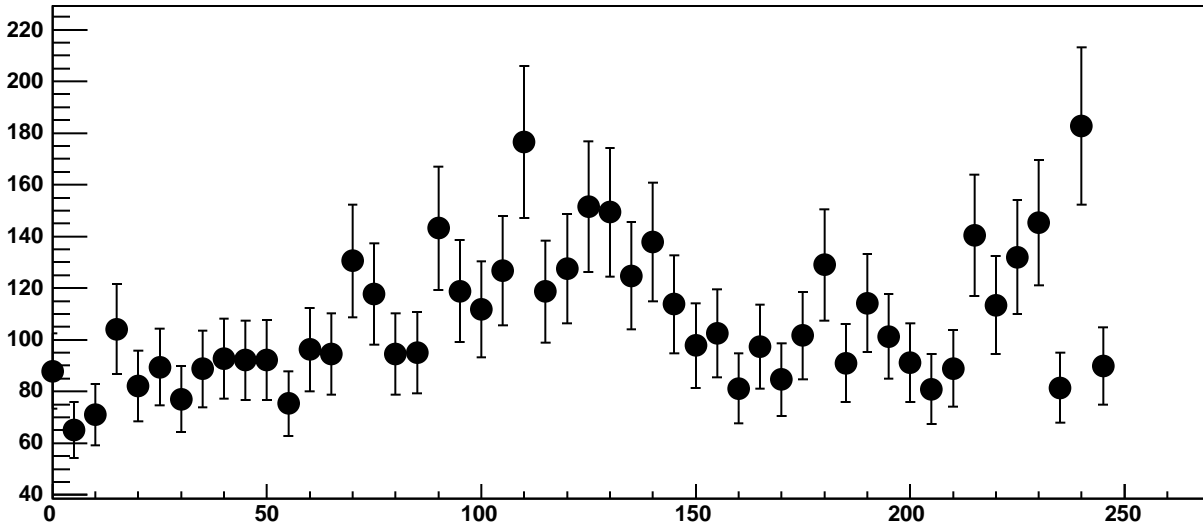


Chip 9, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold

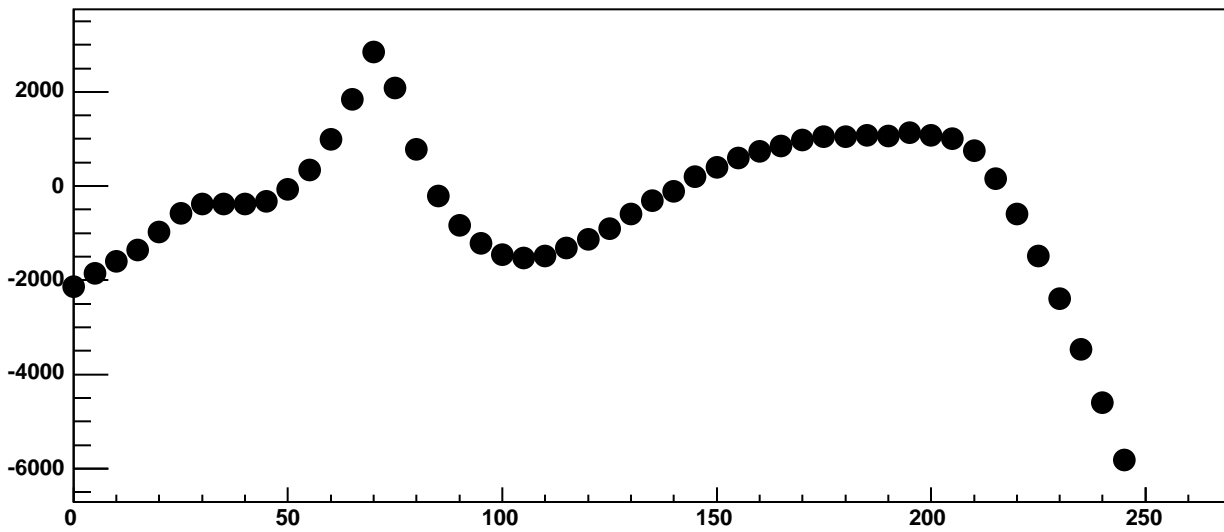


$\chi^2 / \text{ndf}$	1.27e+05 / 41
p0	-3270 ± 9.41
p1	71.58 ± 0.03691
p2	2.765e+04 ± 57.13
p3	47.7 ± 0.1119
p4	-56.49 ± 0.2766

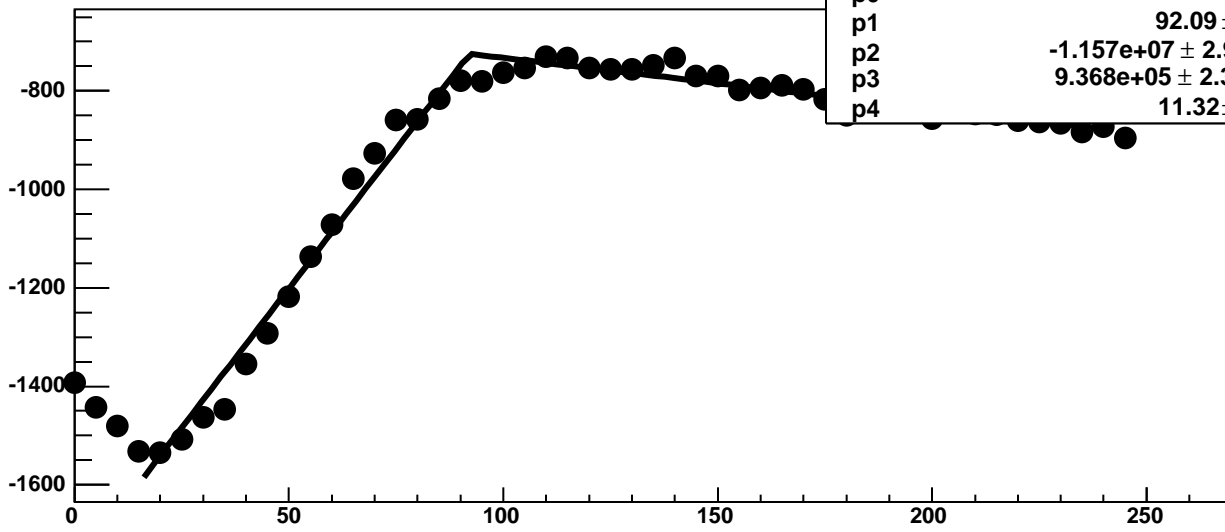
Chip 9, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

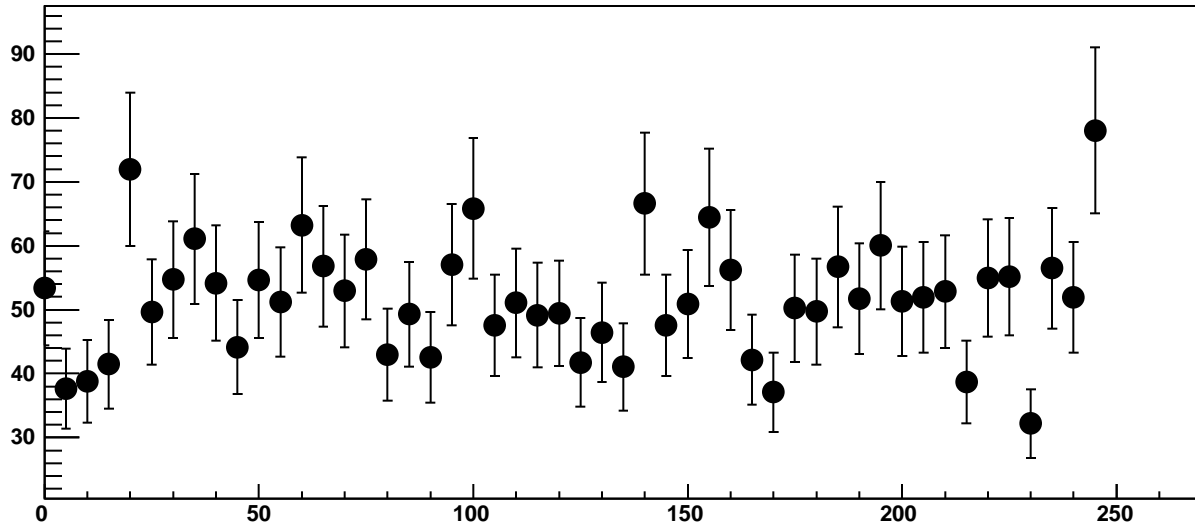


Chip 9, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

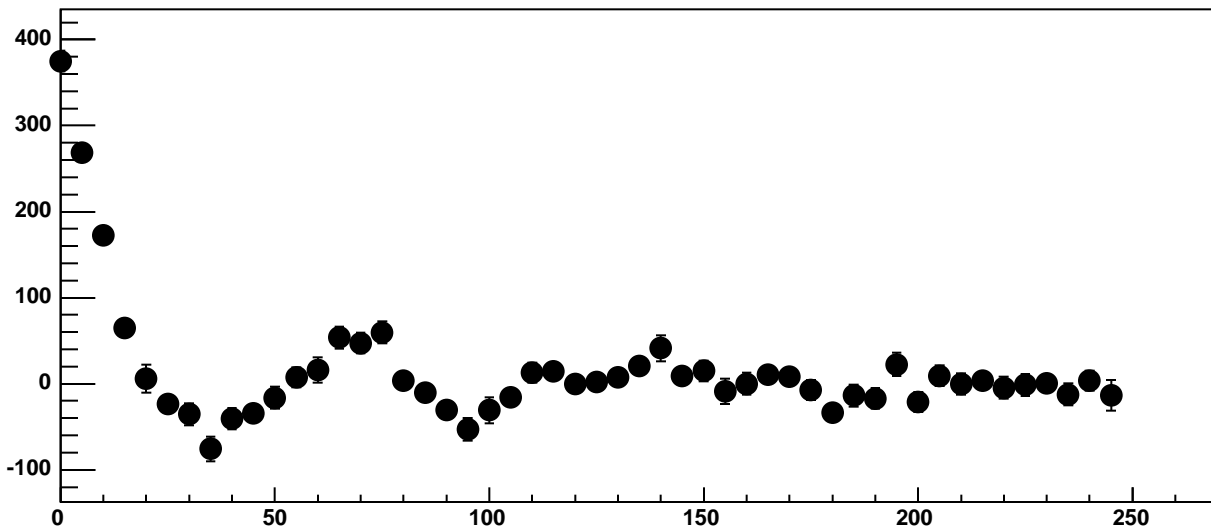


$\chi^2 / \text{ndf}$	241.3 / 41
p0	-724.7 ± 3.897
p1	92.09 ± 0.5597
p2	-1.157e+07 ± 2.913e+06
p3	9.368e+05 ± 2.359e+05
p4	11.32 ± 0.1208

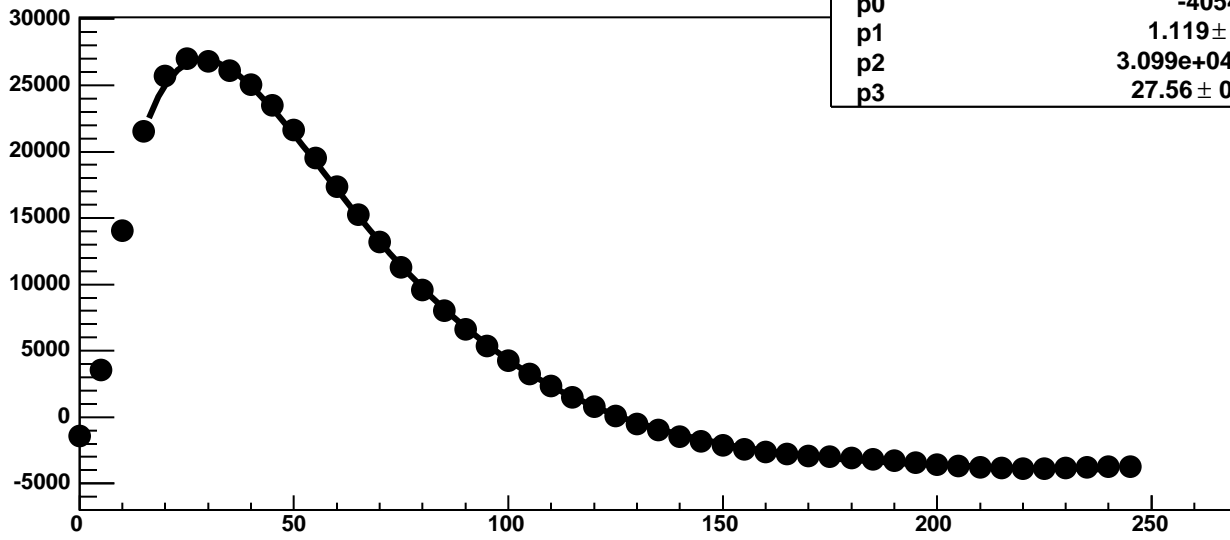
Chip 9, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

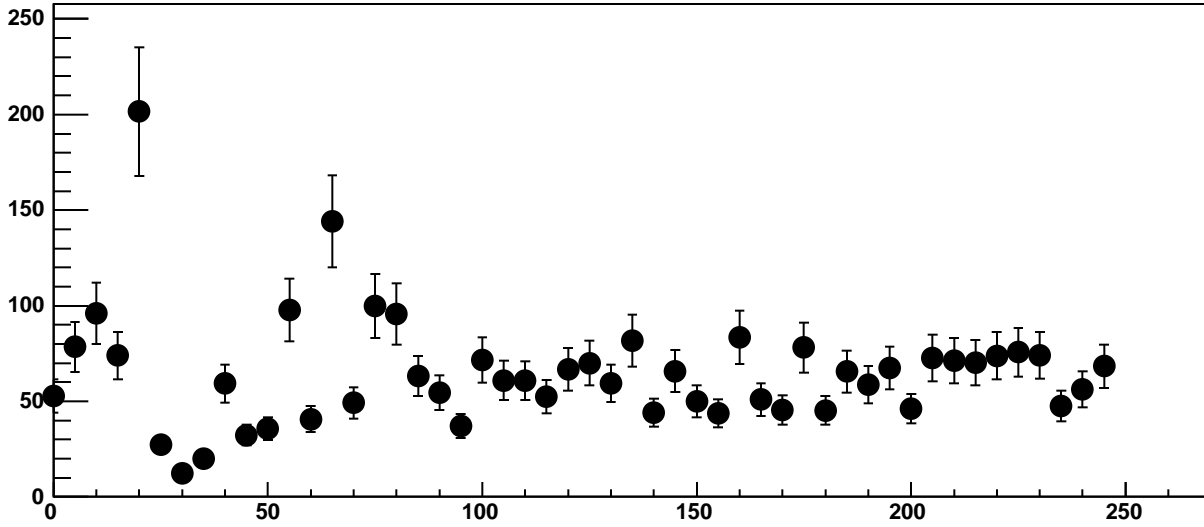


Chip 9, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold

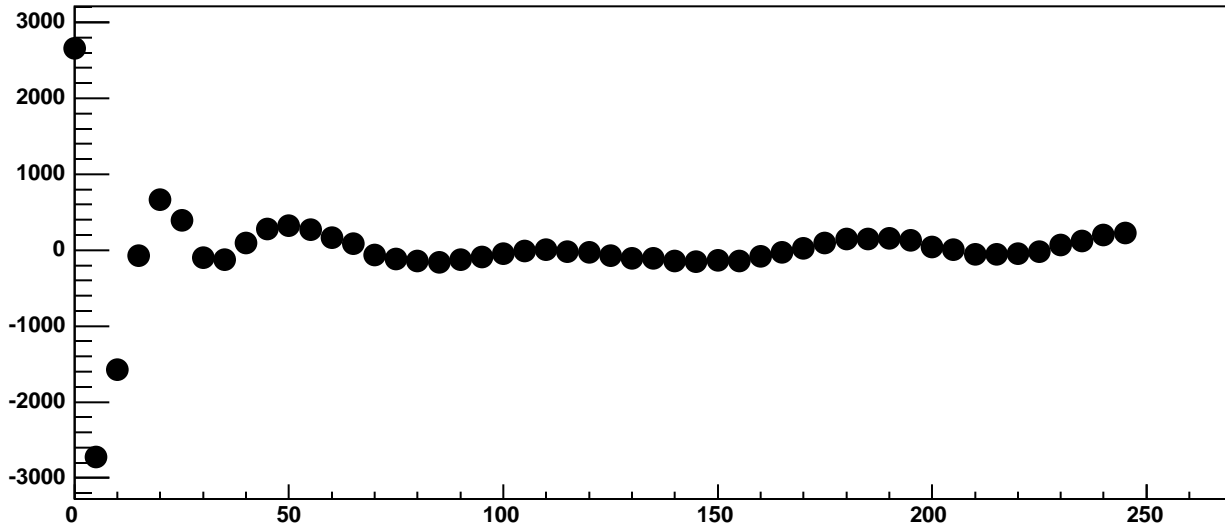


$\chi^2 / \text{ndf}$	1.19e+04 / 42
p0	-4054 ± 3.59
p1	1.119 ± 0.01733
p2	3.099e+04 ± 4.082
p3	27.56 ± 0.009696

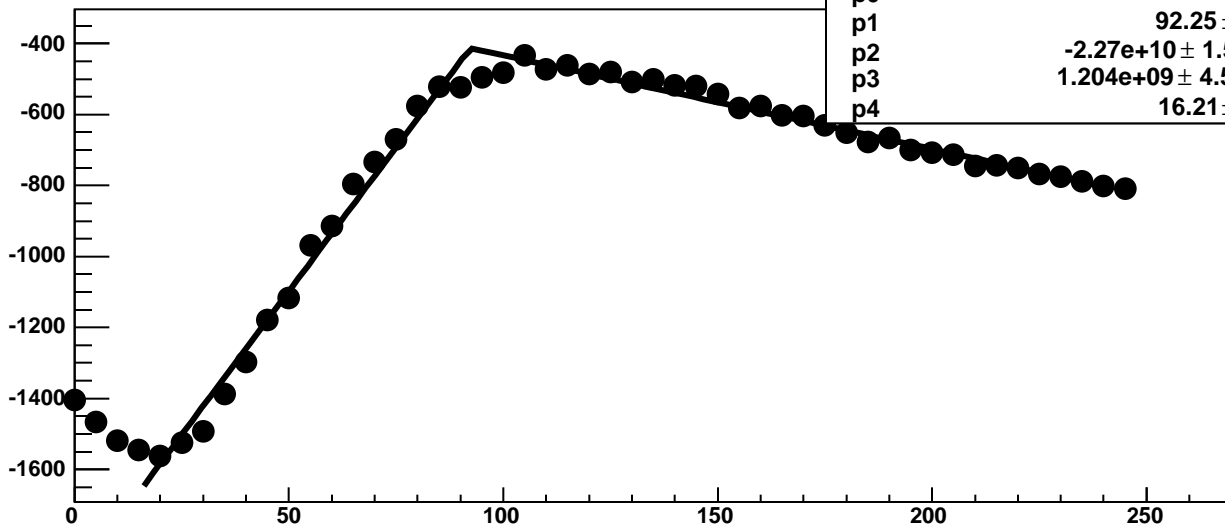
Chip 9, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold

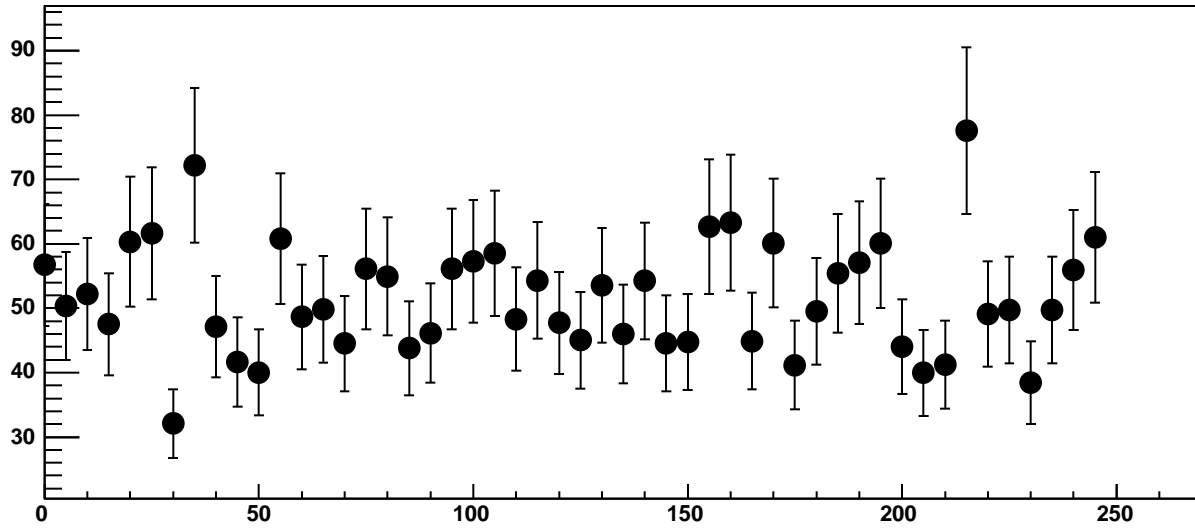


Chip 9, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

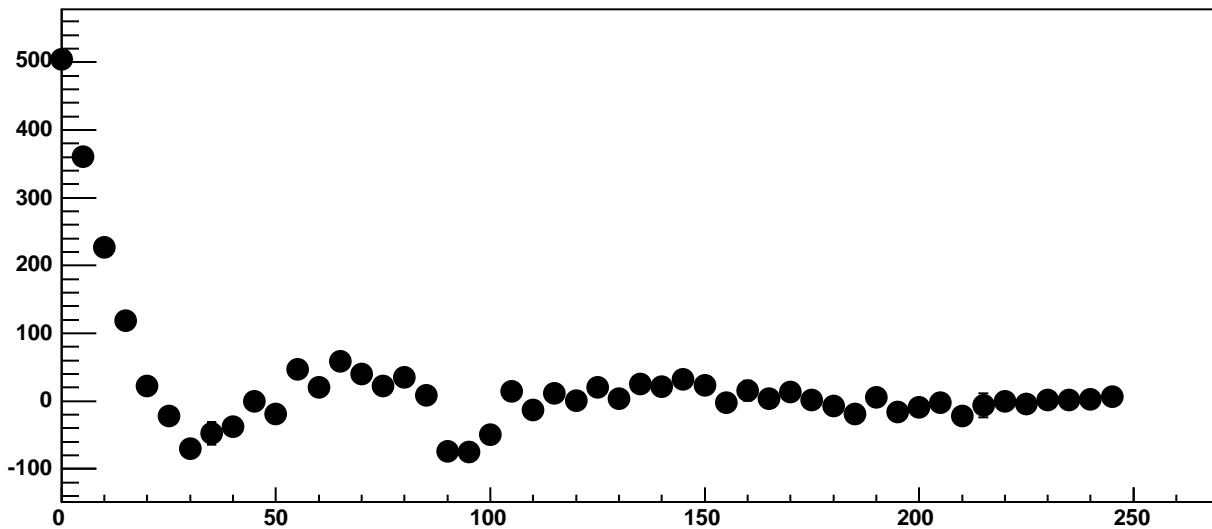


$\chi^2 / \text{ndf}$	449.7 / 41
p0	$-412.7 \pm 3.726$
p1	$92.25 \pm 0.3549$
p2	$-2.27\text{e}+10 \pm 1.552\text{e}+08$
p3	$1.204\text{e}+09 \pm 4.596\text{e}+05$
p4	$16.21 \pm 0.1184$

Chip 9, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

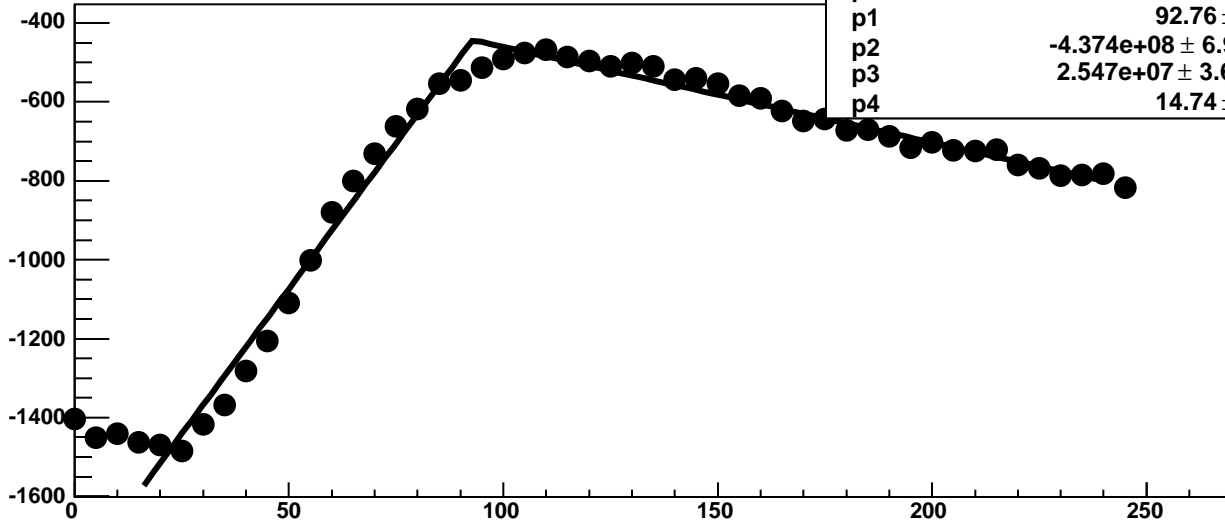


Chip 9, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold



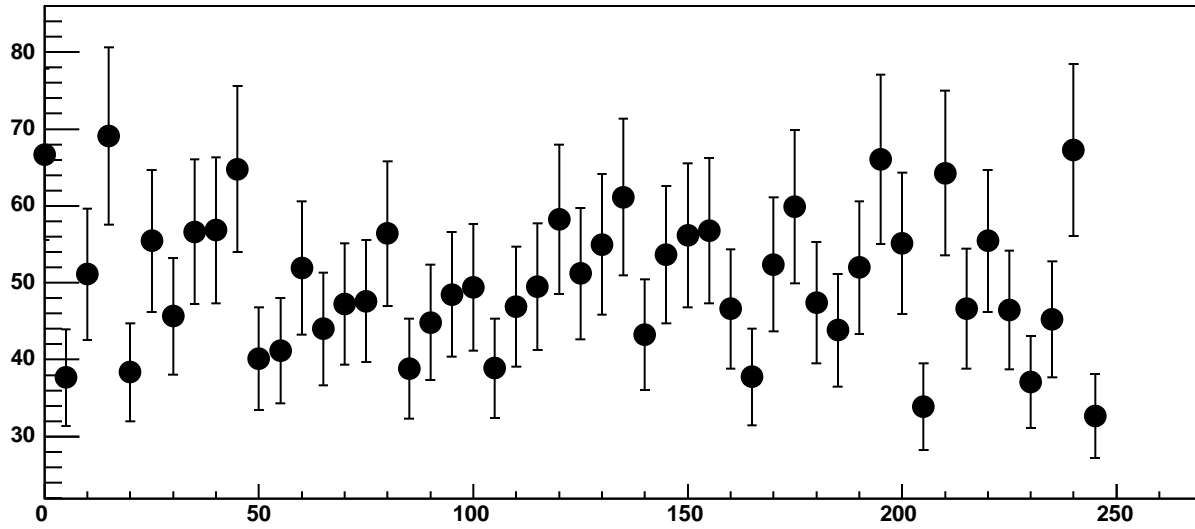


Chip 9, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold

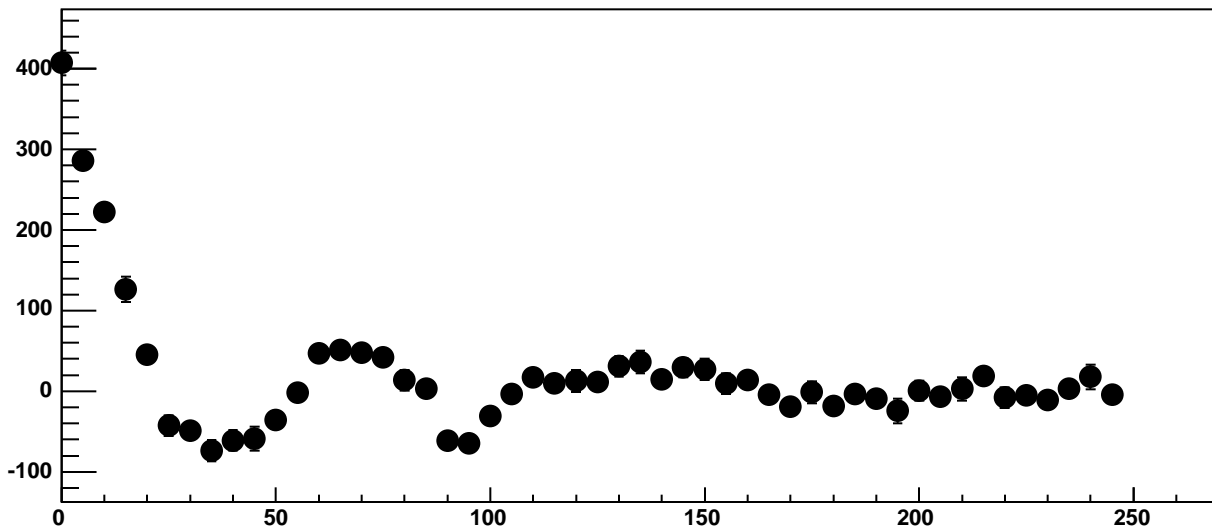


$\chi^2 / \text{ndf}$	409.1 / 41
p0	$-442.7 \pm 3.558$
p1	$92.76 \pm 0.3882$
p2	$-4.374\text{e}+08 \pm 6.994\text{e}+06$
p3	$2.547\text{e}+07 \pm 3.644\text{e}+05$
p4	$14.74 \pm 0.1187$

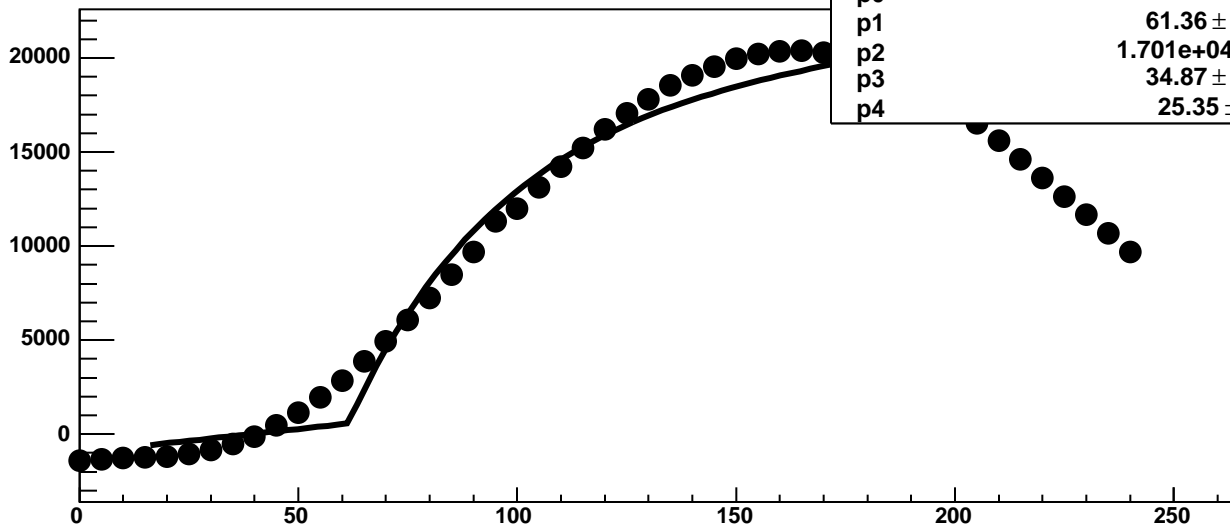
Chip 9, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

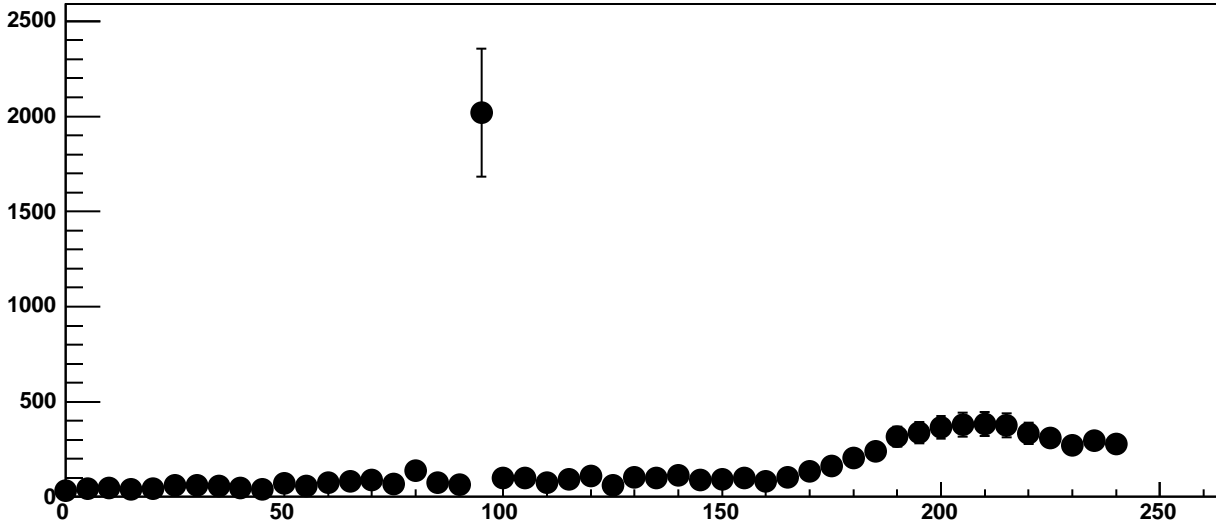


Chip 9, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold

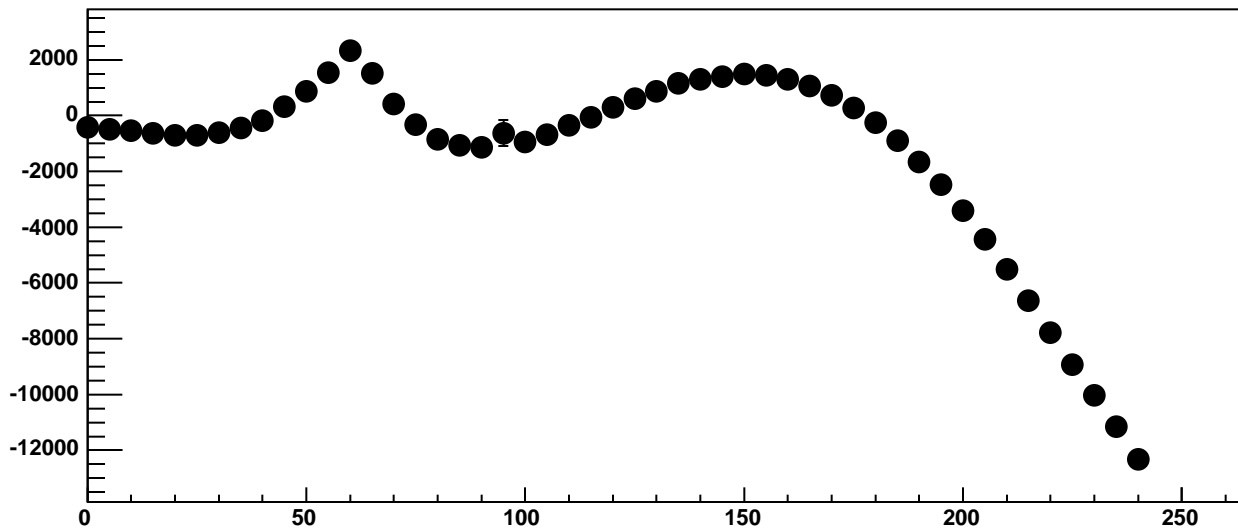


$\chi^2 / \text{ndf}$	2.332e+05 / 41
p0	564.5 ± 7.225
p1	61.36 ± 0.03528
p2	1.701e+04 ± 33.54
p3	34.87 ± 0.08752
p4	25.35 ± 0.2124

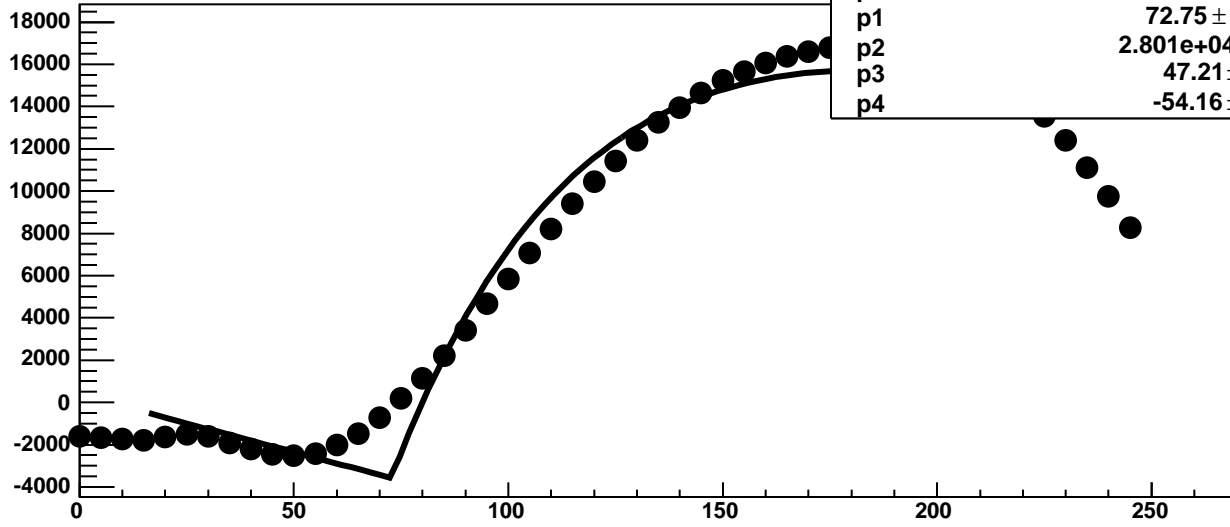
Chip 9, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold

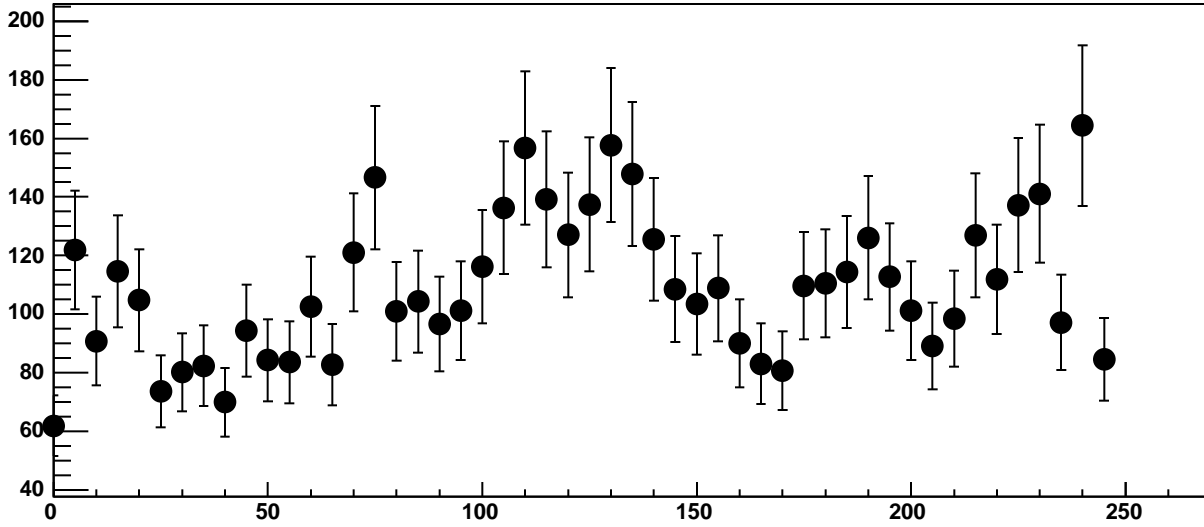


Chip 9, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold

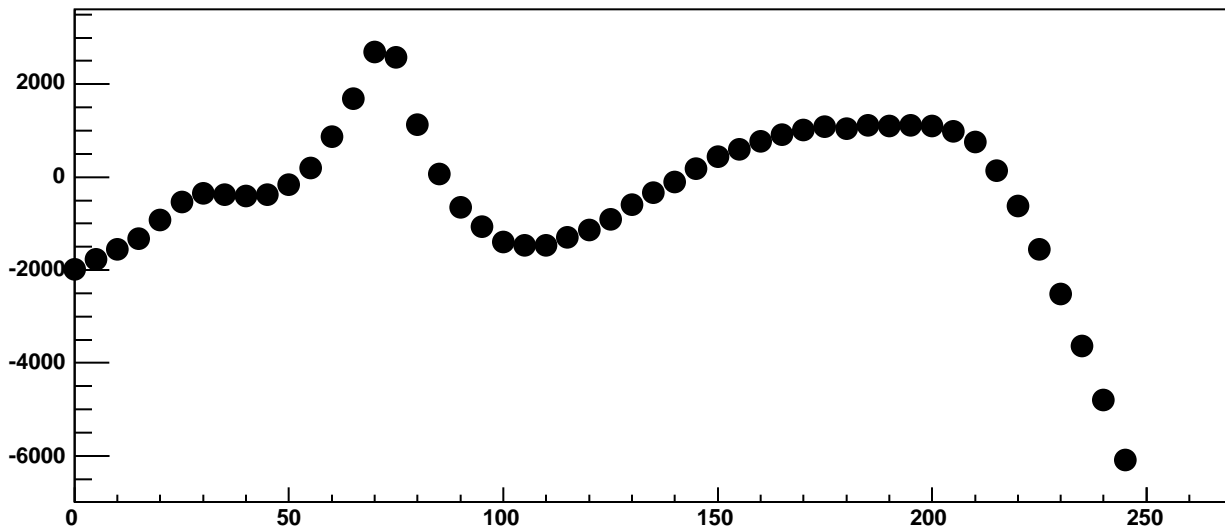


$\chi^2 / \text{ndf}$	1.218e+05 / 41
p0	-3577 ± 9.562
p1	72.75 ± 0.03669
p2	2.801e+04 ± 57.71
p3	47.21 ± 0.1102
p4	-54.16 ± 0.2823

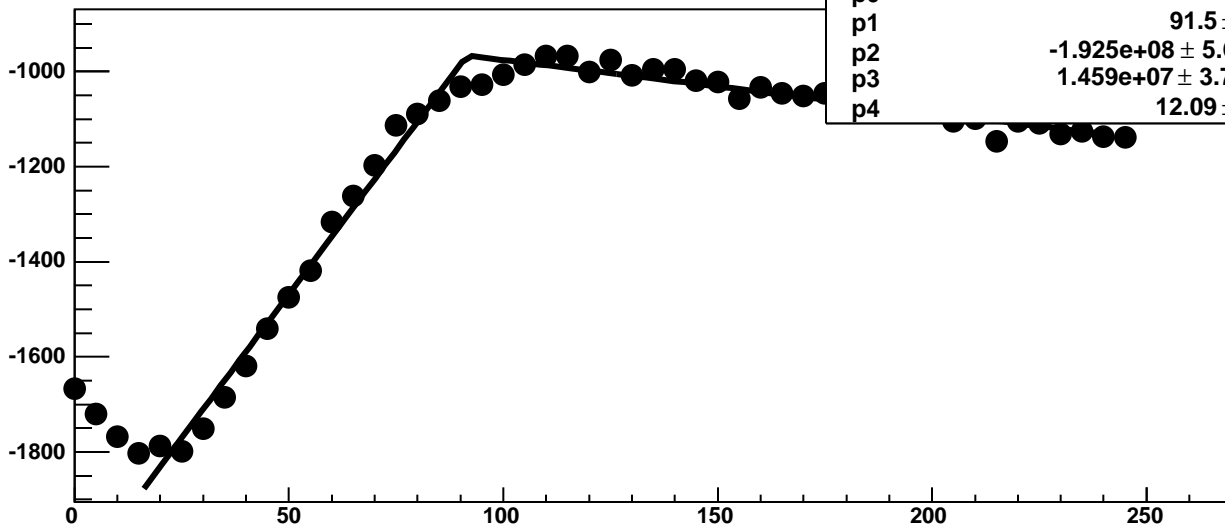
Chip 9, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold

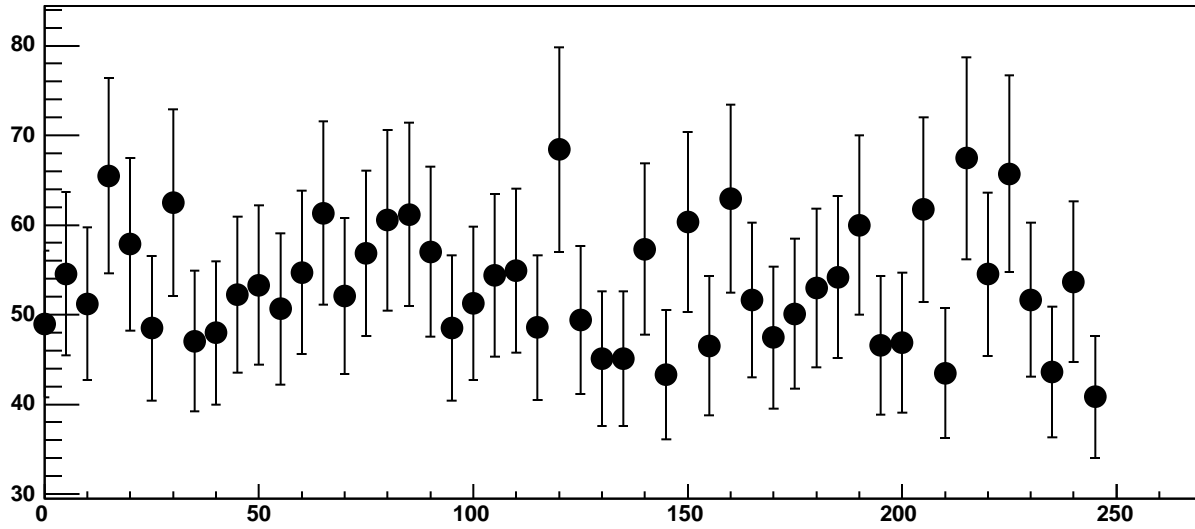


Chip 9, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold

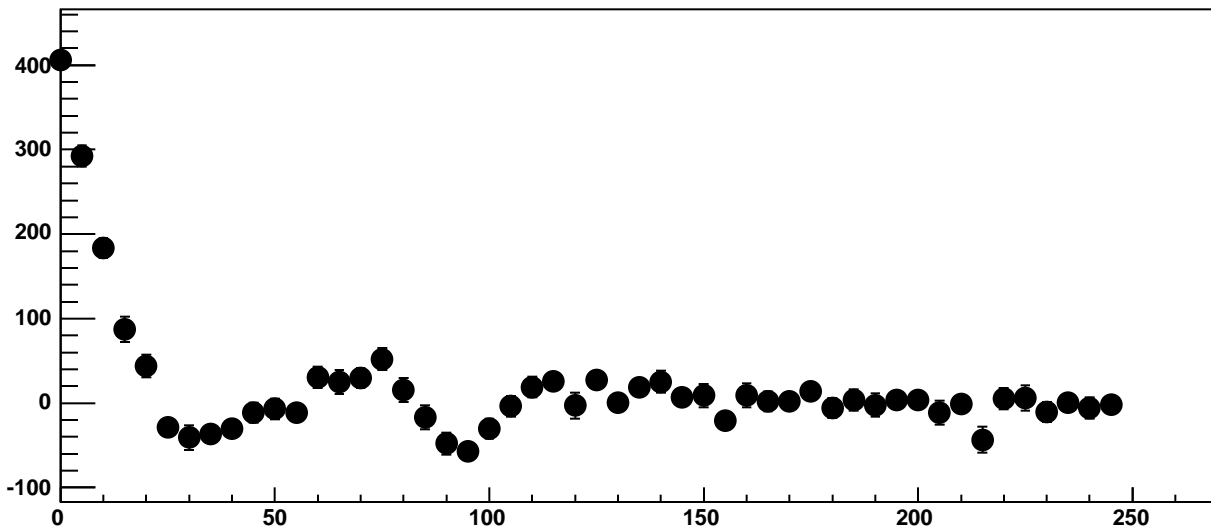


$\chi^2 / \text{ndf}$	199.7 / 41
p0	$-966.5 \pm 4.034$
p1	$91.5 \pm 0.5922$
p2	$-1.925\text{e}+08 \pm 5.696\text{e}+06$
p3	$1.459\text{e}+07 \pm 3.792\text{e}+05$
p4	$12.09 \pm 0.1432$

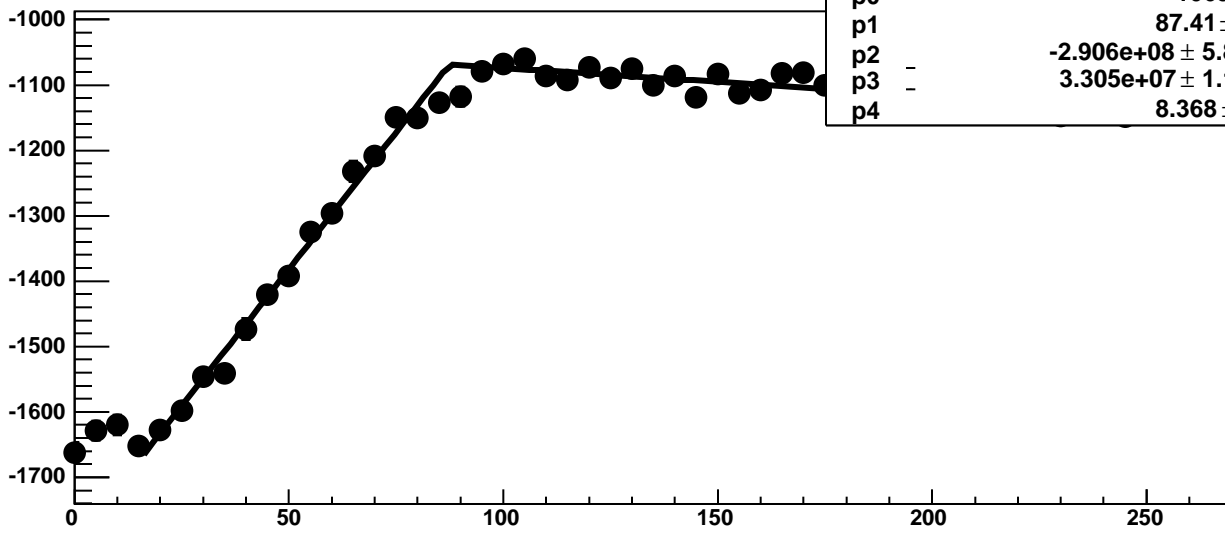
Chip 9, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

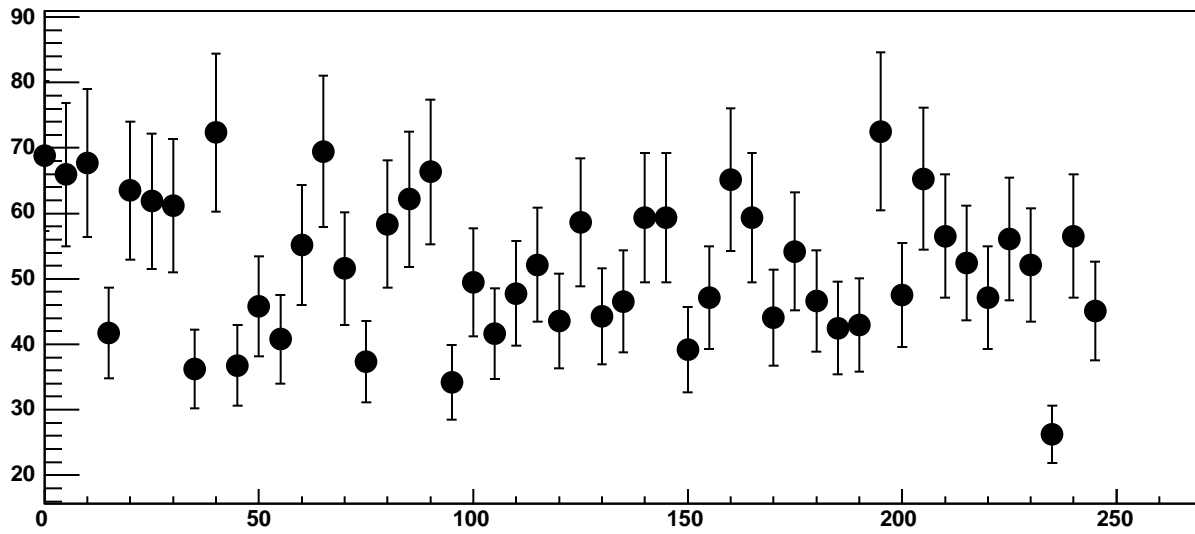


Chip 9, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold

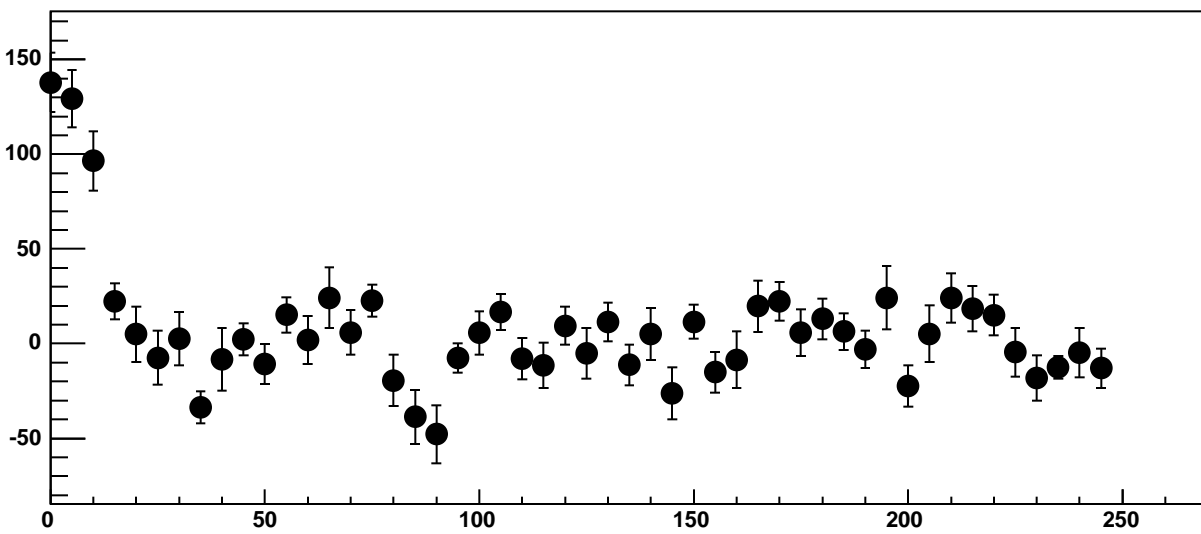


$\chi^2 / \text{ndf}$	102.2 / 41
p0	-1069 ± 3.802
p1	87.41 ± 0.5804
p2	-2.906e+08 ± 5.893e+06
p3	3.305e+07 ± 1.153e+06
p4	8.368 ± 0.1223

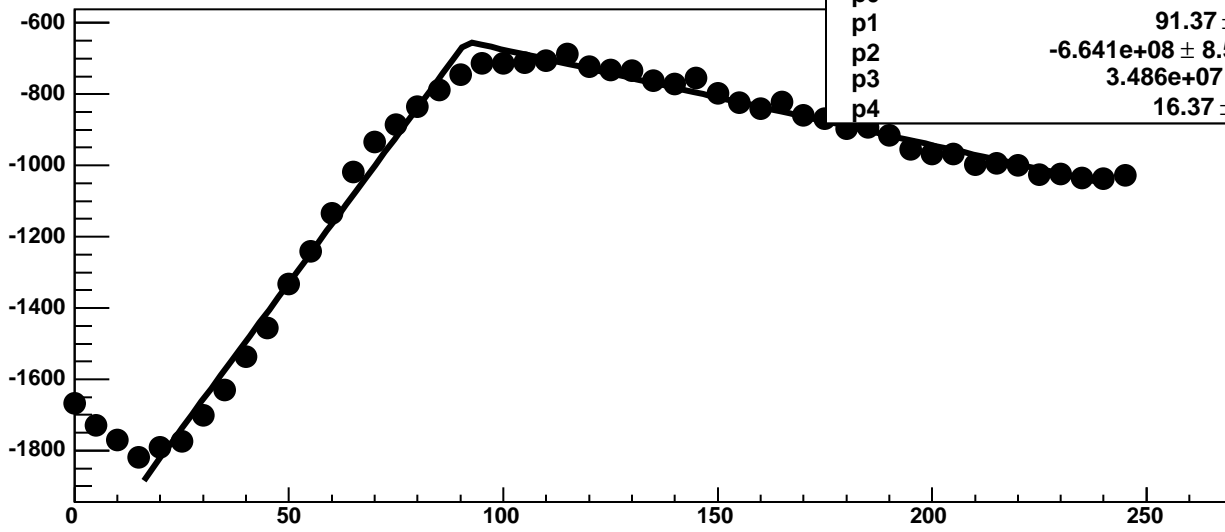
Chip 9, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold

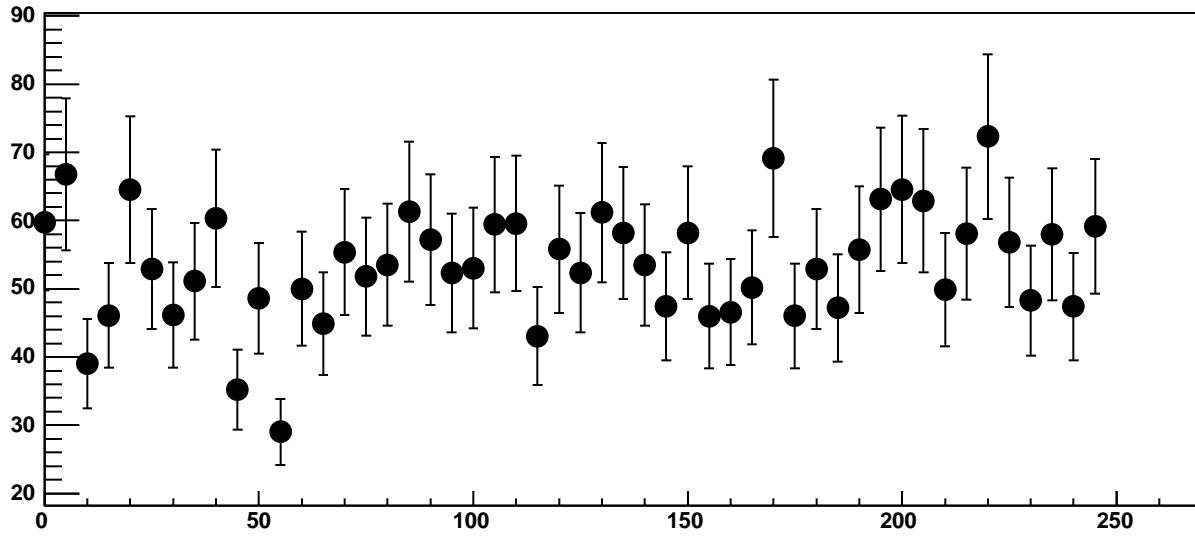


Chip 9, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

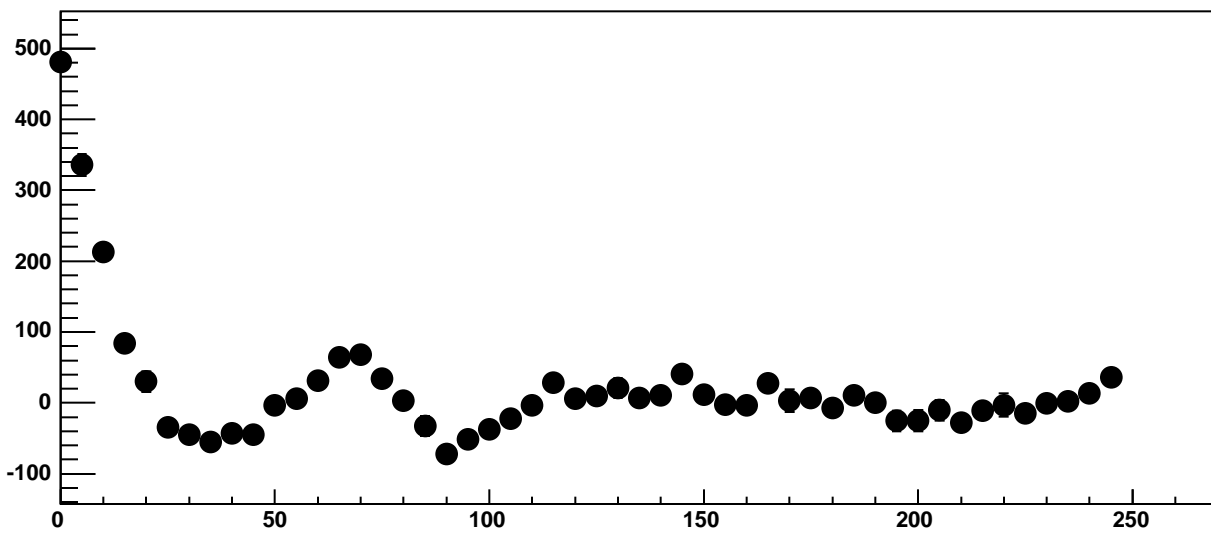


$\chi^2 / \text{ndf}$	357 / 41
p0	-651.9 ± 3.968
p1	91.37 ± 0.3927
p2	-6.641e+08 ± 8.516e+06
p3	3.486e+07 ± 4e+05
p4	16.37 ± 0.1325

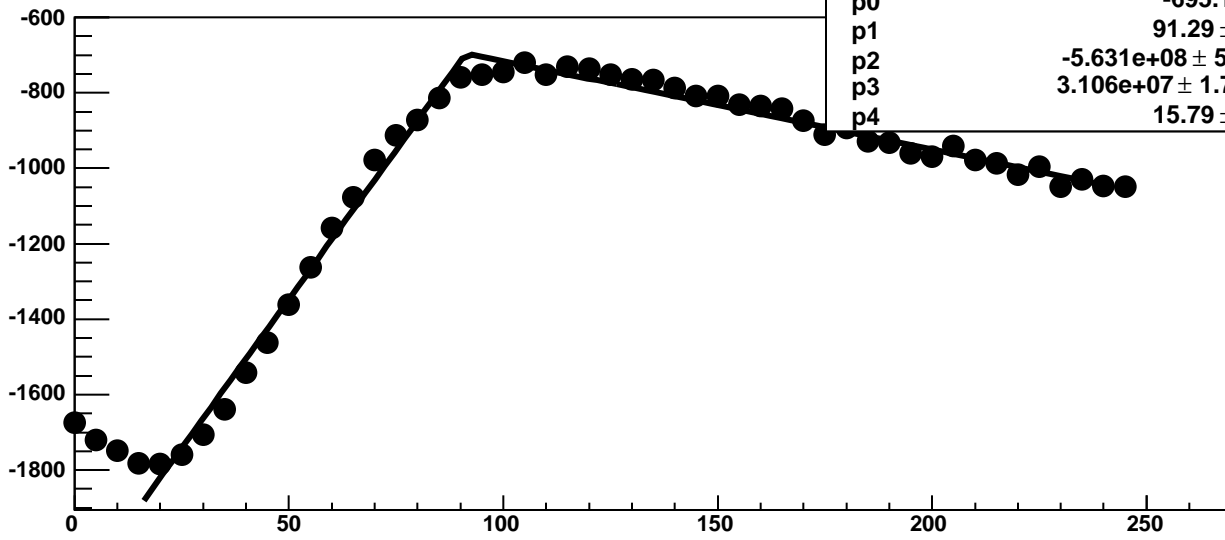
Chip 9, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

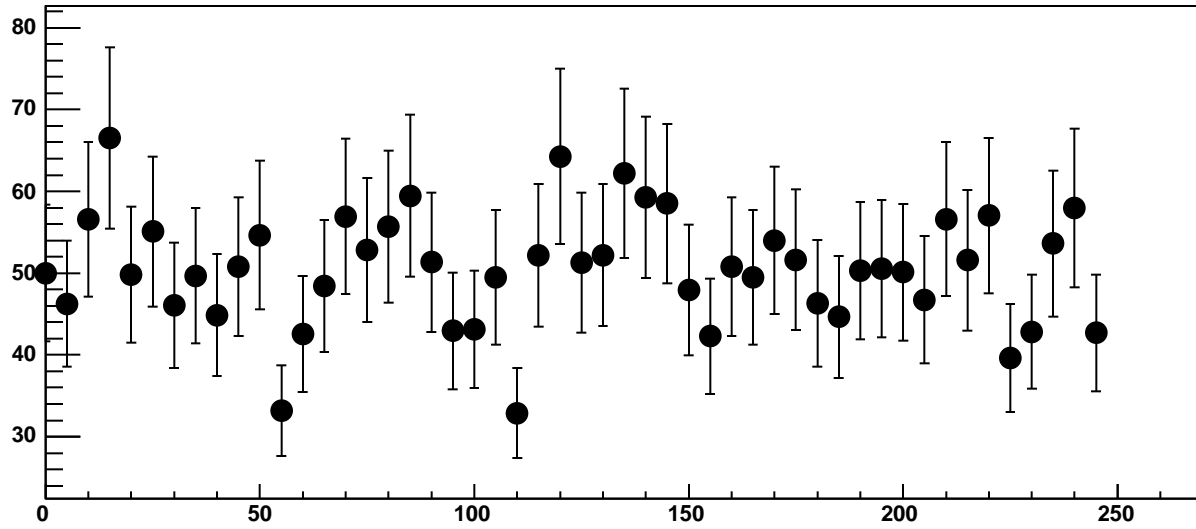


Chip 9, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

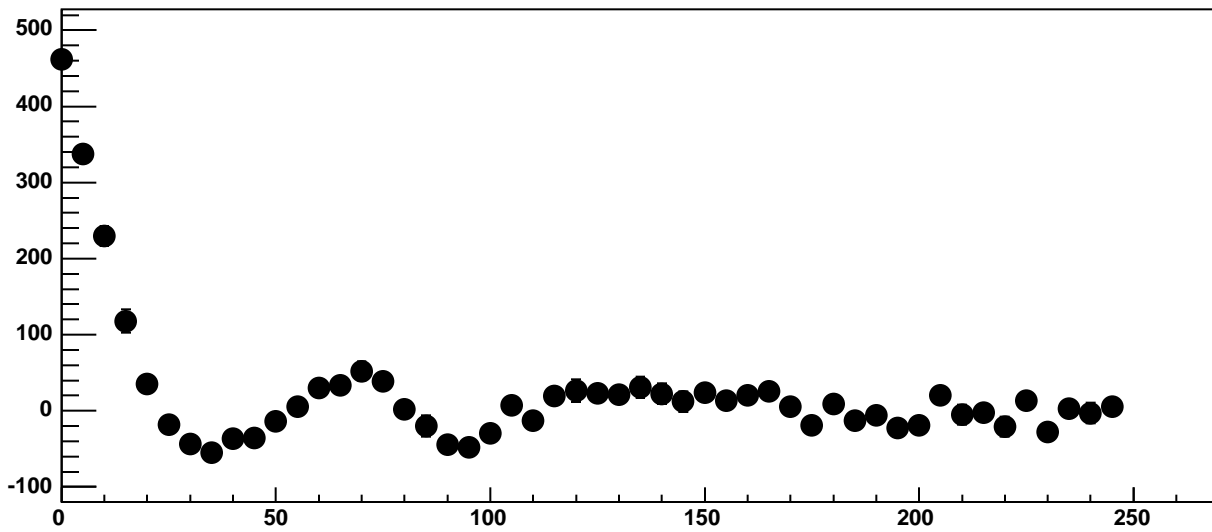


$\chi^2 / \text{ndf}$	296.8 / 41
p0	$-695.1 \pm 3.546$
p1	$91.29 \pm 0.3944$
p2	$-5.631\text{e}+08 \pm 5.34\text{e}+06$
p3	$3.106\text{e}+07 \pm 1.713\text{e}+05$
p4	$15.79 \pm 0.1344$

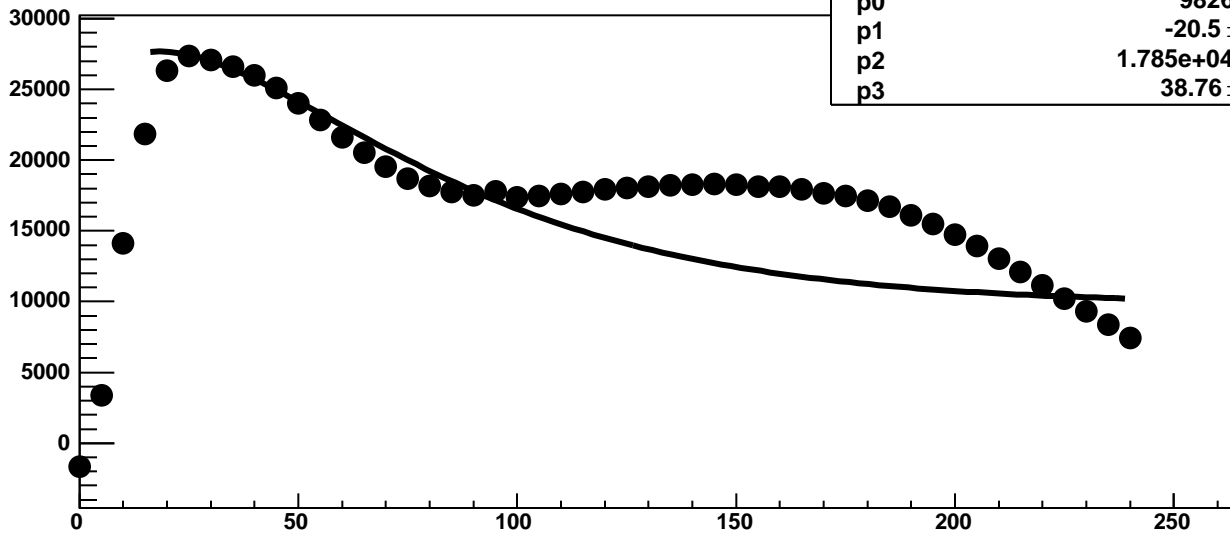
Chip 9, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

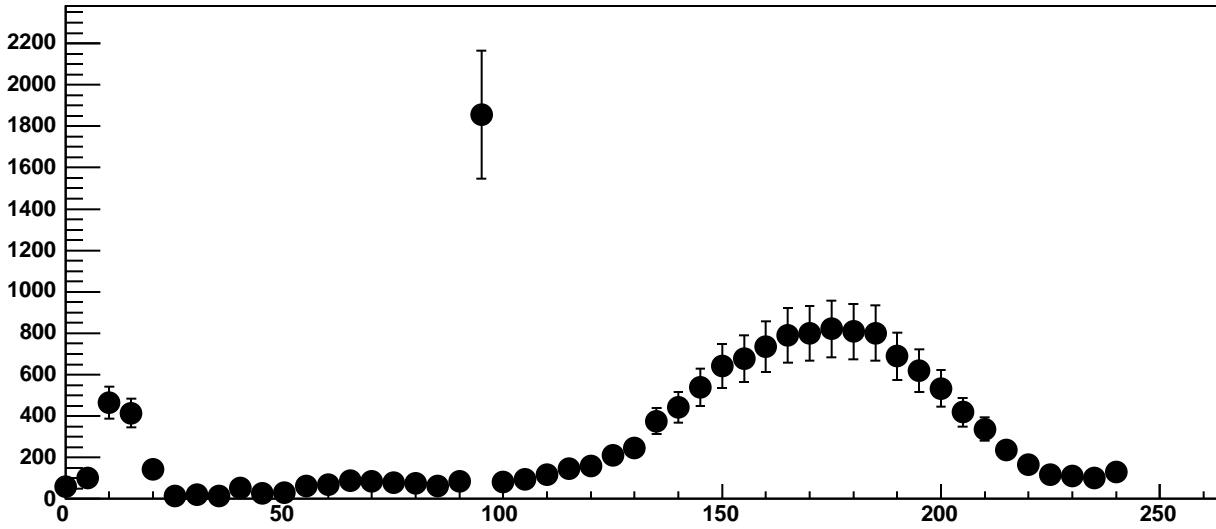


Chip 9, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold

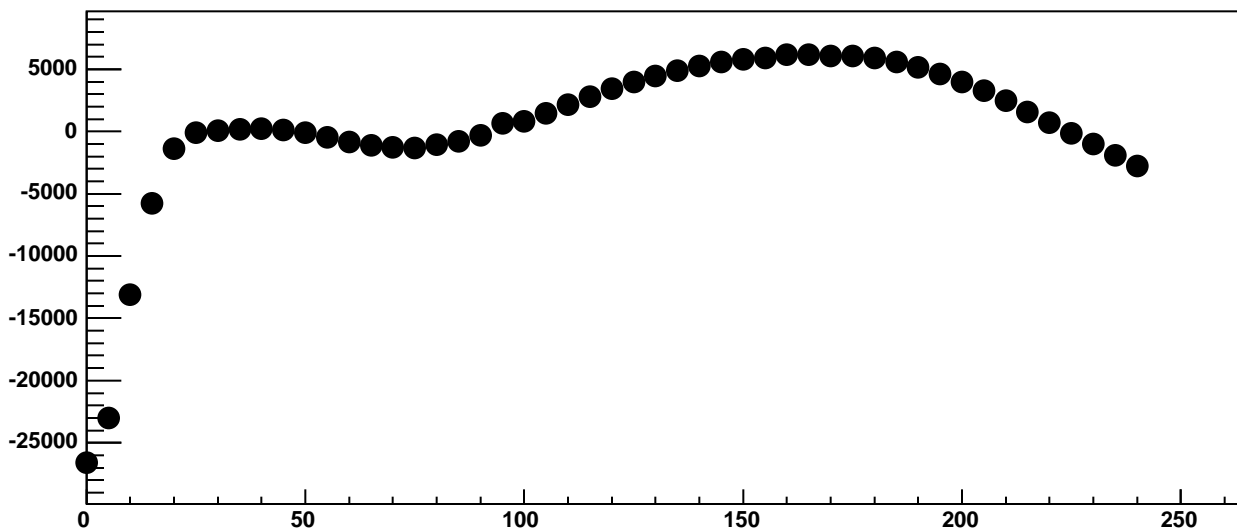


$\chi^2 / \text{ndf}$	1.161e+05 / 42
p0	9826 ± 16.25
p1	-20.5 ± 0.1863
p2	1.785e+04 ± 21.72
p3	38.76 ± 0.0888

Chip 9, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

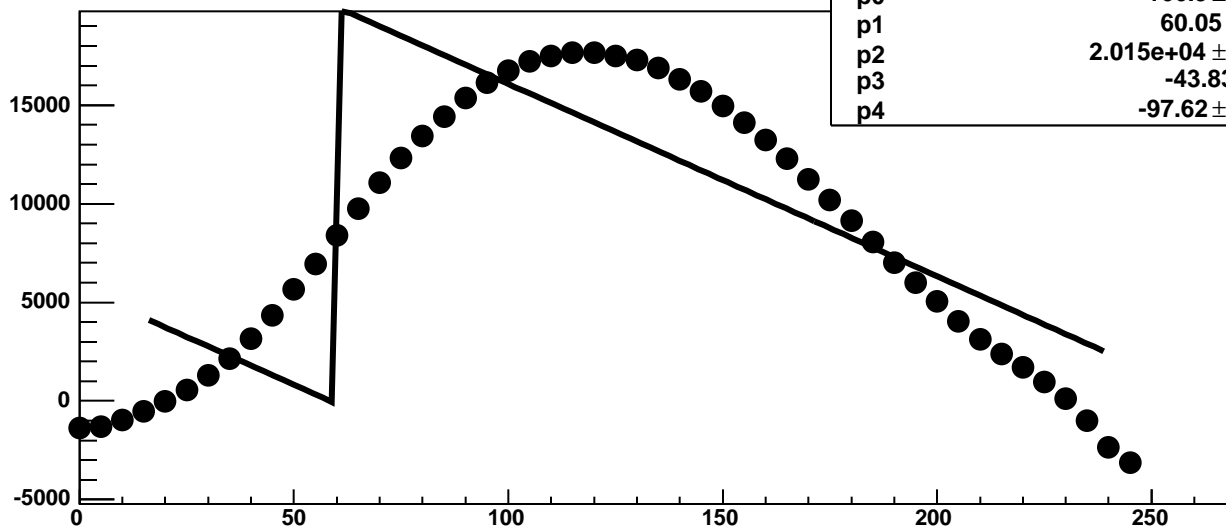


Chip 9, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold



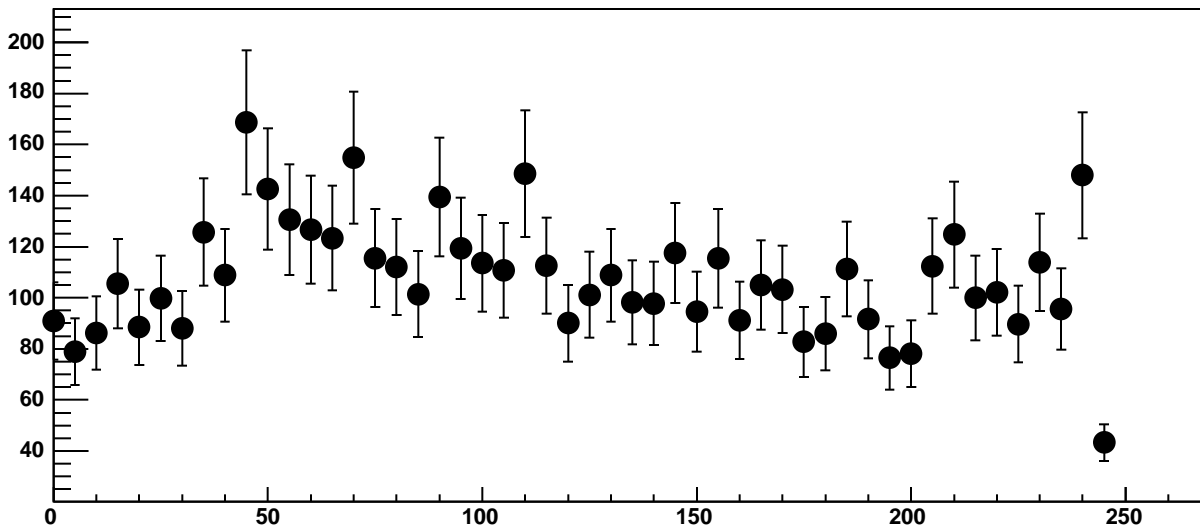


Chip 9, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold

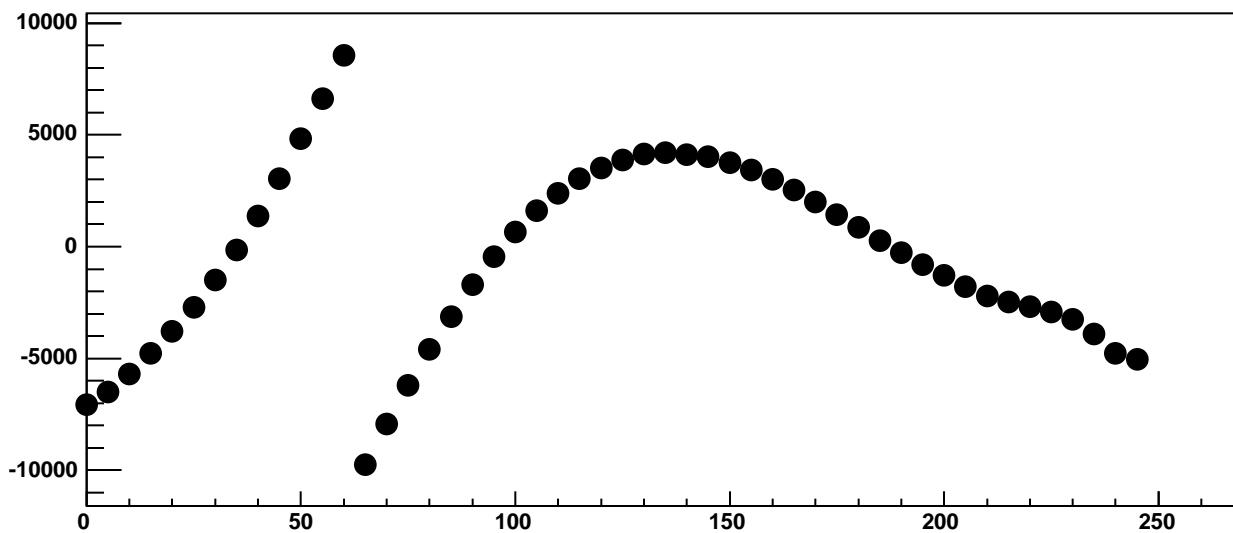


$\chi^2 / \text{ndf}$	9.585e+05 / 41
p0	-166.9 ± 0.06755
p1	60.05 ± 0.3119
p2	2.015e+04 ± 0.06846
p3	-43.83 ± 12.37
p4	-97.62 ± 0.02868

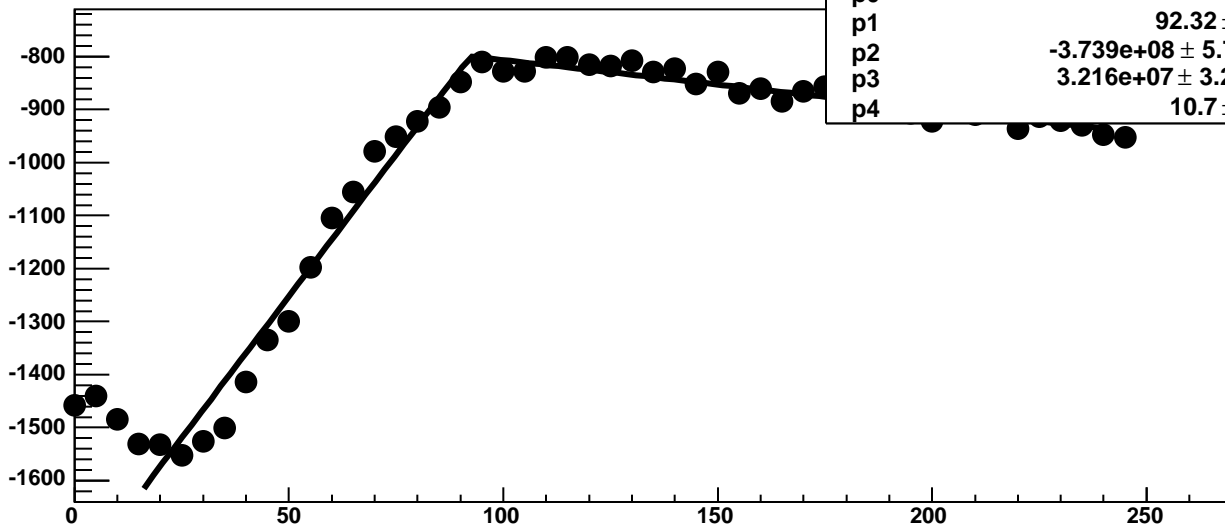
Chip 9, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold

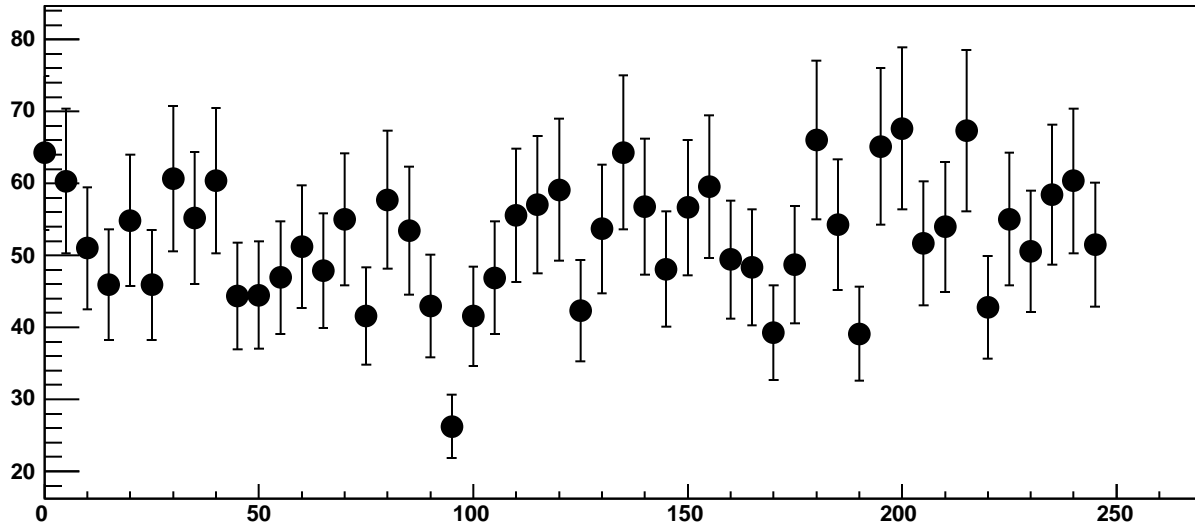


Chip 9, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

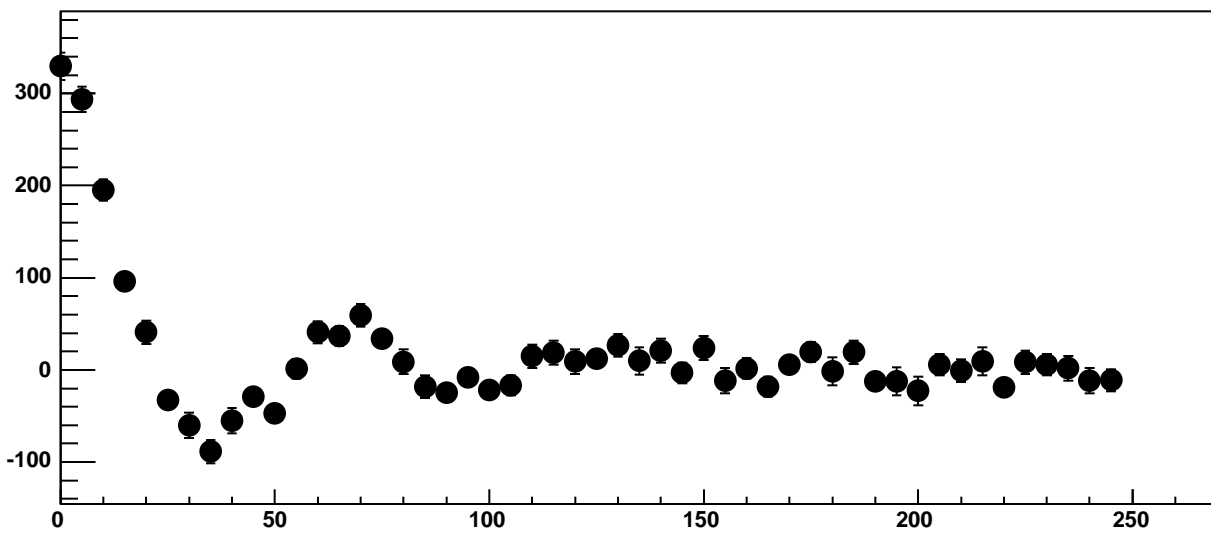


$\chi^2 / \text{ndf}$	329 / 41
p0	$-799.3 \pm 3.416$
p1	$92.32 \pm 0.5692$
p2	$-3.739\text{e}+08 \pm 5.749\text{e}+06$
p3	$3.216\text{e}+07 \pm 3.226\text{e}+05$
p4	$10.7 \pm 0.1218$

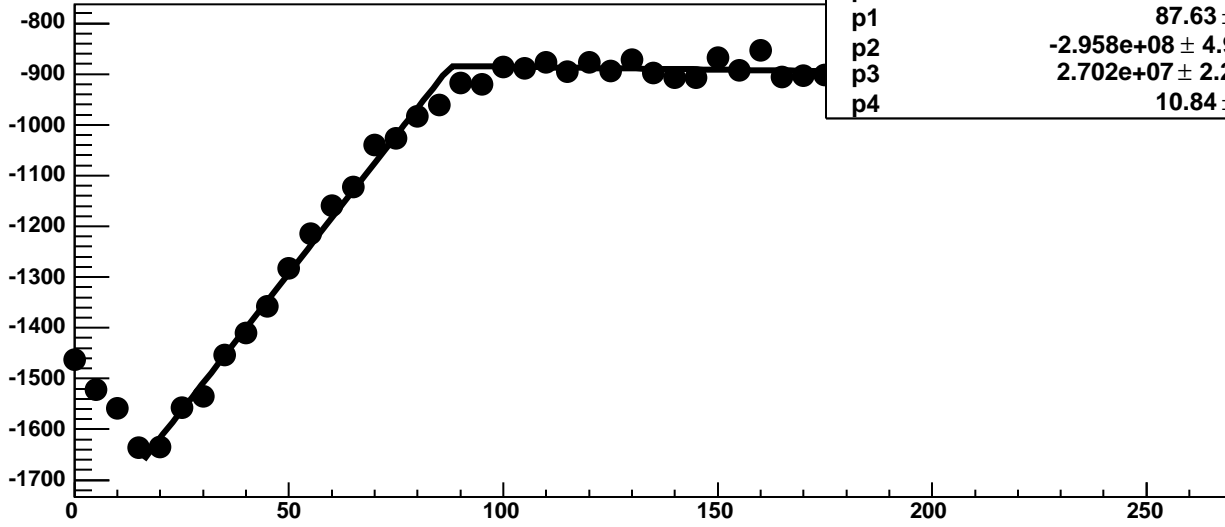
Chip 9, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

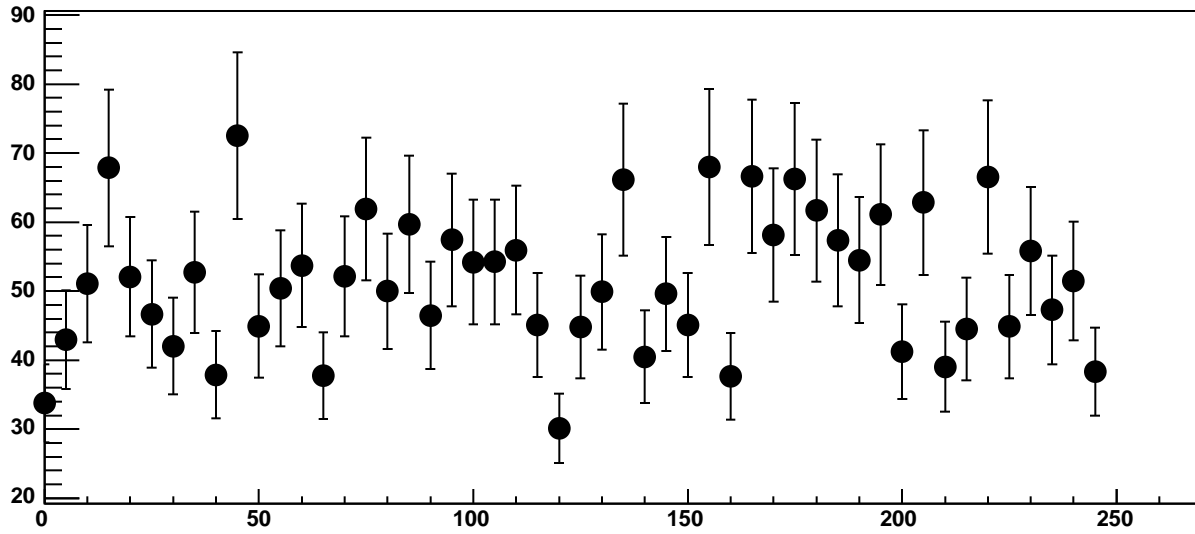


Chip 9, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

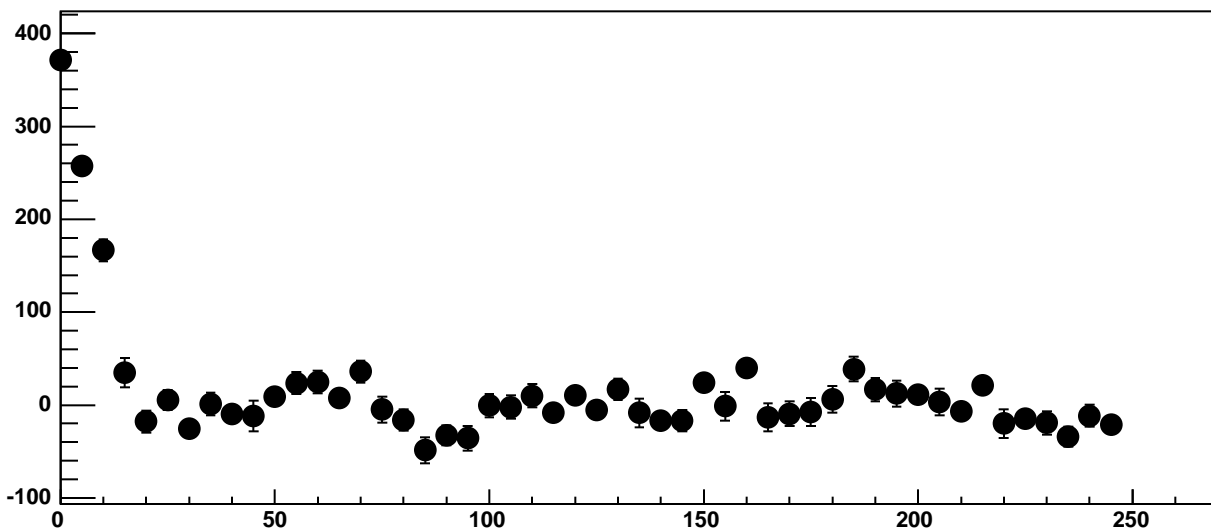


$\chi^2 / \text{ndf}$	141.2 / 41
p0	-884.3 ± 3.931
p1	87.63 ± 0.6843
p2	-2.958e+08 ± 4.925e+06
p3	2.702e+07 ± 2.216e+05
p4	10.84 ± 0.1457

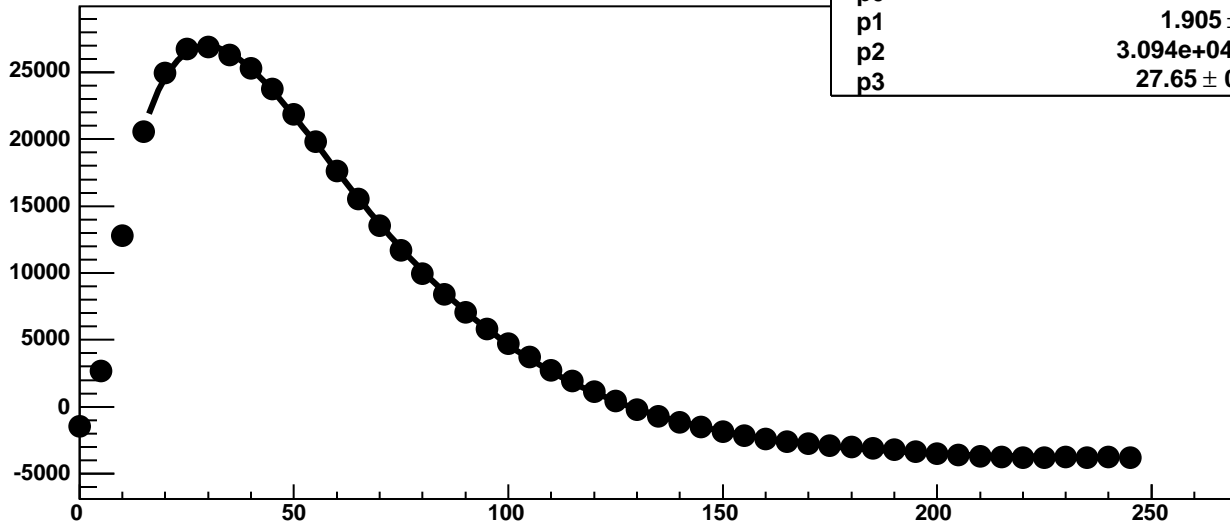
Chip 9, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

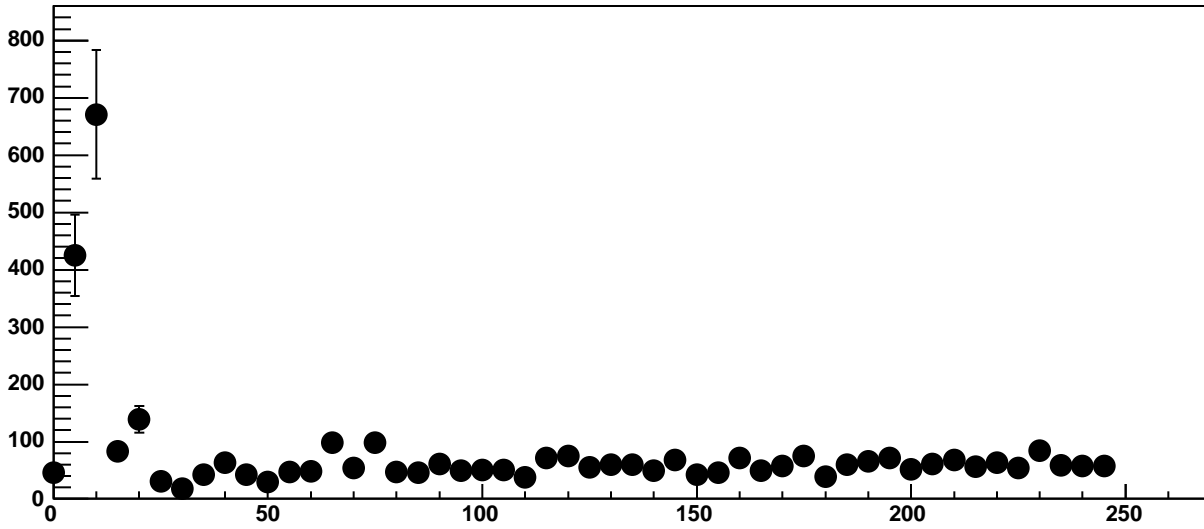


Chip 9, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold

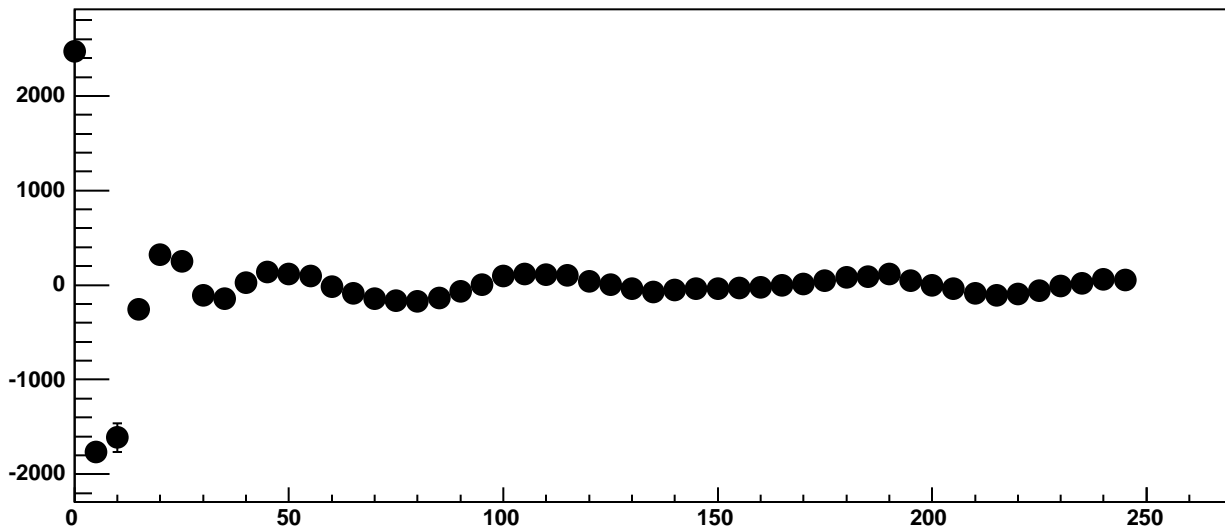


$\chi^2 / \text{ndf}$	4519 / 42
p0	$-3955 \pm 3.571$
p1	$1.905 \pm 0.0177$
p2	$3.094\text{e}+04 \pm 4.359$
p3	$27.65 \pm 0.009861$

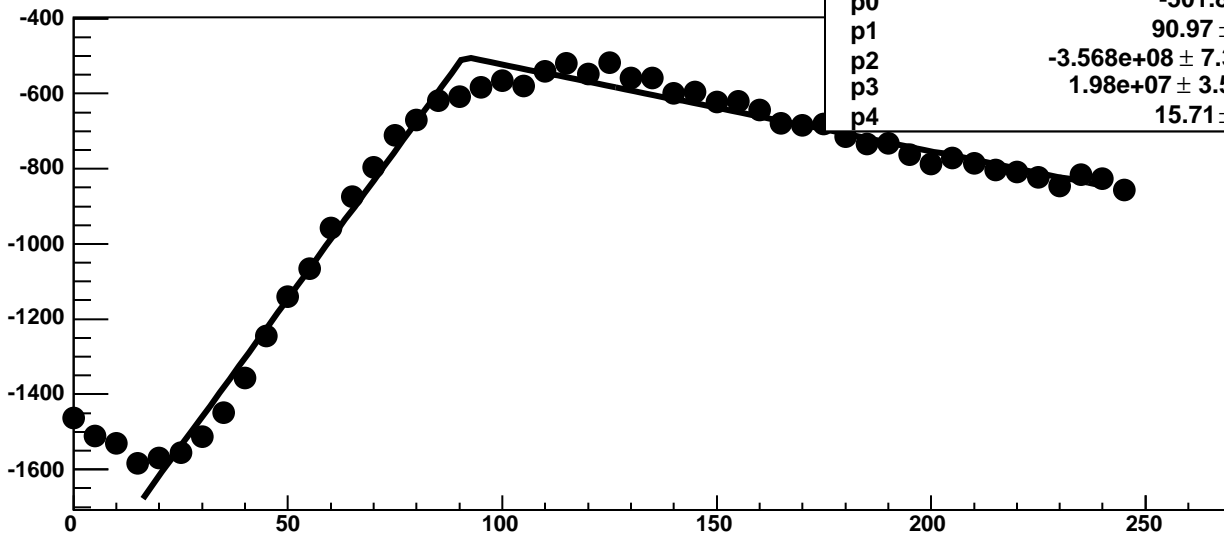
Chip 9, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold

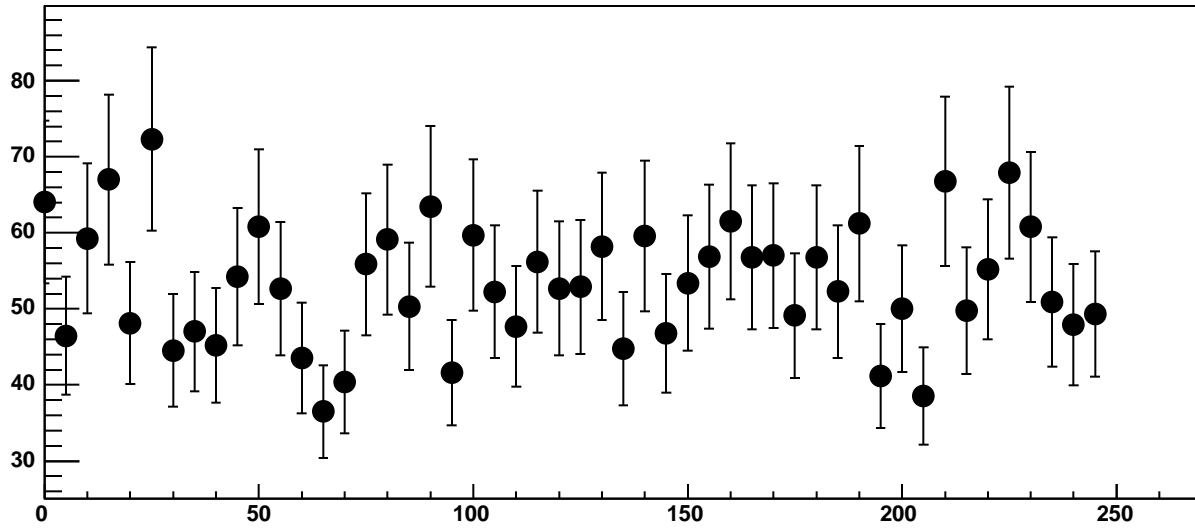


Chip 9, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

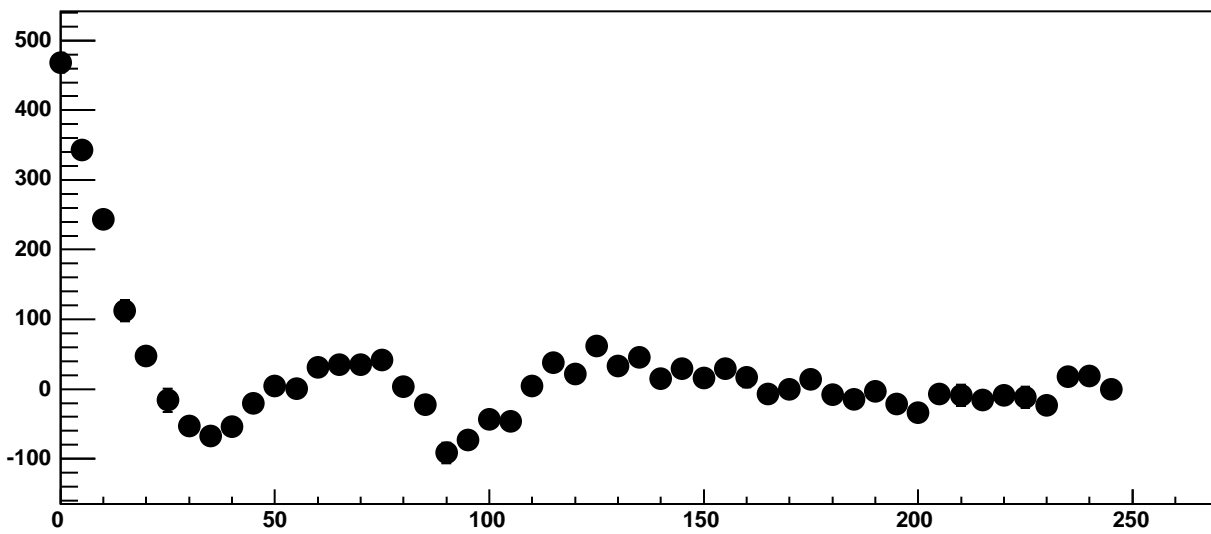


$\chi^2 / \text{ndf}$	458.2 / 41
p0	$-501.8 \pm 3.885$
p1	$90.97 \pm 0.4045$
p2	$-3.568\text{e}+08 \pm 7.306\text{e}+06$
p3	$1.98\text{e}+07 \pm 3.567\text{e}+05$
p4	$15.71 \pm 0.1355$

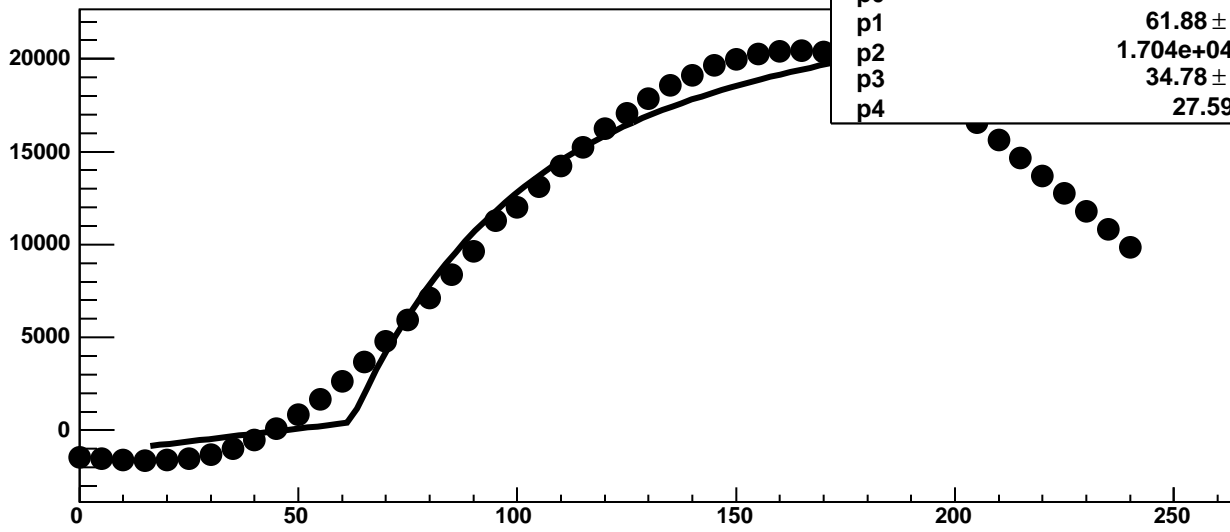
Chip 9, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

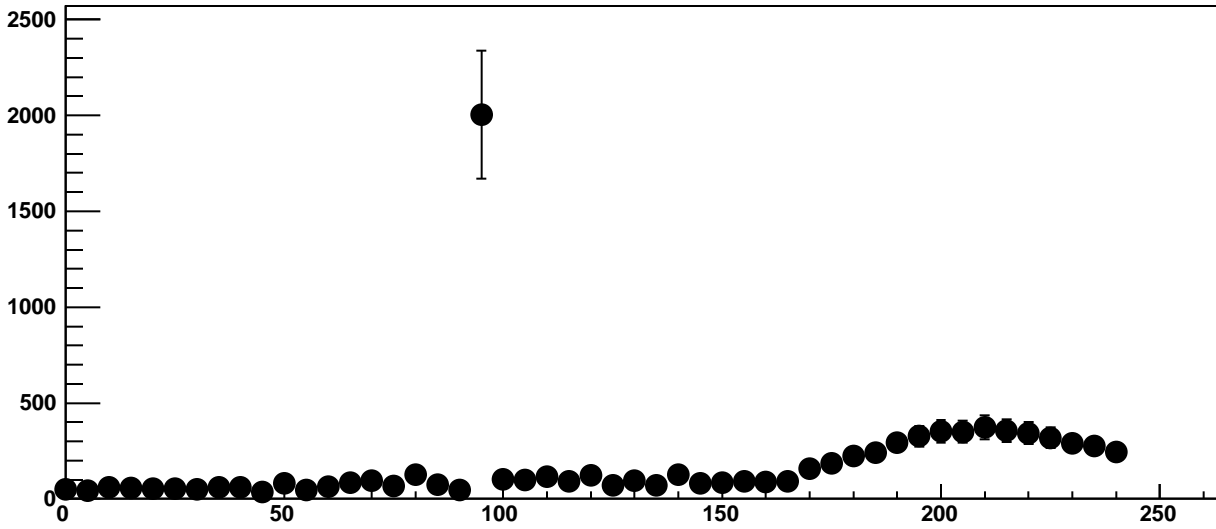


Chip 9, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

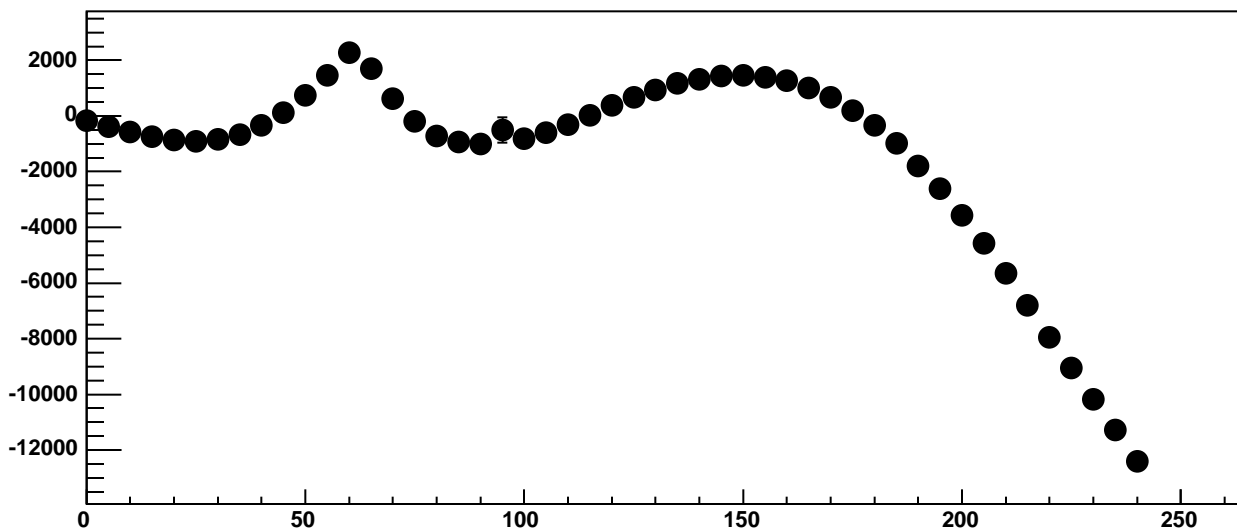


$\chi^2 / \text{ndf}$	2.691e+05 / 41
p0	416.5 ± 6.842
p1	61.88 ± 0.03442
p2	1.704e+04 ± 32.96
p3	34.78 ± 0.08339
p4	27.59 ± 0.215

Chip 9, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold

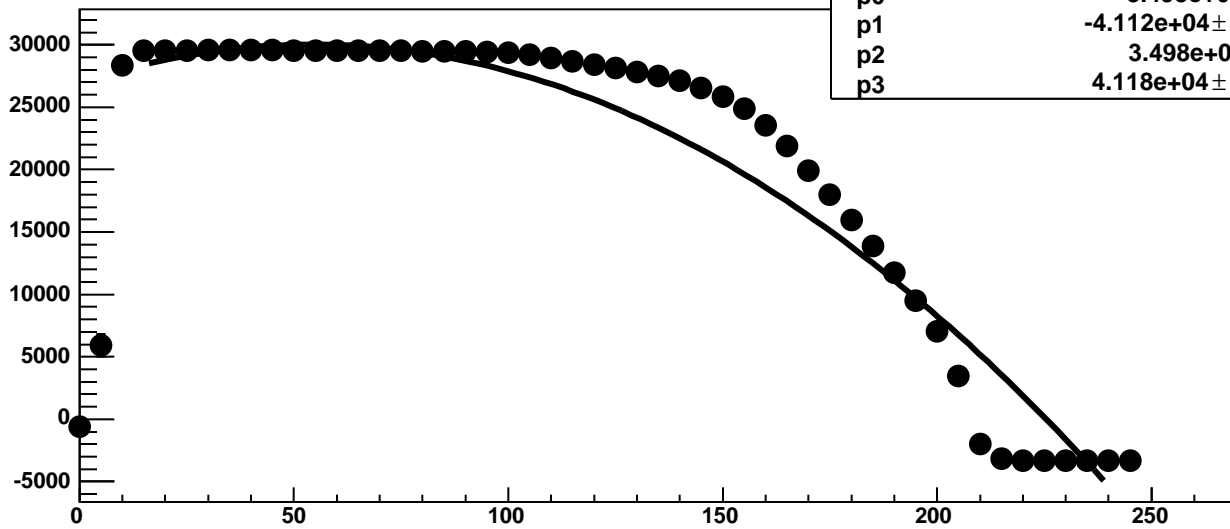


Chip 9, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

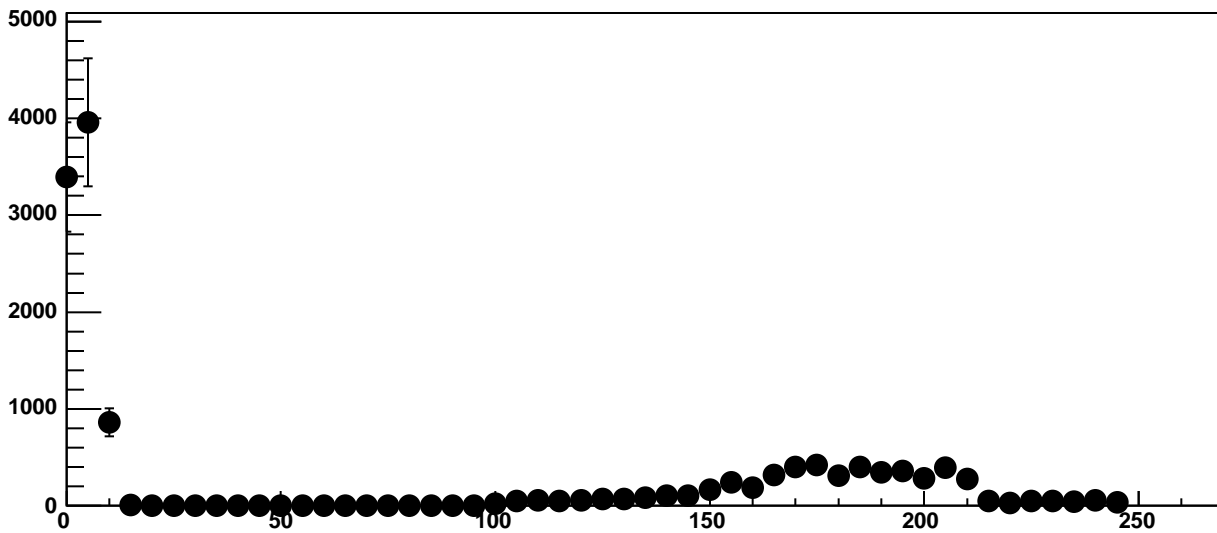


Chip 9, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

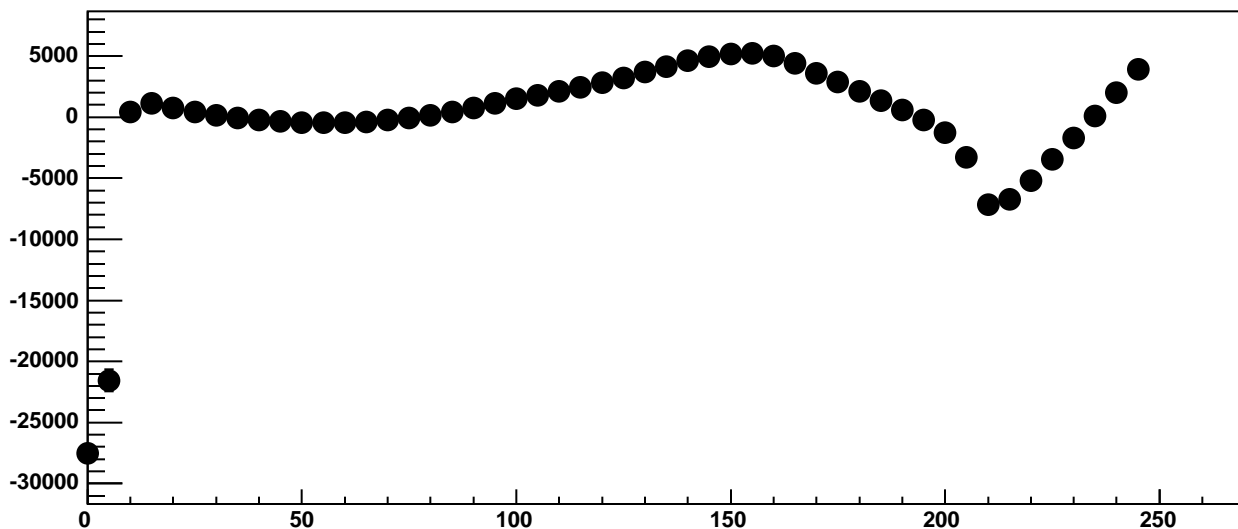
$\chi^2 / \text{ndf}$	5.102e+06 / 42
p0	-3.498e+09 ± 3.61
p1	-4.112e+04 ± 0.06584
p2	3.498e+09 ± 3.61
p3	4.118e+04 ± 0.06579



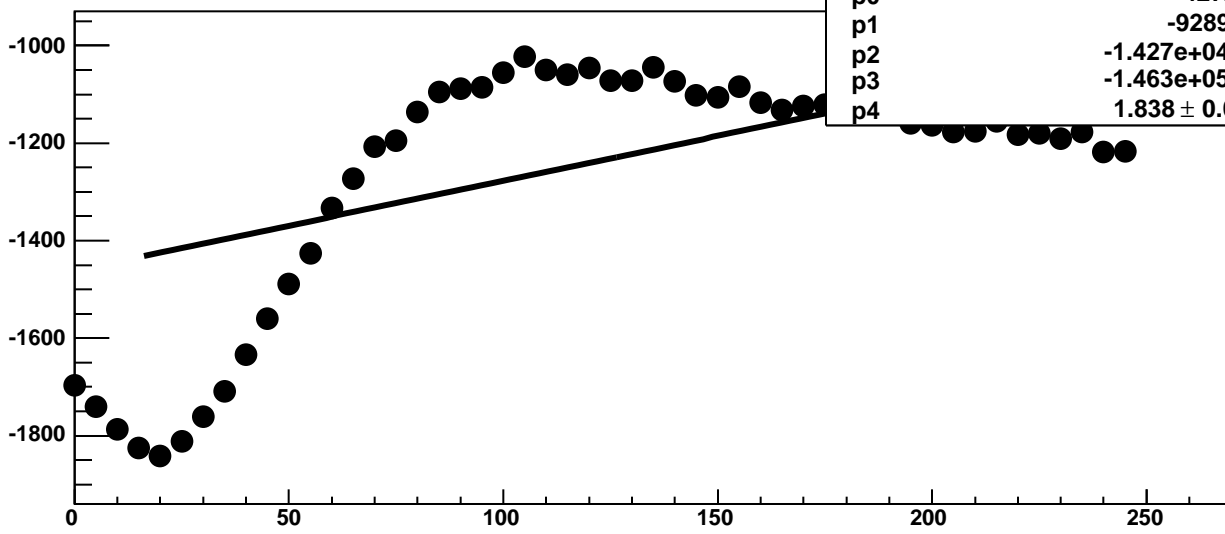
Chip 9, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

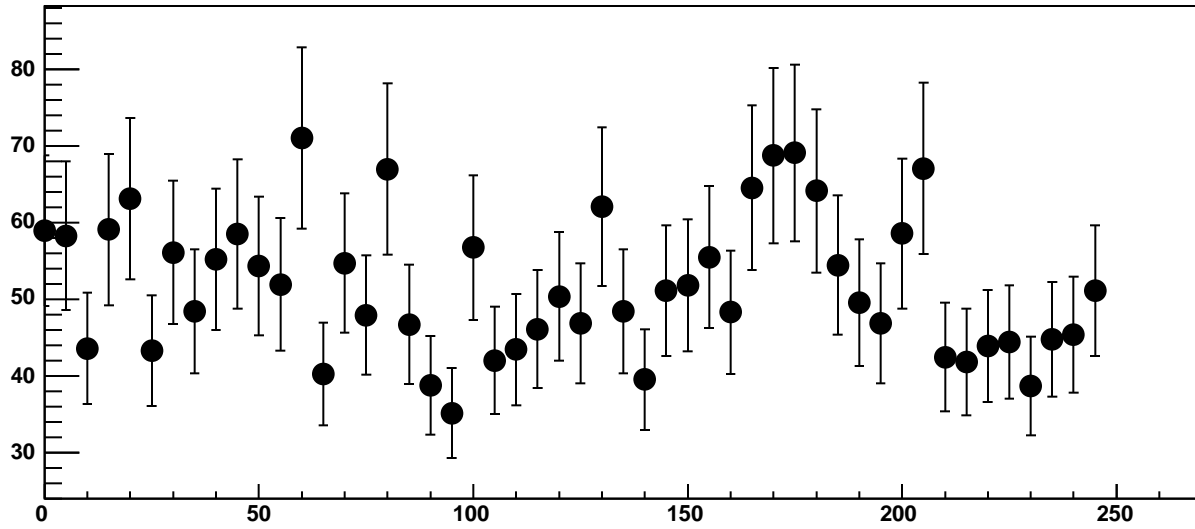


Chip 9, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

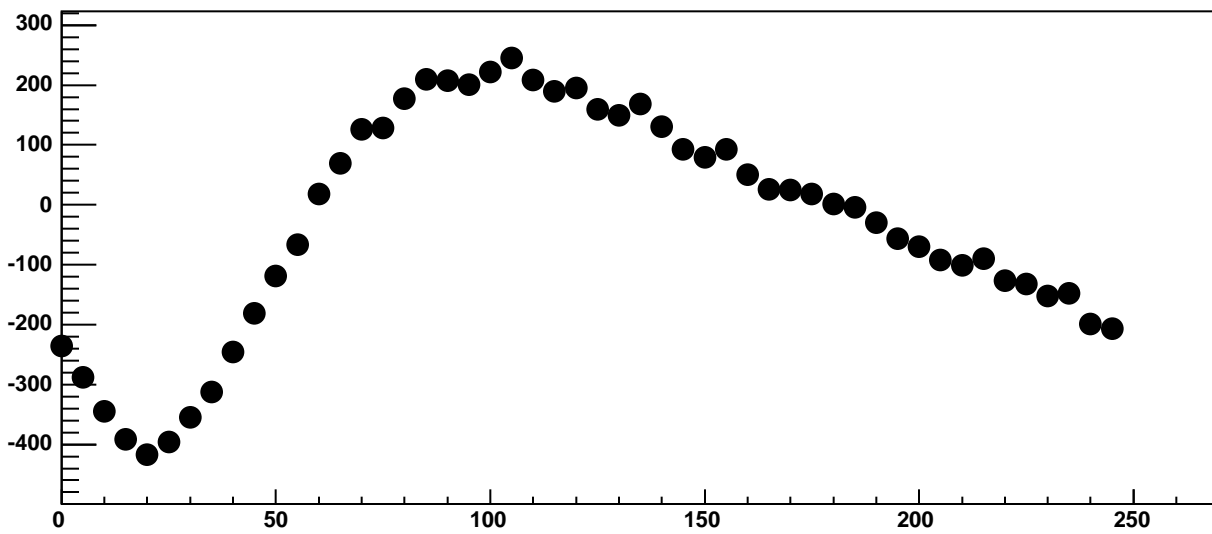


$\chi^2 / \text{ndf}$	1.19e+04 / 41
p0	-4272 ± 8.29
p1	-9289 ± 4.027
p2	-1.427e+04 ± 10.79
p3	-1.463e+05 ± 499.6
p4	1.838 ± 0.0008799

Chip 9, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold

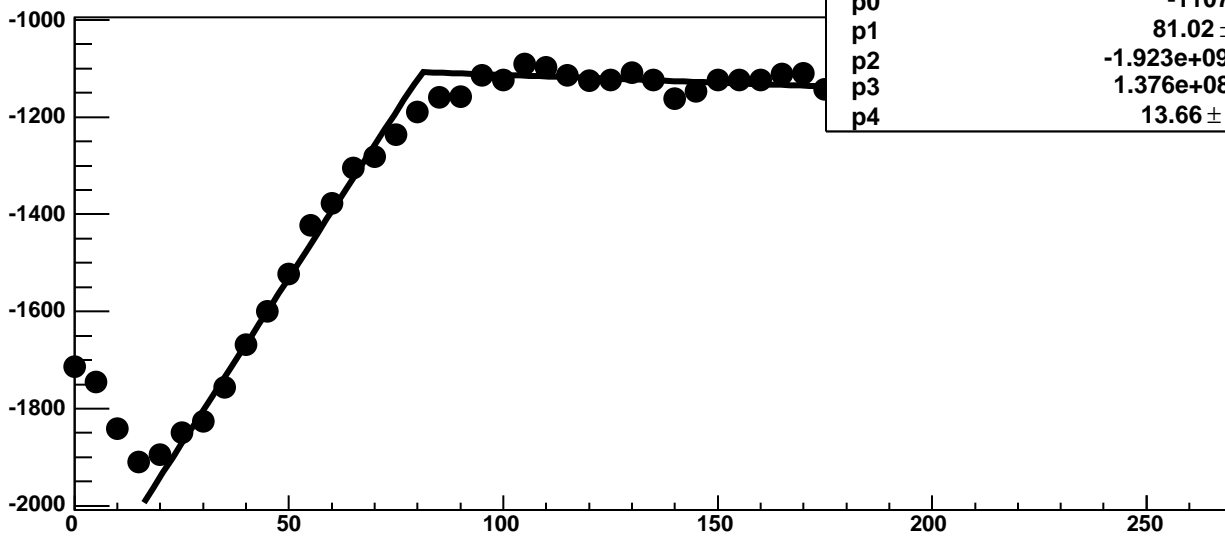


Chip 9, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold



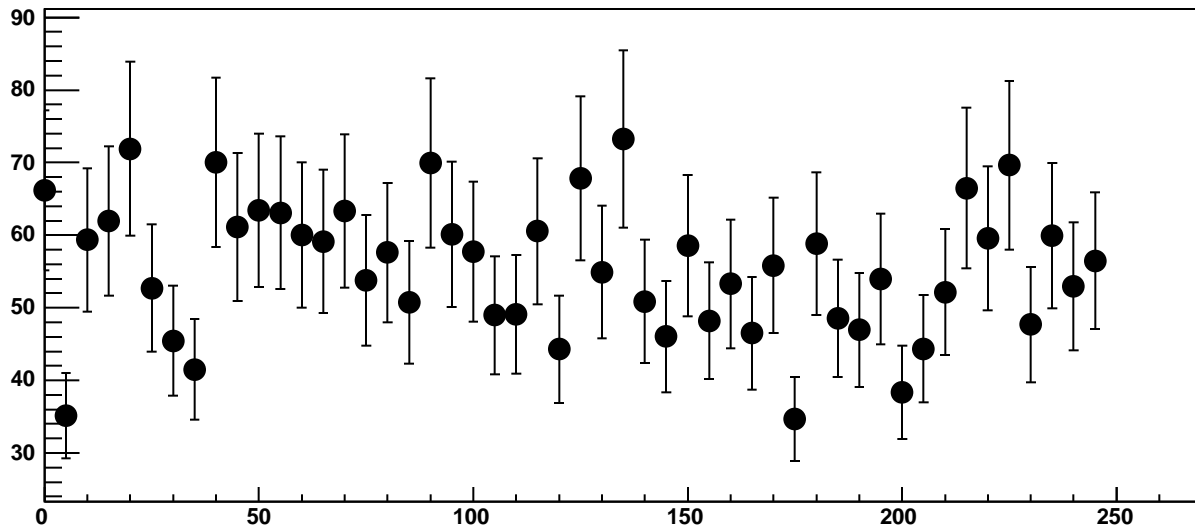


Chip 9, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

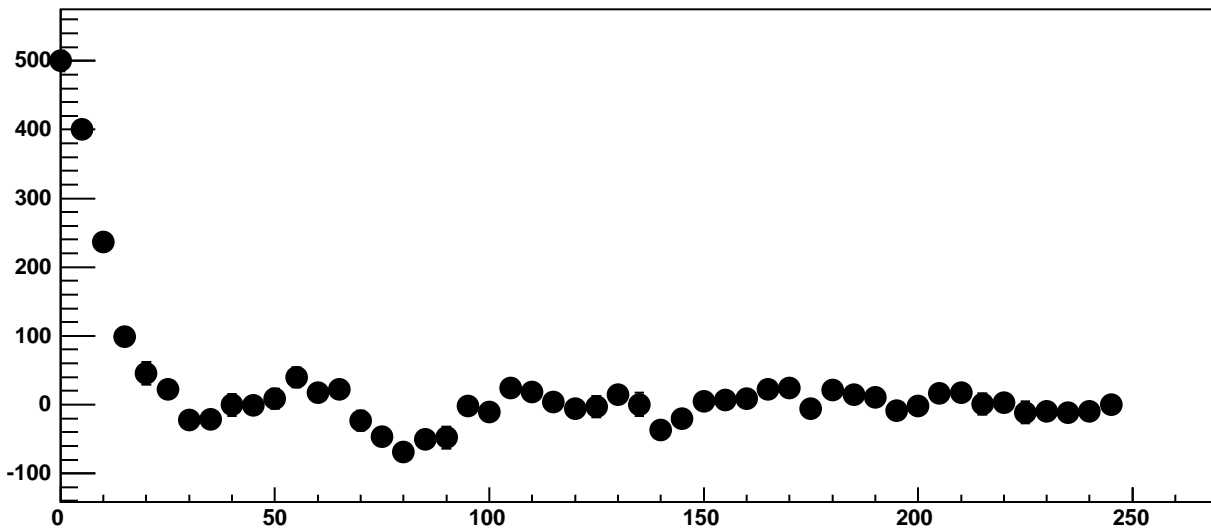


$\chi^2 / \text{ndf}$	198.5 / 41
p0	$-1107 \pm 1.869$
p1	$81.02 \pm 0.3316$
p2	$-1.923\text{e}+09 \pm 1.414$
p3	$1.376\text{e}+08 \pm 1.414$
p4	$13.66 \pm 0.03382$

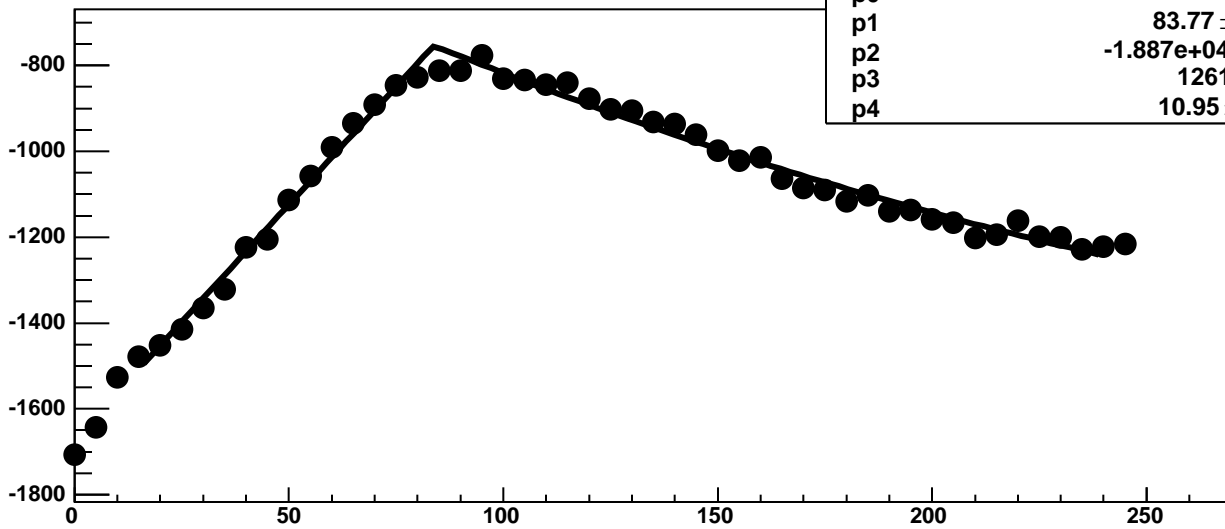
Chip 9, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

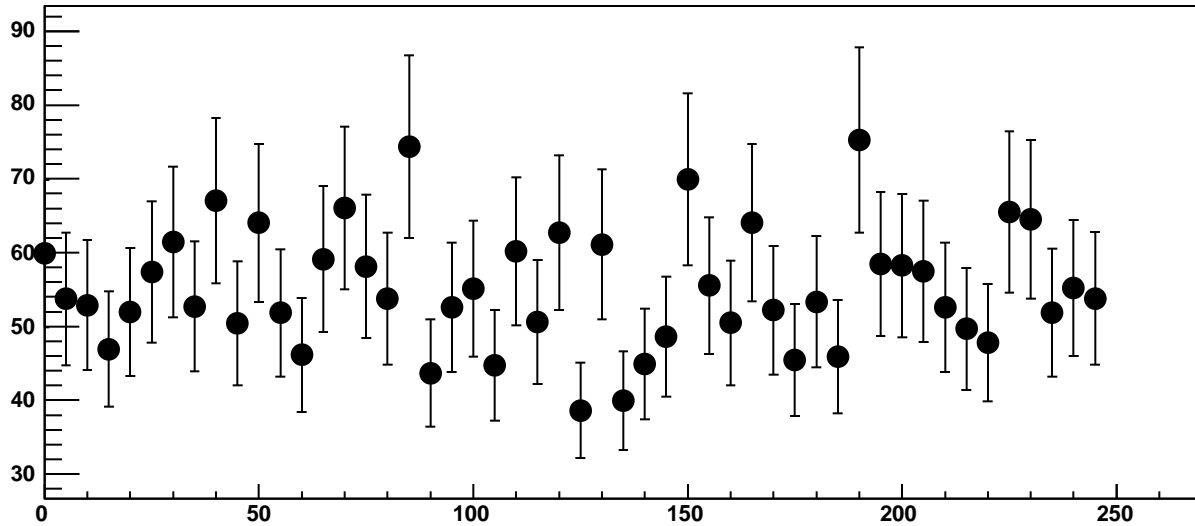


Chip 9, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold

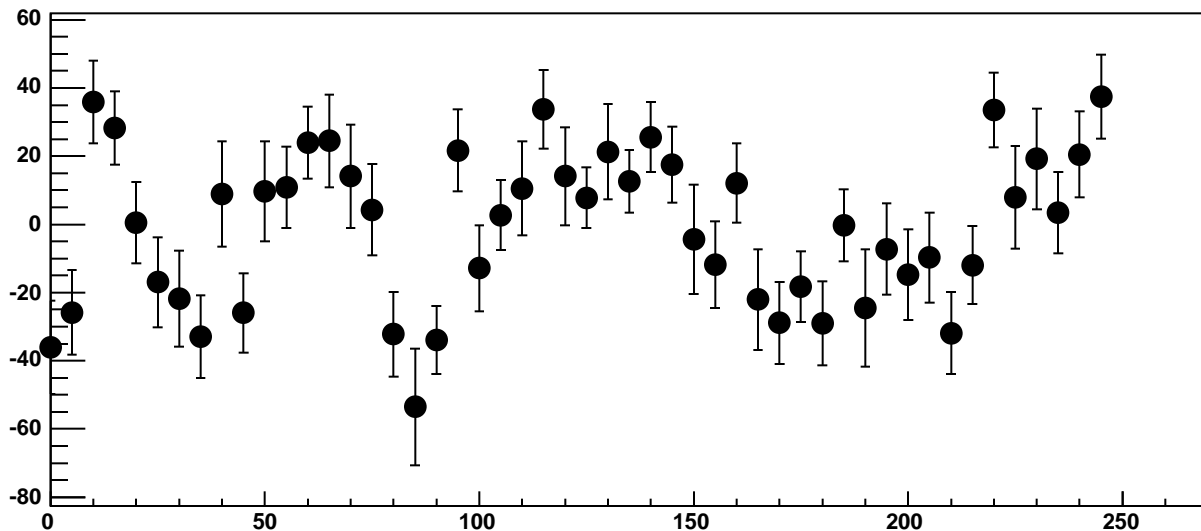


$\chi^2 / \text{ndf}$	135.4 / 41
p0	$-754 \pm 4.521$
p1	$83.77 \pm 0.5894$
p2	$-1.887e+04 \pm 2743$
p3	$1261 \pm 193.8$
p4	$10.95 \pm 0.1641$

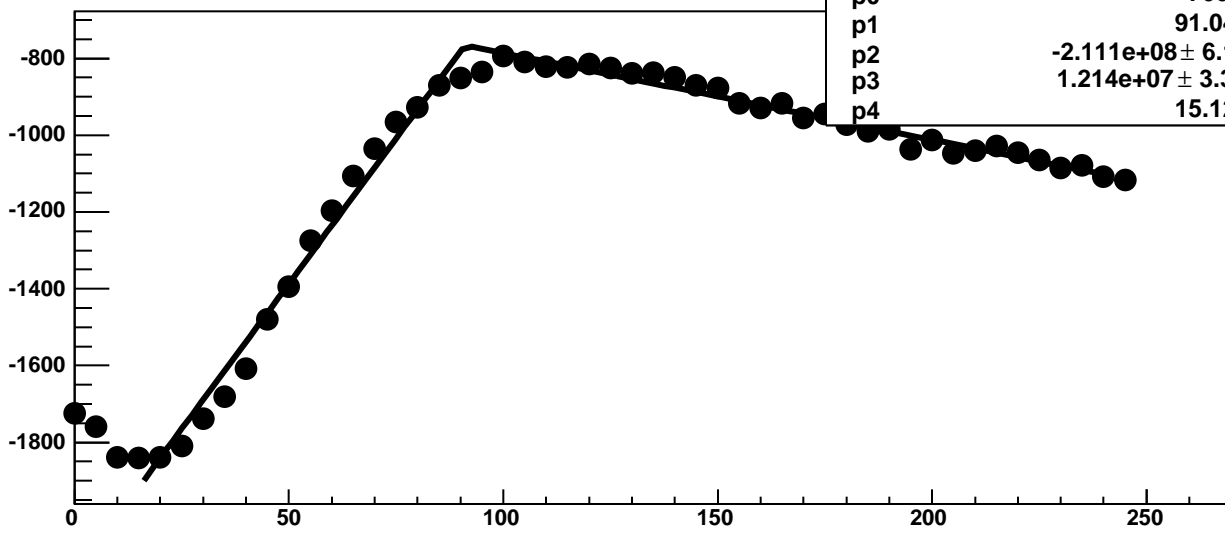
Chip 9, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold

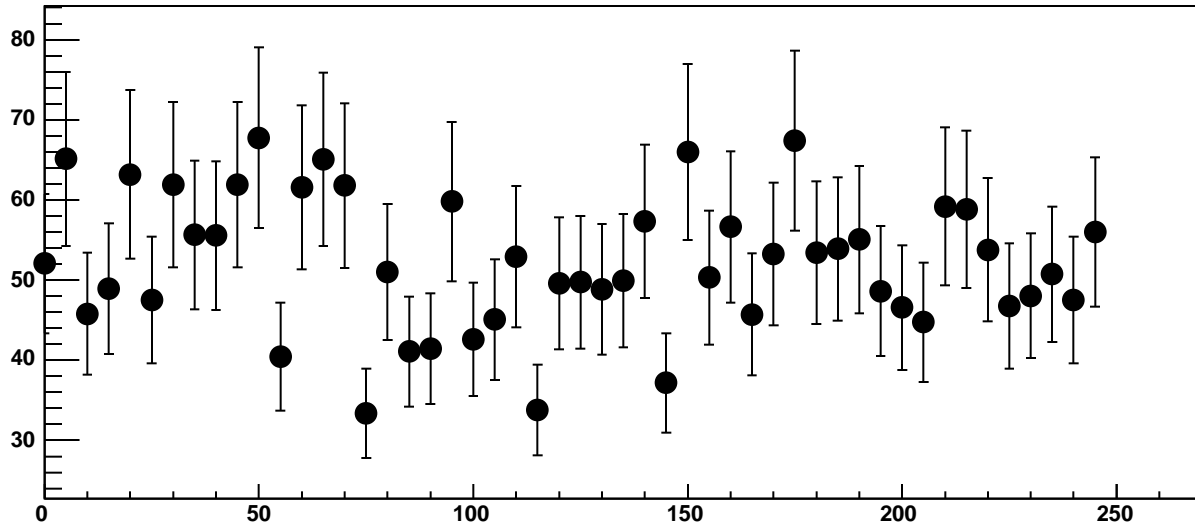


Chip 9, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

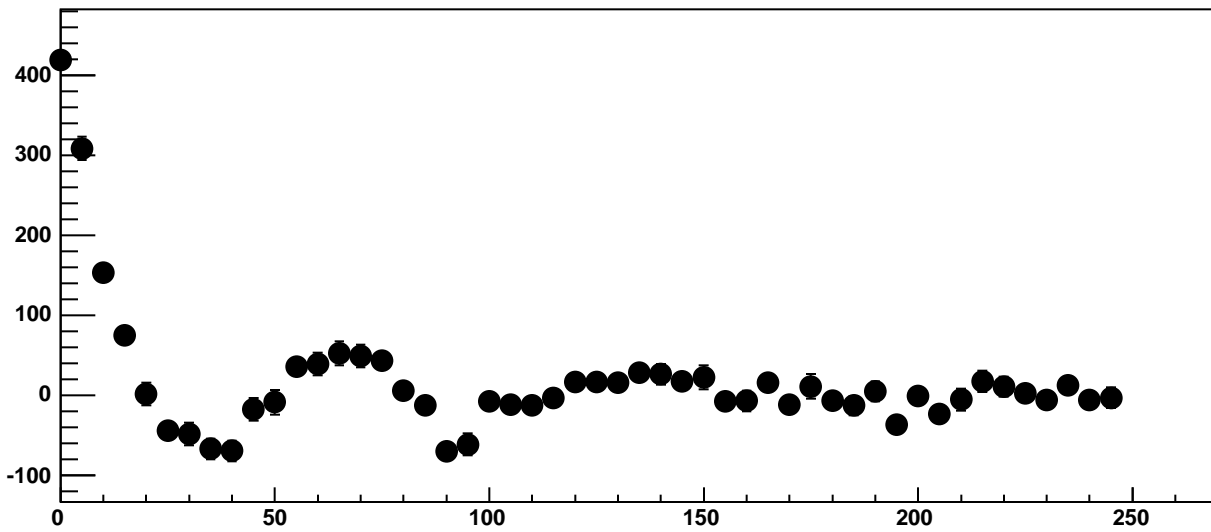


$\chi^2 / \text{ndf}$	341 / 41
p0	-766 ± 3.569
p1	91.04 ± 0.37
p2	-2.111e+08 ± 6.168e+06
p3	1.214e+07 ± 3.343e+05
p4	15.12 ± 0.12

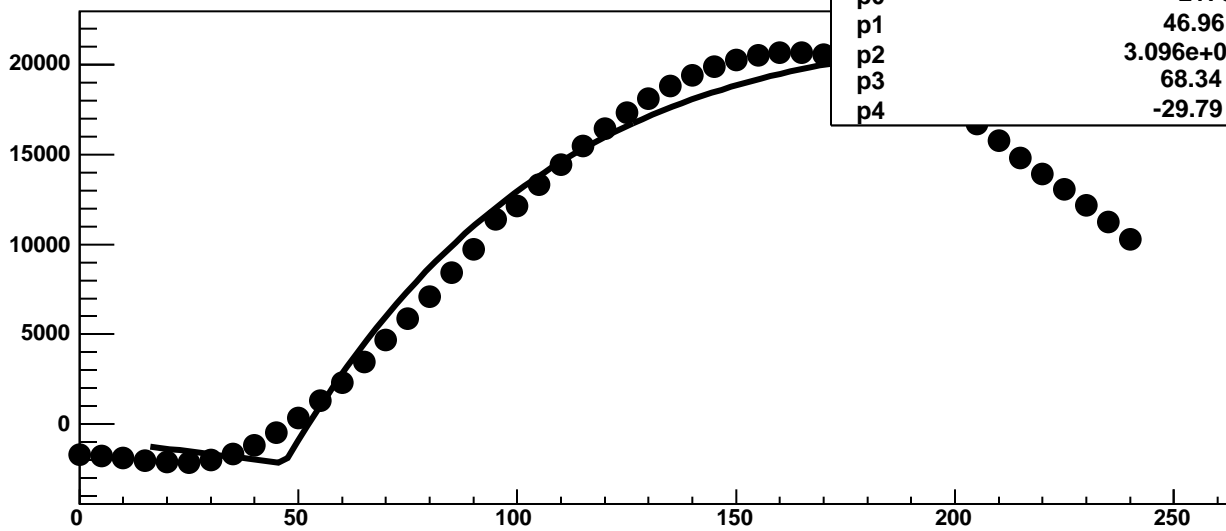
Chip 9, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



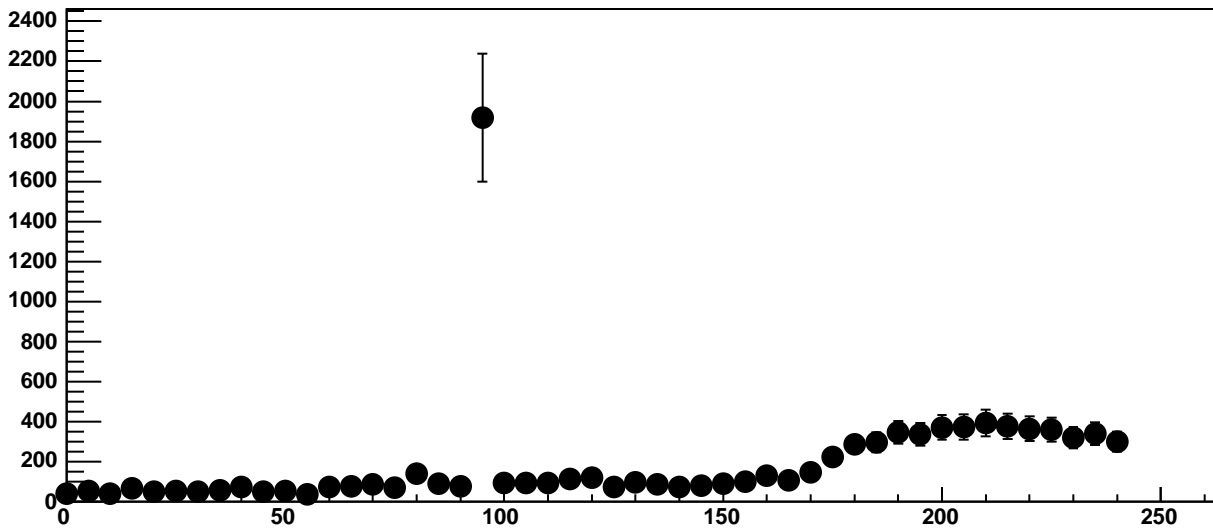
Chip 9, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold



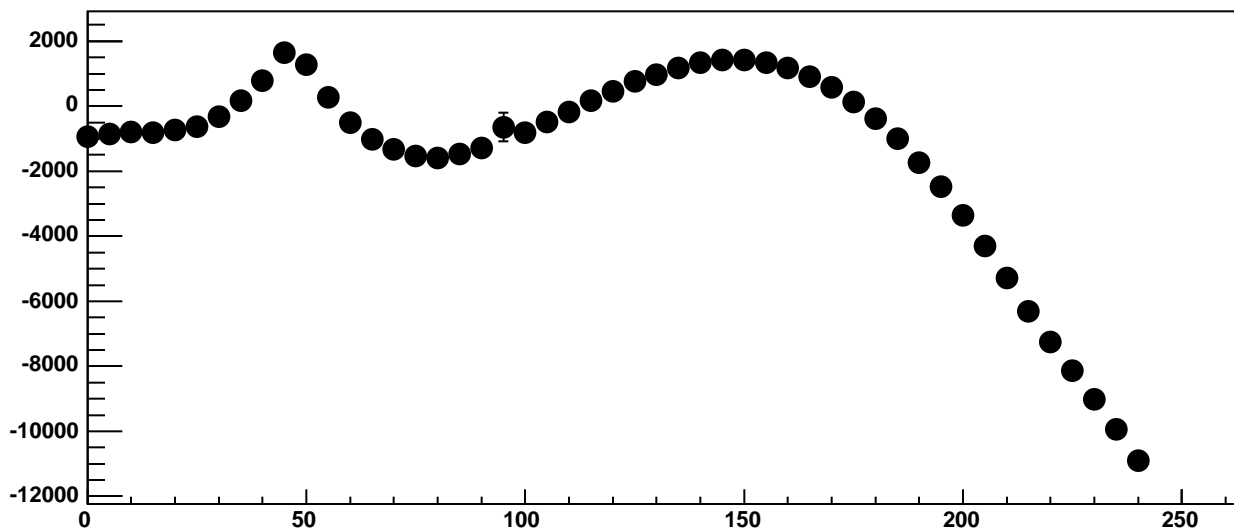
Chip 9, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold



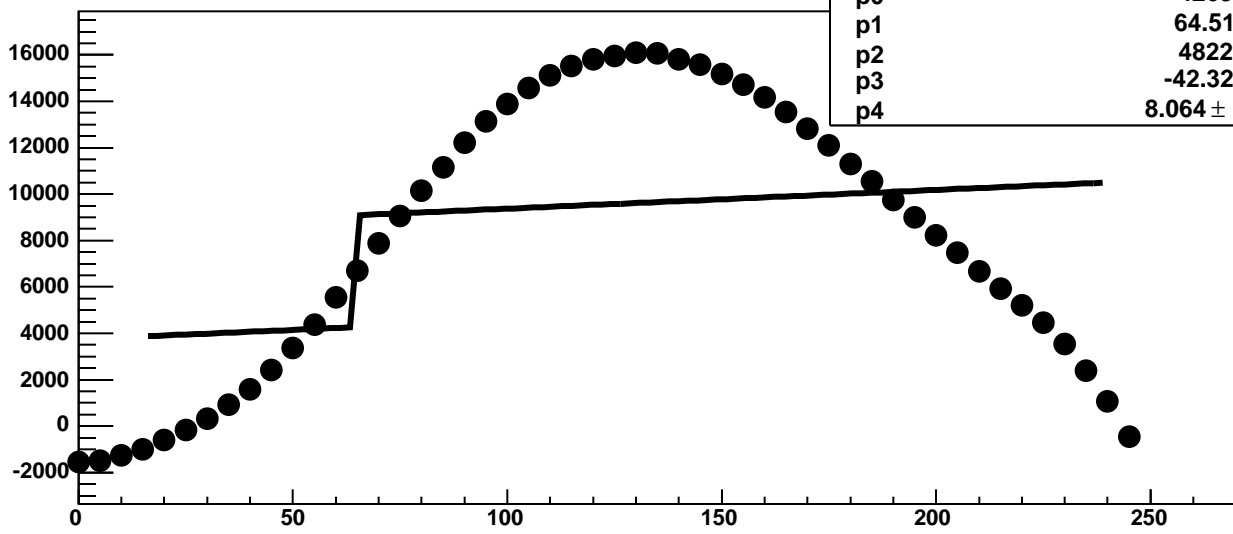
Chip 9, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



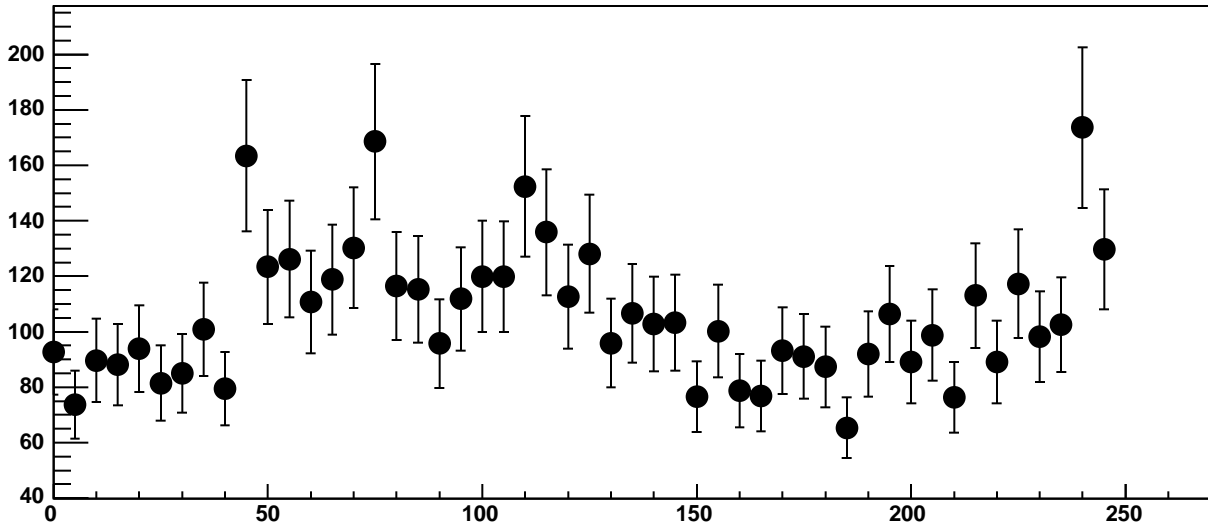
Chip 9, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



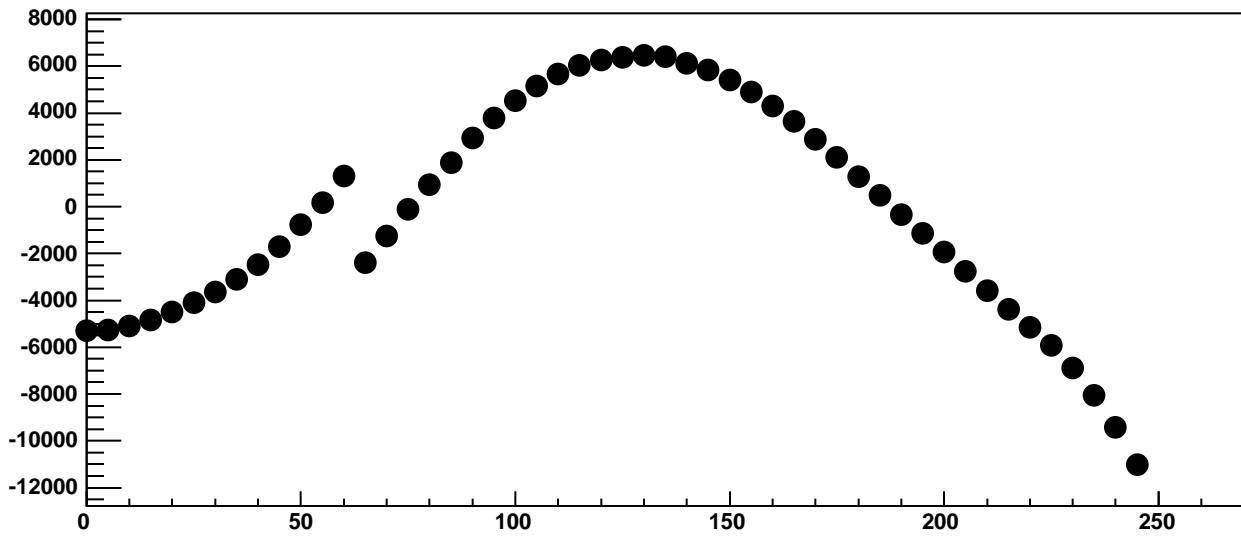
Chip 9, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold



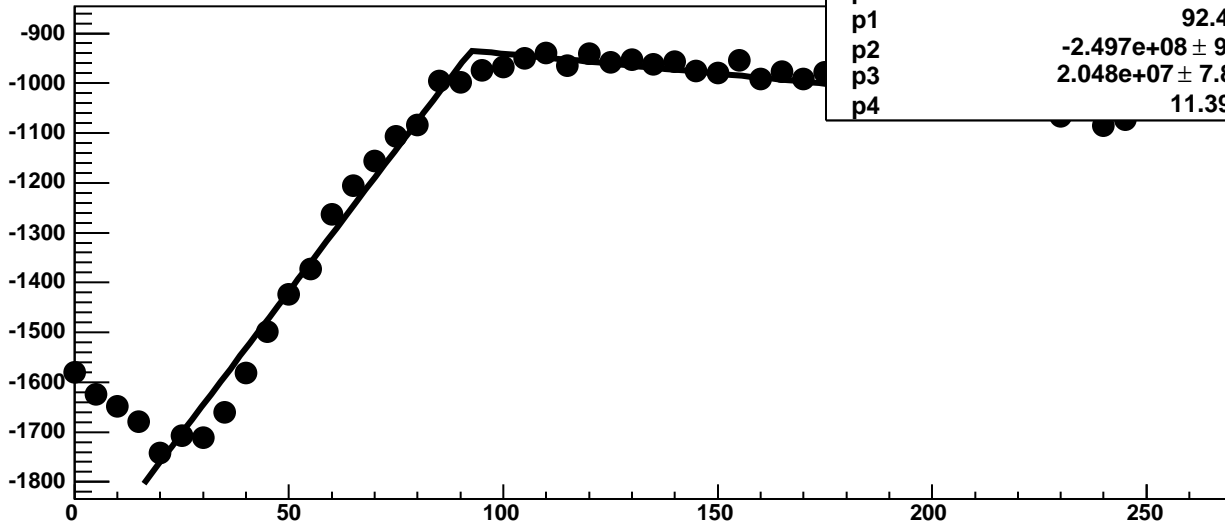
Chip 9, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold

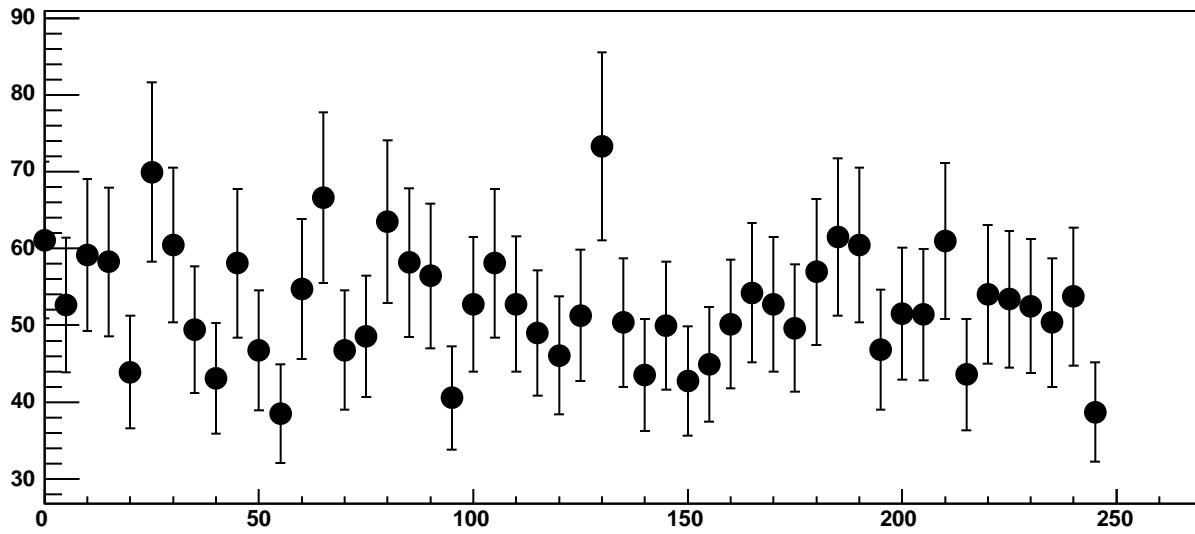


Chip 9, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

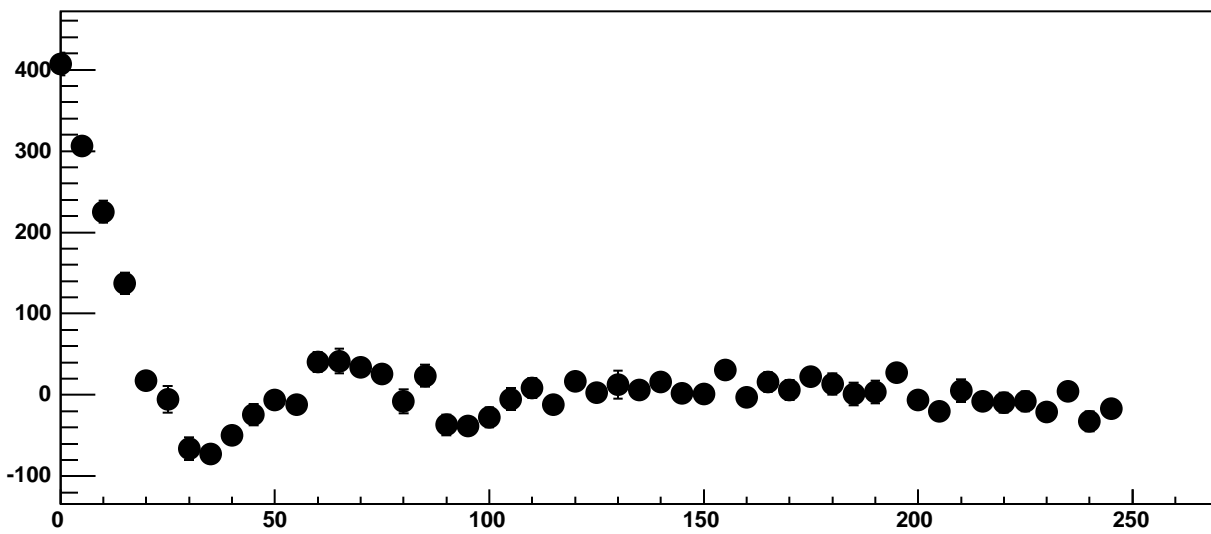


$\chi^2 / \text{ndf}$	314.6 / 41
p0	$-934.7 \pm 3.909$
p1	$92.4 \pm 0.617$
p2	$-2.497\text{e}+08 \pm 9.99\text{e}+06$
p3	$2.048\text{e}+07 \pm 7.887\text{e}+05$
p4	$11.39 \pm 0.136$

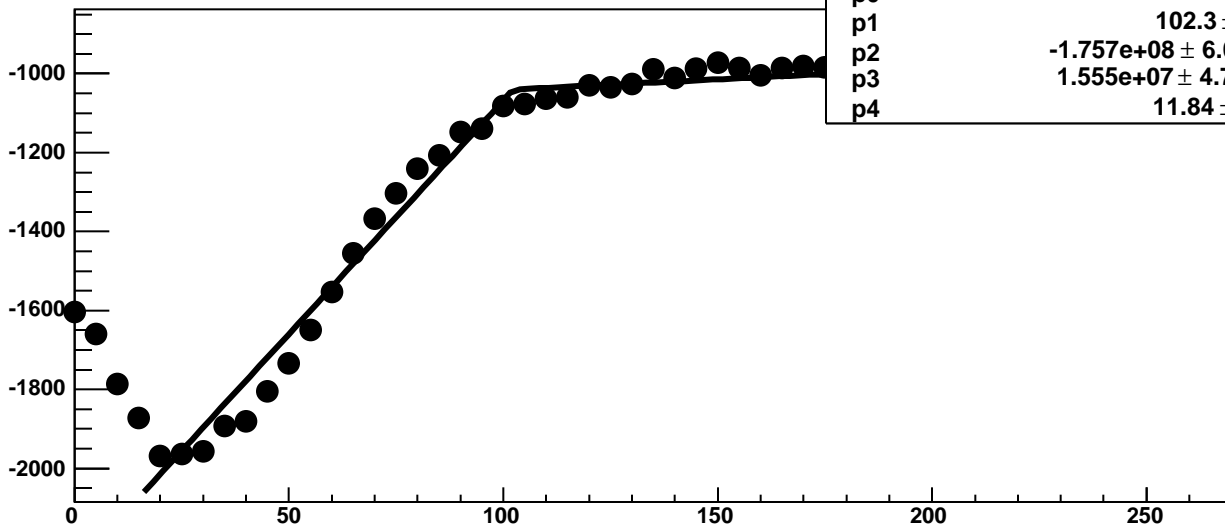
Chip 9, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

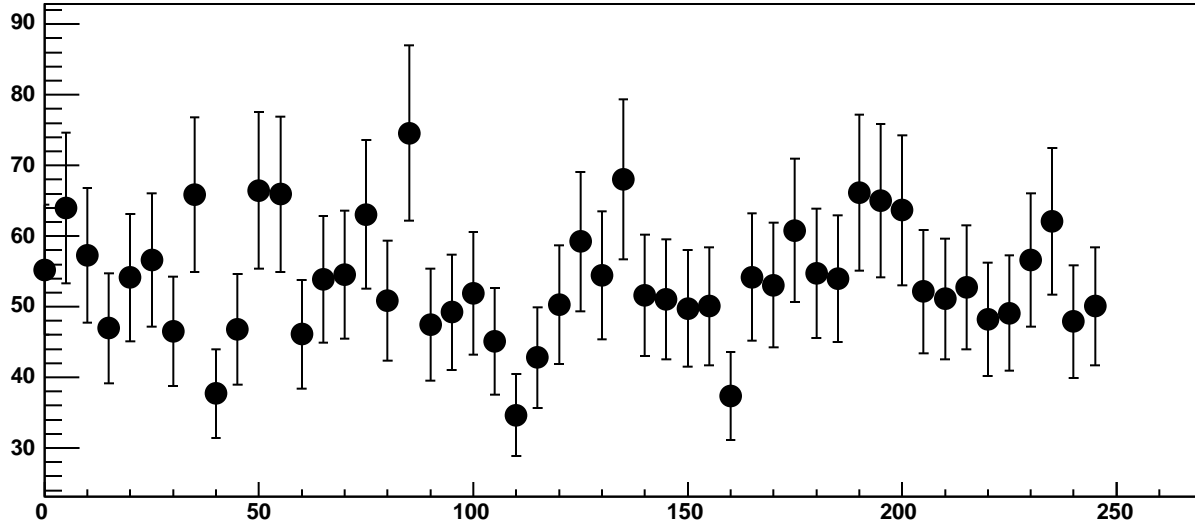


Chip 9, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

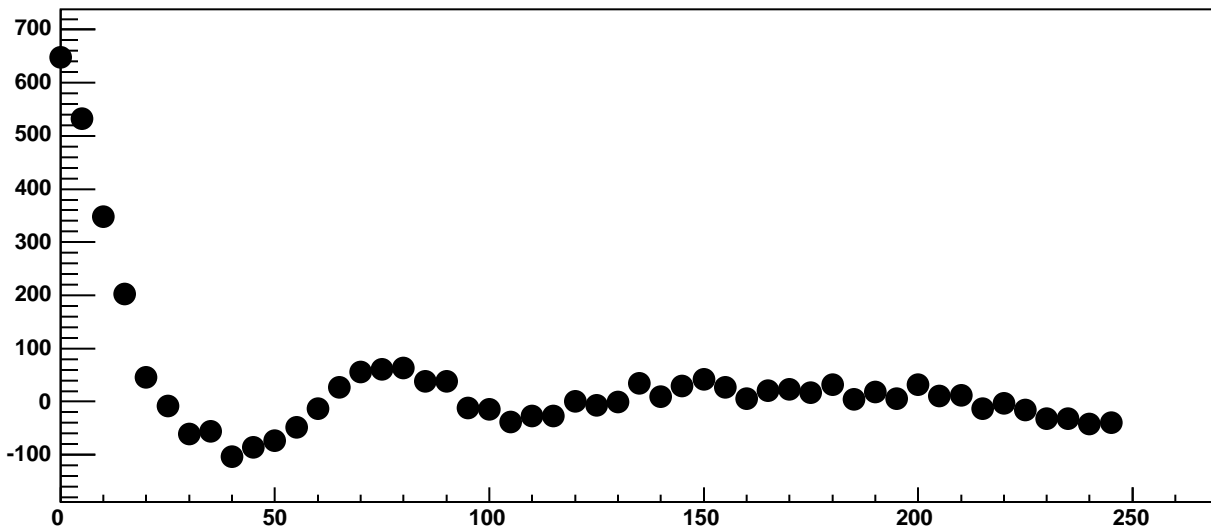


$\chi^2 / \text{ndf}$	860.1 / 41
p0	-1040 ± 4.34
p1	102.3 ± 0.6212
p2	-1.757e+08 ± 6.054e+06
p3	1.555e+07 ± 4.744e+05
p4	11.84 ± 0.1075

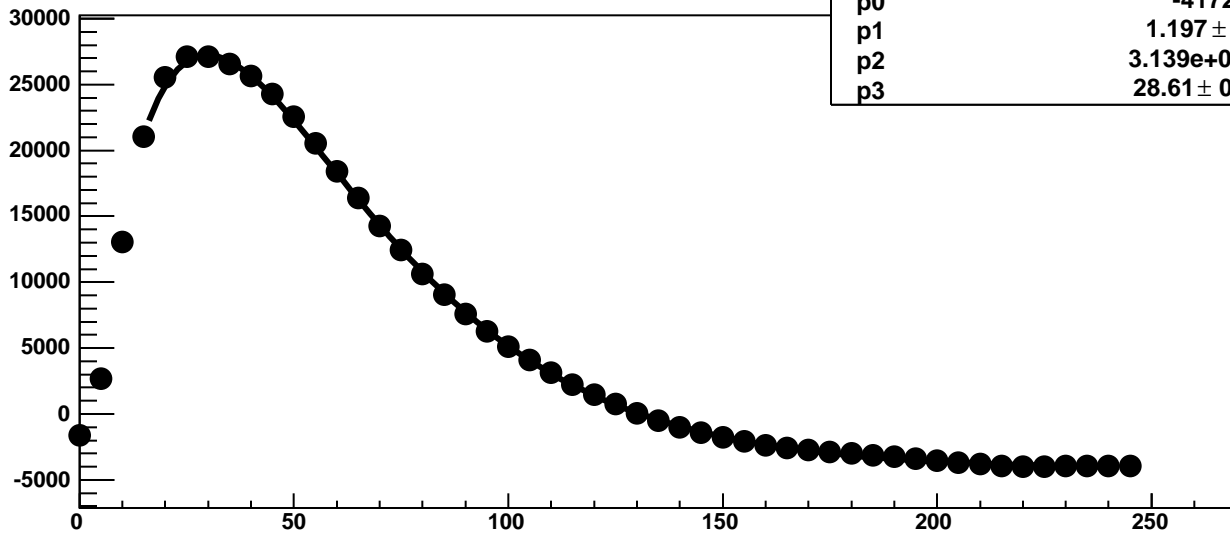
Chip 9, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

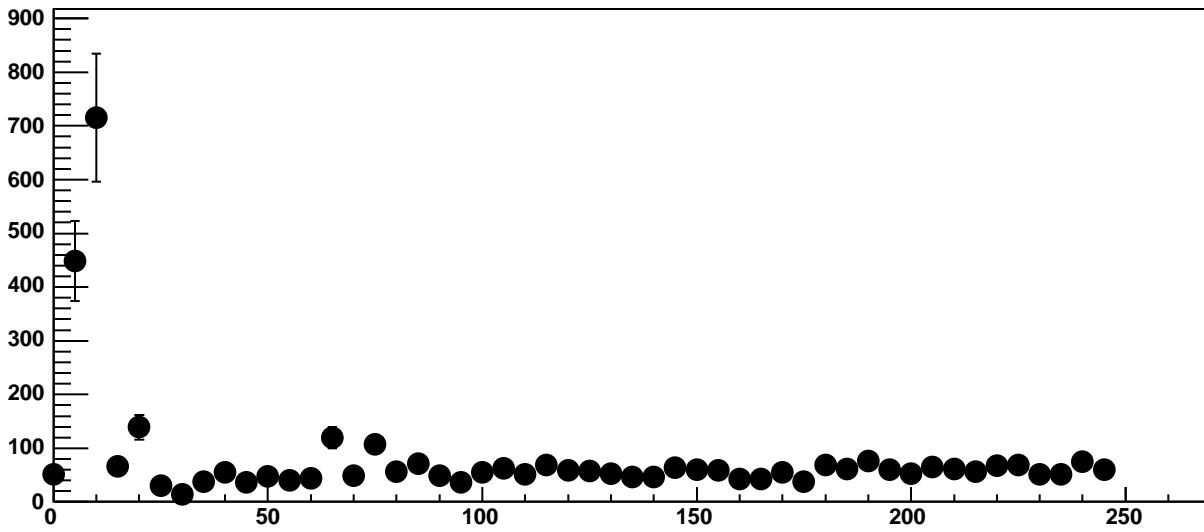


Chip 9, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

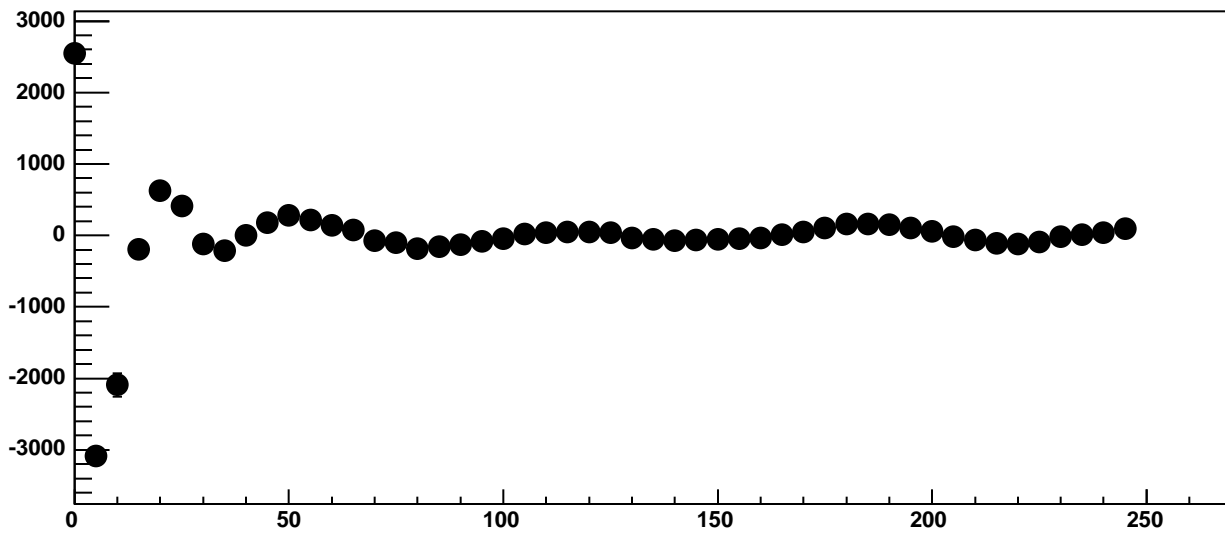


$\chi^2 / \text{ndf}$	9162 / 42
p0	-4172 ± 3.572
p1	1.197 ± 0.01638
p2	3.139e+04 ± 4.11
p3	28.61 ± 0.009499

Chip 9, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

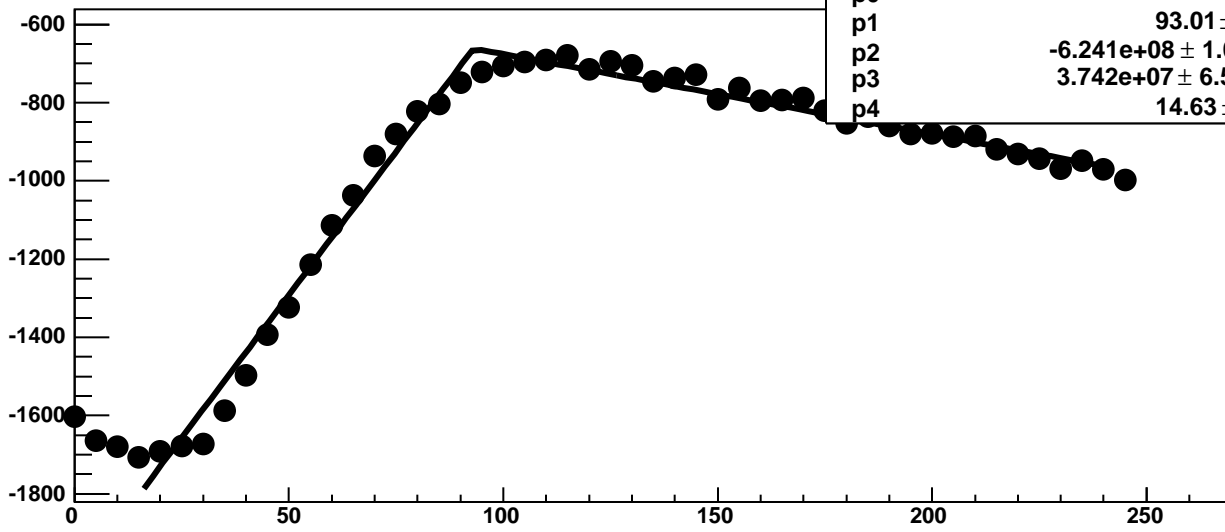


Chip 9, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold



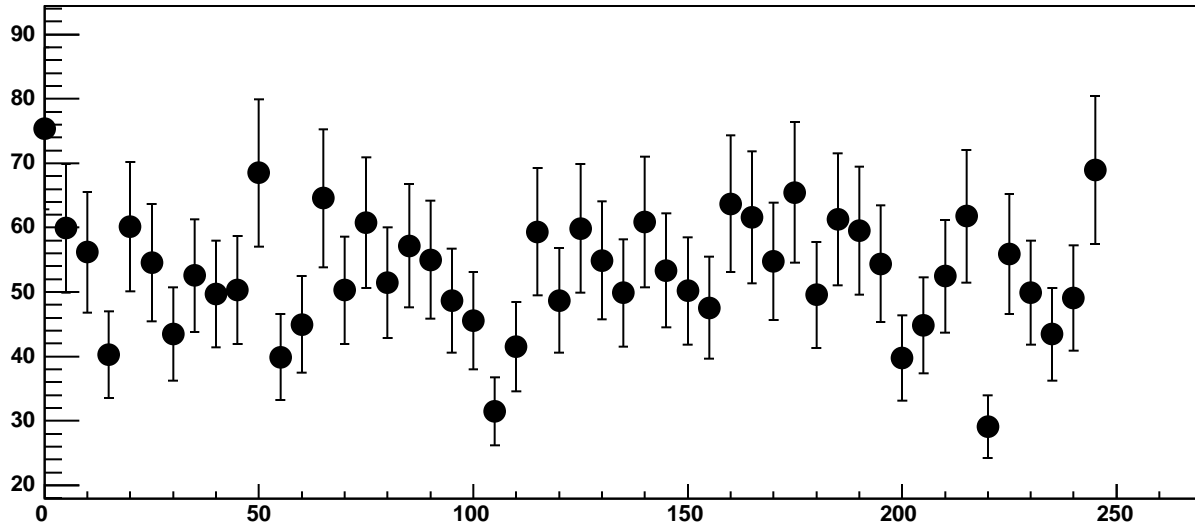


Chip 9, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

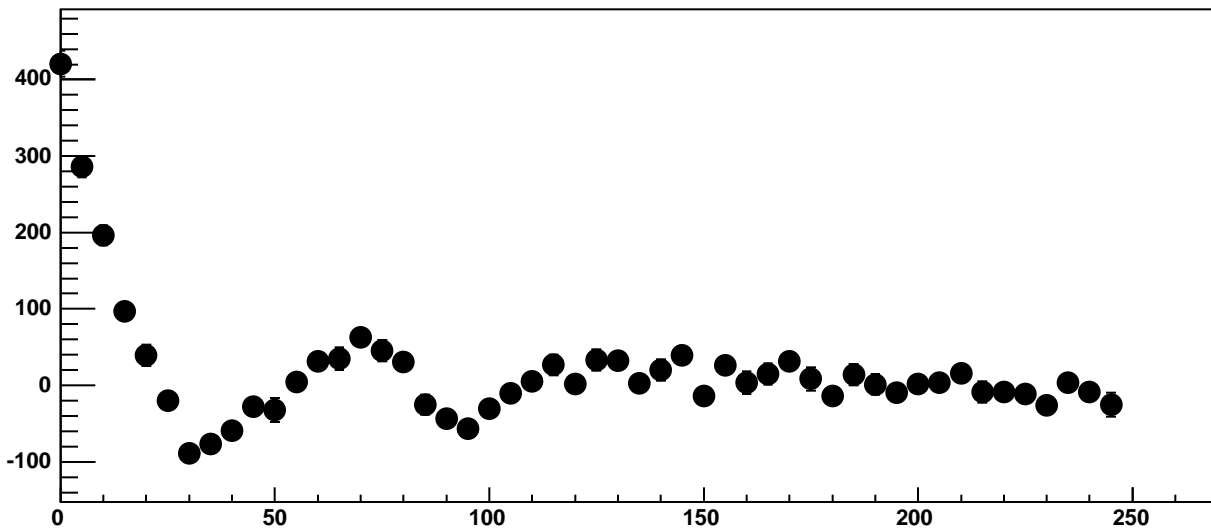


$\chi^2 / \text{ndf}$	449.5 / 41
p0	-661.8 ± 3.398
p1	93.01 ± 0.4066
p2	-6.241e+08 ± 1.036e+07
p3	3.742e+07 ± 6.578e+05
p4	14.63 ± 0.1133

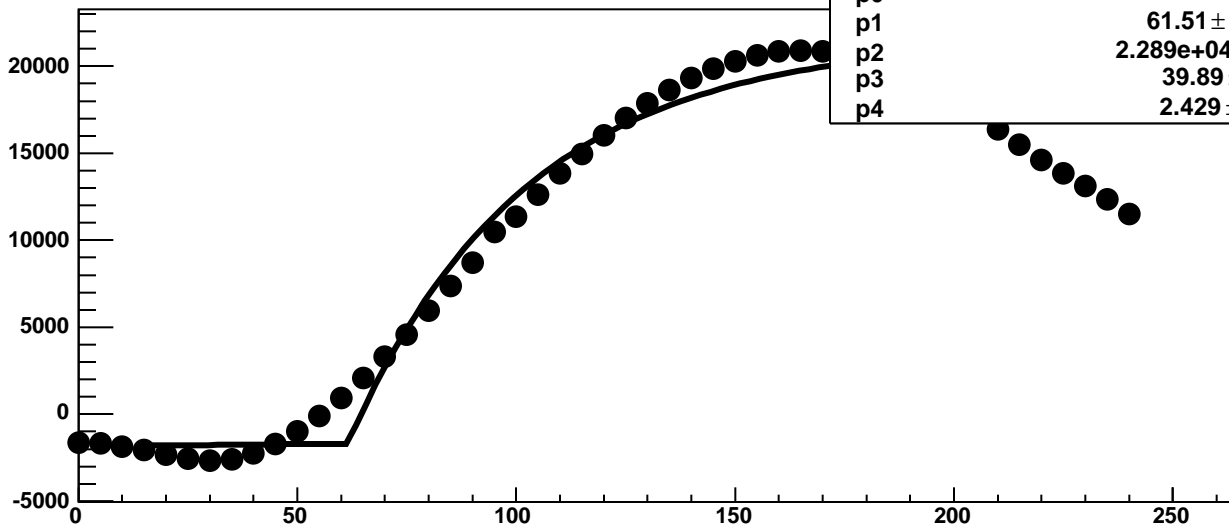
Chip 9, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold

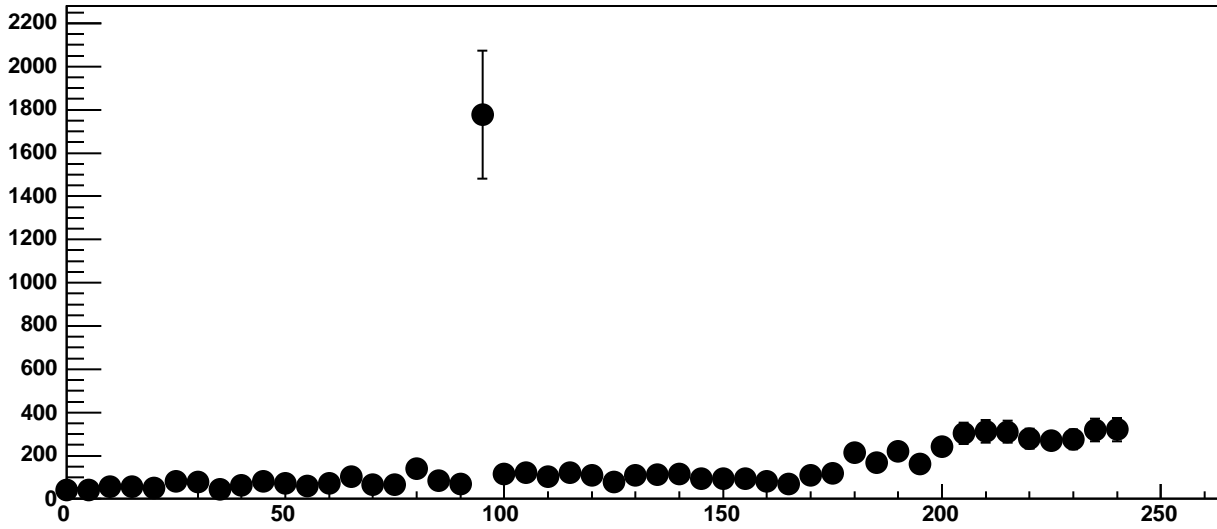


Chip 9, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

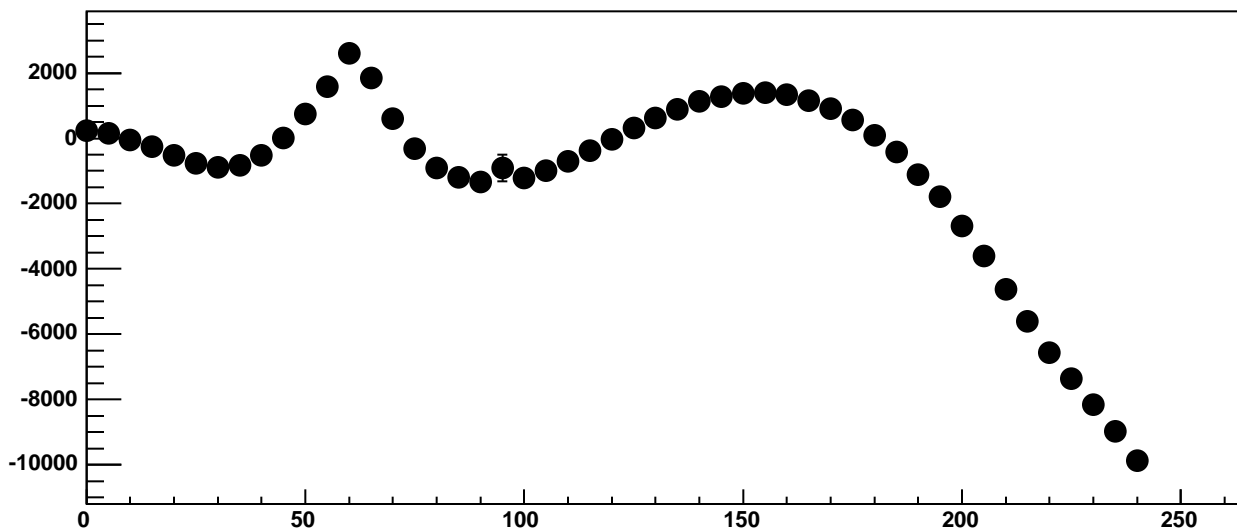


$\chi^2 / \text{ndf}$	1.974e+05 / 41
p0	-1690 ± 7.985
p1	61.51 ± 0.03085
p2	2.289e+04 ± 43.13
p3	39.89 ± 0.0911
p4	2.429 ± 0.2512

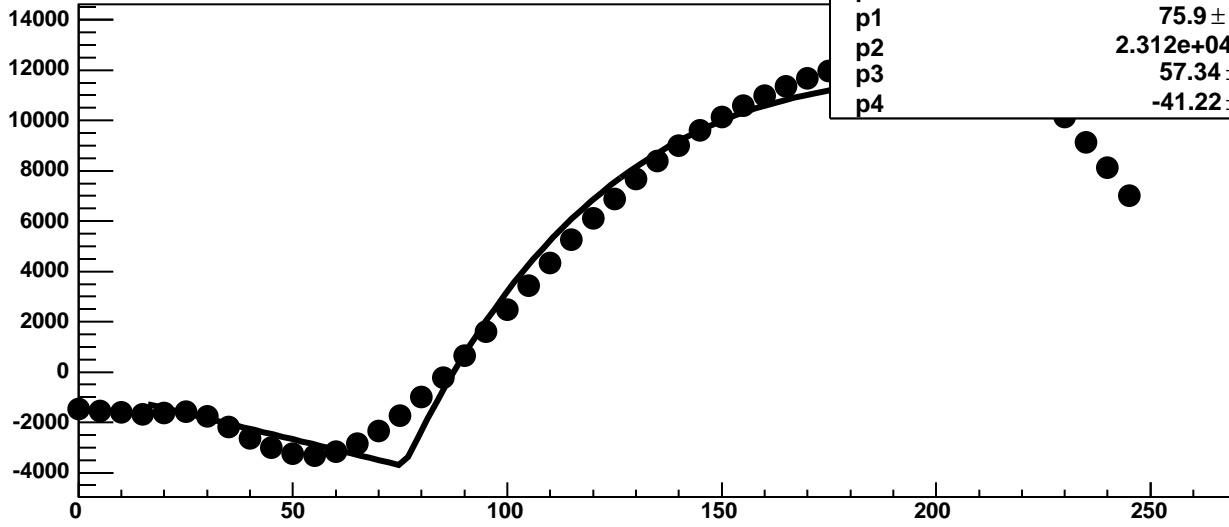
Chip 9, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold



Chip 9, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

6.264e+04 / 41

p0

-3734 ± 9.683

p1

75.9 ± 0.04814

p2

2.312e+04 ± 62.58

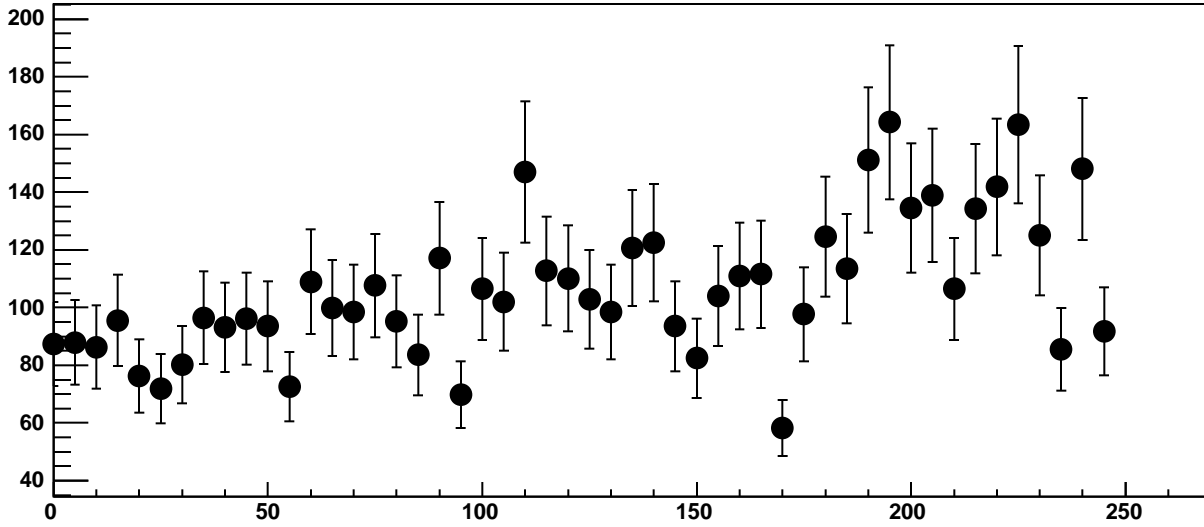
p3

57.34 ± 0.1662

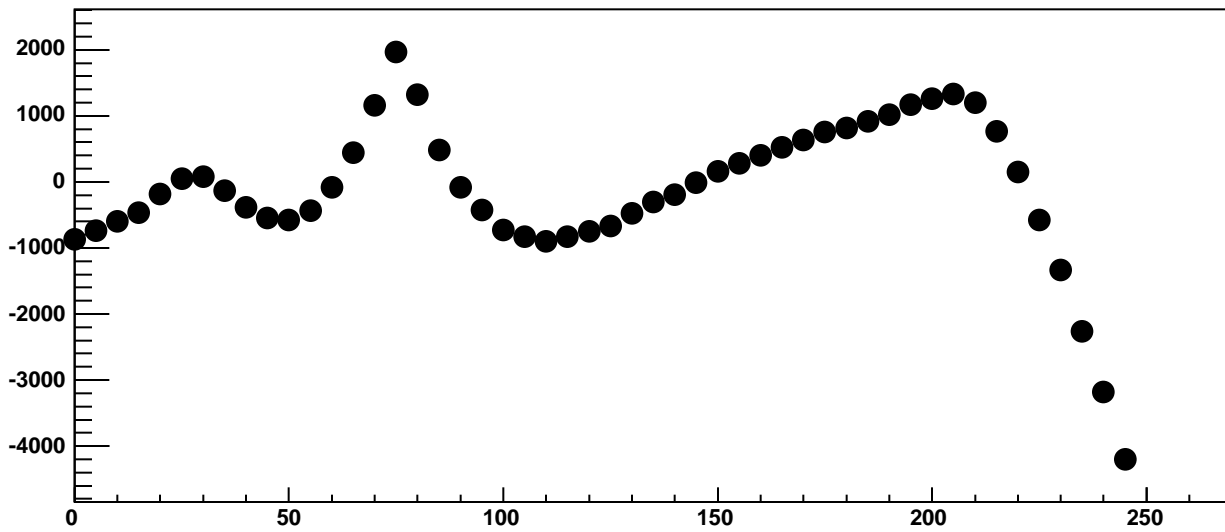
p4

-41.22 ± 0.2718

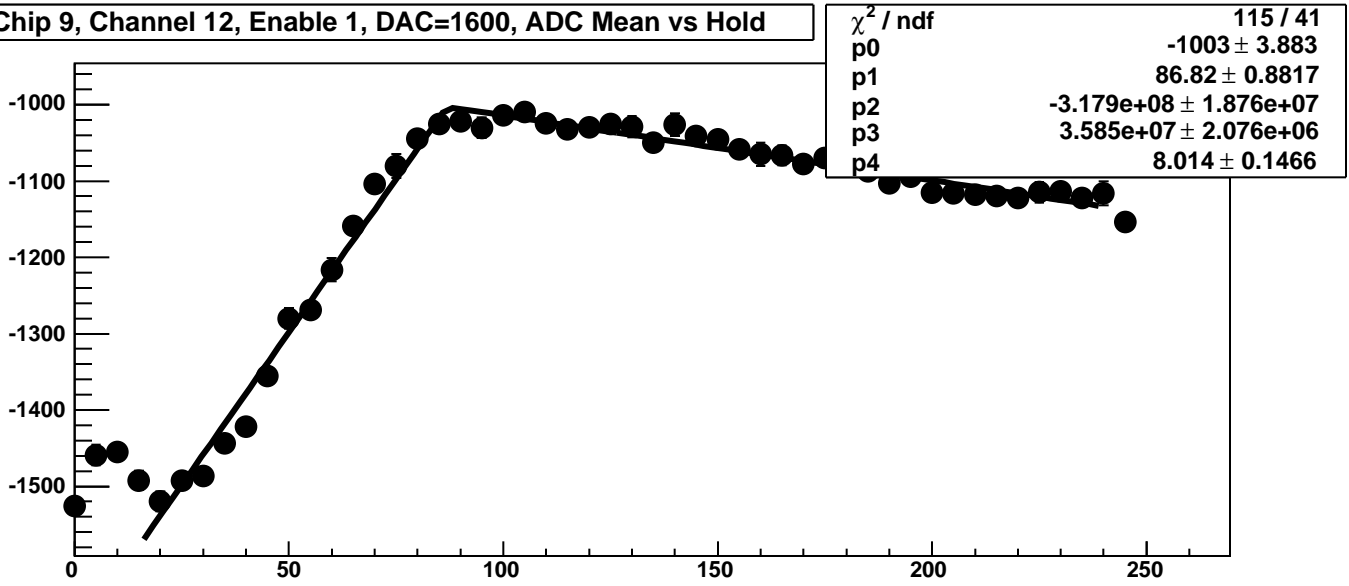
Chip 9, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold



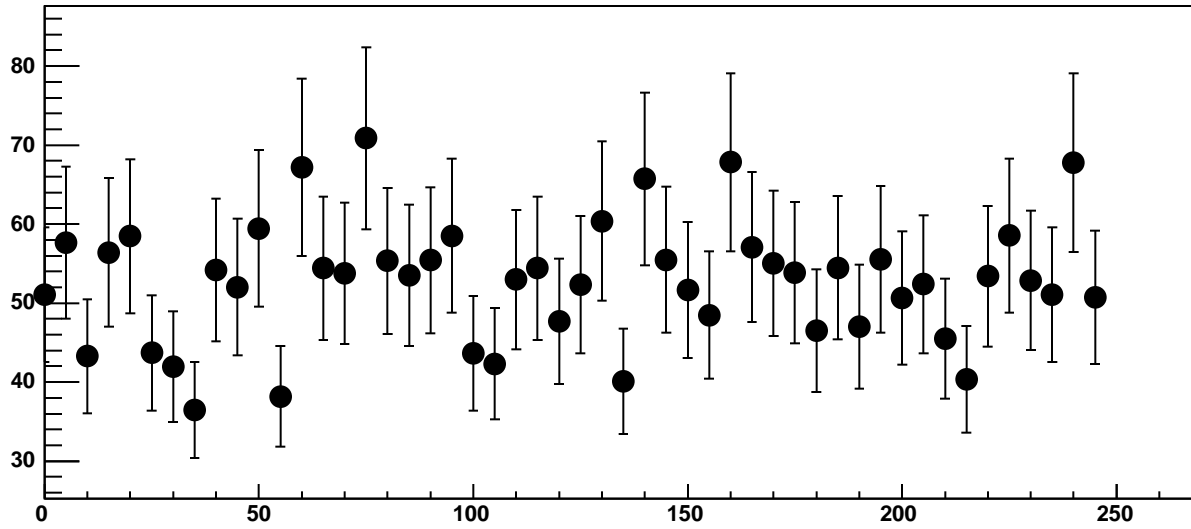
Chip 9, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold



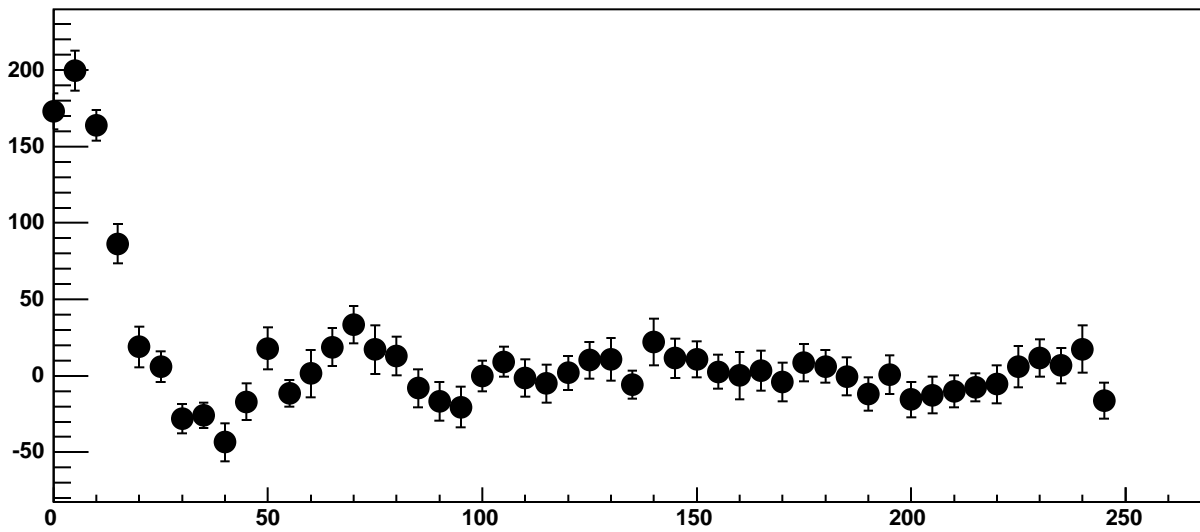
Chip 9, Channel 12, Enable 1, DAC=1600, ADC Mean vs Hold



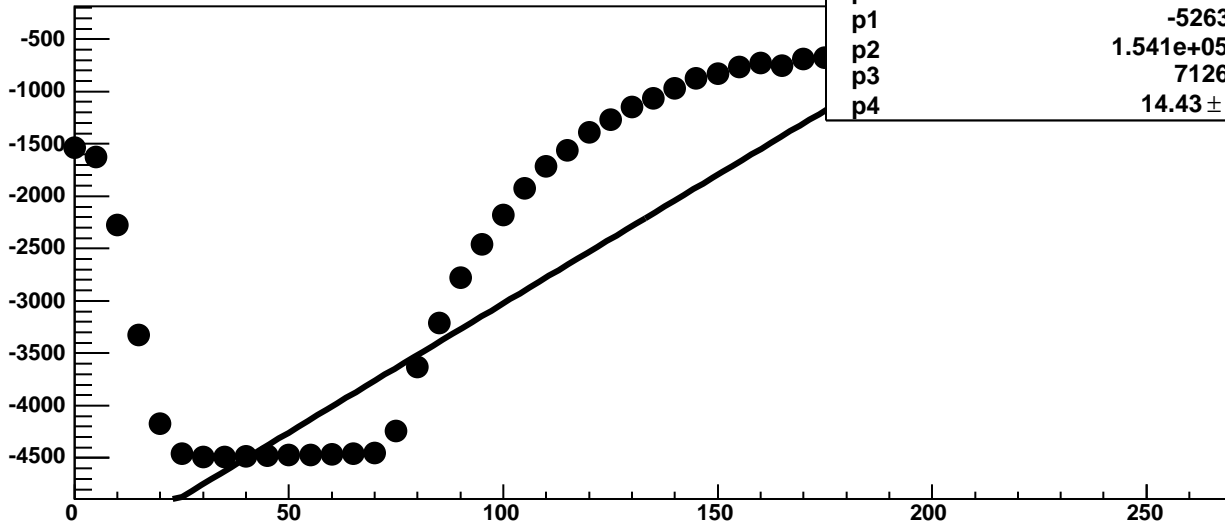
Chip 9, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold

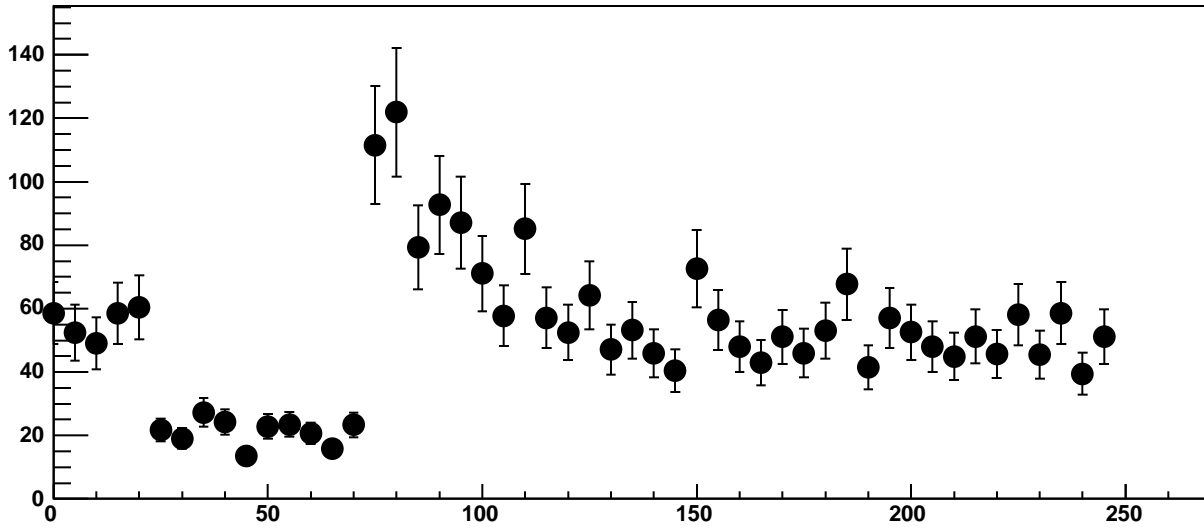


Chip 9, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

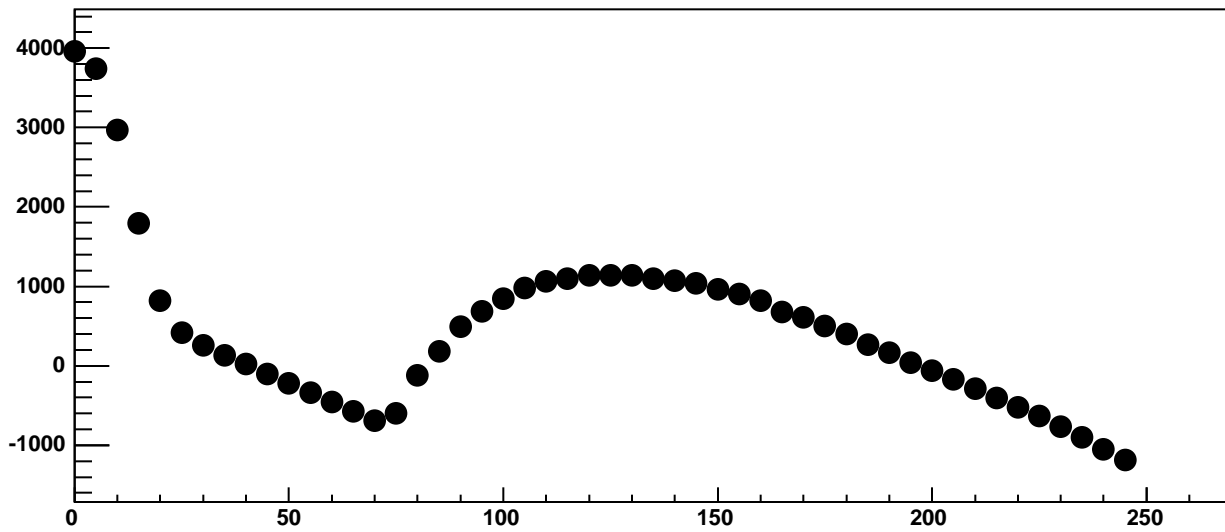


$\chi^2 / \text{ndf}$	2.229e+05 / 41
p0	-1.619e+05 $\pm$ 2346
p1	-5263 $\pm$ 65.92
p2	1.541e+05 $\pm$ 2976
p3	7126 $\pm$ 55.36
p4	14.43 $\pm$ 0.09179

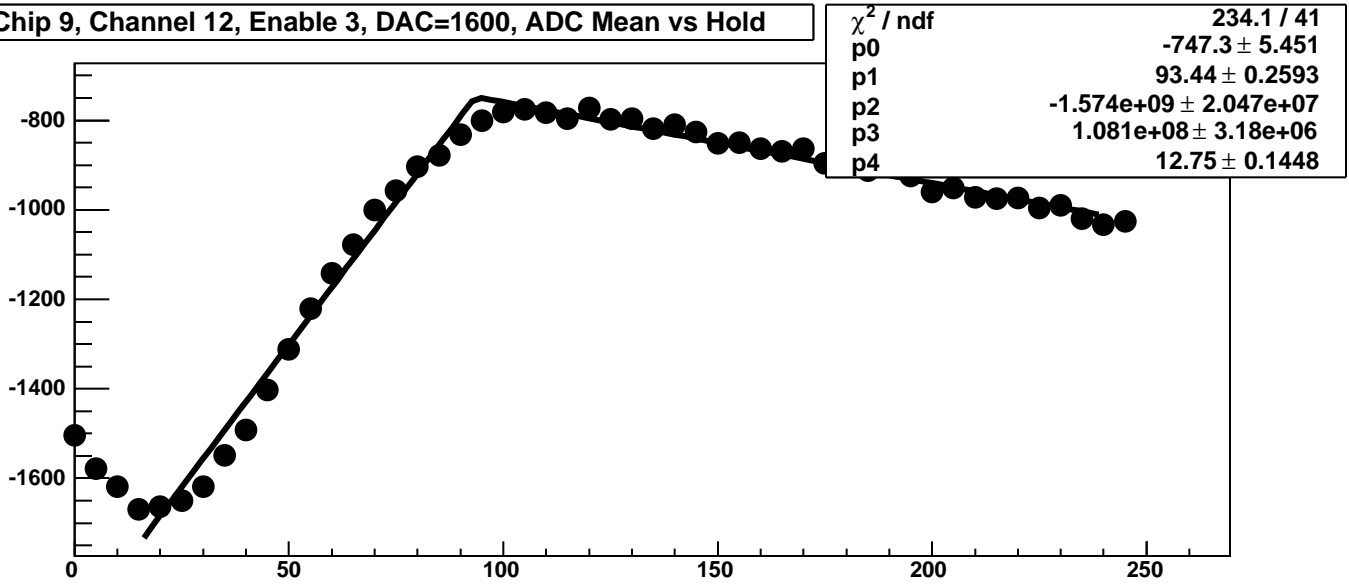
Chip 9, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



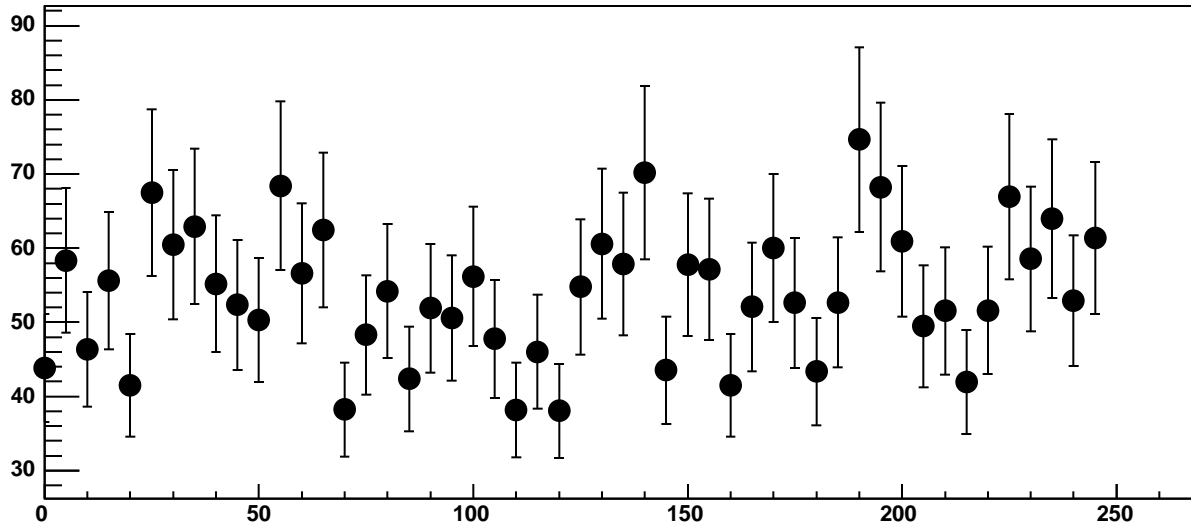
Chip 9, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold



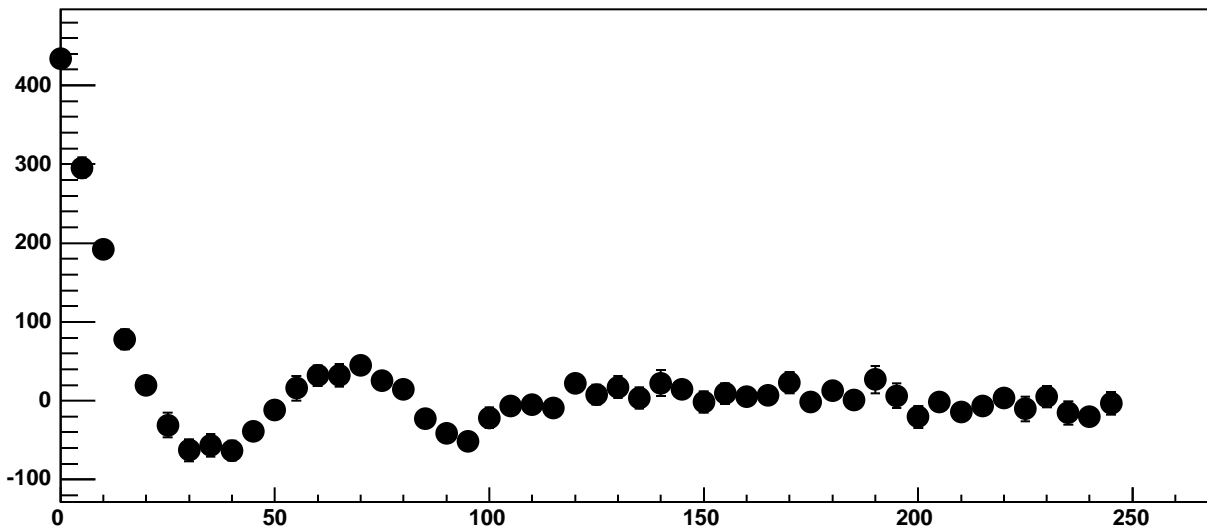
Chip 9, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold



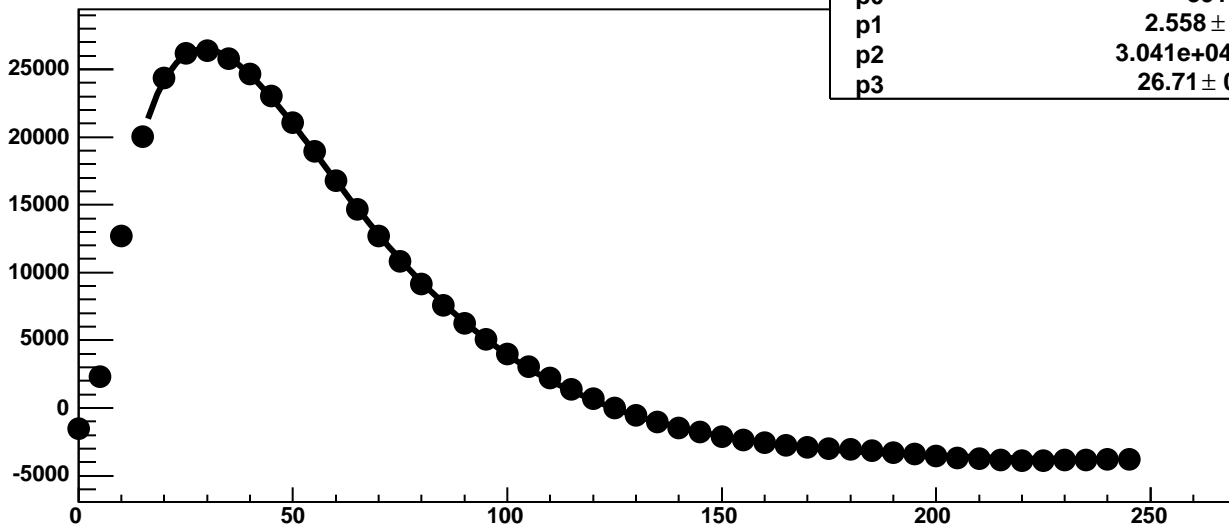
Chip 9, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

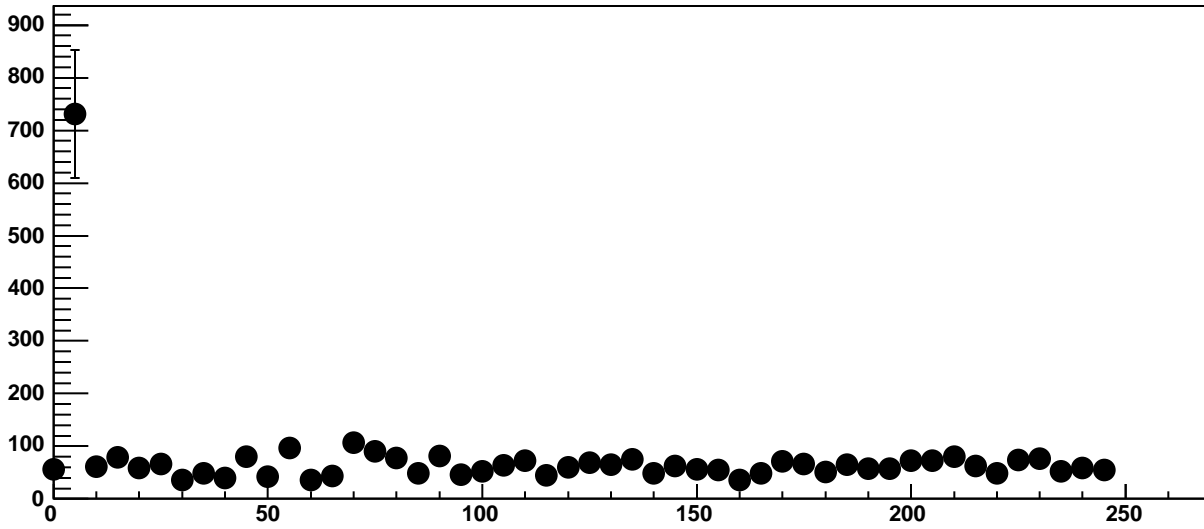


Chip 9, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold

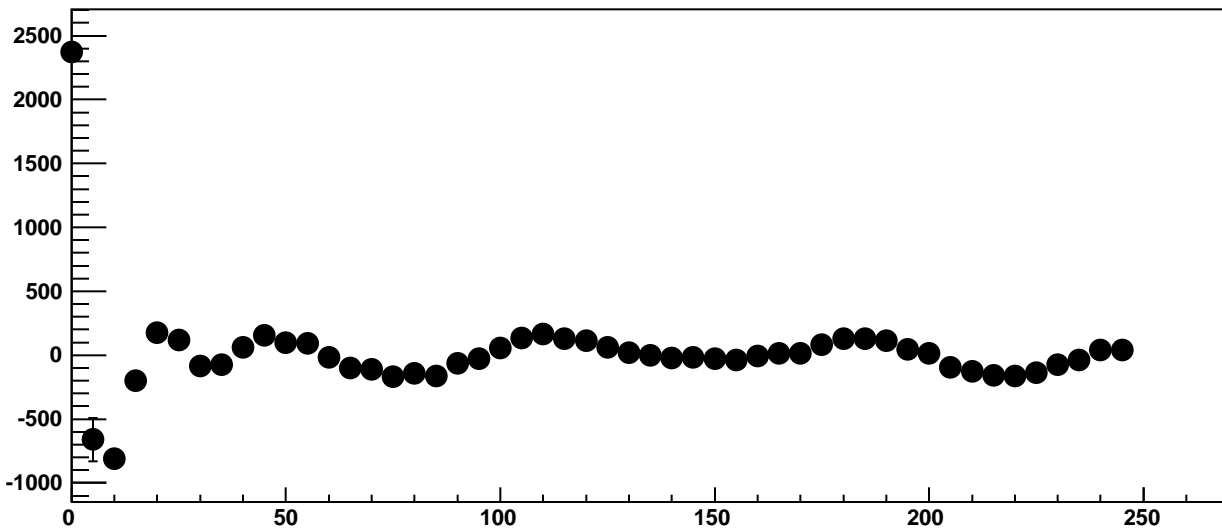


$\chi^2 / \text{ndf}$	2504 / 42
p0	-3910 ± 3.52
p1	2.558 ± 0.01639
p2	3.041e+04 ± 5.234
p3	26.71 ± 0.009751

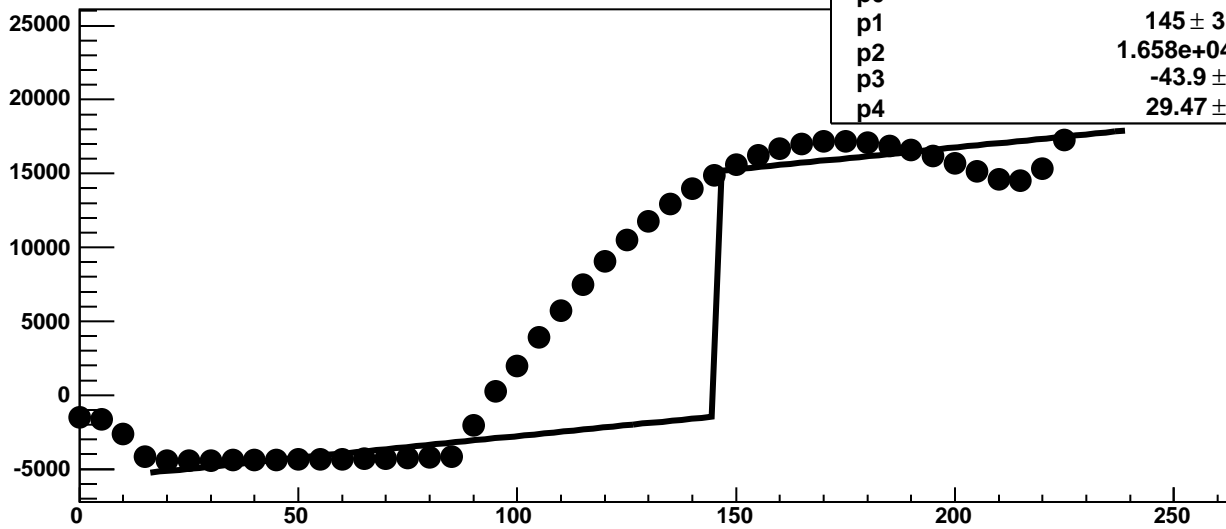
Chip 9, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold

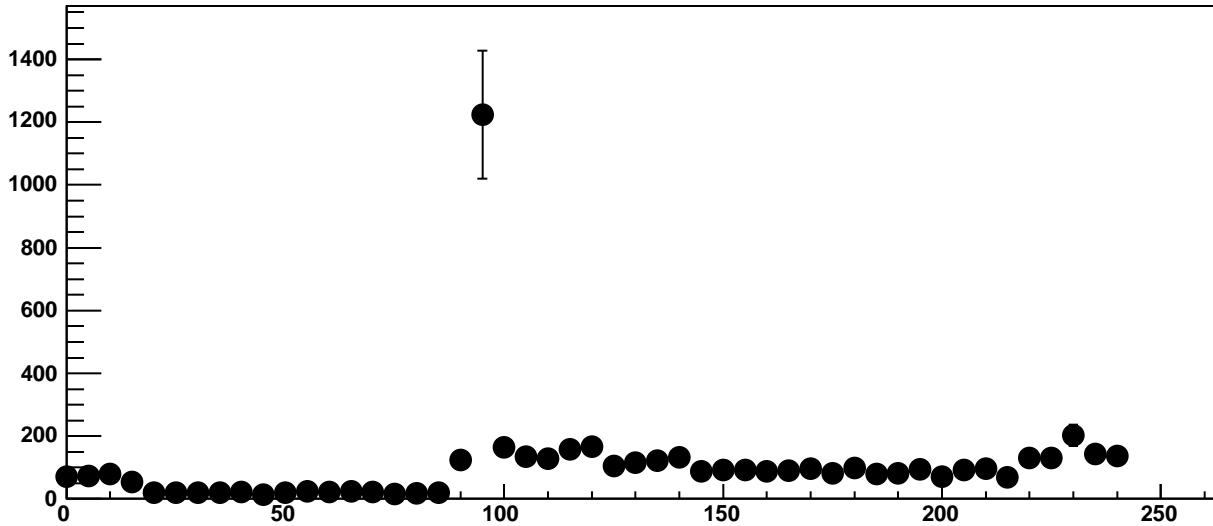


Chip 9, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

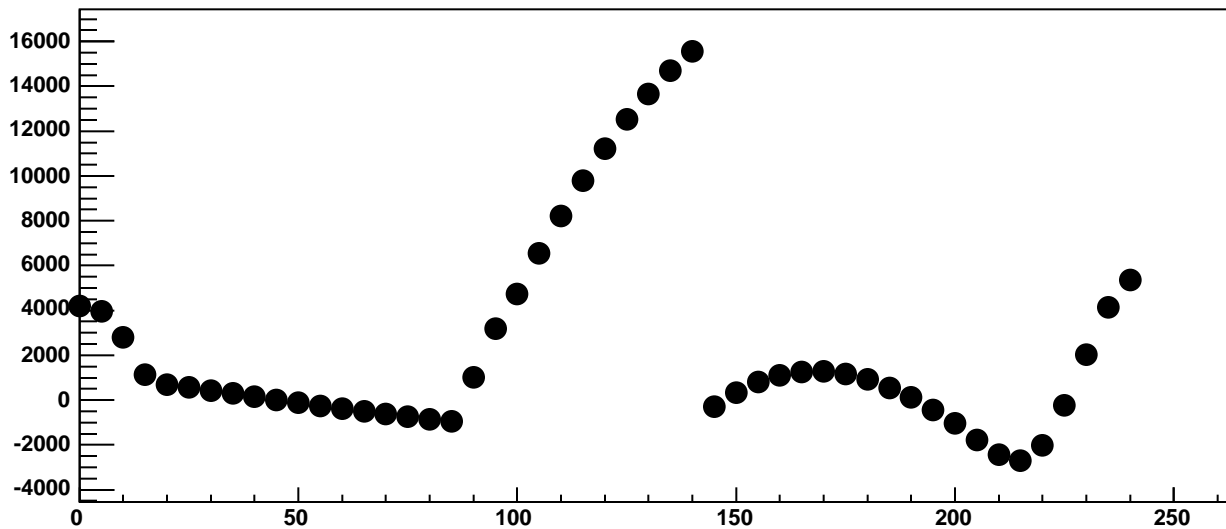


$\chi^2 / \text{ndf}$	1.712e+06 / 41
p0	-1444 ± 2.684
p1	145 ± 3.008e-05
p2	1.658e+04 ± 9.264
p3	-43.9 ± 0.00055
p4	29.47 ± 0.02977

Chip 9, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

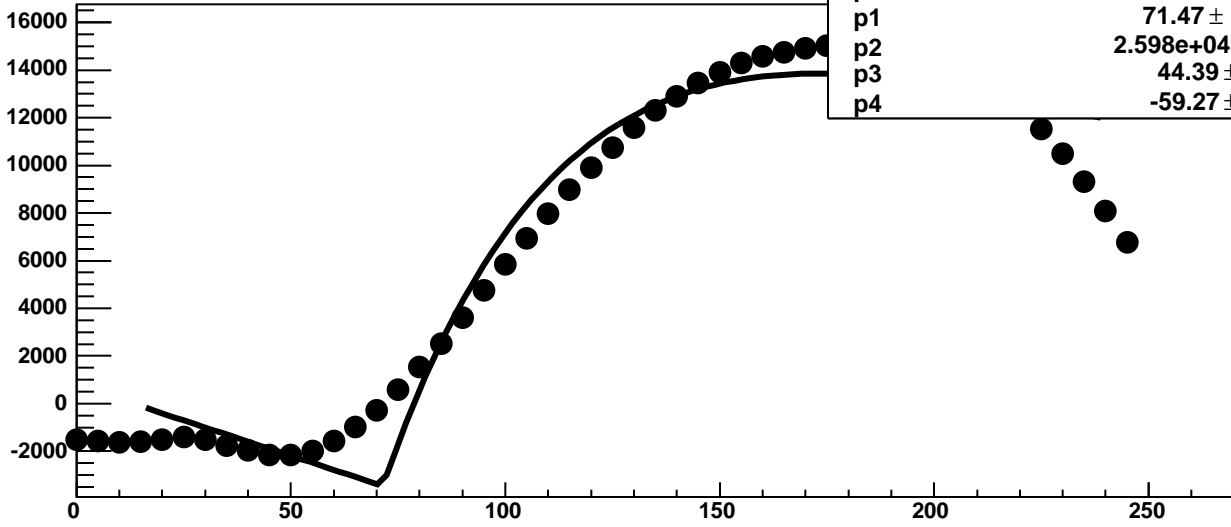


Chip 9, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



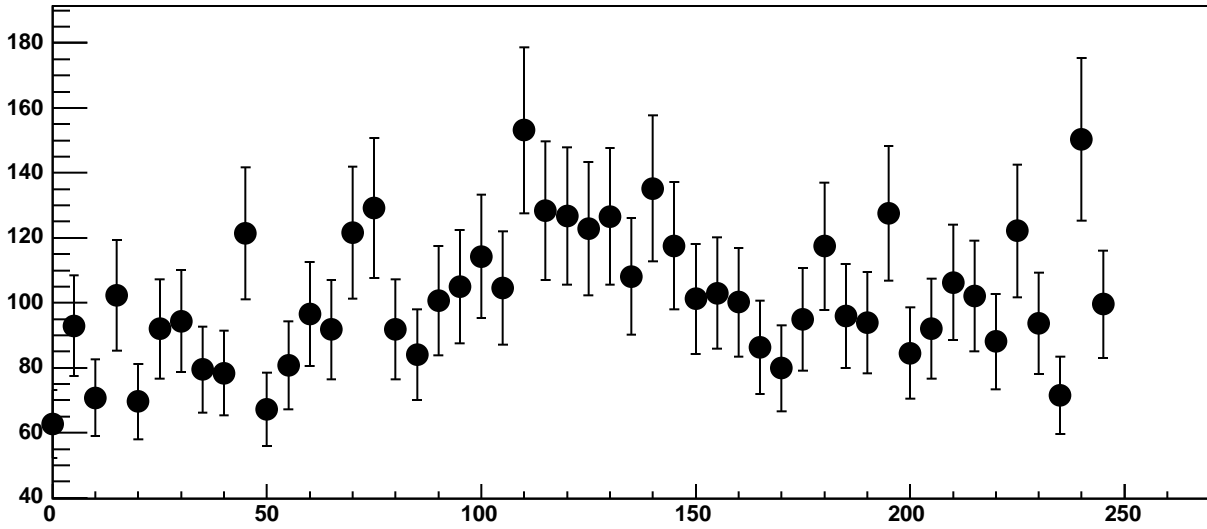


Chip 9, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

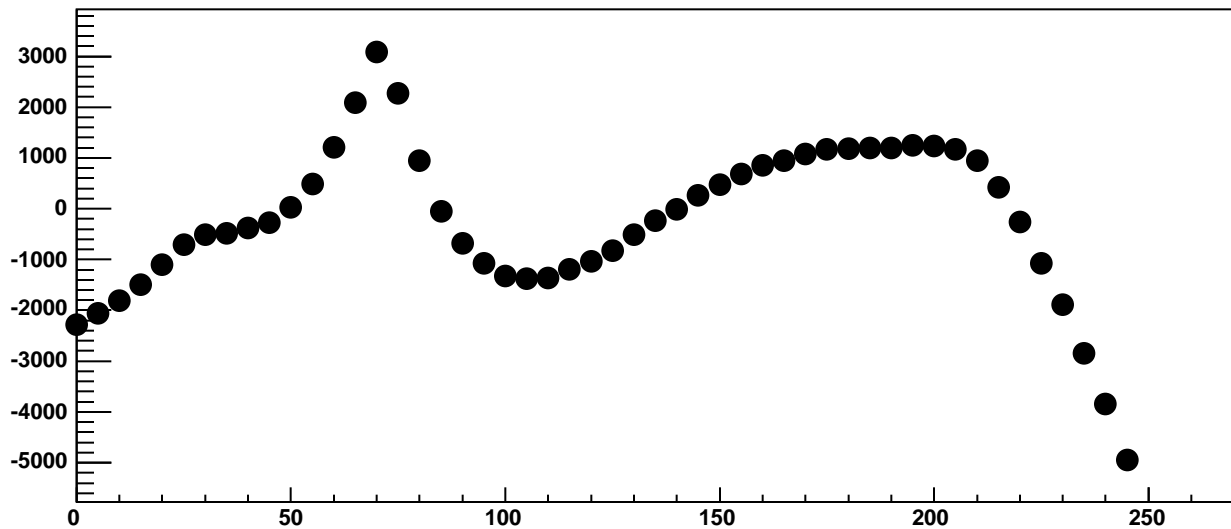


$\chi^2 / \text{ndf}$	1.421e+05 / 41
p0	-3462 ± 8.571
p1	71.47 ± 0.03594
p2	2.598e+04 ± 50.28
p3	44.39 ± 0.1012
p4	-59.27 ± 0.2493

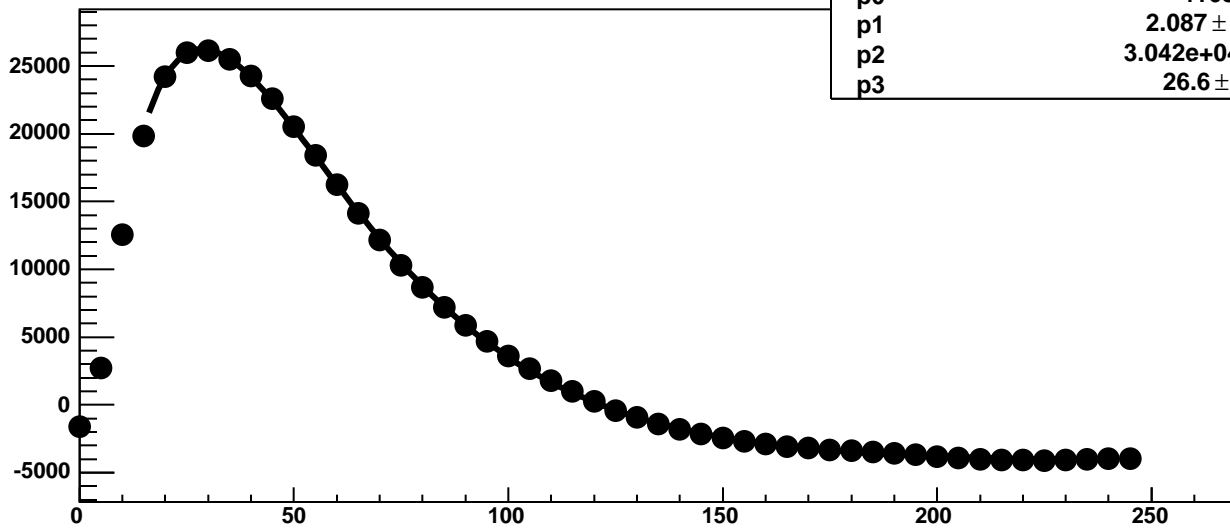
Chip 9, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold

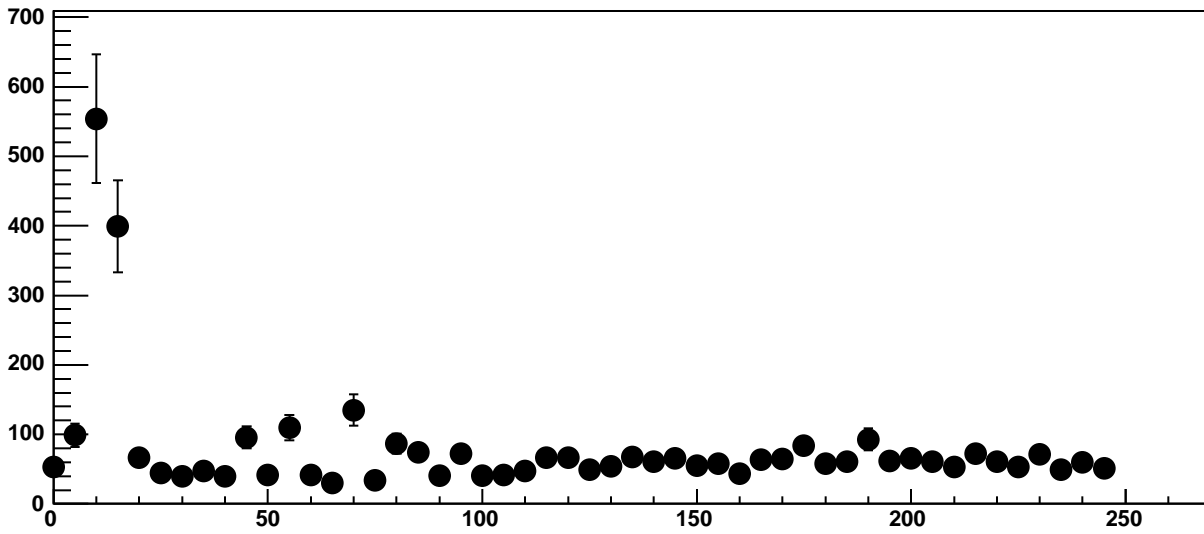


Chip 9, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold

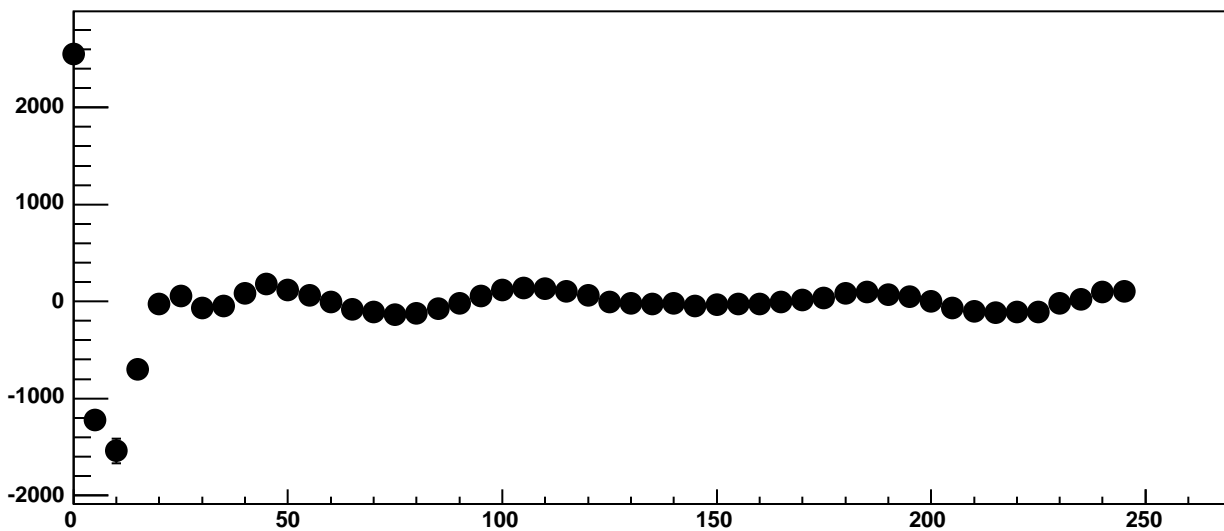


$\chi^2 / \text{ndf}$	2130 / 42
p0	-4168 ± 3.653
p1	2.087 ± 0.02415
p2	3.042e+04 ± 5.62
p3	26.6 ± 0.01148

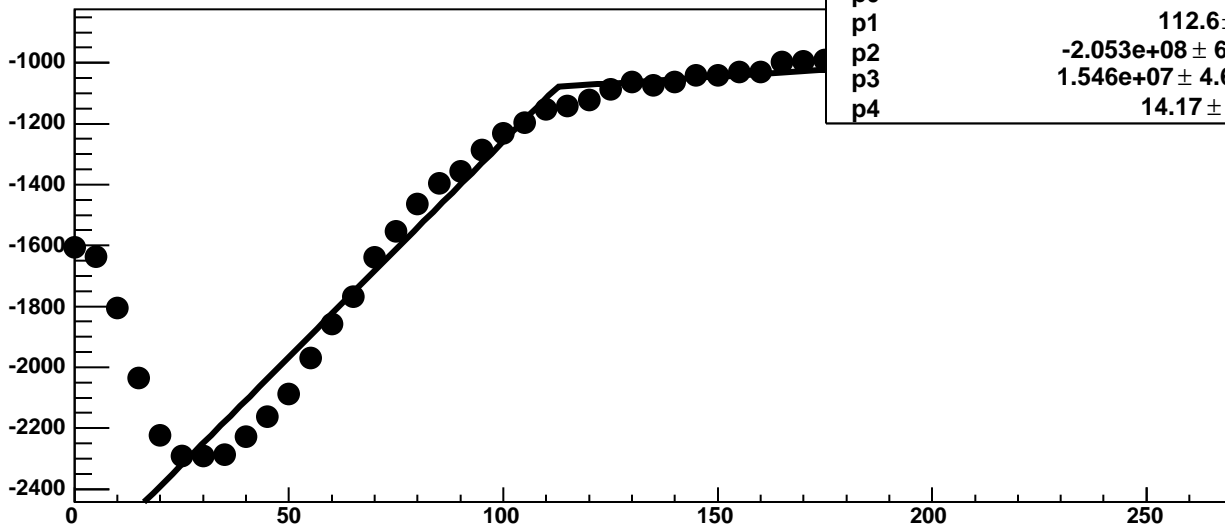
Chip 9, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

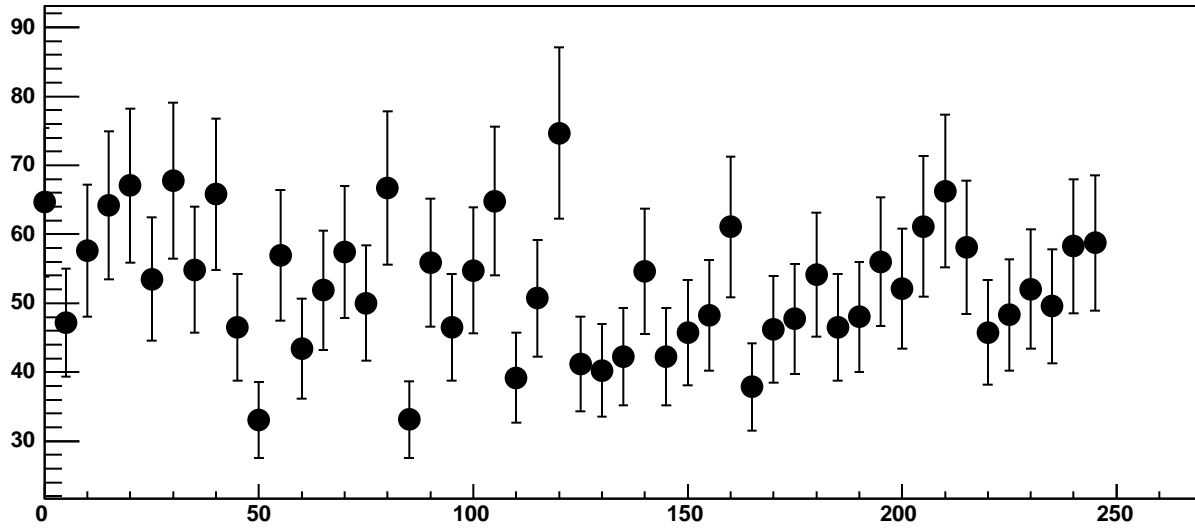


Chip 9, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

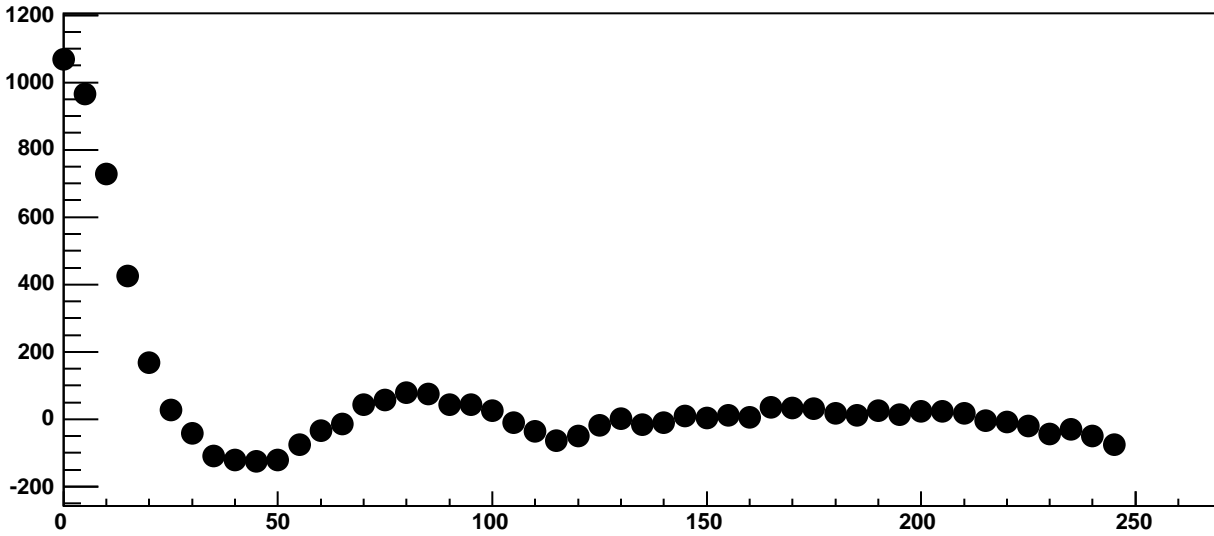


$\chi^2 / \text{ndf}$	1892 / 41
p0	-1079 ± 4.507
p1	112.6 ± 0.4842
p2	-2.053e+08 ± 6.06e+06
p3	1.546e+07 ± 4.604e+05
p4	14.17 ± 0.09078

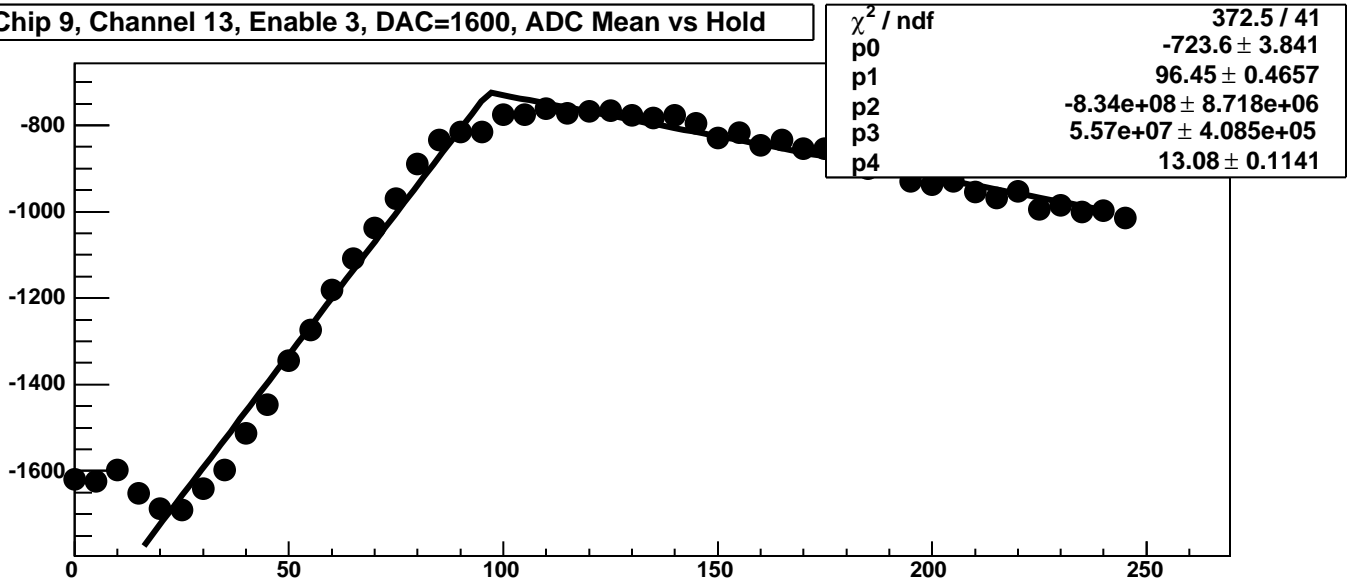
Chip 9, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



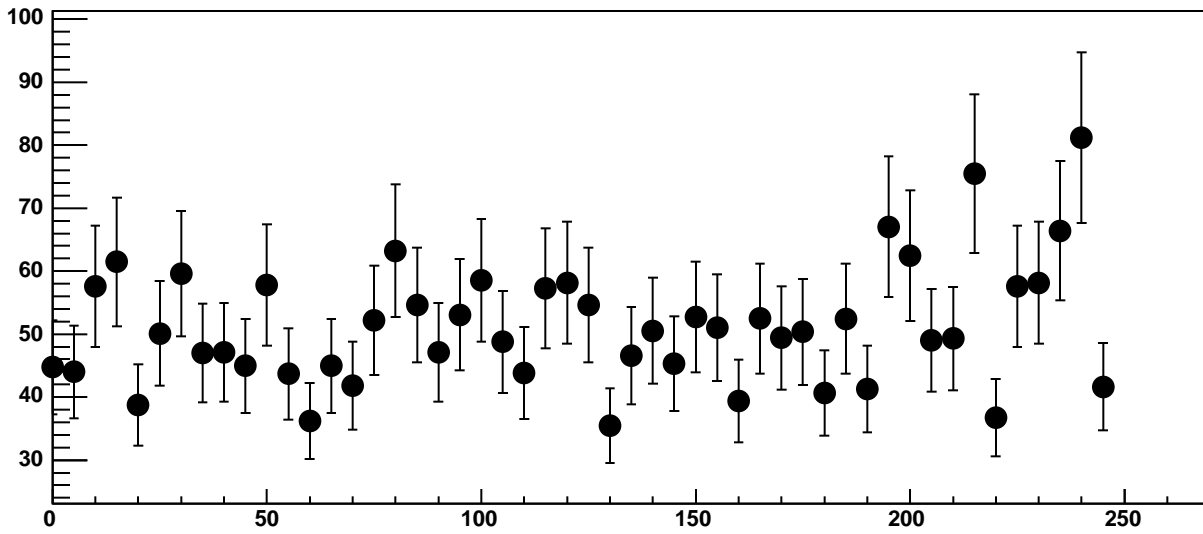
Chip 9, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold



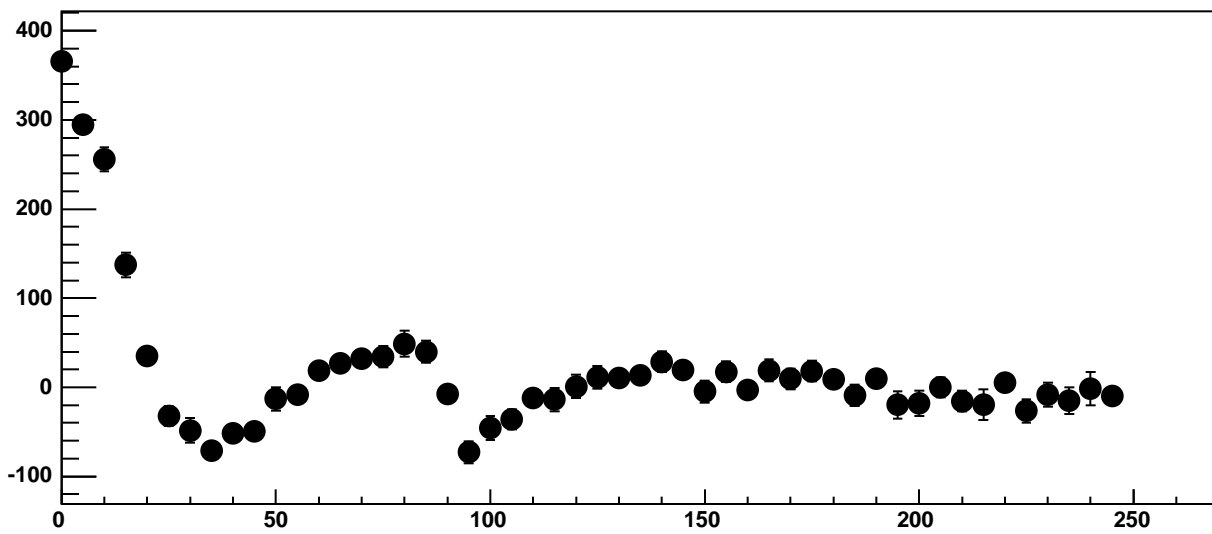
Chip 9, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold



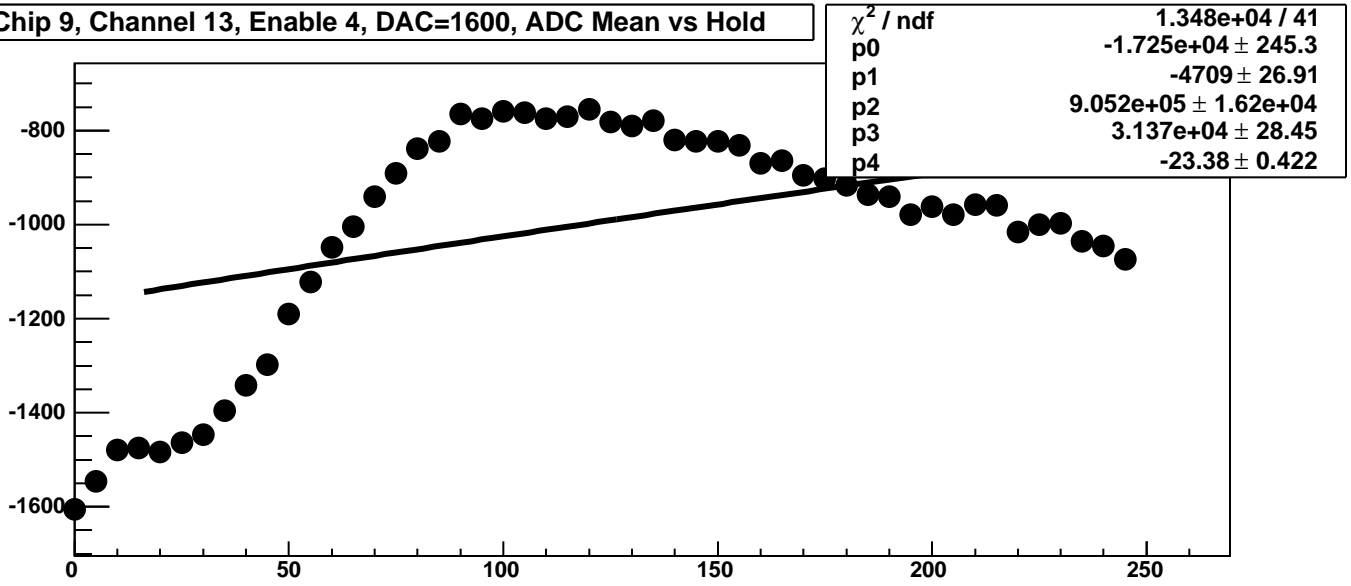
Chip 9, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



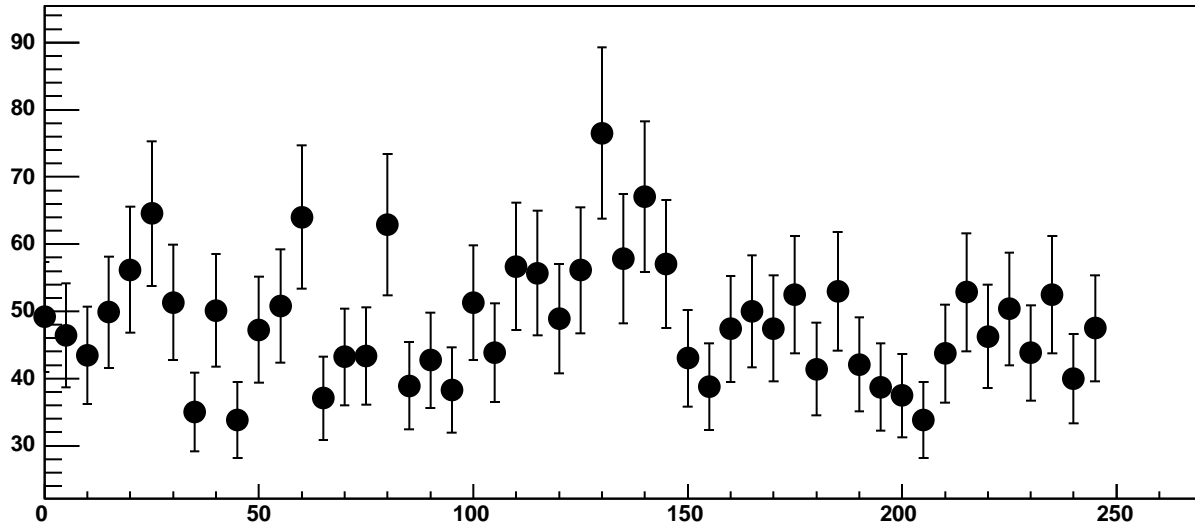
Chip 9, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold



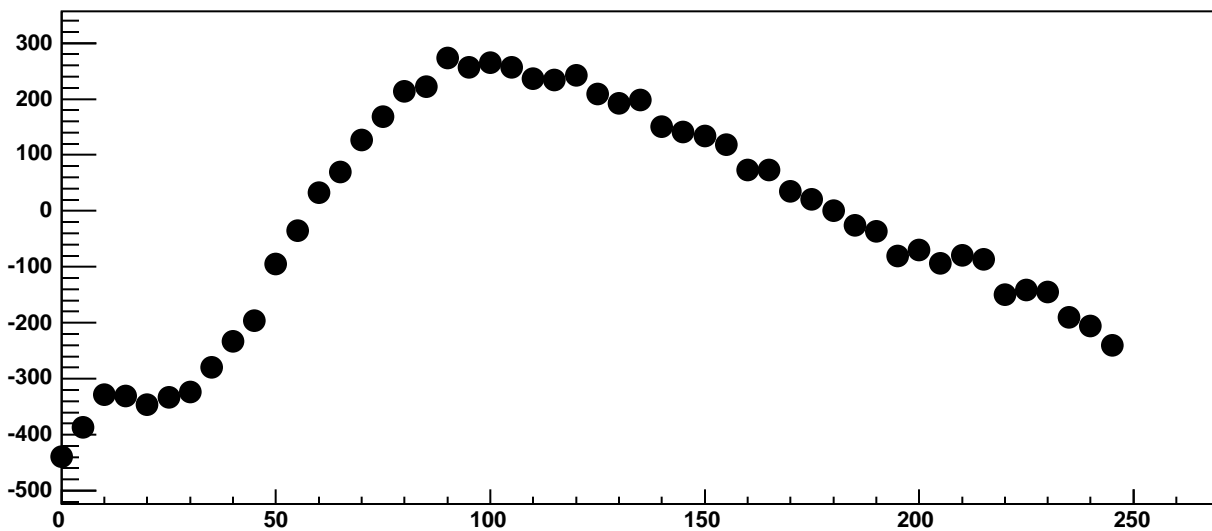
Chip 9, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold



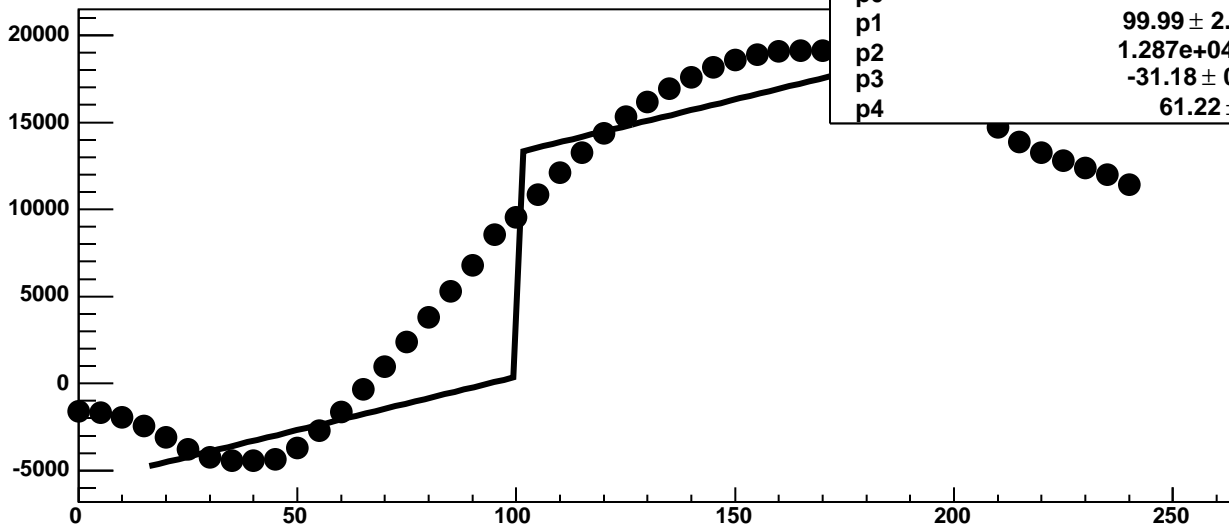
Chip 9, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

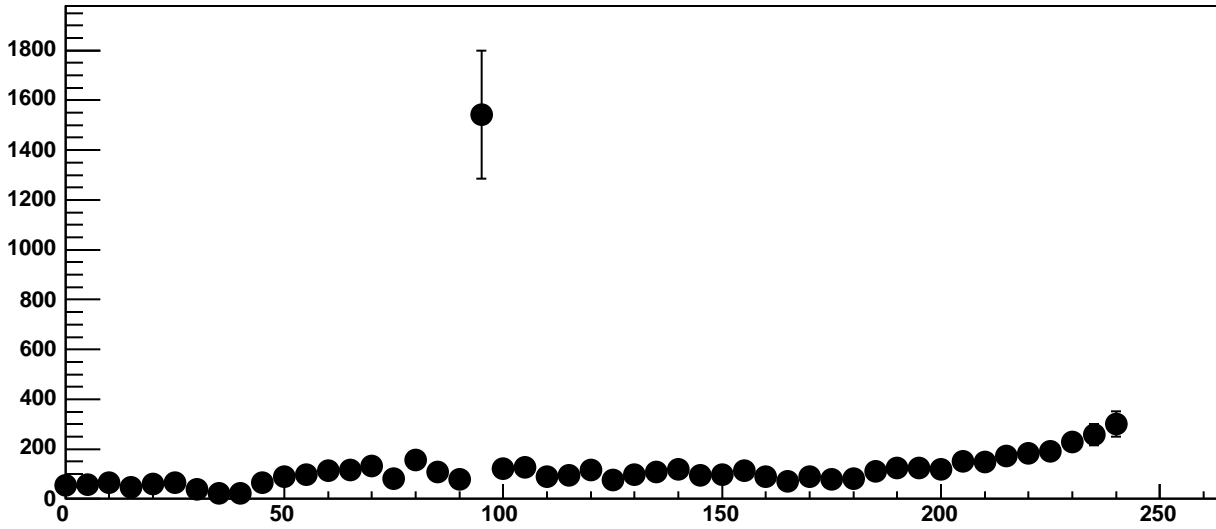


Chip 9, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

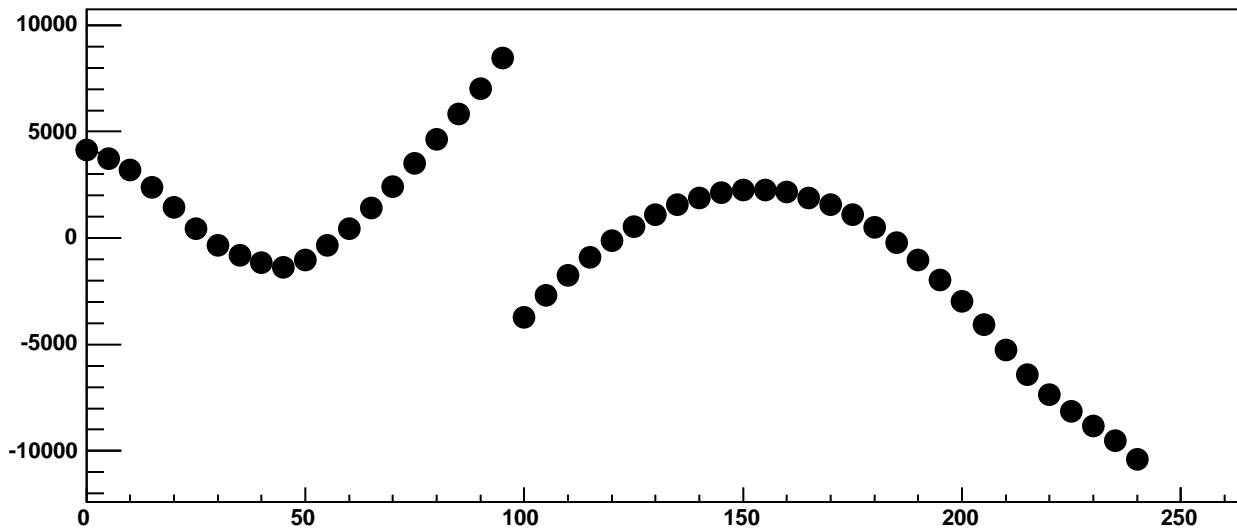


$\chi^2 / \text{ndf}$	7.507e+05 / 41
p0	381.8 ± 7.578
p1	99.99 ± 2.322e-05
p2	1.287e+04 ± 13.51
p3	-31.18 ± 0.006311
p4	61.22 ± 0.1133

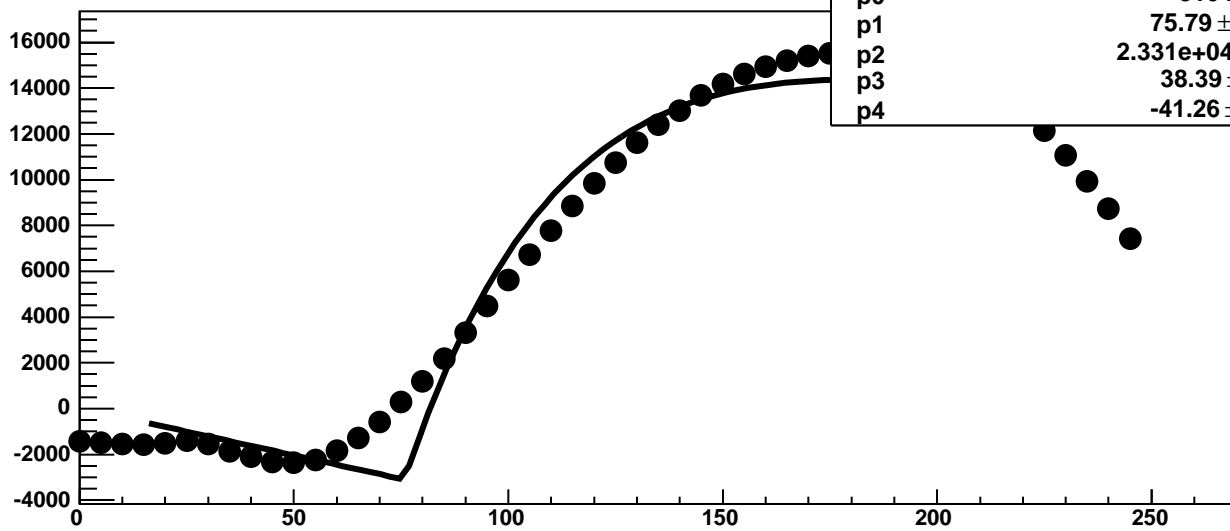
Chip 9, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

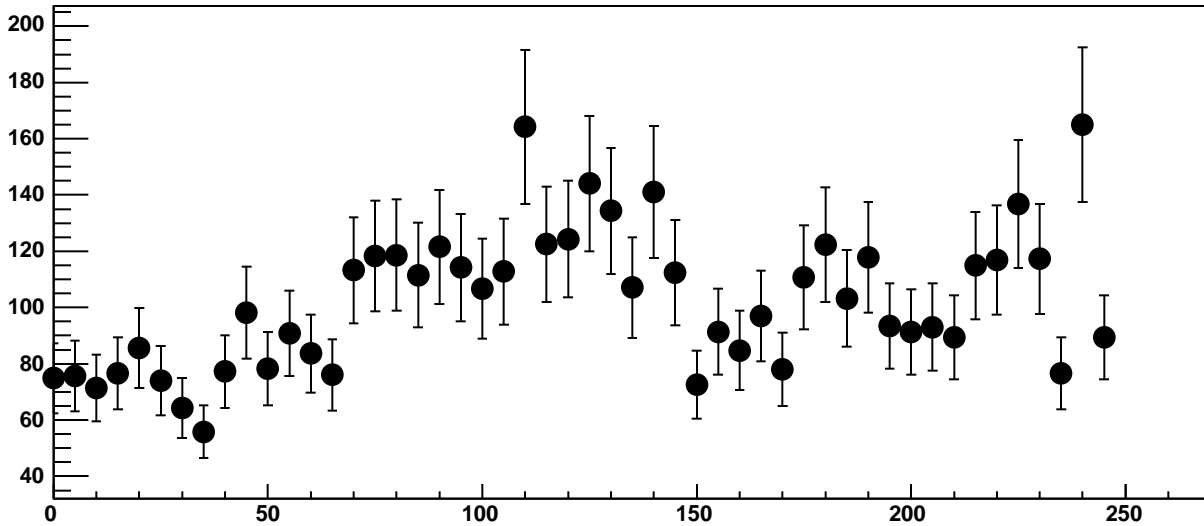


Chip 9, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold

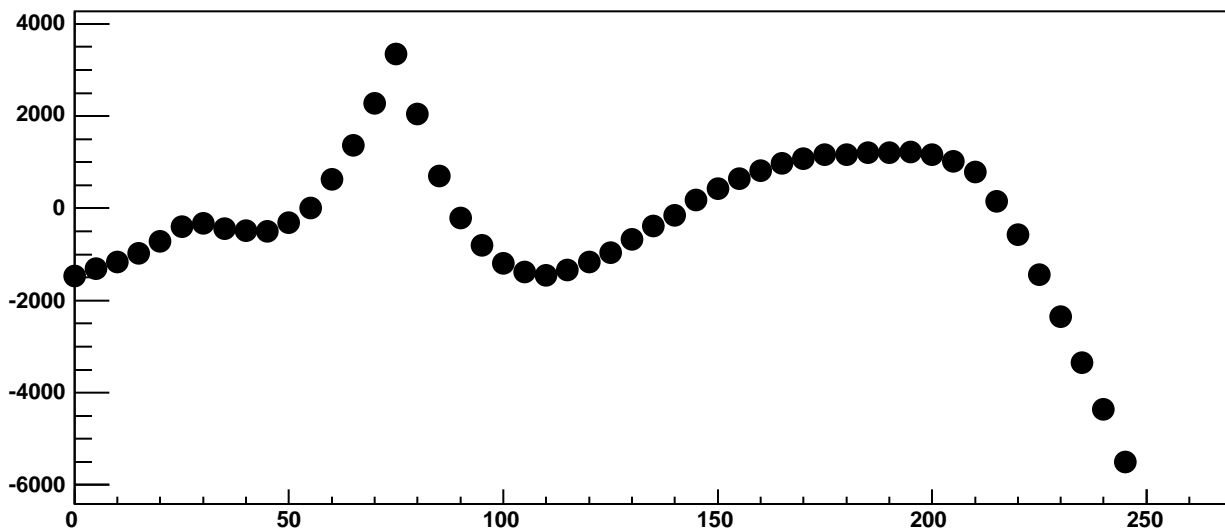


$\chi^2 / \text{ndf}$	1.456e+05 / 41
p0	-3104 ± 8.508
p1	75.79 ± 0.03911
p2	2.331e+04 ± 41.75
p3	38.39 ± 0.0899
p4	-41.26 ± 0.2184

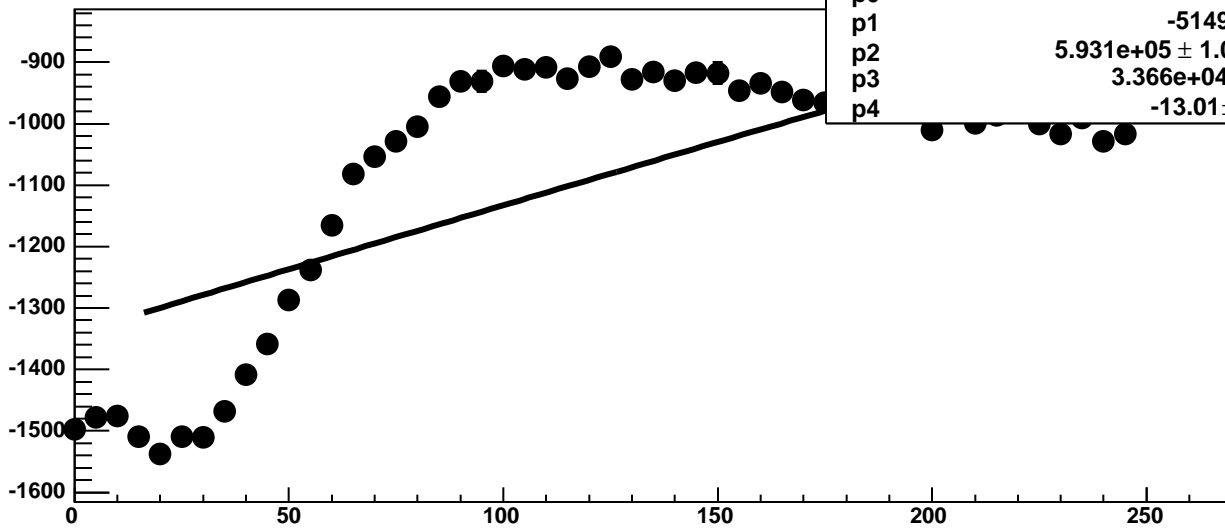
Chip 9, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

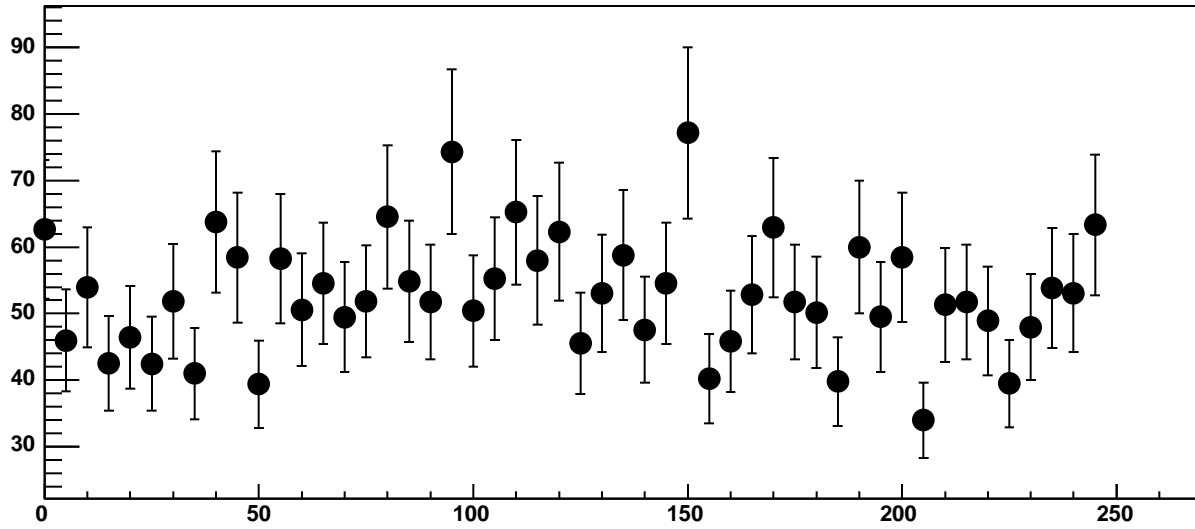


Chip 9, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold

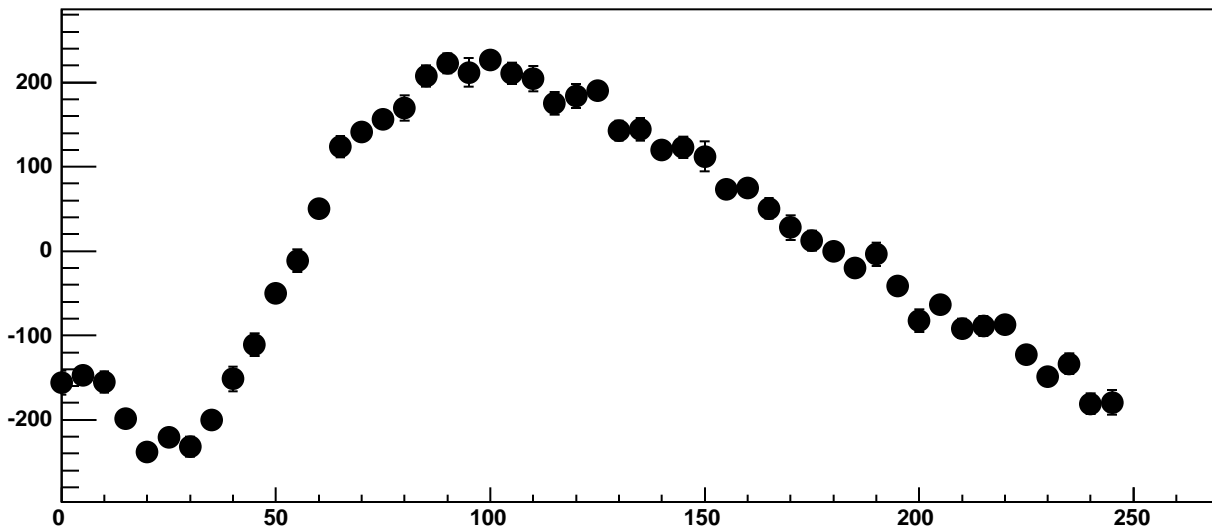


$\chi^2 / \text{ndf}$	6998 / 41
p0	$-1.849\text{e}+04 \pm 274.8$
p1	$-5149 \pm 62.23$
p2	$5.931\text{e}+05 \pm 1.069\text{e}+04$
p3	$3.366\text{e}+04 \pm 59.09$
p4	$-13.01 \pm 0.2692$

Chip 9, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

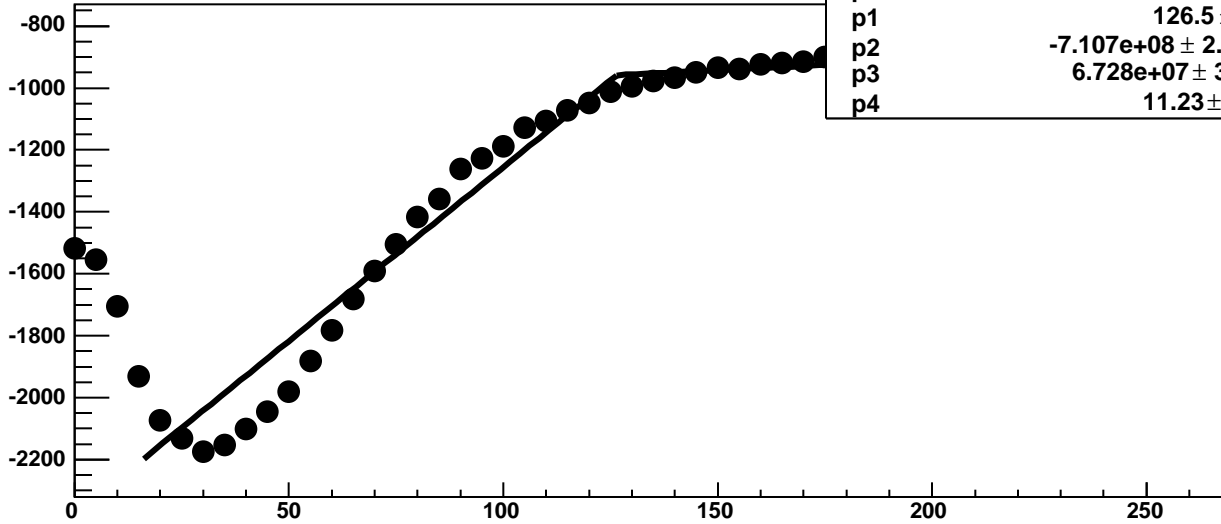


Chip 9, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold



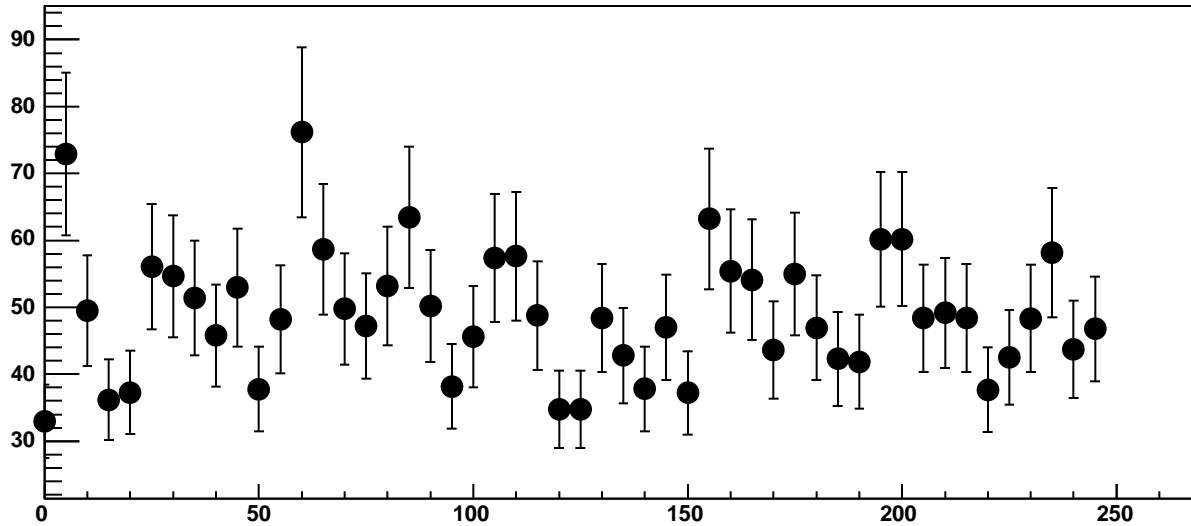


Chip 9, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

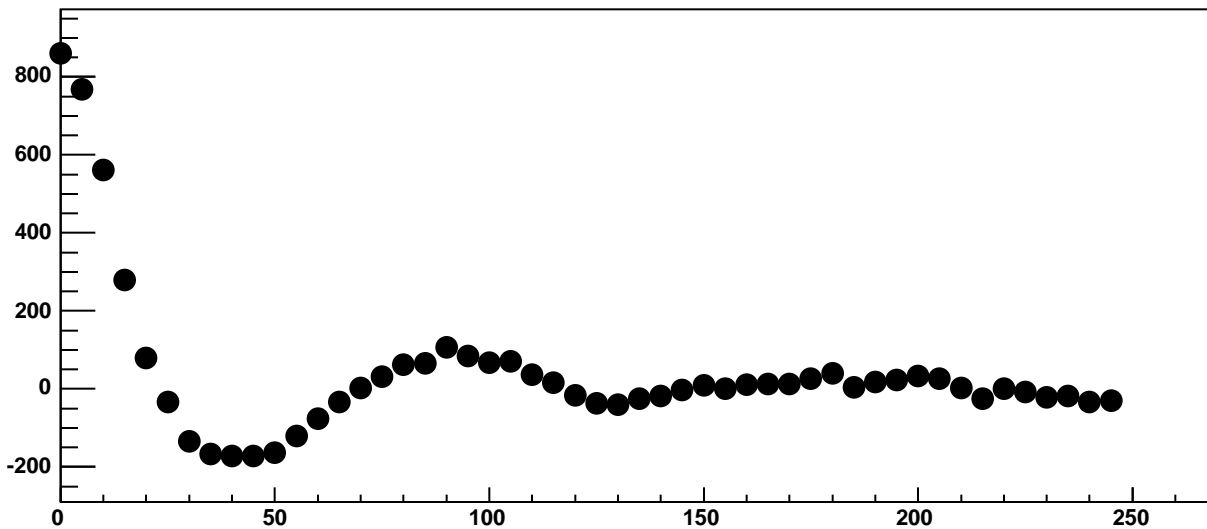


$\chi^2 / \text{ndf}$	2940 / 41
p0	-957.8 ± 4.616
p1	126.5 ± 0.4145
p2	-7.107e+08 ± 2.583e+07
p3	6.728e+07 ± 3.14e+06
p4	11.23 ± 0.07105

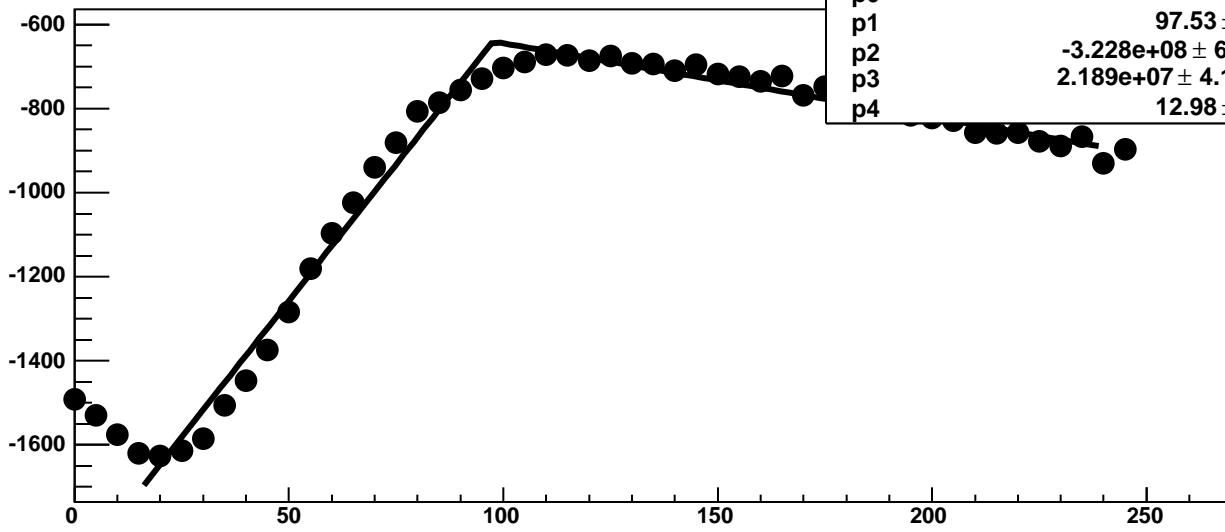
Chip 9, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

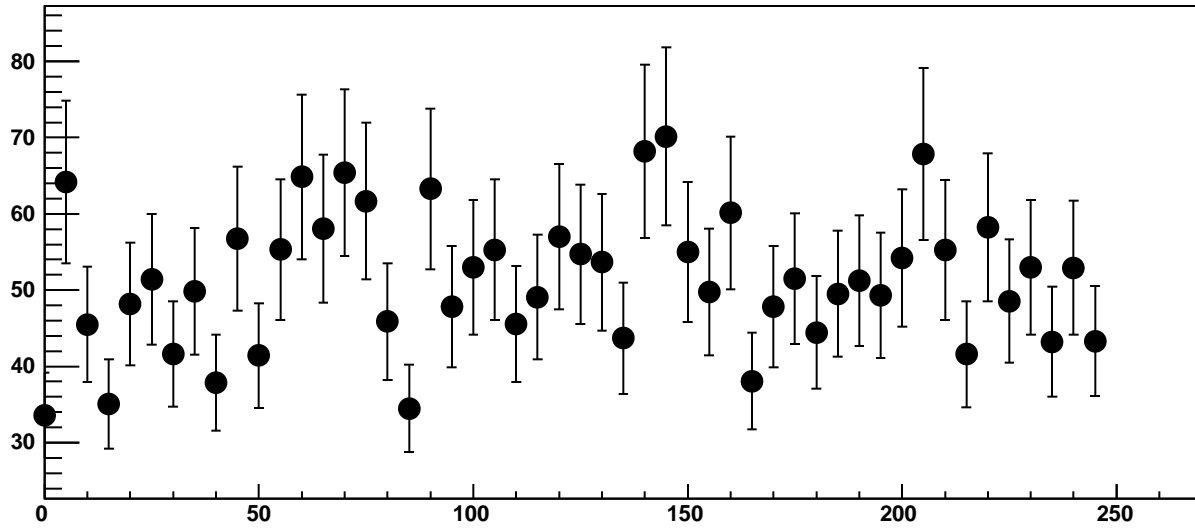


Chip 9, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

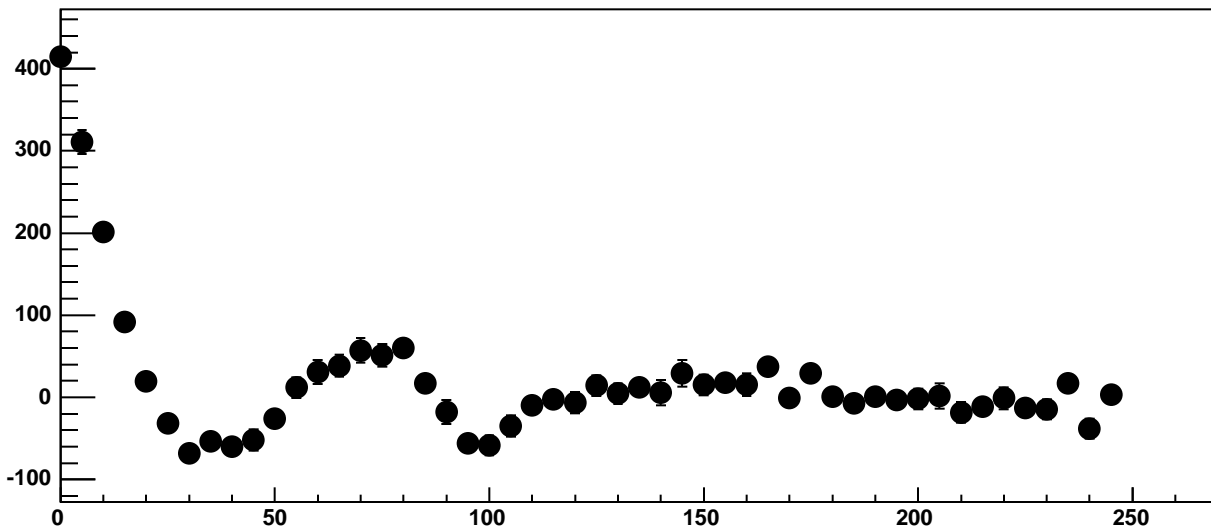


$\chi^2 / \text{ndf}$	477.8 / 41
p0	$-640.2 \pm 3.937$
p1	$97.53 \pm 0.4689$
p2	$-3.228\text{e}+08 \pm 6.66\text{e}+06$
p3	$2.189\text{e}+07 \pm 4.193\text{e}+05$
p4	$12.98 \pm 0.1018$

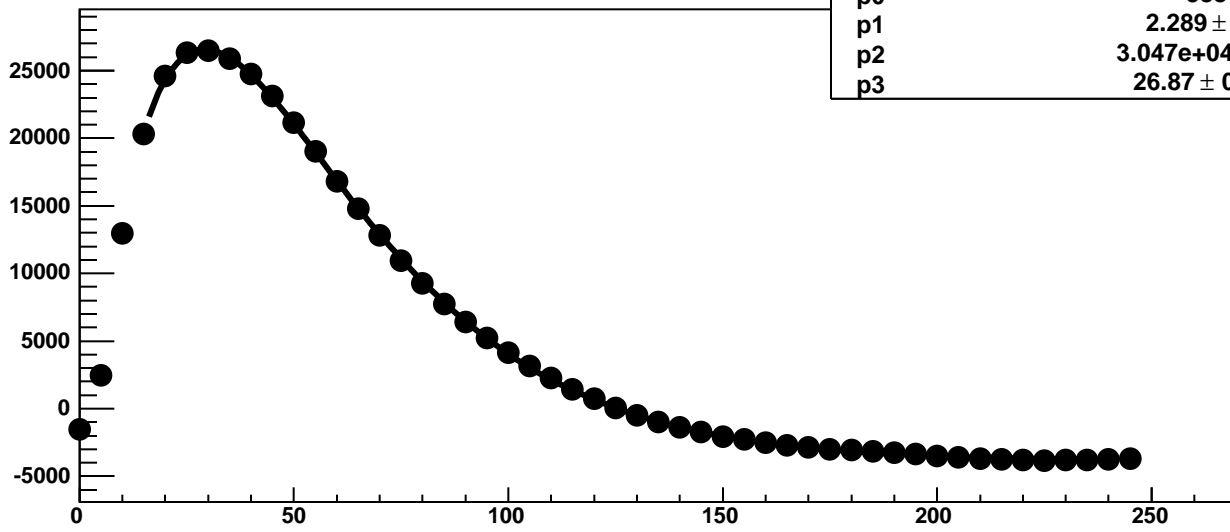
Chip 9, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

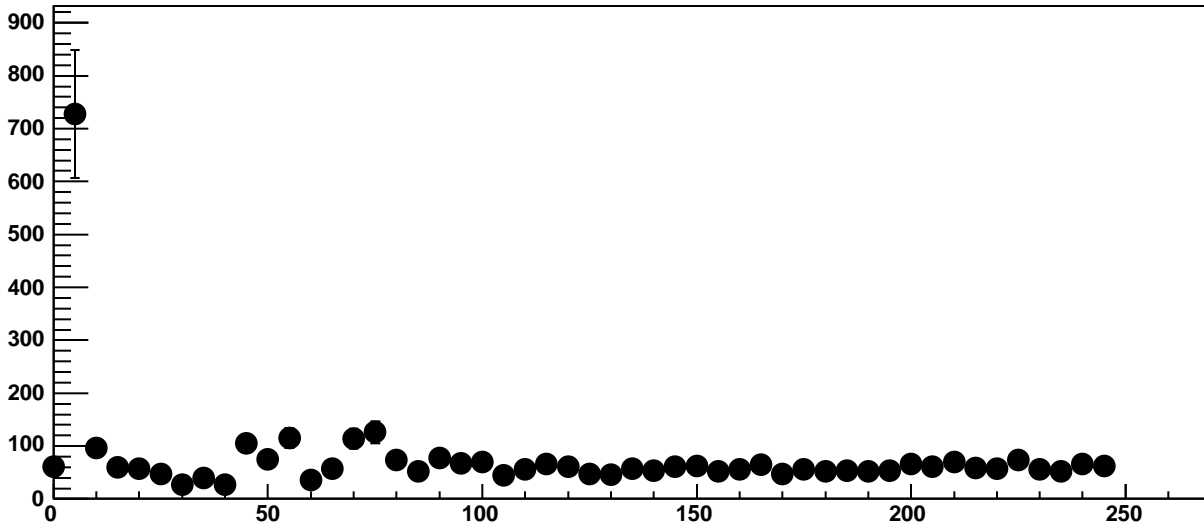


Chip 9, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold

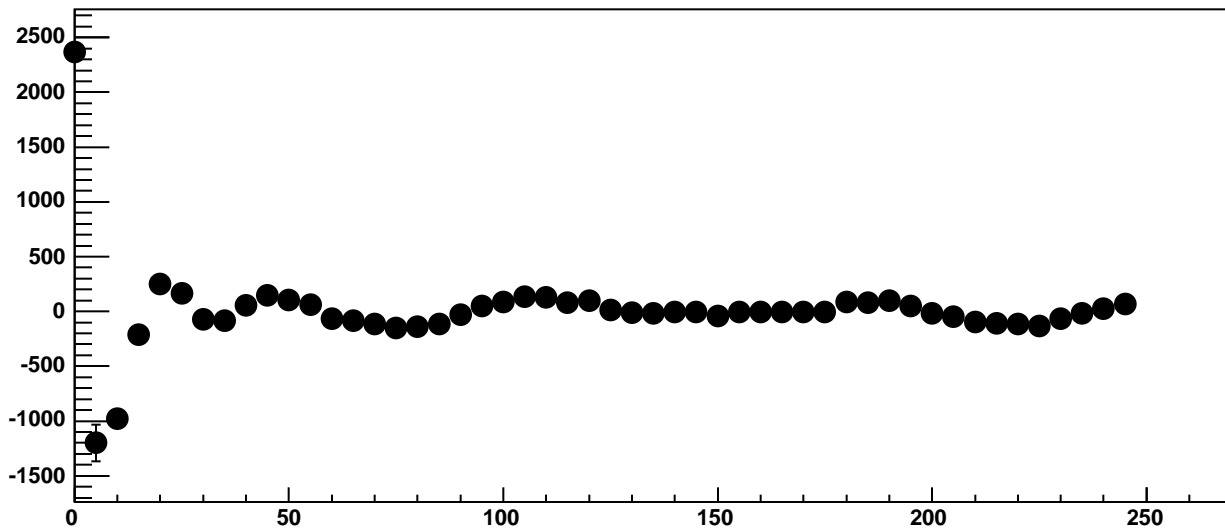


$\chi^2 / \text{ndf}$	2393 / 42
p0	-3881 ± 3.481
p1	2.289 ± 0.01433
p2	3.047e+04 ± 4.603
p3	26.87 ± 0.009562

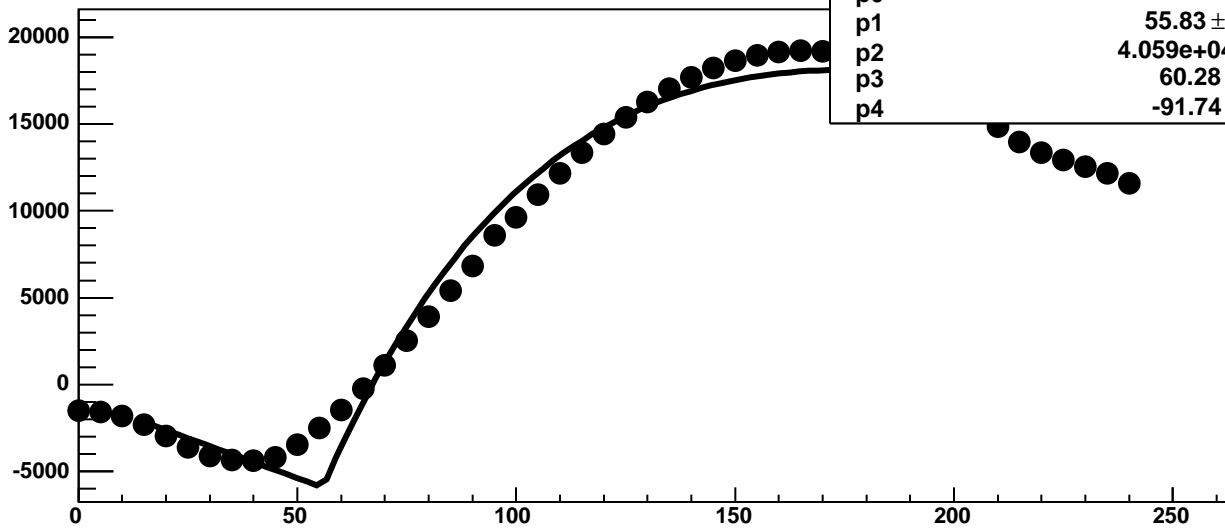
Chip 9, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold

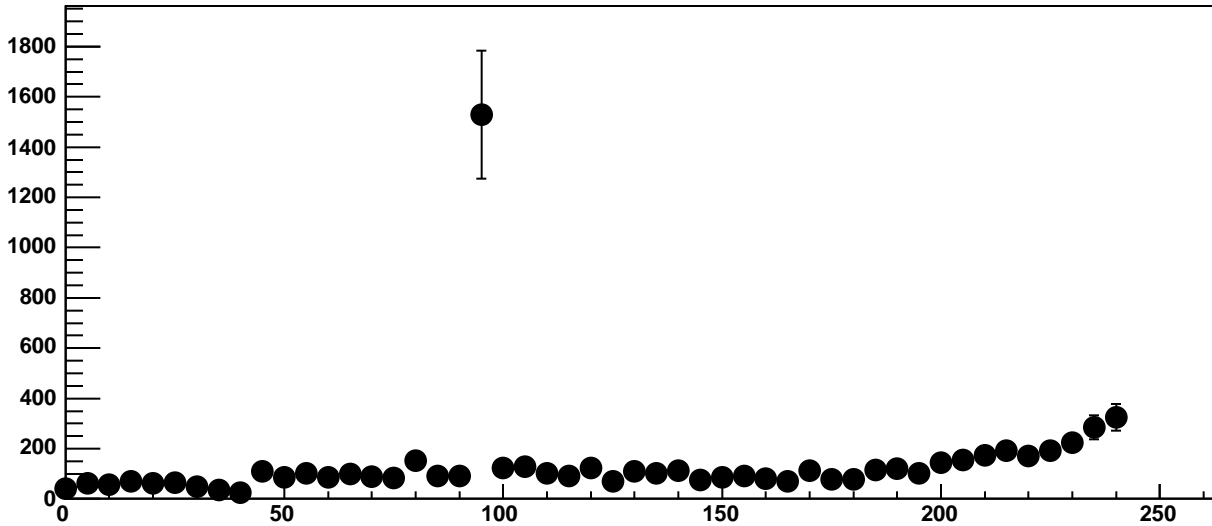


Chip 9, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

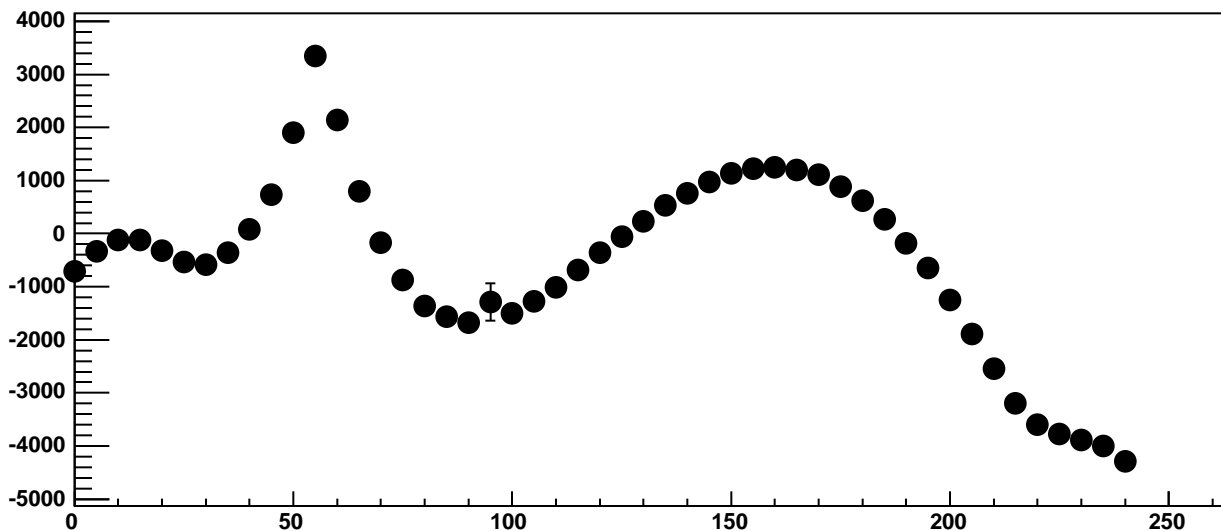


$\chi^2 / \text{ndf}$	1.448e+05 / 41
p0	-5911 ± 7.101
p1	55.83 ± 0.02613
p2	4.059e+04 ± 74.71
p3	60.28 ± 0.1128
p4	-91.74 ± 0.3407

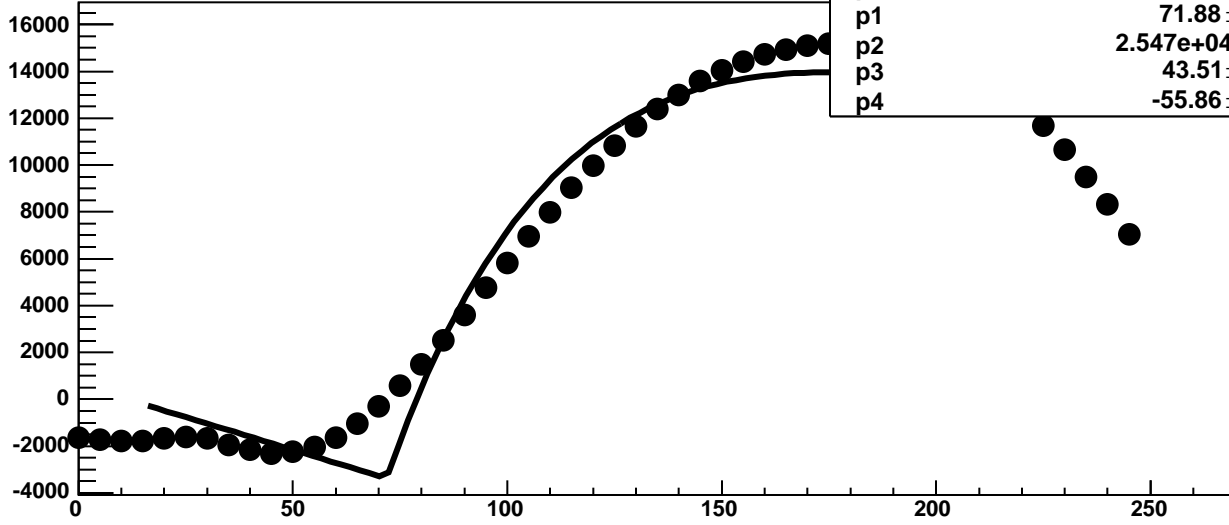
Chip 9, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

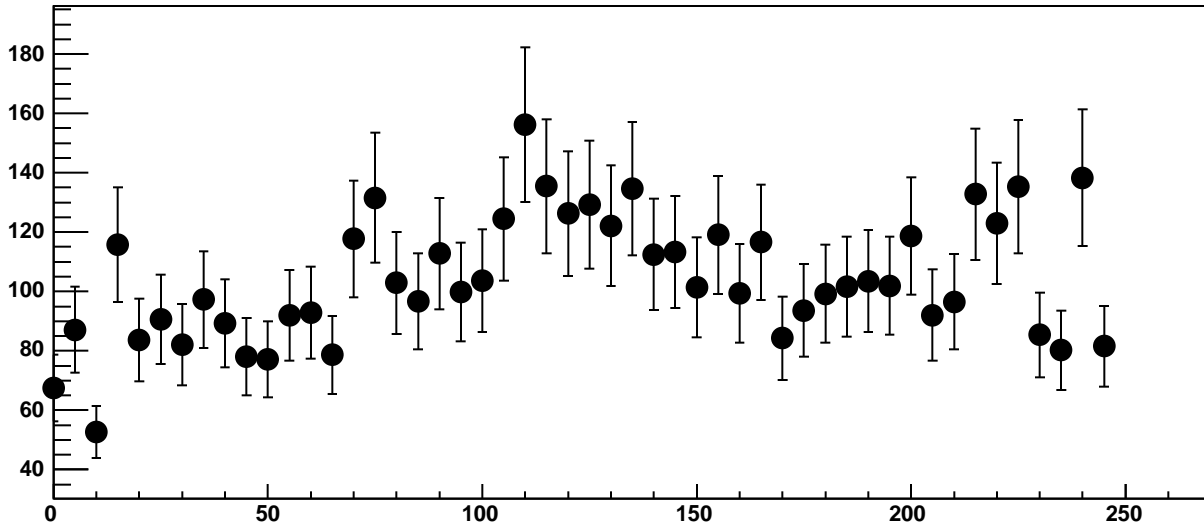


Chip 9, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

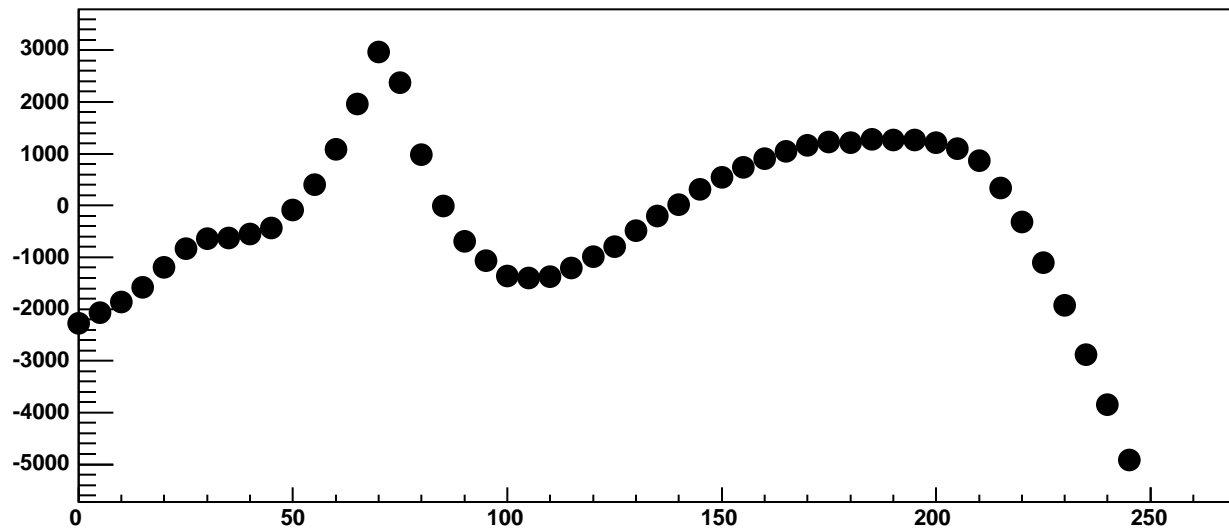


$\chi^2 / \text{ndf}$	1.407e+05 / 41
p0	-3378 ± 8.632
p1	71.88 ± 0.0372
p2	2.547e+04 ± 50.16
p3	43.51 ± 0.1018
p4	-55.86 ± 0.2537

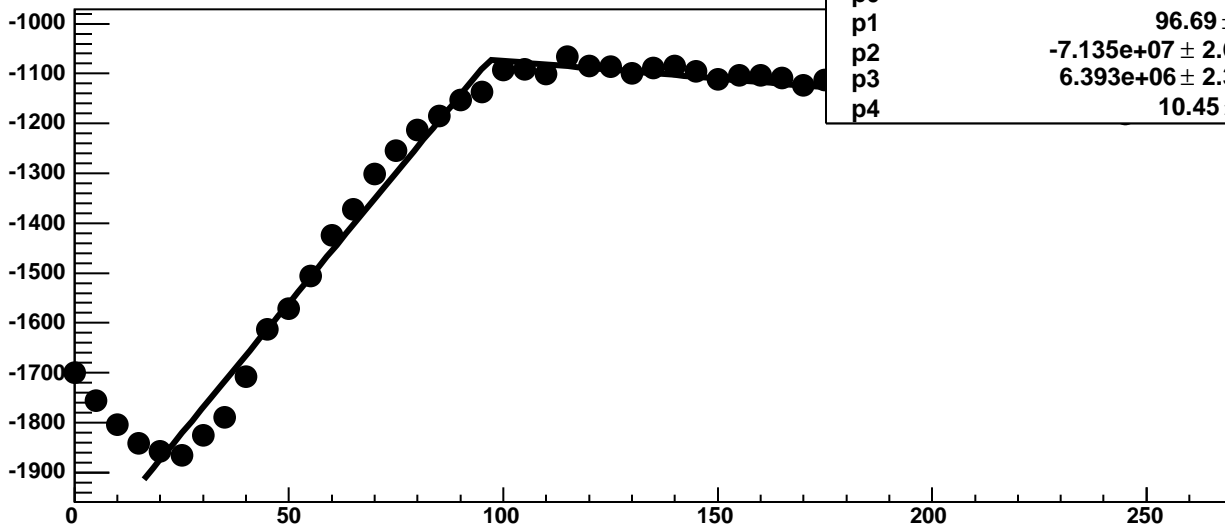
Chip 9, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

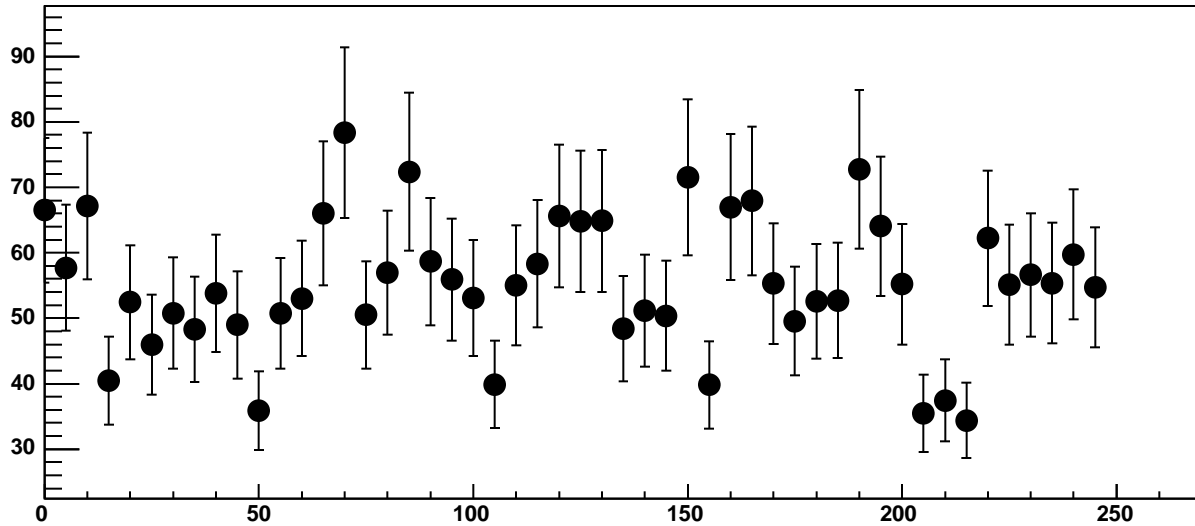


Chip 9, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

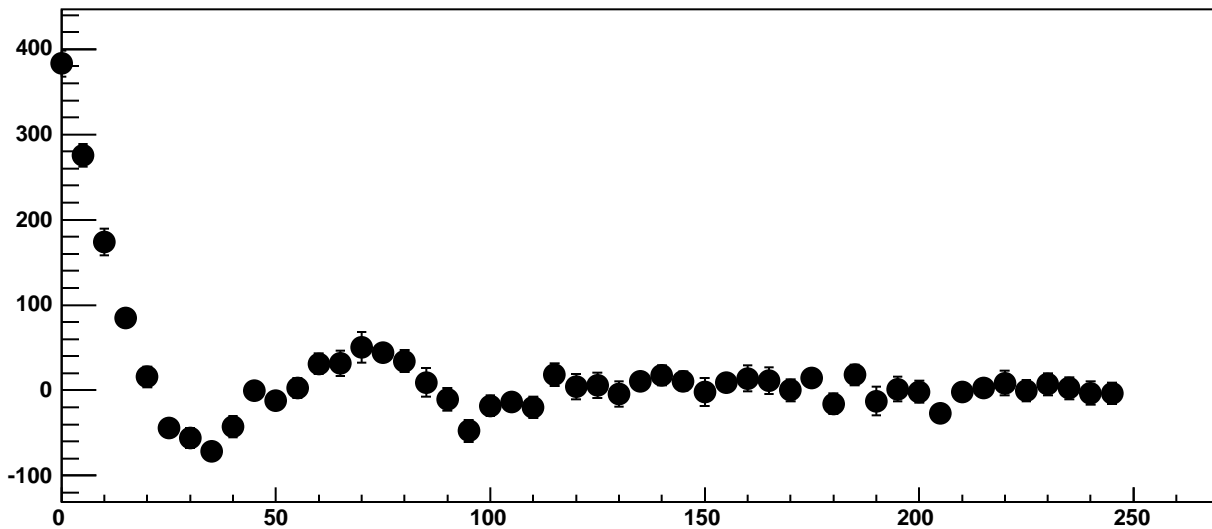


$\chi^2 / \text{ndf}$	271.8 / 41
p0	-1072 ± 4.279
p1	96.69 ± 0.6923
p2	-7.135e+07 ± 2.604e+07
p3	6.393e+06 ± 2.334e+06
p4	10.45 ± 0.1191

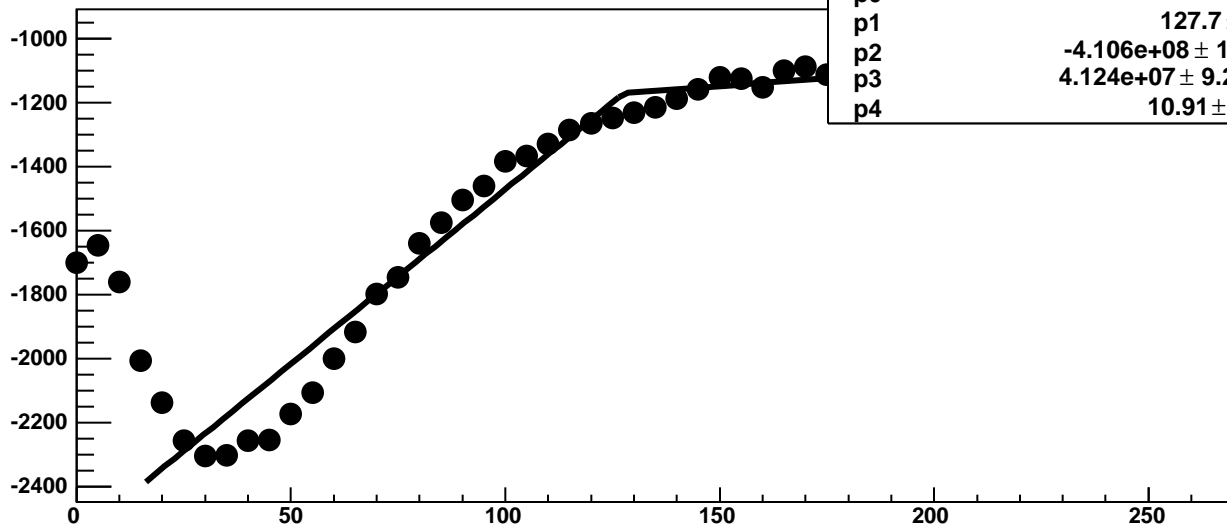
Chip 9, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

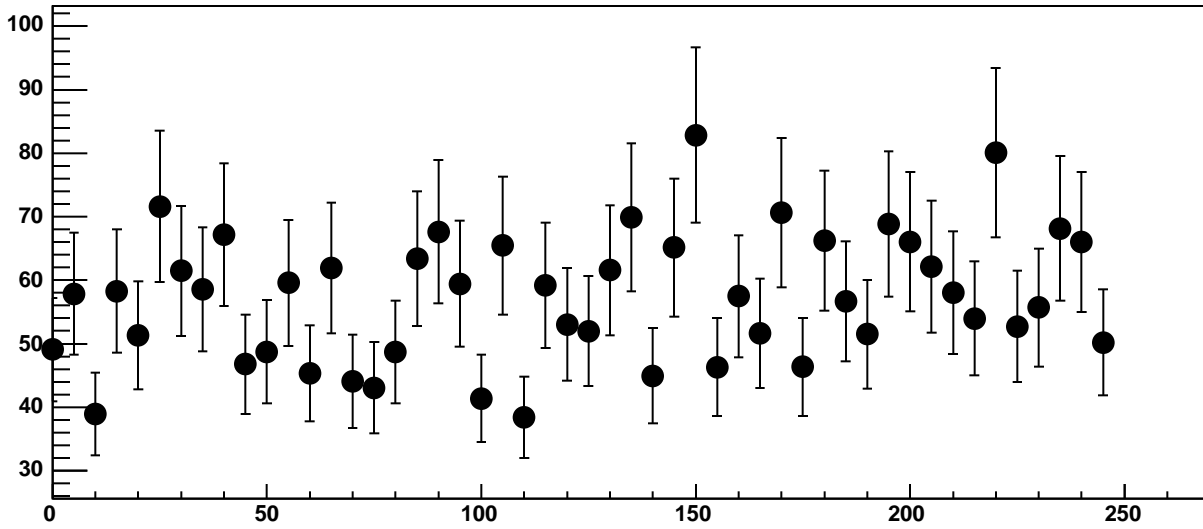


Chip 9, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

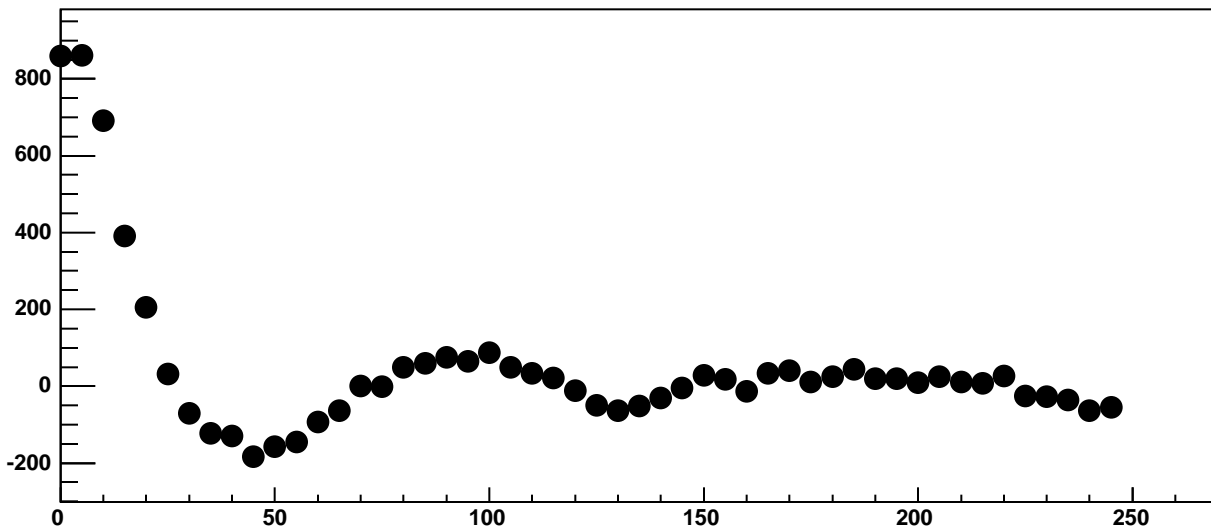


$\chi^2 / \text{ndf}$	2382 / 41
p0	$-1170 \pm 6.133$
p1	$127.7 \pm 0.7531$
p2	$-4.106\text{e}+08 \pm 1.02\text{e}+07$
p3	$4.124\text{e}+07 \pm 9.219\text{e}+05$
p4	$10.91 \pm 0.07861$

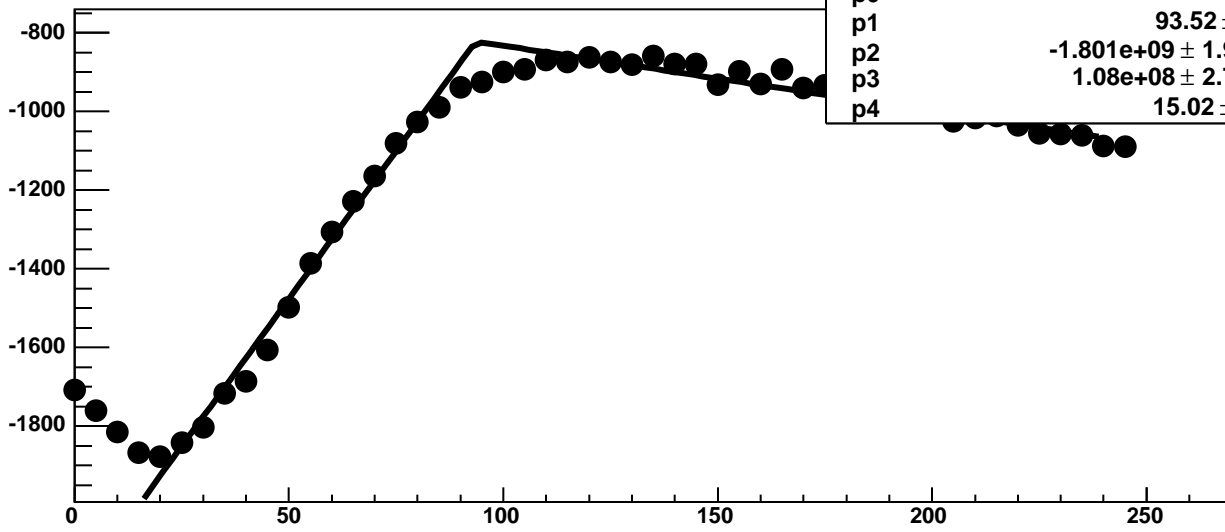
Chip 9, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold

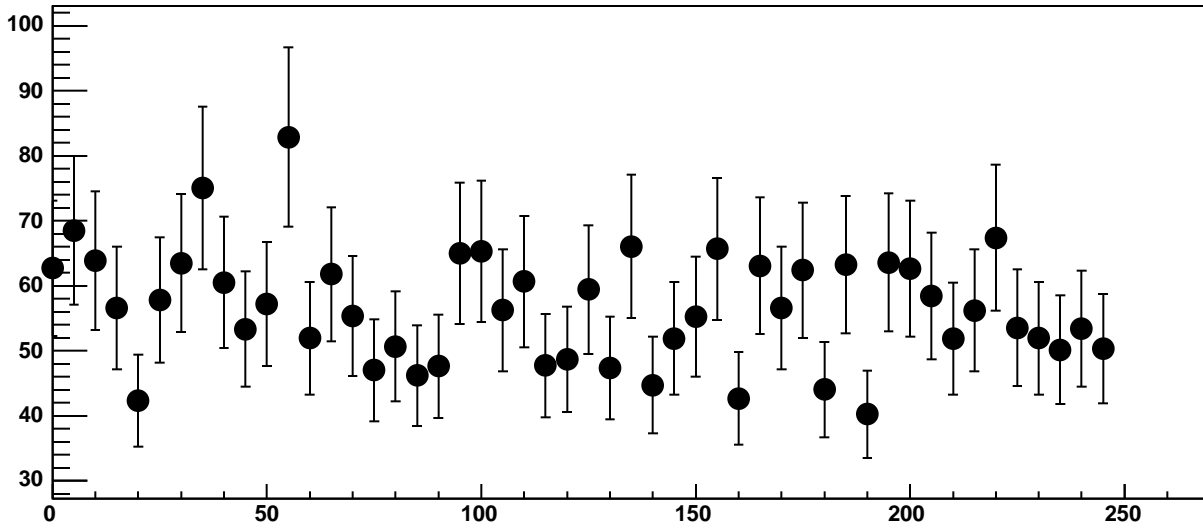


Chip 9, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

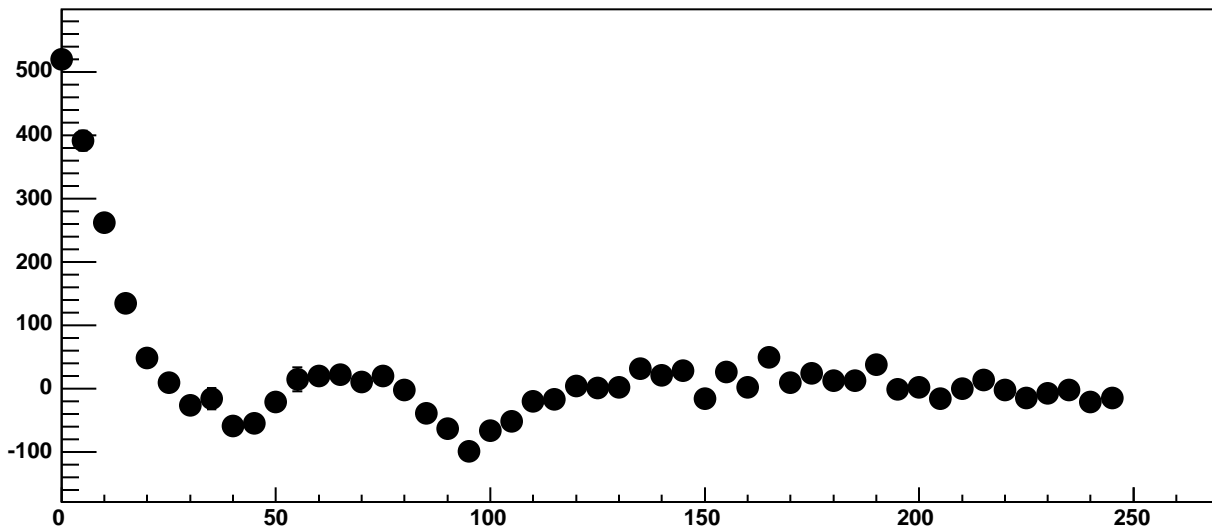


$\chi^2 / \text{ndf}$	378.4 / 41
p0	$-822 \pm 5.975$
p1	$93.52 \pm 0.2243$
p2	$-1.801\text{e}+09 \pm 1.993\text{e}+07$
p3	$1.08\text{e}+08 \pm 2.797\text{e}+06$
p4	$15.02 \pm 0.1436$

Chip 9, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

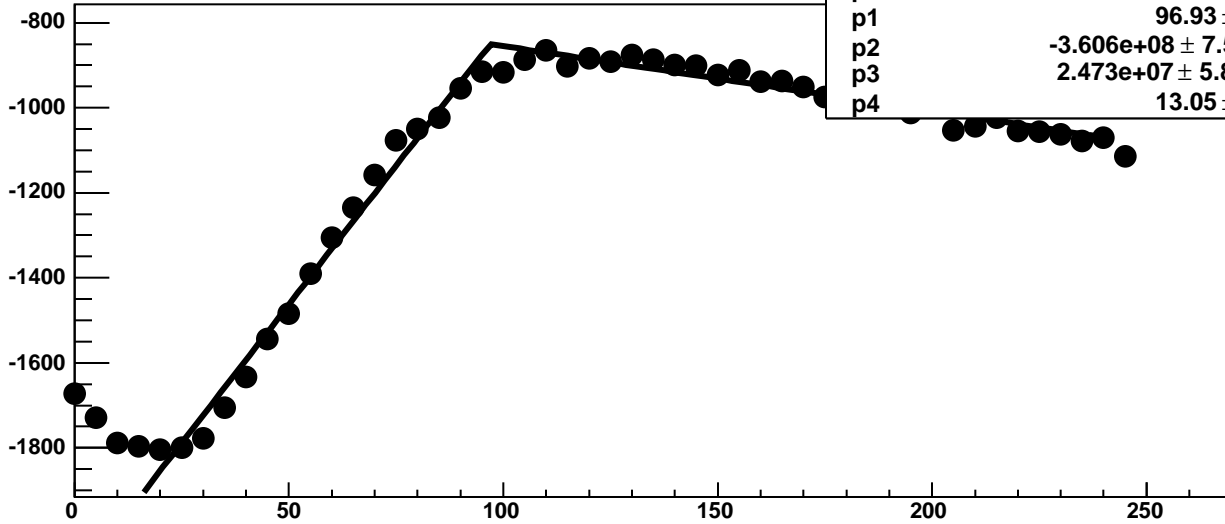


Chip 9, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold



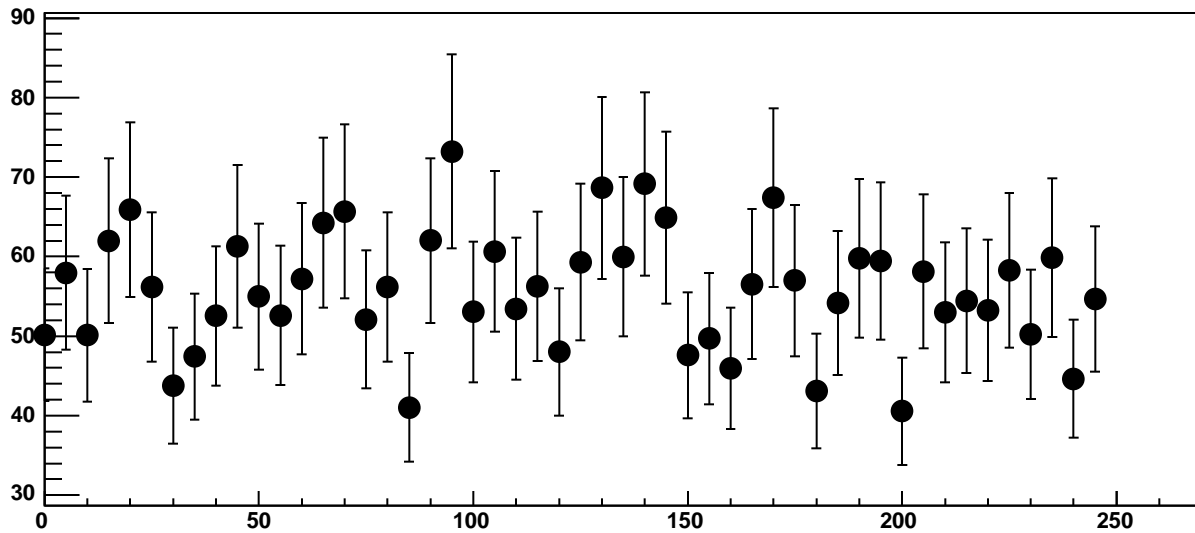


Chip 9, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

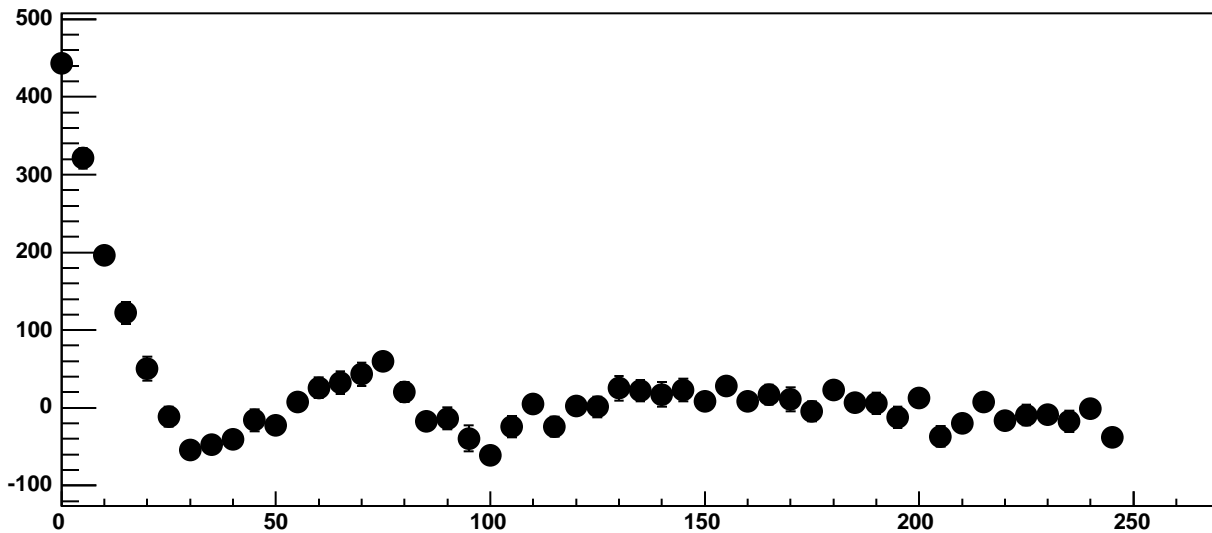


$\chi^2 / \text{ndf}$	278.3 / 41
p0	-850 ± 4.244
p1	96.93 ± 0.4883
p2	-3.606e+08 ± 7.538e+06
p3	2.473e+07 ± 5.889e+05
p4	13.05 ± 0.1133

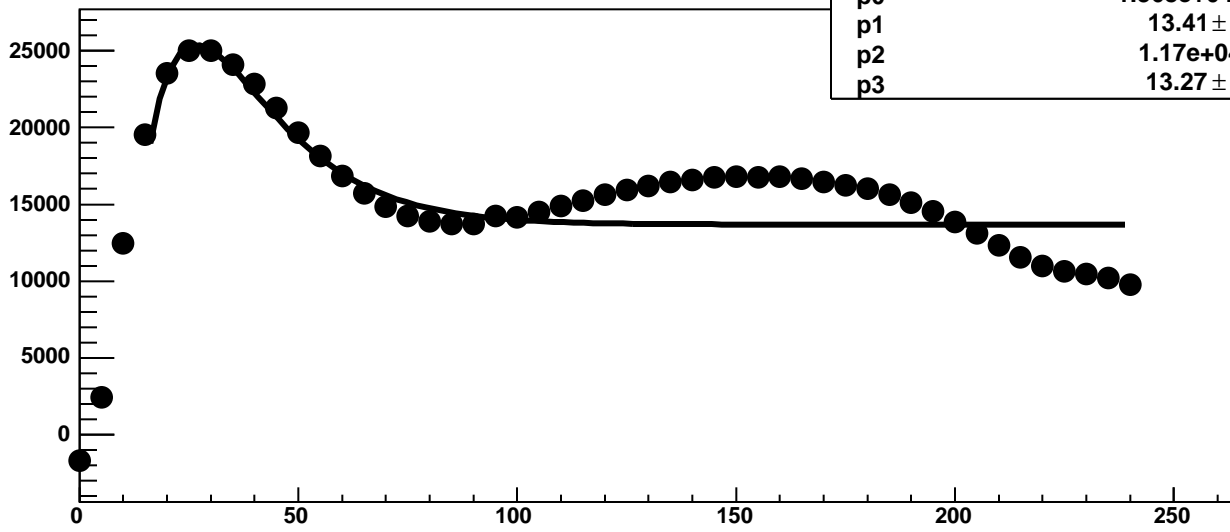
Chip 9, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

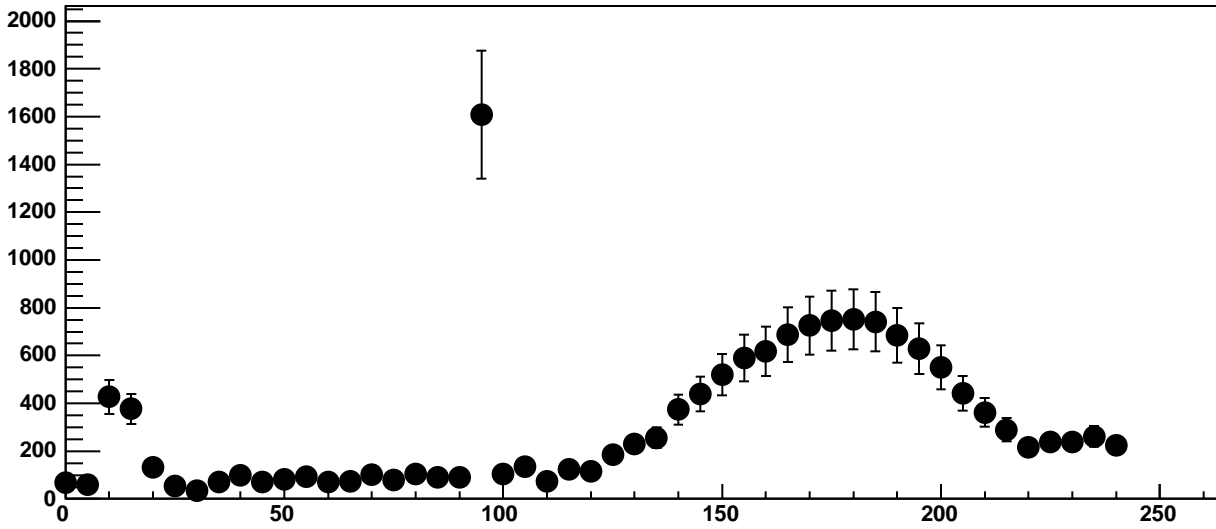


Chip 9, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold

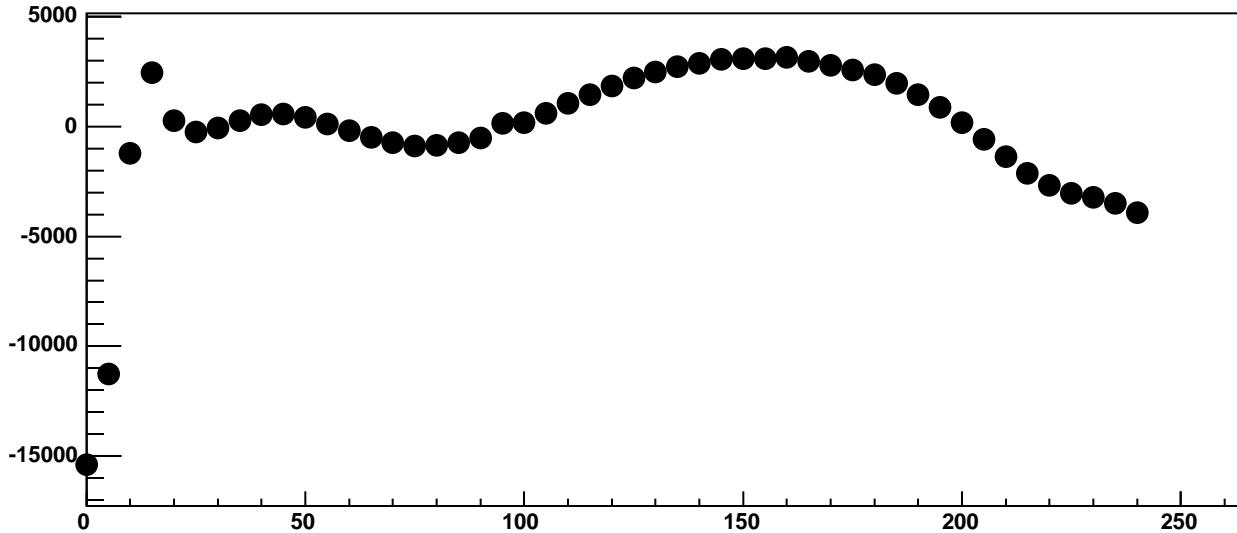


$\chi^2 / \text{ndf}$	5.491e+04 / 42
p0	1.368e+04 $\pm$ 8.015
p1	13.41 $\pm$ 0.03152
p2	1.17e+04 $\pm$ 9.89
p3	13.27 $\pm$ 0.02063

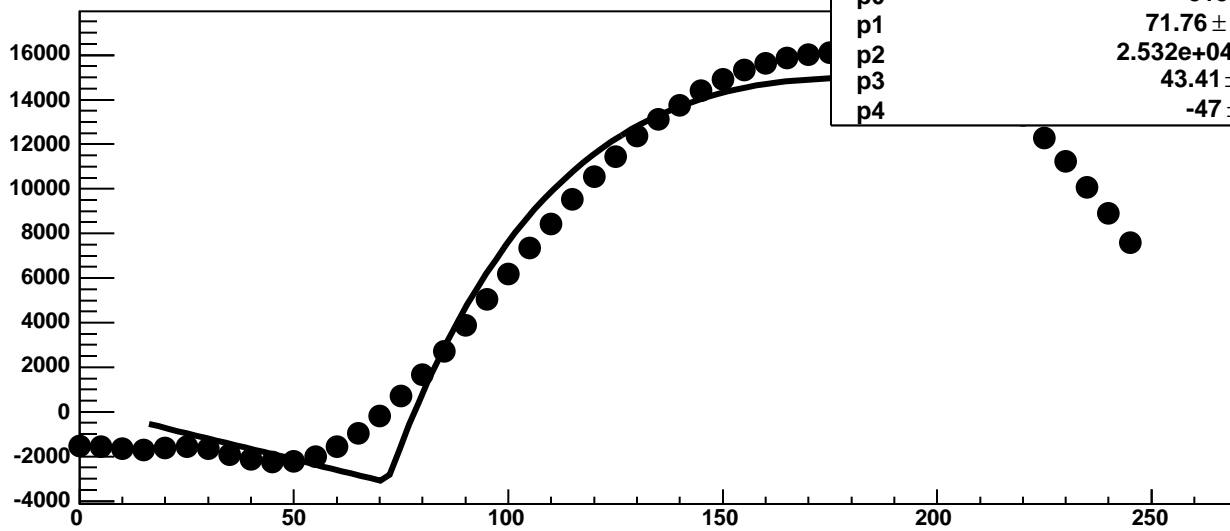
Chip 9, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

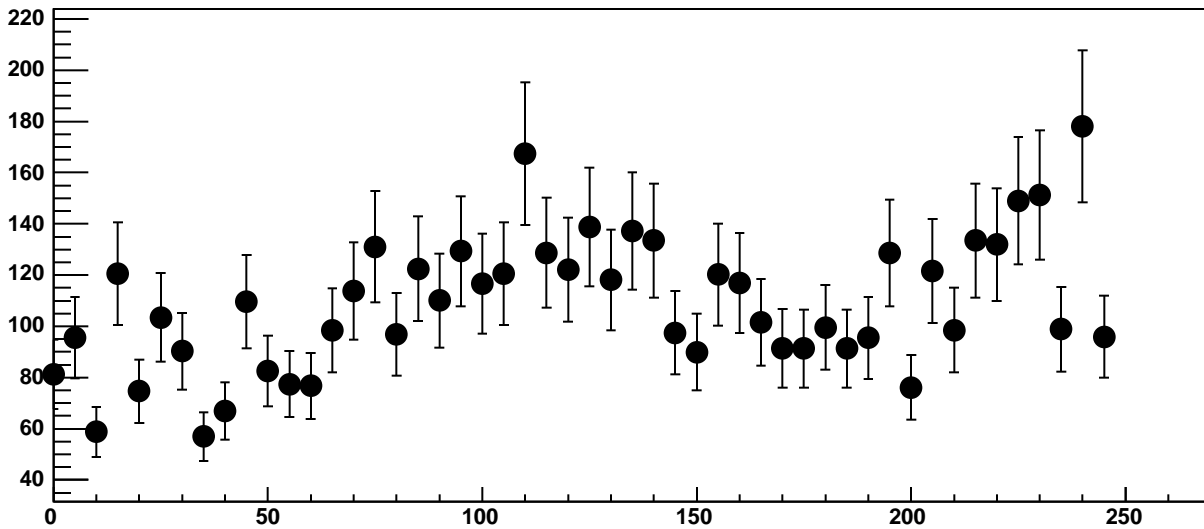


Chip 9, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

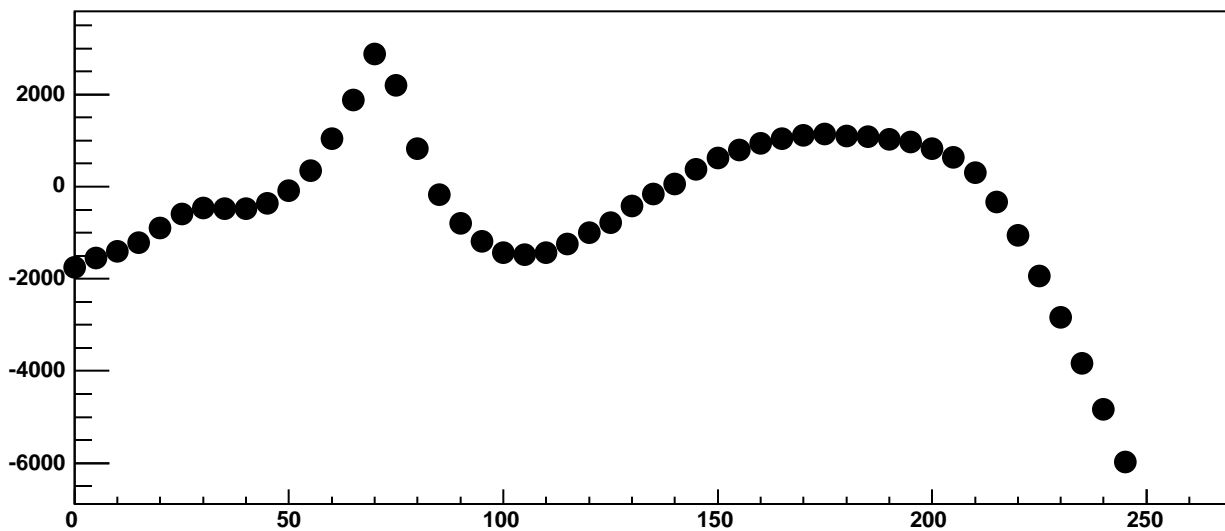


$\chi^2 / \text{ndf}$	1.279e+05 / 41
p0	-3158 ± 8.93
p1	71.76 ± 0.03733
p2	2.532e+04 ± 50.92
p3	43.41 ± 0.1024
p4	-47 ± 0.2619

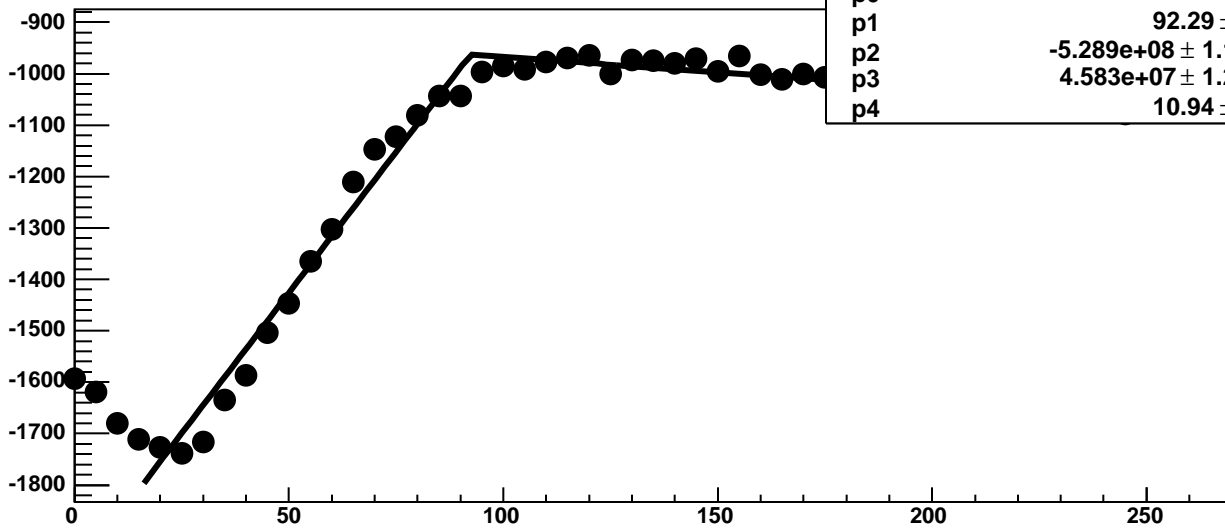
Chip 9, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

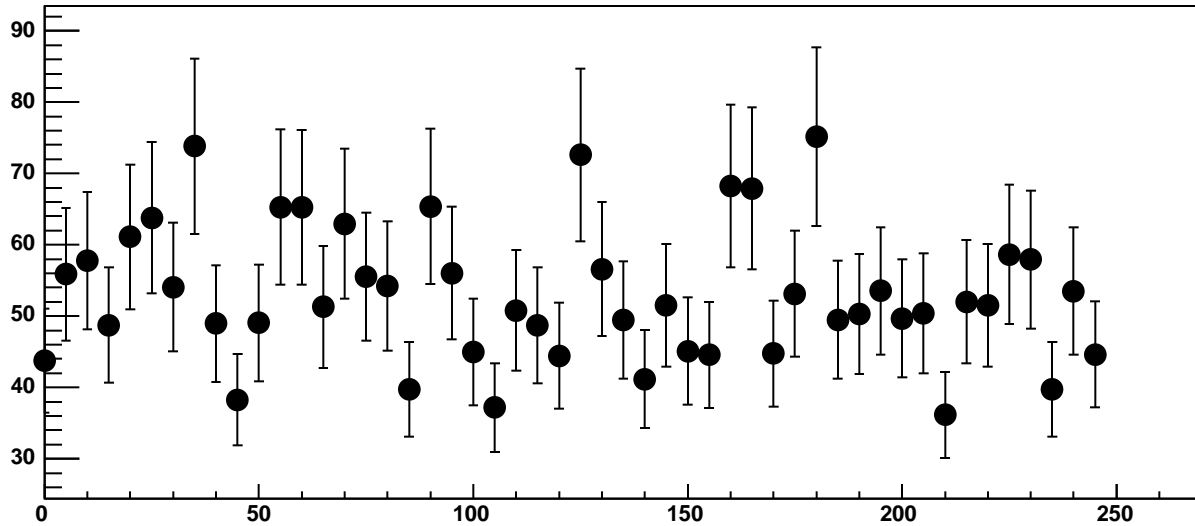


Chip 9, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

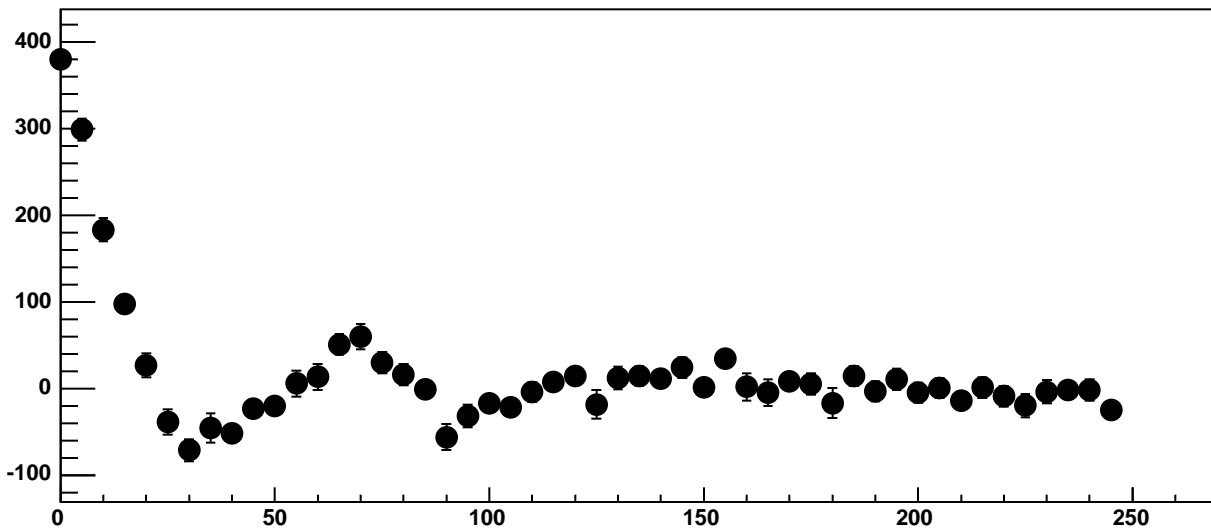


$\chi^2 / \text{ndf}$	265.9 / 41
p0	$-962.8 \pm 3.662$
p1	$92.29 \pm 0.5846$
p2	$-5.289\text{e}+08 \pm 1.146\text{e}+07$
p3	$4.583\text{e}+07 \pm 1.292\text{e}+06$
p4	$10.94 \pm 0.1245$

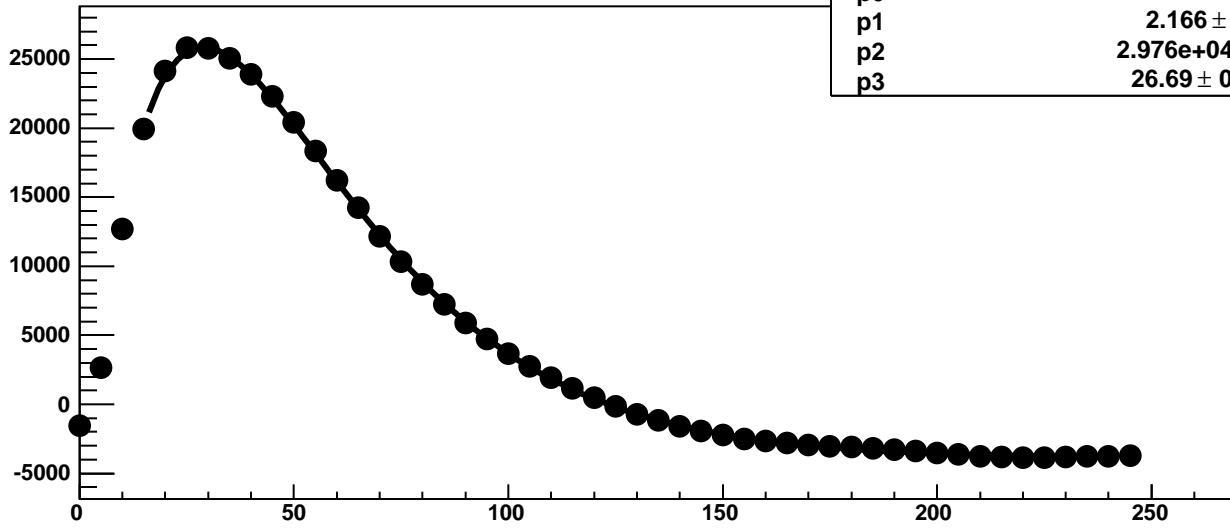
Chip 9, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold

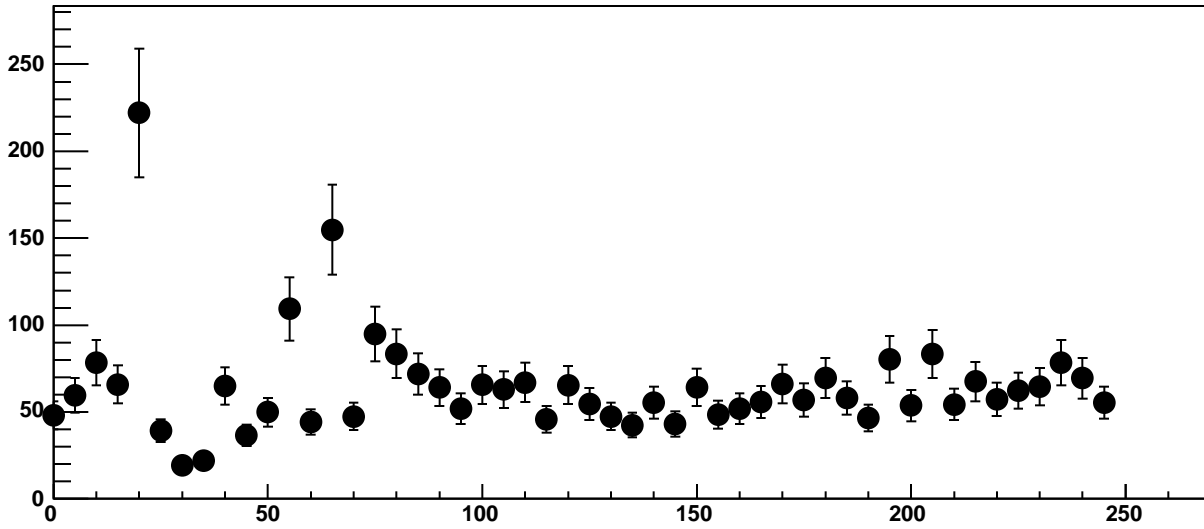


Chip 9, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold

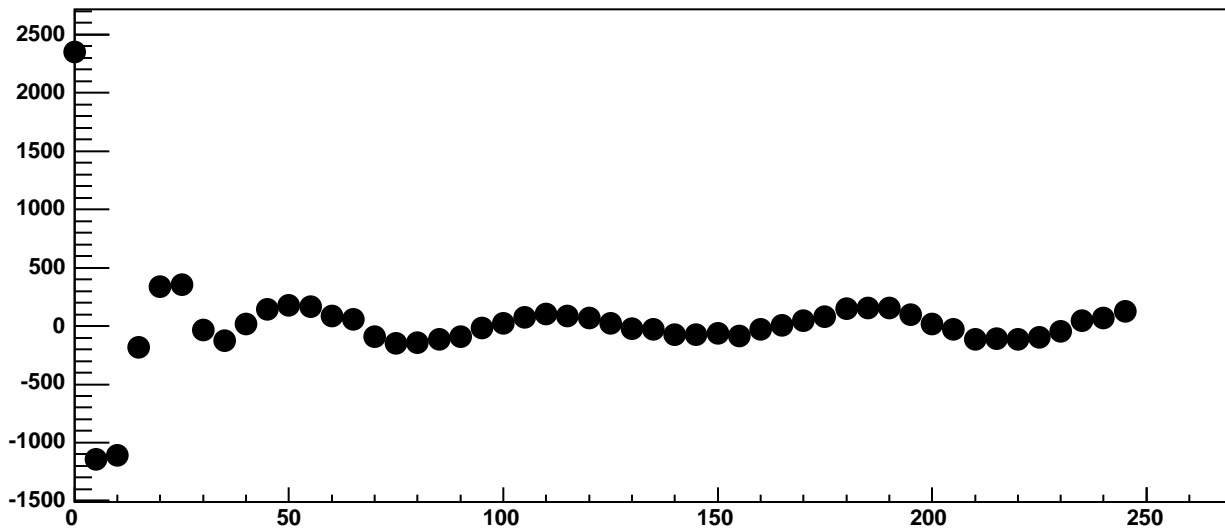


$\chi^2 / \text{ndf}$	4460 / 42
p0	$-3921 \pm 3.575$
p1	$2.166 \pm 0.01647$
p2	$2.976e+04 \pm 4.383$
p3	$26.69 \pm 0.009879$

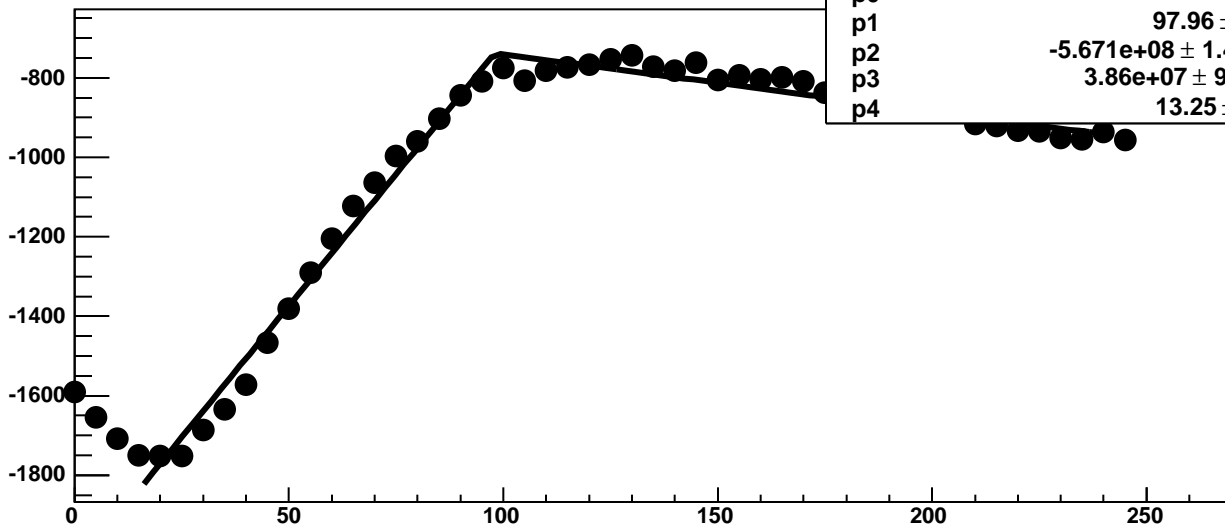
Chip 9, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold

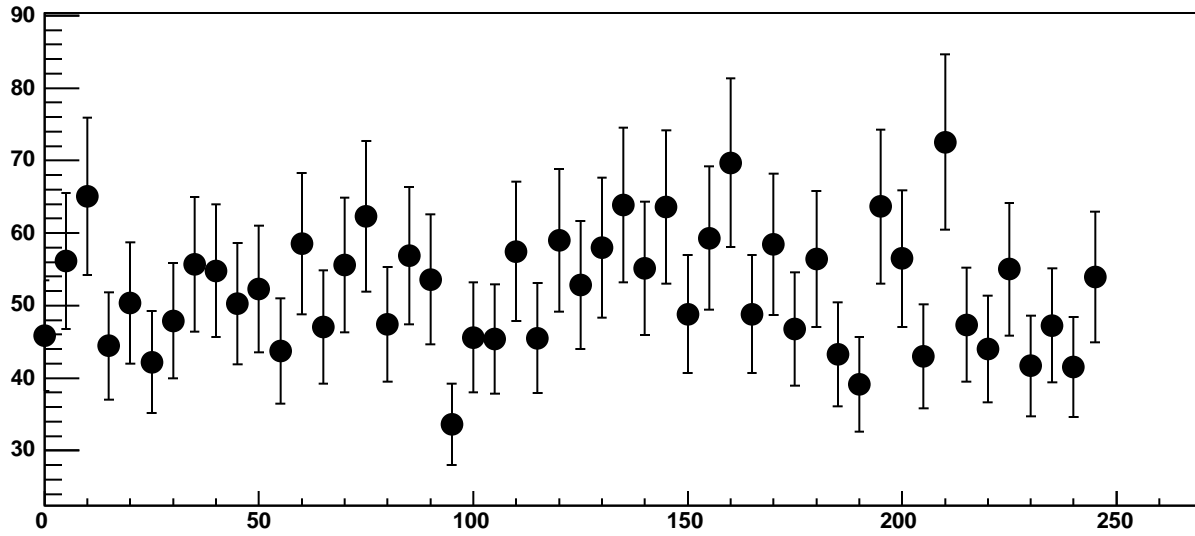


Chip 9, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

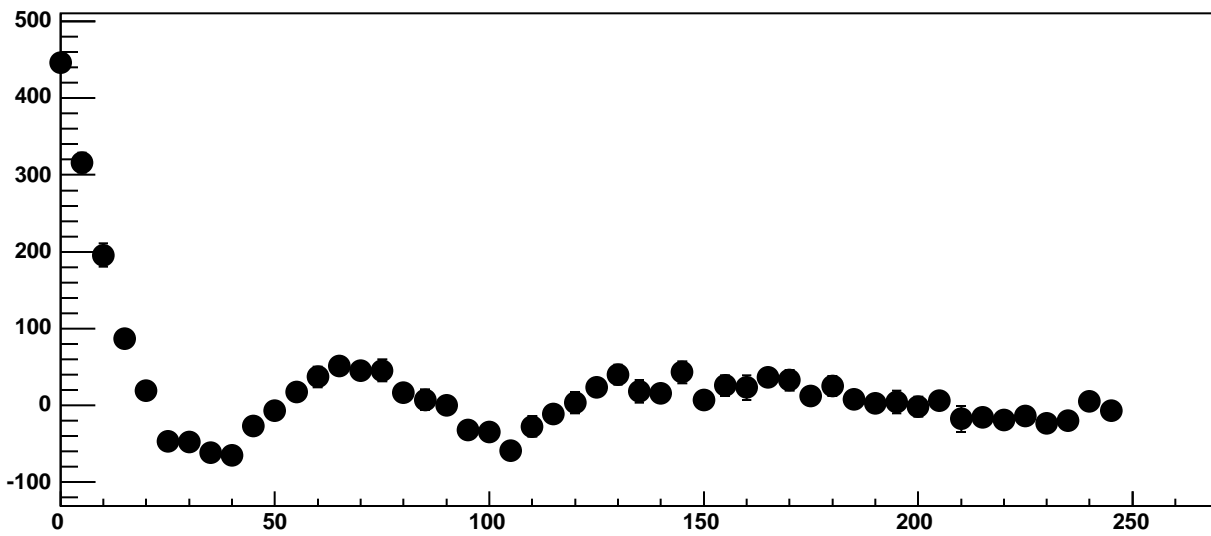


$\chi^2 / \text{ndf}$	368.5 / 41
p0	$-737.7 \pm 3.936$
p1	$97.96 \pm 0.4575$
p2	$-5.671\text{e}+08 \pm 1.423\text{e}+07$
p3	$3.86\text{e}+07 \pm 9.26\text{e}+05$
p4	$13.25 \pm 0.1032$

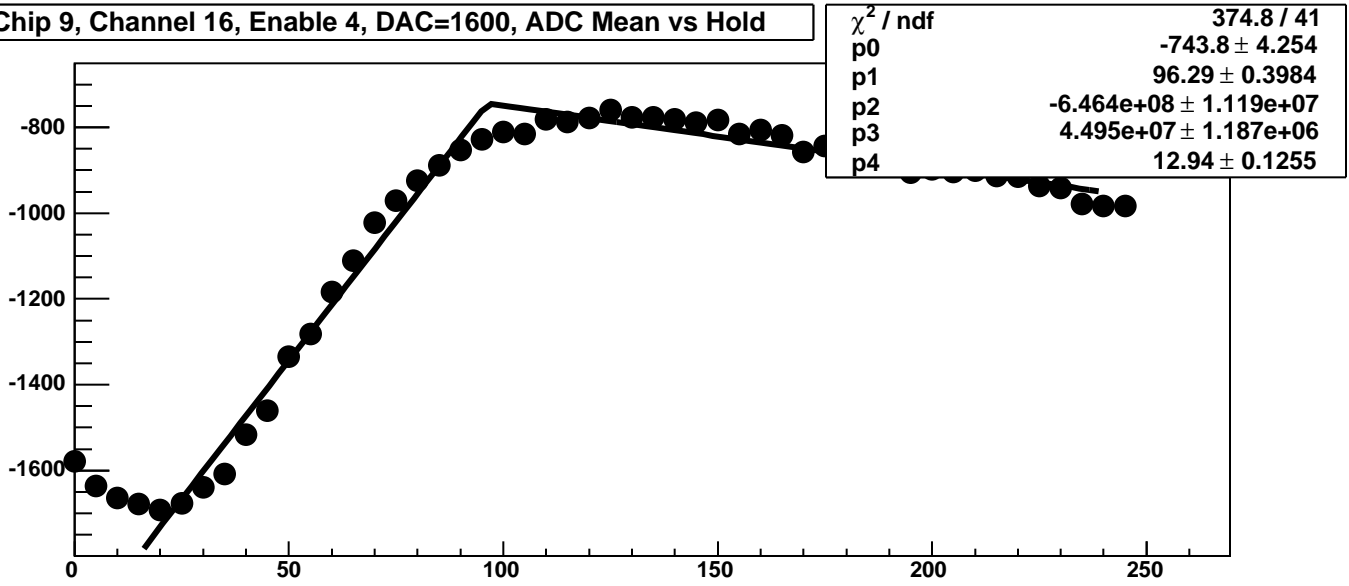
Chip 9, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



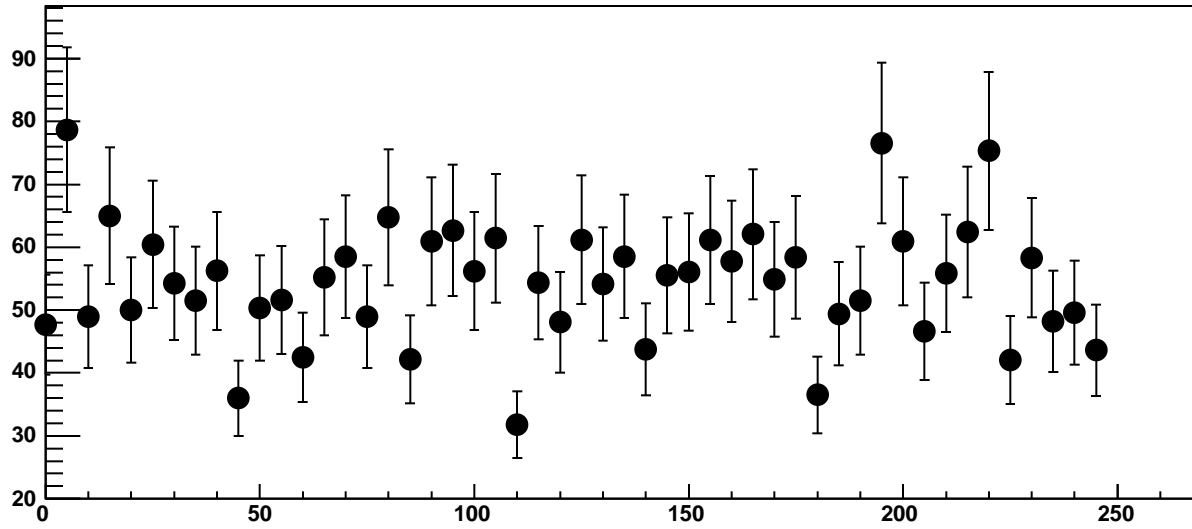
Chip 9, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold



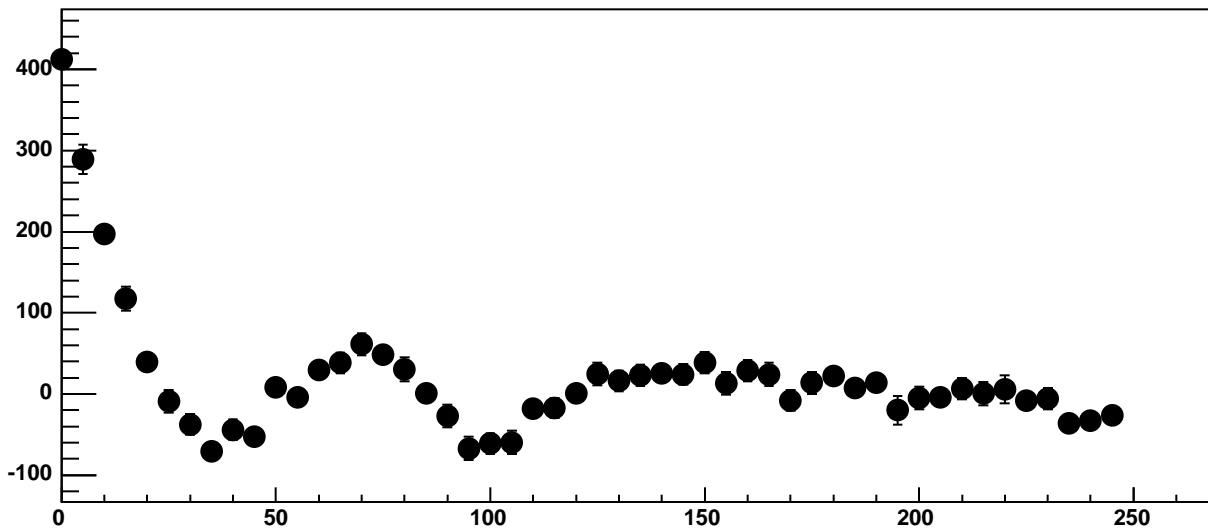
Chip 9, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold



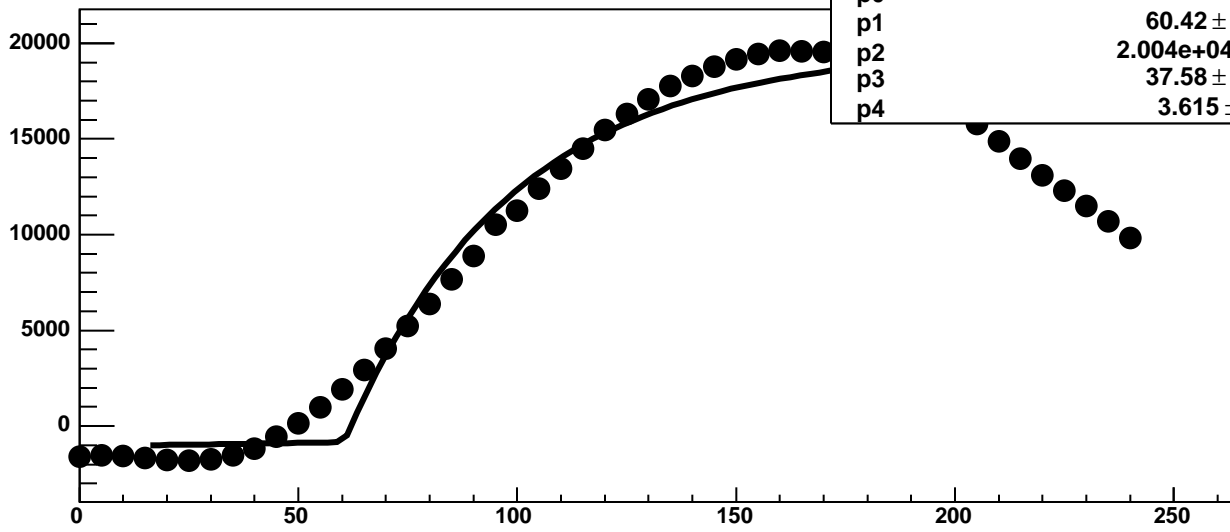
Chip 9, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

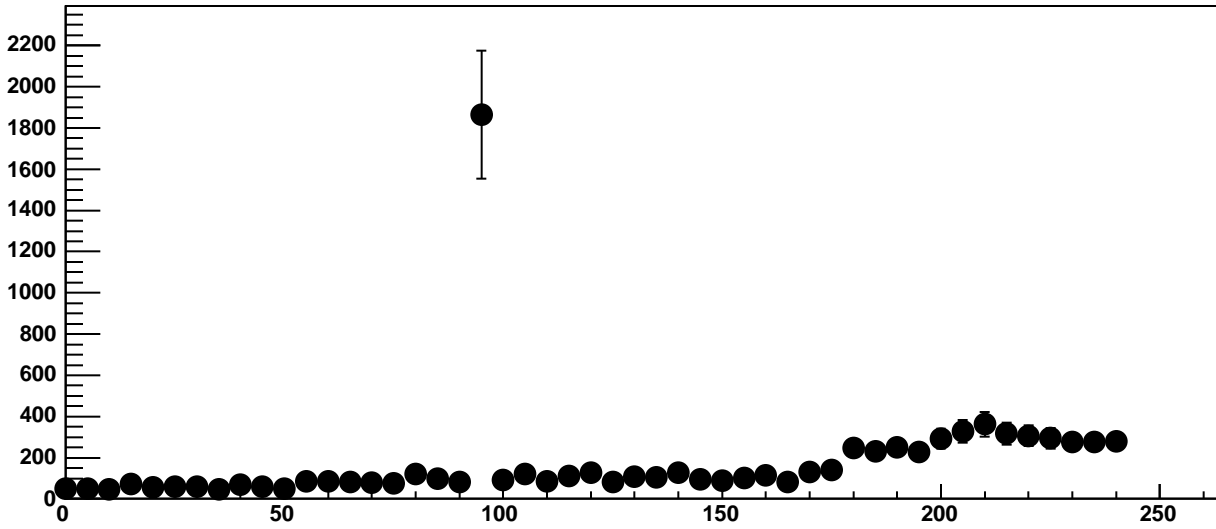


Chip 9, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold

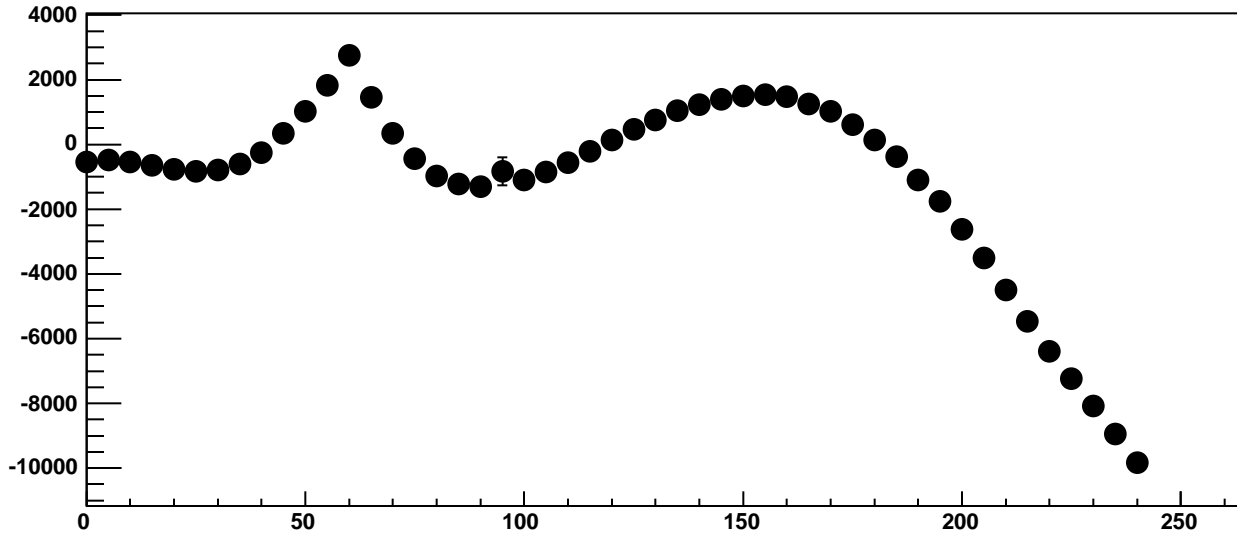


$\chi^2 / \text{ndf}$	1.942e+05 / 41
p0	-843.1 ± 7.535
p1	60.42 ± 0.03442
p2	2.004e+04 ± 41.12
p3	37.58 ± 0.09592
p4	3.615 ± 0.2496

Chip 9, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold

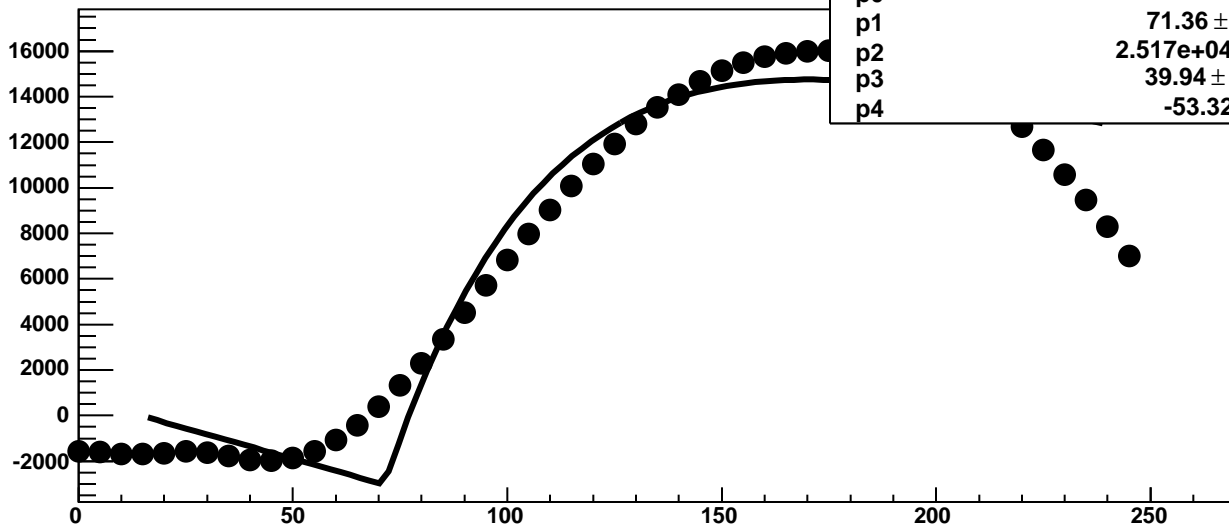


Chip 9, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold



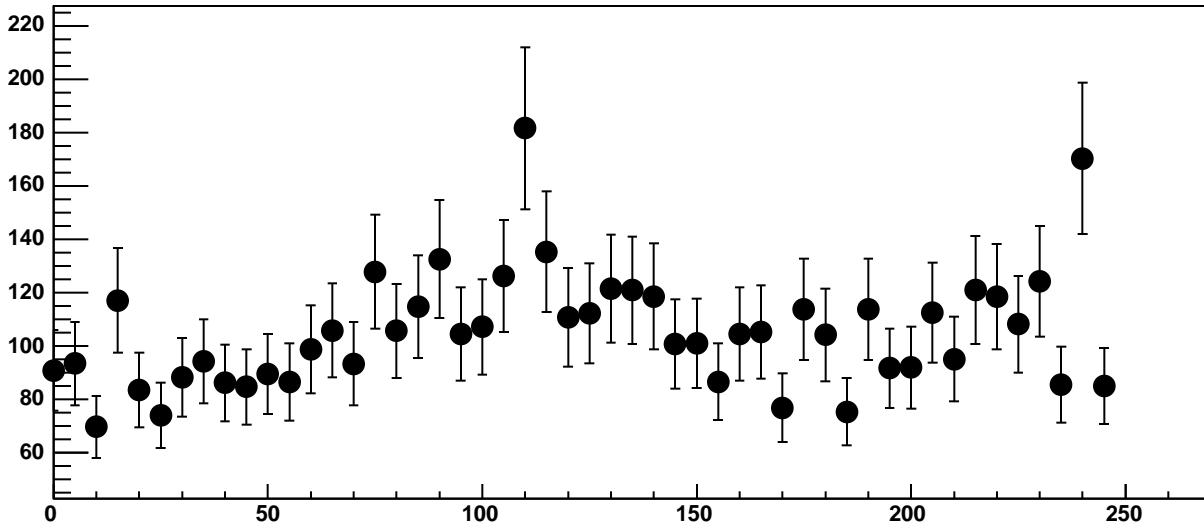


Chip 9, Channel 17, Enable 0, DAC=1600, ADC Mean vs Hold

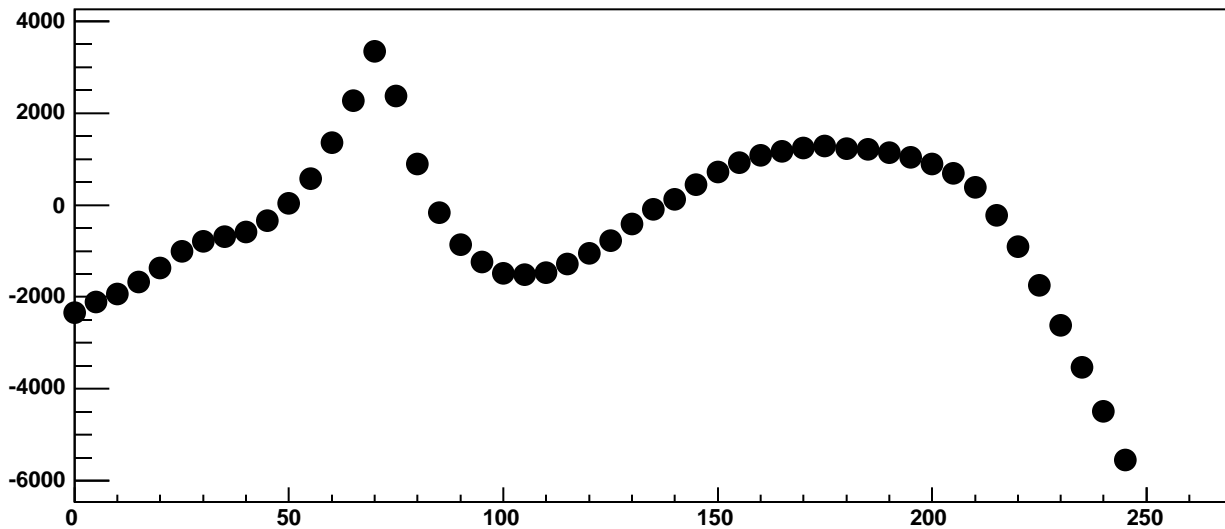


$\chi^2 / \text{ndf}$	1.676e+05 / 41
p0	-3032 ± 8.659
p1	71.36 ± 0.03681
p2	2.517e+04 ± 45.93
p3	39.94 ± 0.09039
p4	-53.32 ± 0.242

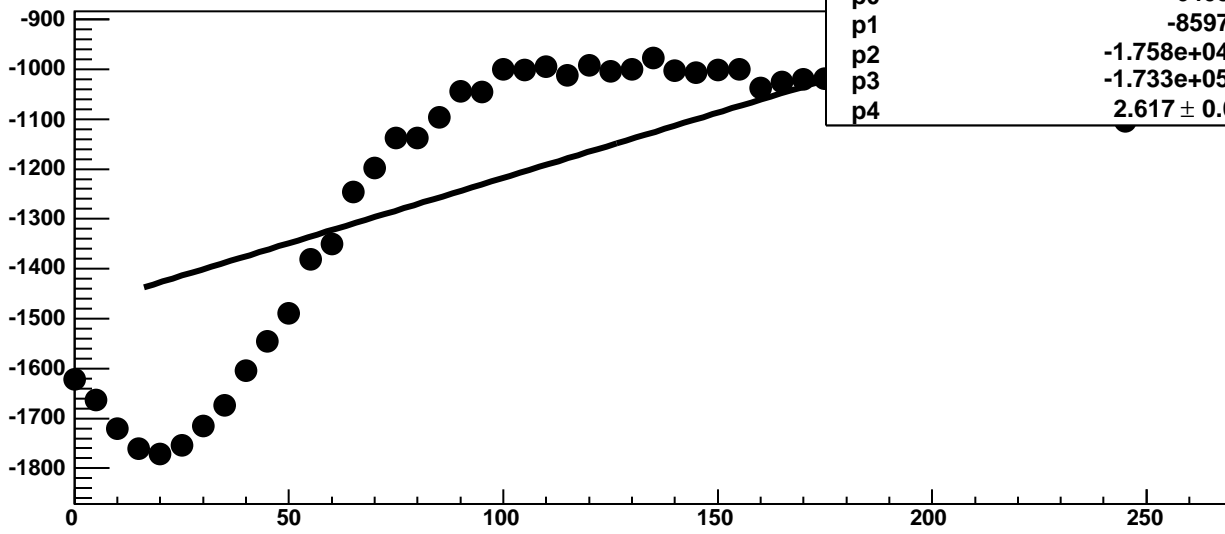
Chip 9, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold

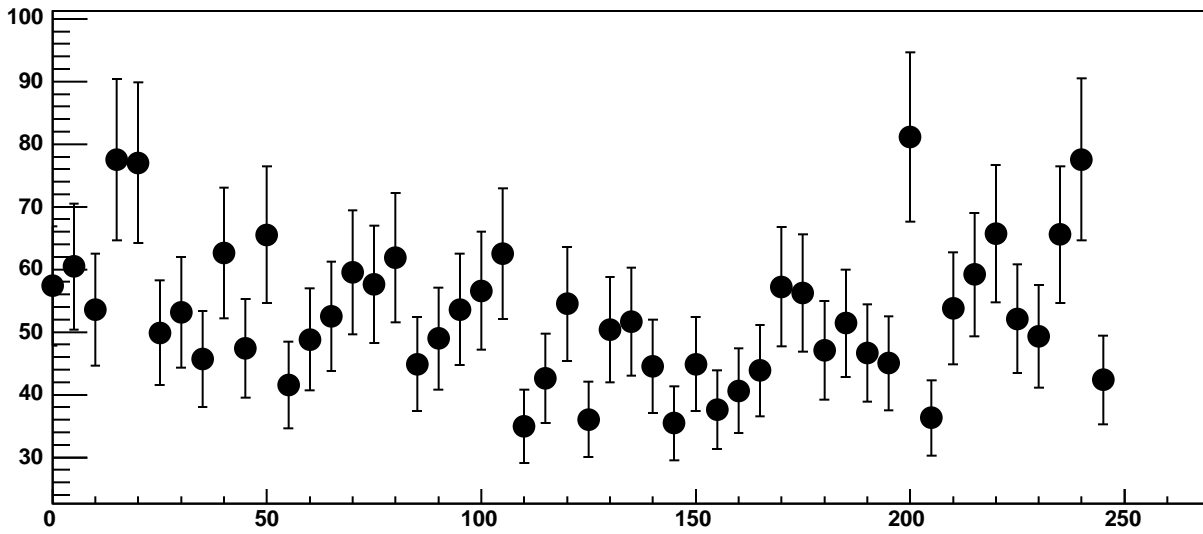


Chip 9, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

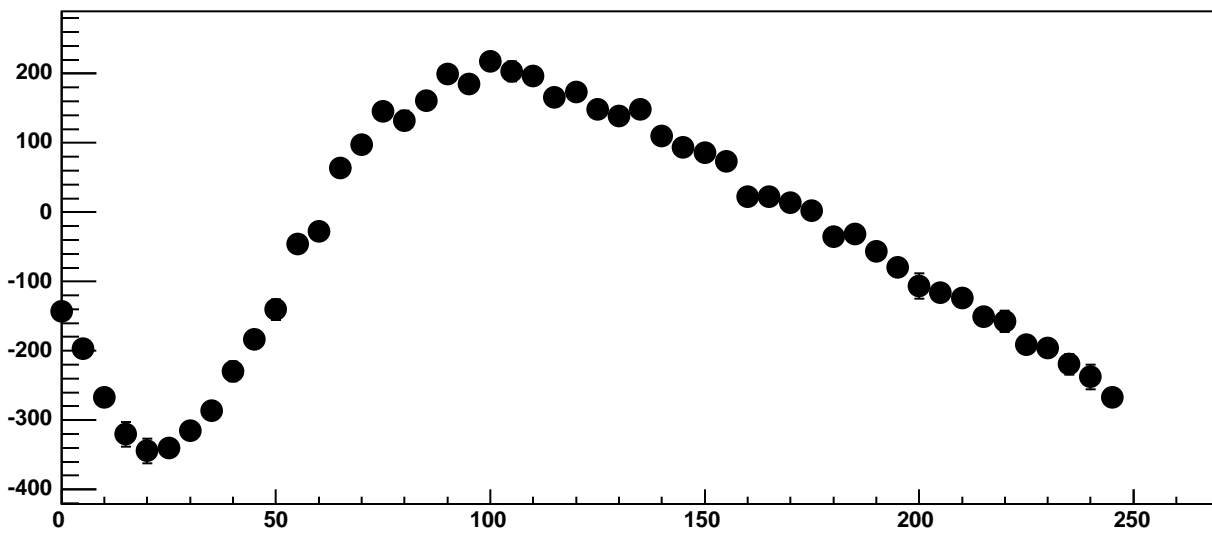


$\chi^2 / \text{ndf}$	8937 / 41
p0	$-6403 \pm 8.488$
p1	$-8597 \pm 2.735$
p2	$-1.758e+04 \pm 10.72$
p3	$-1.733e+05 \pm 365.5$
p4	$2.617 \pm 0.0009726$

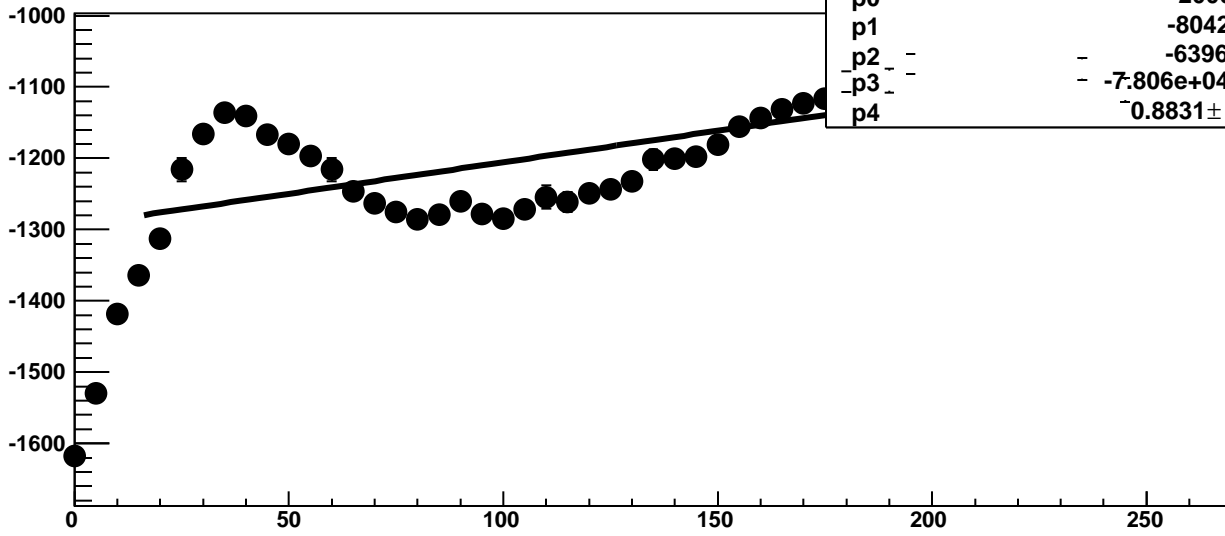
Chip 9, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

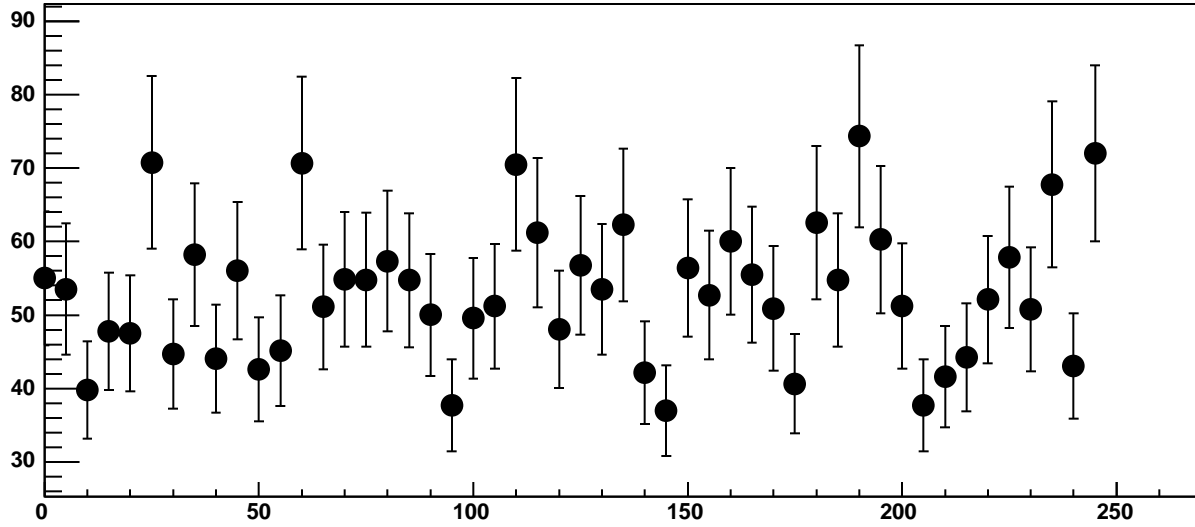


Chip 9, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold

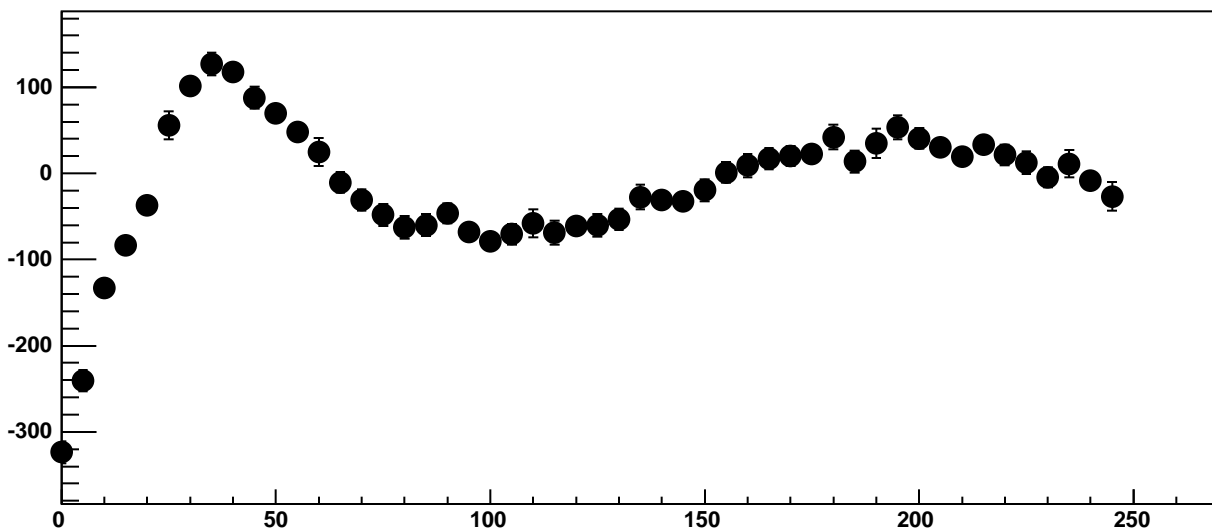


$\chi^2 / \text{ndf}$	980.4 / 41
p0	$-2000 \pm 11.36$
p1	$-8042 \pm 2.203$
p2	$-6396 \pm 6.032$
p3	$-7.806e+04 \pm 703.2$
p4	$0.8831 \pm 0.00139$

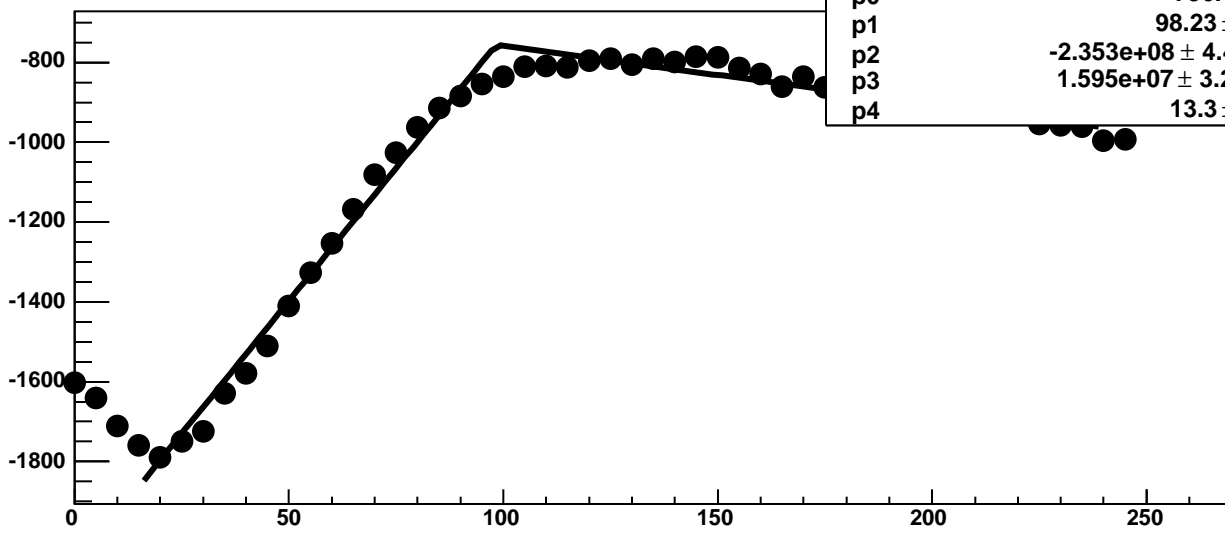
Chip 9, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

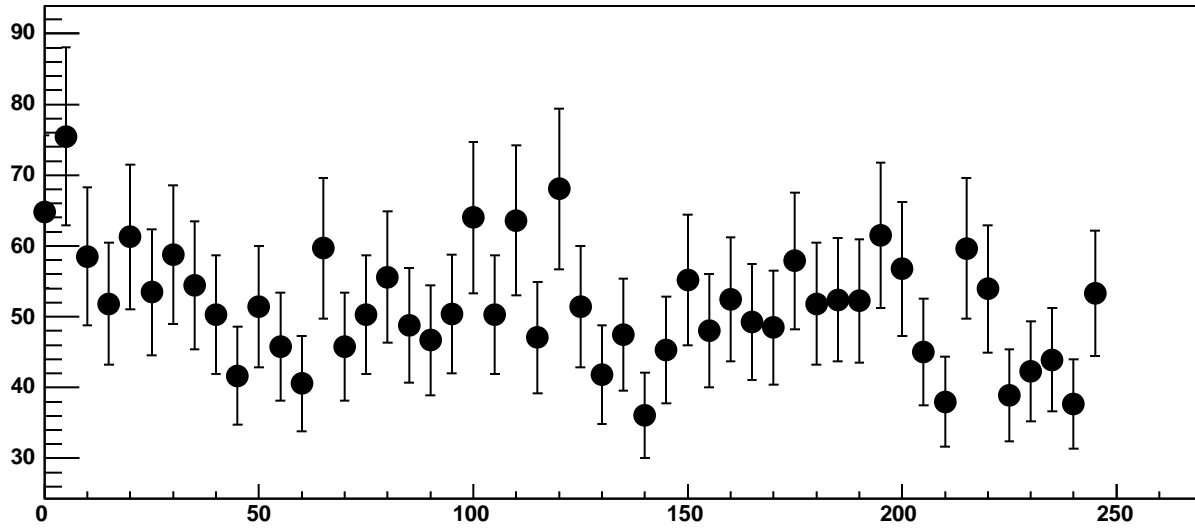


Chip 9, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

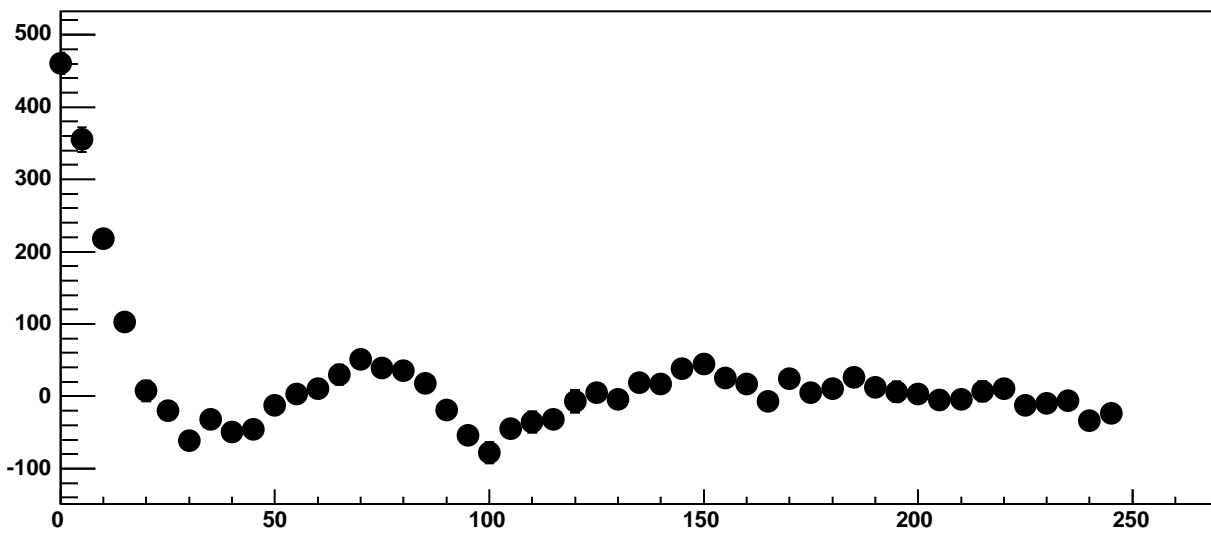


$\chi^2 / \text{ndf}$	354.8 / 41
p0	-756.1 ± 3.771
p1	98.23 ± 0.4489
p2	-2.353e+08 ± 4.453e+06
p3	1.595e+07 ± 3.265e+05
p4	13.3 ± 0.1068

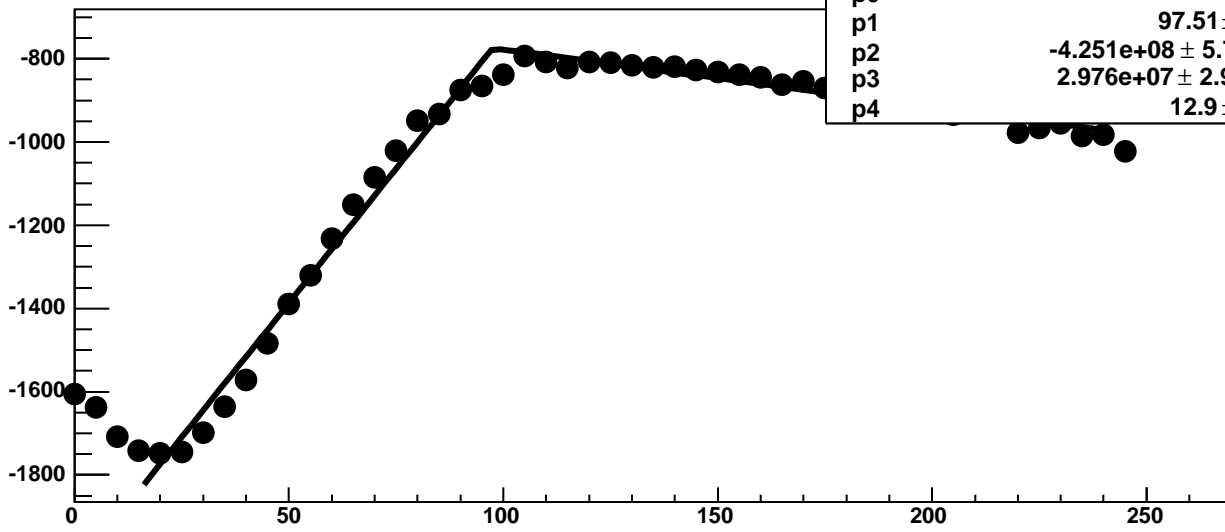
Chip 9, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold

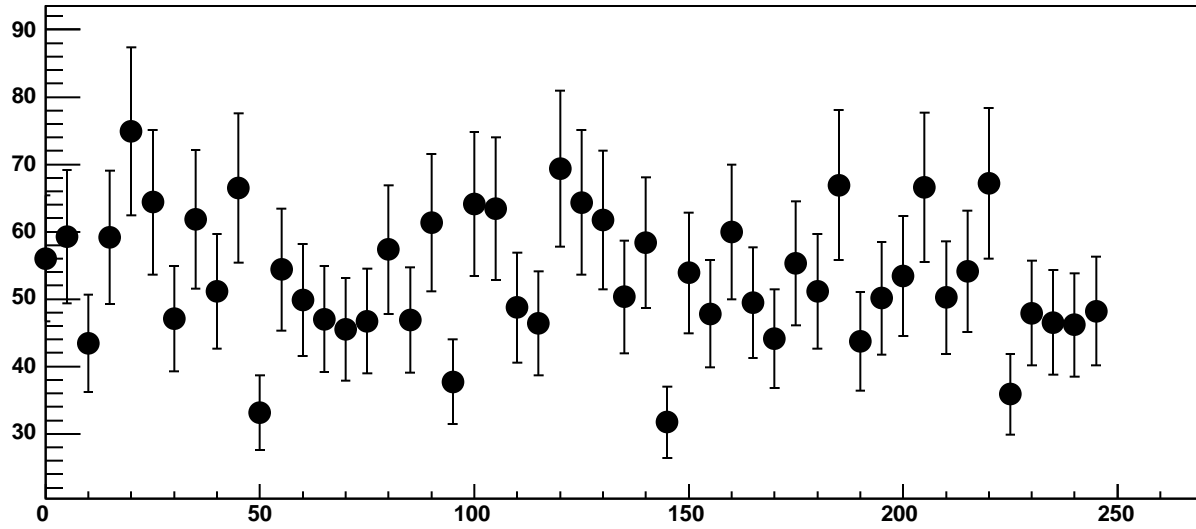


Chip 9, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

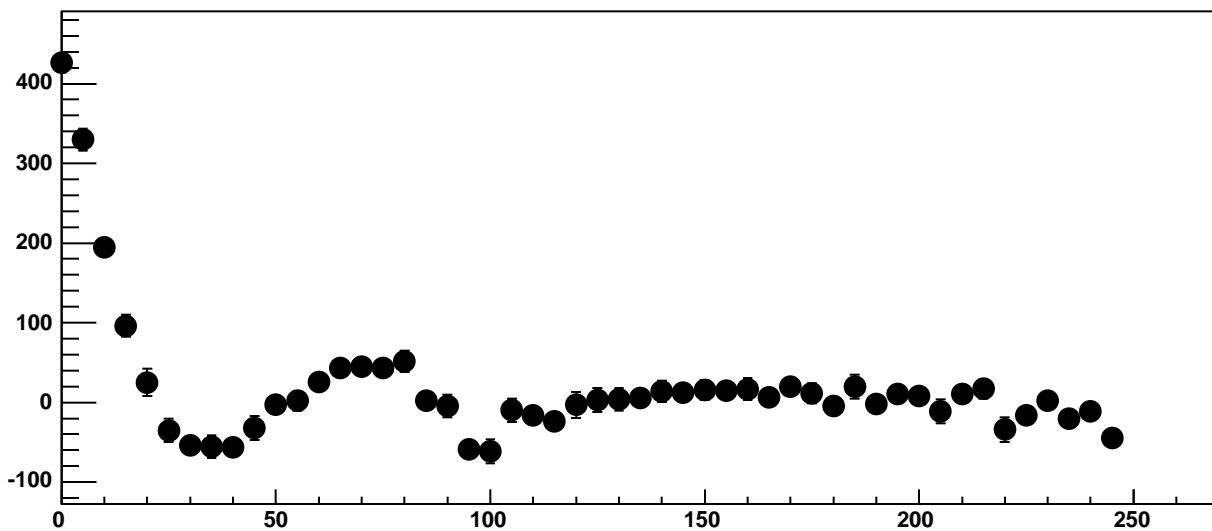


$\chi^2 / \text{ndf}$	302.1 / 41
p0	-774.1 ± 4.114
p1	97.51 ± 0.4902
p2	-4.251e+08 ± 5.768e+06
p3	2.976e+07 ± 2.978e+05
p4	12.9 ± 0.1194

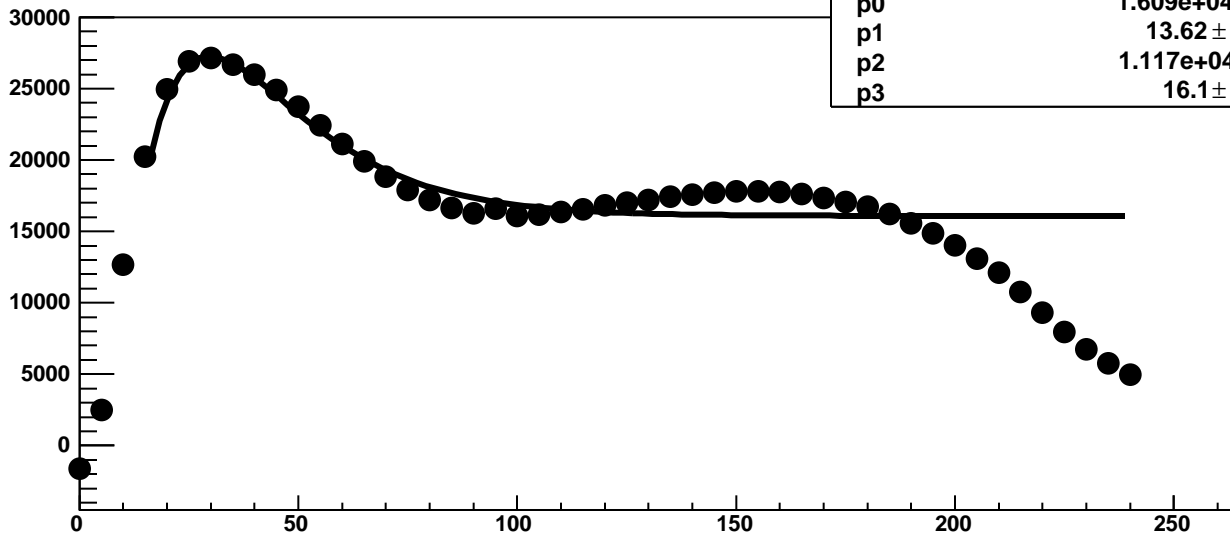
Chip 9, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

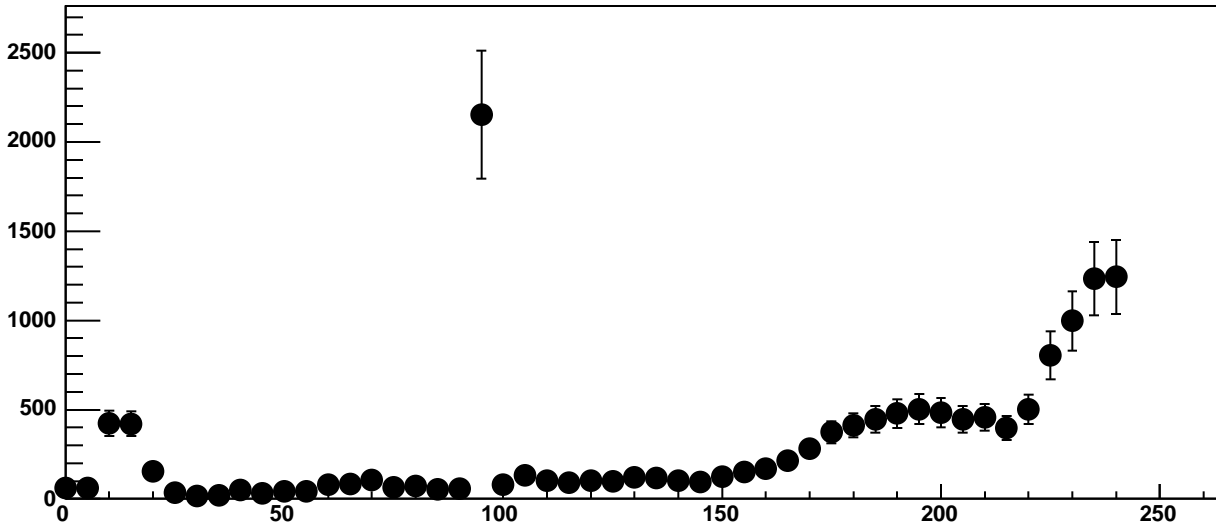


Chip 9, Channel 17, Enable 5!, DAC=1600, ADC Mean vs Hold

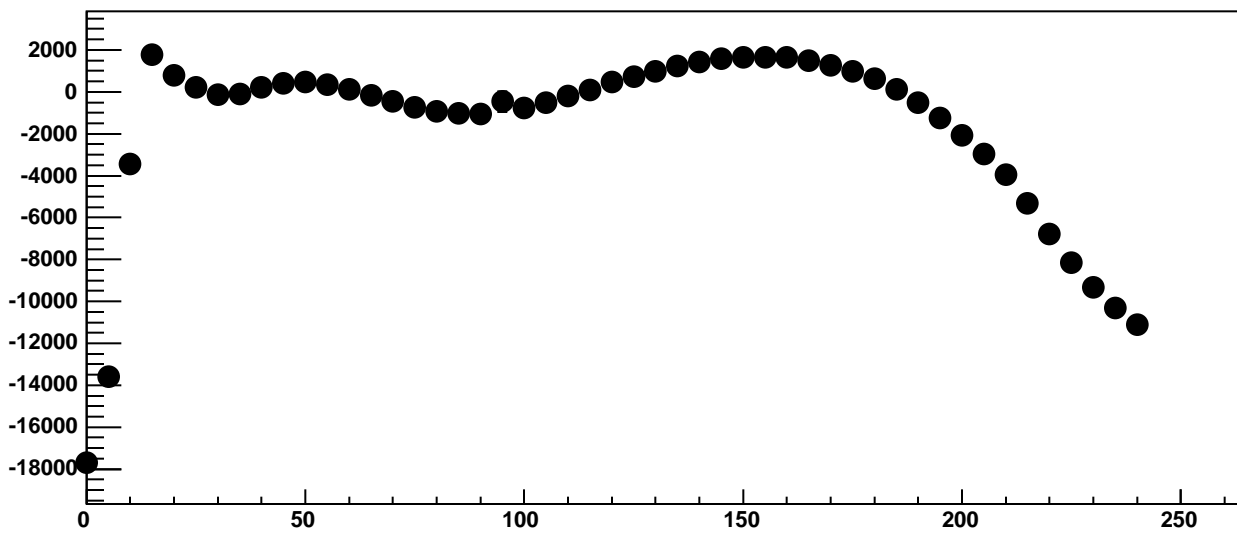


$\chi^2 / \text{ndf}$	7.027e+04 / 42
p0	1.609e+04 $\pm$ 6.504
p1	13.62 $\pm$ 0.02674
p2	1.117e+04 $\pm$ 6.843
p3	16.1 $\pm$ 0.01784

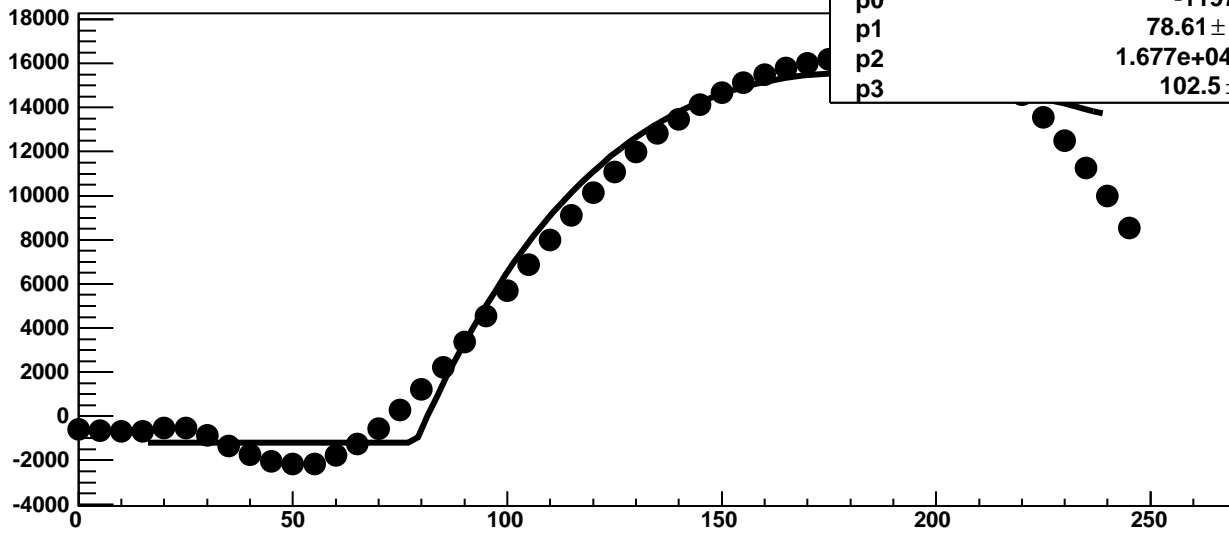
Chip 9, Channel 17, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 9, Channel 17, Enable 5!, DAC=1600, ADC Residuals vs Hold

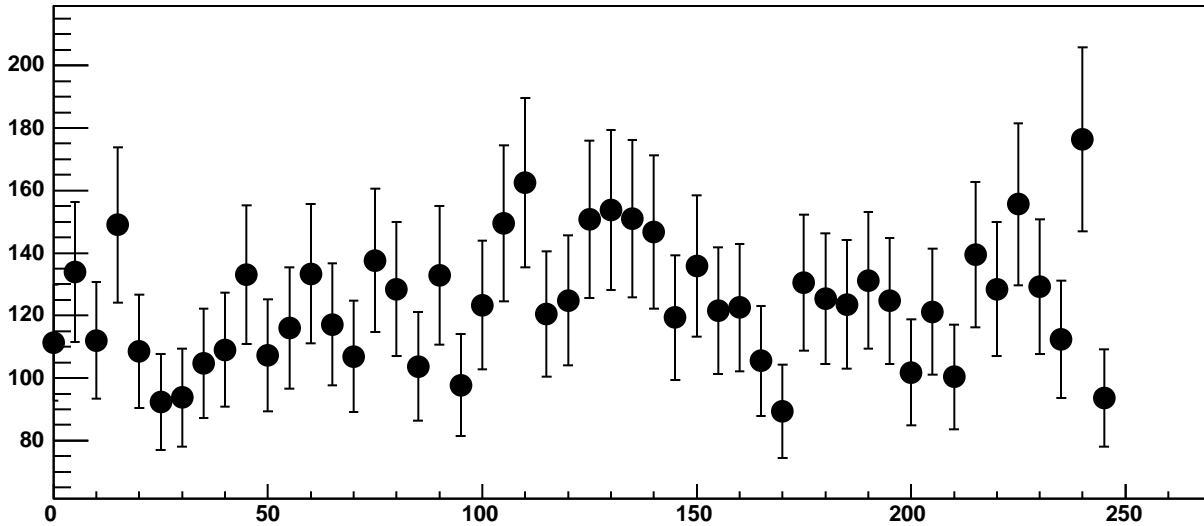


Chip 10, Channel 0, Enable 0!, DAC=1600, ADC Mean vs Hold

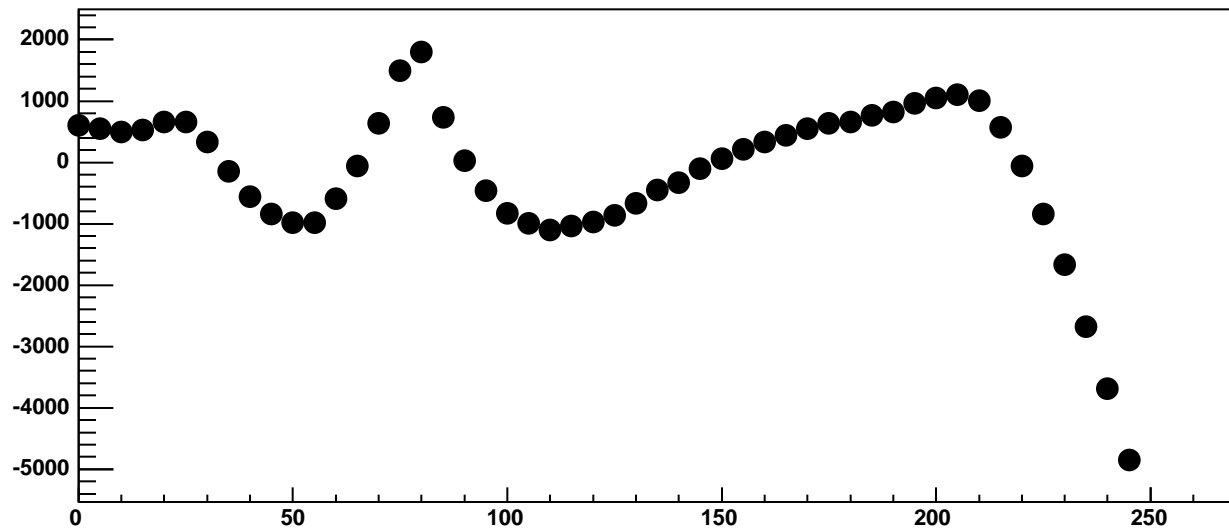


$\chi^2 / \text{ndf}$	5.459e+04 / 42
p0	-1197 $\pm$ 7.115
p1	78.61 $\pm$ 0.04146
p2	1.677e+04 $\pm$ 9.409
p3	102.5 $\pm$ 0.1289

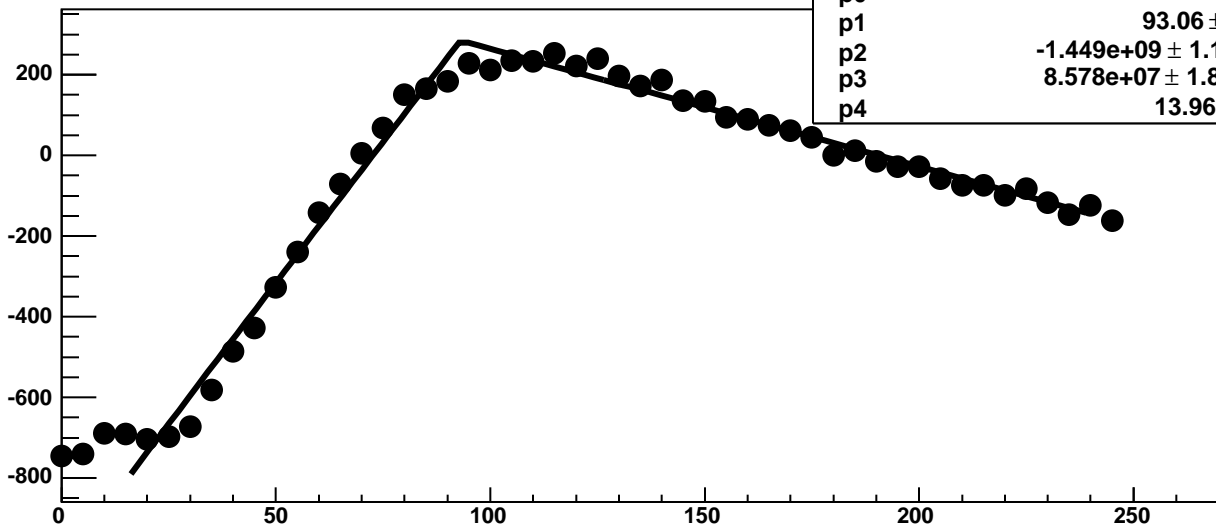
Chip 10, Channel 0, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 0, Enable 0!, DAC=1600, ADC Residuals vs Hold

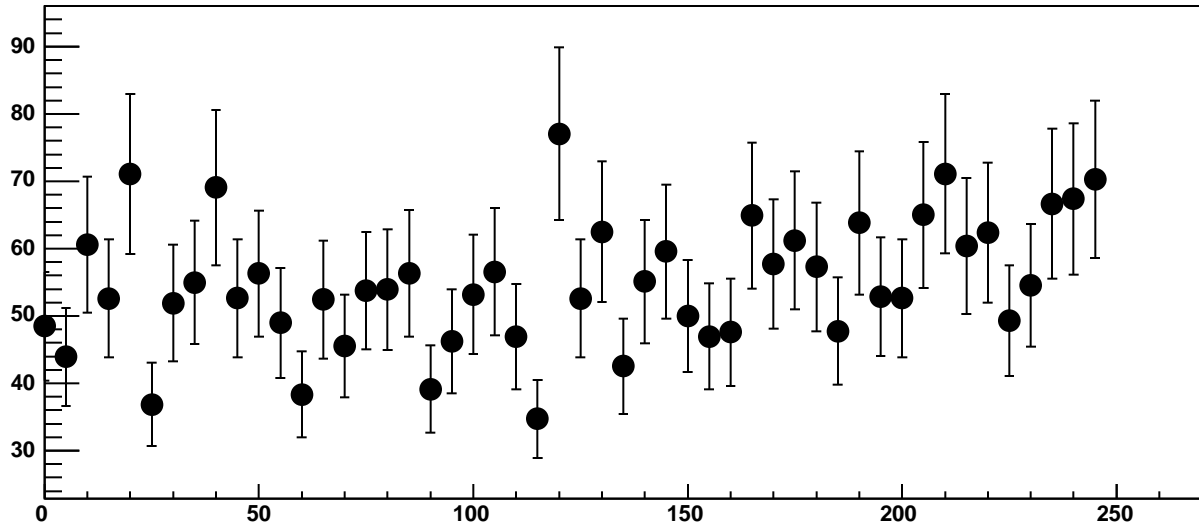


Chip 10, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

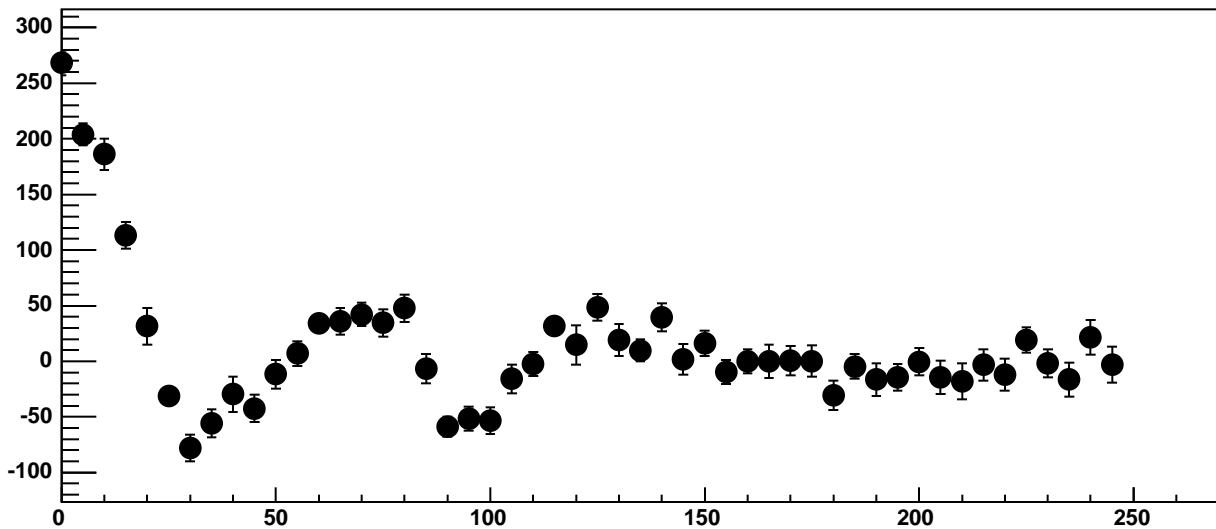


$\chi^2 / \text{ndf}$	400.4 / 41
p0	$285.3 \pm 3.615$
p1	$93.06 \pm 0.4117$
p2	$-1.449\text{e}+09 \pm 1.181\text{e}+07$
p3	$8.578\text{e}+07 \pm 1.893\text{e}+05$
p4	$13.96 \pm 0.122$

Chip 10, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold

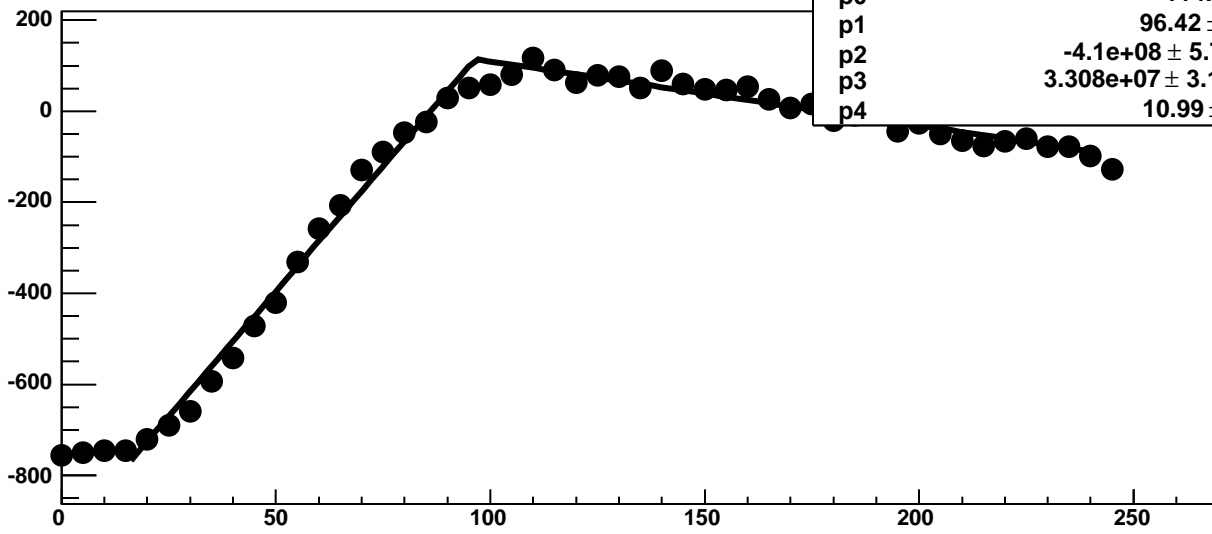


Chip 10, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



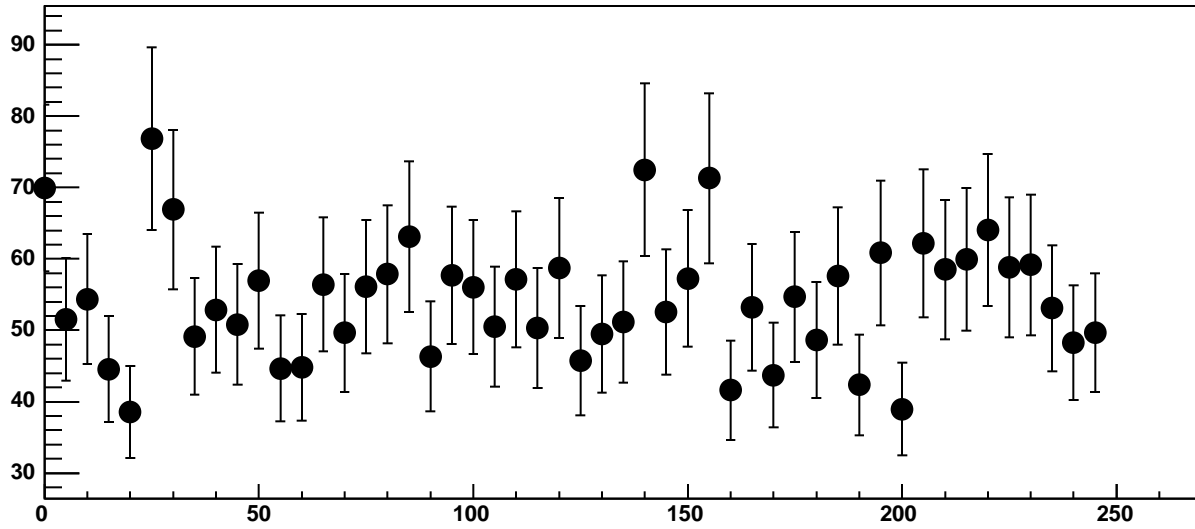


Chip 10, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold

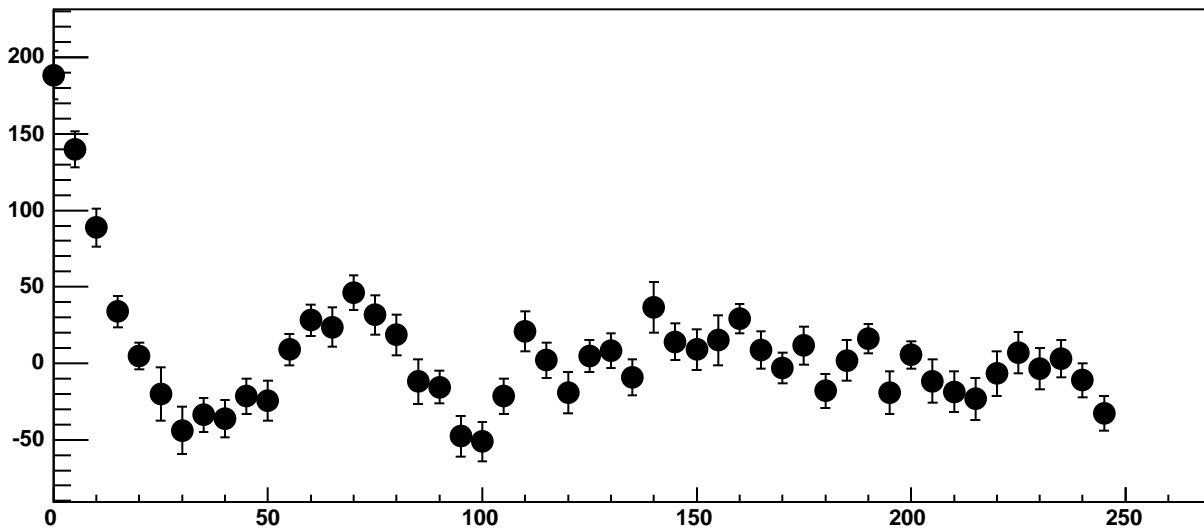


$\chi^2 / \text{ndf}$	155.5 / 41
p0	$114.6 \pm 4.12$
p1	$96.42 \pm 0.5946$
p2	$-4.1e+08 \pm 5.705e+06$
p3	$3.308e+07 \pm 3.106e+05$
p4	$10.99 \pm 0.1158$

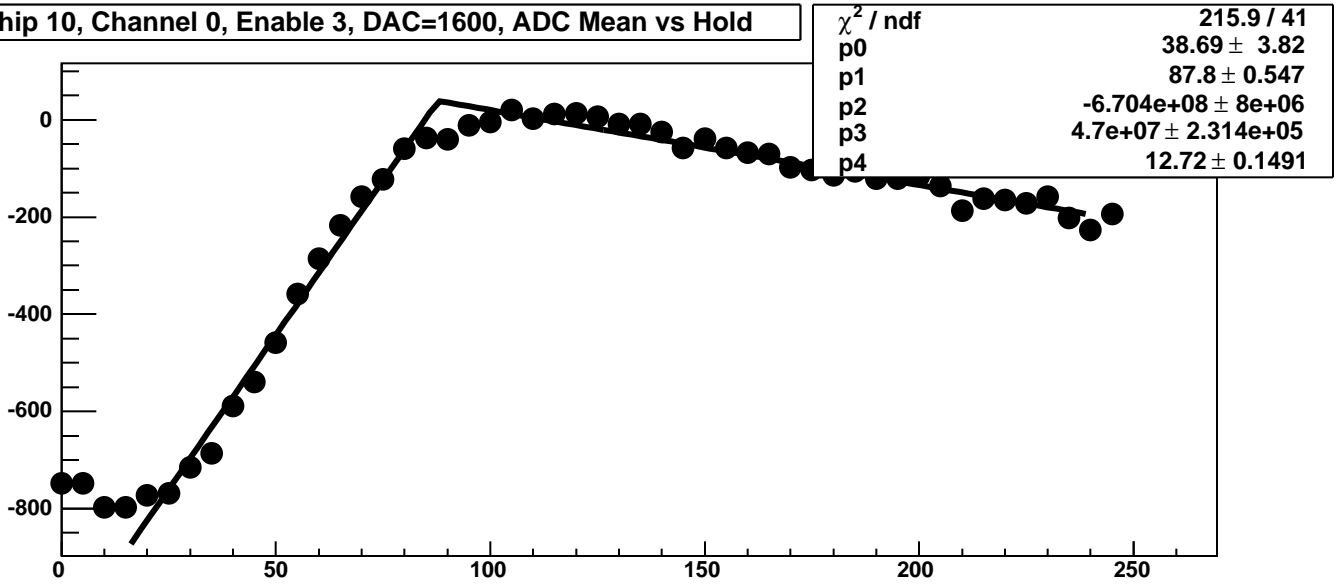
Chip 10, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



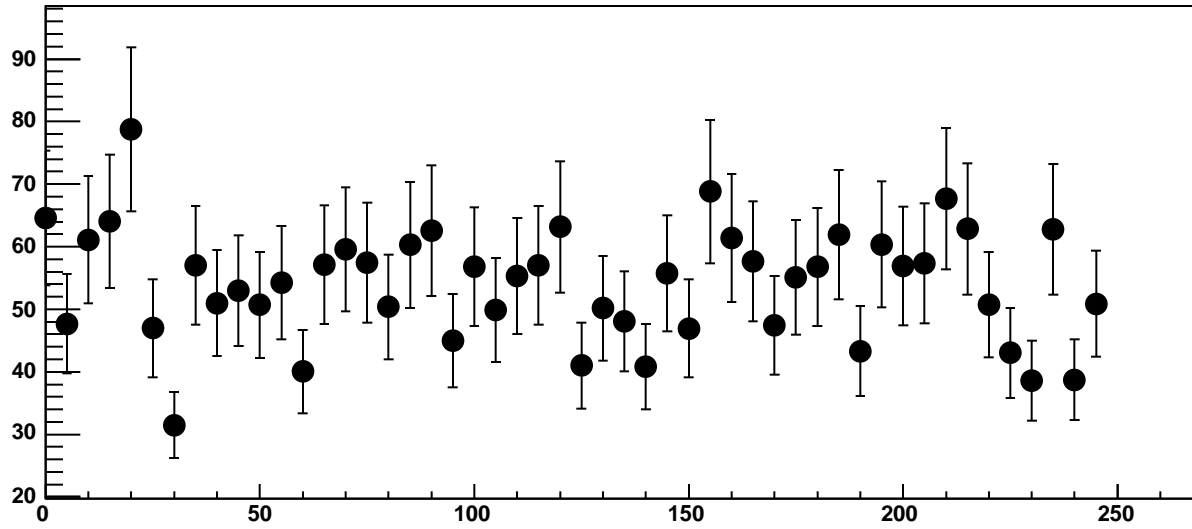
Chip 10, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



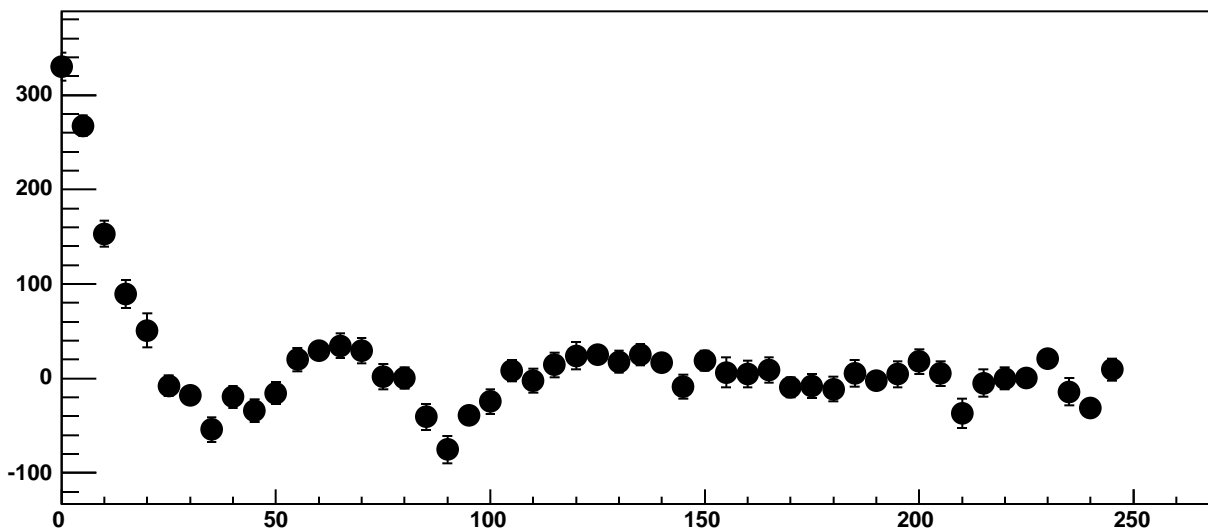
Chip 10, Channel 0, Enable 3, DAC=1600, ADC Mean vs Hold



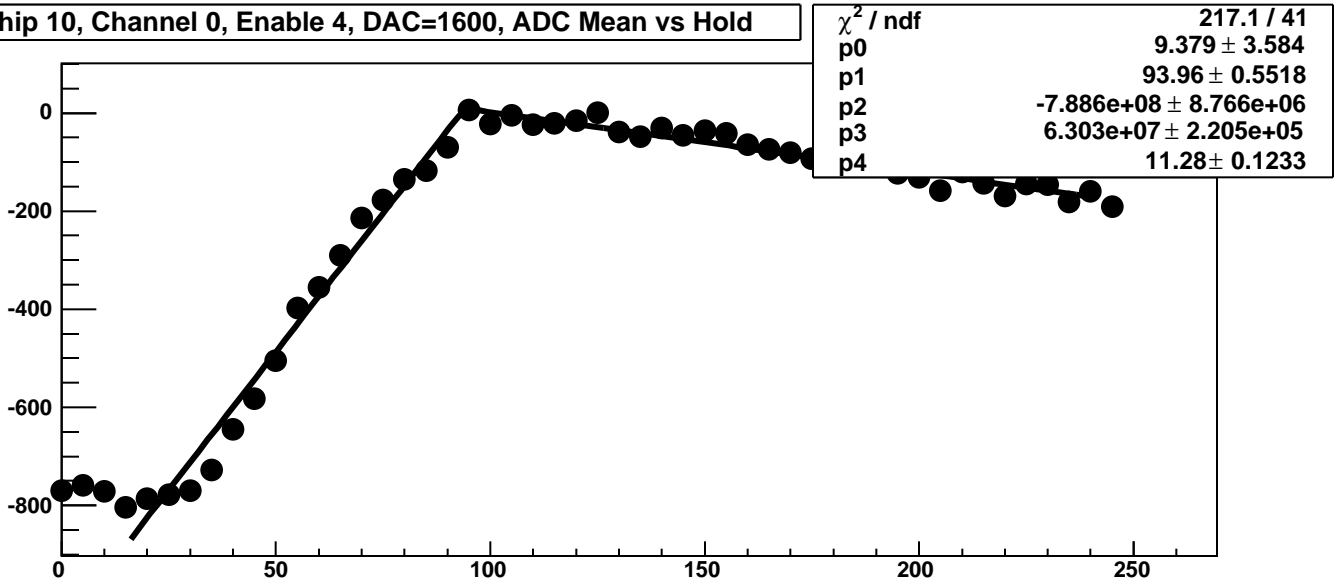
Chip 10, Channel 0, Enable 3, DAC=1600, ADC Noise vs Hold



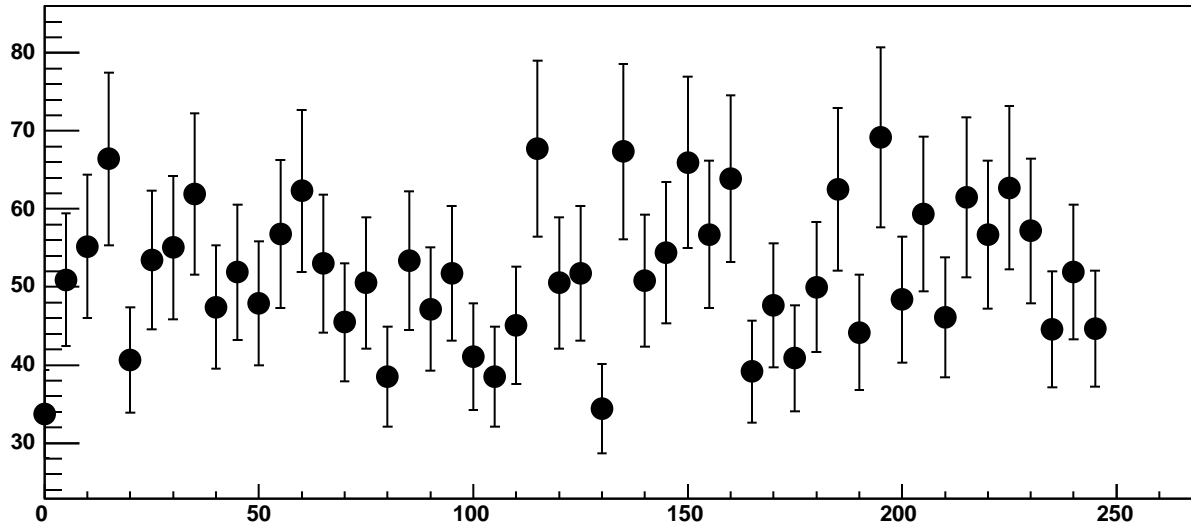
Chip 10, Channel 0, Enable 3, DAC=1600, ADC Residuals vs Hold



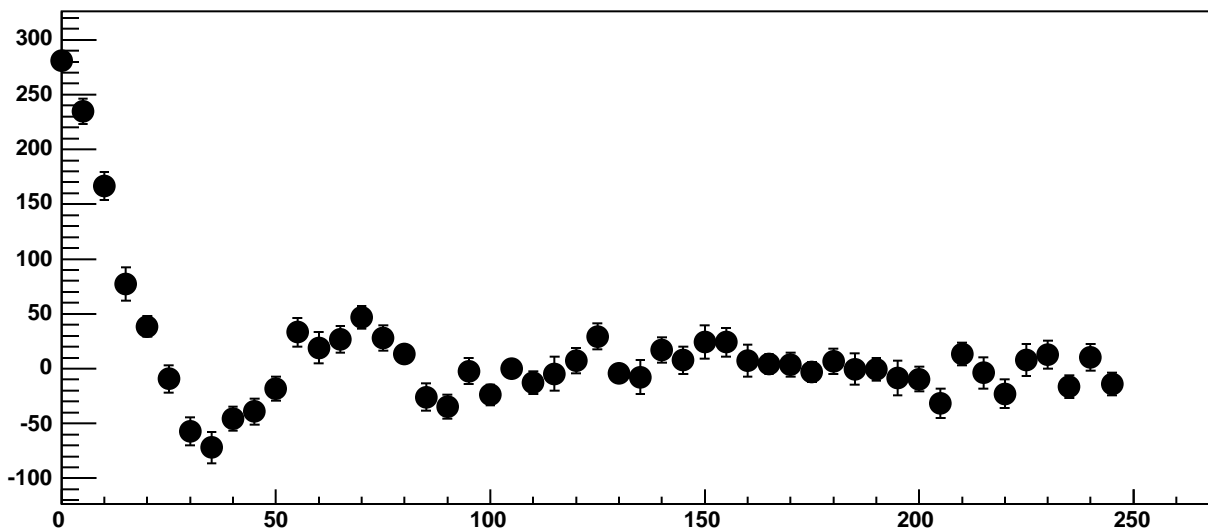
Chip 10, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold



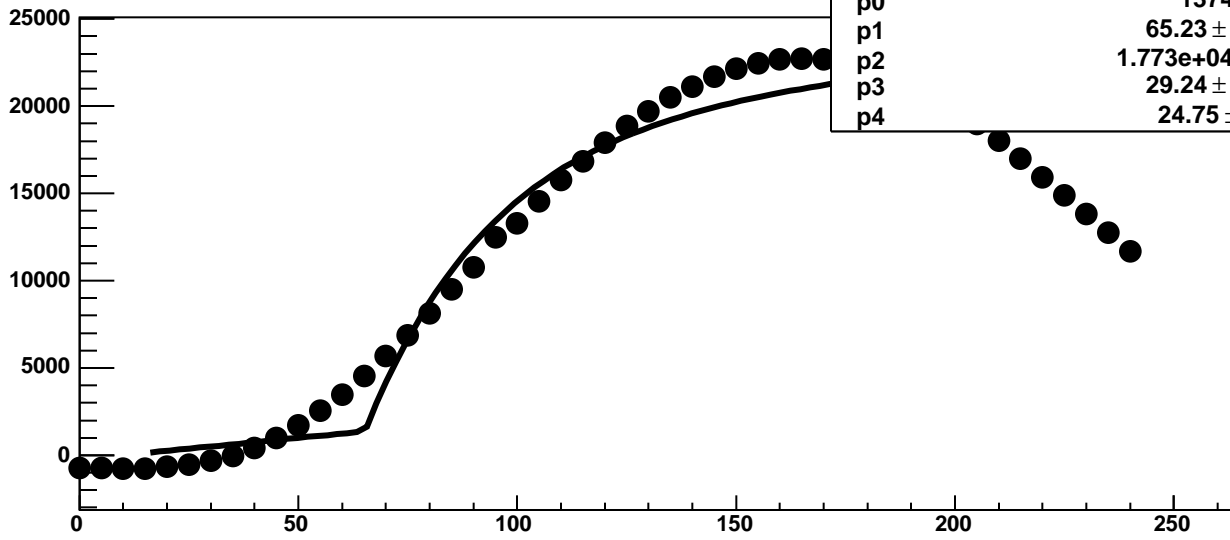
Chip 10, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

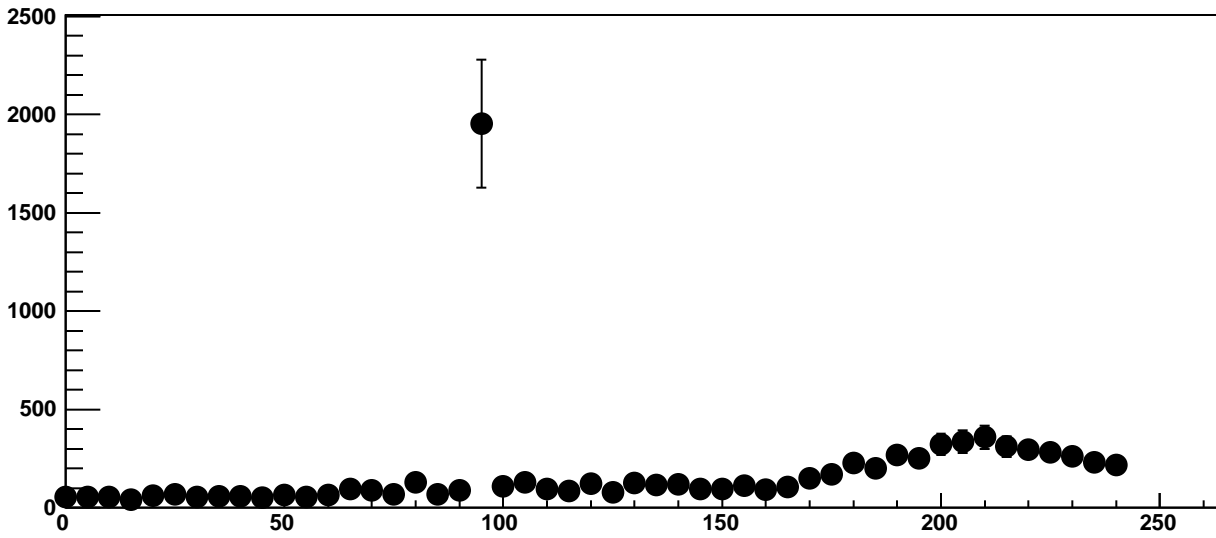


Chip 10, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

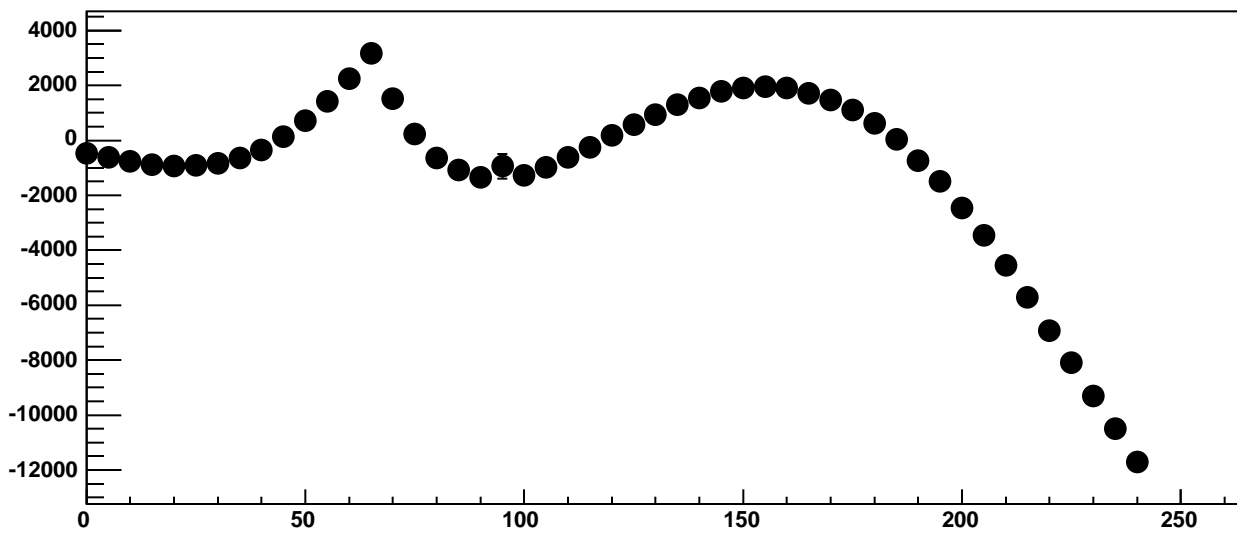


$\chi^2 / \text{ndf}$	2.996e+05 / 41
p0	1374 ± 7.318
p1	65.23 ± 0.03166
p2	1.773e+04 ± 29.96
p3	29.24 ± 0.06877
p4	24.75 ± 0.1956

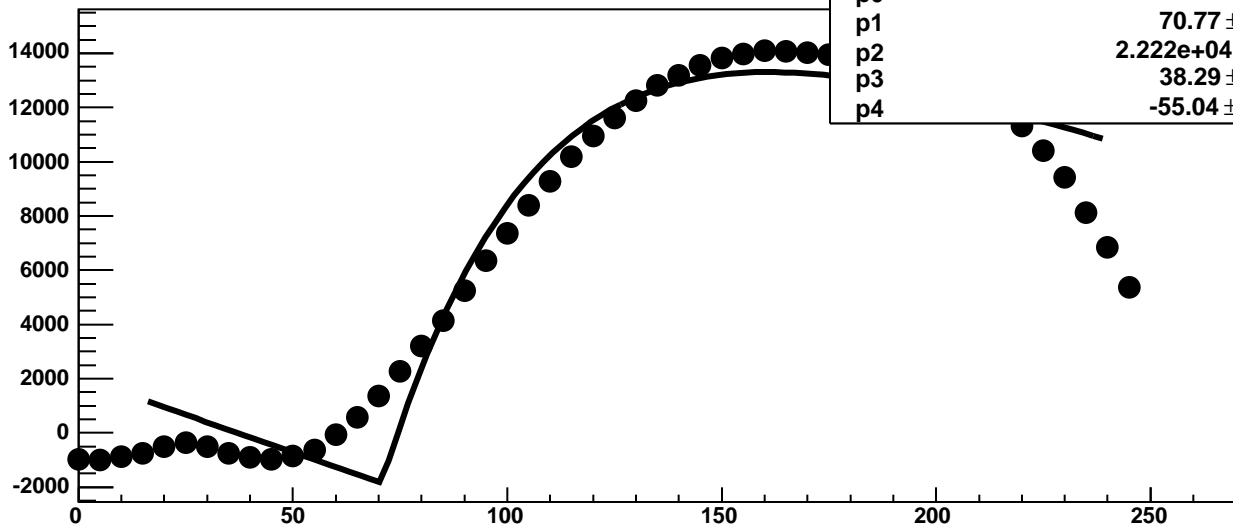
Chip 10, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

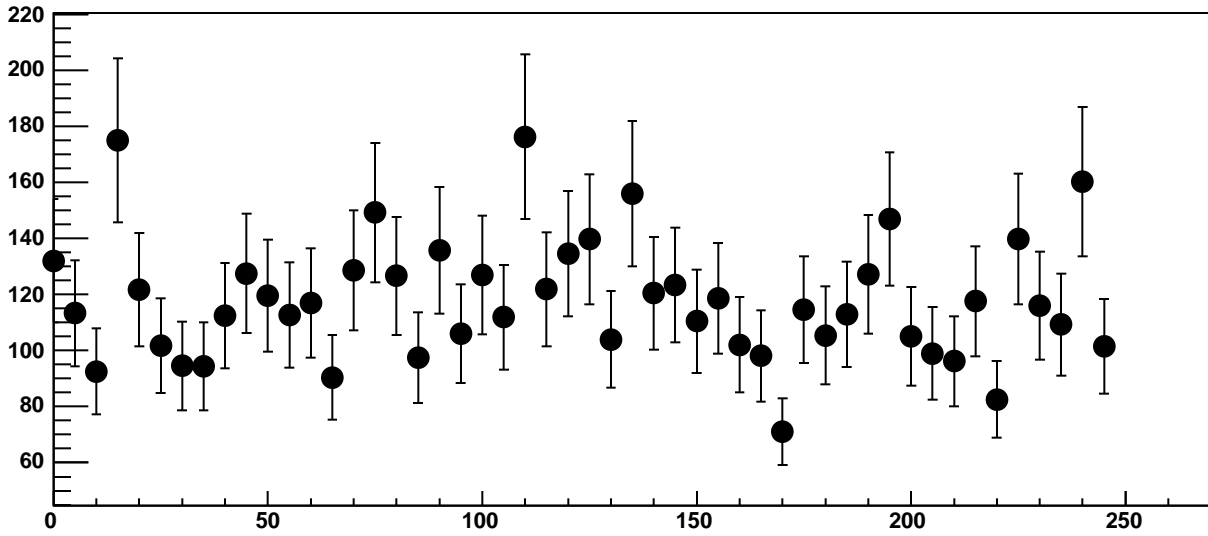


Chip 10, Channel 1, Enable 0, DAC=1600, ADC Mean vs Hold

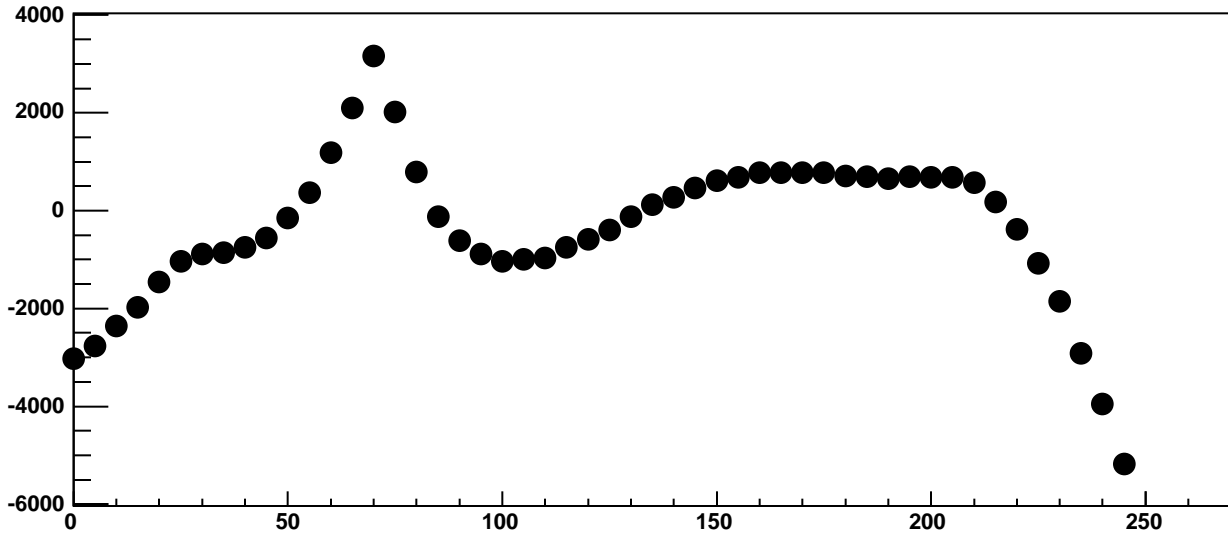


$\chi^2 / \text{ndf}$	8.936e+04 / 41
p0	-1848 ± 9.593
p1	70.77 ± 0.0473
p2	2.222e+04 ± 51.46
p3	38.29 ± 0.1145
p4	-55.04 ± 0.2754

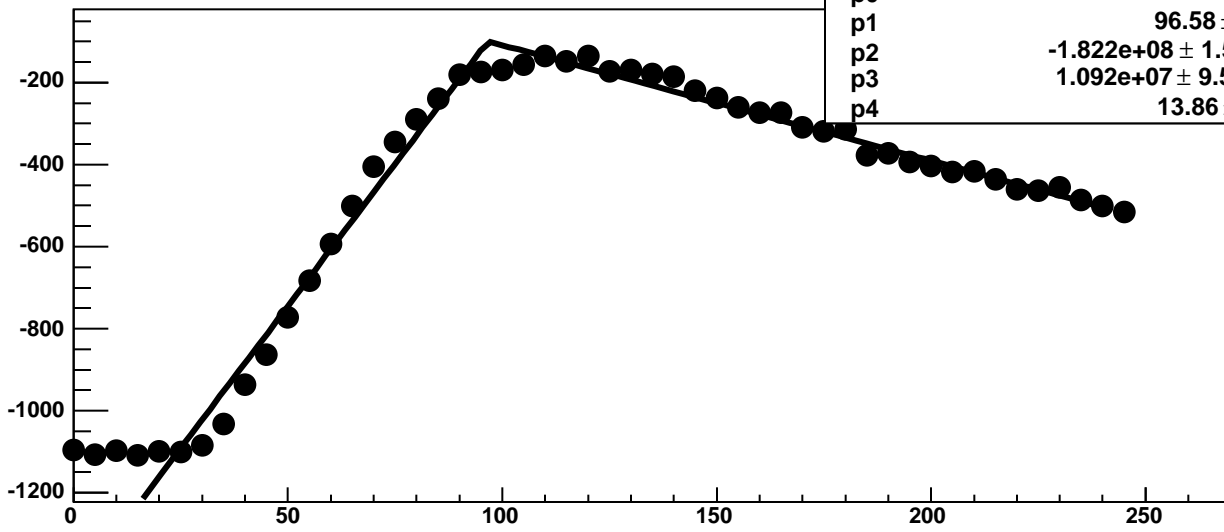
Chip 10, Channel 1, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 1, Enable 0, DAC=1600, ADC Residuals vs Hold

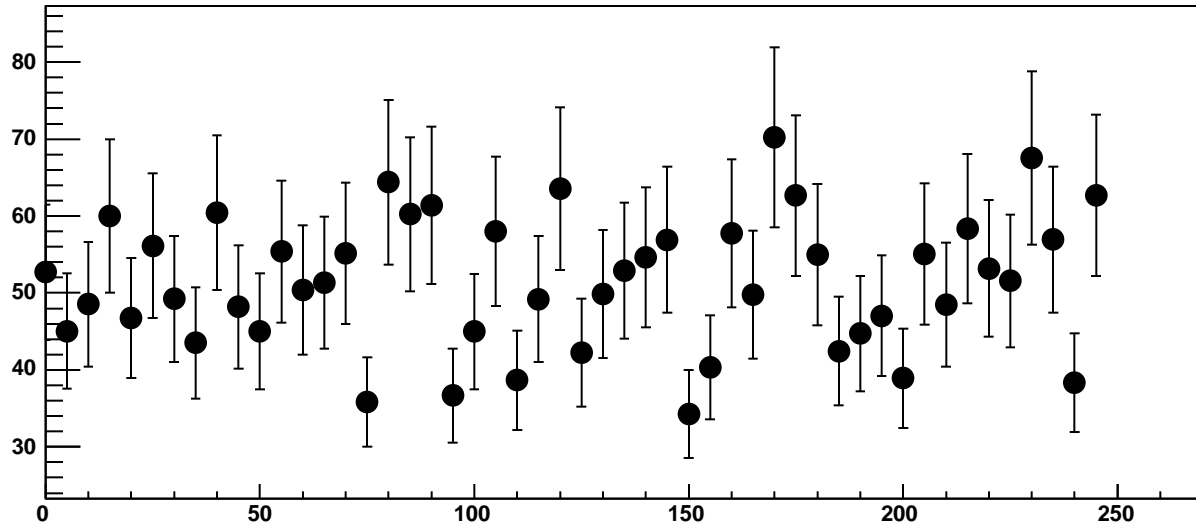


Chip 10, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold

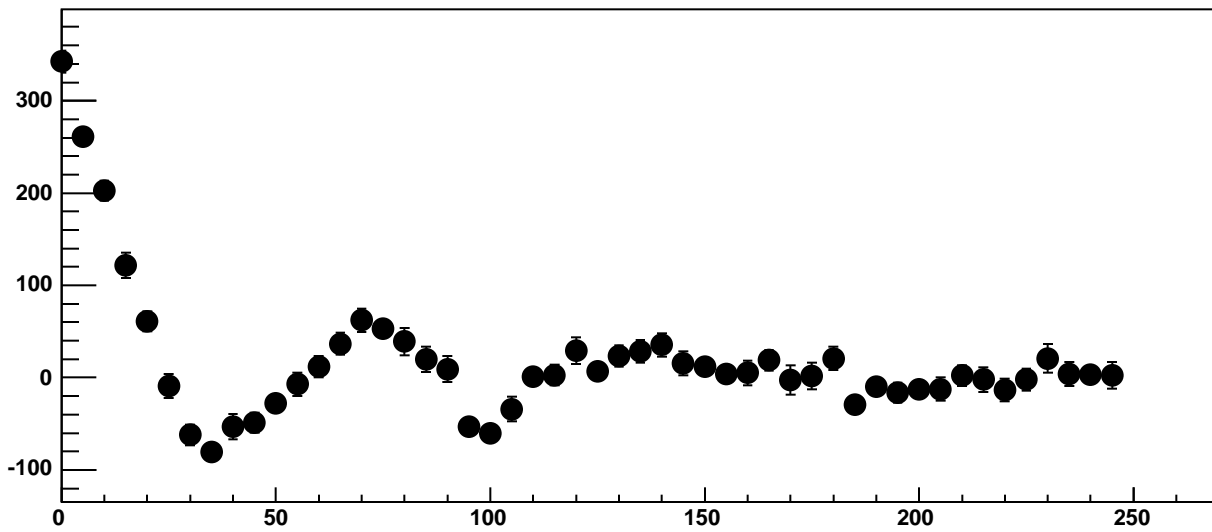


$\chi^2 / \text{ndf}$	467.6 / 41
p0	-99.02 ± 3.538
p1	96.58 ± 0.3992
p2	-1.822e+08 ± 1.593e+07
p3	1.092e+07 ± 9.522e+05
p4	13.86 ± 0.1117

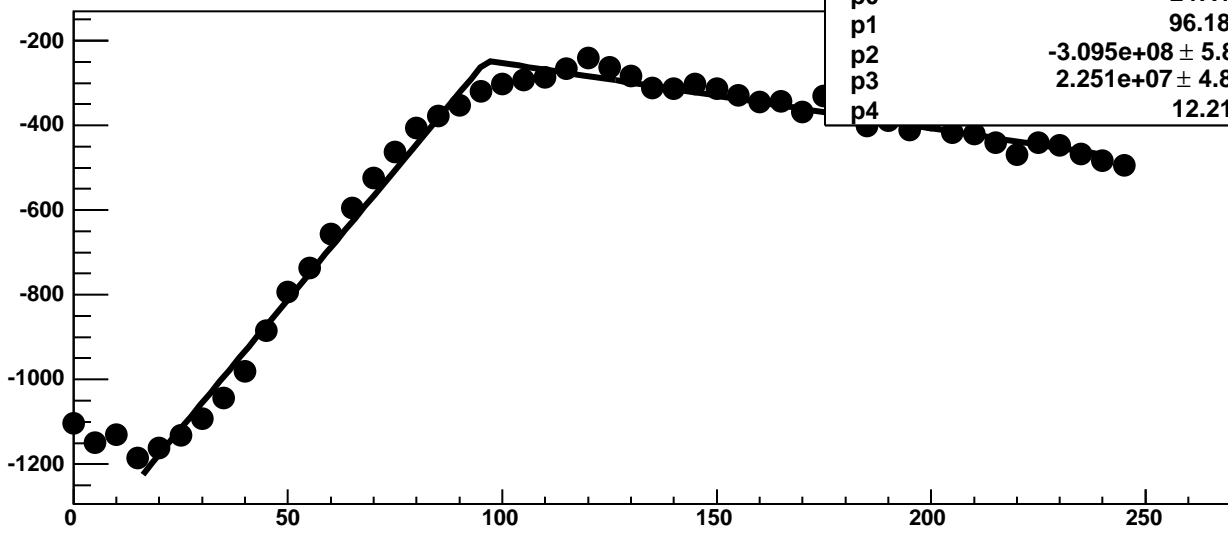
Chip 10, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



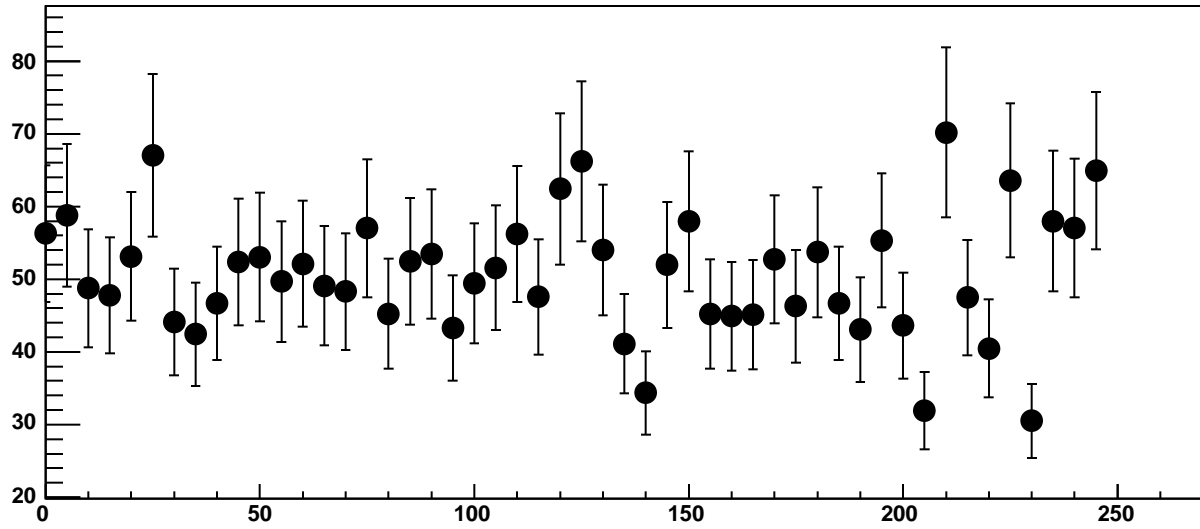
Chip 10, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold



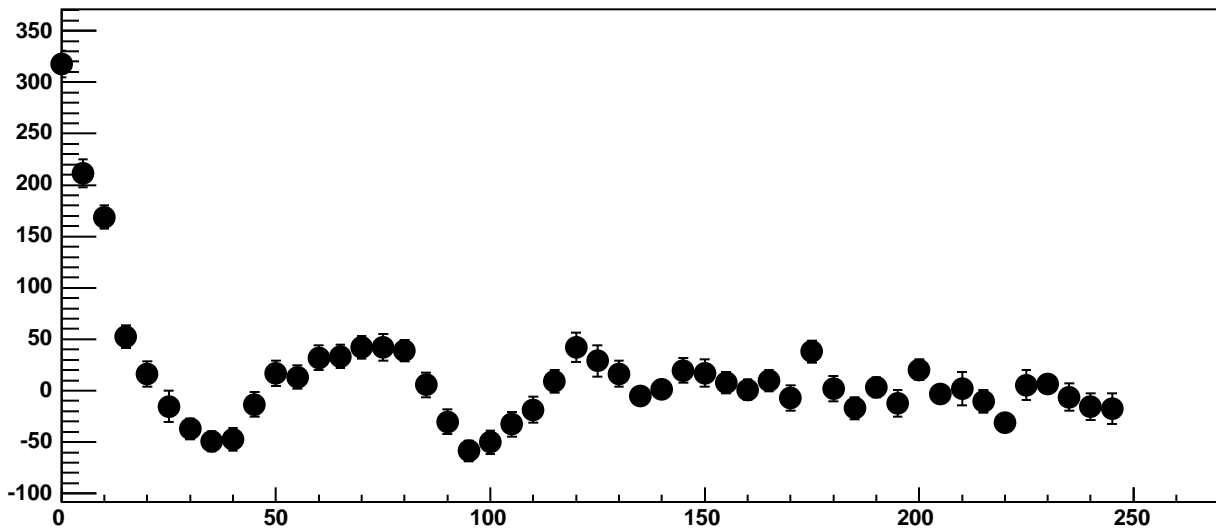
Chip 10, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold



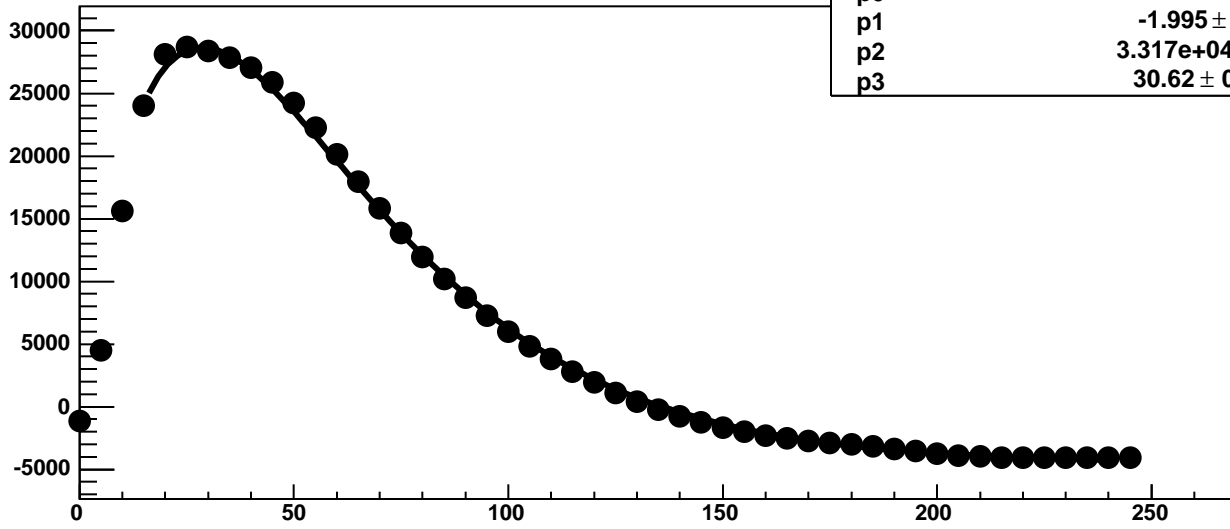
Chip 10, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

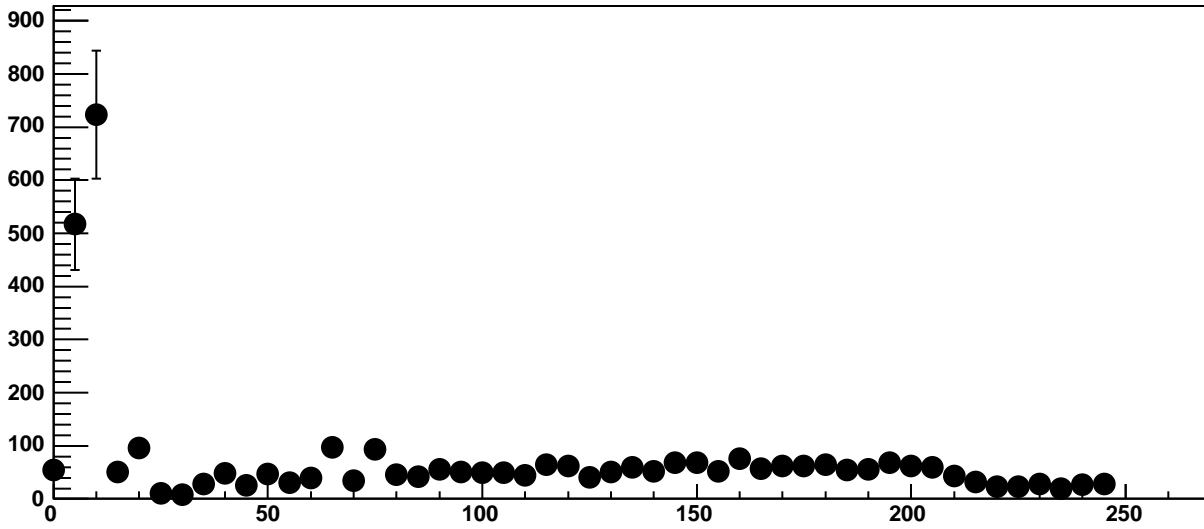


Chip 10, Channel 1, Enable 3!, DAC=1600, ADC Mean vs Hold

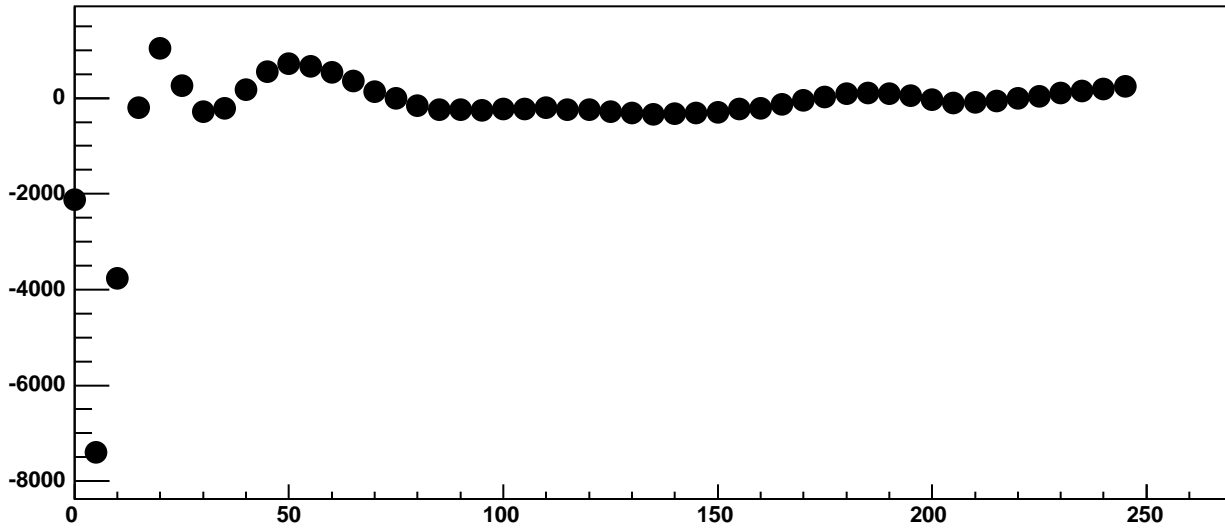


$\chi^2 / \text{ndf}$	7.351e+04 / 42
p0	-4511 ± 2.282
p1	-1.995 ± 0.01337
p2	3.317e+04 ± 2.539
p3	30.62 ± 0.007562

Chip 10, Channel 1, Enable 3!, DAC=1600, ADC Noise vs Hold

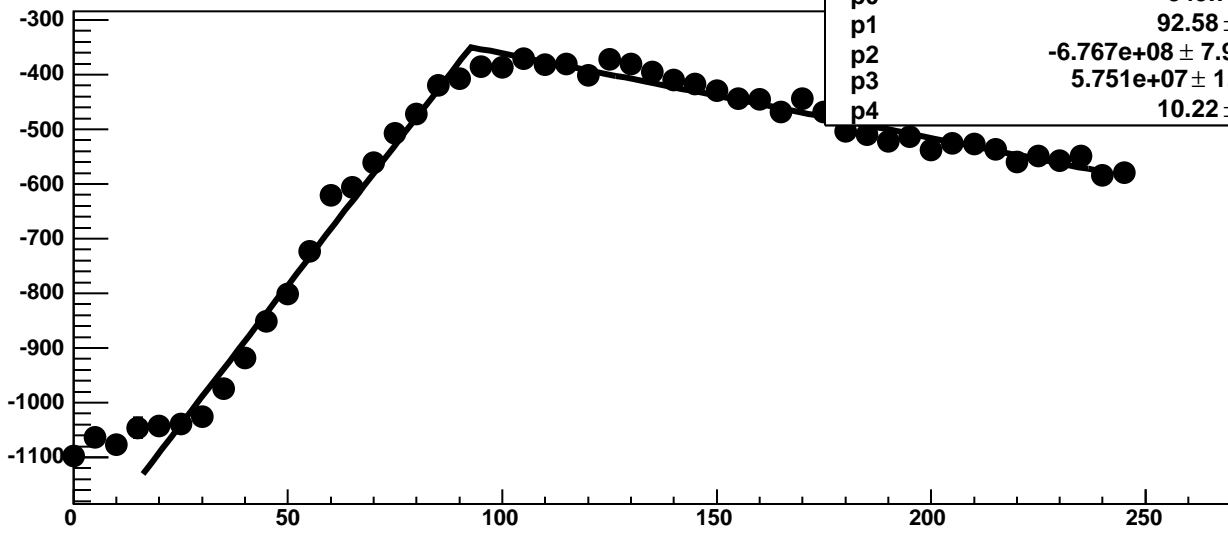


Chip 10, Channel 1, Enable 3!, DAC=1600, ADC Residuals vs Hold



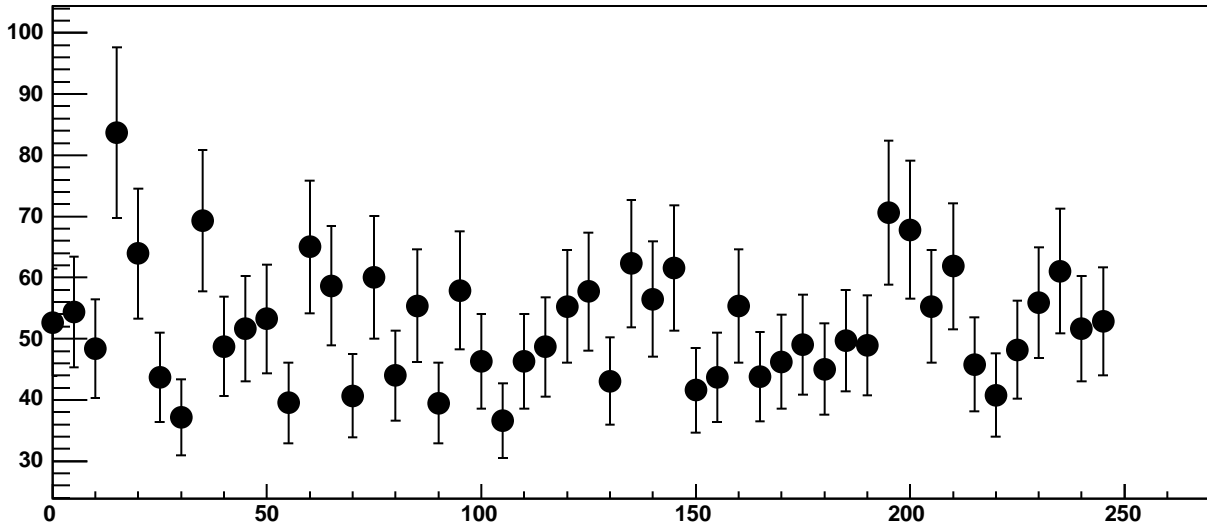


Chip 10, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold

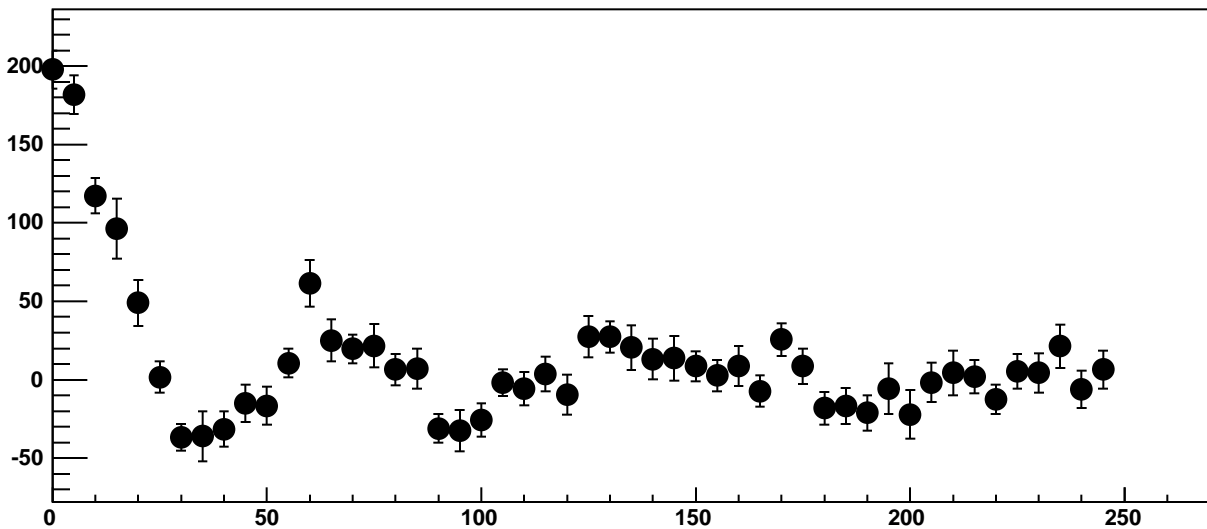


$\chi^2 / \text{ndf}$	165.4 / 41
p0	$-349.7 \pm 3.603$
p1	$92.58 \pm 0.5801$
p2	$-6.767\text{e}+08 \pm 7.962\text{e}+06$
p3	$5.751\text{e}+07 \pm 1.74\text{e}+05$
p4	$10.22 \pm 0.1251$

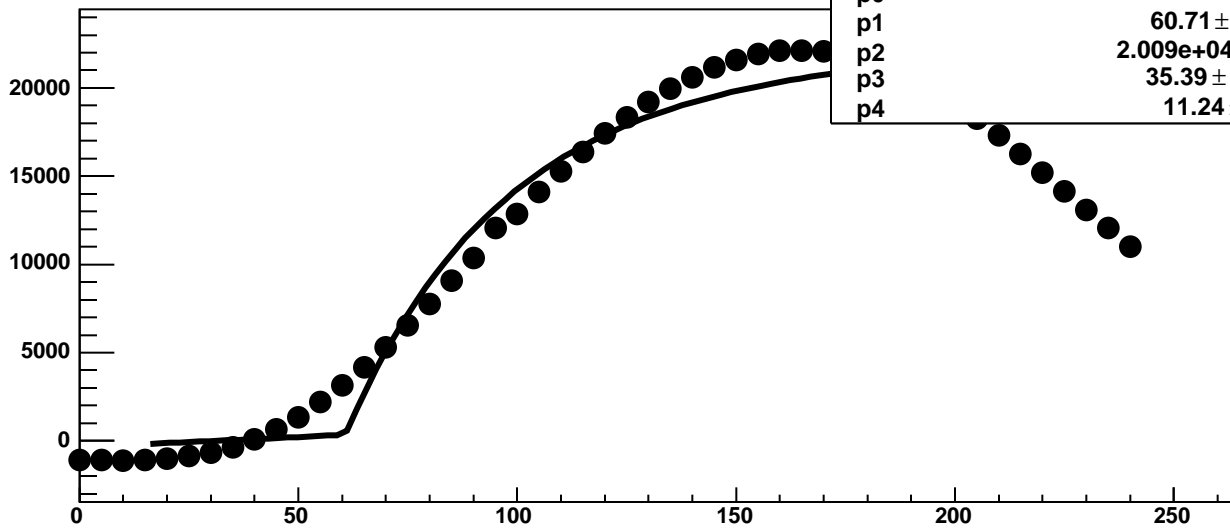
Chip 10, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

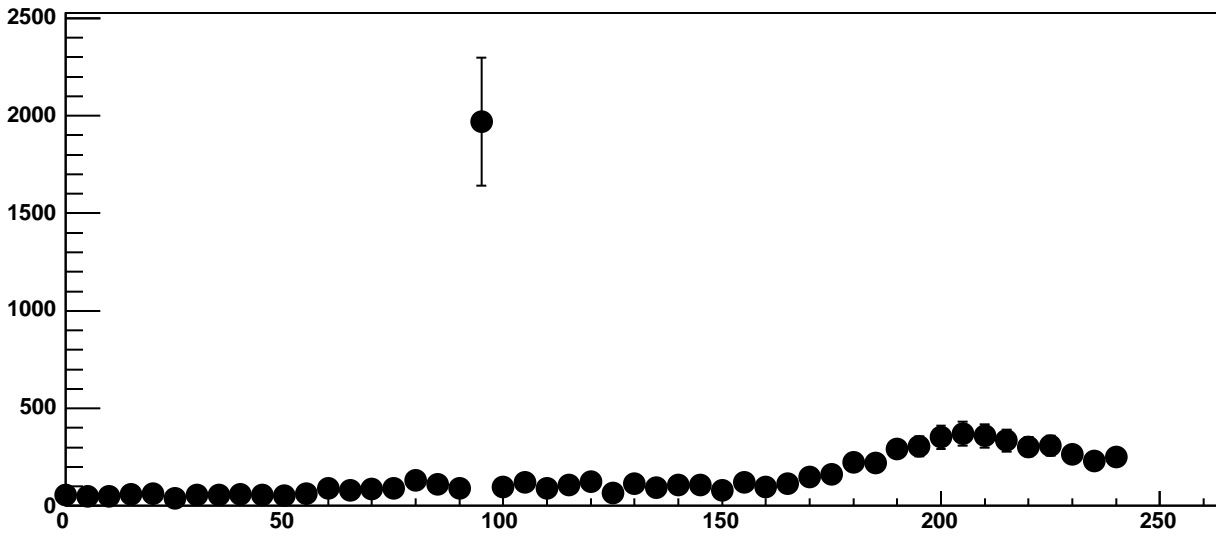


Chip 10, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

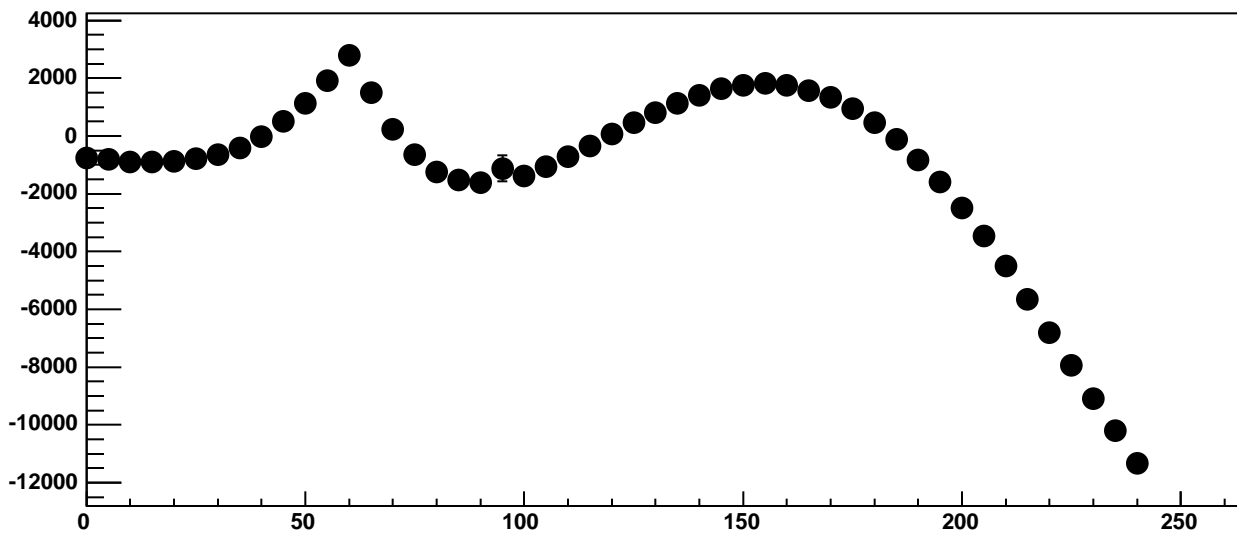


$\chi^2 / \text{ndf}$	2.621e+05 / 41
p0	341.5 ± 7.104
p1	60.71 ± 0.03201
p2	2.009e+04 ± 36.74
p3	35.39 ± 0.08407
p4	11.24 ± 0.2281

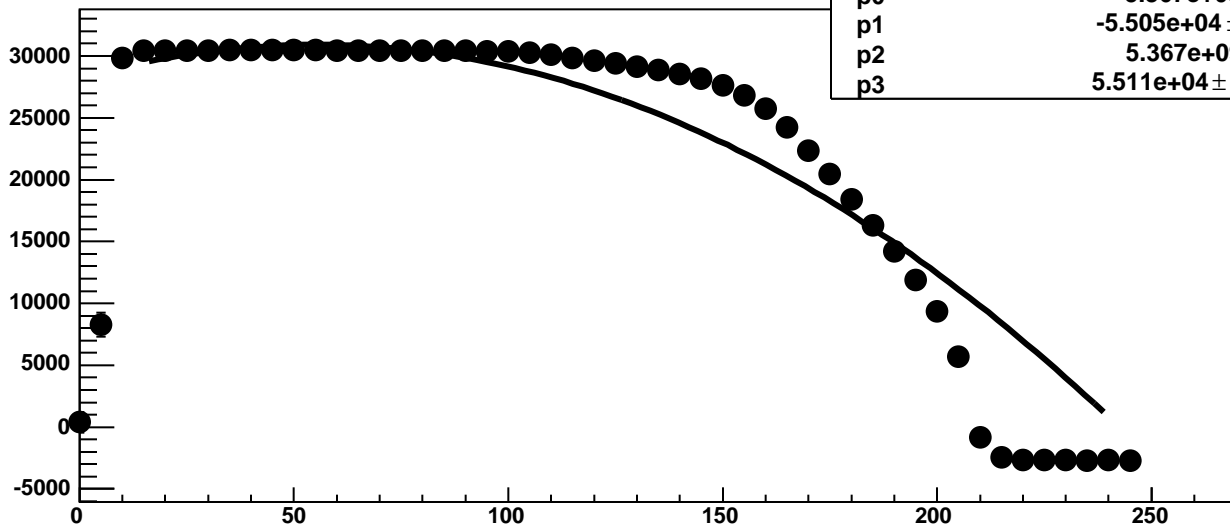
Chip 10, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold

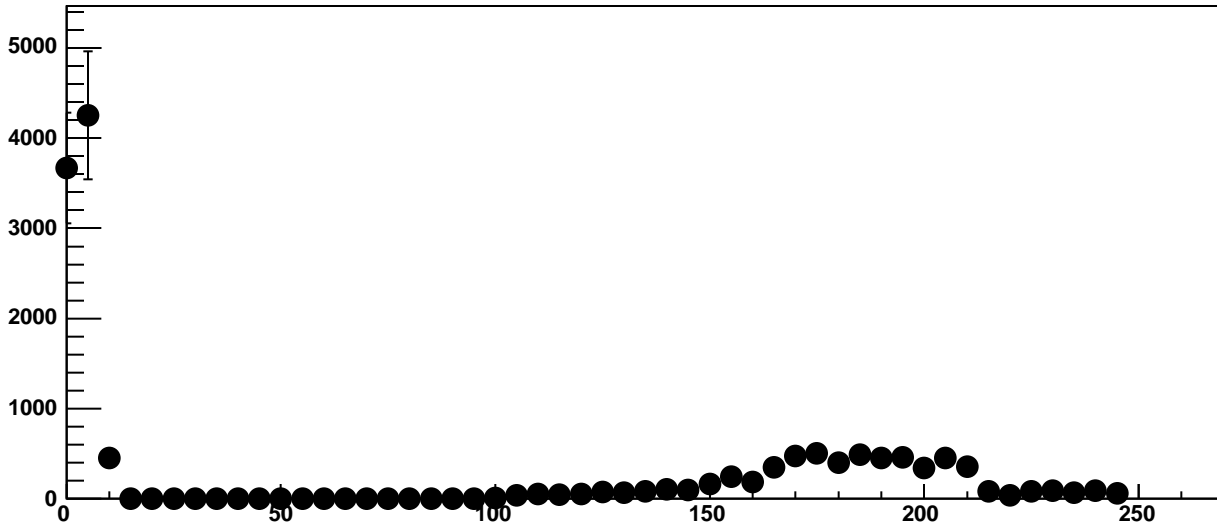


Chip 10, Channel 2, Enable 0!, DAC=1600, ADC Mean vs Hold

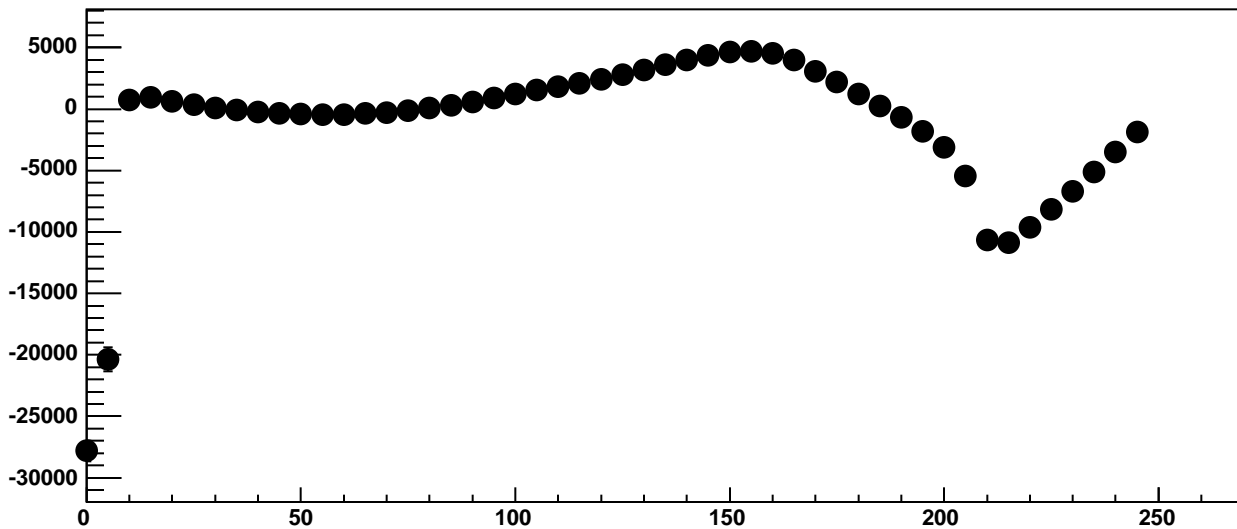


$\chi^2 / \text{ndf}$	6.508e+06 / 42
p0	-5.367e+09 ± 2.97
p1	-5.505e+04 ± 0.0618
p2	5.367e+09 ± 2.97
p3	5.511e+04 ± 0.06179

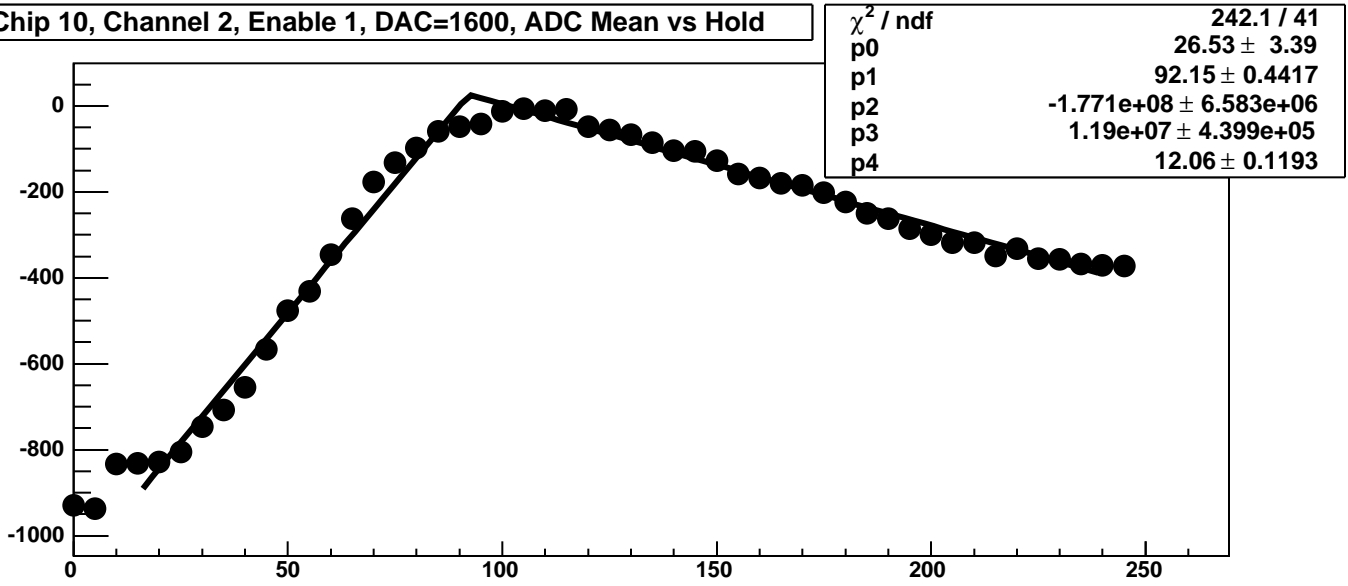
Chip 10, Channel 2, Enable 0!, DAC=1600, ADC Noise vs Hold



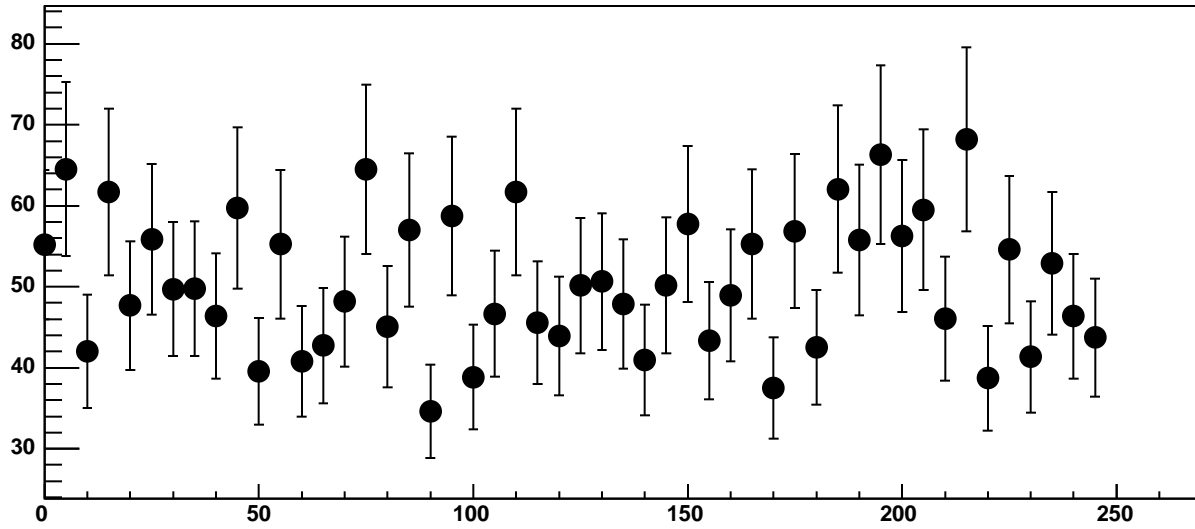
Chip 10, Channel 2, Enable 0!, DAC=1600, ADC Residuals vs Hold



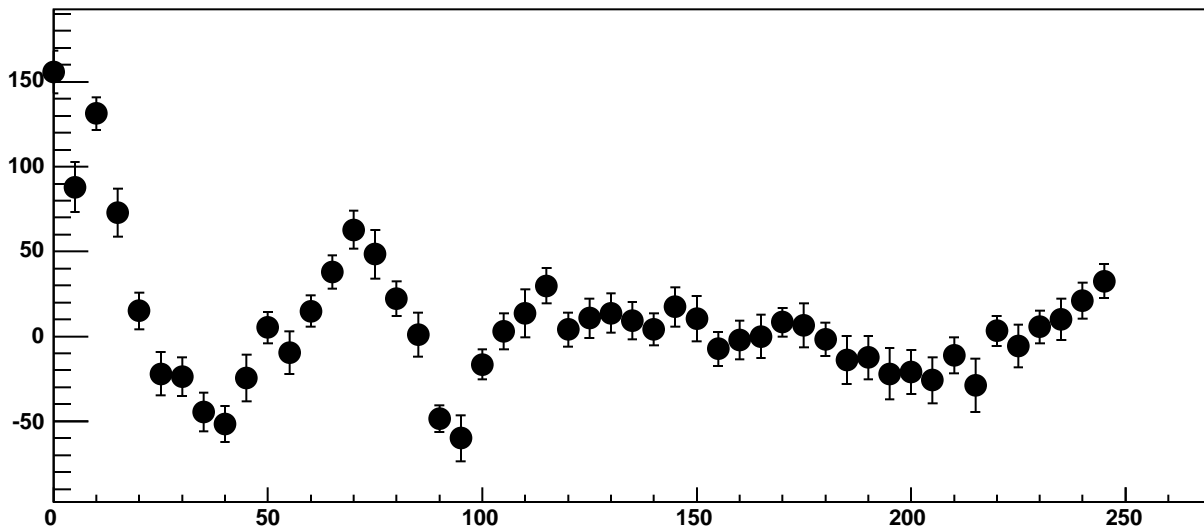
Chip 10, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold



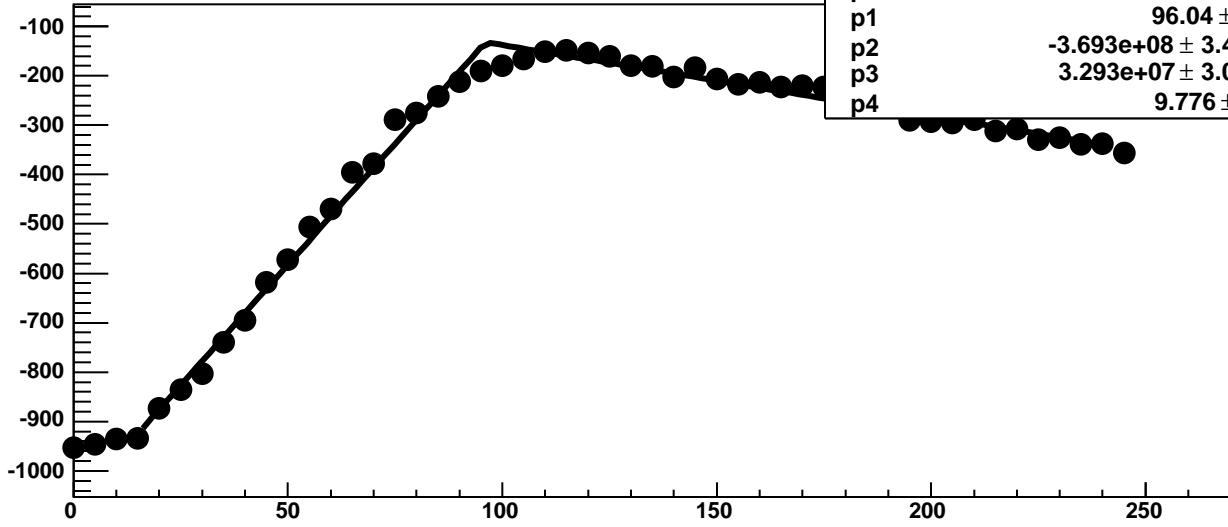
Chip 10, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold

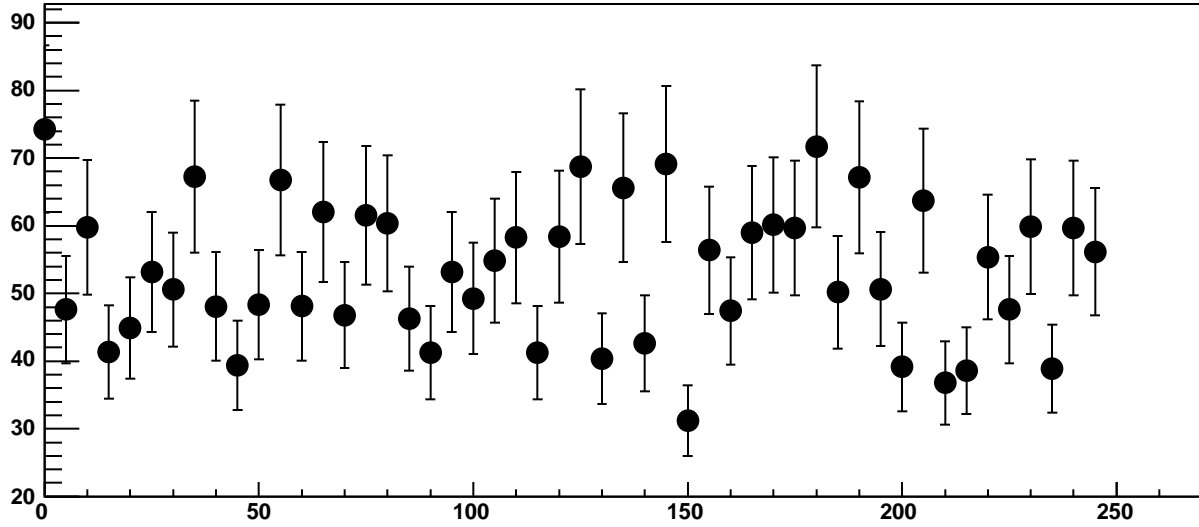


Chip 10, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

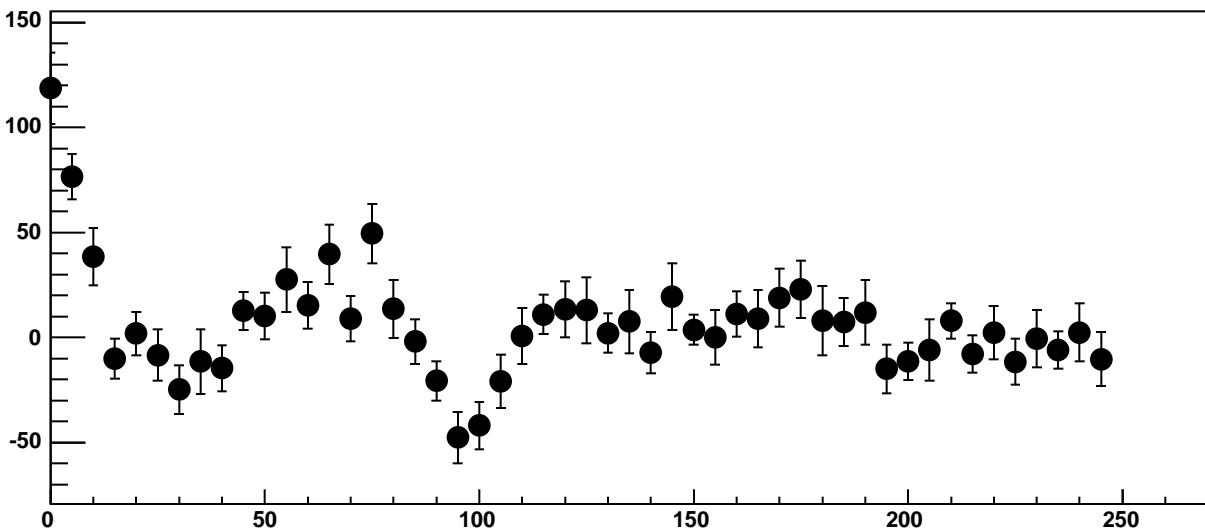


$\chi^2 / \text{ndf}$	94.56 / 41
p0	-132.1 ± 3.853
p1	96.04 ± 0.6264
p2	-3.693e+08 ± 3.446e+07
p3	3.293e+07 ± 3.012e+06
p4	9.776 ± 0.1087

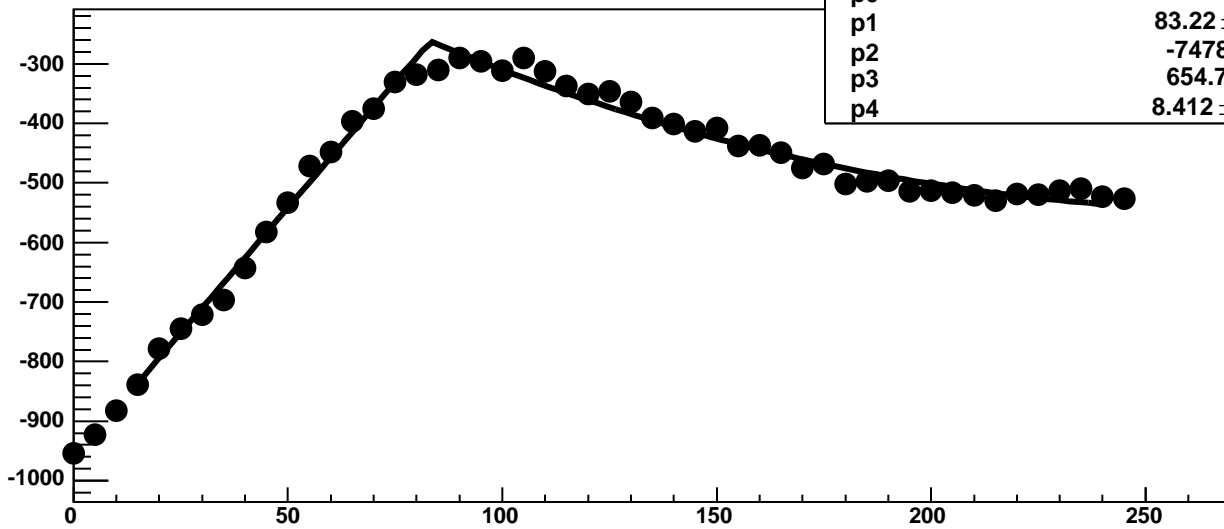
Chip 10, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

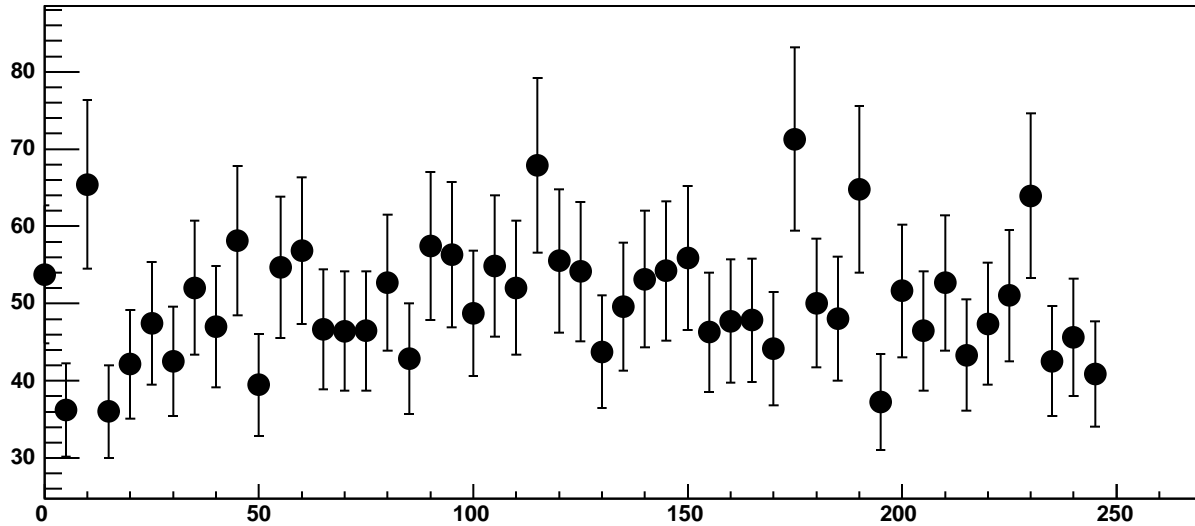


Chip 10, Channel 2, Enable 3, DAC=1600, ADC Mean vs Hold

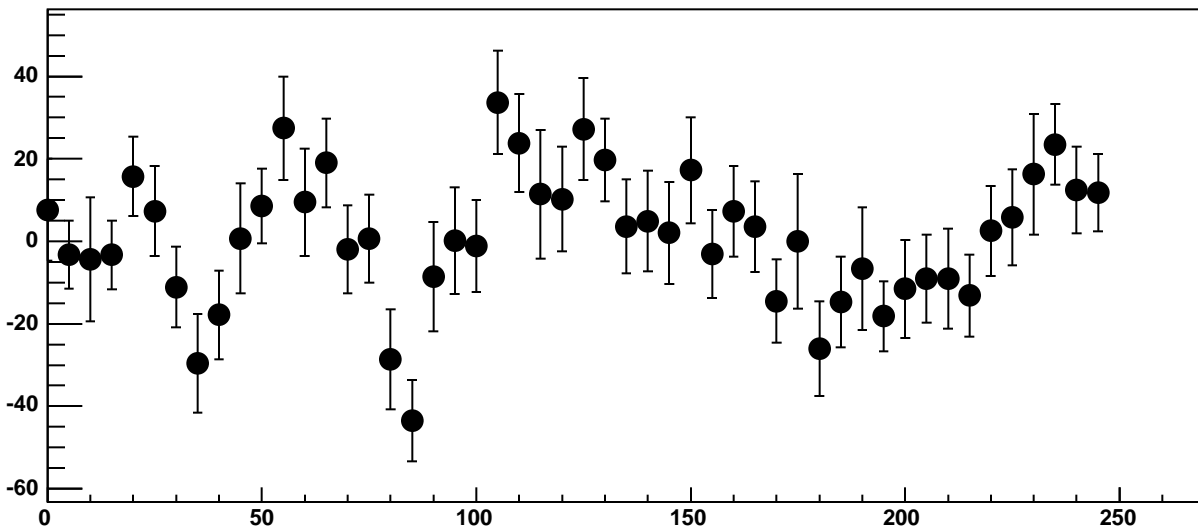


$\chi^2 / \text{ndf}$	98.48 / 41
p0	$-261.9 \pm 4.738$
p1	$83.22 \pm 0.7448$
p2	$-7478 \pm 890.5$
p3	$654.7 \pm 86.24$
p4	$8.412 \pm 0.1354$

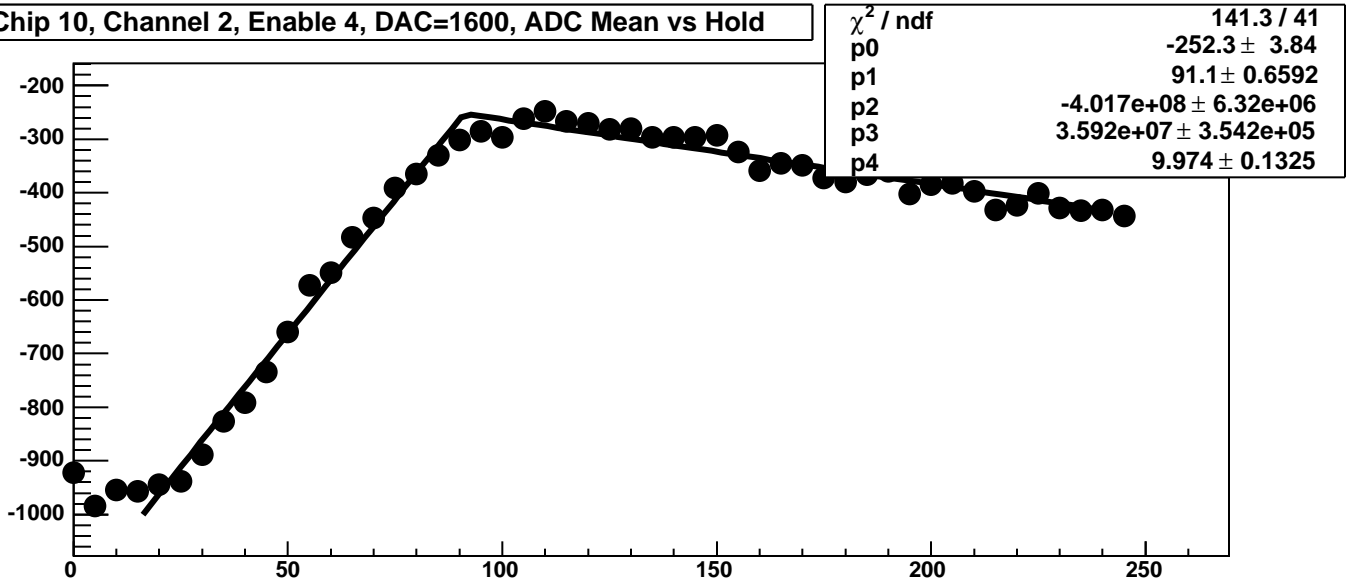
Chip 10, Channel 2, Enable 3, DAC=1600, ADC Noise vs Hold



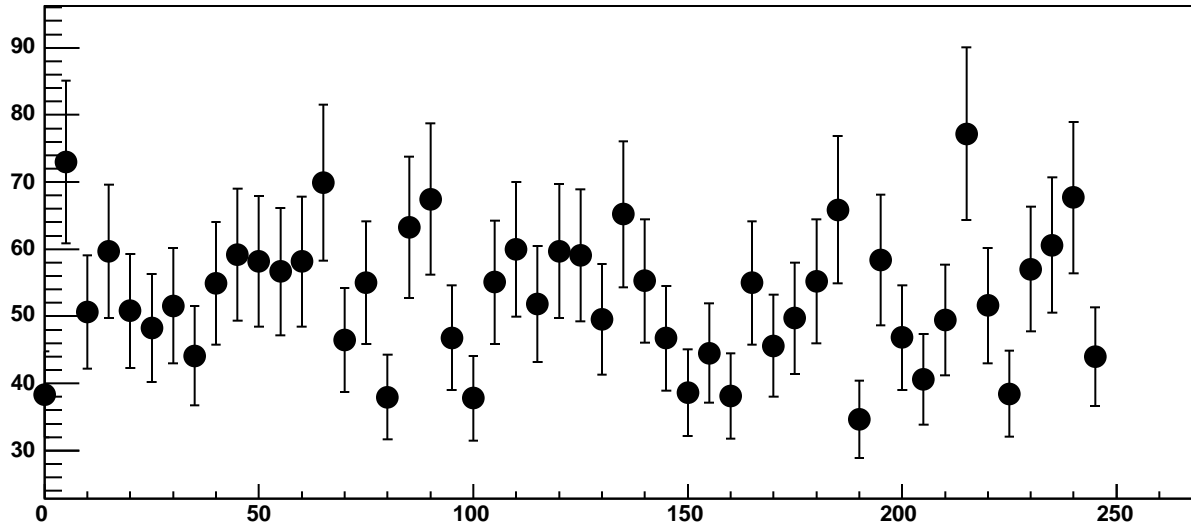
Chip 10, Channel 2, Enable 3, DAC=1600, ADC Residuals vs Hold



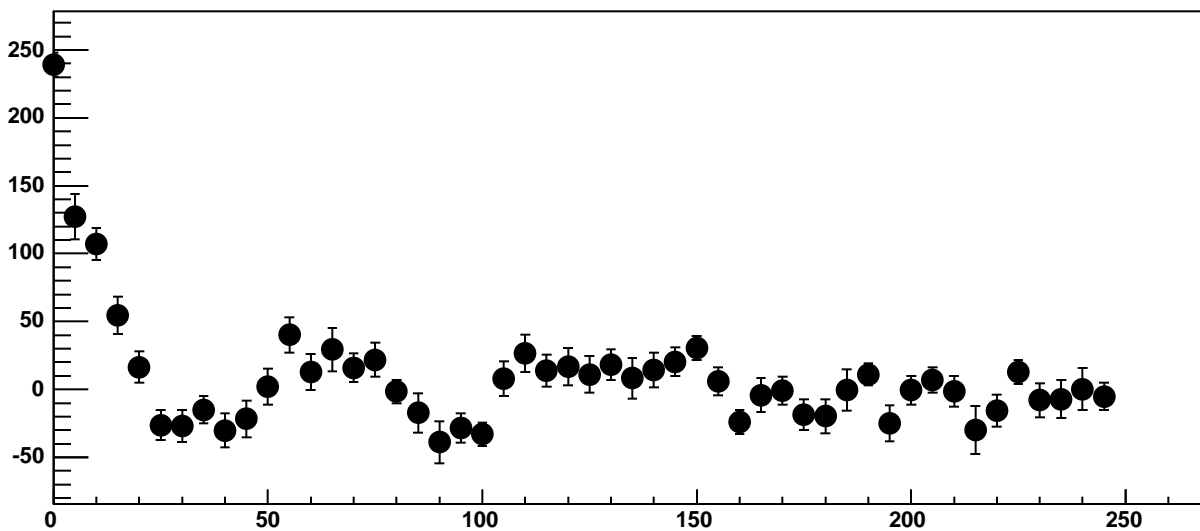
Chip 10, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold



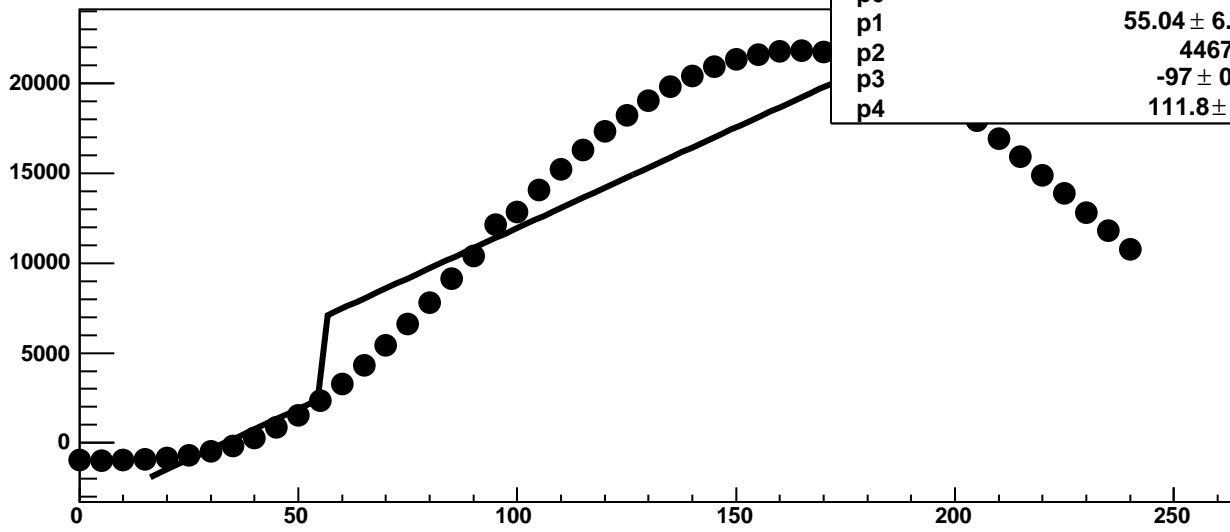
Chip 10, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

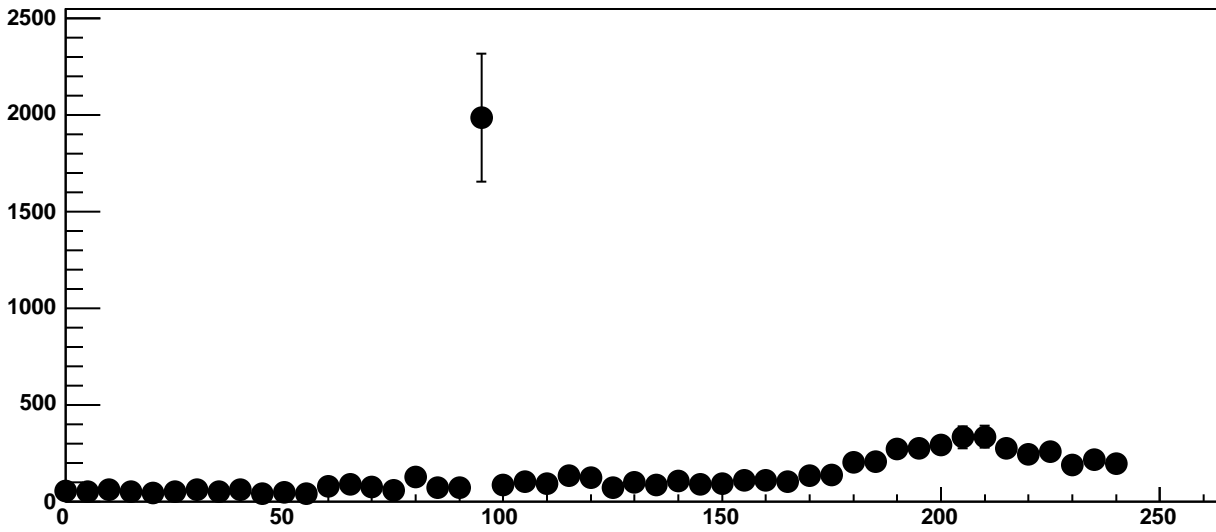


Chip 10, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

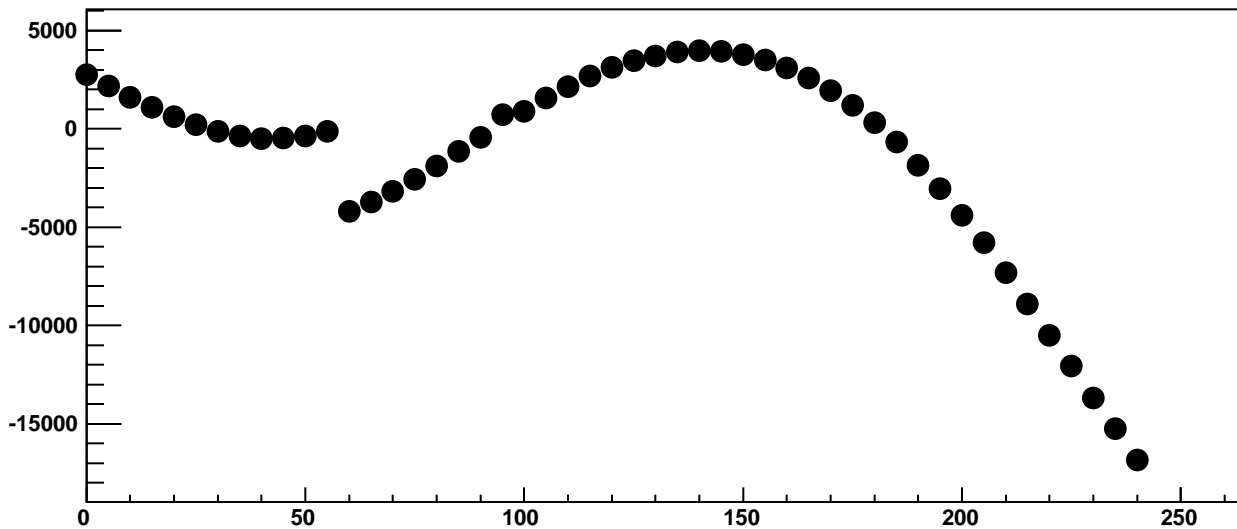


$\chi^2 / \text{ndf}$	9.054e+05 / 41
p0	2451 ± 4.271
p1	55.04 ± 6.154e-05
p2	4467 ± 9.455
p3	-97 ± 0.002029
p4	111.8 ± 0.09257

Chip 10, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold

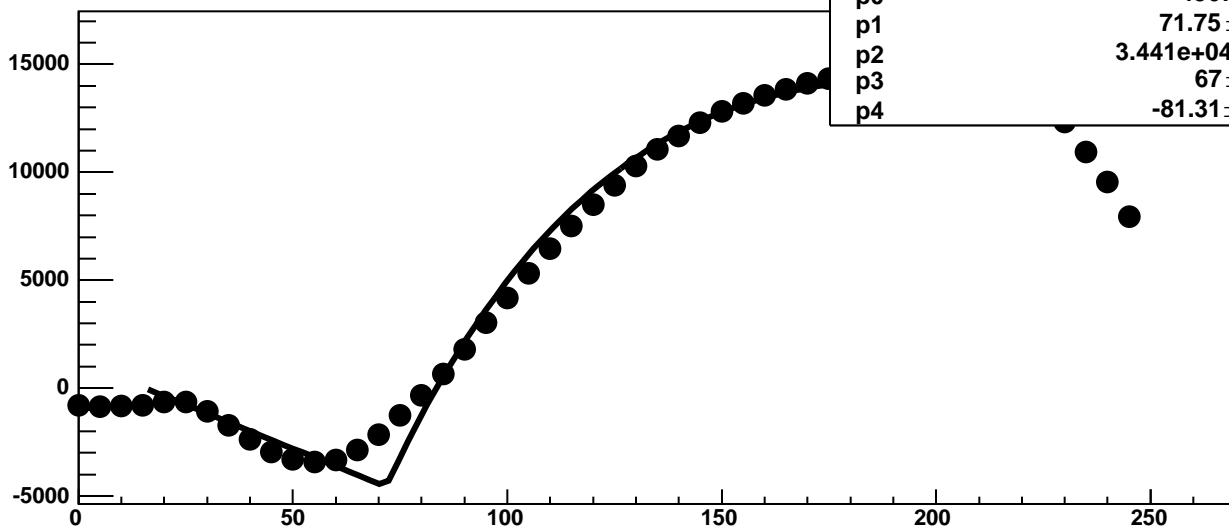


Chip 10, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



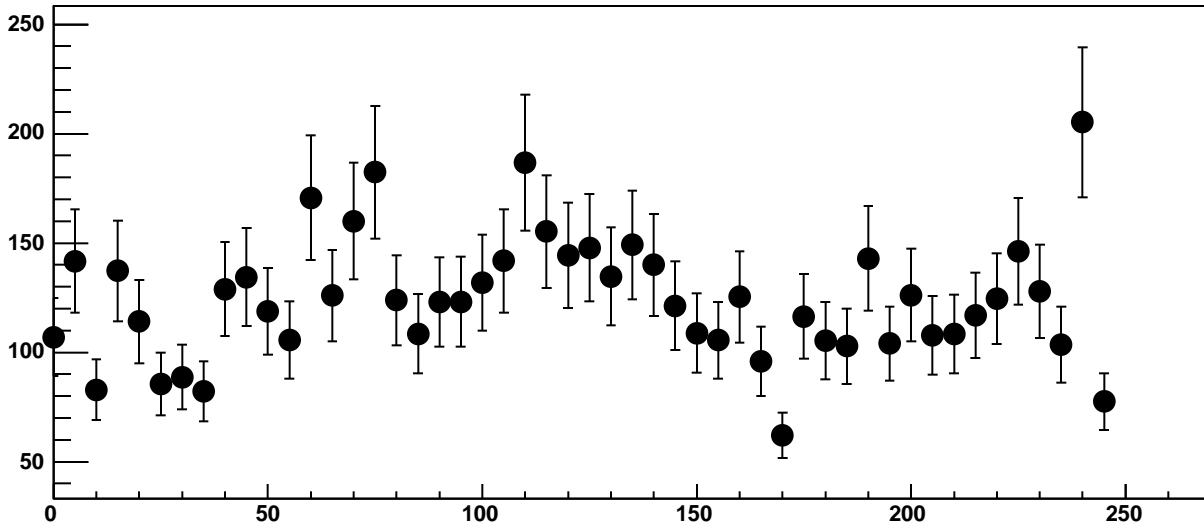


Chip 10, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold

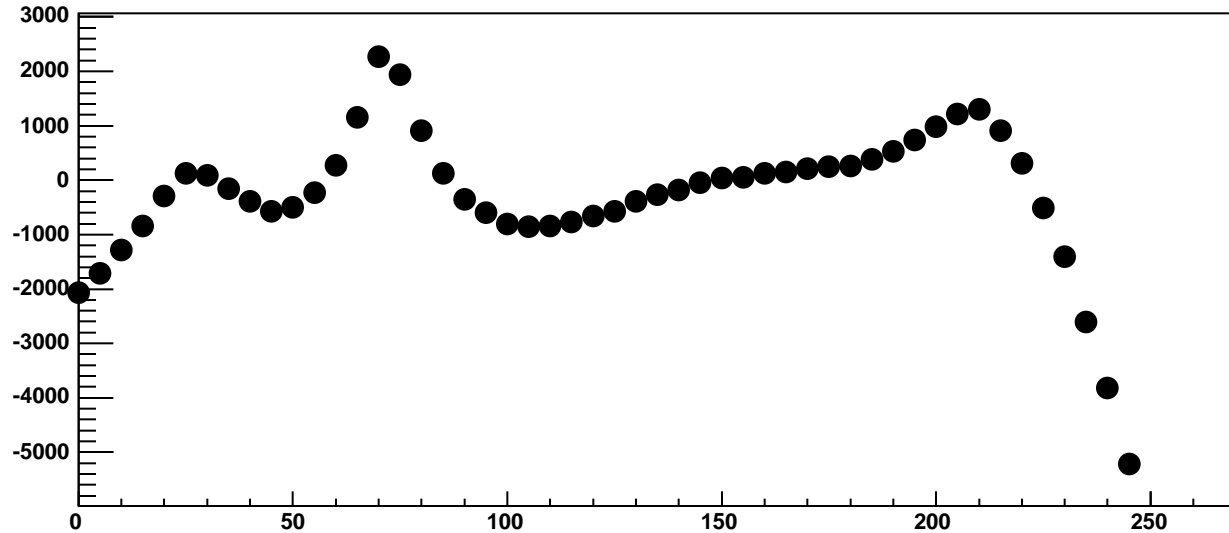


$\chi^2 / \text{ndf}$	4.51e+04 / 41
p0	-4567 ± 13.29
p1	71.75 ± 0.0532
p2	3.441e+04 ± 106.5
p3	67 ± 0.2047
p4	-81.31 ± 0.4206

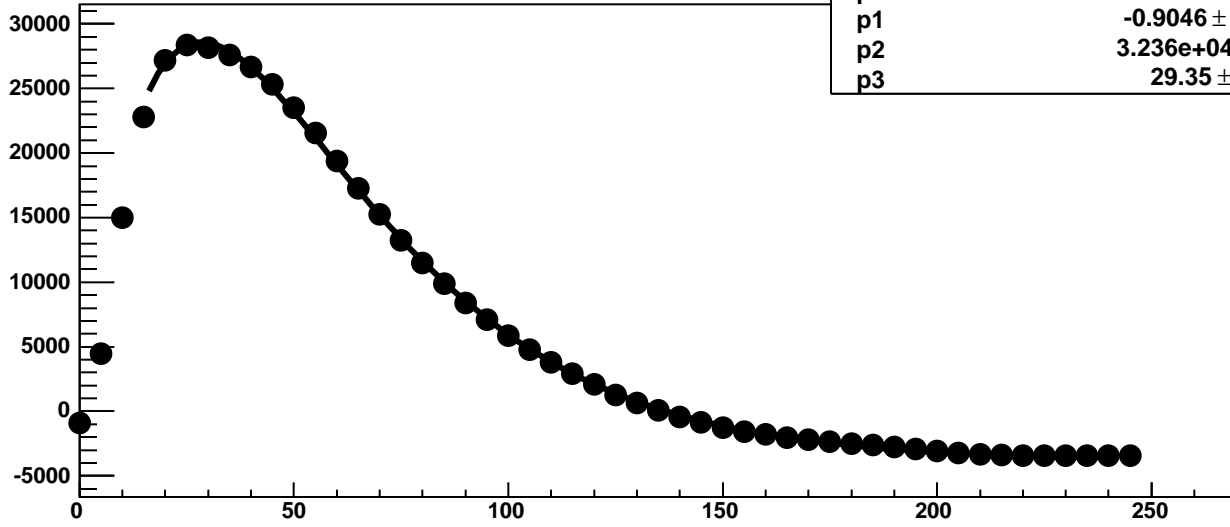
Chip 10, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold



Chip 10, Channel 3, Enable 1!, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

9081 / 42

p0

-3774 ± 4.1

p1

-0.9046 ± 0.01887

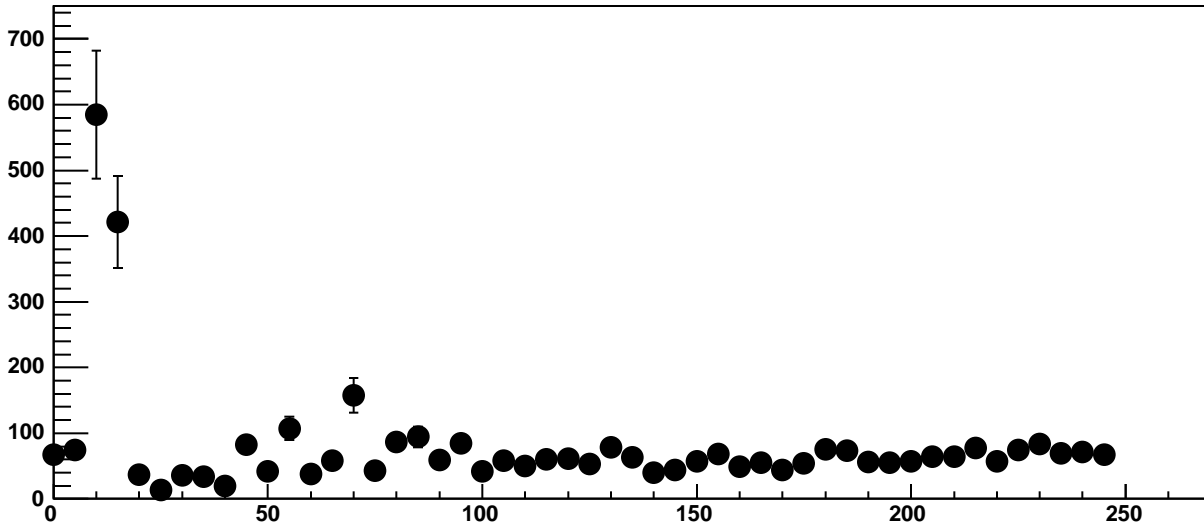
p2

3.236e+04 ± 4.256

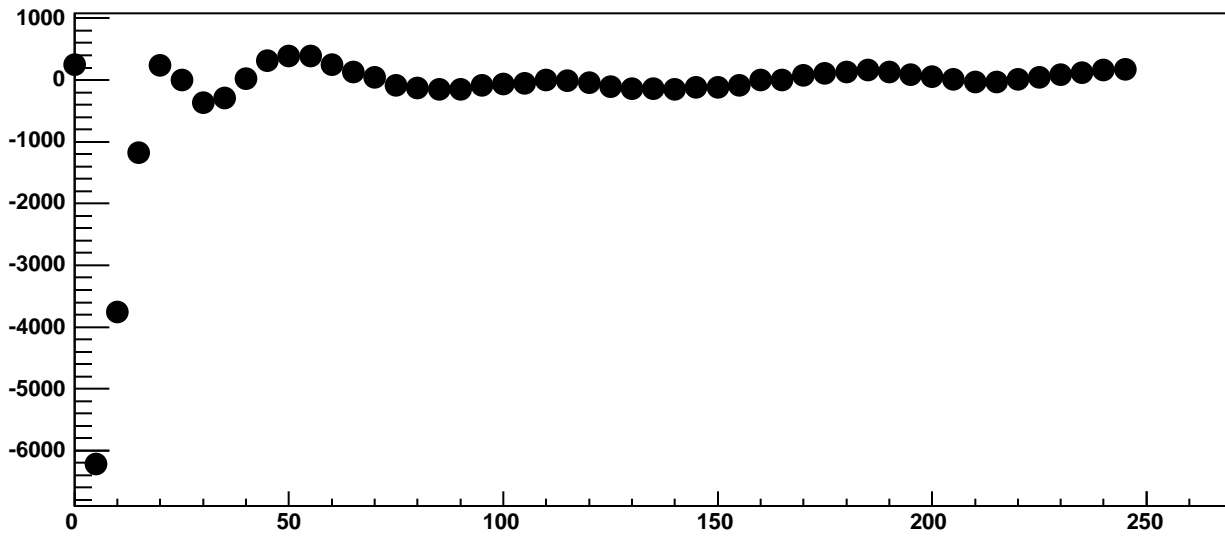
p3

29.35 ± 0.01131

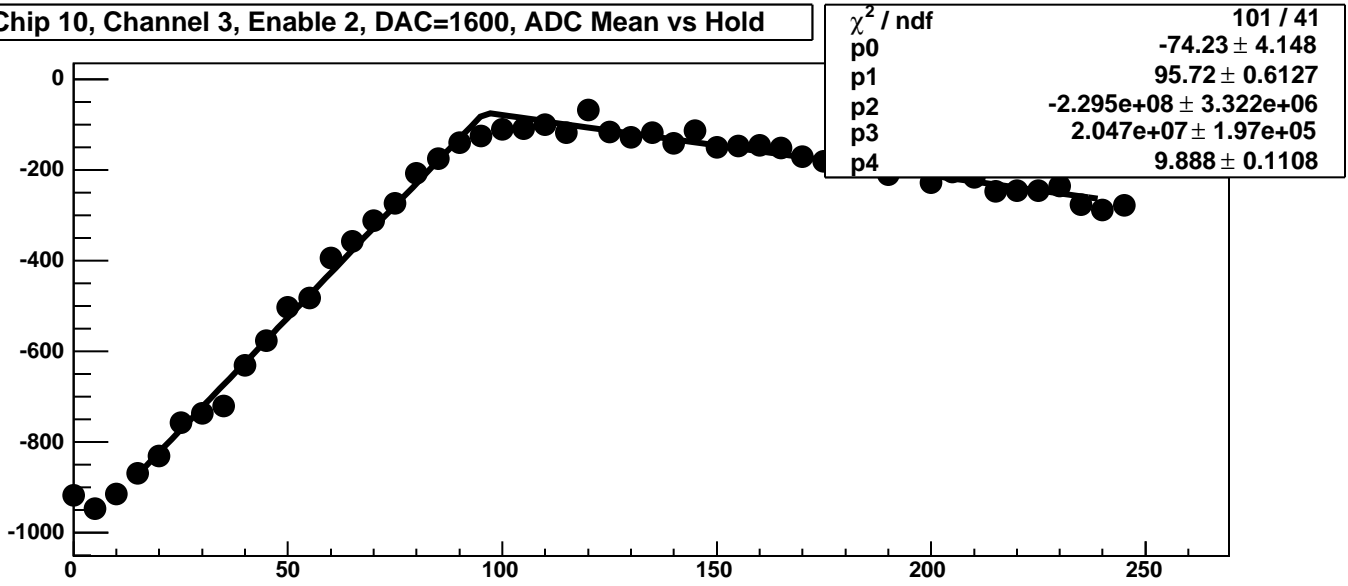
Chip 10, Channel 3, Enable 1!, DAC=1600, ADC Noise vs Hold



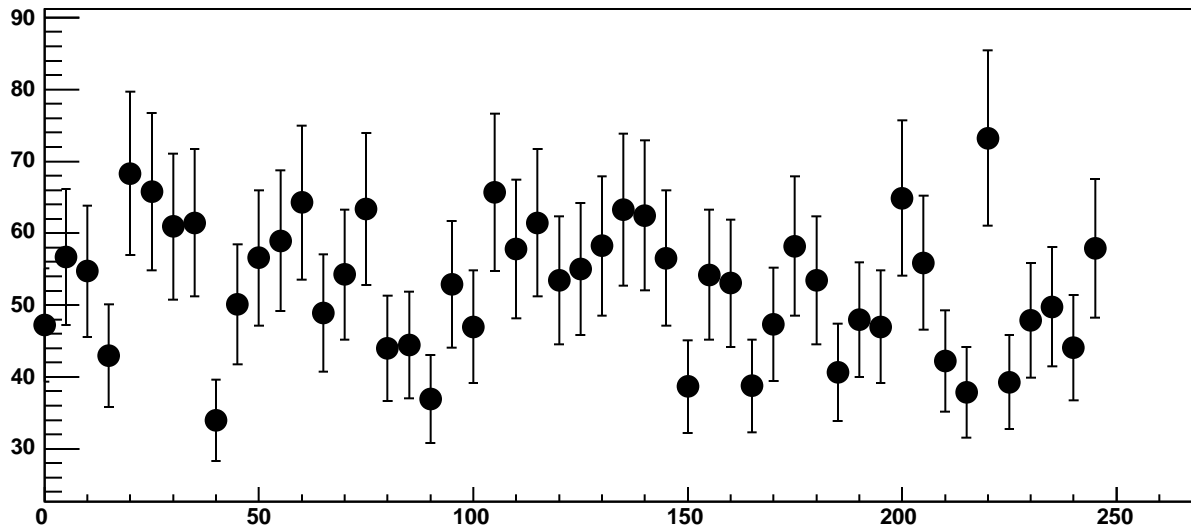
Chip 10, Channel 3, Enable 1!, DAC=1600, ADC Residuals vs Hold



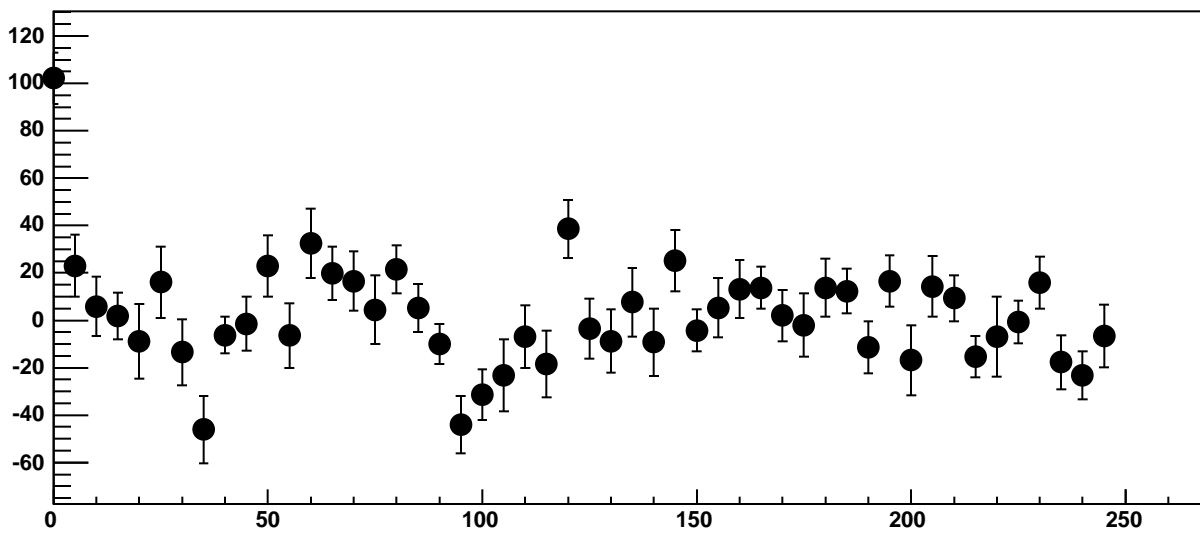
Chip 10, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold



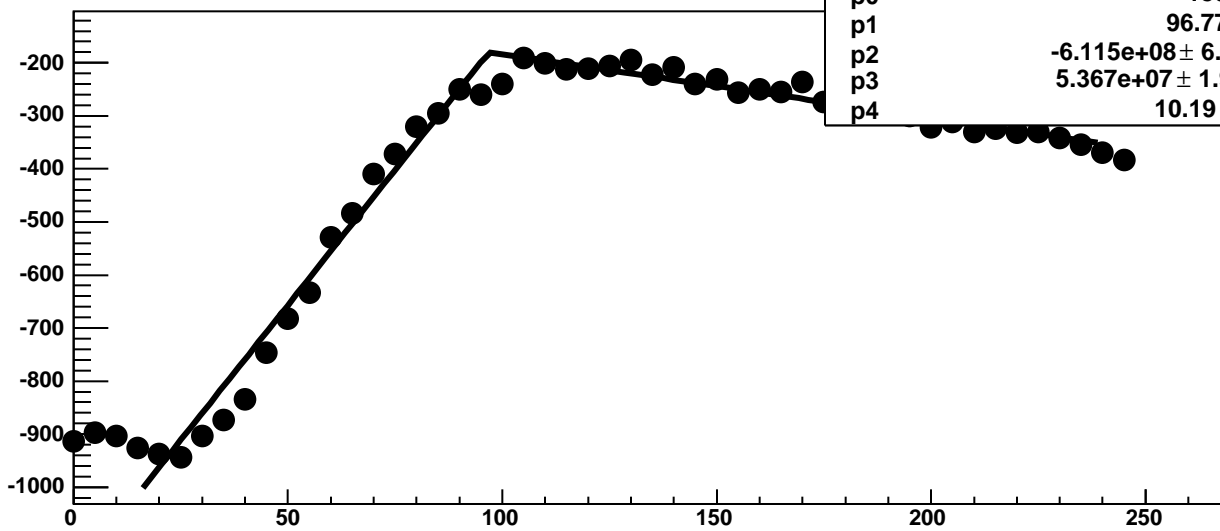
Chip 10, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold

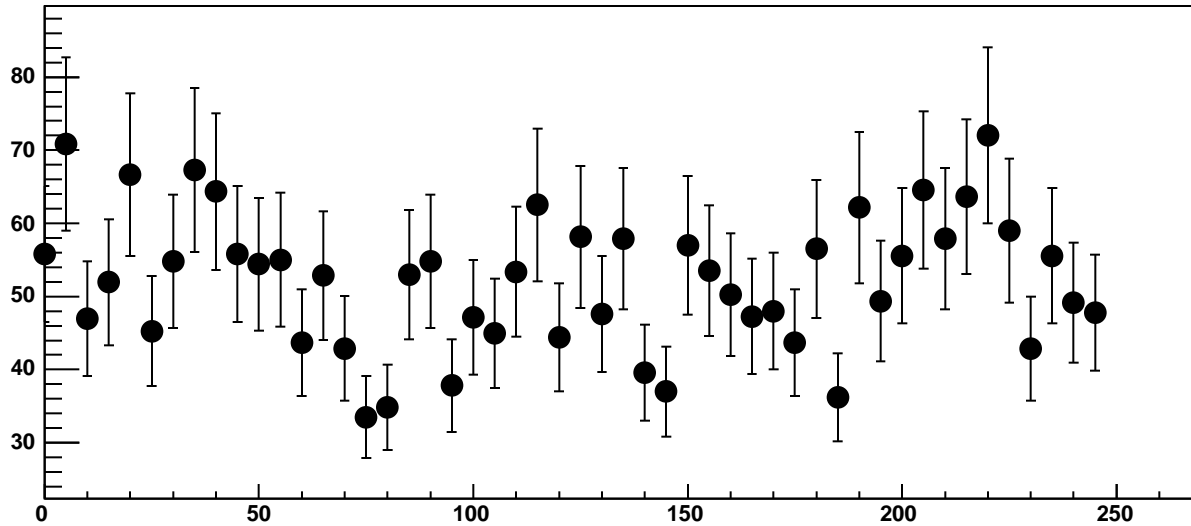


Chip 10, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold

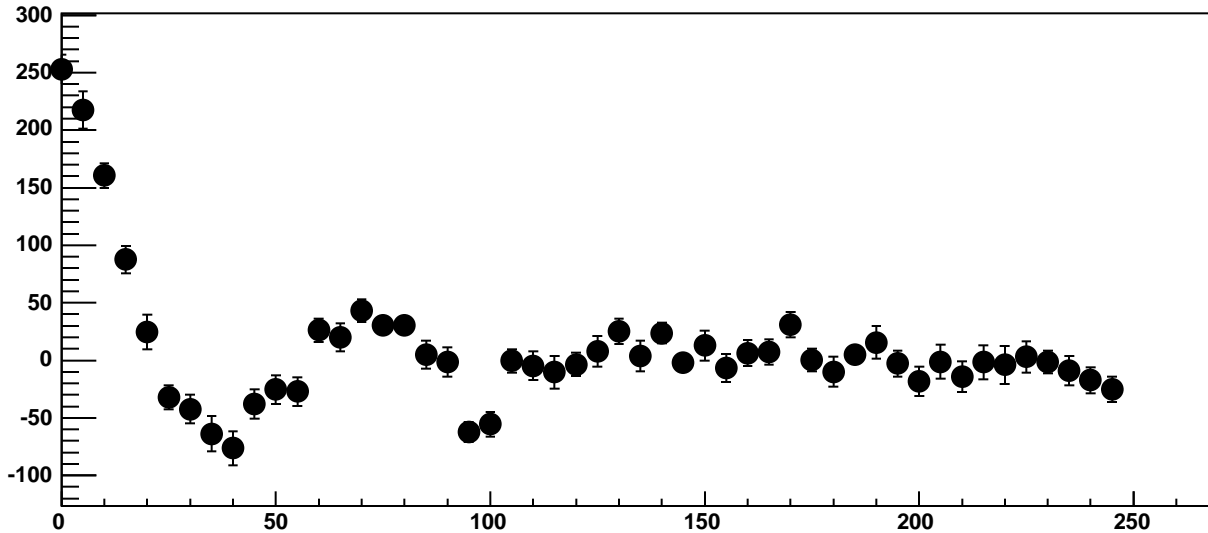


$\chi^2 / \text{ndf}$	308.3 / 41
p0	$-180 \pm 3.818$
p1	$96.77 \pm 0.559$
p2	$-6.115\text{e}+08 \pm 6.901\text{e}+06$
p3	$5.367\text{e}+07 \pm 1.929\text{e}+05$
p4	$10.19 \pm 0.1103$

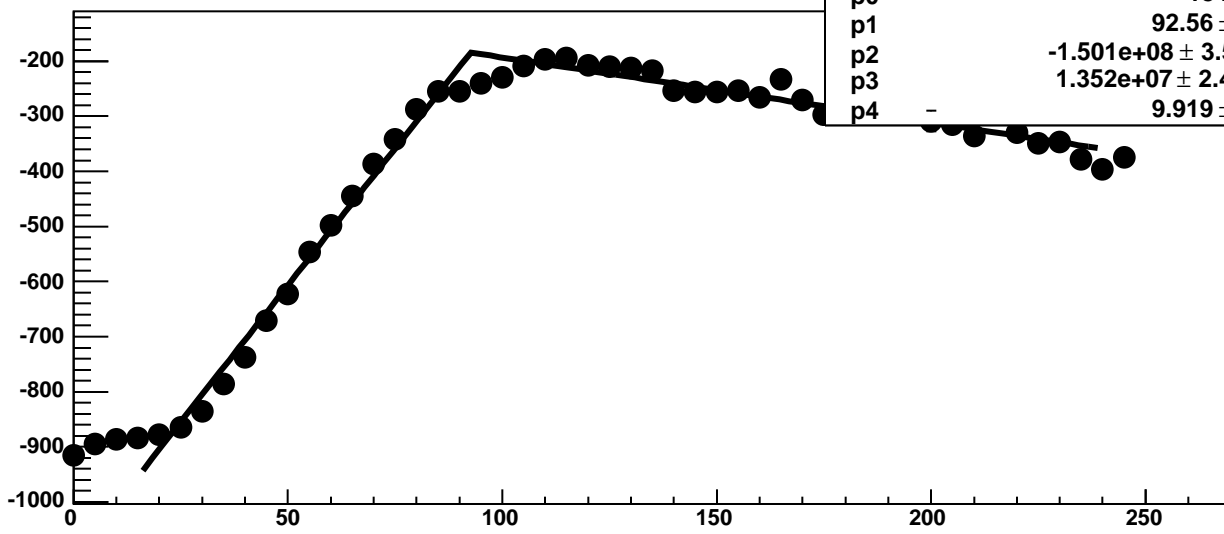
Chip 10, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold

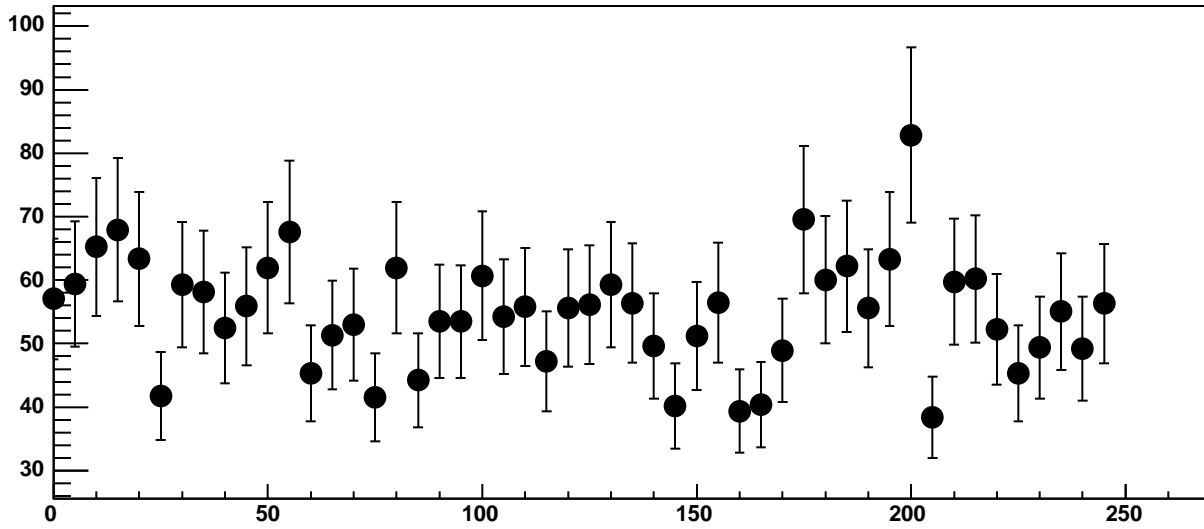


Chip 10, Channel 3, Enable 4, DAC=1600, ADC Mean vs Hold

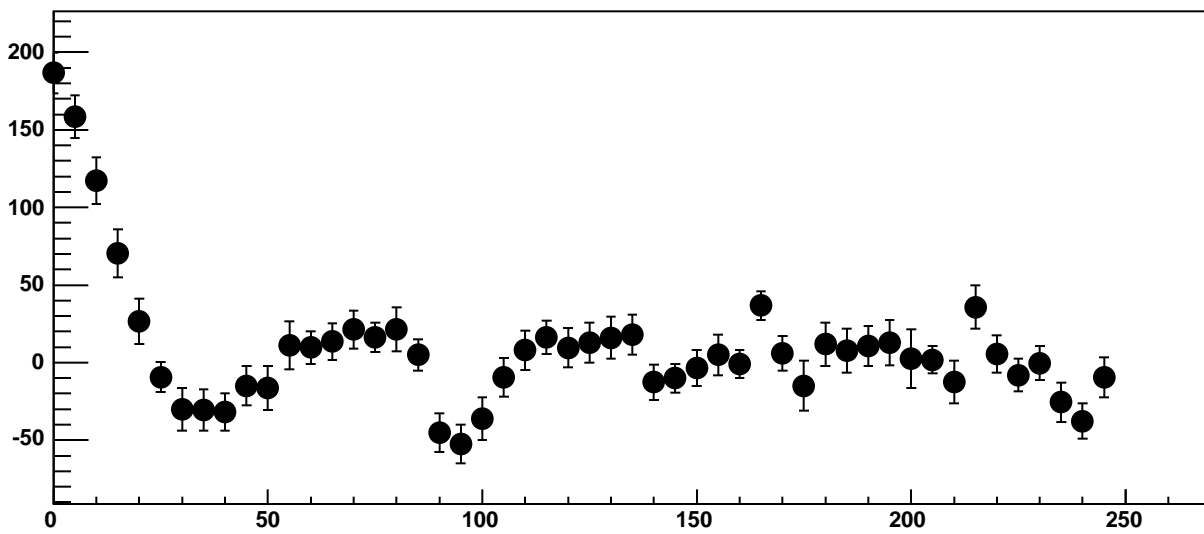


$\chi^2 / \text{ndf}$	148 / 41
p0	-184.5 ± 4
p1	92.56 ± 0.6594
p2	-1.501e+08 ± 3.568e+06
p3	1.352e+07 ± 2.478e+05
p4	9.919 ± 0.1326

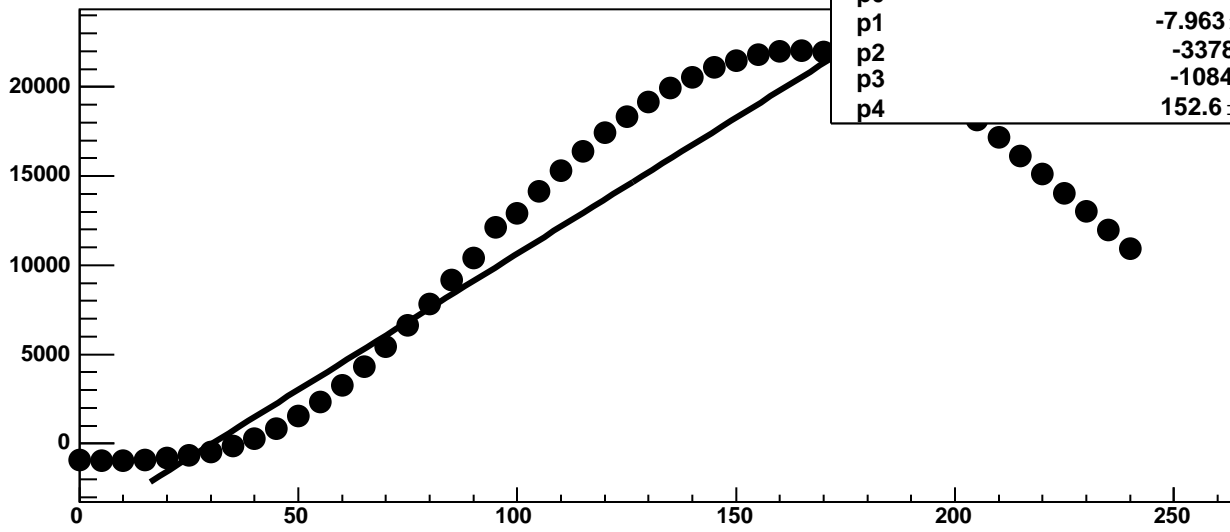
Chip 10, Channel 3, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 3, Enable 4, DAC=1600, ADC Residuals vs Hold

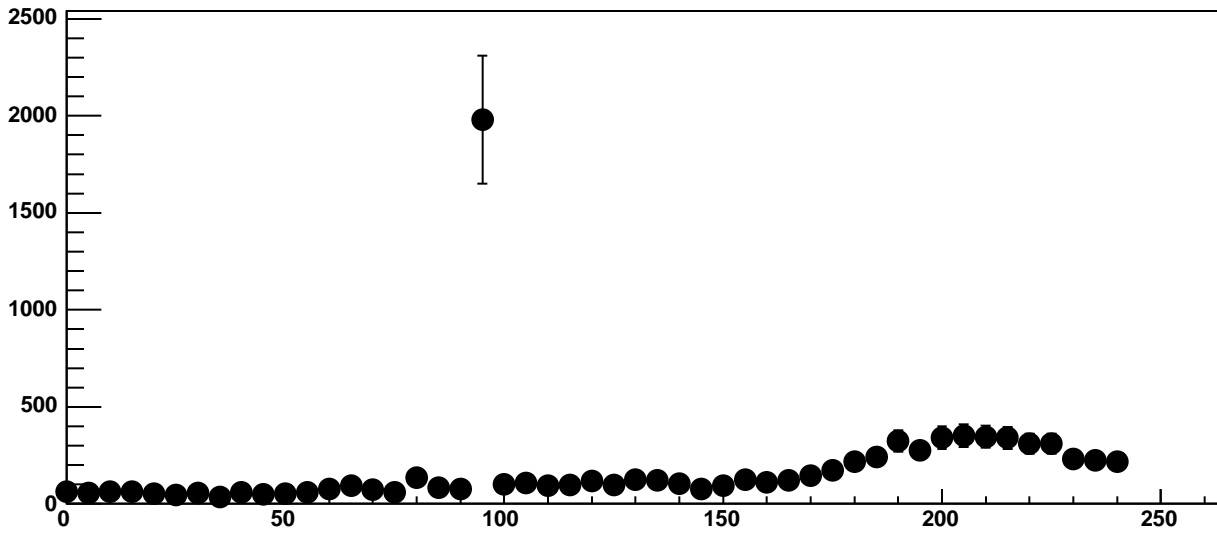


Chip 10, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

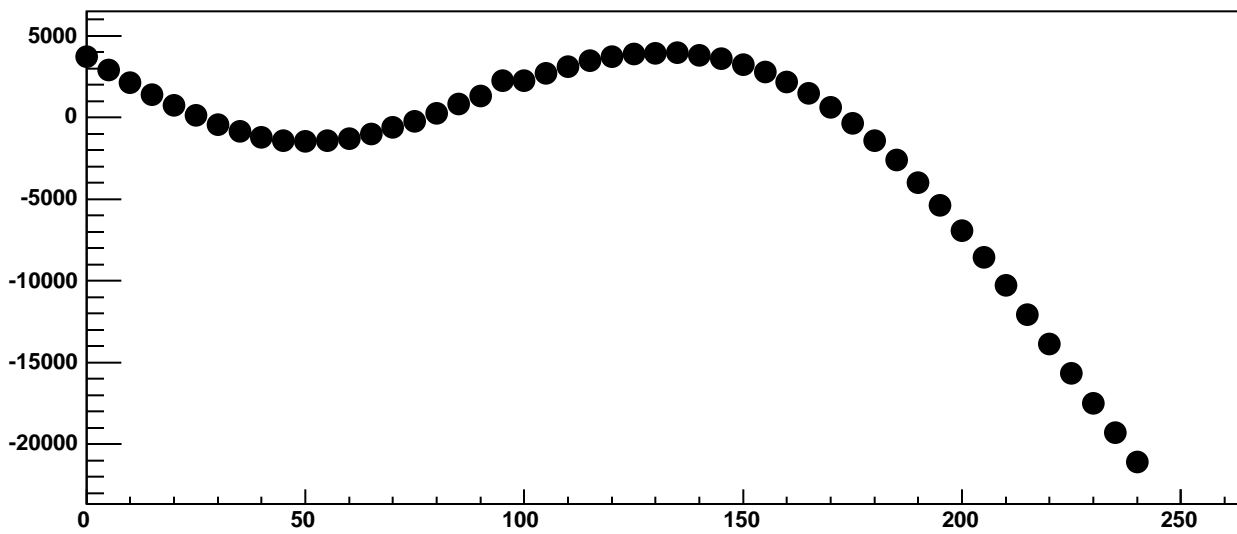


$\chi^2 / \text{ndf}$	9.379e+05 / 41
p0	-2456 ± 16.9
p1	-7.963 ± 0.1051
p2	-3378 ± 19.09
p3	-1084 ± 24.87
p4	152.6 ± 0.1139

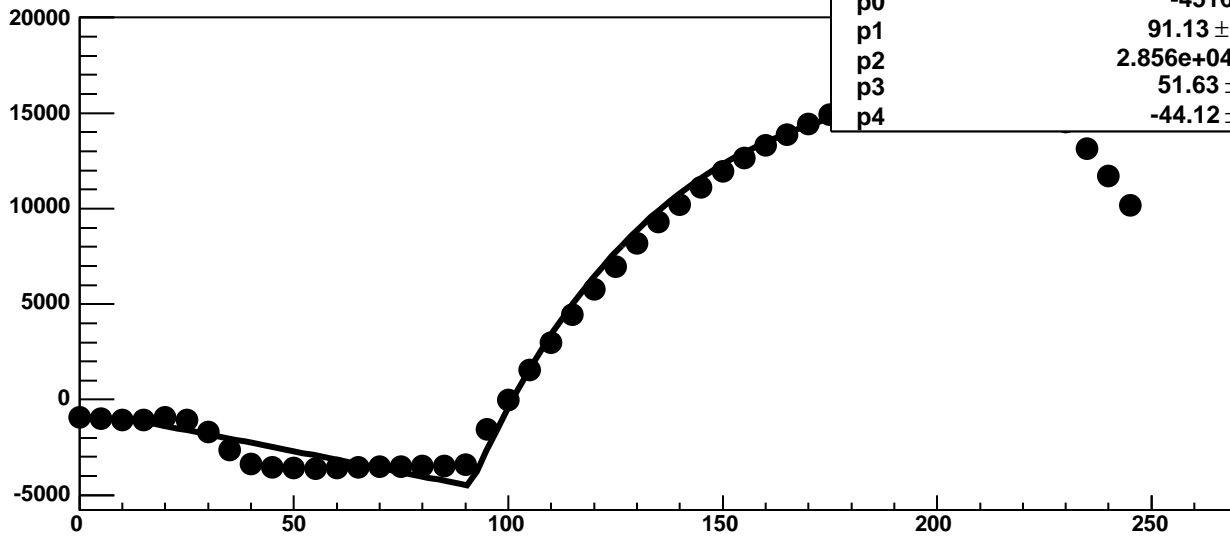
Chip 10, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold

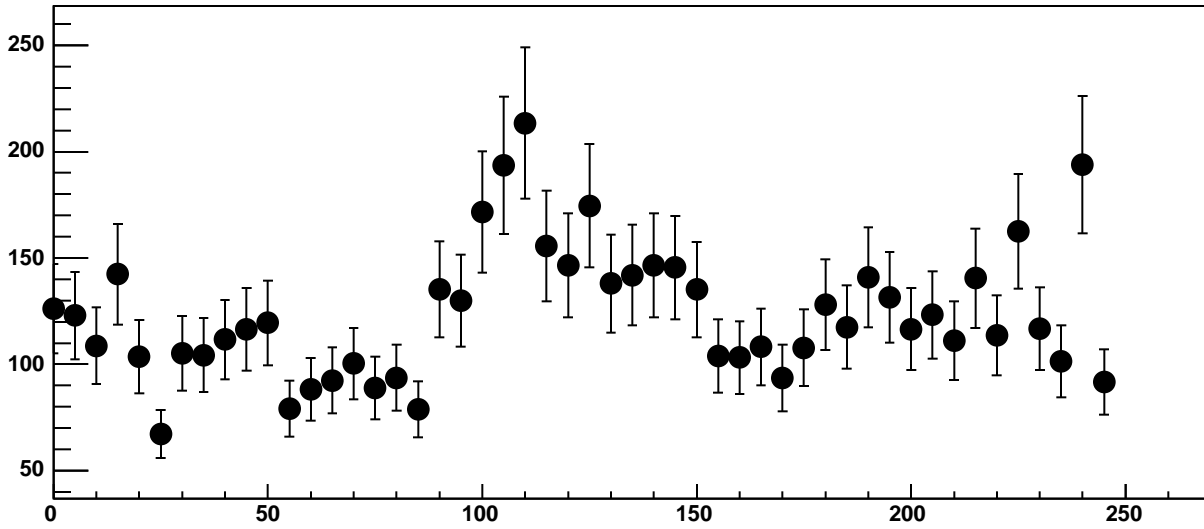


Chip 10, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold

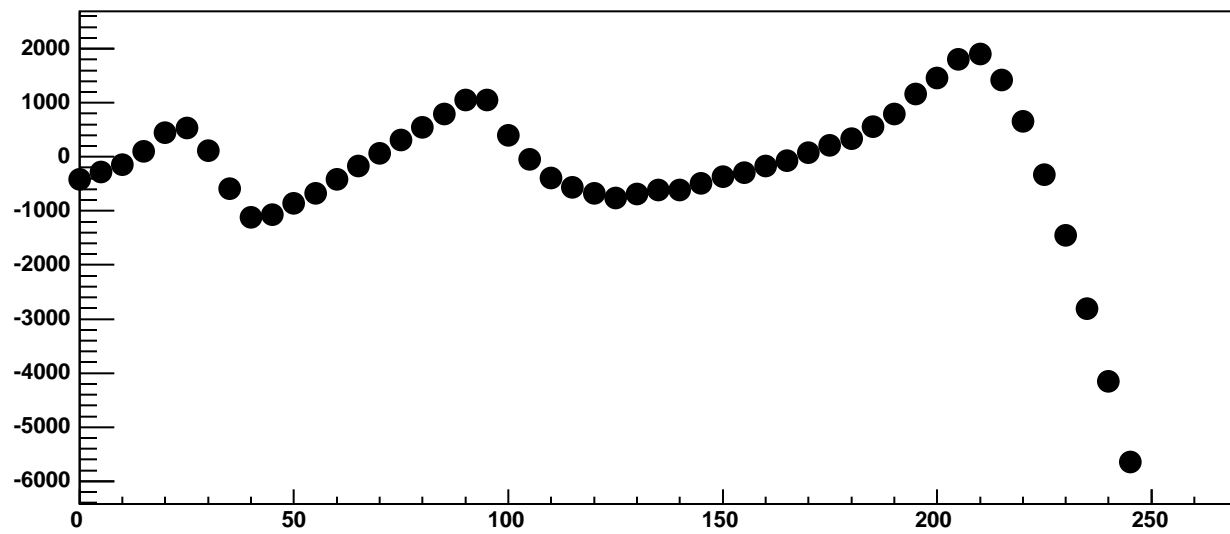


$\chi^2 / \text{ndf}$	6.087e+04 / 41
p0	-4516 ± 9.752
p1	91.13 ± 0.05041
p2	2.856e+04 ± 53.44
p3	51.63 ± 0.1345
p4	-44.12 ± 0.2346

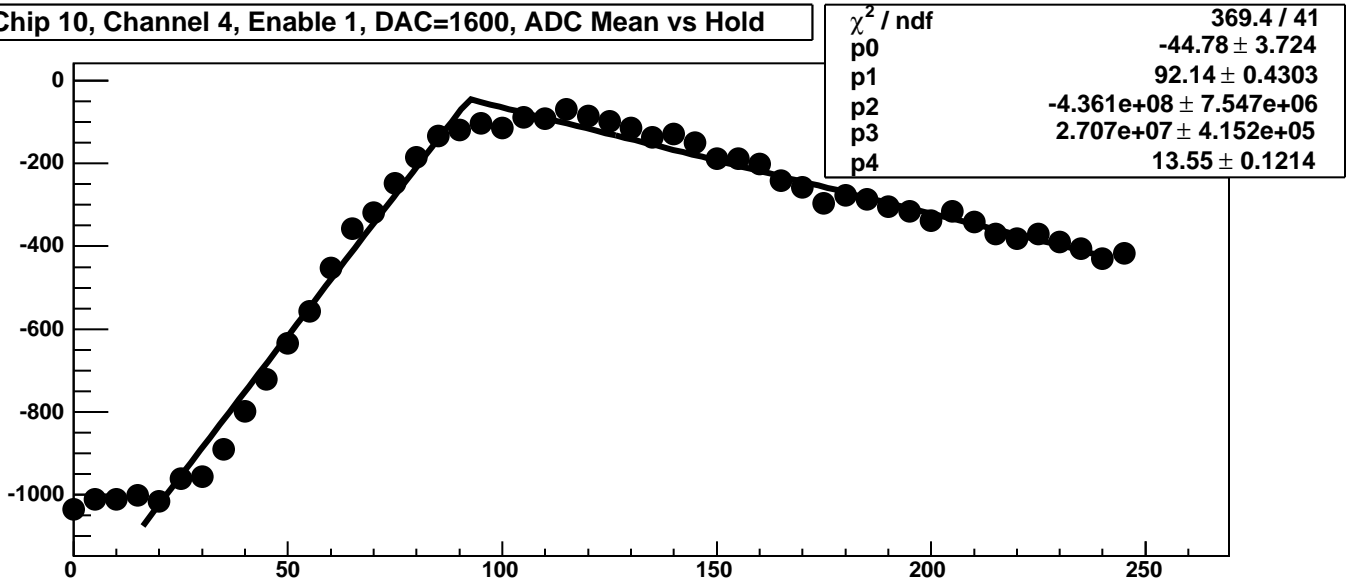
Chip 10, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



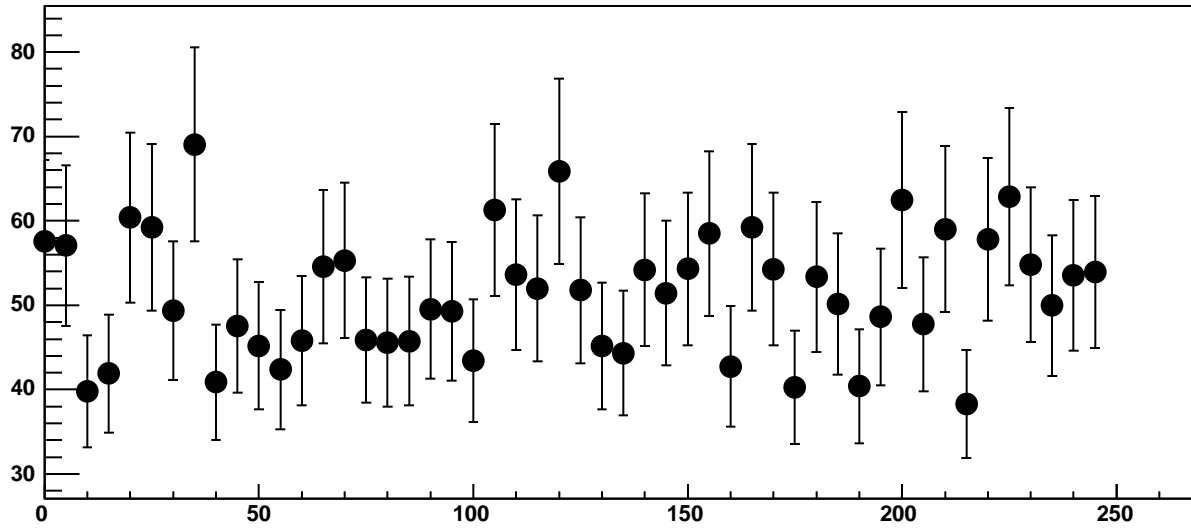
Chip 10, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



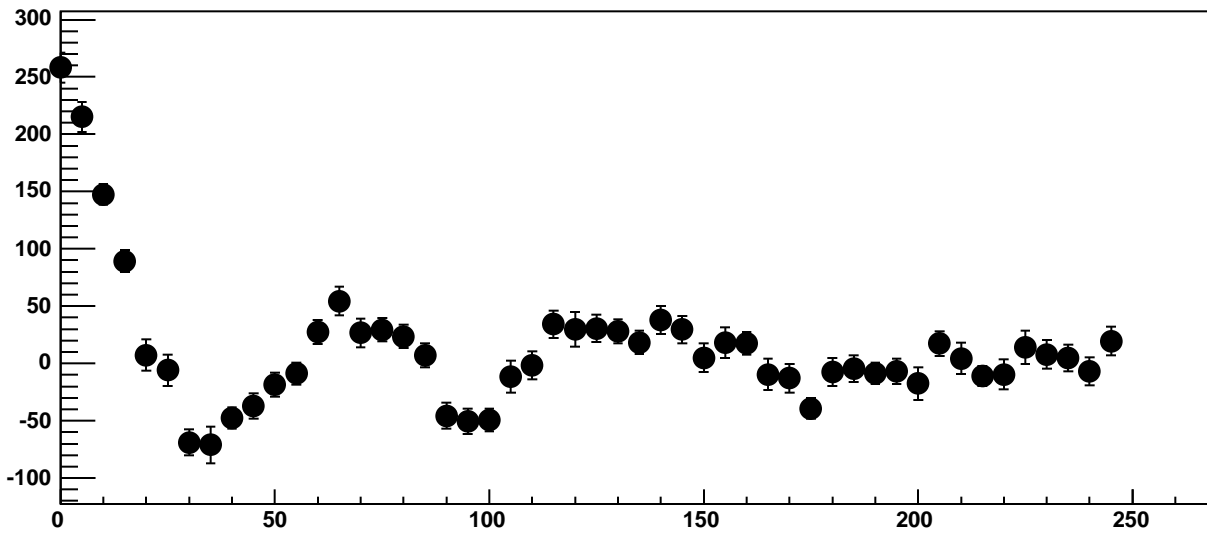
Chip 10, Channel 4, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 10, Channel 4, Enable 1, DAC=1600, ADC Noise vs Hold

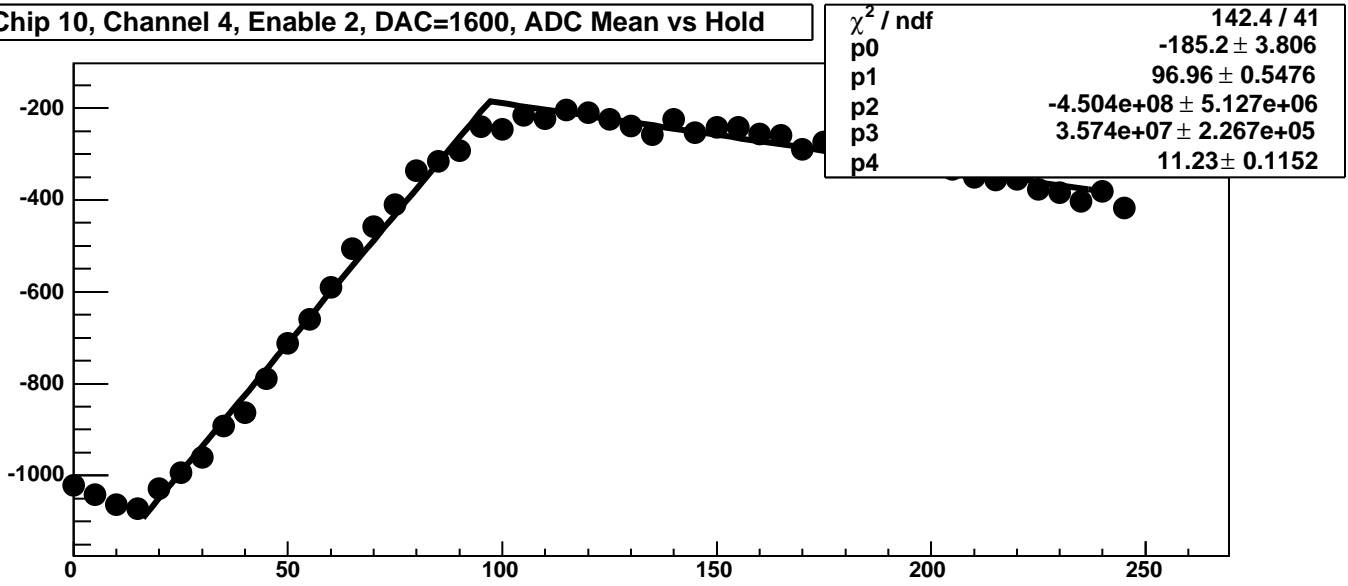


Chip 10, Channel 4, Enable 1, DAC=1600, ADC Residuals vs Hold

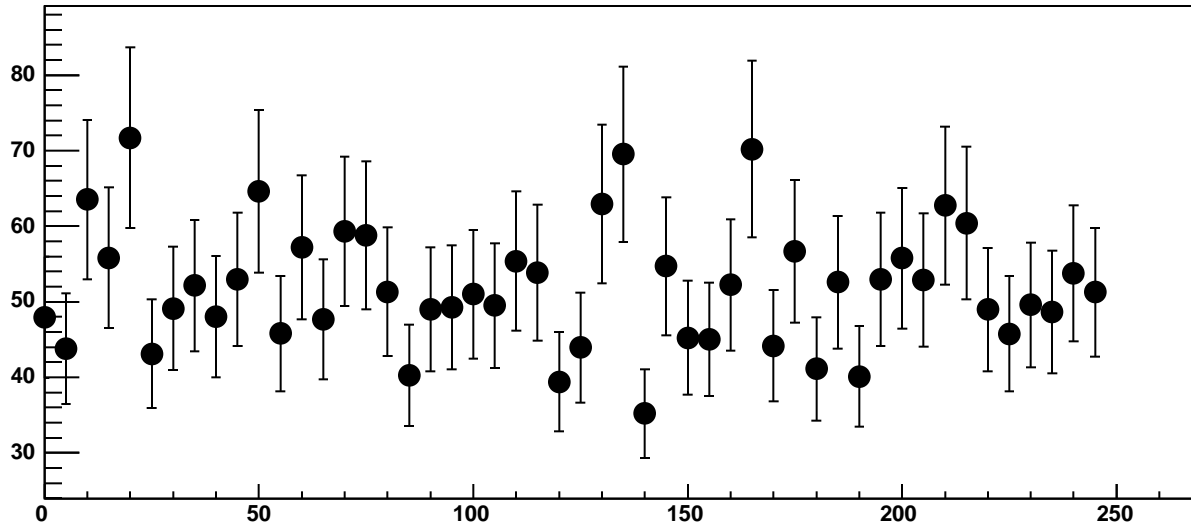




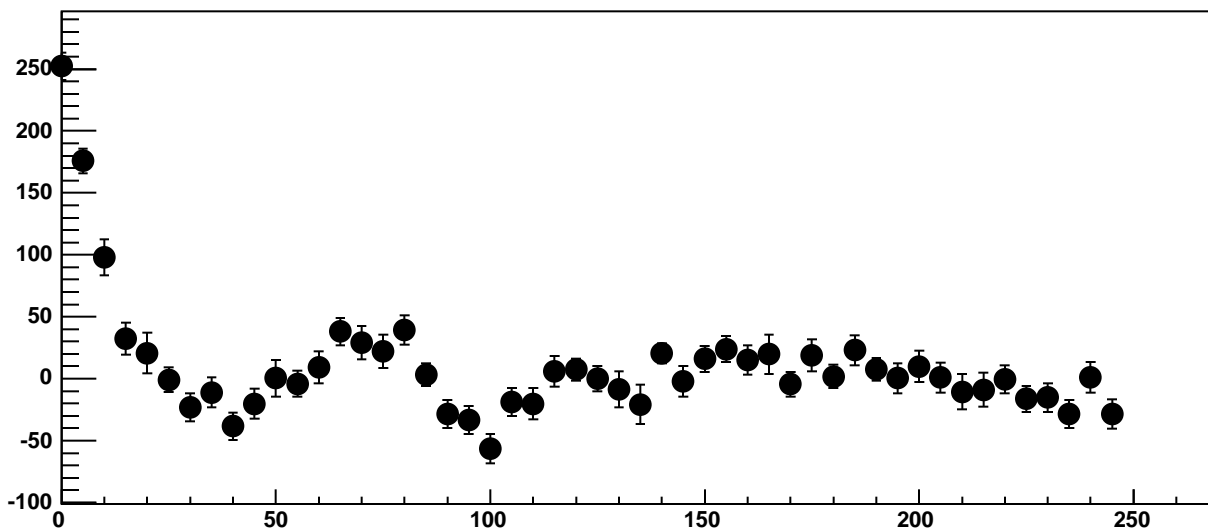
Chip 10, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold



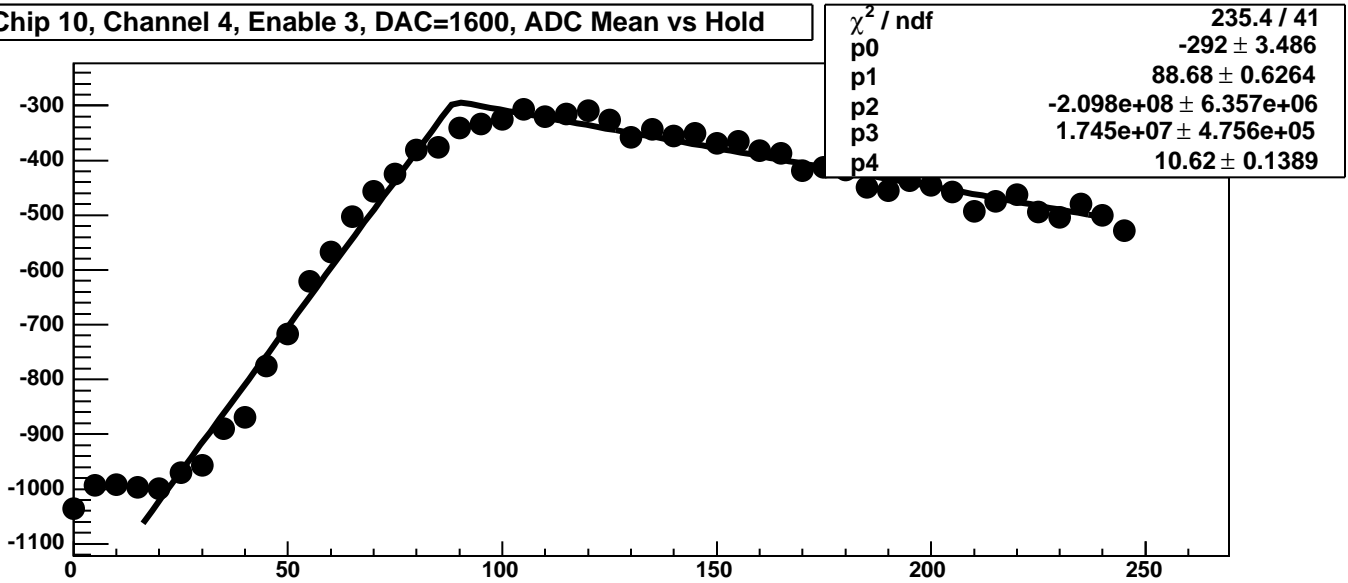
Chip 10, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



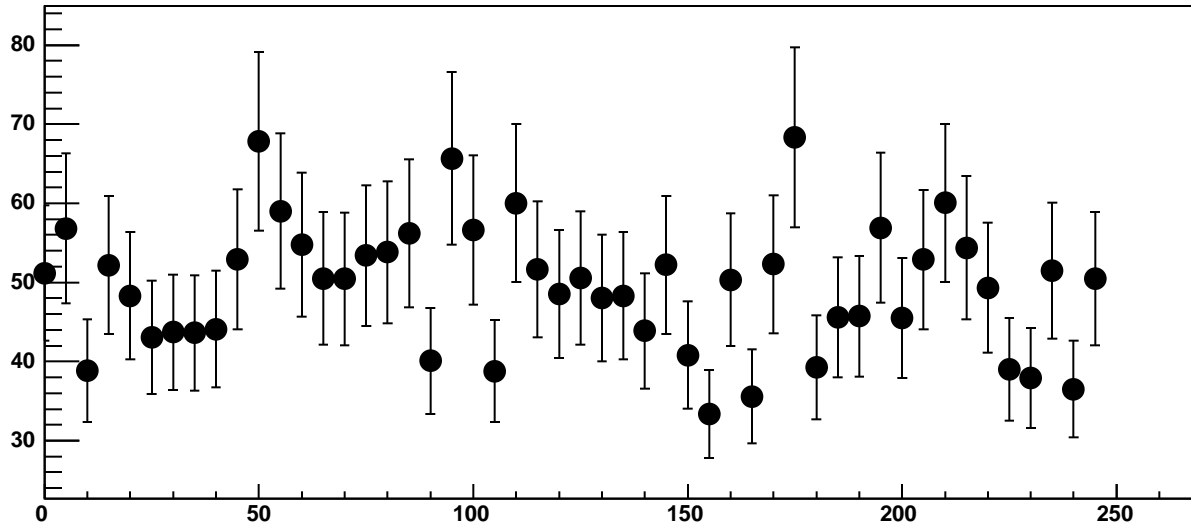
Chip 10, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold



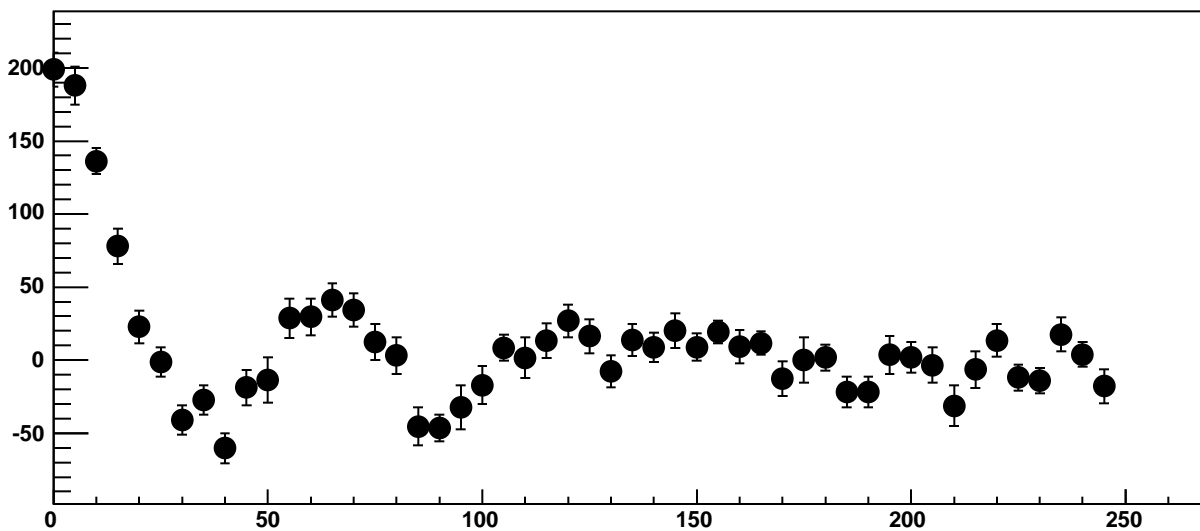
Chip 10, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold



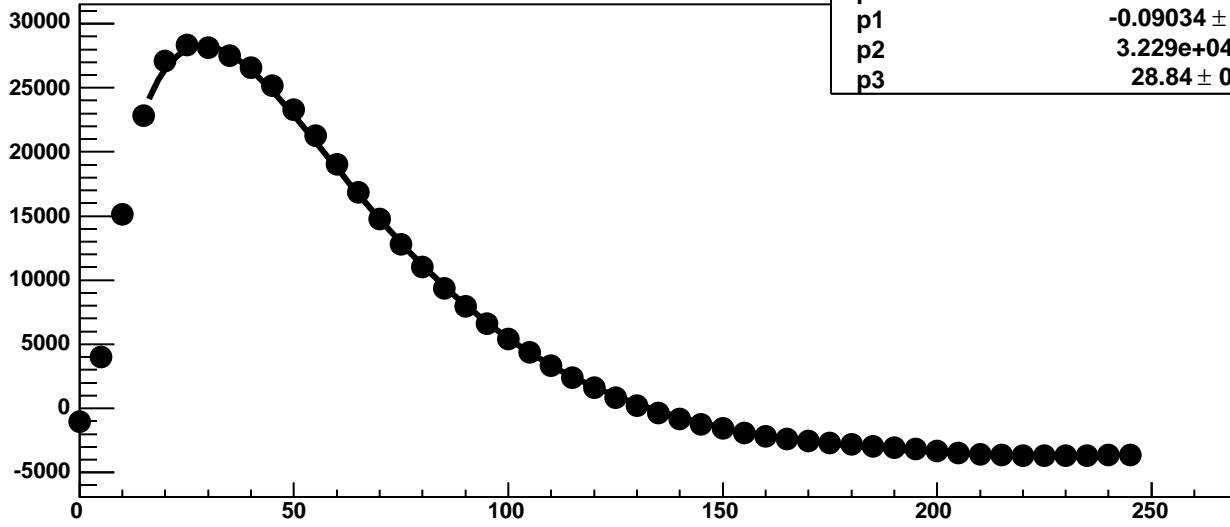
Chip 10, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

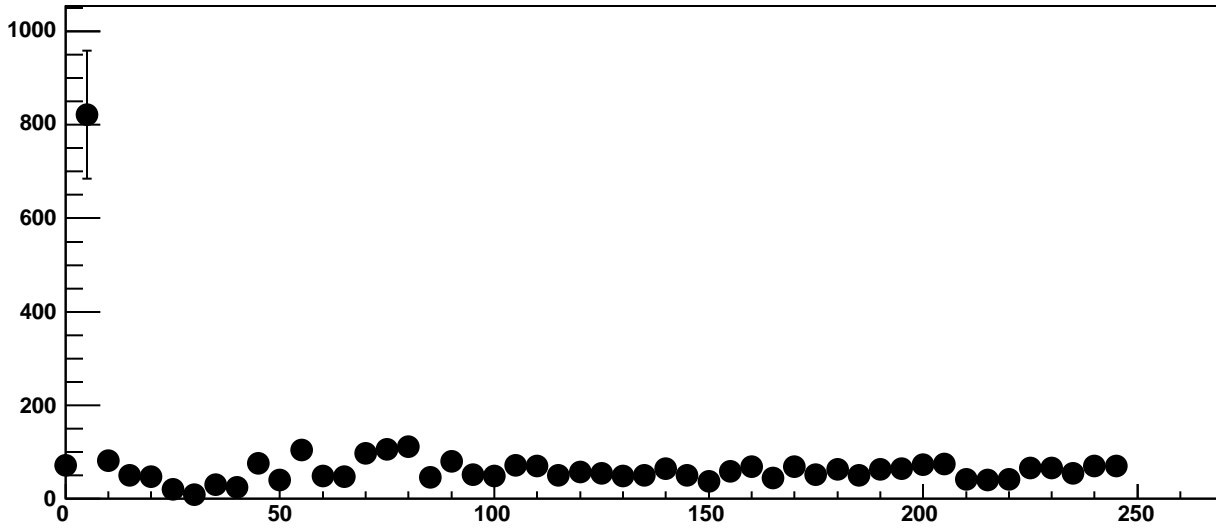


Chip 10, Channel 4, Enable 4!, DAC=1600, ADC Mean vs Hold

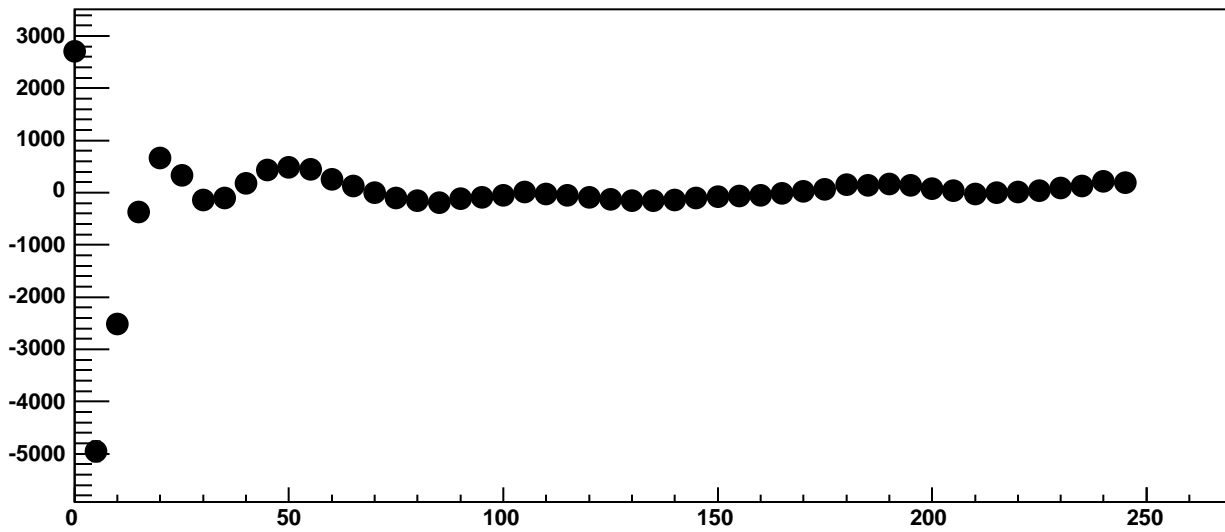


$\chi^2 / \text{ndf}$	2.103e+04 / 42
p0	-4005 ± 3.462
p1	-0.09034 ± 0.01349
p2	3.229e+04 ± 3.724
p3	28.84 ± 0.008713

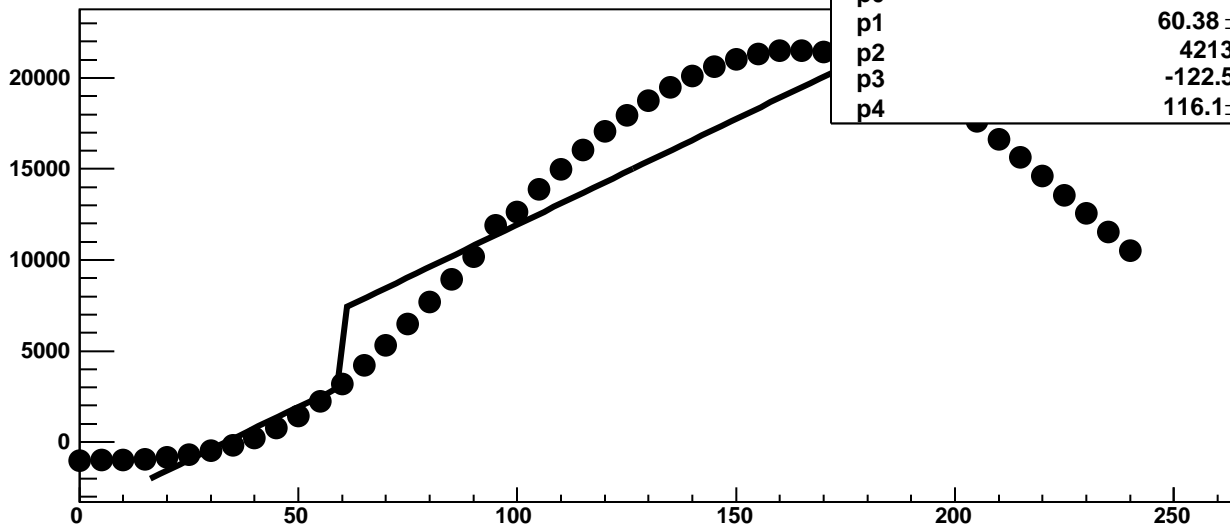
Chip 10, Channel 4, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 4, Enable 4!, DAC=1600, ADC Residuals vs Hold

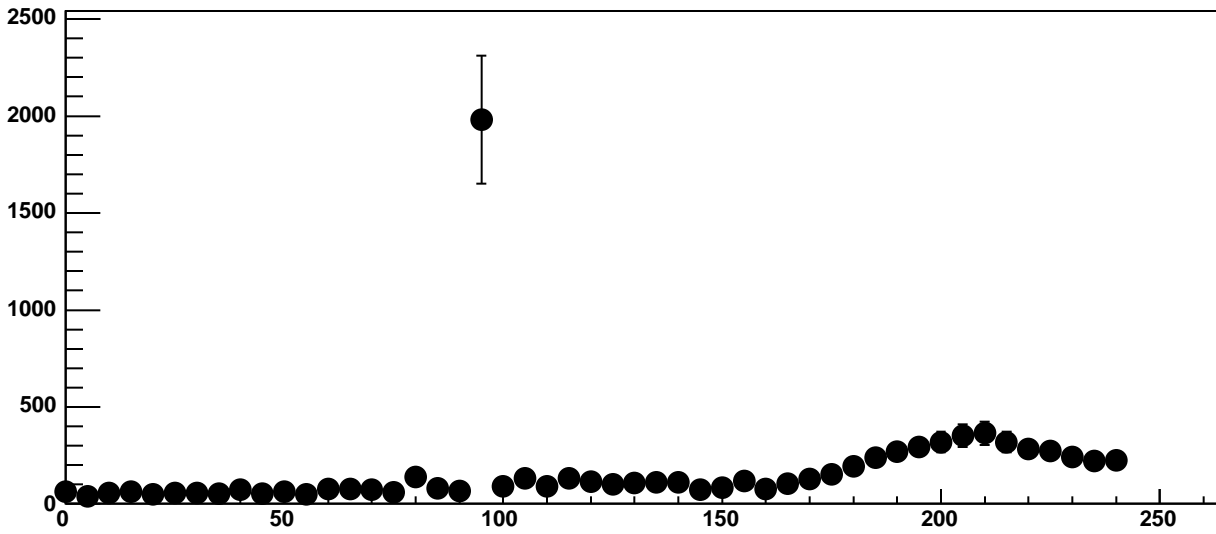


Chip 10, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

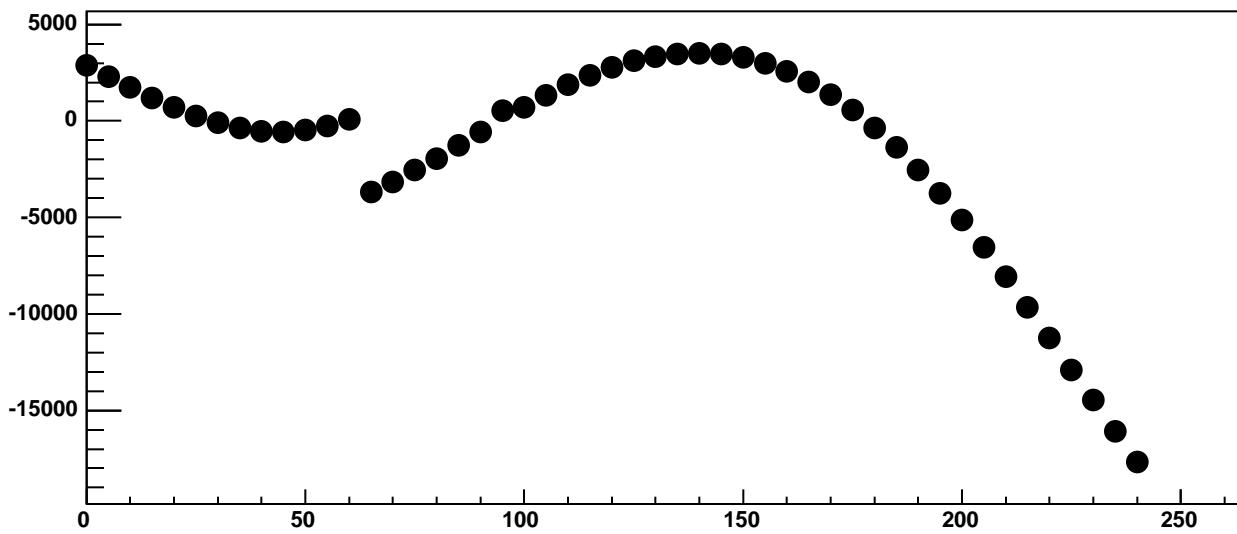


$\chi^2 / \text{ndf}$	7.56e+05 / 41
p0	3128 ± 13.95
p1	60.38 ± 0.1355
p2	4213 ± 30.52
p3	-122.5 ± 15.65
p4	116.1 ± 0.4405

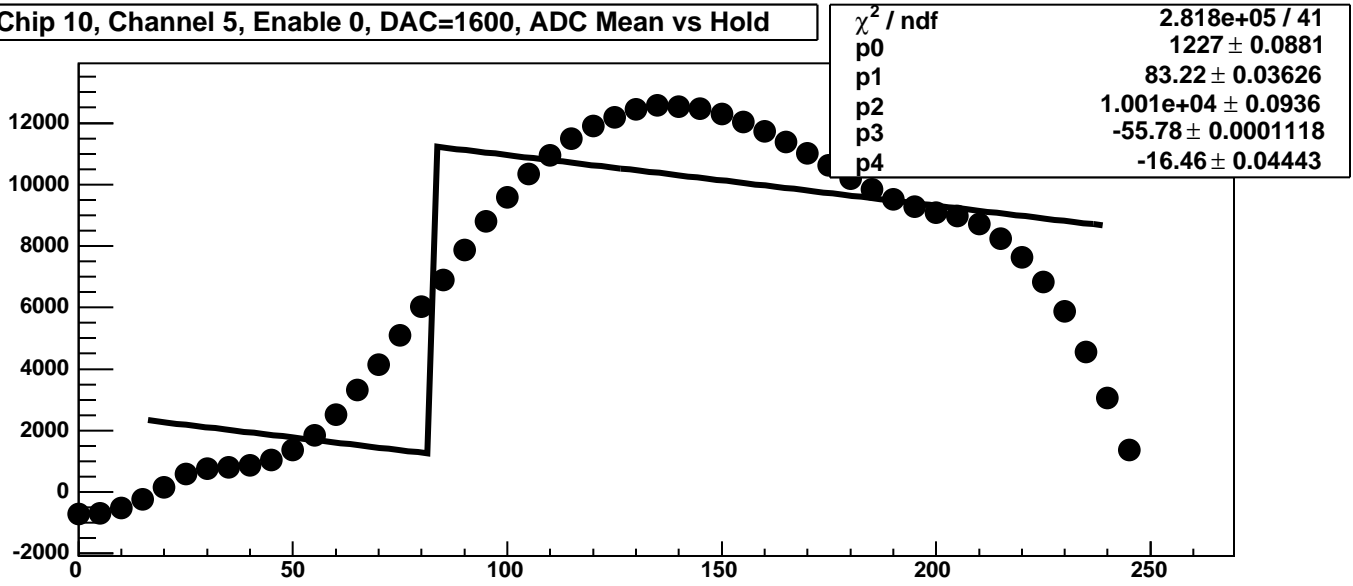
Chip 10, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold



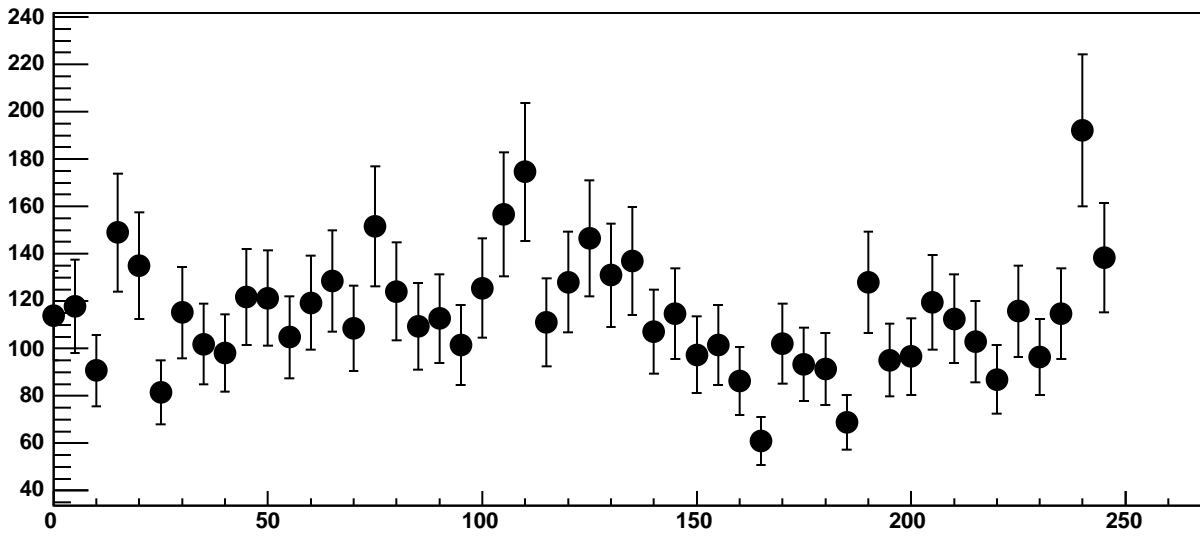
Chip 10, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



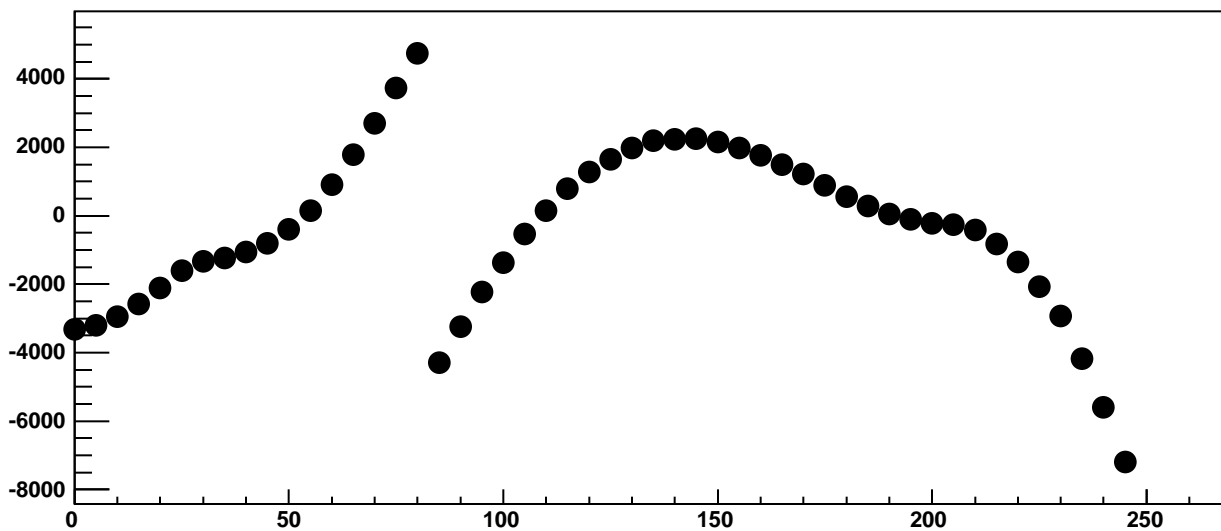
Chip 10, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold



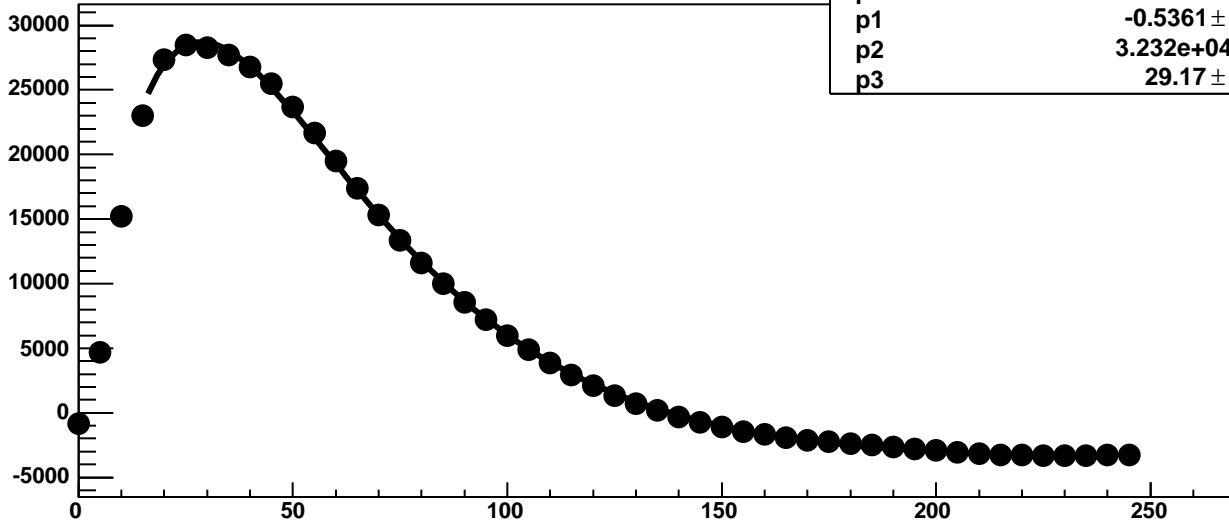
Chip 10, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



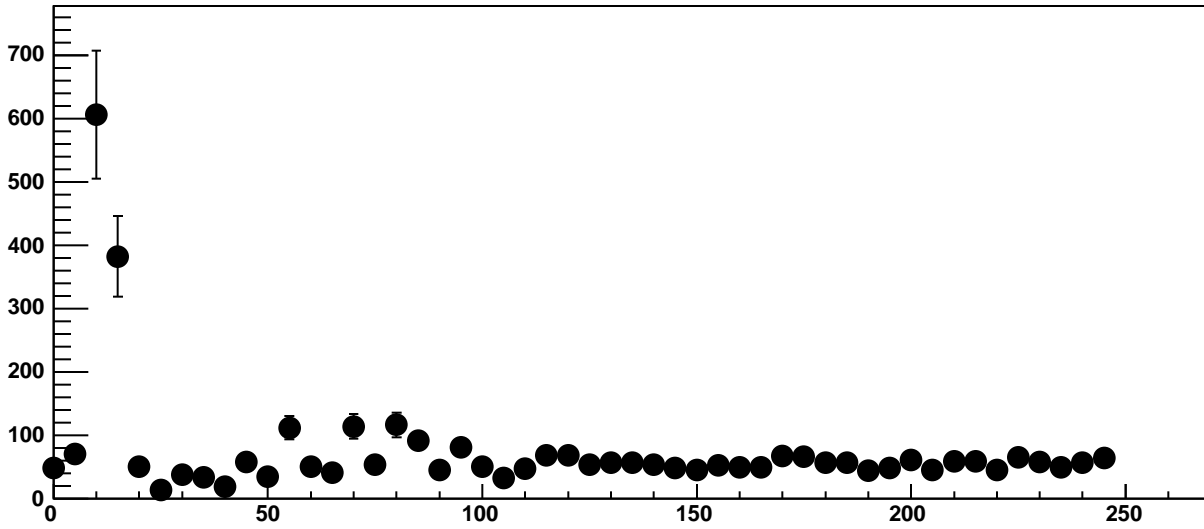
Chip 10, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold



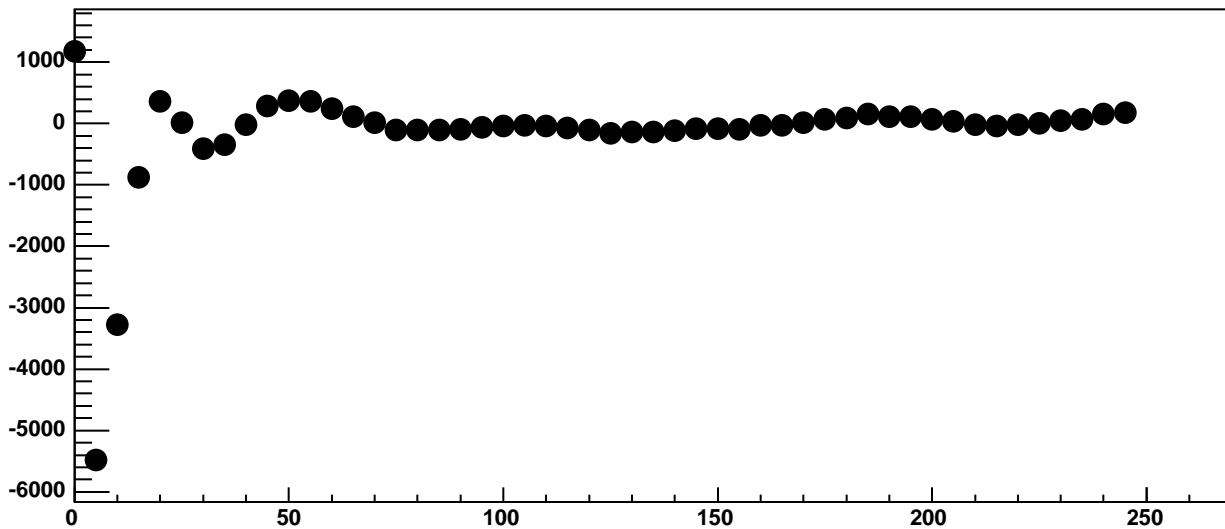
Chip 10, Channel 5, Enable 1!, DAC=1600, ADC Mean vs Hold



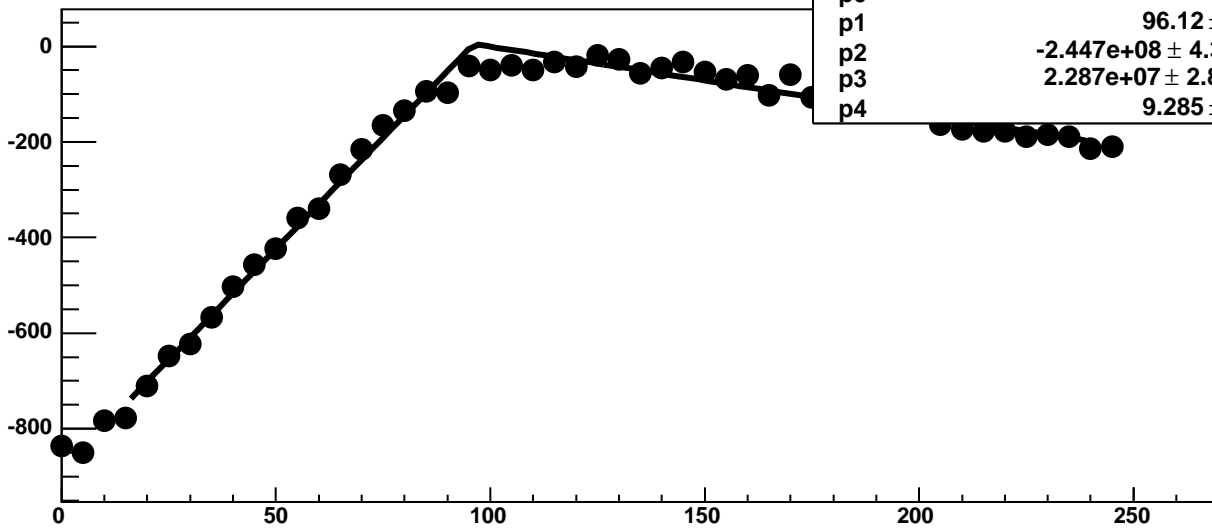
Chip 10, Channel 5, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 5, Enable 1!, DAC=1600, ADC Residuals vs Hold

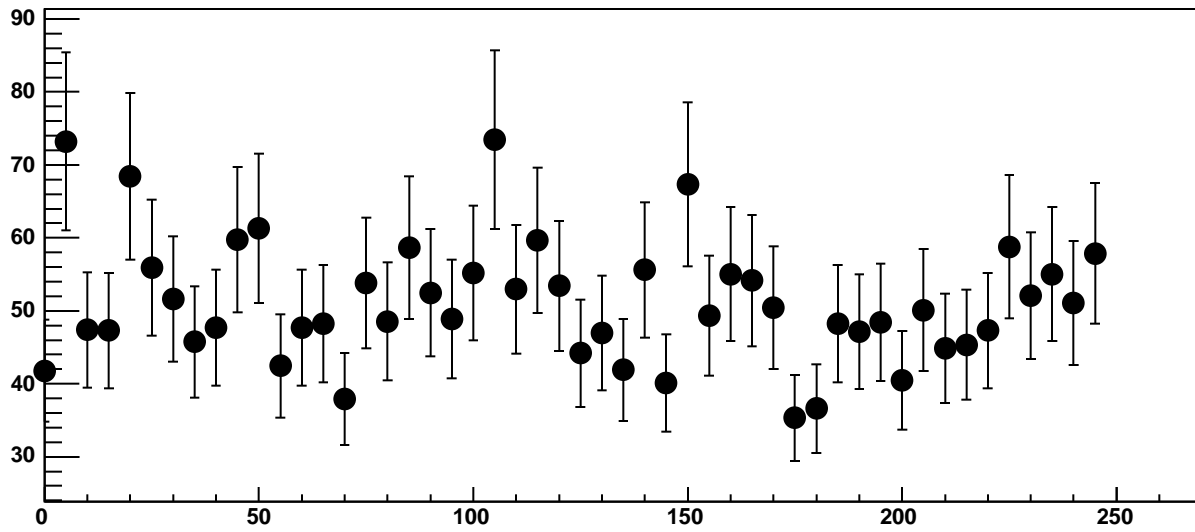


Chip 10, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

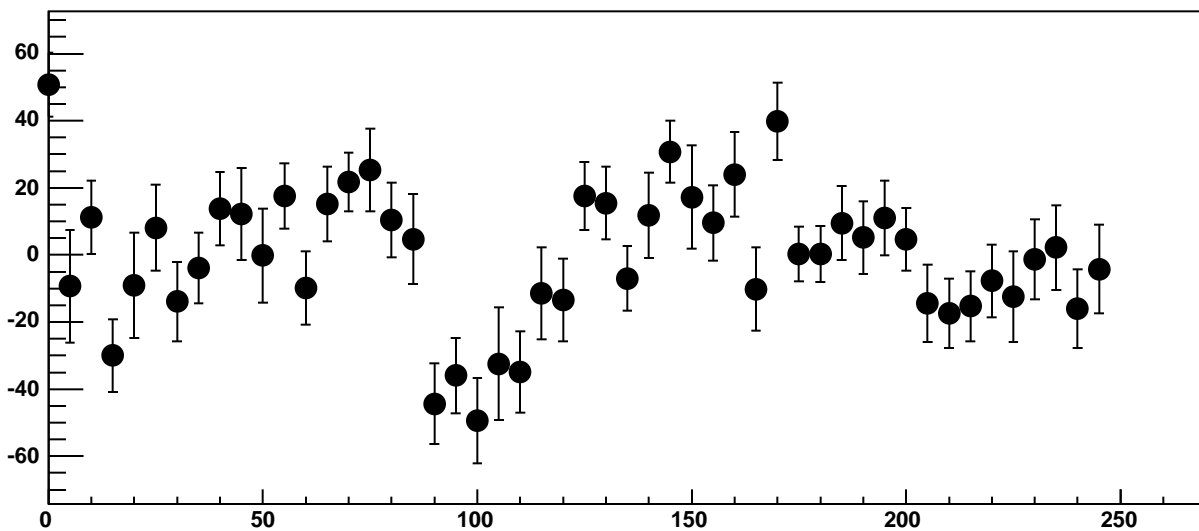


$\chi^2 / \text{ndf}$	130.3 / 41
p0	$4.963 \pm 4.014$
p1	$96.12 \pm 0.6639$
p2	$-2.447\text{e}+08 \pm 4.365\text{e}+06$
p3	$2.287\text{e}+07 \pm 2.826\text{e}+05$
p4	$9.285 \pm 0.1176$

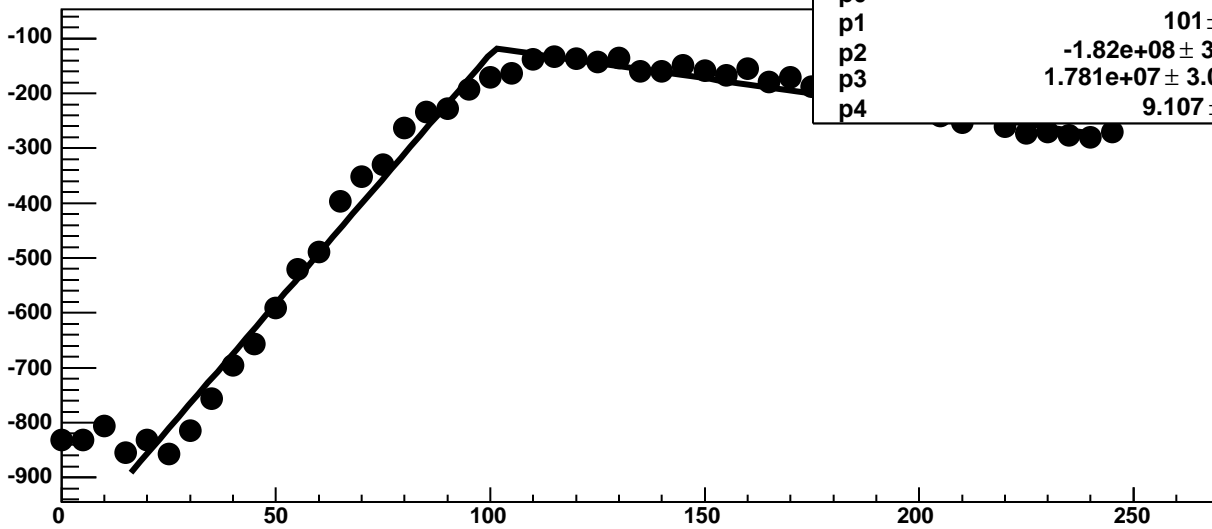
Chip 10, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold

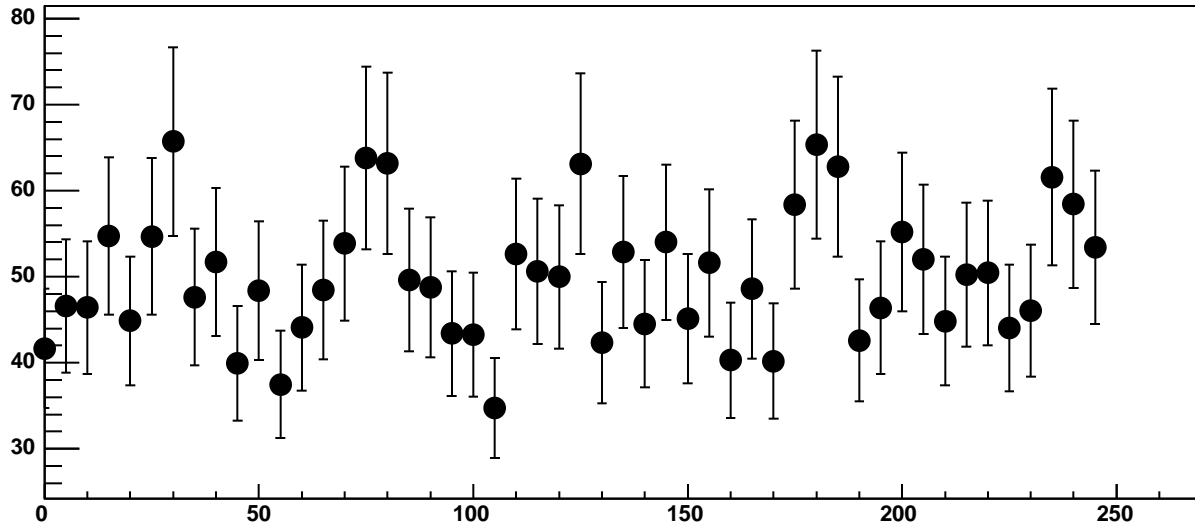


Chip 10, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold

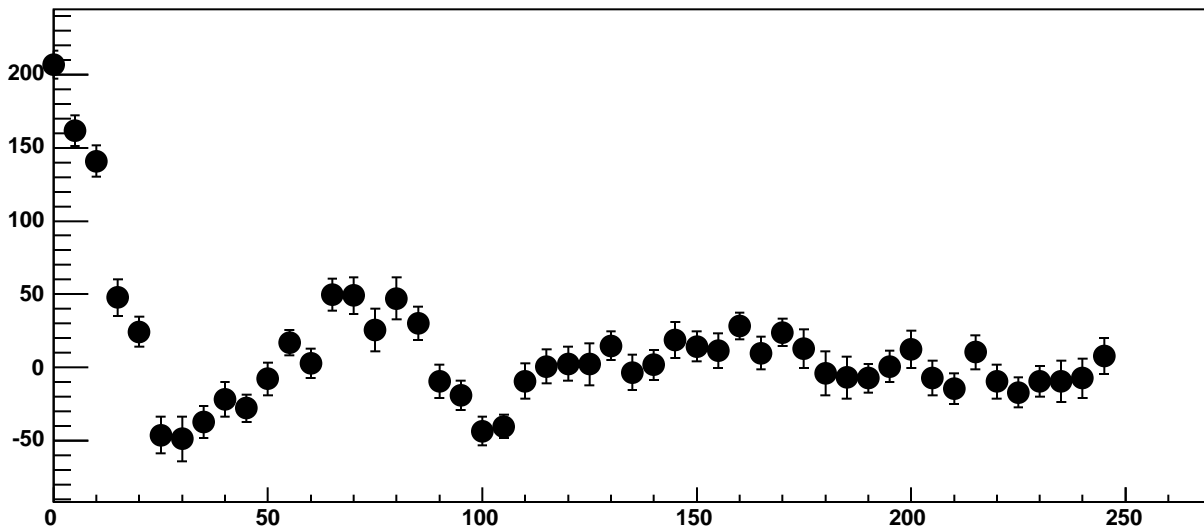


$\chi^2 / \text{ndf}$	214.8 / 41
p0	$-118.2 \pm 3.725$
p1	$101 \pm 0.6425$
p2	$-1.82\text{e}+08 \pm 3.78\text{e}+06$
p3	$1.781\text{e}+07 \pm 3.098\text{e}+05$
p4	$9.107 \pm 0.1023$

Chip 10, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold

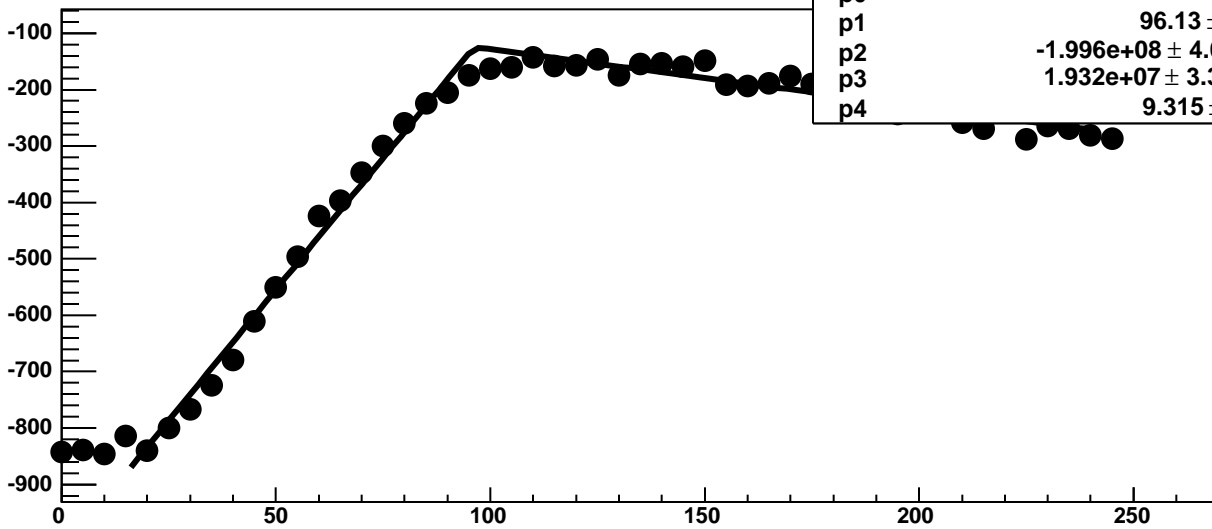


Chip 10, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold



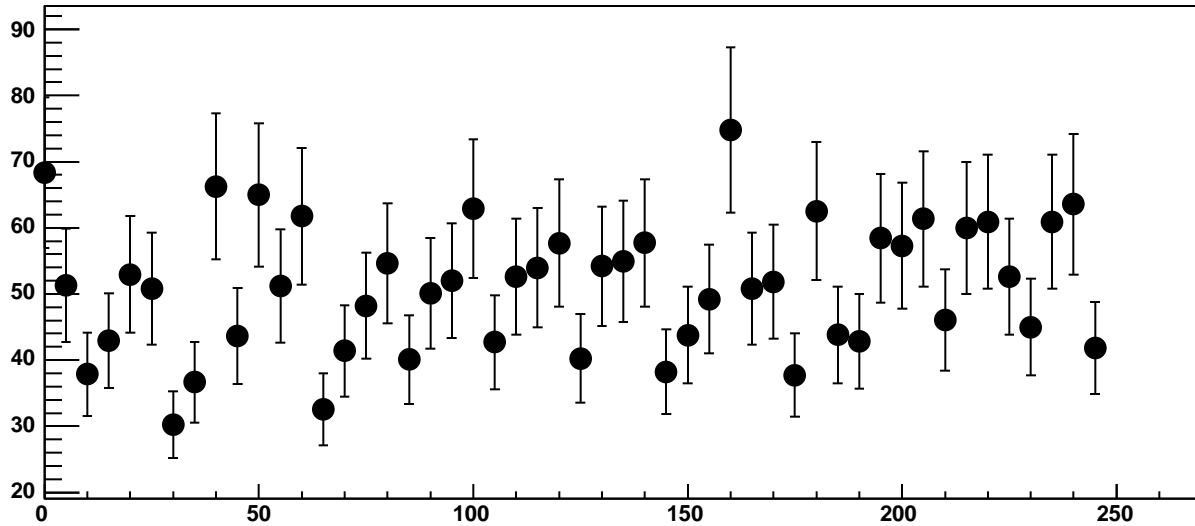


Chip 10, Channel 5, Enable 4, DAC=1600, ADC Mean vs Hold

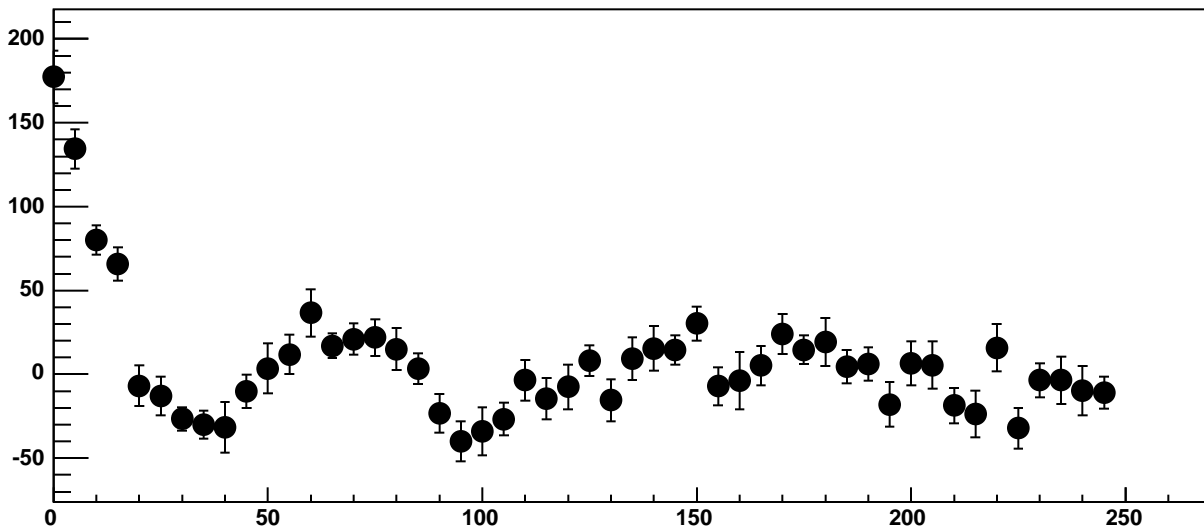


$\chi^2 / \text{ndf}$	175.8 / 41
p0	-124.4 ± 4
p1	96.13 ± 0.6494
p2	-1.996e+08 ± 4.096e+06
p3	1.932e+07 ± 3.339e+05
p4	9.315 ± 0.1029

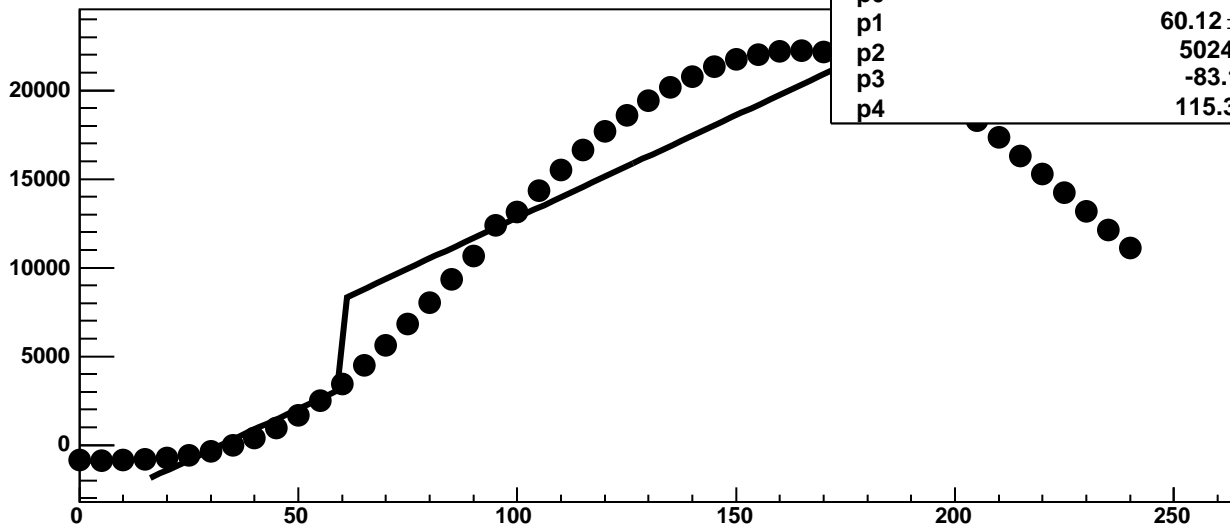
Chip 10, Channel 5, Enable 4, DAC=1600, ADC Noise vs Hold



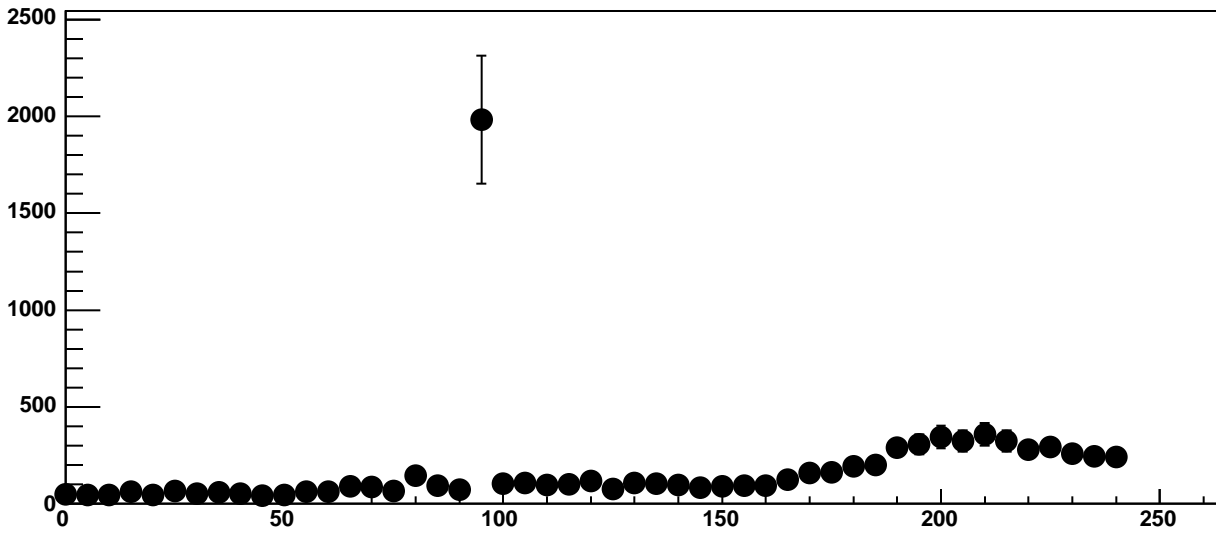
Chip 10, Channel 5, Enable 4, DAC=1600, ADC Residuals vs Hold



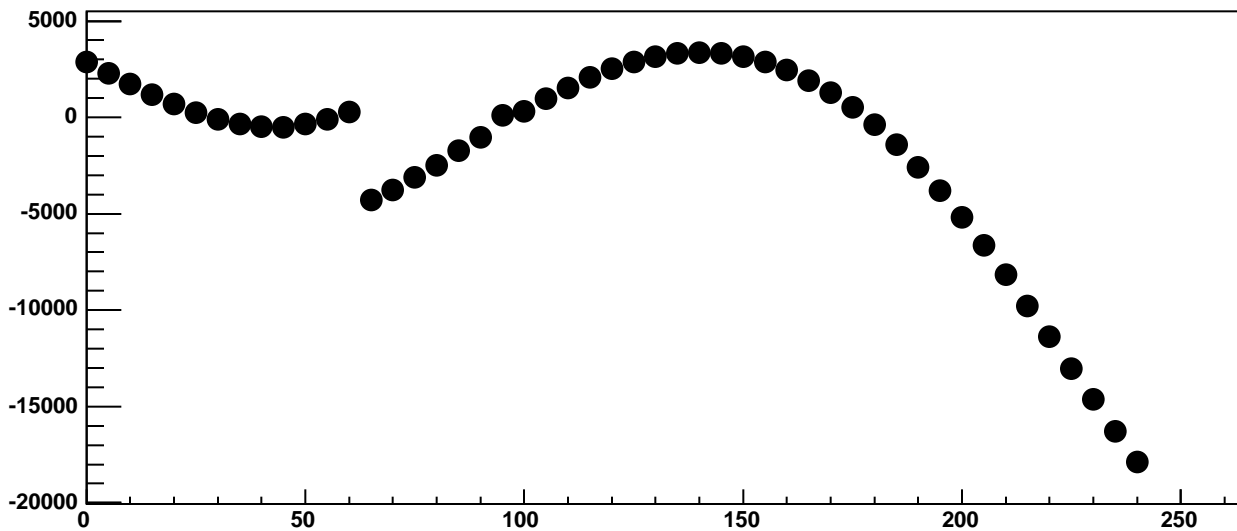
Chip 10, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold



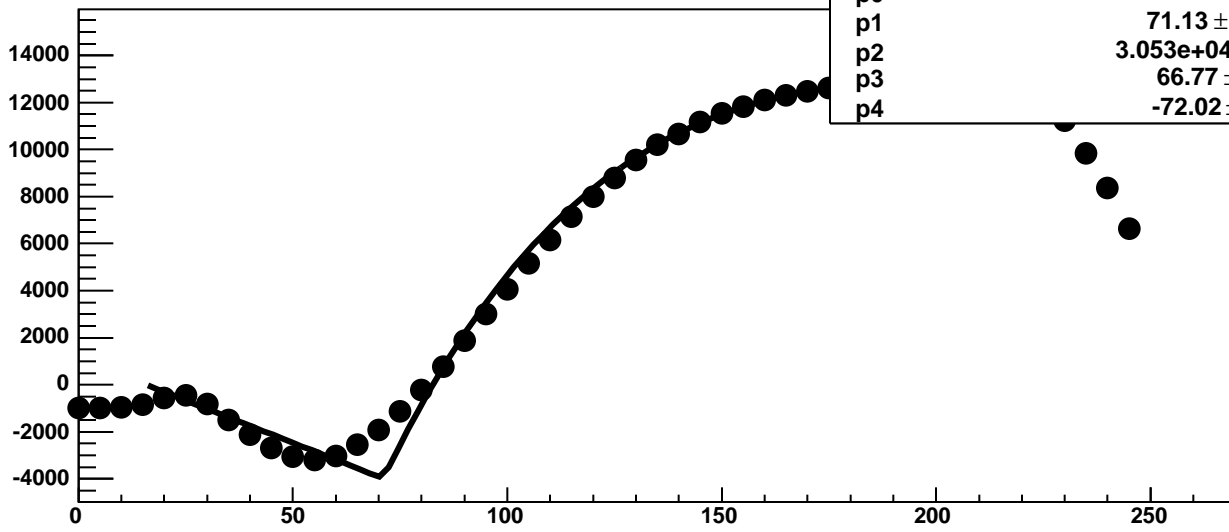
Chip 10, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

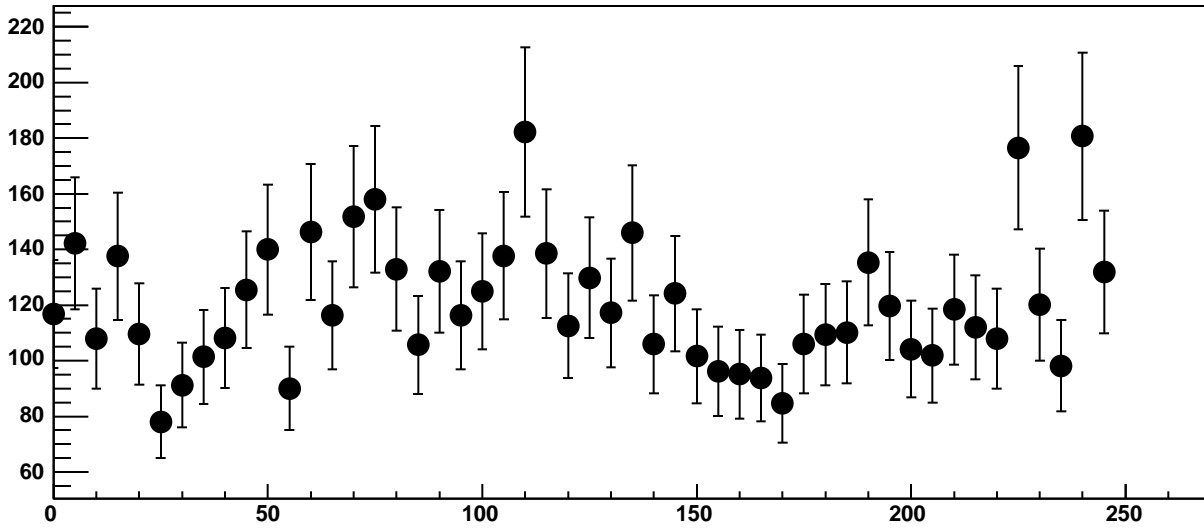


Chip 10, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

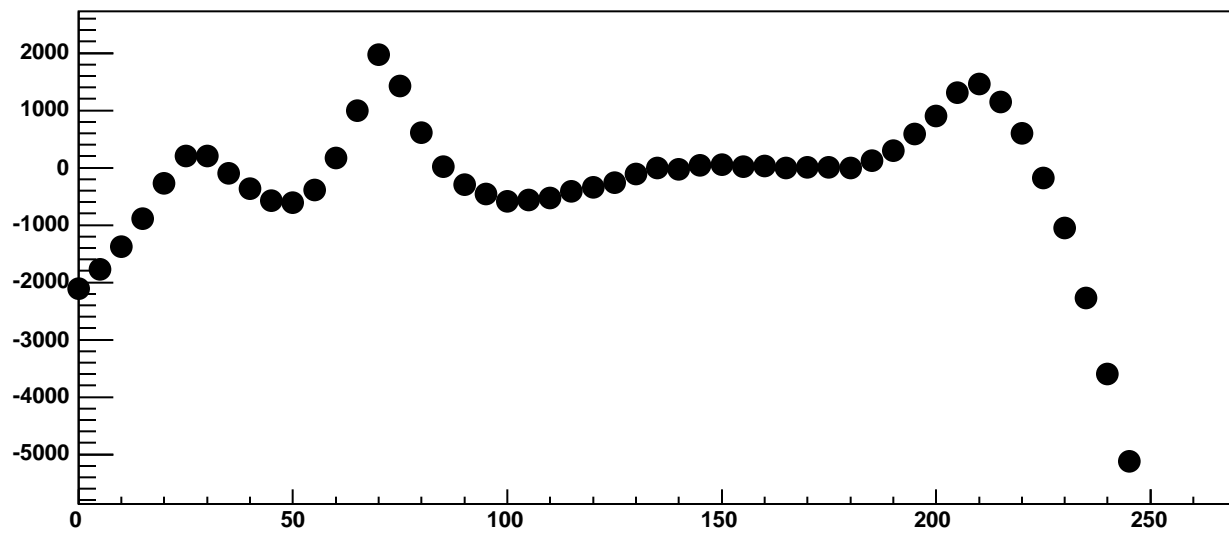


$\chi^2 / \text{ndf}$	4.063e+04 / 41
p0	-3986 ± 12.35
p1	71.13 ± 0.05861
p2	3.053e+04 ± 101.7
p3	66.77 ± 0.2224
p4	-72.02 ± 0.4023

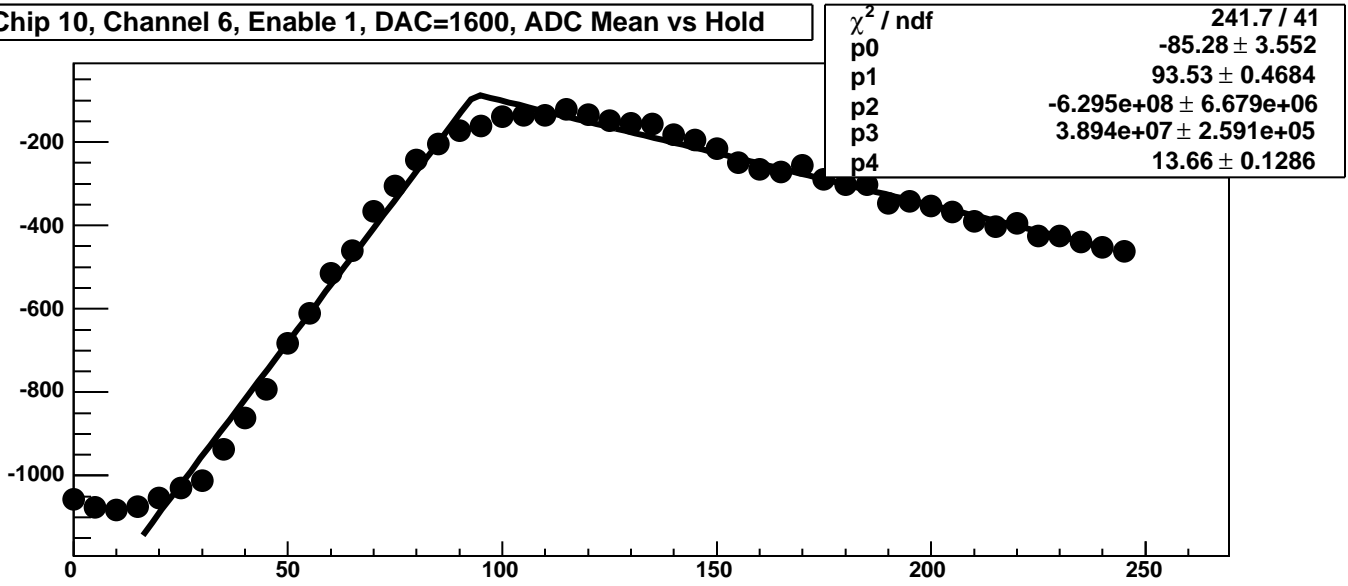
Chip 10, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



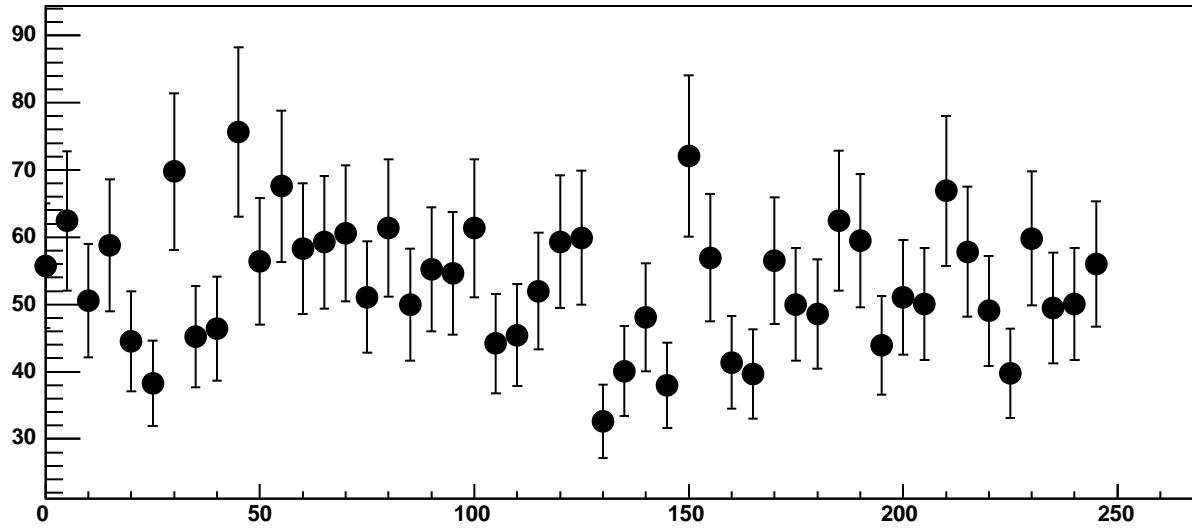
Chip 10, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



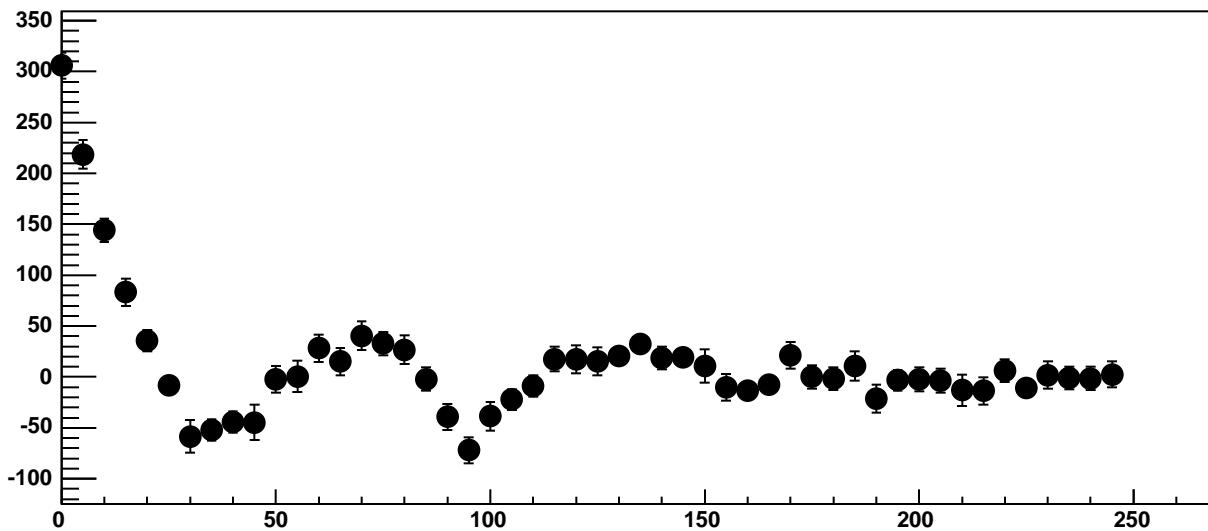
Chip 10, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



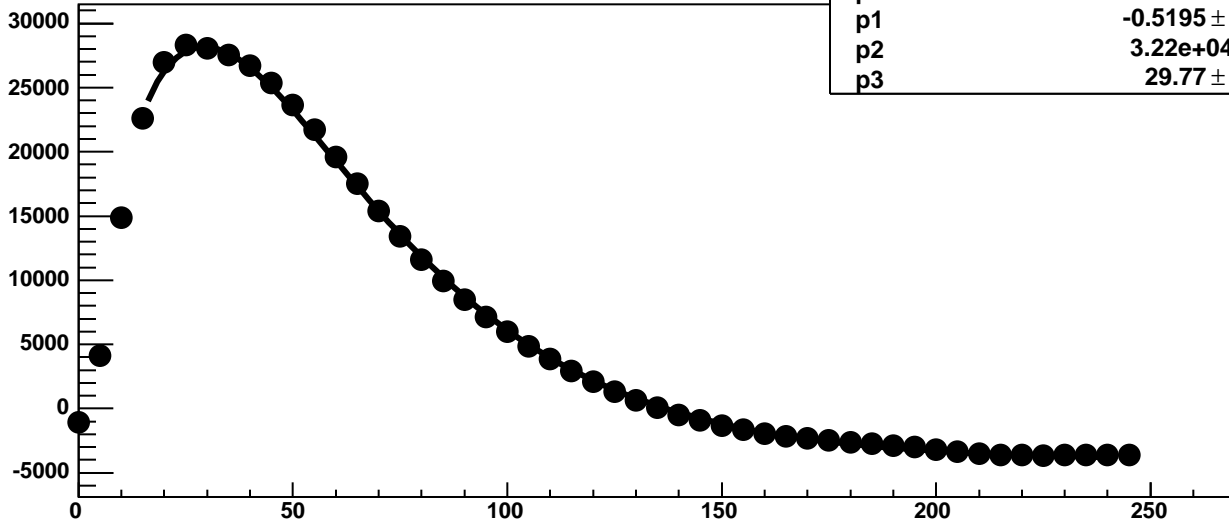
Chip 10, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold

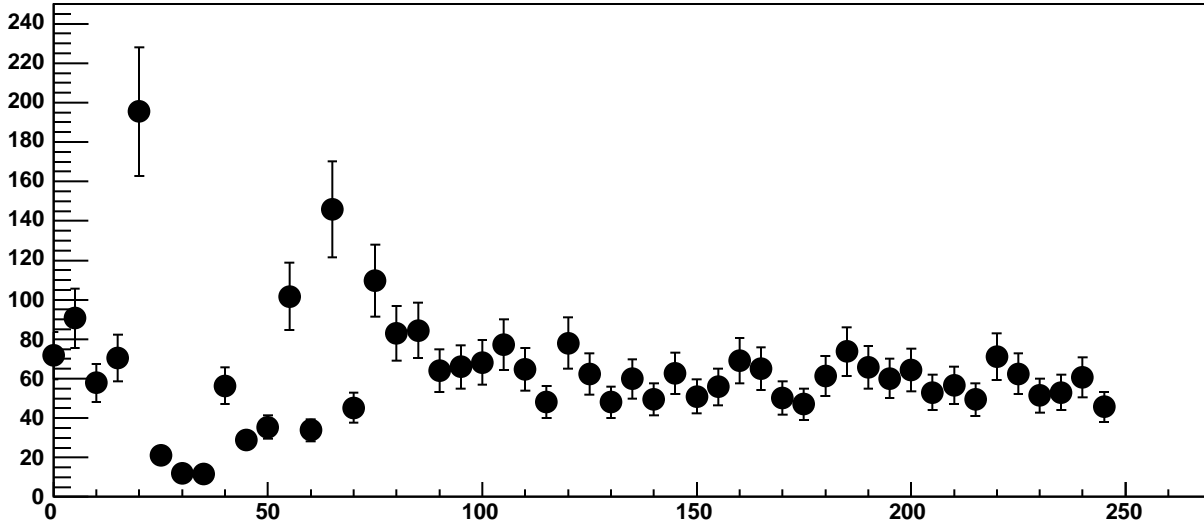


Chip 10, Channel 6, Enable 2!, DAC=1600, ADC Mean vs Hold

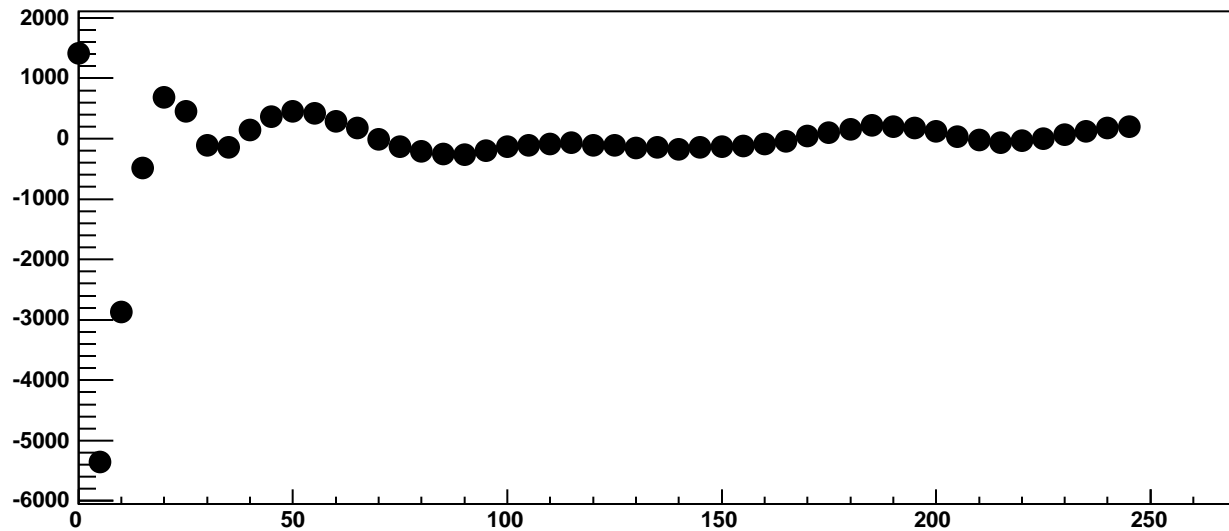


$\chi^2 / \text{ndf}$	2.559e+04 / 42
p0	-3999 ± 3.785
p1	-0.5195 ± 0.01688
p2	3.22e+04 ± 4.077
p3	29.77 ± 0.01025

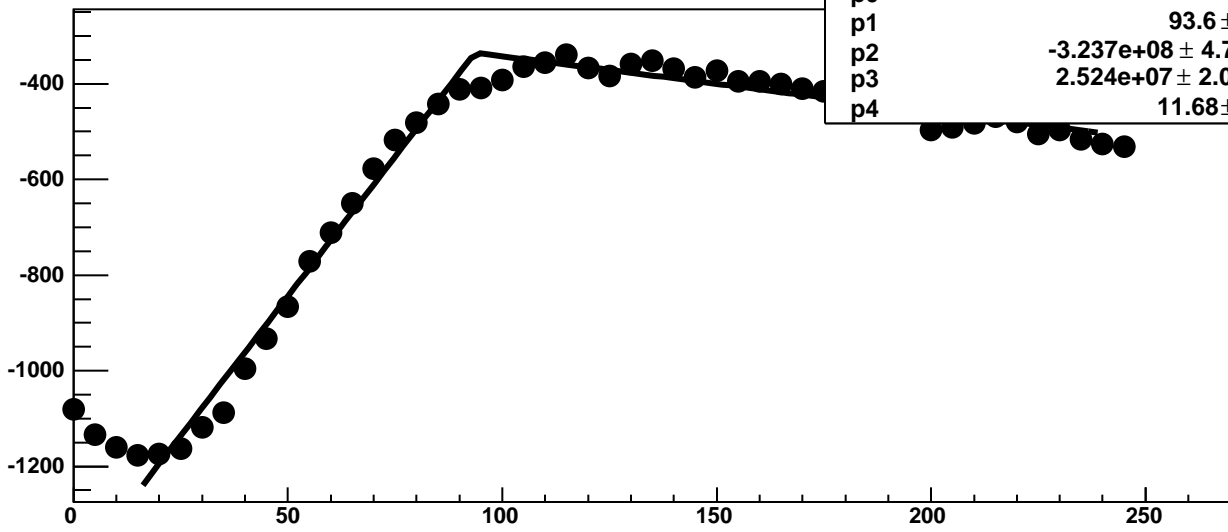
Chip 10, Channel 6, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 6, Enable 2!, DAC=1600, ADC Residuals vs Hold

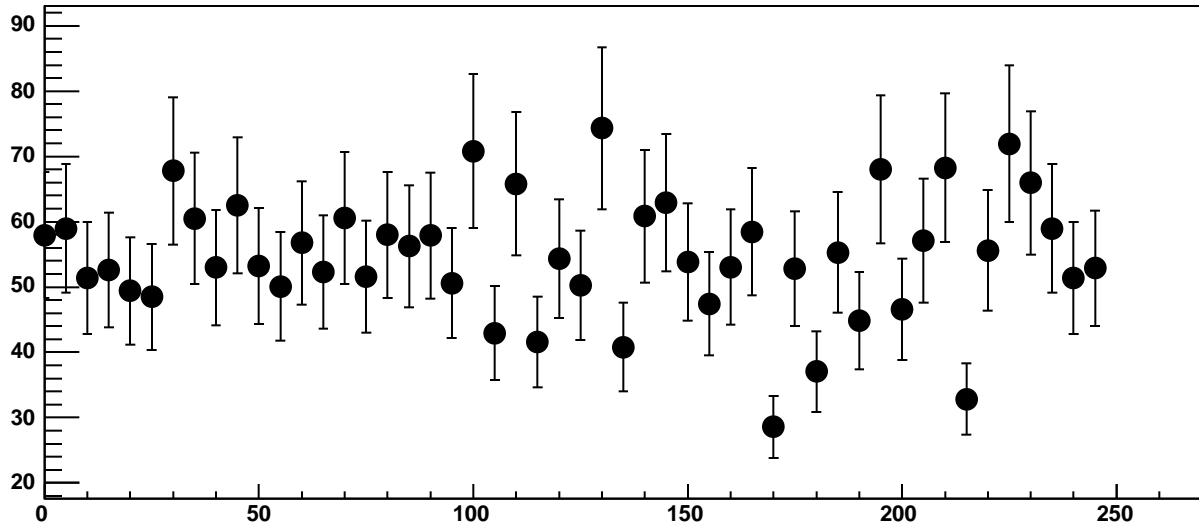


Chip 10, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

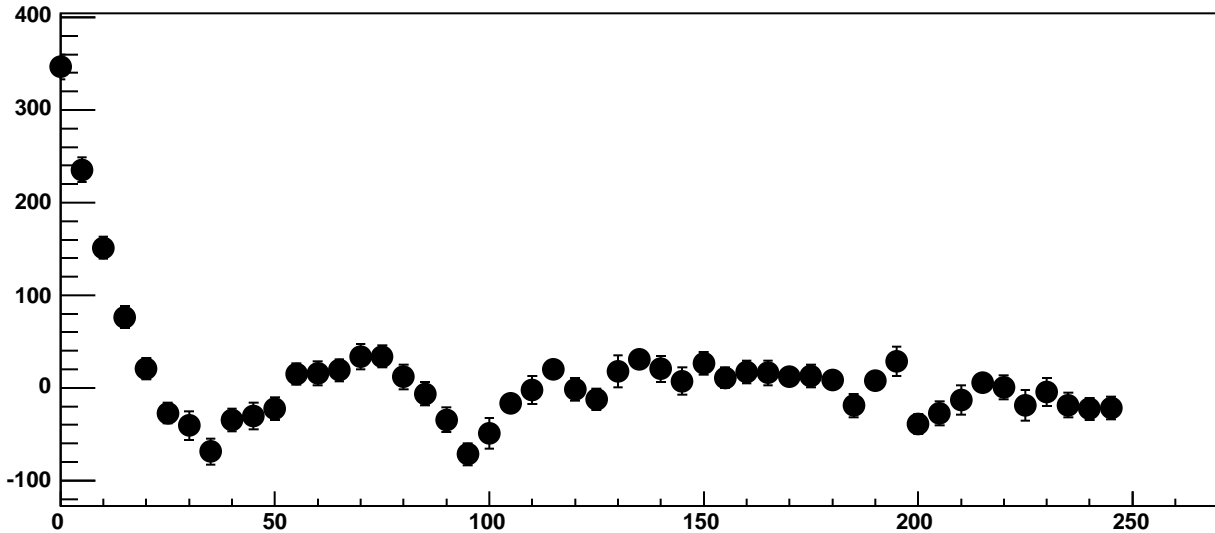


$\chi^2 / \text{ndf}$	240.8 / 41
p0	$-334.9 \pm 3.987$
p1	$93.6 \pm 0.6089$
p2	$-3.237\text{e}+08 \pm 4.742\text{e}+06$
p3	$2.524\text{e}+07 \pm 2.088\text{e}+05$
p4	$11.68 \pm 0.1359$

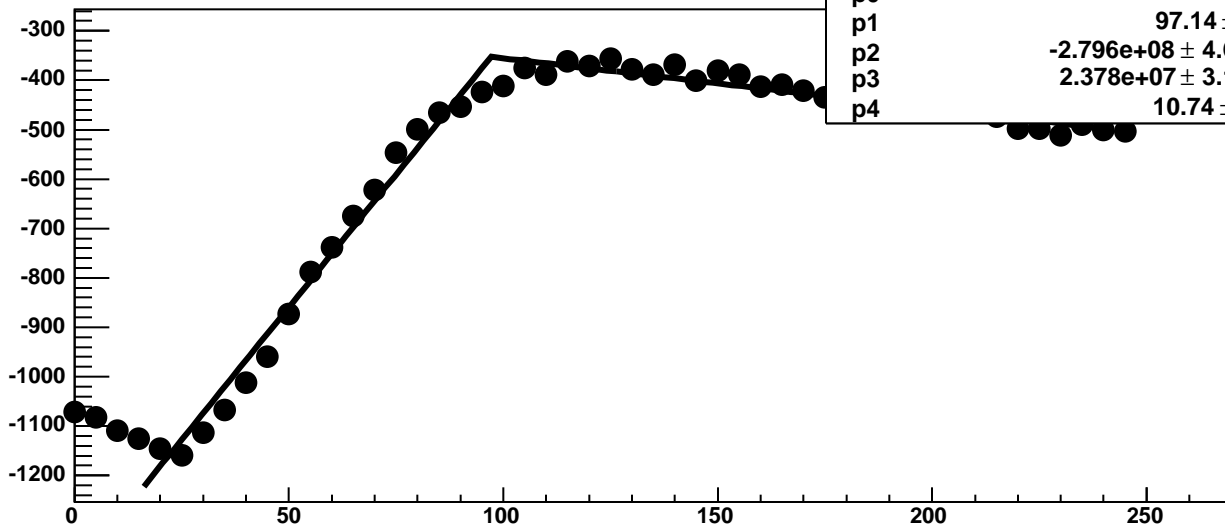
Chip 10, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold

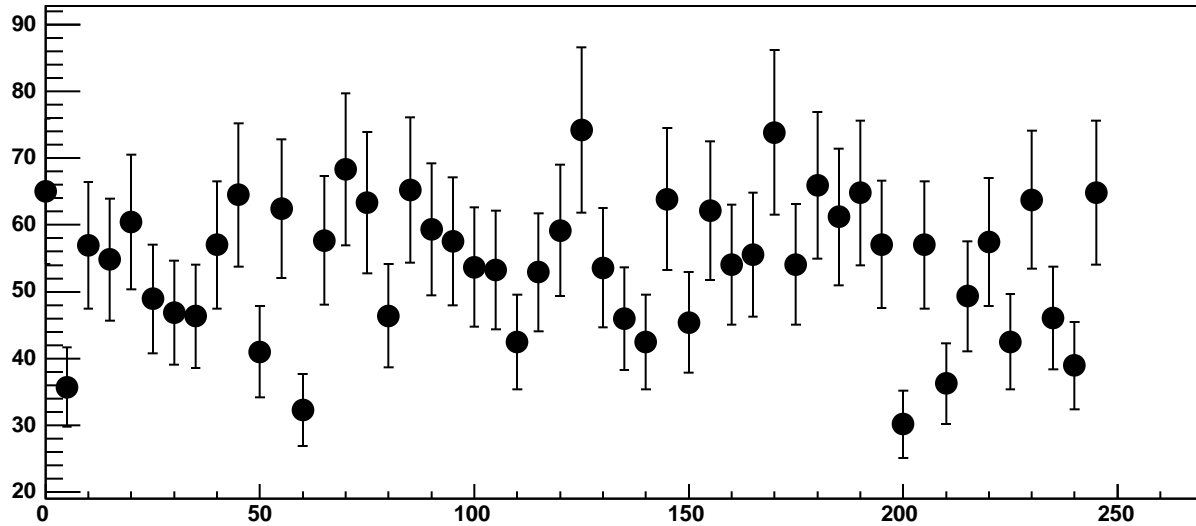


Chip 10, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold

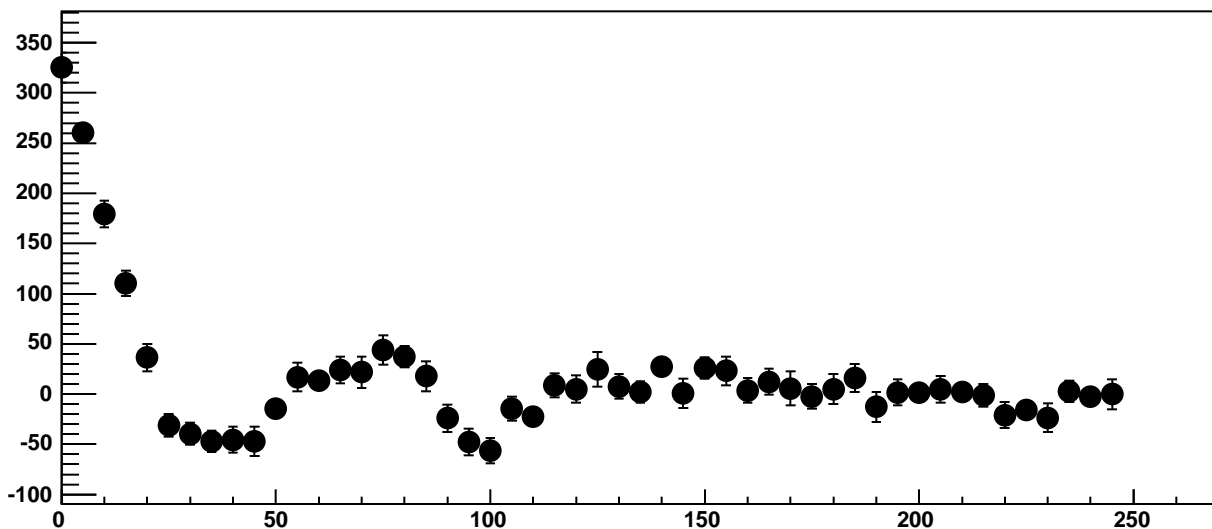


$\chi^2 / \text{ndf}$	256.9 / 41
p0	$-352.6 \pm 4.048$
p1	$97.14 \pm 0.6457$
p2	$-2.796\text{e}+08 \pm 4.686\text{e}+06$
p3	$2.378\text{e}+07 \pm 3.118\text{e}+05$
p4	$10.74 \pm 0.1254$

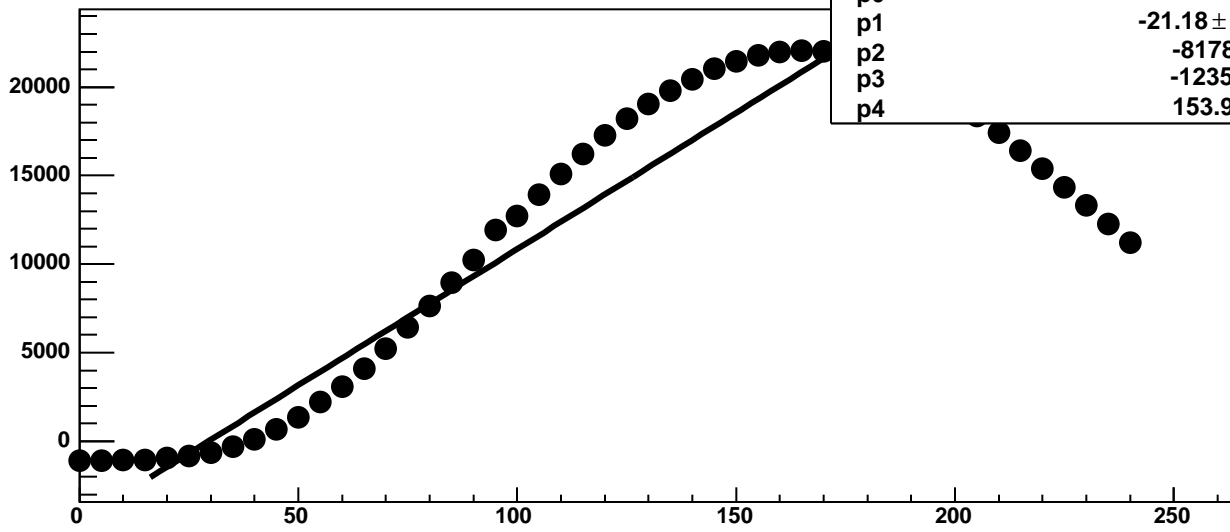
Chip 10, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

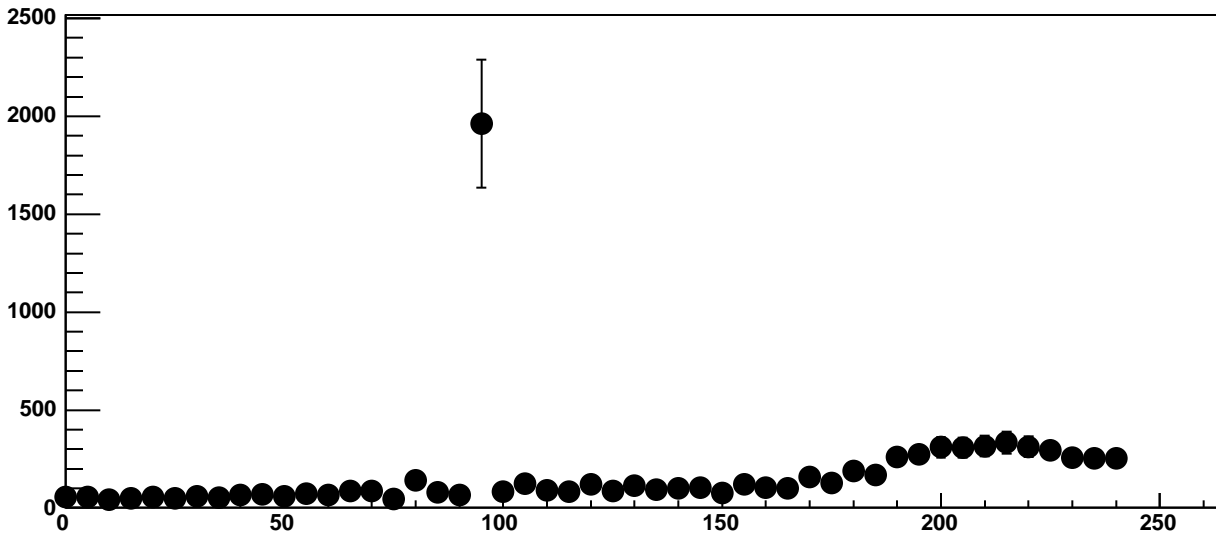


Chip 10, Channel 6, Enable 5, DAC=1600, ADC Mean vs Hold

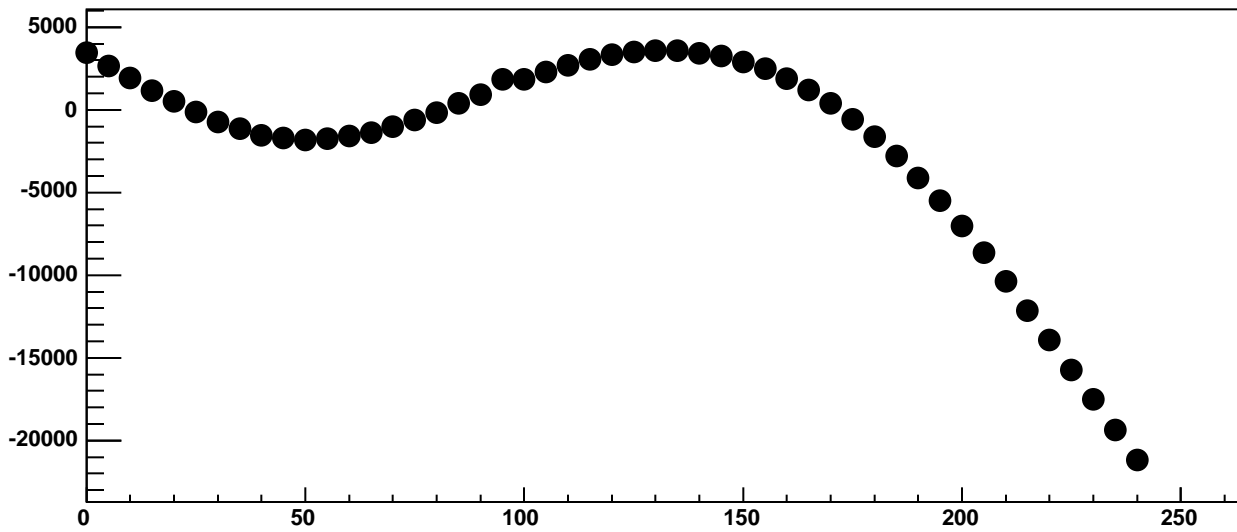


$\chi^2 / \text{ndf}$	8.431e+05 / 41
p0	383.5 ± 16.75
p1	-21.18 ± 0.09985
p2	-8178 ± 19.55
p3	-1235 ± 13.45
p4	153.9 ± 0.108

Chip 10, Channel 6, Enable 5, DAC=1600, ADC Noise vs Hold

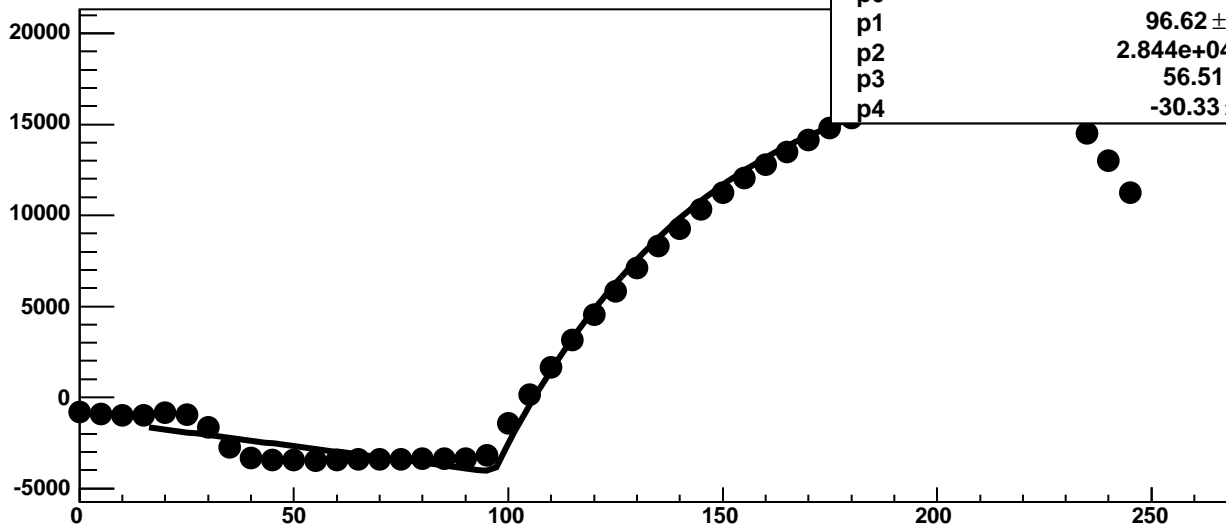


Chip 10, Channel 6, Enable 5, DAC=1600, ADC Residuals vs Hold





Chip 10, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

6.888e+04 / 41

p0

-4094 ± 8.771

p1

96.62 ± 0.05558

p2

2.844e+04 ± 51.98

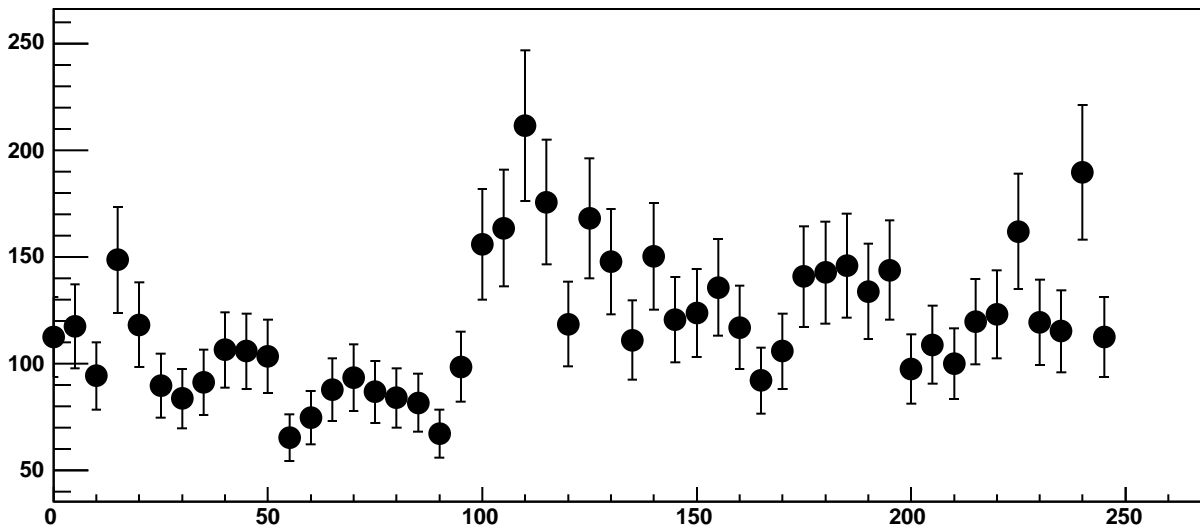
p3

56.51 ± 0.1617

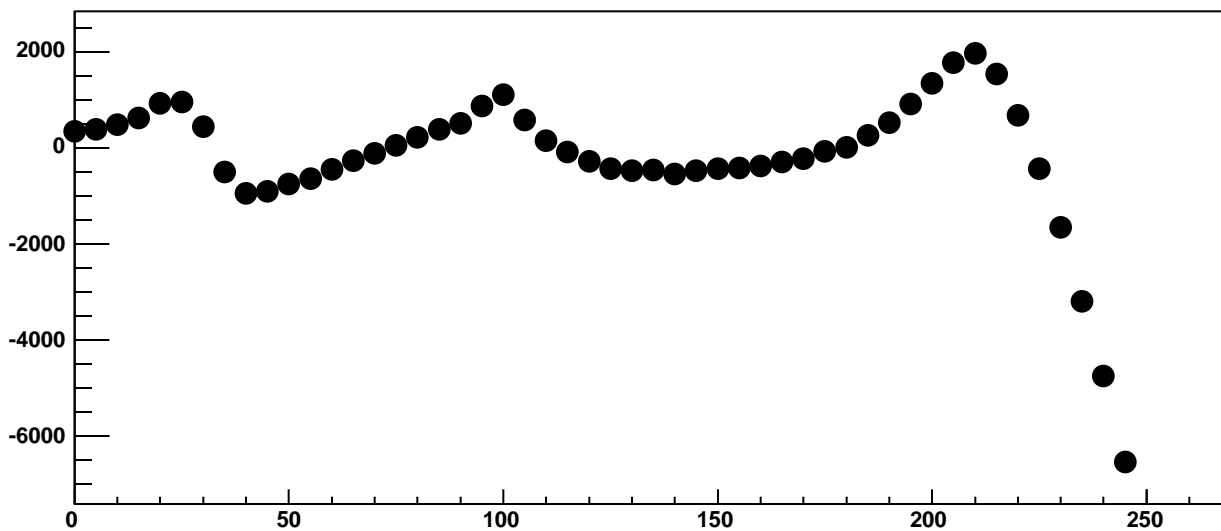
p4

-30.33 ± 0.2096

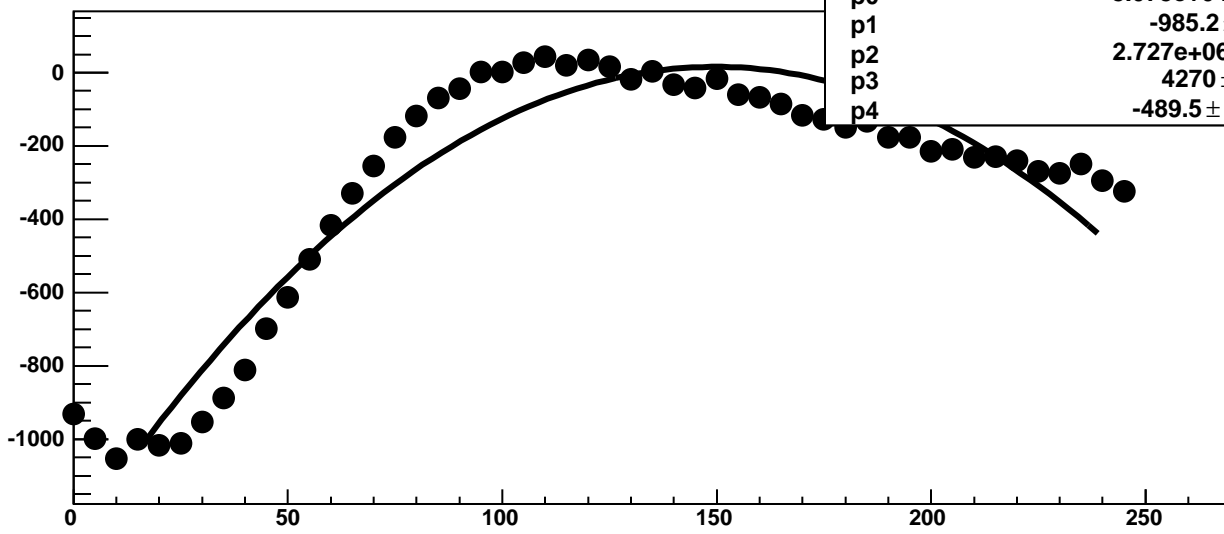
Chip 10, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

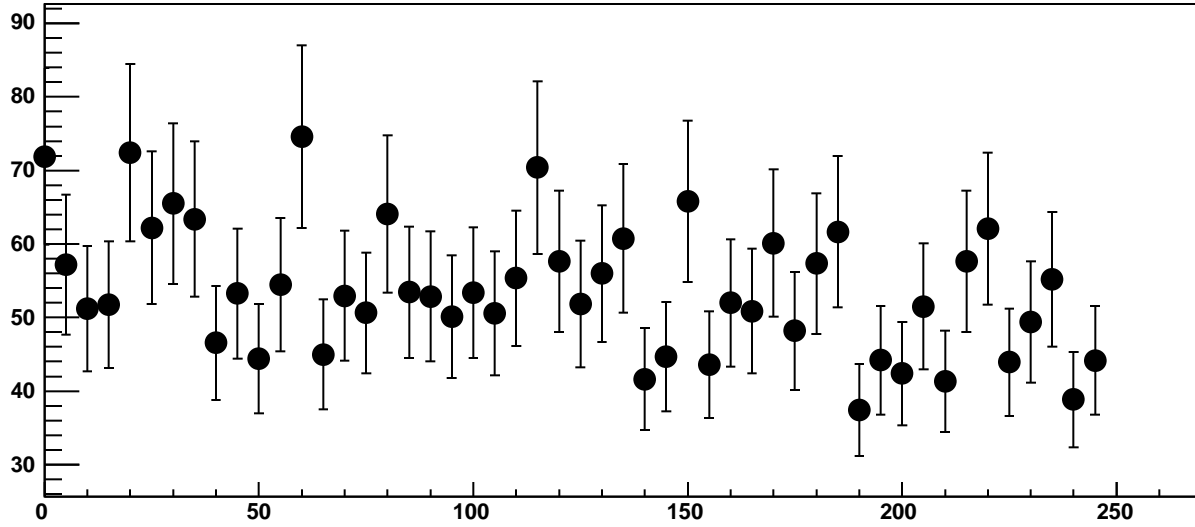


Chip 10, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

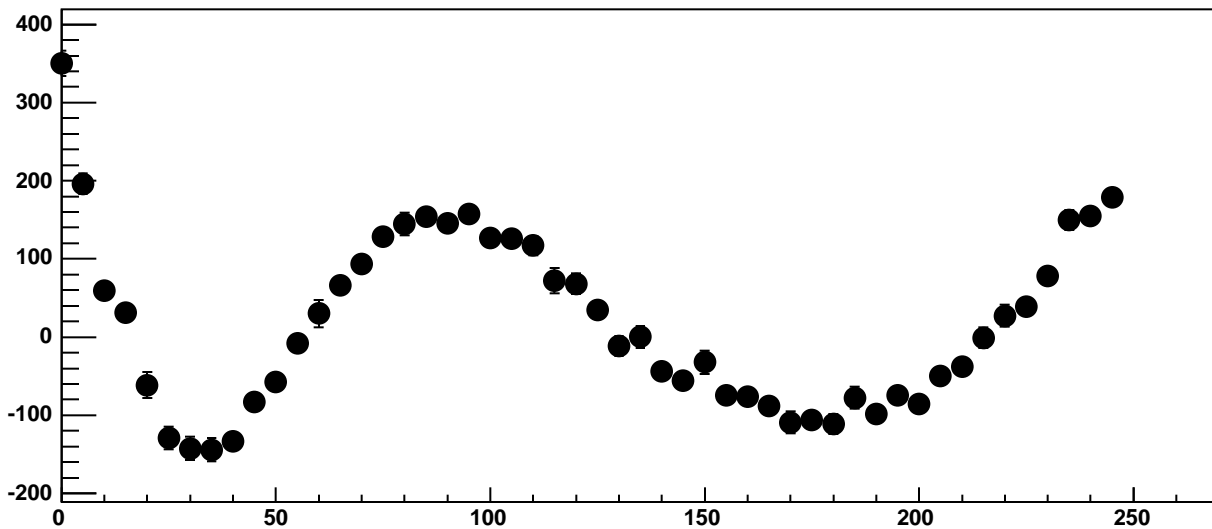


$\chi^2 / \text{ndf}$	2979 / 41
p0	$-8.078\text{e}+04 \pm 23.75$
p1	$-985.2 \pm 0.2781$
p2	$2.727\text{e}+06 \pm 102.6$
p3	$4270 \pm 0.1839$
p4	$-489.5 \pm 0.02109$

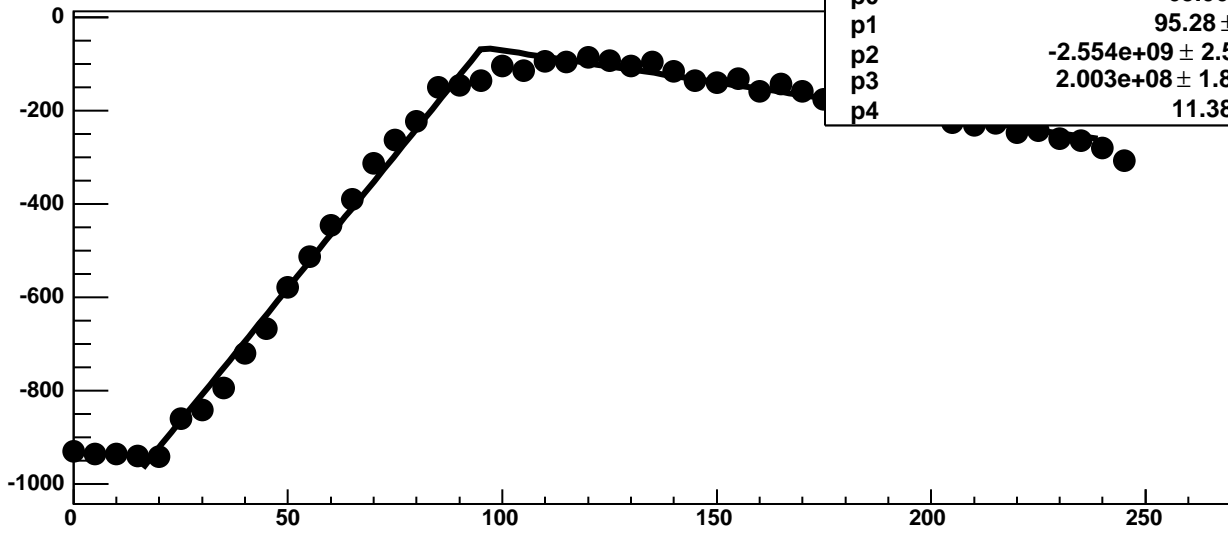
Chip 10, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold

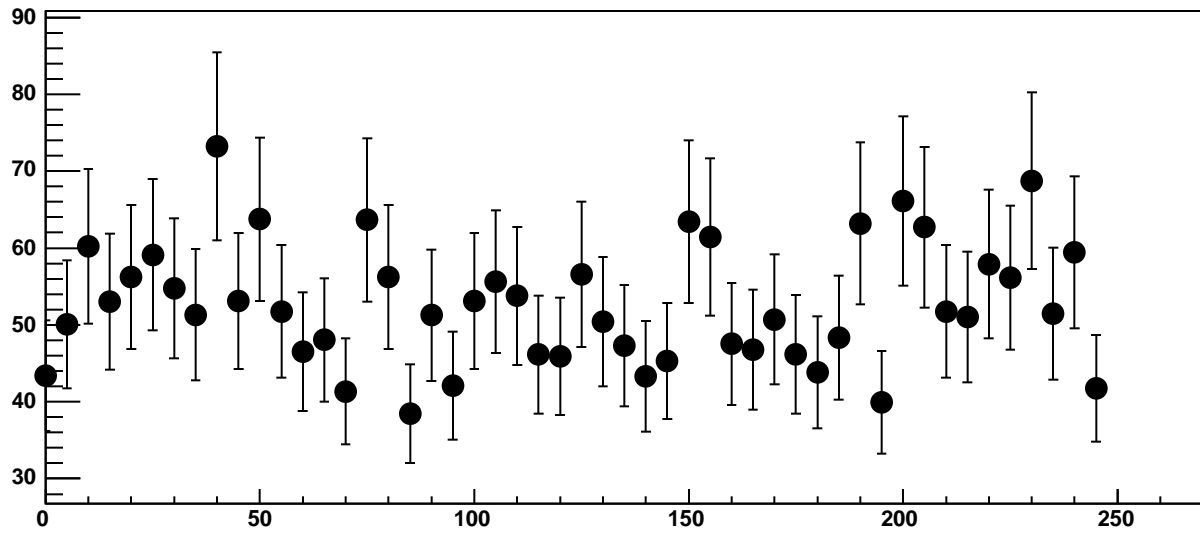


Chip 10, Channel 7, Enable 2, DAC=1600, ADC Mean vs Hold

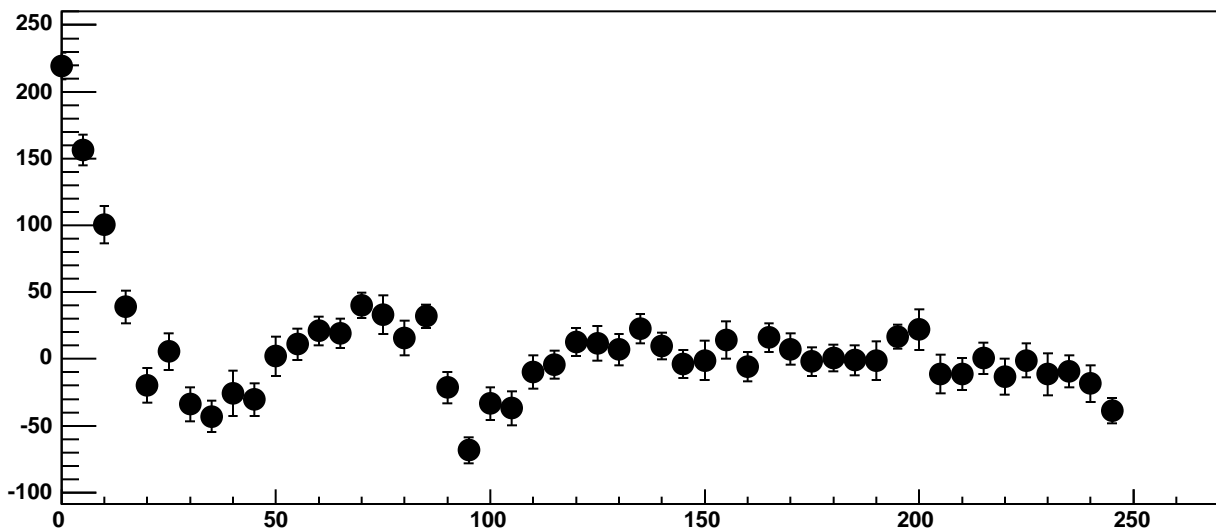


$\chi^2 / \text{ndf}$	180.5 / 41
p0	$-65.06 \pm 4.039$
p1	$95.28 \pm 0.5297$
p2	$-2.554\text{e}+09 \pm 2.549\text{e}+07$
p3	$2.003\text{e}+08 \pm 1.841\text{e}+05$
p4	$11.38 \pm 0.115$

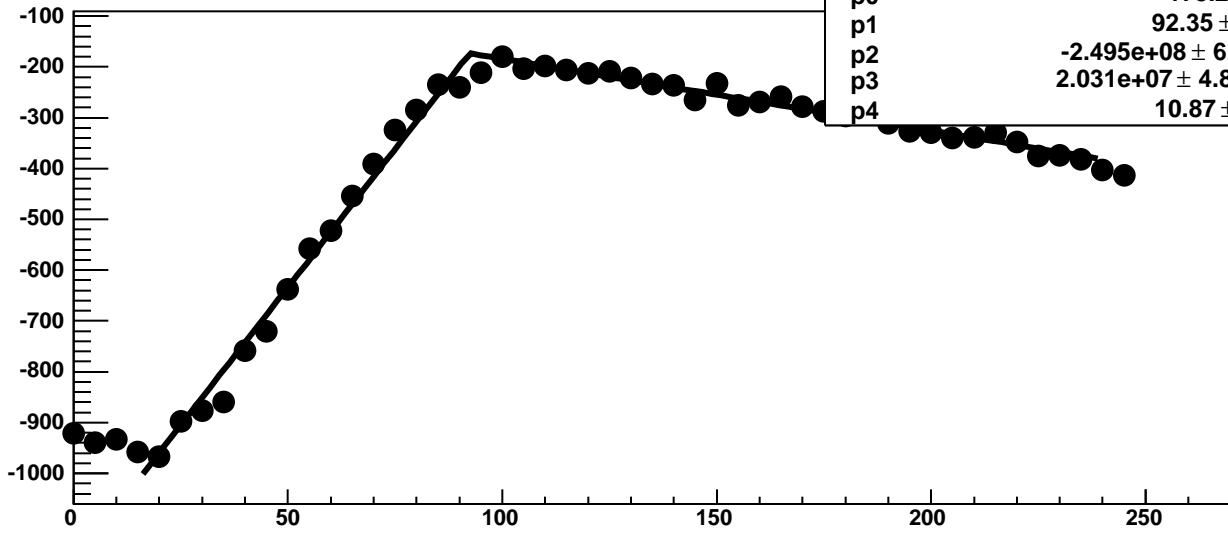
Chip 10, Channel 7, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 7, Enable 2, DAC=1600, ADC Residuals vs Hold

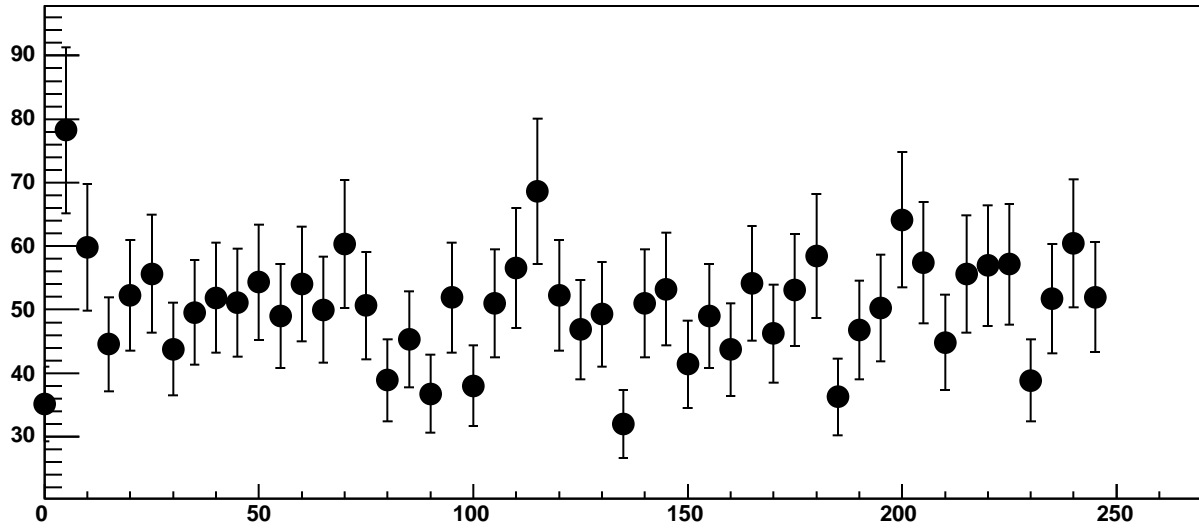


Chip 10, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold

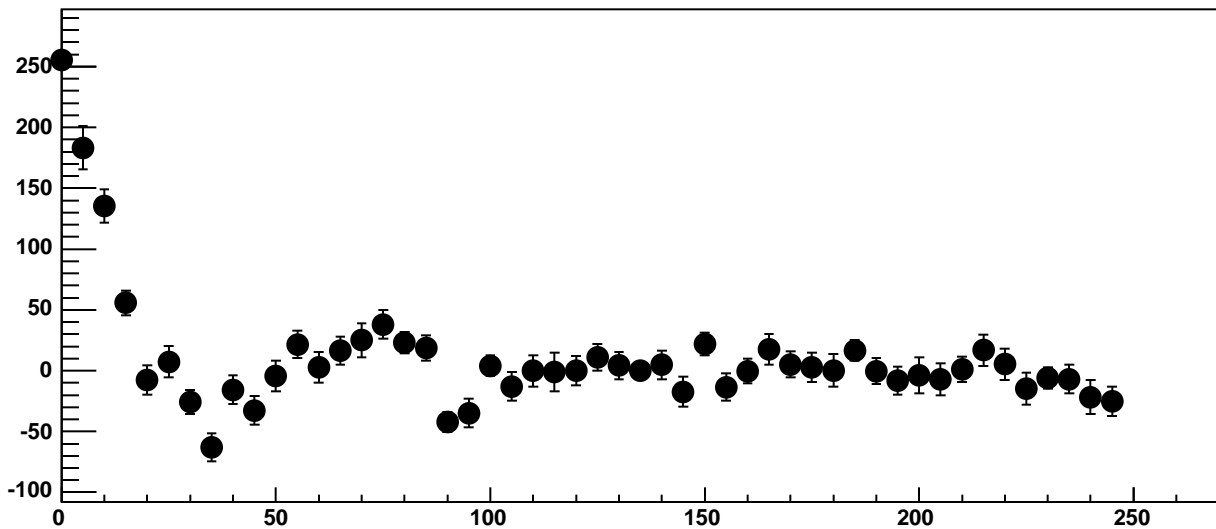


$\chi^2 / \text{ndf}$	165.7 / 41
p0	$-173.2 \pm 3.618$
p1	$92.35 \pm 0.5276$
p2	$-2.495\text{e}+08 \pm 6.78\text{e}+06$
p3	$2.031\text{e}+07 \pm 4.829\text{e}+05$
p4	$10.87 \pm 0.1147$

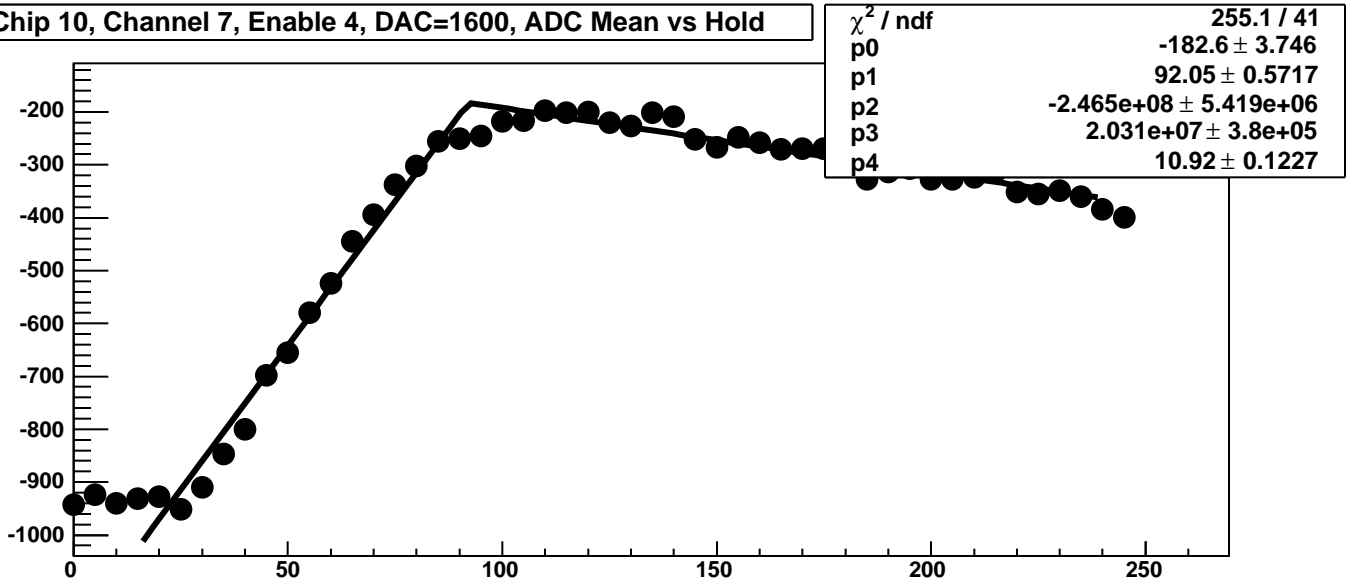
Chip 10, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold



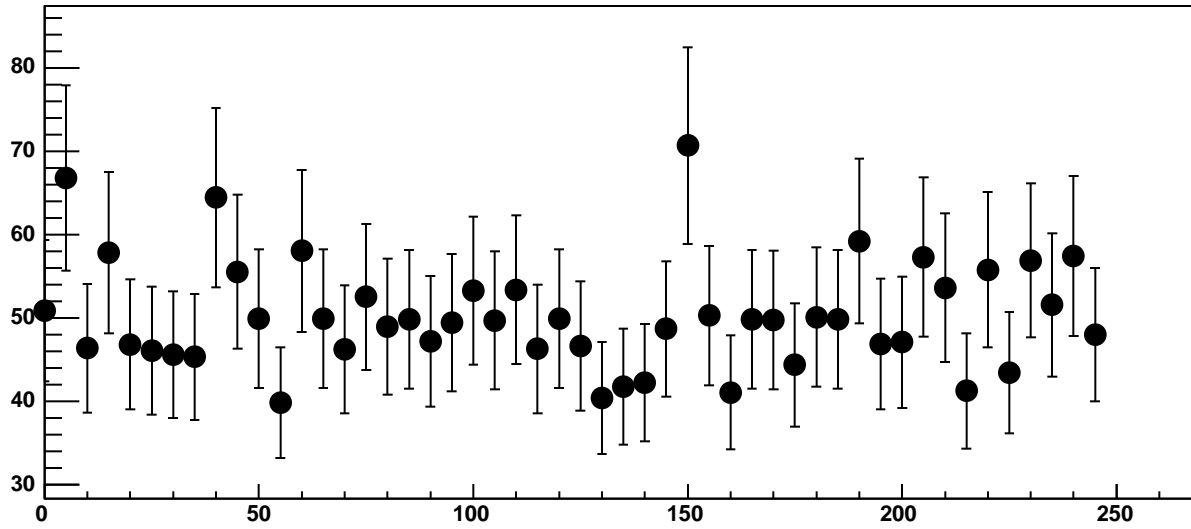
Chip 10, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold



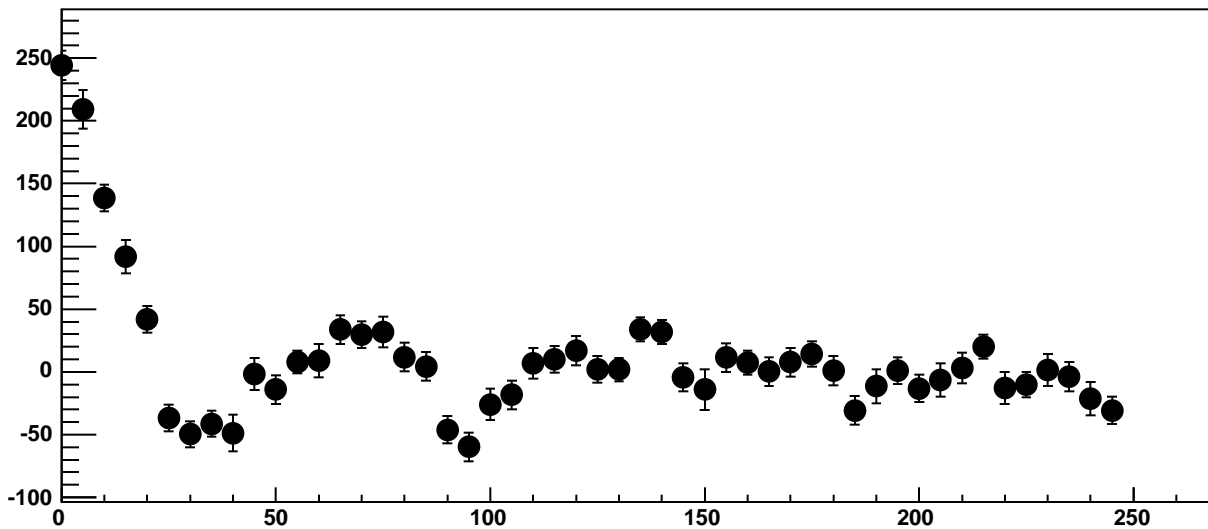
Chip 10, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold



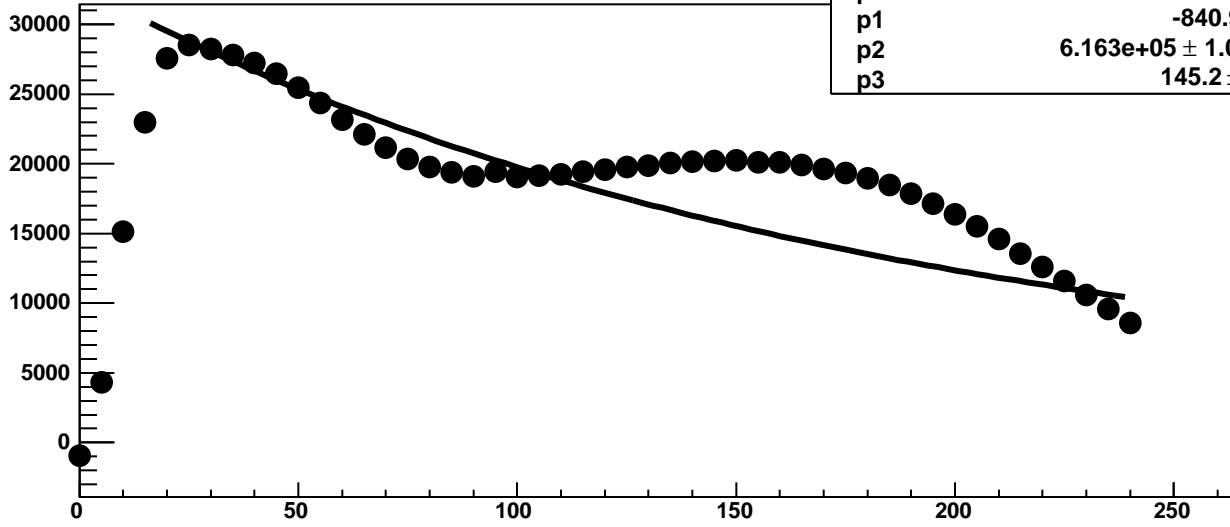
Chip 10, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold

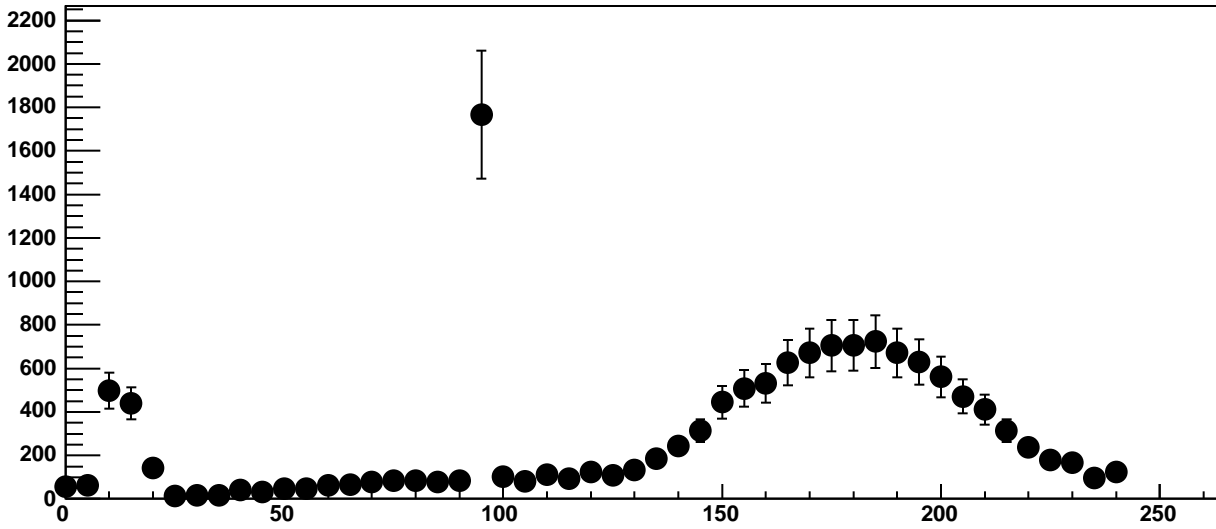


Chip 10, Channel 7, Enable 5!, DAC=1600, ADC Mean vs Hold

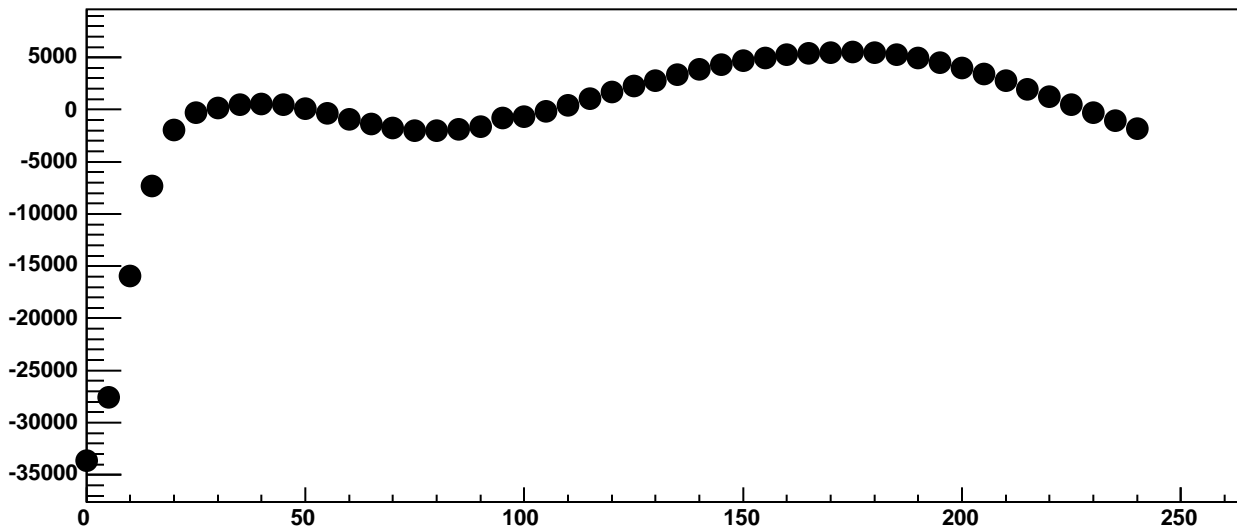


$\chi^2 / \text{ndf}$	1.724e+05 / 42
p0	3123 ± 59.21
p1	-840.9 ± 4.45
p2	6.163e+05 ± 1.043e+04
p3	145.2 ± 0.4857

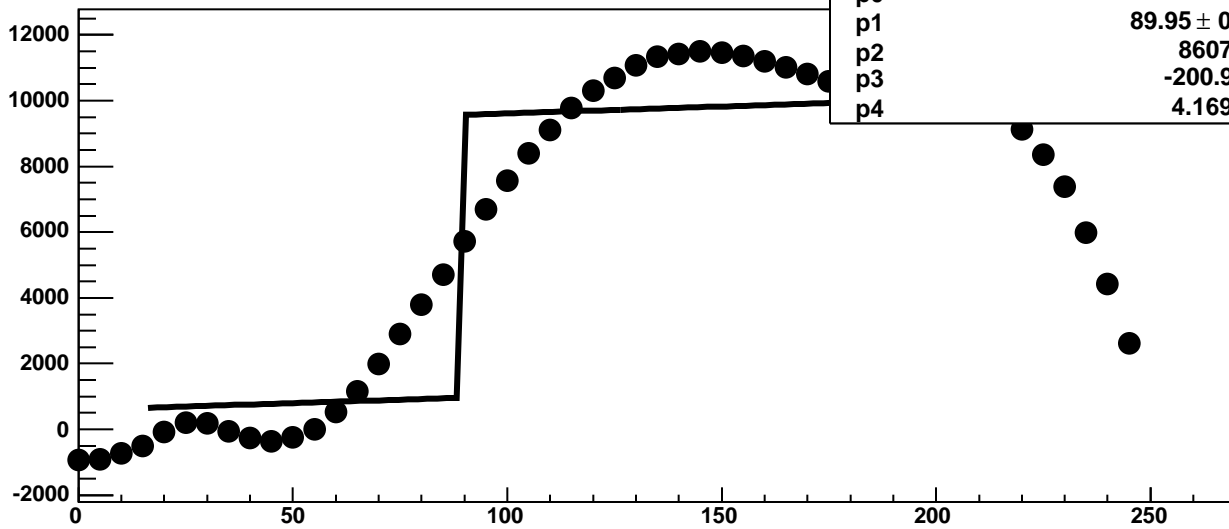
Chip 10, Channel 7, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 7, Enable 5!, DAC=1600, ADC Residuals vs Hold



Chip 10, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

1.806e+05 / 41

p0

966.5 ± 45.08

p1

89.95 ± 0.004883

p2

8607 ± 17.05

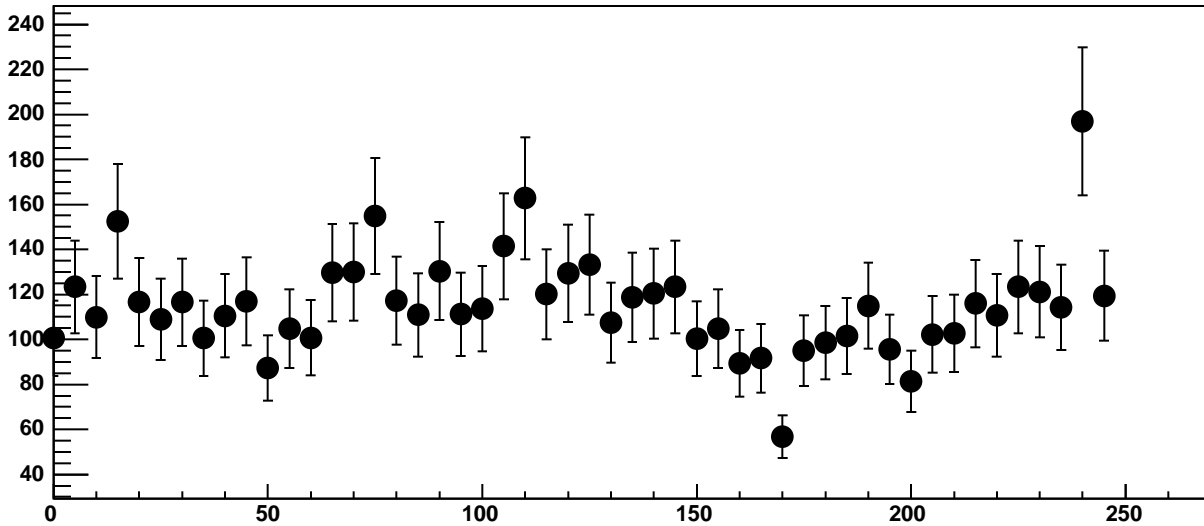
p3

-200.9 ± 4.986

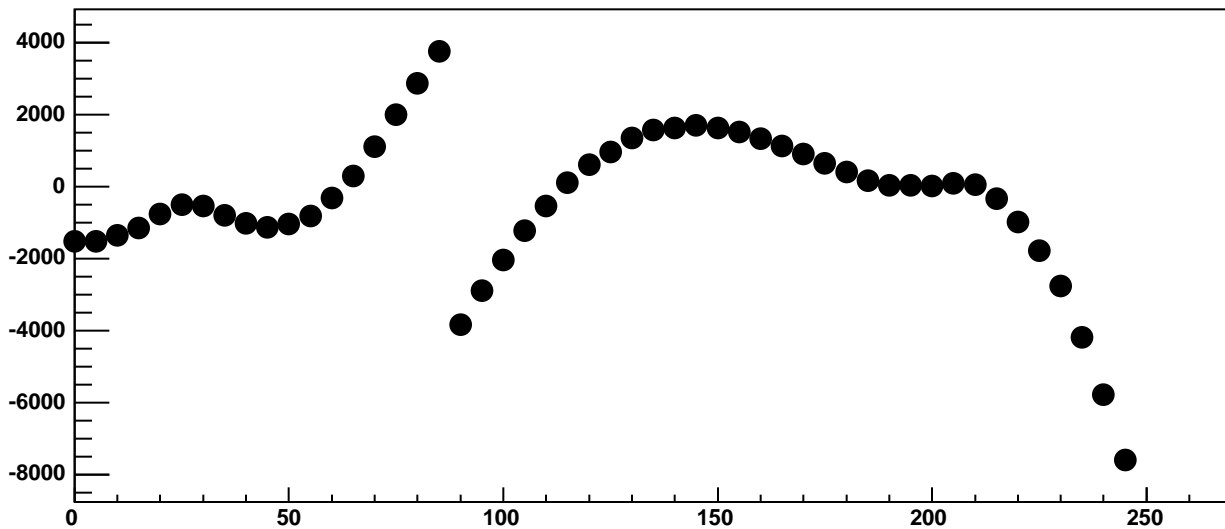
p4

4.169 ± 0.124

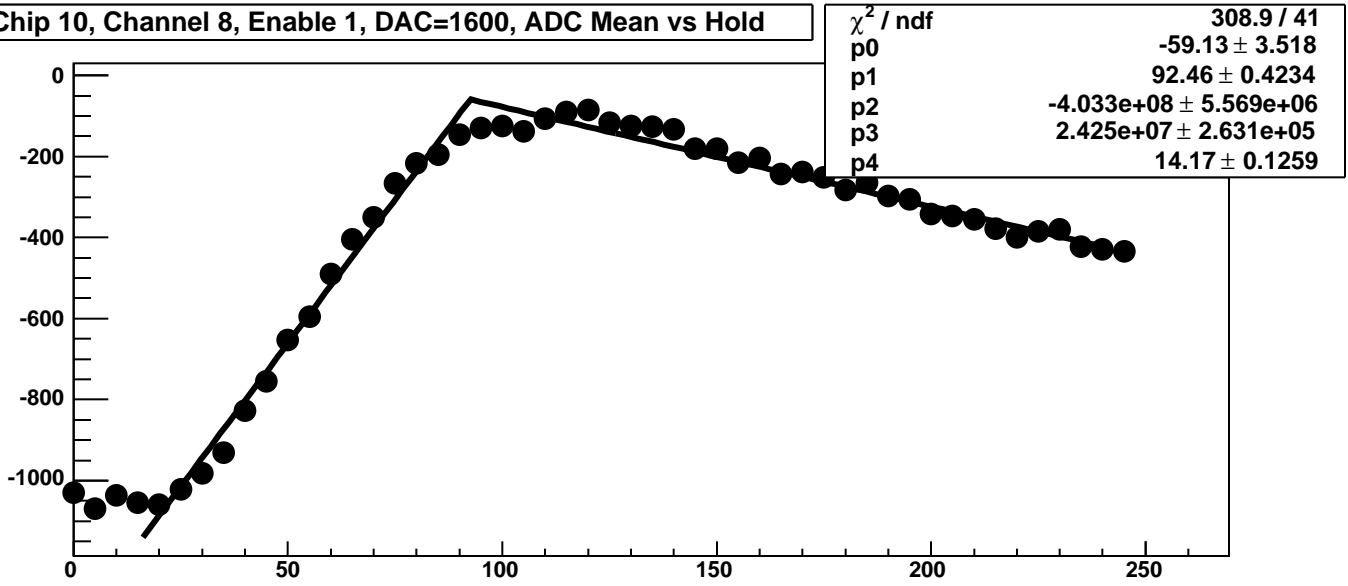
Chip 10, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



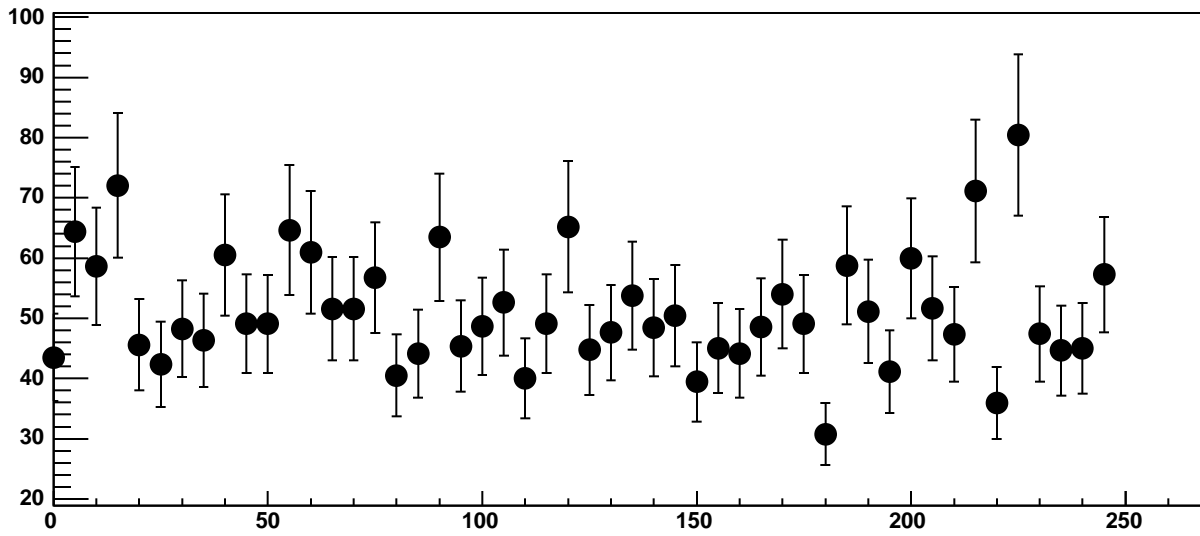
Chip 10, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold



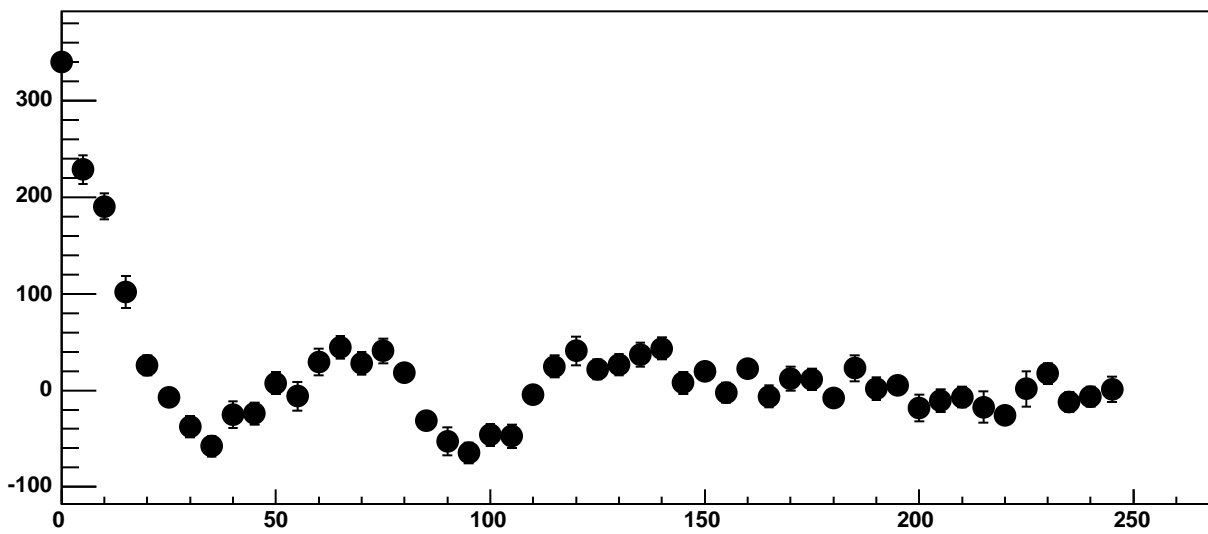
Chip 10, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 10, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold

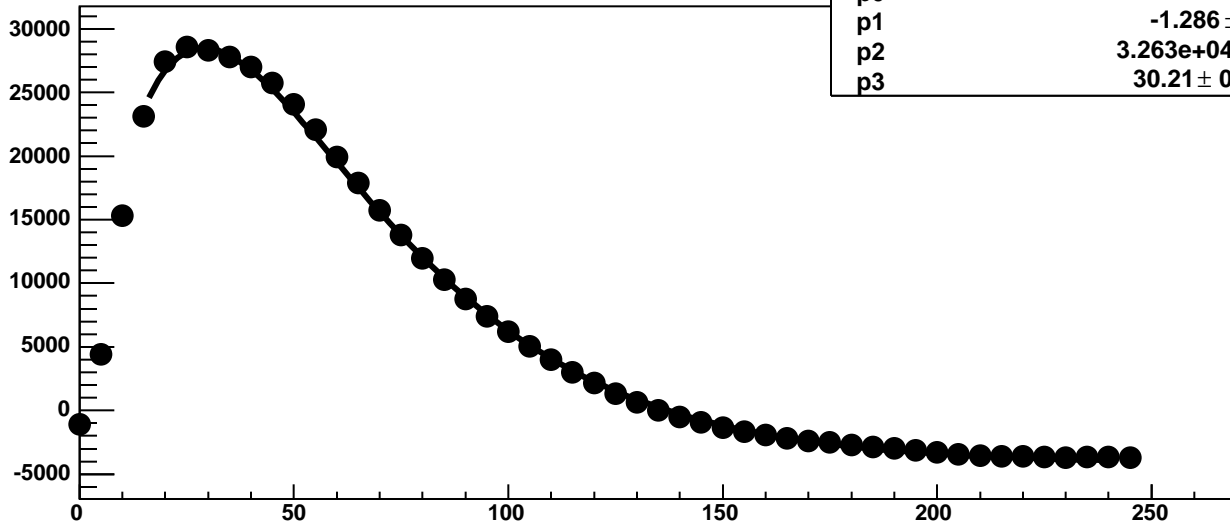


Chip 10, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold



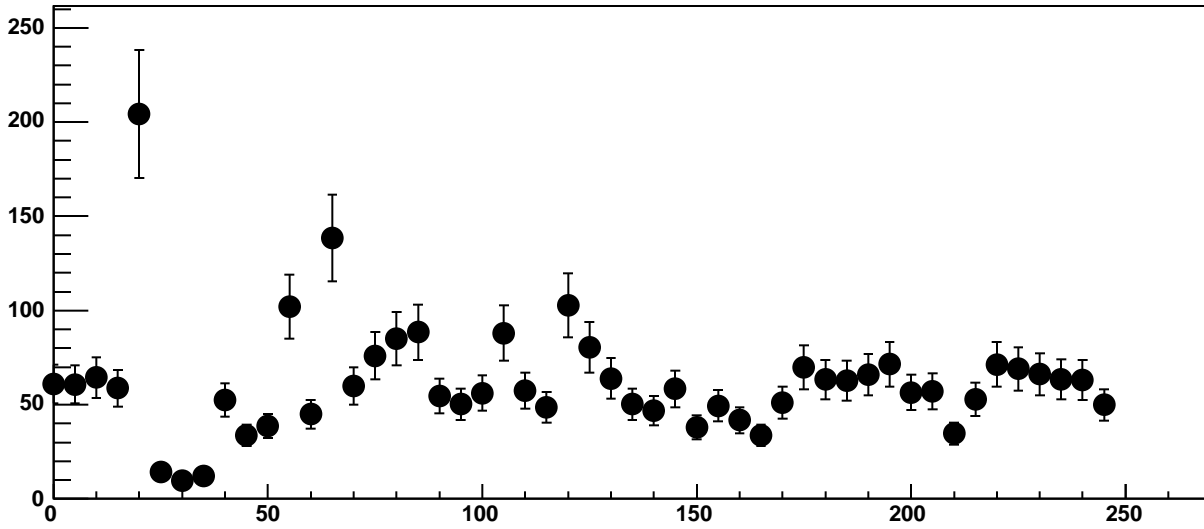


Chip 10, Channel 8, Enable 2!, DAC=1600, ADC Mean vs Hold

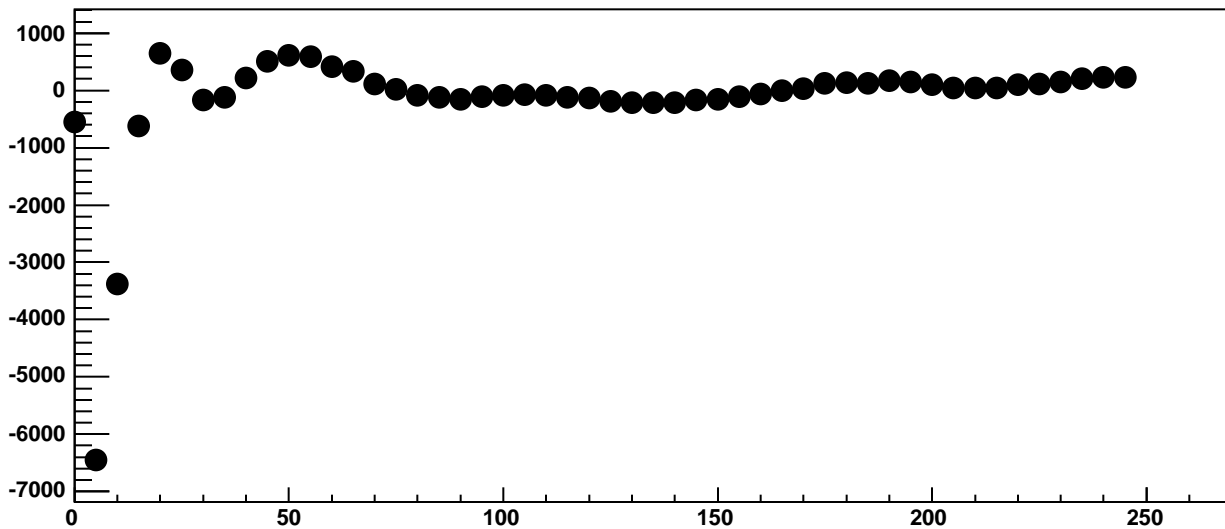


$\chi^2 / \text{ndf}$	3.619e+04 / 42
p0	-4146 ± 3.709
p1	-1.286 ± 0.0156
p2	3.263e+04 ± 3.865
p3	30.21 ± 0.009953

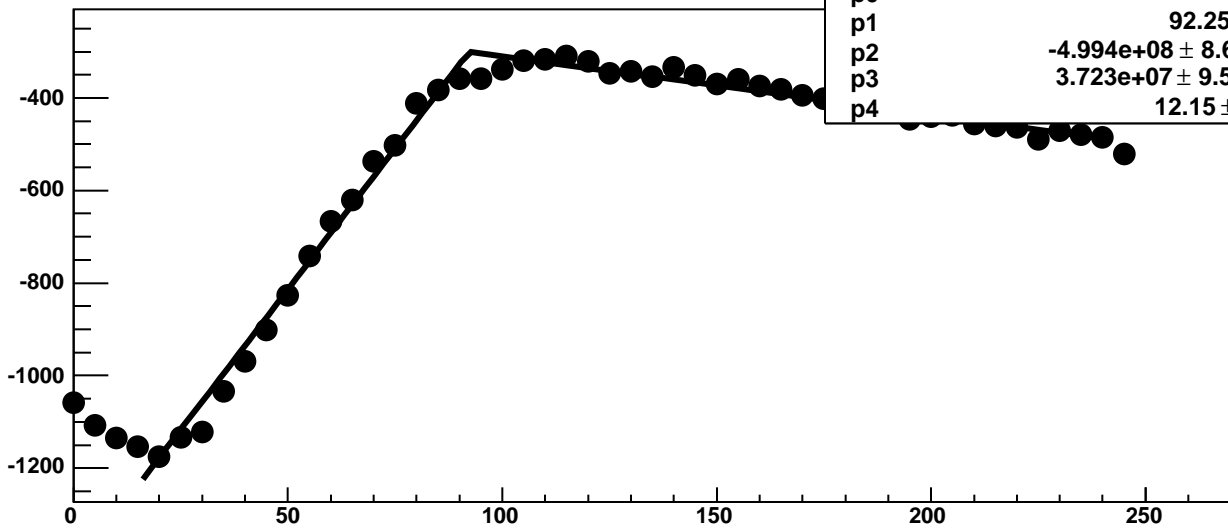
Chip 10, Channel 8, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 8, Enable 2!, DAC=1600, ADC Residuals vs Hold

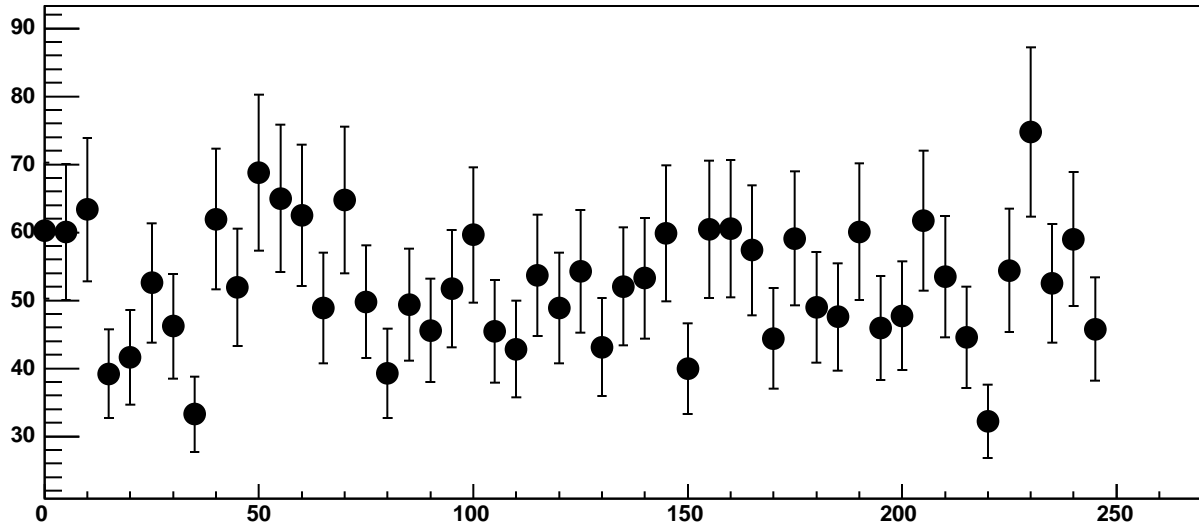


Chip 10, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold

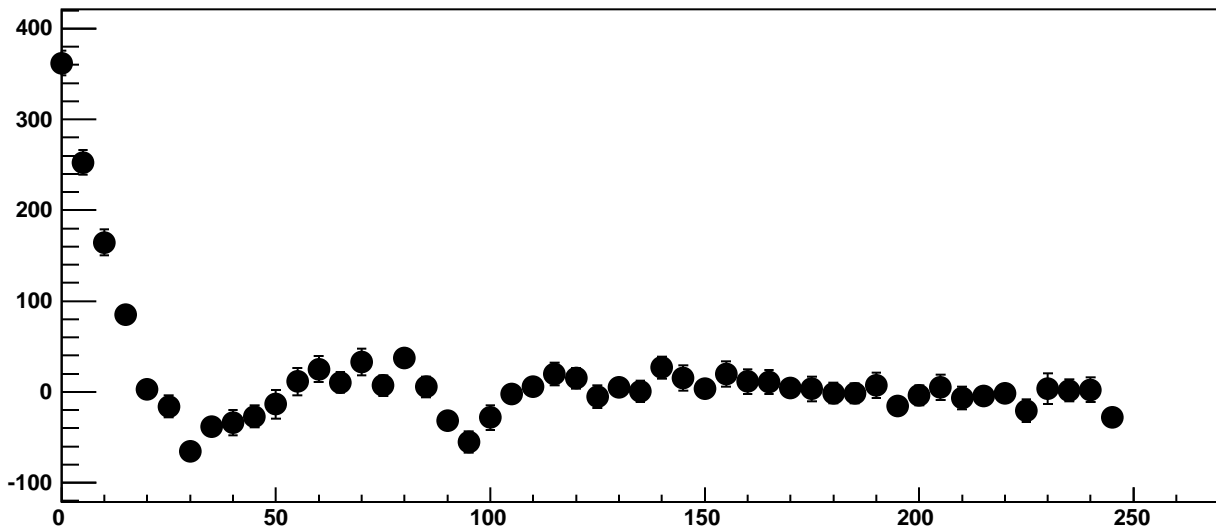


$\chi^2 / \text{ndf}$	249.3 / 41
p0	-300 ± 4.296
p1	92.25 ± 0.401
p2	-4.994e+08 ± 8.689e+06
p3	3.723e+07 ± 9.579e+05
p4	12.15 ± 0.1073

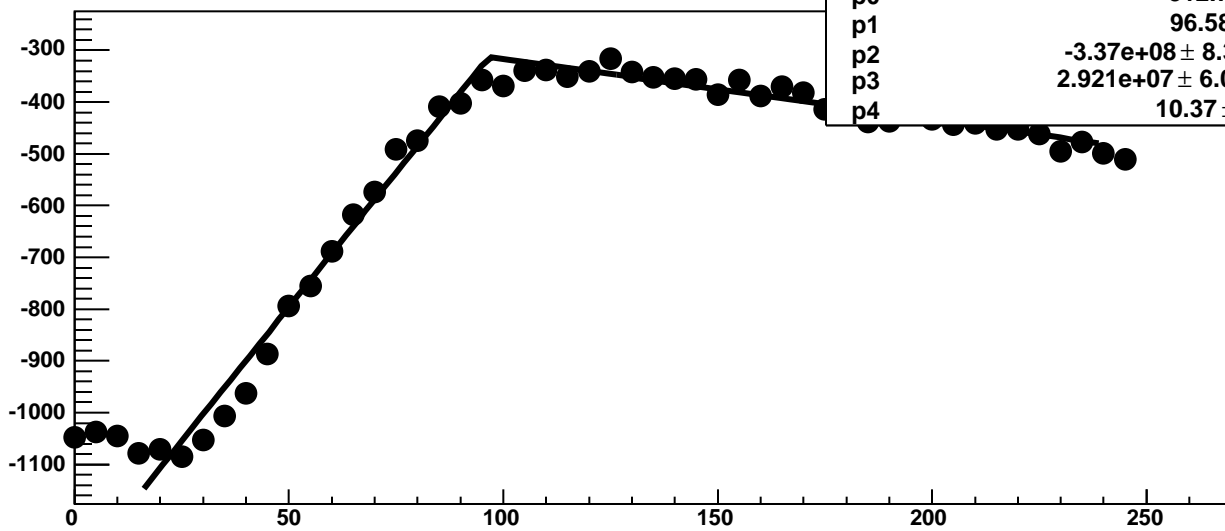
Chip 10, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold

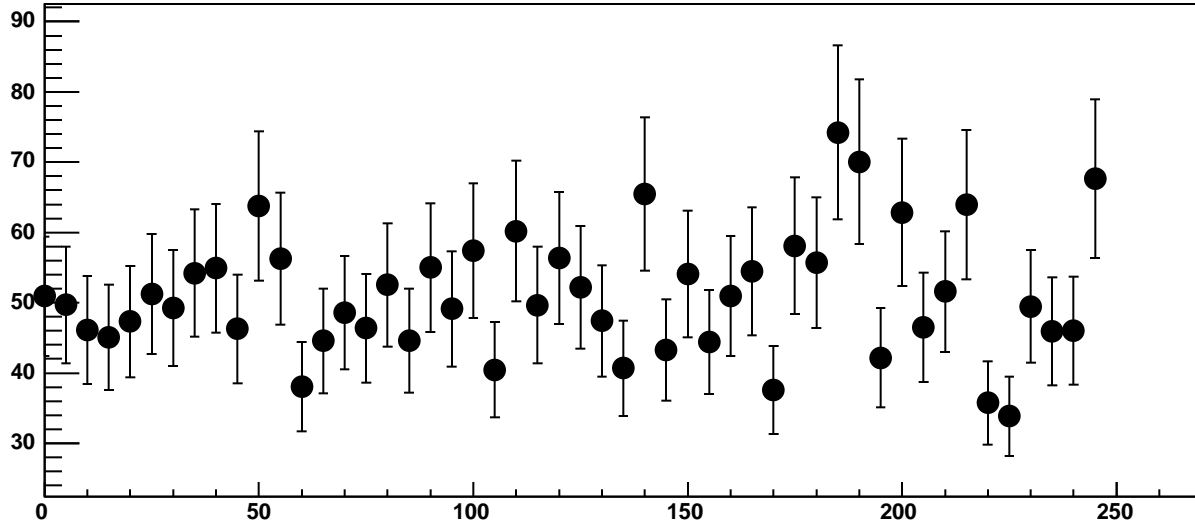


Chip 10, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold

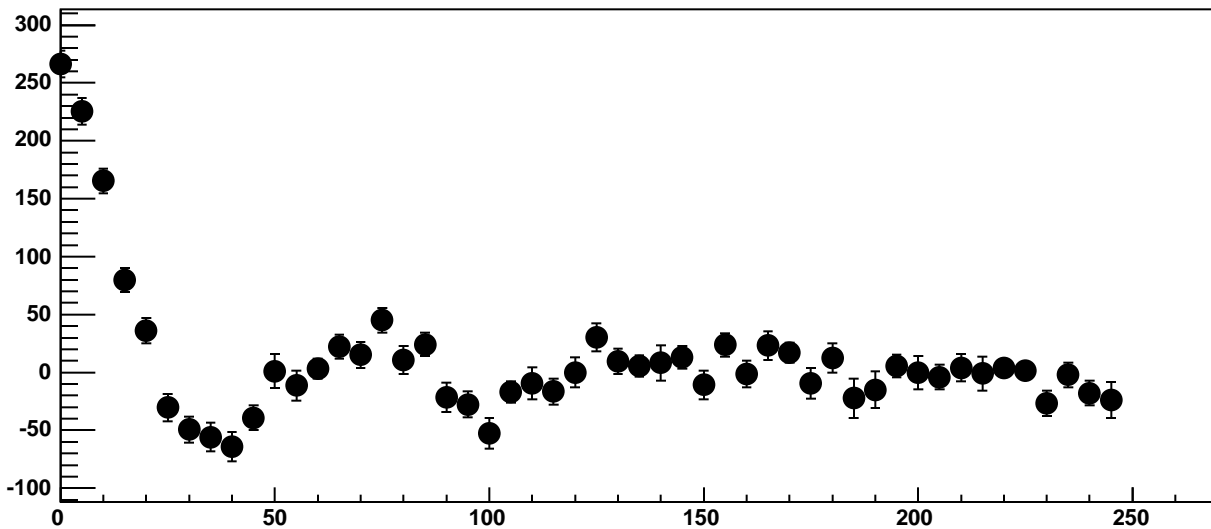


$\chi^2 / \text{ndf}$	255 / 41
p0	$-312.7 \pm 3.838$
p1	$96.58 \pm 0.581$
p2	$-3.37\text{e}+08 \pm 8.369\text{e}+06$
p3	$2.921\text{e}+07 \pm 6.093\text{e}+05$
p4	$10.37 \pm 0.1093$

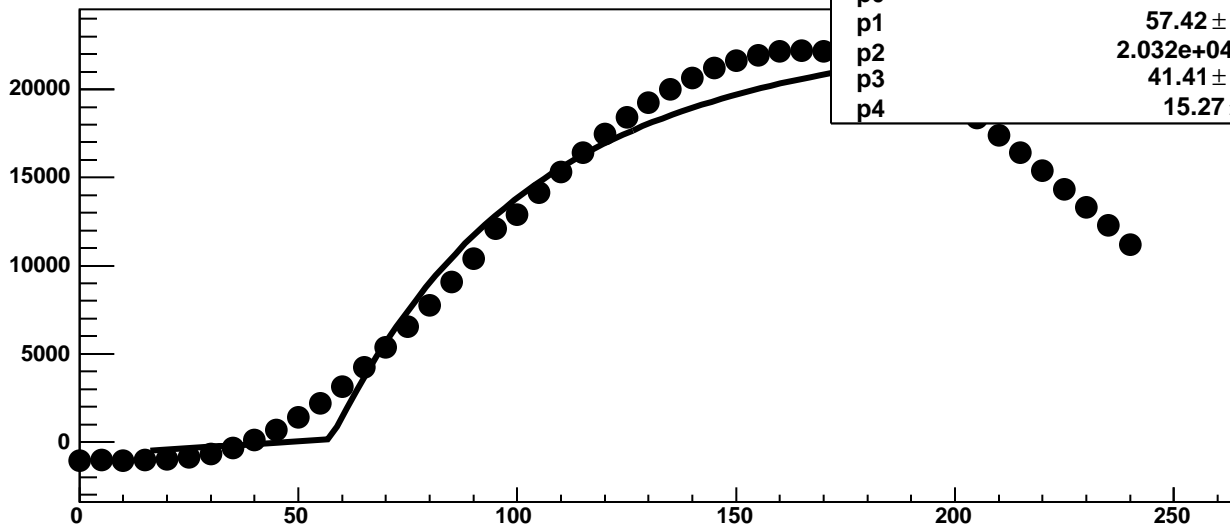
Chip 10, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

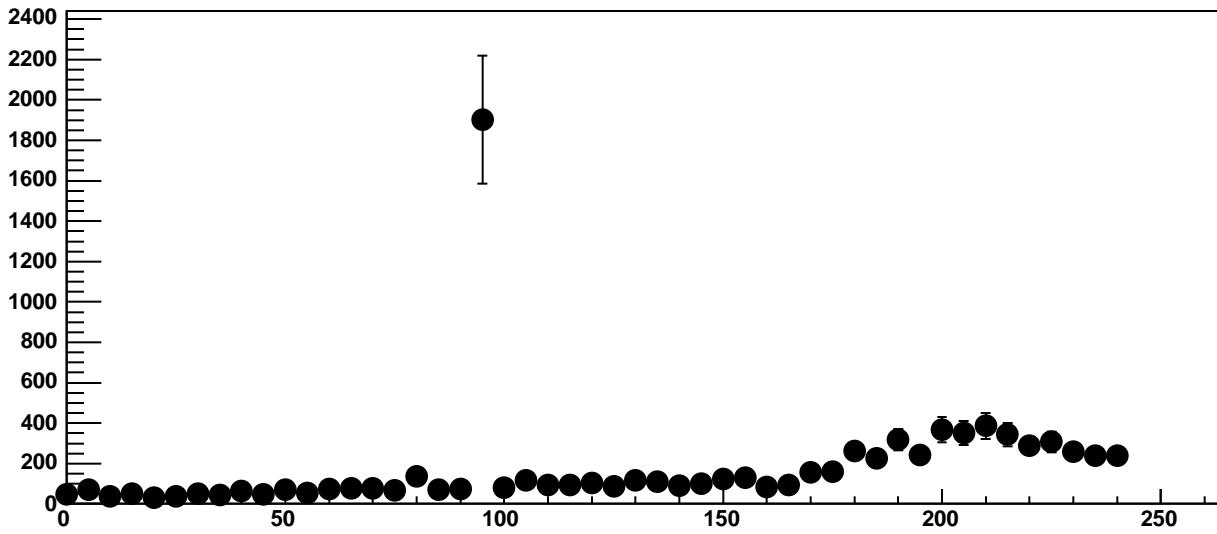


Chip 10, Channel 8, Enable 5, DAC=1600, ADC Mean vs Hold

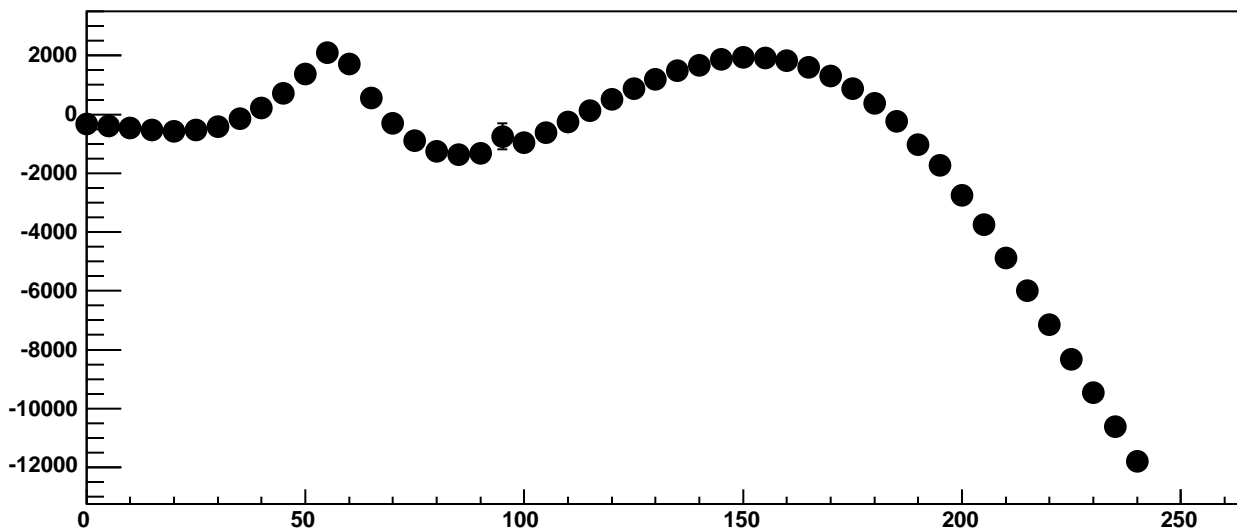


$\chi^2 / \text{ndf}$	2.822e+05 / 41
p0	146.4 ± 7.019
p1	57.42 ± 0.02964
p2	2.032e+04 ± 38.53
p3	41.41 ± 0.08953
p4	15.27 ± 0.2221

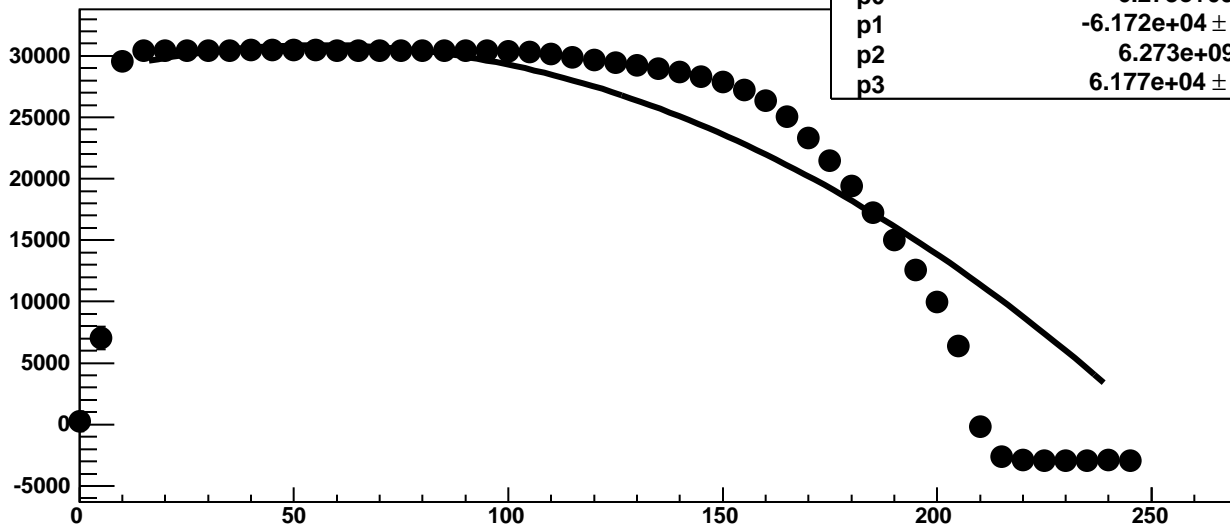
Chip 10, Channel 8, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 8, Enable 5, DAC=1600, ADC Residuals vs Hold

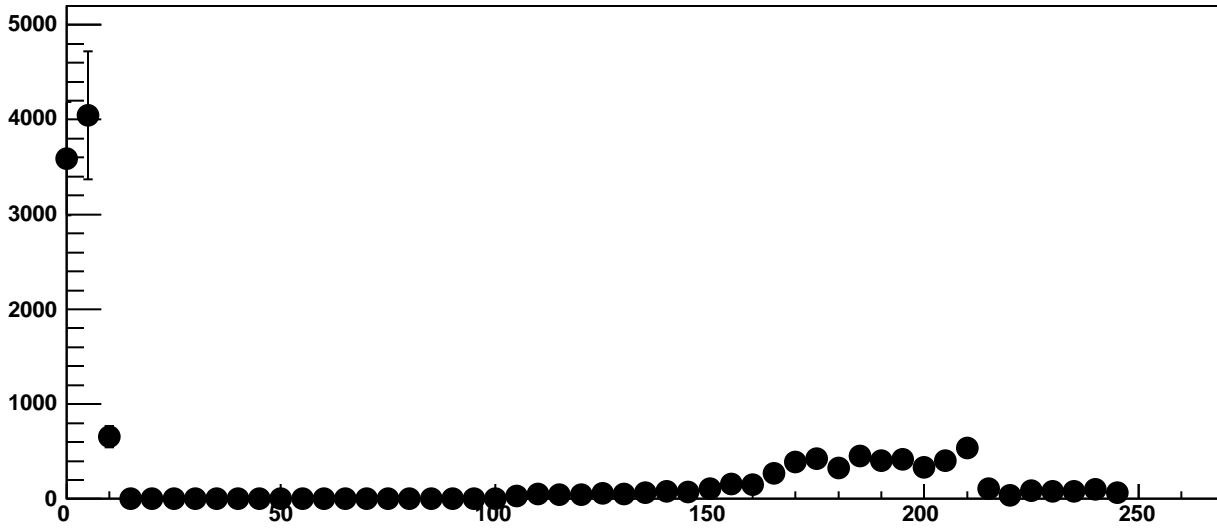


Chip 10, Channel 9, Enable 0!, DAC=1600, ADC Mean vs Hold

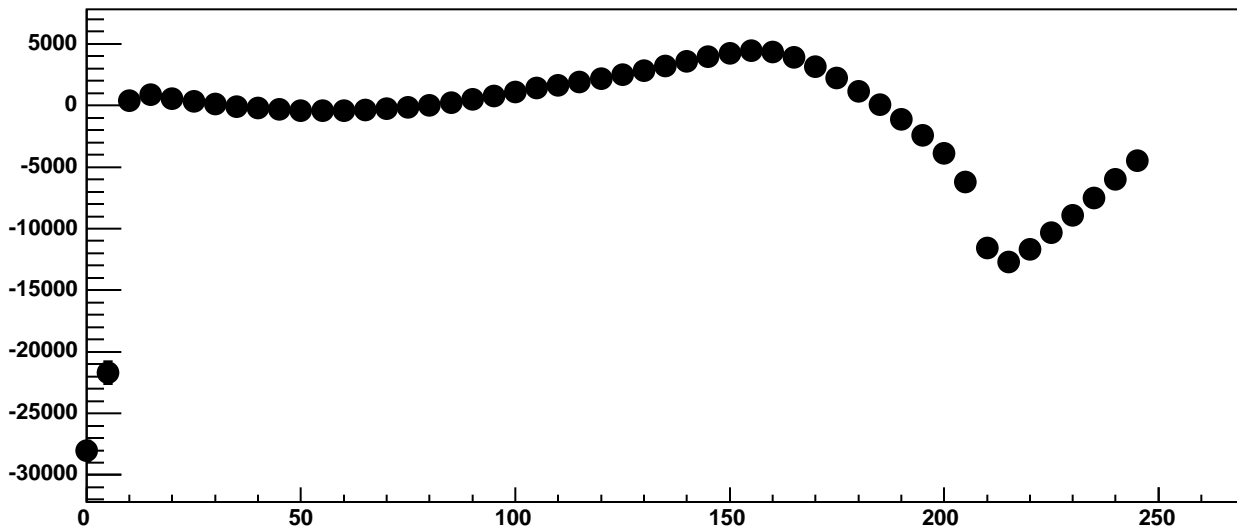


$\chi^2 / \text{ndf}$	8.578e+06 / 42
p0	-6.273e+09 ± 2.618
p1	-6.172e+04 ± 0.05664
p2	6.273e+09 ± 2.618
p3	6.177e+04 ± 0.05663

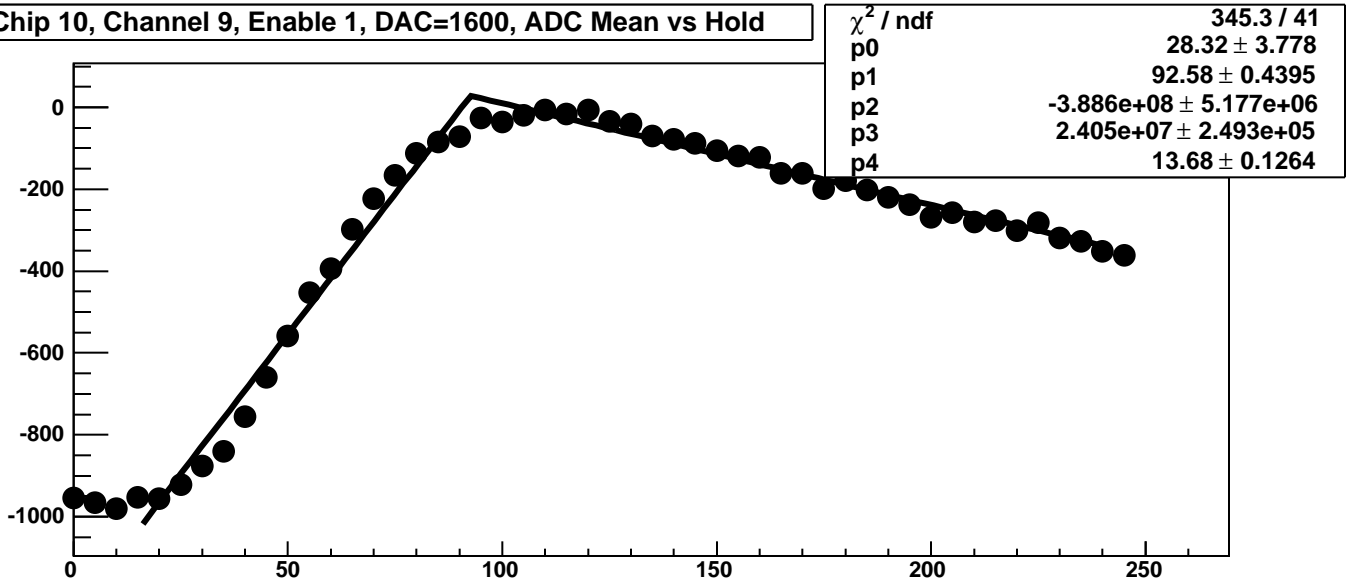
Chip 10, Channel 9, Enable 0!, DAC=1600, ADC Noise vs Hold



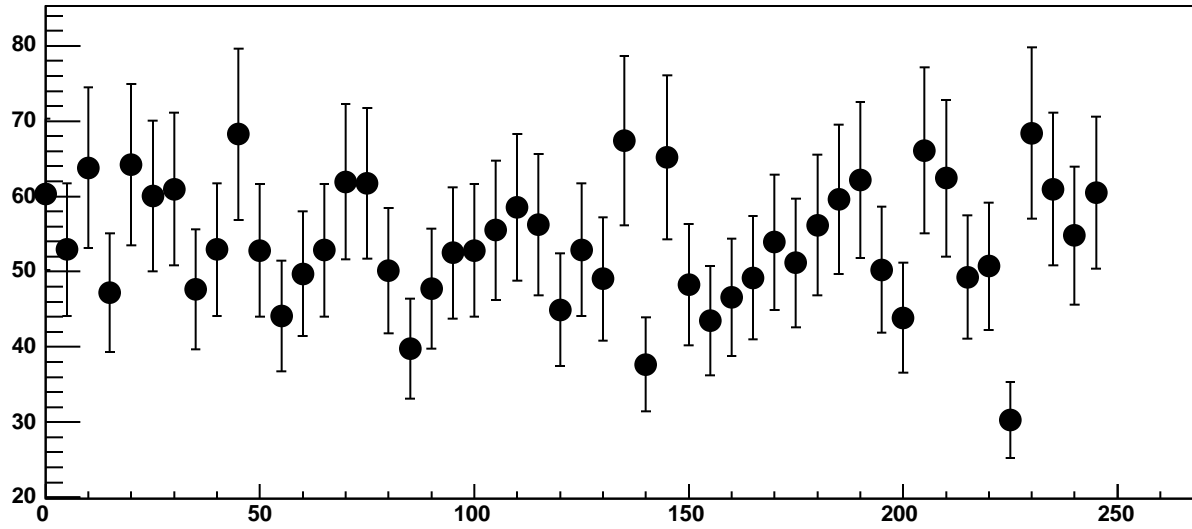
Chip 10, Channel 9, Enable 0!, DAC=1600, ADC Residuals vs Hold



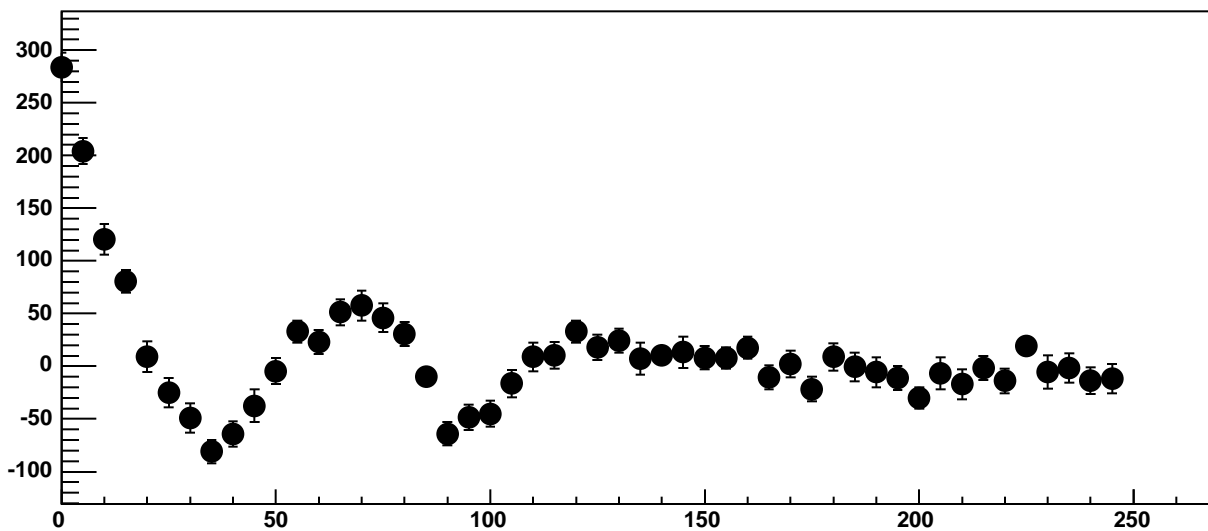
Chip 10, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold



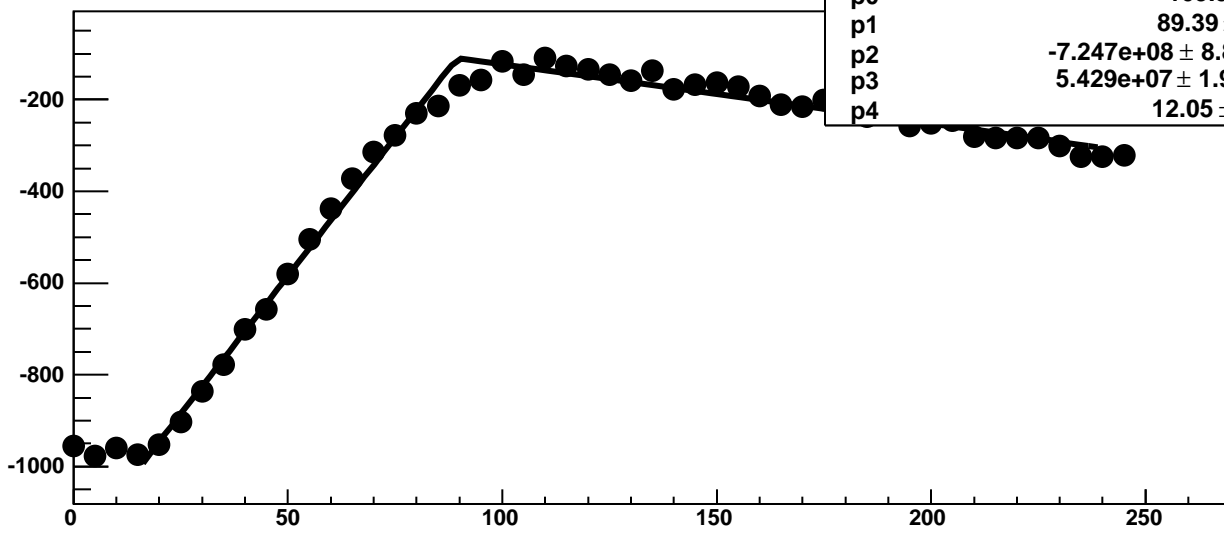
Chip 10, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

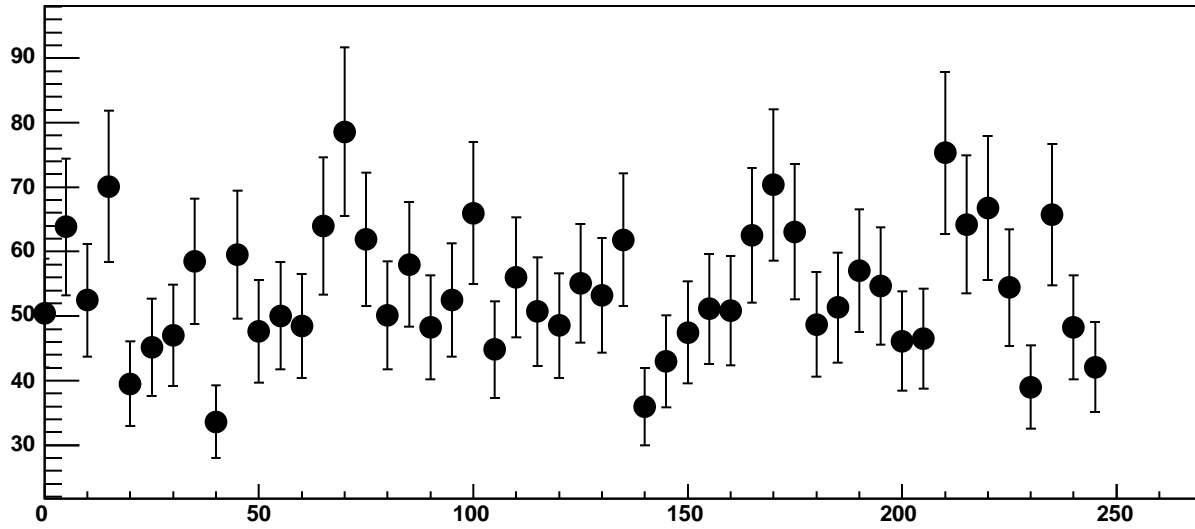


Chip 10, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

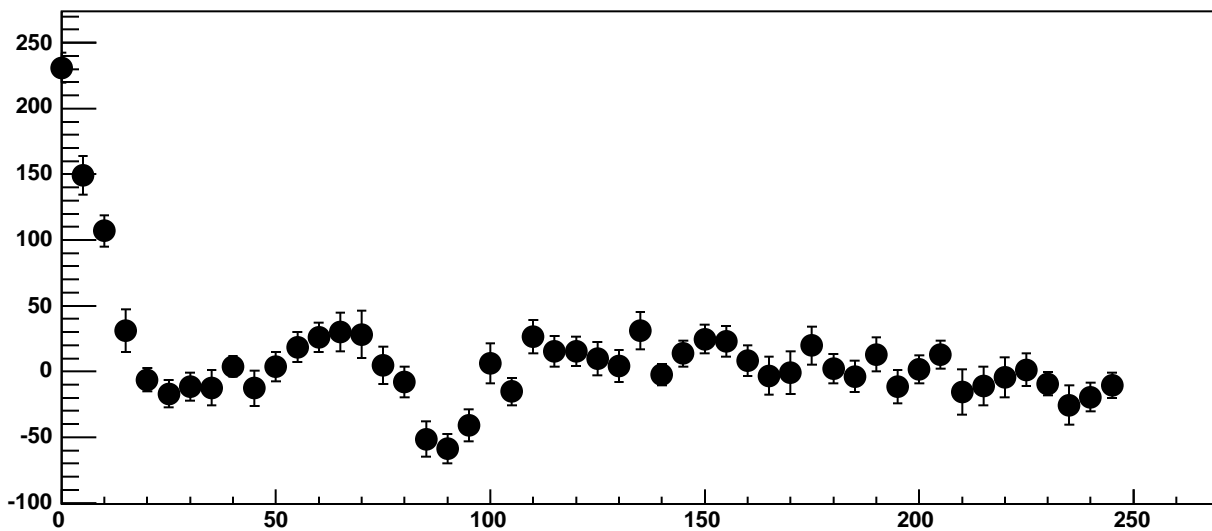


$\chi^2 / \text{ndf}$	121.1 / 41
p0	-109.5 ± 3.788
p1	89.39 ± 0.6071
p2	-7.247e+08 ± 8.852e+06
p3	5.429e+07 ± 1.972e+05
p4	12.05 ± 0.1465

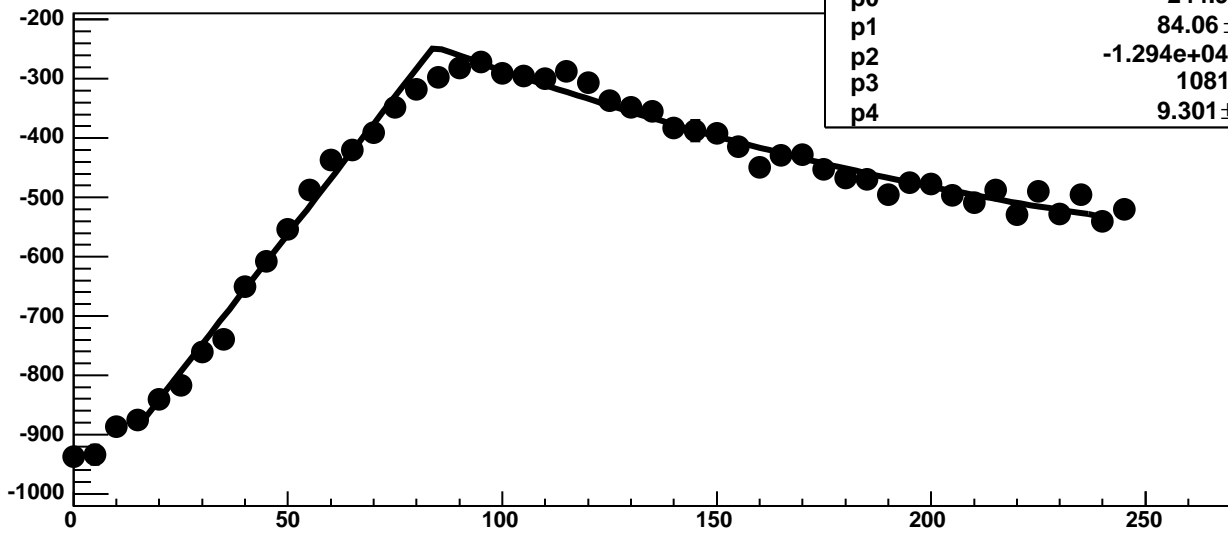
Chip 10, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



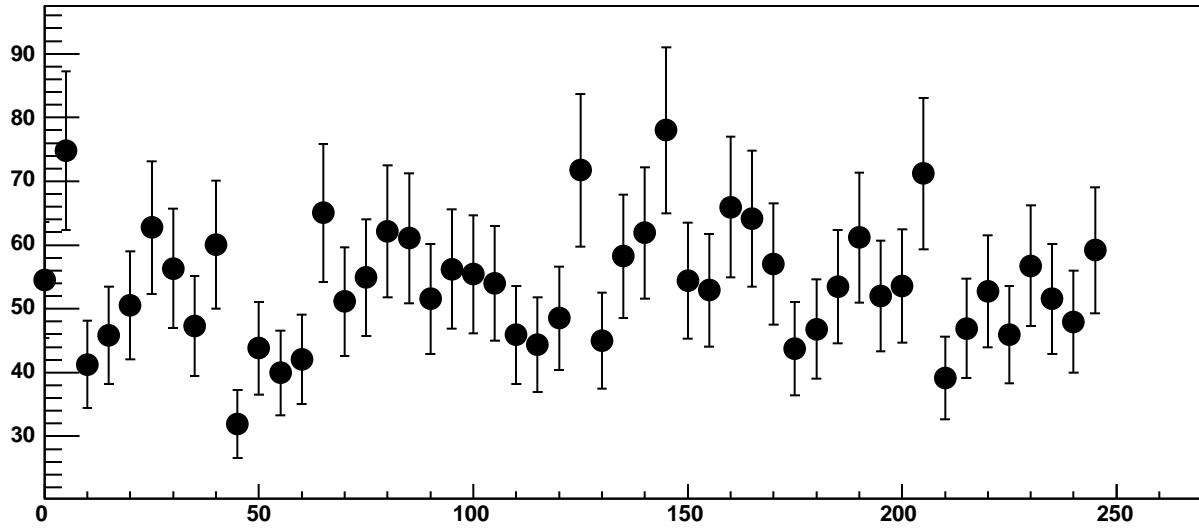
Chip 10, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold



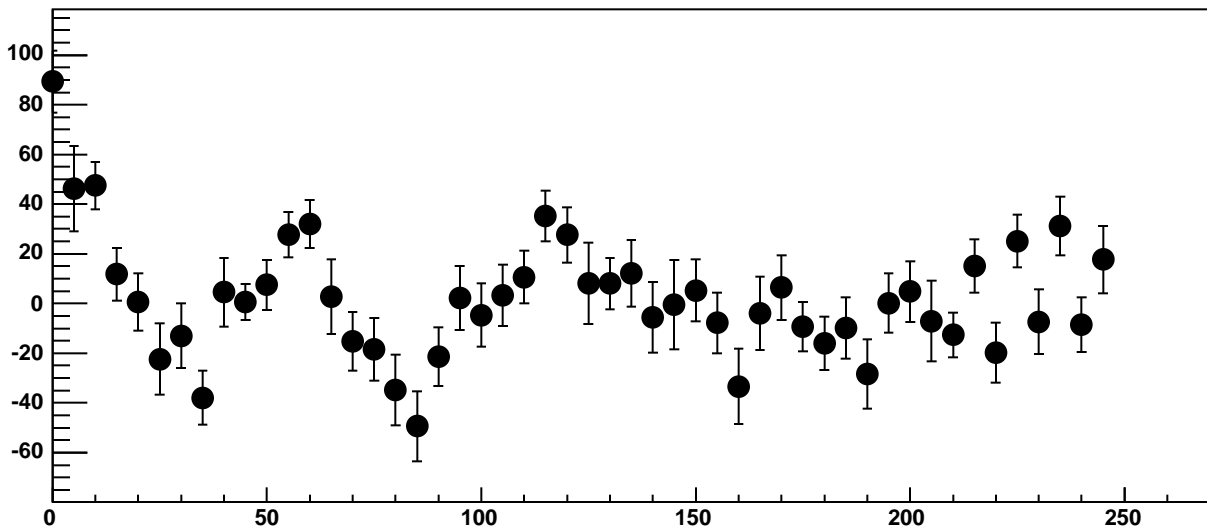
Chip 10, Channel 9, Enable 3, DAC=1600, ADC Mean vs Hold



Chip 10, Channel 9, Enable 3, DAC=1600, ADC Noise vs Hold

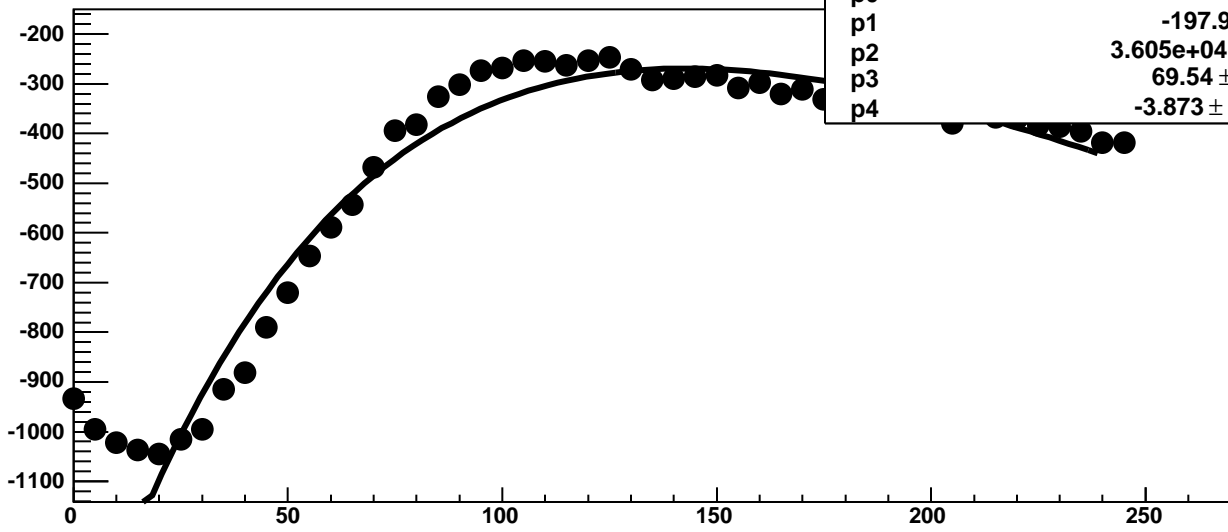


Chip 10, Channel 9, Enable 3, DAC=1600, ADC Residuals vs Hold

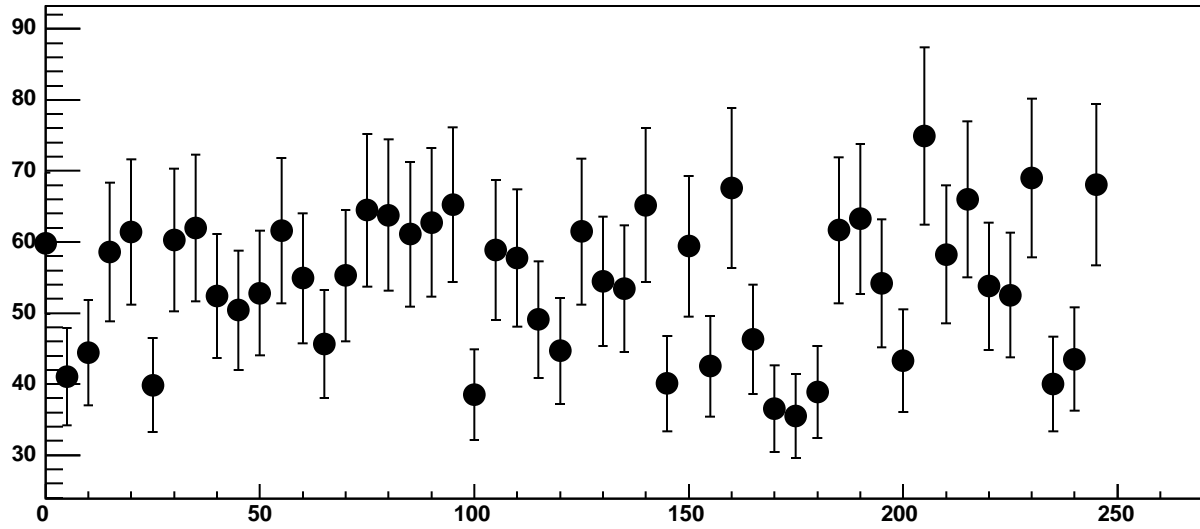




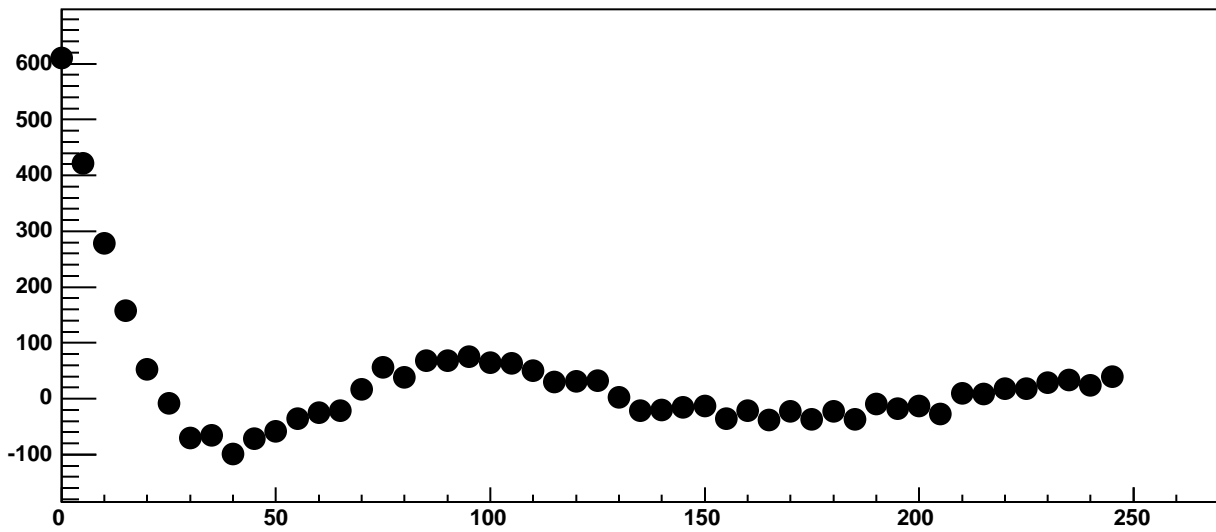
Chip 10, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold



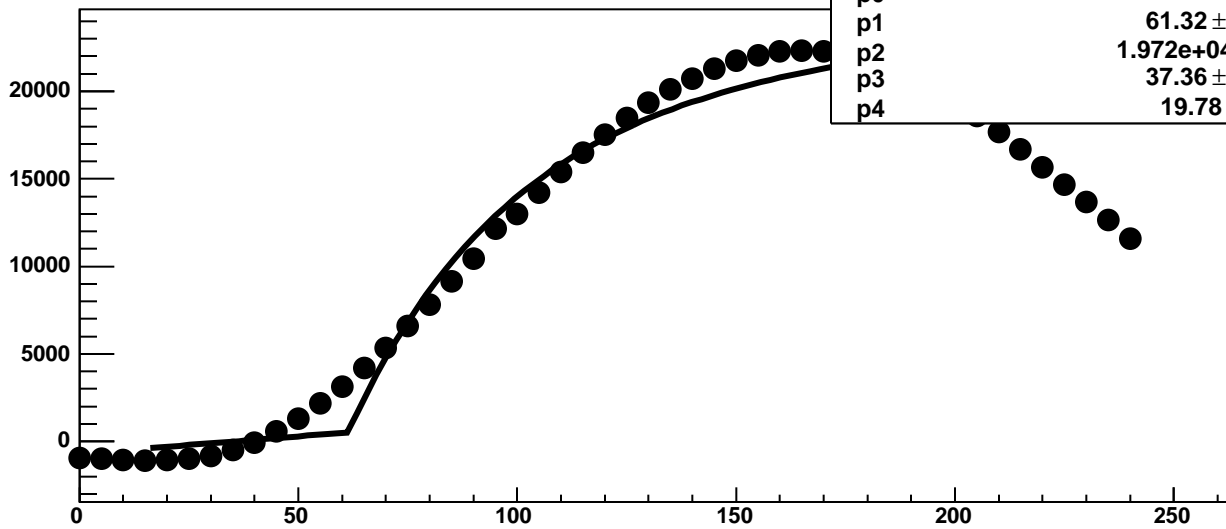
Chip 10, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold

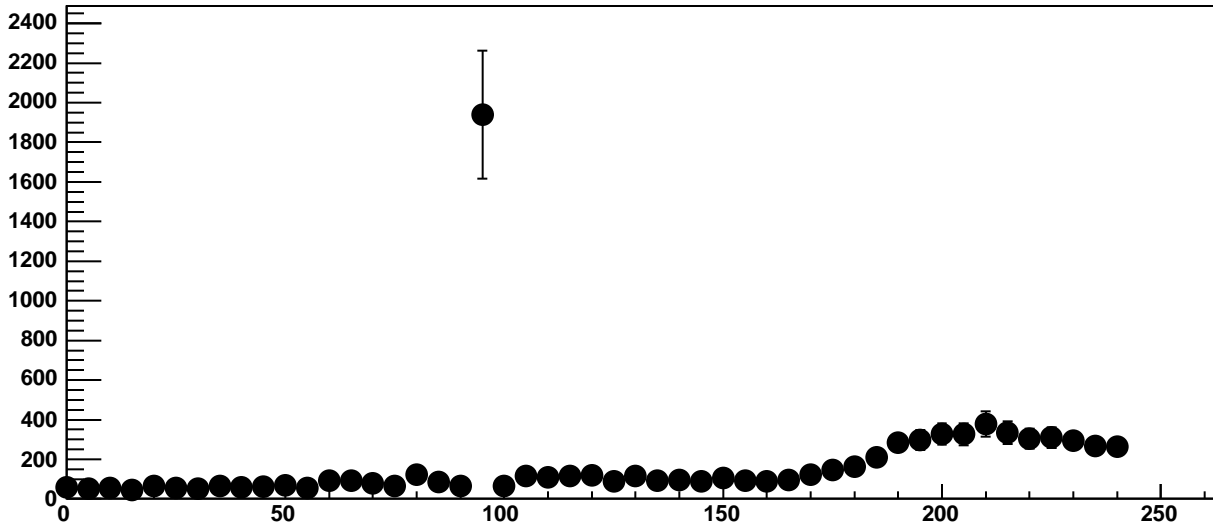


Chip 10, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold

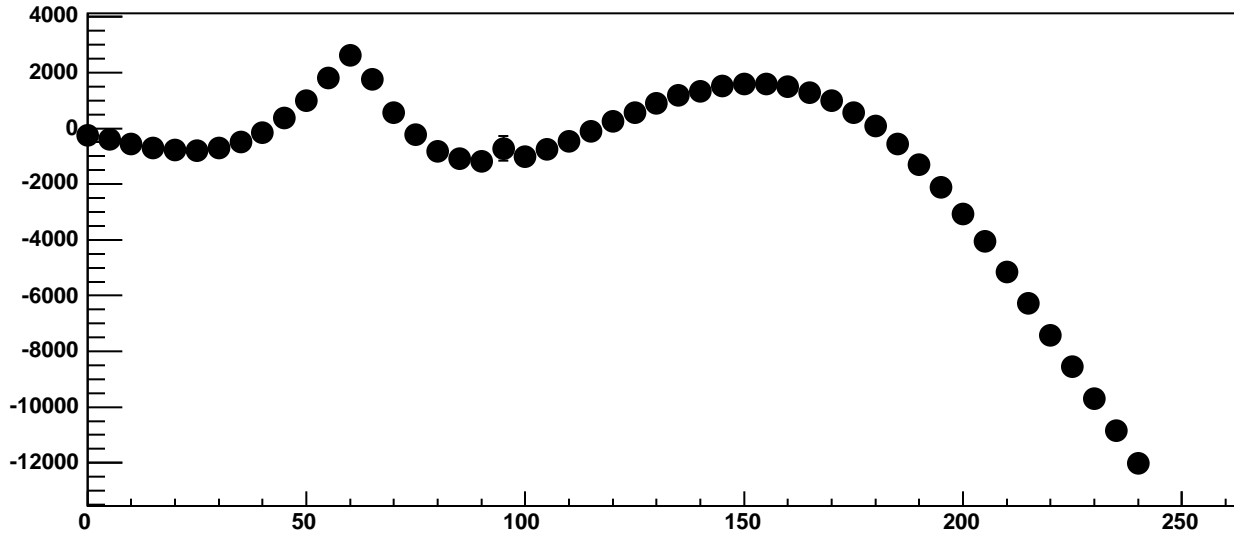


$\chi^2 / \text{ndf}$	2.477e+05 / 41
p0	510.4 ± 7.876
p1	61.32 ± 0.03322
p2	1.972e+04 ± 38.19
p3	37.36 ± 0.08728
p4	19.78 ± 0.2319

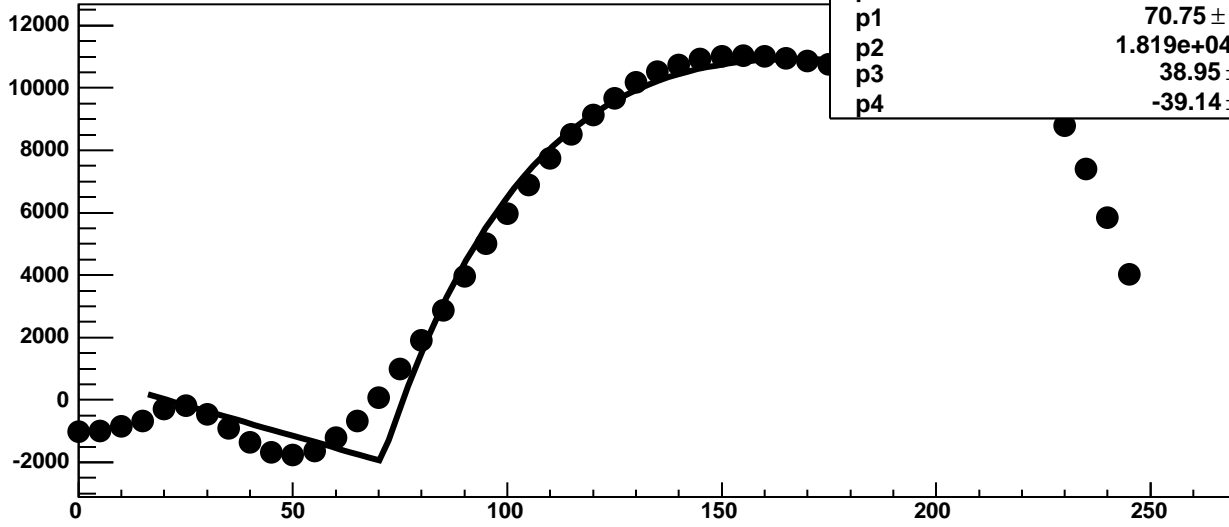
Chip 10, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



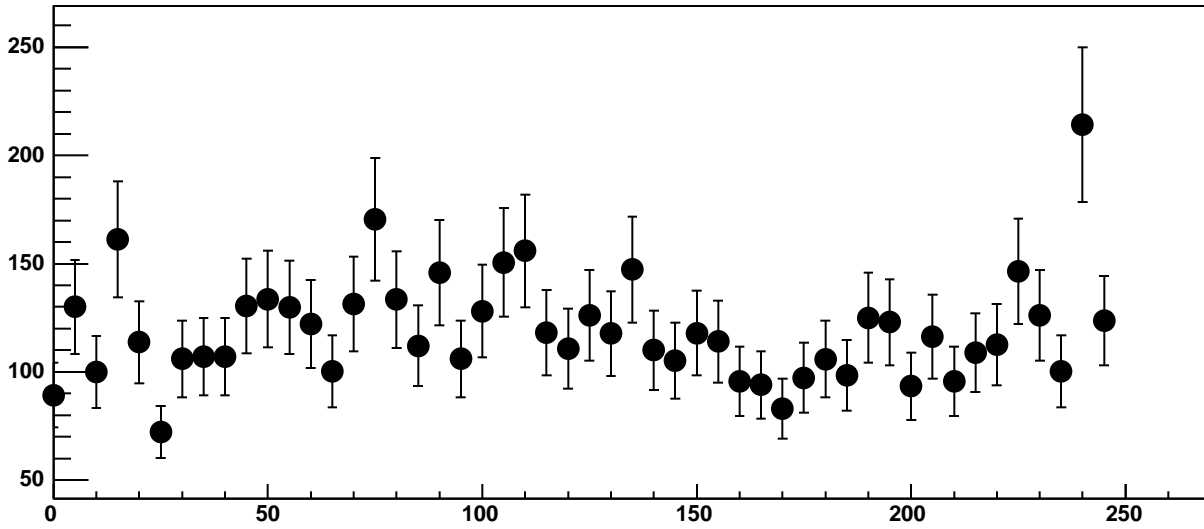
Chip 10, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold



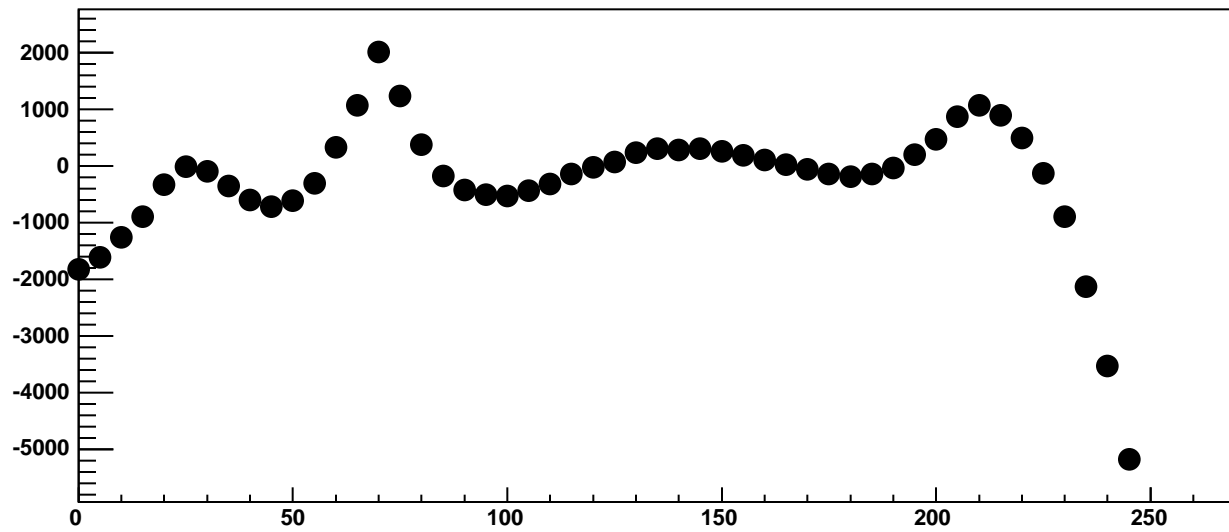
Chip 10, Channel 10, Enable 0, DAC=1600, ADC Mean vs Hold



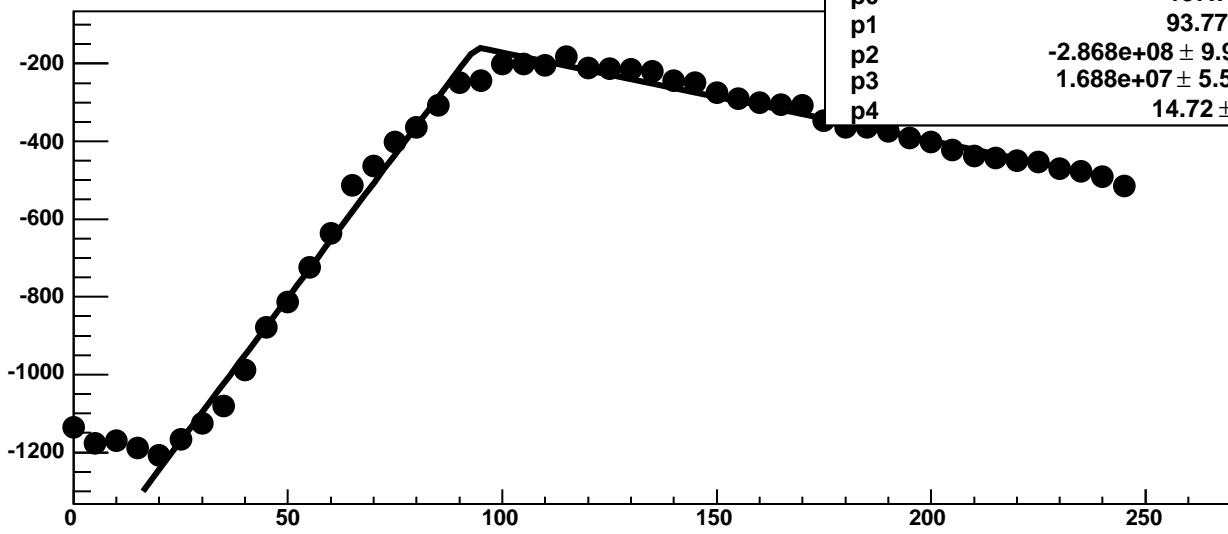
Chip 10, Channel 10, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 10, Enable 0, DAC=1600, ADC Residuals vs Hold

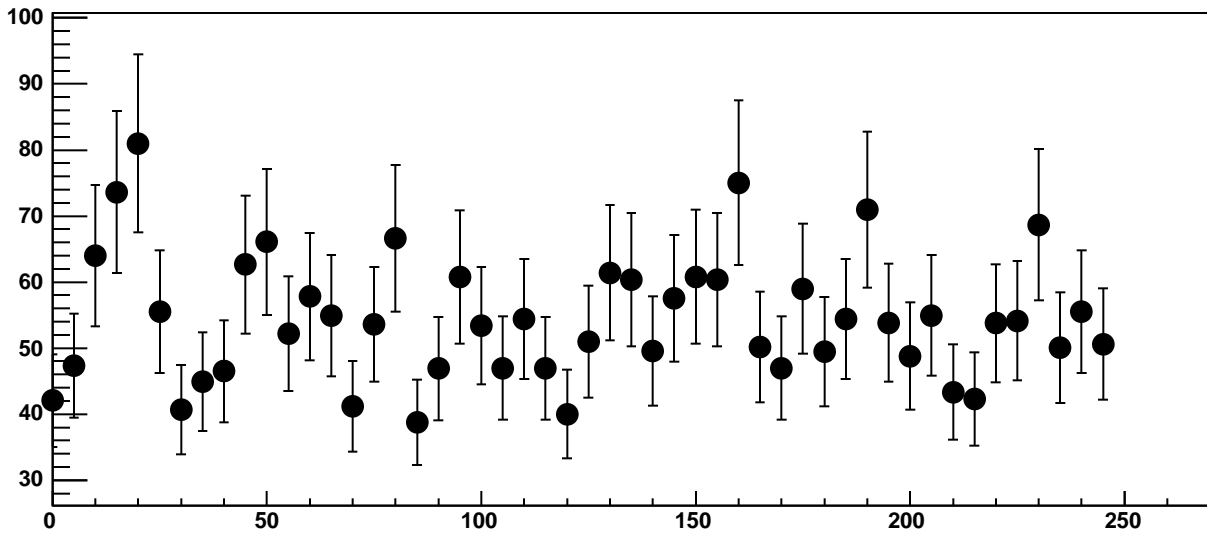


Chip 10, Channel 10, Enable 1, DAC=1600, ADC Mean vs Hold

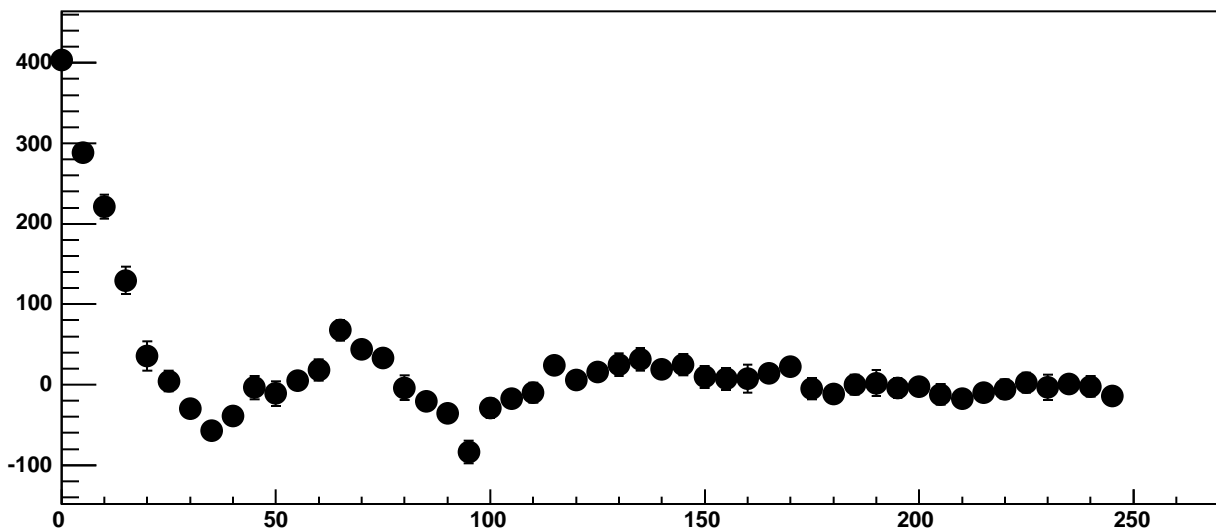


$\chi^2 / \text{ndf}$	273.2 / 41
p0	$-157.7 \pm 3.847$
p1	$93.77 \pm 0.427$
p2	$-2.868\text{e}+08 \pm 9.994\text{e}+06$
p3	$1.688\text{e}+07 \pm 5.544\text{e}+05$
p4	$14.72 \pm 0.1306$

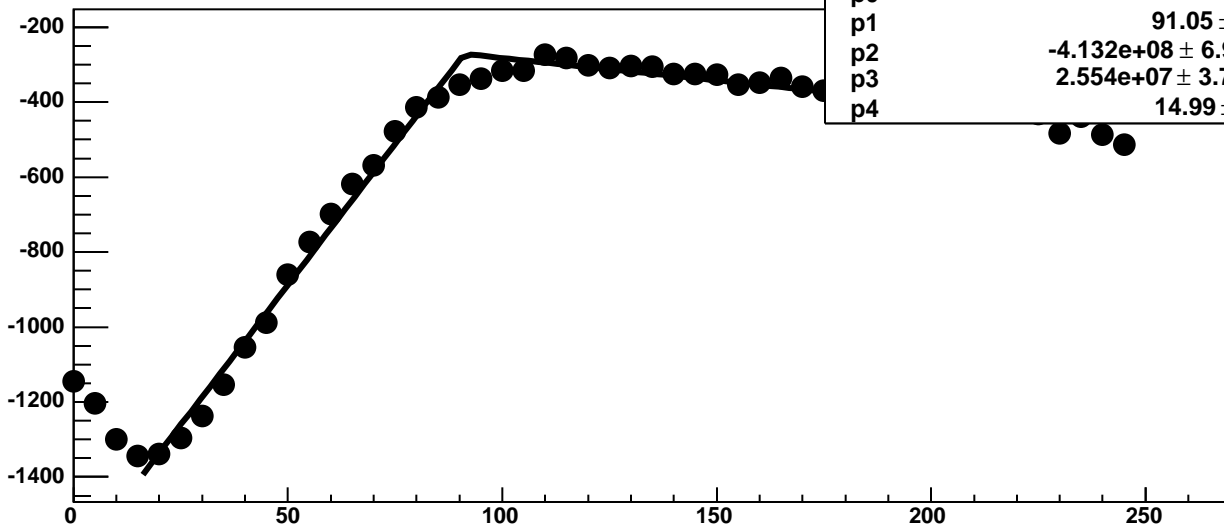
Chip 10, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold

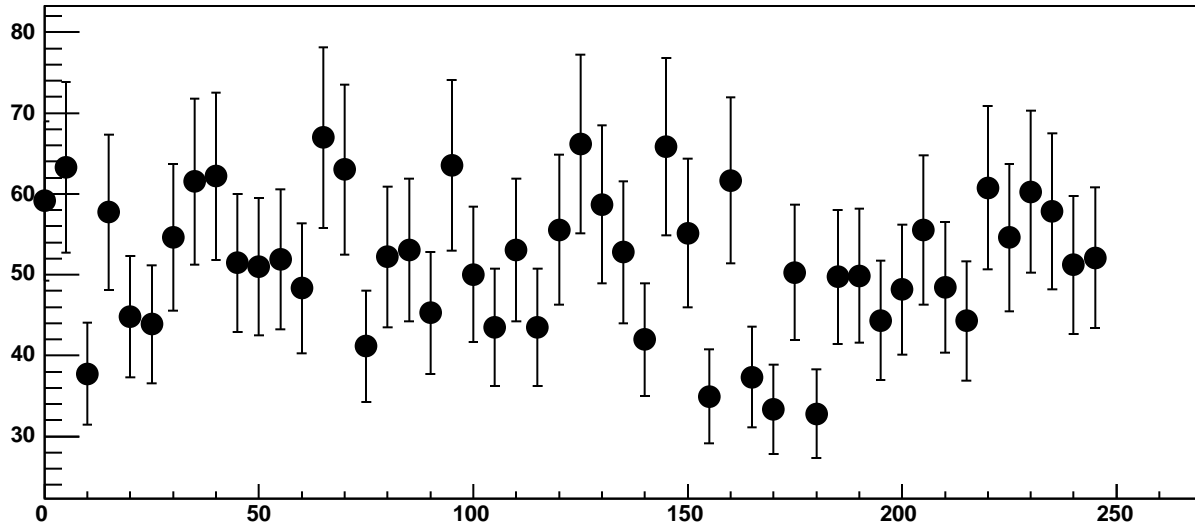


Chip 10, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

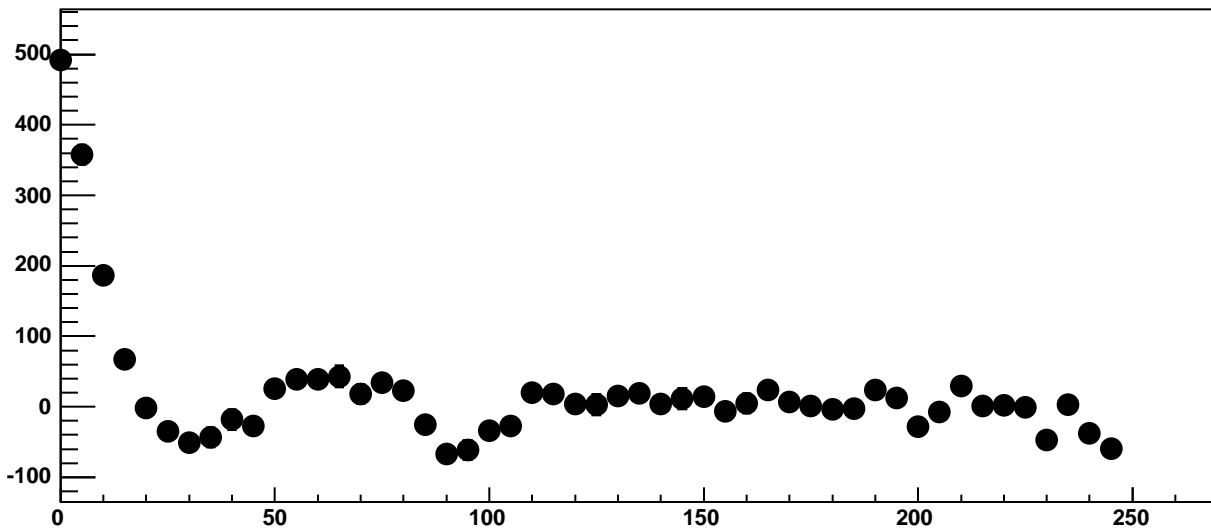


$\chi^2 / \text{ndf}$	266.7 / 41
p0	$-271.5 \pm 4.06$
p1	$91.05 \pm 0.4366$
p2	$-4.132\text{e}+08 \pm 6.947\text{e}+06$
p3	$2.554\text{e}+07 \pm 3.764\text{e}+05$
p4	$14.99 \pm 0.1239$

Chip 10, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold

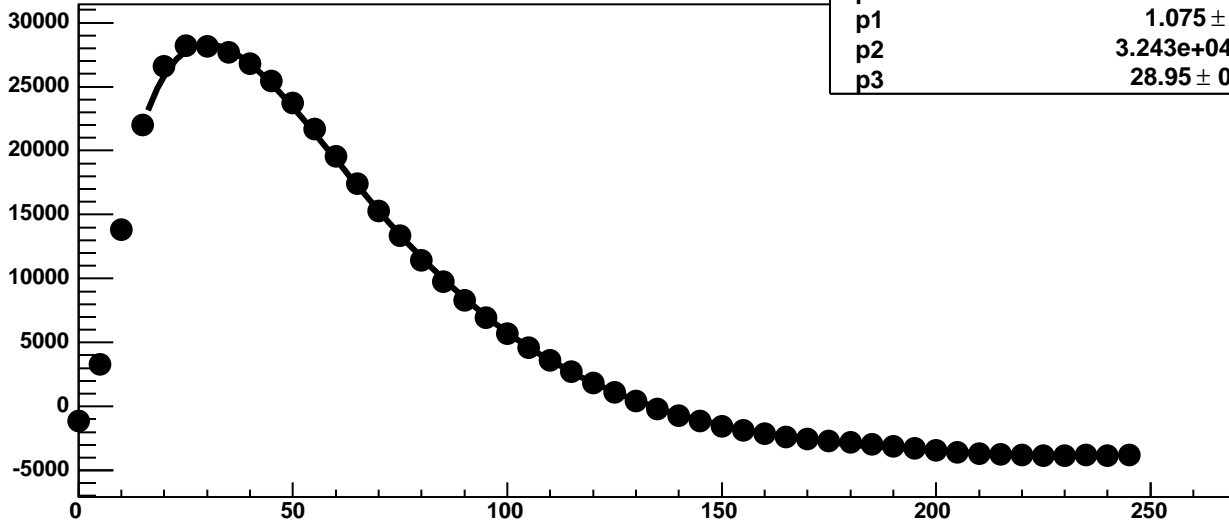


Chip 10, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

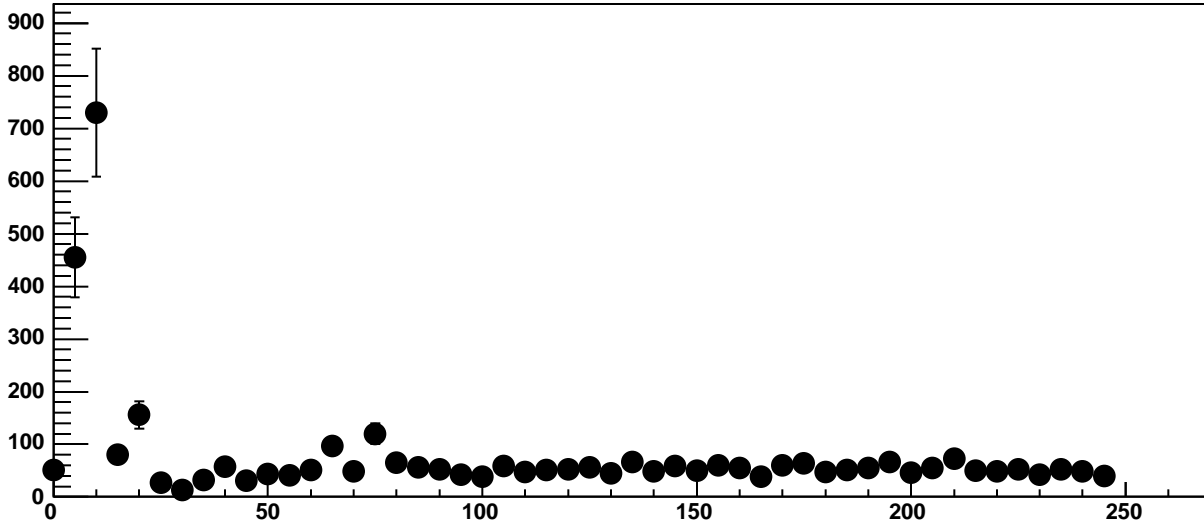


Chip 10, Channel 10, Enable 3!, DAC=1600, ADC Mean vs Hold

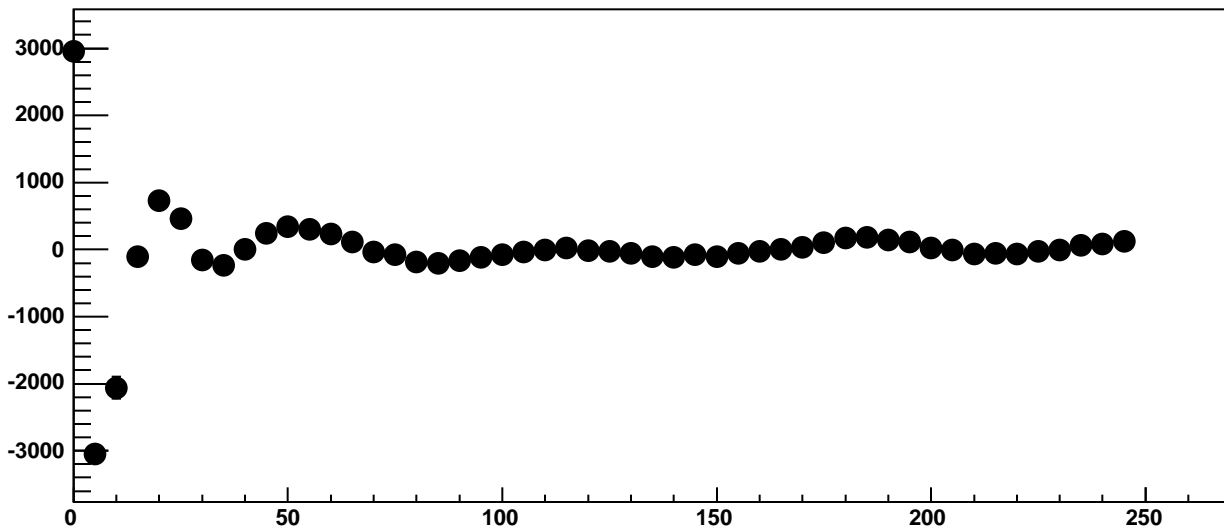
$\chi^2 / \text{ndf}$	1.493e+04 / 42
p0	-4103 ± 3.338
p1	1.075 ± 0.01666
p2	3.243e+04 ± 3.867
p3	28.95 ± 0.009179



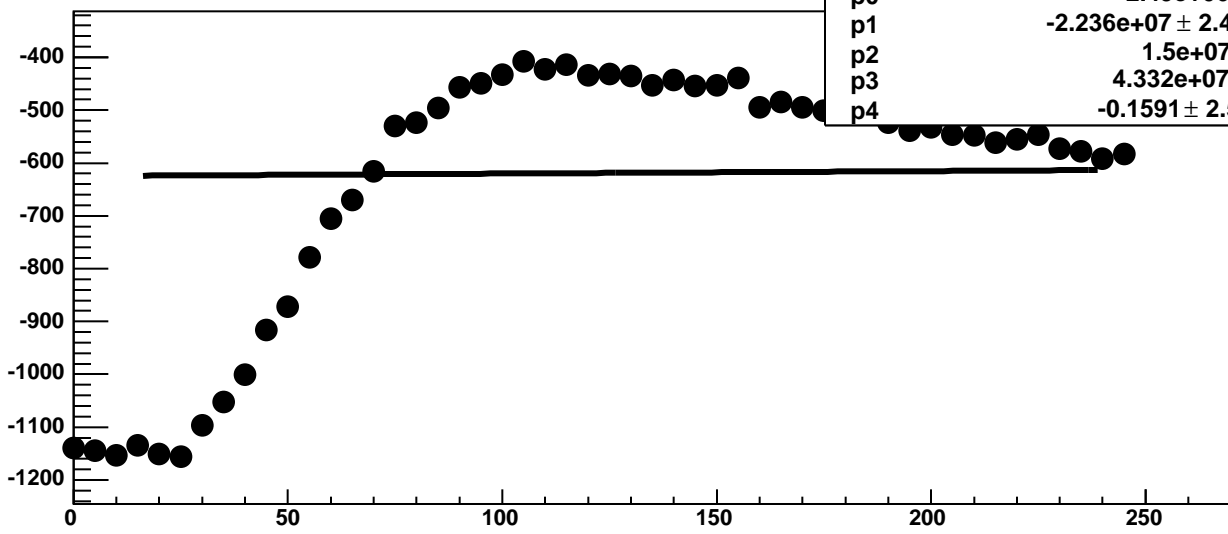
Chip 10, Channel 10, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 10, Enable 3!, DAC=1600, ADC Residuals vs Hold

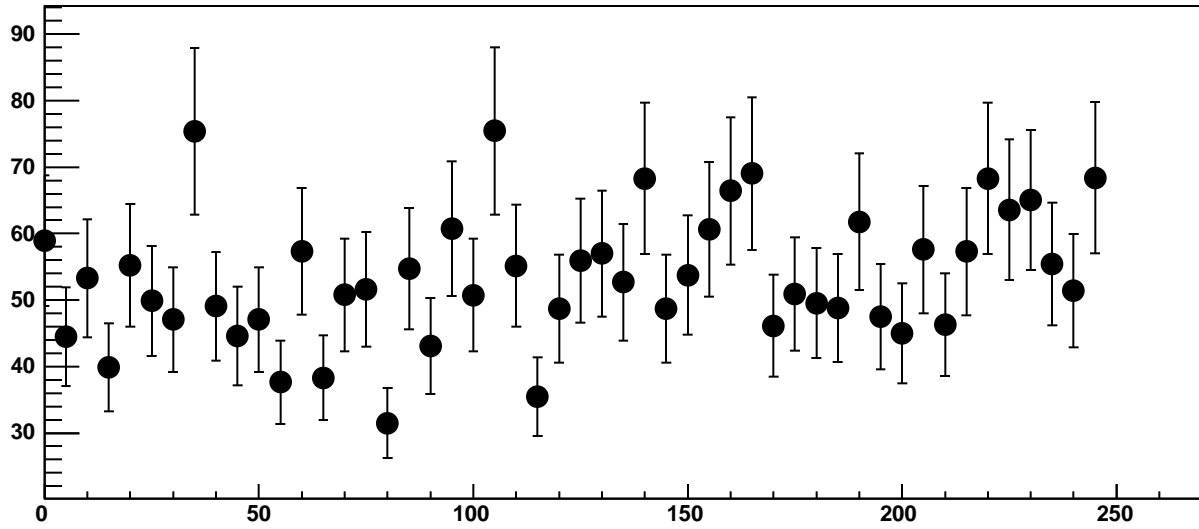


Chip 10, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold

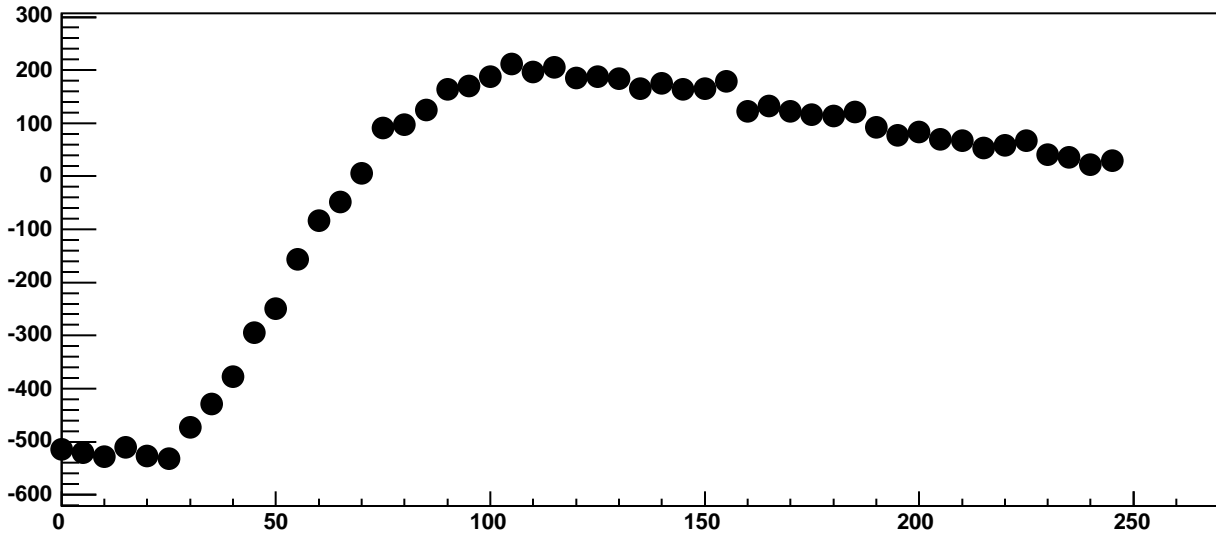


$\chi^2 / \text{ndf}$	1.691e+04 / 41
p0	-2.49e+06 ± 339.9
p1	-2.236e+07 ± 2.449e+04
p2	1.5e+07 ± 1175
p3	4.332e+07 ± 4286
p4	-0.1591 ± 2.553e-05

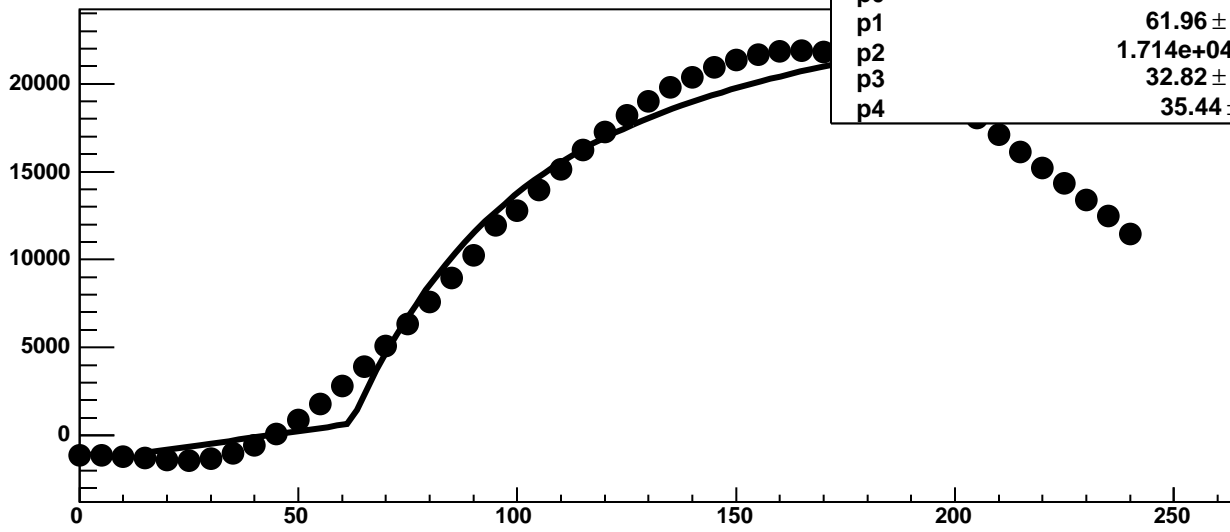
Chip 10, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

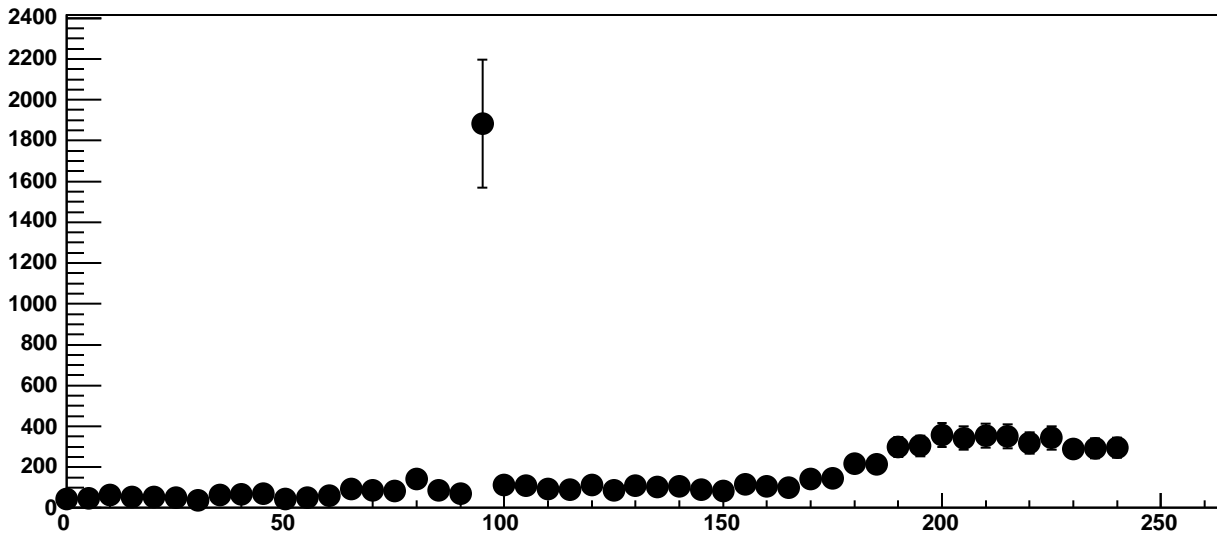


Chip 10, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

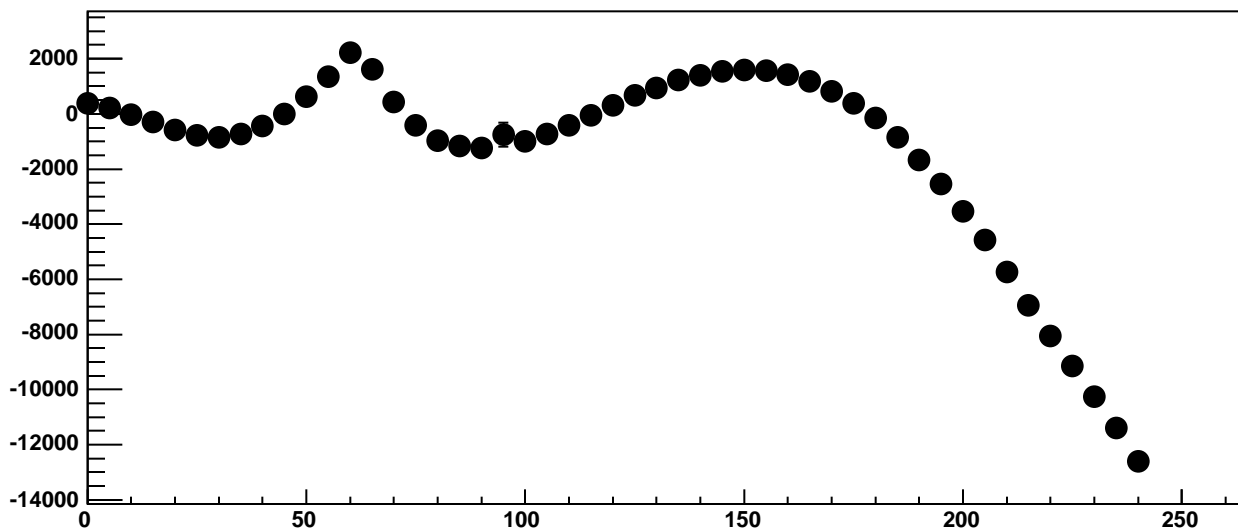


$\chi^2 / \text{ndf}$	2.459e+05 / 41
p0	658.6 ± 7.098
p1	61.96 ± 0.03474
p2	1.714e+04 ± 32.17
p3	32.82 ± 0.08278
p4	35.44 ± 0.2115

Chip 10, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



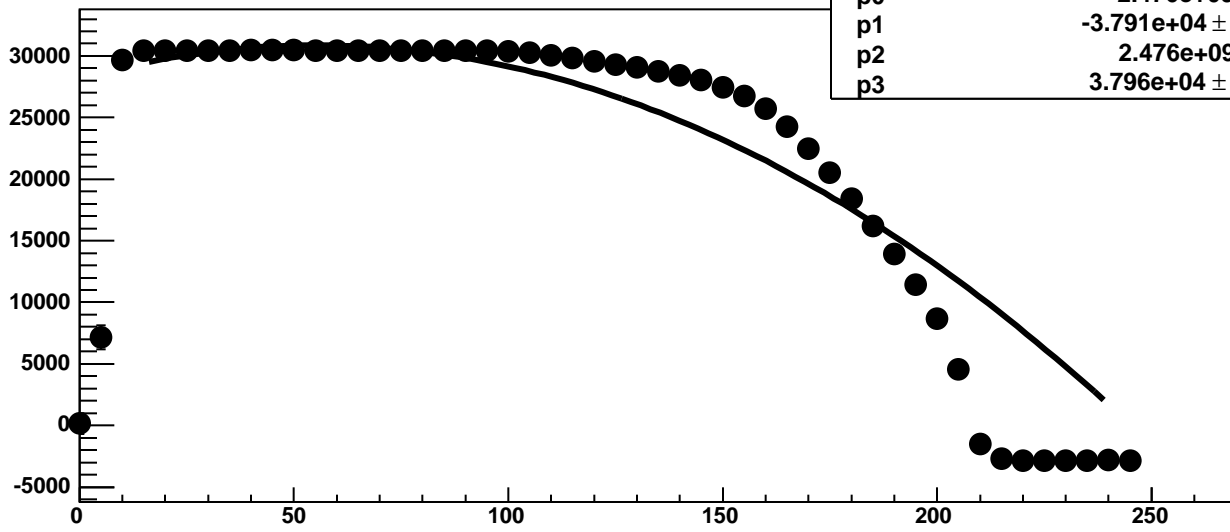
Chip 10, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



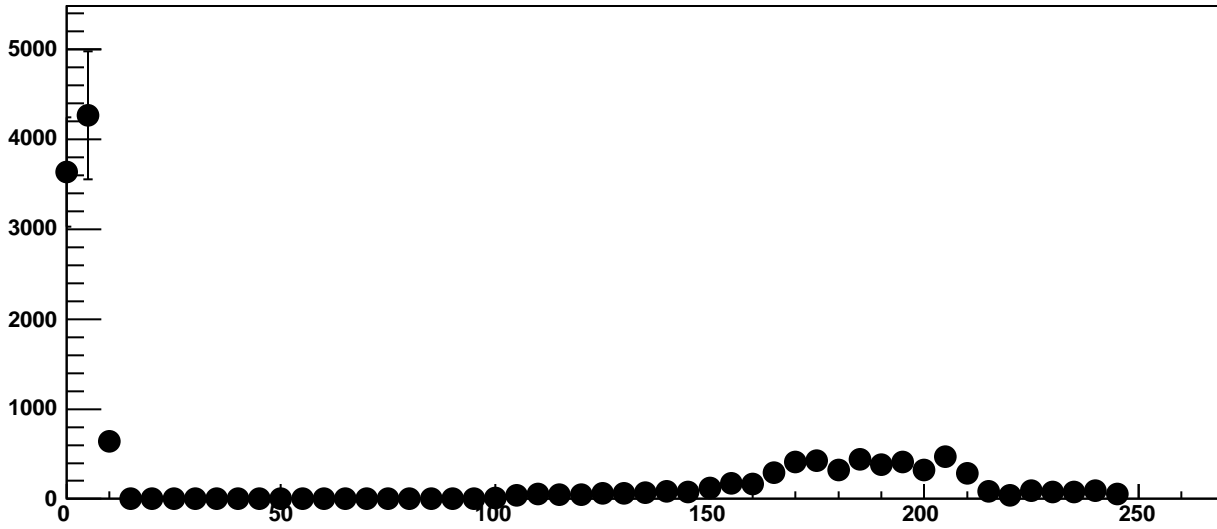


Chip 10, Channel 11, Enable 0!, DAC=1600, ADC Mean vs Hold

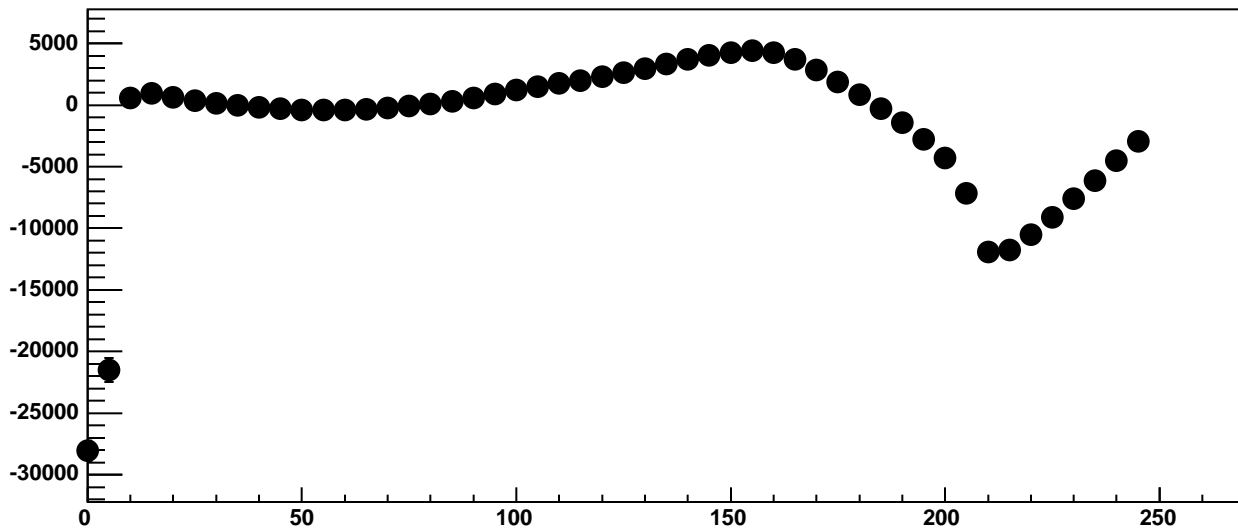
$\chi^2 / \text{ndf}$	7.233e+06 / 42
p0	-2.476e+09 $\pm$ 2.975
p1	-3.791e+04 $\pm$ 0.07305
p2	2.476e+09 $\pm$ 2.975
p3	3.796e+04 $\pm$ 0.07303



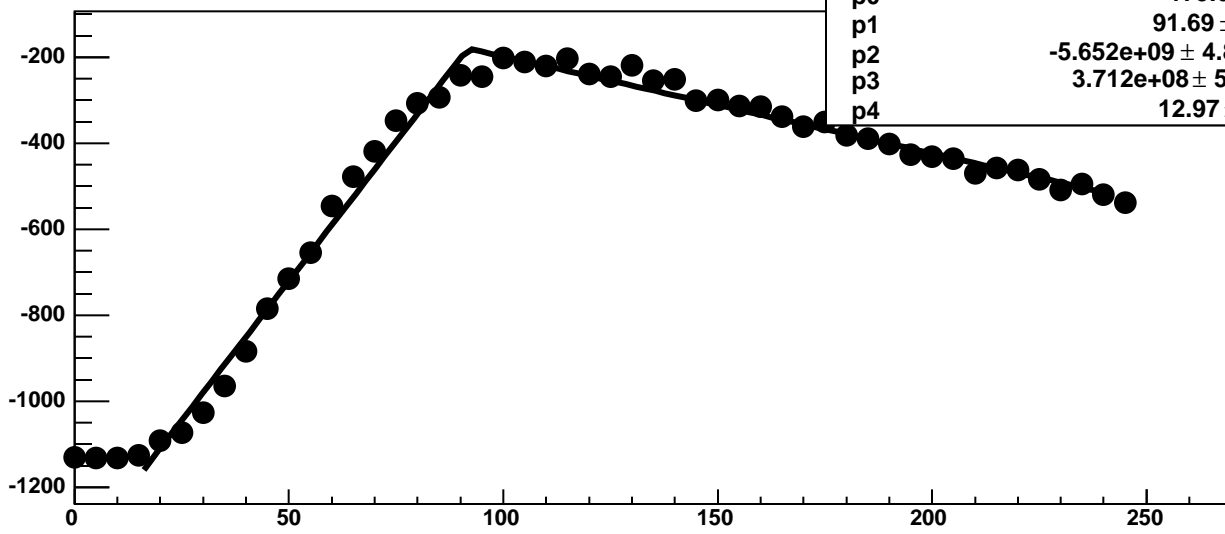
Chip 10, Channel 11, Enable 0!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 11, Enable 0!, DAC=1600, ADC Residuals vs Hold

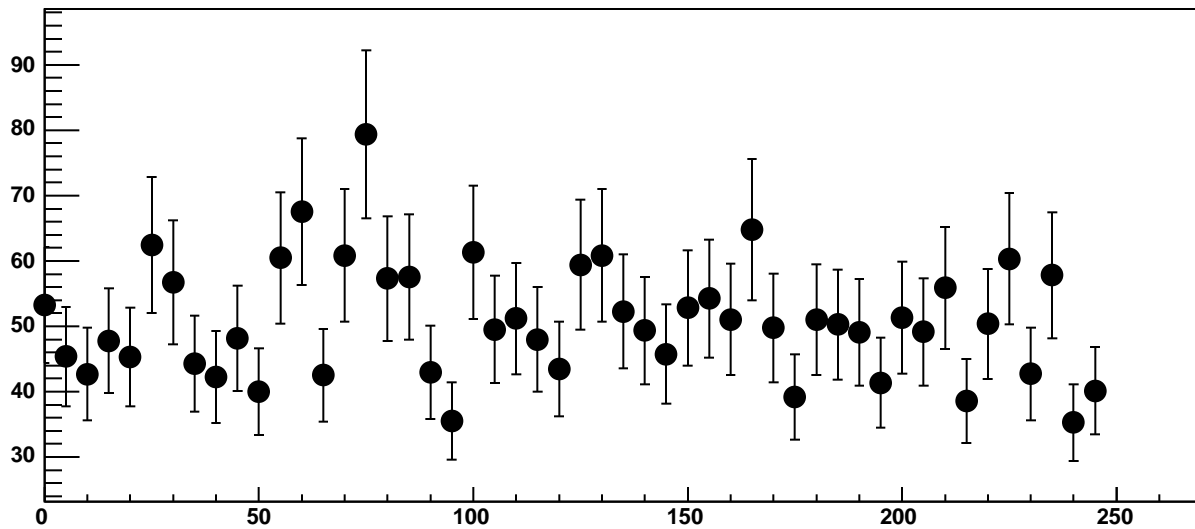


Chip 10, Channel 11, Enable 1, DAC=1600, ADC Mean vs Hold

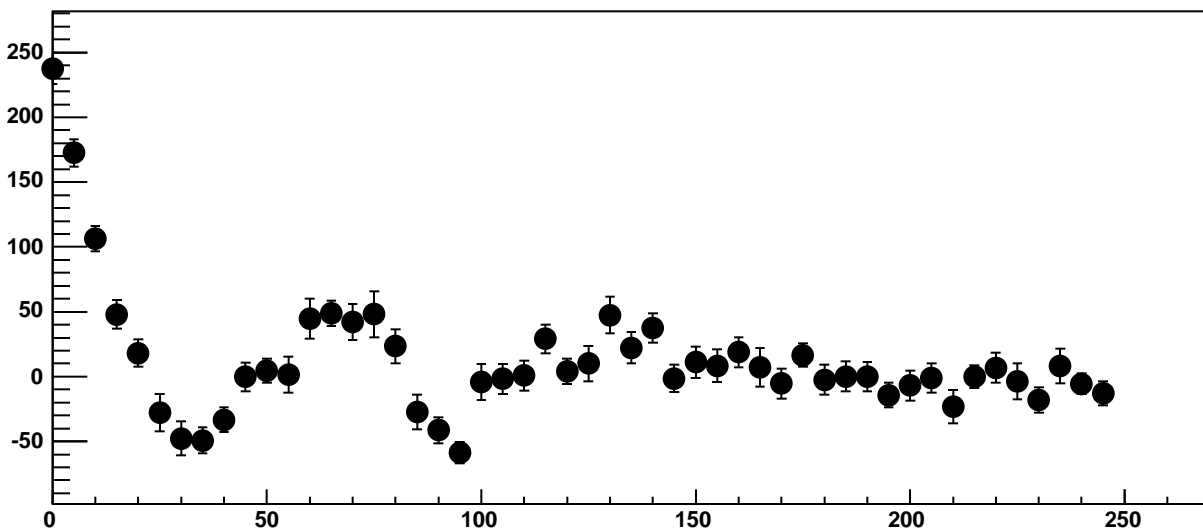


$\chi^2 / \text{ndf}$	253.5 / 41
p0	$-179.6 \pm 3.502$
p1	$91.69 \pm 0.4824$
p2	$-5.652\text{e}+09 \pm 4.872\text{e}+07$
p3	$3.712\text{e}+08 \pm 5.17\text{e}+05$
p4	$12.97 \pm 0.1291$

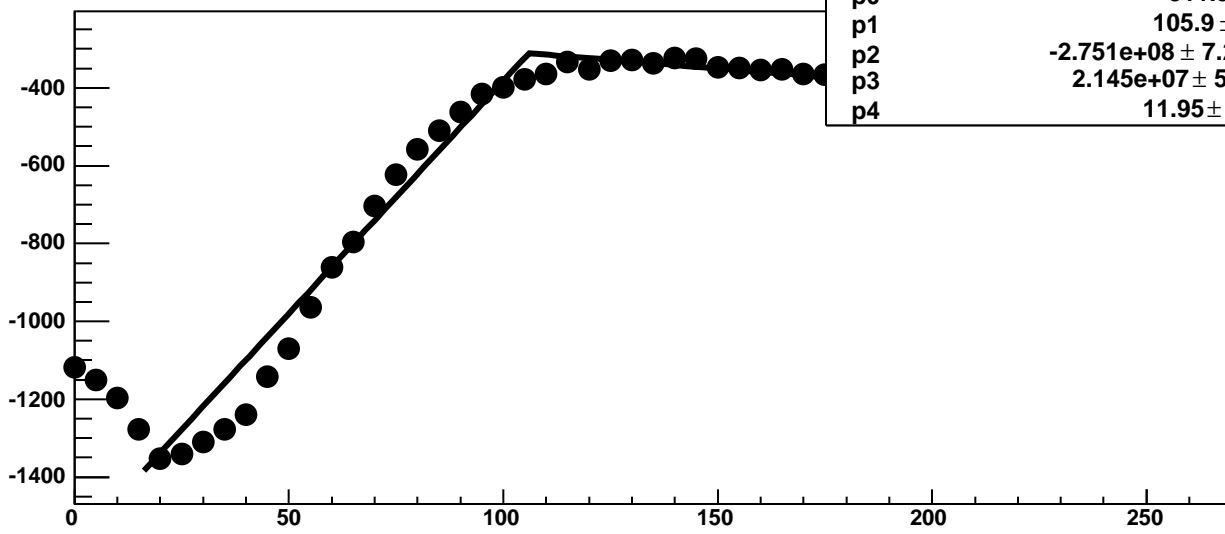
Chip 10, Channel 11, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 11, Enable 1, DAC=1600, ADC Residuals vs Hold

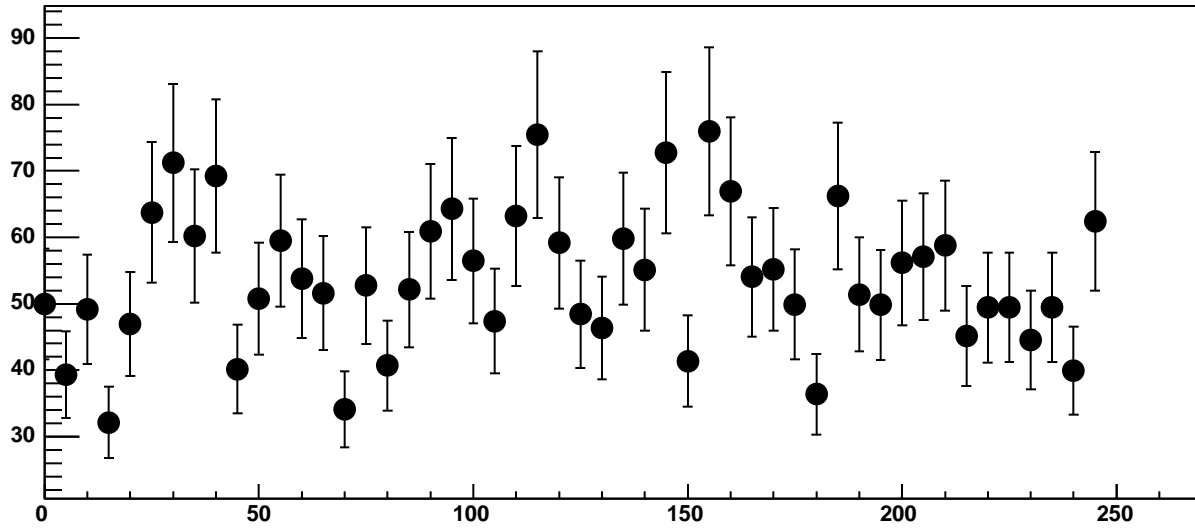


Chip 10, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

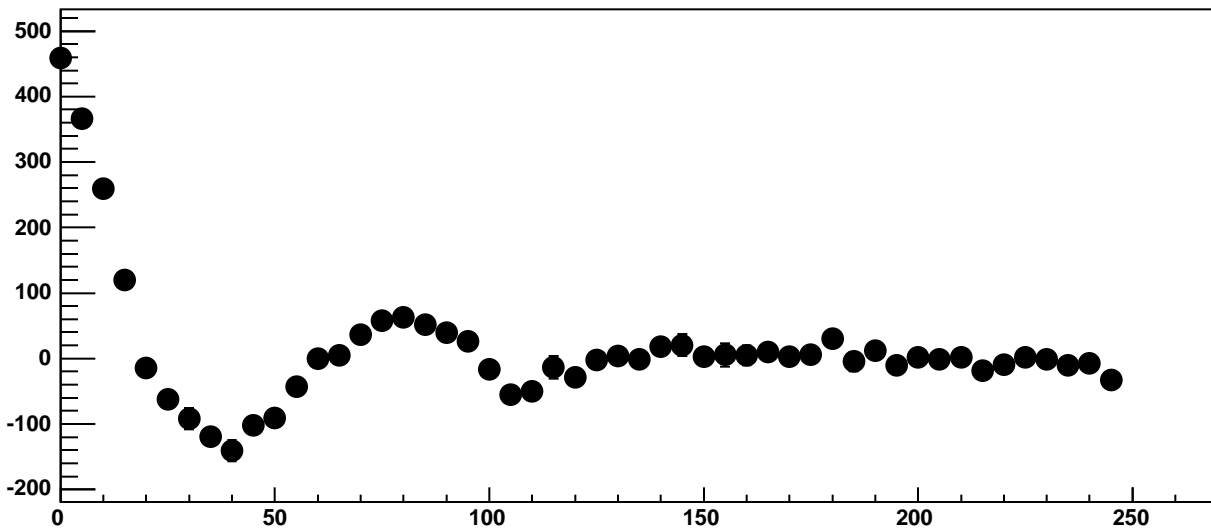


$\chi^2 / \text{ndf}$	850.9 / 41
p0	-311.3 ± 4.648
p1	105.9 ± 0.5534
p2	-2.751e+08 ± 7.255e+06
p3	2.145e+07 ± 5.16e+05
p4	11.95 ± 0.09279

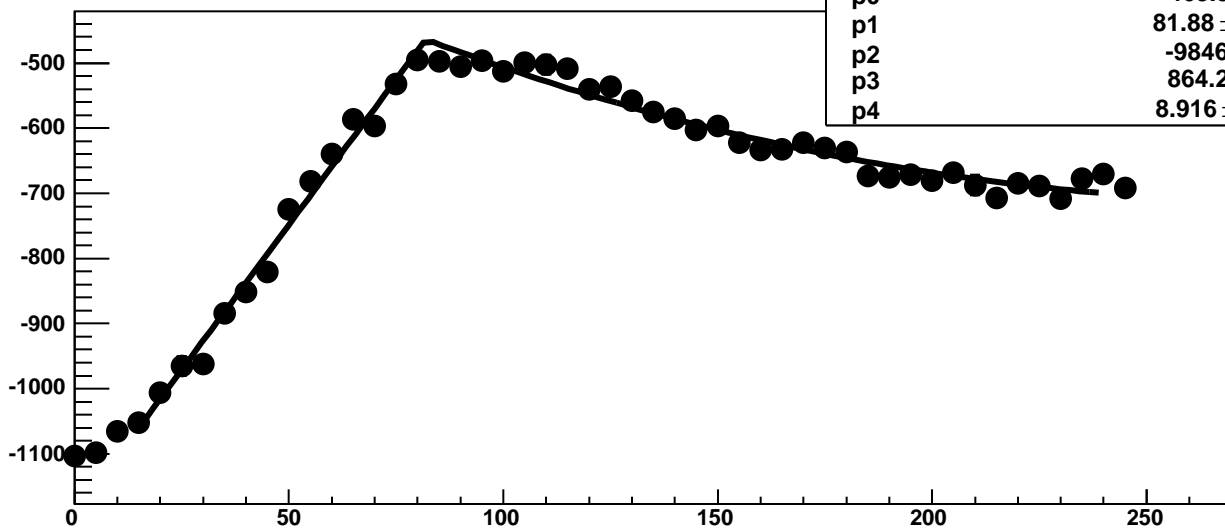
Chip 10, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

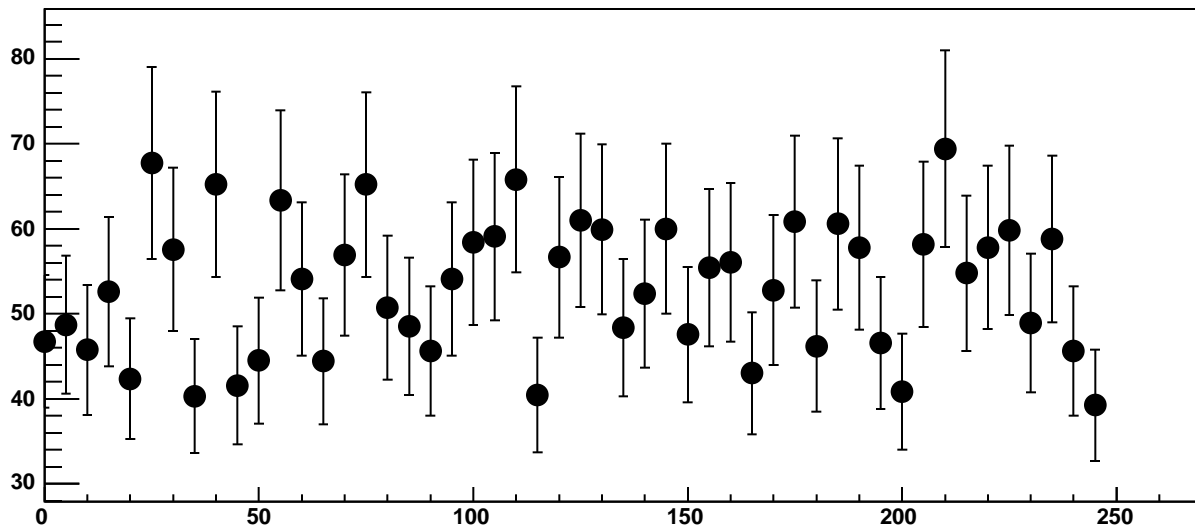


Chip 10, Channel 11, Enable 3, DAC=1600, ADC Mean vs Hold

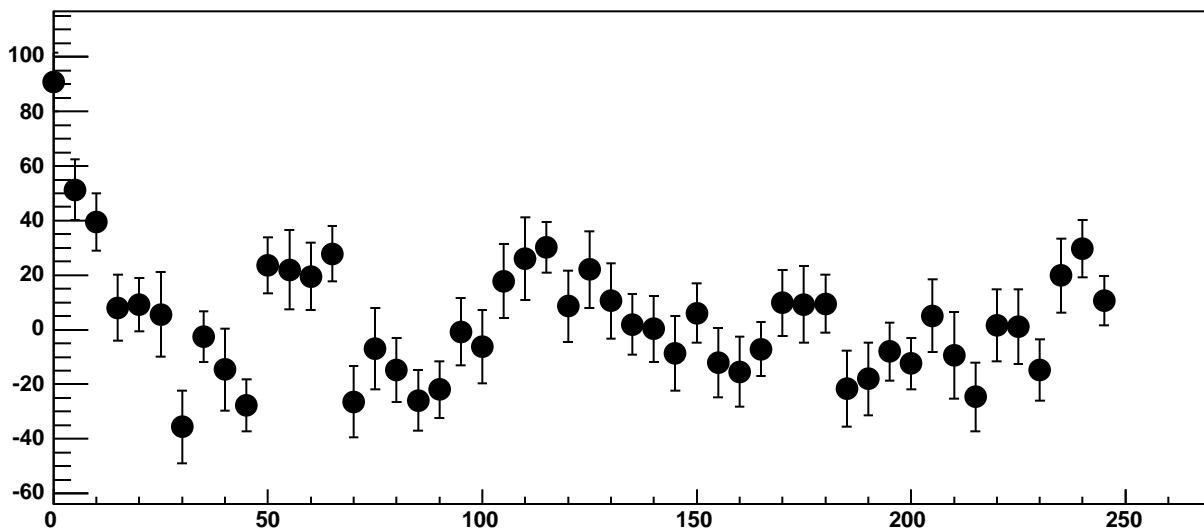


$\chi^2 / \text{ndf}$	98.84 / 41
p0	$-463.8 \pm 4.858$
p1	$81.88 \pm 0.7584$
p2	$-9846 \pm 1388$
p3	$864.2 \pm 131.7$
p4	$8.916 \pm 0.1588$

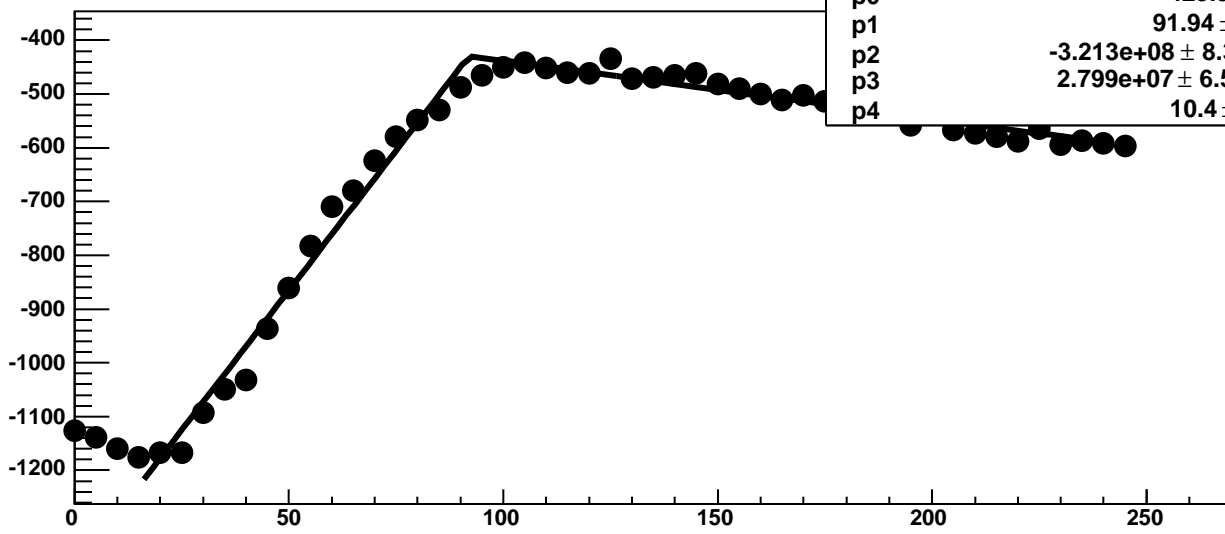
Chip 10, Channel 11, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 11, Enable 3, DAC=1600, ADC Residuals vs Hold

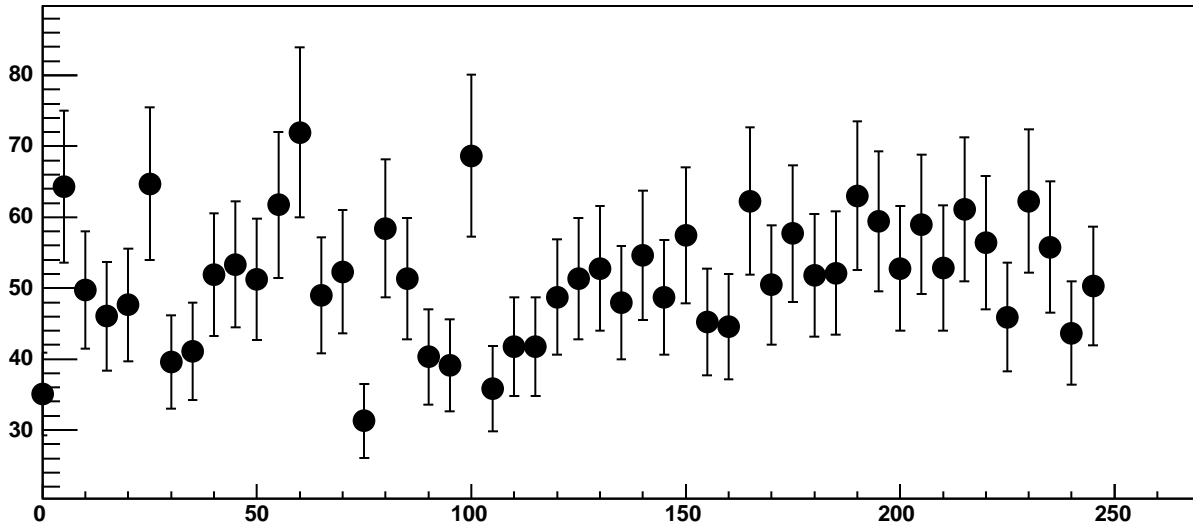


Chip 10, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold

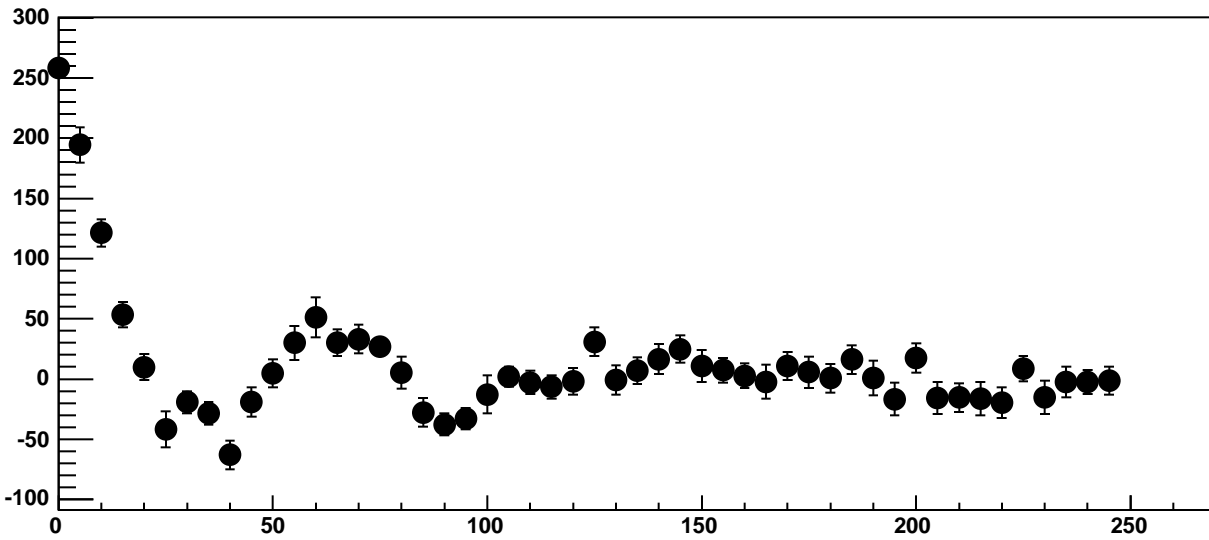


$\chi^2 / \text{ndf}$	188.9 / 41
p0	-429.3 ± 3.542
p1	91.94 ± 0.5615
p2	-3.213e+08 ± 8.384e+06
p3	2.799e+07 ± 6.591e+05
p4	10.4 ± 0.1138

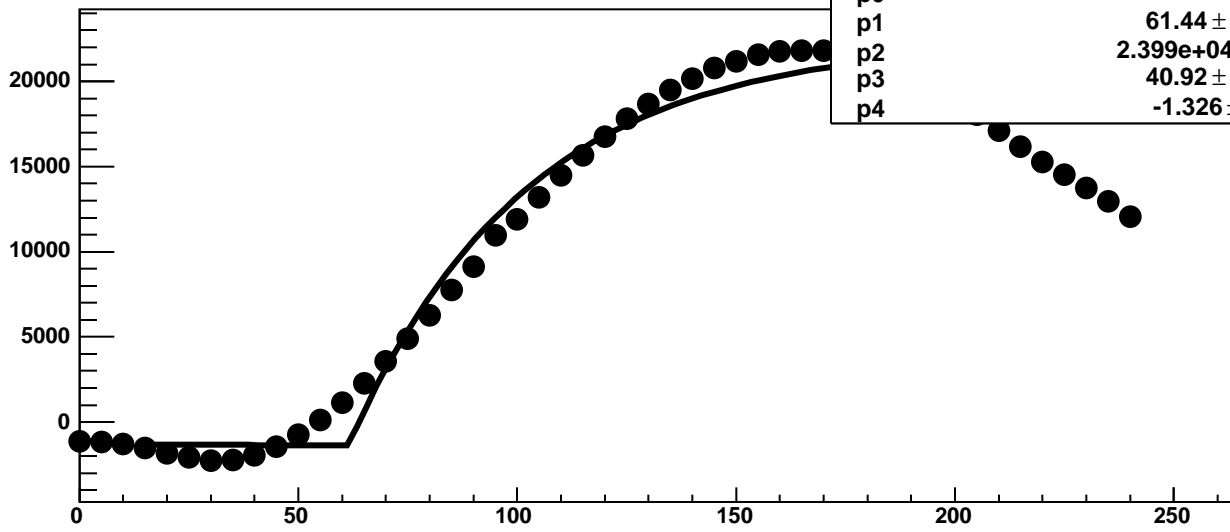
Chip 10, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



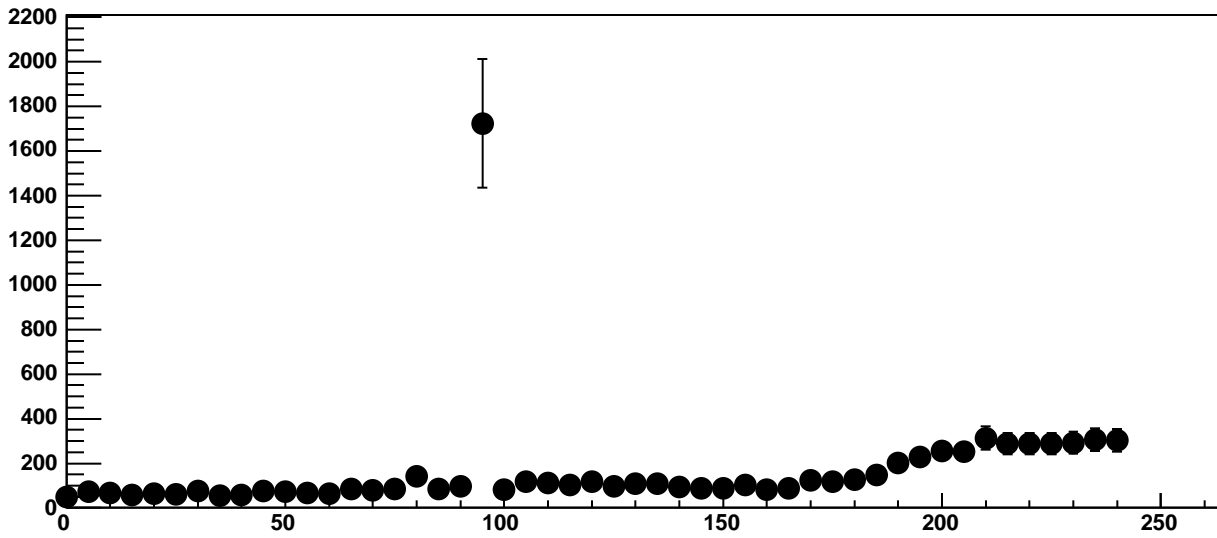
Chip 10, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold



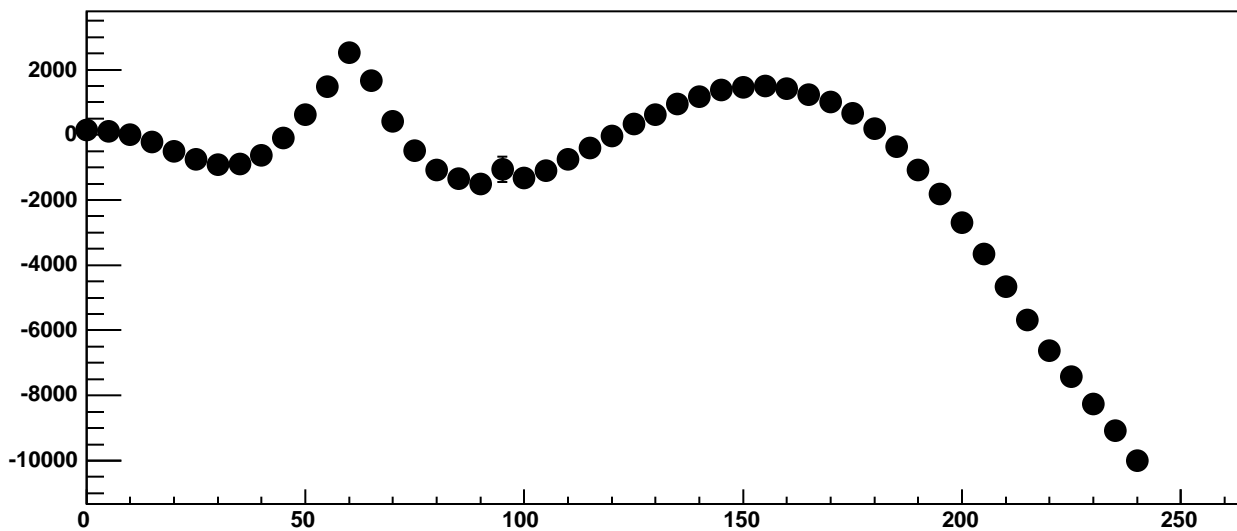
Chip 10, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold

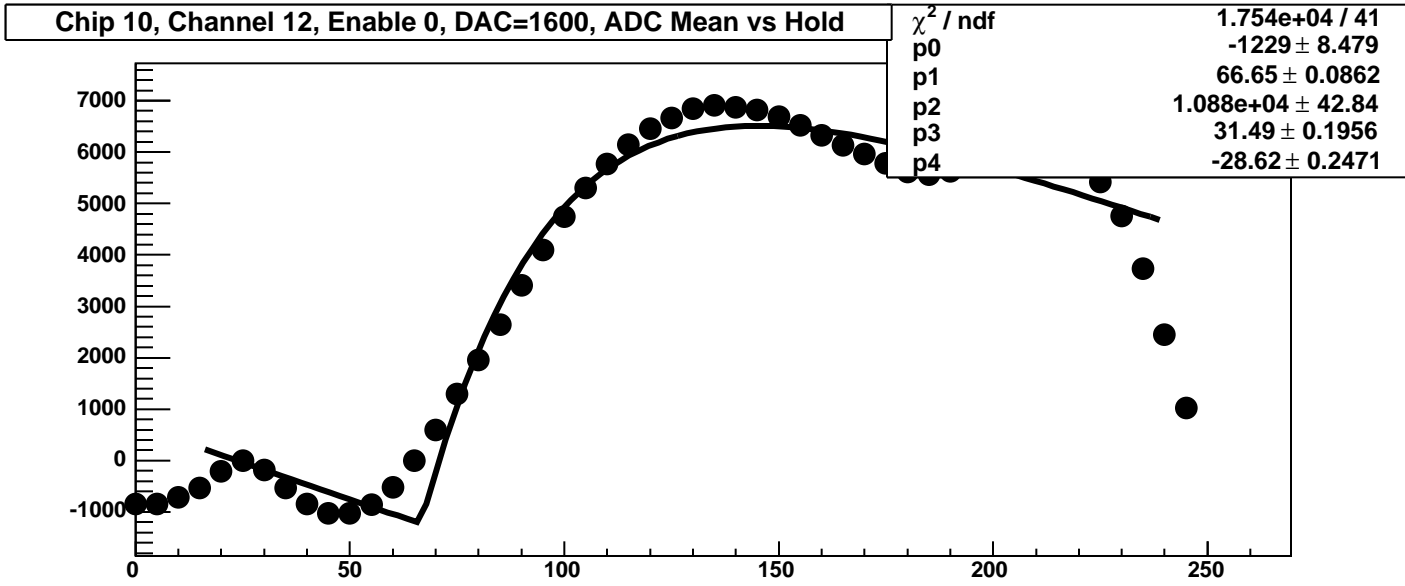


Chip 10, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold

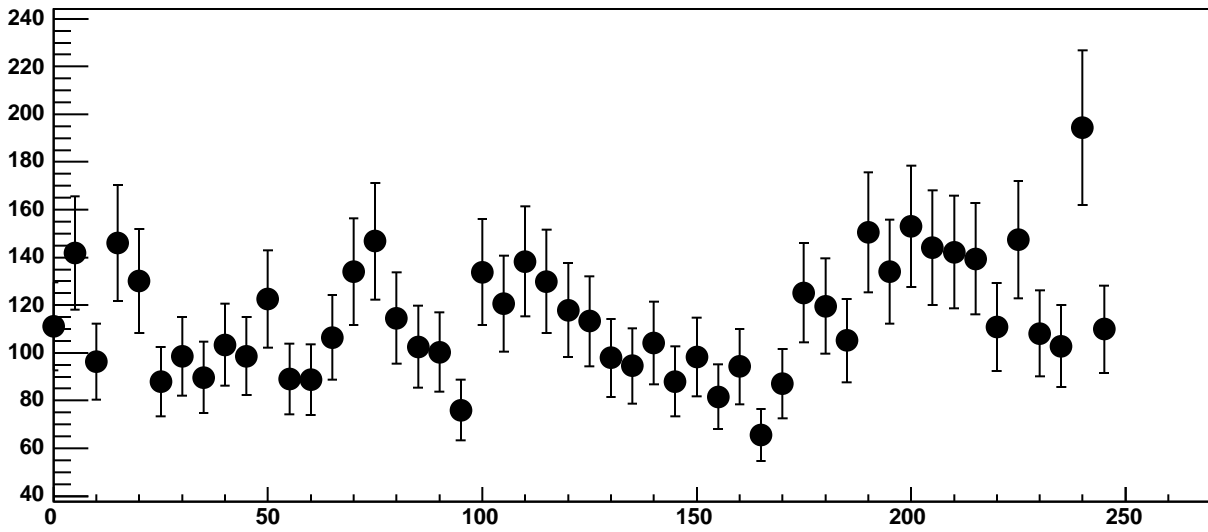


Chip 10, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

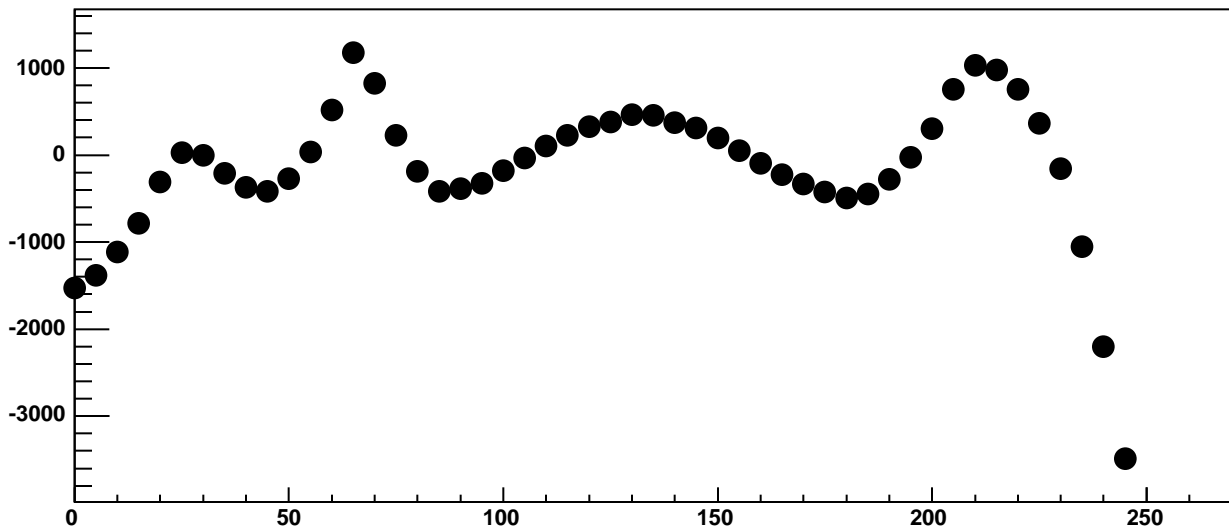




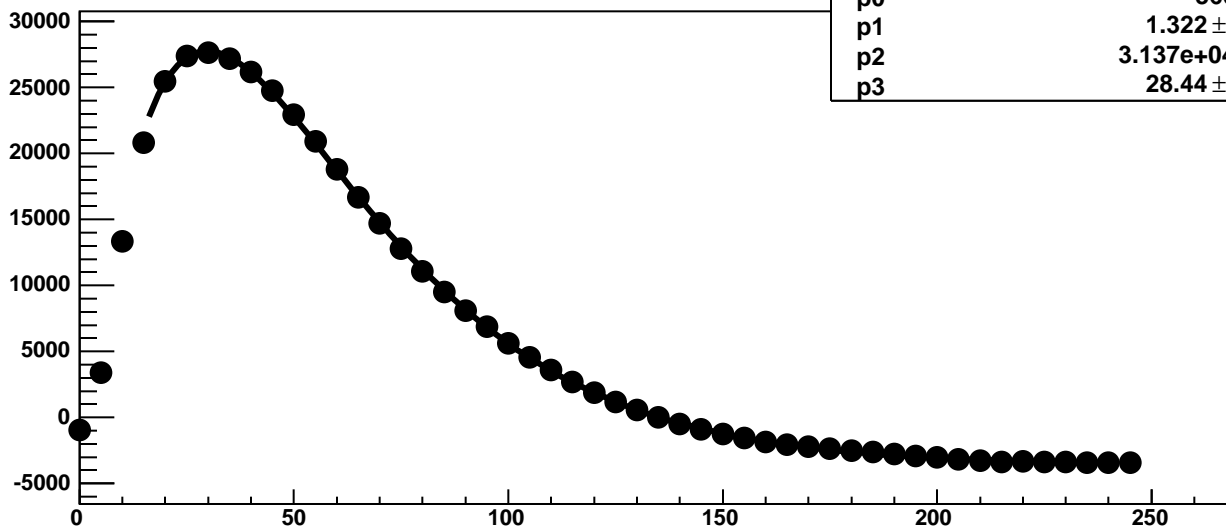
**Chip 10, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold**

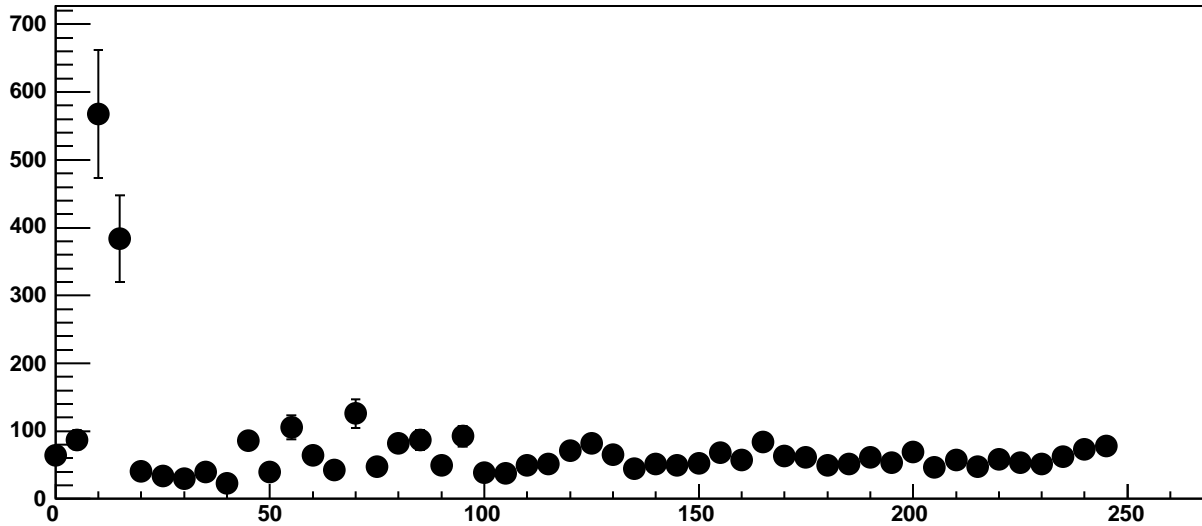


Chip 10, Channel 12, Enable 1!, DAC=1600, ADC Mean vs Hold

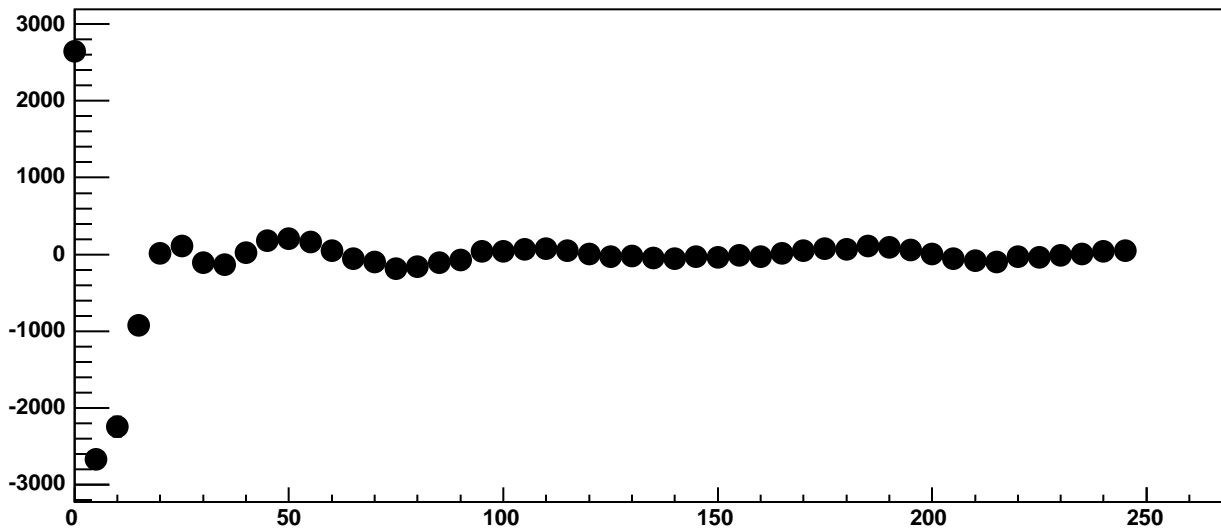


$\chi^2 / \text{ndf}$	2494 / 42
p0	-3607 ± 3.6
p1	1.322 ± 0.01797
p2	3.137e+04 ± 4.361
p3	28.44 ± 0.01034

Chip 10, Channel 12, Enable 1!, DAC=1600, ADC Noise vs Hold

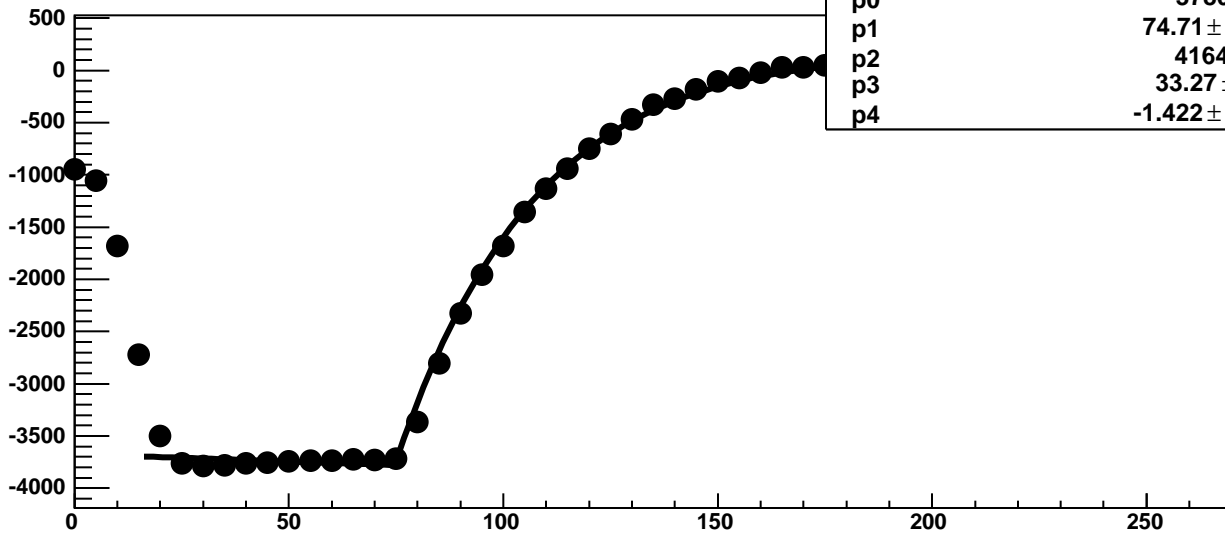


Chip 10, Channel 12, Enable 1!, DAC=1600, ADC Residuals vs Hold



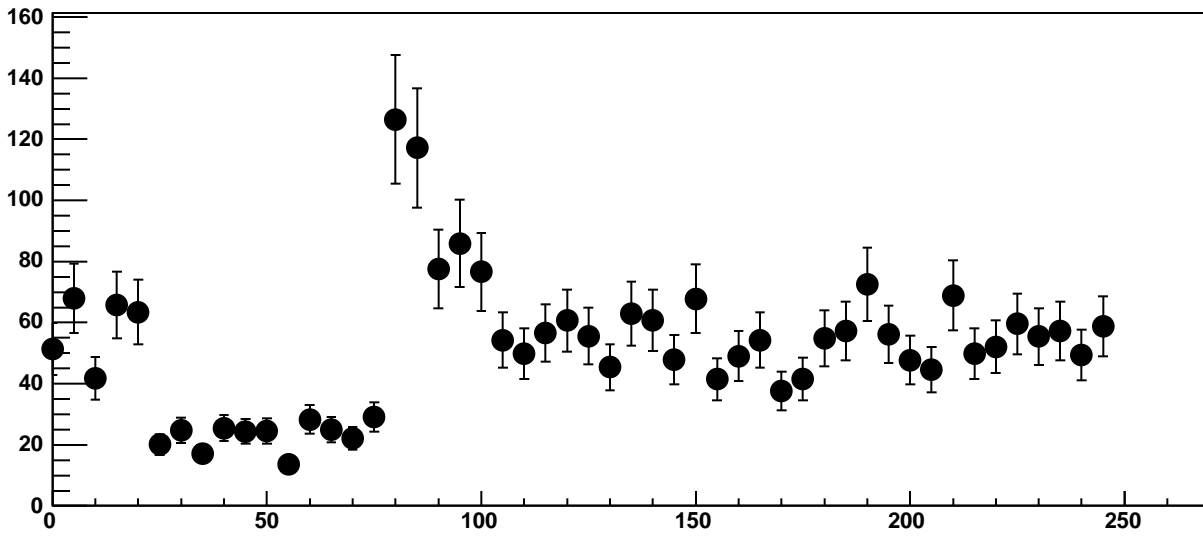


Chip 10, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

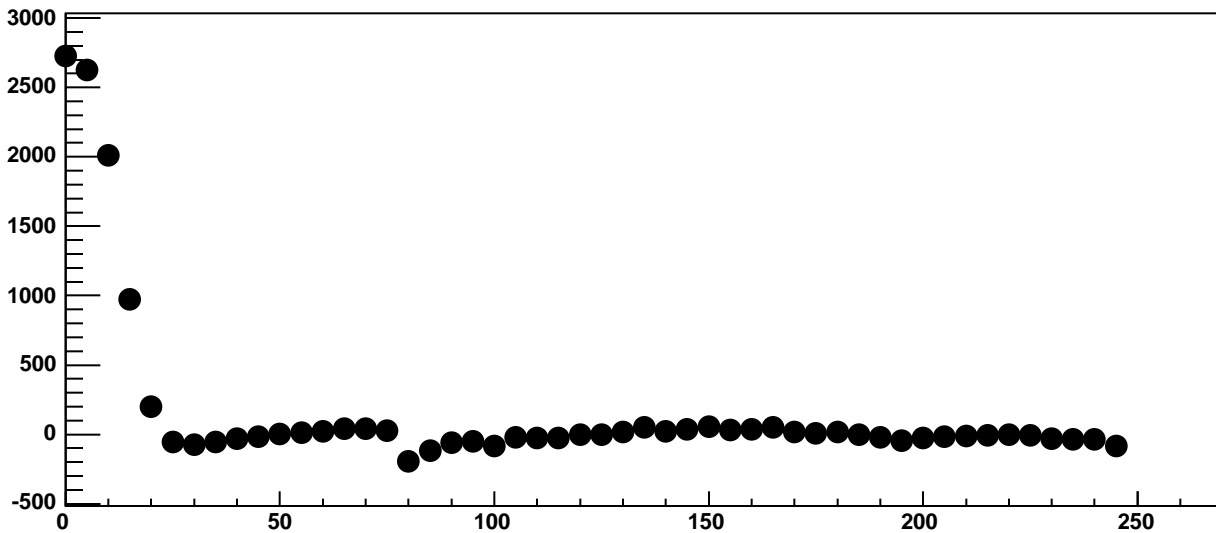


$\chi^2 / \text{ndf}$	5317 / 41
p0	$-3780 \pm 2.932$
p1	$74.71 \pm 0.05886$
p2	$4164 \pm 16.48$
p3	$33.27 \pm 0.1997$
p4	$-1.422 \pm 0.09108$

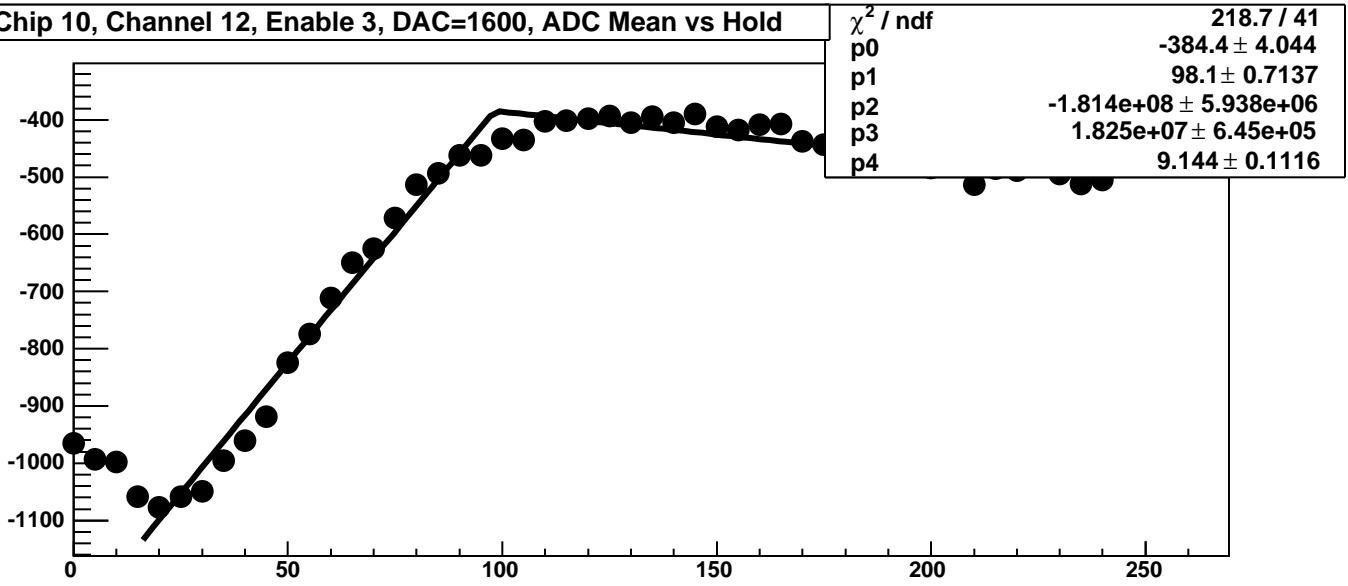
Chip 10, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



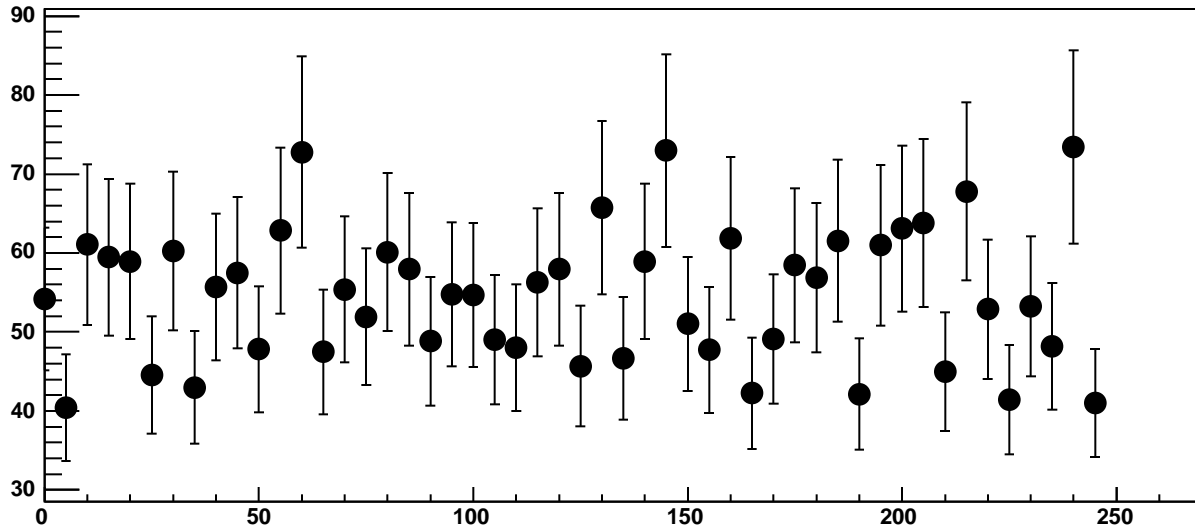
Chip 10, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold



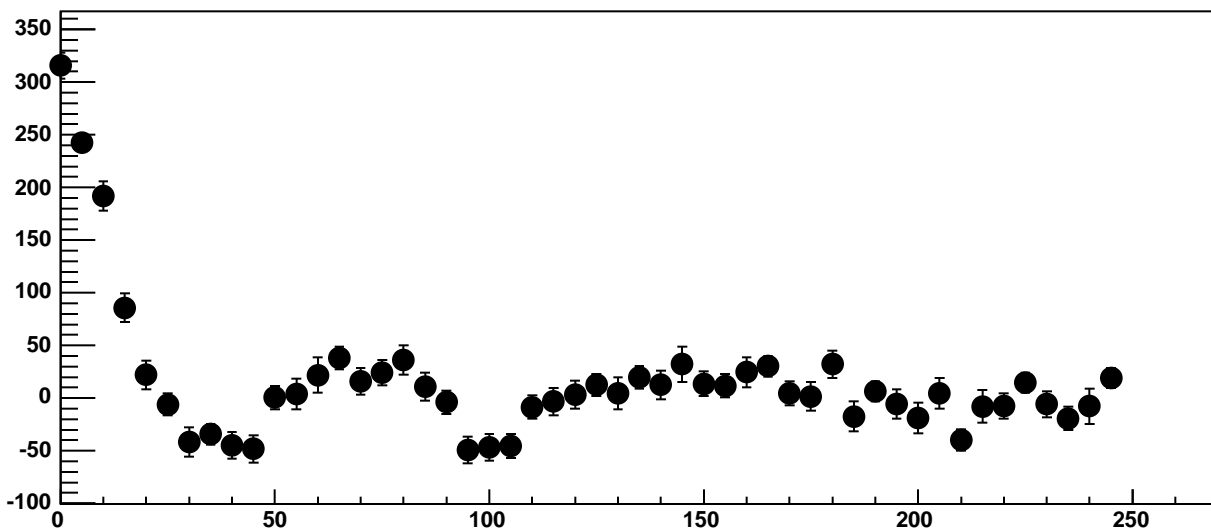
Chip 10, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

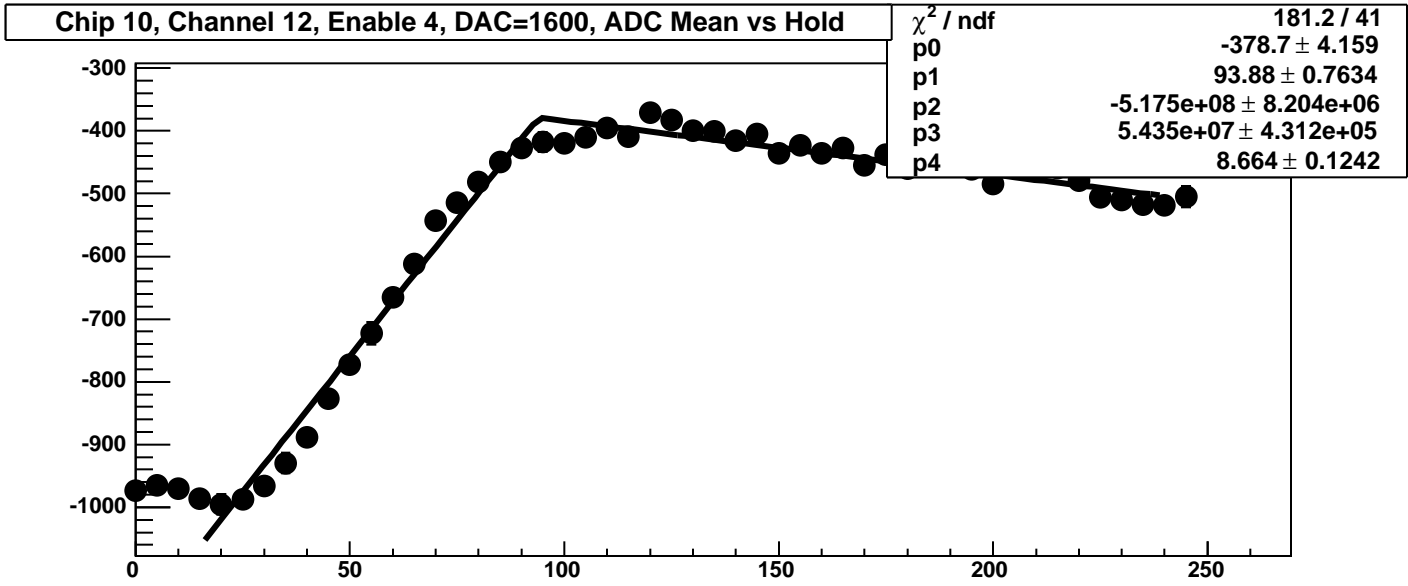


Chip 10, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold

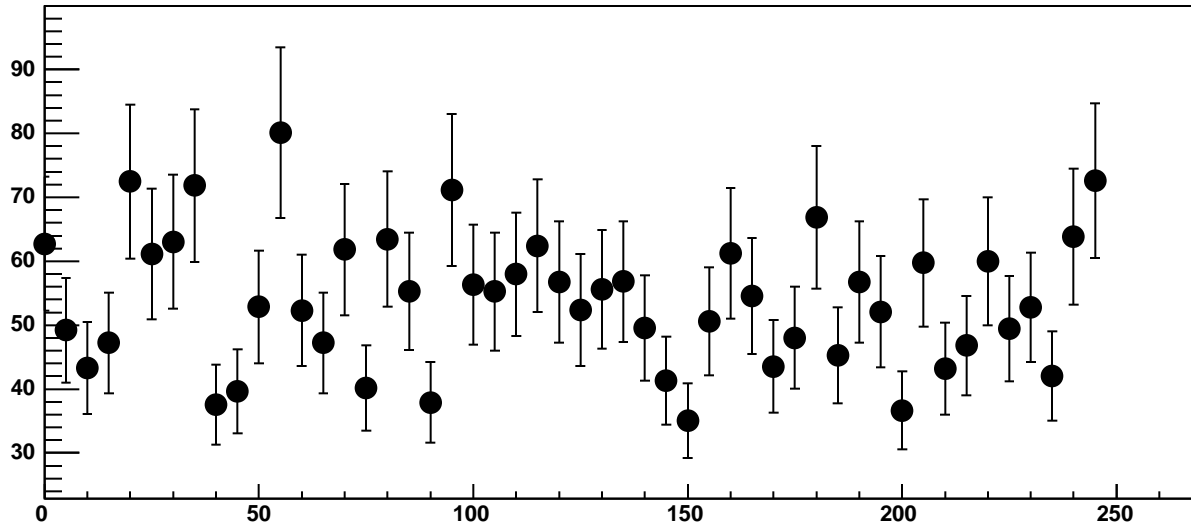


Chip 10, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold

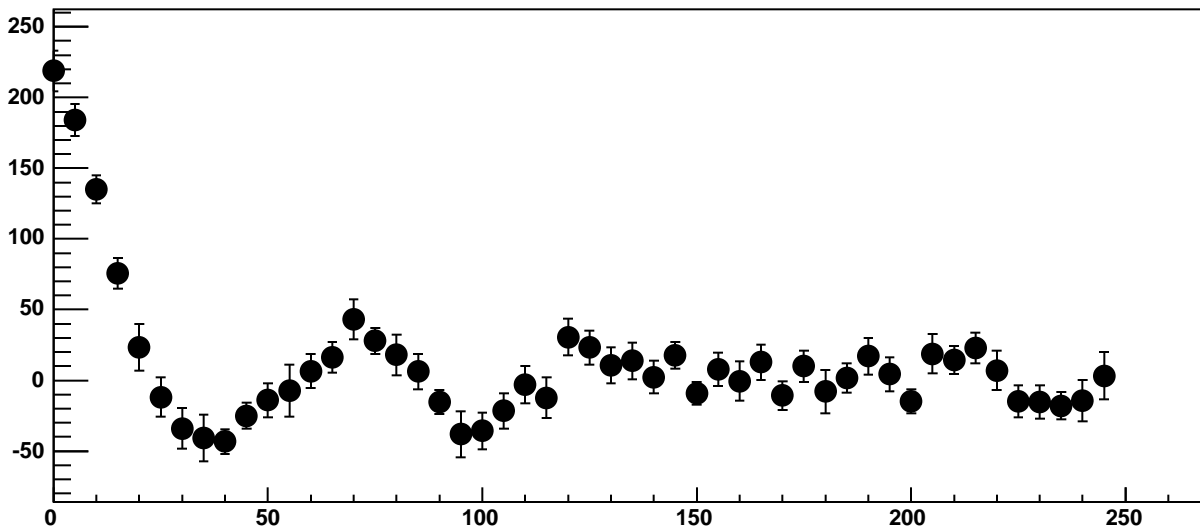




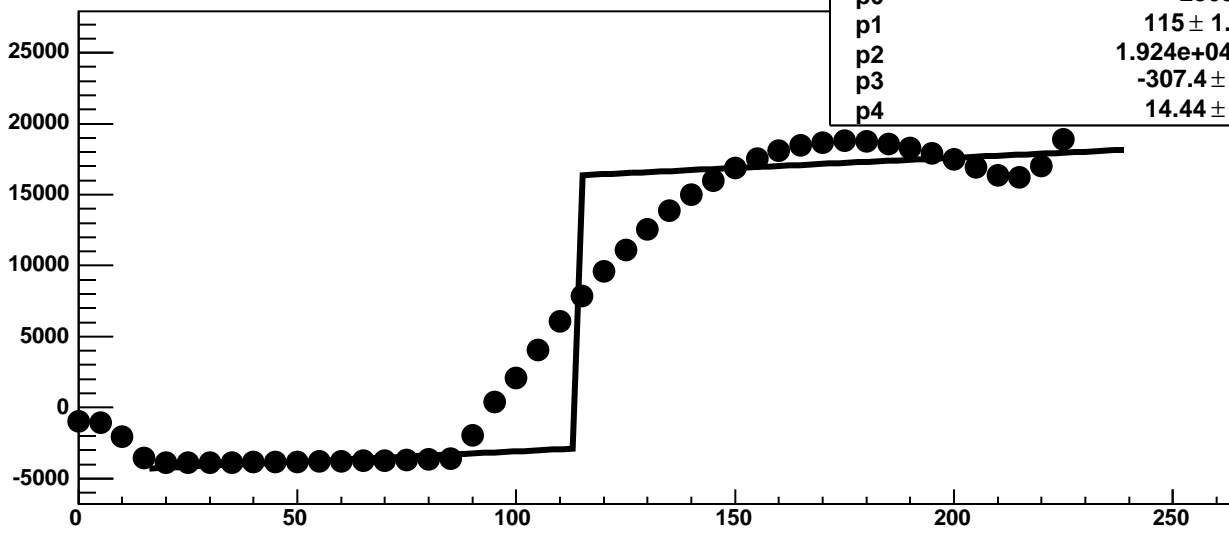
**Chip 10, Channel 12, Enable 4, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 12, Enable 4, DAC=1600, ADC Residuals vs Hold**

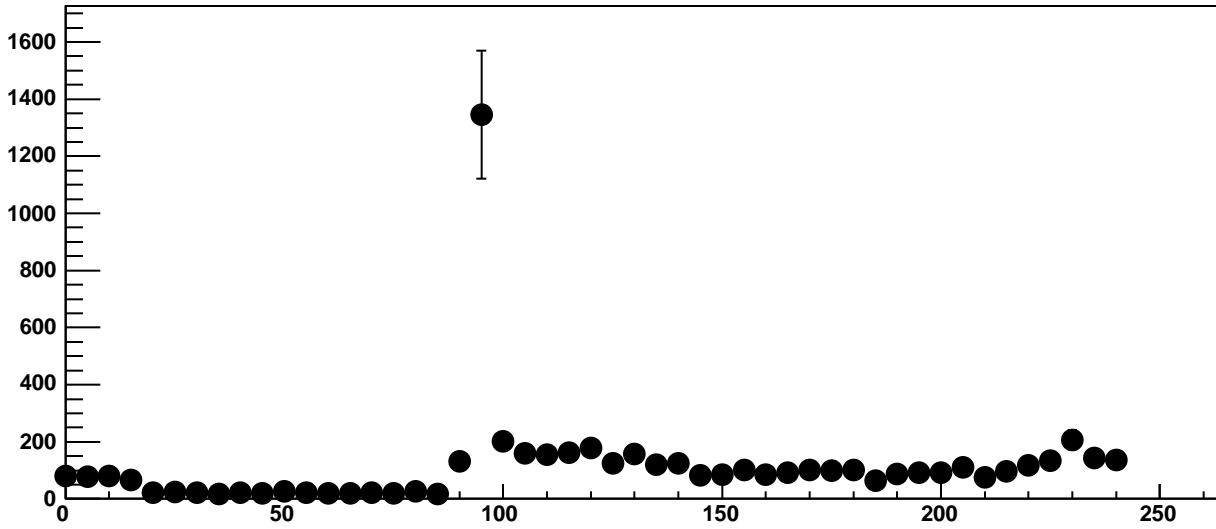


Chip 10, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

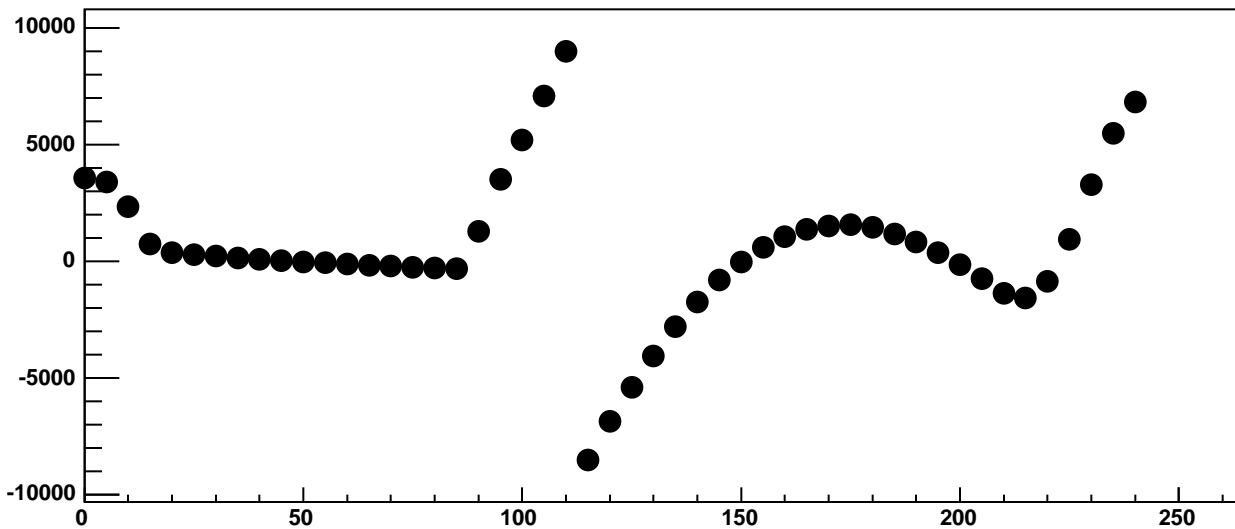


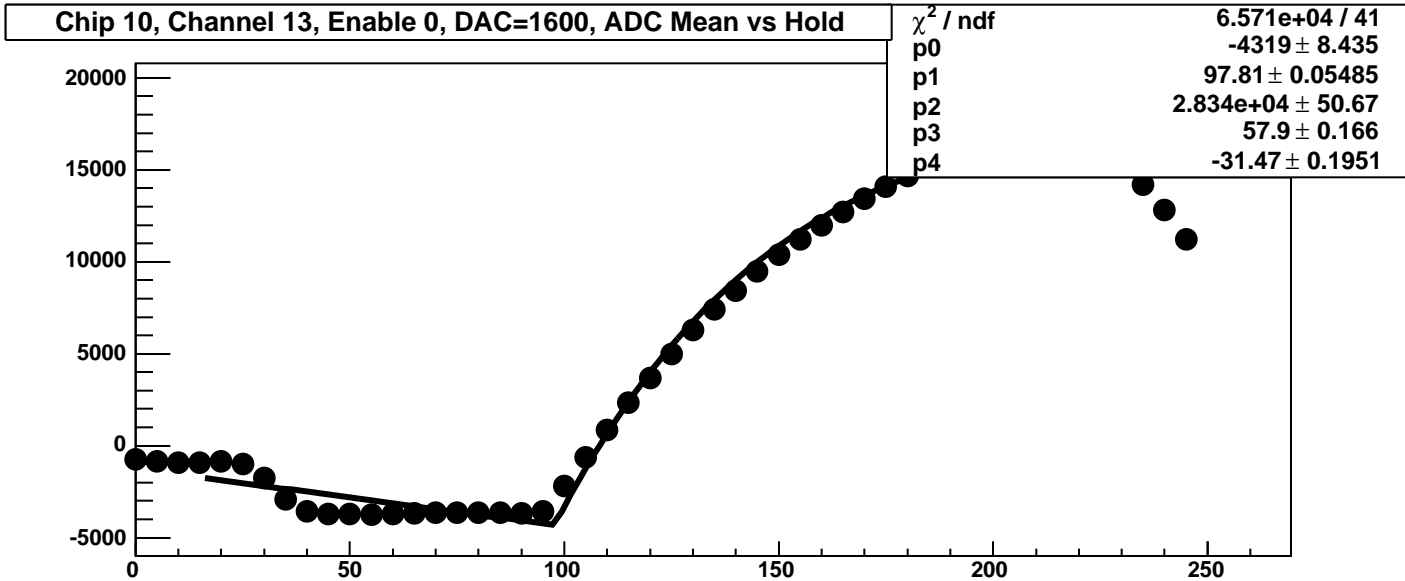
$\chi^2 / \text{ndf}$	4.12e+05 / 41
p0	-2868 ± 2.167
p1	115 ± 1.693e-05
p2	1.924e+04 ± 6.019
p3	-307.4 ± 0.01747
p4	14.44 ± 0.03228

Chip 10, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

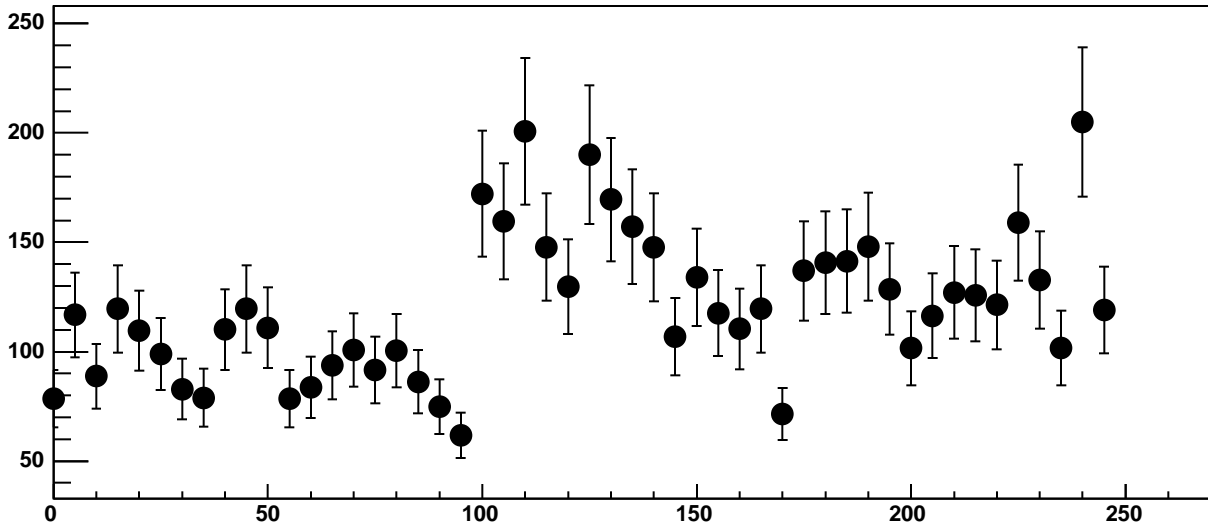


Chip 10, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold

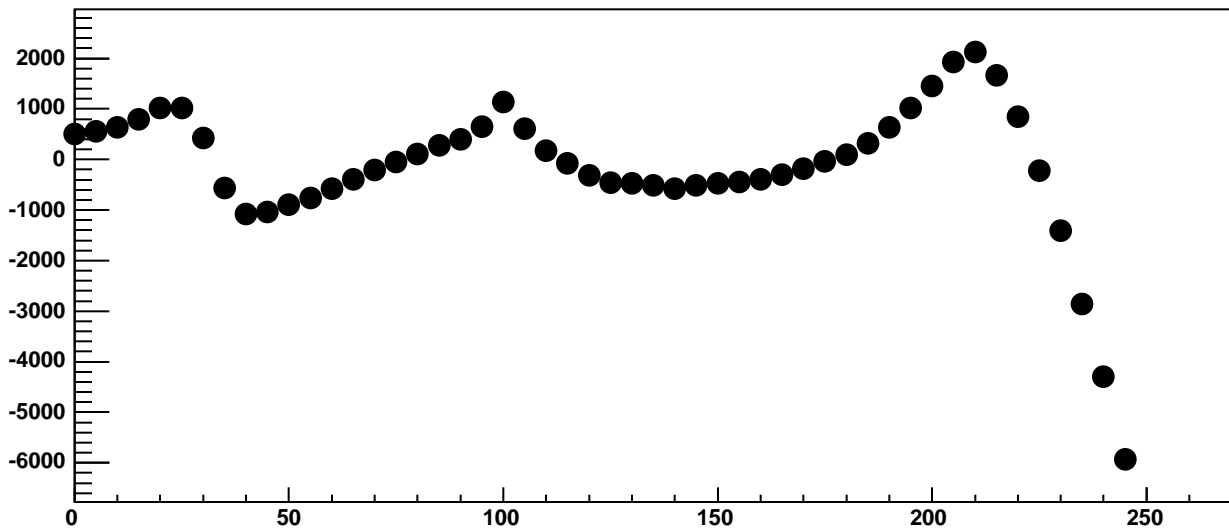




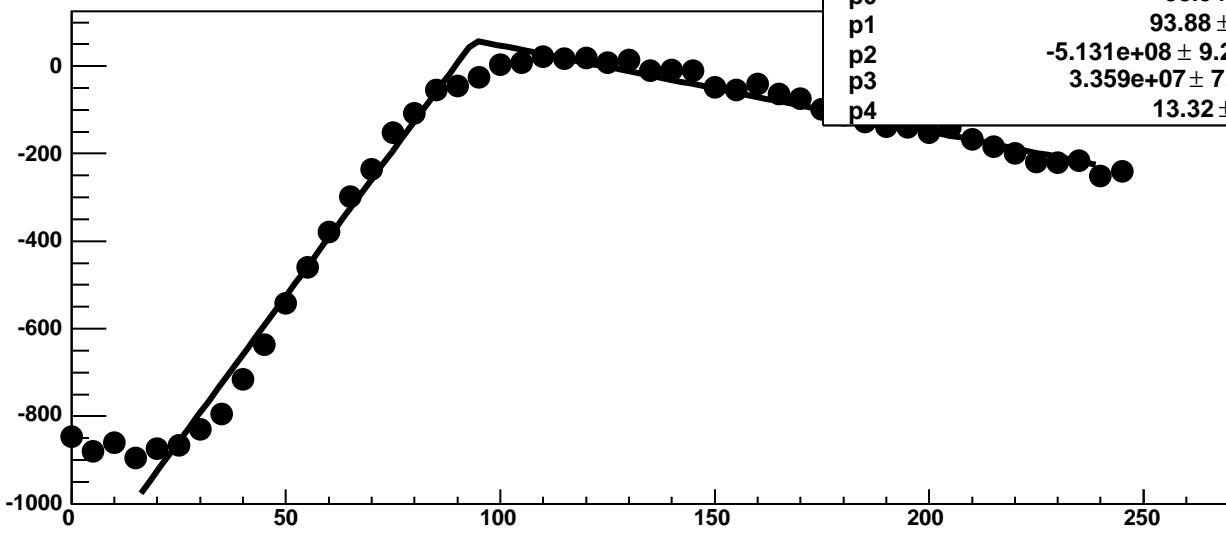
**Chip 10, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold**

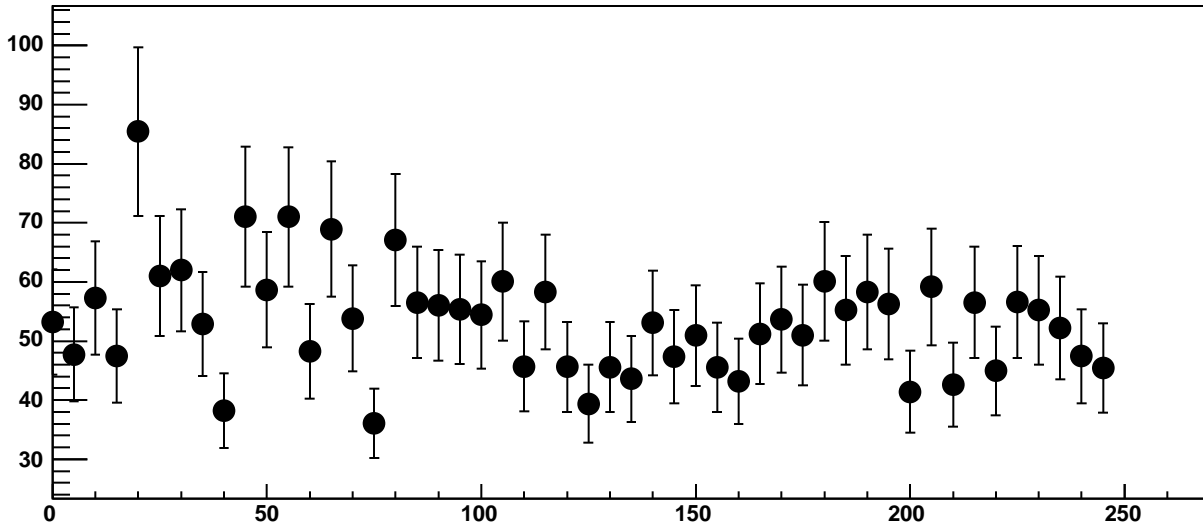


Chip 10, Channel 13, Enable 1, DAC=1600, ADC Mean vs Hold

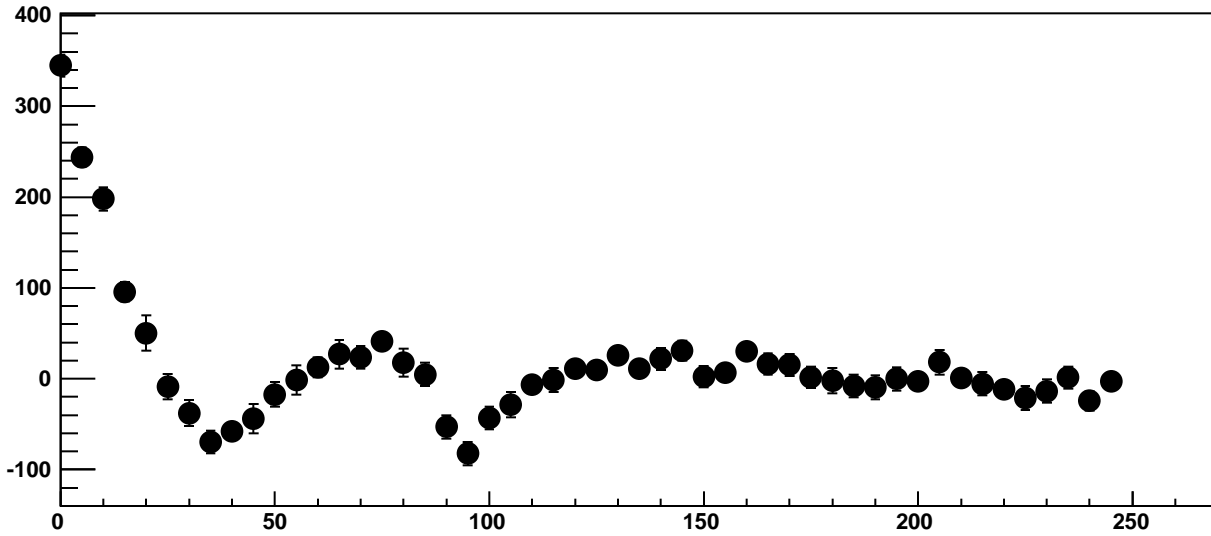


$\chi^2 / \text{ndf}$	335.1 / 41
p0	$58.94 \pm 3.558$
p1	$93.88 \pm 0.4675$
p2	$-5.131\text{e}+08 \pm 9.239\text{e}+06$
p3	$3.359\text{e}+07 \pm 7.19\text{e}+05$
p4	$13.32 \pm 0.1253$

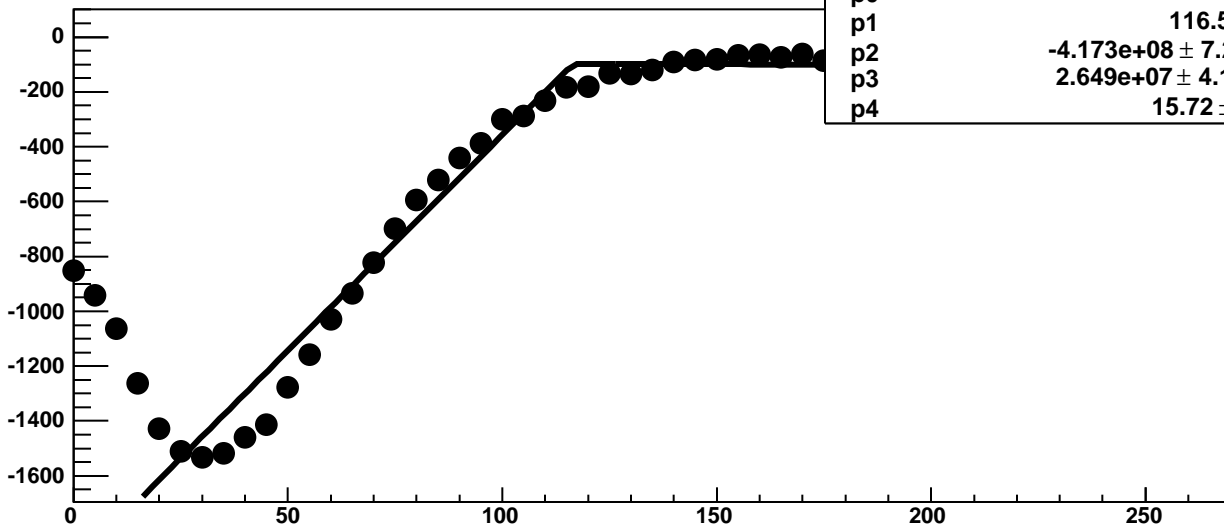
Chip 10, Channel 13, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 13, Enable 1, DAC=1600, ADC Residuals vs Hold

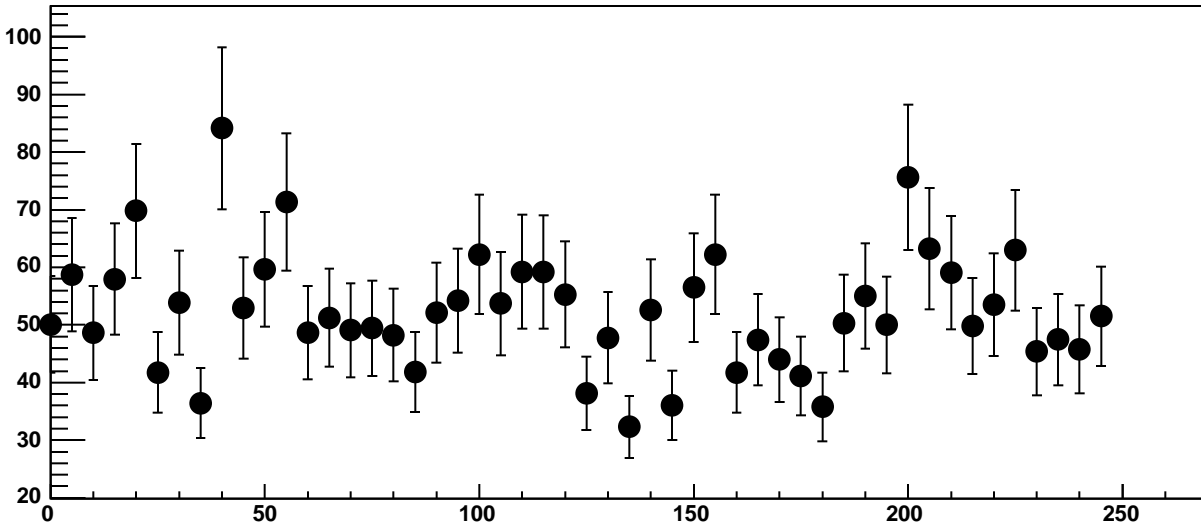


Chip 10, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

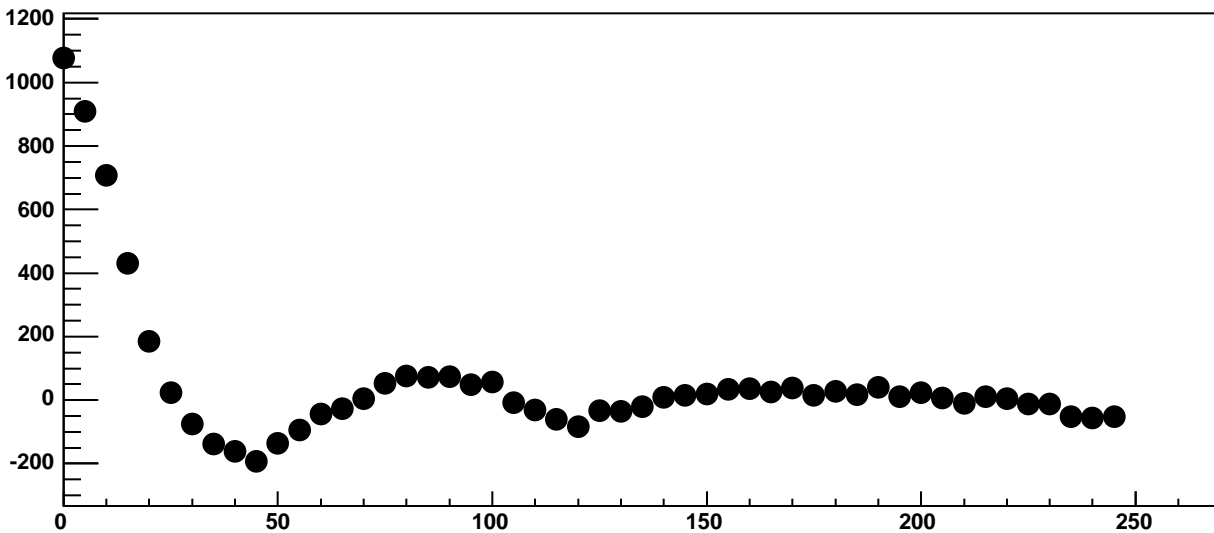


$\chi^2 / \text{ndf}$	2405 / 41
p0	-98.11 ± 4.092
p1	116.5 ± 0.429
p2	-4.173e+08 ± 7.267e+06
p3	2.649e+07 ± 4.175e+05
p4	15.72 ± 0.0894

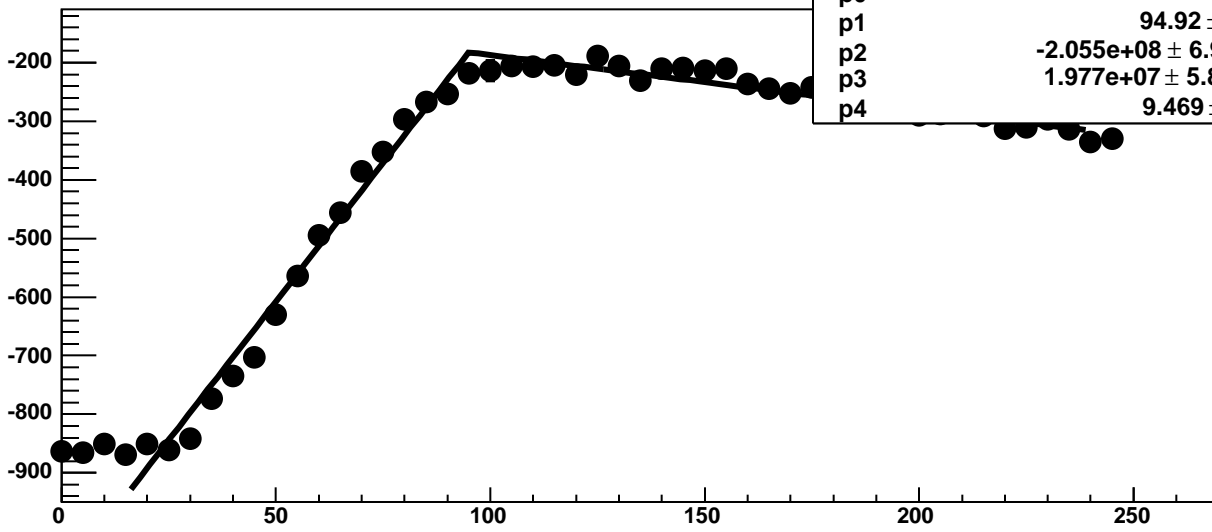
Chip 10, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

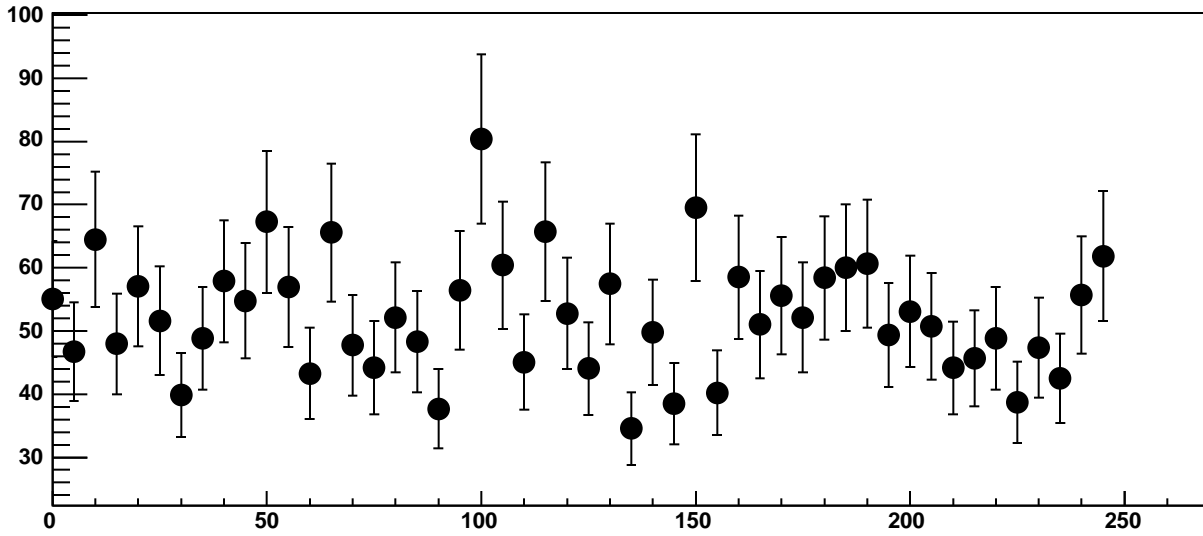


Chip 10, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

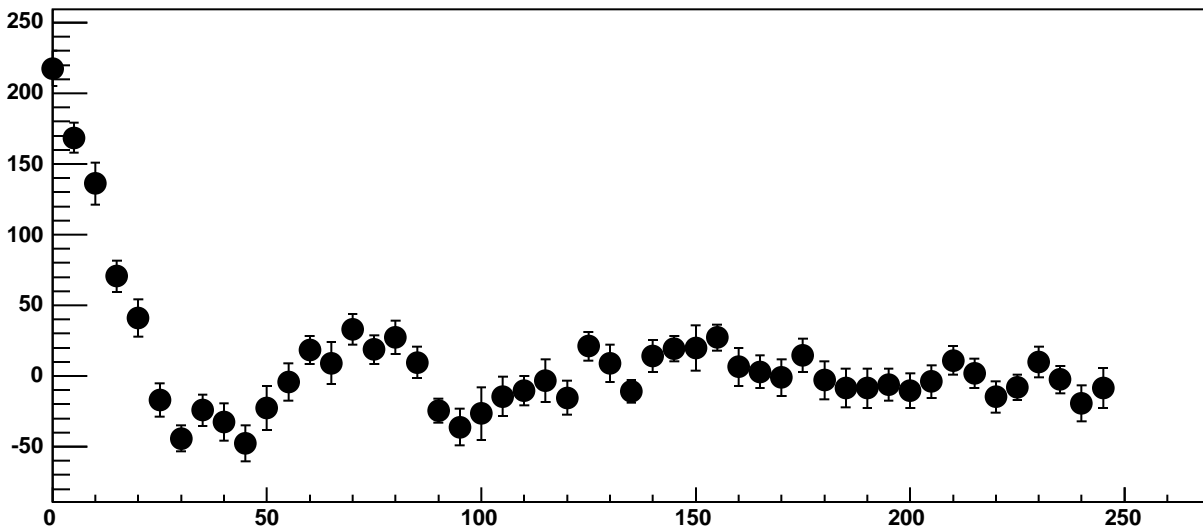


$\chi^2 / \text{ndf}$	181.6 / 41
p0	-182.3 ± 3.968
p1	94.92 ± 0.6744
p2	-2.055e+08 ± 6.958e+06
p3	1.977e+07 ± 5.812e+05
p4	9.469 ± 0.1176

Chip 10, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold

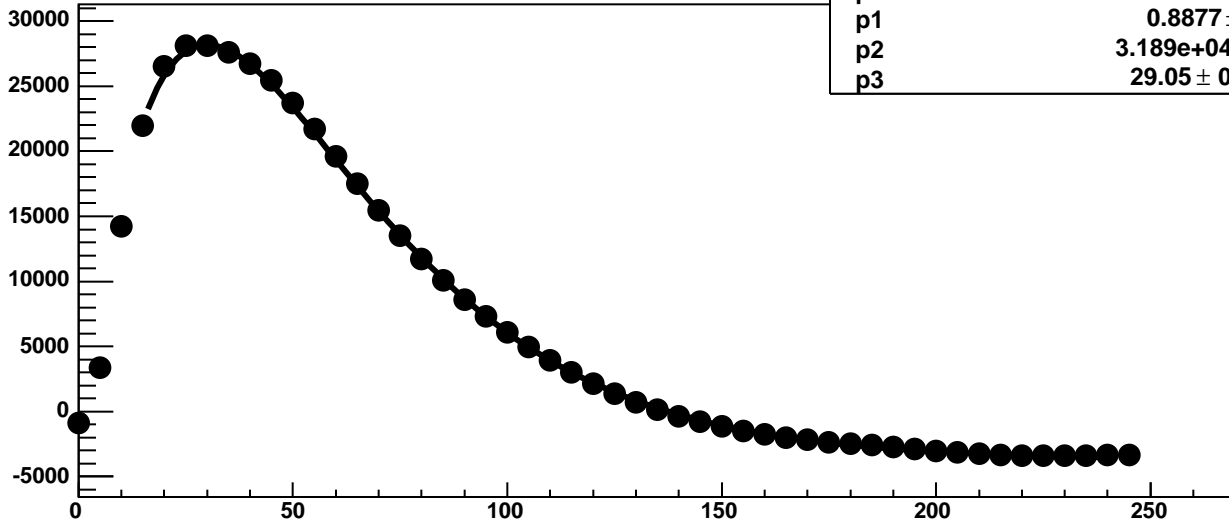


Chip 10, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

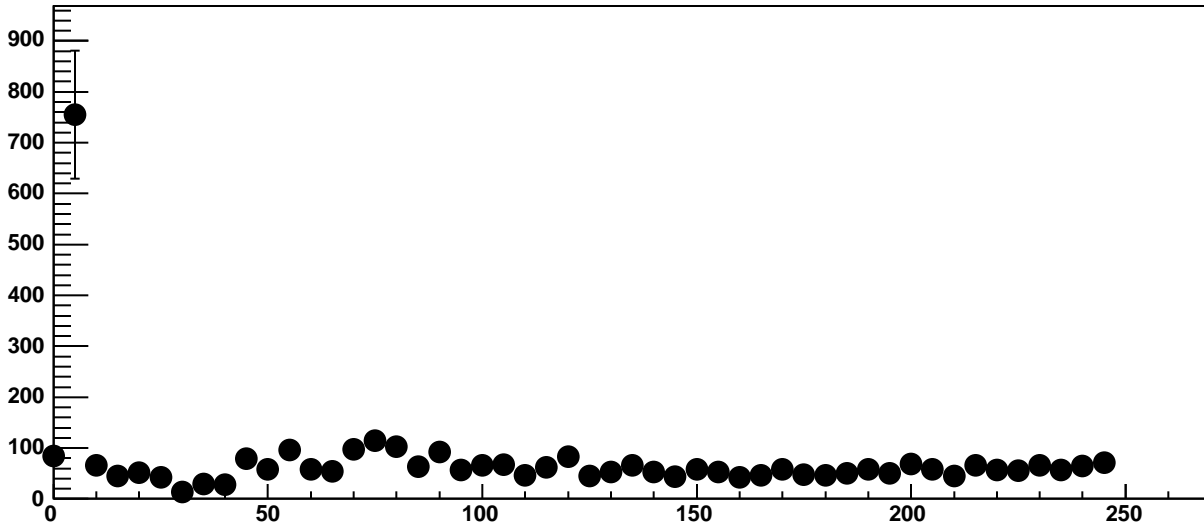




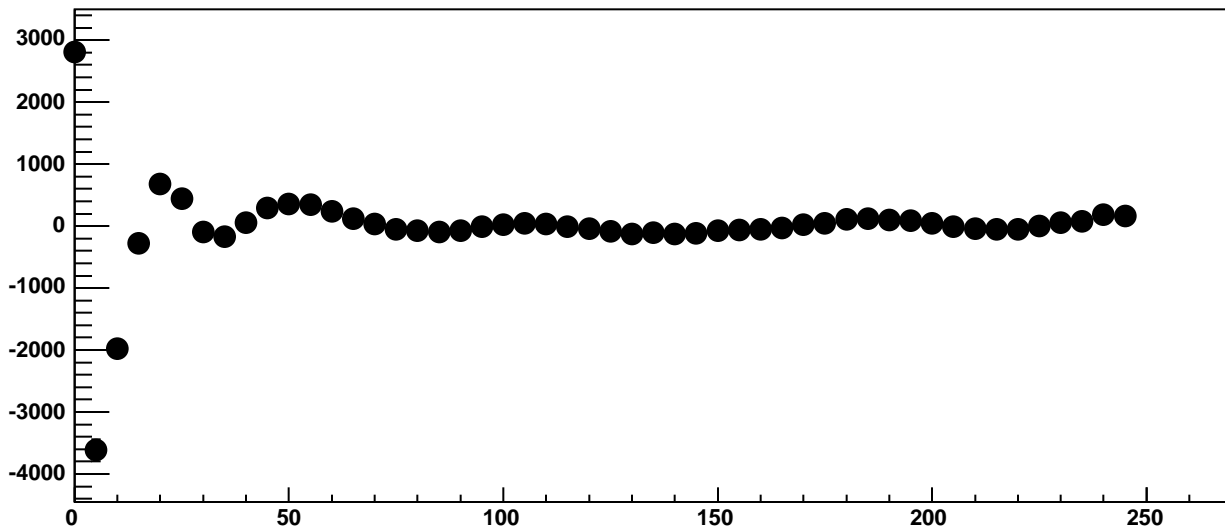
Chip 10, Channel 13, Enable 4!, DAC=1600, ADC Mean vs Hold



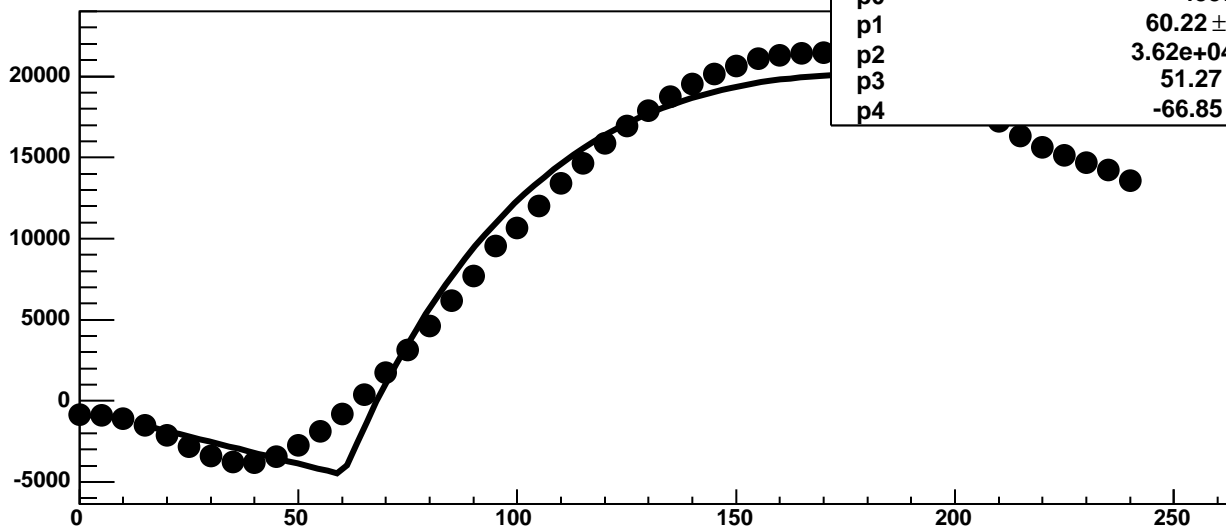
Chip 10, Channel 13, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 13, Enable 4!, DAC=1600, ADC Residuals vs Hold

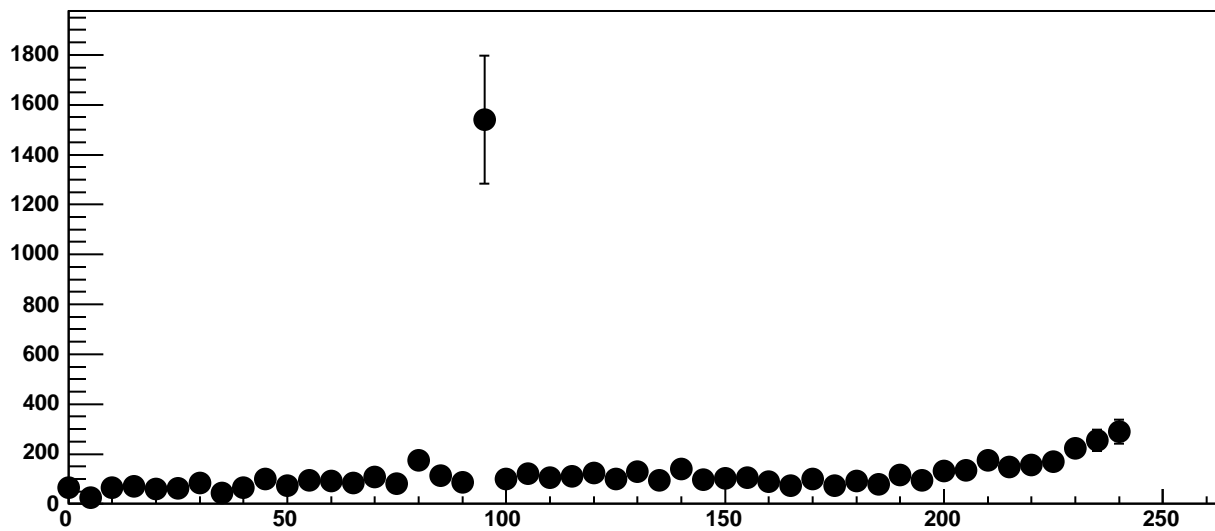


Chip 10, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

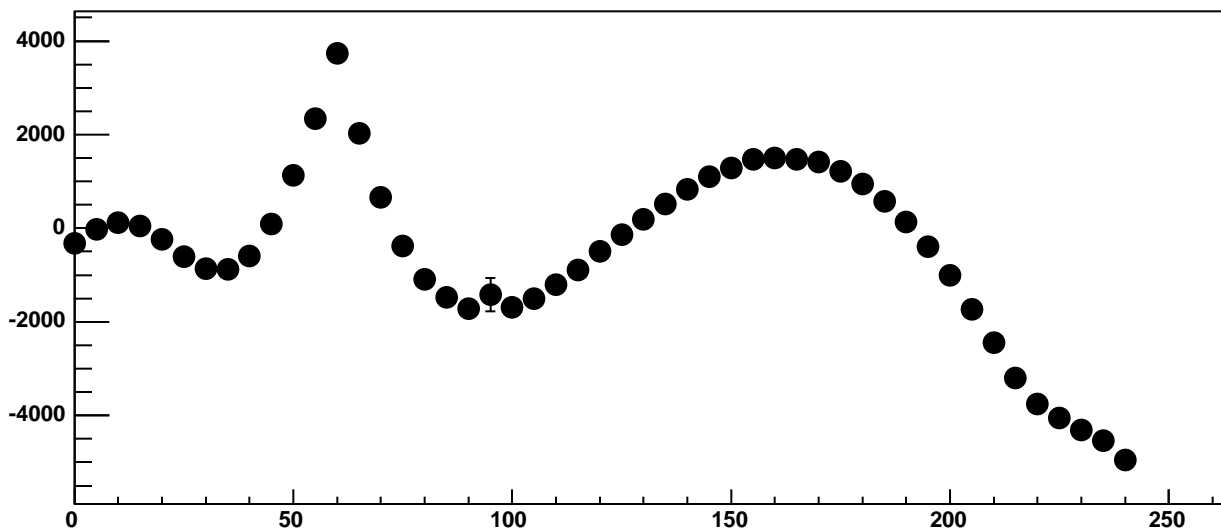


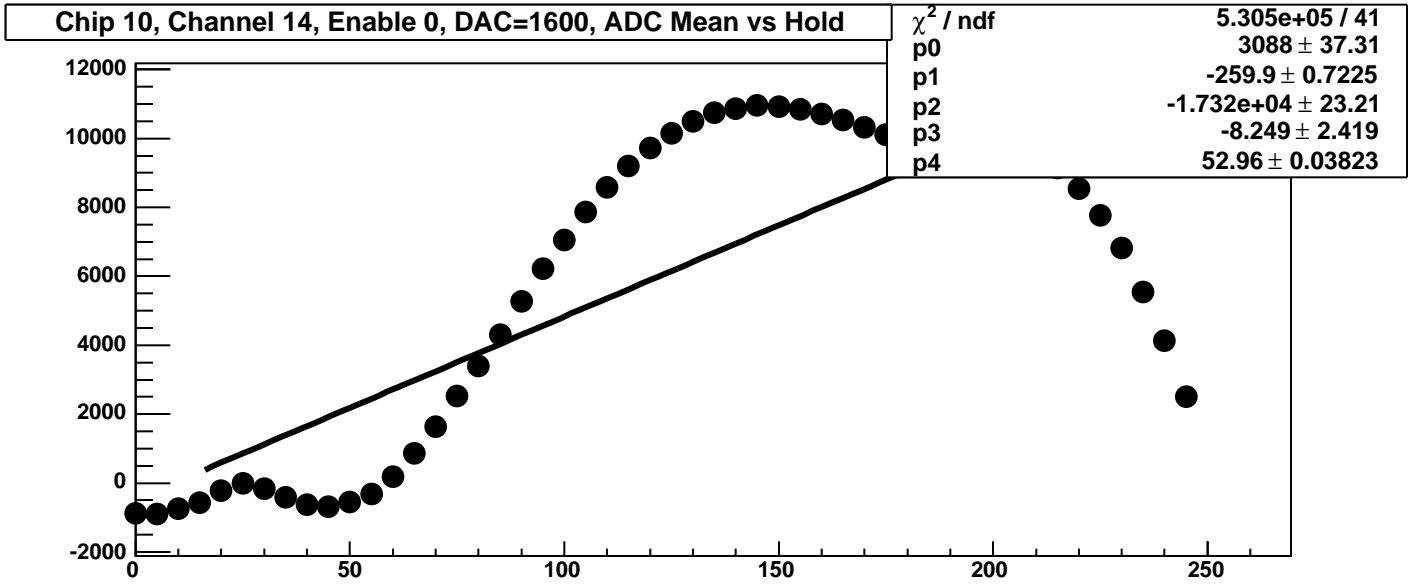
$\chi^2 / \text{ndf}$	1.897e+05 / 41
p0	-4557 ± 8.337
p1	60.22 ± 0.02635
p2	3.62e+04 ± 60.79
p3	51.27 ± 0.0923
p4	-66.85 ± 0.2979

Chip 10, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold

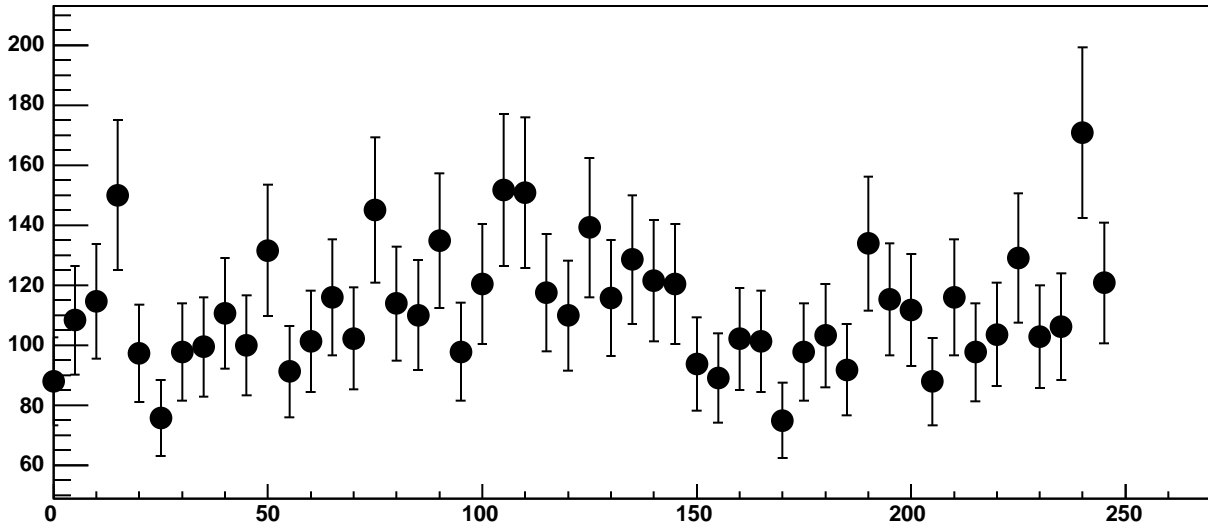


Chip 10, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold

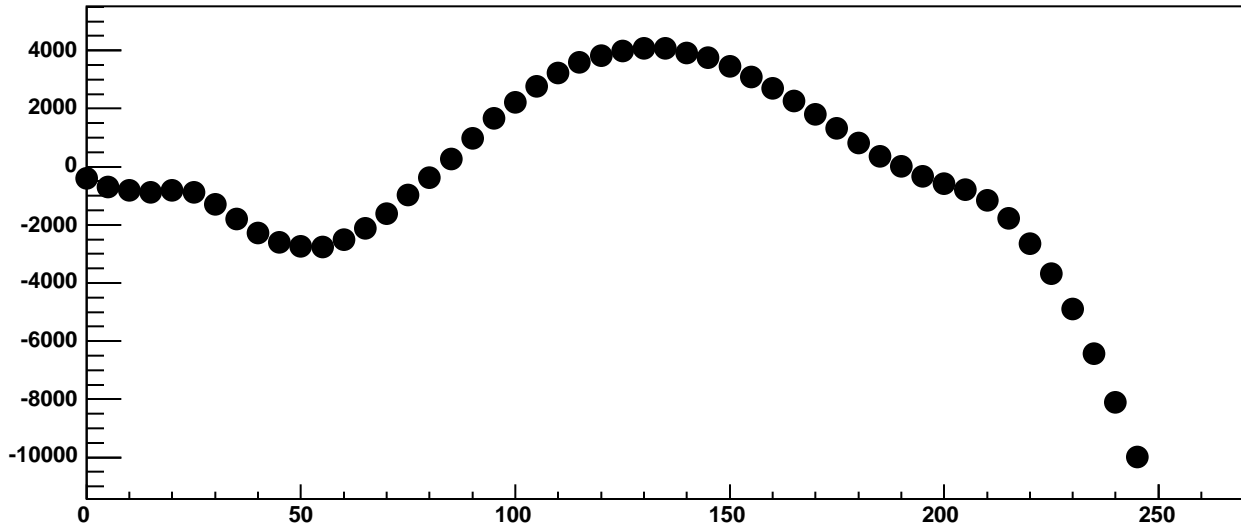




**Chip 10, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold**

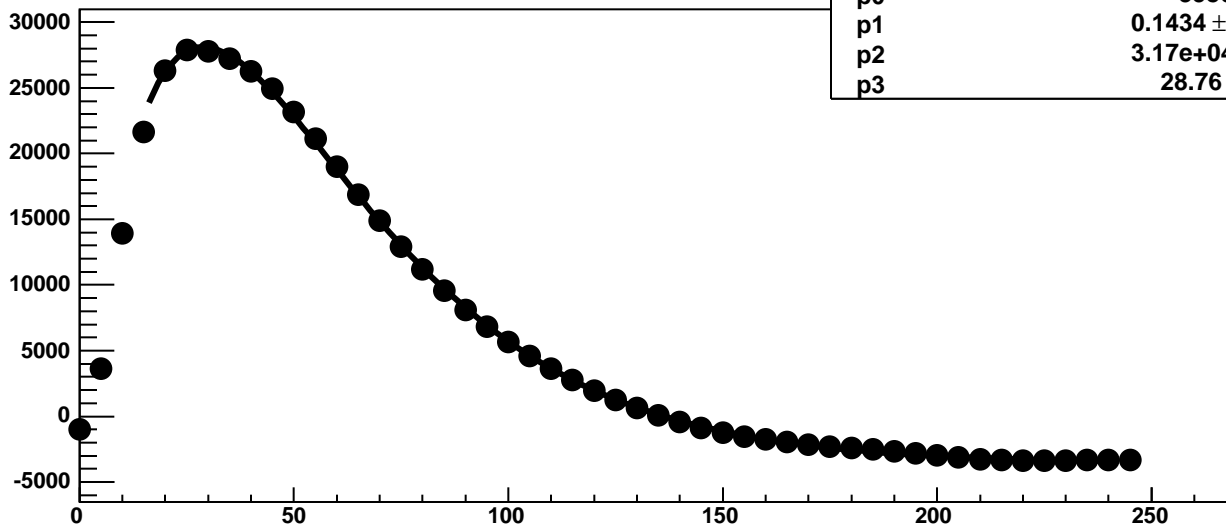


**Chip 10, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold**

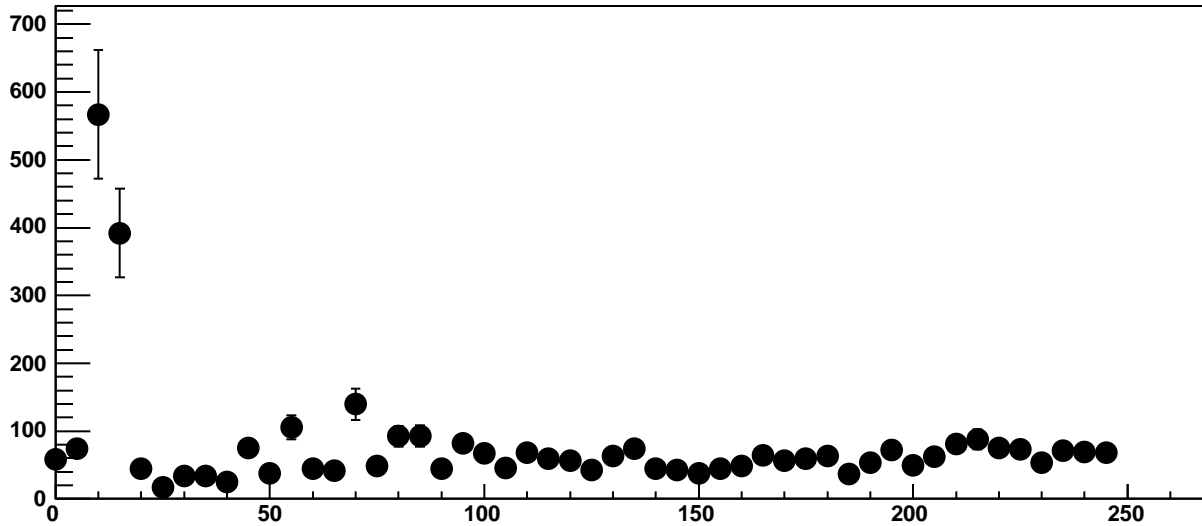


Chip 10, Channel 14, Enable 1!, DAC=1600, ADC Mean vs Hold

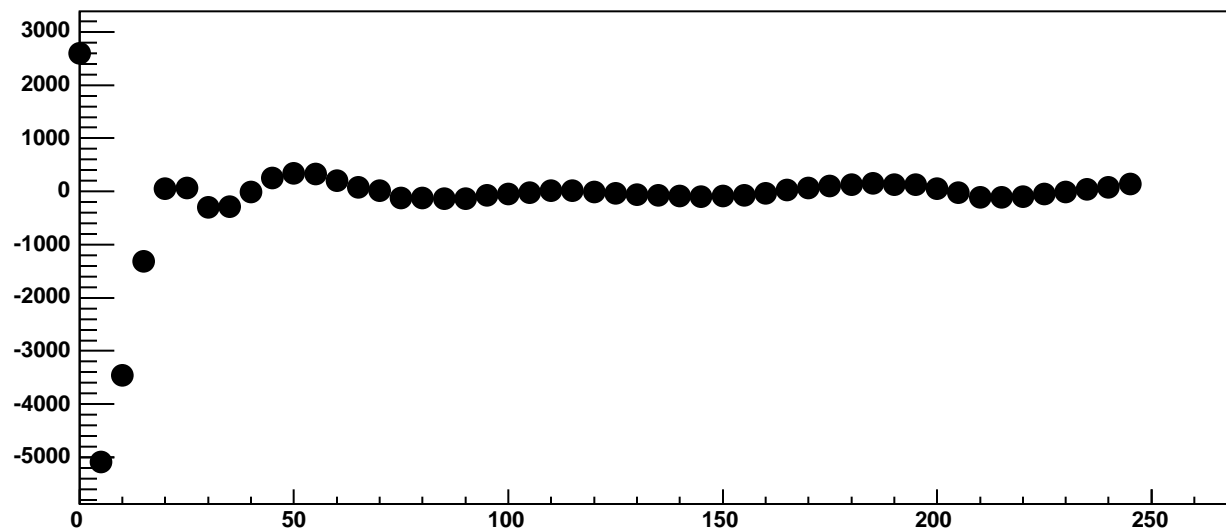
$\chi^2 / \text{ndf}$	7560 / 42
p0	-3586 ± 3.862
p1	0.1434 ± 0.01973
p2	3.17e+04 ± 4.213
p3	28.76 ± 0.0115



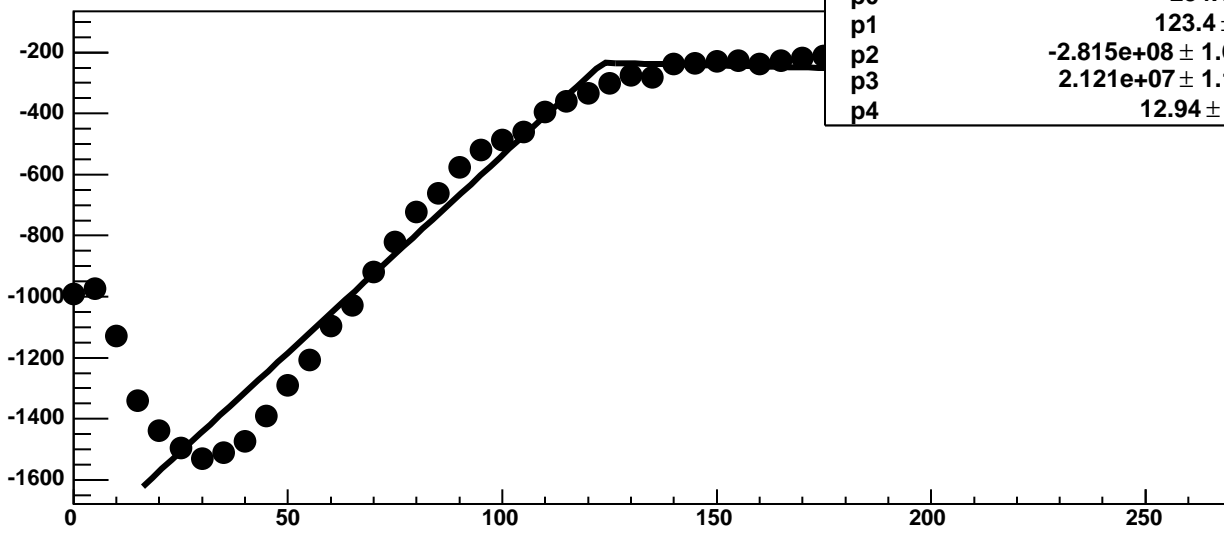
Chip 10, Channel 14, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 14, Enable 1!, DAC=1600, ADC Residuals vs Hold

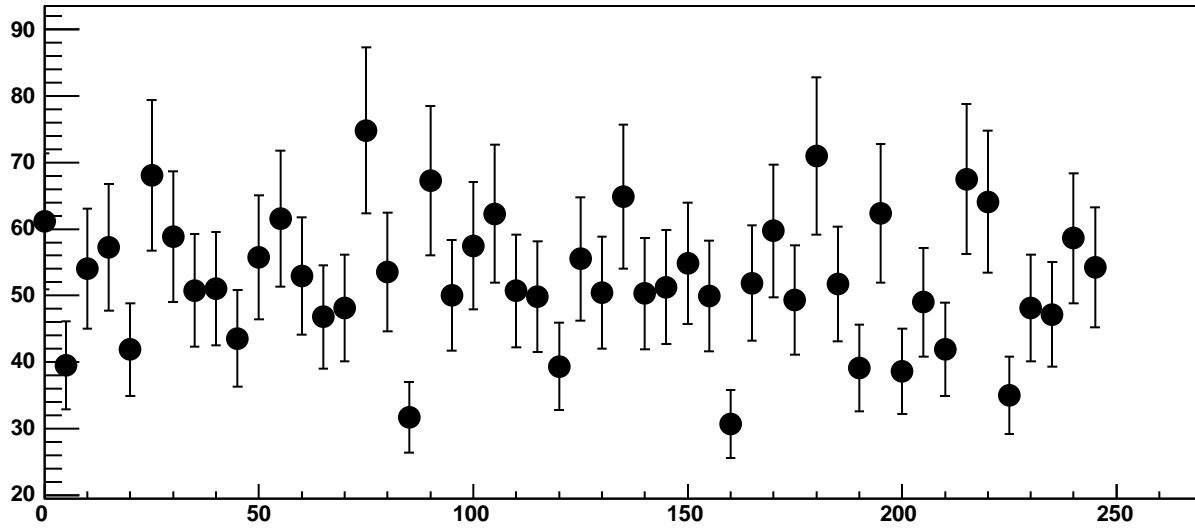


Chip 10, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

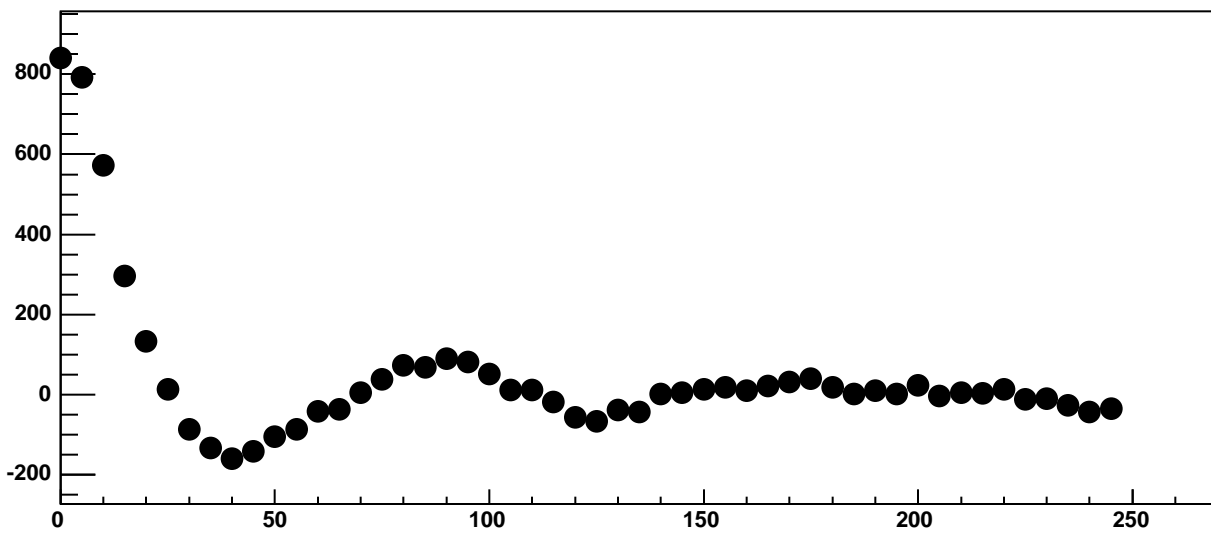


$\chi^2 / \text{ndf}$	1772 / 41
p0	-234.1 ± 4.478
p1	123.4 ± 0.4982
p2	-2.815e+08 ± 1.614e+07
p3	2.121e+07 ± 1.171e+06
p4	12.94 ± 0.07557

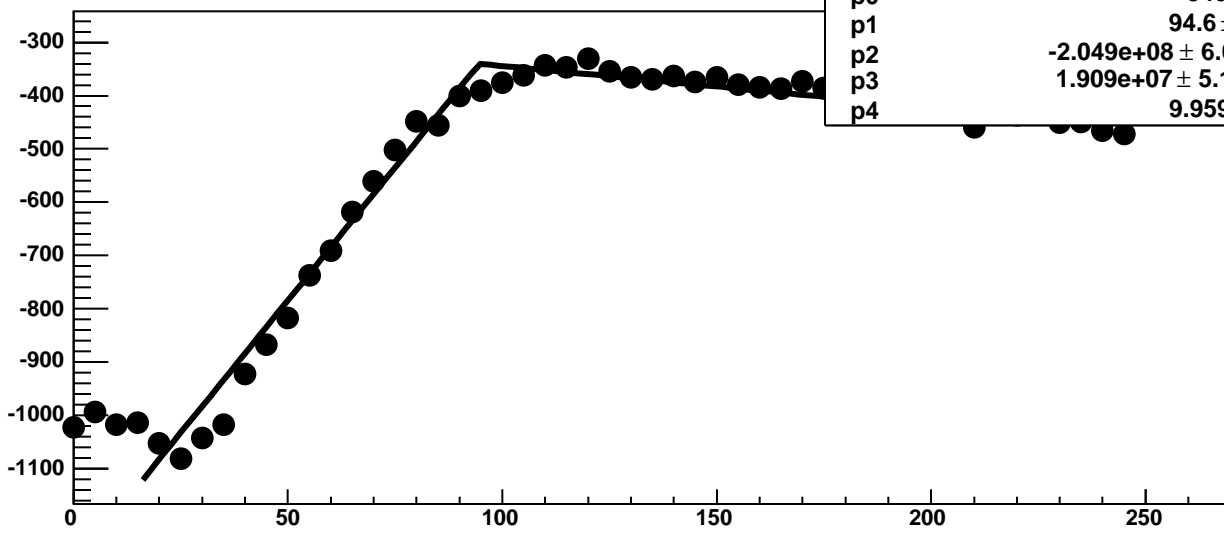
Chip 10, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

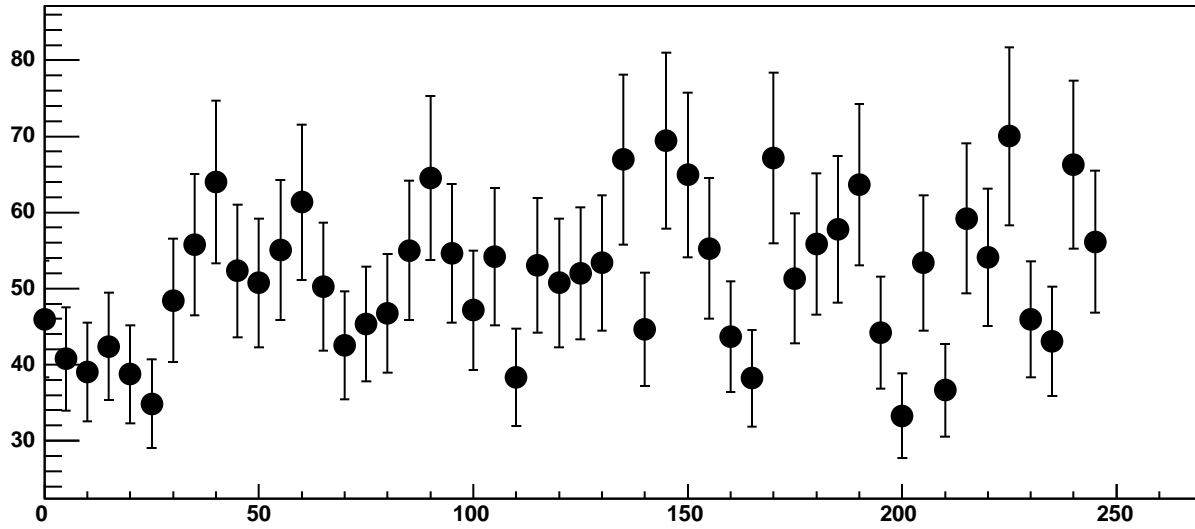


Chip 10, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

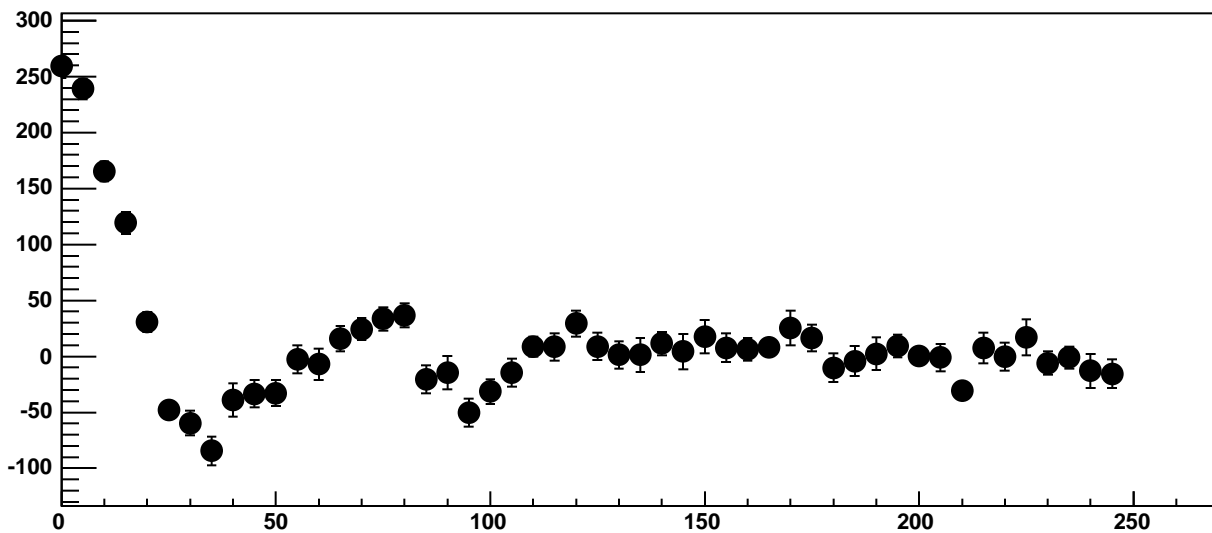


$\chi^2 / \text{ndf}$	388.1 / 41
p0	$-340 \pm 3.866$
p1	$94.6 \pm 0.6799$
p2	$-2.049\text{e}+08 \pm 6.069\text{e}+06$
p3	$1.909\text{e}+07 \pm 5.182\text{e}+05$
p4	$9.959 \pm 0.116$

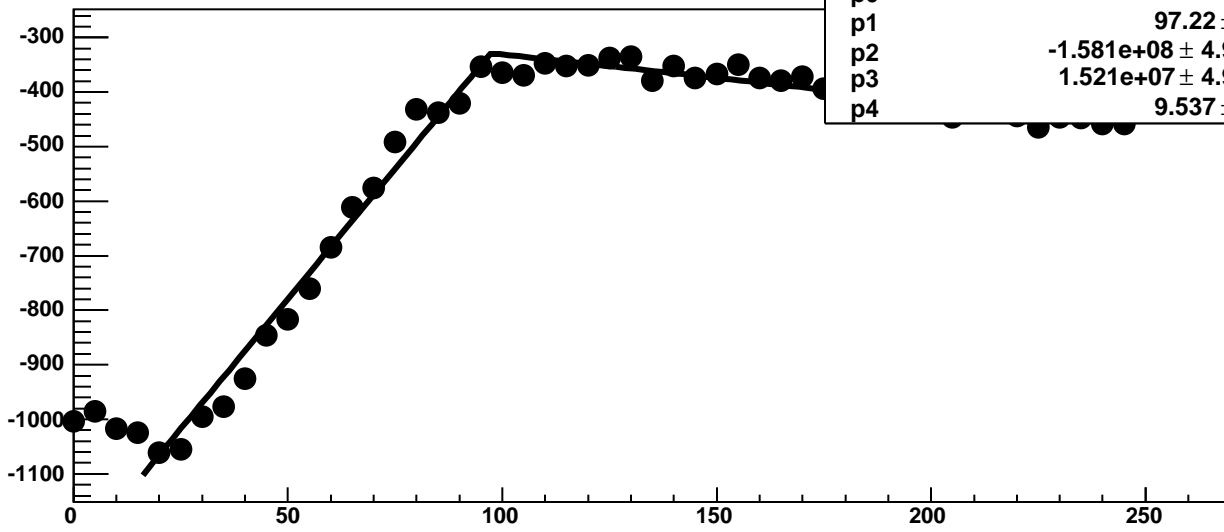
Chip 10, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

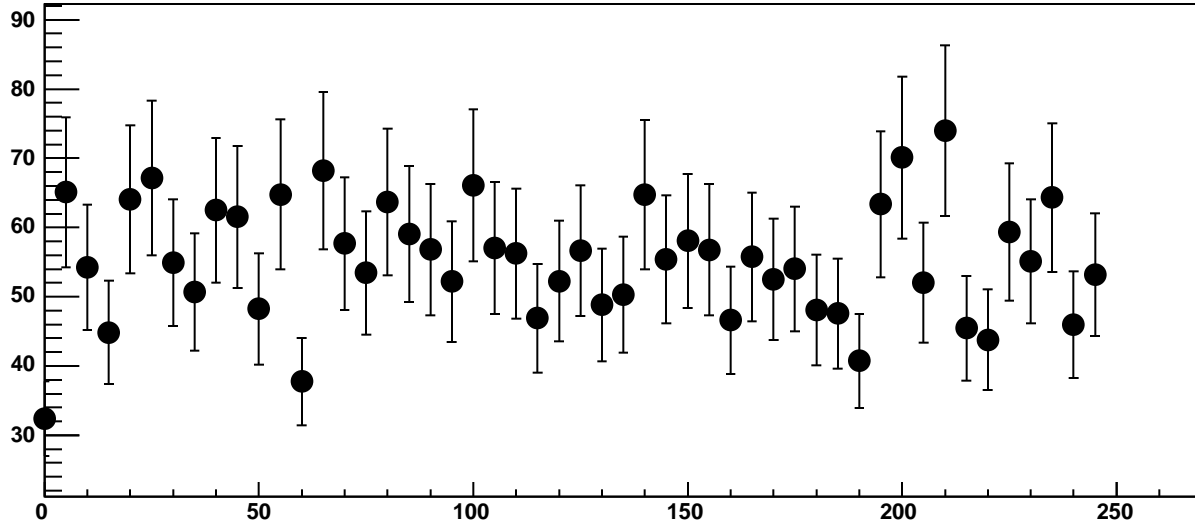


Chip 10, Channel 14, Enable 4, DAC=1600, ADC Mean vs Hold

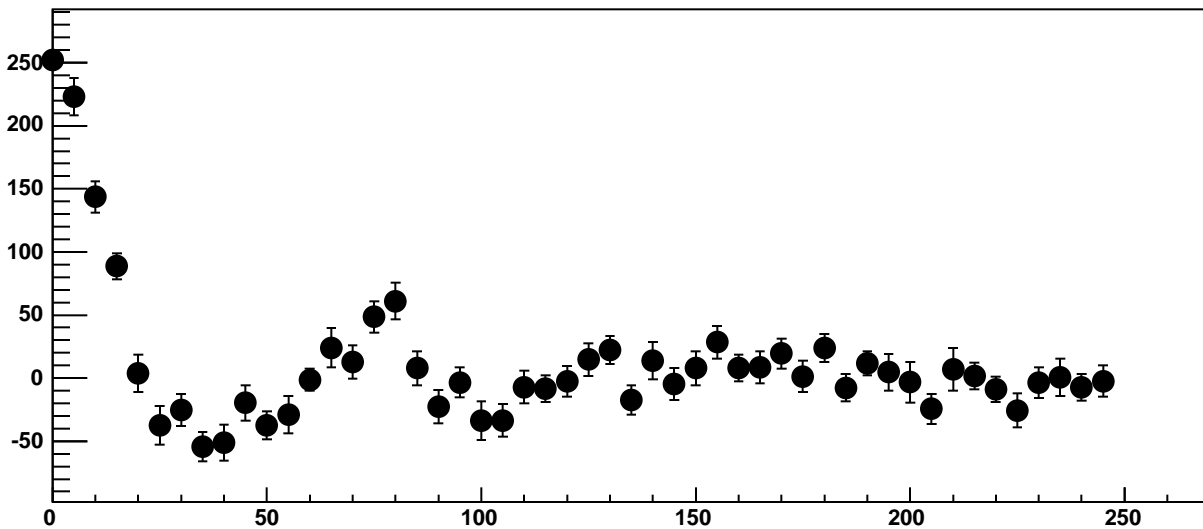


$\chi^2 / \text{ndf}$	221.5 / 41
p0	$-328.7 \pm 4.219$
p1	$97.22 \pm 0.7048$
p2	$-1.581\text{e}+08 \pm 4.922\text{e}+06$
p3	$1.521\text{e}+07 \pm 4.911\text{e}+05$
p4	$9.537 \pm 0.1148$

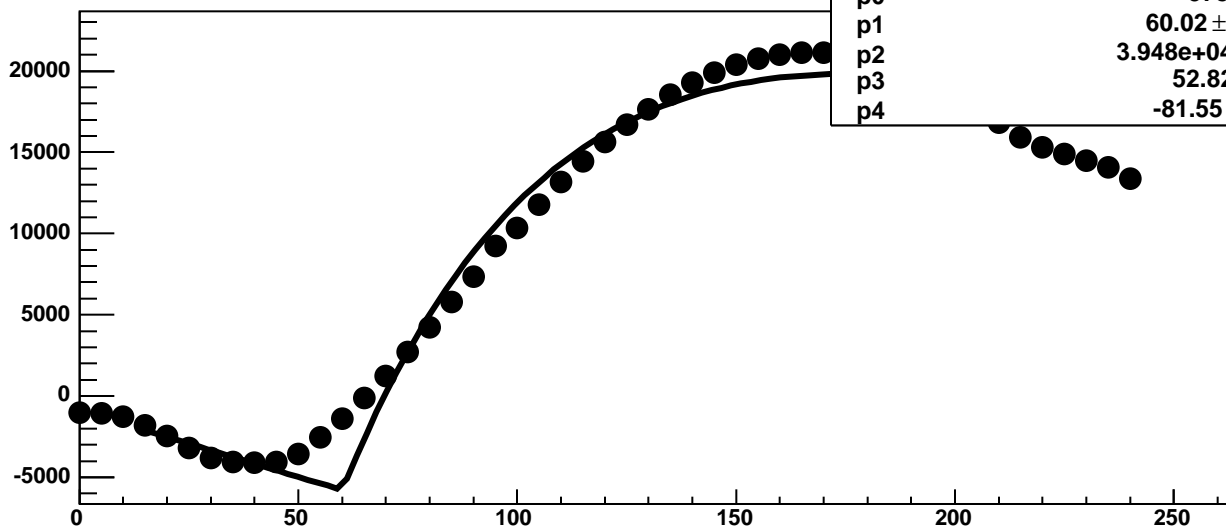
Chip 10, Channel 14, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 14, Enable 4, DAC=1600, ADC Residuals vs Hold

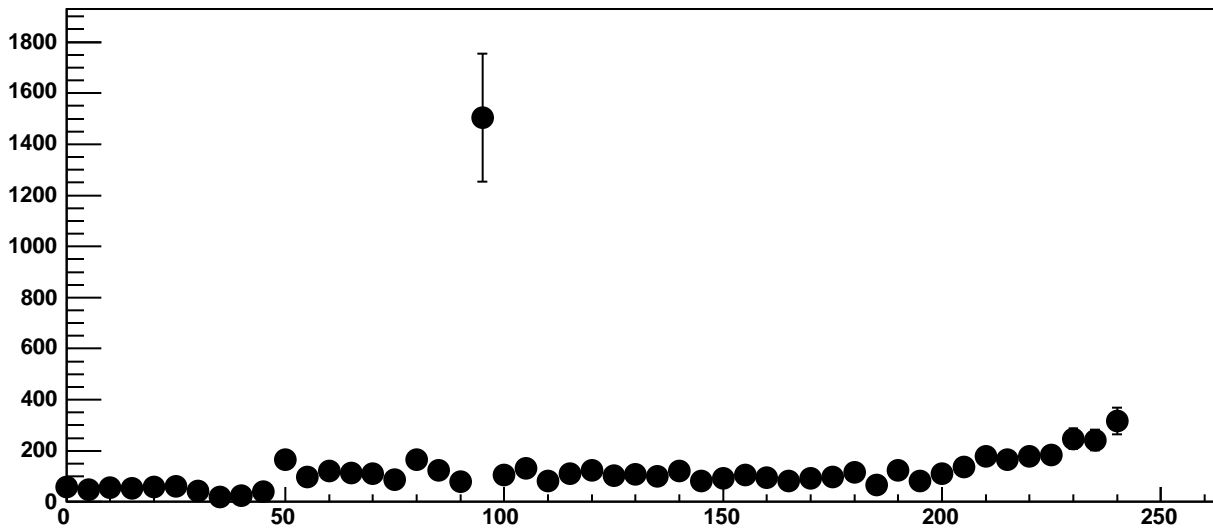


Chip 10, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

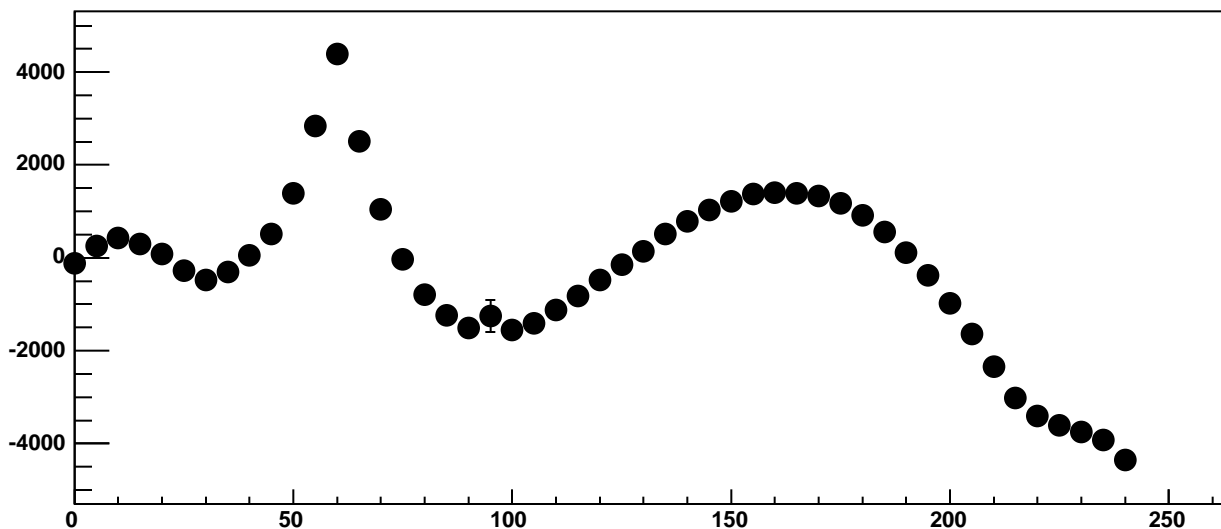


$\chi^2 / \text{ndf}$	1.563e+05 / 41
p0	-5789 ± 6.94
p1	60.02 ± 0.02867
p2	3.948e+04 ± 60.63
p3	52.82 ± 0.093
p4	-81.55 ± 0.2877

Chip 10, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold

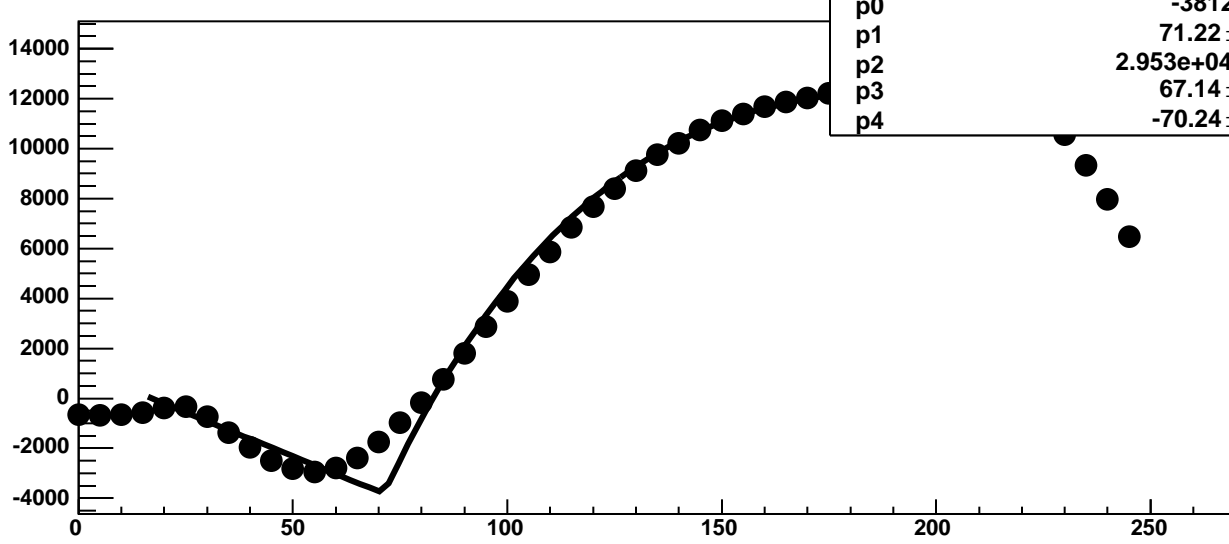


Chip 10, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold



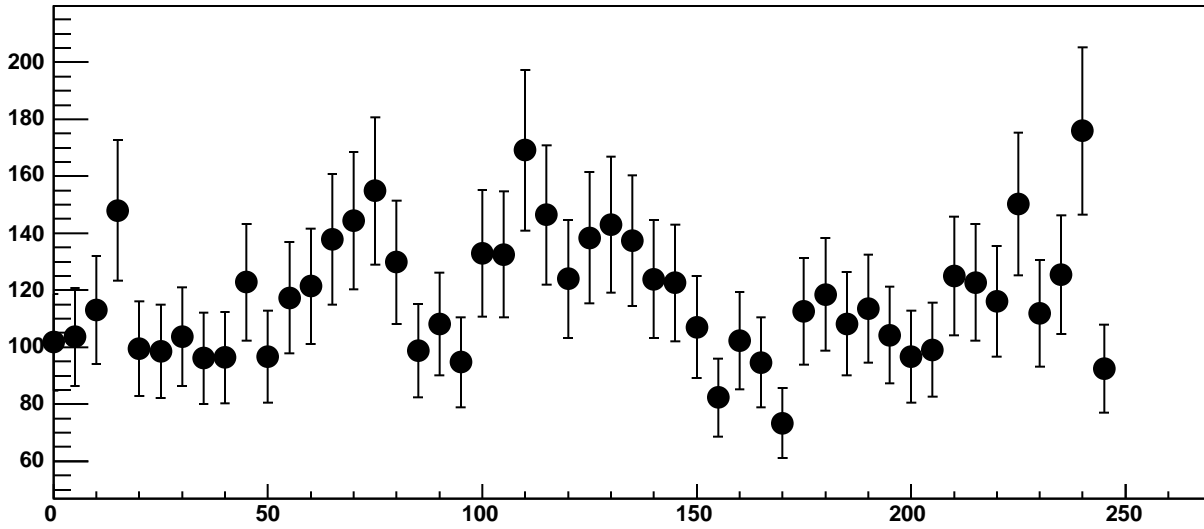


Chip 10, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

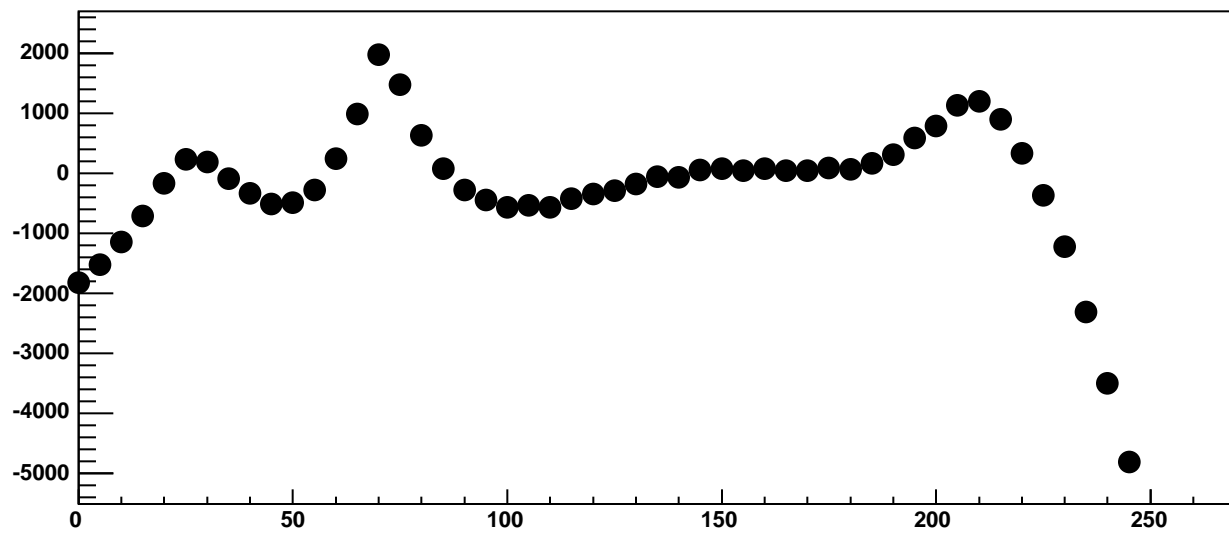


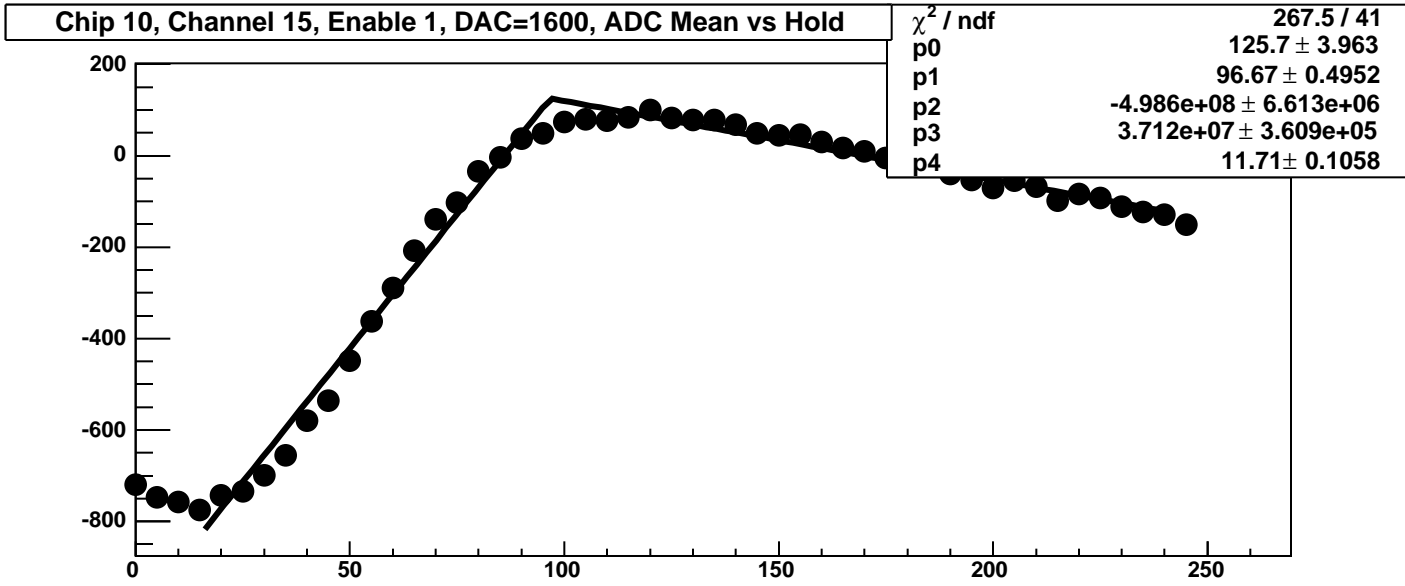
$\chi^2 / \text{ndf}$	3.438e+04 / 41
p0	-3812 ± 12.42
p1	71.22 ± 0.0593
p2	2.953e+04 ± 104.6
p3	67.14 ± 0.2359
p4	-70.24 ± 0.4158

Chip 10, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold

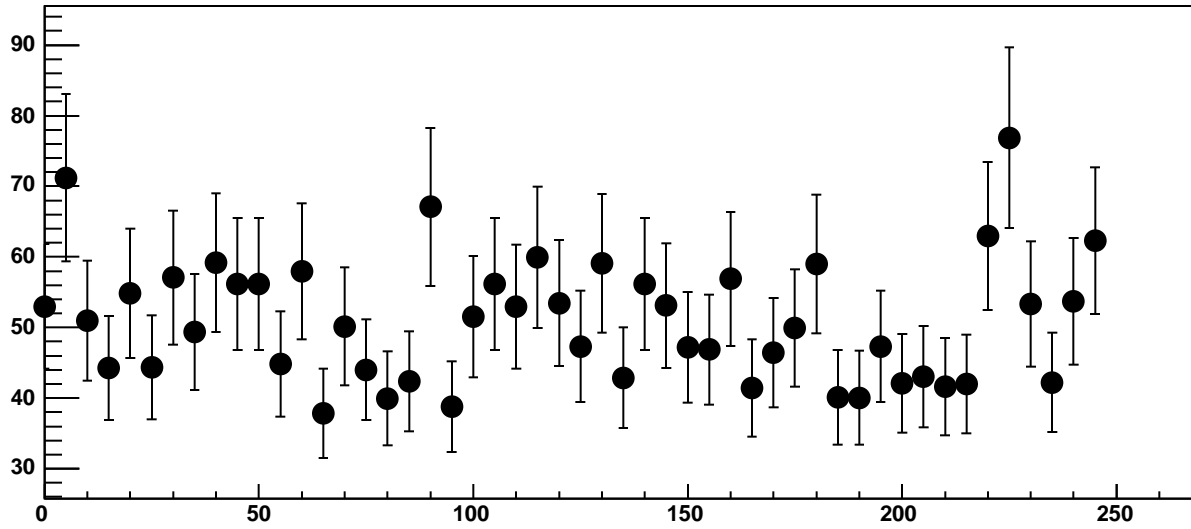


Chip 10, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

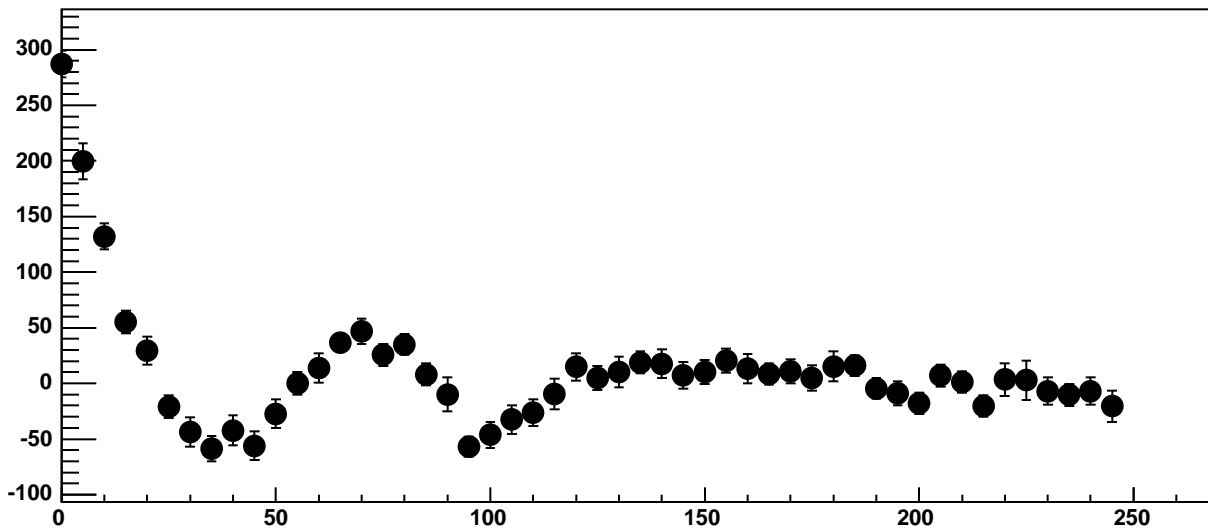




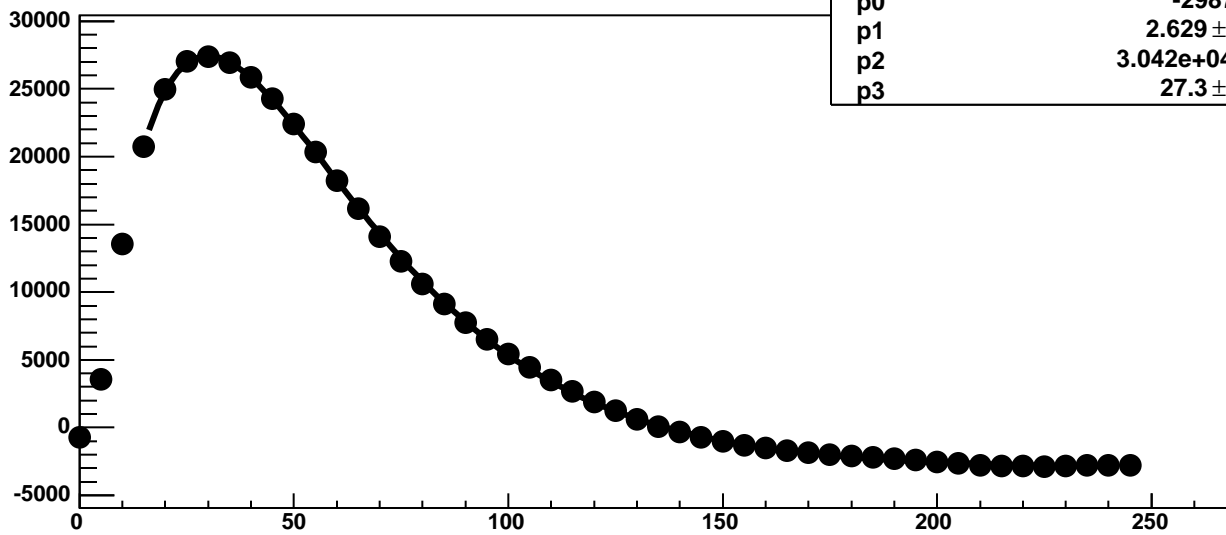
**Chip 10, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold**



Chip 10, Channel 15, Enable 2!, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

2033 / 42

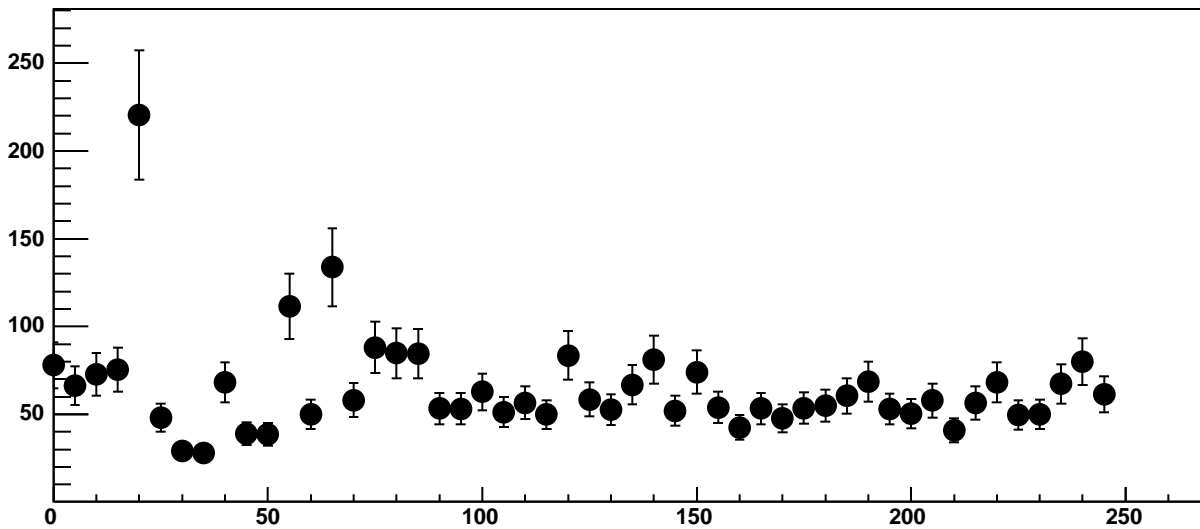
p0 -2987 ± 3.415

p1 2.629 ± 0.01694

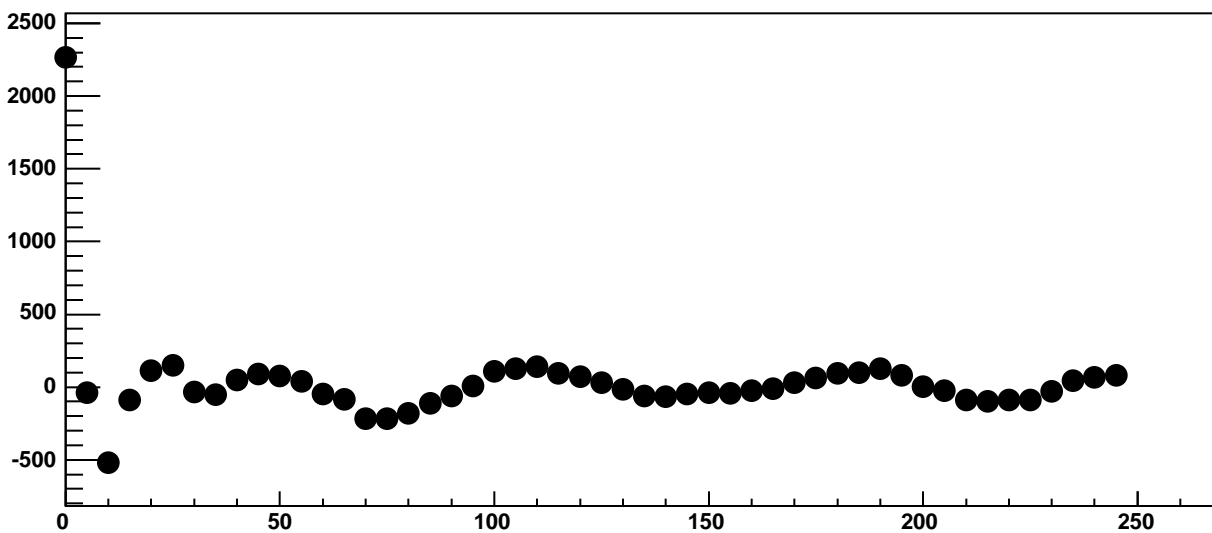
p2 3.042e+04 ± 4.735

p3 27.3 ± 0.01005

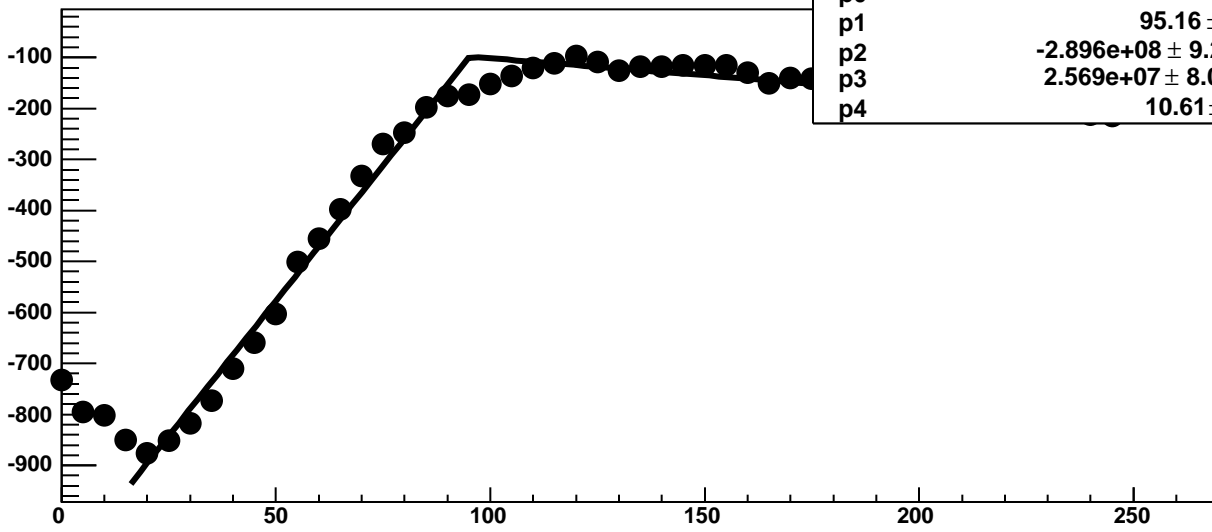
Chip 10, Channel 15, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 15, Enable 2!, DAC=1600, ADC Residuals vs Hold

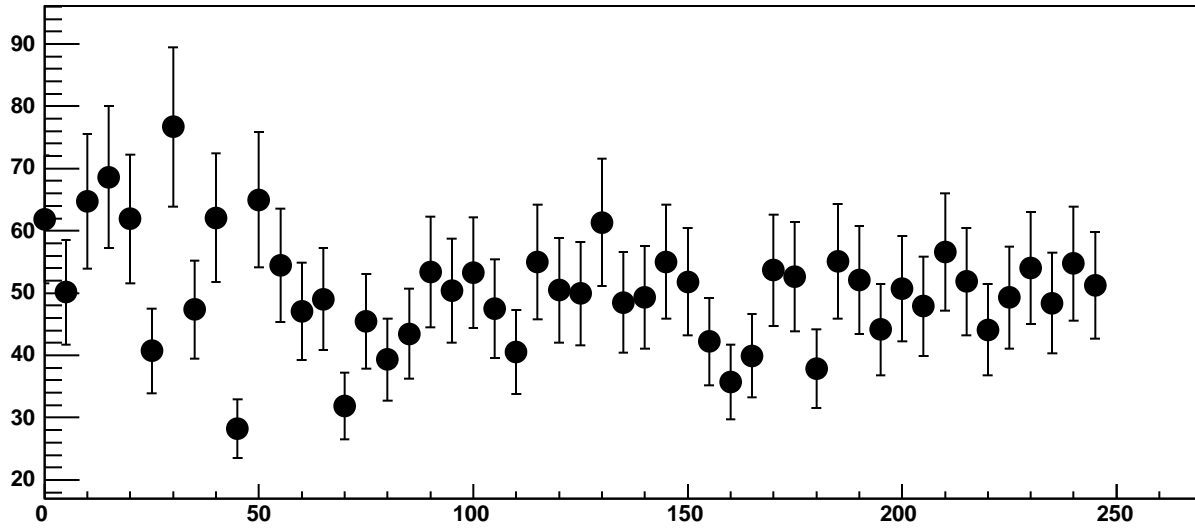


Chip 10, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

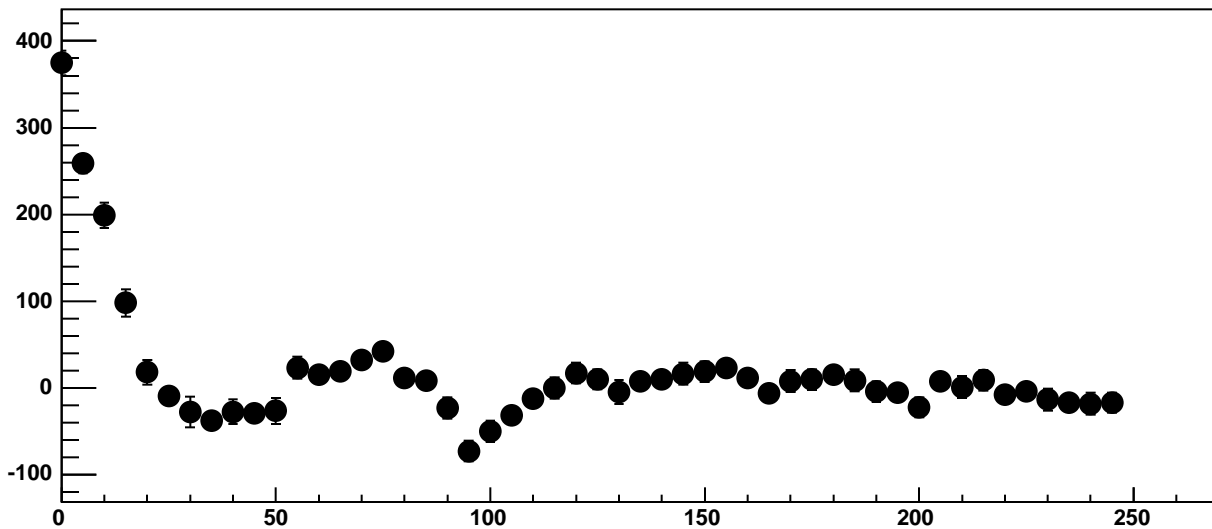


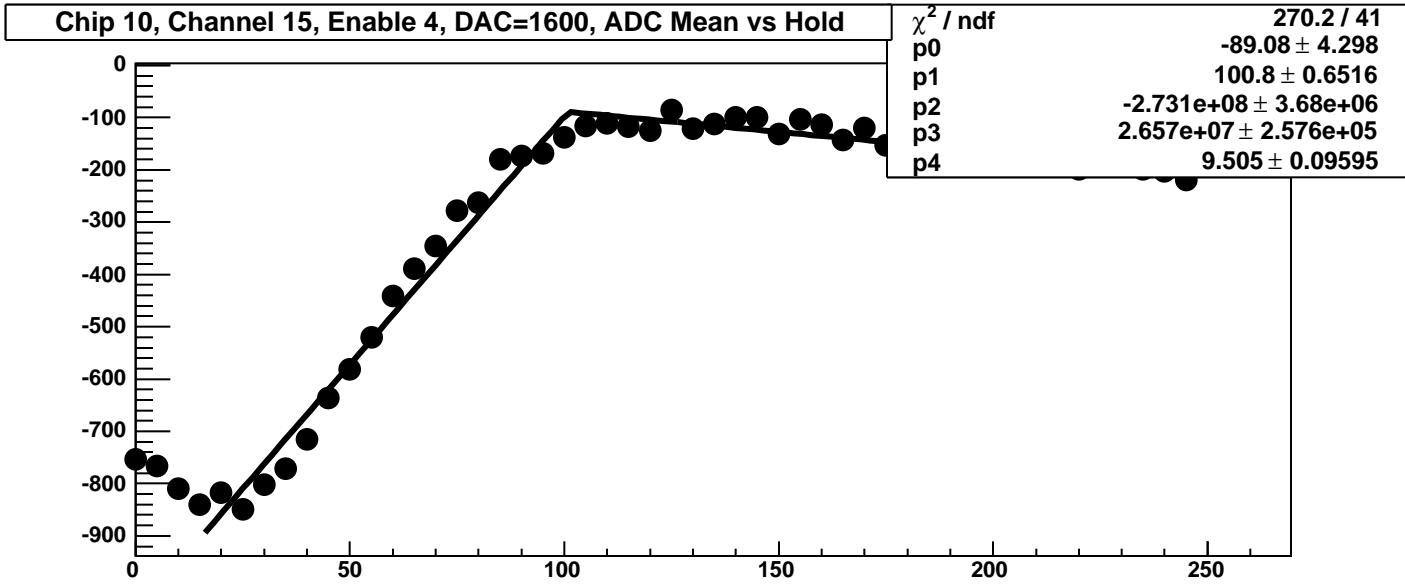
$\chi^2 / \text{ndf}$	231.9 / 41
p0	-98.19 ± 4.037
p1	95.16 ± 0.5816
p2	-2.896e+08 ± 9.266e+06
p3	2.569e+07 ± 8.057e+05
p4	10.61 ± 0.1146

Chip 10, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

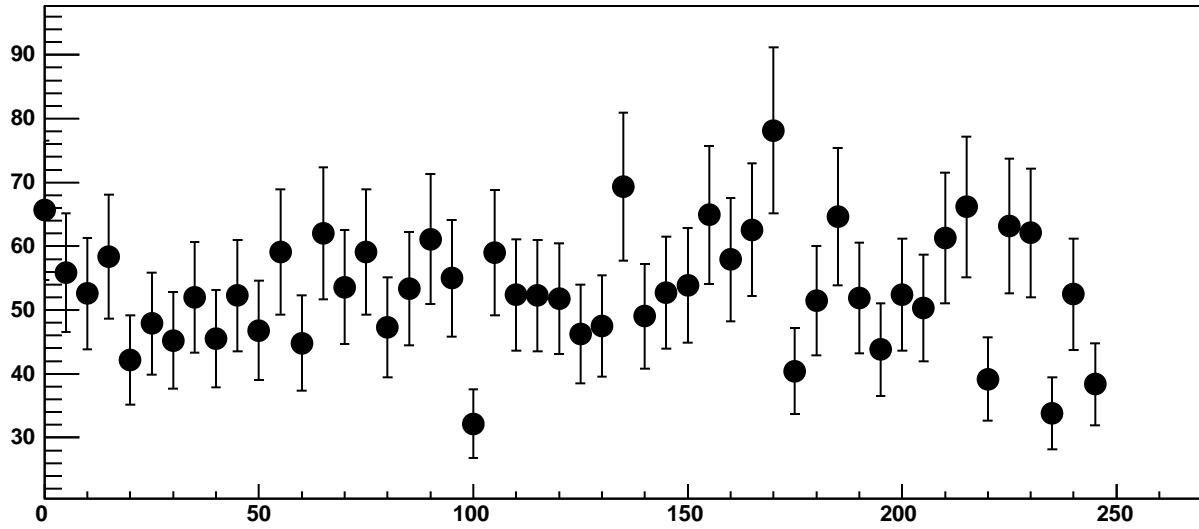


Chip 10, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold

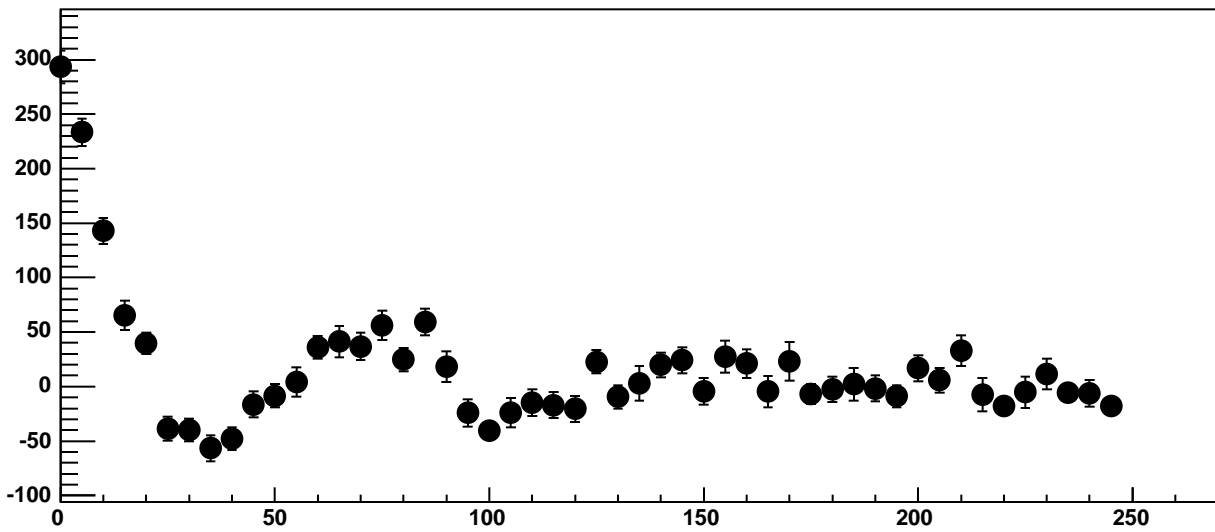




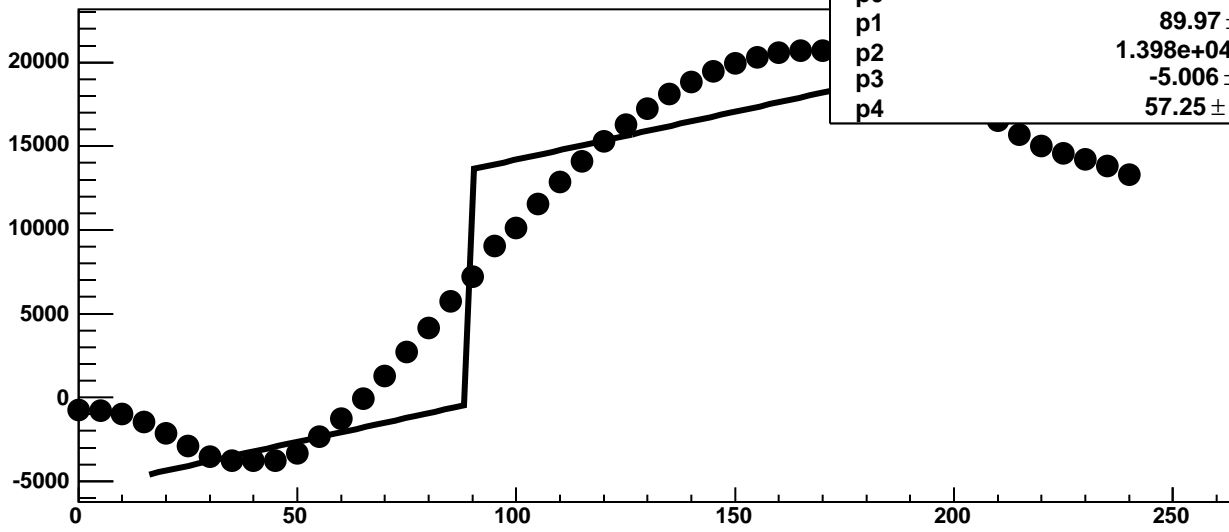
**Chip 10, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold**

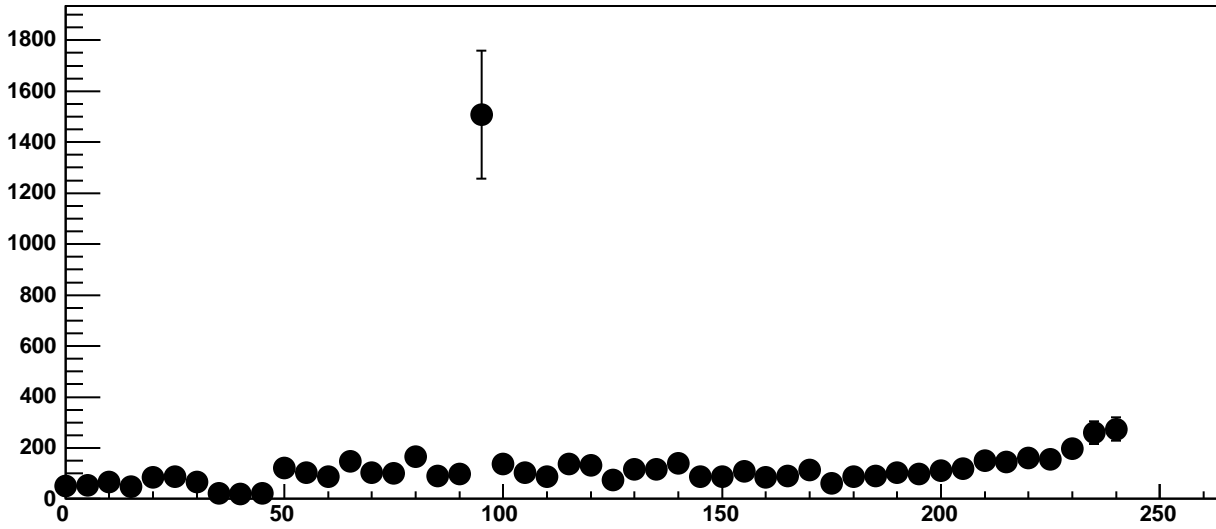


Chip 10, Channel 15, Enable 5, DAC=1600, ADC Mean vs Hold

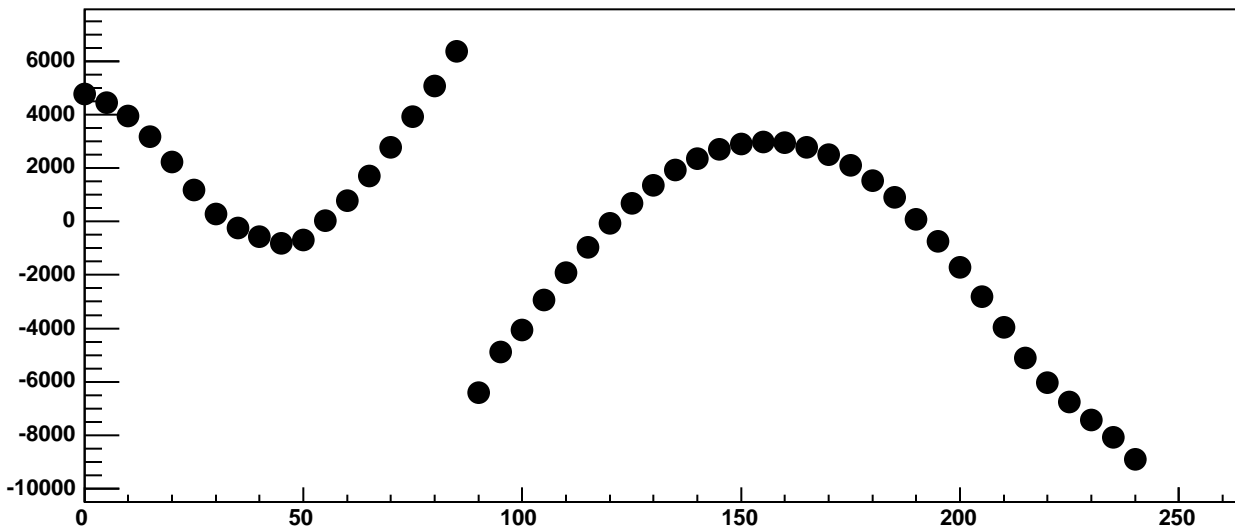


$\chi^2 / \text{ndf}$	7.584e+05 / 41
p0	-360.1 ± 1.291
p1	89.97 ± 0.3338
p2	1.398e+04 ± 5.233
p3	-5.006 ± 0.9326
p4	57.25 ± 0.03694

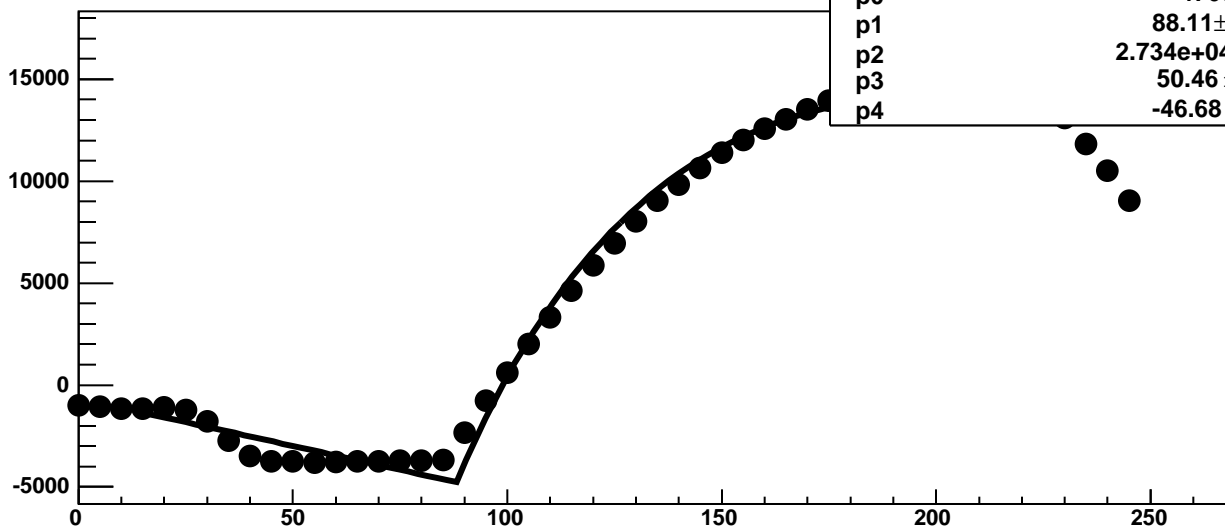
Chip 10, Channel 15, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 15, Enable 5, DAC=1600, ADC Residuals vs Hold

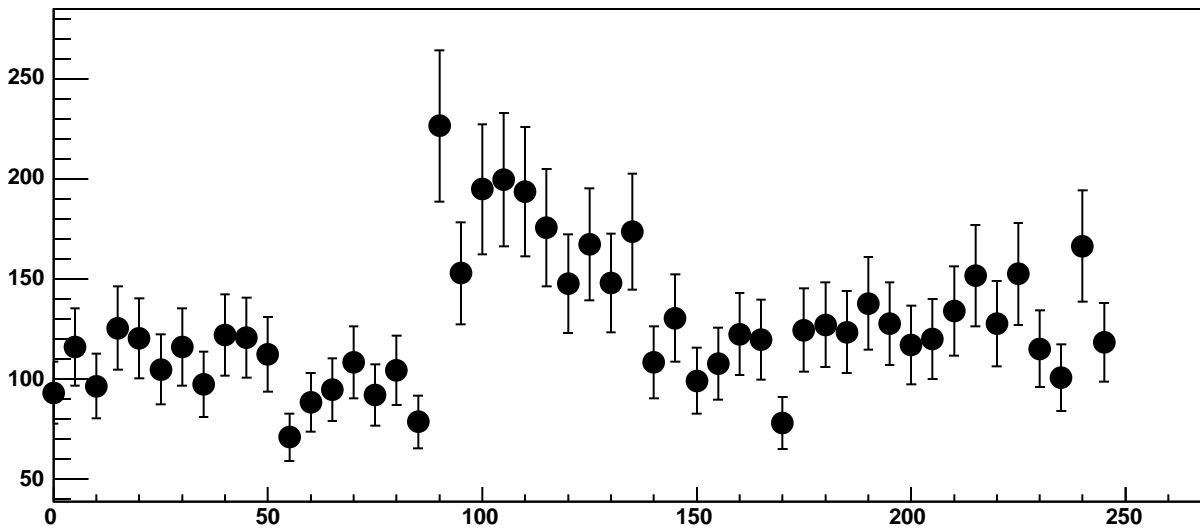


Chip 10, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

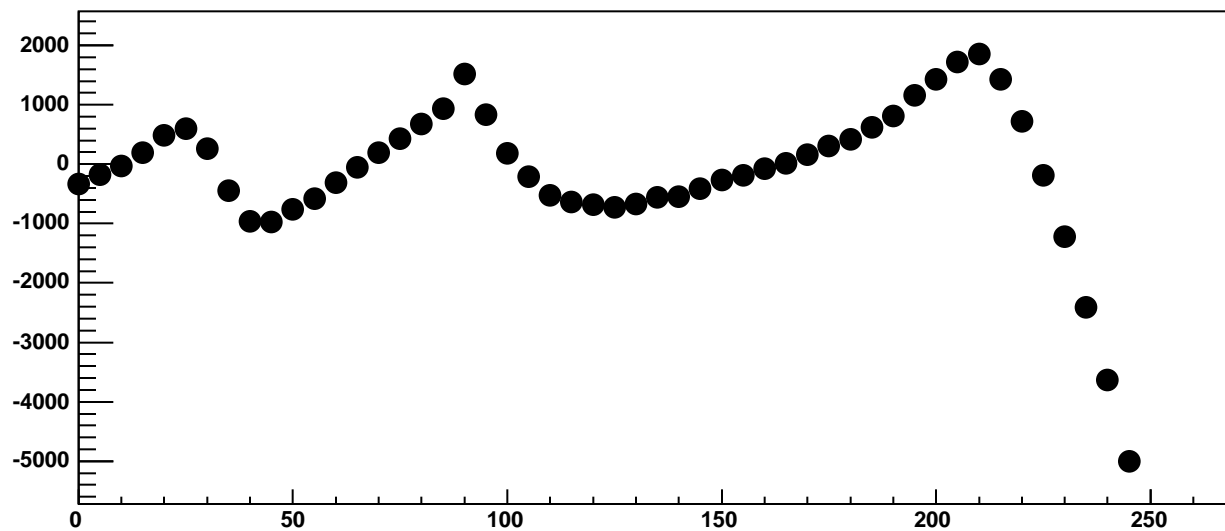


$\chi^2 / \text{ndf}$	5.22e+04 / 41
p0	-4766 ± 10.01
p1	88.11 ± 0.05621
p2	2.734e+04 ± 58.16
p3	50.46 ± 0.1435
p4	-46.68 ± 0.2643

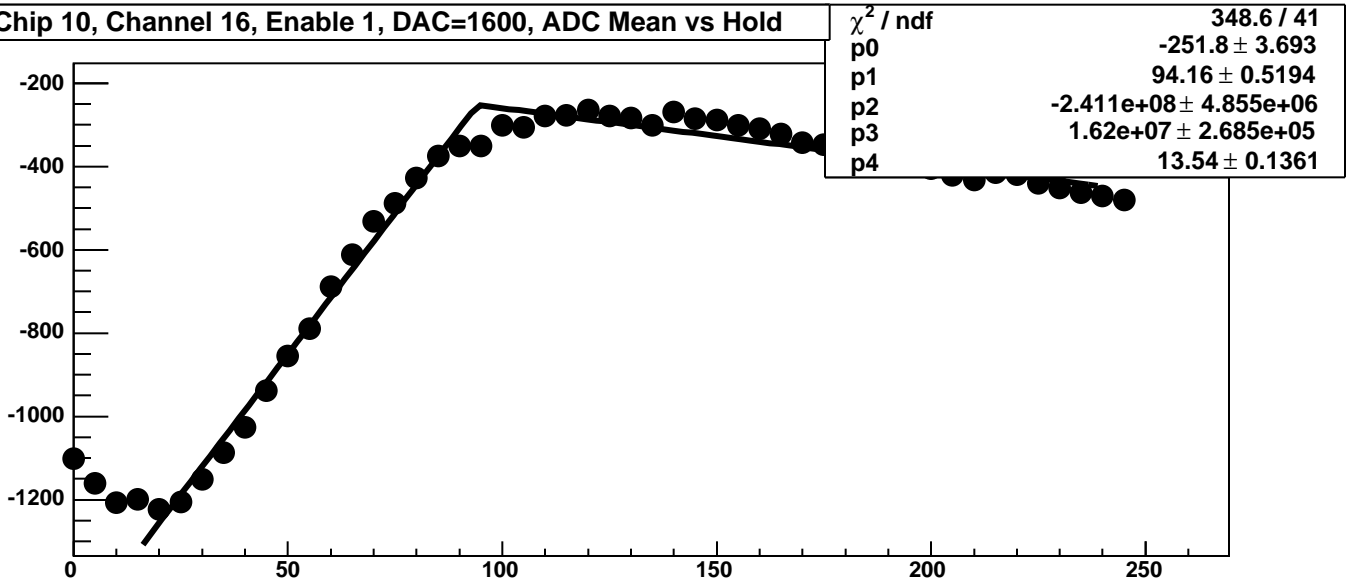
Chip 10, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



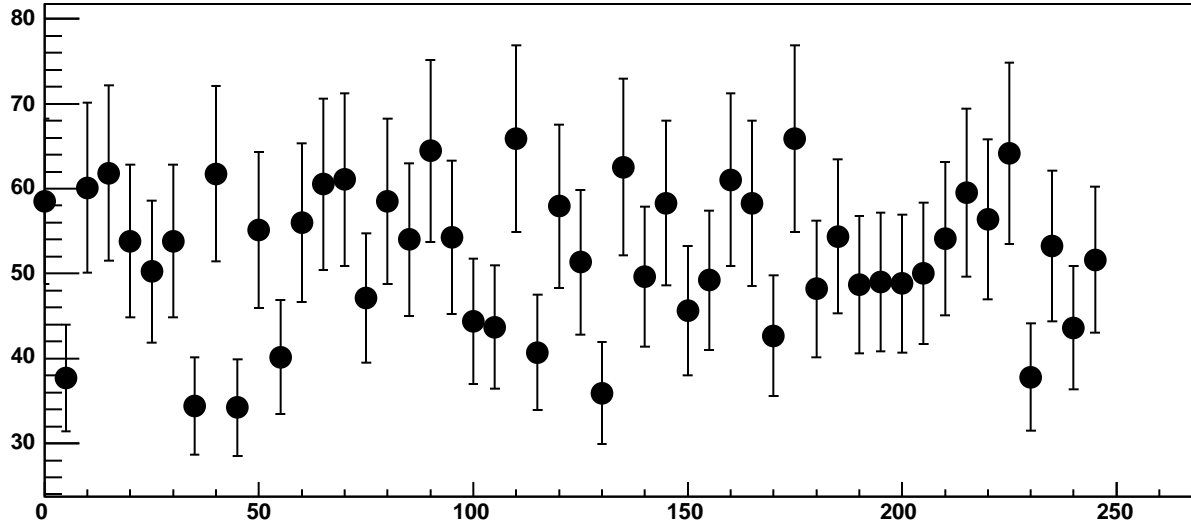
Chip 10, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold



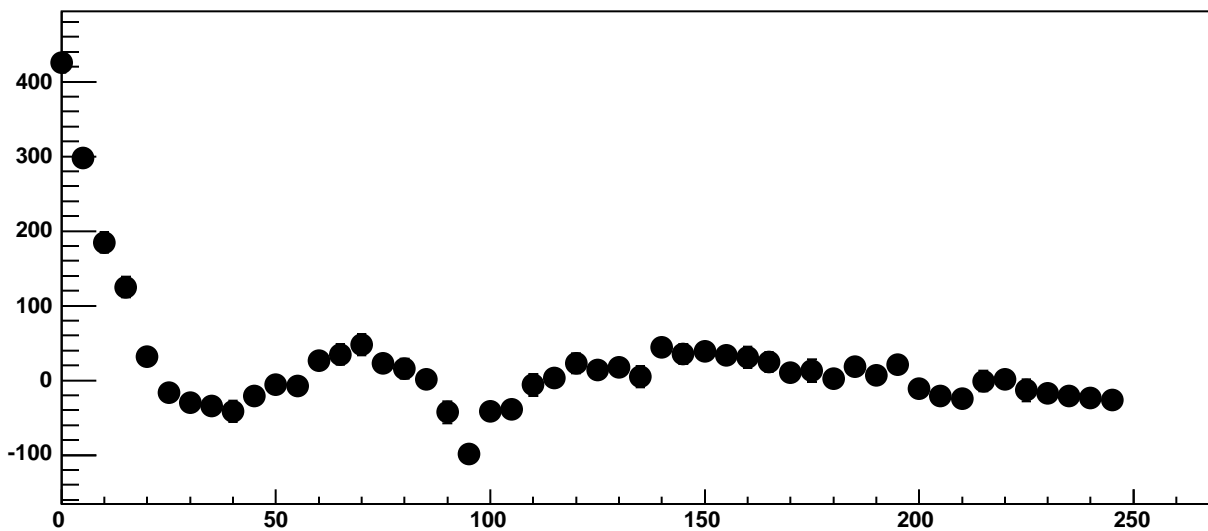
Chip 10, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 10, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold

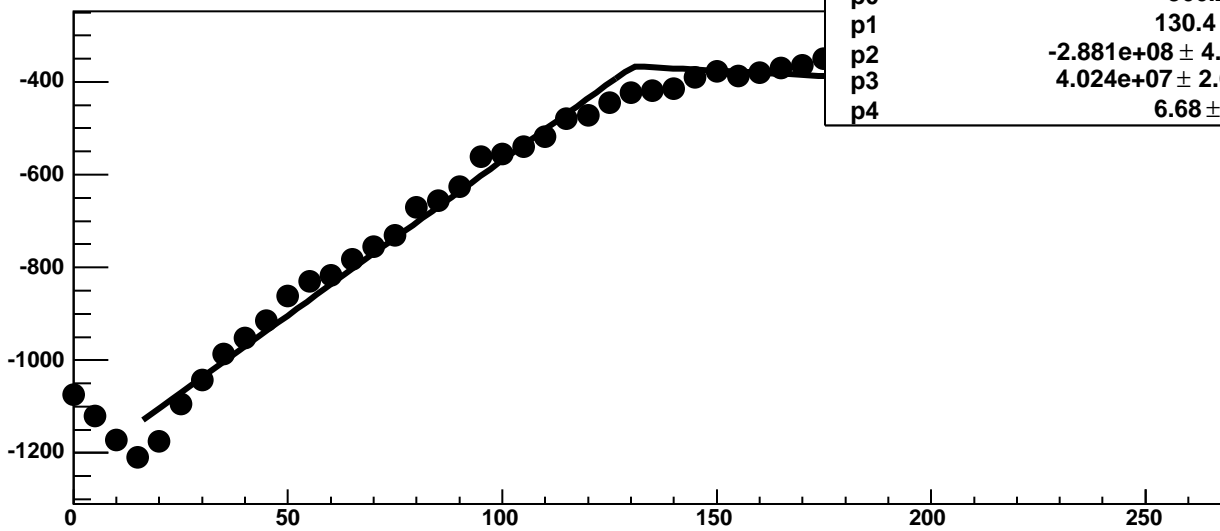


Chip 10, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold





Chip 10, Channel 16, Enable 2, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

283.3 / 41

p0

$-366.2 \pm 4.785$

p1

$130.4 \pm 0.9527$

p2

$-2.881\text{e}+08 \pm 4.528\text{e}+06$

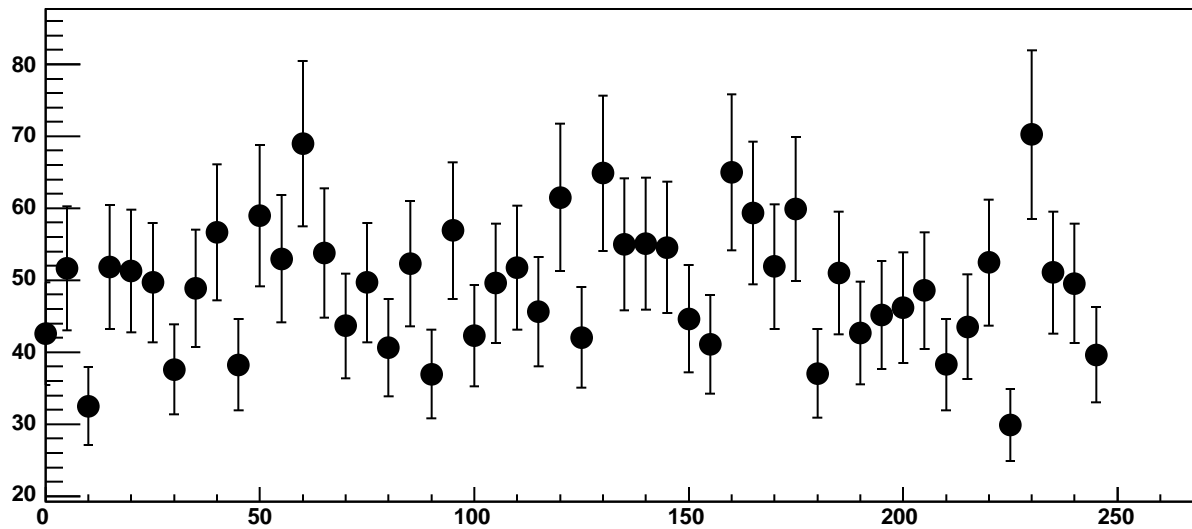
p3

$4.024\text{e}+07 \pm 2.656\text{e}+05$

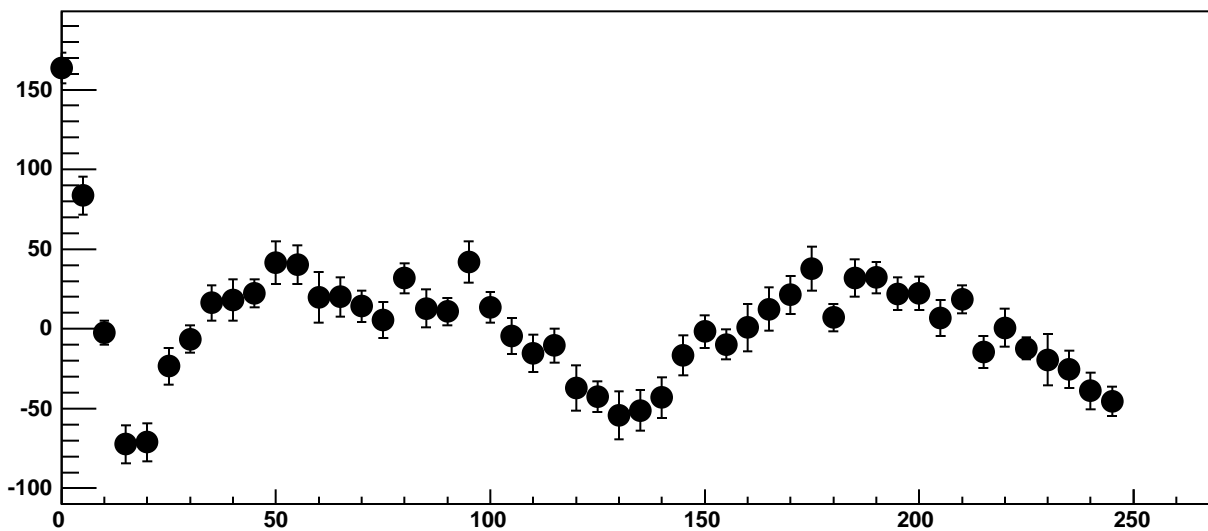
p4

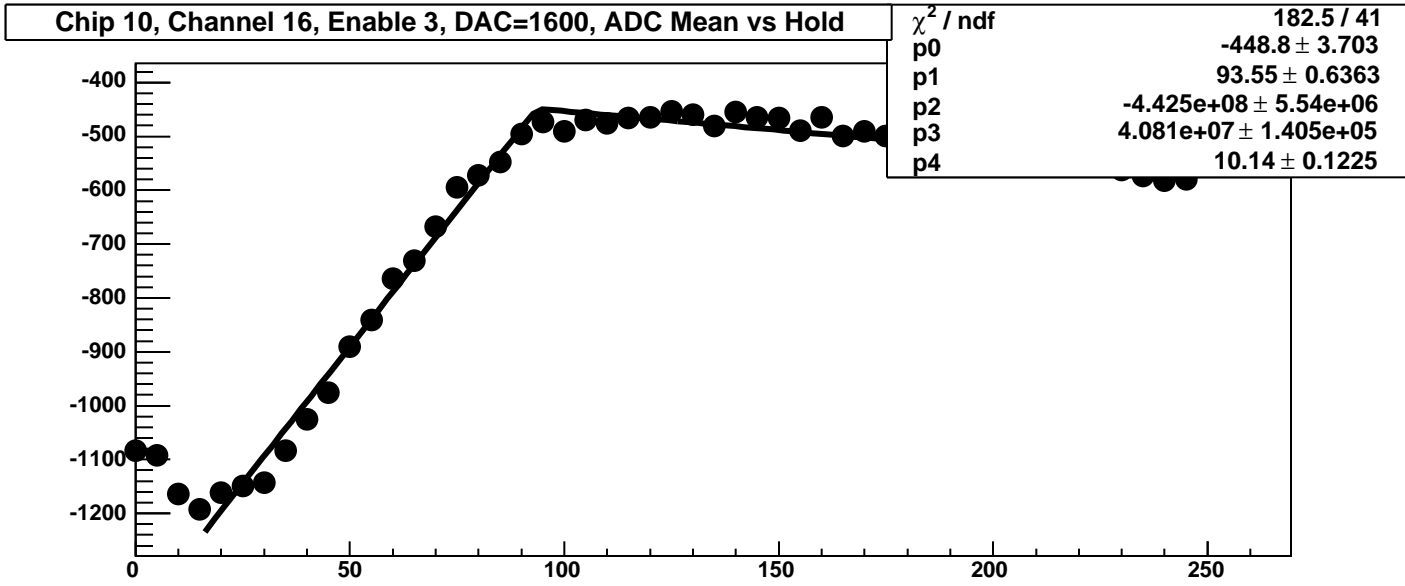
$6.68 \pm 0.06662$

Chip 10, Channel 16, Enable 2, DAC=1600, ADC Noise vs Hold

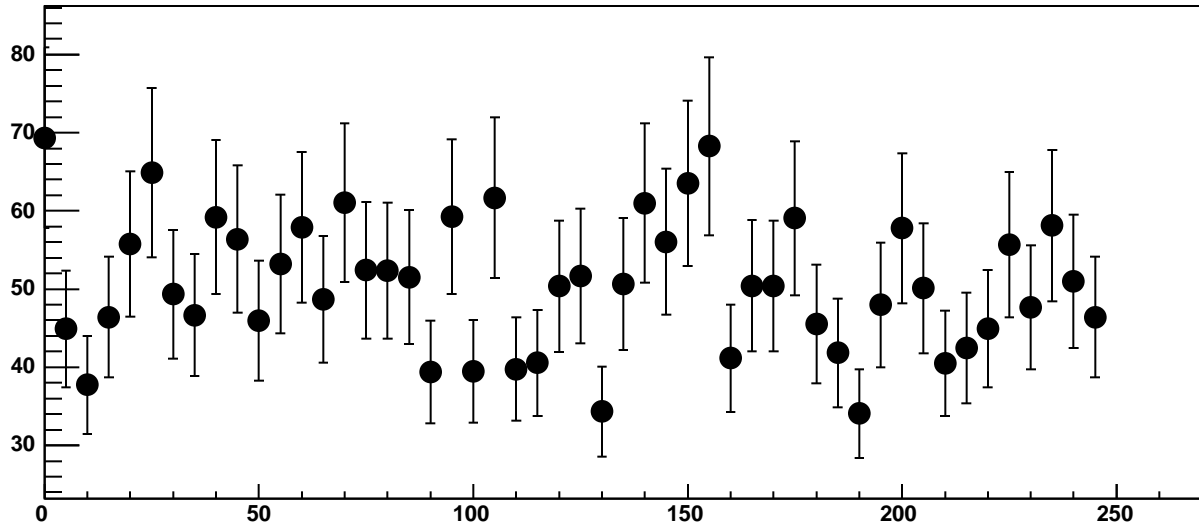


Chip 10, Channel 16, Enable 2, DAC=1600, ADC Residuals vs Hold

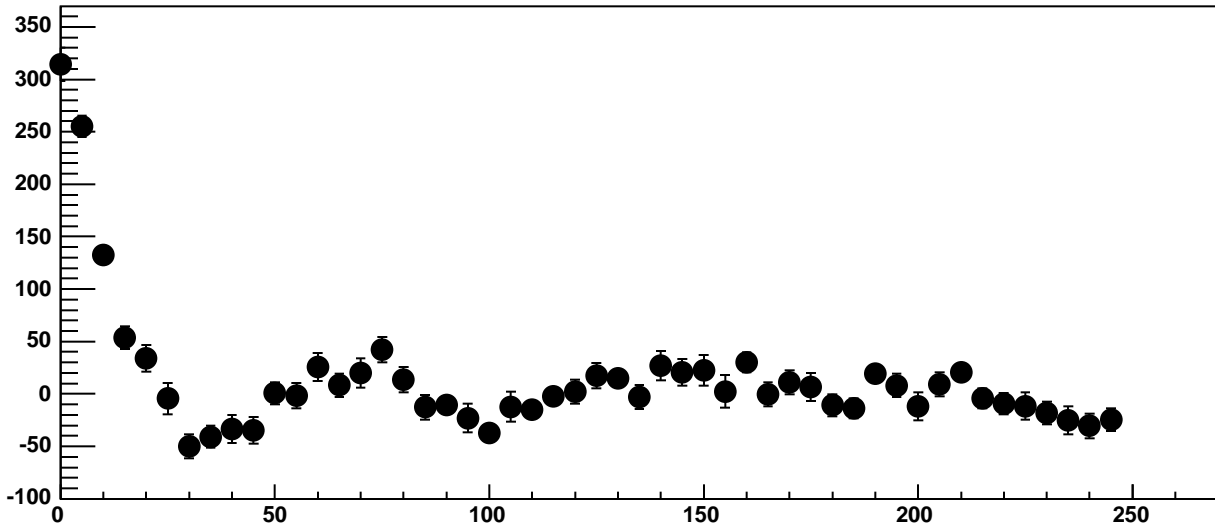




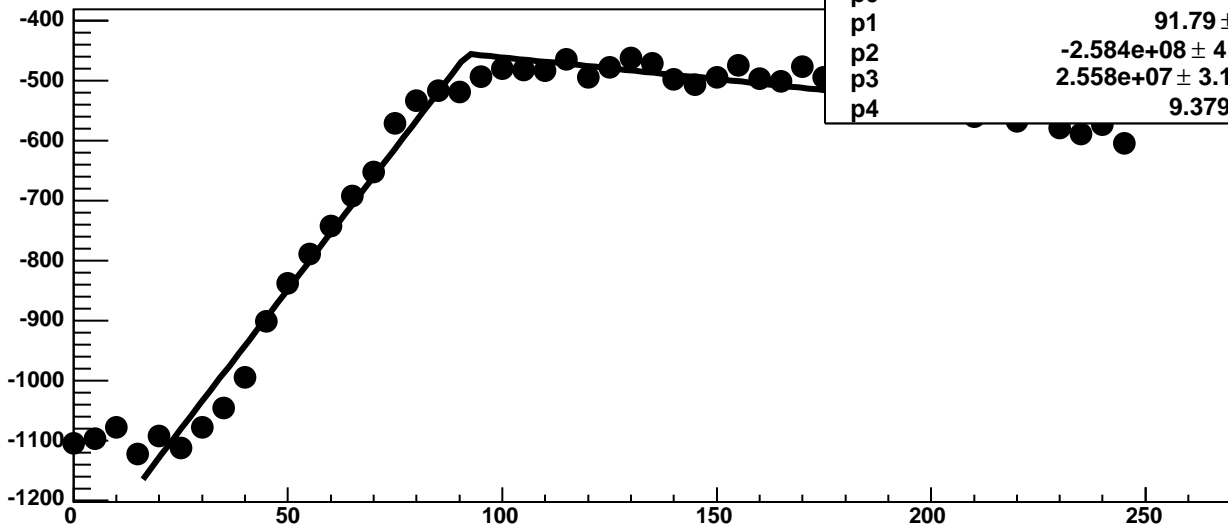
**Chip 10, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold**



**Chip 10, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold**

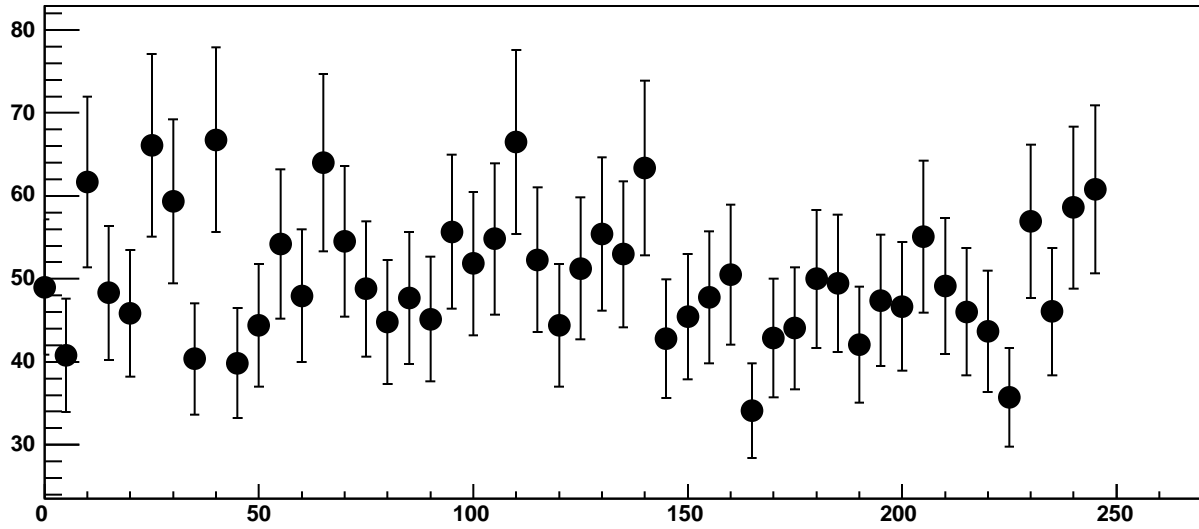


Chip 10, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold

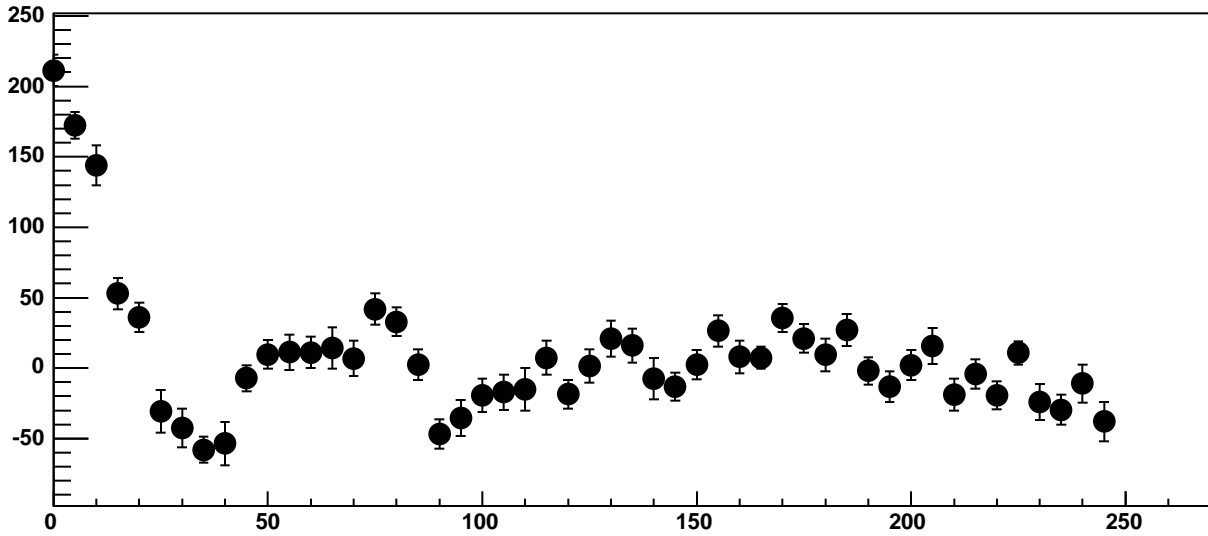


$\chi^2 / \text{ndf}$	227.1 / 41
p0	$-455.8 \pm 4.07$
p1	$91.79 \pm 0.6909$
p2	$-2.584\text{e}+08 \pm 4.57\text{e}+06$
p3	$2.558\text{e}+07 \pm 3.122\text{e}+05$
p4	$9.379 \pm 0.121$

Chip 10, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold

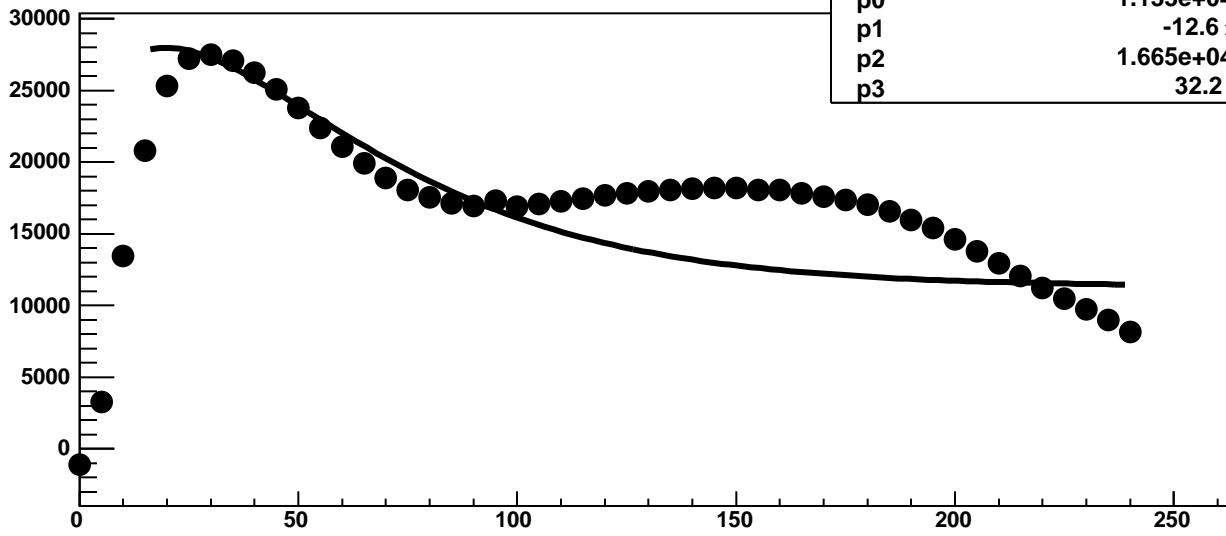


Chip 10, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold

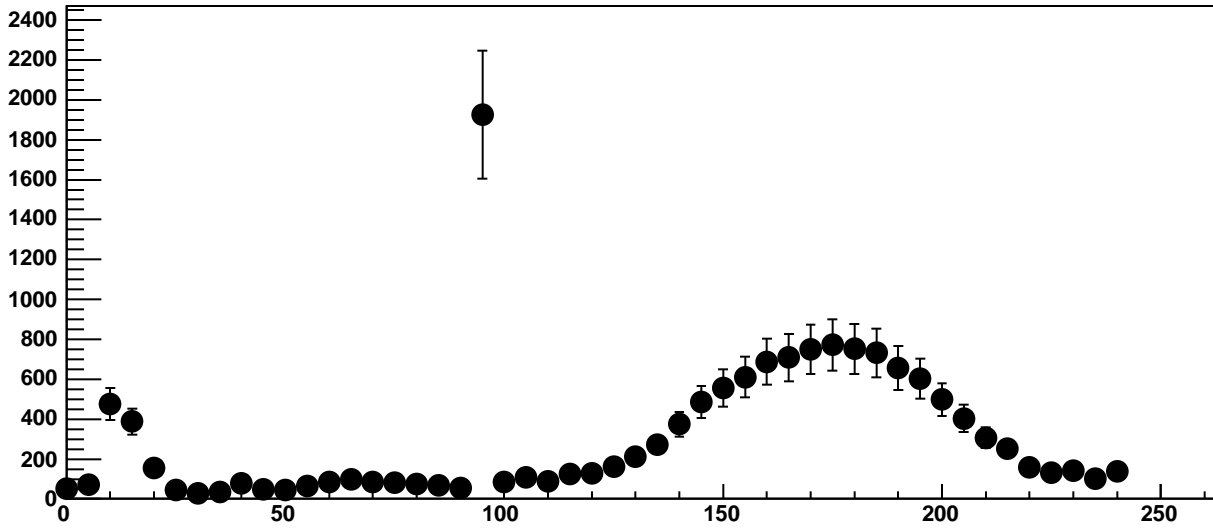


Chip 10, Channel 16, Enable 5!, DAC=1600, ADC Mean vs Hold

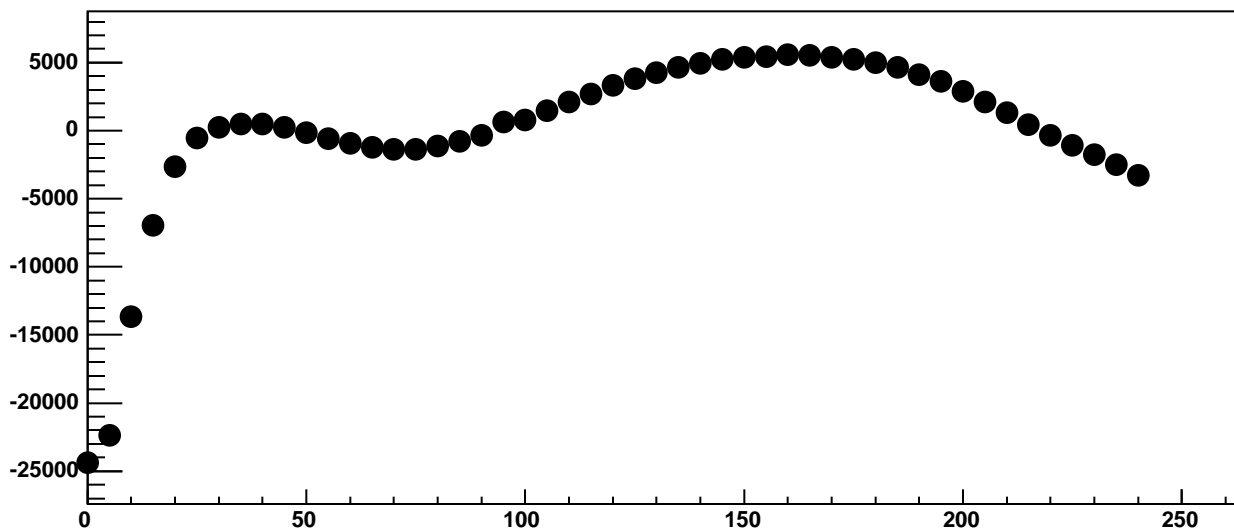
$\chi^2 / \text{ndf}$	1.511e+05 / 42
p0	1.133e+04 $\pm$ 19.47
p1	-12.6 $\pm$ 0.3056
p2	1.665e+04 $\pm$ 36.15
p3	32.2 $\pm$ 0.1222

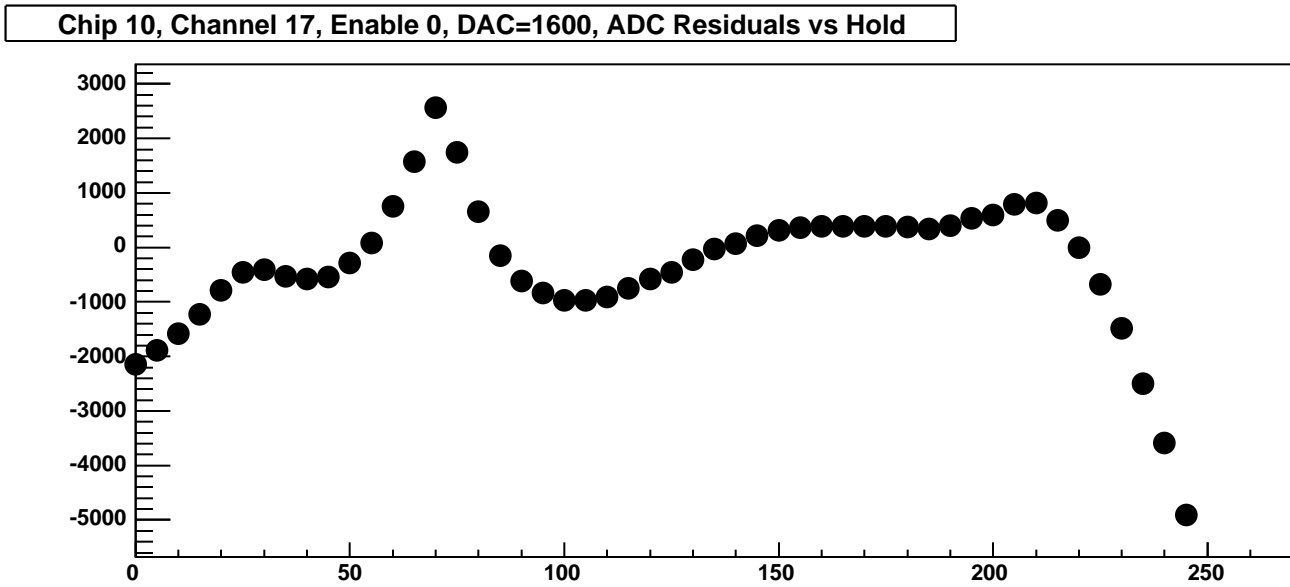
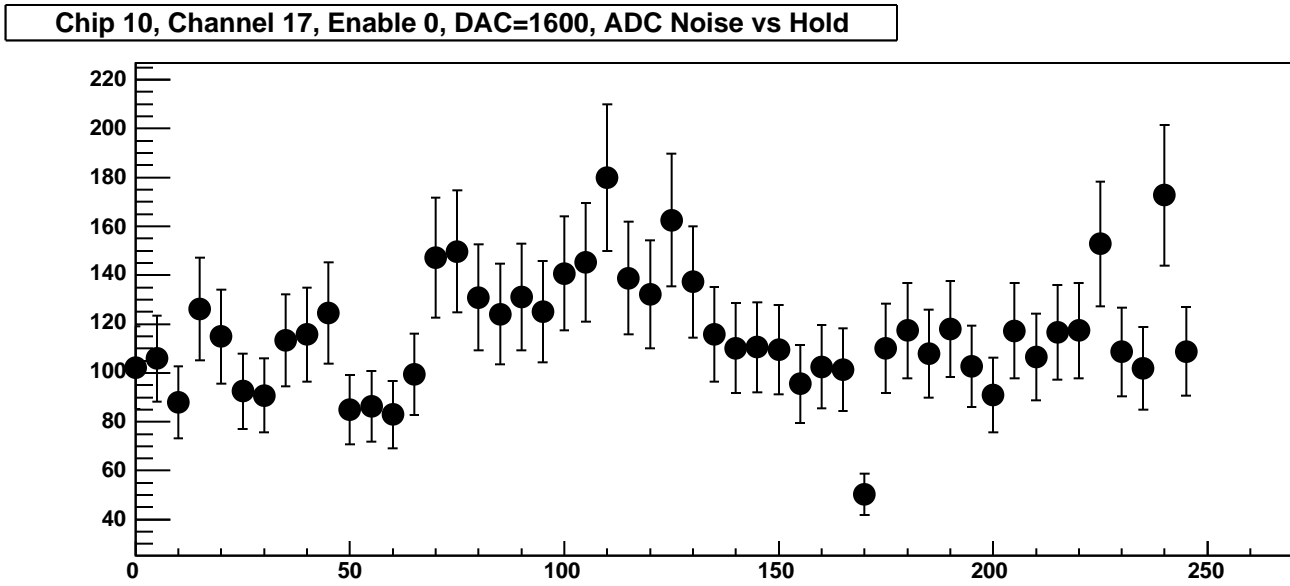
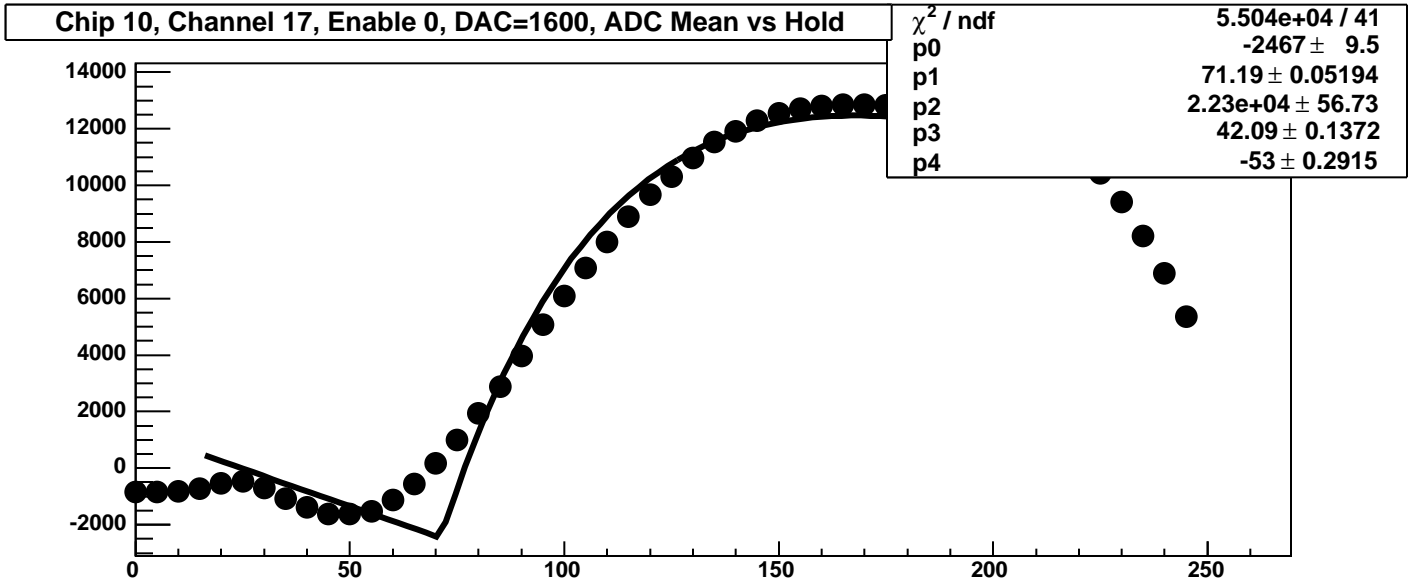


Chip 10, Channel 16, Enable 5!, DAC=1600, ADC Noise vs Hold

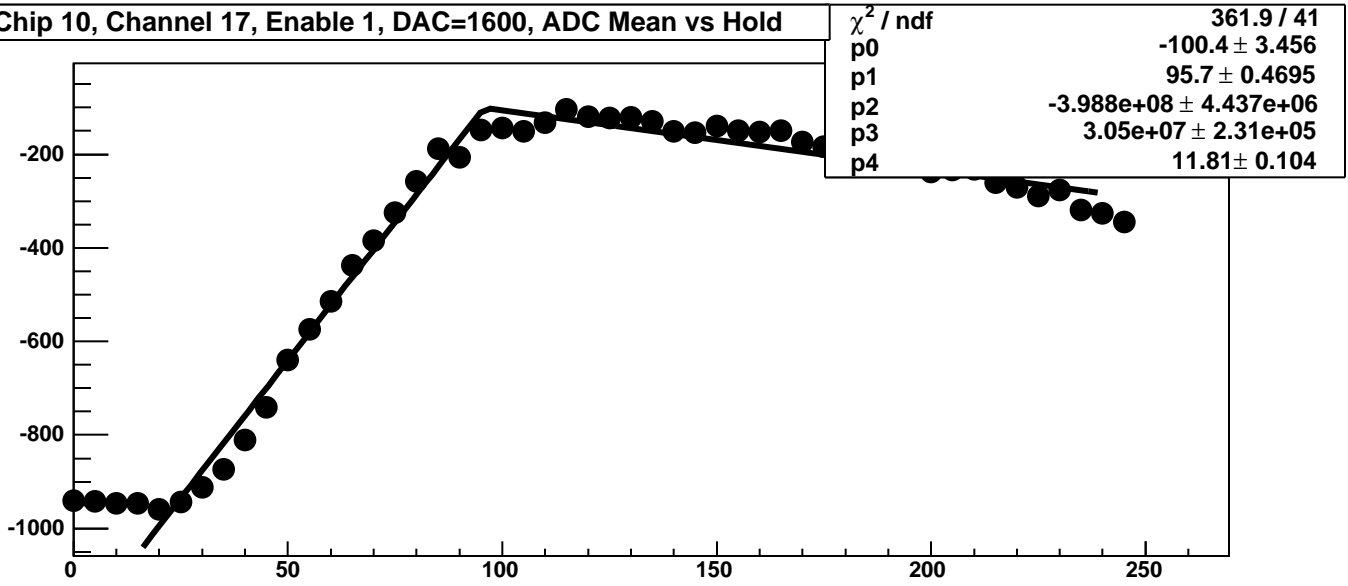


Chip 10, Channel 16, Enable 5!, DAC=1600, ADC Residuals vs Hold

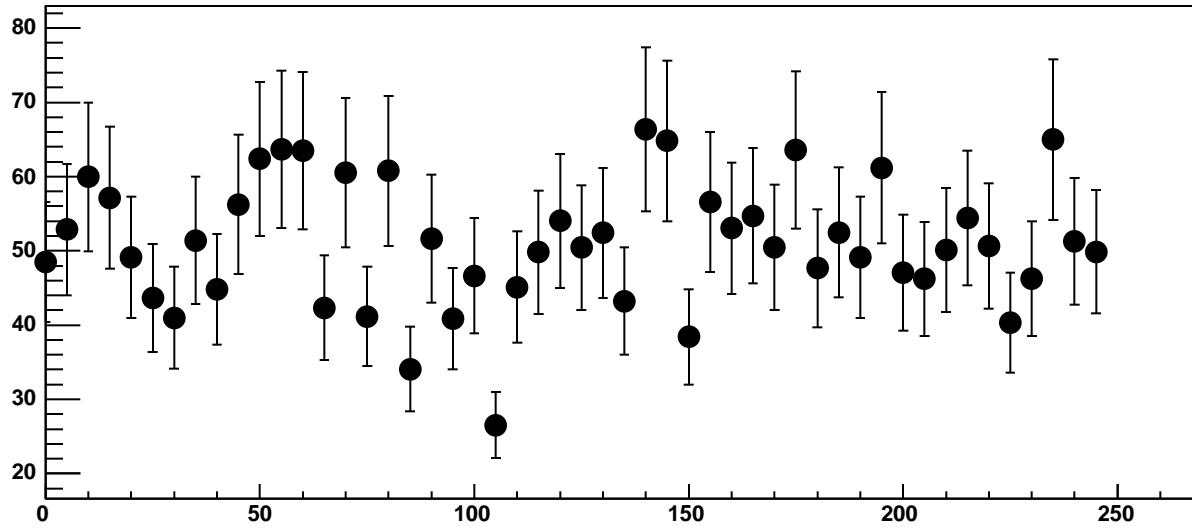




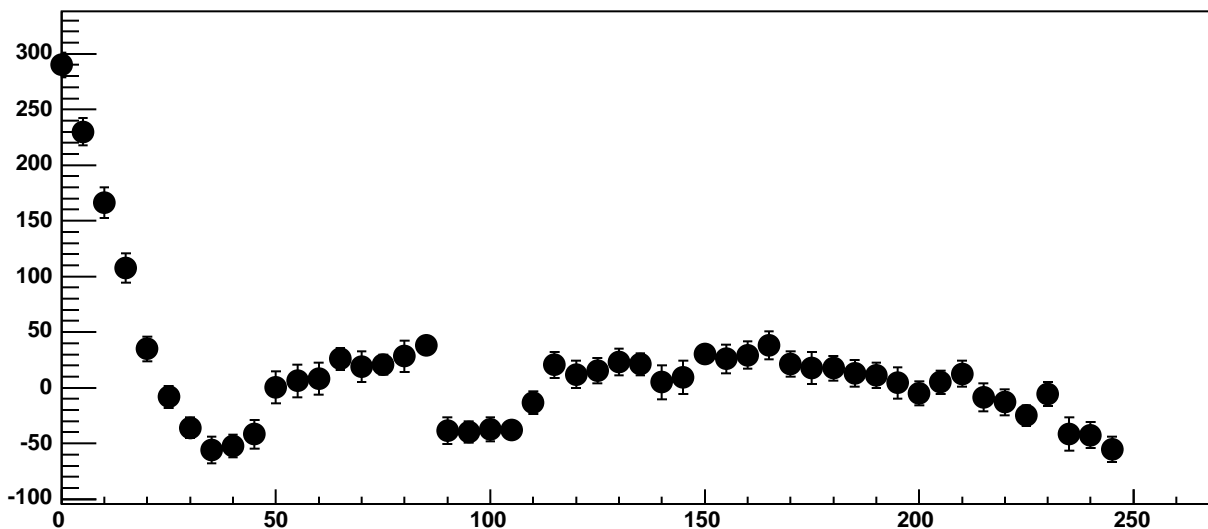
Chip 10, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 10, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold



Chip 10, Channel 17, Enable 2!, DAC=1600, ADC Mean vs Hold

$\chi^2 / \text{ndf}$

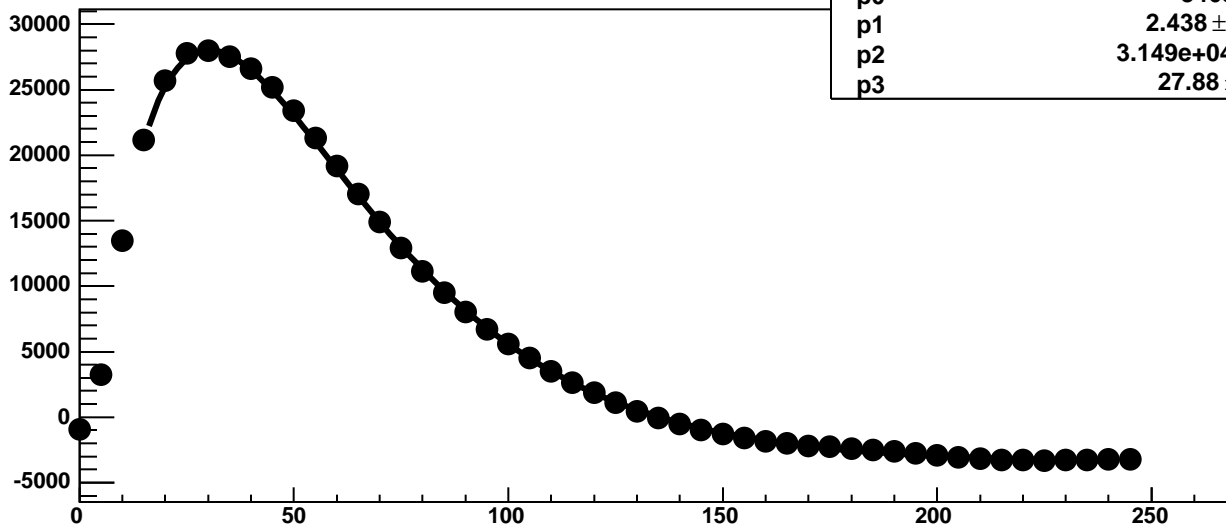
6968 / 42

p0  $-3468 \pm 3.195$

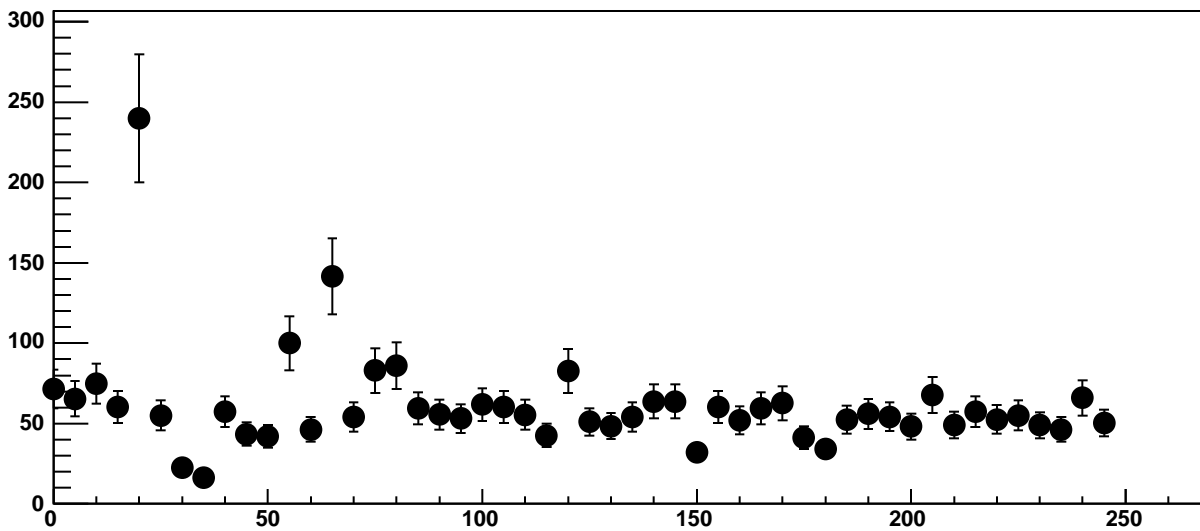
p1  $2.438 \pm 0.01384$

p2  $3.149\text{e}+04 \pm 3.999$

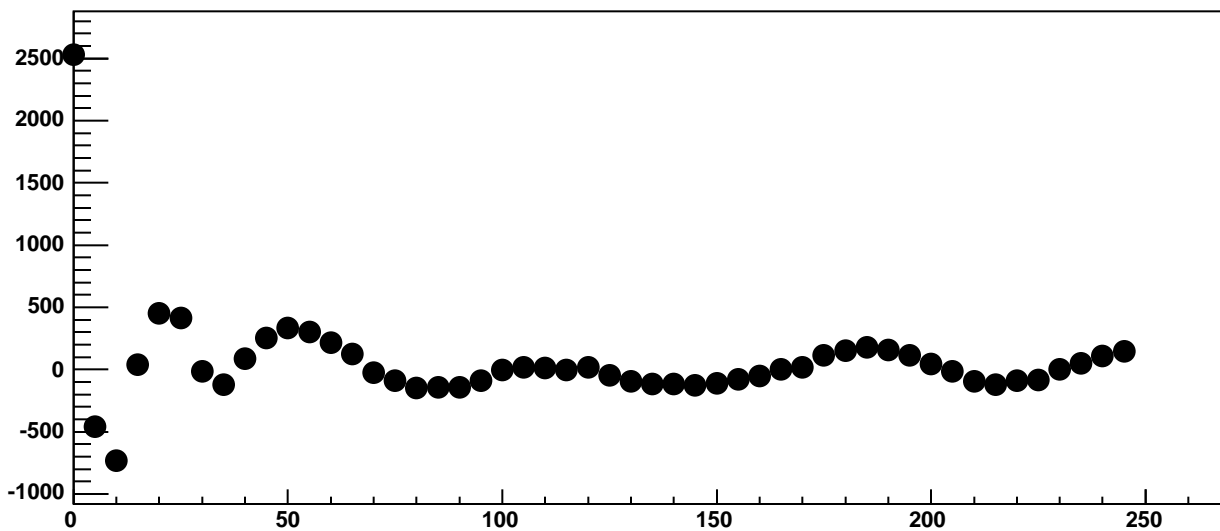
p3  $27.88 \pm 0.0086$

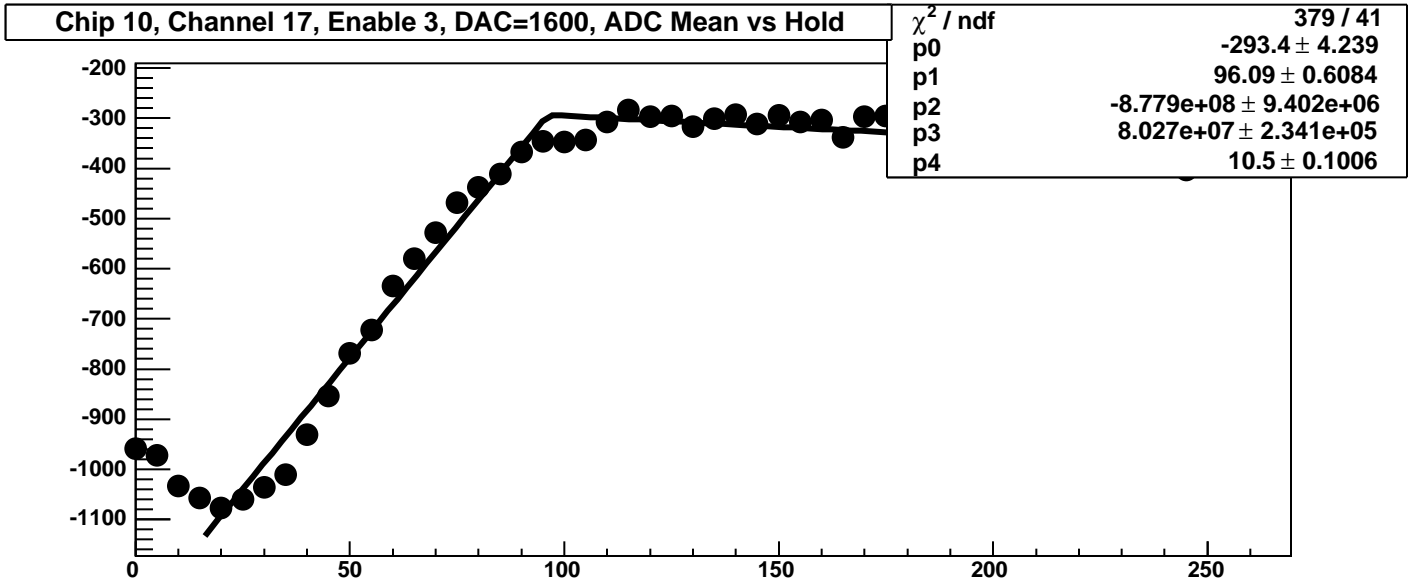


Chip 10, Channel 17, Enable 2!, DAC=1600, ADC Noise vs Hold

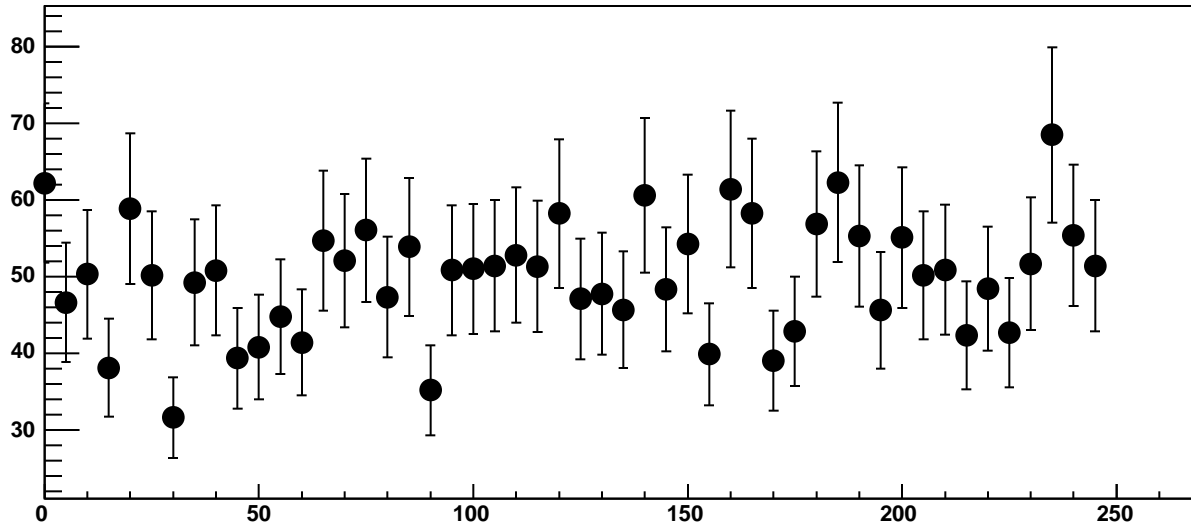


Chip 10, Channel 17, Enable 2!, DAC=1600, ADC Residuals vs Hold

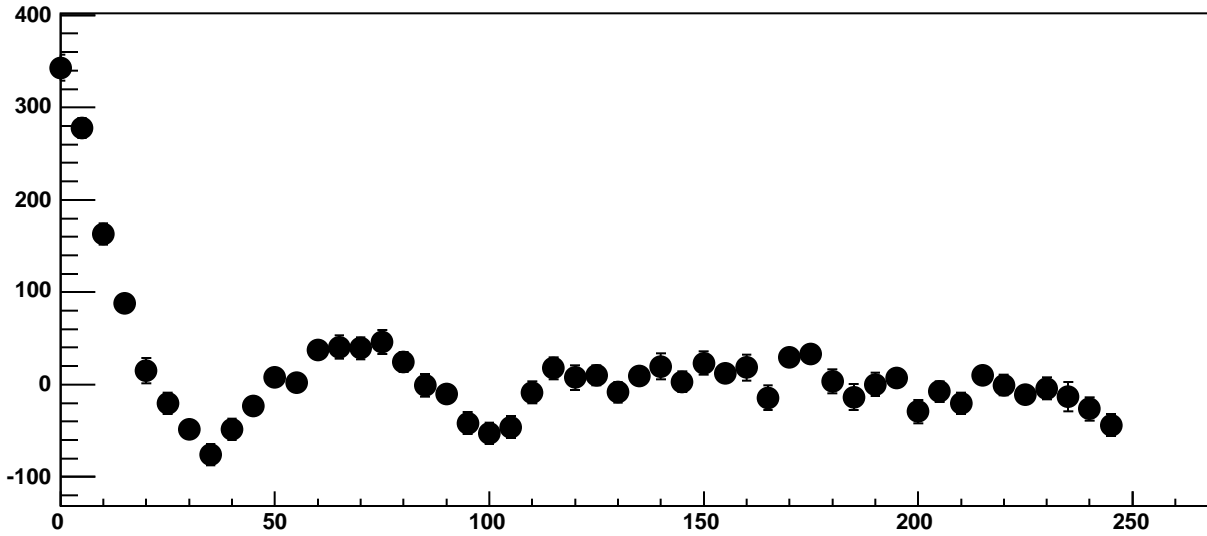




**Chip 10, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold**

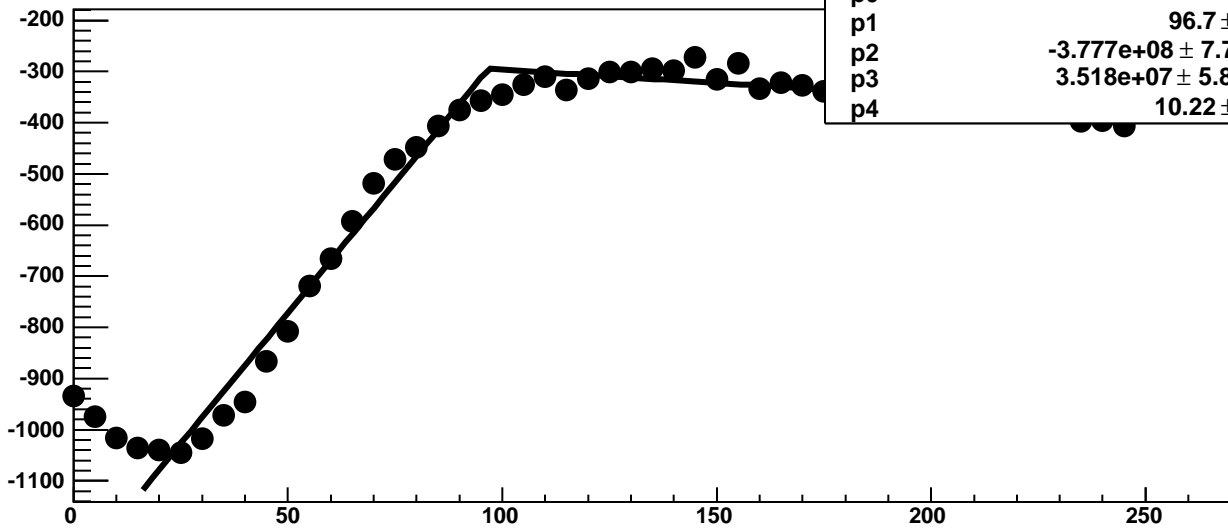


**Chip 10, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold**



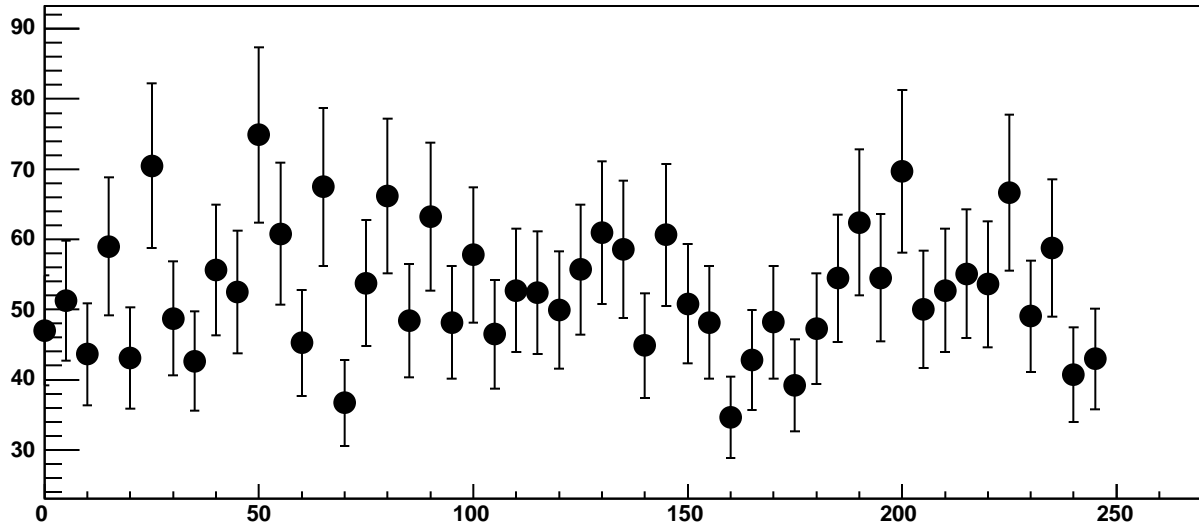


Chip 10, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold

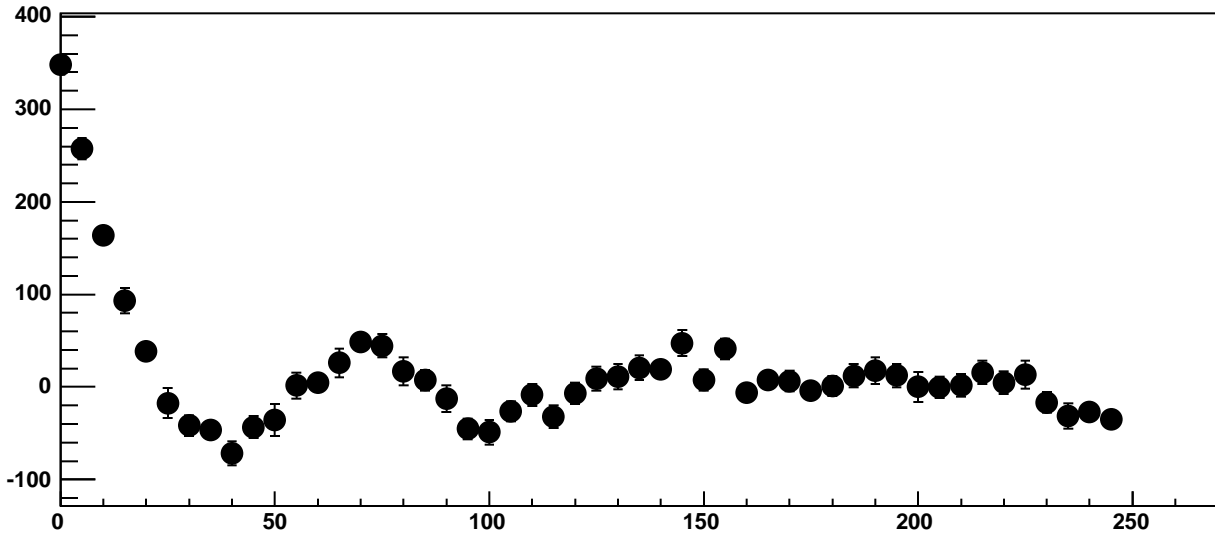


$\chi^2 / \text{ndf}$	301.6 / 41
p0	$-294.5 \pm 4.214$
p1	$96.7 \pm 0.6742$
p2	$-3.777\text{e}+08 \pm 7.721\text{e}+06$
p3	$3.518\text{e}+07 \pm 5.841\text{e}+05$
p4	$10.22 \pm 0.1184$

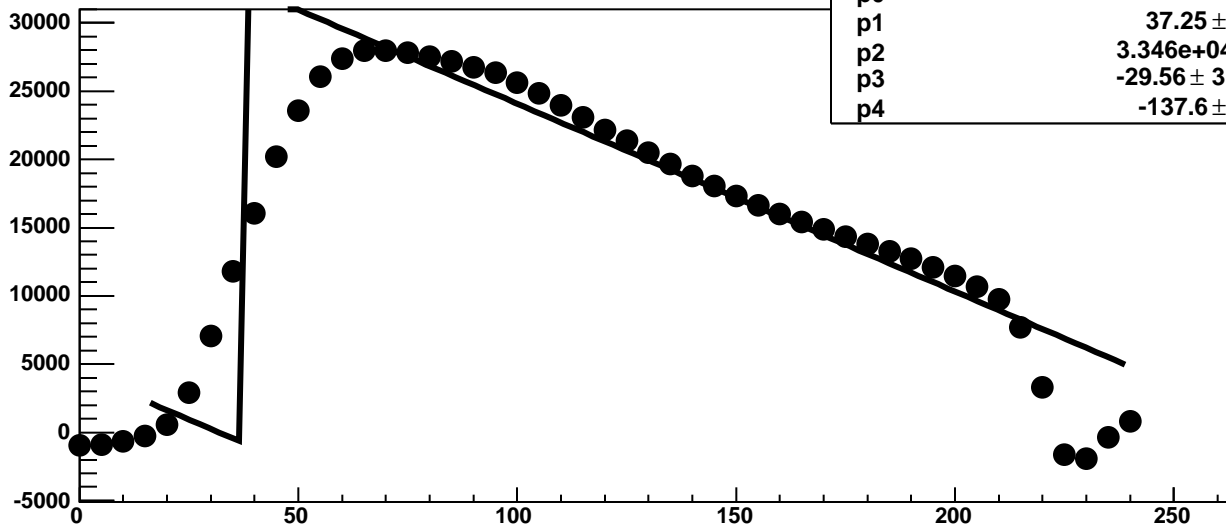
Chip 10, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

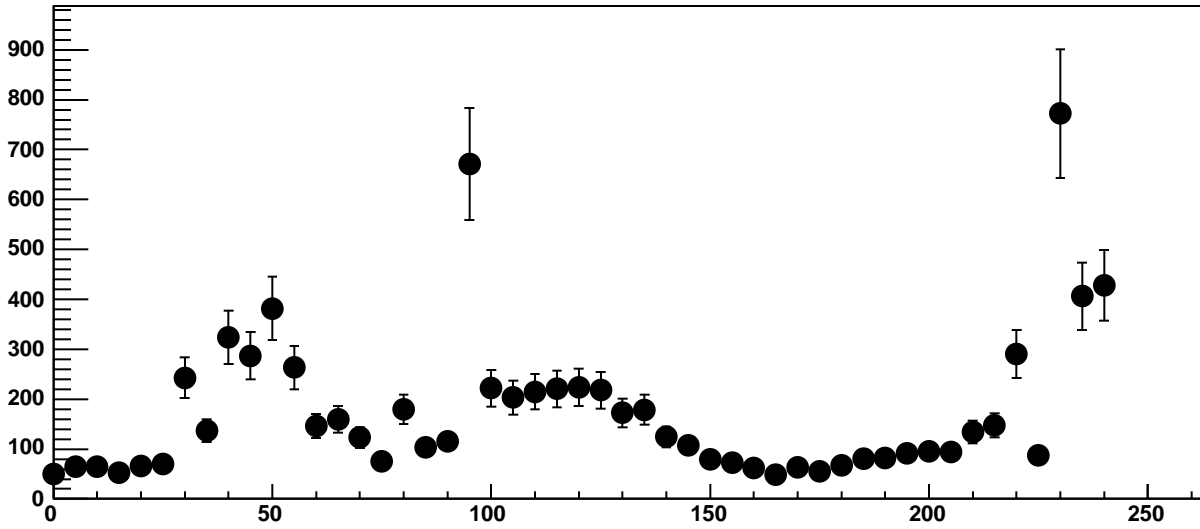


Chip 10, Channel 17, Enable 5, DAC=1600, ADC Mean vs Hold

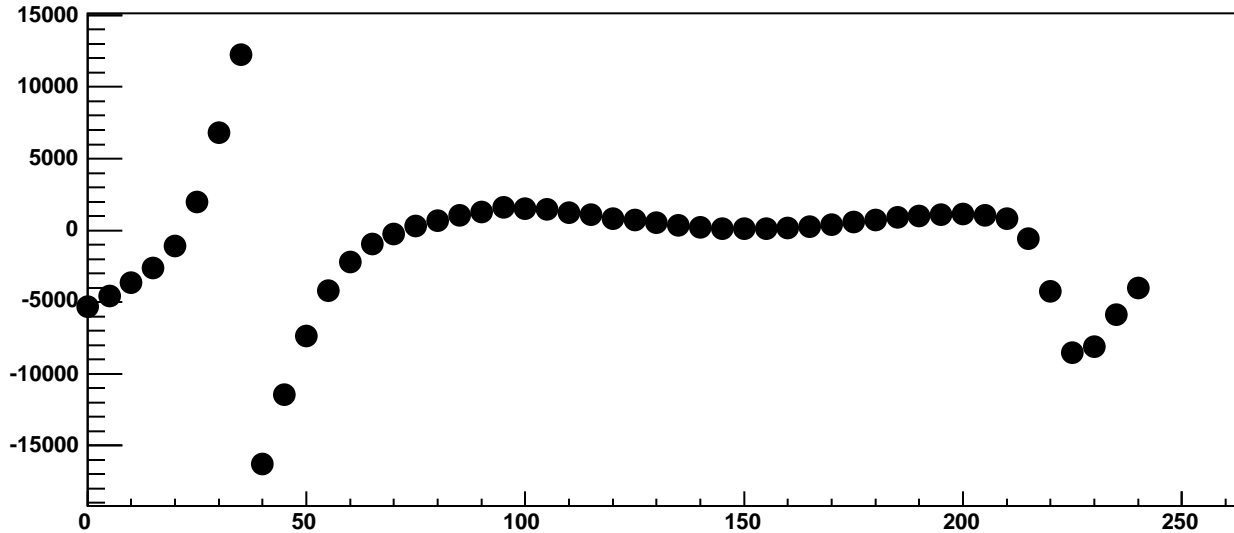


$\chi^2 / \text{ndf}$	5.515e+05 / 41
p0	-745.9 ± 6.075
p1	37.25 ± 0.02762
p2	3.346e+04 ± 14.56
p3	-29.56 ± 3.959e-07
p4	-137.6 ± 0.08638

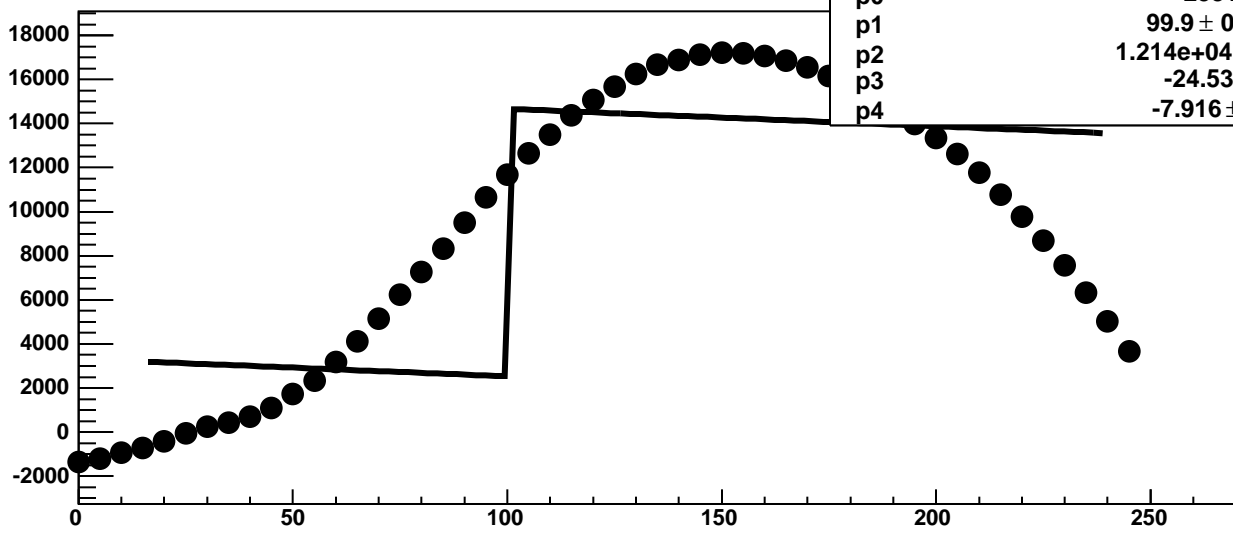
Chip 10, Channel 17, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 10, Channel 17, Enable 5, DAC=1600, ADC Residuals vs Hold

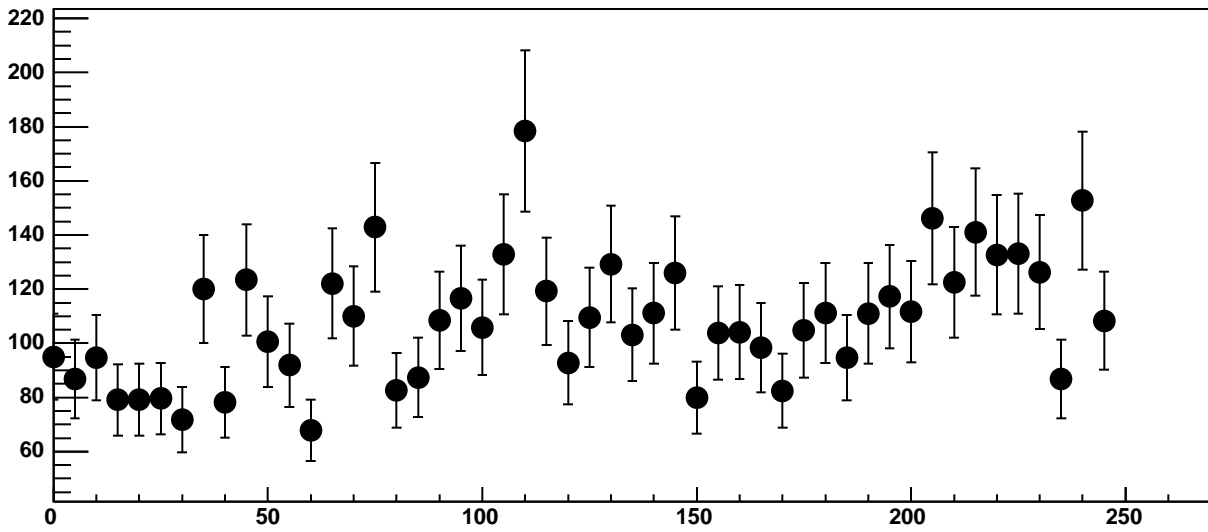


Chip 11, Channel 0, Enable 0, DAC=1600, ADC Mean vs Hold

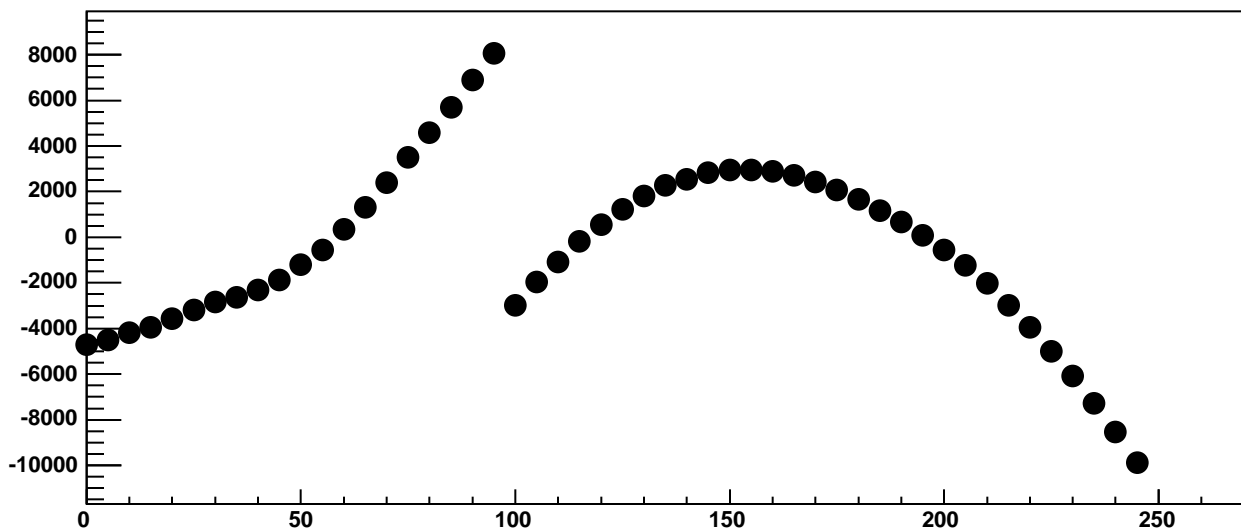


$\chi^2 / \text{ndf}$	9.627e+05 / 41
p0	2531 ± 41.41
p1	99.9 ± 0.008902
p2	1.214e+04 ± 28.09
p3	-24.53 ± 1.243
p4	-7.916 ± 0.1457

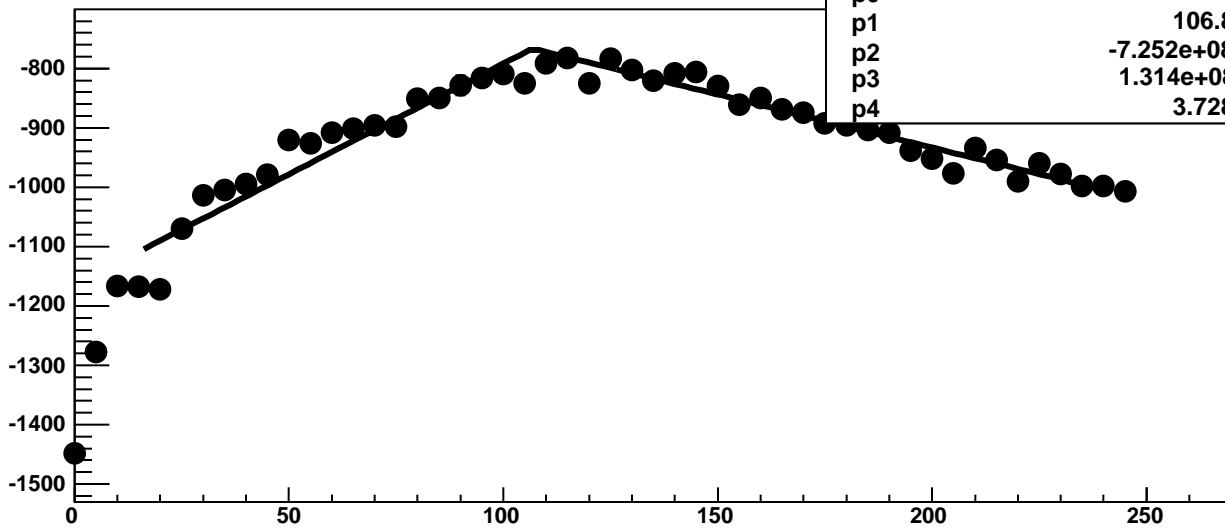
Chip 11, Channel 0, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 0, Enable 0, DAC=1600, ADC Residuals vs Hold

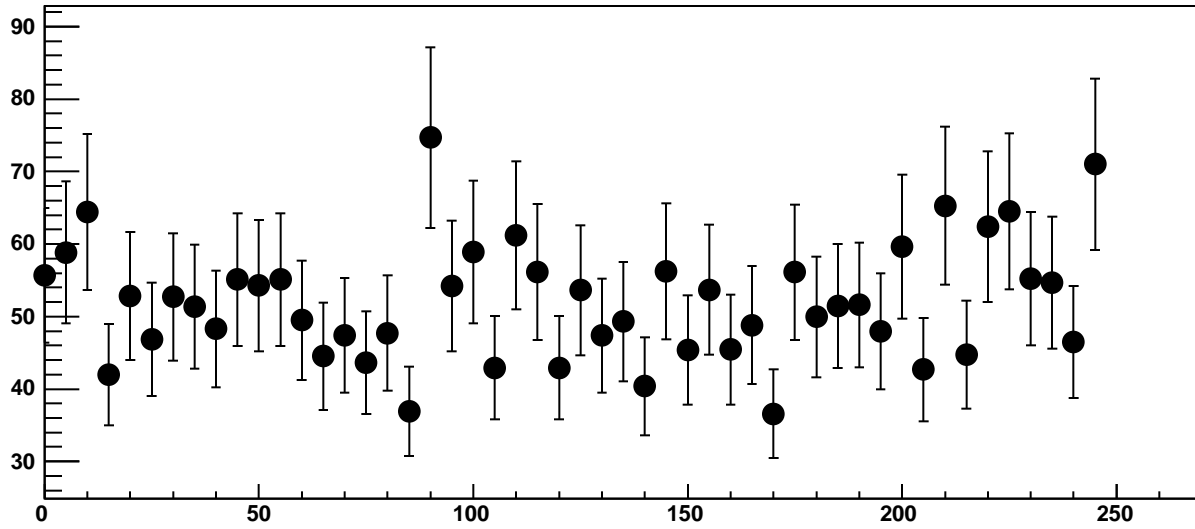


Chip 11, Channel 0, Enable 1, DAC=1600, ADC Mean vs Hold

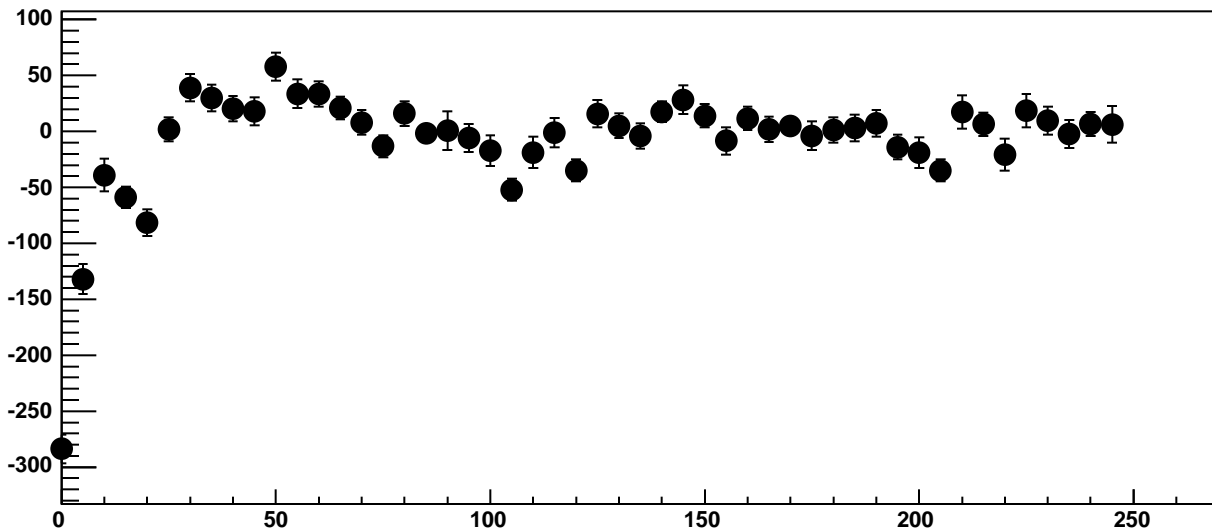


$\chi^2 / \text{ndf}$		233 / 41
p0	$-766.4 \pm$	nan
p1	$106.8 \pm$	nan
p2	$-7.252e+08 \pm$	nan
p3	$1.314e+08 \pm$	nan
p4	$3.728 \pm$	nan

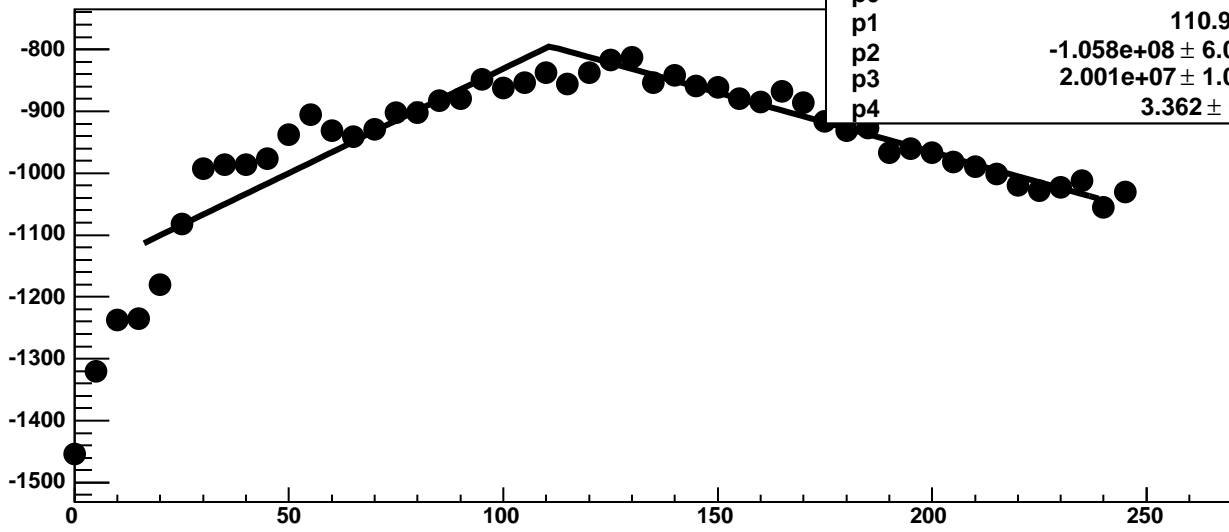
Chip 11, Channel 0, Enable 1, DAC=1600, ADC Noise vs Hold



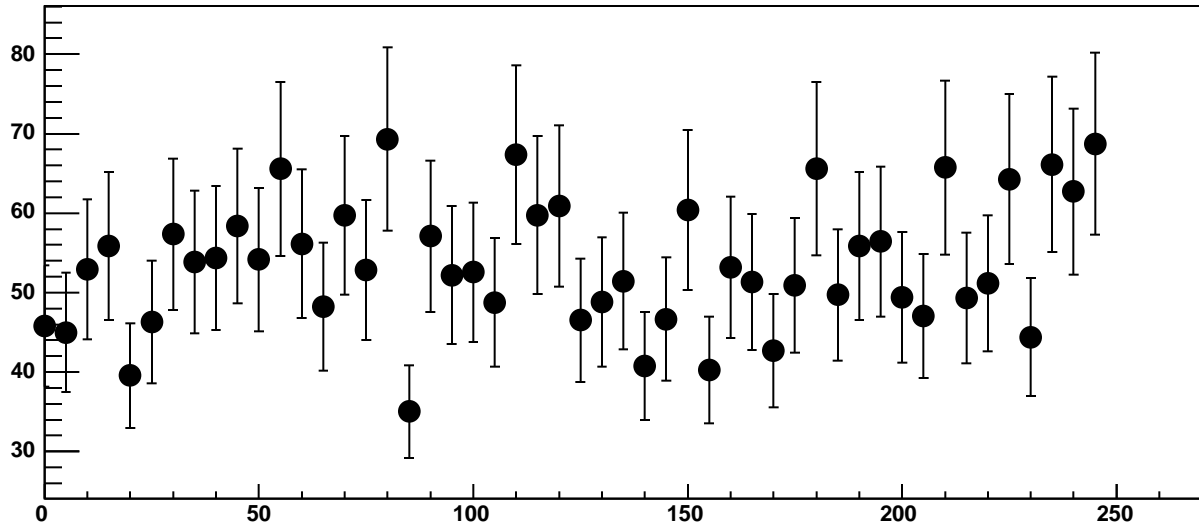
Chip 11, Channel 0, Enable 1, DAC=1600, ADC Residuals vs Hold



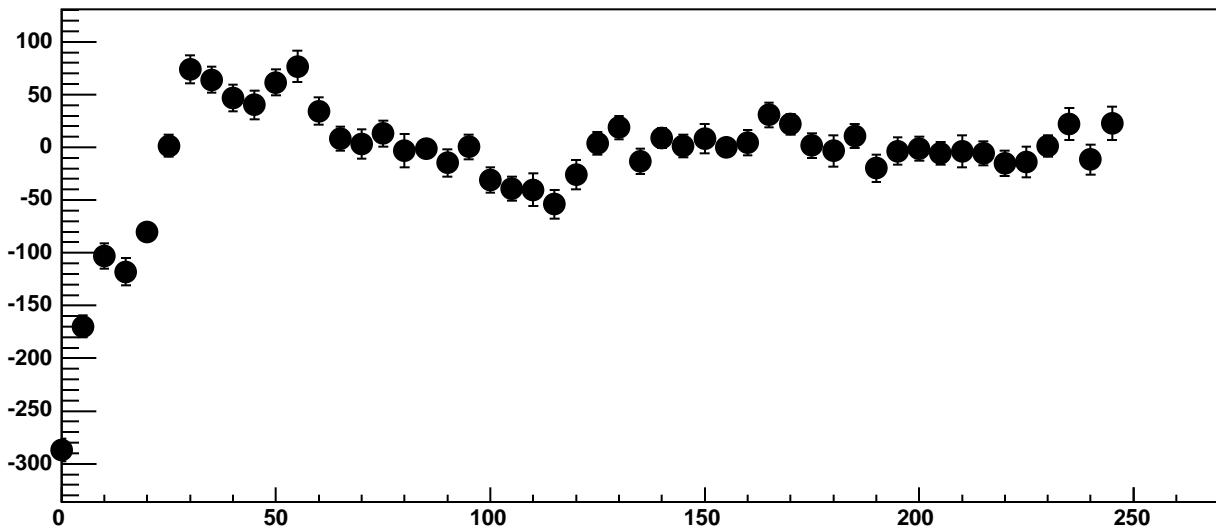
Chip 11, Channel 0, Enable 2, DAC=1600, ADC Mean vs Hold



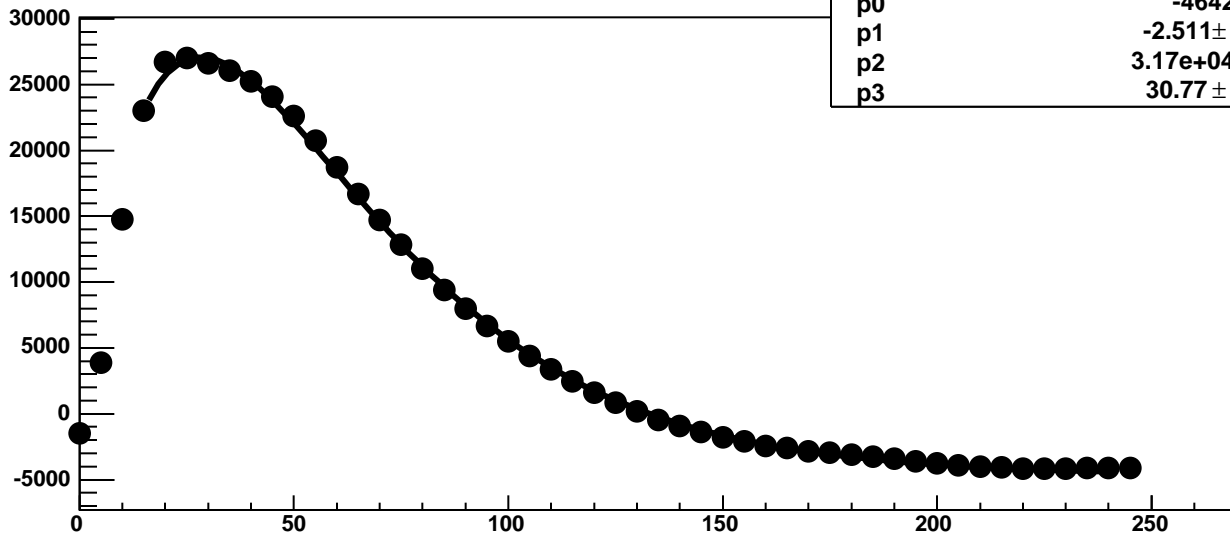
Chip 11, Channel 0, Enable 2, DAC=1600, ADC Noise vs Hold



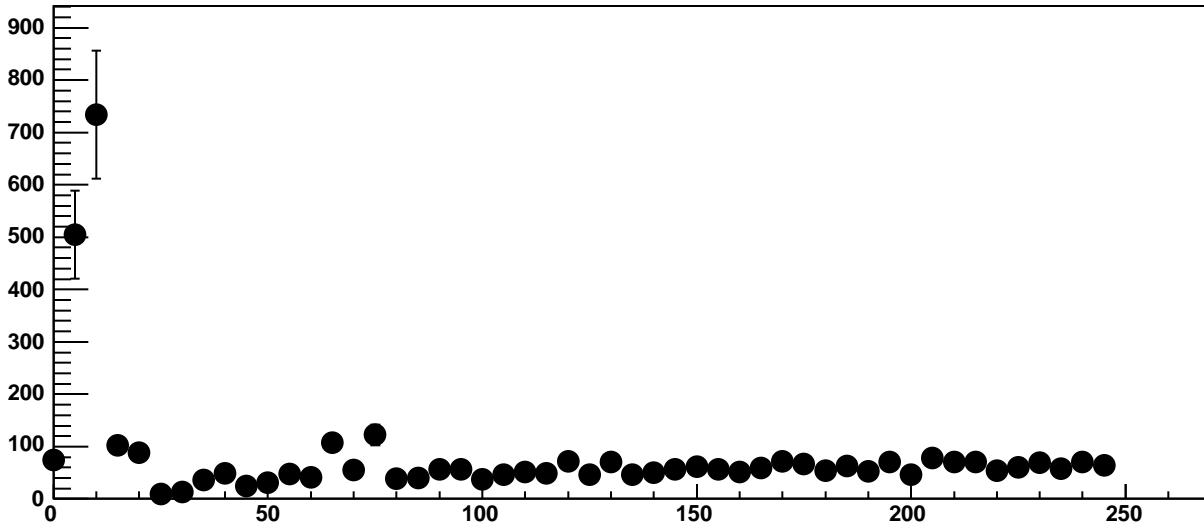
Chip 11, Channel 0, Enable 2, DAC=1600, ADC Residuals vs Hold



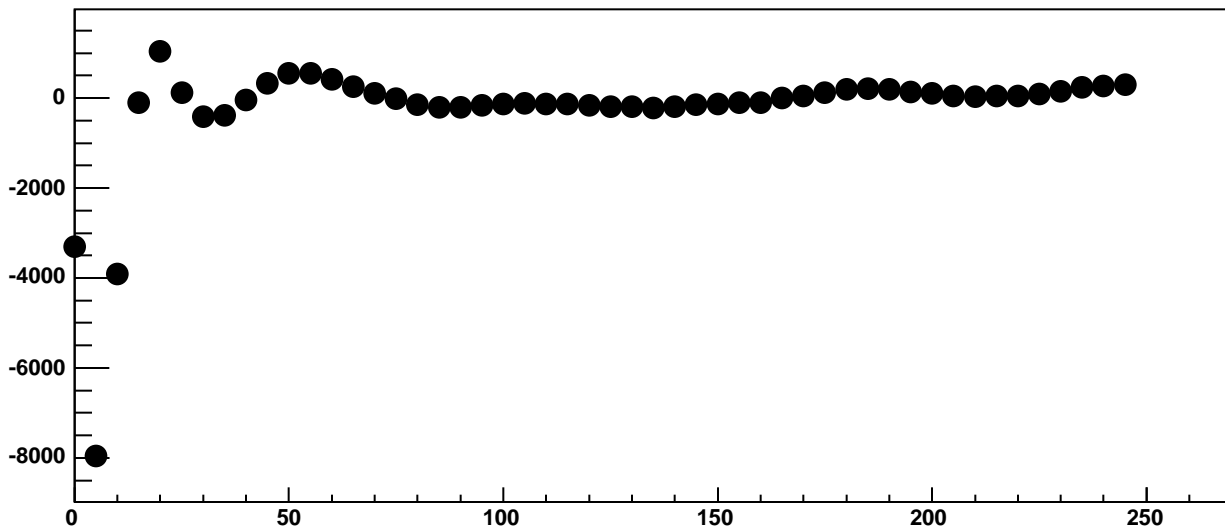
Chip 11, Channel 0, Enable 3!, DAC=1600, ADC Mean vs Hold



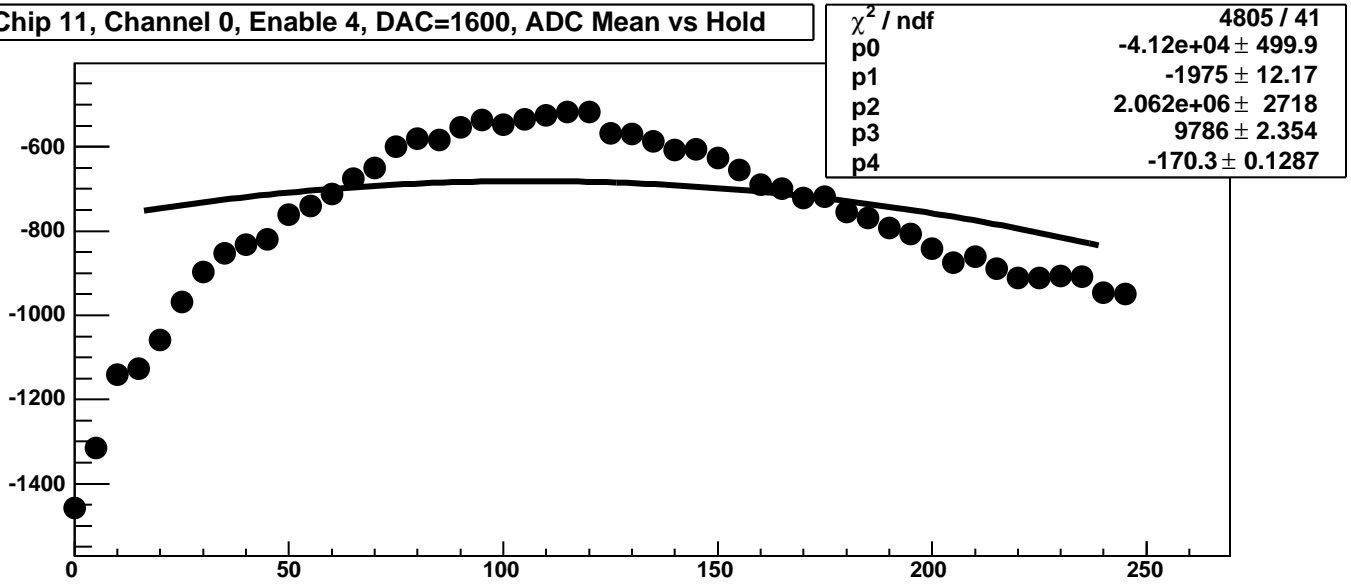
Chip 11, Channel 0, Enable 3!, DAC=1600, ADC Noise vs Hold



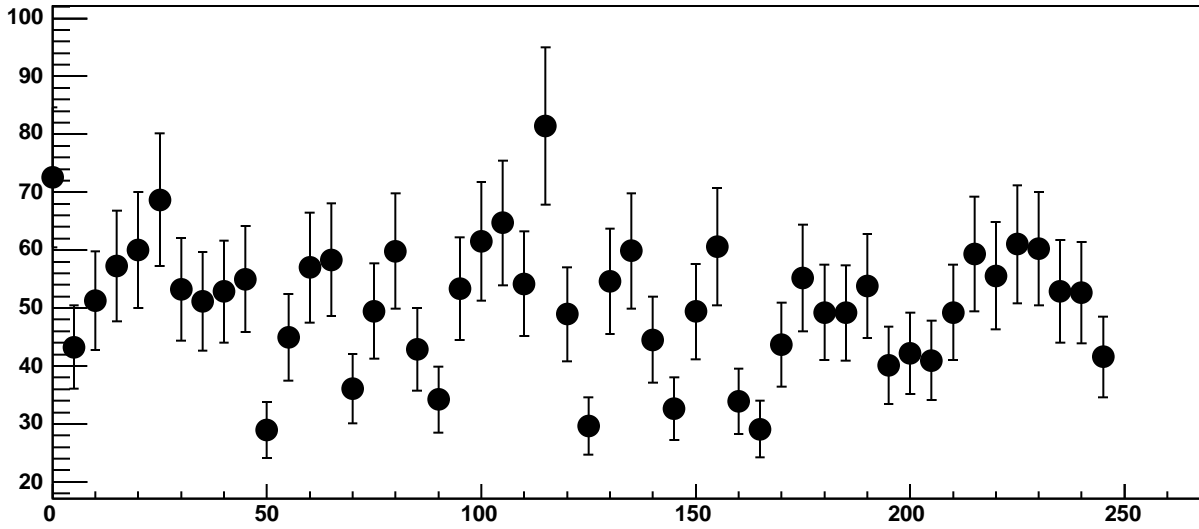
Chip 11, Channel 0, Enable 3!, DAC=1600, ADC Residuals vs Hold



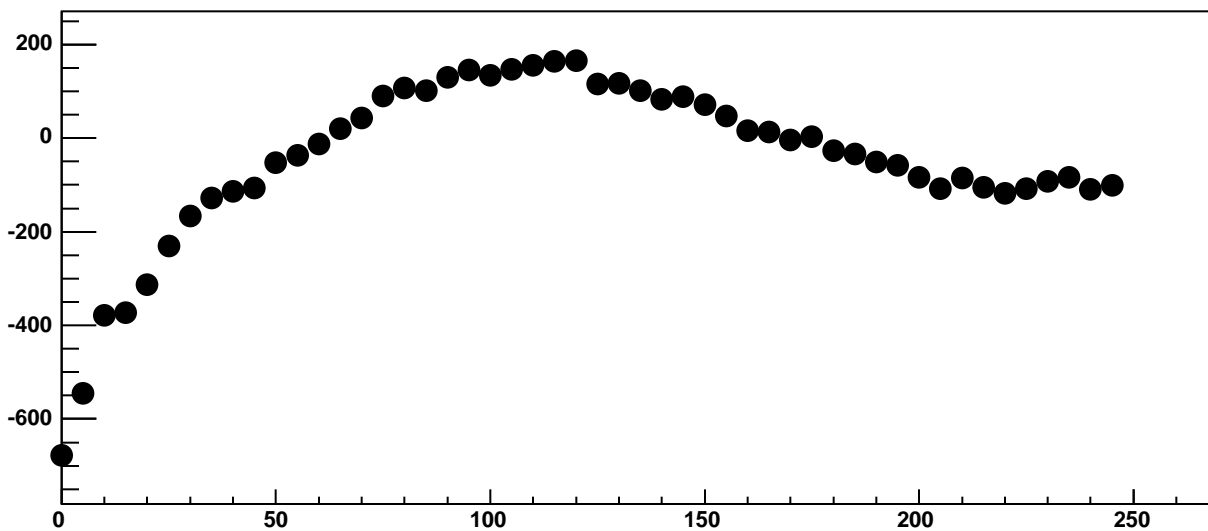
Chip 11, Channel 0, Enable 4, DAC=1600, ADC Mean vs Hold



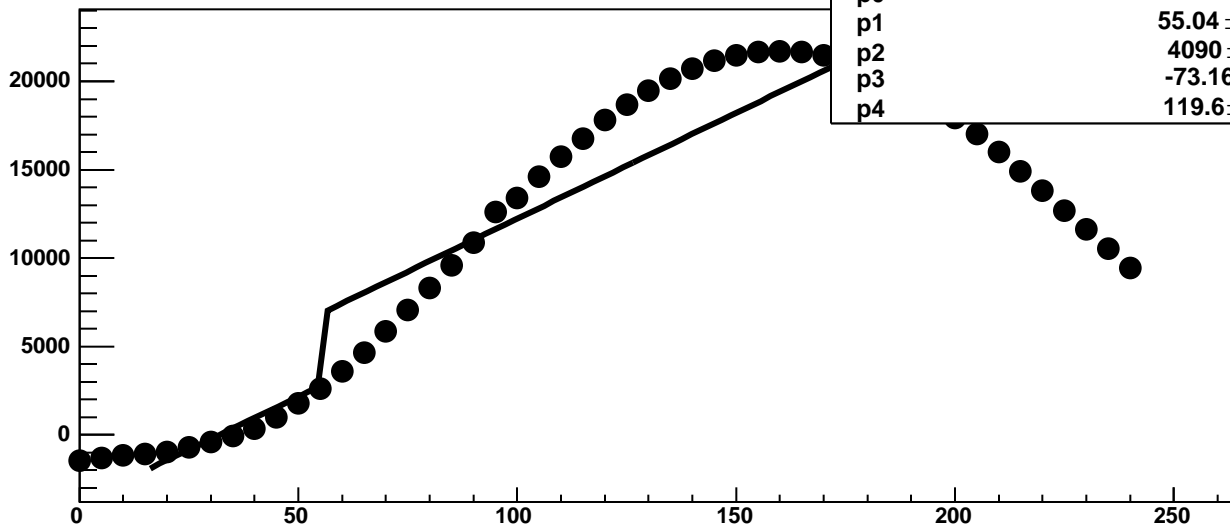
Chip 11, Channel 0, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 0, Enable 4, DAC=1600, ADC Residuals vs Hold

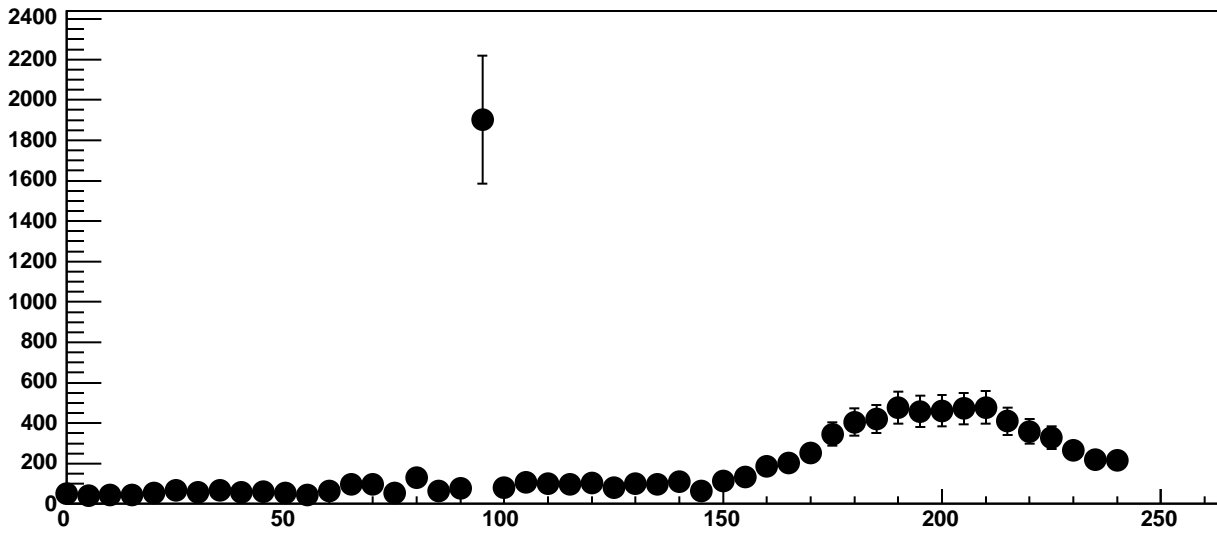


Chip 11, Channel 0, Enable 5, DAC=1600, ADC Mean vs Hold

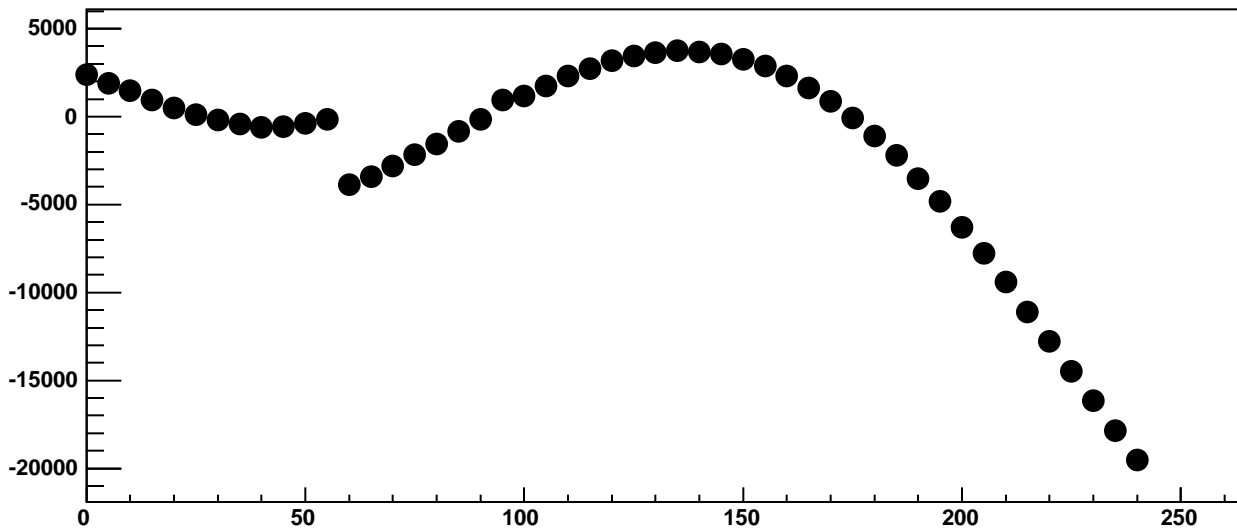


$\chi^2 / \text{ndf}$	8.513e+05 / 41
p0	2762 ± 1.124
p1	55.04 ± 0.2176
p2	4090 ± 0.9969
p3	-73.16 ± 14.03
p4	119.6 ± 0.2243

Chip 11, Channel 0, Enable 5, DAC=1600, ADC Noise vs Hold

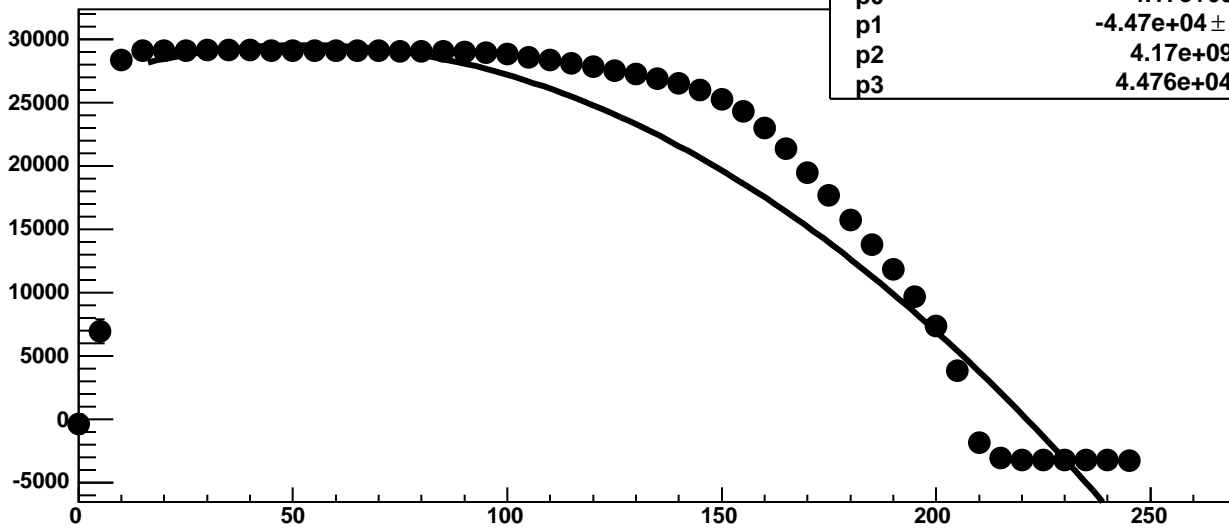


Chip 11, Channel 0, Enable 5, DAC=1600, ADC Residuals vs Hold

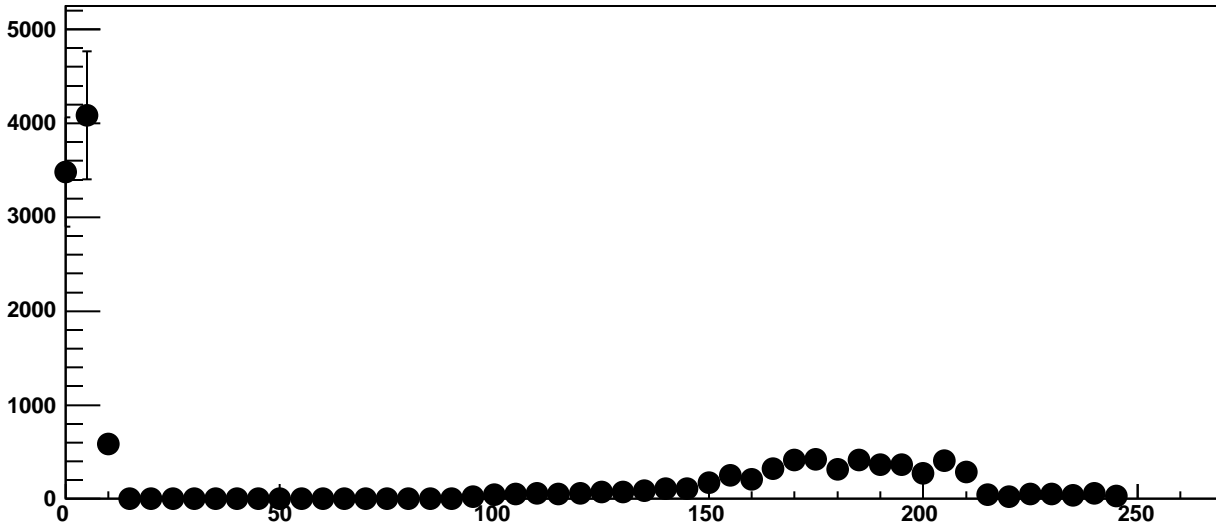




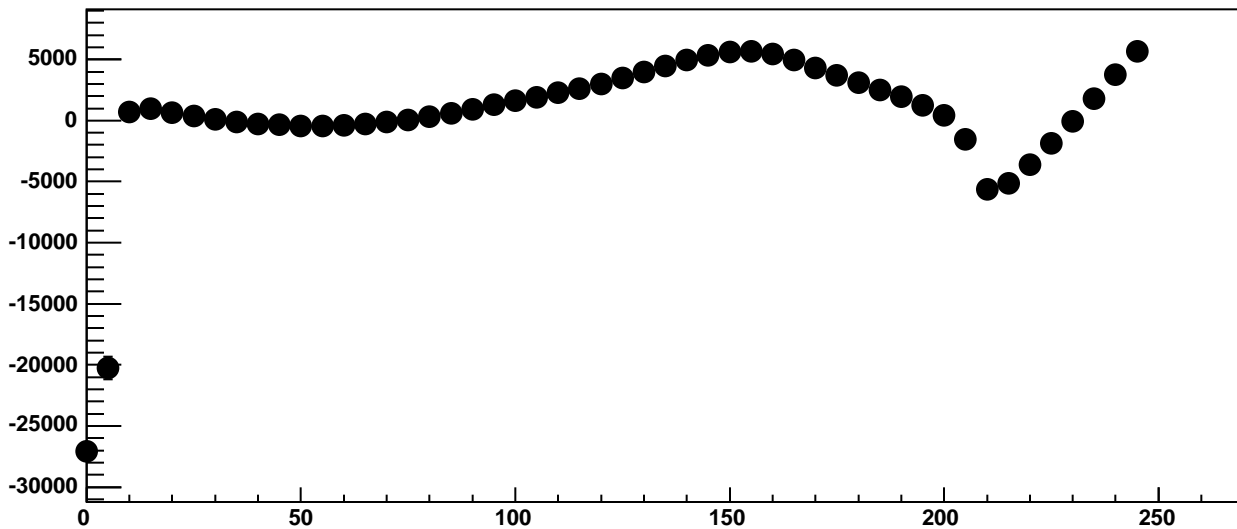
Chip 11, Channel 1, Enable 0!, DAC=1600, ADC Mean vs Hold



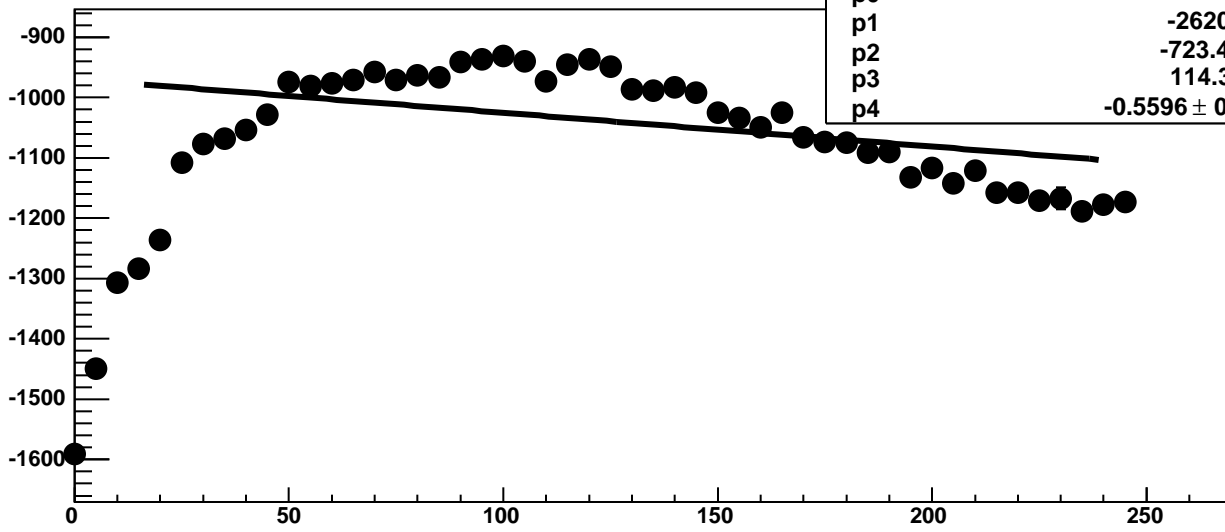
Chip 11, Channel 1, Enable 0!, DAC=1600, ADC Noise vs Hold



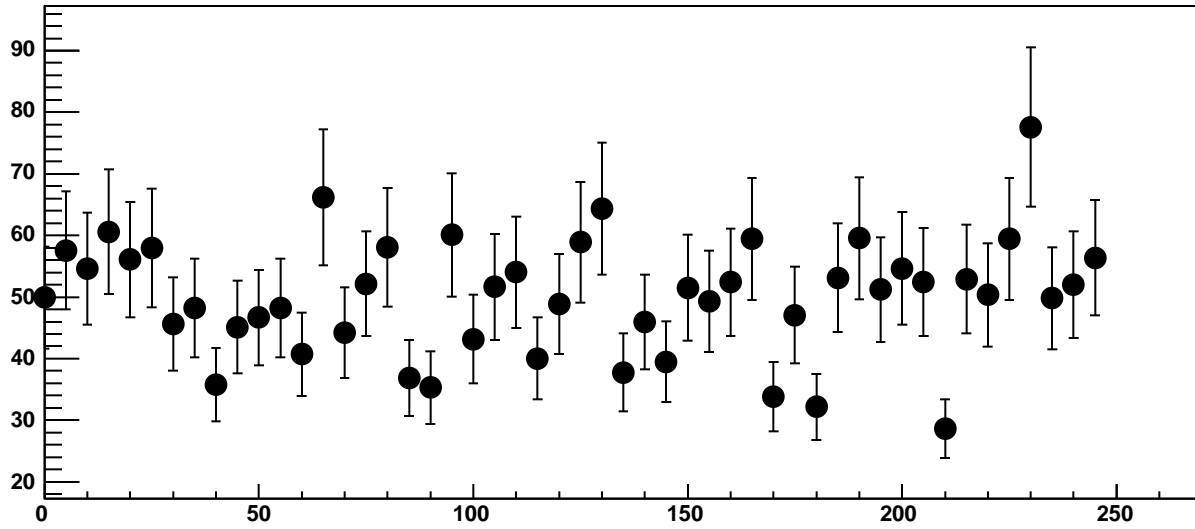
Chip 11, Channel 1, Enable 0!, DAC=1600, ADC Residuals vs Hold



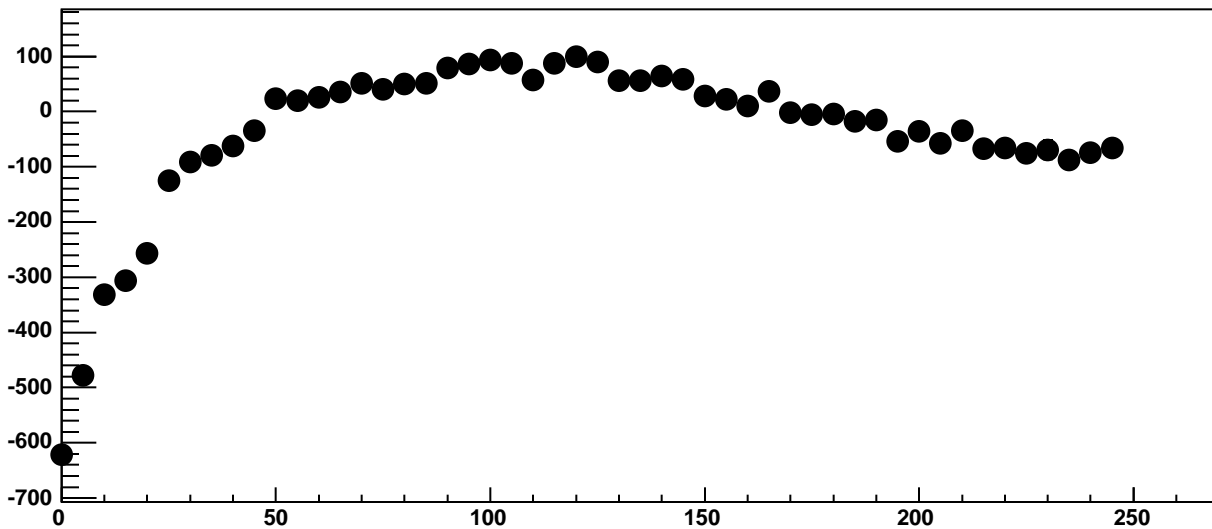
Chip 11, Channel 1, Enable 1, DAC=1600, ADC Mean vs Hold



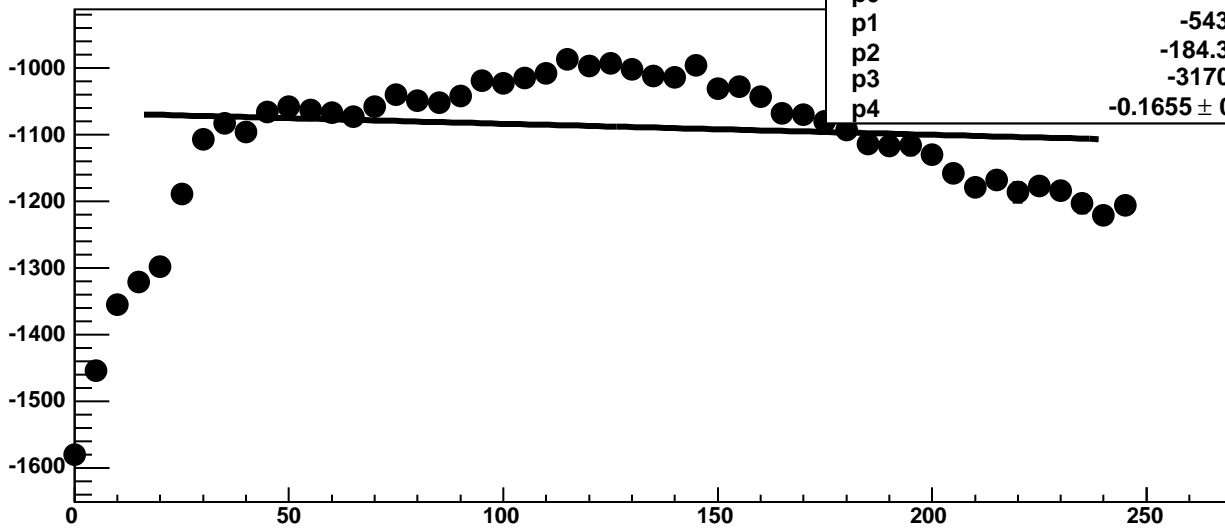
Chip 11, Channel 1, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 1, Enable 1, DAC=1600, ADC Residuals vs Hold

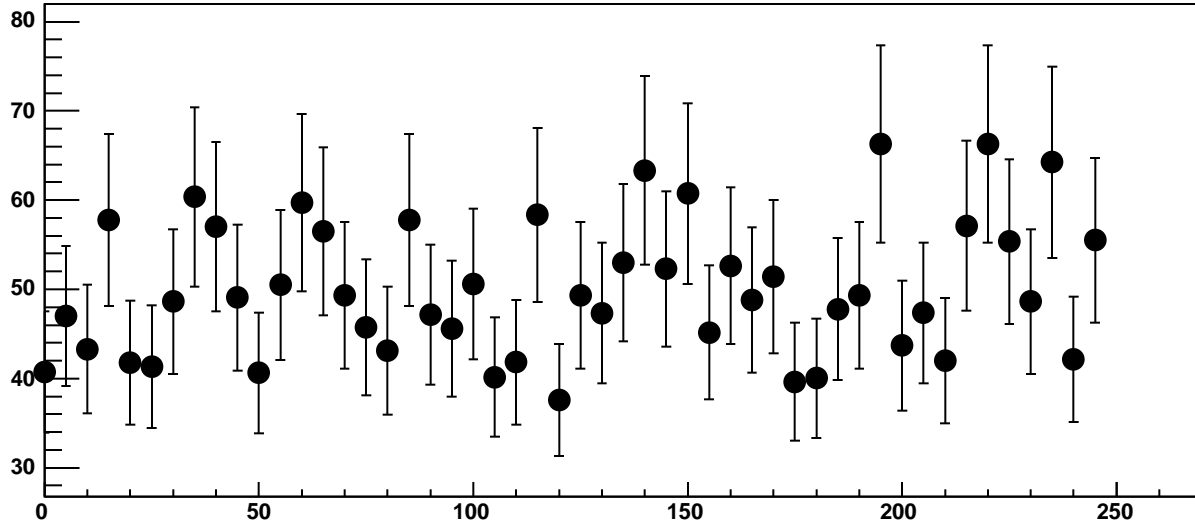


Chip 11, Channel 1, Enable 2, DAC=1600, ADC Mean vs Hold

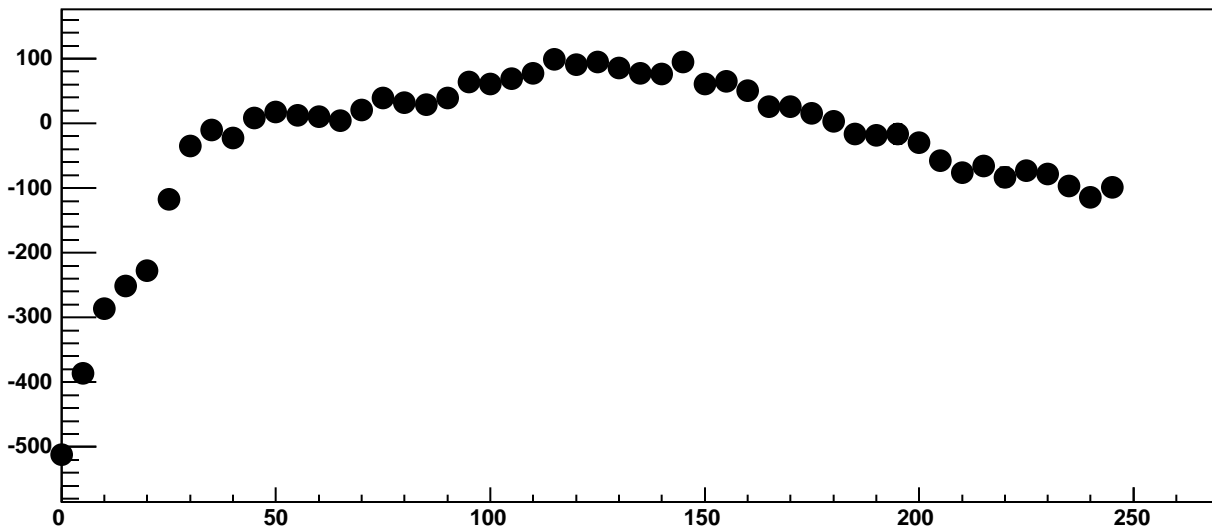


$\chi^2 / \text{ndf}$	2275 / 41
p0	$16.78 \pm 7.515$
p1	$-5436 \pm 55$
p2	$-184.3 \pm 7.755$
p3	$-3170 \pm 2827$
p4	$-0.1655 \pm 0.001351$

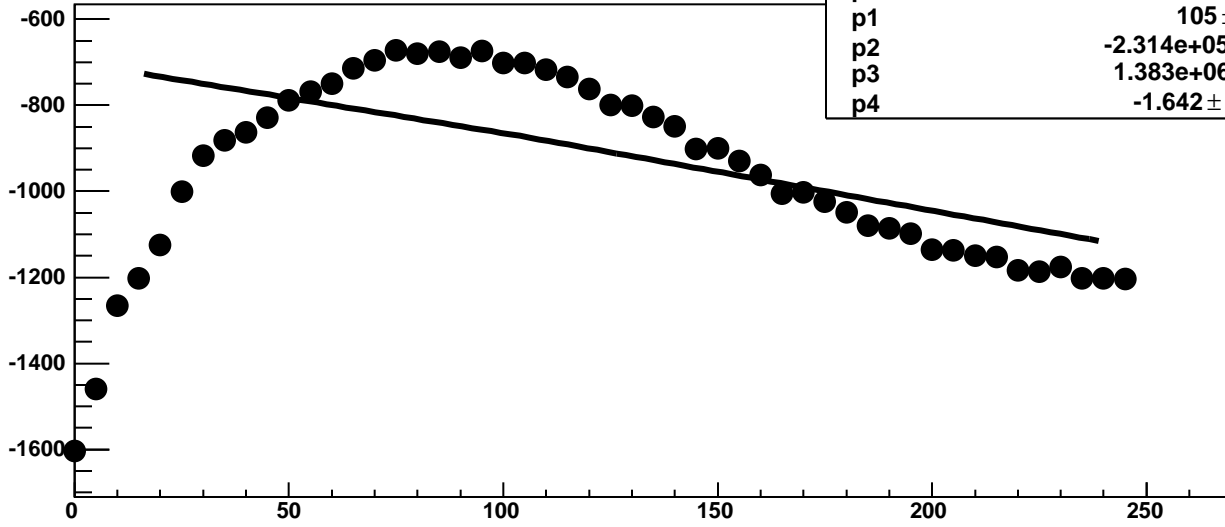
Chip 11, Channel 1, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 1, Enable 2, DAC=1600, ADC Residuals vs Hold

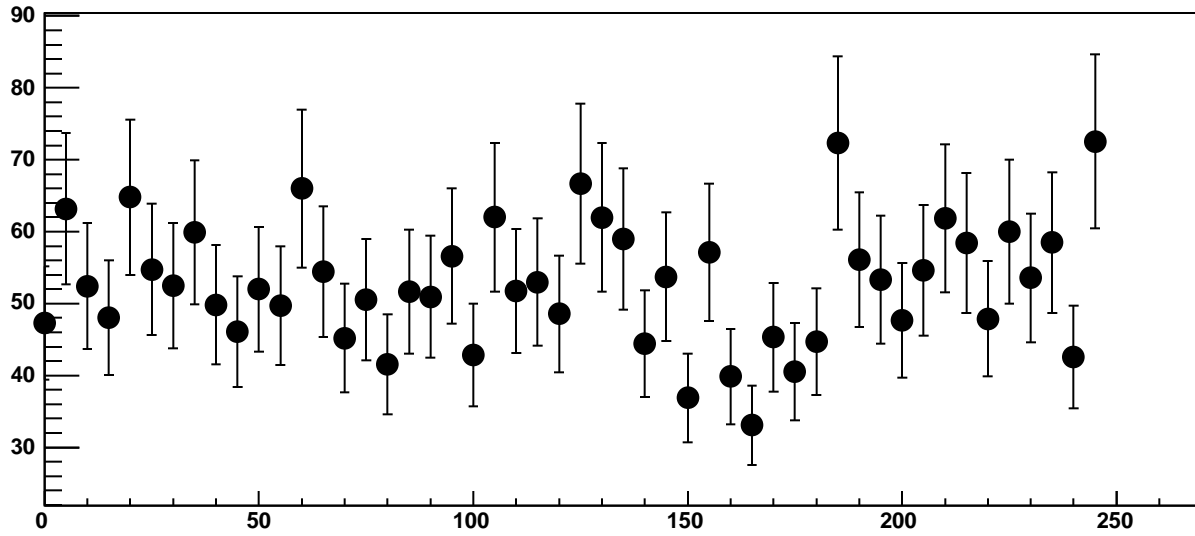


Chip 11, Channel 1, Enable 3, DAC=1600, ADC Mean vs Hold

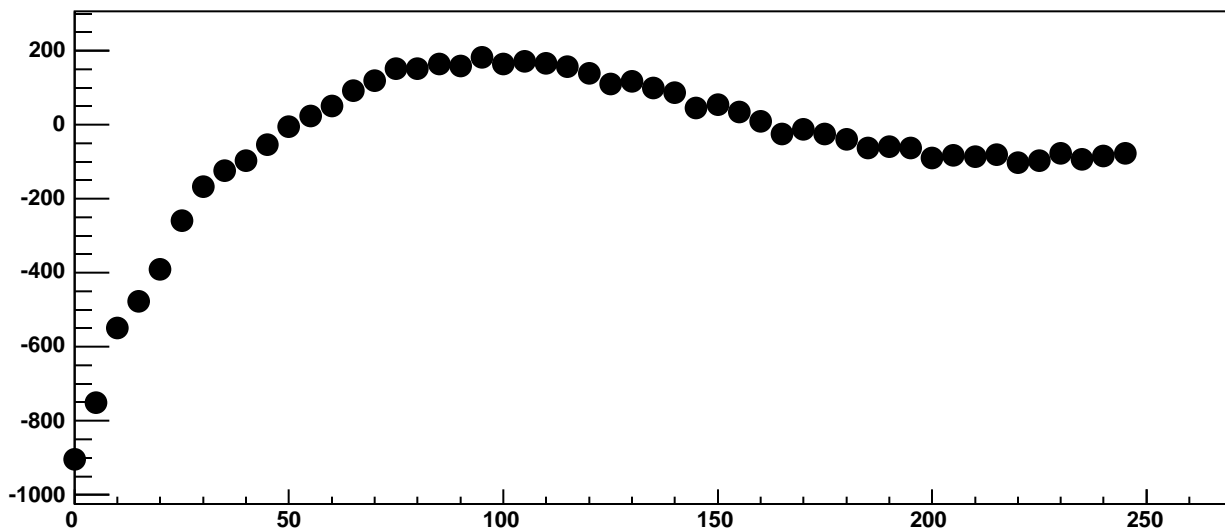


$\chi^2 / \text{ndf}$	6395 / 41
p0	$-873.2 \pm 1.128$
p1	$105 \pm 0.2762$
p2	$-2.314e+05 \pm 1.426$
p3	$1.383e+06 \pm 1.415$
p4	$-1.642 \pm 0.02534$

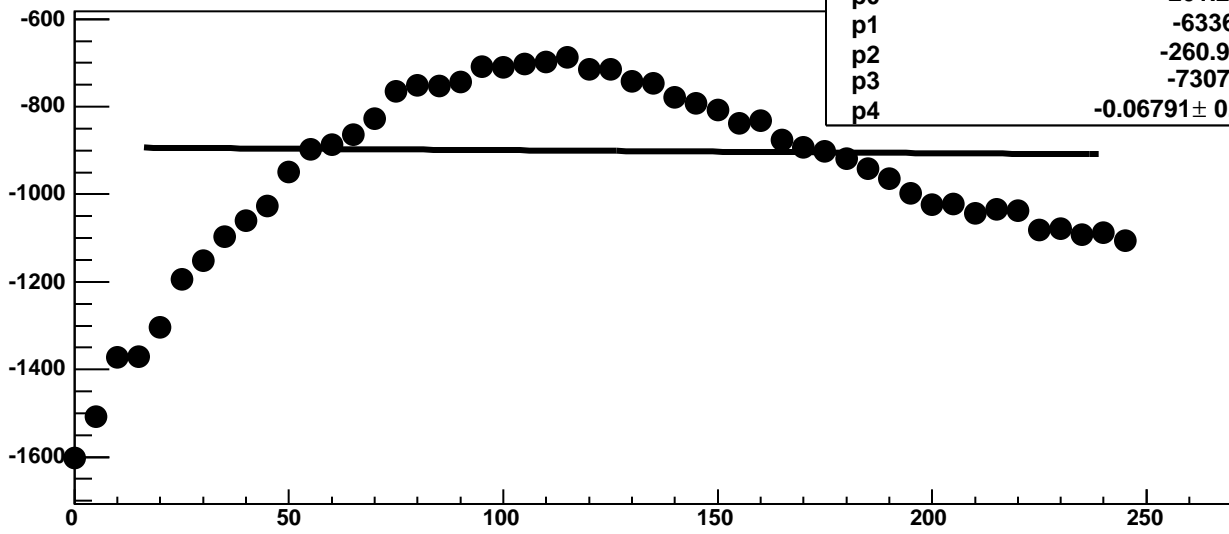
Chip 11, Channel 1, Enable 3, DAC=1600, ADC Noise vs Hold



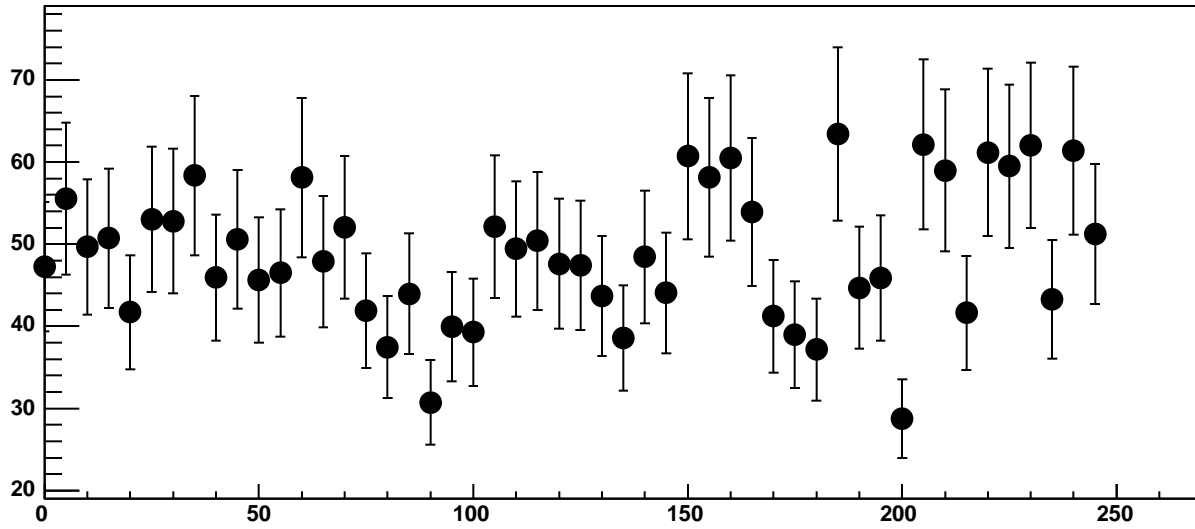
Chip 11, Channel 1, Enable 3, DAC=1600, ADC Residuals vs Hold



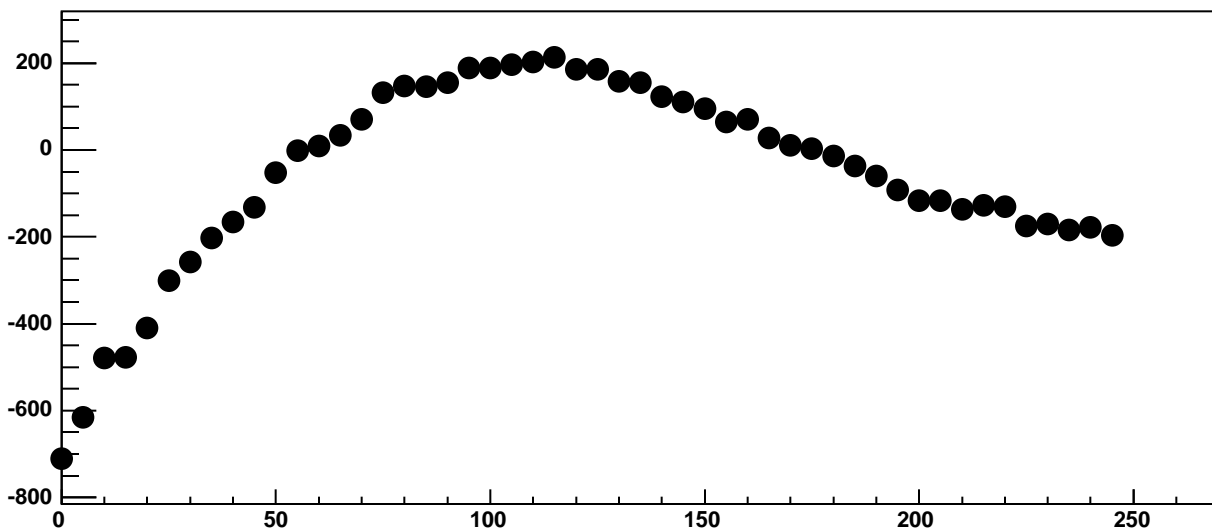
Chip 11, Channel 1, Enable 4, DAC=1600, ADC Mean vs Hold



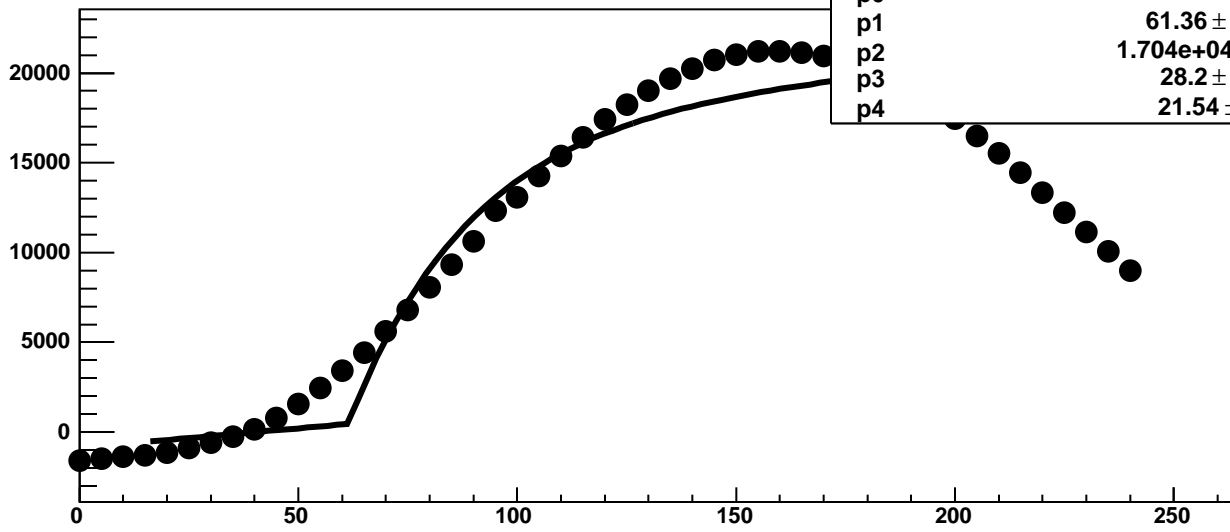
Chip 11, Channel 1, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 1, Enable 4, DAC=1600, ADC Residuals vs Hold

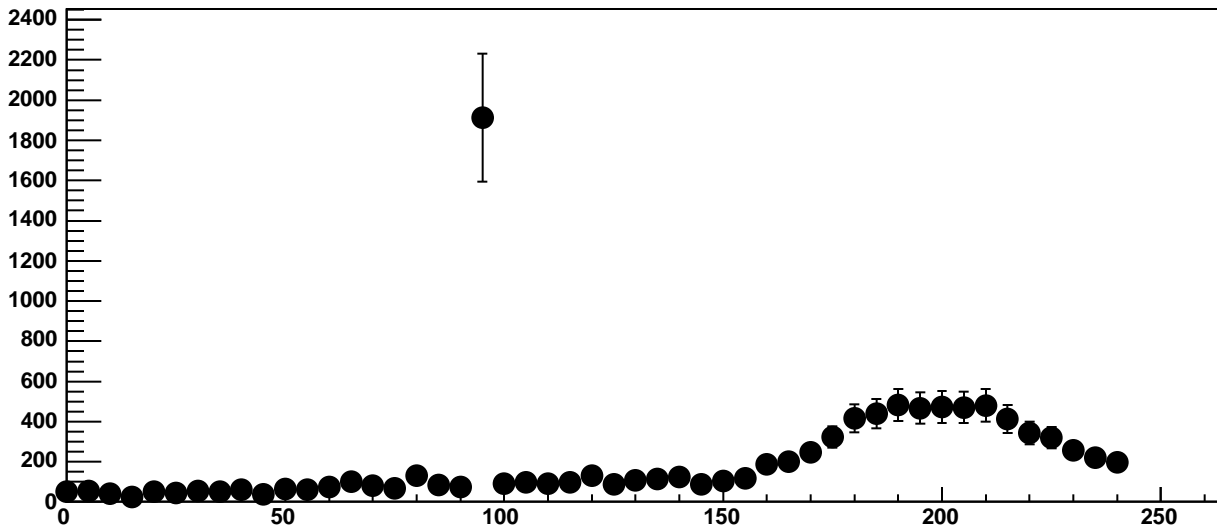


Chip 11, Channel 1, Enable 5, DAC=1600, ADC Mean vs Hold

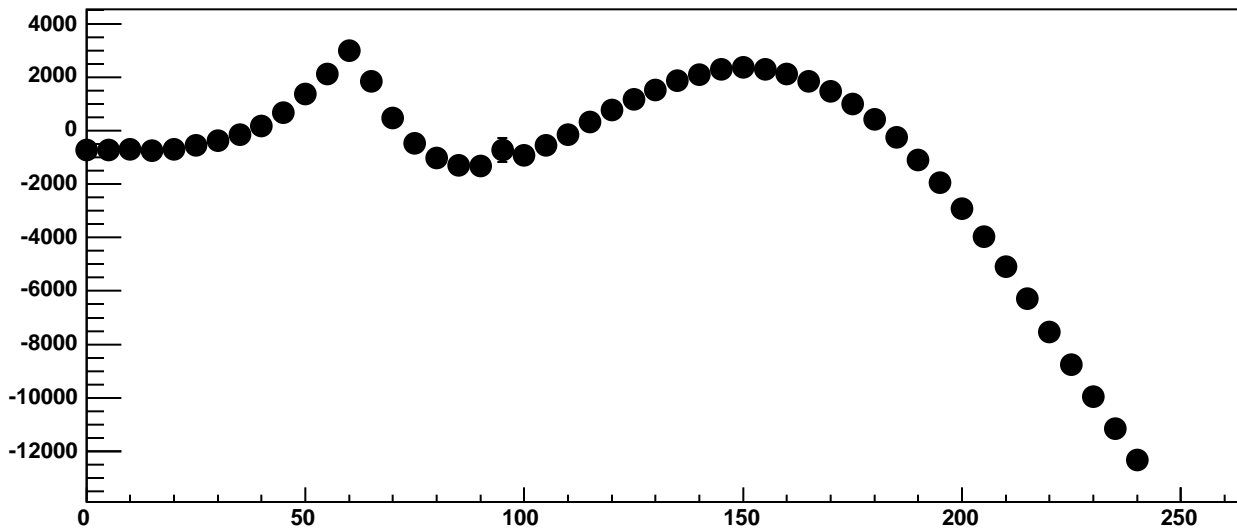


$\chi^2 / \text{ndf}$	3.494e+05 / 41
p0	453 ± 6.732
p1	61.36 ± 0.03249
p2	1.704e+04 ± 27.13
p3	28.2 ± 0.06674
p4	21.54 ± 0.1795

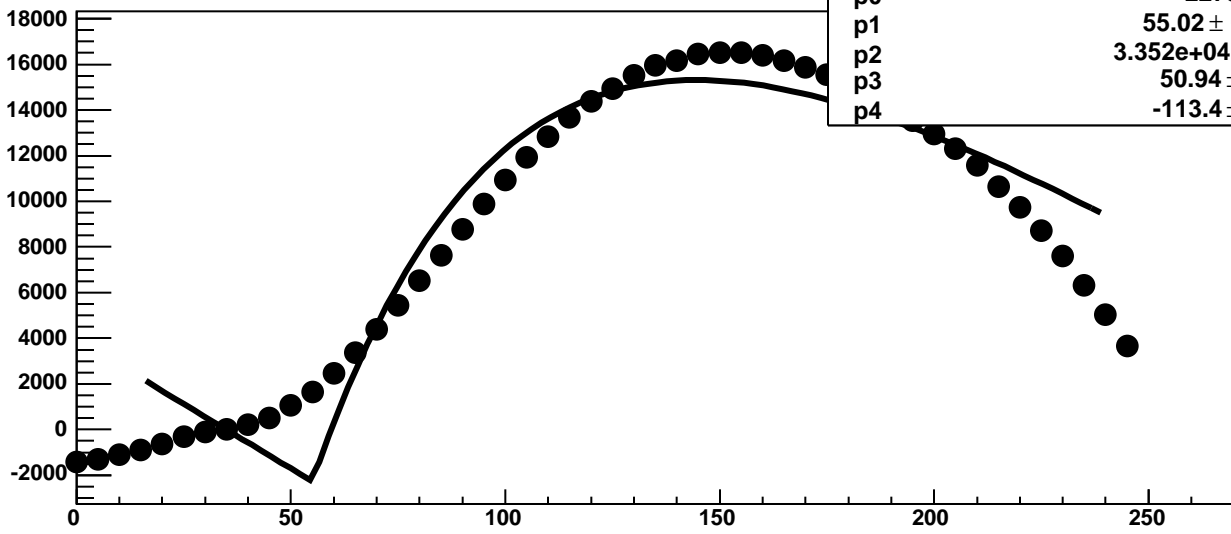
Chip 11, Channel 1, Enable 5, DAC=1600, ADC Noise vs Hold



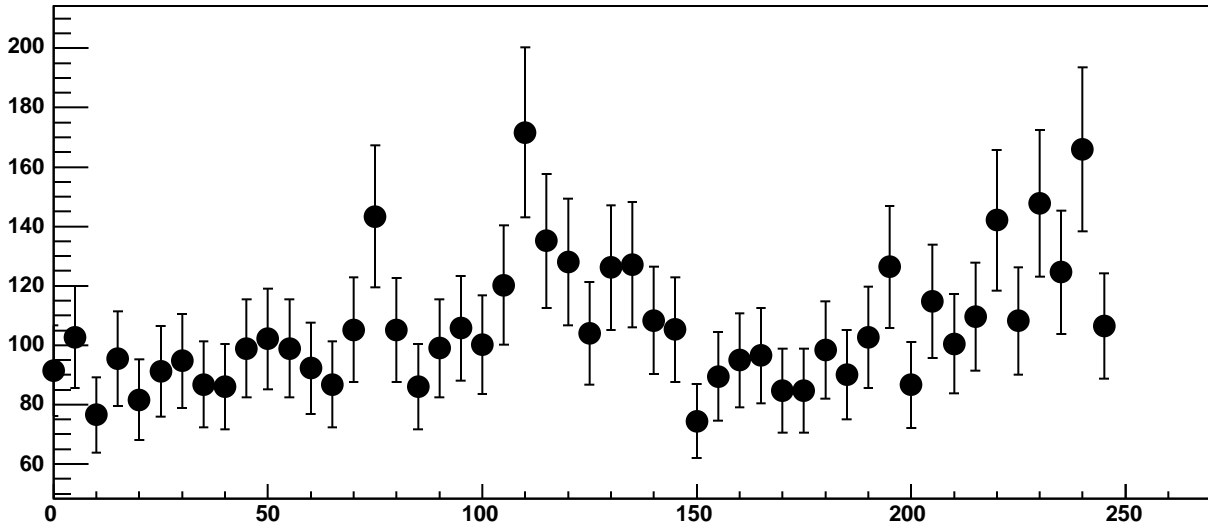
Chip 11, Channel 1, Enable 5, DAC=1600, ADC Residuals vs Hold



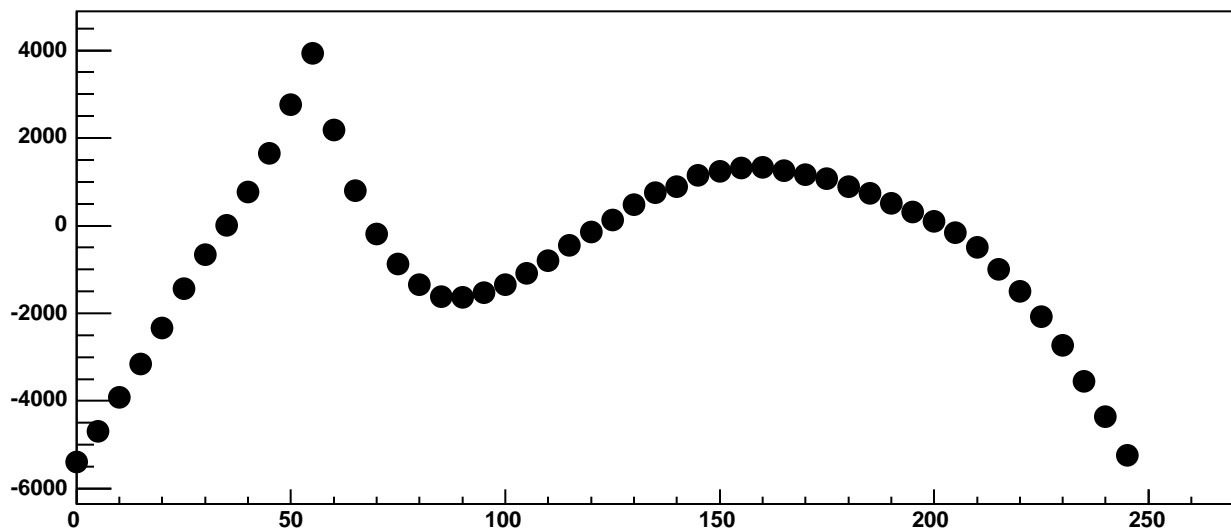
Chip 11, Channel 2, Enable 0, DAC=1600, ADC Mean vs Hold



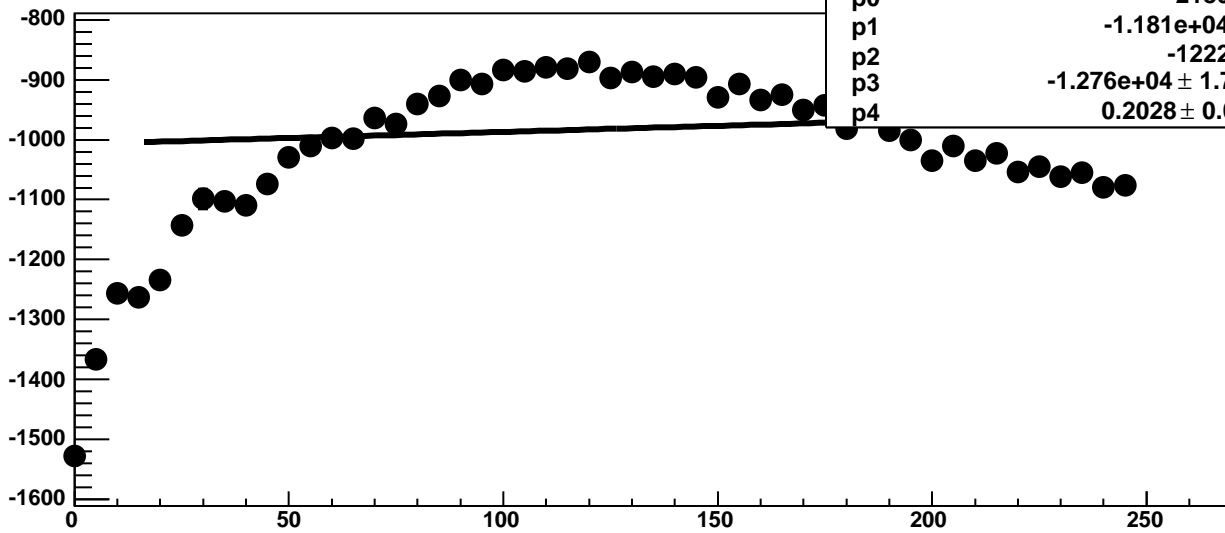
Chip 11, Channel 2, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 2, Enable 0, DAC=1600, ADC Residuals vs Hold

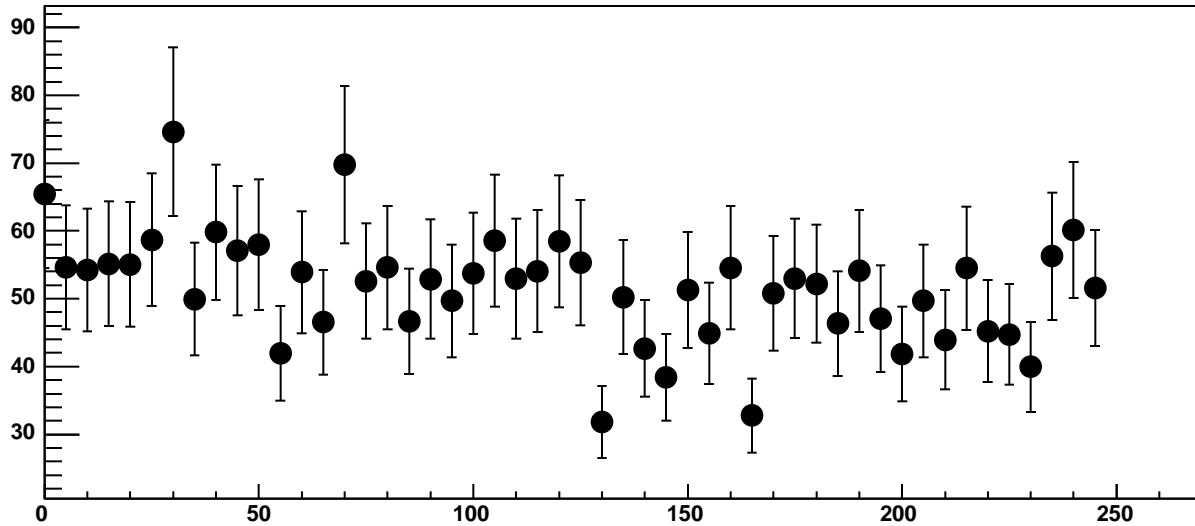


Chip 11, Channel 2, Enable 1, DAC=1600, ADC Mean vs Hold

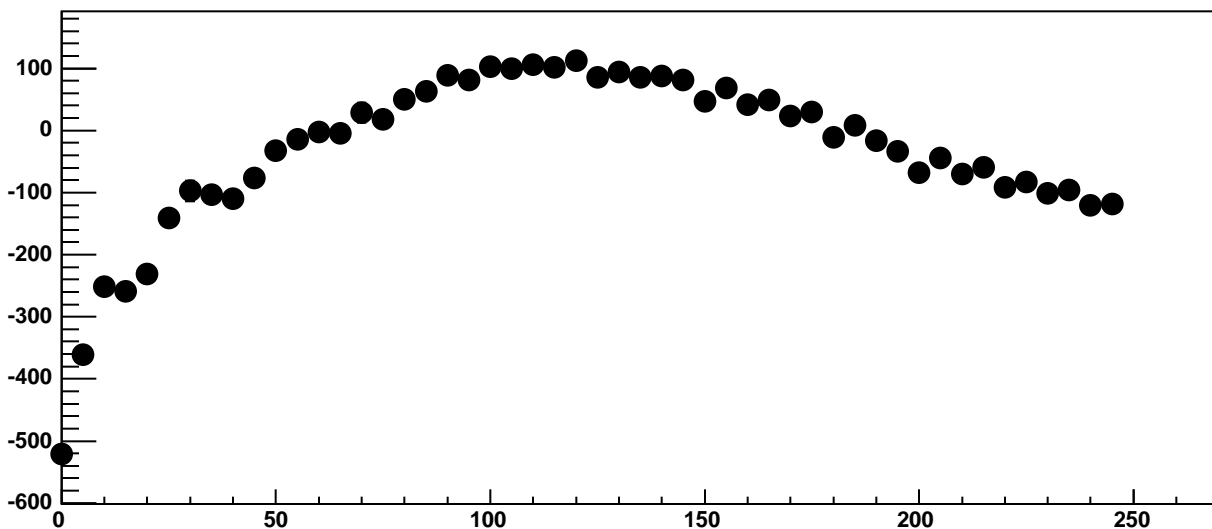


$\chi^2 / \text{ndf}$	2682 / 41
p0	-2180 ± 6.014
p1	-1.181e+04 ± 28.56
p2	-1222 ± 5.942
p3	-1.276e+04 ± 1.739e+05
p4	0.2028 ± 0.0005027

Chip 11, Channel 2, Enable 1, DAC=1600, ADC Noise vs Hold

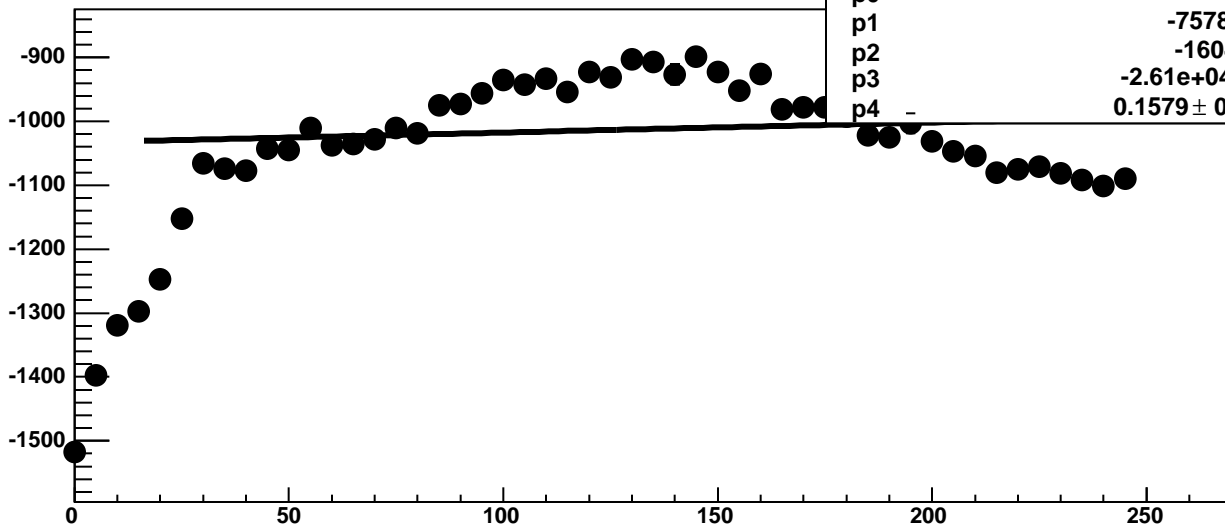


Chip 11, Channel 2, Enable 1, DAC=1600, ADC Residuals vs Hold



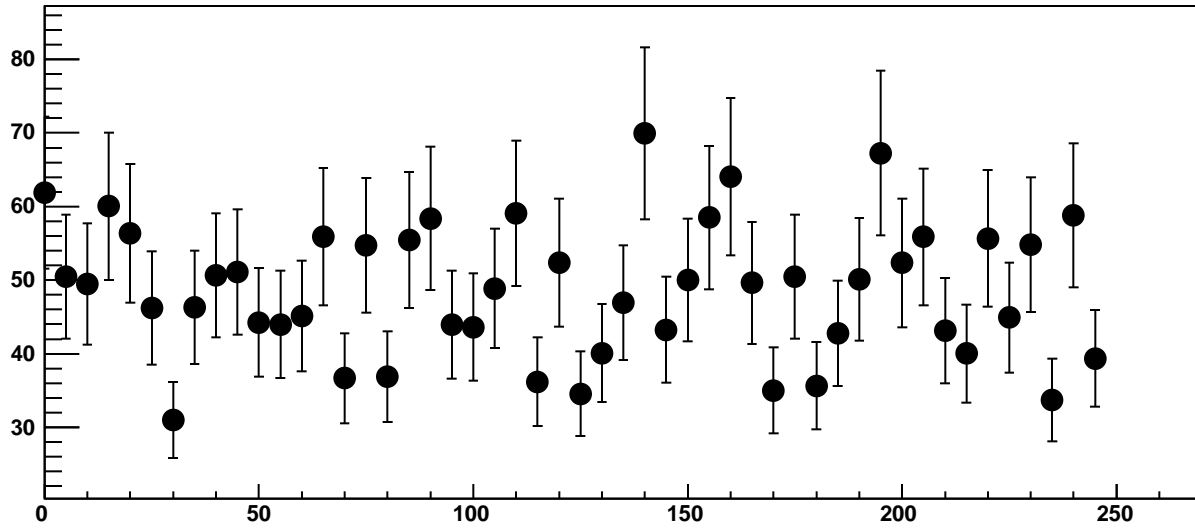


Chip 11, Channel 2, Enable 2, DAC=1600, ADC Mean vs Hold

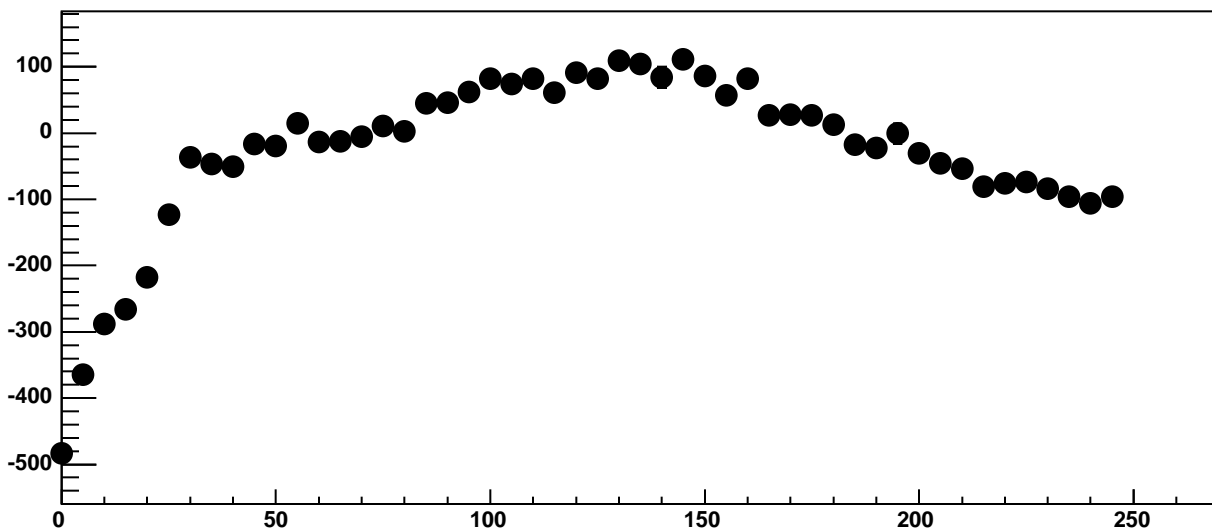


$\chi^2 / \text{ndf}$	2301 / 41
p0	$-625.8 \pm 7.989$
p1	$-7578 \pm 40.29$
p2	$-1604 \pm 10.1$
p3	$-2.61\text{e}+04 \pm 1841$
p4	$0.1579 \pm 0.001037$

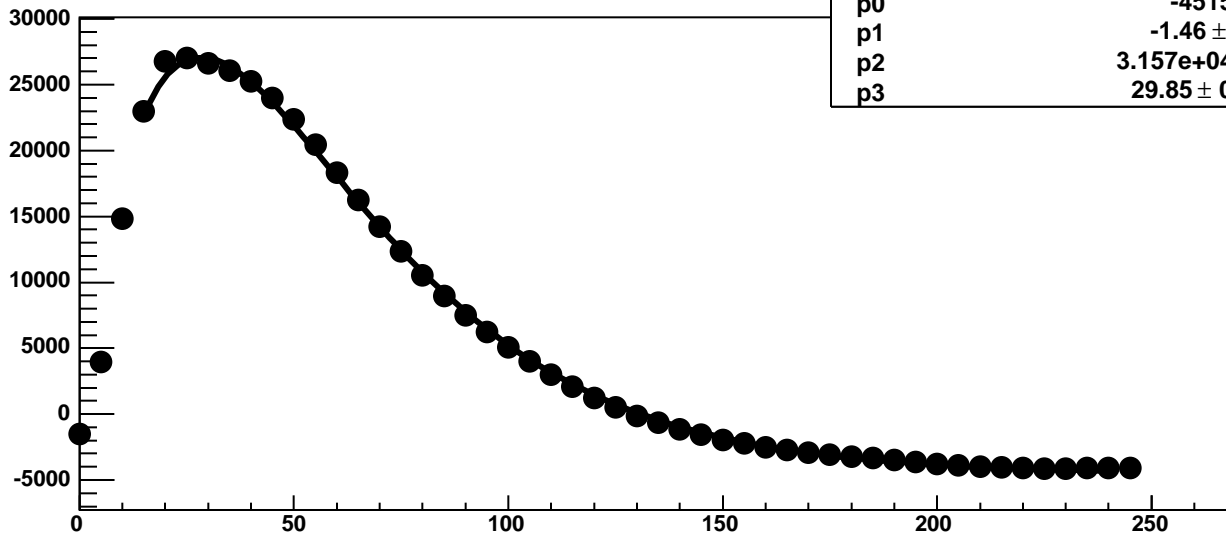
Chip 11, Channel 2, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 2, Enable 2, DAC=1600, ADC Residuals vs Hold

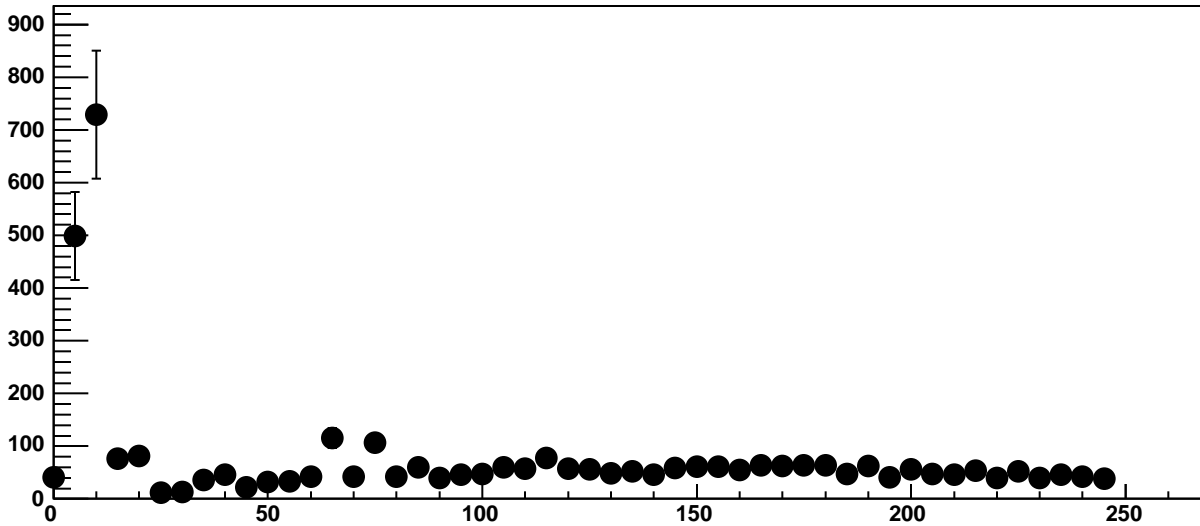


Chip 11, Channel 2, Enable 3!, DAC=1600, ADC Mean vs Hold

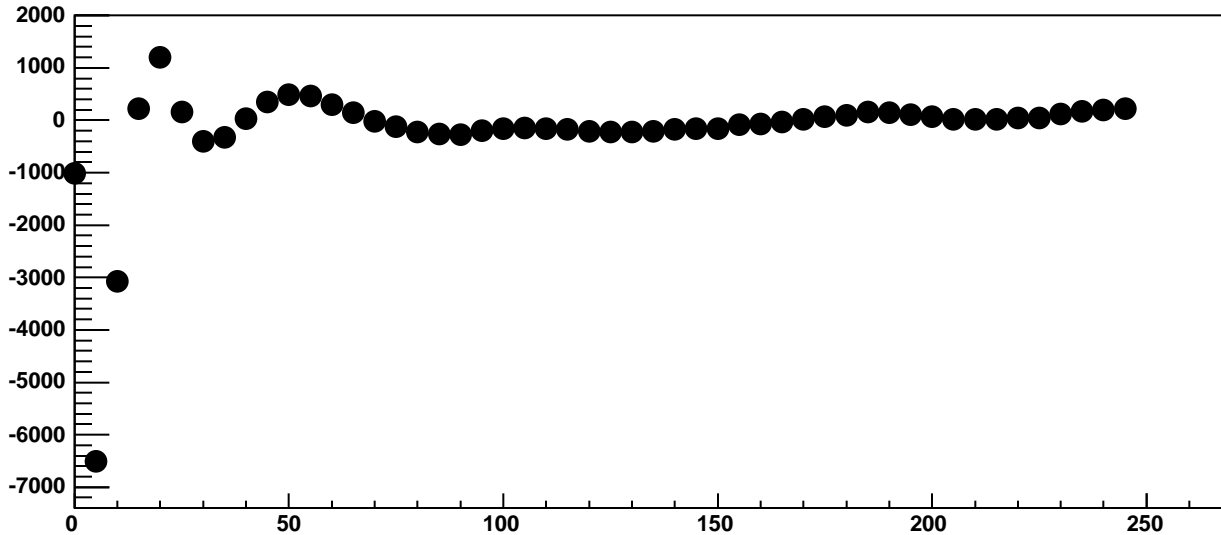


$\chi^2 / \text{ndf}$	4.721e+04 / 42
p0	-4515 $\pm$ 3.217
p1	-1.46 $\pm$ 0.01695
p2	3.157e+04 $\pm$ 3.475
p3	29.85 $\pm$ 0.009618

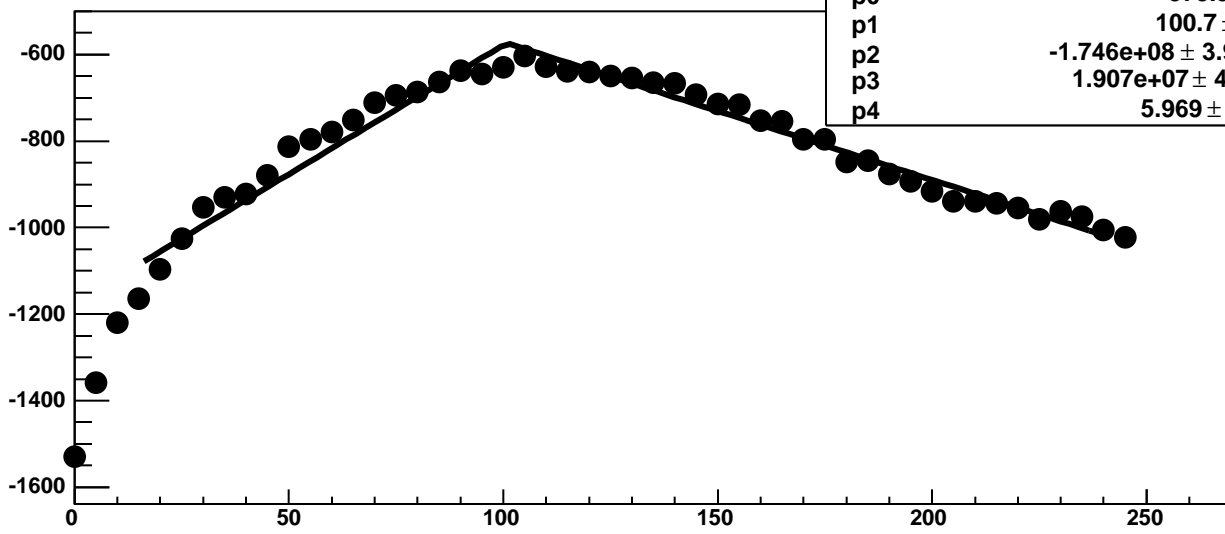
Chip 11, Channel 2, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 2, Enable 3!, DAC=1600, ADC Residuals vs Hold

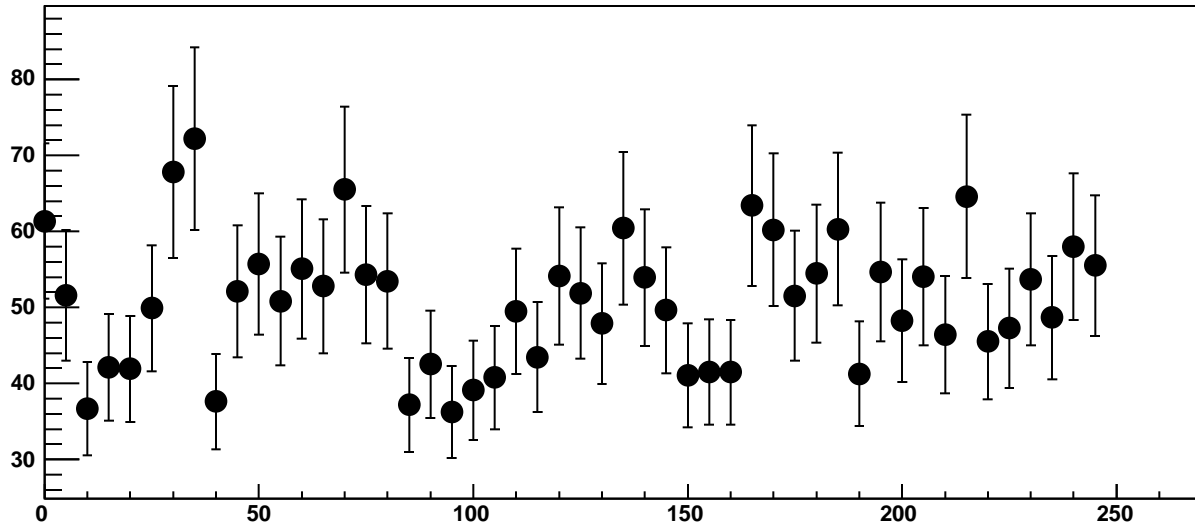


Chip 11, Channel 2, Enable 4, DAC=1600, ADC Mean vs Hold

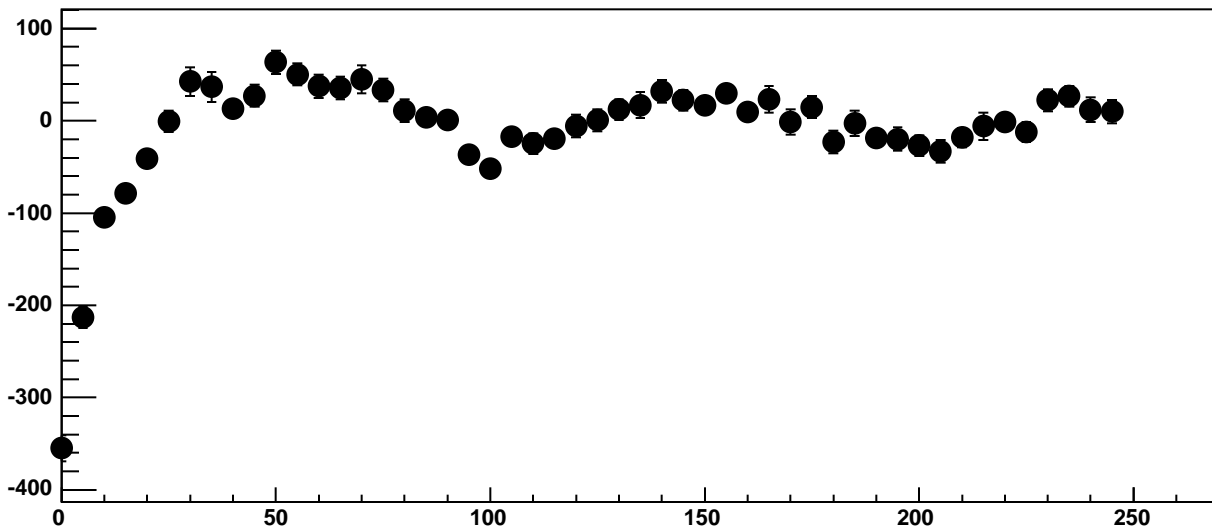


$\chi^2 / \text{ndf}$	315.5 / 41
p0	$-573.5 \pm 3.167$
p1	$100.7 \pm 0.6819$
p2	$-1.746\text{e}+08 \pm 3.953\text{e}+06$
p3	$1.907\text{e}+07 \pm 4.06\text{e}+05$
p4	$5.969 \pm 0.09034$

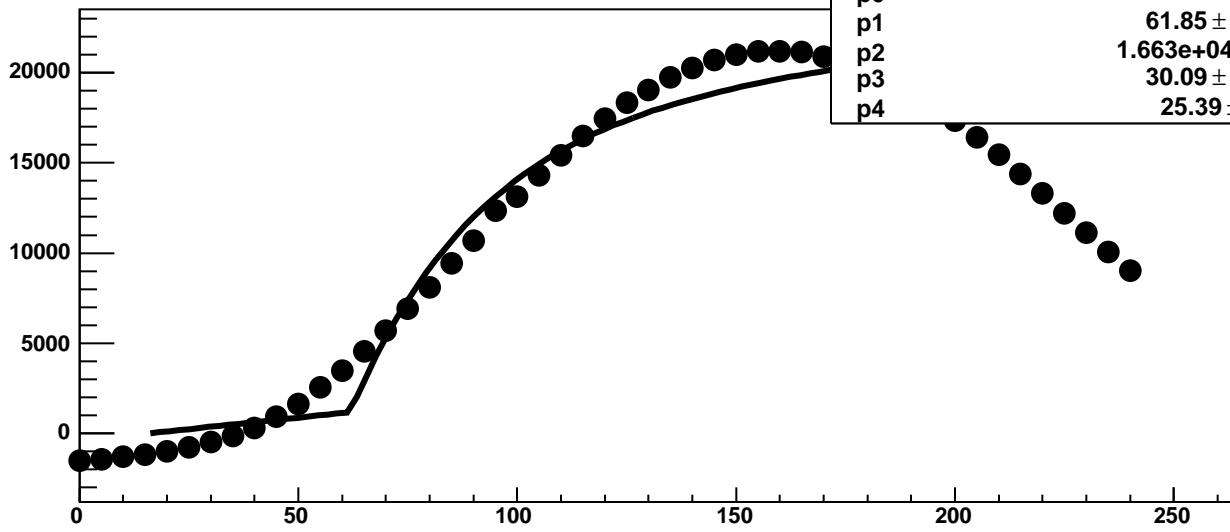
Chip 11, Channel 2, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 2, Enable 4, DAC=1600, ADC Residuals vs Hold

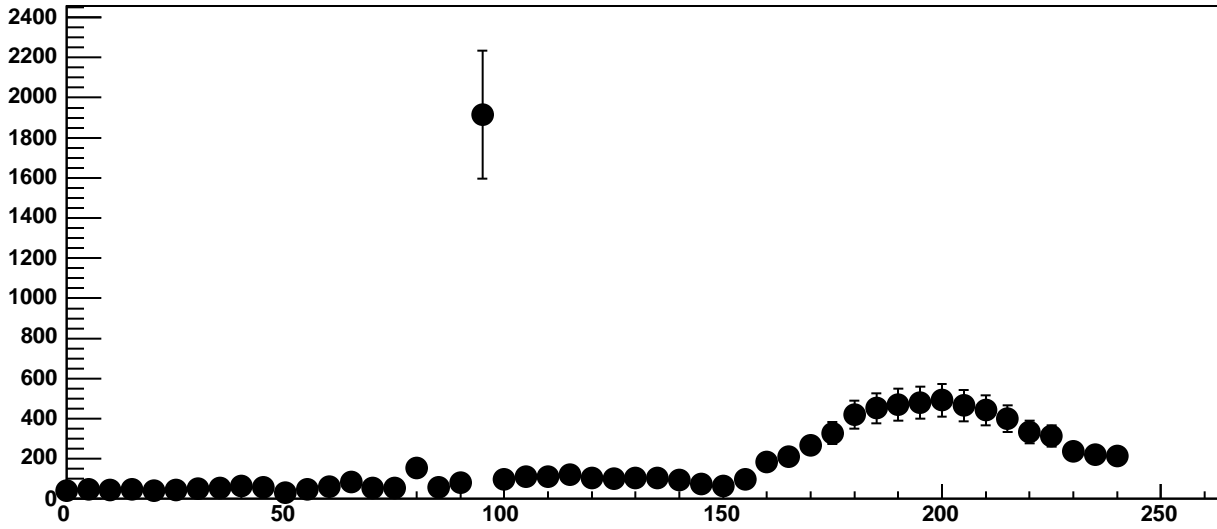


Chip 11, Channel 2, Enable 5, DAC=1600, ADC Mean vs Hold

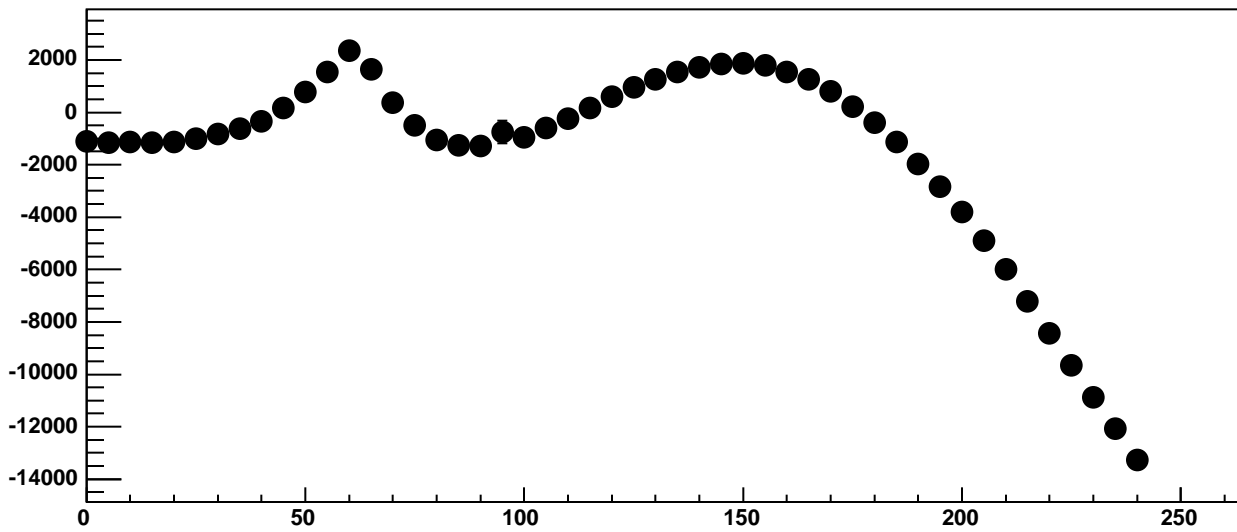


$\chi^2 / \text{ndf}$	3.882e+05 / 41
p0	1173 ± 5.906
p1	61.85 ± 0.02703
p2	1.663e+04 ± 26.69
p3	30.09 ± 0.06726
p4	25.39 ± 0.1849

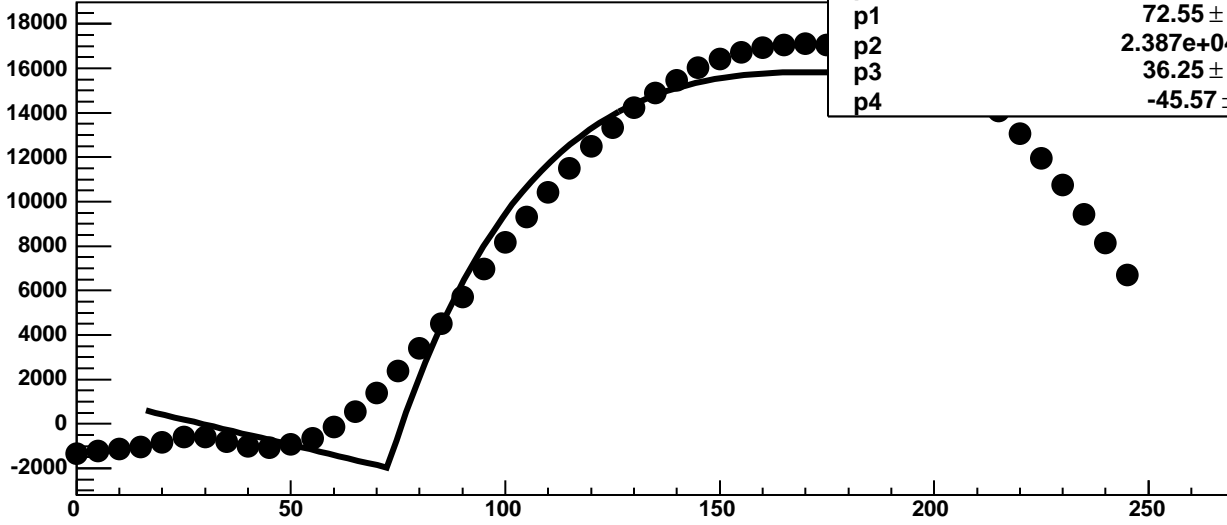
Chip 11, Channel 2, Enable 5, DAC=1600, ADC Noise vs Hold



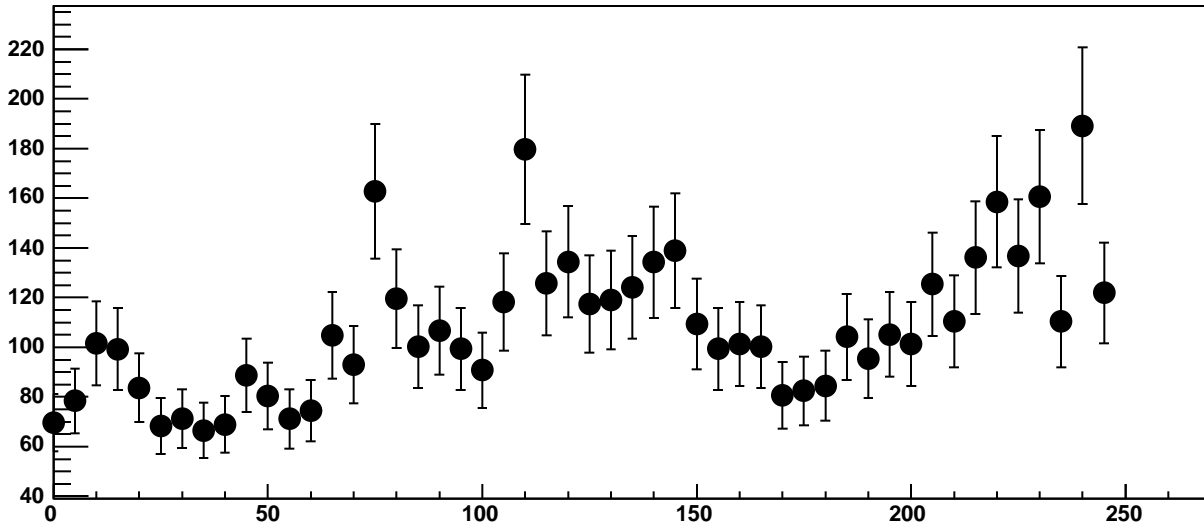
Chip 11, Channel 2, Enable 5, DAC=1600, ADC Residuals vs Hold



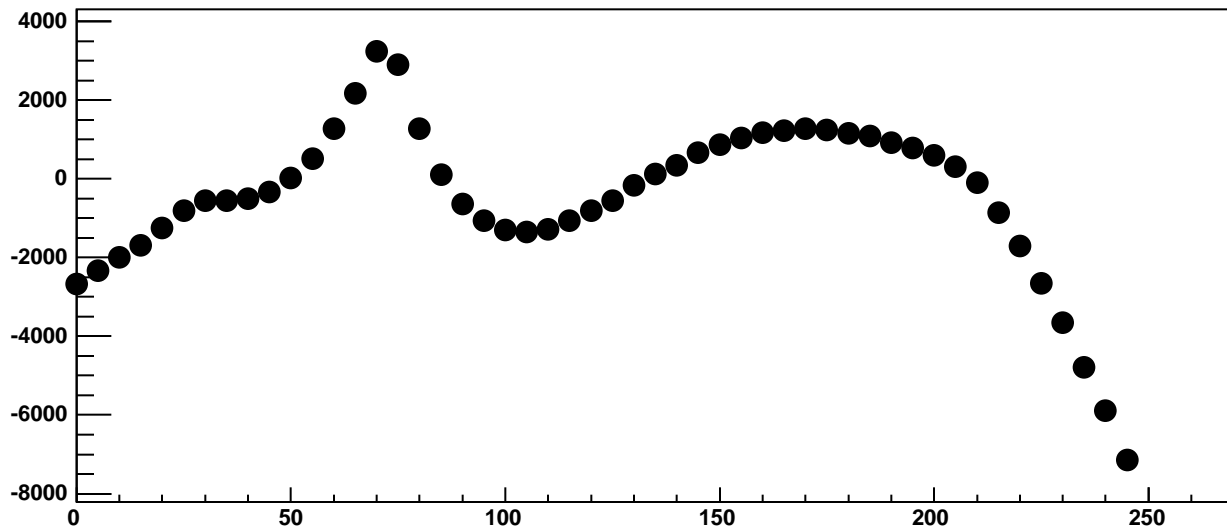
Chip 11, Channel 3, Enable 0, DAC=1600, ADC Mean vs Hold



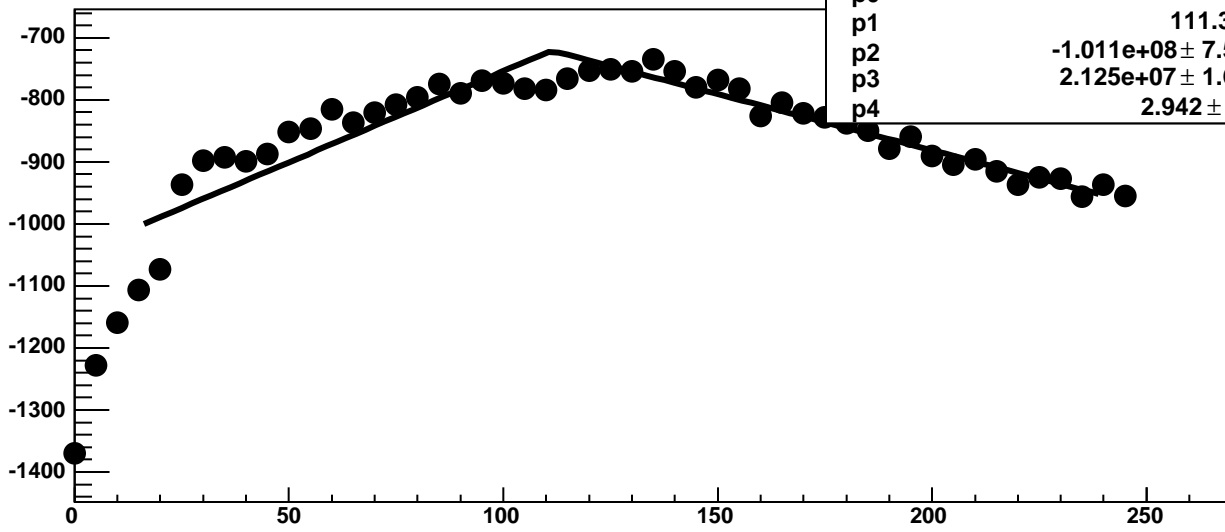
Chip 11, Channel 3, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 3, Enable 0, DAC=1600, ADC Residuals vs Hold

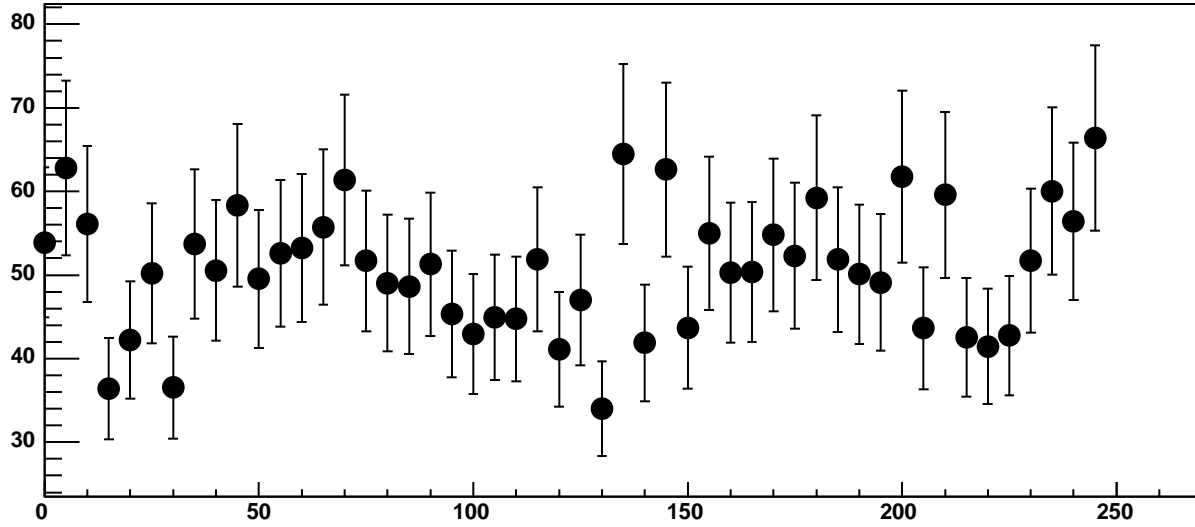


Chip 11, Channel 3, Enable 1, DAC=1600, ADC Mean vs Hold

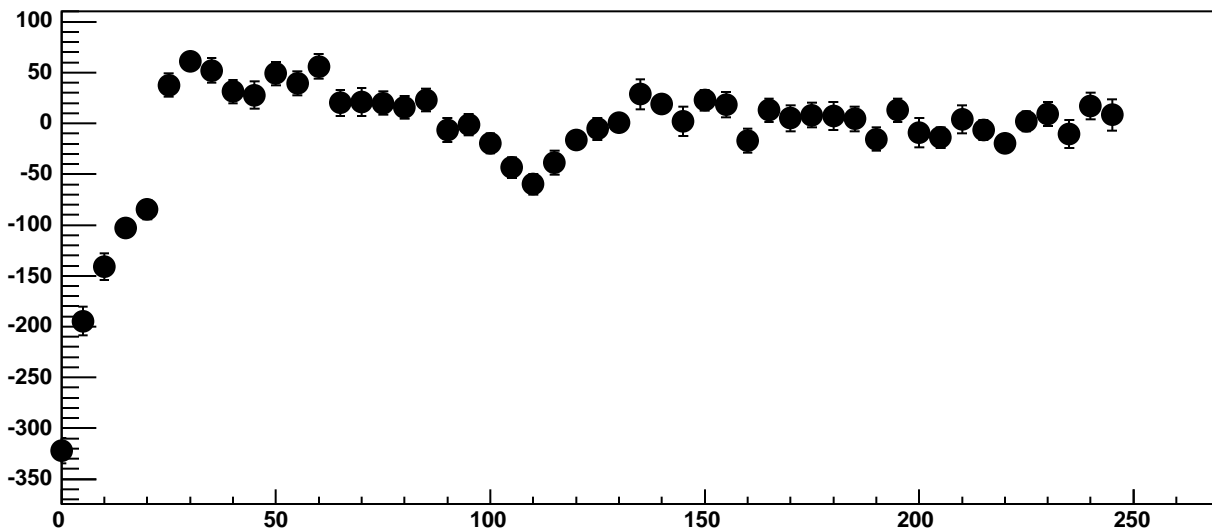


$\chi^2 / \text{ndf}$	488.4 / 41
p0	$-720.4 \pm 3.107$
p1	$111.3 \pm 1.297$
p2	$-1.011\text{e}+08 \pm 7.582\text{e}+06$
p3	$2.125\text{e}+07 \pm 1.621\text{e}+06$
p4	$2.942 \pm 0.07529$

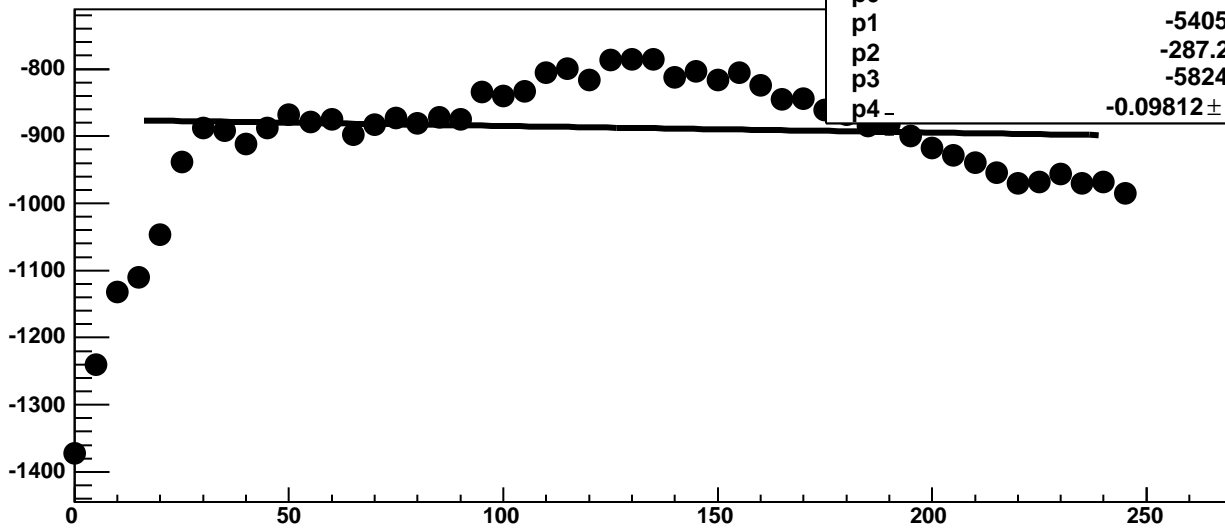
Chip 11, Channel 3, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 3, Enable 1, DAC=1600, ADC Residuals vs Hold

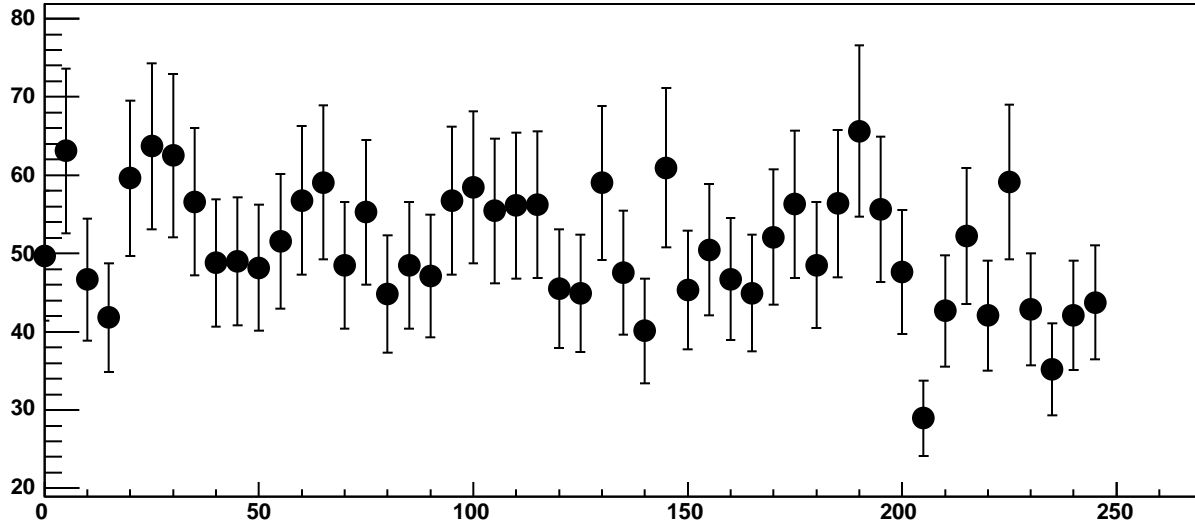


Chip 11, Channel 3, Enable 2, DAC=1600, ADC Mean vs Hold

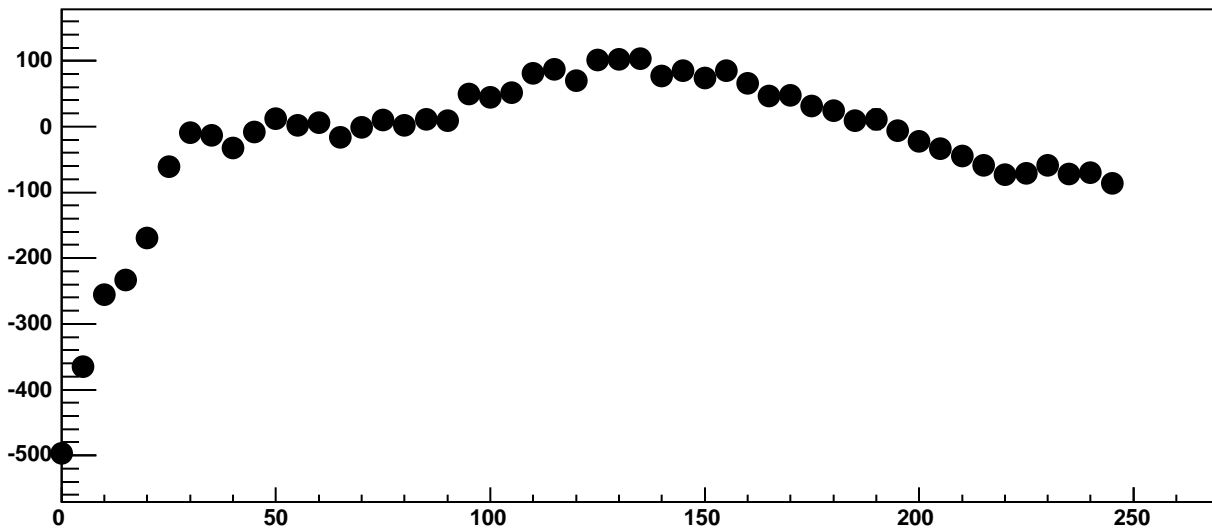


$\chi^2 / \text{ndf}$	1819 / 41
p0	$-57.43 \pm 39.87$
p1	$-5405 \pm 201.7$
p2	$-287.2 \pm 68.55$
p3	$-5824 \pm 1406$
p4	$-0.09812 \pm 0.02313$

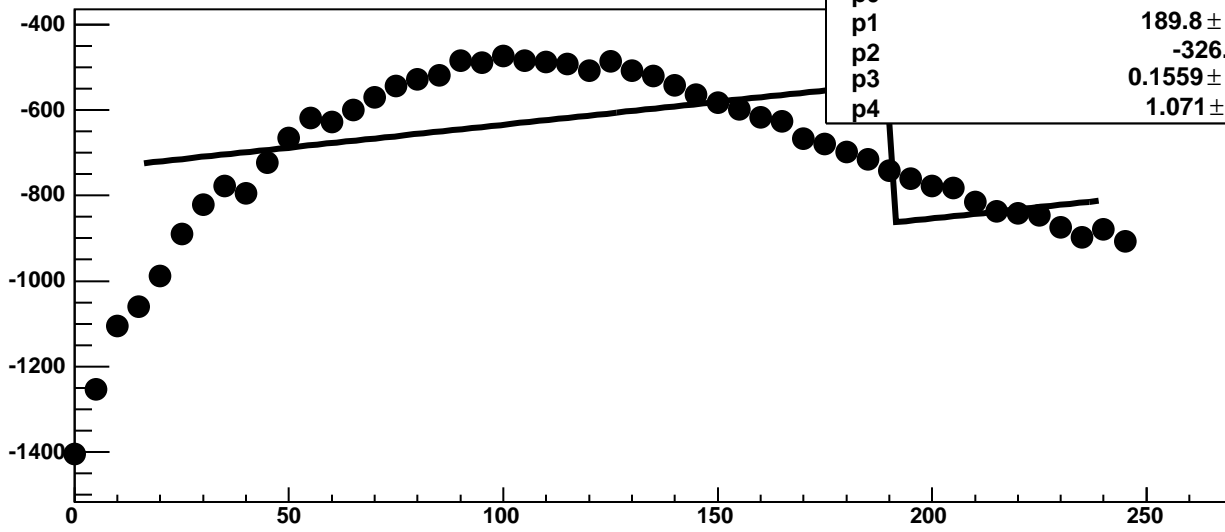
Chip 11, Channel 3, Enable 2, DAC=1600, ADC Noise vs Hold



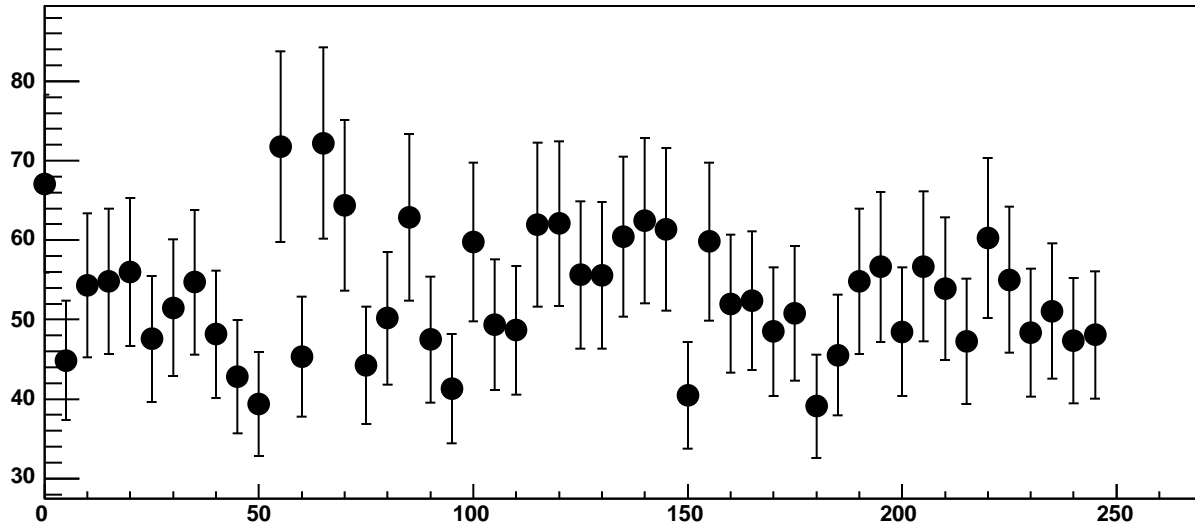
Chip 11, Channel 3, Enable 2, DAC=1600, ADC Residuals vs Hold



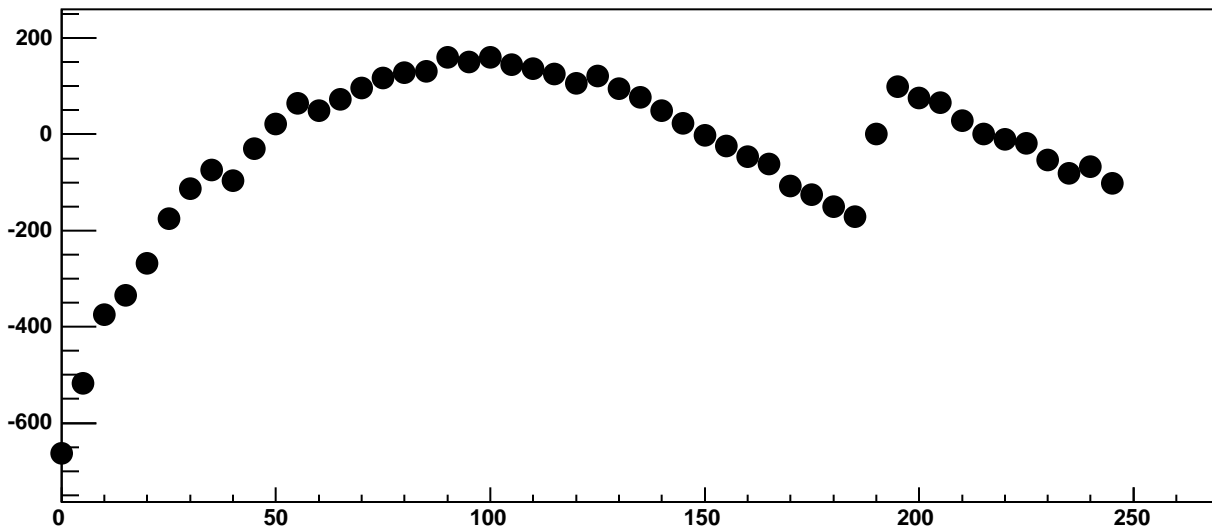
Chip 11, Channel 3, Enable 3, DAC=1600, ADC Mean vs Hold



Chip 11, Channel 3, Enable 3, DAC=1600, ADC Noise vs Hold

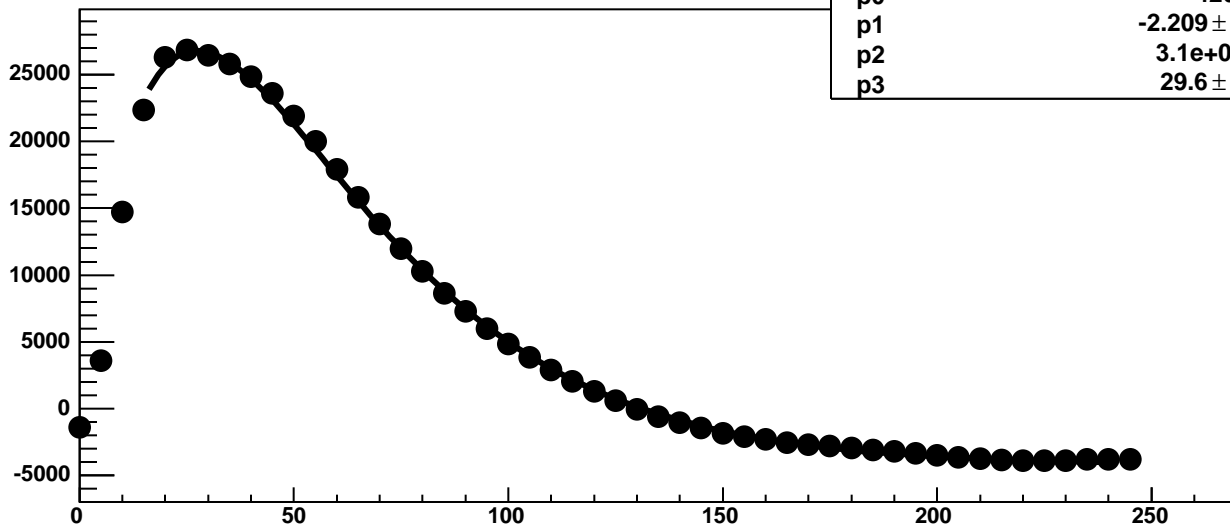


Chip 11, Channel 3, Enable 3, DAC=1600, ADC Residuals vs Hold



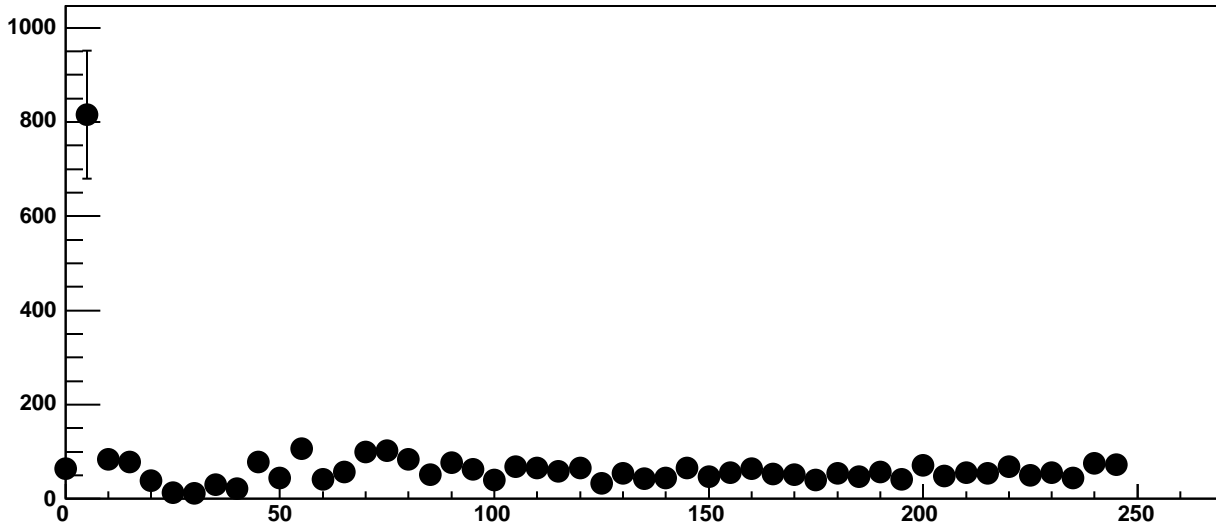


Chip 11, Channel 3, Enable 4!, DAC=1600, ADC Mean vs Hold

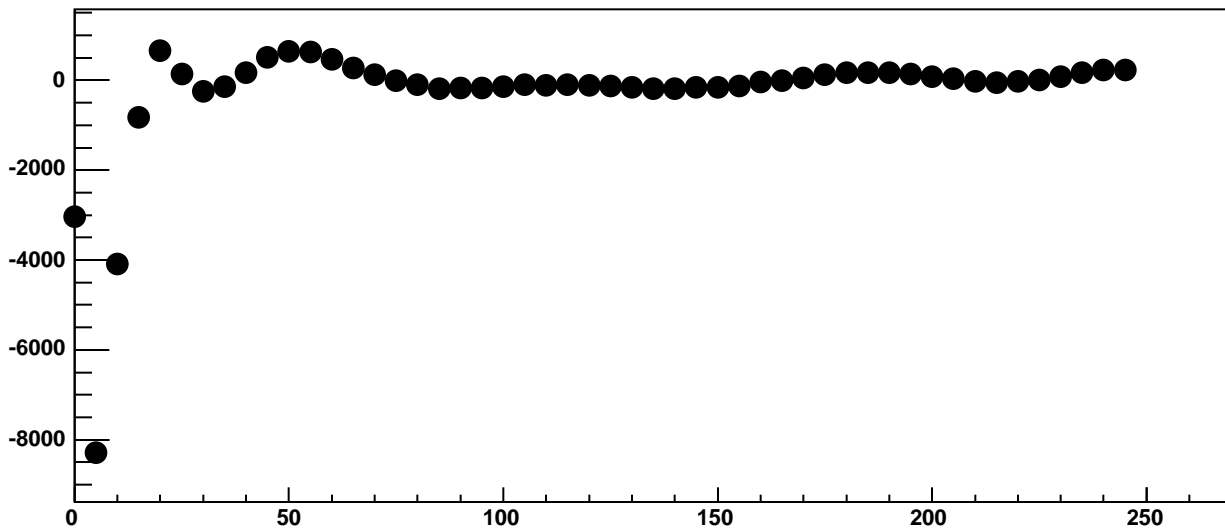


$\chi^2 / \text{ndf}$	3.09e+04 / 42
p0	-4208 ± 3.5
p1	-2.209 ± 0.01824
p2	3.1e+04 ± 3.81
p3	29.6 ± 0.01048

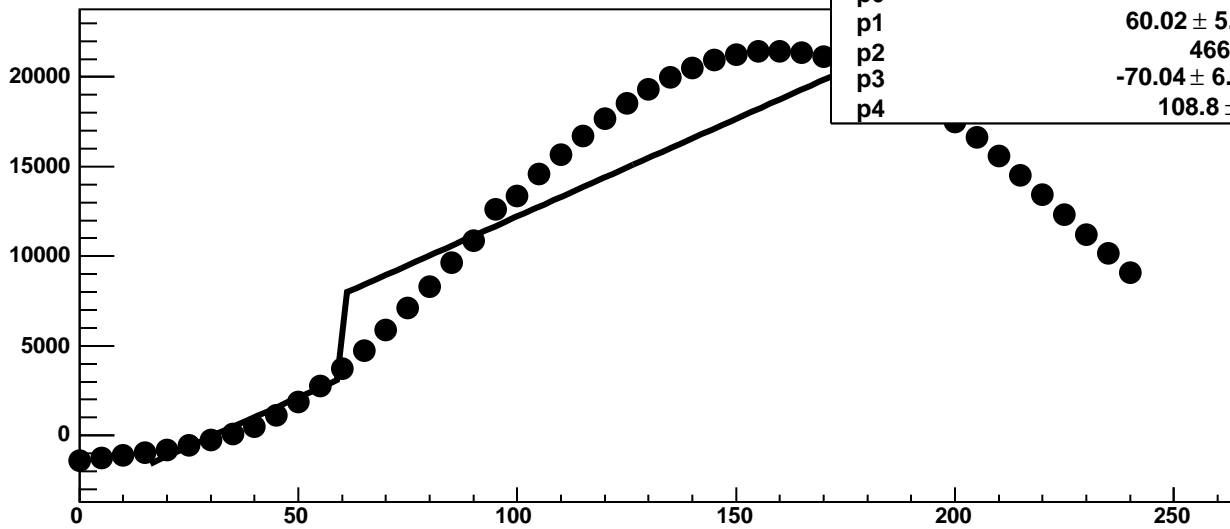
Chip 11, Channel 3, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 3, Enable 4!, DAC=1600, ADC Residuals vs Hold

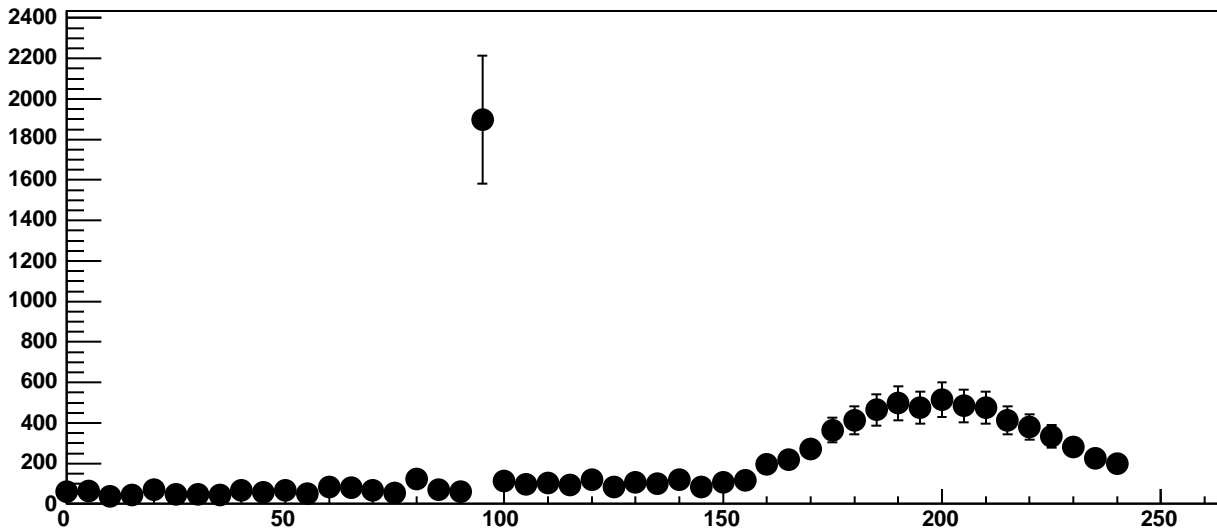


Chip 11, Channel 3, Enable 5, DAC=1600, ADC Mean vs Hold

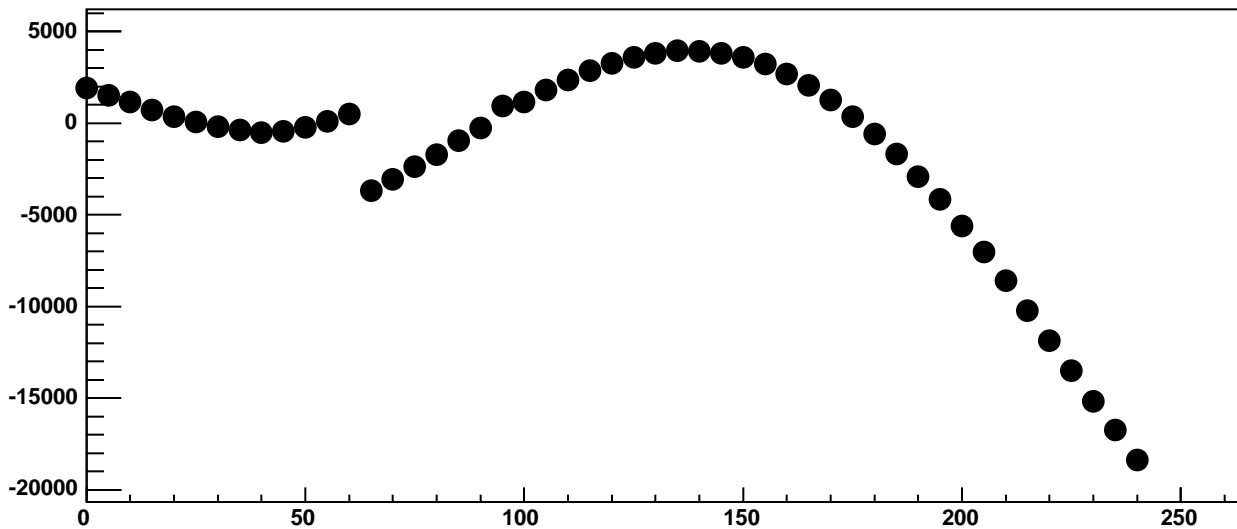


$\chi^2 / \text{ndf}$	7.689e+05 / 41
p0	3203 $\pm$ 4.887
p1	60.02 $\pm$ 5.116e-05
p2	4664 $\pm$ 10.1
p3	-70.04 $\pm$ 6.749e-06
p4	108.8 $\pm$ 0.1094

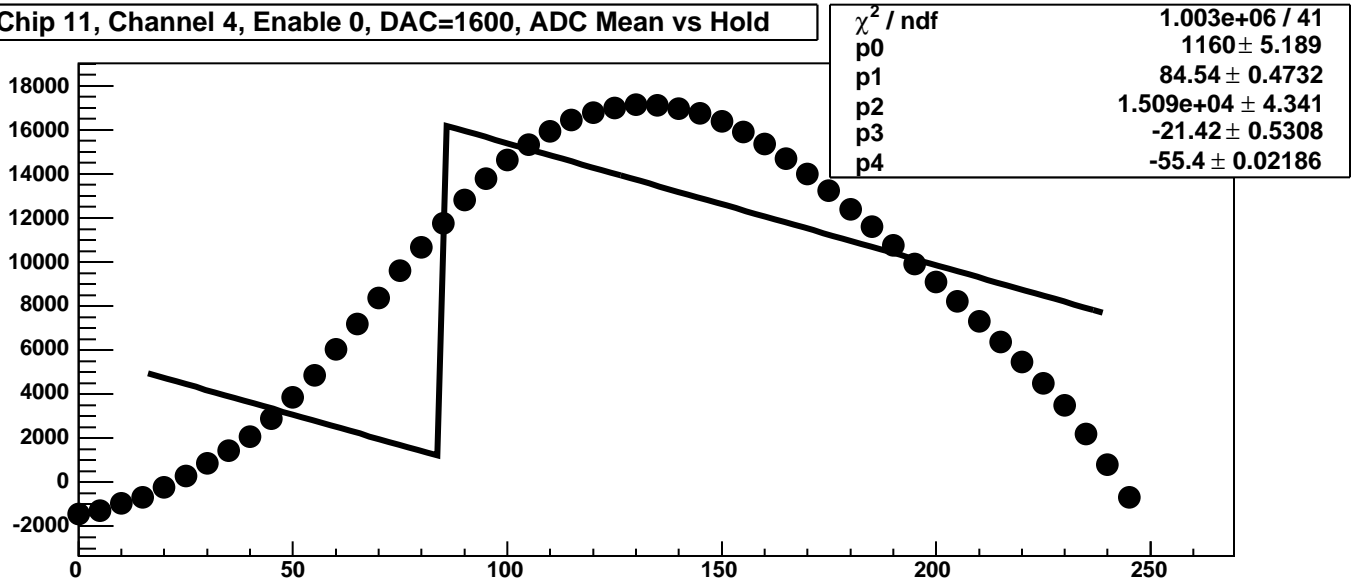
Chip 11, Channel 3, Enable 5, DAC=1600, ADC Noise vs Hold



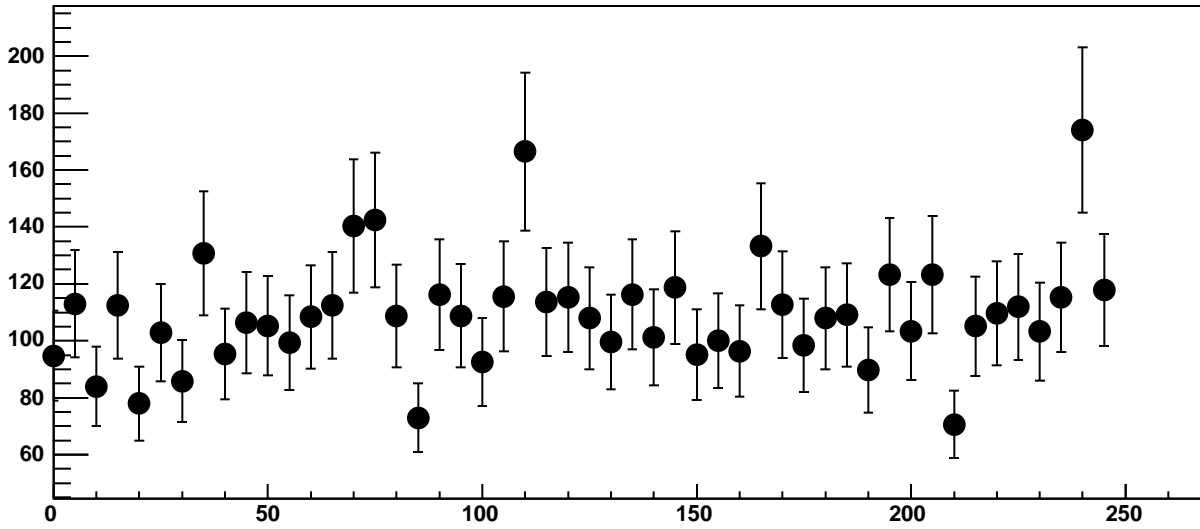
Chip 11, Channel 3, Enable 5, DAC=1600, ADC Residuals vs Hold



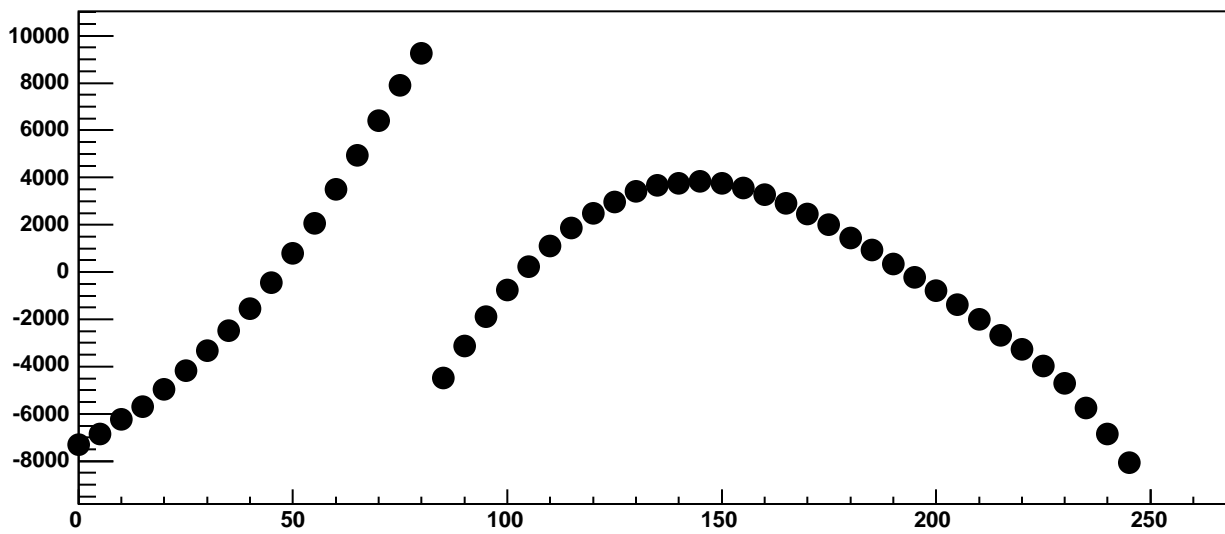
Chip 11, Channel 4, Enable 0, DAC=1600, ADC Mean vs Hold



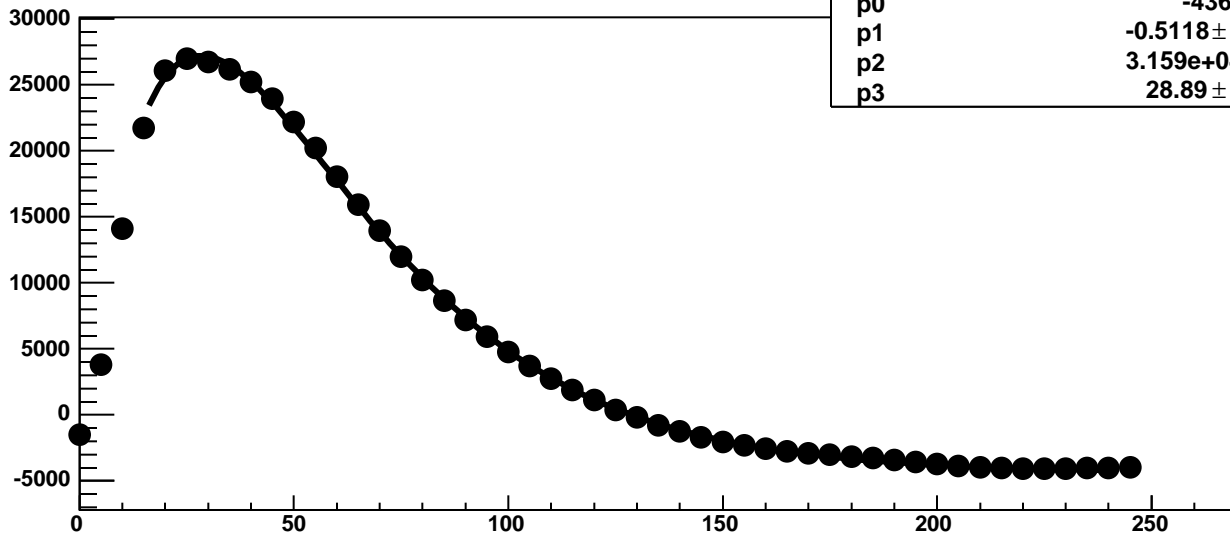
Chip 11, Channel 4, Enable 0, DAC=1600, ADC Noise vs Hold



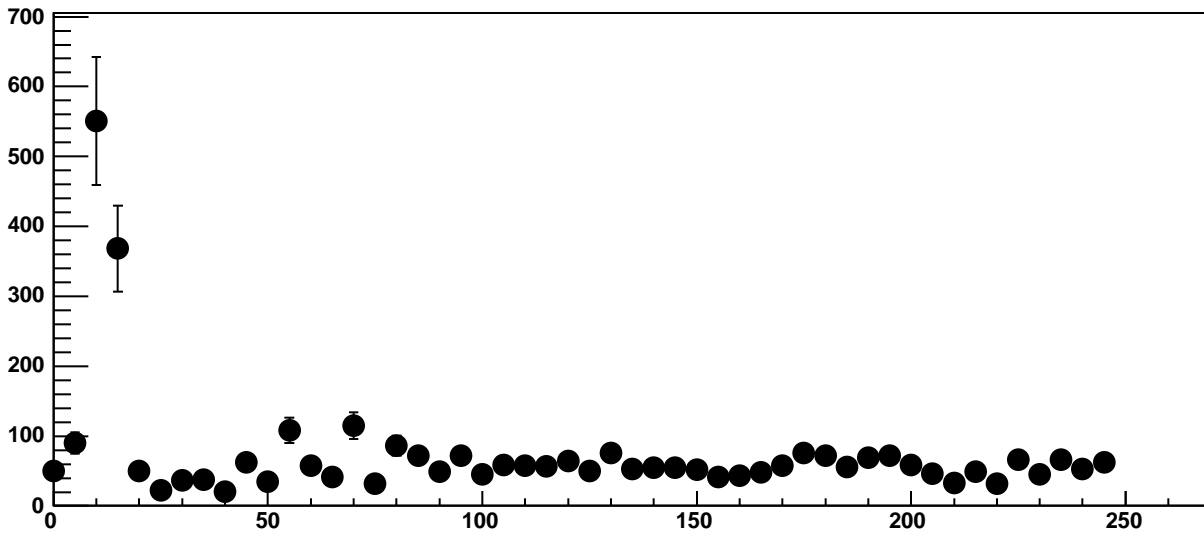
Chip 11, Channel 4, Enable 0, DAC=1600, ADC Residuals vs Hold



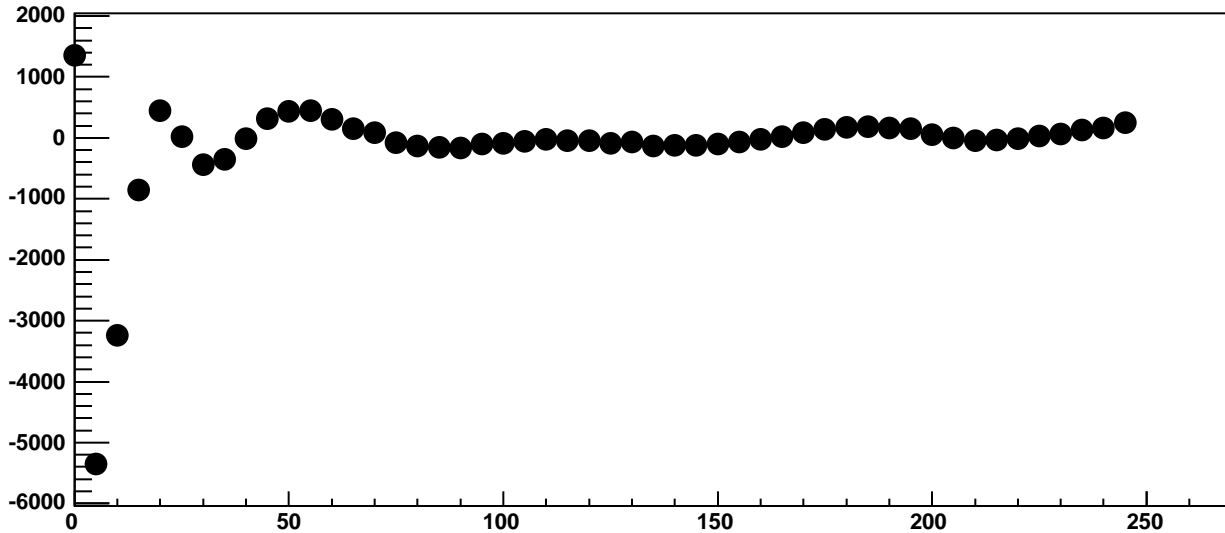
Chip 11, Channel 4, Enable 1!, DAC=1600, ADC Mean vs Hold



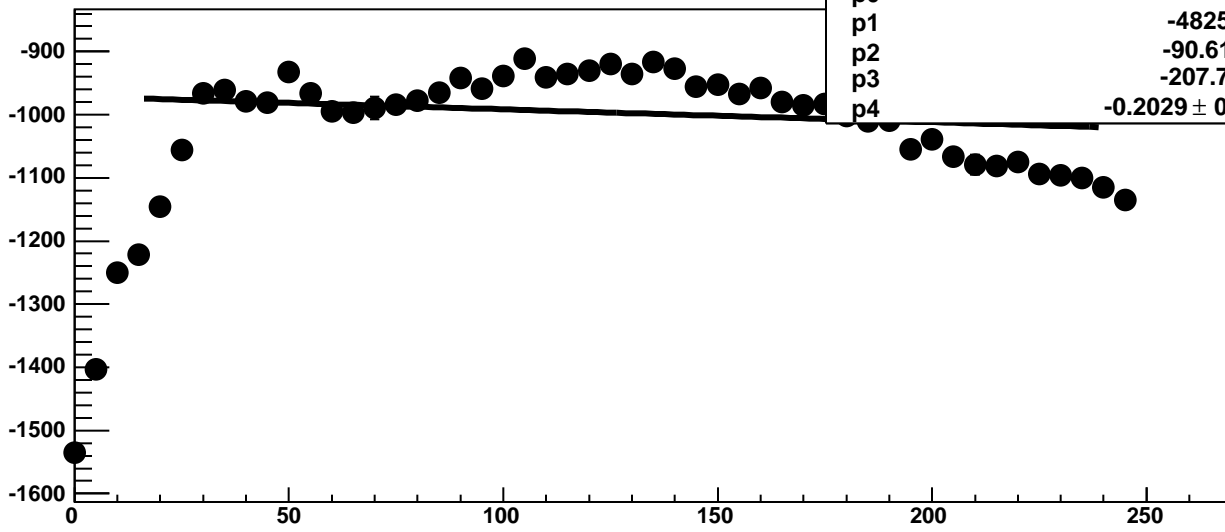
Chip 11, Channel 4, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 4, Enable 1!, DAC=1600, ADC Residuals vs Hold

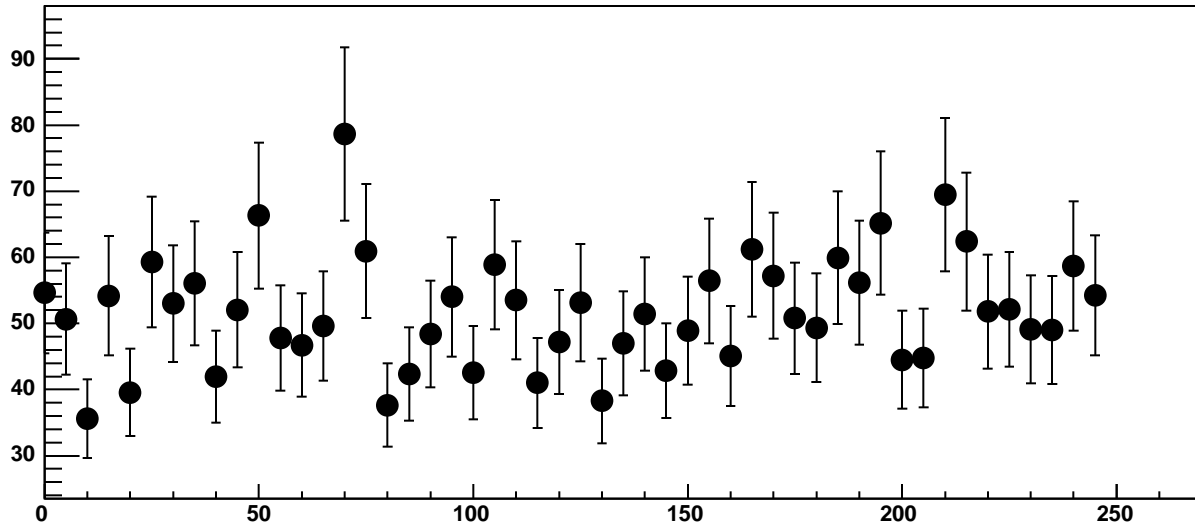


Chip 11, Channel 4, Enable 2, DAC=1600, ADC Mean vs Hold

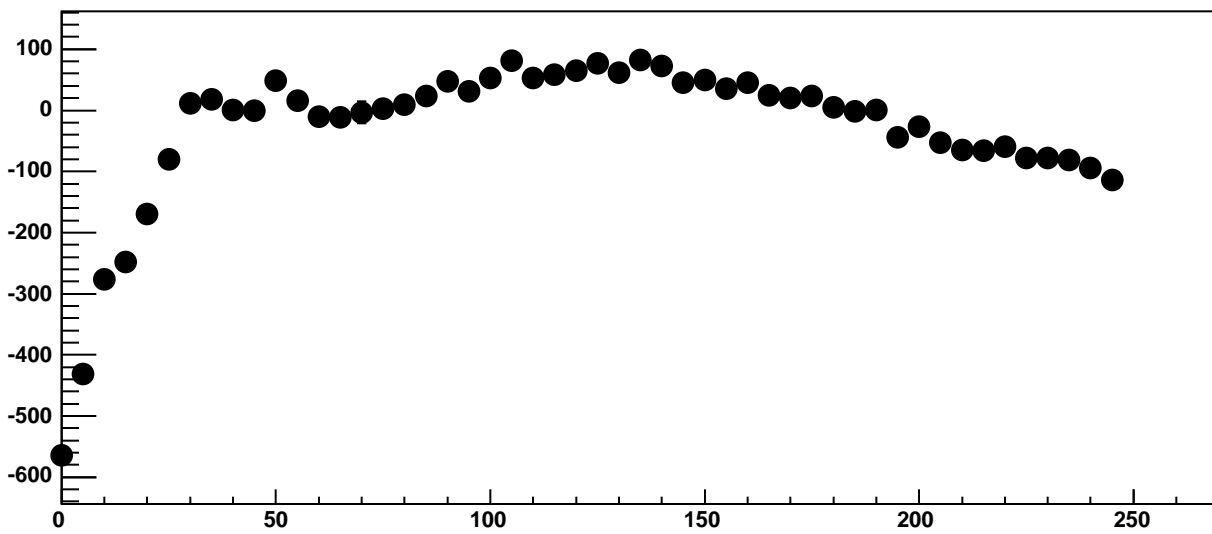


$\chi^2 / \text{ndf}$	1548 / 41
p0	$98.3 \pm 7.28$
p1	$-4825 \pm 41.31$
p2	$-90.61 \pm 1.944$
p3	$-207.7 \pm 4816$
p4	$-0.2029 \pm 0.001468$

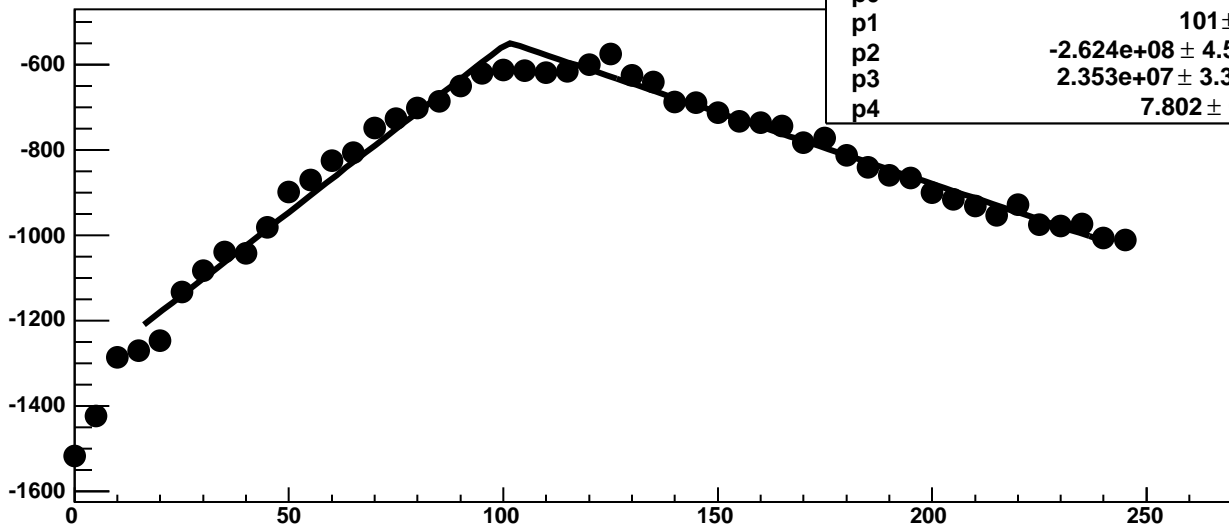
Chip 11, Channel 4, Enable 2, DAC=1600, ADC Noise vs Hold



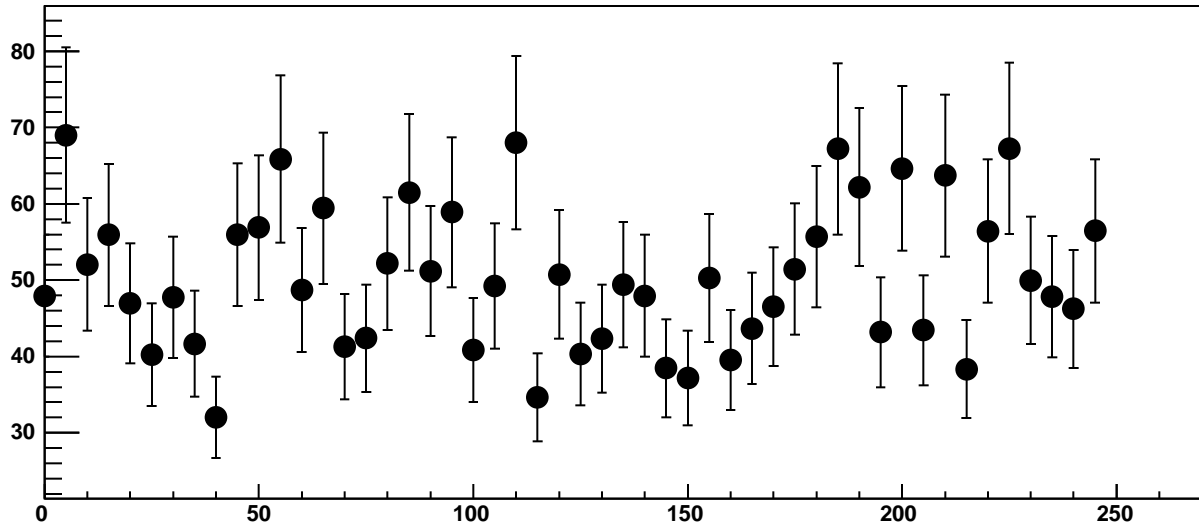
Chip 11, Channel 4, Enable 2, DAC=1600, ADC Residuals vs Hold



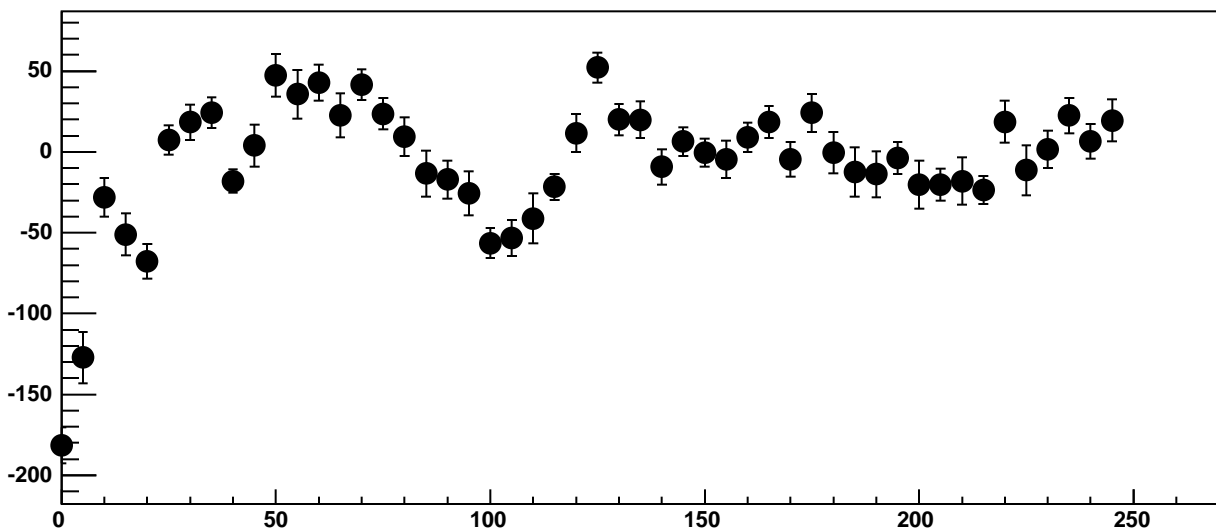
Chip 11, Channel 4, Enable 3, DAC=1600, ADC Mean vs Hold



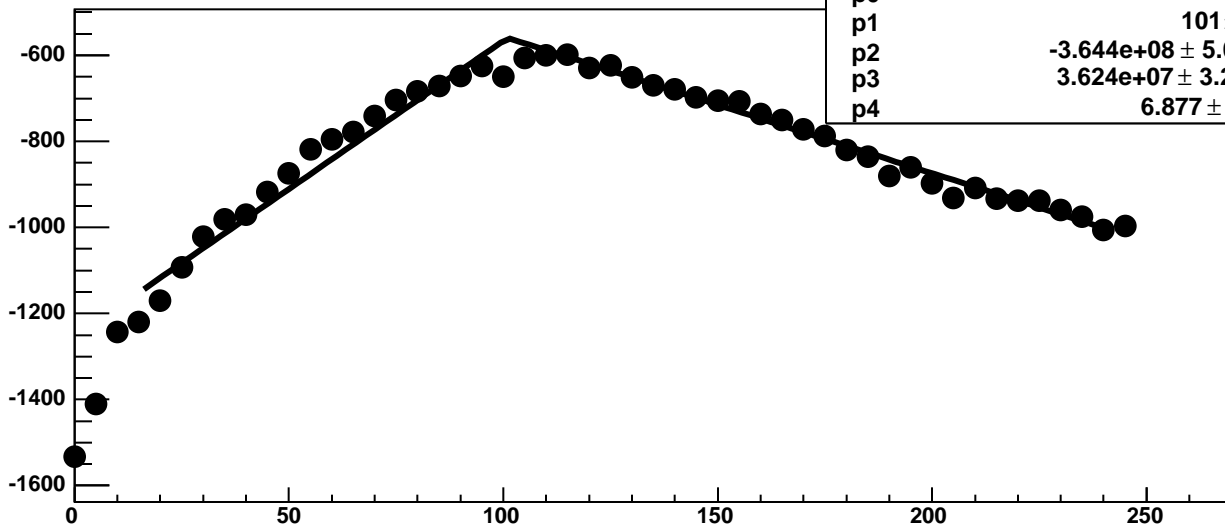
Chip 11, Channel 4, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 4, Enable 3, DAC=1600, ADC Residuals vs Hold

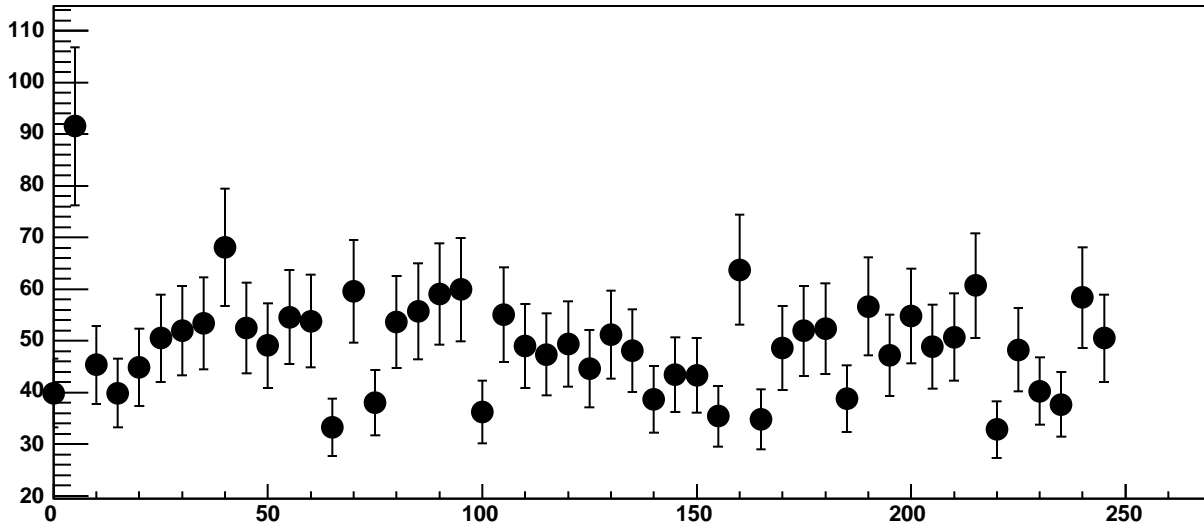


Chip 11, Channel 4, Enable 4, DAC=1600, ADC Mean vs Hold

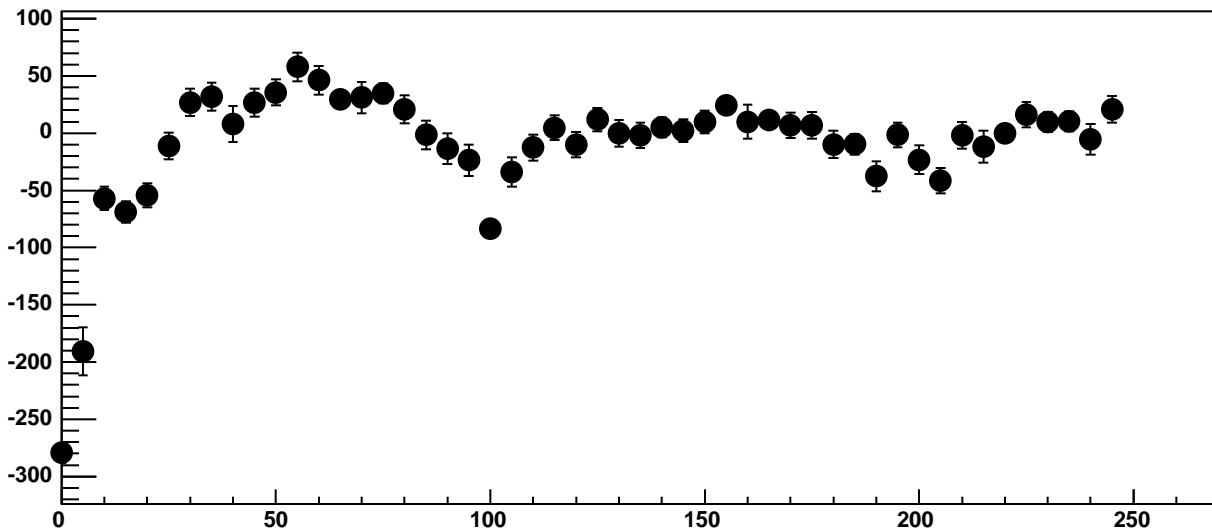


$\chi^2 / \text{ndf}$	349.6 / 41
p0	-559.4 ± 3.214
p1	101 ± 0.6371
p2	-3.644e+08 ± 5.094e+06
p3	3.624e+07 ± 3.209e+05
p4	6.877 ± 0.09654

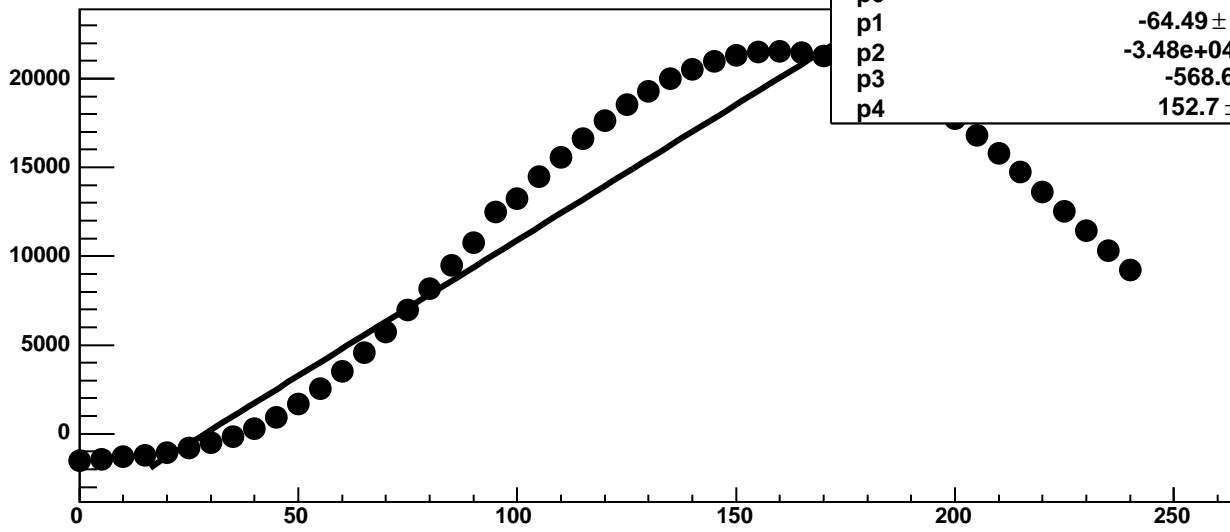
Chip 11, Channel 4, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 4, Enable 4, DAC=1600, ADC Residuals vs Hold

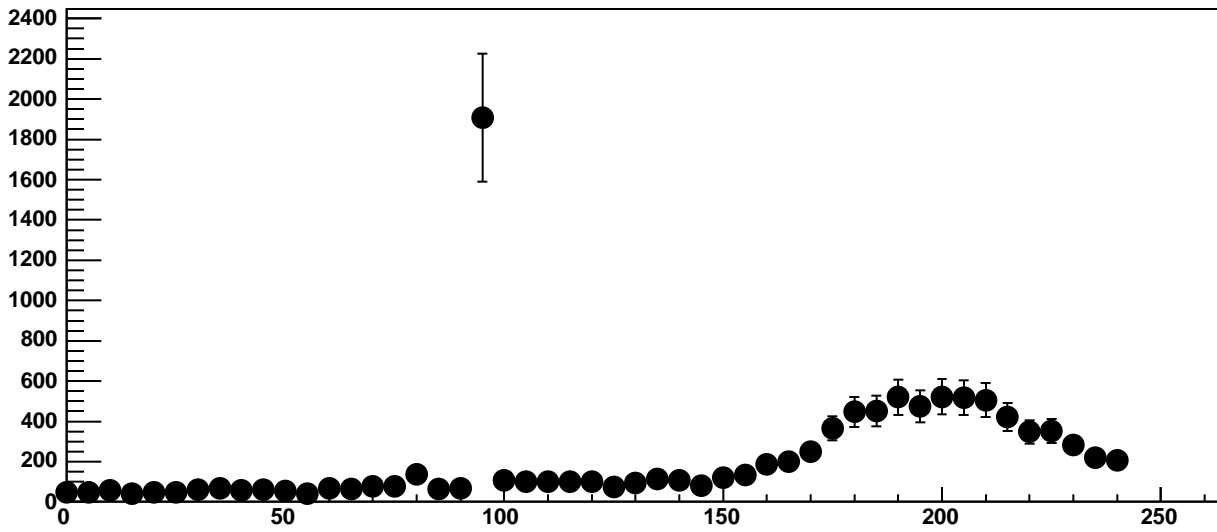


Chip 11, Channel 4, Enable 5, DAC=1600, ADC Mean vs Hold

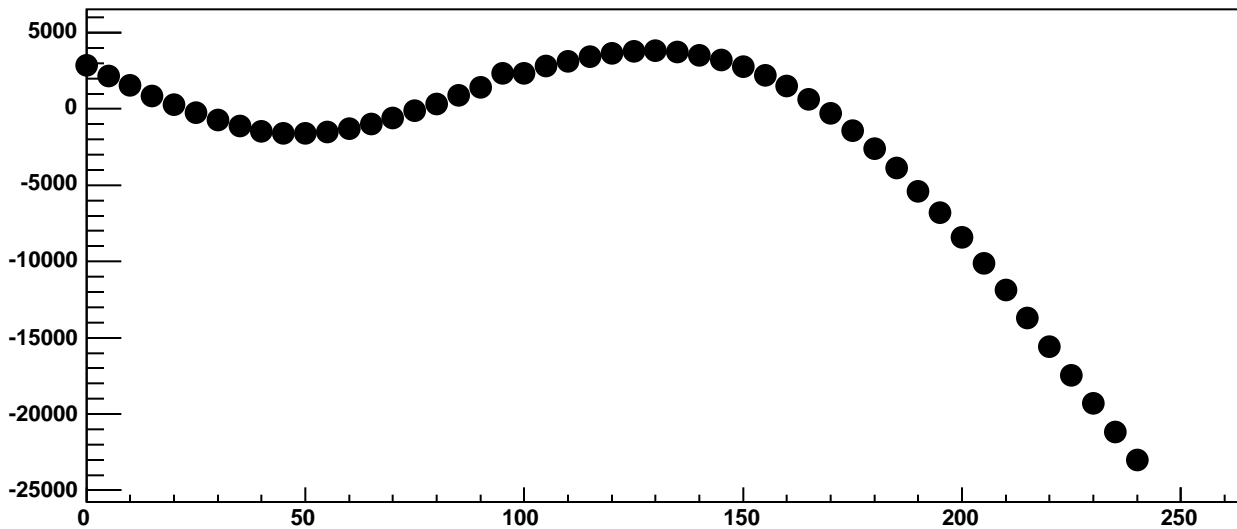


$\chi^2 / \text{ndf}$	1e+06 / 41
p0	2.059e+04 ± 18.18
p1	-64.49 ± 0.06385
p2	-3.48e+04 ± 19.25
p3	-568.6 ± 1.956
p4	152.7 ± 0.1074

Chip 11, Channel 4, Enable 5, DAC=1600, ADC Noise vs Hold

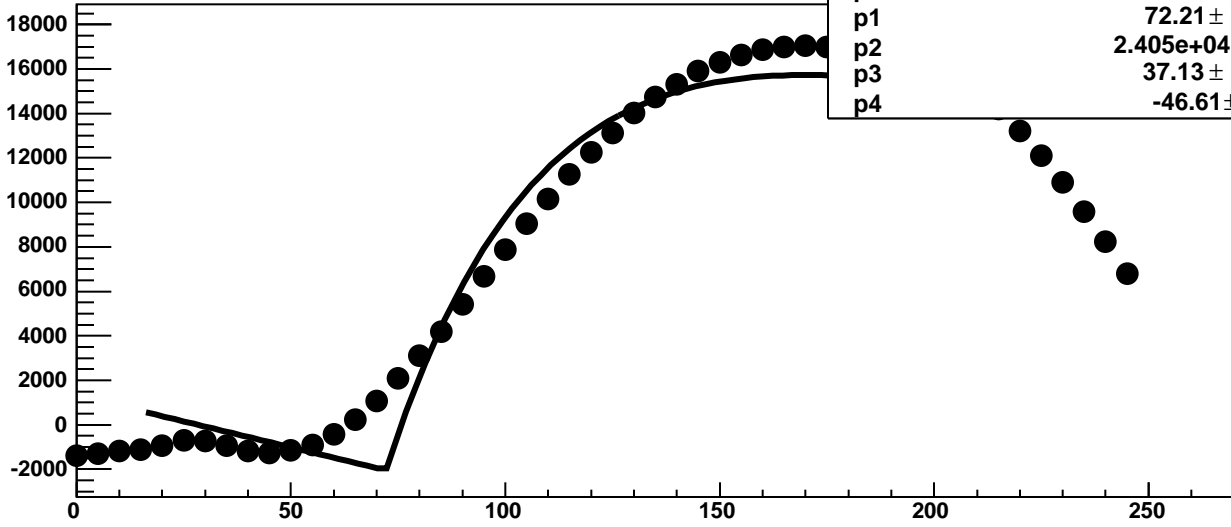


Chip 11, Channel 4, Enable 5, DAC=1600, ADC Residuals vs Hold



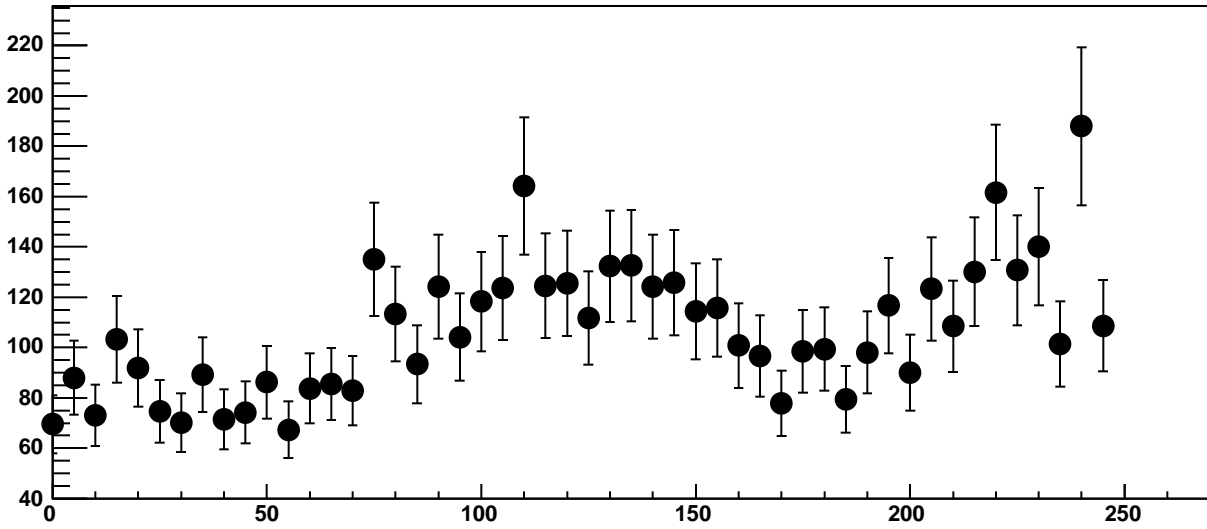


Chip 11, Channel 5, Enable 0, DAC=1600, ADC Mean vs Hold

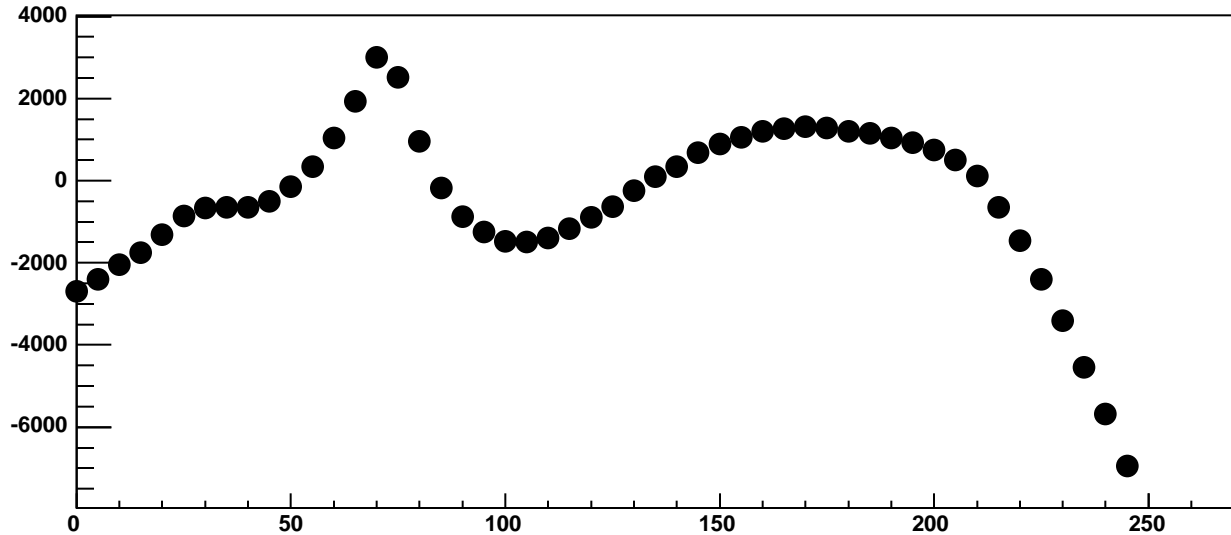


$\chi^2 / \text{ndf}$	1.823e+05 / 41
p0	-2041 ± 8.002
p1	72.21 ± 0.03477
p2	2.405e+04 ± 41.37
p3	37.13 ± 0.08232
p4	-46.61 ± 0.2303

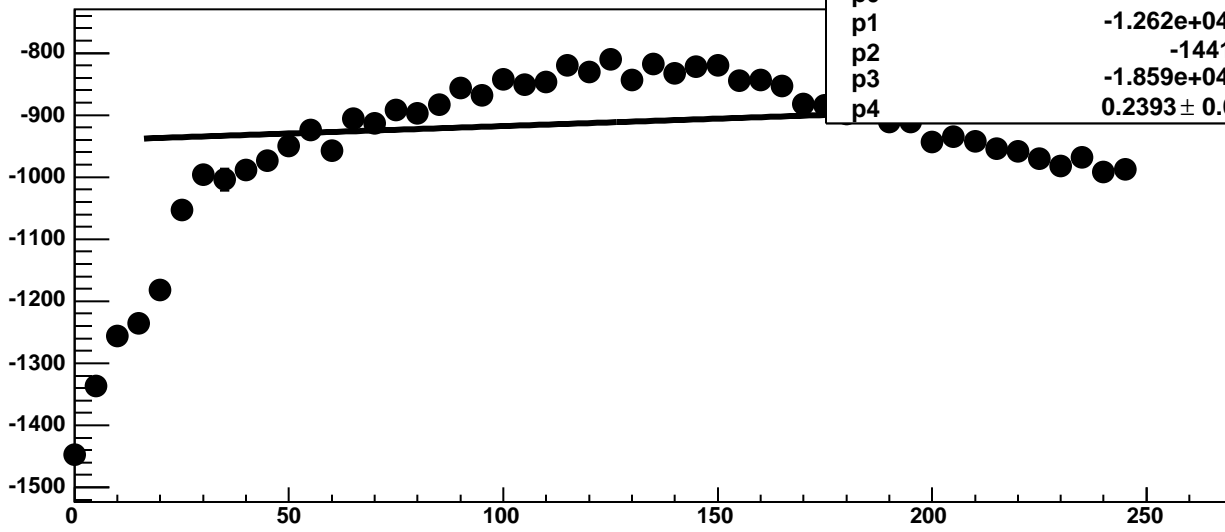
Chip 11, Channel 5, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 5, Enable 0, DAC=1600, ADC Residuals vs Hold

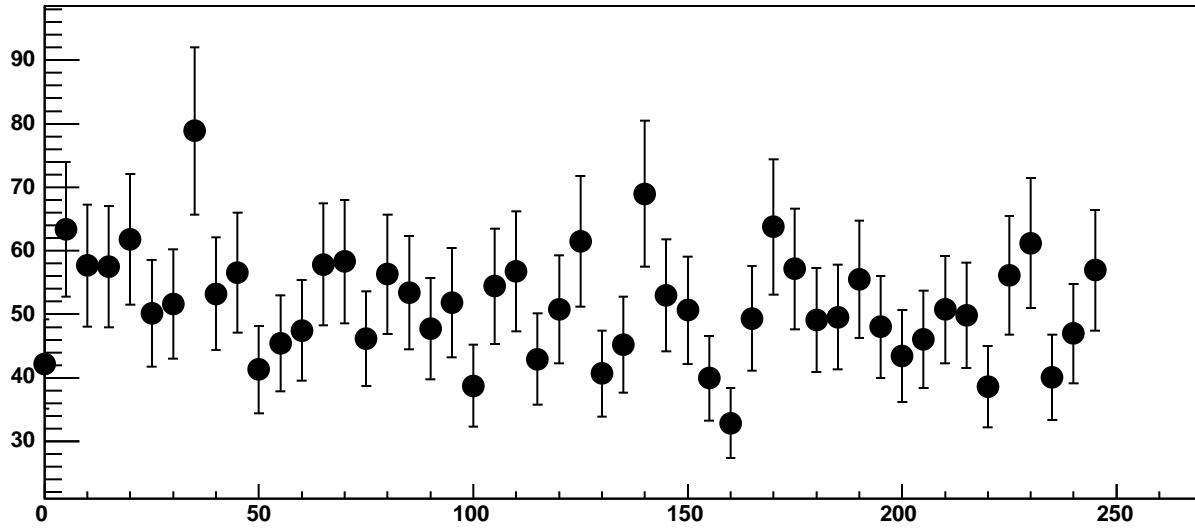


Chip 11, Channel 5, Enable 1, DAC=1600, ADC Mean vs Hold

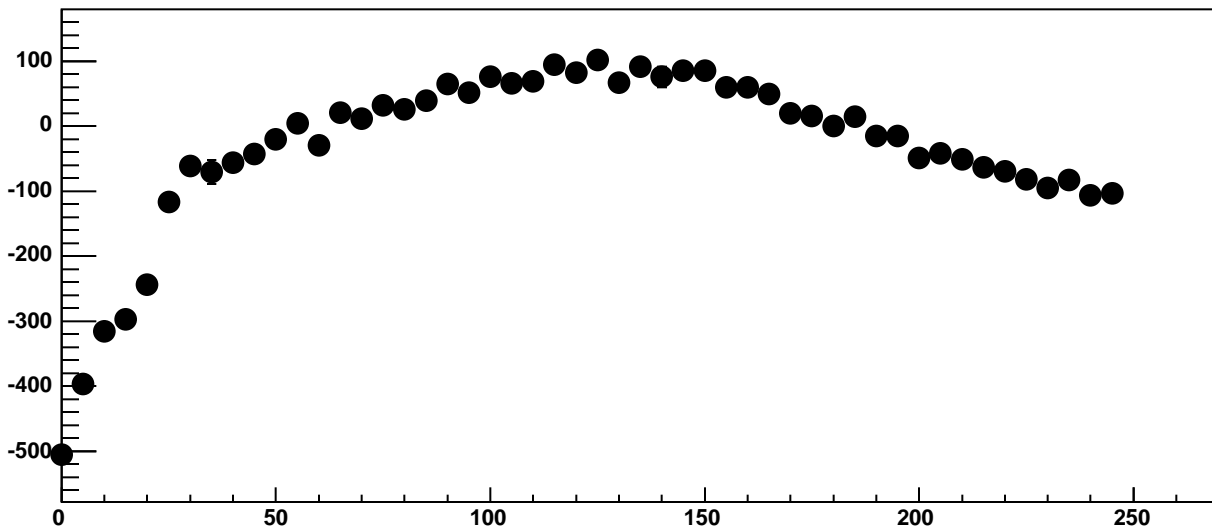


$\chi^2 / \text{ndf}$	2203 / 41
p0	$-2520 \pm 8.331$
p1	$-1.262\text{e}+04 \pm 30.78$
p2	$-1441 \pm 10.52$
p3	$-1.859\text{e}+04 \pm 2246$
p4	$0.2393 \pm 0.0006534$

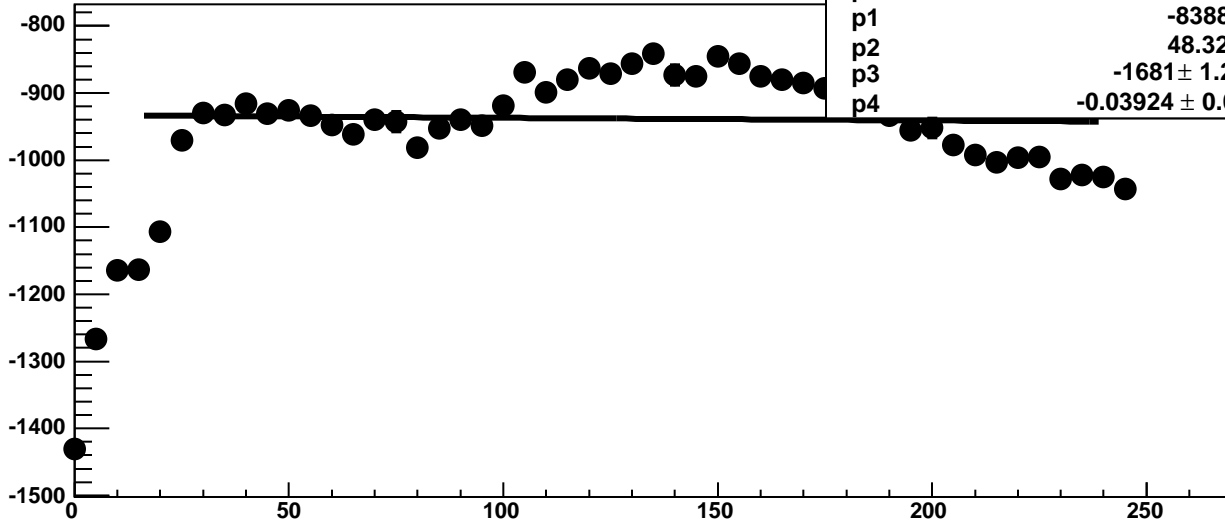
Chip 11, Channel 5, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 5, Enable 1, DAC=1600, ADC Residuals vs Hold

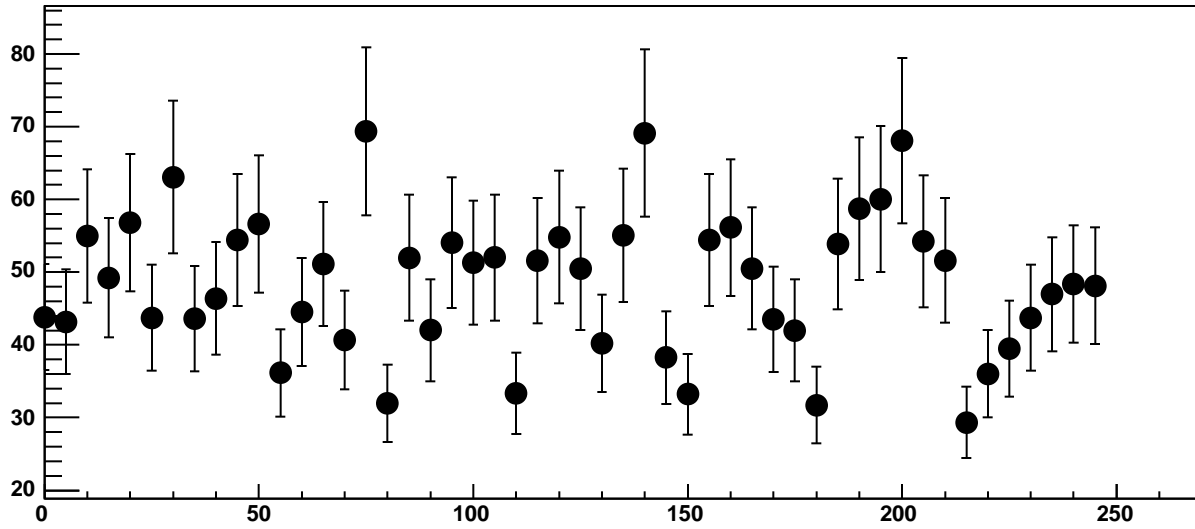


Chip 11, Channel 5, Enable 2, DAC=1600, ADC Mean vs Hold

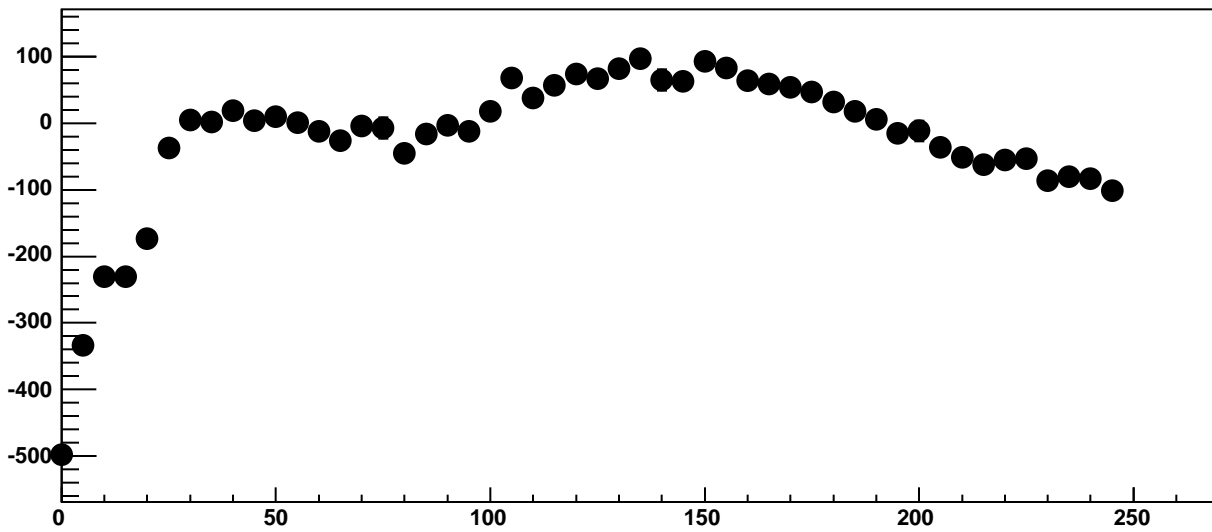


$\chi^2 / \text{ndf}$	1712 / 41
p0	-652.2 ± 8.051
p1	-8388 ± 164.2
p2	48.32 ± 5.798
p3	-1681 ± 1.243e+04
p4	-0.03924 ± 0.0009448

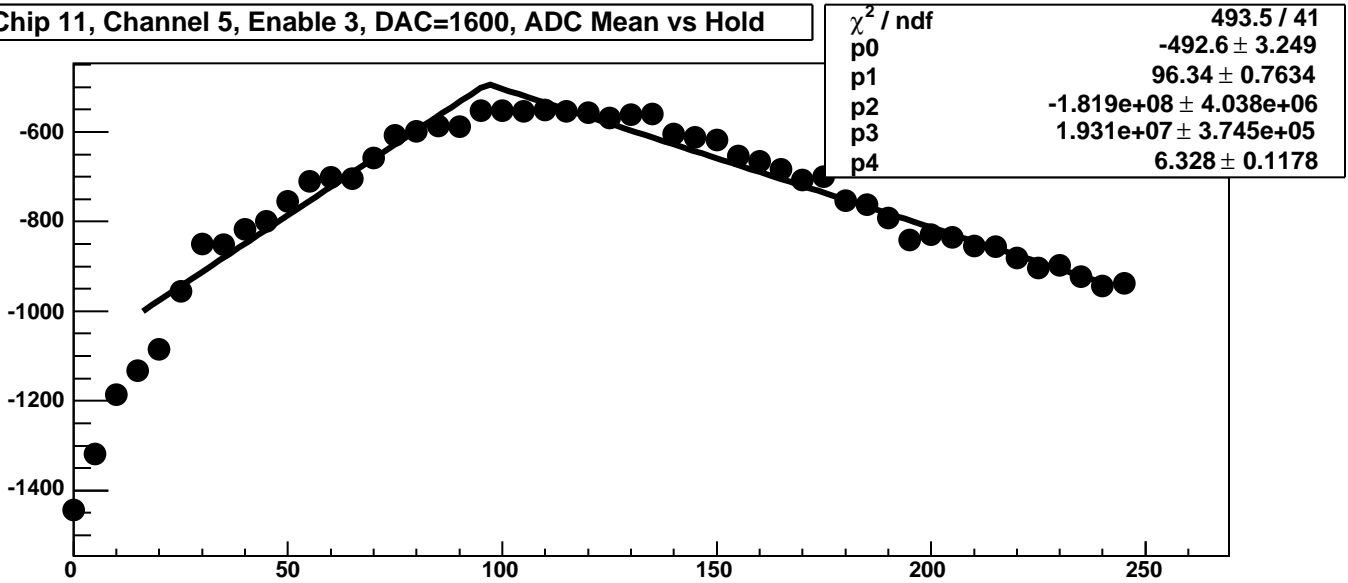
Chip 11, Channel 5, Enable 2, DAC=1600, ADC Noise vs Hold



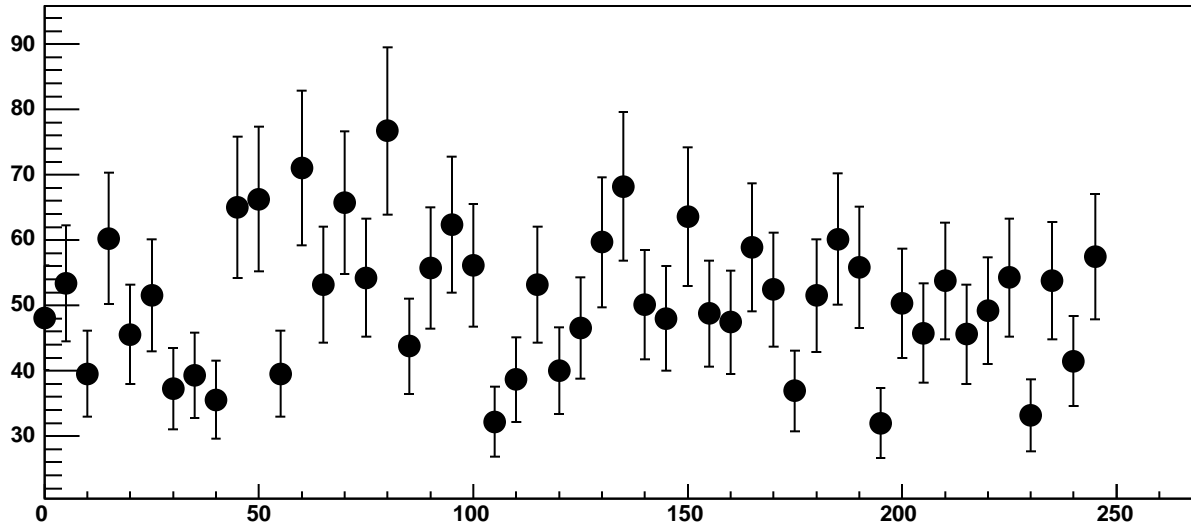
Chip 11, Channel 5, Enable 2, DAC=1600, ADC Residuals vs Hold



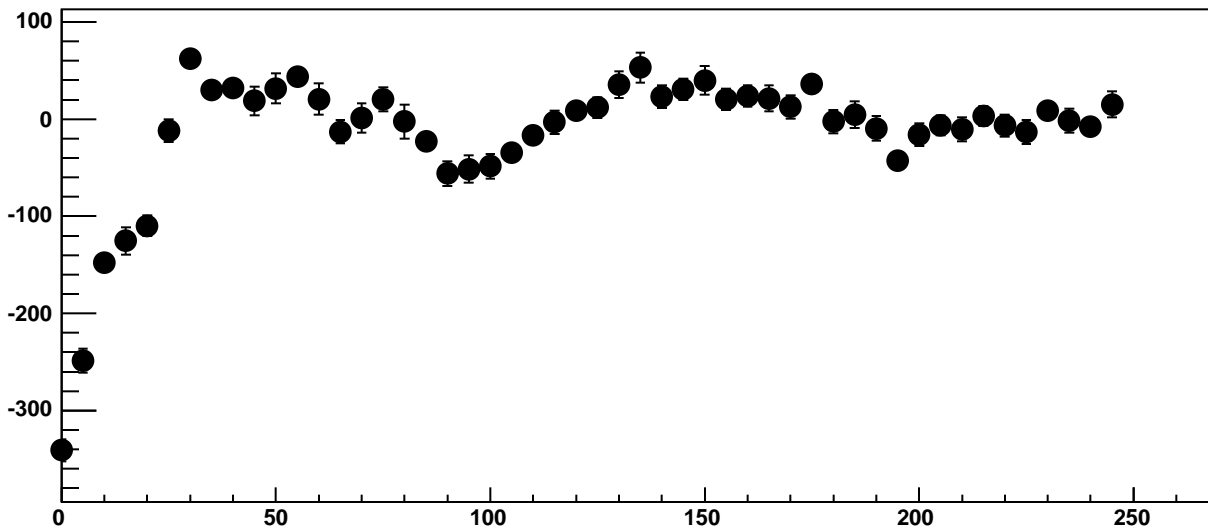
Chip 11, Channel 5, Enable 3, DAC=1600, ADC Mean vs Hold



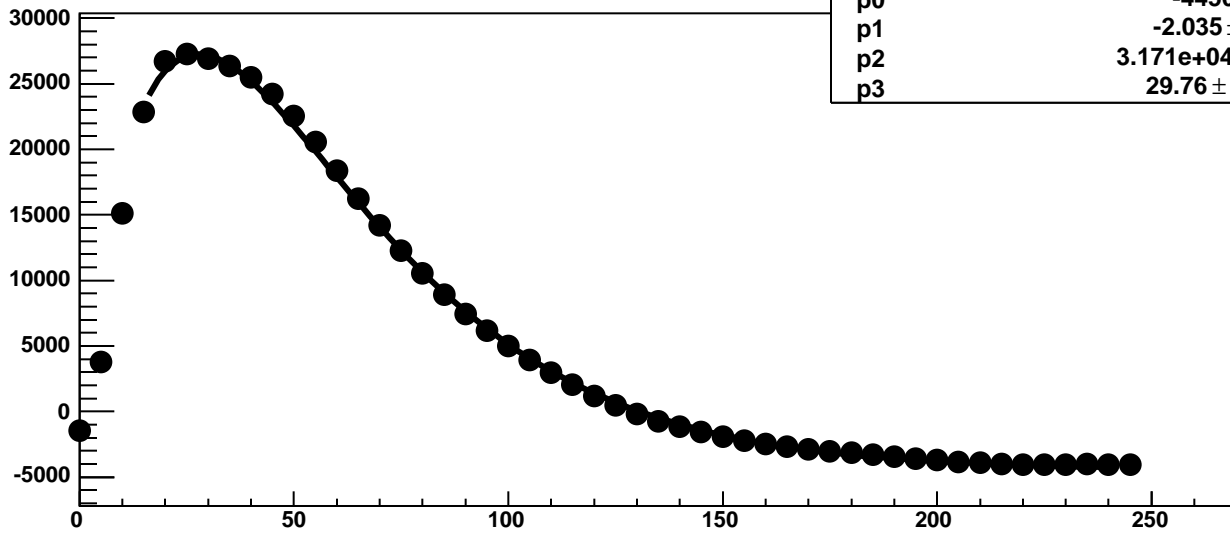
Chip 11, Channel 5, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 5, Enable 3, DAC=1600, ADC Residuals vs Hold

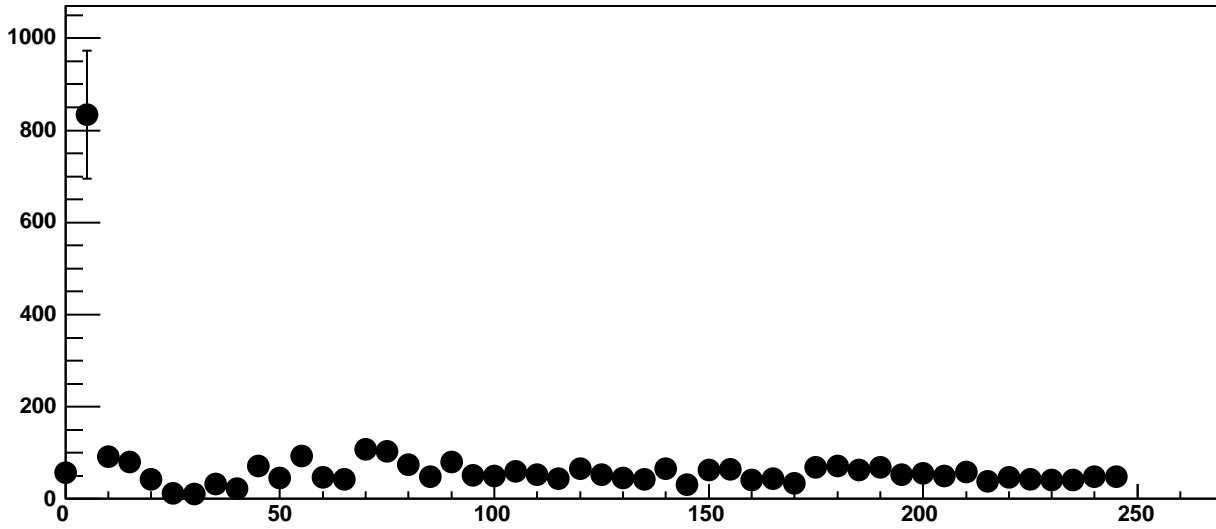


Chip 11, Channel 5, Enable 4!, DAC=1600, ADC Mean vs Hold

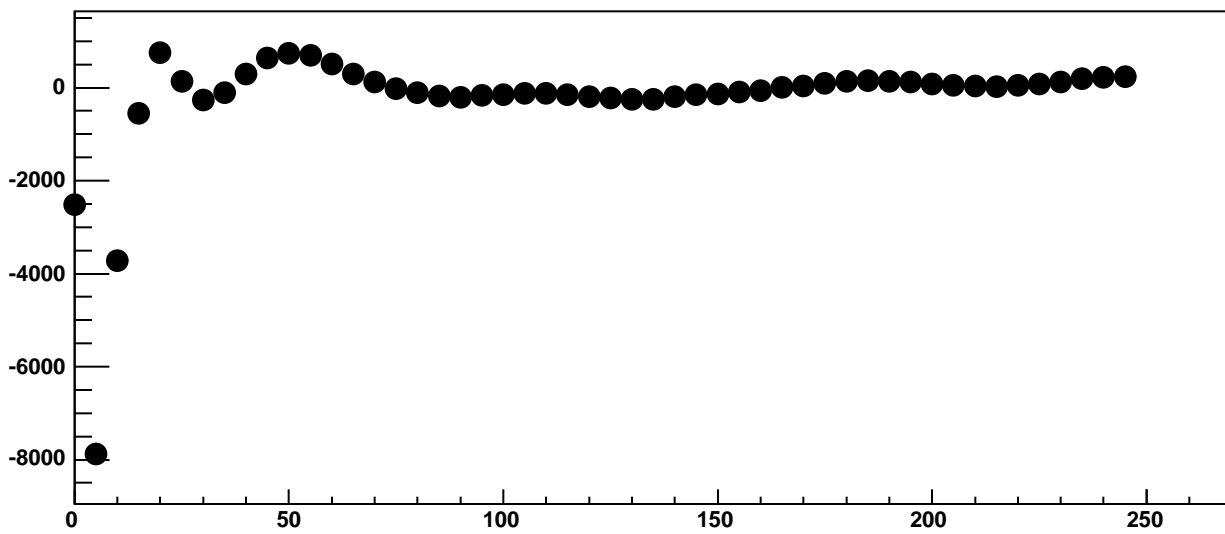


$\chi^2 / \text{ndf}$	4.025e+04 / 42
p0	-4450 ± 3.109
p1	-2.035 ± 0.0168
p2	3.171e+04 ± 3.377
p3	29.76 ± 0.00957

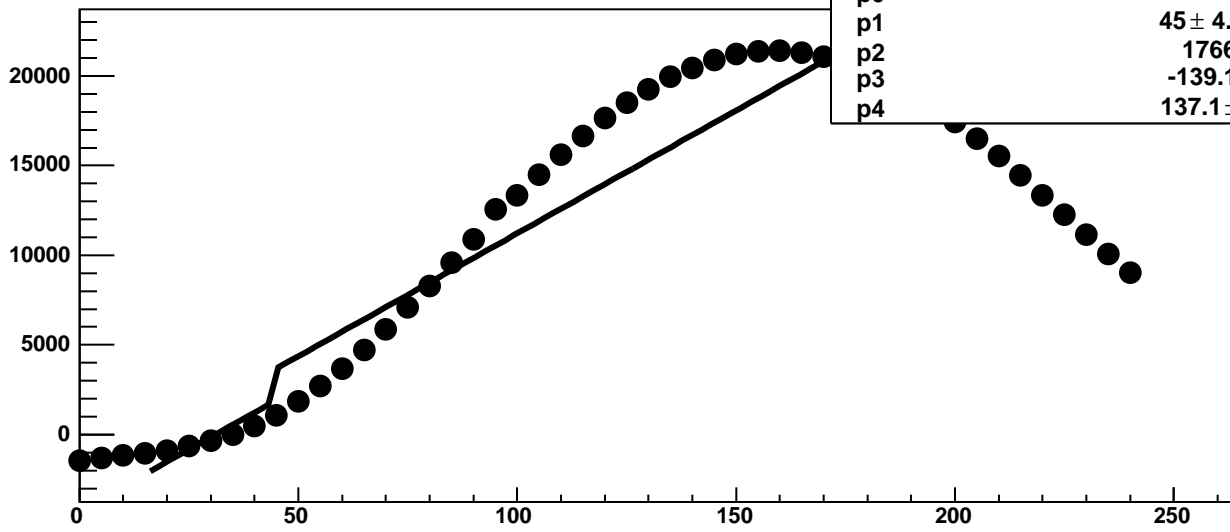
Chip 11, Channel 5, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 5, Enable 4!, DAC=1600, ADC Residuals vs Hold

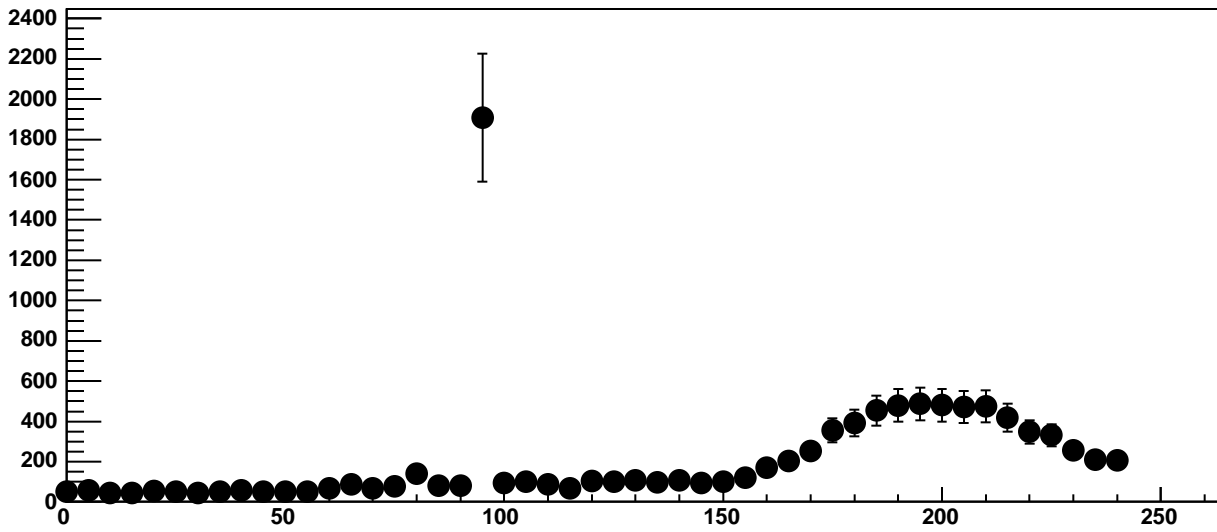


Chip 11, Channel 5, Enable 5, DAC=1600, ADC Mean vs Hold

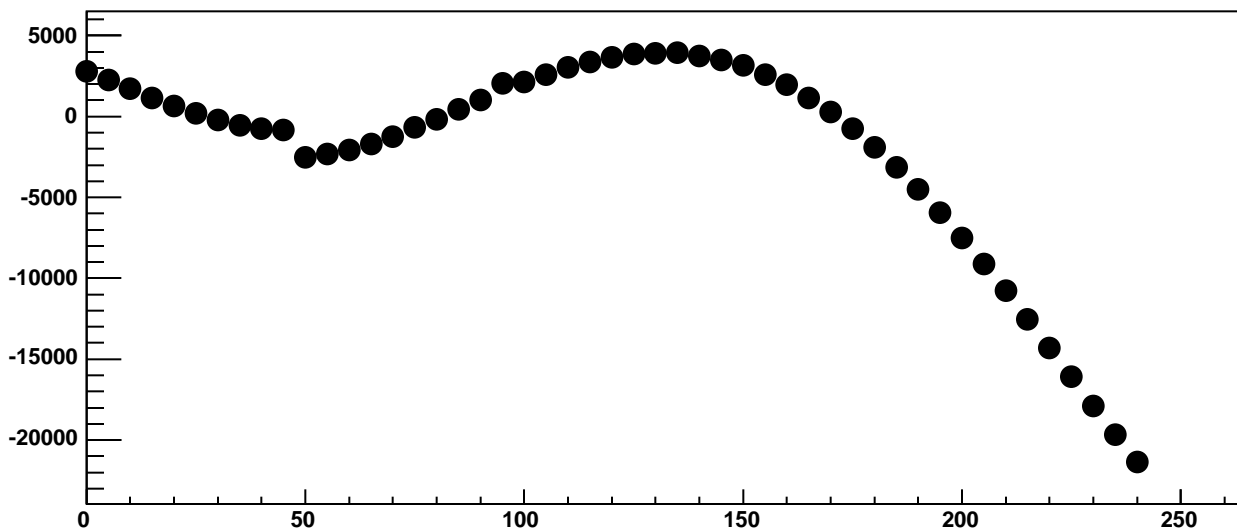


$\chi^2 / \text{ndf}$	1.006e+06 / 41
p0	1914 ± 24.69
p1	45 ± 4.906e-05
p2	1766 ± 11.35
p3	-139.1 ± 23.17
p4	137.1 ± 0.2634

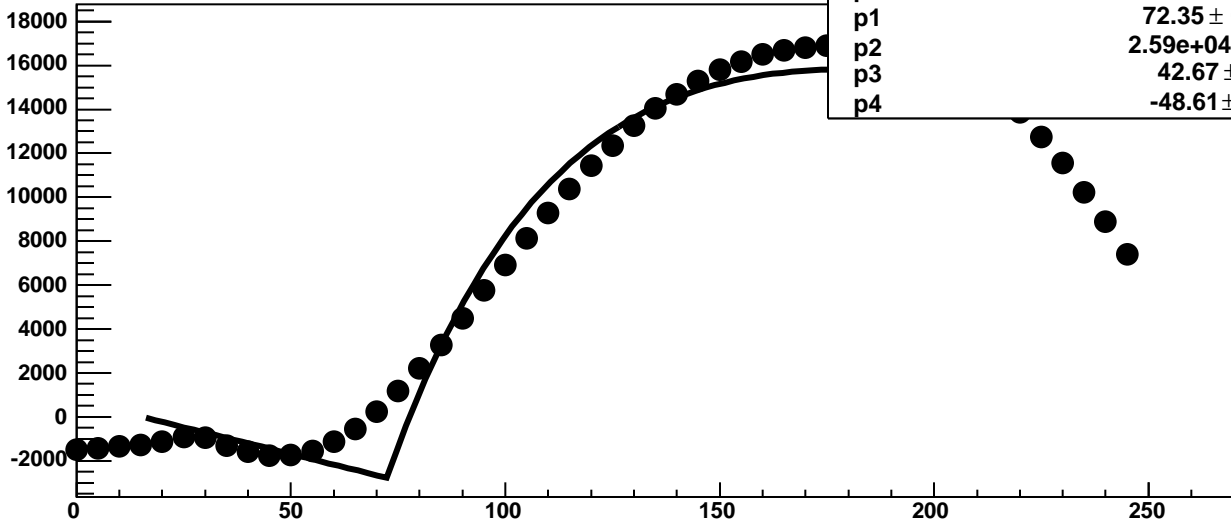
Chip 11, Channel 5, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 5, Enable 5, DAC=1600, ADC Residuals vs Hold

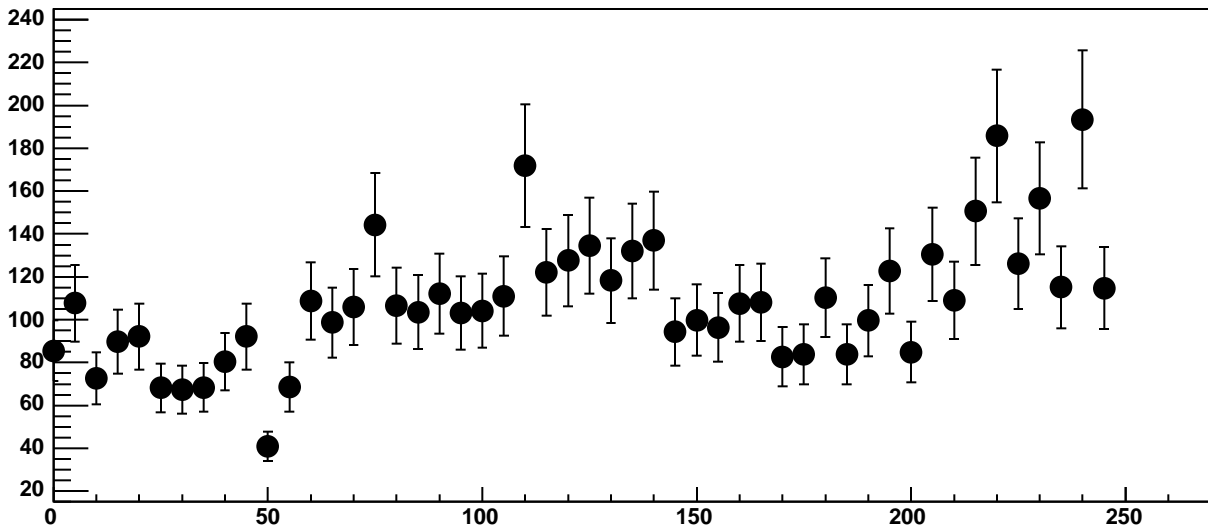


Chip 11, Channel 6, Enable 0, DAC=1600, ADC Mean vs Hold

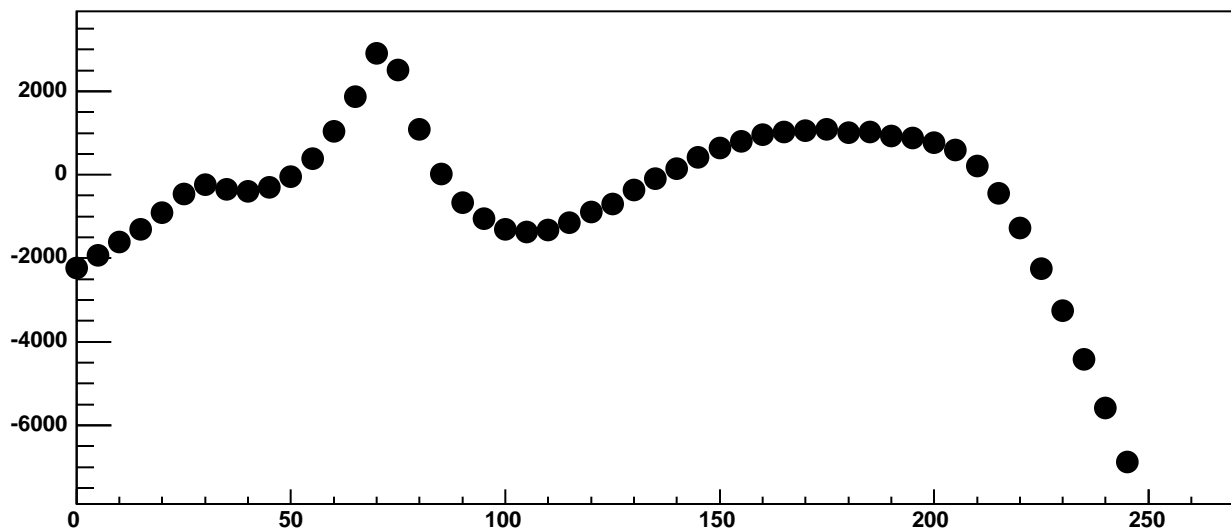


$\chi^2 / \text{ndf}$	1.324e+05 / 41
p0	-2770 ± 8.445
p1	72.35 ± 0.03666
p2	2.59e+04 ± 48.82
p3	42.67 ± 0.0979
p4	-48.61 ± 0.2544

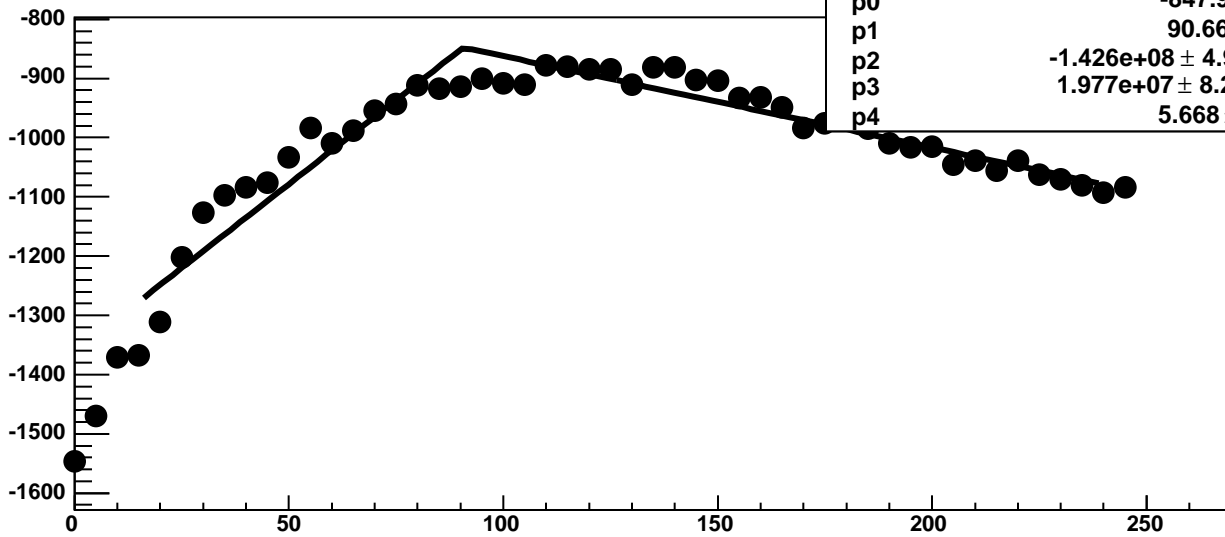
Chip 11, Channel 6, Enable 0, DAC=1600, ADC Noise vs Hold



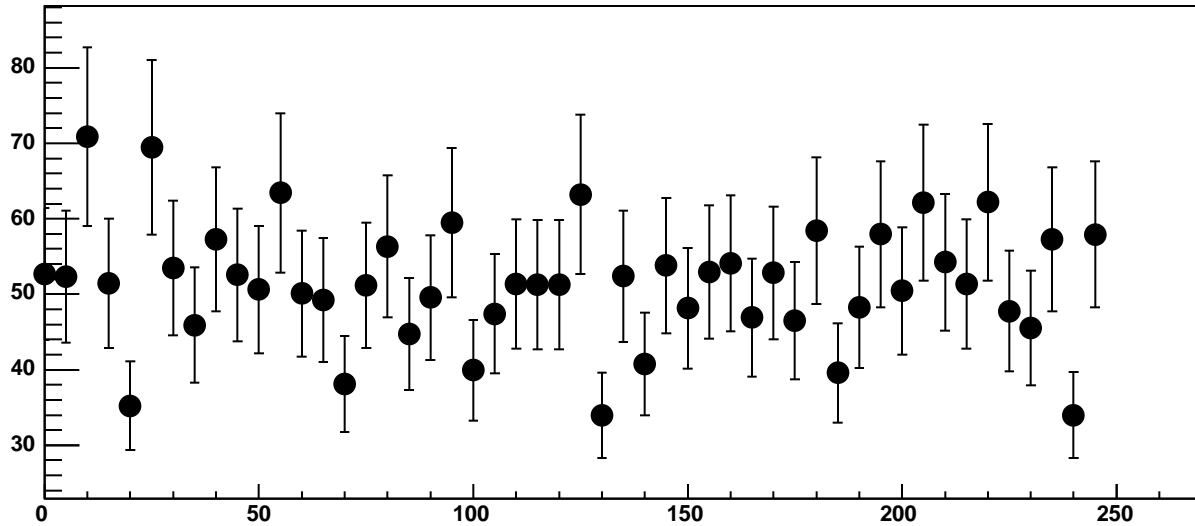
Chip 11, Channel 6, Enable 0, DAC=1600, ADC Residuals vs Hold



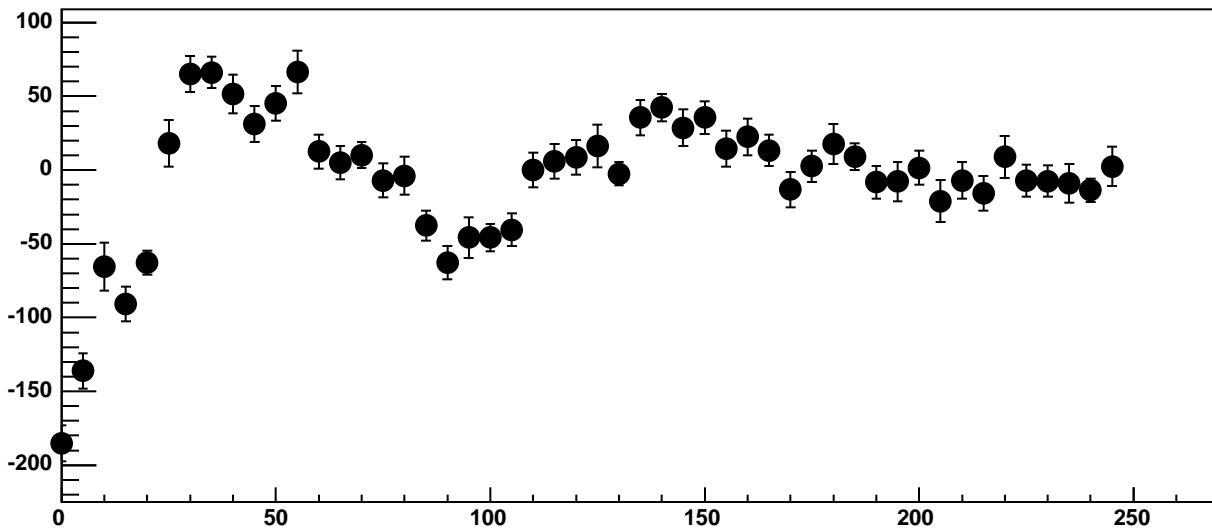
Chip 11, Channel 6, Enable 1, DAC=1600, ADC Mean vs Hold



Chip 11, Channel 6, Enable 1, DAC=1600, ADC Noise vs Hold

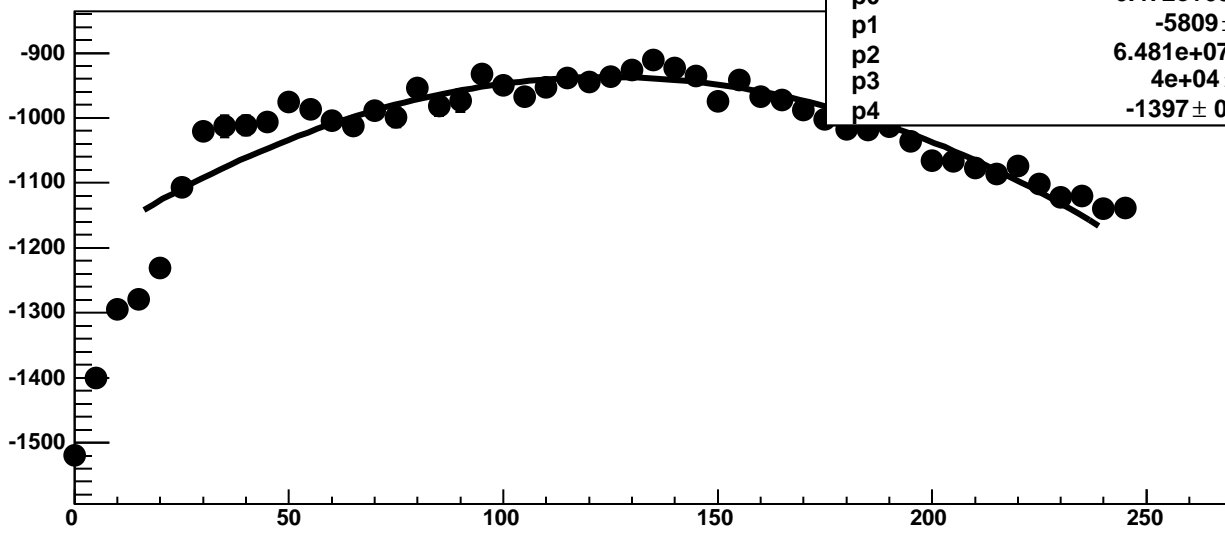


Chip 11, Channel 6, Enable 1, DAC=1600, ADC Residuals vs Hold



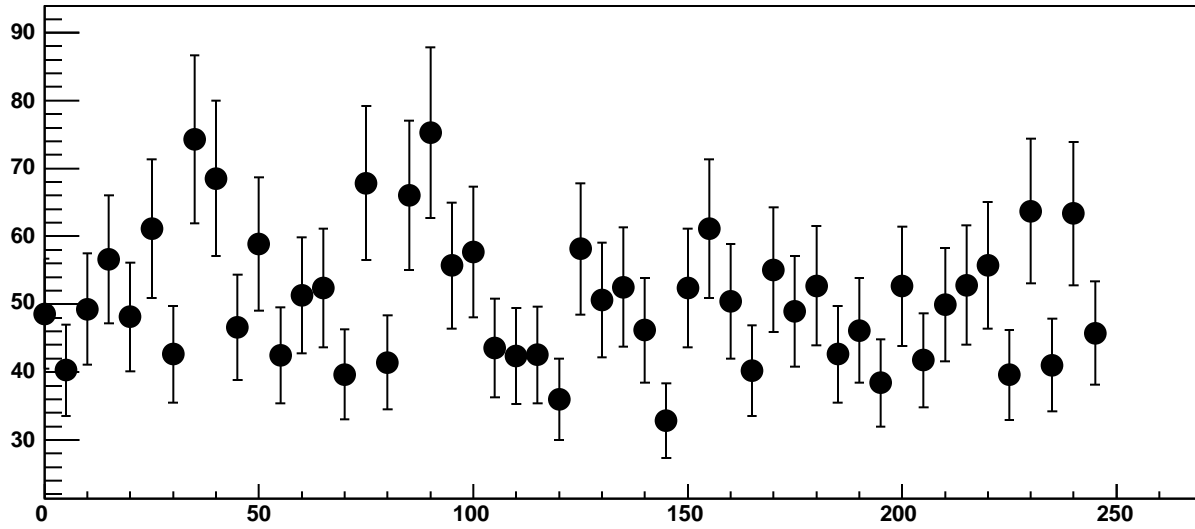


Chip 11, Channel 6, Enable 2, DAC=1600, ADC Mean vs Hold

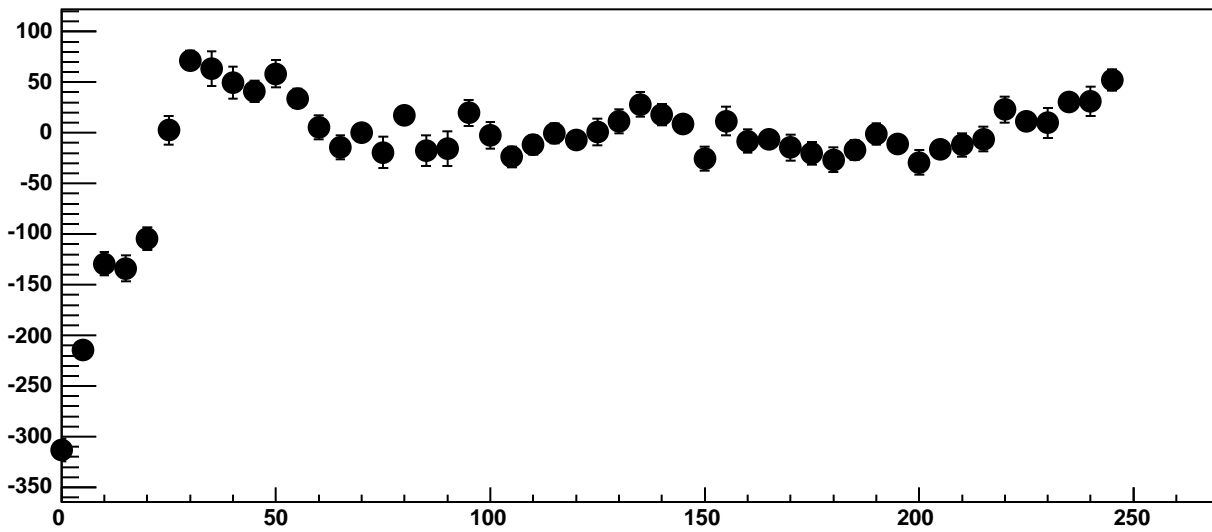


$\chi^2 / \text{ndf}$	398.8 / 41
p0	$-6.472\text{e}+05 \pm 22.41$
p1	$-5809 \pm 0.7399$
p2	$6.481\text{e}+07 \pm 162.5$
p3	$4\text{e}+04 \pm 0.1081$
p4	$-1397 \pm 0.003774$

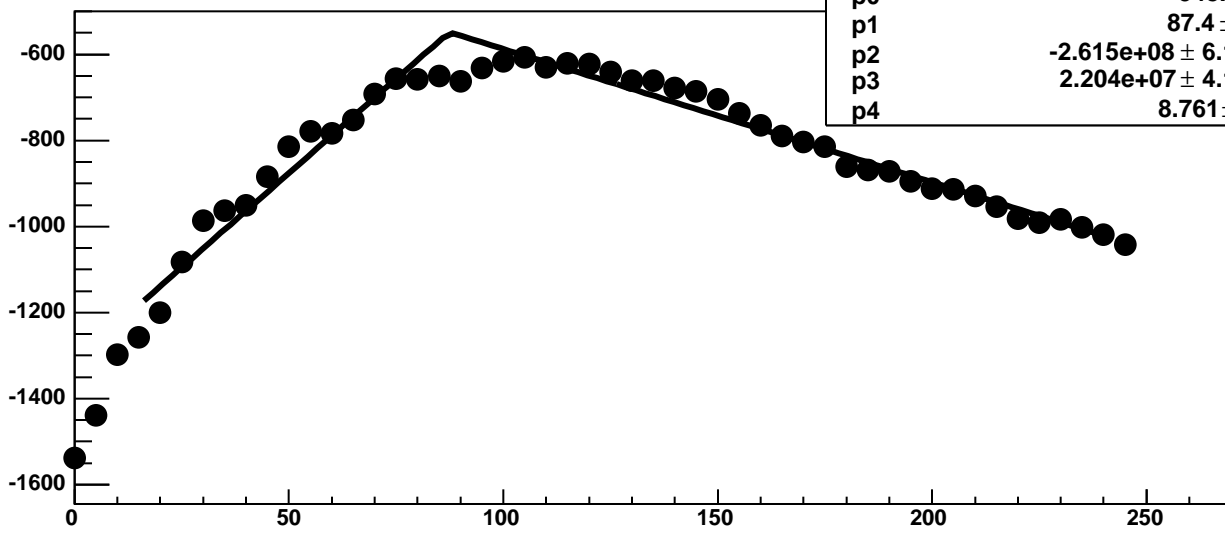
Chip 11, Channel 6, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 6, Enable 2, DAC=1600, ADC Residuals vs Hold

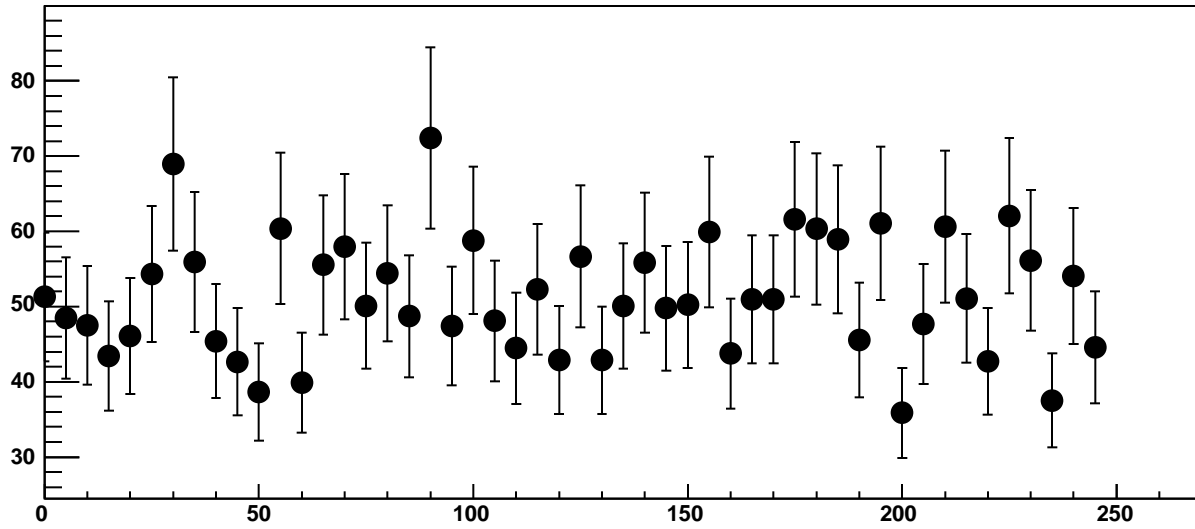


Chip 11, Channel 6, Enable 3, DAC=1600, ADC Mean vs Hold

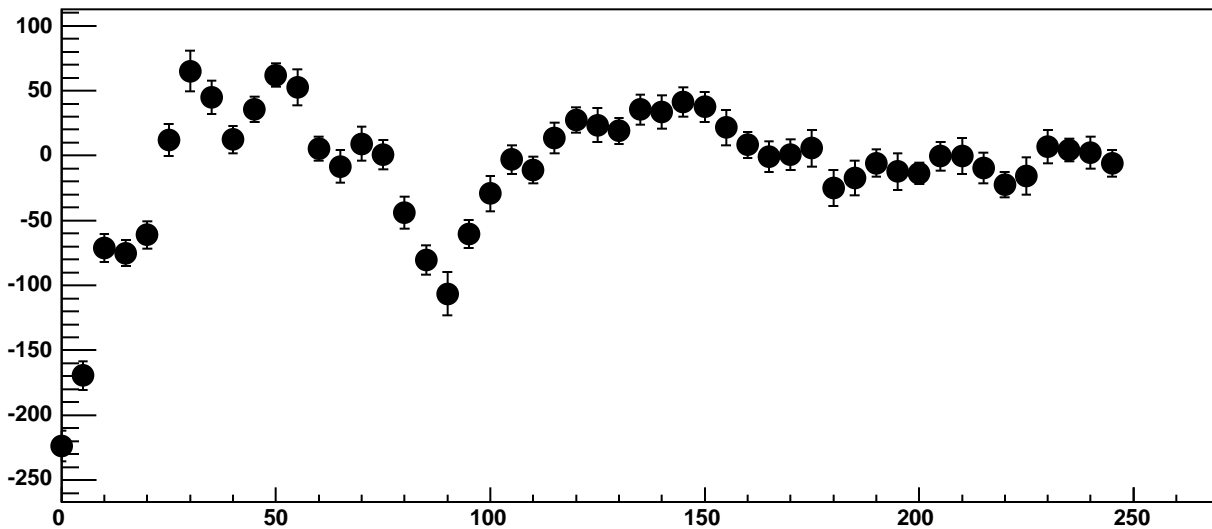


$\chi^2 / \text{ndf}$	417.7 / 41
p0	$-548.3 \pm 3.51$
p1	$87.4 \pm 0.6135$
p2	$-2.615\text{e}+08 \pm 6.135\text{e}+06$
p3	$2.204\text{e}+07 \pm 4.113\text{e}+05$
p4	$8.761 \pm 0.1367$

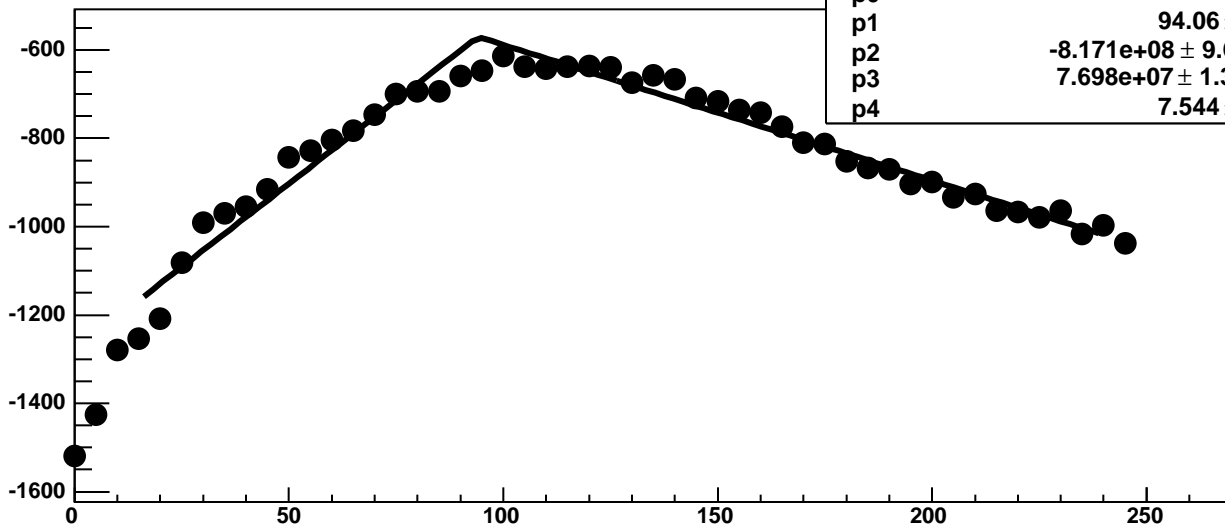
Chip 11, Channel 6, Enable 3, DAC=1600, ADC Noise vs Hold



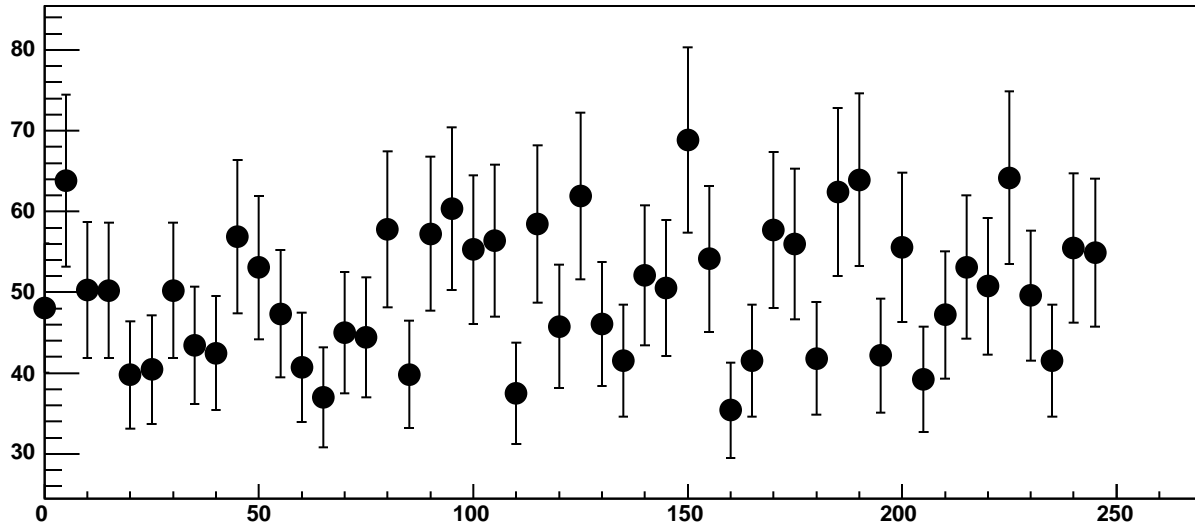
Chip 11, Channel 6, Enable 3, DAC=1600, ADC Residuals vs Hold



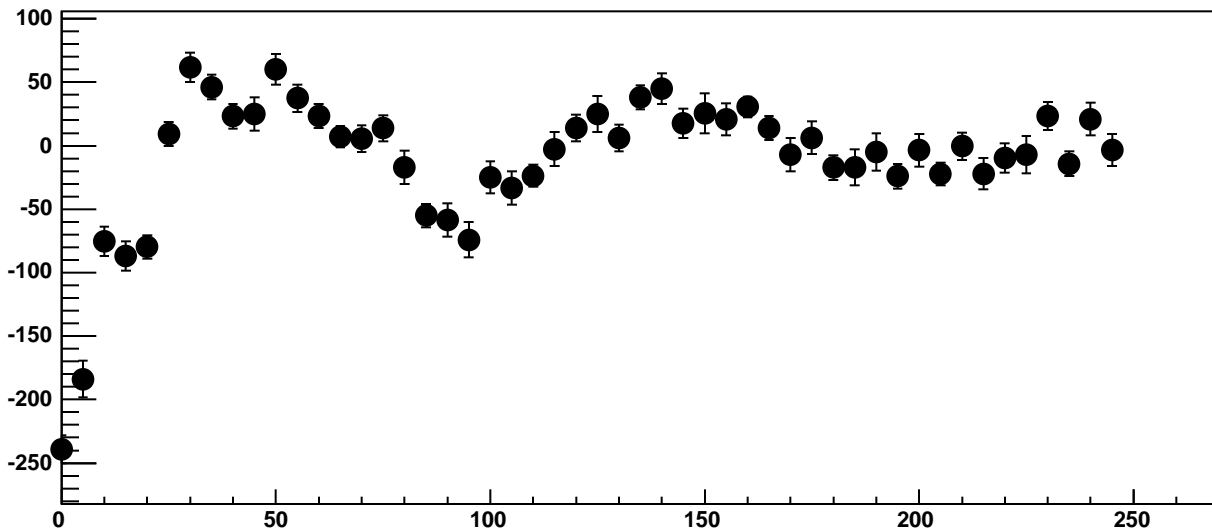
Chip 11, Channel 6, Enable 4, DAC=1600, ADC Mean vs Hold



Chip 11, Channel 6, Enable 4, DAC=1600, ADC Noise vs Hold

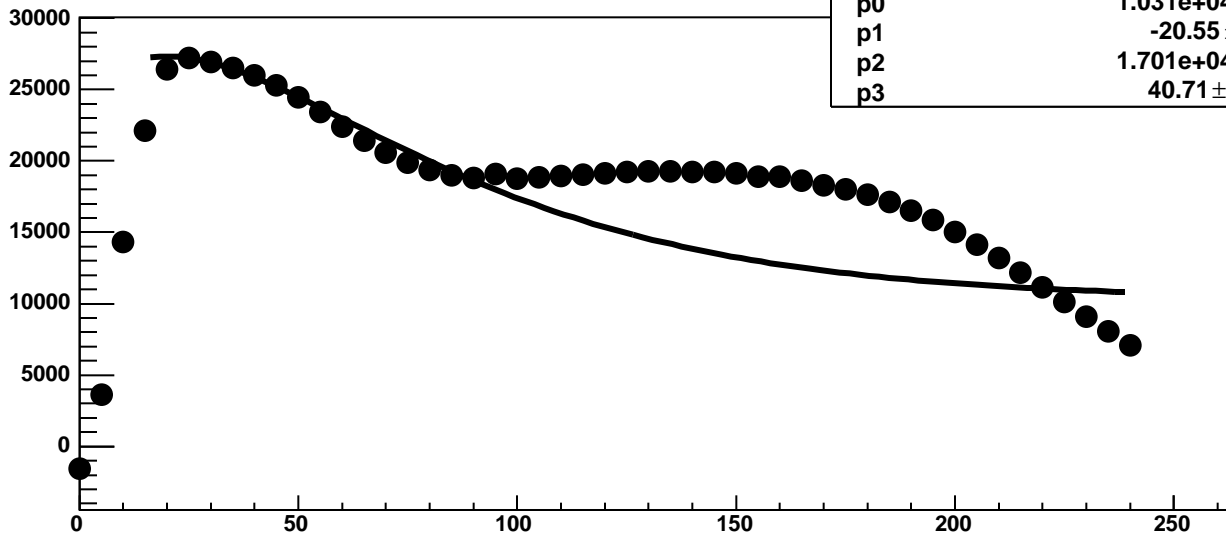


Chip 11, Channel 6, Enable 4, DAC=1600, ADC Residuals vs Hold

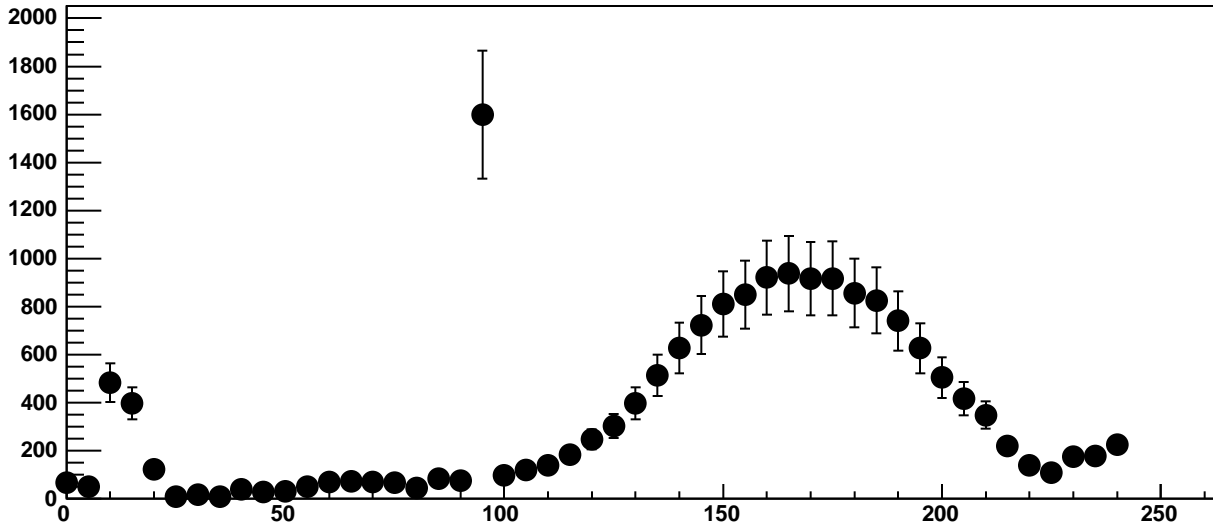


Chip 11, Channel 6, Enable 5!, DAC=1600, ADC Mean vs Hold

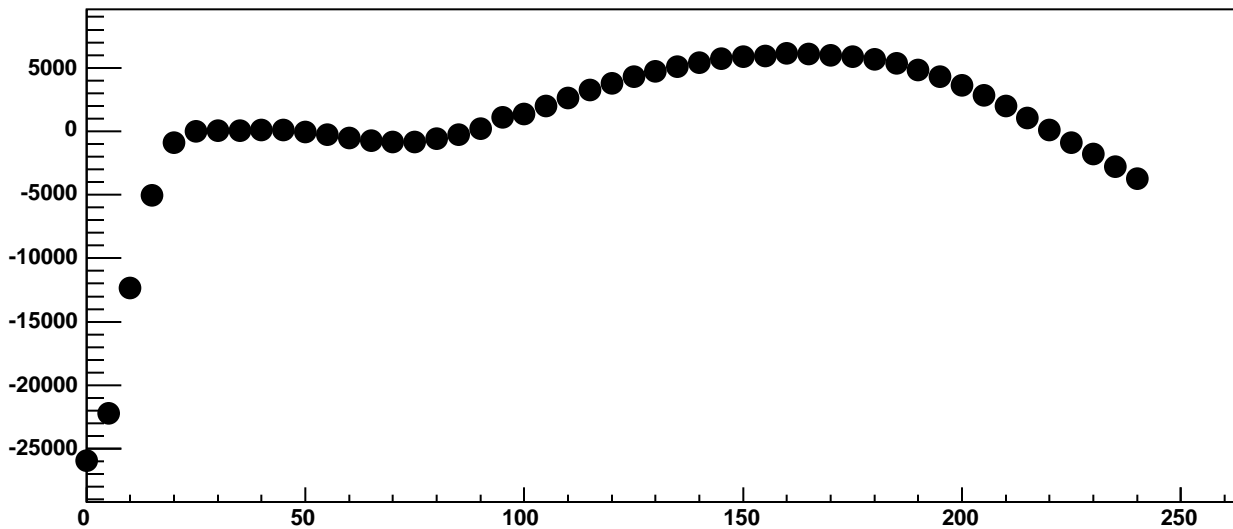
$\chi^2 / \text{ndf}$	7.948e+04 / 42
p0	1.031e+04 $\pm$ 19.07
p1	-20.55 $\pm$ 0.1446
p2	1.701e+04 $\pm$ 21.15
p3	40.71 $\pm$ 0.08247



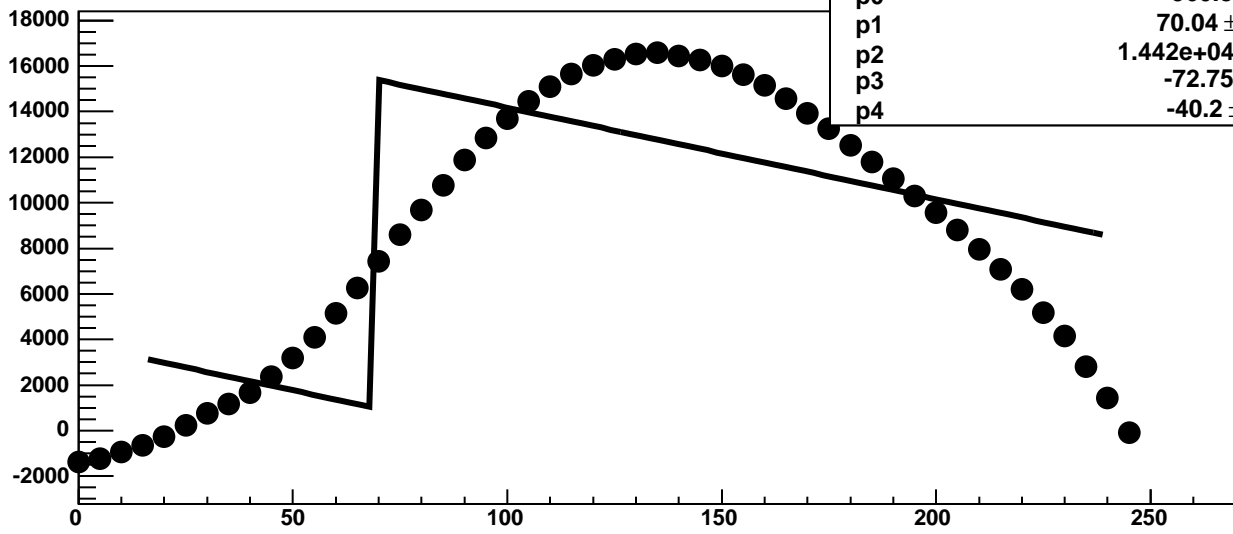
Chip 11, Channel 6, Enable 5!, DAC=1600, ADC Noise vs Hold



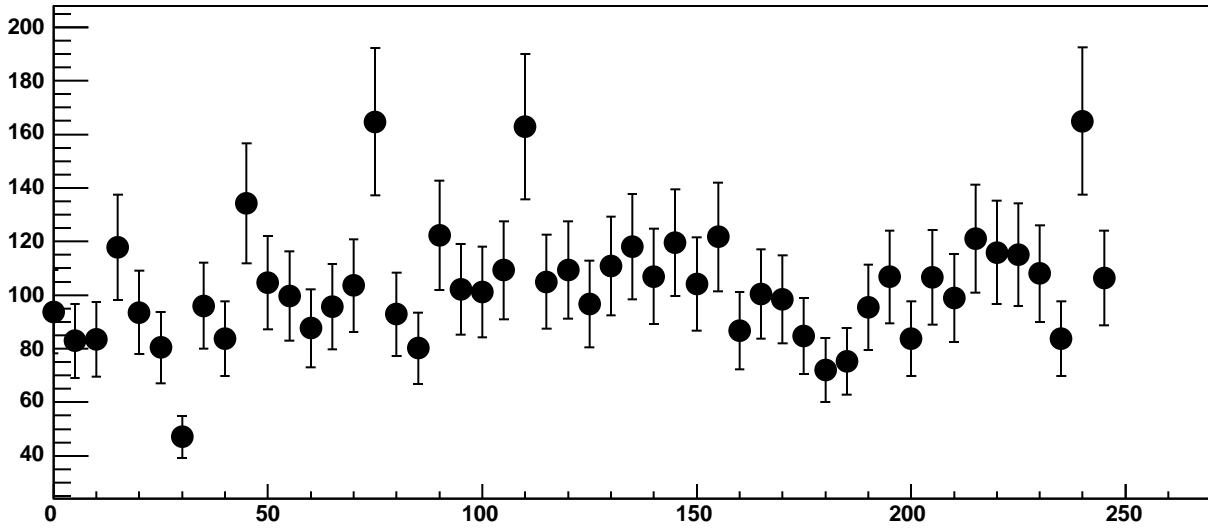
Chip 11, Channel 6, Enable 5!, DAC=1600, ADC Residuals vs Hold



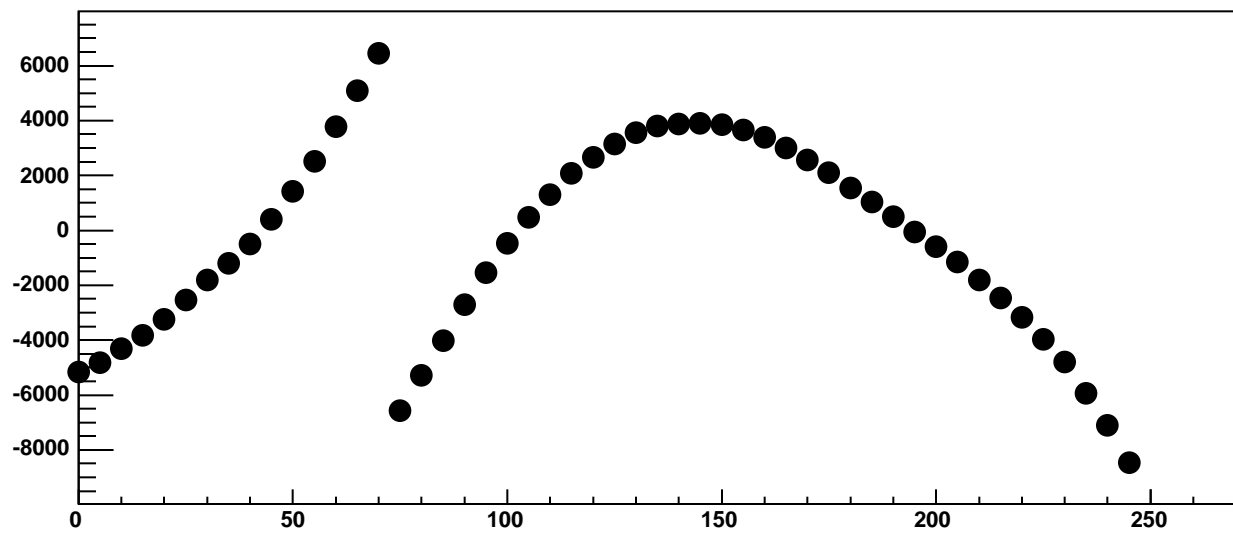
Chip 11, Channel 7, Enable 0, DAC=1600, ADC Mean vs Hold



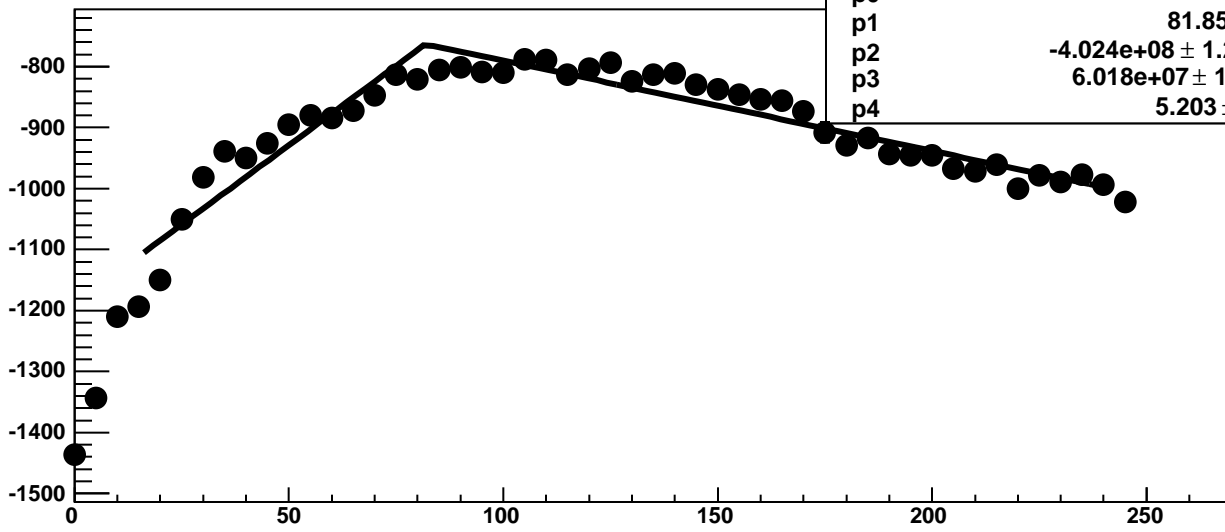
Chip 11, Channel 7, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 7, Enable 0, DAC=1600, ADC Residuals vs Hold

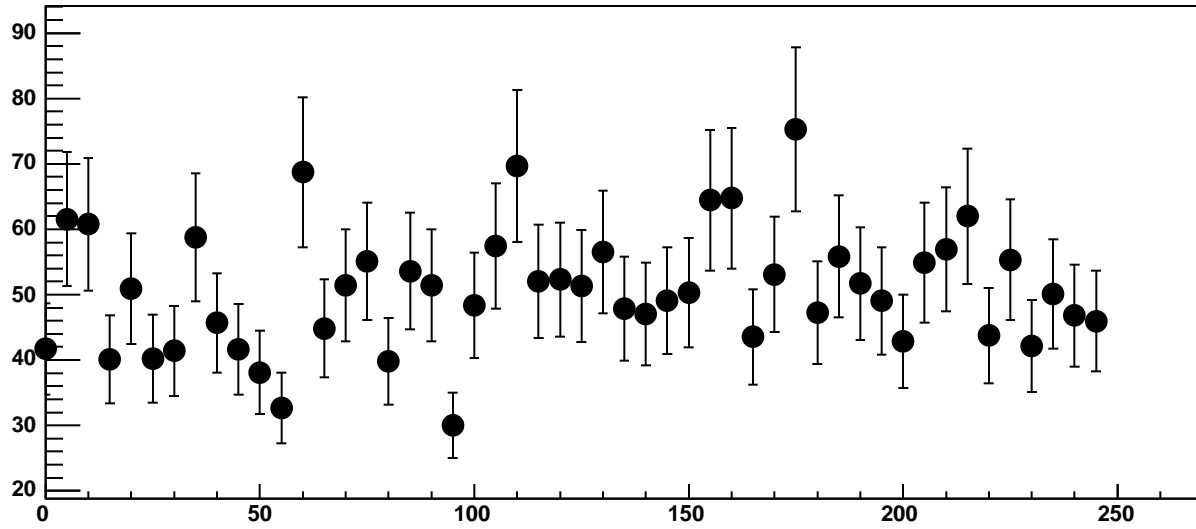


Chip 11, Channel 7, Enable 1, DAC=1600, ADC Mean vs Hold

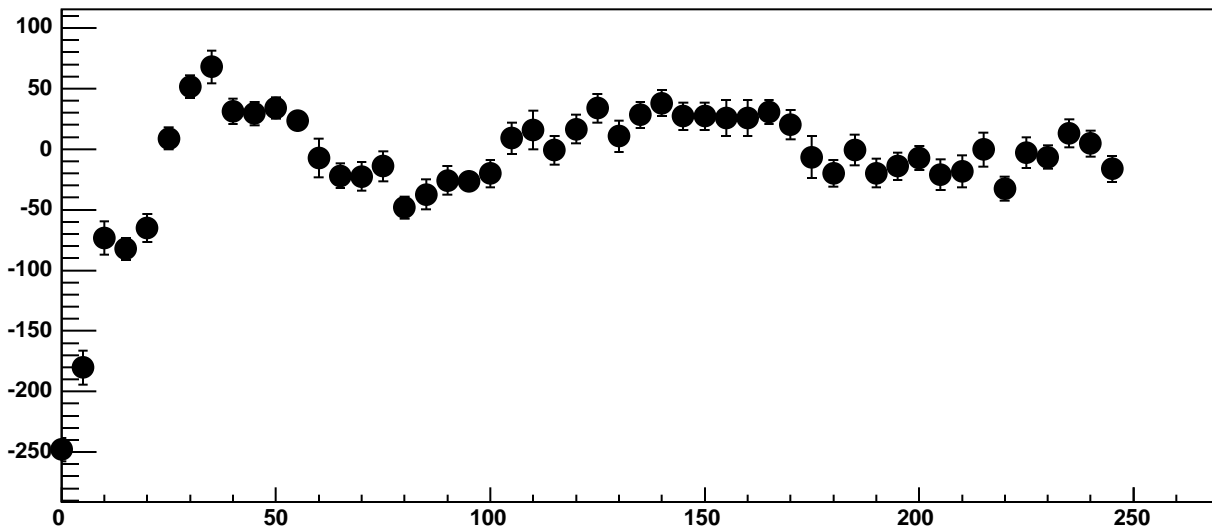


$\chi^2 / \text{ndf}$	366.5 / 41
p0	-763 ± 3.272
p1	81.85 ± 1.003
p2	-4.024e+08 ± 1.249e+07
p3	6.018e+07 ± 1.35e+06
p4	5.203 ± 0.1353

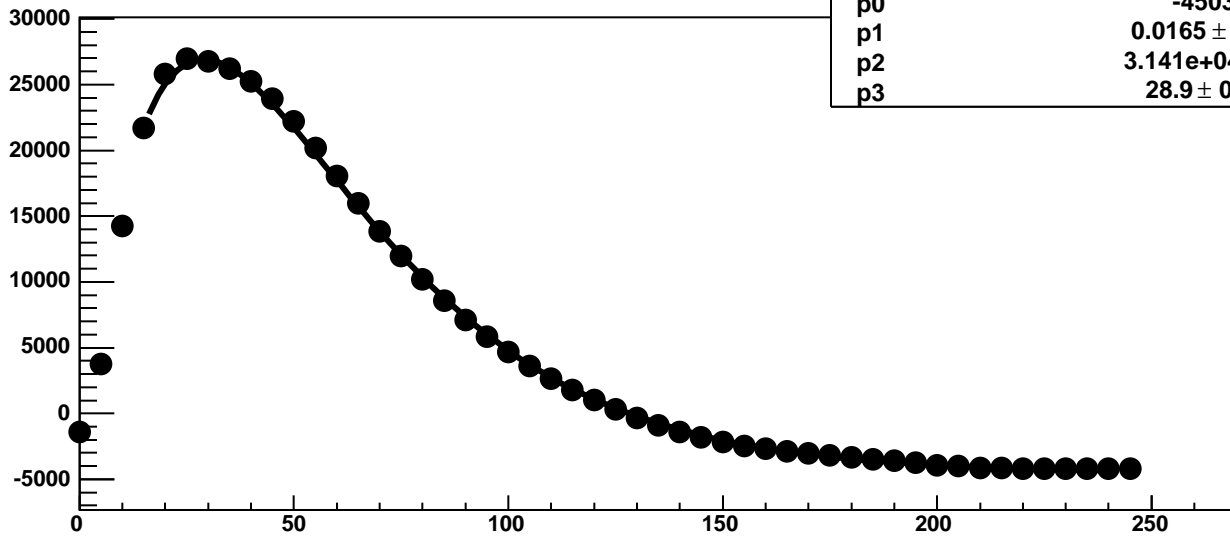
Chip 11, Channel 7, Enable 1, DAC=1600, ADC Noise vs Hold



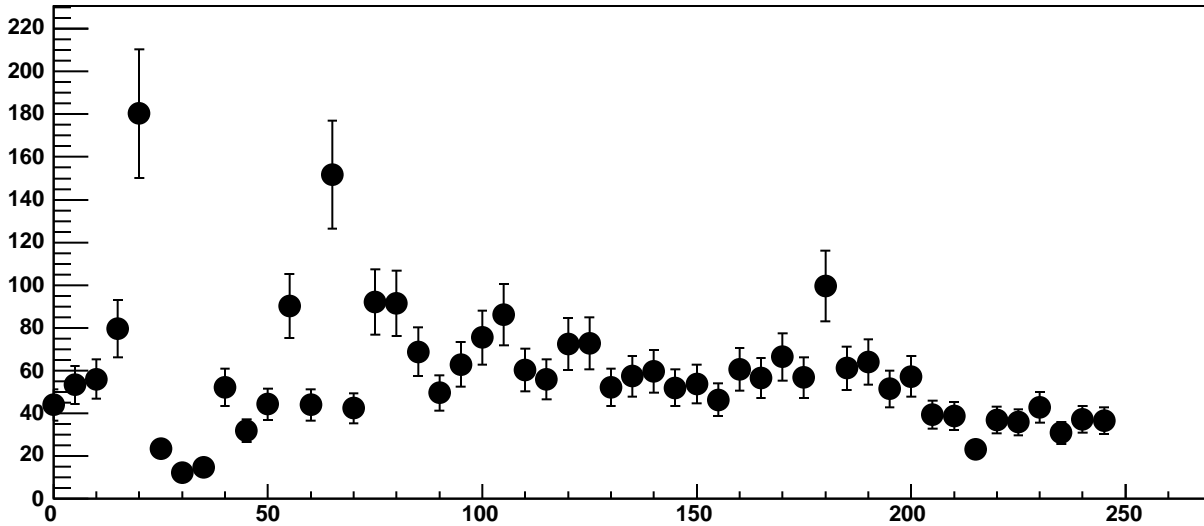
Chip 11, Channel 7, Enable 1, DAC=1600, ADC Residuals vs Hold



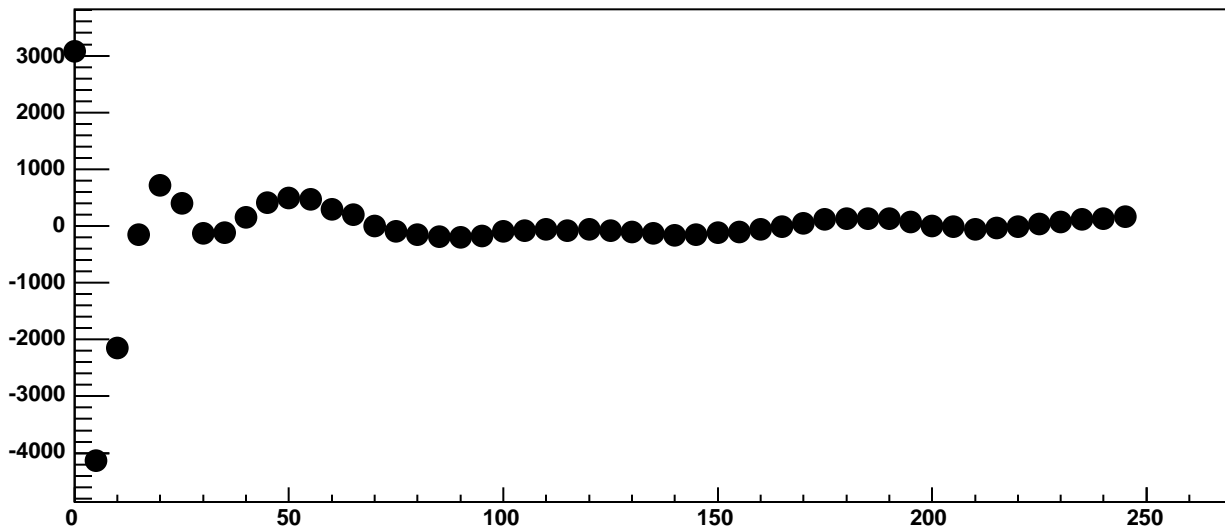
Chip 11, Channel 7, Enable 2!, DAC=1600, ADC Mean vs Hold



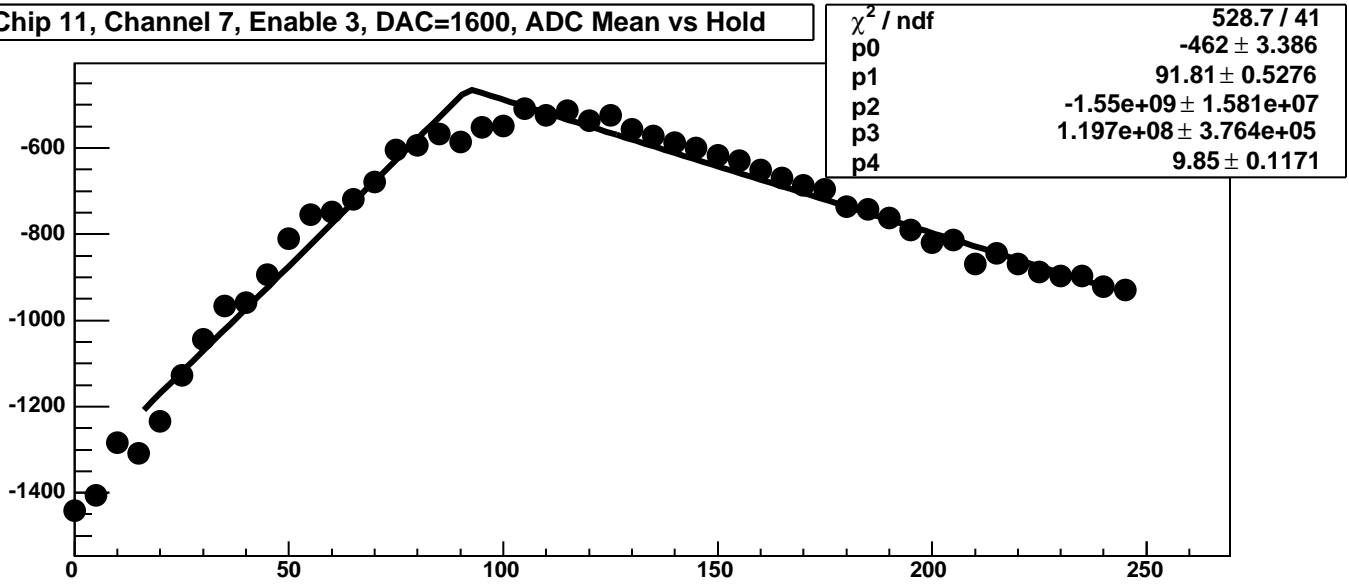
Chip 11, Channel 7, Enable 2!, DAC=1600, ADC Noise vs Hold



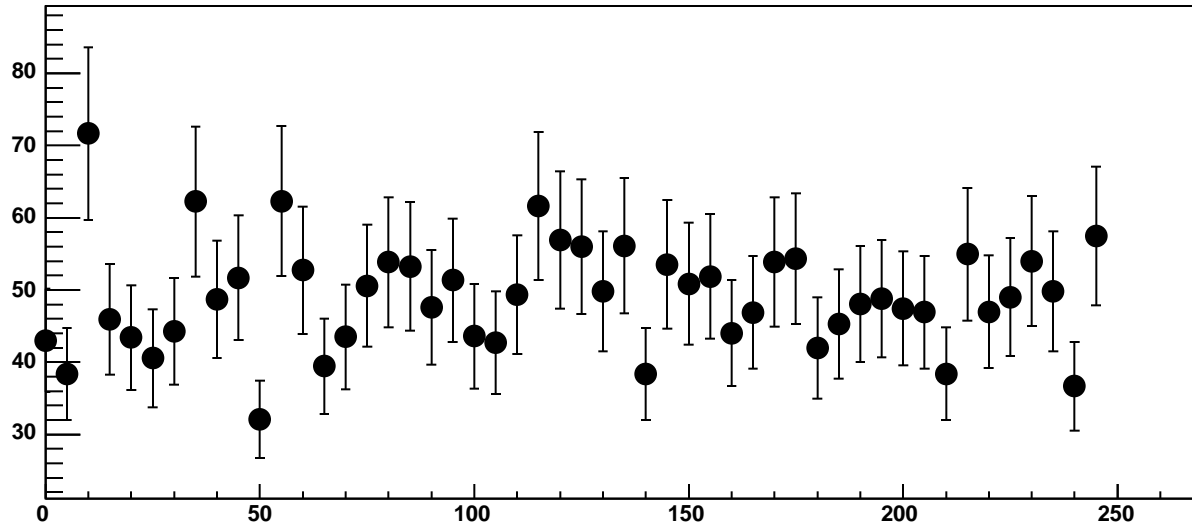
Chip 11, Channel 7, Enable 2!, DAC=1600, ADC Residuals vs Hold



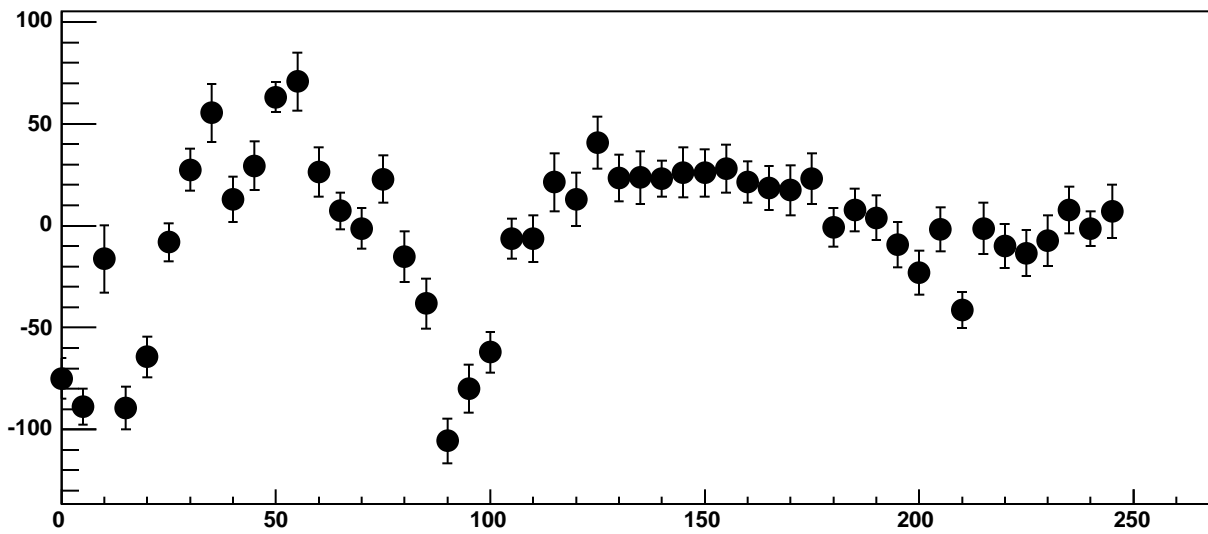
Chip 11, Channel 7, Enable 3, DAC=1600, ADC Mean vs Hold



Chip 11, Channel 7, Enable 3, DAC=1600, ADC Noise vs Hold

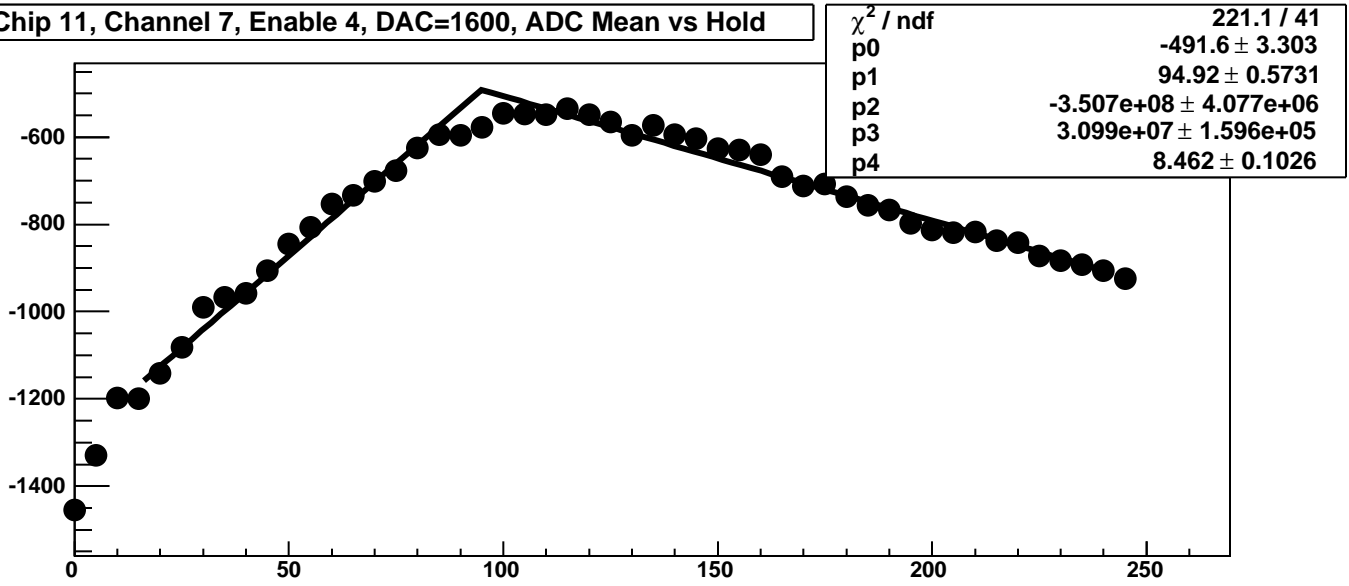


Chip 11, Channel 7, Enable 3, DAC=1600, ADC Residuals vs Hold

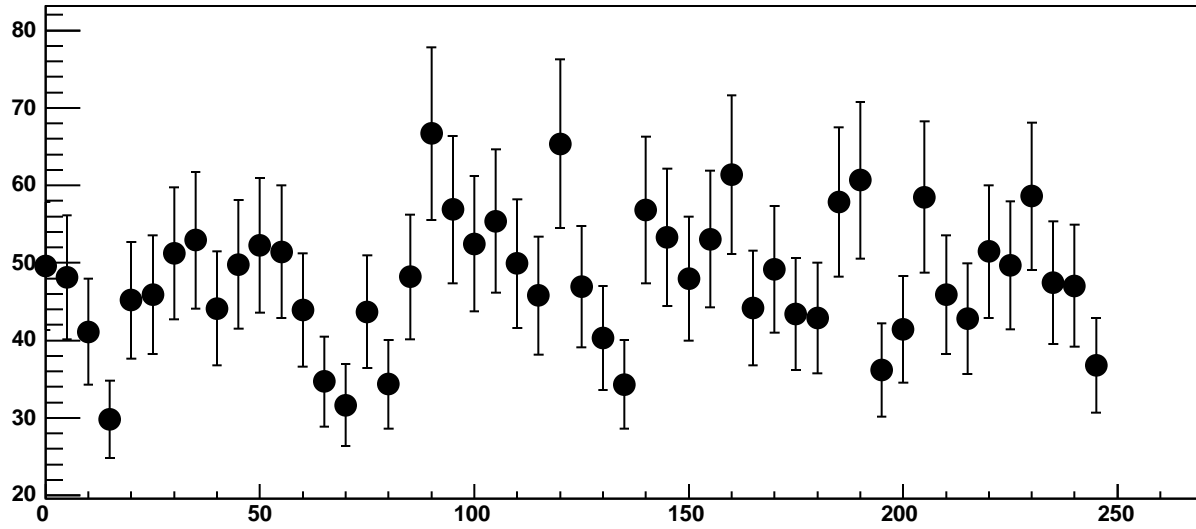




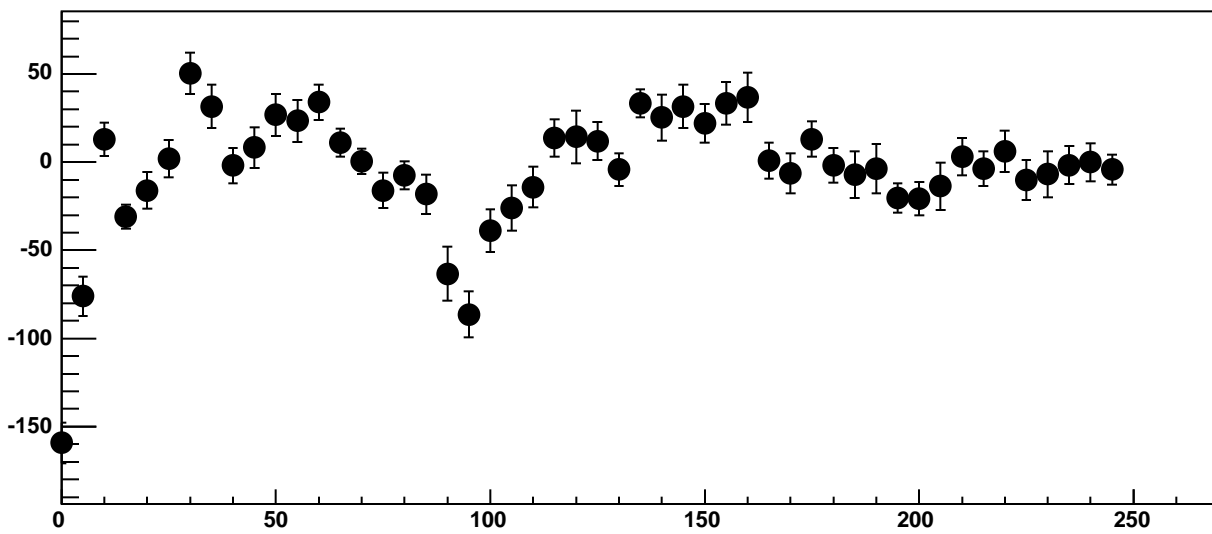
Chip 11, Channel 7, Enable 4, DAC=1600, ADC Mean vs Hold



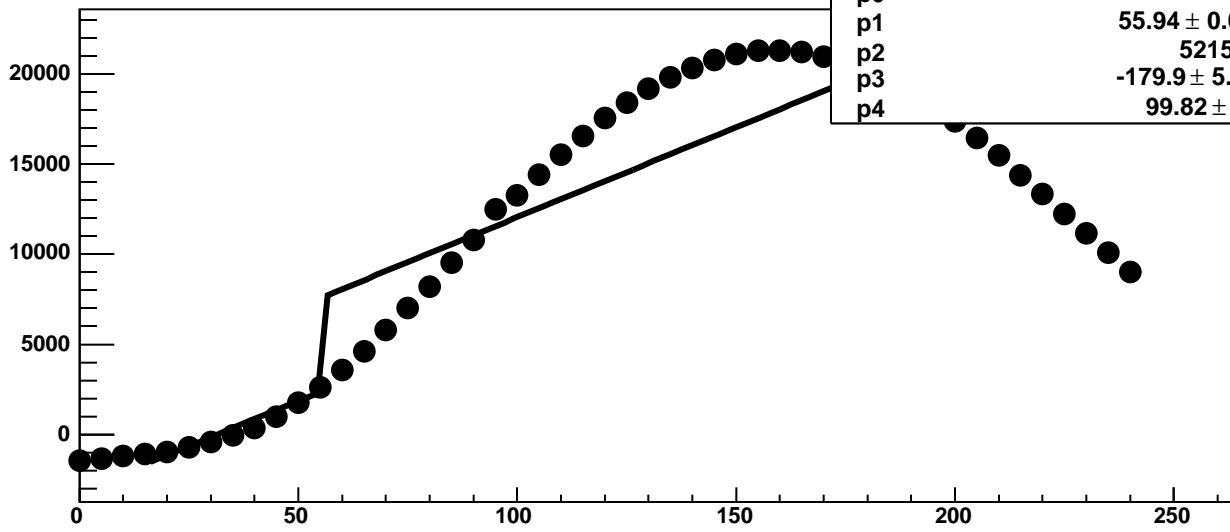
Chip 11, Channel 7, Enable 4, DAC=1600, ADC Noise vs Hold



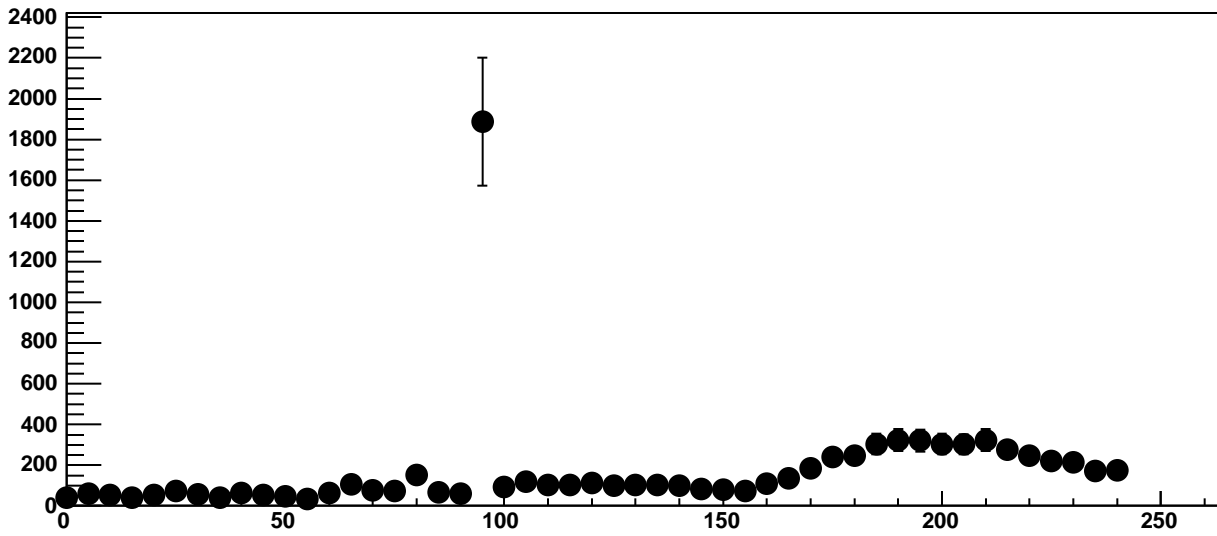
Chip 11, Channel 7, Enable 4, DAC=1600, ADC Residuals vs Hold



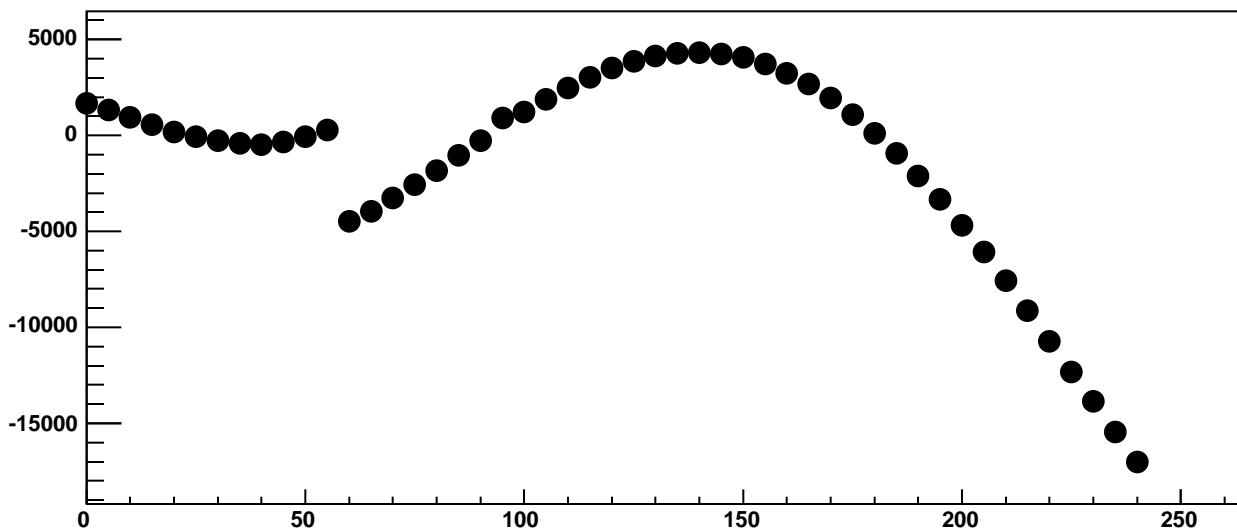
Chip 11, Channel 7, Enable 5, DAC=1600, ADC Mean vs Hold



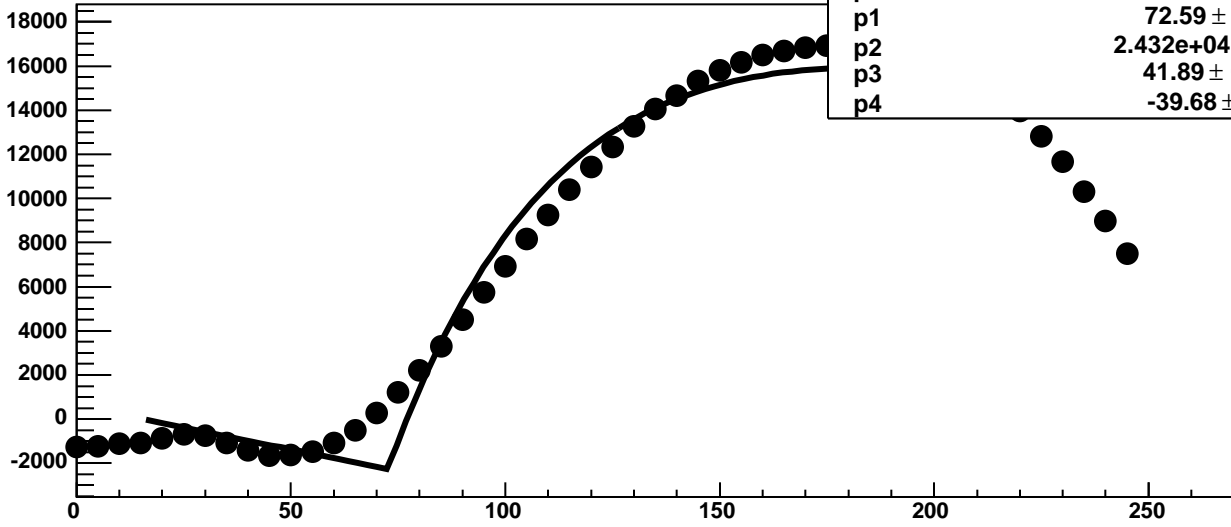
Chip 11, Channel 7, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 7, Enable 5, DAC=1600, ADC Residuals vs Hold

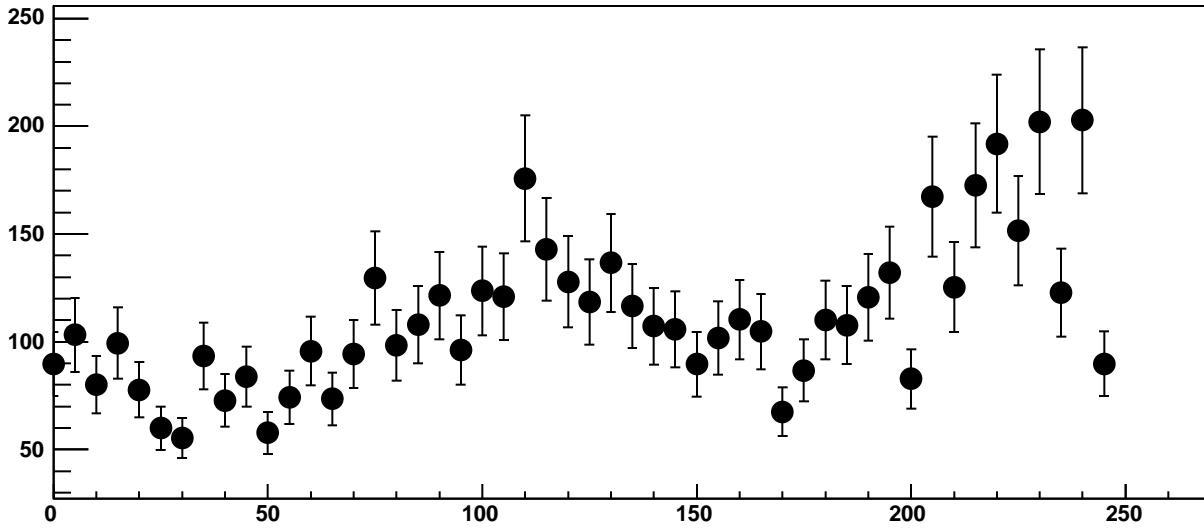


Chip 11, Channel 8, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$	1.239e+05 / 41
p0	-2268 ± 8.484
p1	72.59 ± 0.03631
p2	2.432e+04 ± 46.27
p3	41.89 ± 0.09855
p4	-39.68 ± 0.2434

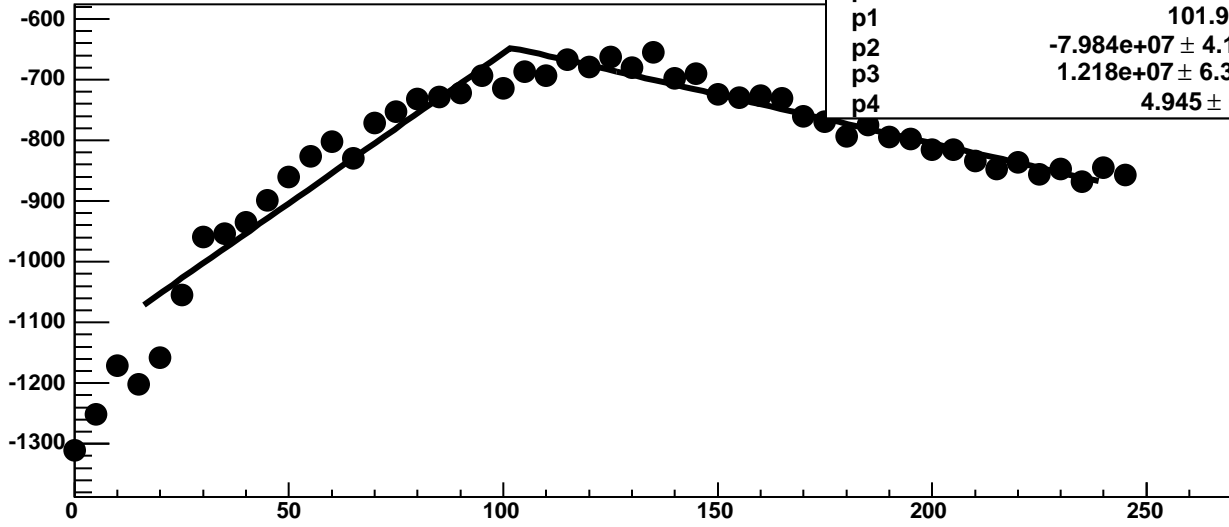
Chip 11, Channel 8, Enable 0, DAC=1600, ADC Noise vs Hold



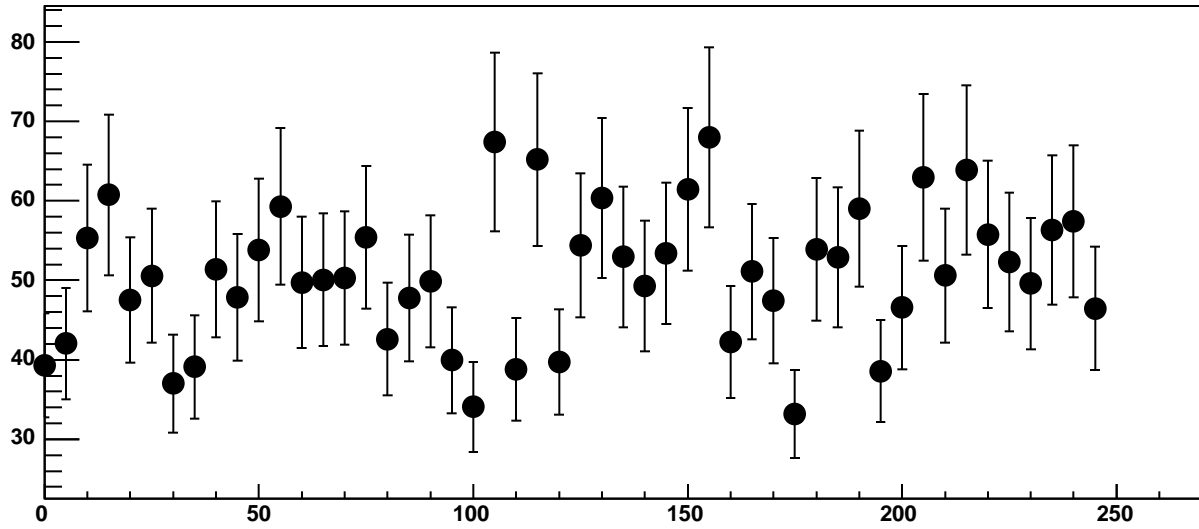
Chip 11, Channel 8, Enable 0, DAC=1600, ADC Residuals vs Hold



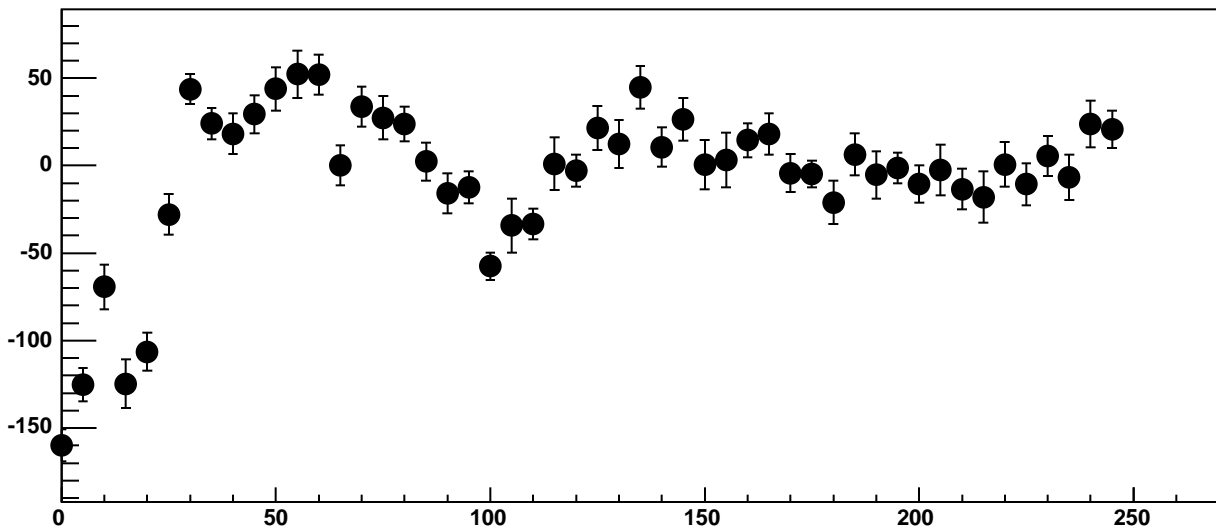
Chip 11, Channel 8, Enable 1, DAC=1600, ADC Mean vs Hold



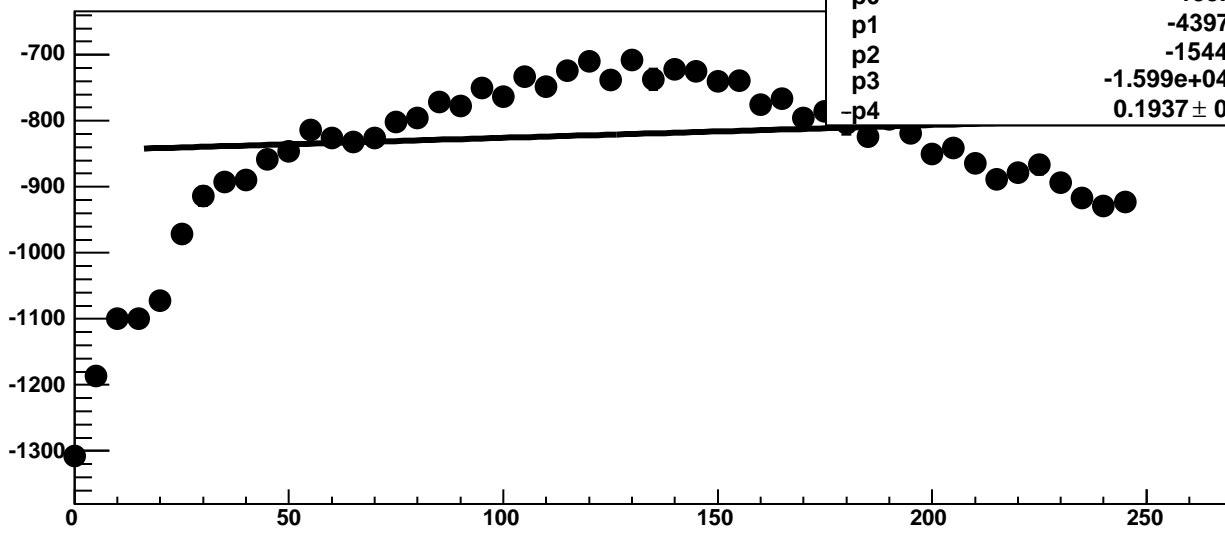
Chip 11, Channel 8, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 8, Enable 1, DAC=1600, ADC Residuals vs Hold

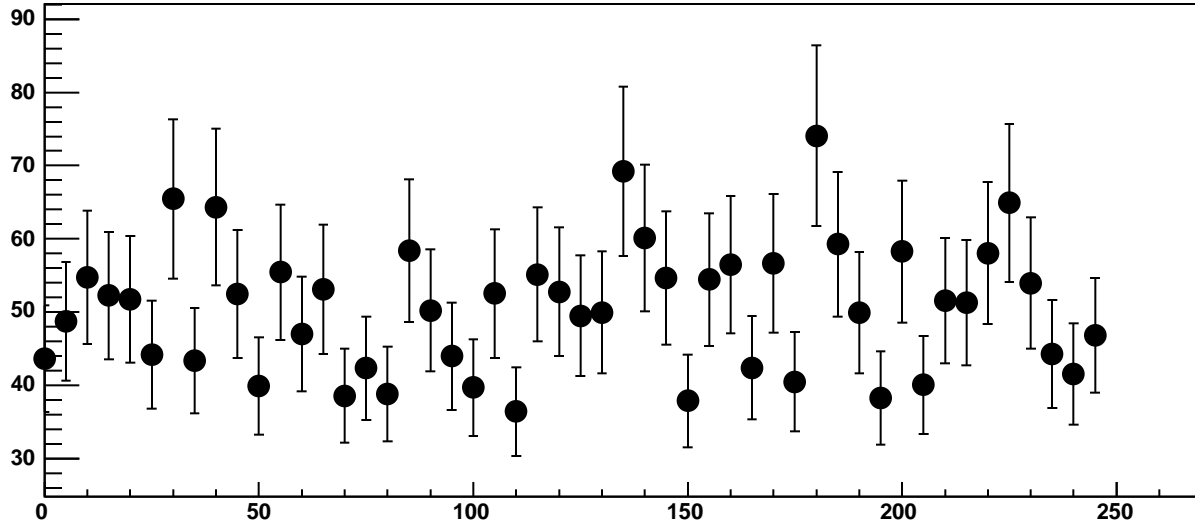


Chip 11, Channel 8, Enable 2, DAC=1600, ADC Mean vs Hold

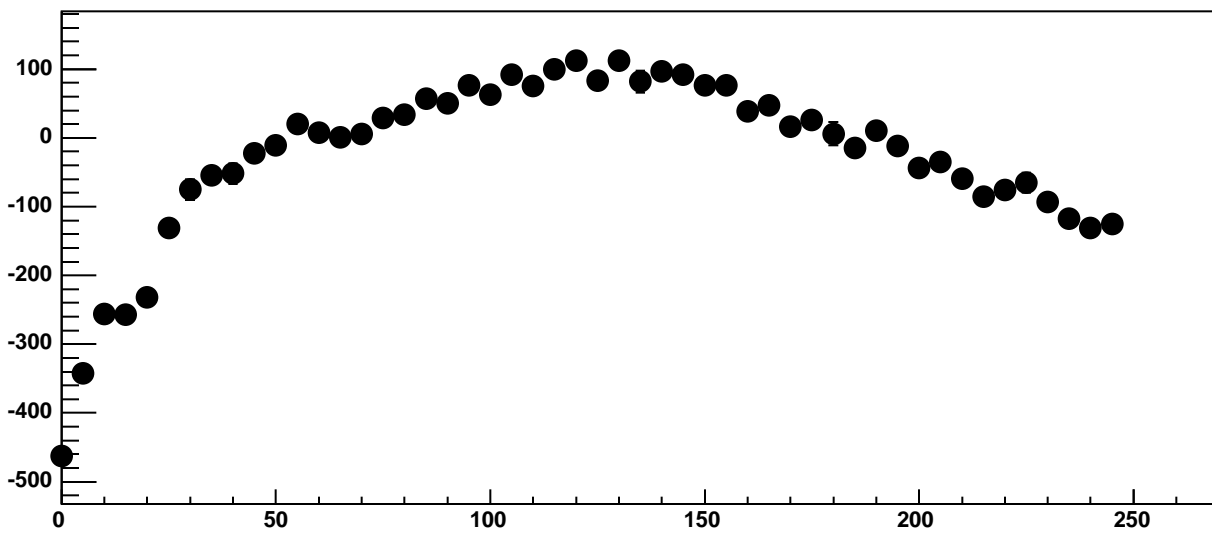


$\chi^2 / \text{ndf}$	2510 / 41
p0	$-153.1 \pm 8.23$
p1	$-4397 \pm 36.46$
p2	$-1544 \pm 10.75$
p3	$-1.599\text{e}+04 \pm 2036$
p4	$0.1937 \pm 0.001819$

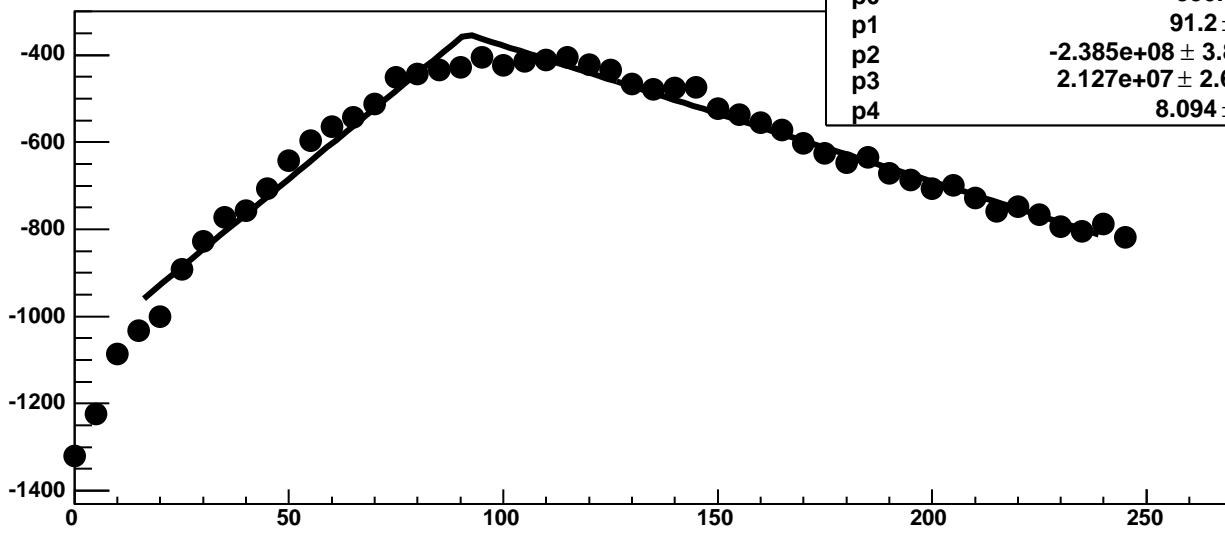
Chip 11, Channel 8, Enable 2, DAC=1600, ADC Noise vs Hold



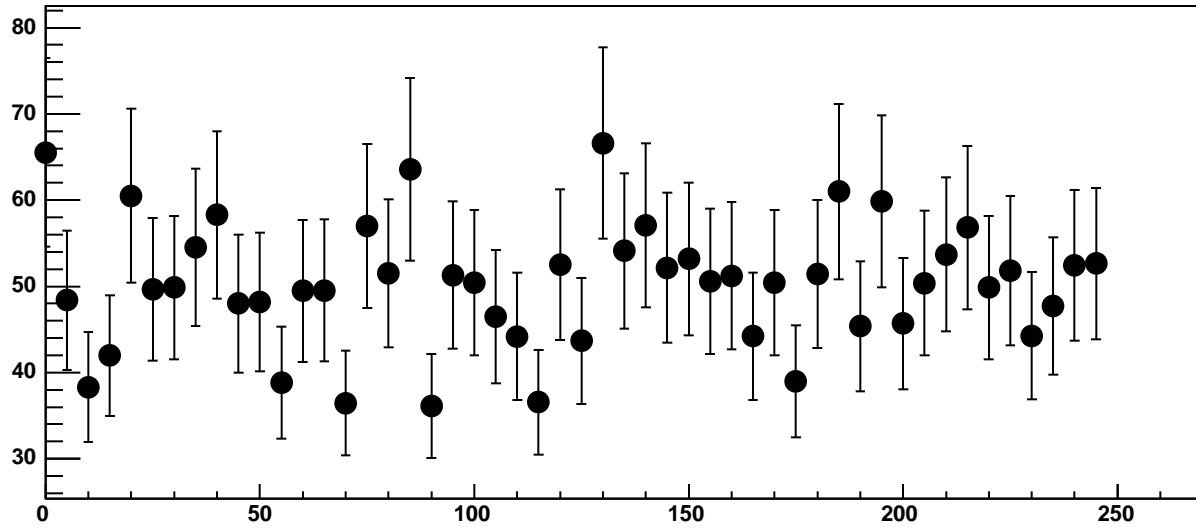
Chip 11, Channel 8, Enable 2, DAC=1600, ADC Residuals vs Hold



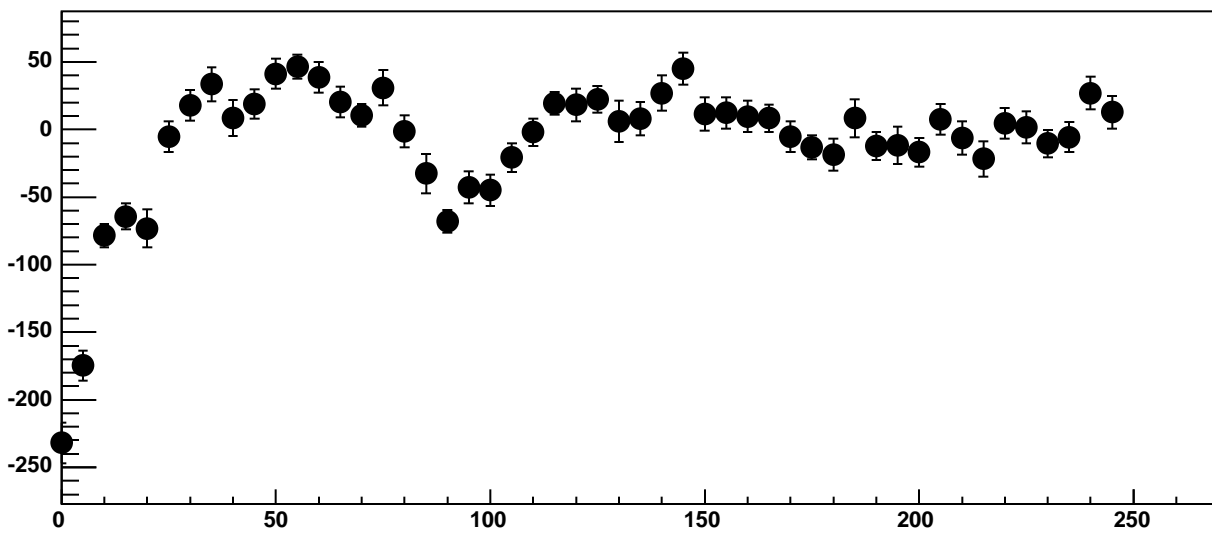
Chip 11, Channel 8, Enable 3, DAC=1600, ADC Mean vs Hold



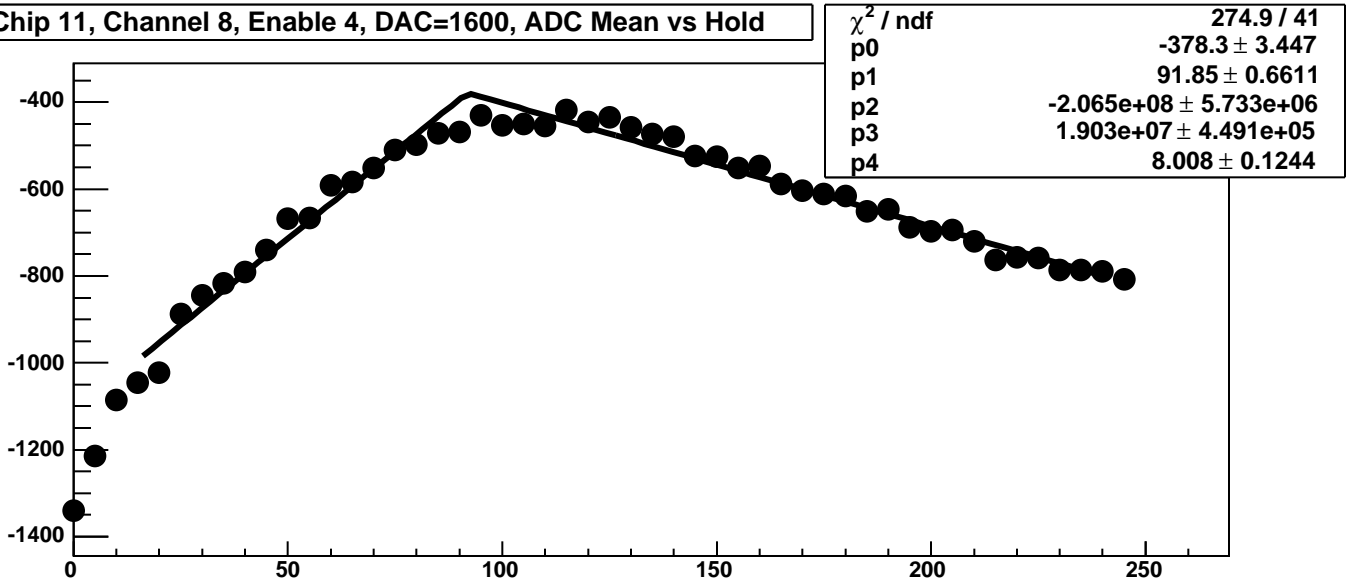
Chip 11, Channel 8, Enable 3, DAC=1600, ADC Noise vs Hold



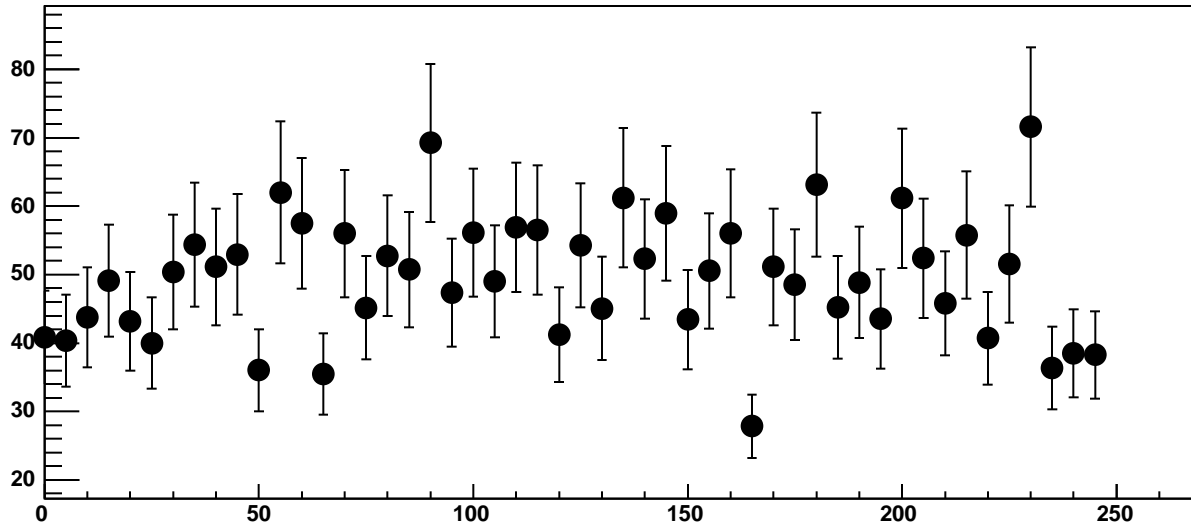
Chip 11, Channel 8, Enable 3, DAC=1600, ADC Residuals vs Hold



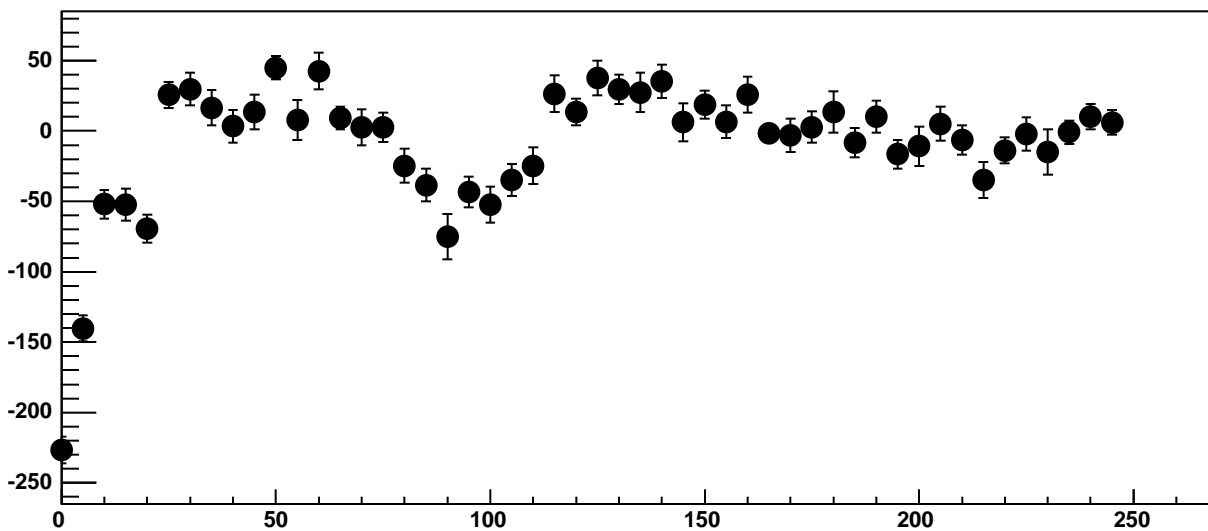
Chip 11, Channel 8, Enable 4, DAC=1600, ADC Mean vs Hold



Chip 11, Channel 8, Enable 4, DAC=1600, ADC Noise vs Hold

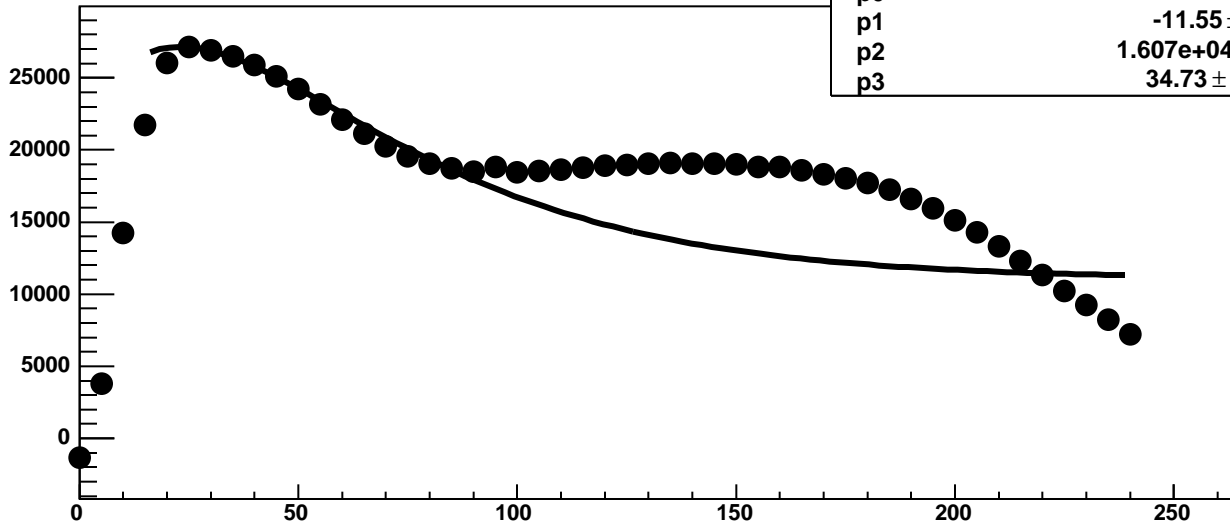


Chip 11, Channel 8, Enable 4, DAC=1600, ADC Residuals vs Hold

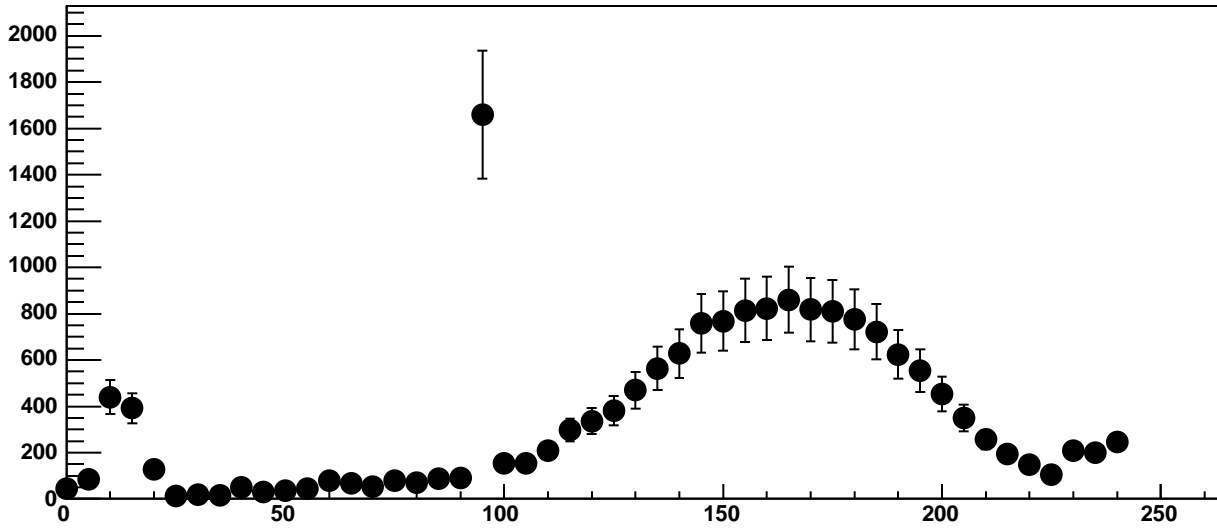


Chip 11, Channel 8, Enable 5!, DAC=1600, ADC Mean vs Hold

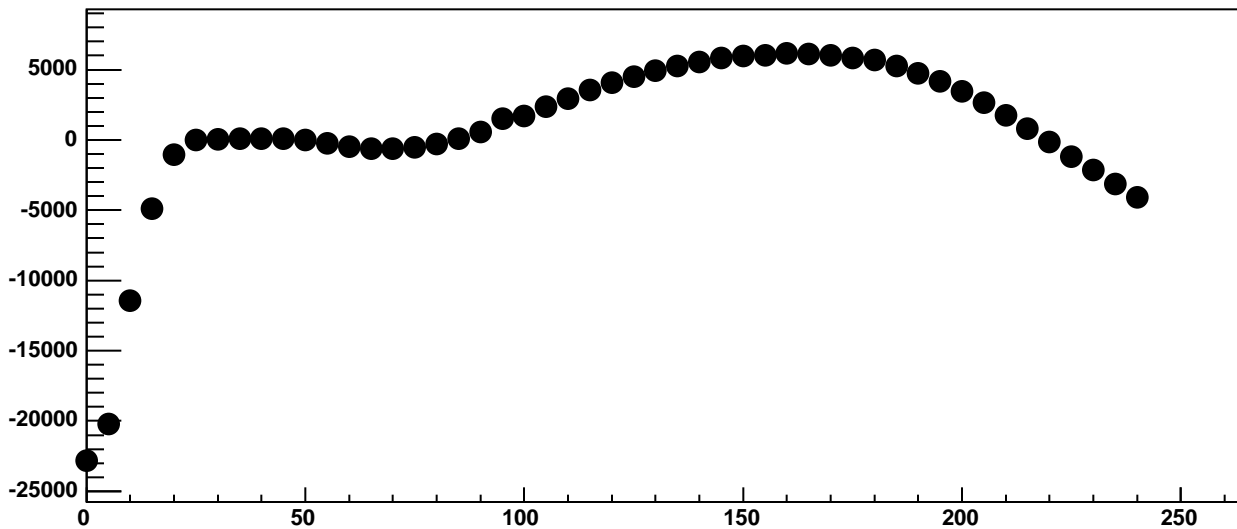
$\chi^2 / \text{ndf}$	6.527e+04 / 42
p0	1.108e+04 $\pm$ 17.26
p1	-11.55 $\pm$ 0.1313
p2	1.607e+04 $\pm$ 18.69
p3	34.73 $\pm$ 0.07374



Chip 11, Channel 8, Enable 5!, DAC=1600, ADC Noise vs Hold

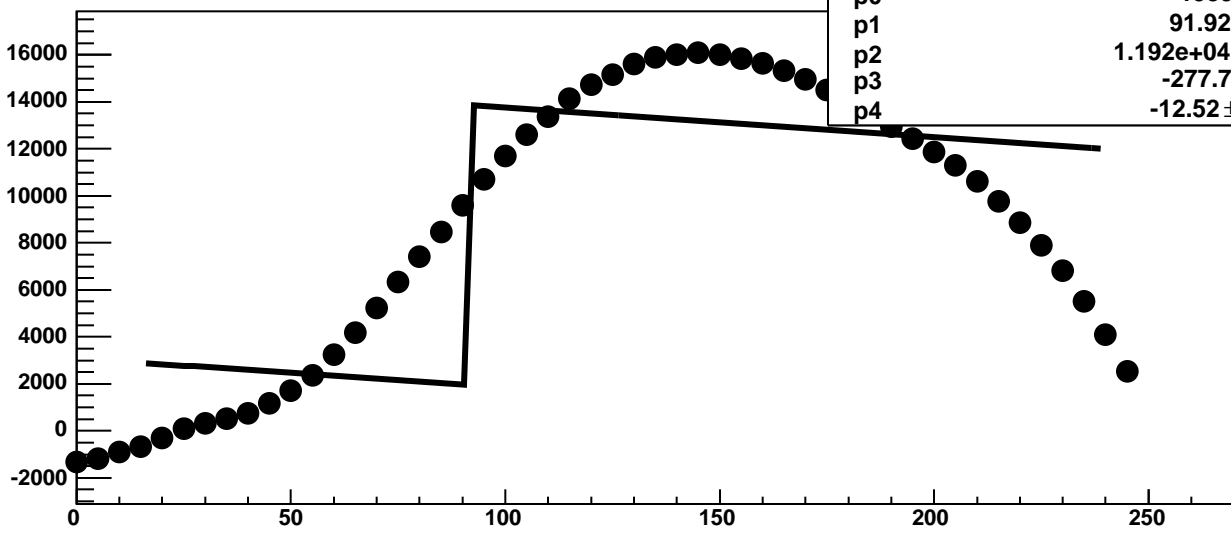


Chip 11, Channel 8, Enable 5!, DAC=1600, ADC Residuals vs Hold

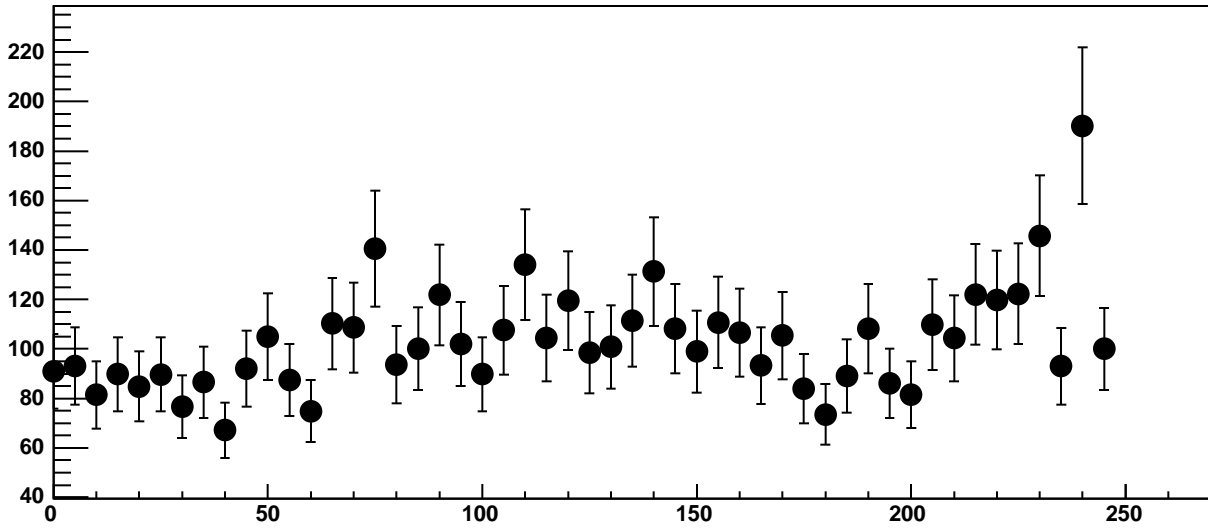




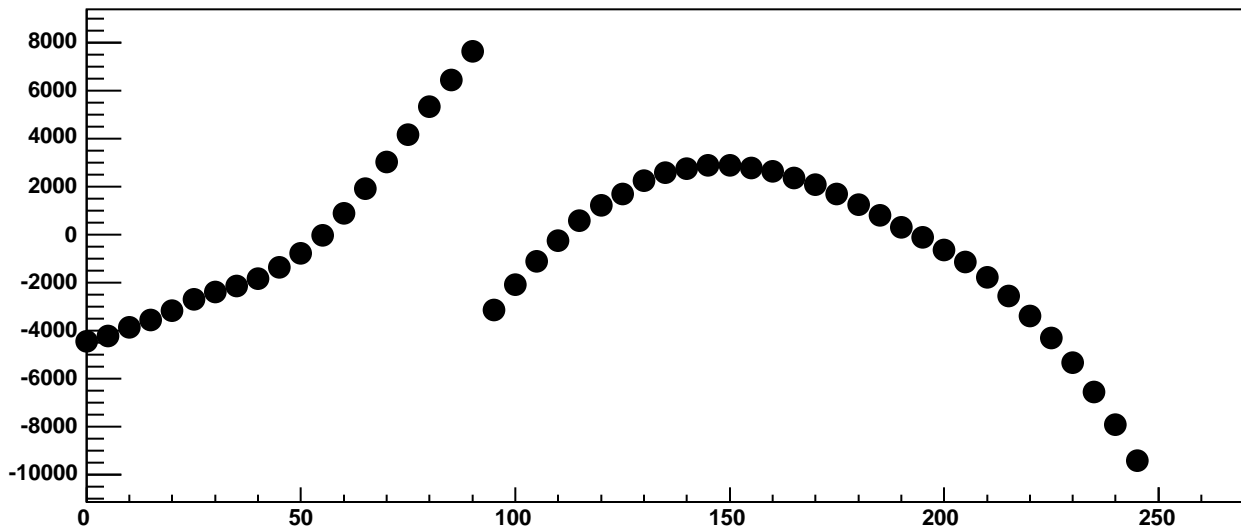
Chip 11, Channel 9, Enable 0, DAC=1600, ADC Mean vs Hold



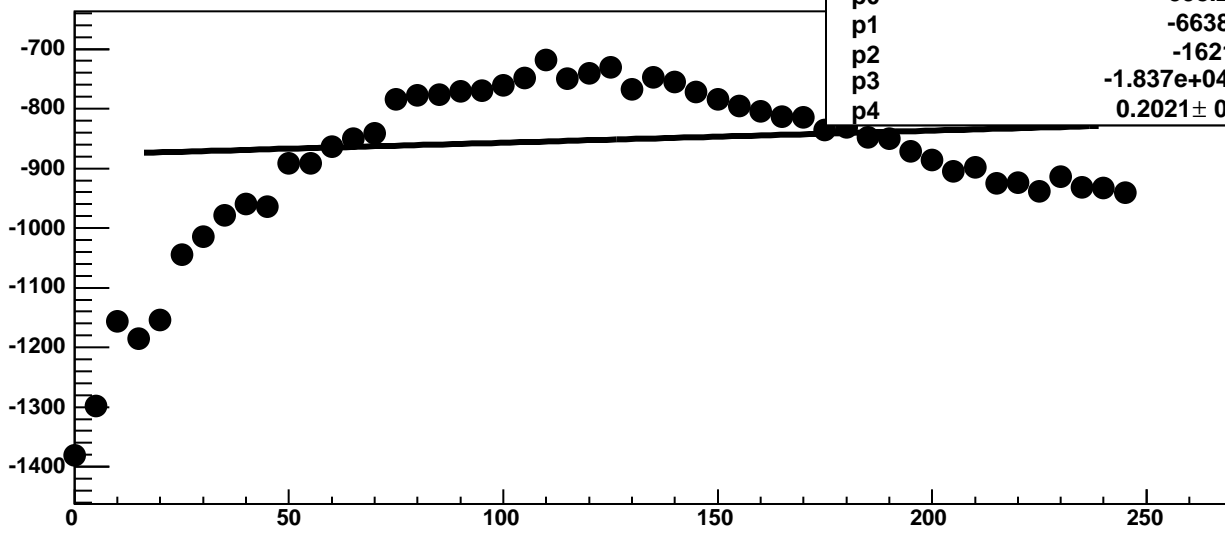
Chip 11, Channel 9, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 9, Enable 0, DAC=1600, ADC Residuals vs Hold

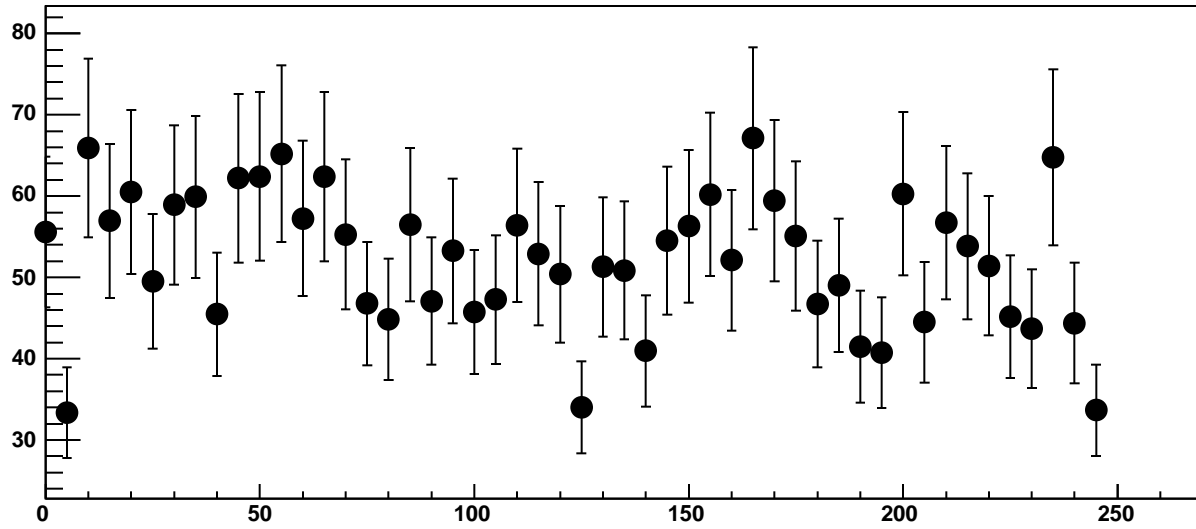


Chip 11, Channel 9, Enable 1, DAC=1600, ADC Mean vs Hold

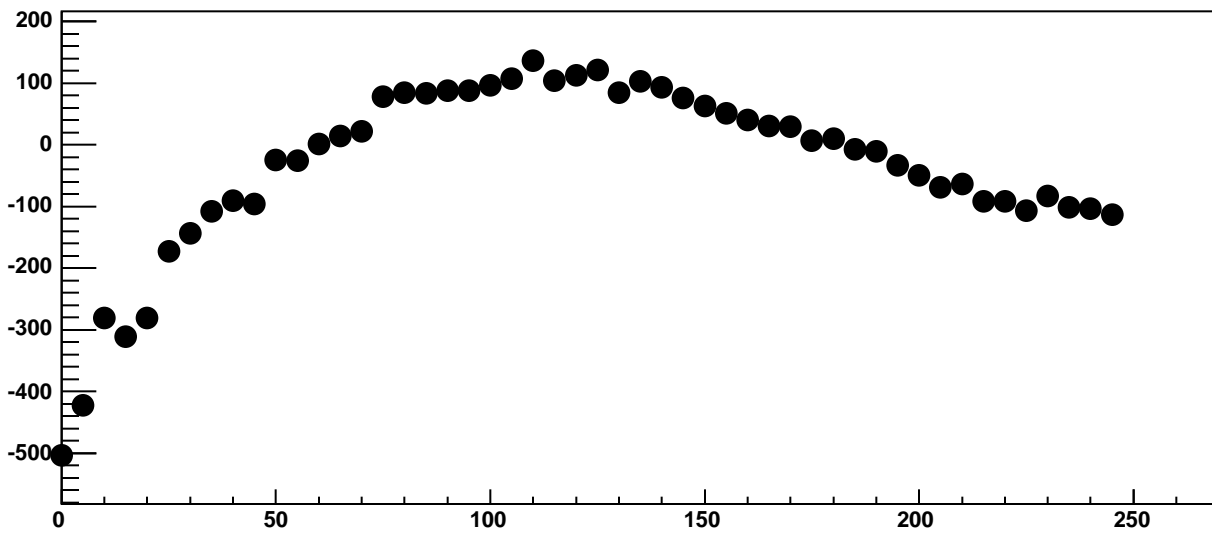


$\chi^2 / \text{ndf}$	3361 / 41
p0	$-598.2 \pm 8.595$
p1	$-6638 \pm 37.28$
p2	$-1621 \pm 11.22$
p3	$-1.837\text{e}+04 \pm 2384$
p4	$0.2021 \pm 0.001269$

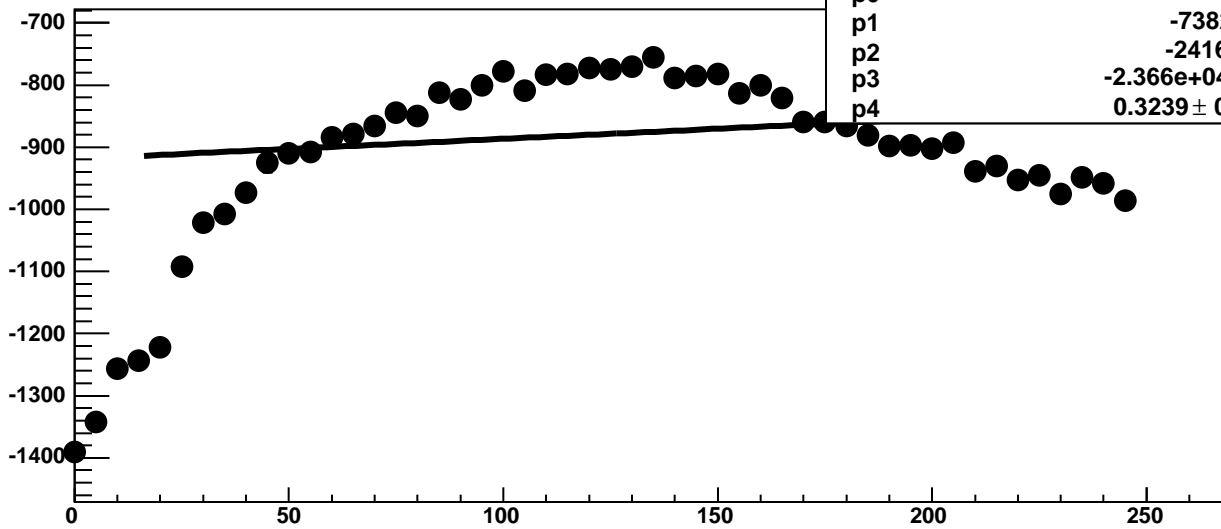
Chip 11, Channel 9, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 9, Enable 1, DAC=1600, ADC Residuals vs Hold

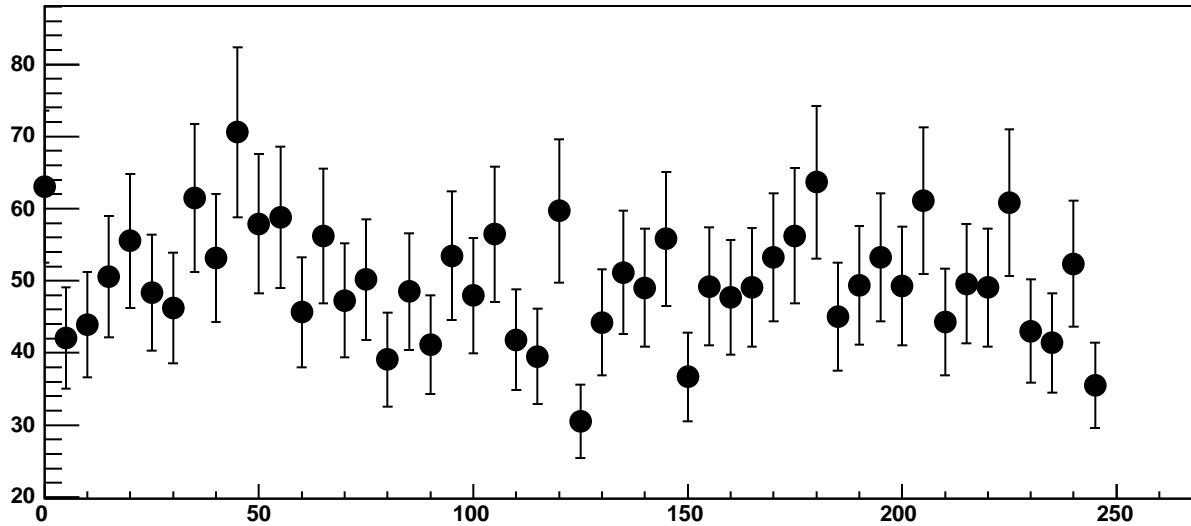


Chip 11, Channel 9, Enable 2, DAC=1600, ADC Mean vs Hold

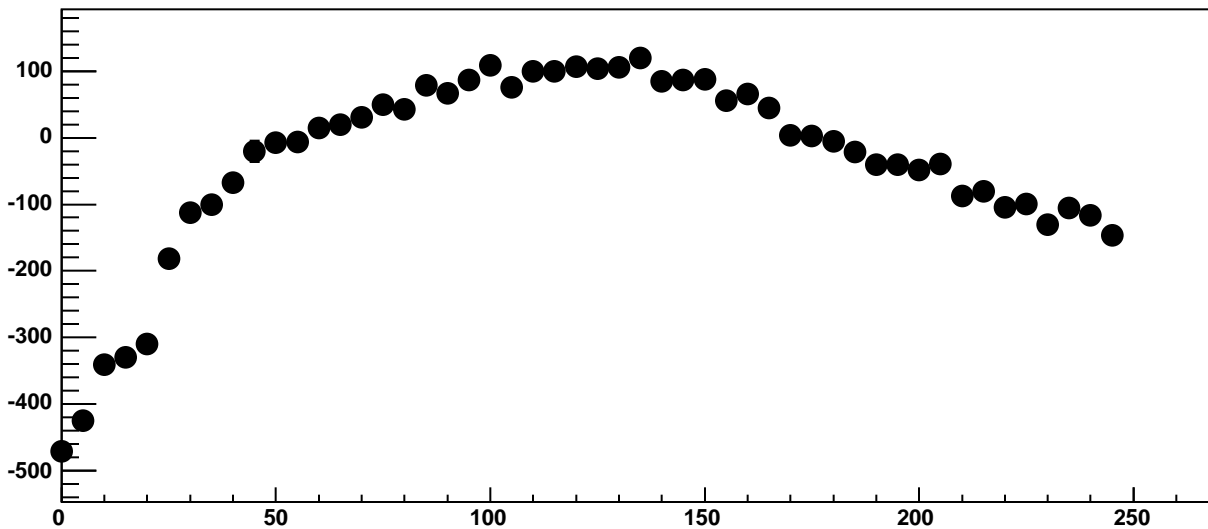


$\chi^2 / \text{ndf}$	3922 / 41
p0	-893.9 ± 8.146
p1	-7382 ± 22.41
p2	-2416 ± 10.65
p3	-2.366e+04 ± 1649
p4	0.3239 ± 0.001084

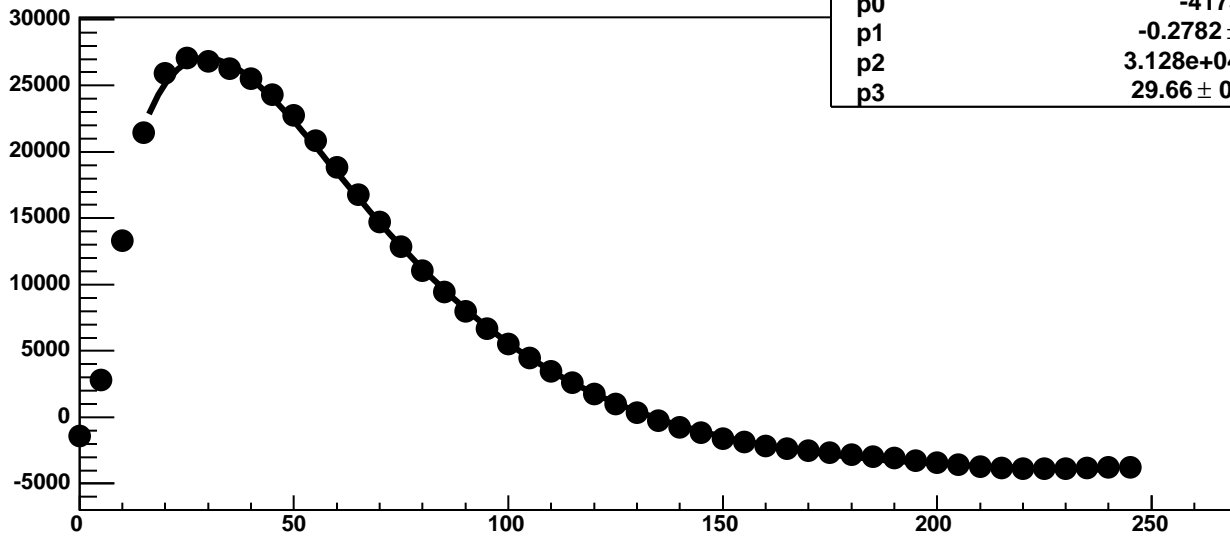
Chip 11, Channel 9, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 9, Enable 2, DAC=1600, ADC Residuals vs Hold

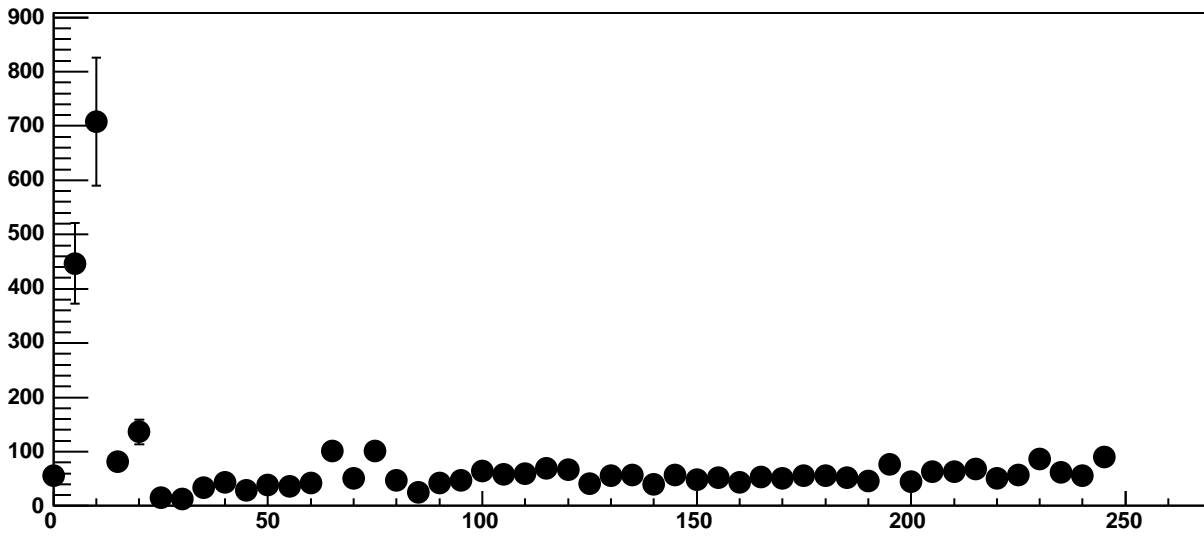


Chip 11, Channel 9, Enable 3!, DAC=1600, ADC Mean vs Hold

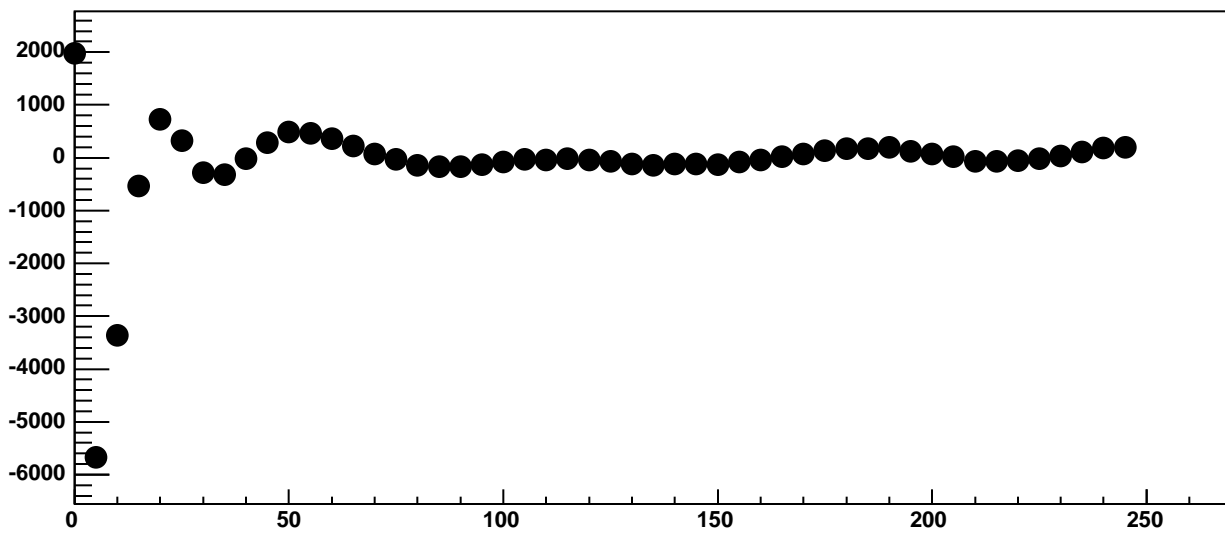


$\chi^2 / \text{ndf}$	3.432e+04 / 42
p0	-4173 ± 3.36
p1	-0.2782 ± 0.0163
p2	3.128e+04 ± 3.69
p3	29.66 ± 0.008665

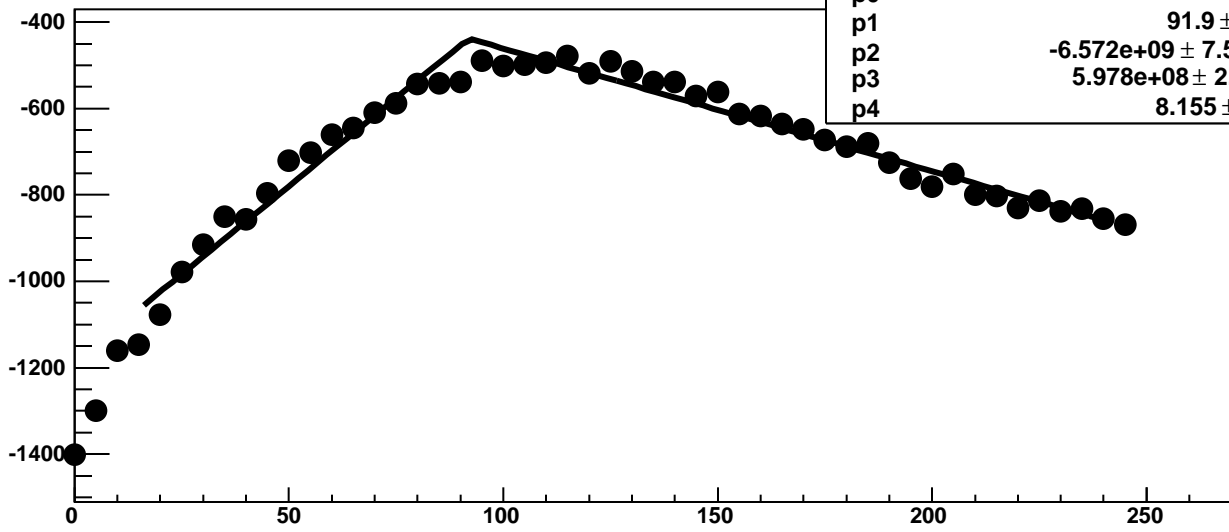
Chip 11, Channel 9, Enable 3!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 9, Enable 3!, DAC=1600, ADC Residuals vs Hold

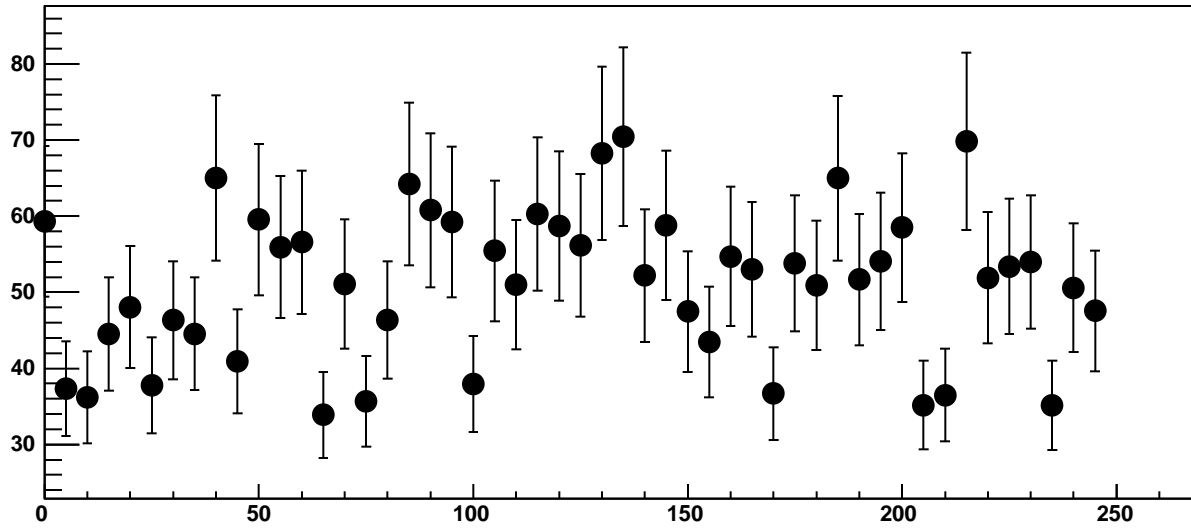


Chip 11, Channel 9, Enable 4, DAC=1600, ADC Mean vs Hold

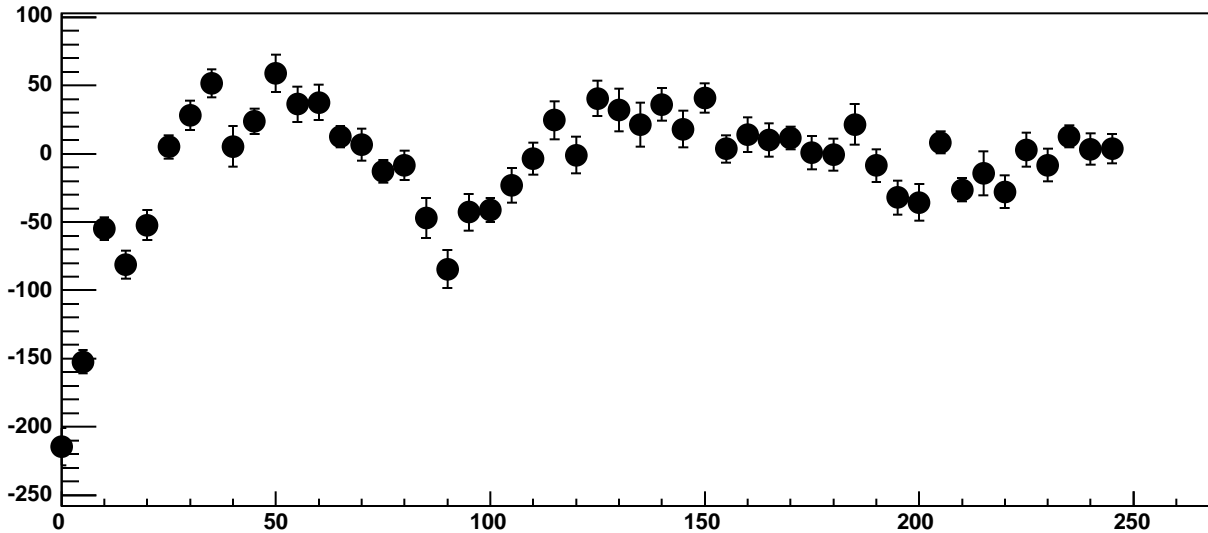


$\chi^2 / \text{ndf}$	333.7 / 41
p0	$-438 \pm 3.527$
p1	$91.9 \pm 0.6434$
p2	$-6.572\text{e}+09 \pm 7.576\text{e}+07$
p3	$5.978\text{e}+08 \pm 2.73\text{e}+05$
p4	$8.155 \pm 0.1182$

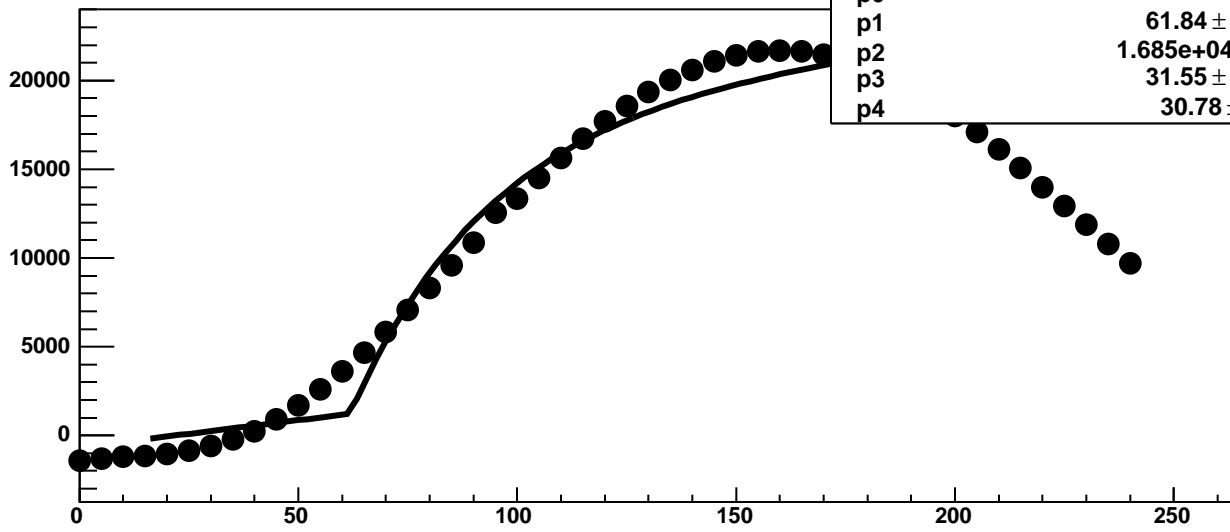
Chip 11, Channel 9, Enable 4, DAC=1600, ADC Noise vs Hold



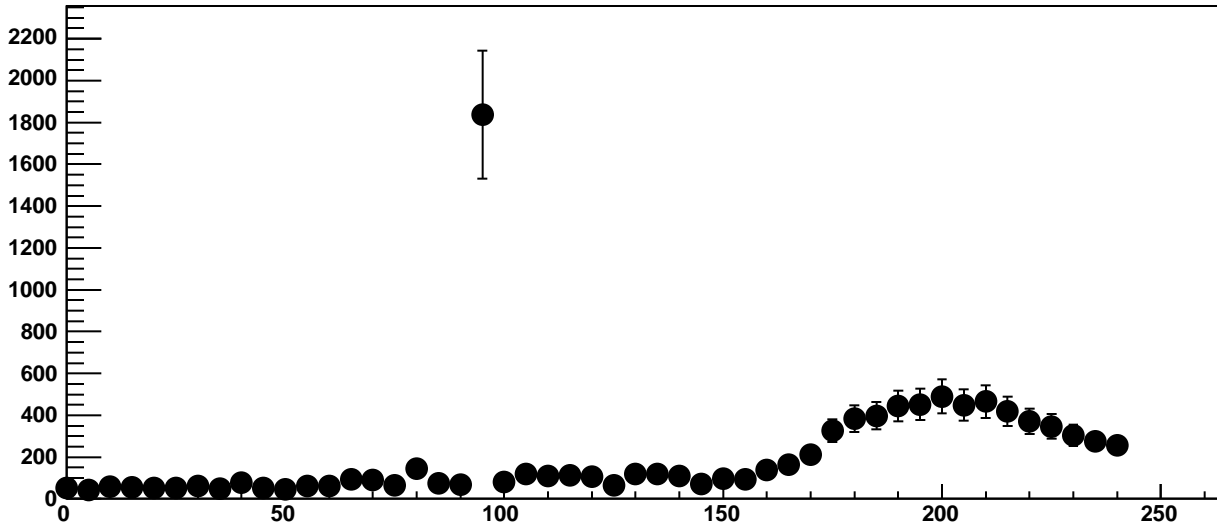
Chip 11, Channel 9, Enable 4, DAC=1600, ADC Residuals vs Hold



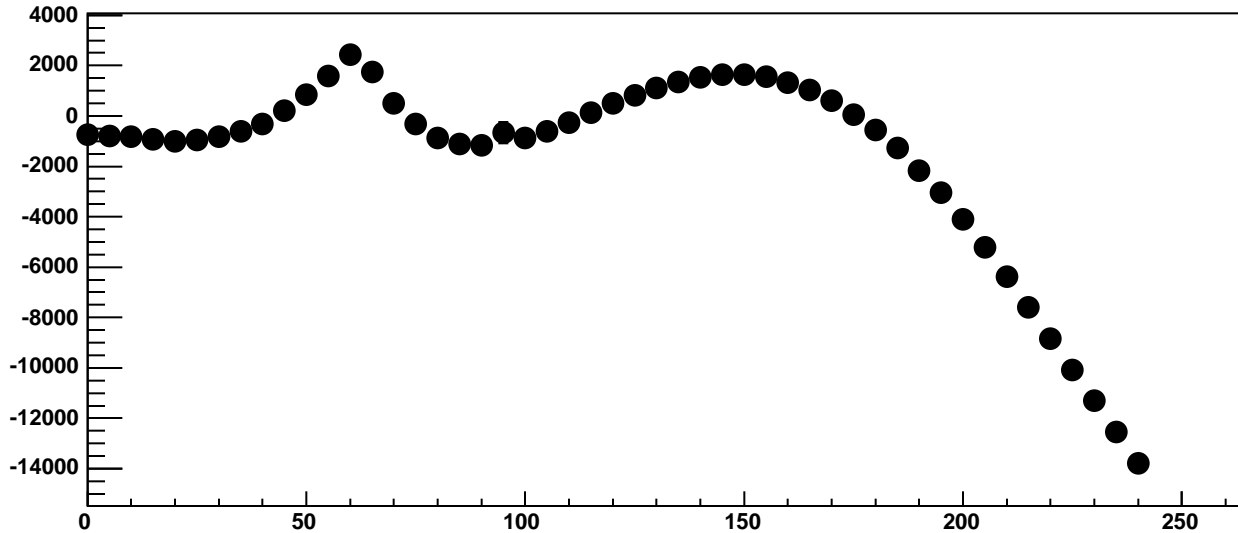
Chip 11, Channel 9, Enable 5, DAC=1600, ADC Mean vs Hold



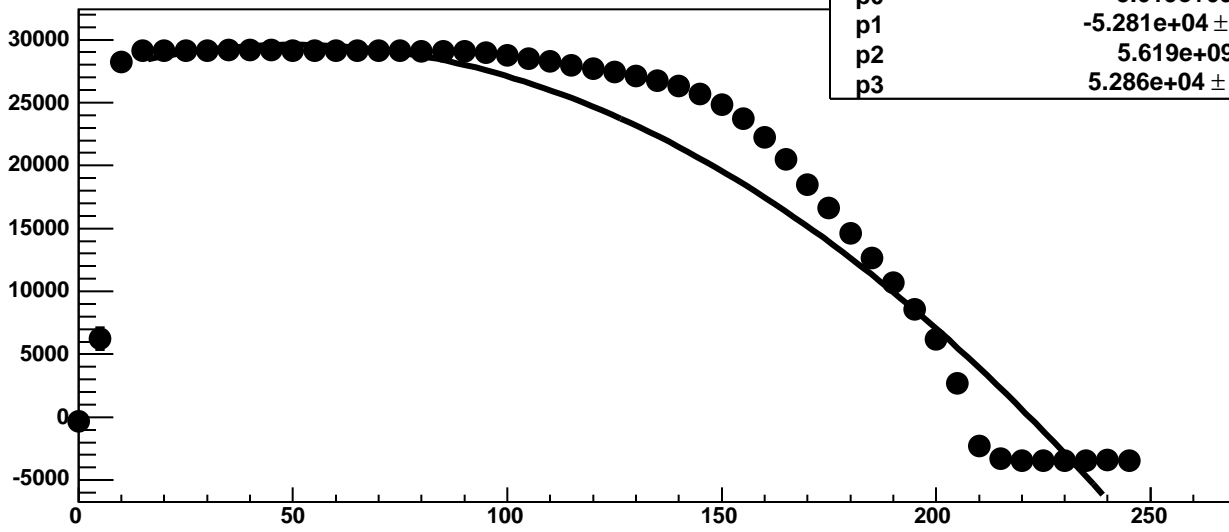
Chip 11, Channel 9, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 9, Enable 5, DAC=1600, ADC Residuals vs Hold

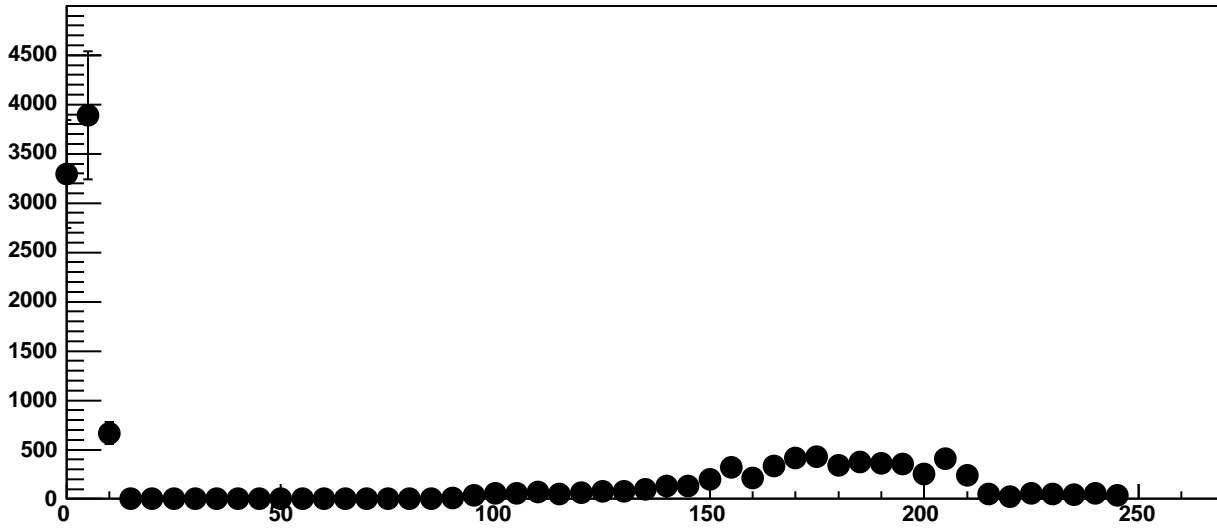


Chip 11, Channel 10, Enable 0!, DAC=1600, ADC Mean vs Hold

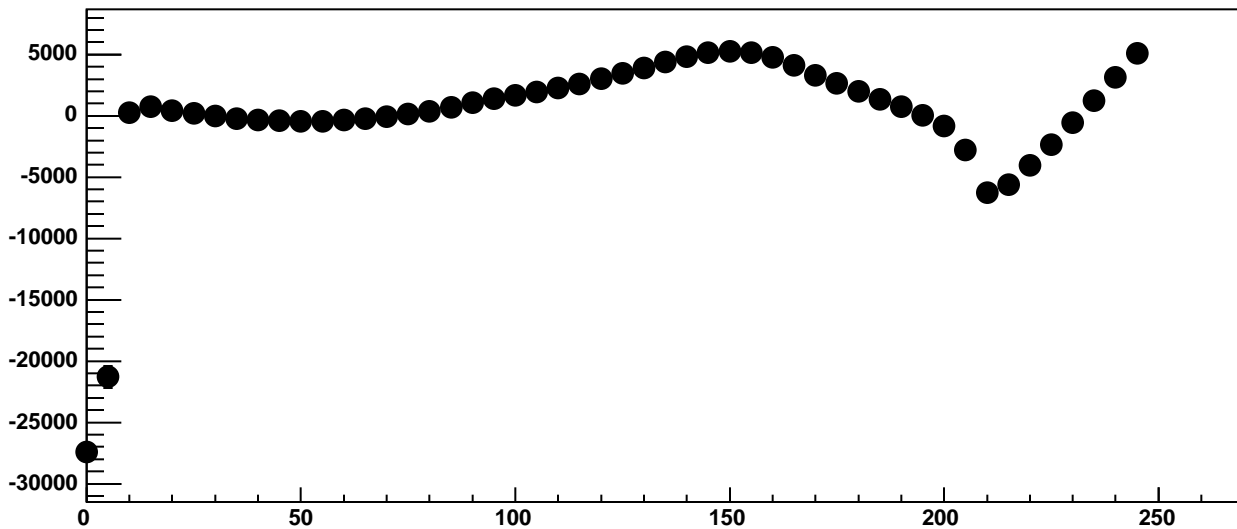


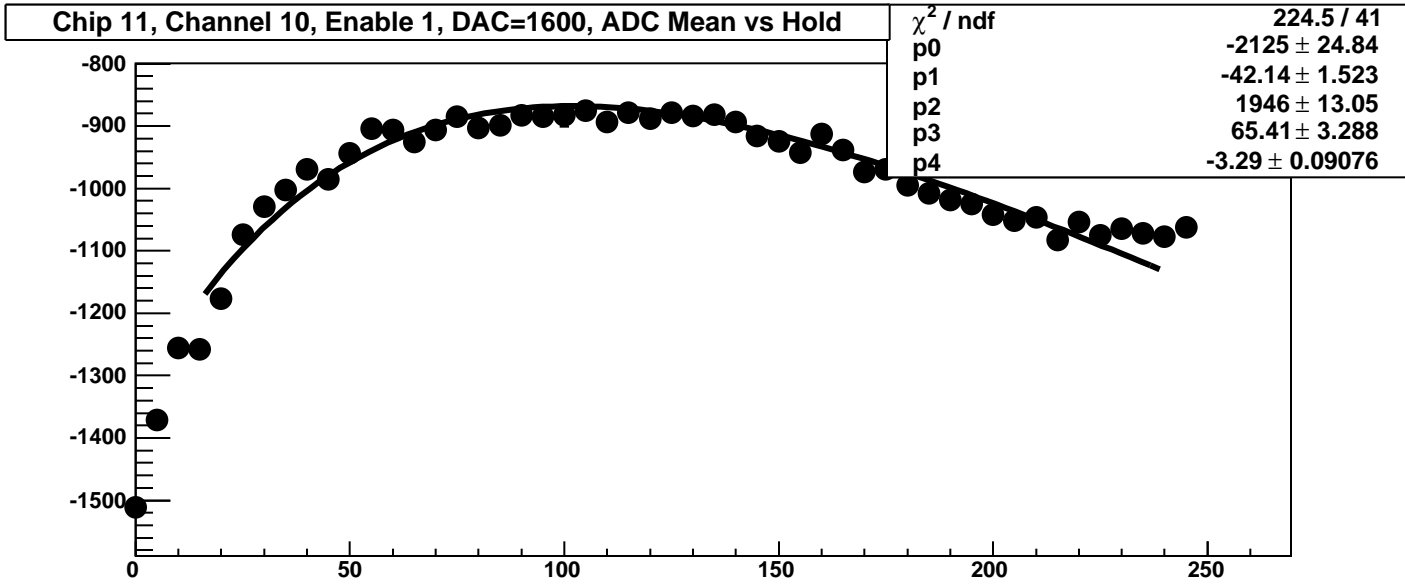
$\chi^2 / \text{ndf}$	4.106e+06 / 42
p0	-5.619e+09 $\pm$ 3.237
p1	-5.281e+04 $\pm$ 0.06091
p2	5.619e+09 $\pm$ 3.237
p3	5.286e+04 $\pm$ 0.06087

Chip 11, Channel 10, Enable 0!, DAC=1600, ADC Noise vs Hold

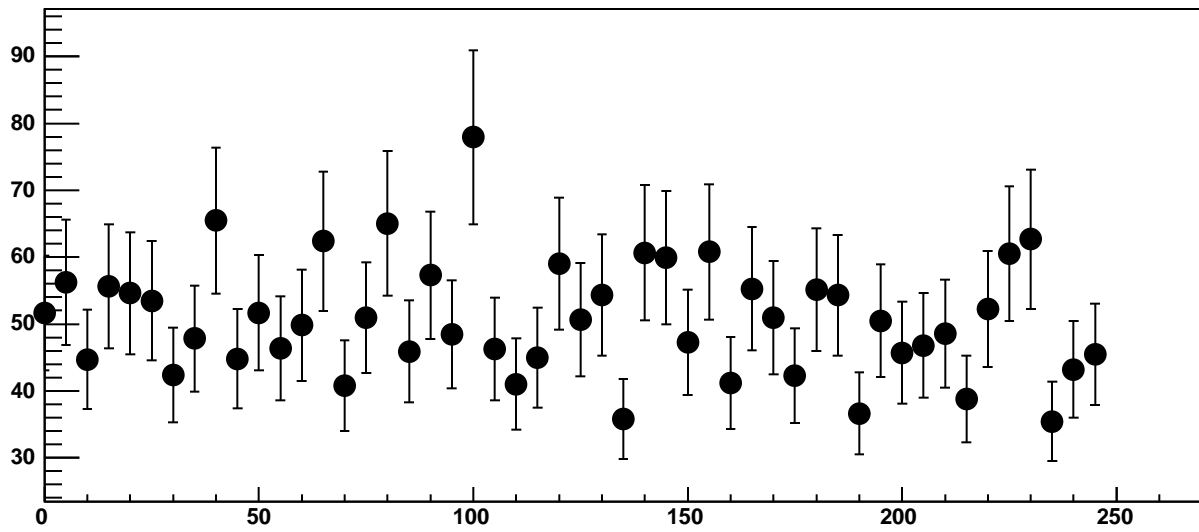


Chip 11, Channel 10, Enable 0!, DAC=1600, ADC Residuals vs Hold

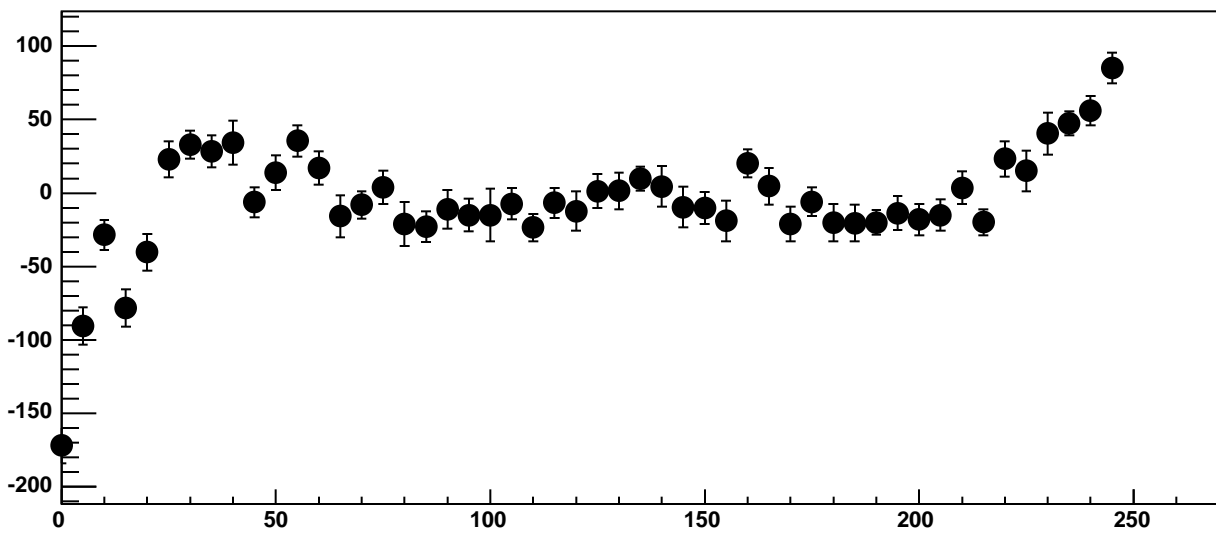




**Chip 11, Channel 10, Enable 1, DAC=1600, ADC Noise vs Hold**

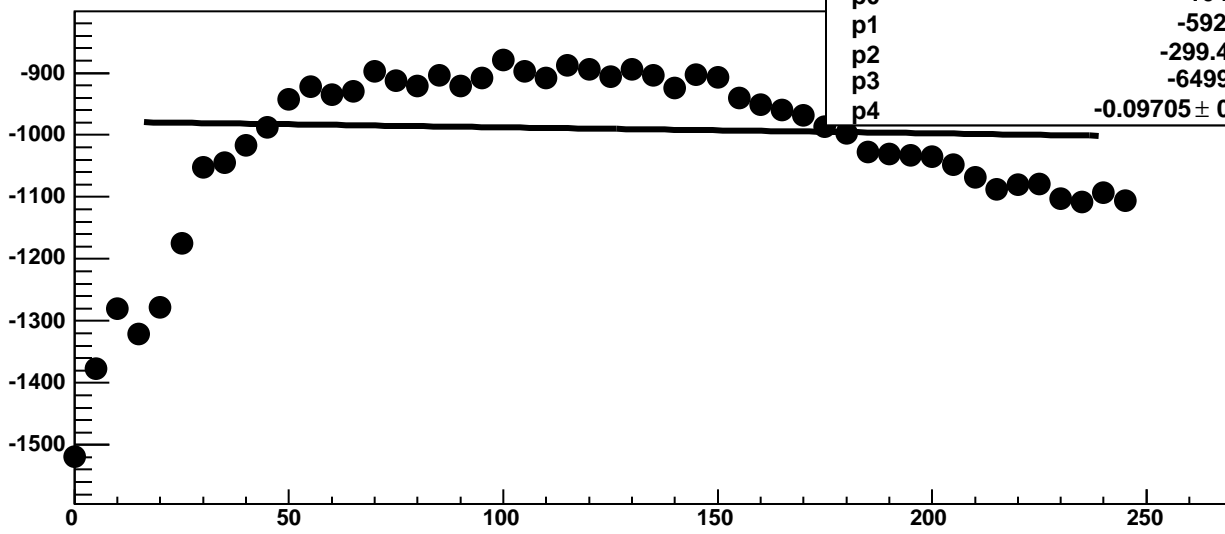


**Chip 11, Channel 10, Enable 1, DAC=1600, ADC Residuals vs Hold**



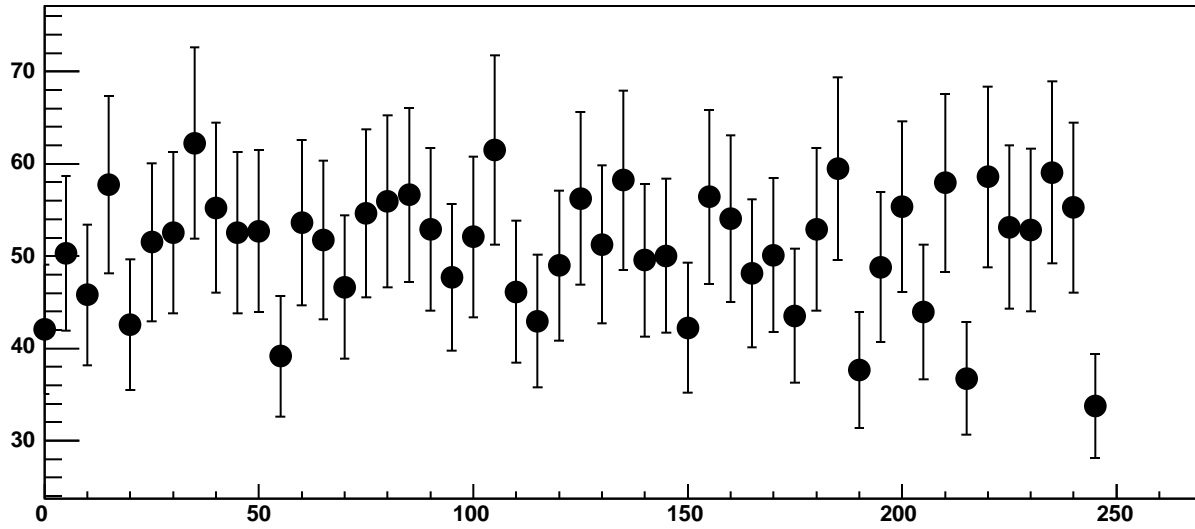


Chip 11, Channel 10, Enable 2, DAC=1600, ADC Mean vs Hold

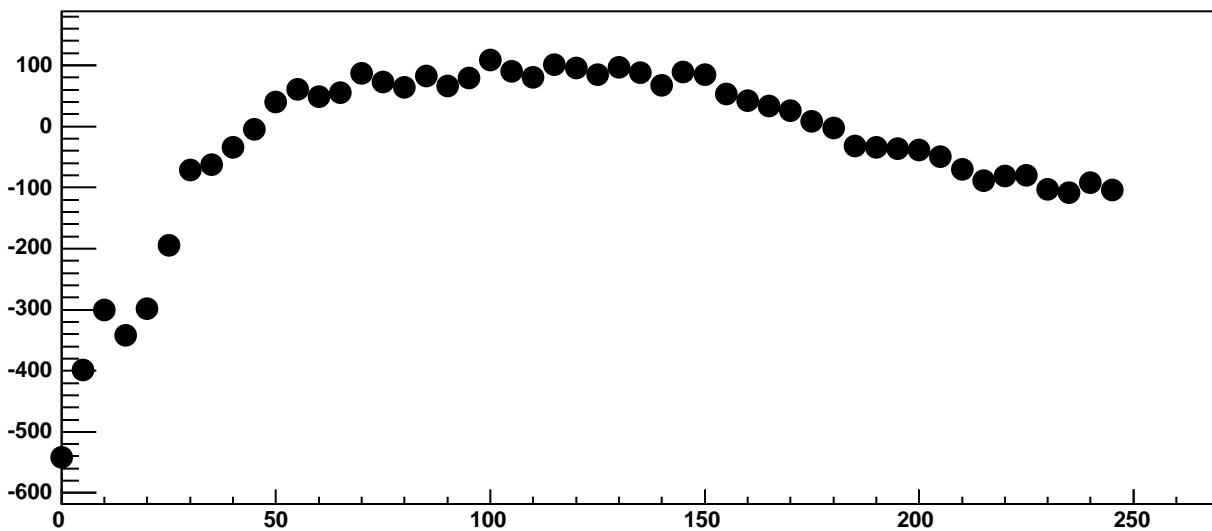


$\chi^2 / \text{ndf}$	3472 / 41
p0	-104 ± 6.816
p1	-5920 ± 112
p2	-299.4 ± 7.108
p3	-6499 ± 2362
p4	-0.09705 ± 0.001127

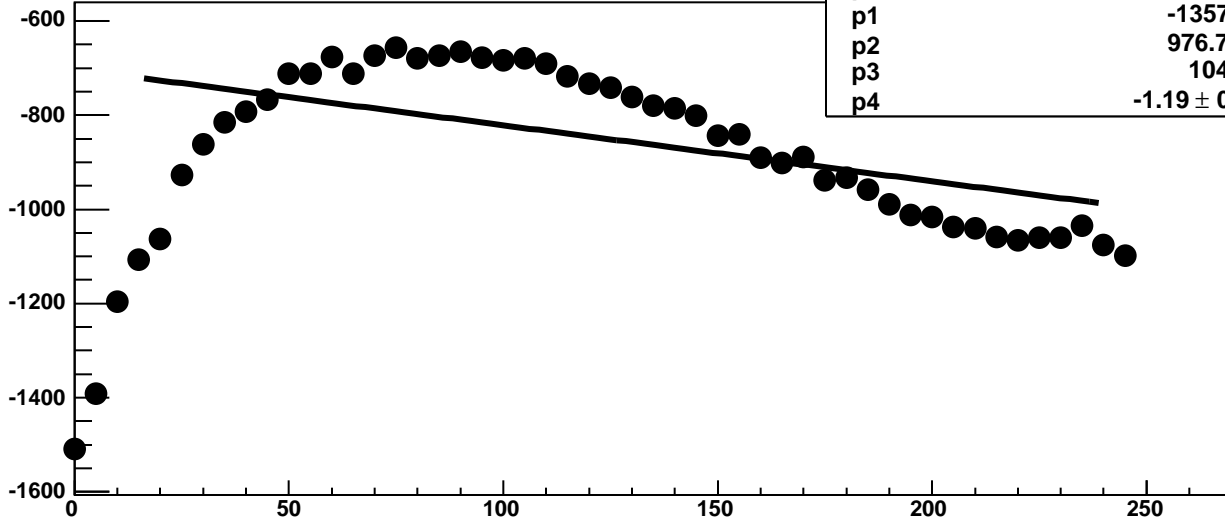
Chip 11, Channel 10, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 10, Enable 2, DAC=1600, ADC Residuals vs Hold

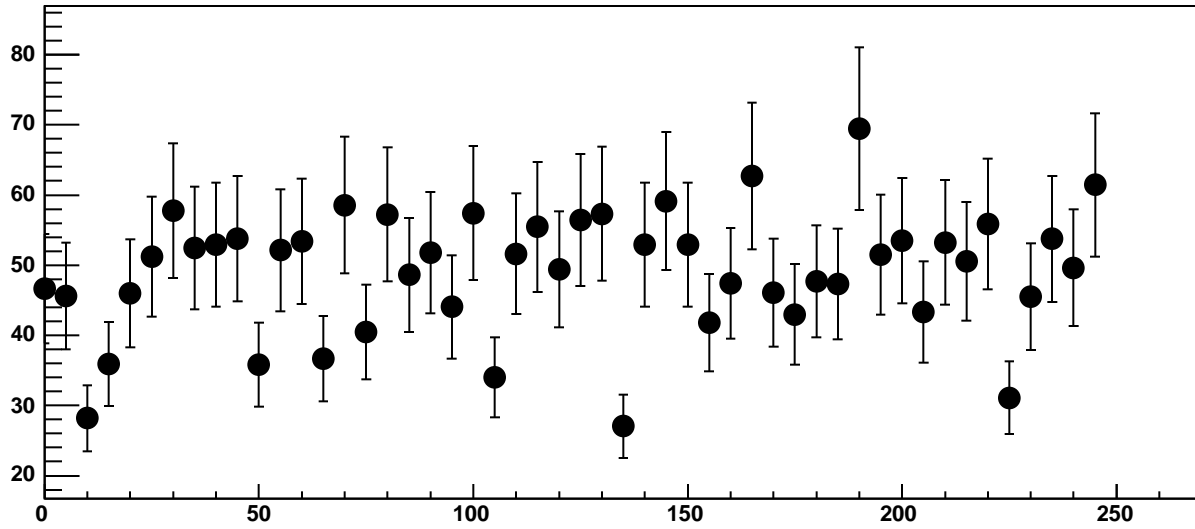


Chip 11, Channel 10, Enable 3, DAC=1600, ADC Mean vs Hold

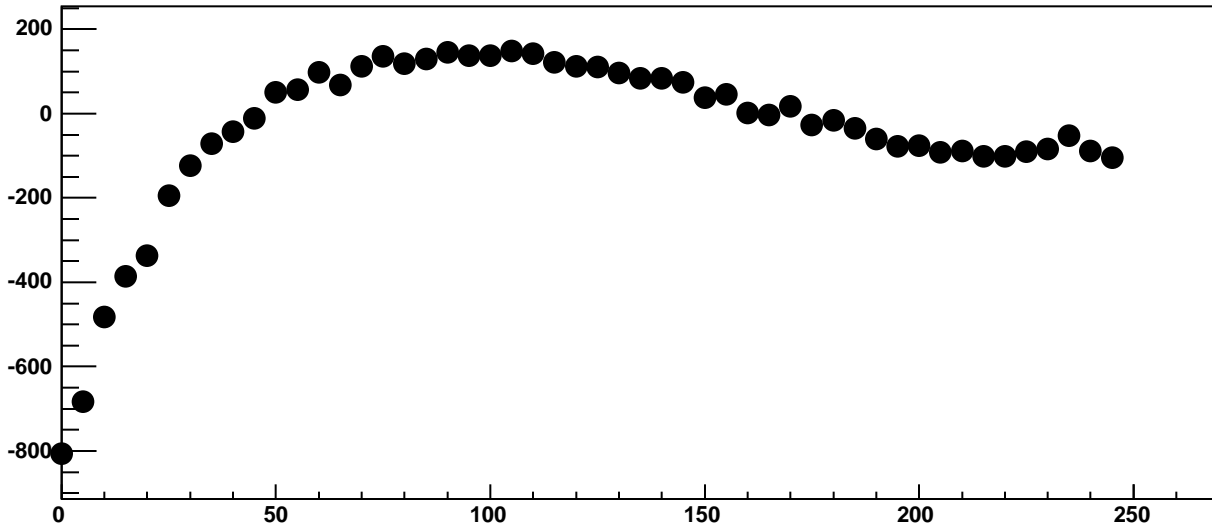


$\chi^2 / \text{ndf}$	6559 / 41
p0	$-64.07 \pm 1.413$
p1	$-1357 \pm 1.412$
p2	$976.7 \pm 1.413$
p3	$104 \pm 1.414$
p4	$-1.19 \pm 0.002052$

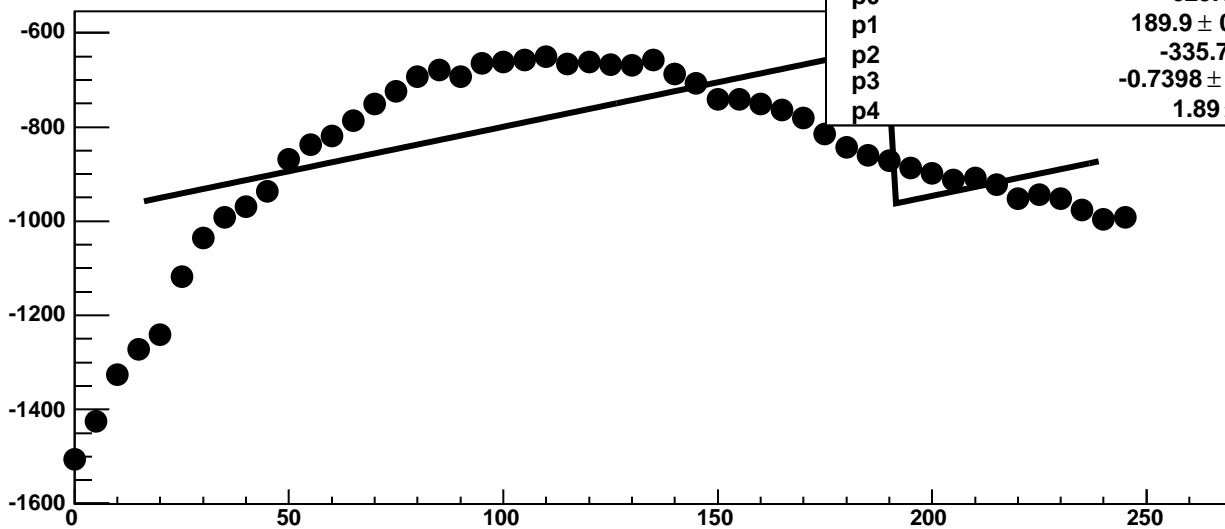
Chip 11, Channel 10, Enable 3, DAC=1600, ADC Noise vs Hold



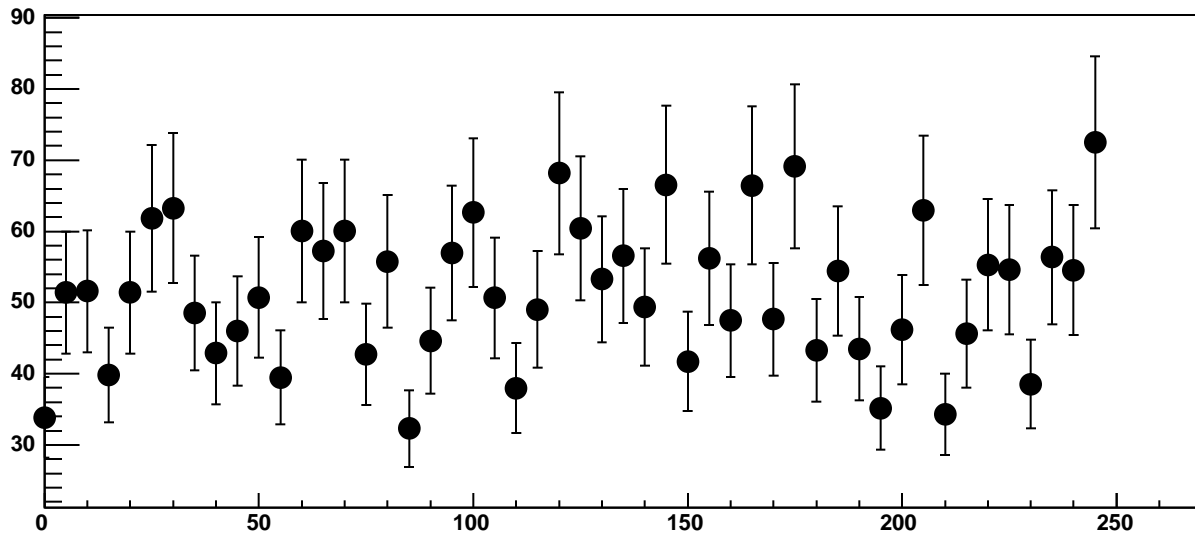
Chip 11, Channel 10, Enable 3, DAC=1600, ADC Residuals vs Hold



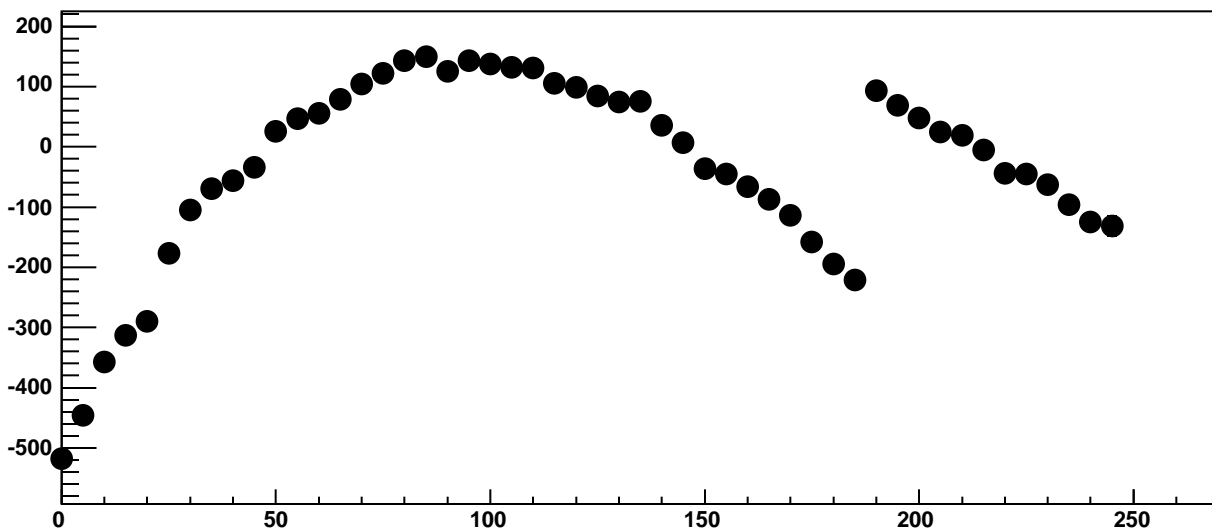
Chip 11, Channel 10, Enable 4, DAC=1600, ADC Mean vs Hold



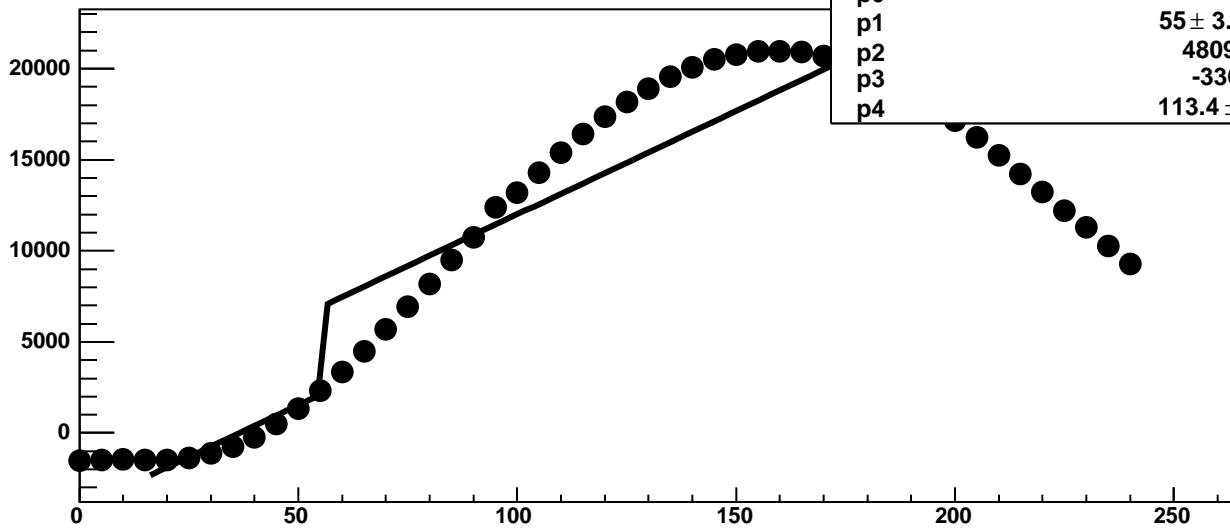
Chip 11, Channel 10, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 10, Enable 4, DAC=1600, ADC Residuals vs Hold

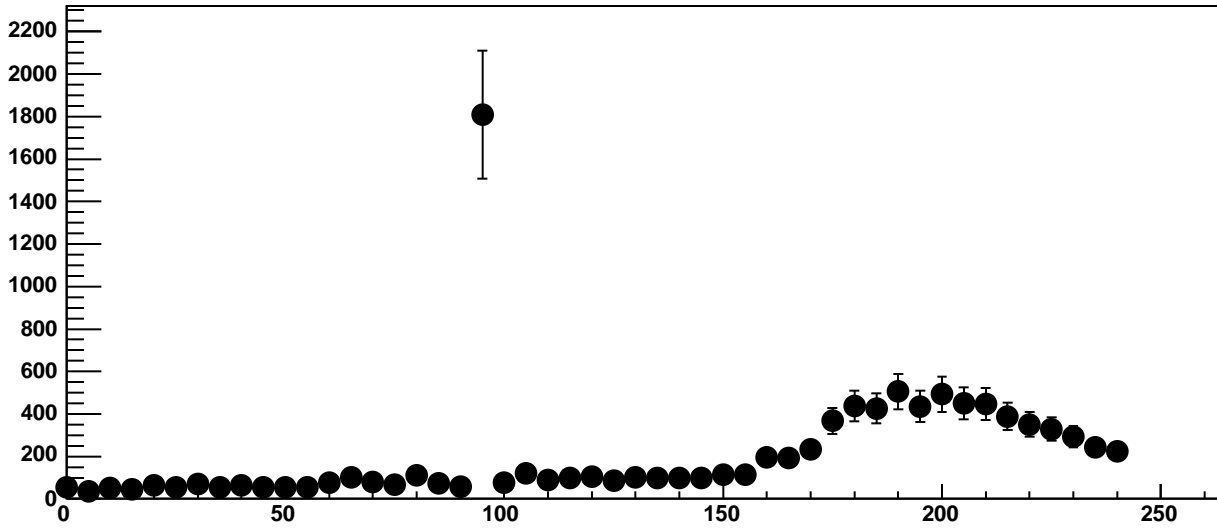


Chip 11, Channel 10, Enable 5, DAC=1600, ADC Mean vs Hold

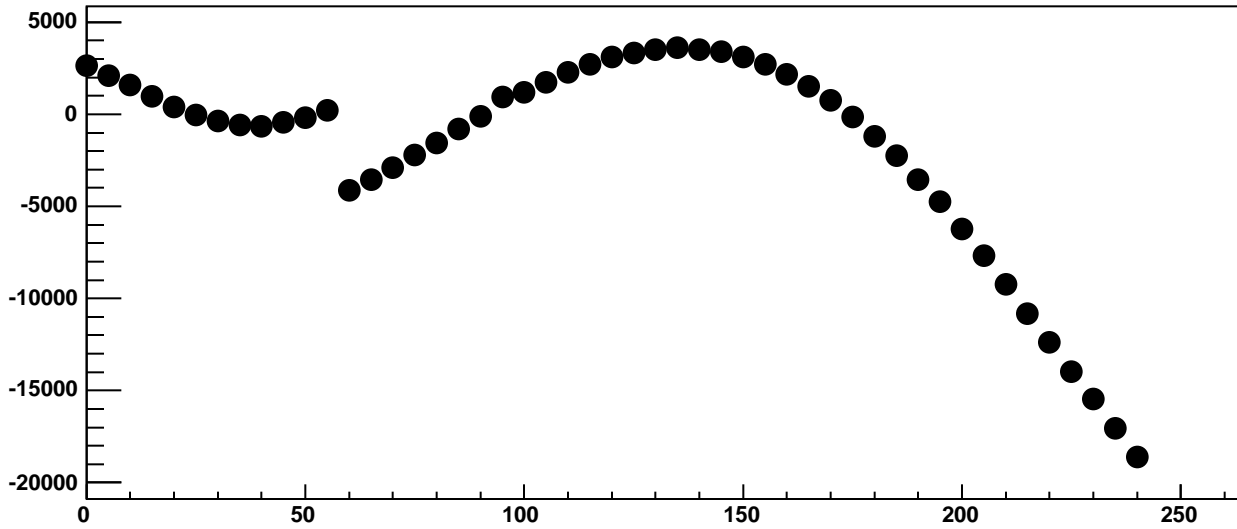


$\chi^2 / \text{ndf}$	7.217e+05 / 41
p0	2092 ± 26.09
p1	55 ± 3.339e-05
p2	4809 ± 33.71
p3	-336 ± 15.6
p4	113.4 ± 0.5976

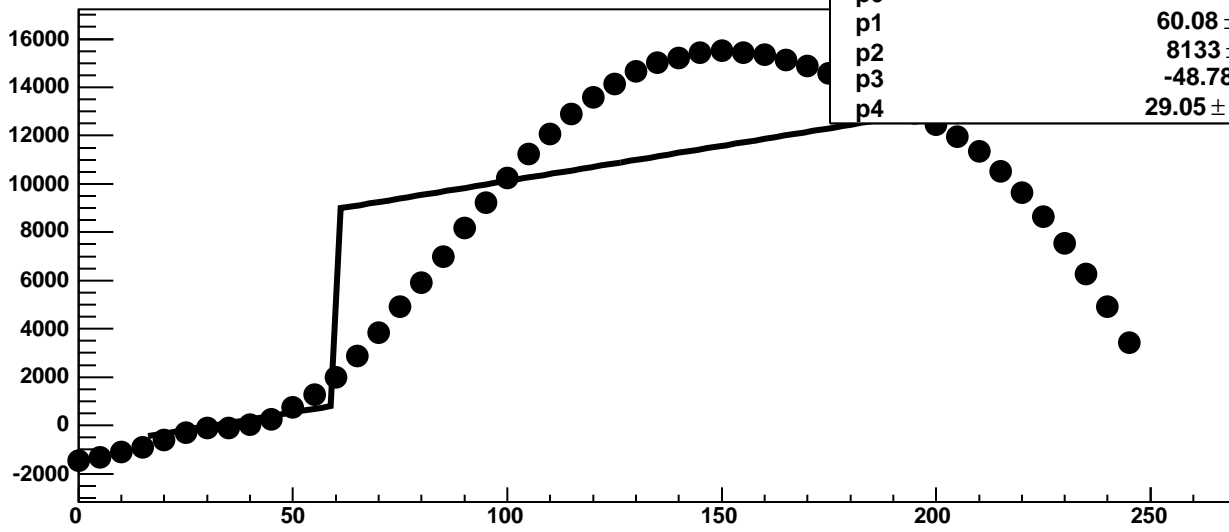
Chip 11, Channel 10, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 10, Enable 5, DAC=1600, ADC Residuals vs Hold



Chip 11, Channel 11, Enable 0, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

7.611e+05 / 41

p0

$829.3 \pm 0.1129$

p1

$60.08 \pm 0.9166$

p2

$8133 \pm 0.1139$

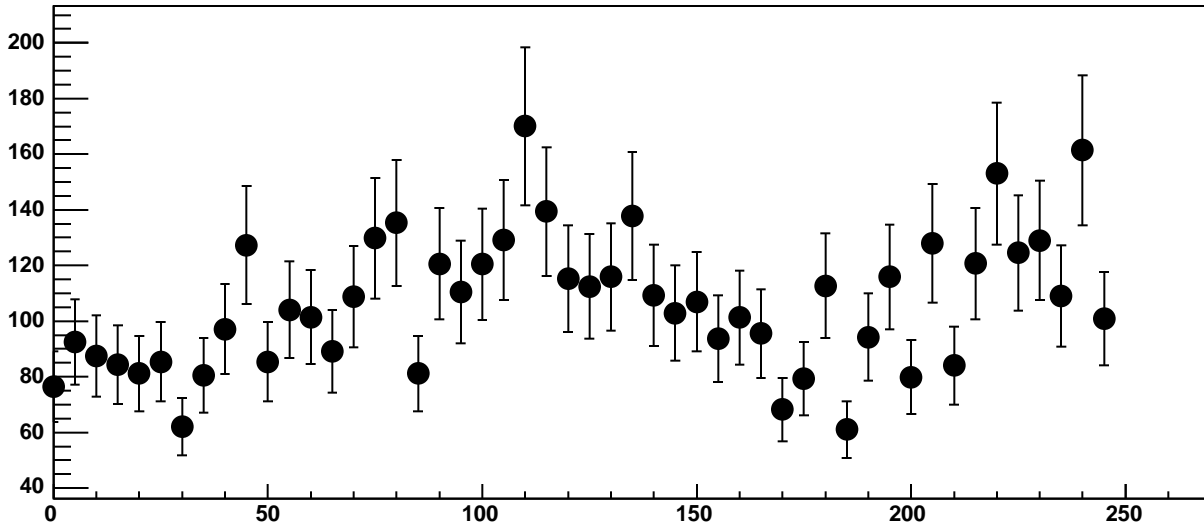
p3

$-48.78 \pm 12.83$

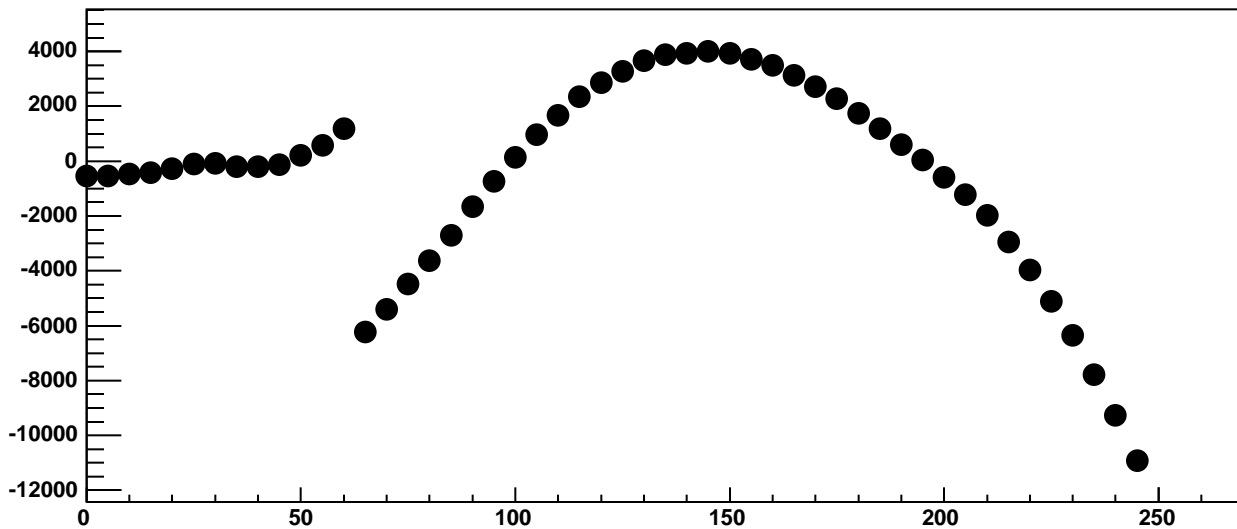
p4

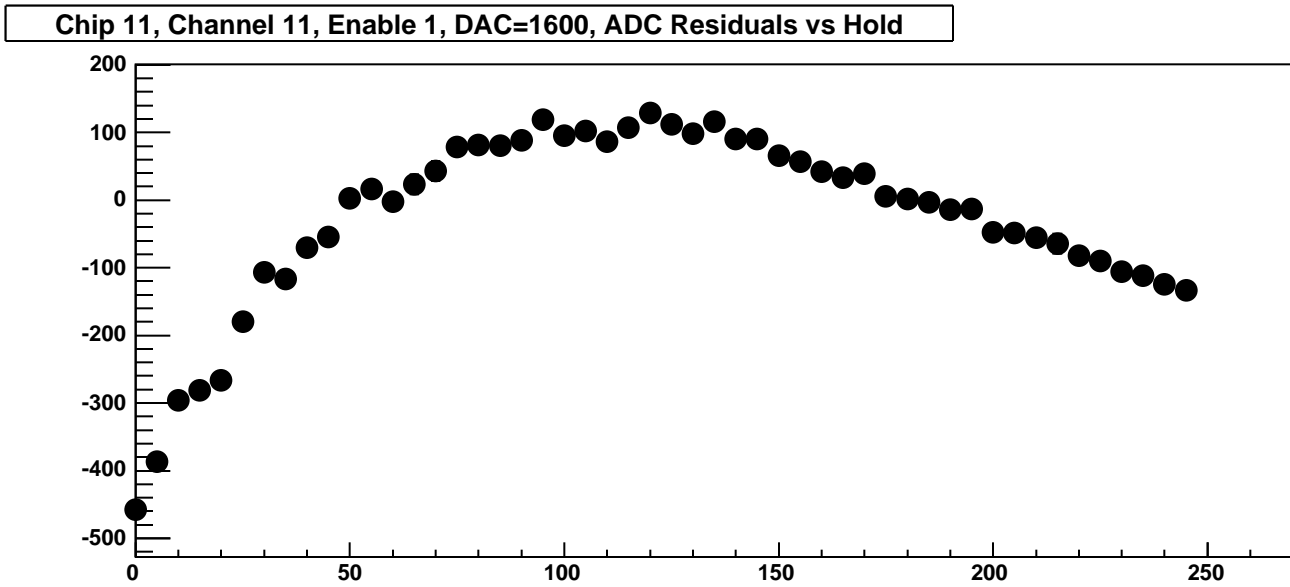
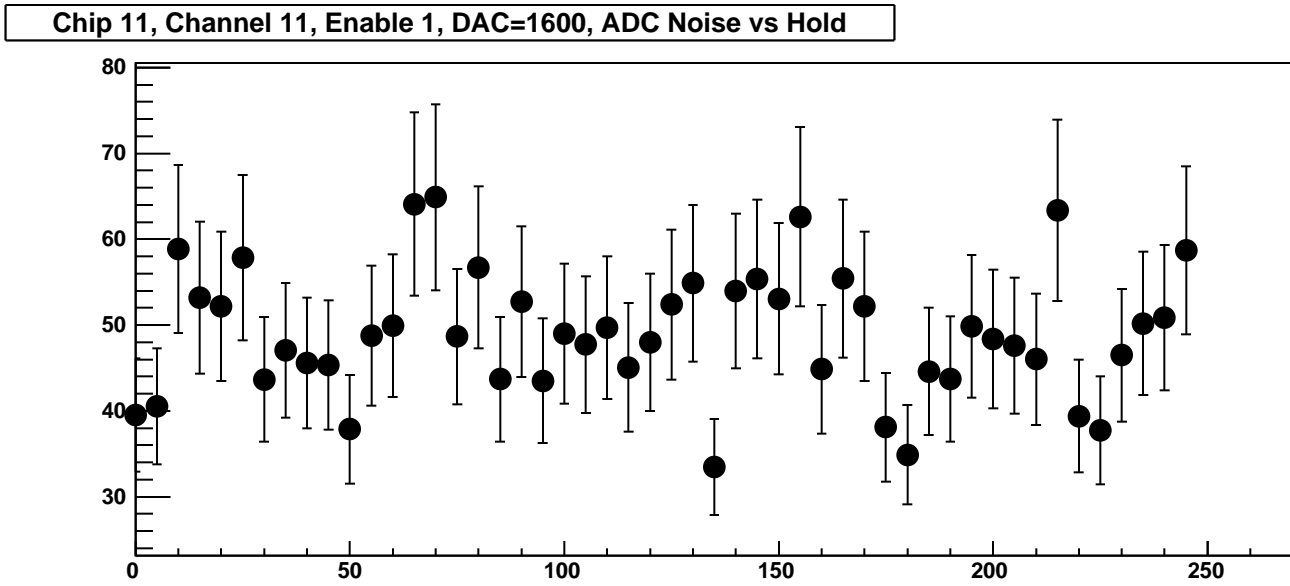
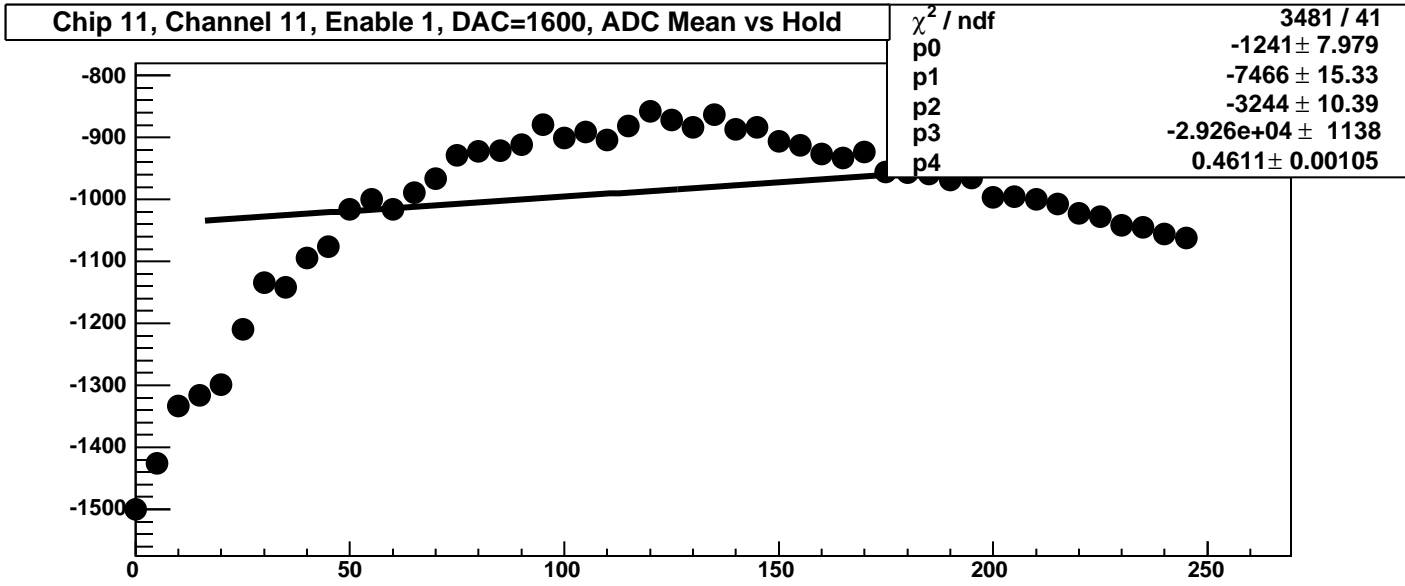
$29.05 \pm 0.05885$

Chip 11, Channel 11, Enable 0, DAC=1600, ADC Noise vs Hold

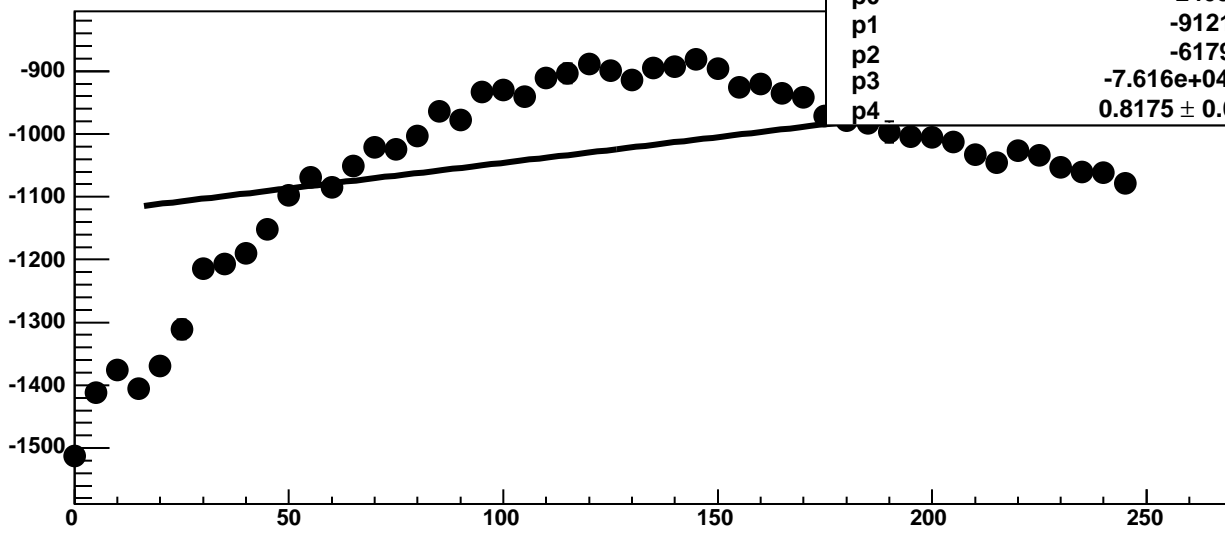


Chip 11, Channel 11, Enable 0, DAC=1600, ADC Residuals vs Hold



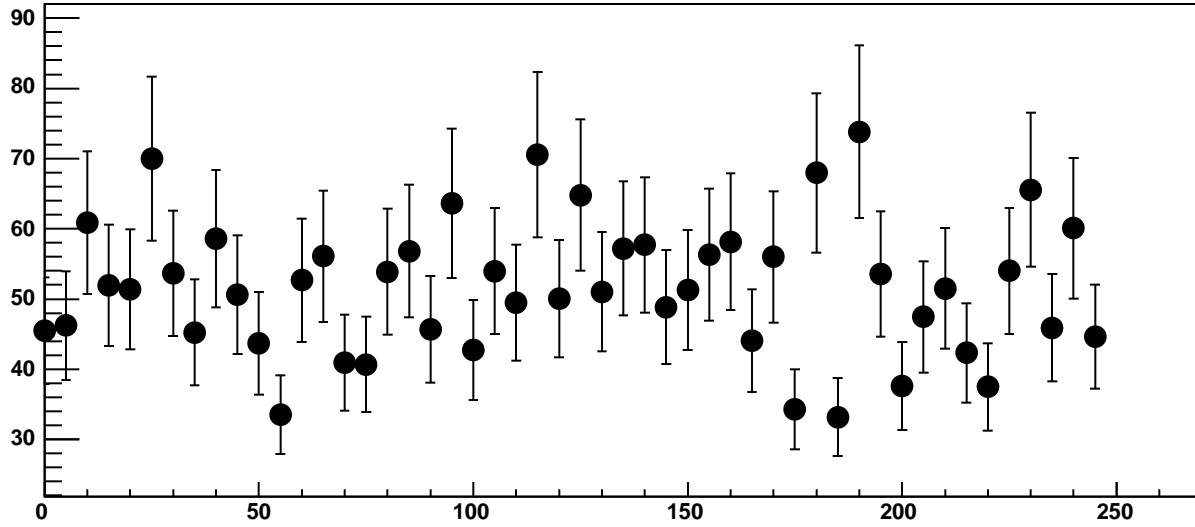


Chip 11, Channel 11, Enable 2, DAC=1600, ADC Mean vs Hold

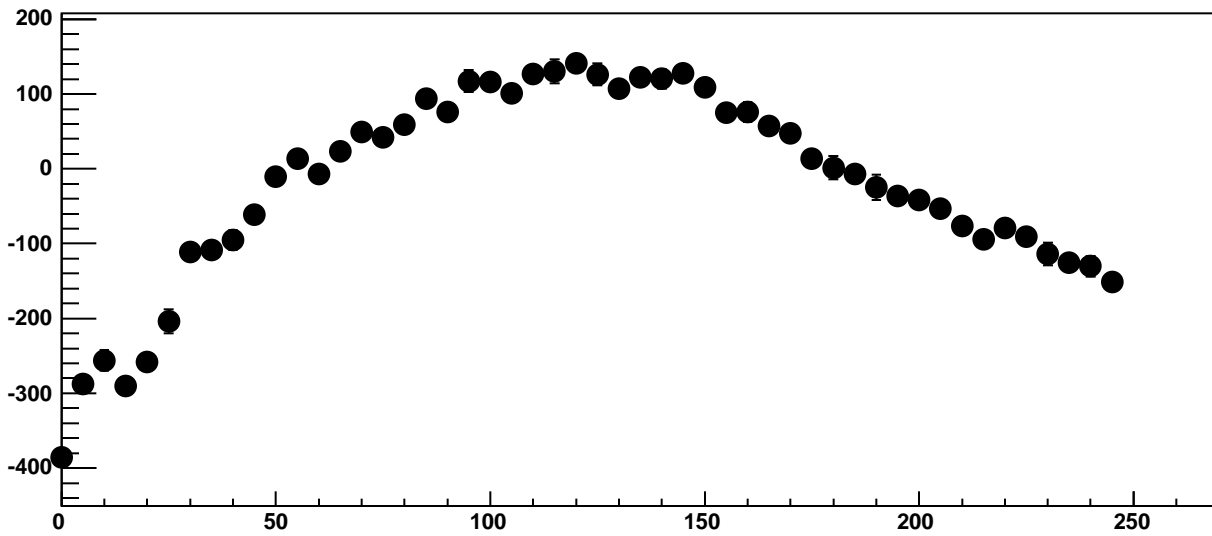


$\chi^2 / \text{ndf}$	3576 / 41
p0	-2405 ± 8.471
p1	-9121 ± 8.522
p2	-6179 ± 10.61
p3	-7.616e+04 ± 655.8
p4	0.8175 ± 0.0009157

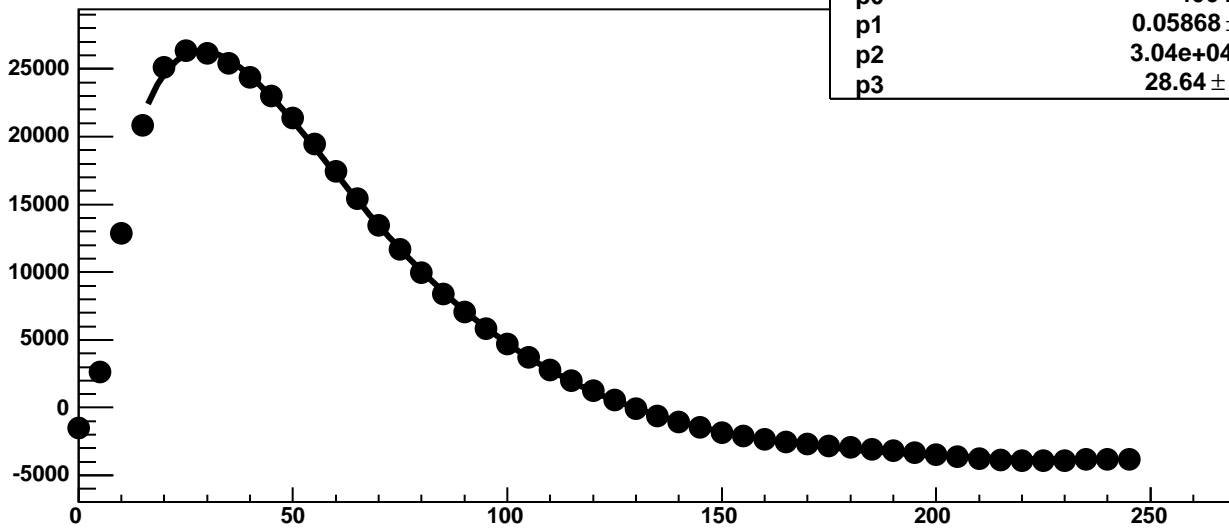
Chip 11, Channel 11, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 11, Enable 2, DAC=1600, ADC Residuals vs Hold

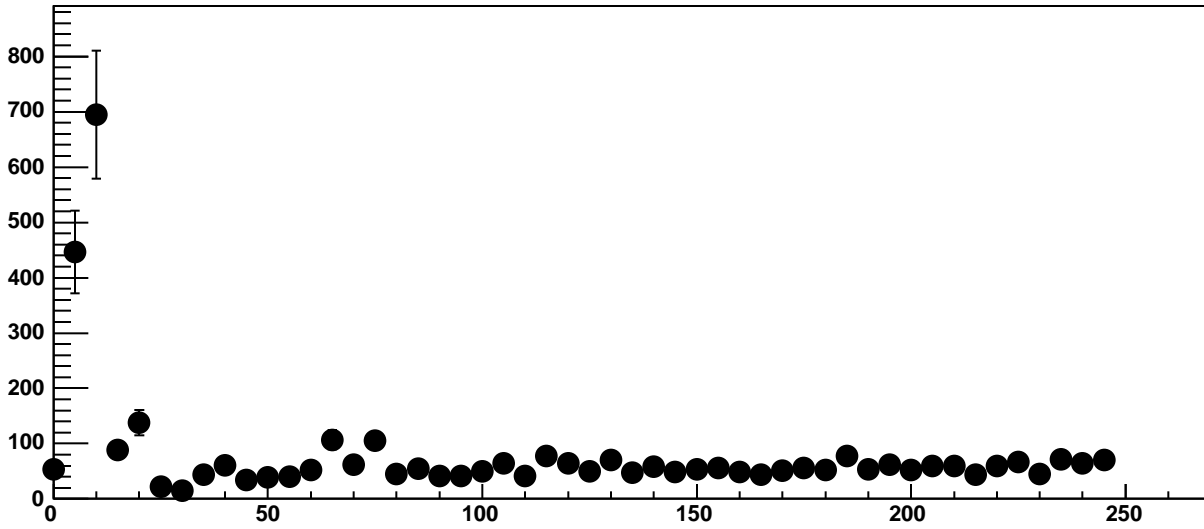


Chip 11, Channel 11, Enable 3!, DAC=1600, ADC Mean vs Hold

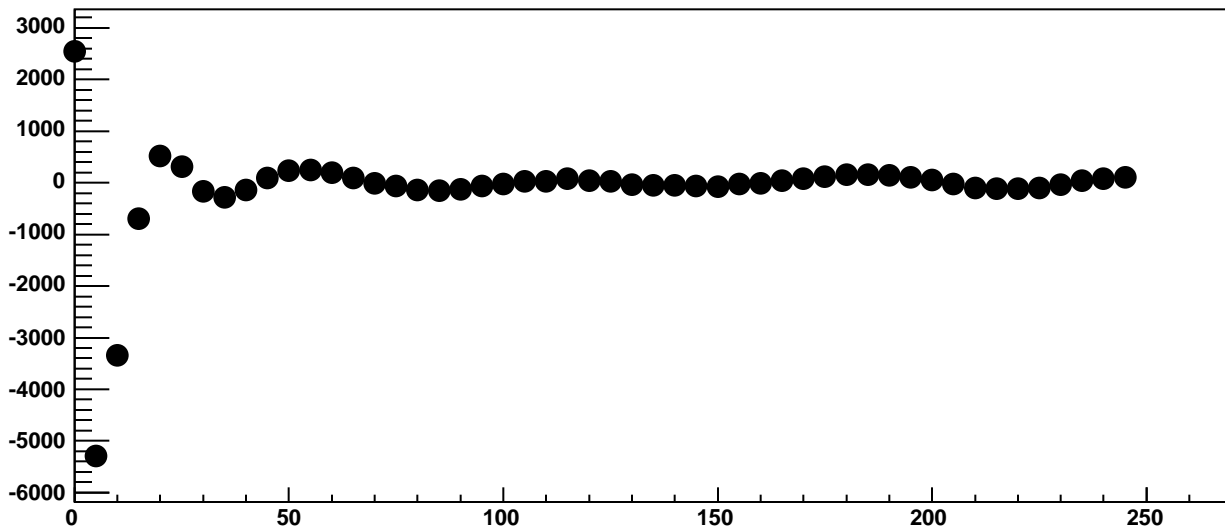


$\chi^2 / \text{ndf}$	1.187e+04 / 42
p0	-4064 ± 3.552
p1	0.05868 ± 0.0203
p2	3.04e+04 ± 4.143
p3	28.64 ± 0.01068

Chip 11, Channel 11, Enable 3!, DAC=1600, ADC Noise vs Hold

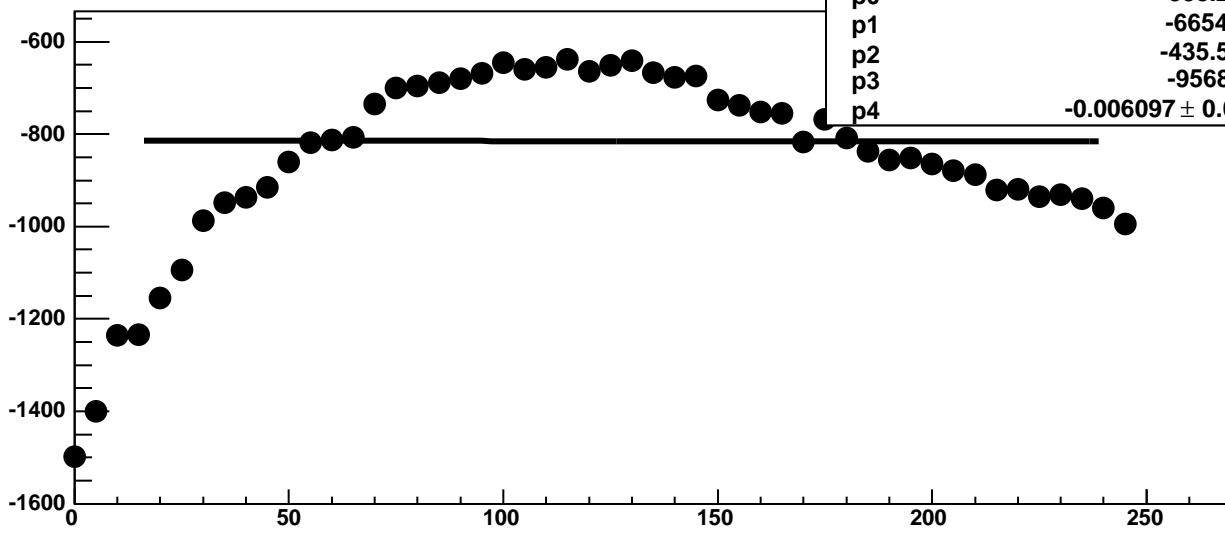


Chip 11, Channel 11, Enable 3!, DAC=1600, ADC Residuals vs Hold





Chip 11, Channel 11, Enable 4, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

7008 / 41

p0  $-338.2 \pm 1.219$

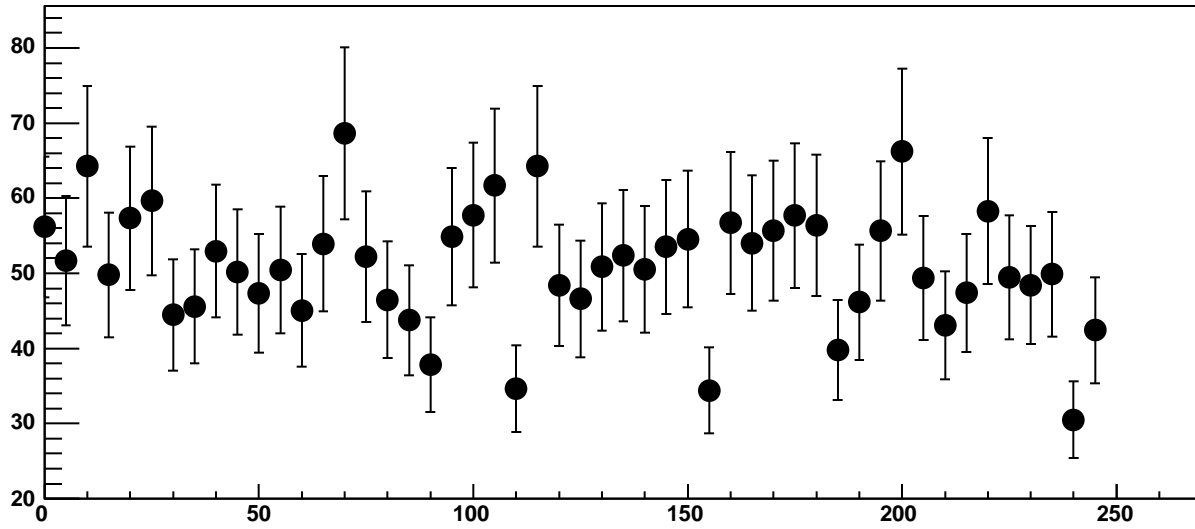
p1  $-6654 \pm 2078$

p2  $-435.5 \pm 1.477$

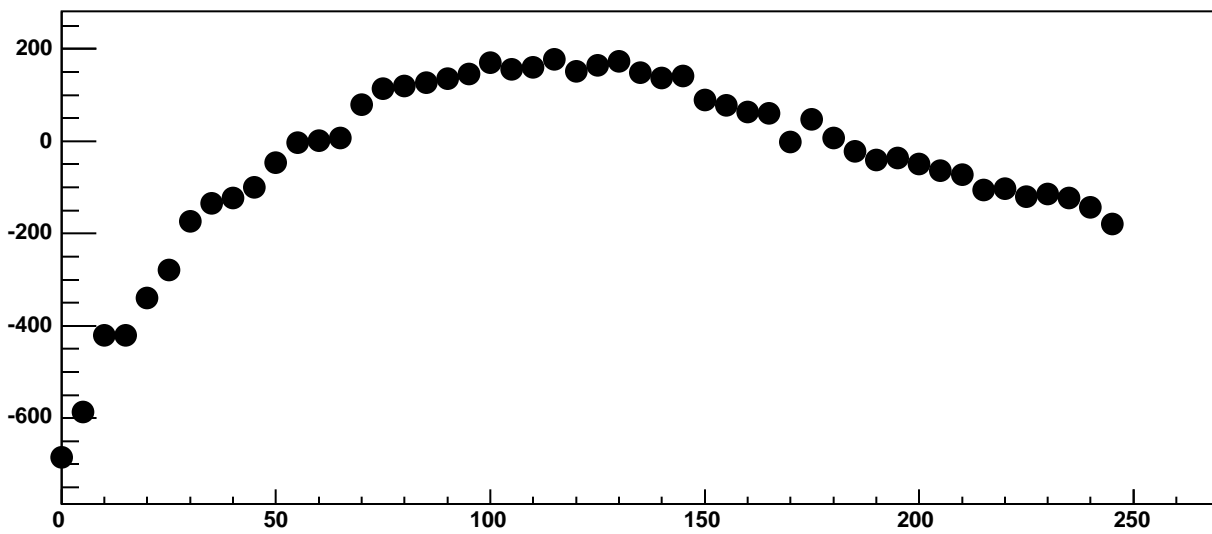
p3  $-9568 \pm 1606$

p4  $-0.006097 \pm 0.0001806$

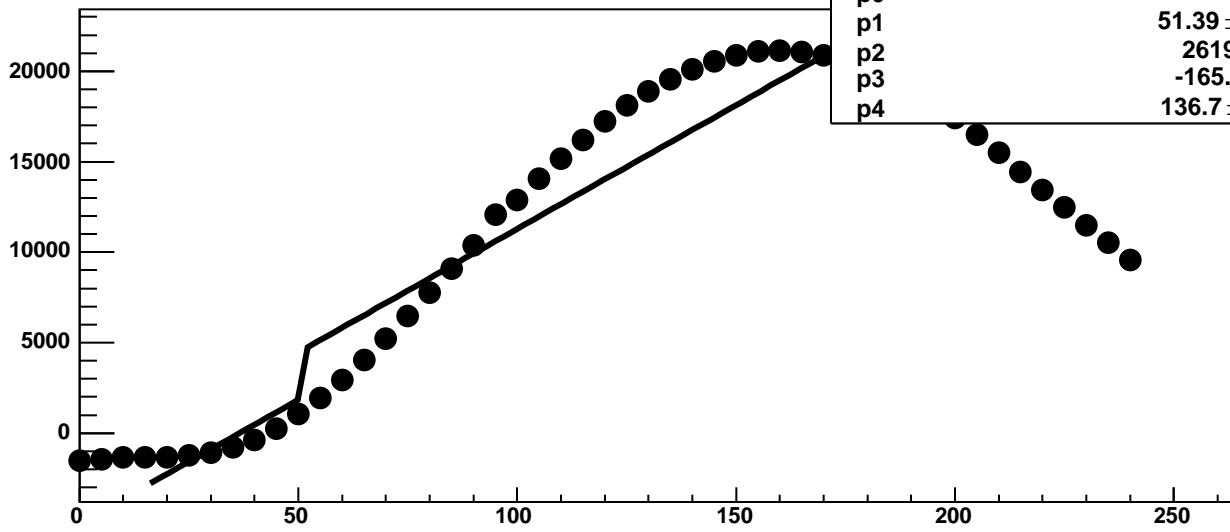
Chip 11, Channel 11, Enable 4, DAC=1600, ADC Noise vs Hold



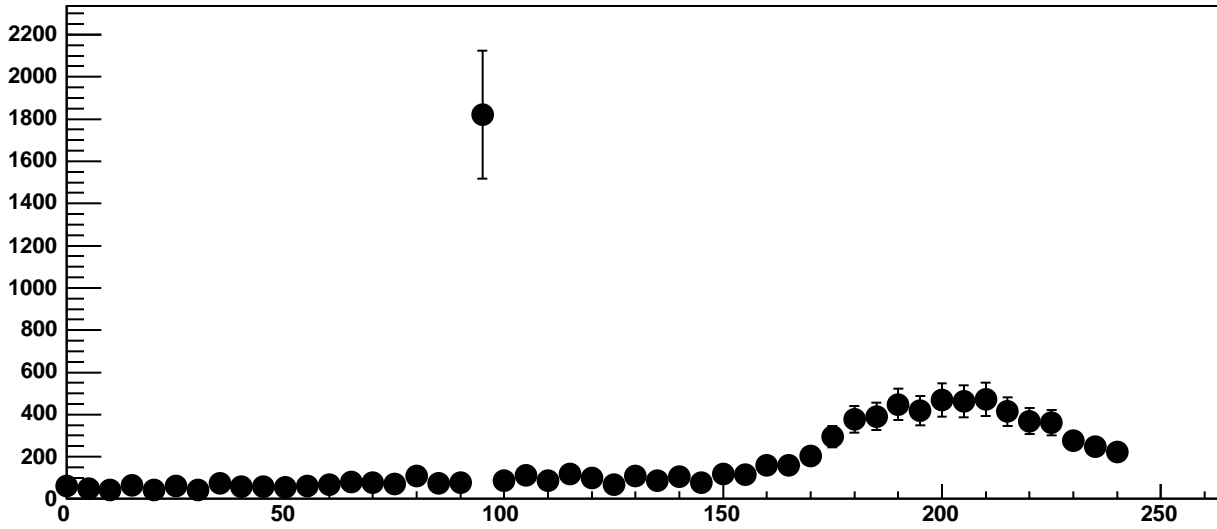
Chip 11, Channel 11, Enable 4, DAC=1600, ADC Residuals vs Hold



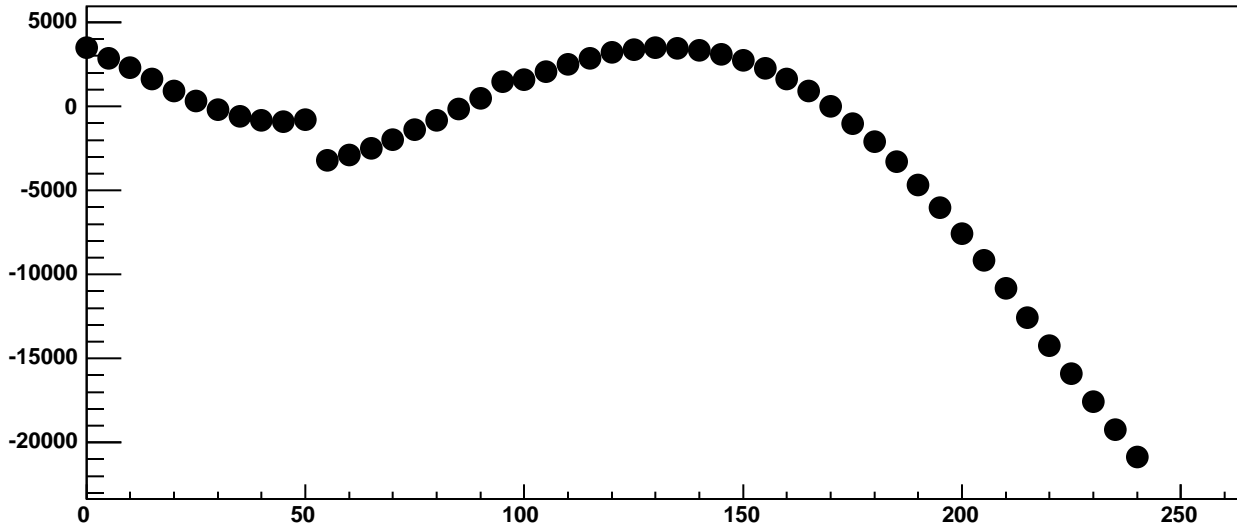
Chip 11, Channel 11, Enable 5, DAC=1600, ADC Mean vs Hold



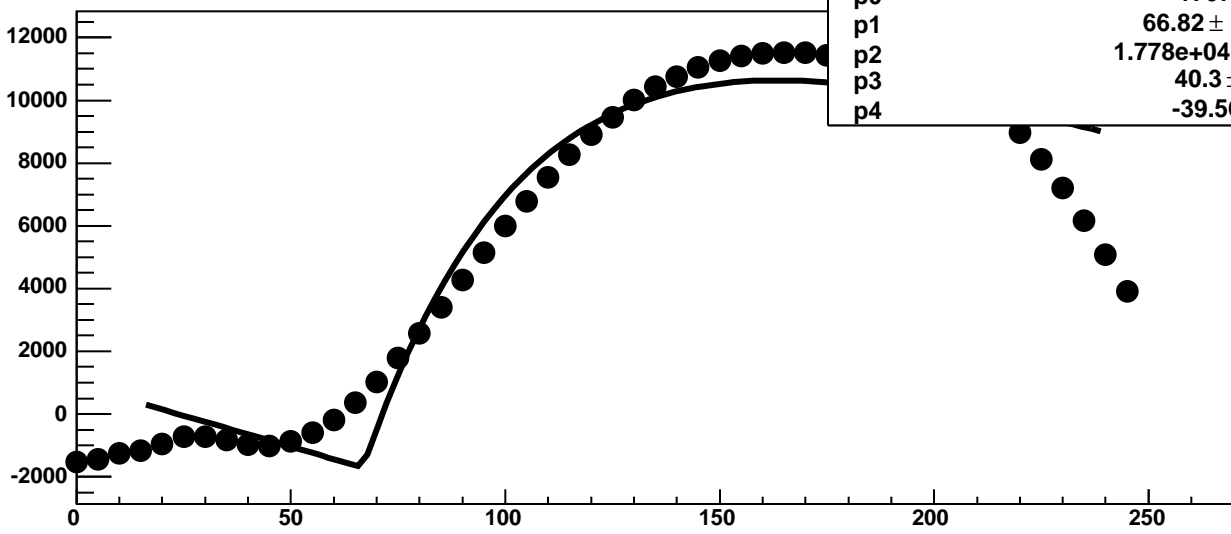
Chip 11, Channel 11, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 11, Enable 5, DAC=1600, ADC Residuals vs Hold

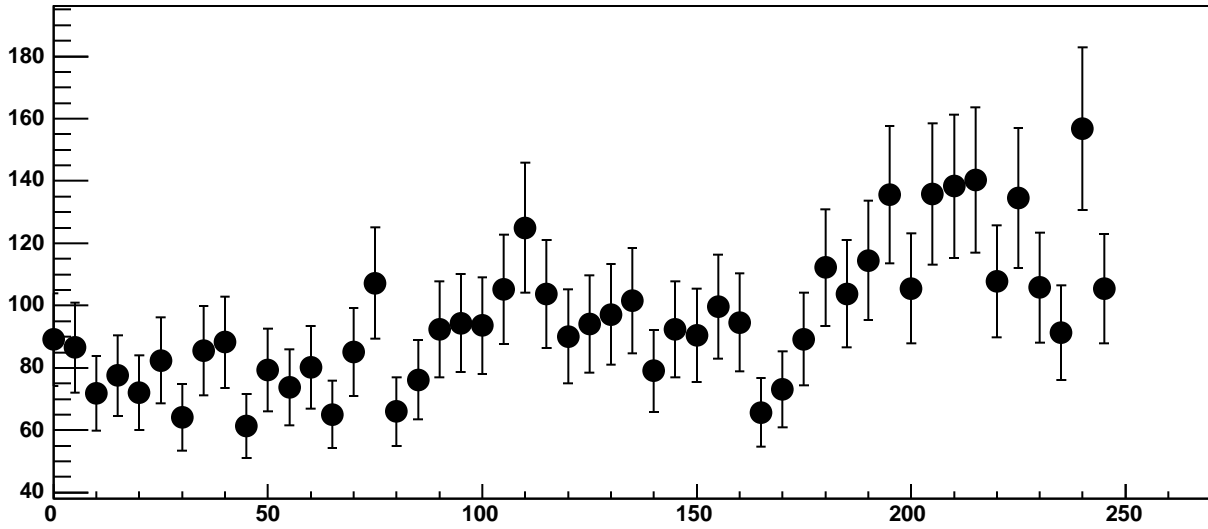


Chip 11, Channel 12, Enable 0, DAC=1600, ADC Mean vs Hold

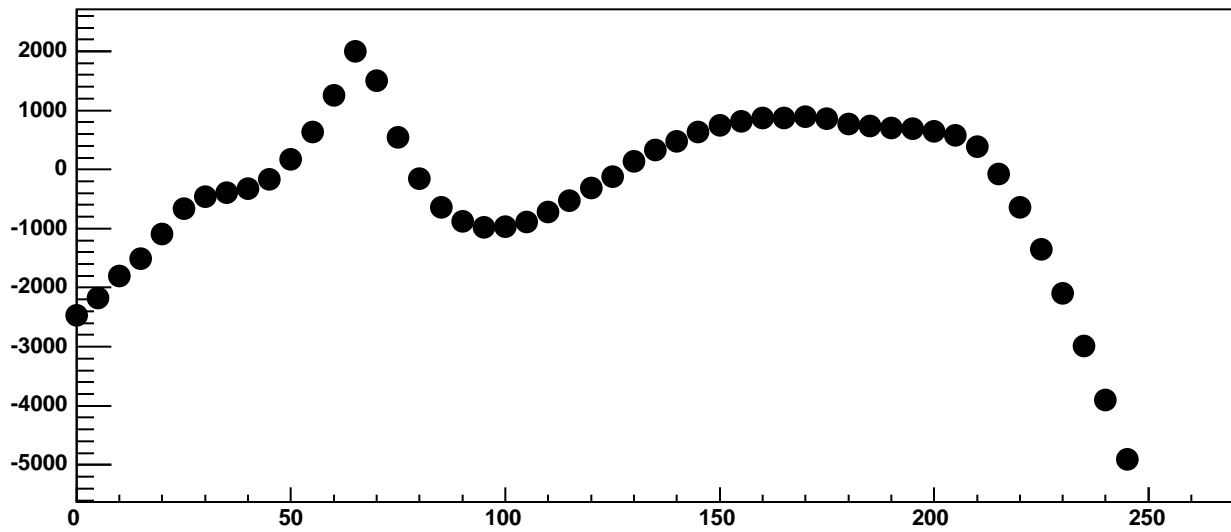


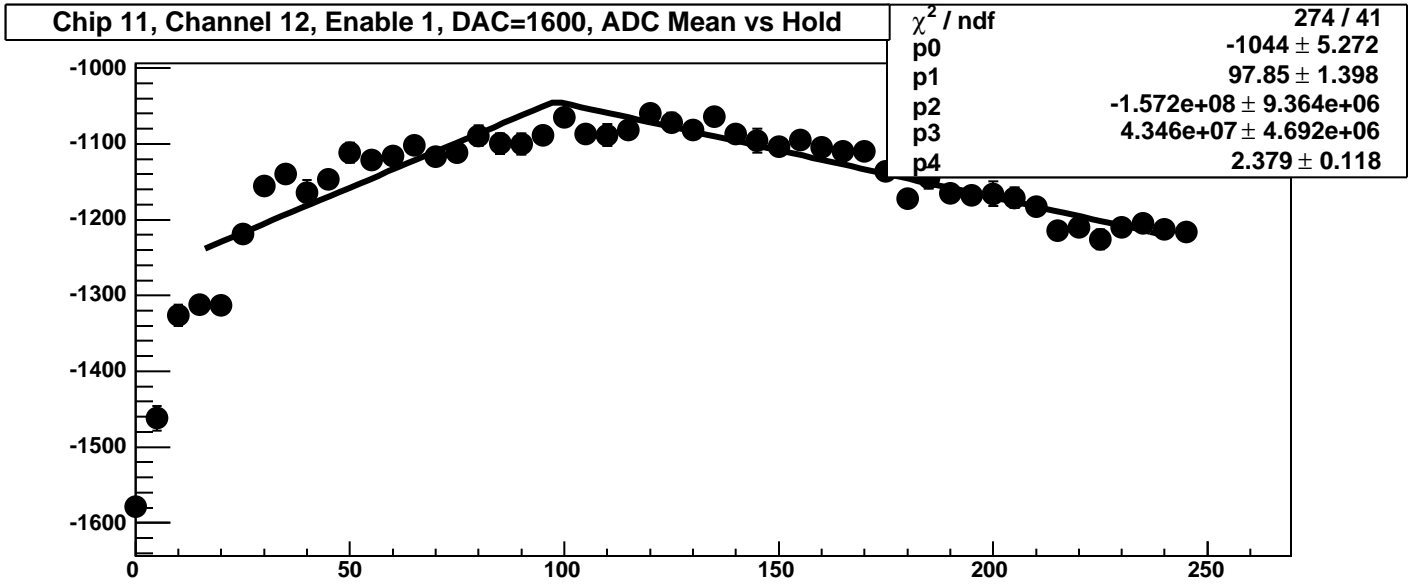
$\chi^2 / \text{ndf}$	1.155e+05 / 41
p0	-1707 ± 6.858
p1	66.82 ± 0.03885
p2	1.778e+04 ± 38.99
p3	40.3 ± 0.1071
p4	-39.56 ± 0.21

Chip 11, Channel 12, Enable 0, DAC=1600, ADC Noise vs Hold

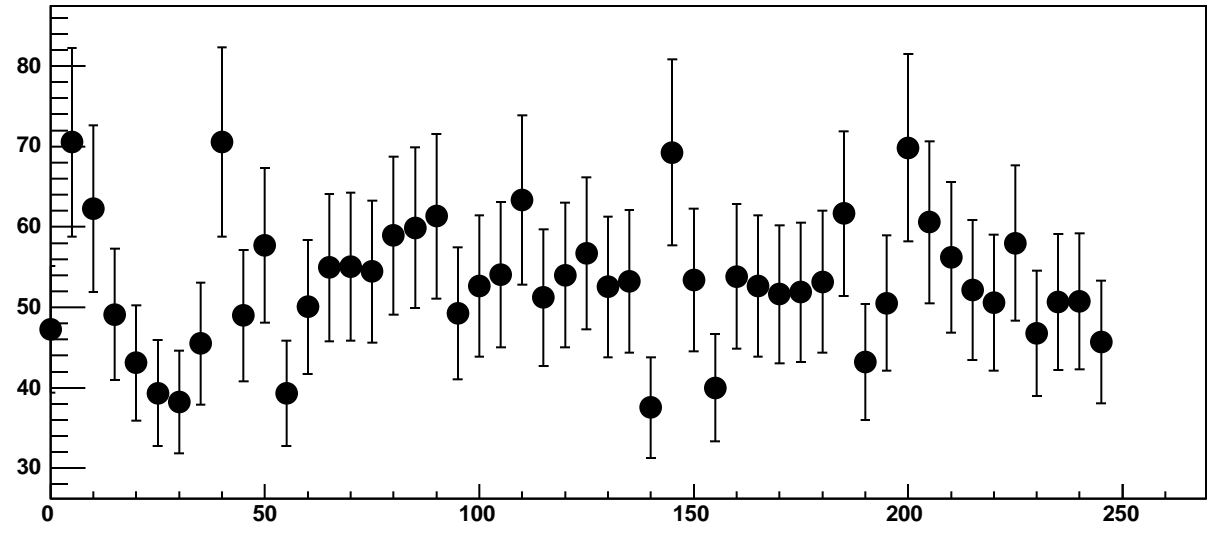


Chip 11, Channel 12, Enable 0, DAC=1600, ADC Residuals vs Hold

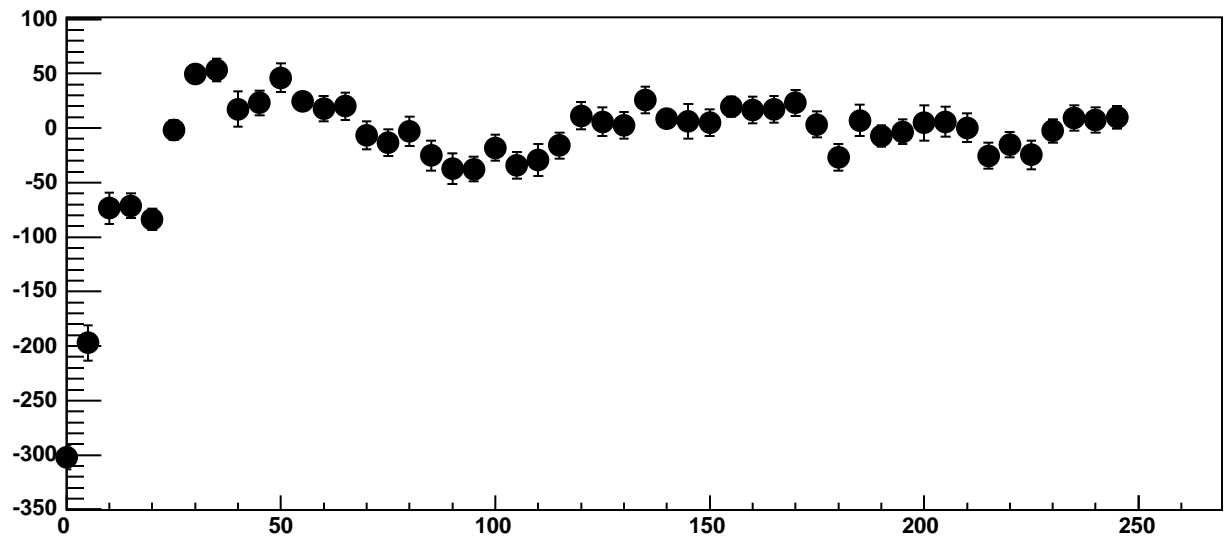




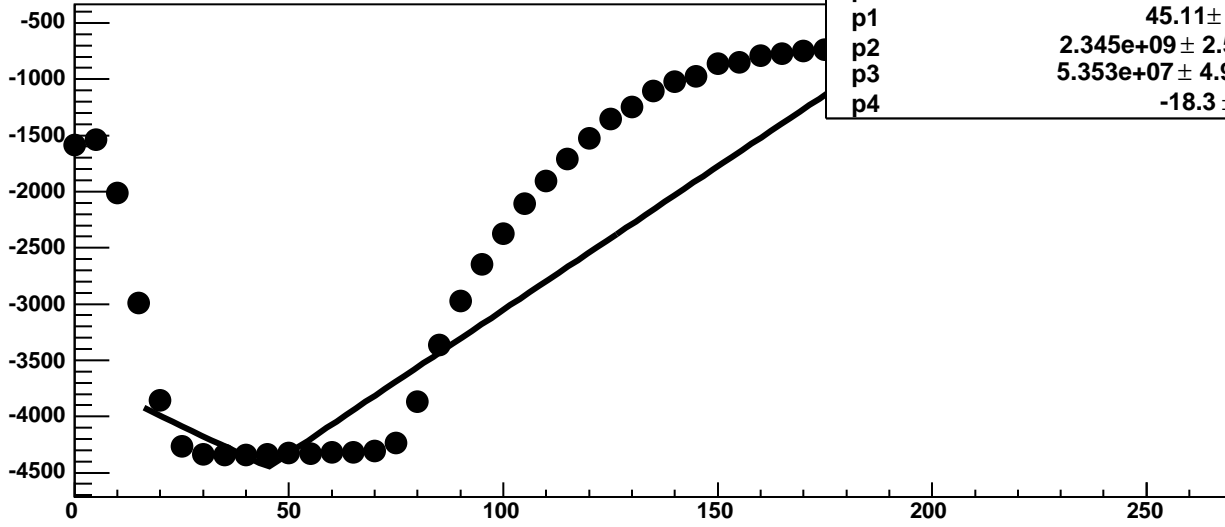
**Chip 11, Channel 12, Enable 1, DAC=1600, ADC Noise vs Hold**



**Chip 11, Channel 12, Enable 1, DAC=1600, ADC Residuals vs Hold**

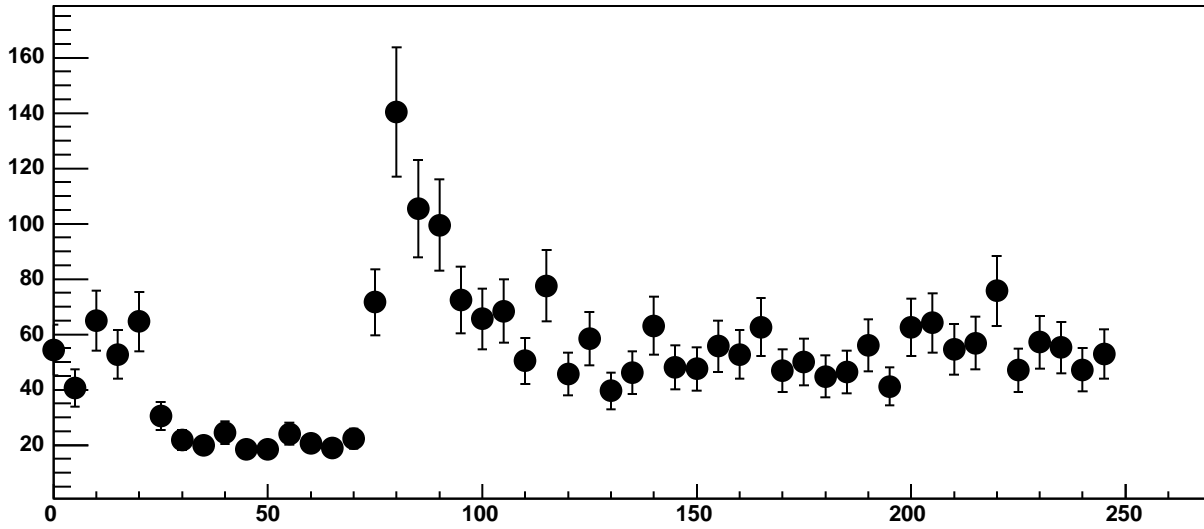


Chip 11, Channel 12, Enable 2, DAC=1600, ADC Mean vs Hold

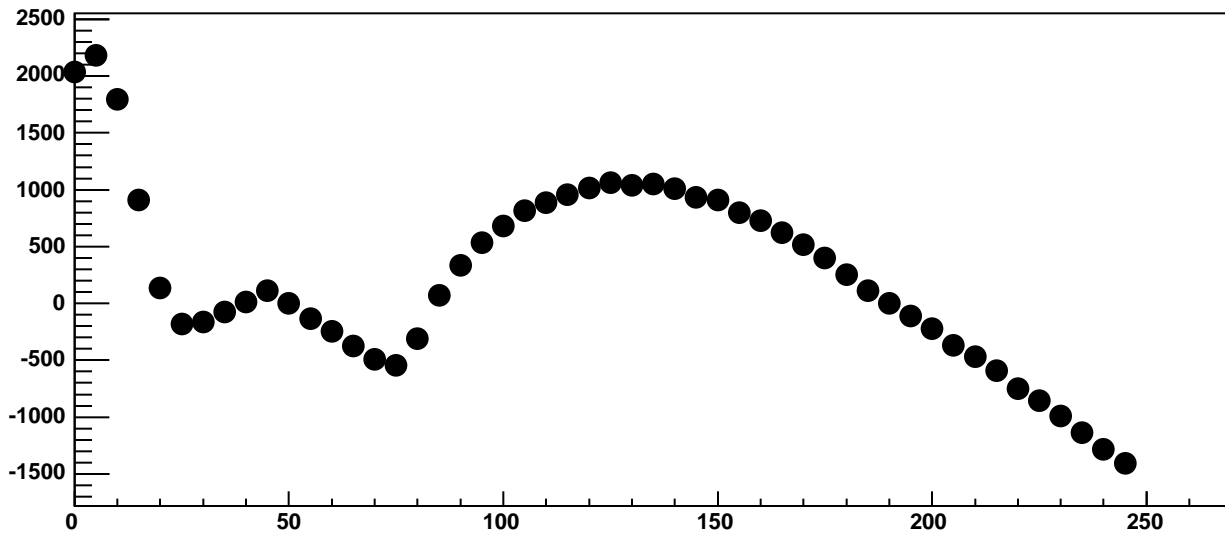


$\chi^2 / \text{ndf}$	1.559e+05 / 41
p0	-4451 ± 2.204
p1	45.11 ± 0.09354
p2	2.345e+09 ± 2.589e+07
p3	5.353e+07 ± 4.982e+05
p4	-18.3 ± 0.2749

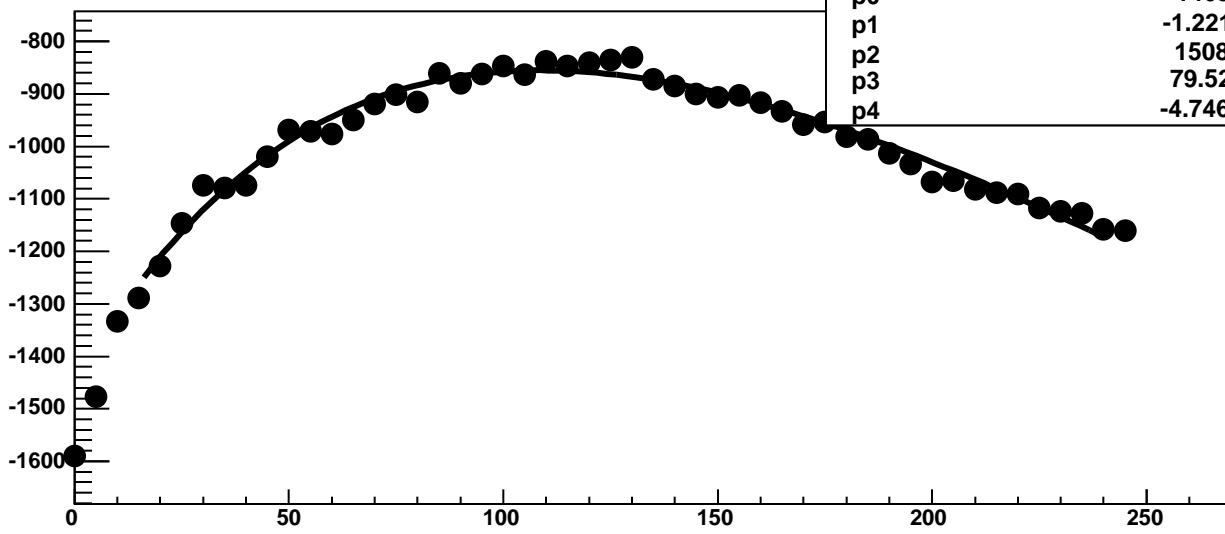
Chip 11, Channel 12, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 12, Enable 2, DAC=1600, ADC Residuals vs Hold

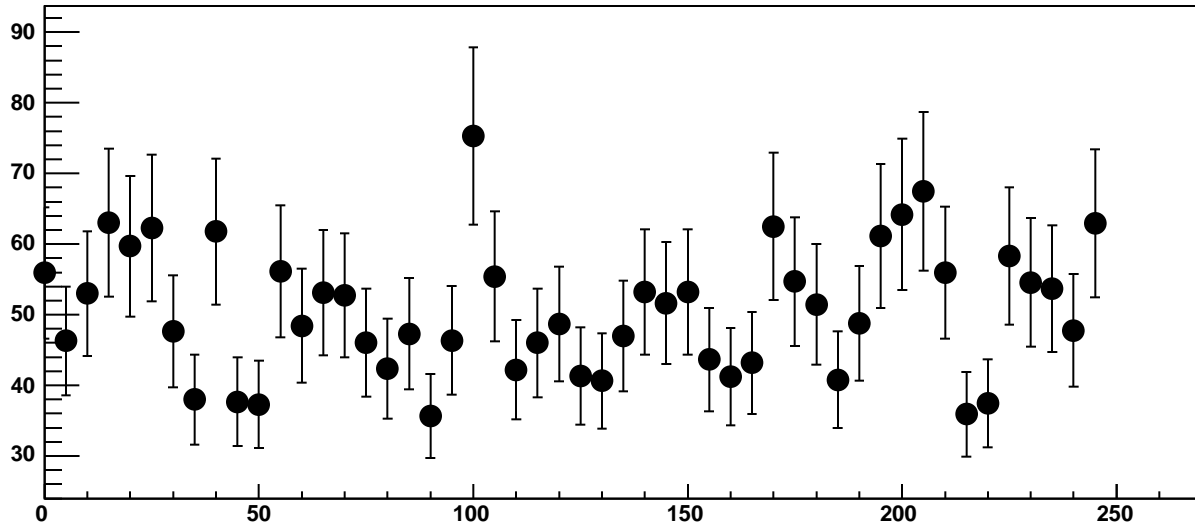


Chip 11, Channel 12, Enable 3, DAC=1600, ADC Mean vs Hold

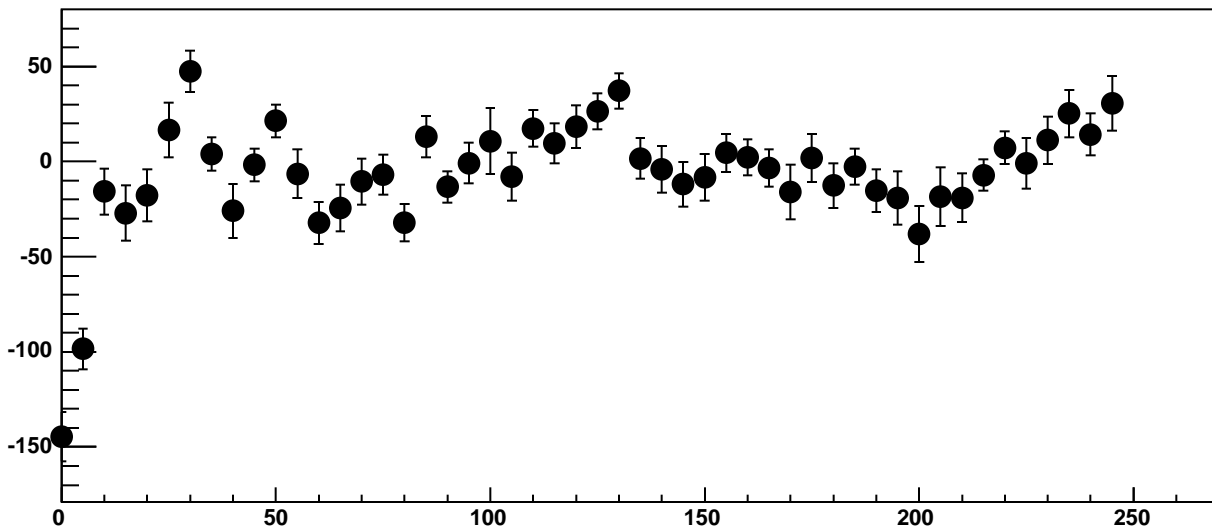


$\chi^2 / \text{ndf}$	122 / 41
p0	$-1463 \pm 21.73$
p1	$-1.221 \pm 1.538$
p2	$1508 \pm 29.23$
p3	$79.52 \pm 2.041$
p4	$-4.746 \pm 0.107$

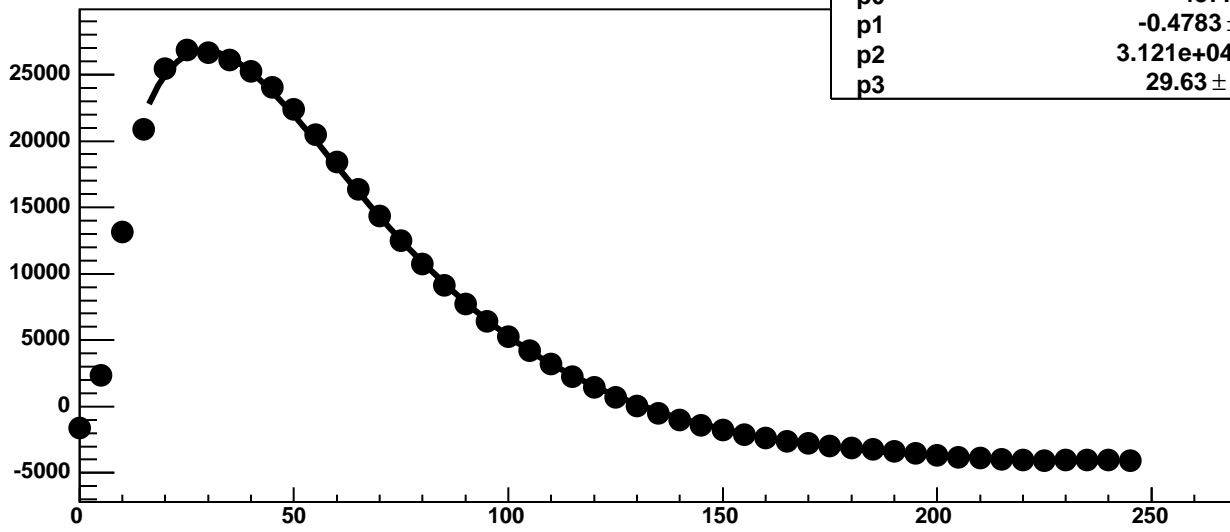
Chip 11, Channel 12, Enable 3, DAC=1600, ADC Noise vs Hold



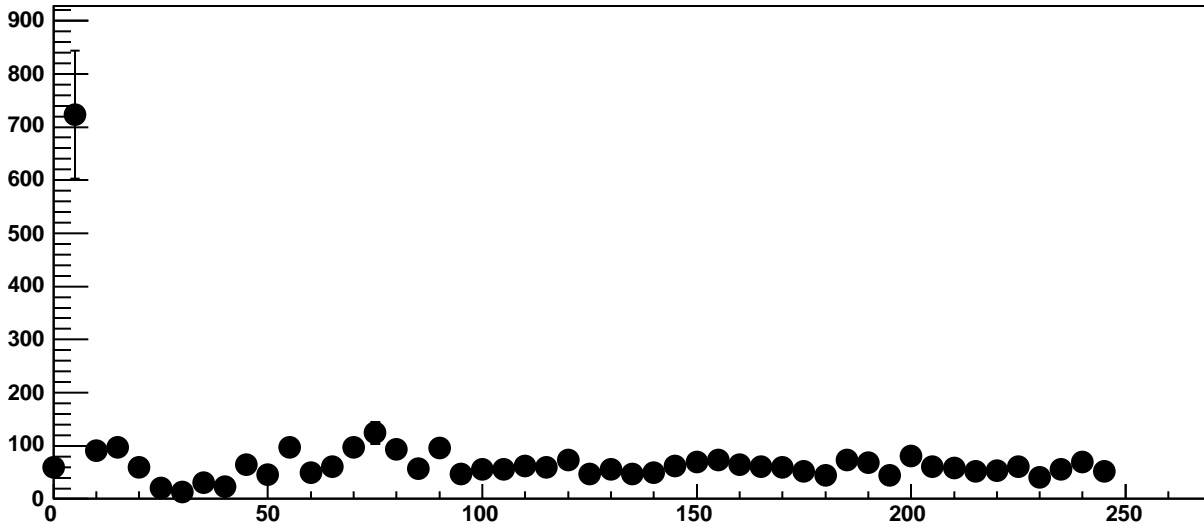
Chip 11, Channel 12, Enable 3, DAC=1600, ADC Residuals vs Hold



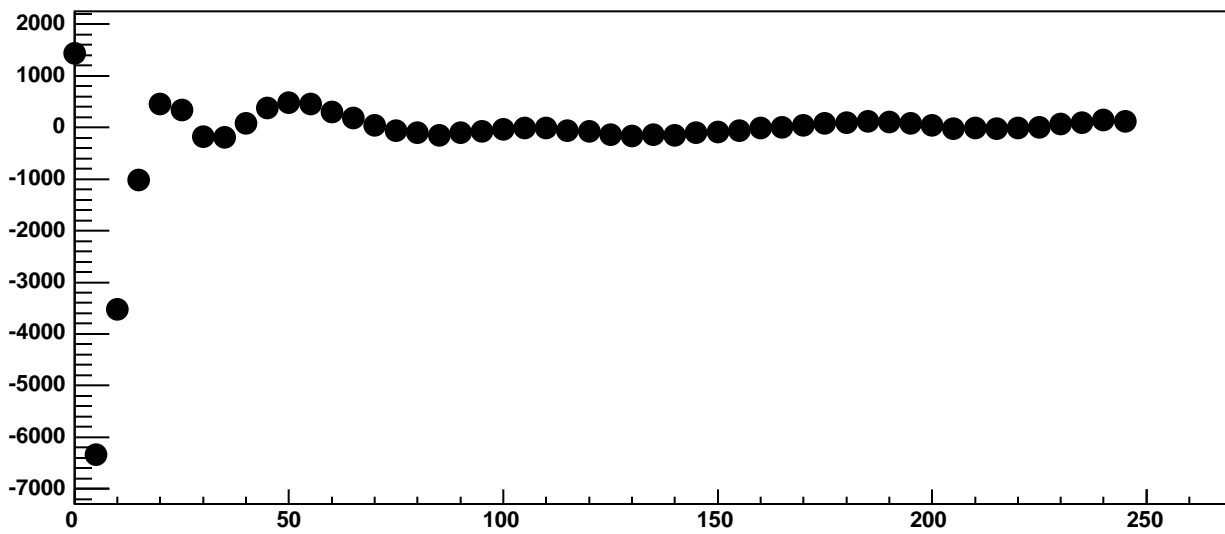
Chip 11, Channel 12, Enable 4!, DAC=1600, ADC Mean vs Hold



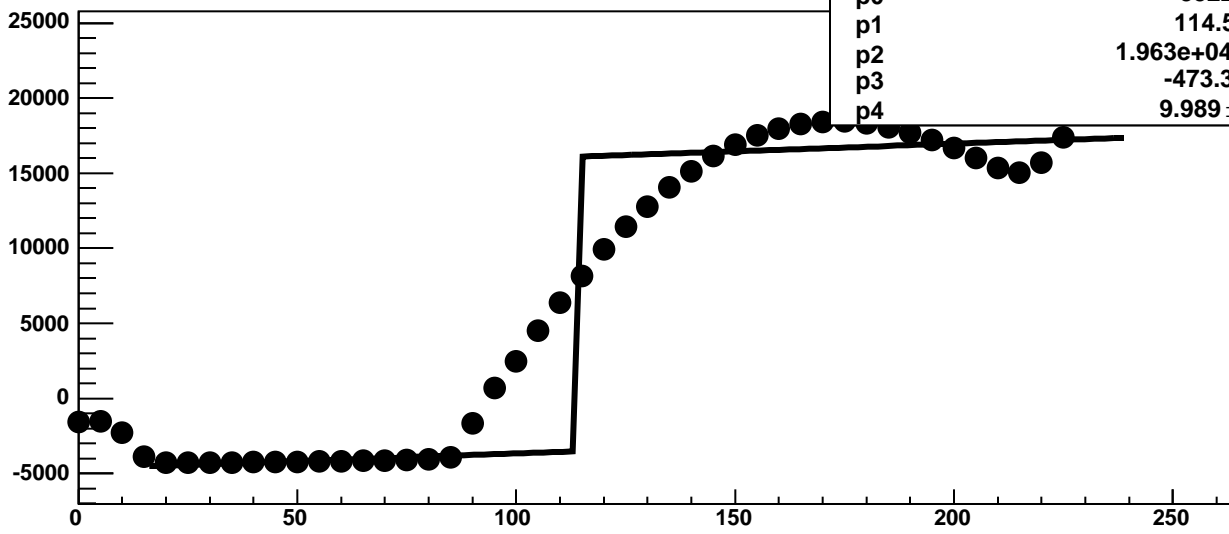
Chip 11, Channel 12, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 12, Enable 4!, DAC=1600, ADC Residuals vs Hold

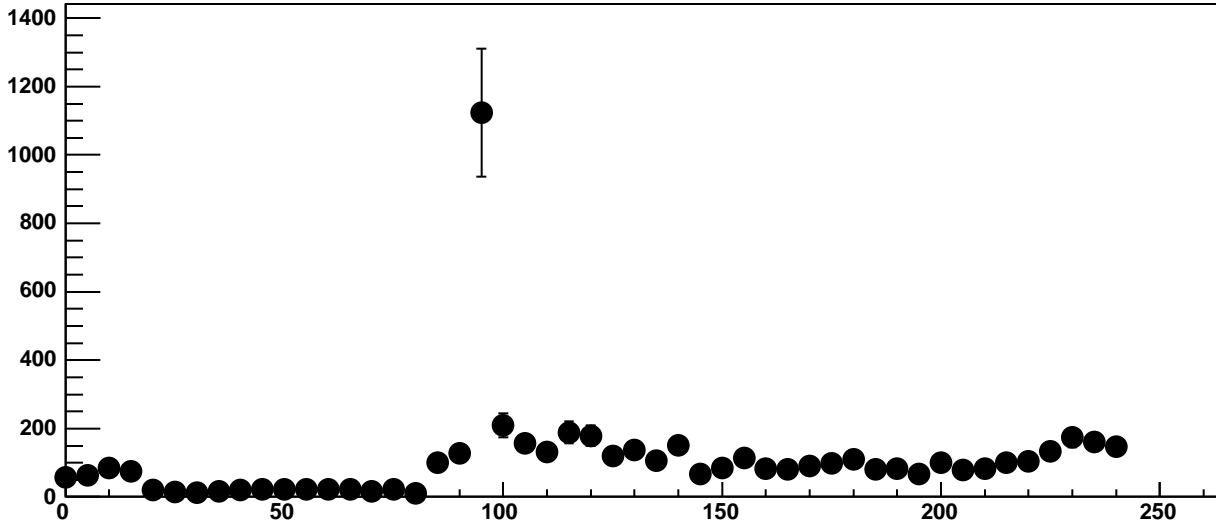


Chip 11, Channel 12, Enable 5, DAC=1600, ADC Mean vs Hold

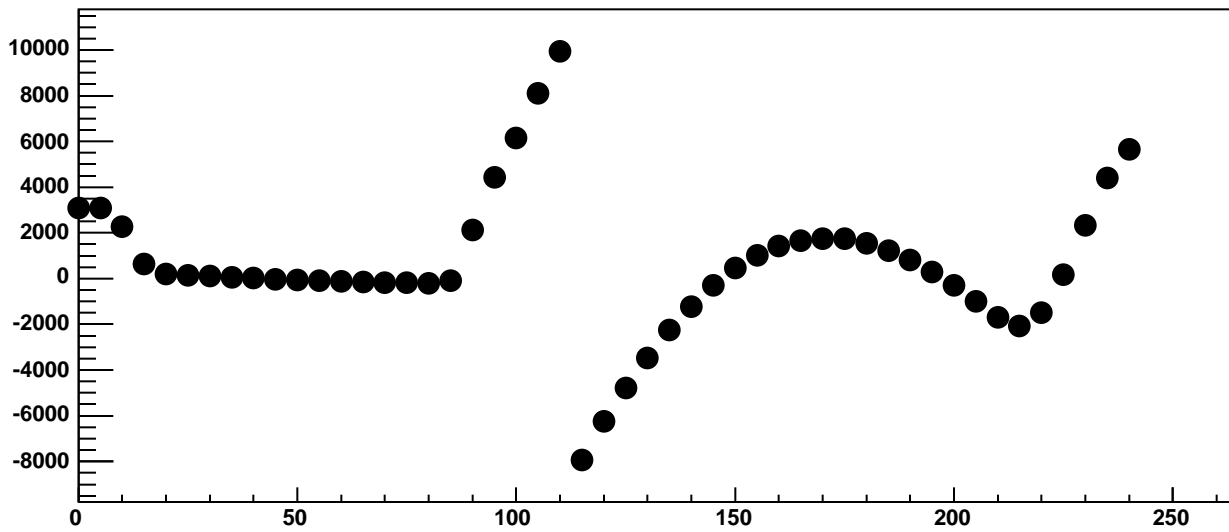


$\chi^2 / \text{ndf}$	4.148e+05 / 41
p0	-3522 ± 1.465
p1	114.5 ± 1.264
p2	1.963e+04 ± 15.29
p3	-473.3 ± 5.648
p4	9.989 ± 0.1583

Chip 11, Channel 12, Enable 5, DAC=1600, ADC Noise vs Hold

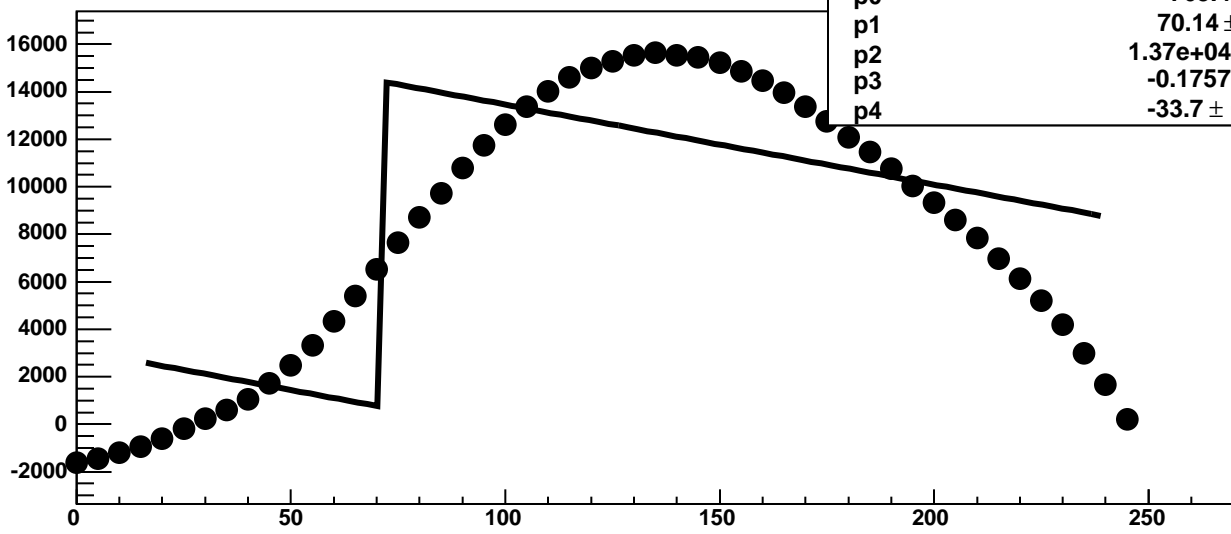


Chip 11, Channel 12, Enable 5, DAC=1600, ADC Residuals vs Hold



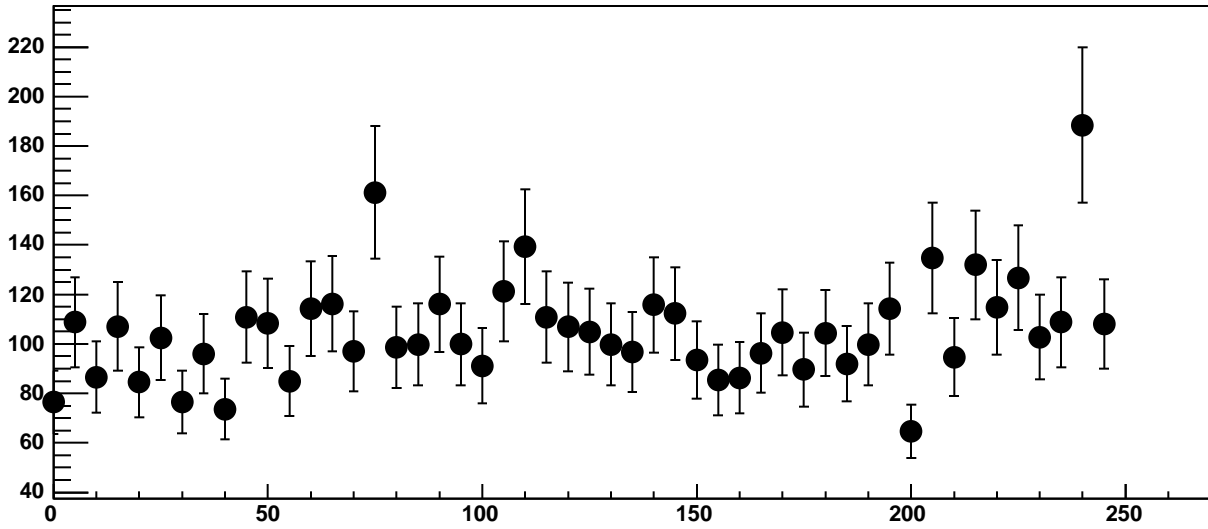


Chip 11, Channel 13, Enable 0, DAC=1600, ADC Mean vs Hold

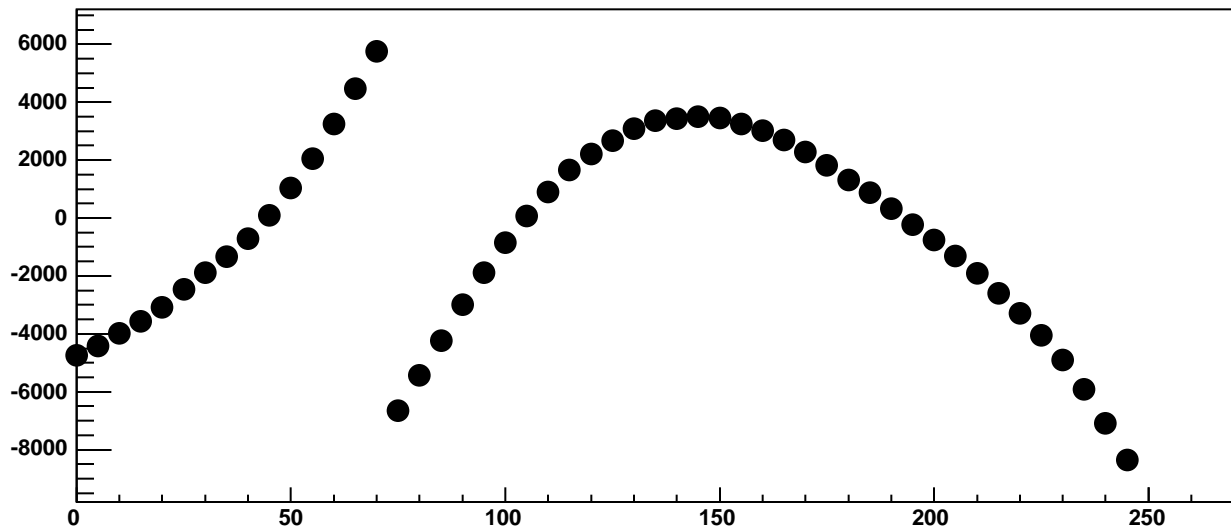


$\chi^2 / \text{ndf}$	7.384e+05 / 41
p0	765.4 ± 1.414
p1	70.14 ± 0.1363
p2	1.37e+04 ± 1.405
p3	-0.1757 ± 1.414
p4	-33.7 ± 0.05177

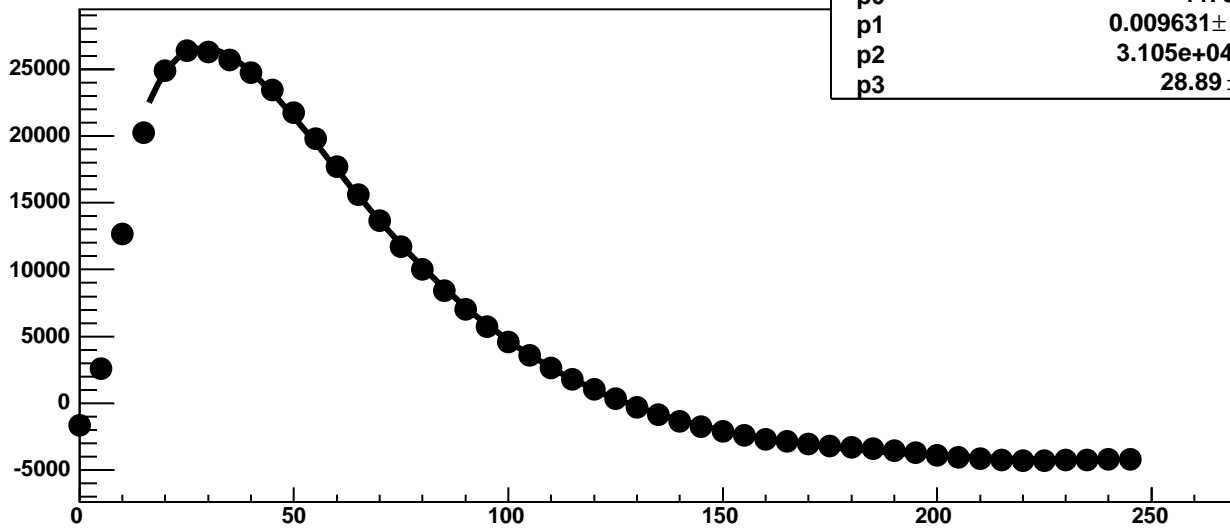
Chip 11, Channel 13, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 13, Enable 0, DAC=1600, ADC Residuals vs Hold



Chip 11, Channel 13, Enable 1!, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$

8601 / 42

p0

$-4470 \pm 4.077$

p1

$0.009631 \pm 0.02059$

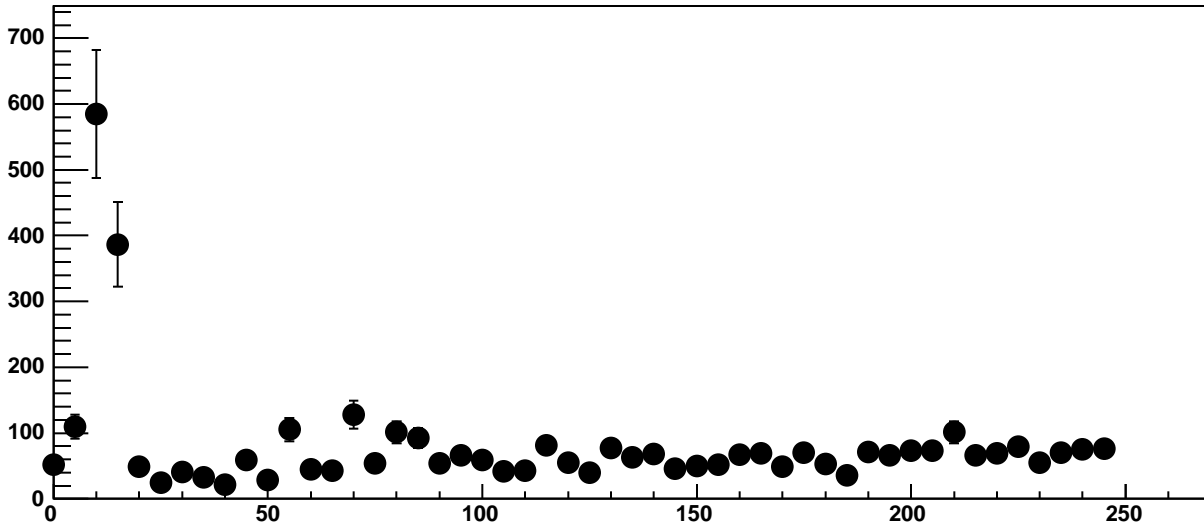
p2

$3.105e+04 \pm 4.753$

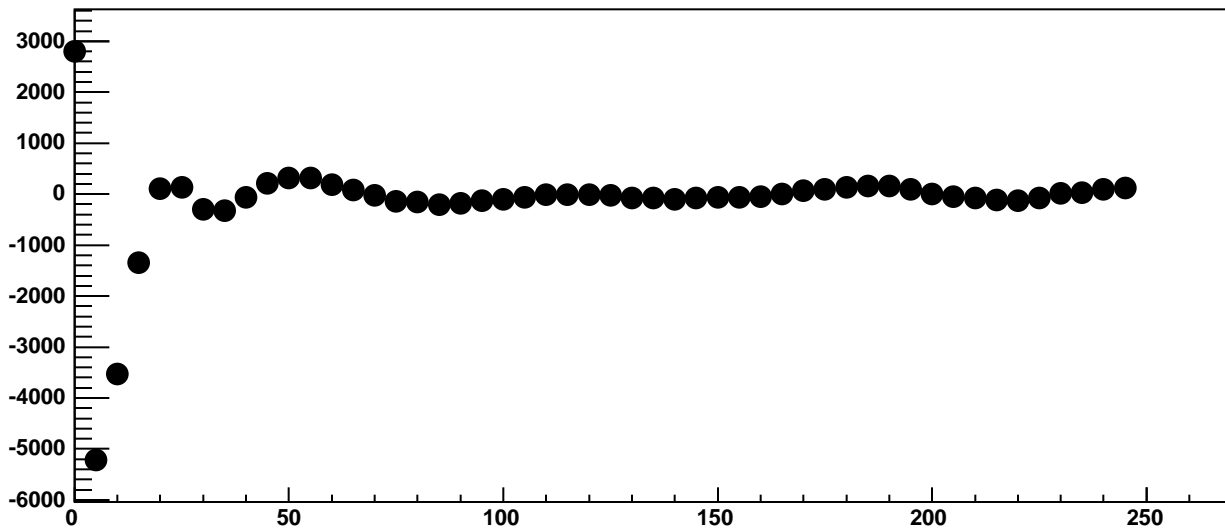
p3

$28.89 \pm 0.0118$

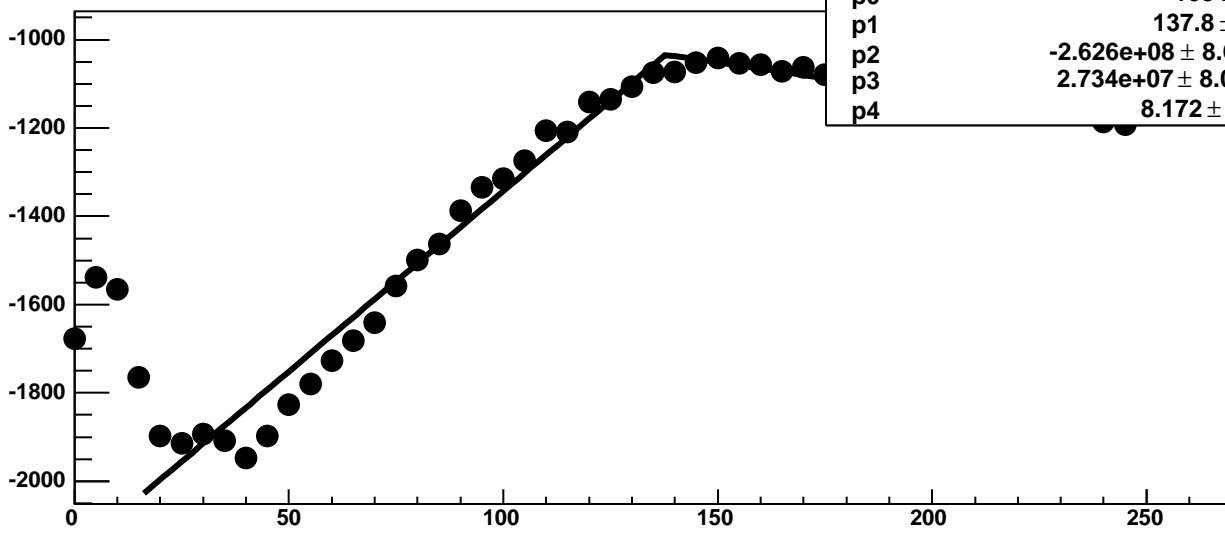
Chip 11, Channel 13, Enable 1!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 13, Enable 1!, DAC=1600, ADC Residuals vs Hold

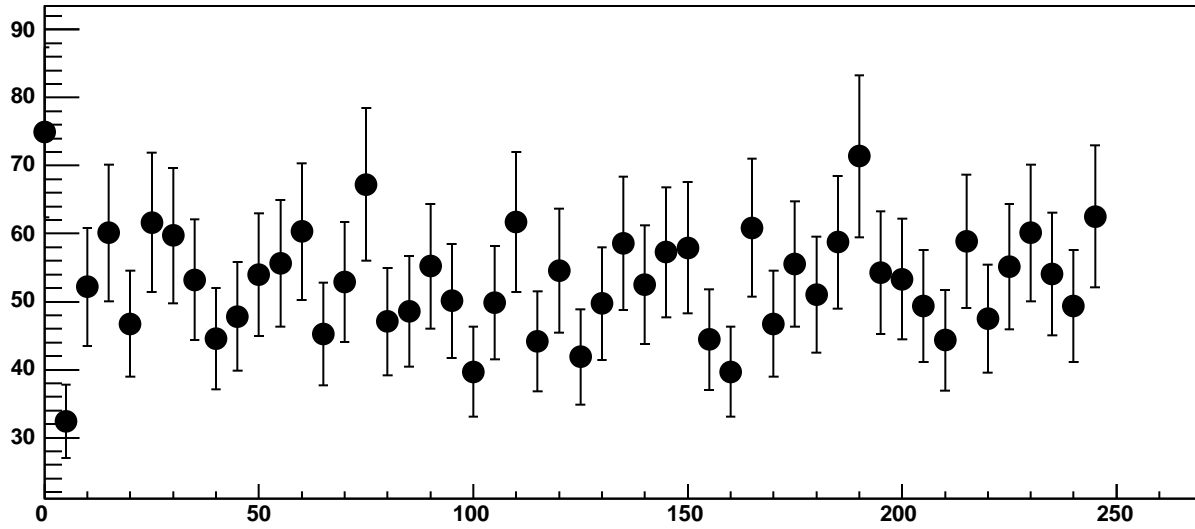


Chip 11, Channel 13, Enable 2, DAC=1600, ADC Mean vs Hold

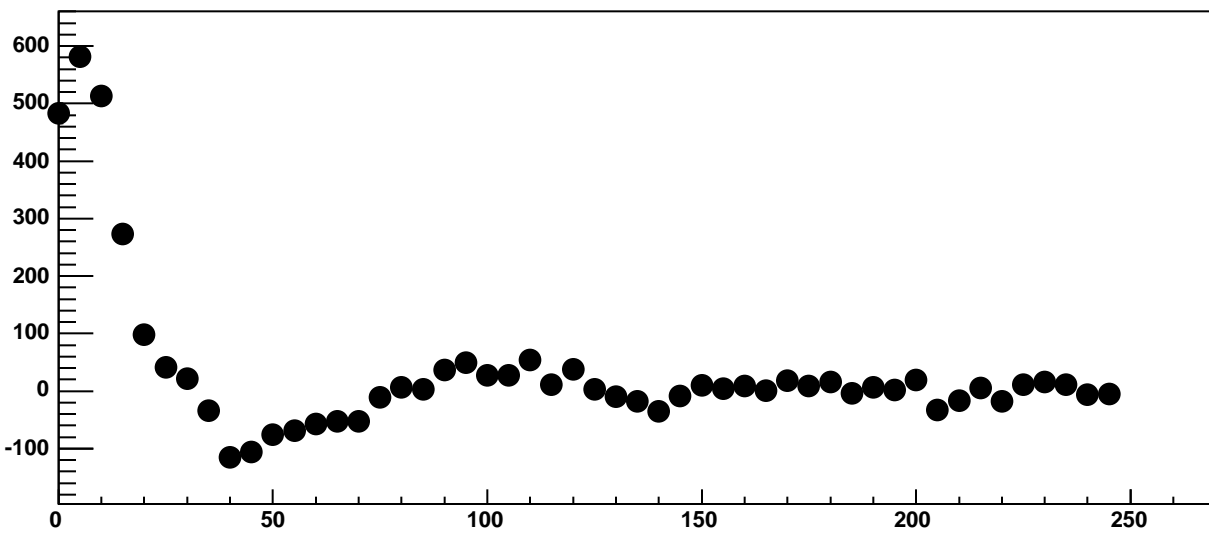


$\chi^2 / \text{ndf}$	949.1 / 41
p0	-1034 ± 4.422
p1	137.8 ± 0.7175
p2	-2.626e+08 ± 8.613e+06
p3	2.734e+07 ± 8.066e+05
p4	8.172 ± 0.06589

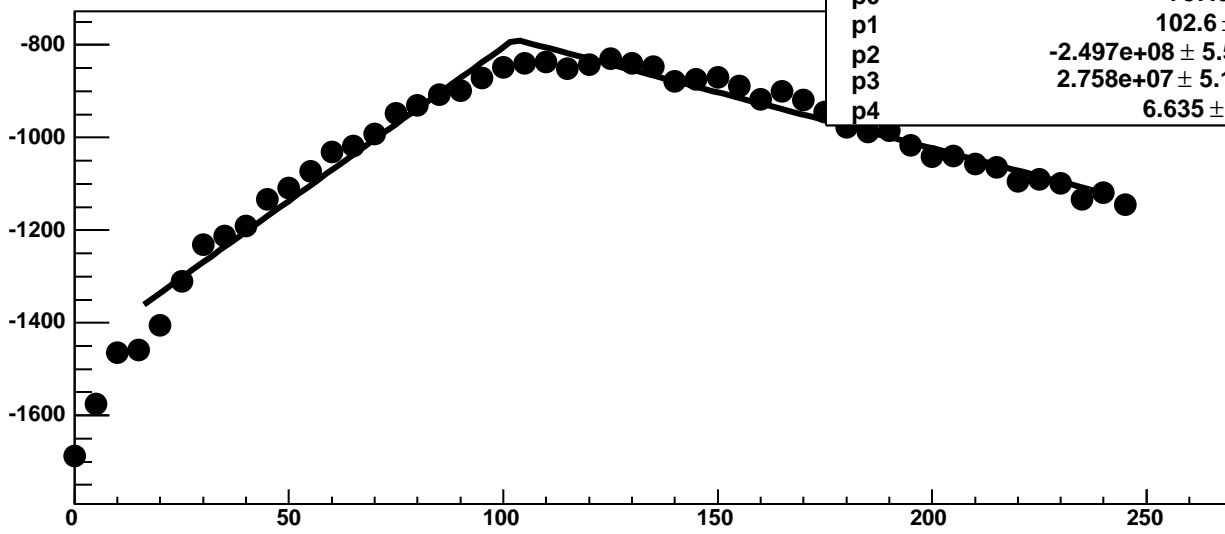
Chip 11, Channel 13, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 13, Enable 2, DAC=1600, ADC Residuals vs Hold

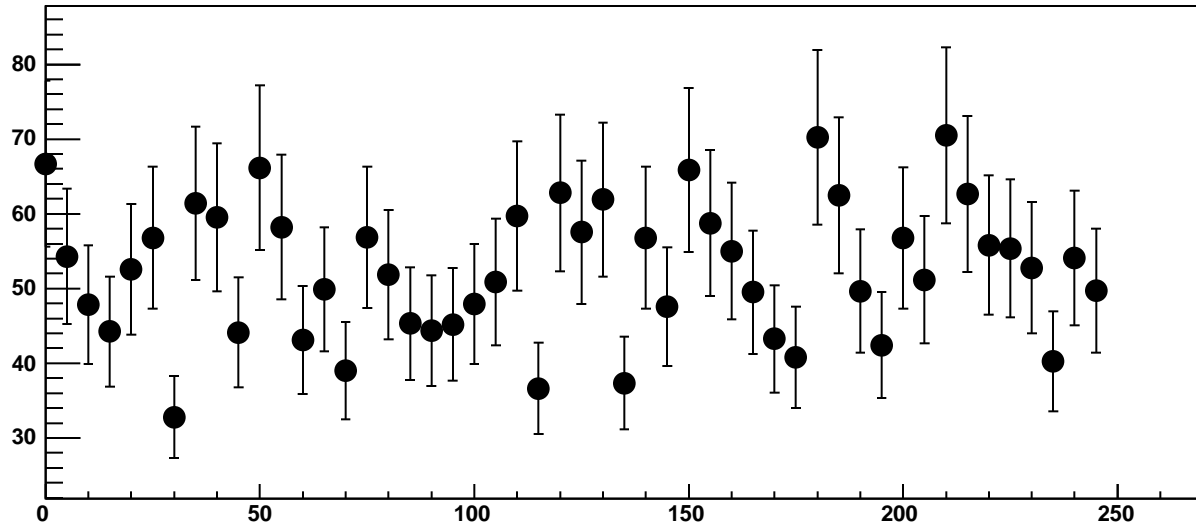


Chip 11, Channel 13, Enable 3, DAC=1600, ADC Mean vs Hold

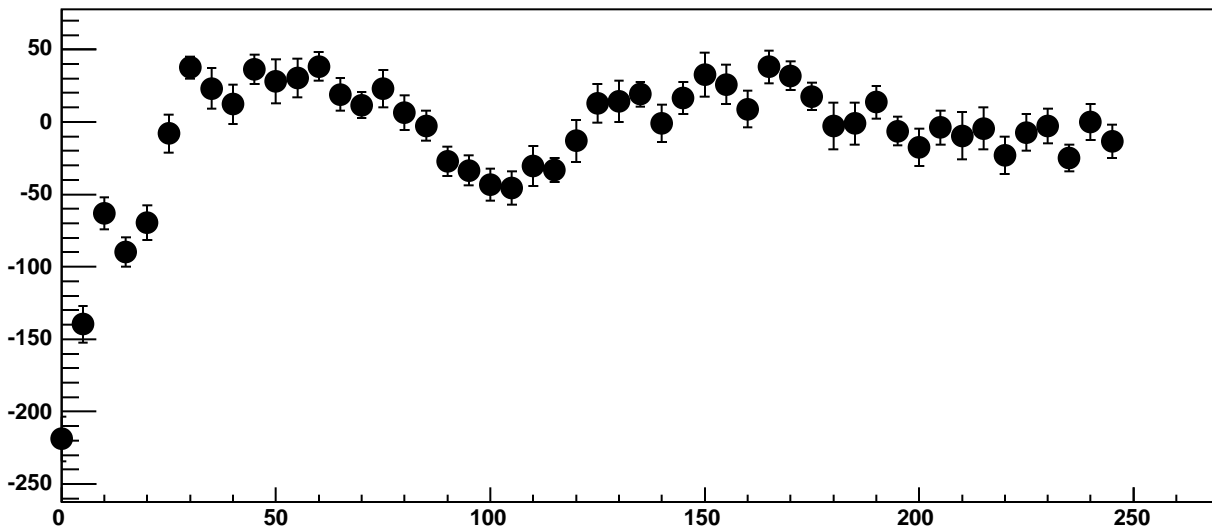


$\chi^2 / \text{ndf}$	313.1 / 41
p0	$-787.6 \pm 3.465$
p1	$102.6 \pm 0.7372$
p2	$-2.497\text{e}+08 \pm 5.598\text{e}+06$
p3	$2.758\text{e}+07 \pm 5.168\text{e}+05$
p4	$6.635 \pm 0.09721$

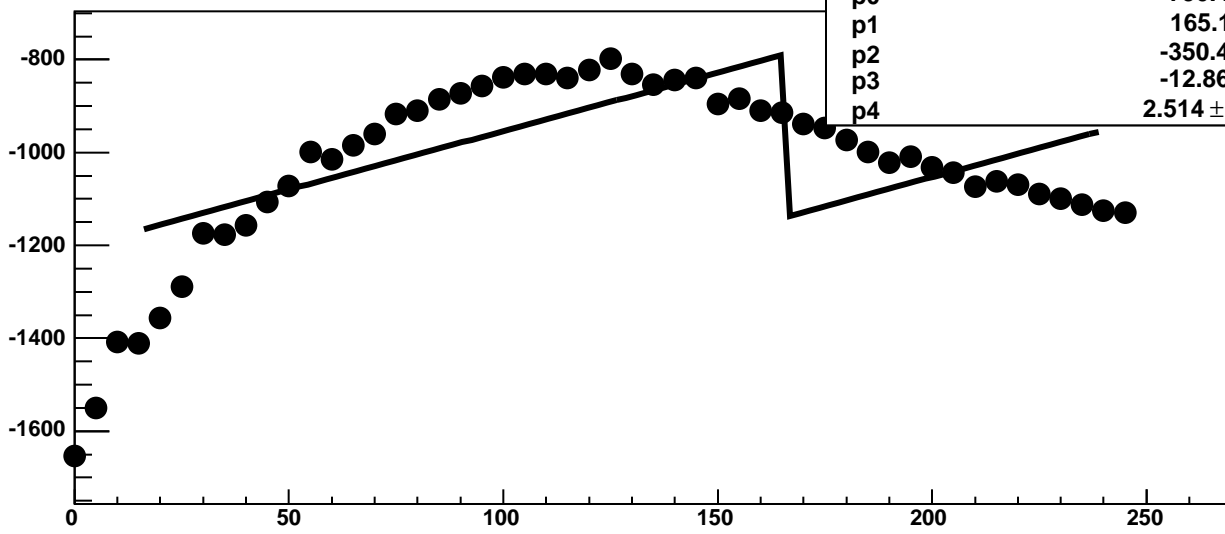
Chip 11, Channel 13, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 13, Enable 3, DAC=1600, ADC Residuals vs Hold

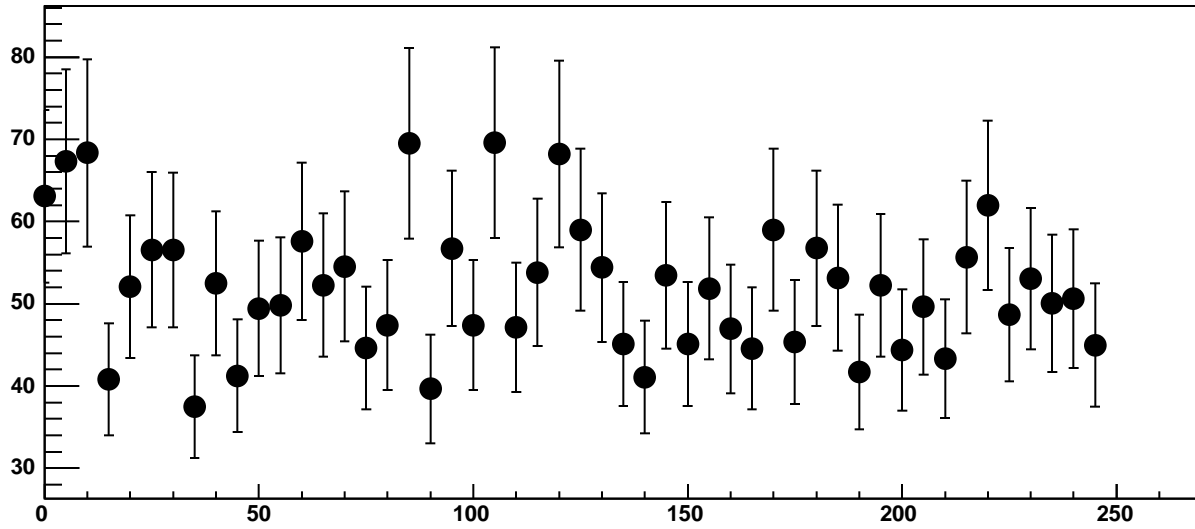


Chip 11, Channel 13, Enable 4, DAC=1600, ADC Mean vs Hold

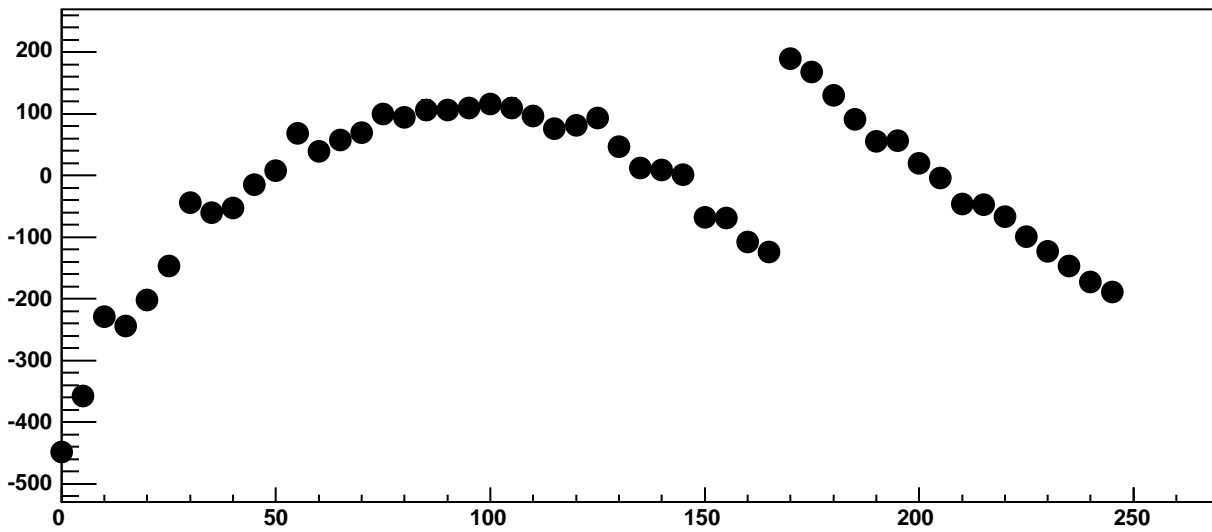


$\chi^2 / \text{ndf}$	3682 / 41
p0	-790.4 ± 12.43
p1	165.1 ± 4.254
p2	-350.4 ± 21.79
p3	-12.86 ± 29.96
p4	2.514 ± 0.03571

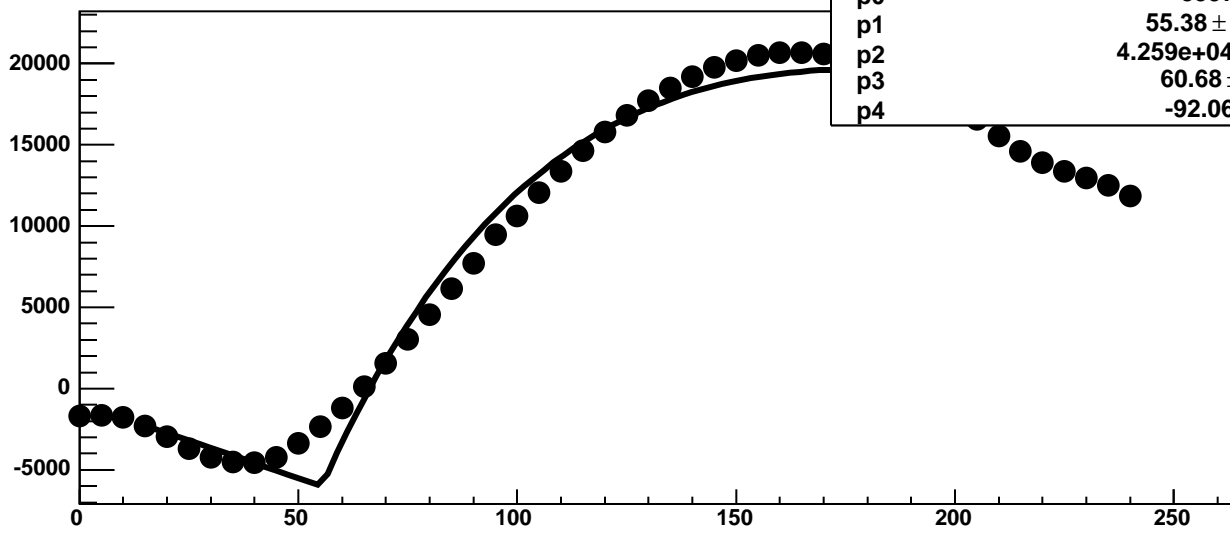
Chip 11, Channel 13, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 13, Enable 4, DAC=1600, ADC Residuals vs Hold

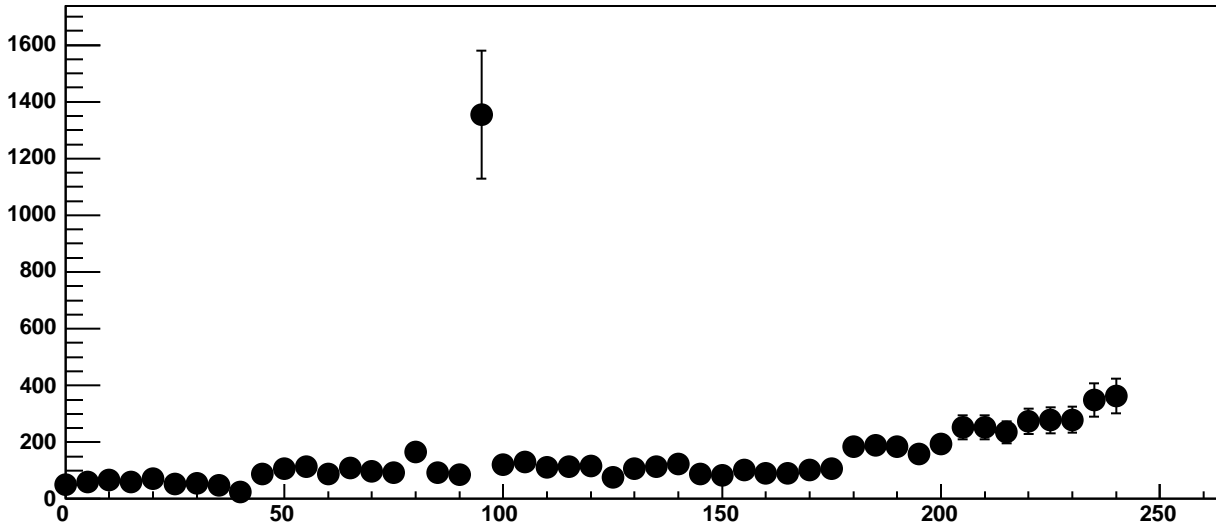


Chip 11, Channel 13, Enable 5, DAC=1600, ADC Mean vs Hold

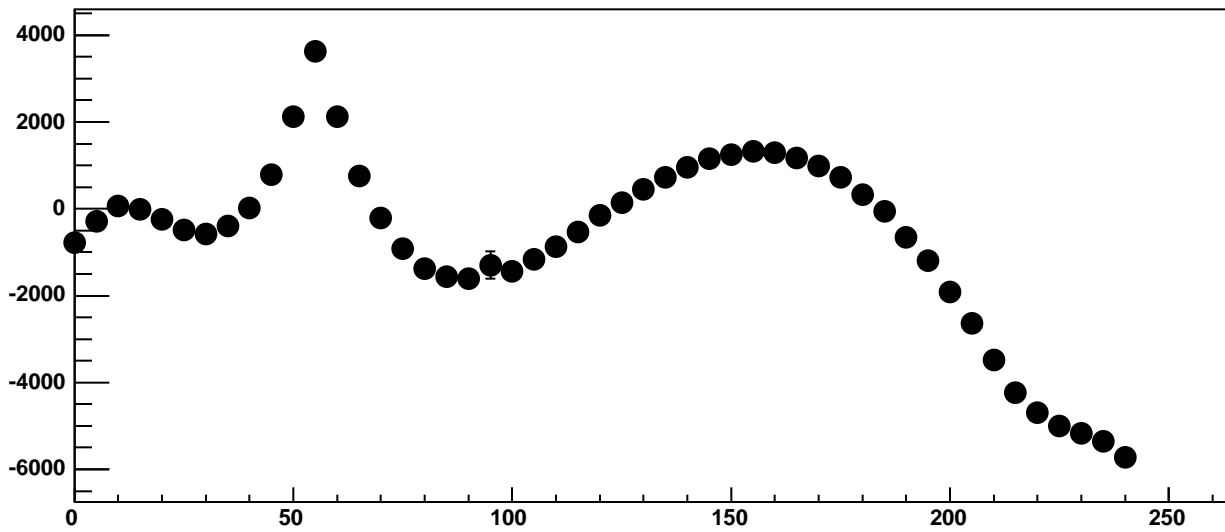


$\chi^2 / \text{ndf}$	1.317e+05 / 41
p0	-5997 $\pm$ 7.313
p1	55.38 $\pm$ 0.02689
p2	4.259e+04 $\pm$ 77.04
p3	60.68 $\pm$ 0.1163
p4	-92.06 $\pm$ 0.352

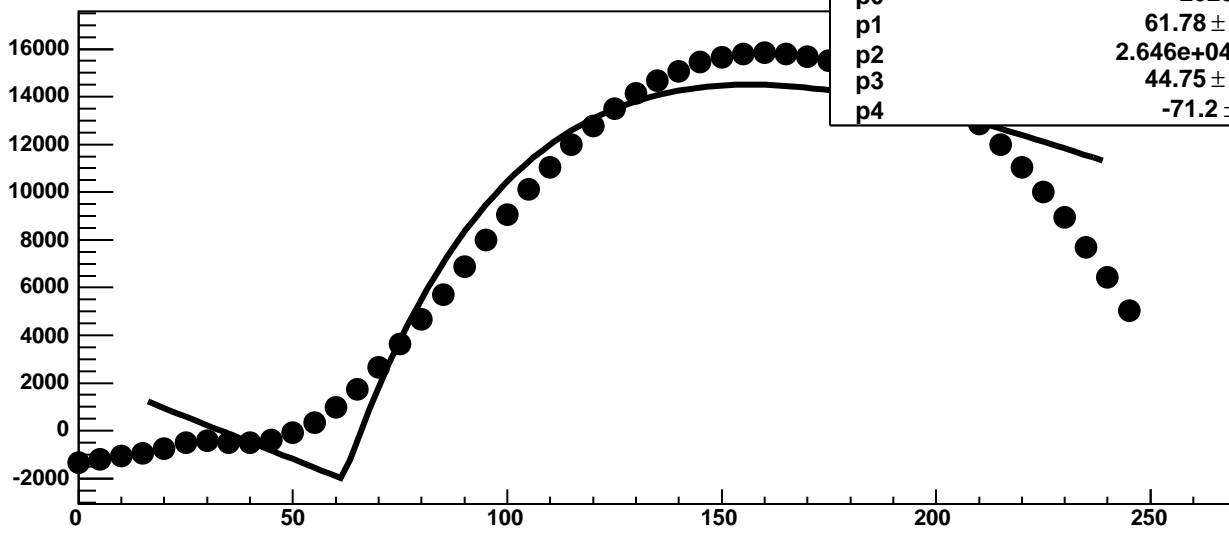
Chip 11, Channel 13, Enable 5, DAC=1600, ADC Noise vs Hold



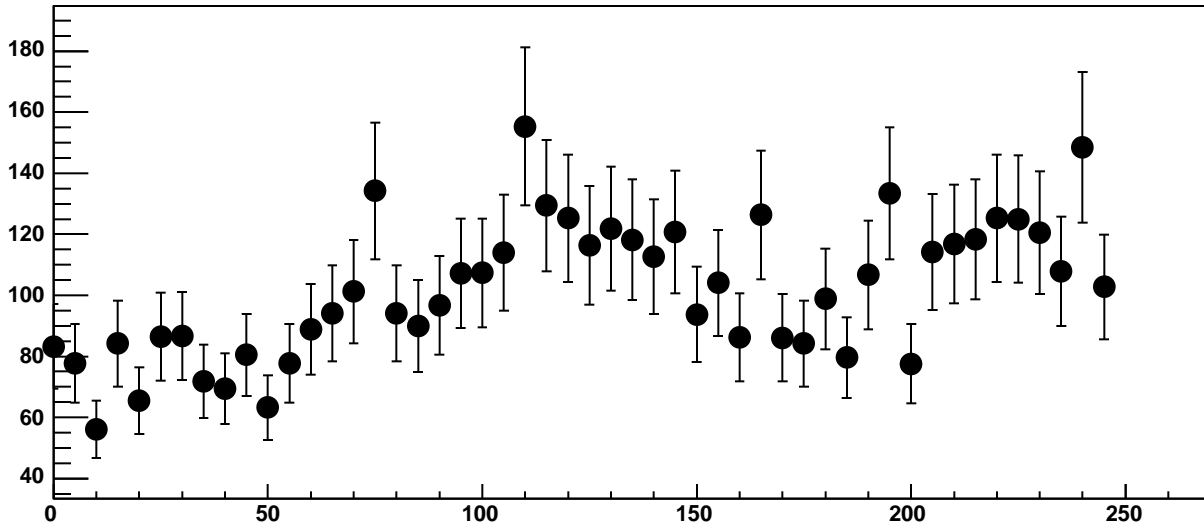
Chip 11, Channel 13, Enable 5, DAC=1600, ADC Residuals vs Hold



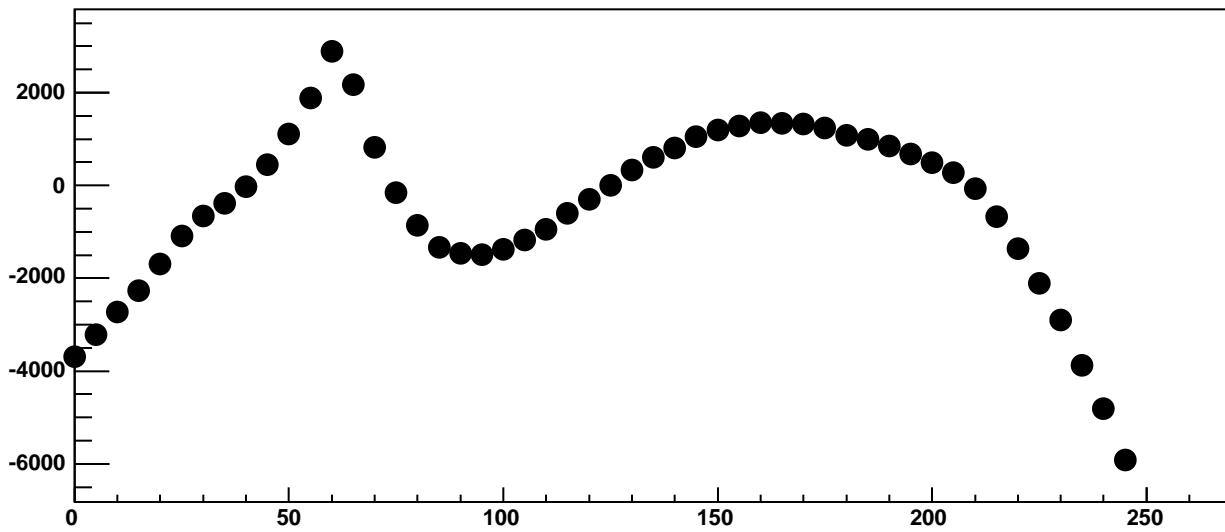
Chip 11, Channel 14, Enable 0, DAC=1600, ADC Mean vs Hold



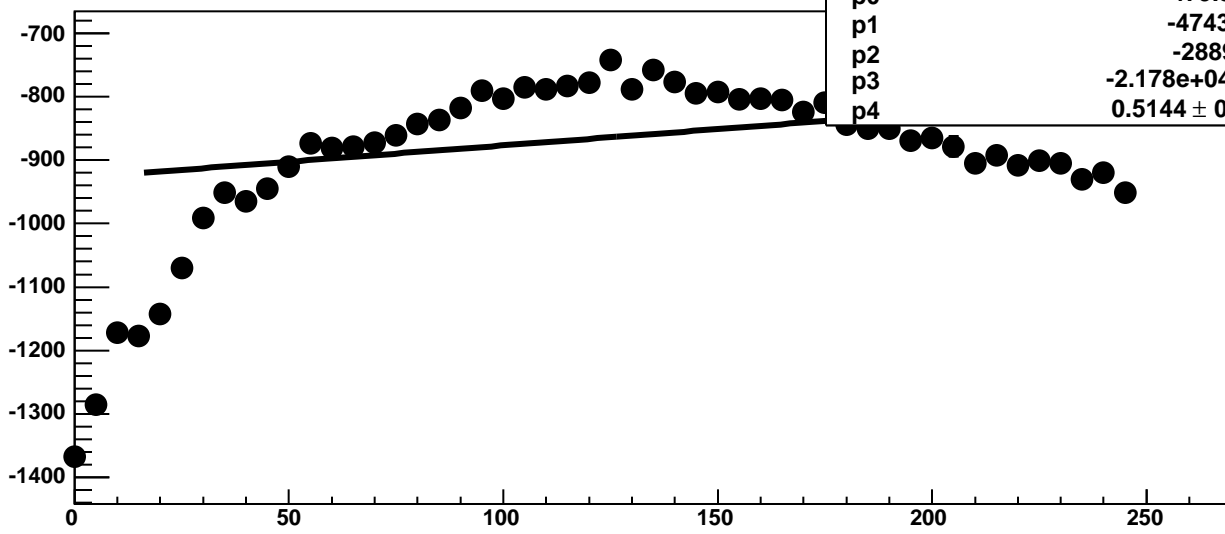
Chip 11, Channel 14, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 14, Enable 0, DAC=1600, ADC Residuals vs Hold

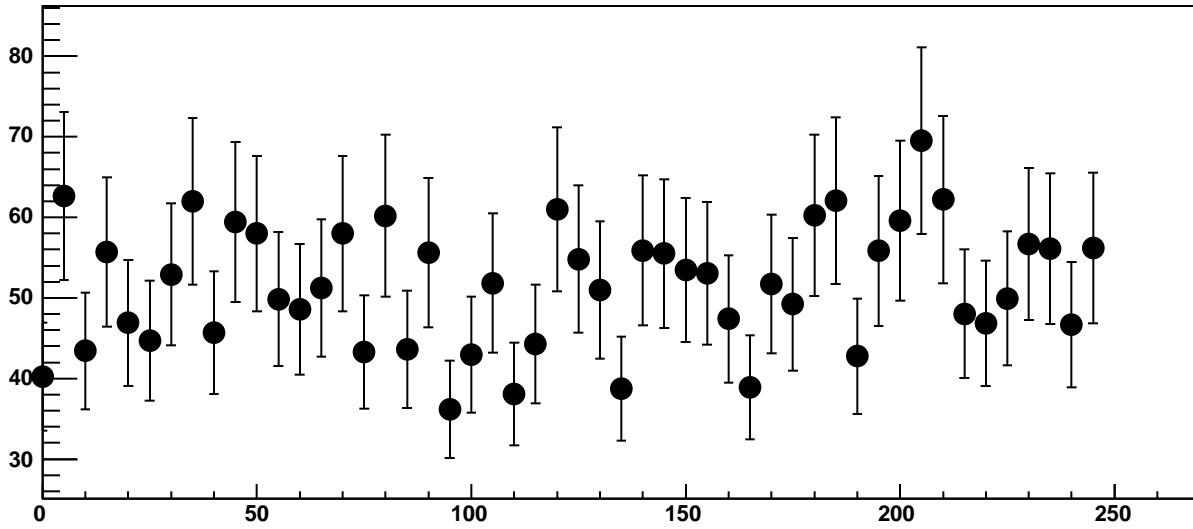


Chip 11, Channel 14, Enable 1, DAC=1600, ADC Mean vs Hold

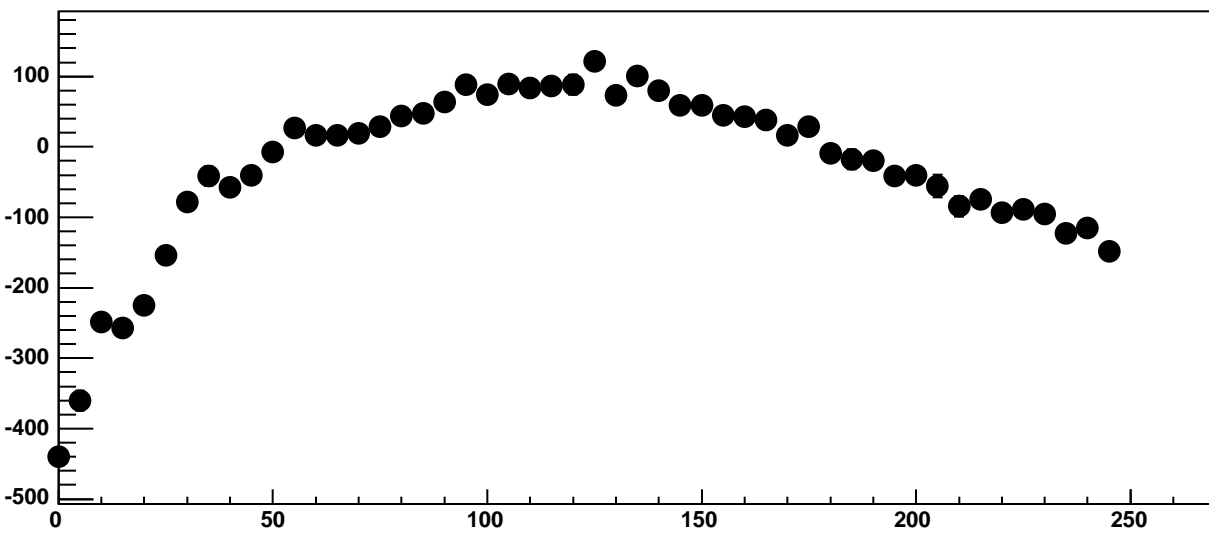


$\chi^2 / \text{ndf}$	2579 / 41
p0	-479.5 ± 8.371
p1	-4743 ± 14.59
p2	-2889 ± 11.01
p3	-2.178e+04 ± 1142
p4	0.5144 ± 0.001719

Chip 11, Channel 14, Enable 1, DAC=1600, ADC Noise vs Hold

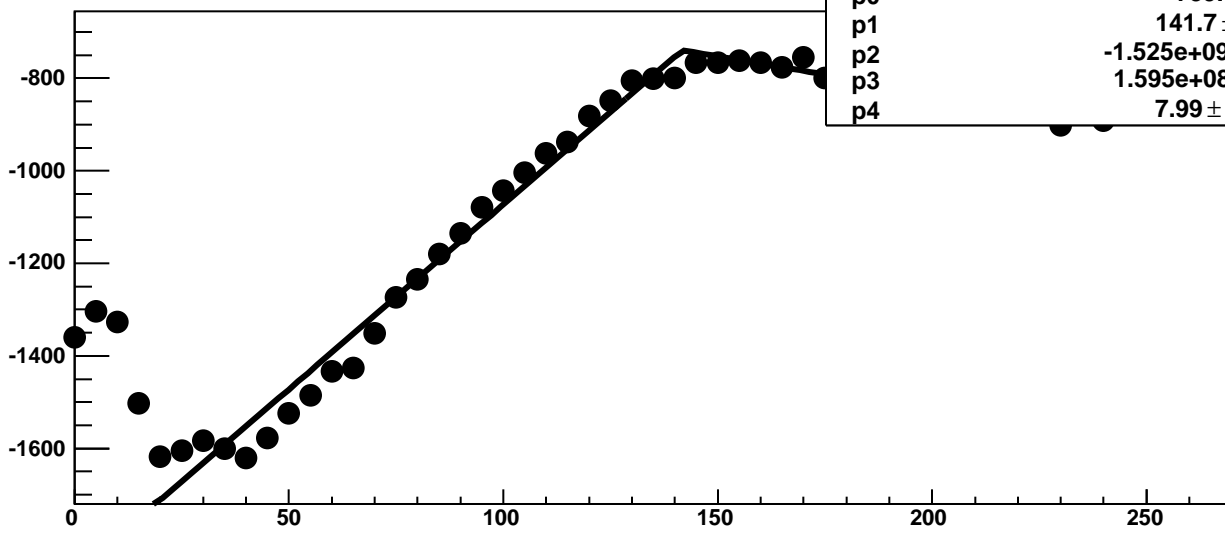


Chip 11, Channel 14, Enable 1, DAC=1600, ADC Residuals vs Hold



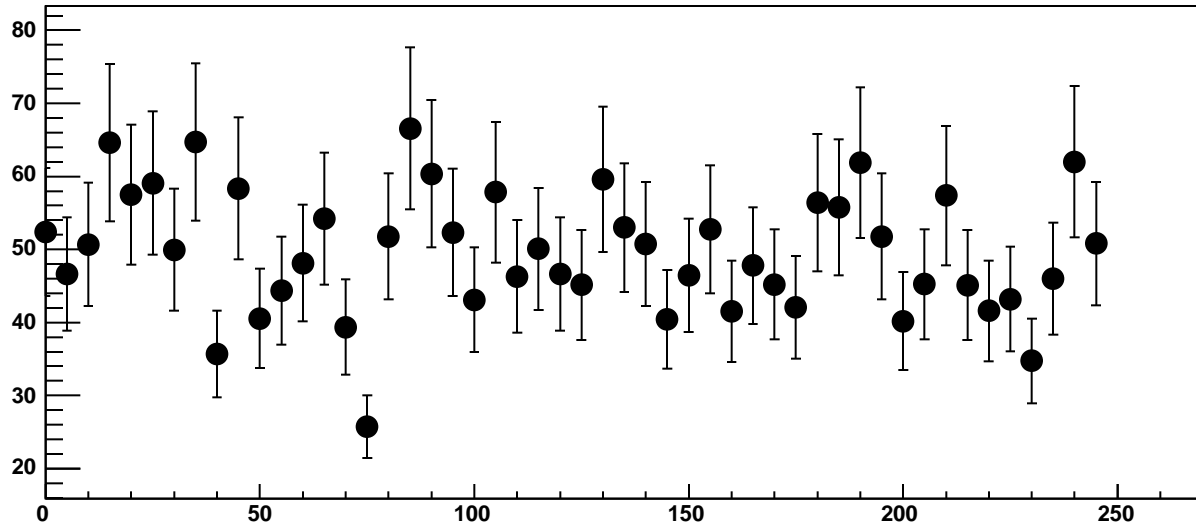


Chip 11, Channel 14, Enable 2, DAC=1600, ADC Mean vs Hold

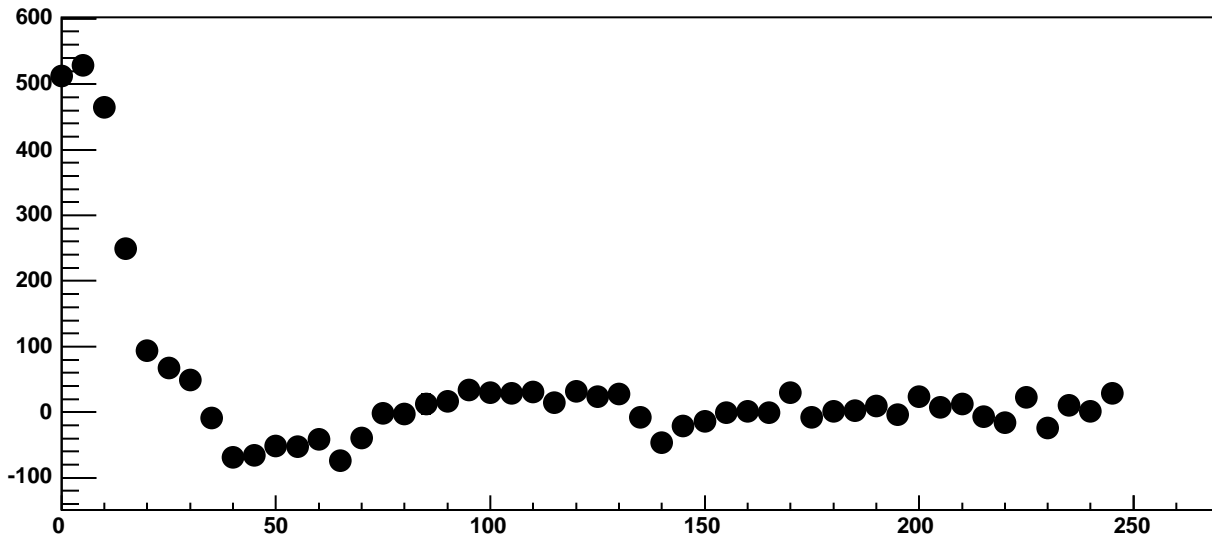


$\chi^2 / \text{ndf}$	709.7 / 41
p0	-739.3 ± 1.22
p1	141.7 ± 0.4707
p2	-1.525e+09 ± 1.414
p3	1.595e+08 ± 1.414
p4	7.99 ± 0.03975

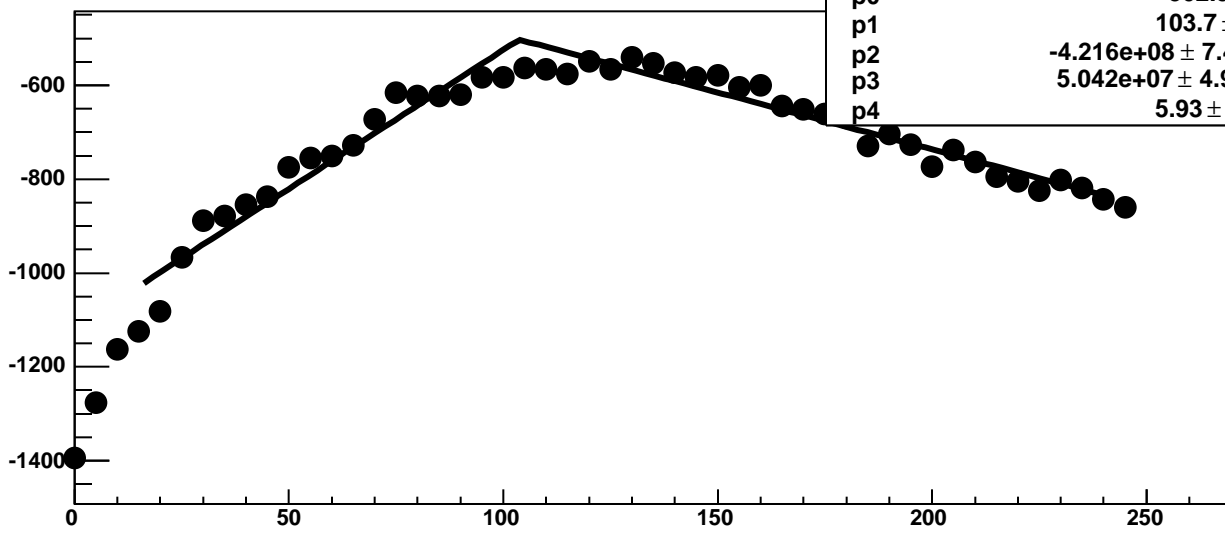
Chip 11, Channel 14, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 14, Enable 2, DAC=1600, ADC Residuals vs Hold

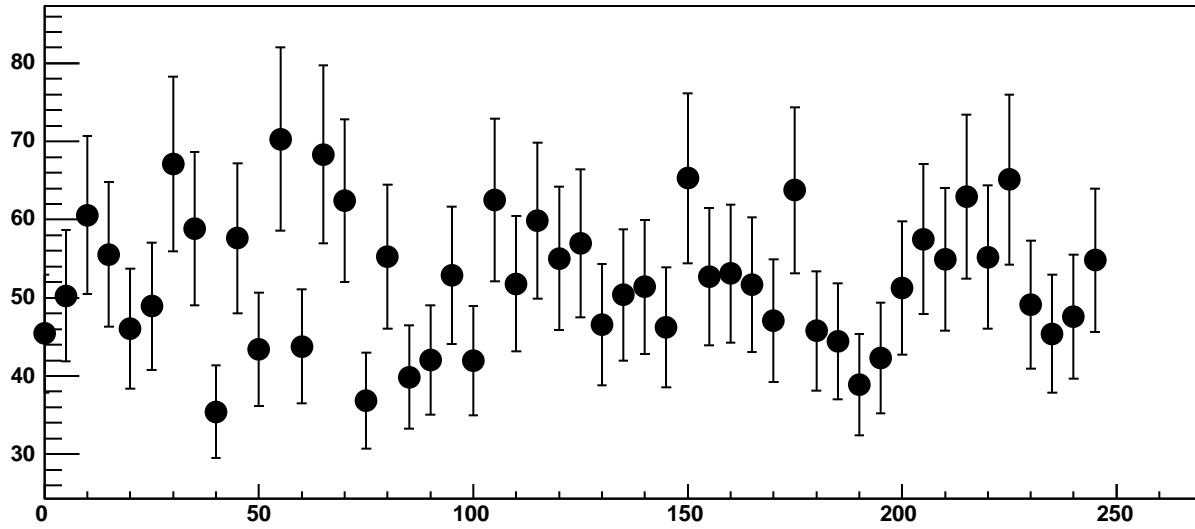


Chip 11, Channel 14, Enable 3, DAC=1600, ADC Mean vs Hold

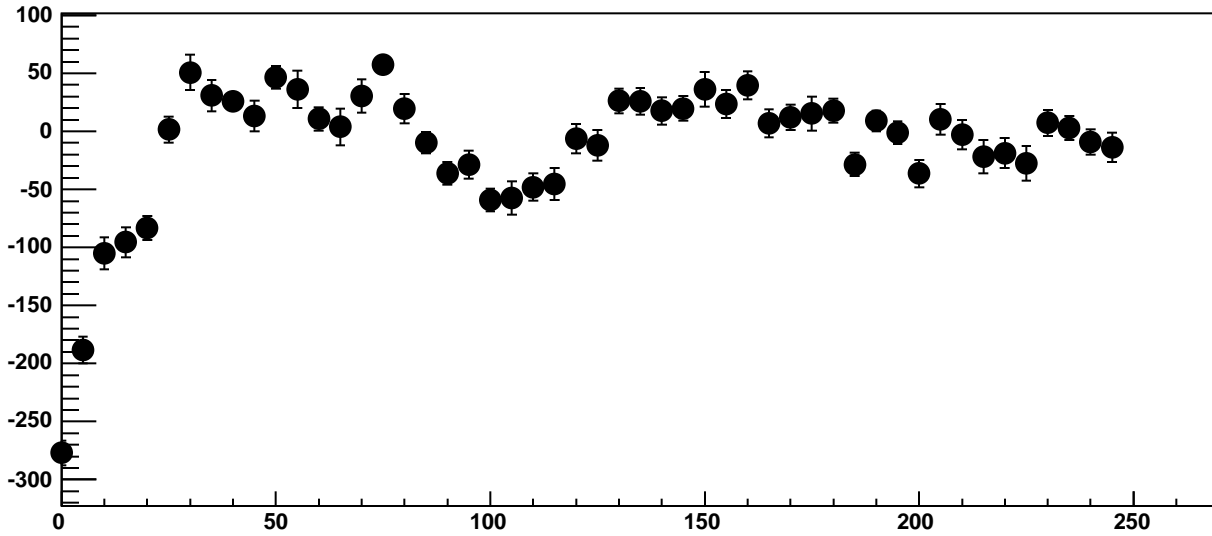


$\chi^2 / \text{ndf}$	400 / 41
p0	$-502.5 \pm 3.589$
p1	$103.7 \pm 0.8228$
p2	$-4.216\text{e}+08 \pm 7.496\text{e}+06$
p3	$5.042\text{e}+07 \pm 4.927\text{e}+05$
p4	$5.93 \pm 0.09985$

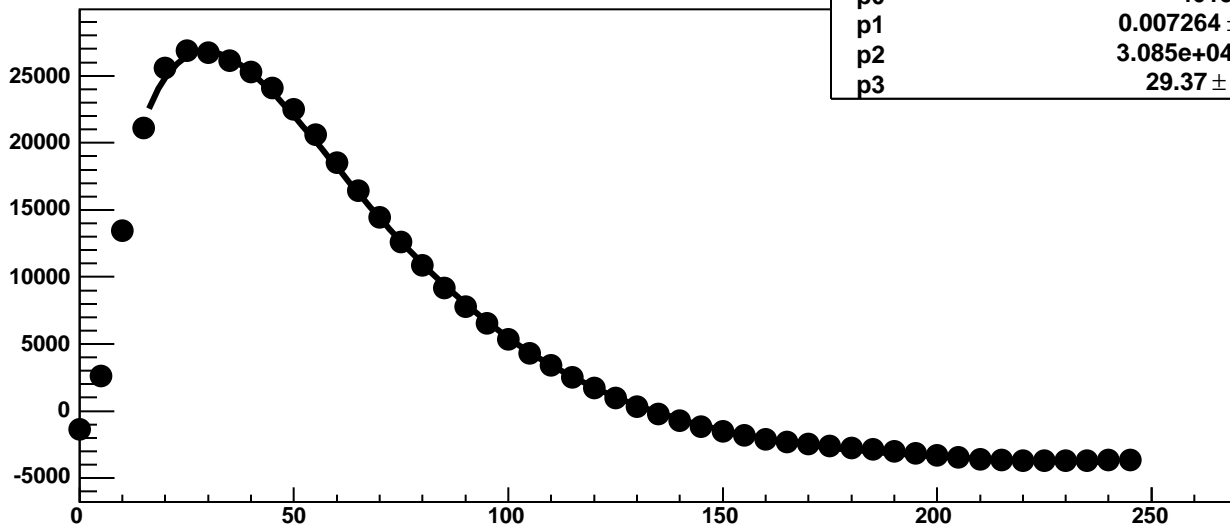
Chip 11, Channel 14, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 14, Enable 3, DAC=1600, ADC Residuals vs Hold

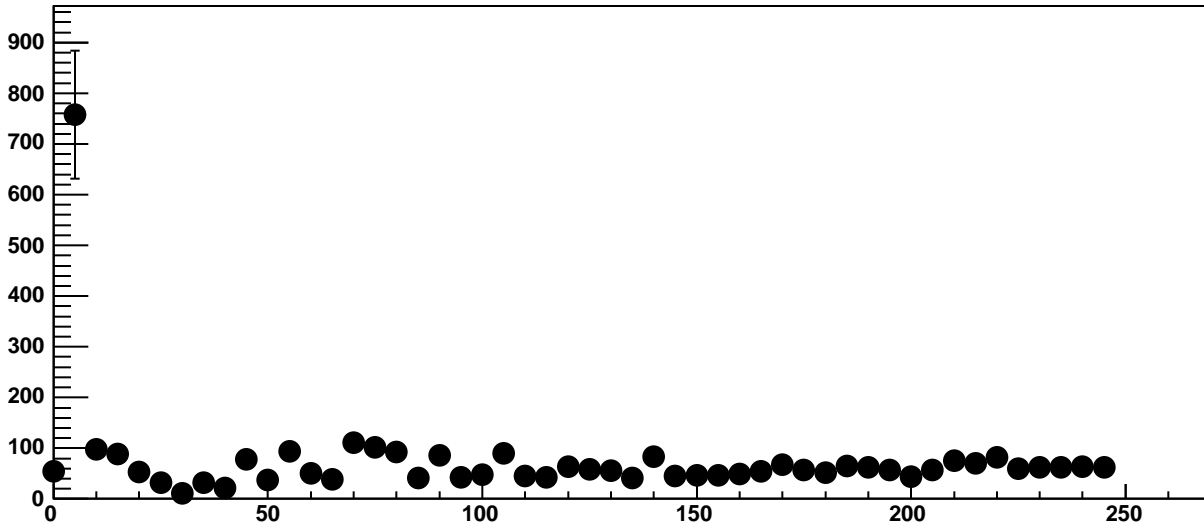


Chip 11, Channel 14, Enable 4!, DAC=1600, ADC Mean vs Hold

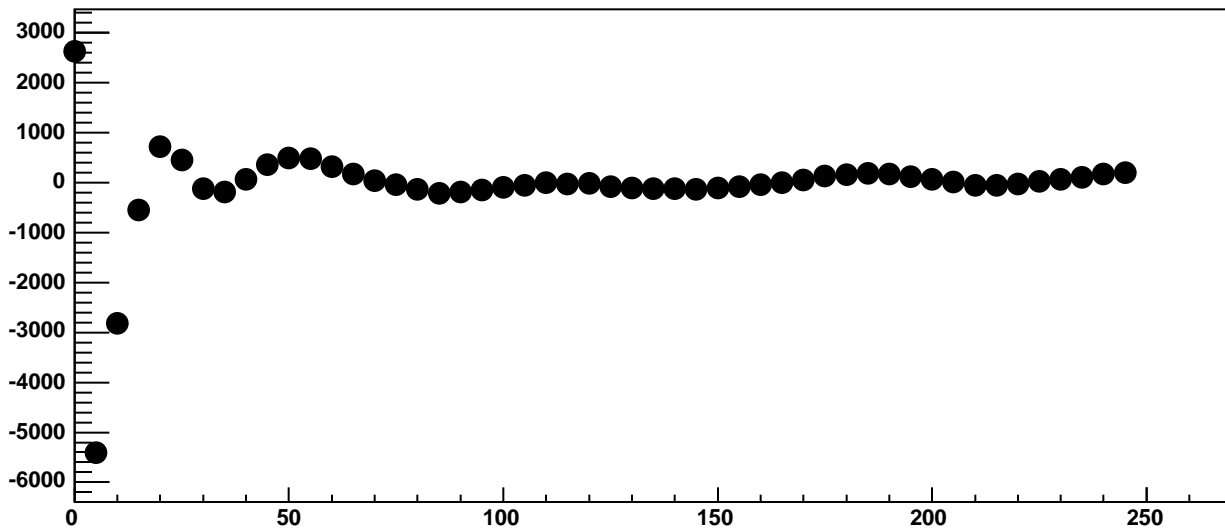


$\chi^2 / \text{ndf}$	1.853e+04 / 42
p0	-4015 ± 3.799
p1	0.007264 ± 0.0182
p2	3.085e+04 ± 4.165
p3	29.37 ± 0.01033

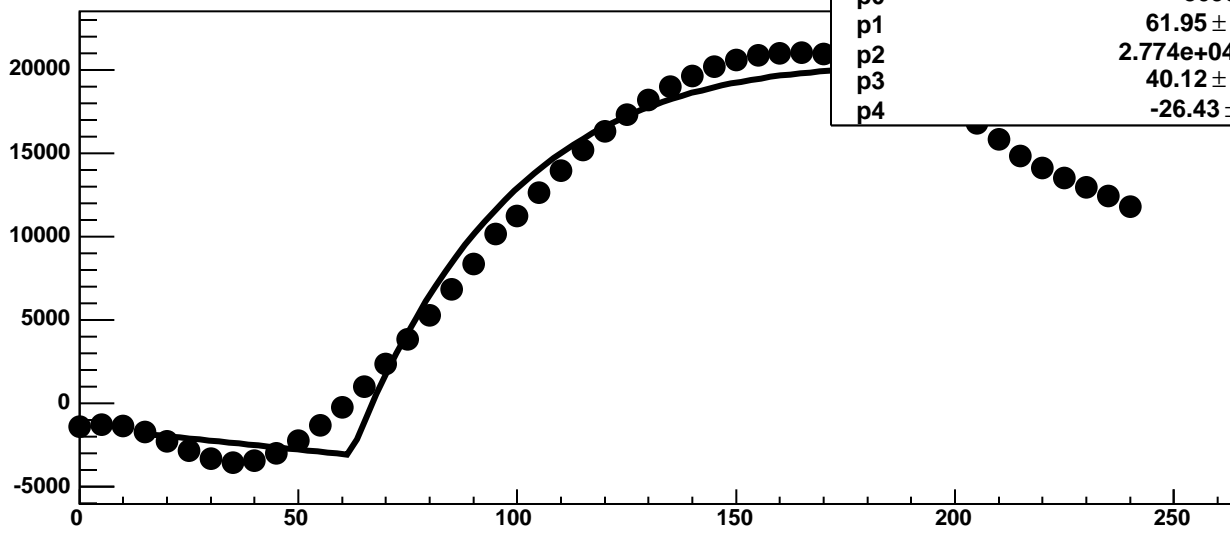
Chip 11, Channel 14, Enable 4!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 14, Enable 4!, DAC=1600, ADC Residuals vs Hold

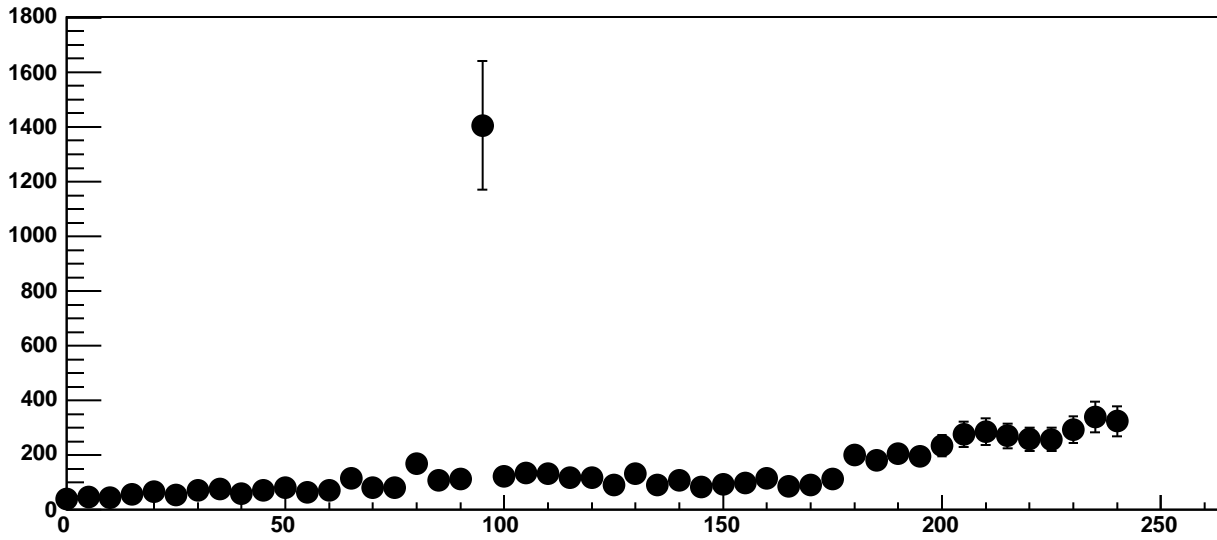


Chip 11, Channel 14, Enable 5, DAC=1600, ADC Mean vs Hold

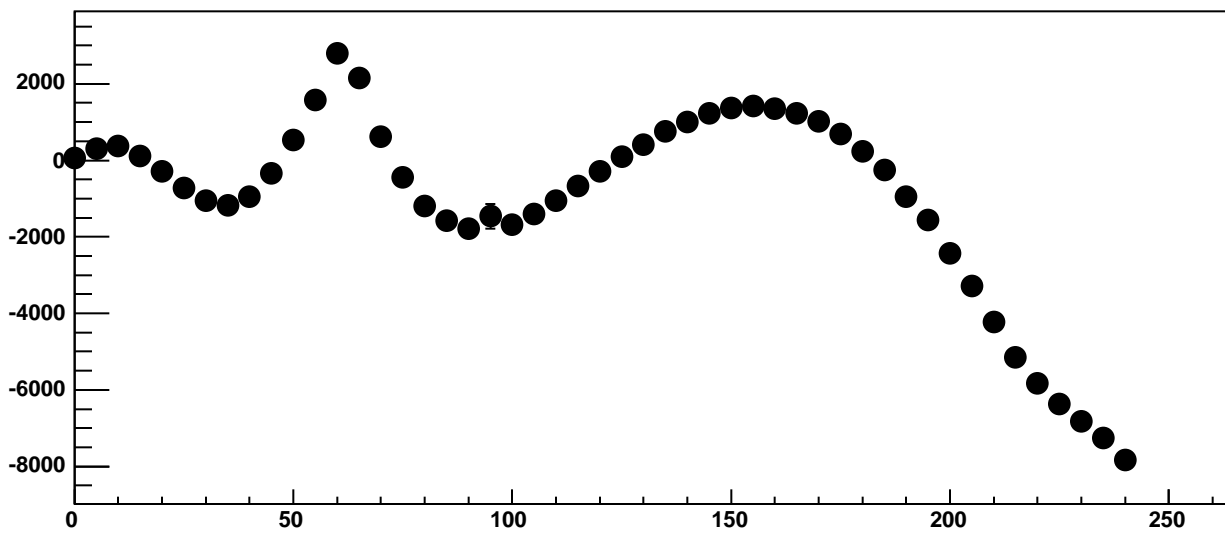


$\chi^2 / \text{ndf}$	1.776e+05 / 41
p0	-3090 ± 8.121
p1	61.95 ± 0.02882
p2	2.774e+04 ± 46.61
p3	40.12 ± 0.08627
p4	-26.43 ± 0.2636

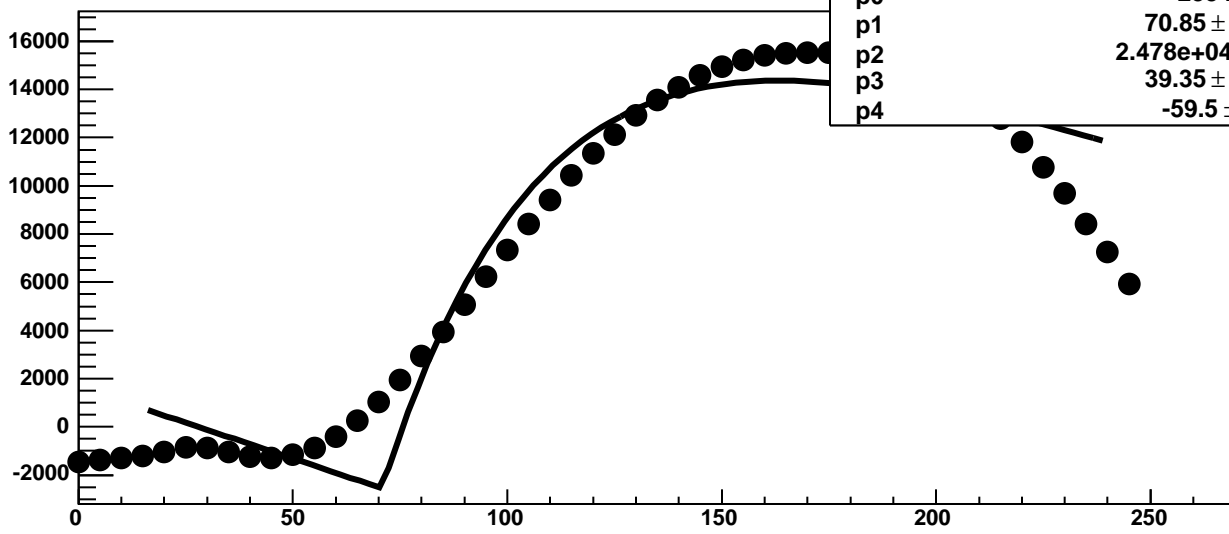
Chip 11, Channel 14, Enable 5, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 14, Enable 5, DAC=1600, ADC Residuals vs Hold

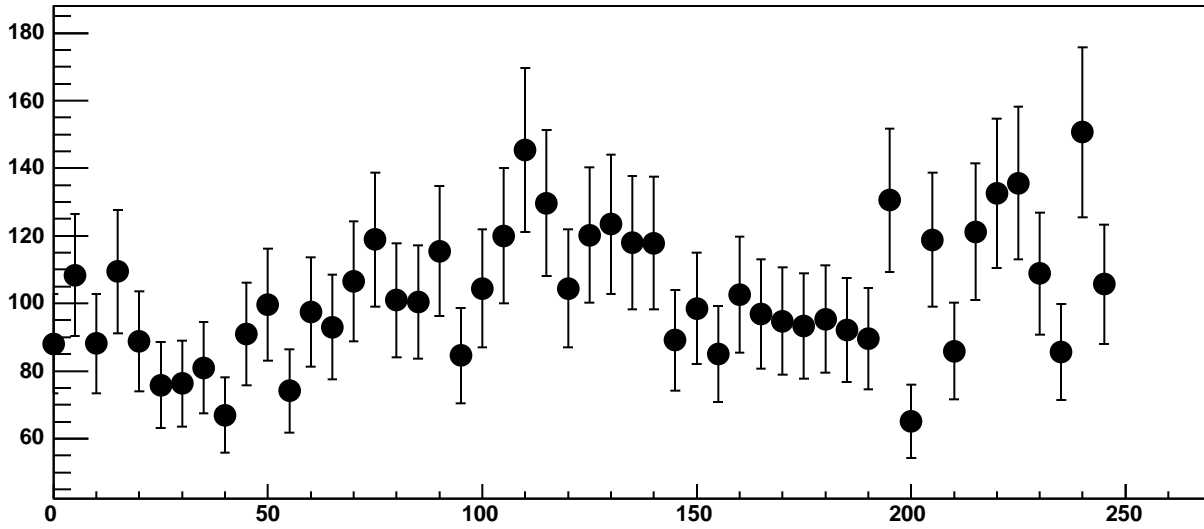


Chip 11, Channel 15, Enable 0, DAC=1600, ADC Mean vs Hold

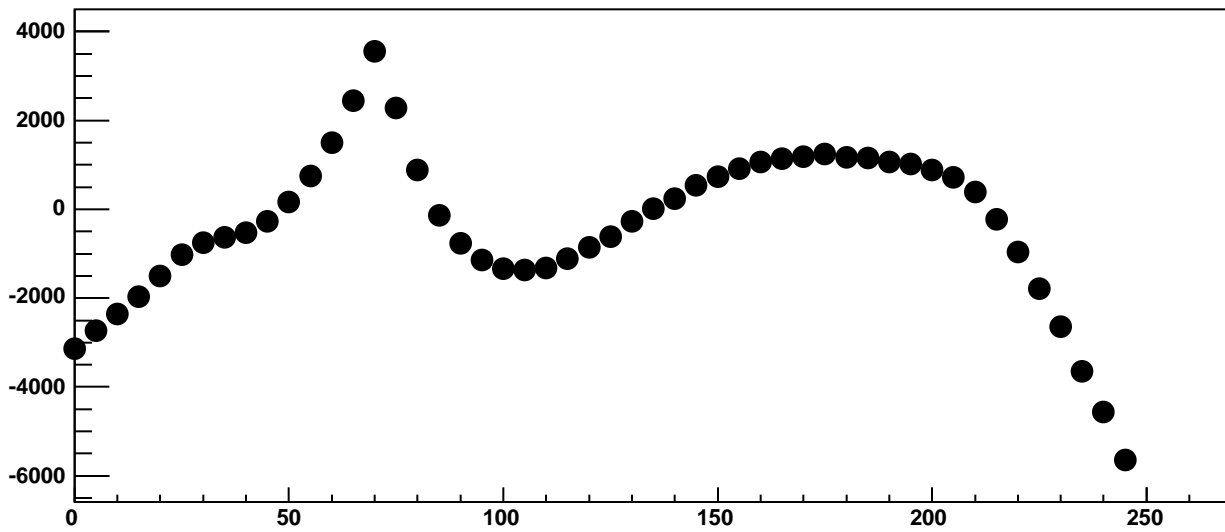


$\chi^2 / \text{ndf}$	1.8e+05 / 41
p0	-2554 ± 8.197
p1	70.85 ± 0.03565
p2	2.478e+04 ± 44.16
p3	39.35 ± 0.08756
p4	-59.5 ± 0.2346

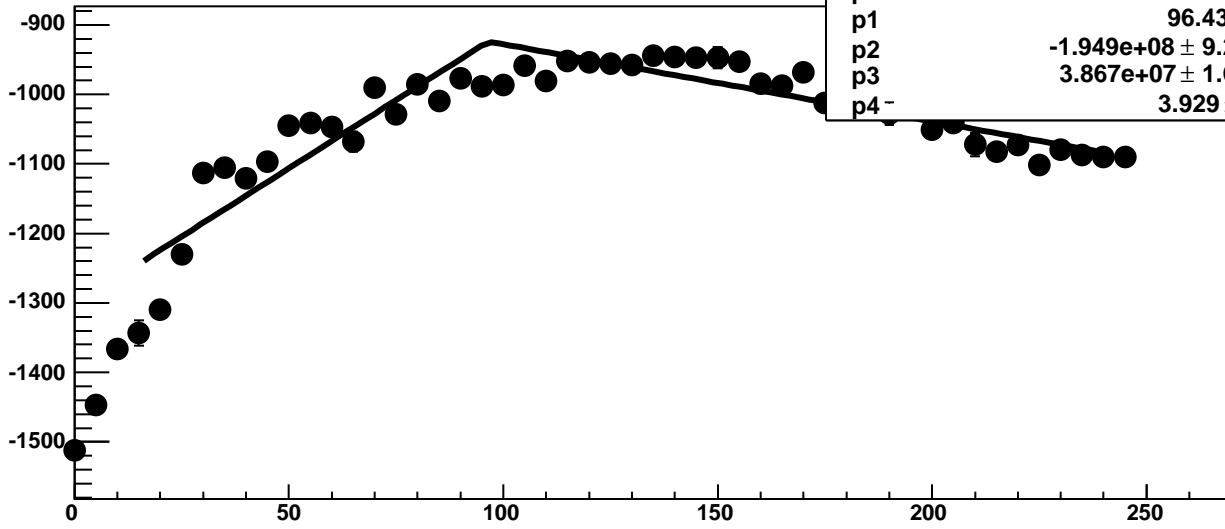
Chip 11, Channel 15, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 15, Enable 0, DAC=1600, ADC Residuals vs Hold

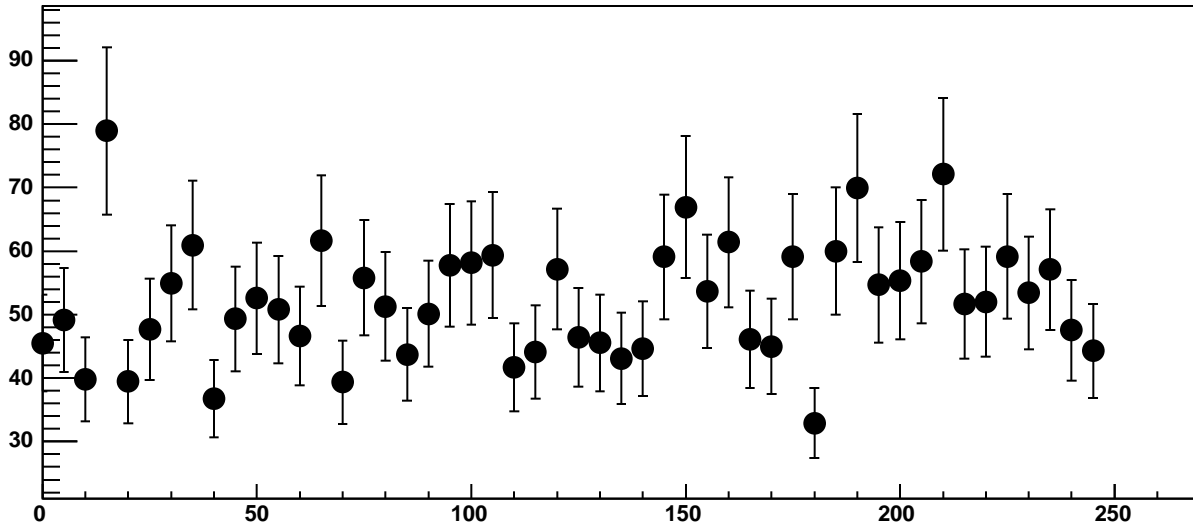


Chip 11, Channel 15, Enable 1, DAC=1600, ADC Mean vs Hold

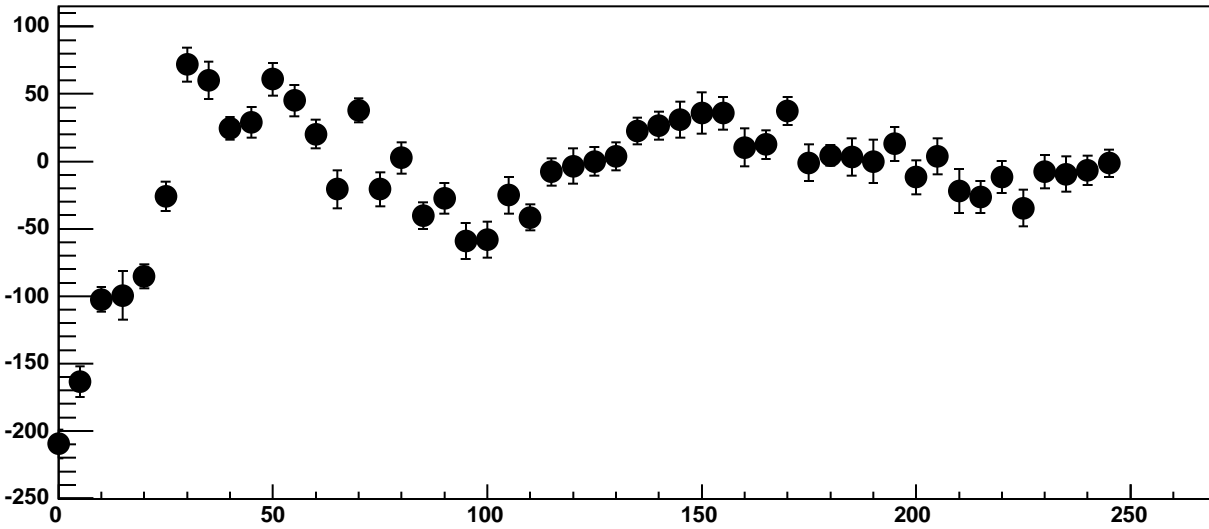


$\chi^2 / \text{ndf}$	405.4 / 41
p0	$-923.8 \pm 3.574$
p1	$96.43 \pm 1.397$
p2	$-1.949\text{e}+08 \pm 9.238\text{e}+06$
p3	$3.867\text{e}+07 \pm 1.634\text{e}+06$
p4	$3.929 \pm 0.1151$

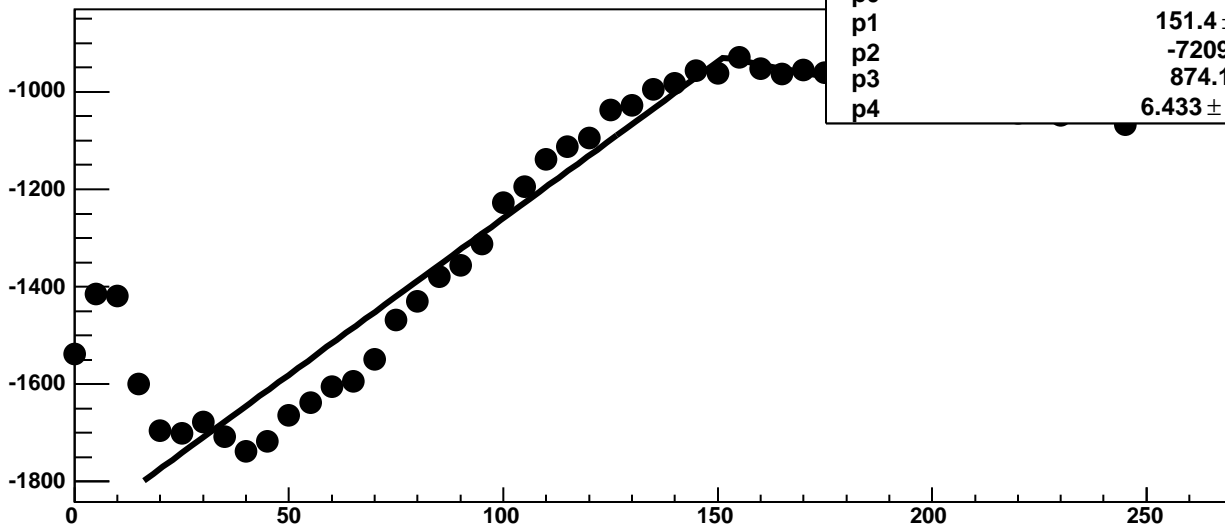
Chip 11, Channel 15, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 15, Enable 1, DAC=1600, ADC Residuals vs Hold

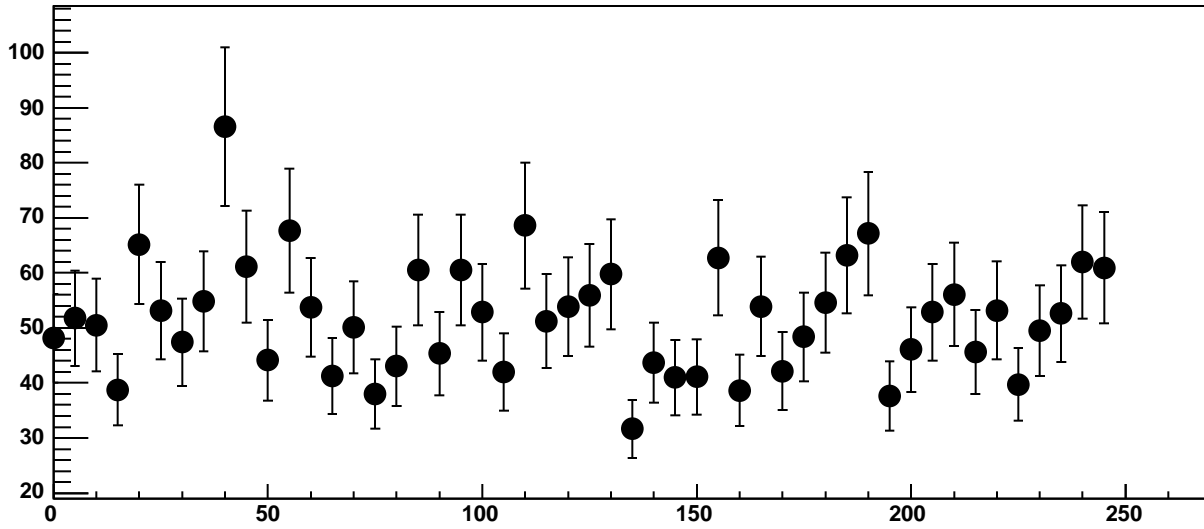


Chip 11, Channel 15, Enable 2, DAC=1600, ADC Mean vs Hold

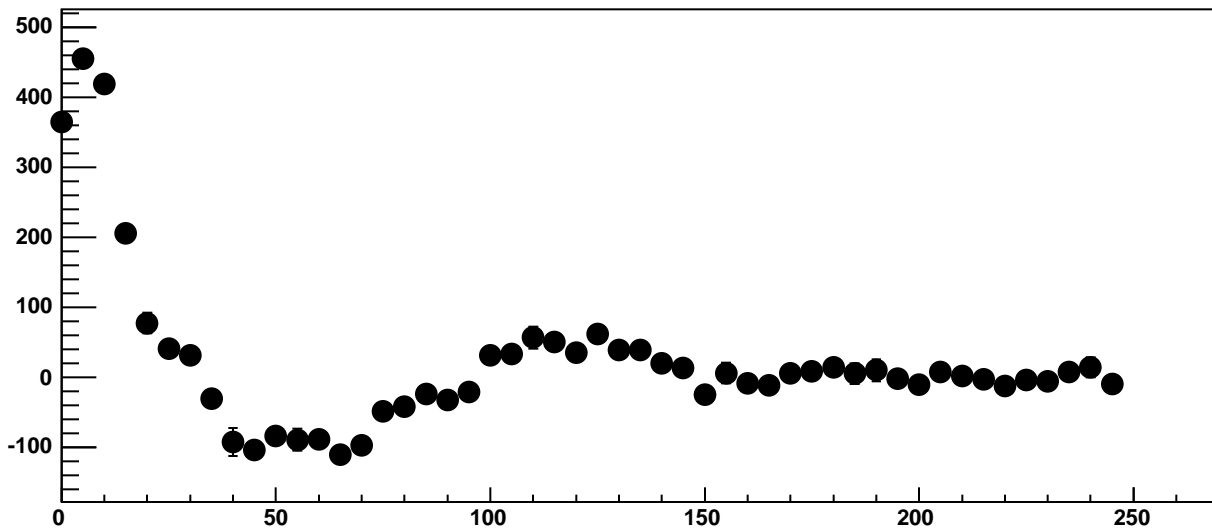


$\chi^2 / \text{ndf}$	1228 / 41
p0	$-928.4 \pm 4.569$
p1	$151.4 \pm 0.8358$
p2	$-7209 \pm 1738$
p3	$874.1 \pm 221.7$
p4	$6.433 \pm 0.05028$

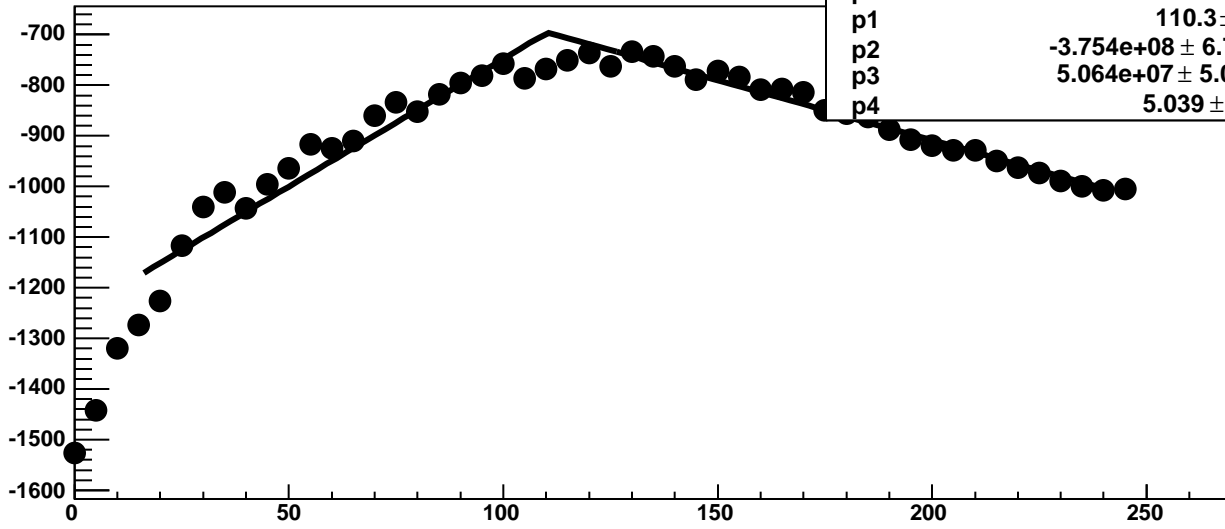
Chip 11, Channel 15, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 15, Enable 2, DAC=1600, ADC Residuals vs Hold

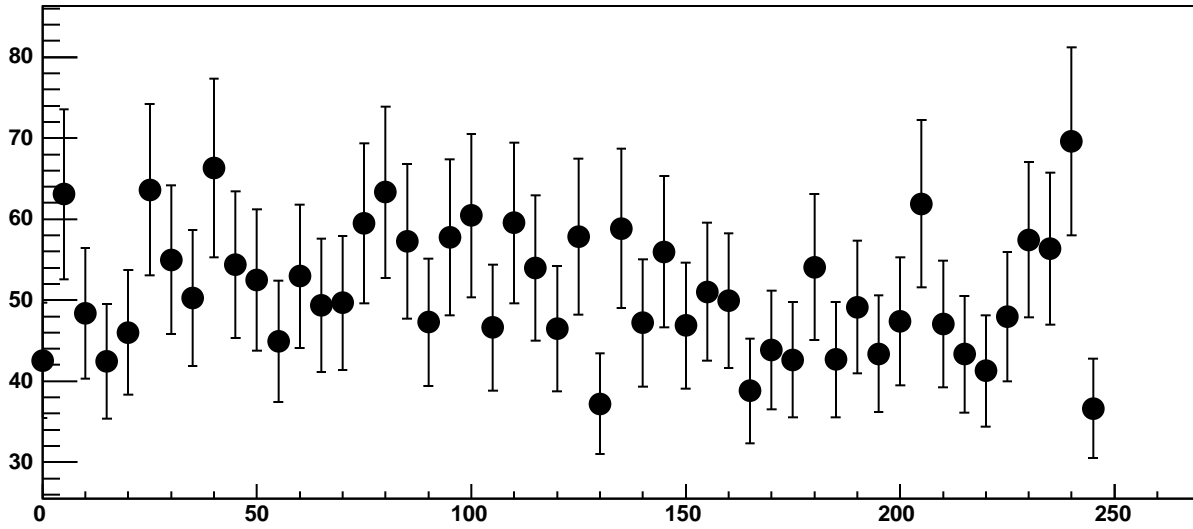


Chip 11, Channel 15, Enable 3, DAC=1600, ADC Mean vs Hold

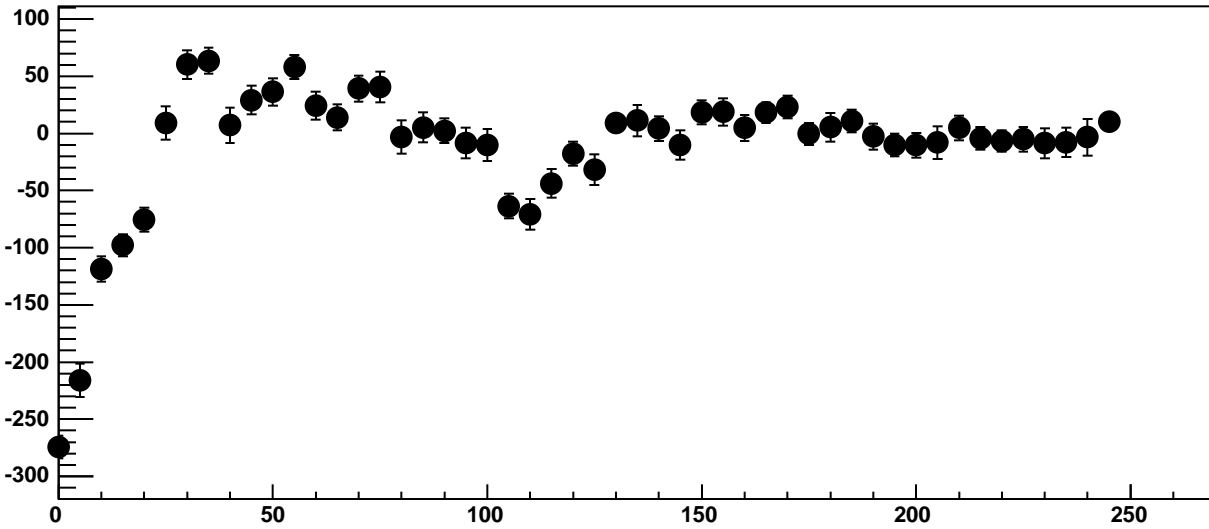


$\chi^2 / \text{ndf}$	386.3 / 41
p0	$-695.9 \pm 3.531$
p1	$110.3 \pm 0.9446$
p2	$-3.754e+08 \pm 6.742e+06$
p3	$5.064e+07 \pm 5.061e+05$
p4	$5.039 \pm 0.09221$

Chip 11, Channel 15, Enable 3, DAC=1600, ADC Noise vs Hold

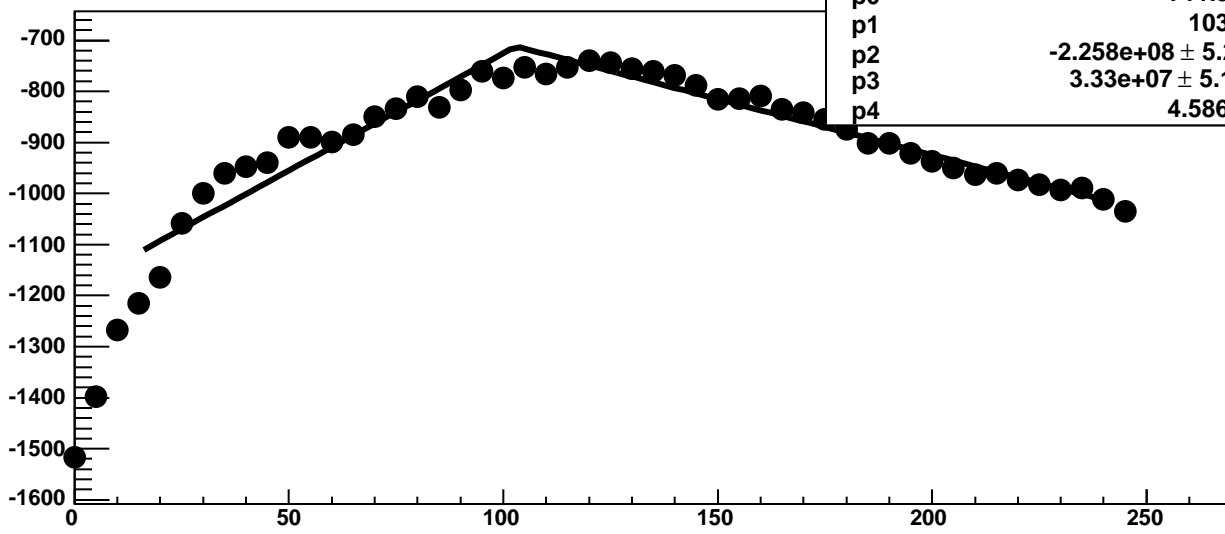


Chip 11, Channel 15, Enable 3, DAC=1600, ADC Residuals vs Hold



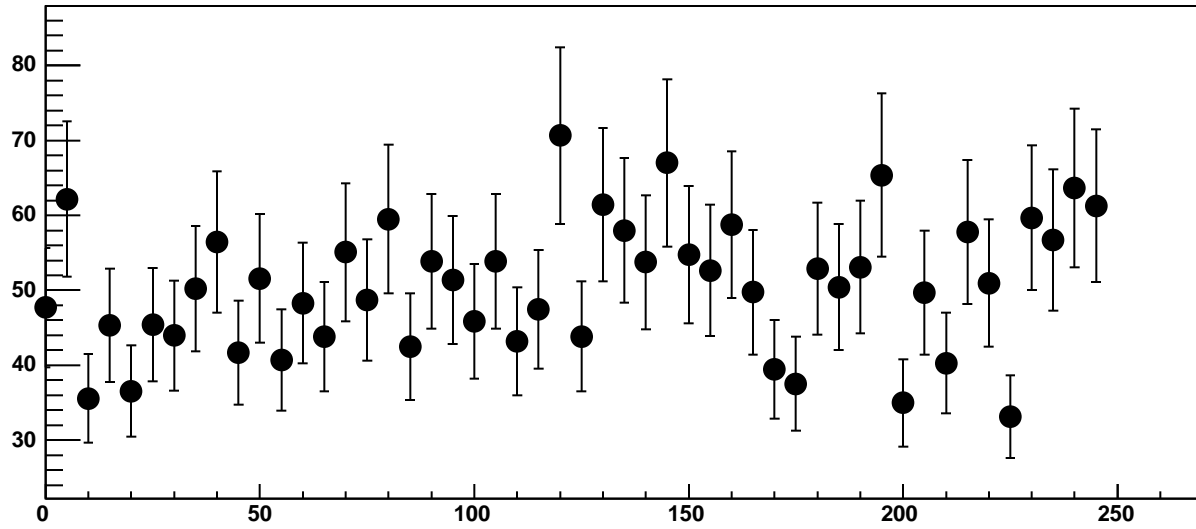


Chip 11, Channel 15, Enable 4, DAC=1600, ADC Mean vs Hold

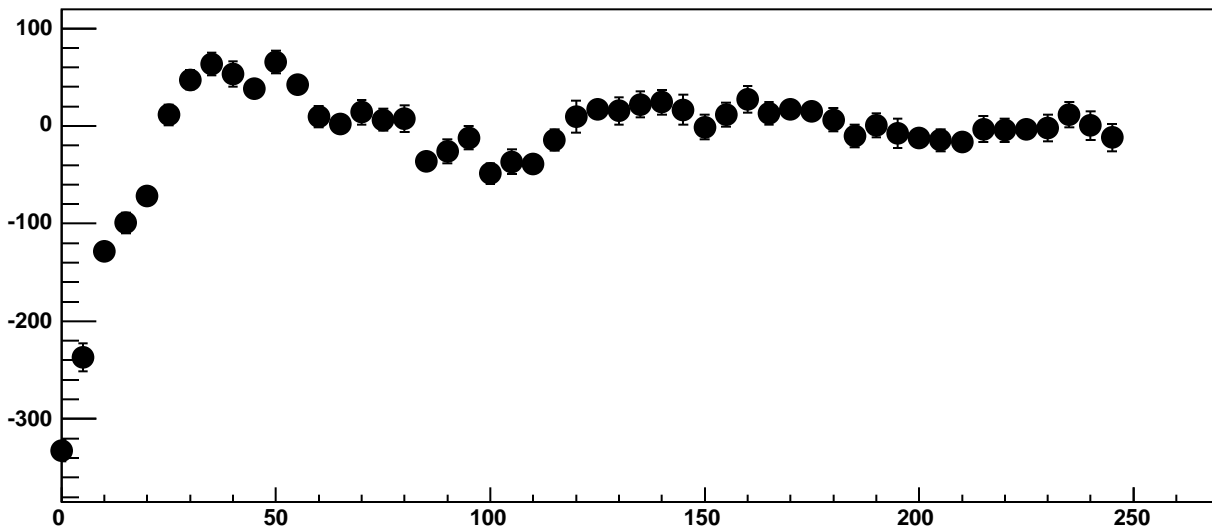


$\chi^2 / \text{ndf}$	406.3 / 41
p0	-711.9 ± 3.467
p1	103 ± 1.016
p2	-2.258e+08 ± 5.222e+06
p3	3.33e+07 ± 5.108e+05
p4	4.586 ± 0.096

Chip 11, Channel 15, Enable 4, DAC=1600, ADC Noise vs Hold

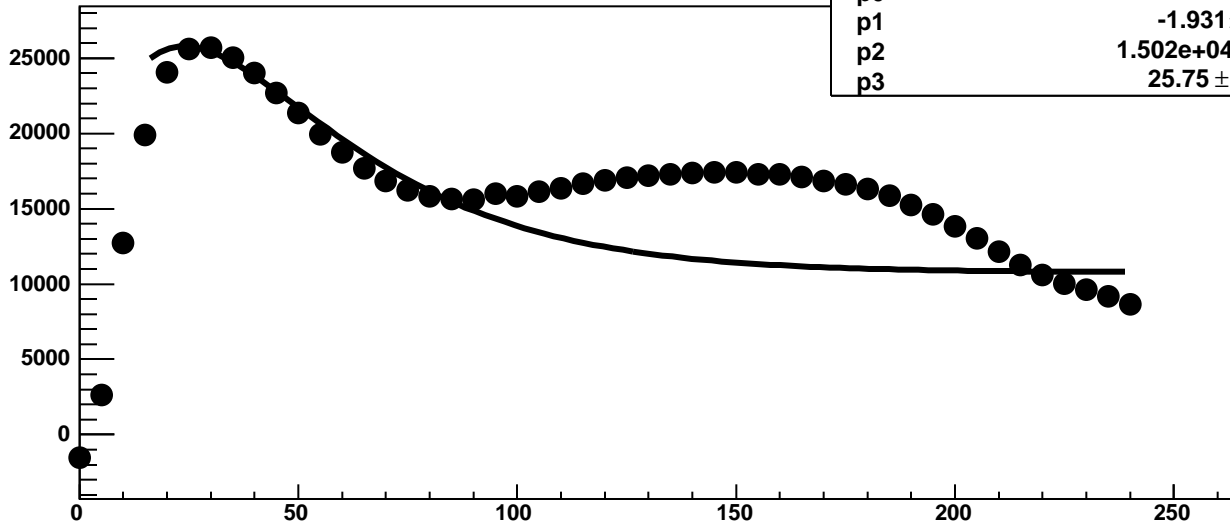


Chip 11, Channel 15, Enable 4, DAC=1600, ADC Residuals vs Hold

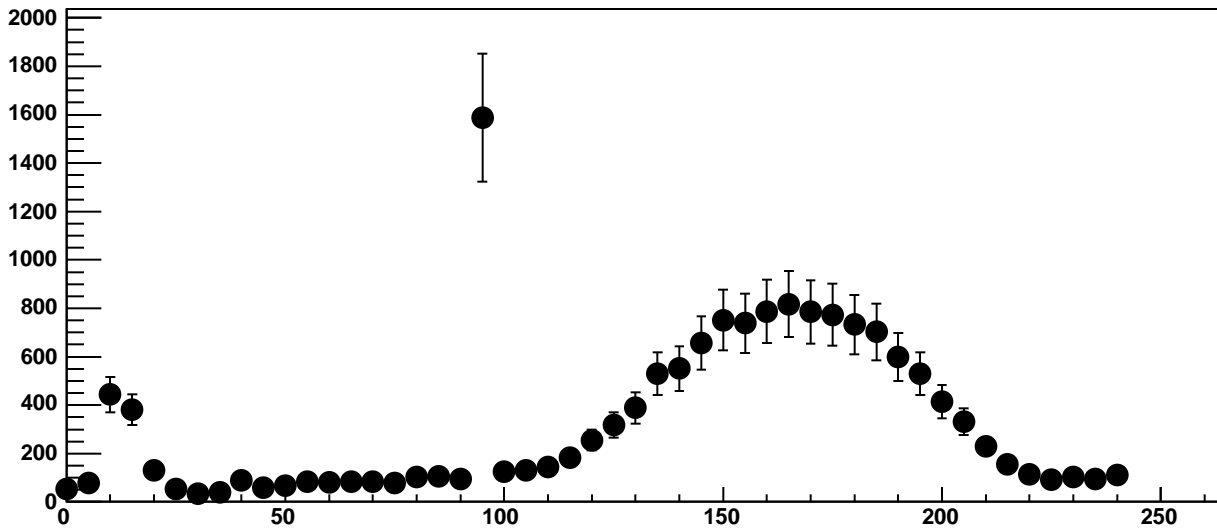


Chip 11, Channel 15, Enable 5!, DAC=1600, ADC Mean vs Hold

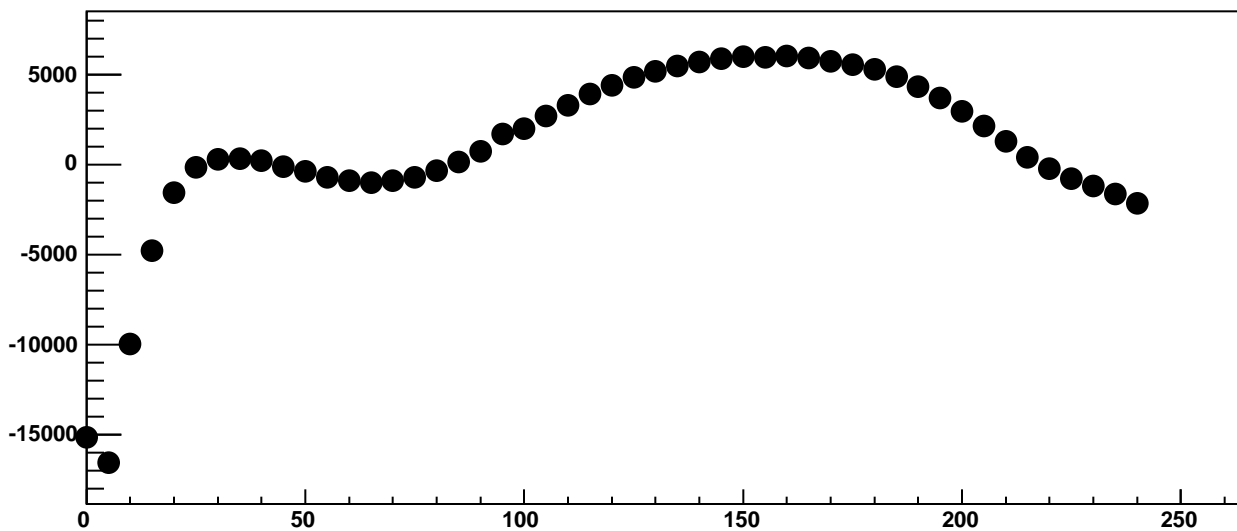
$\chi^2 / \text{ndf}$	1.008e+05 / 42
p0	1.077e+04 $\pm$ 11.18
p1	-1.931 $\pm$ 0.1641
p2	1.502e+04 $\pm$ 17.12
p3	25.75 $\pm$ 0.07171



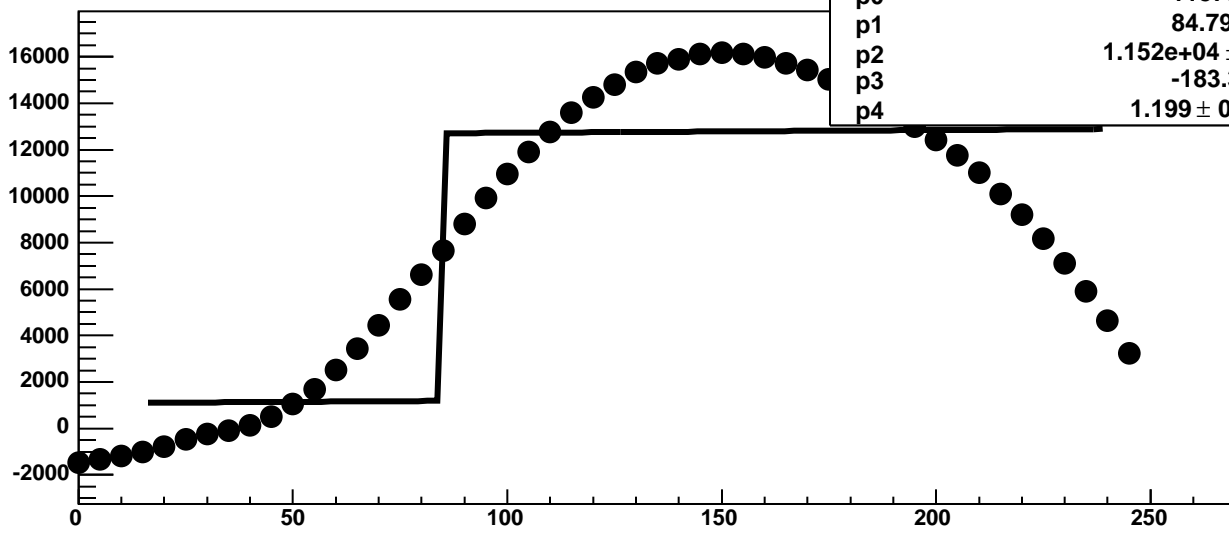
Chip 11, Channel 15, Enable 5!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 15, Enable 5!, DAC=1600, ADC Residuals vs Hold

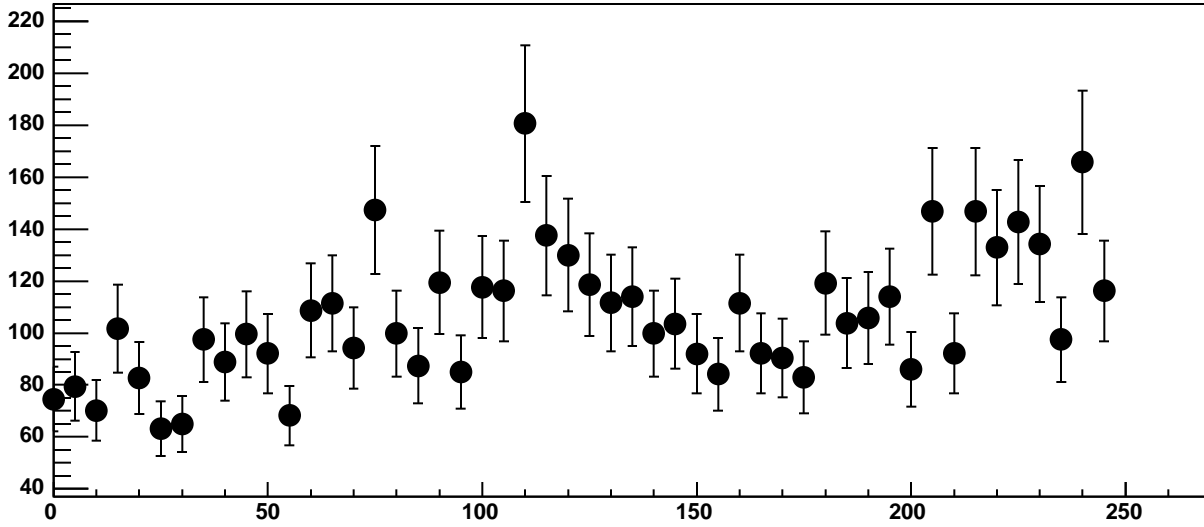


Chip 11, Channel 16, Enable 0, DAC=1600, ADC Mean vs Hold

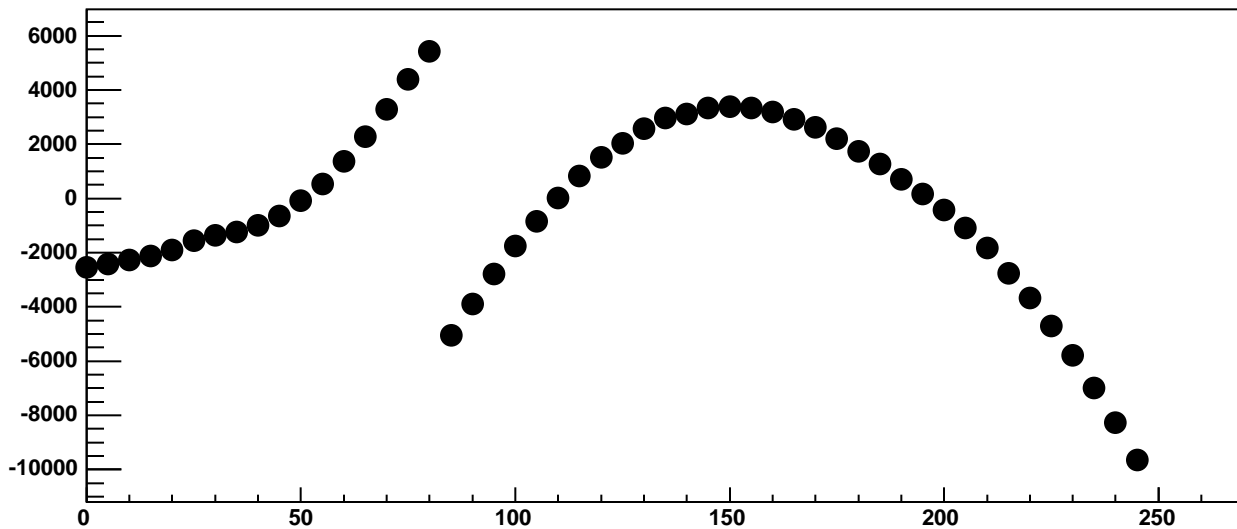


$\chi^2 / \text{ndf}$	6.908e+05 / 41
p0	1187 ± 0.5521
p1	84.79 ± 10.15
p2	1.152e+04 ± 0.7343
p3	-183.3 ± 1.03
p4	1.199 ± 0.007926

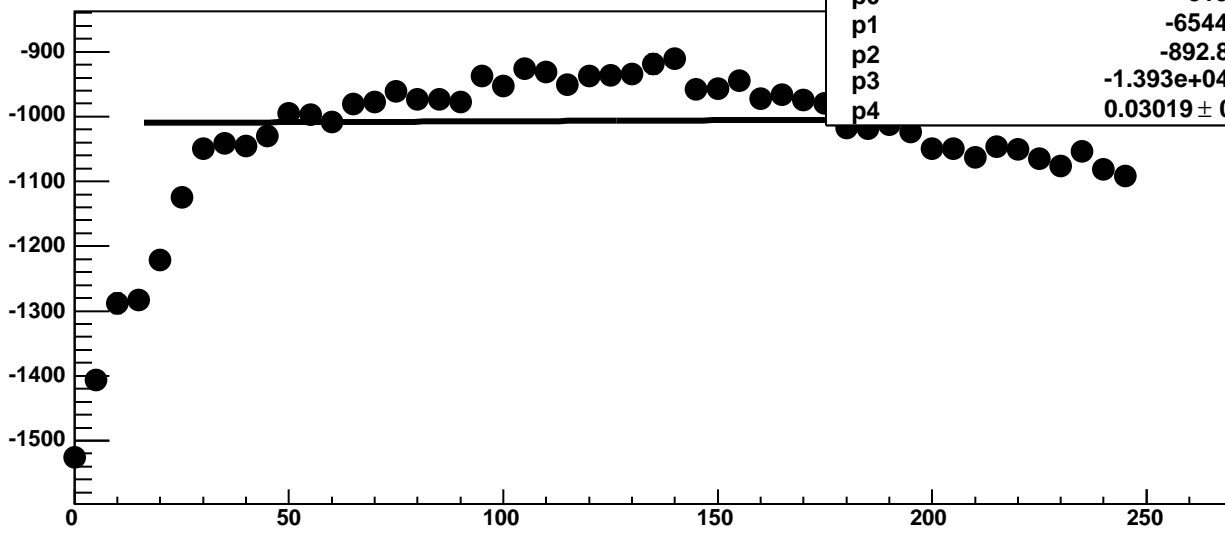
Chip 11, Channel 16, Enable 0, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 16, Enable 0, DAC=1600, ADC Residuals vs Hold

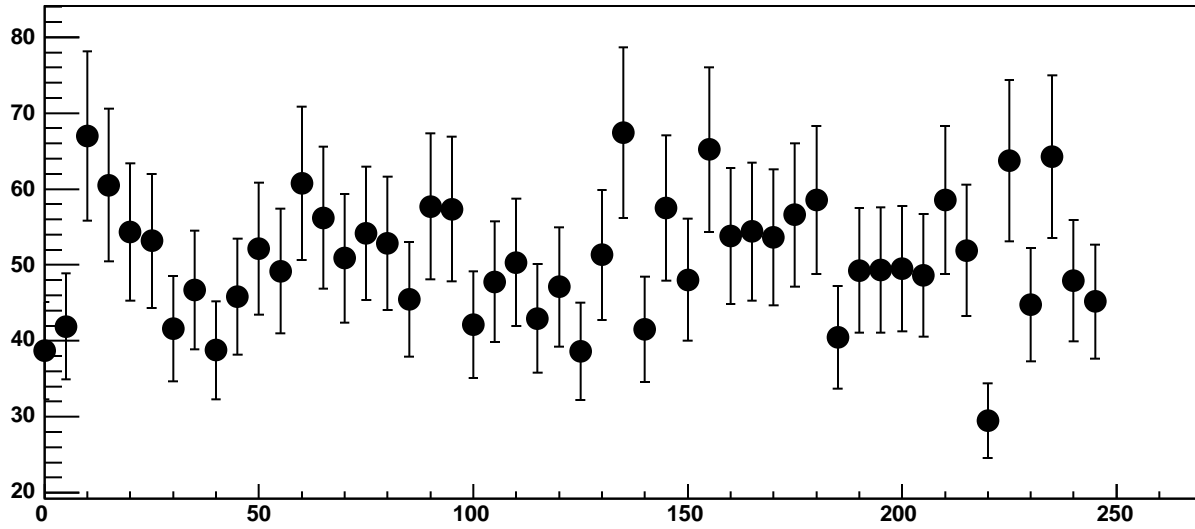


Chip 11, Channel 16, Enable 1, DAC=1600, ADC Mean vs Hold

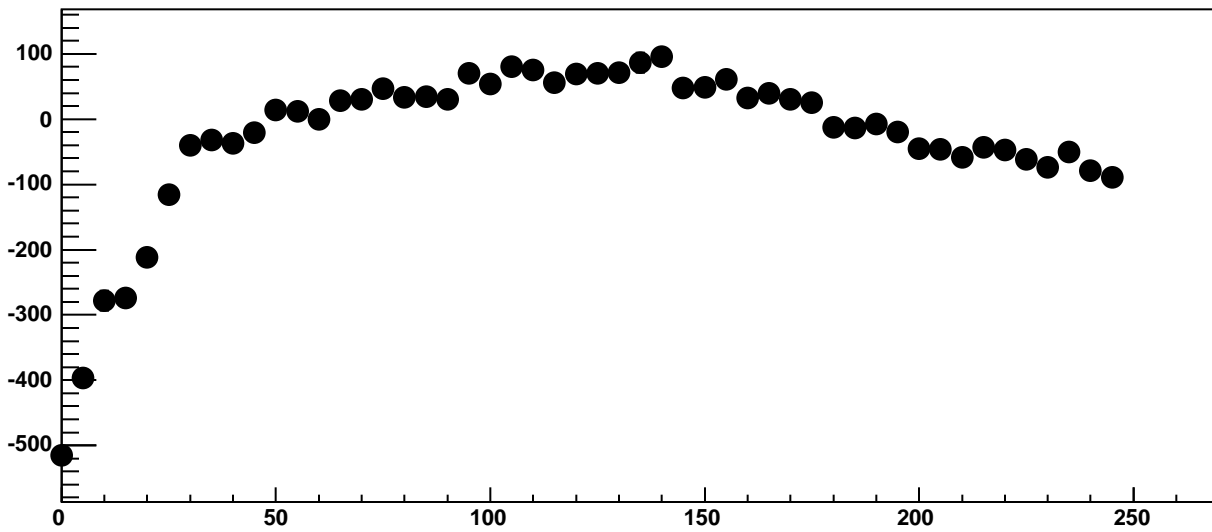


$\chi^2 / \text{ndf}$	1656 / 41
p0	$-315 \pm 9.749$
p1	$-6544 \pm 130.6$
p2	$-892.8 \pm 10.96$
p3	$-1.393\text{e}+04 \pm 2966$
p4	$0.03019 \pm 0.001461$

Chip 11, Channel 16, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 16, Enable 1, DAC=1600, ADC Residuals vs Hold



Chip 11, Channel 16, Enable 2!, DAC=1600, ADC Mean vs Hold

$\chi^2 / \text{ndf}$

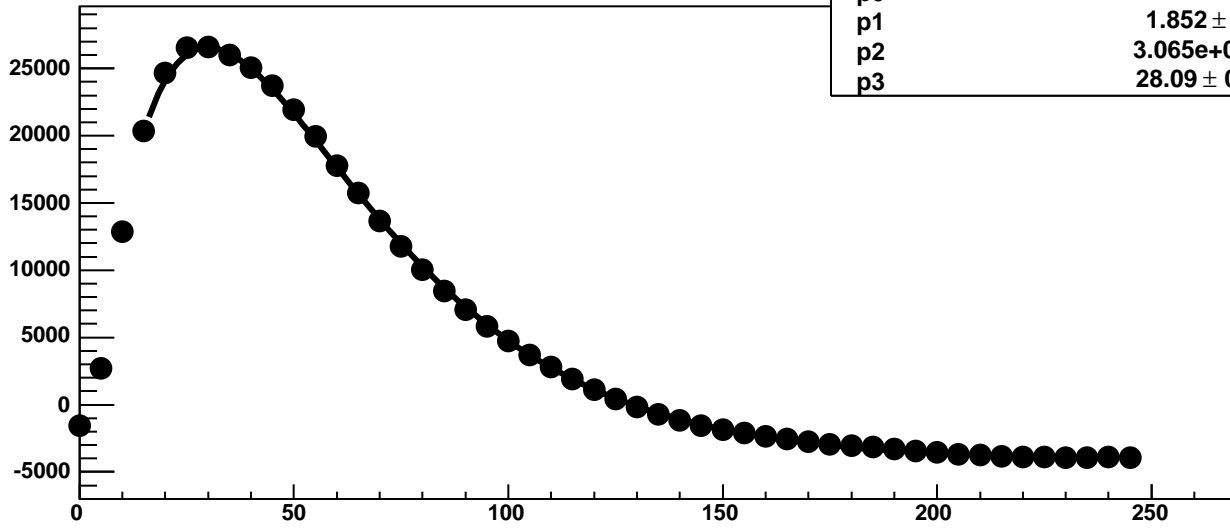
6310 / 42

p0 -4085 ± 3.404

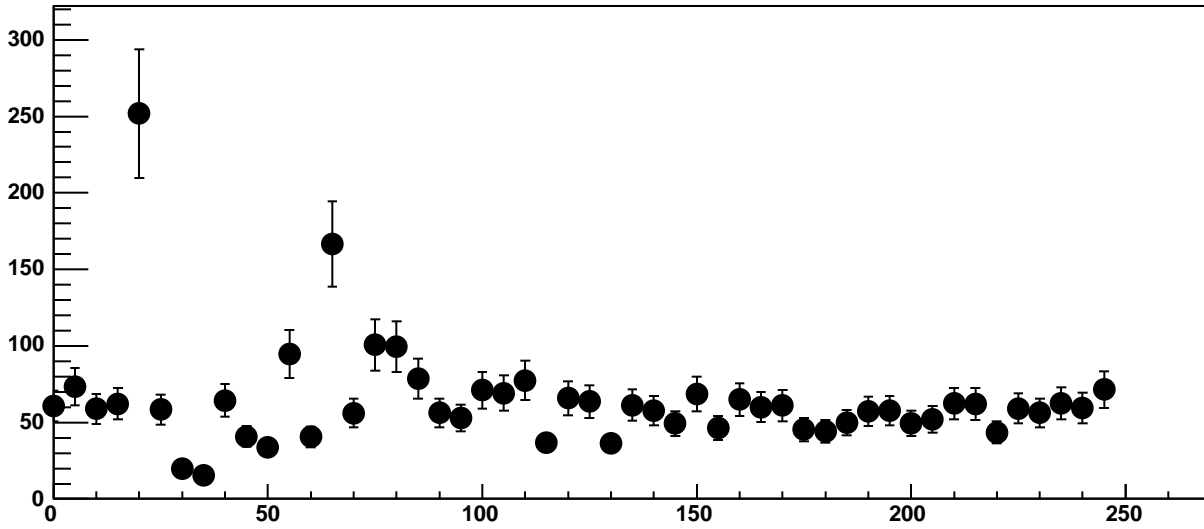
p1 1.852 ± 0.01509

p2 3.065e+04 ± 4.1

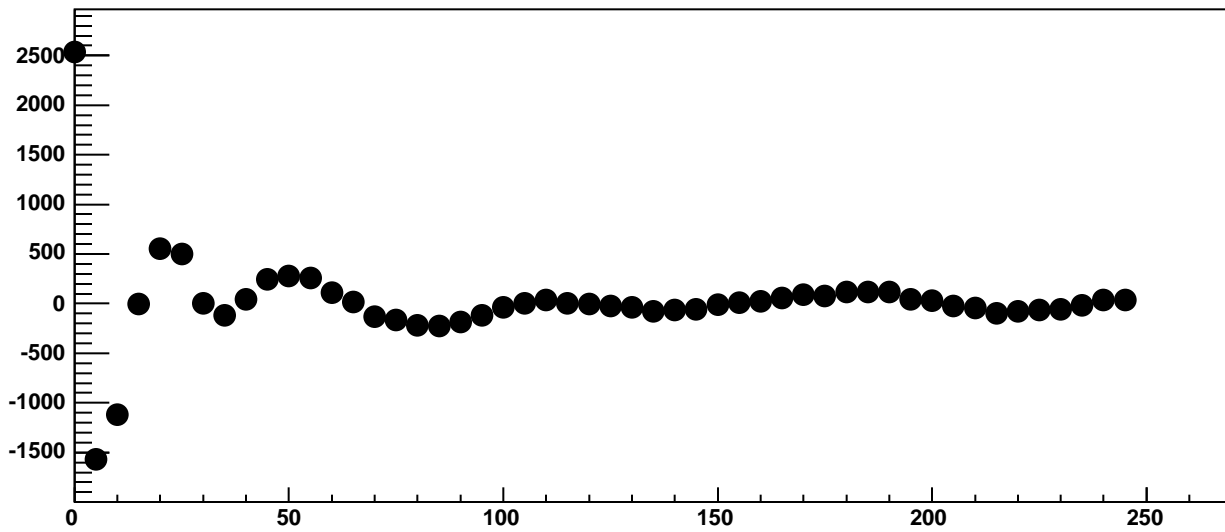
p3 28.09 ± 0.009231



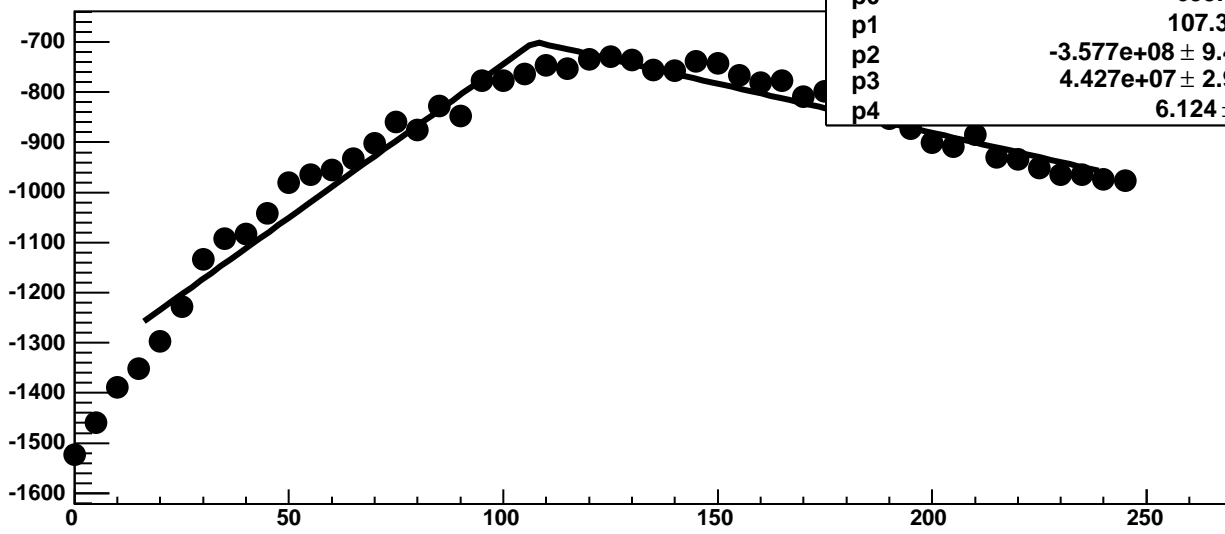
Chip 11, Channel 16, Enable 2!, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 16, Enable 2!, DAC=1600, ADC Residuals vs Hold

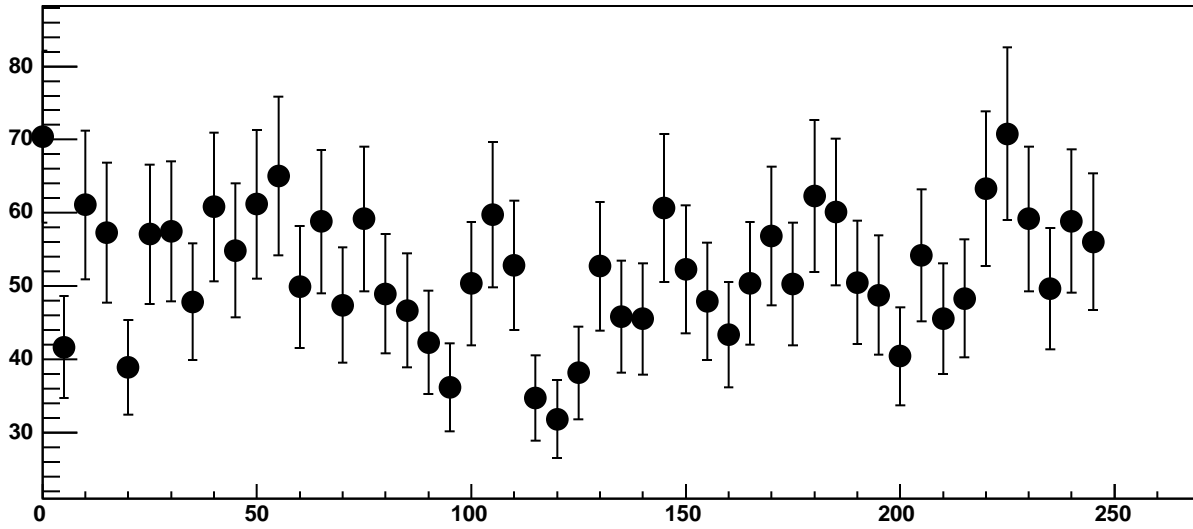


Chip 11, Channel 16, Enable 3, DAC=1600, ADC Mean vs Hold

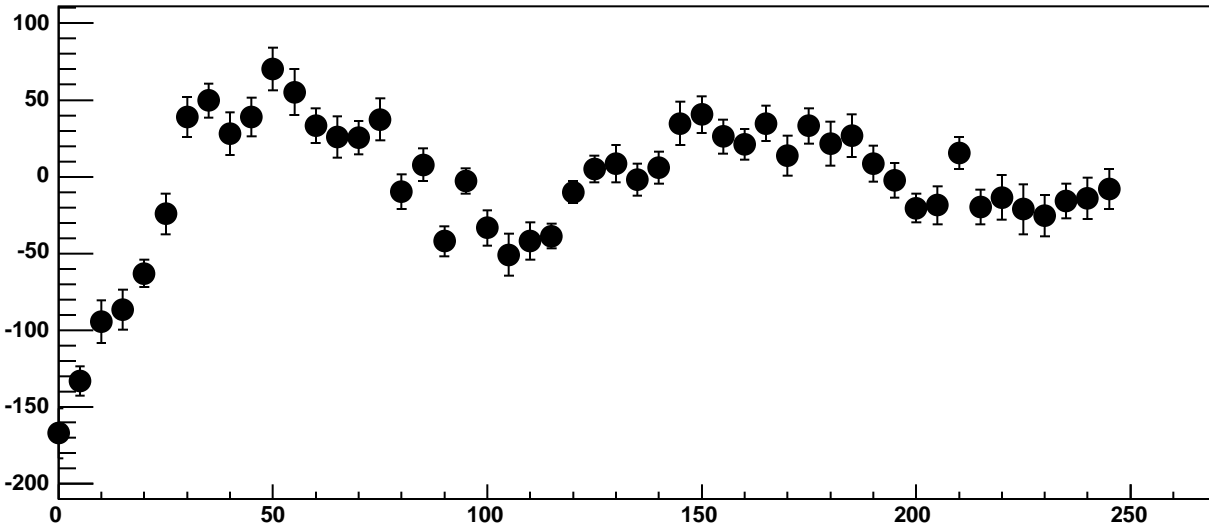


$\chi^2 / \text{ndf}$	358.1 / 41
p0	$-699.4 \pm 6.55$
p1	$107.3 \pm 0.502$
p2	$-3.577\text{e}+08 \pm 9.485\text{e}+06$
p3	$4.427\text{e}+07 \pm 2.975\text{e}+06$
p4	$6.124 \pm 0.1313$

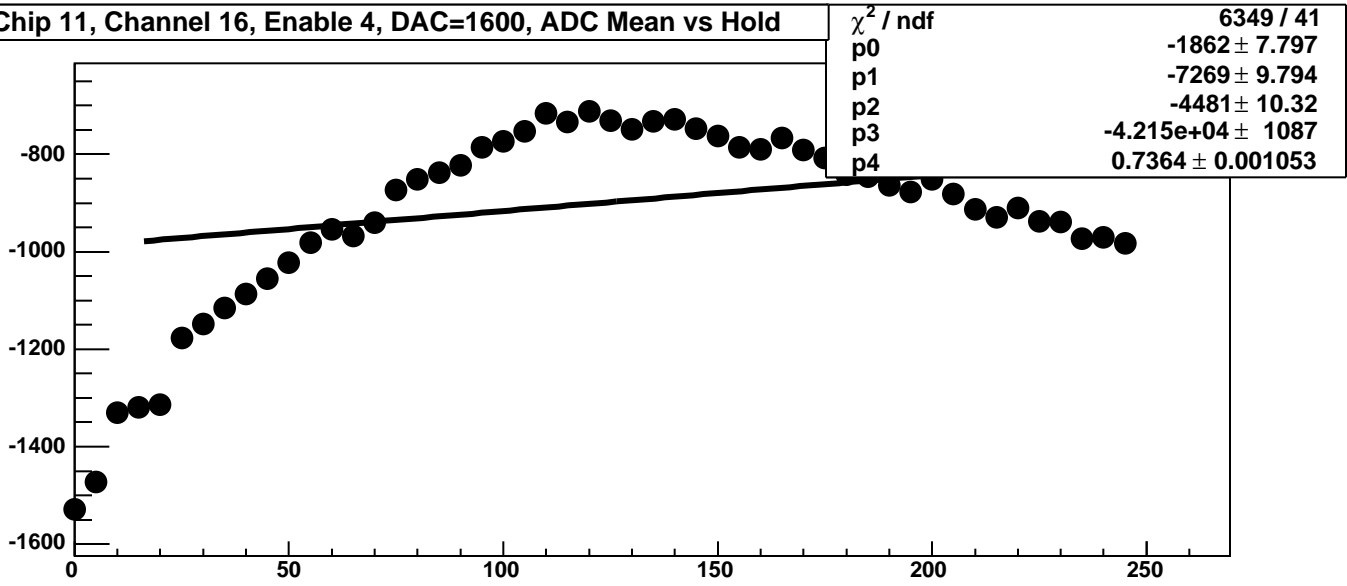
Chip 11, Channel 16, Enable 3, DAC=1600, ADC Noise vs Hold



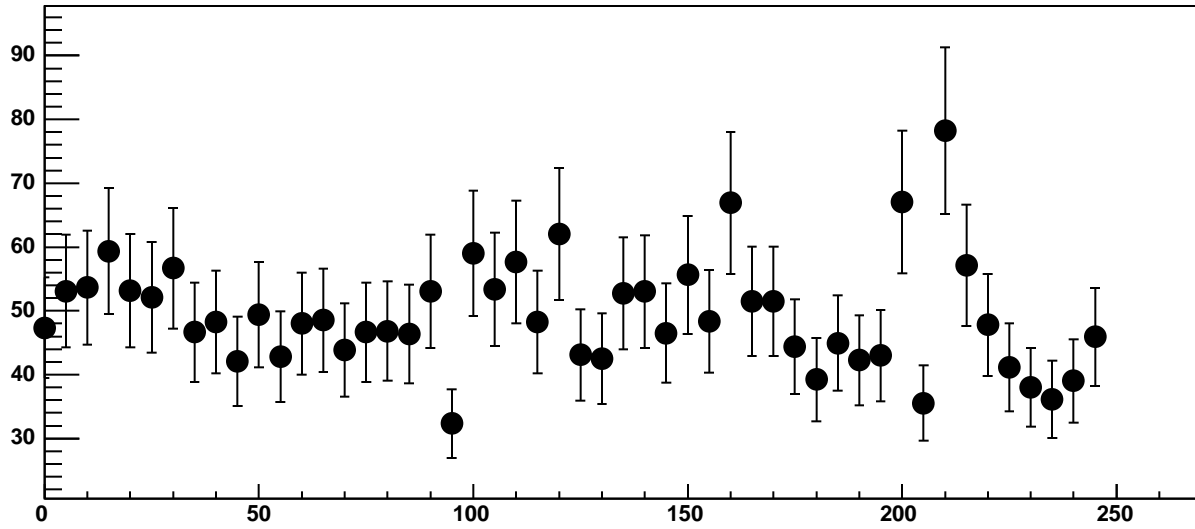
Chip 11, Channel 16, Enable 3, DAC=1600, ADC Residuals vs Hold



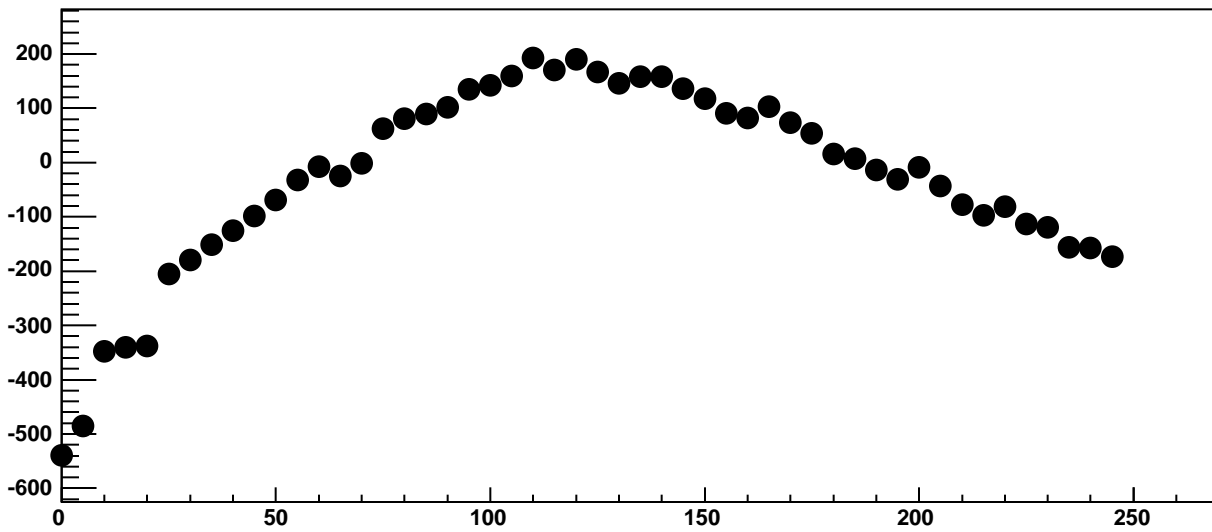
Chip 11, Channel 16, Enable 4, DAC=1600, ADC Mean vs Hold



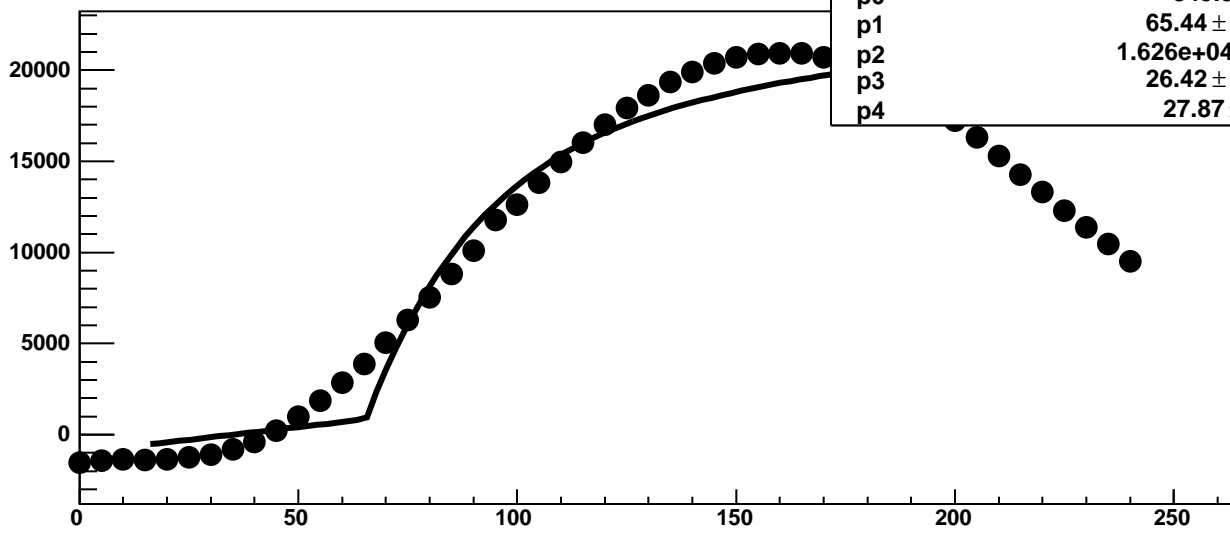
Chip 11, Channel 16, Enable 4, DAC=1600, ADC Noise vs Hold



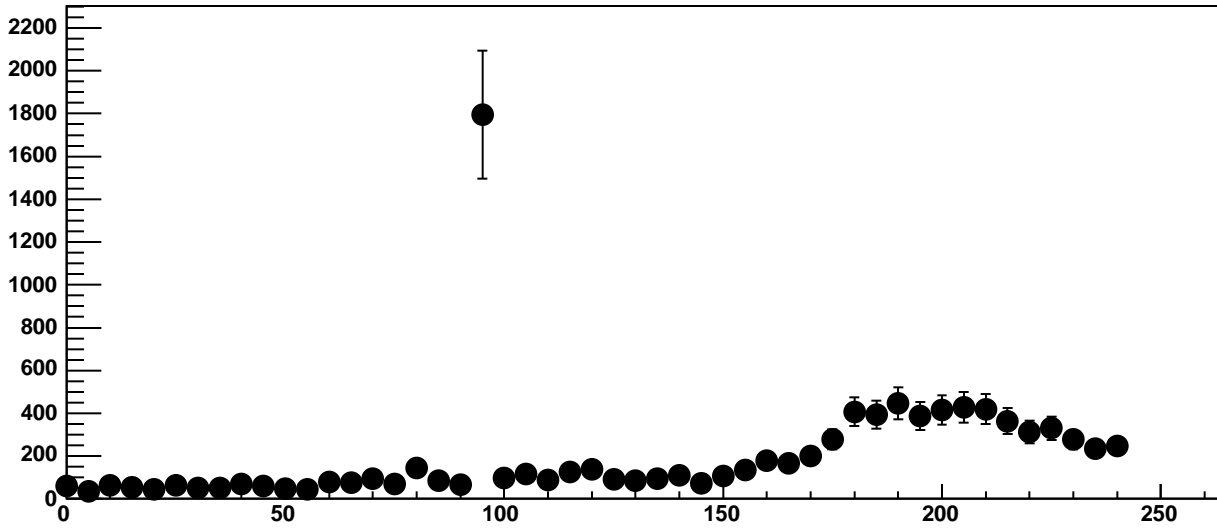
Chip 11, Channel 16, Enable 4, DAC=1600, ADC Residuals vs Hold



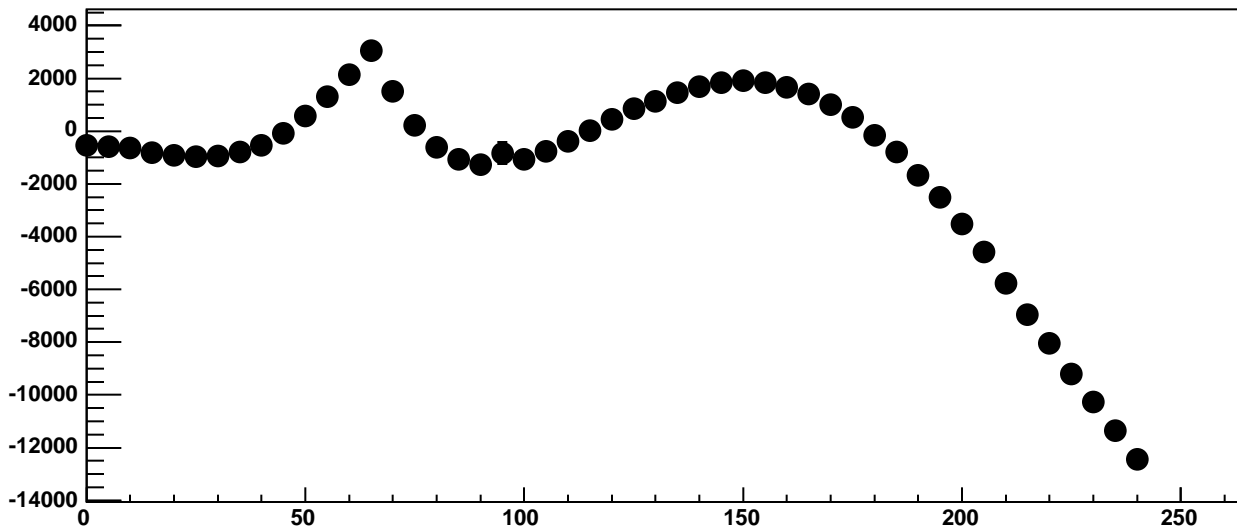
Chip 11, Channel 16, Enable 5, DAC=1600, ADC Mean vs Hold



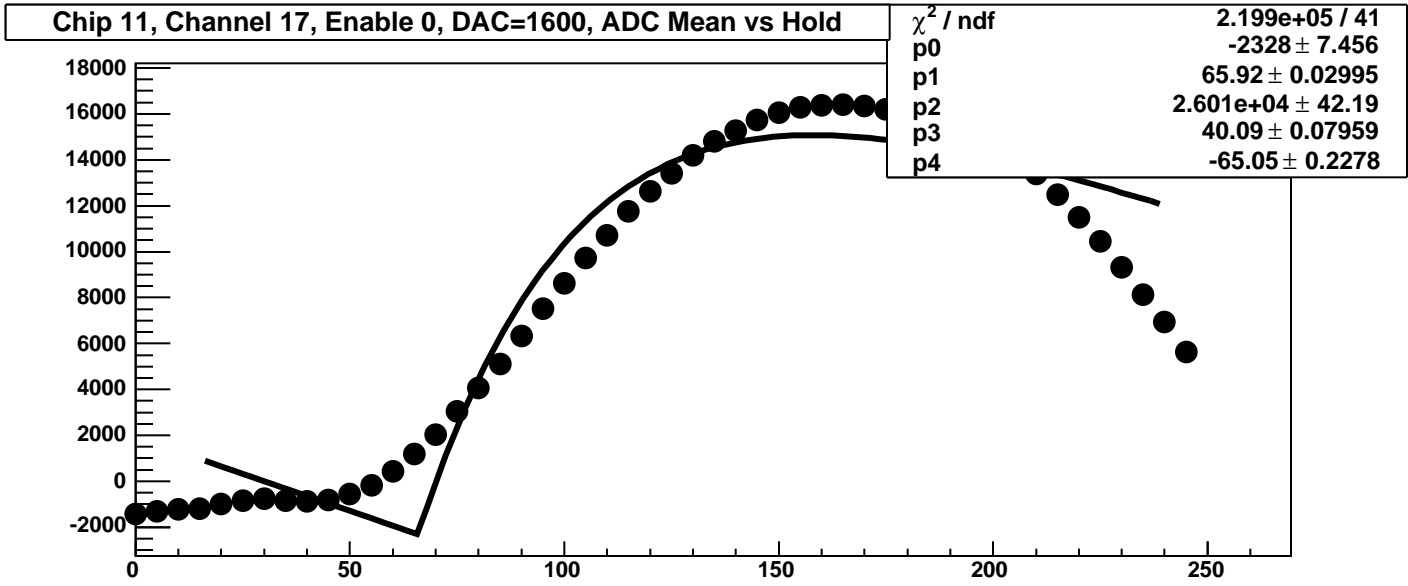
Chip 11, Channel 16, Enable 5, DAC=1600, ADC Noise vs Hold



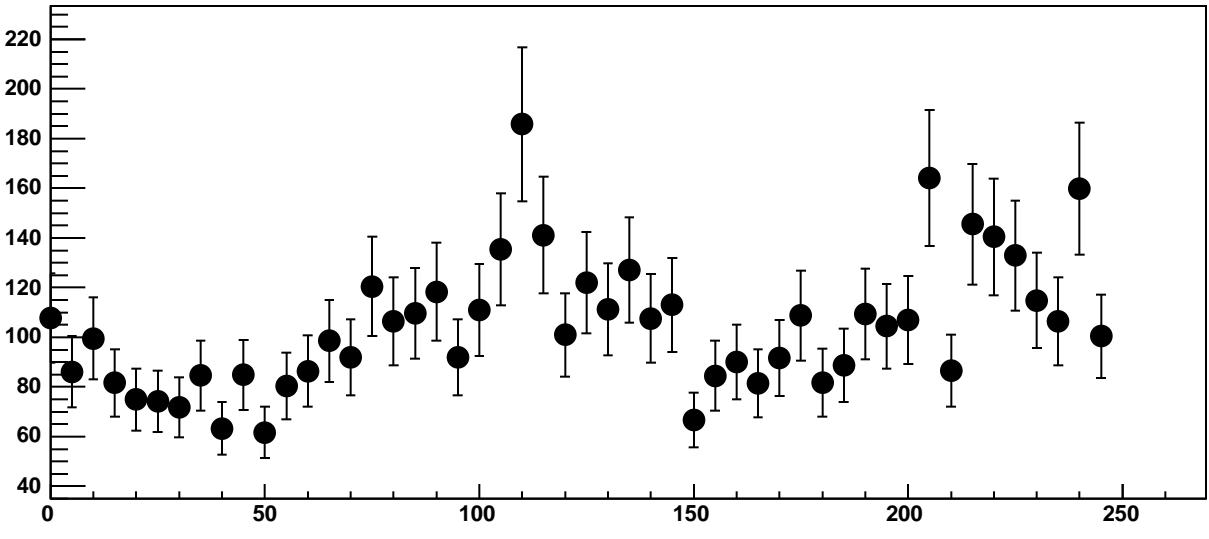
Chip 11, Channel 16, Enable 5, DAC=1600, ADC Residuals vs Hold



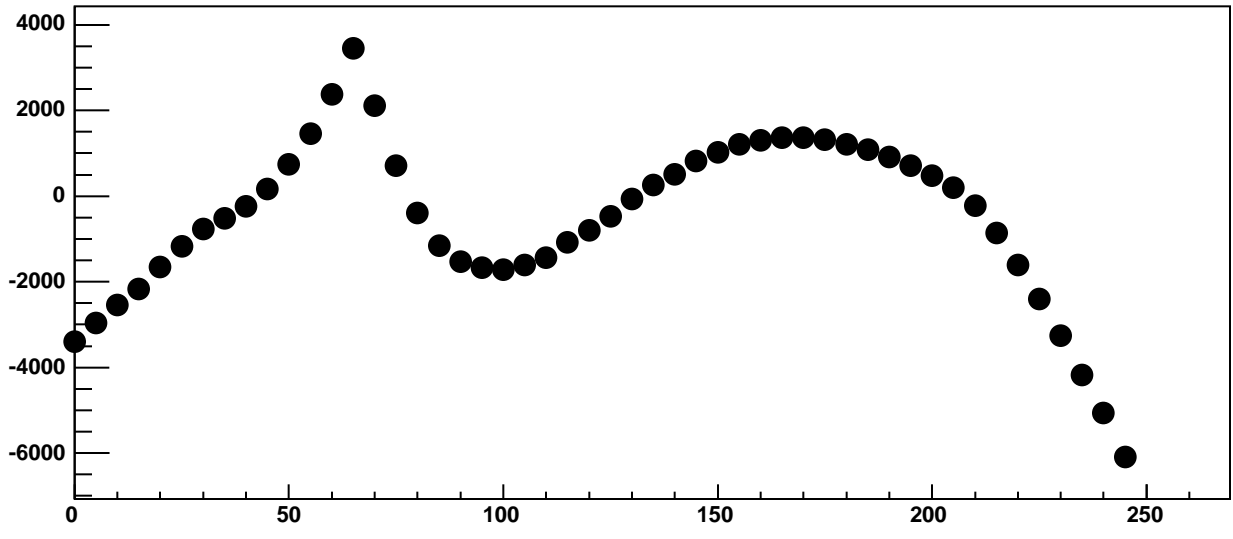




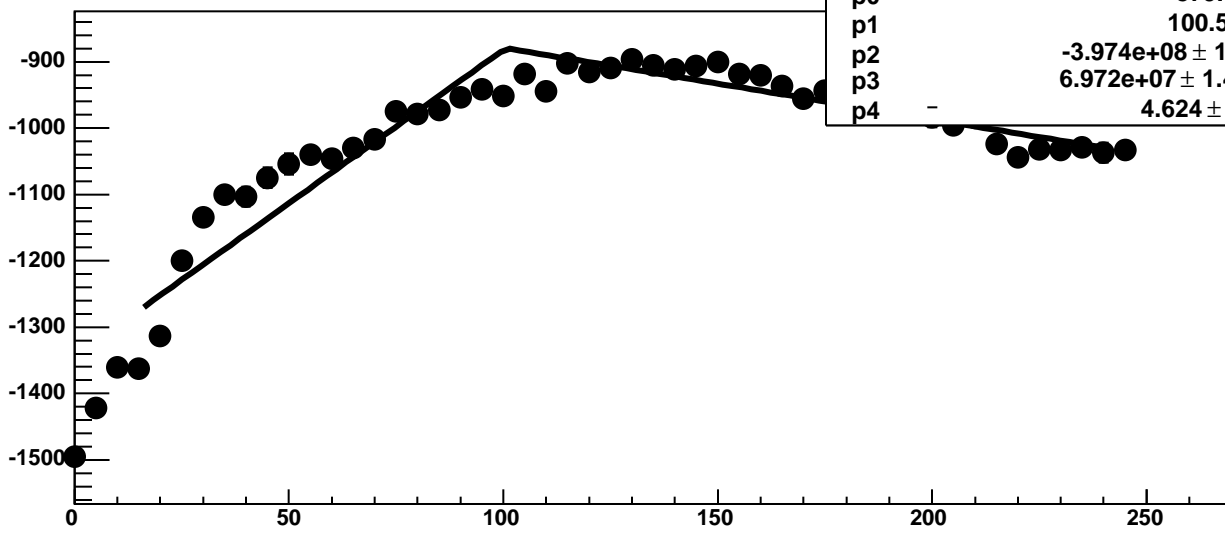
**Chip 11, Channel 17, Enable 0, DAC=1600, ADC Noise vs Hold**



**Chip 11, Channel 17, Enable 0, DAC=1600, ADC Residuals vs Hold**

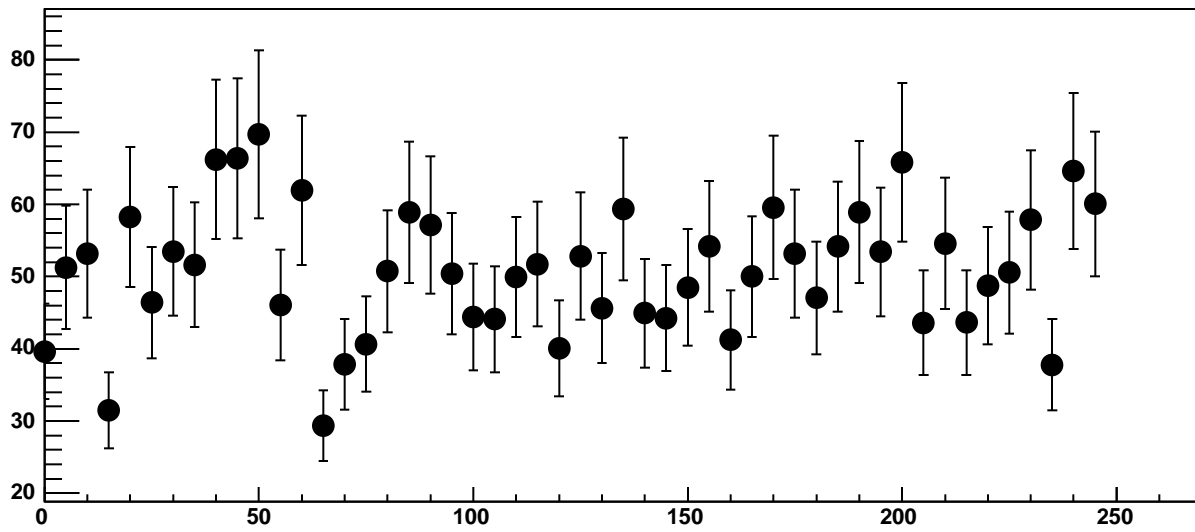


Chip 11, Channel 17, Enable 1, DAC=1600, ADC Mean vs Hold

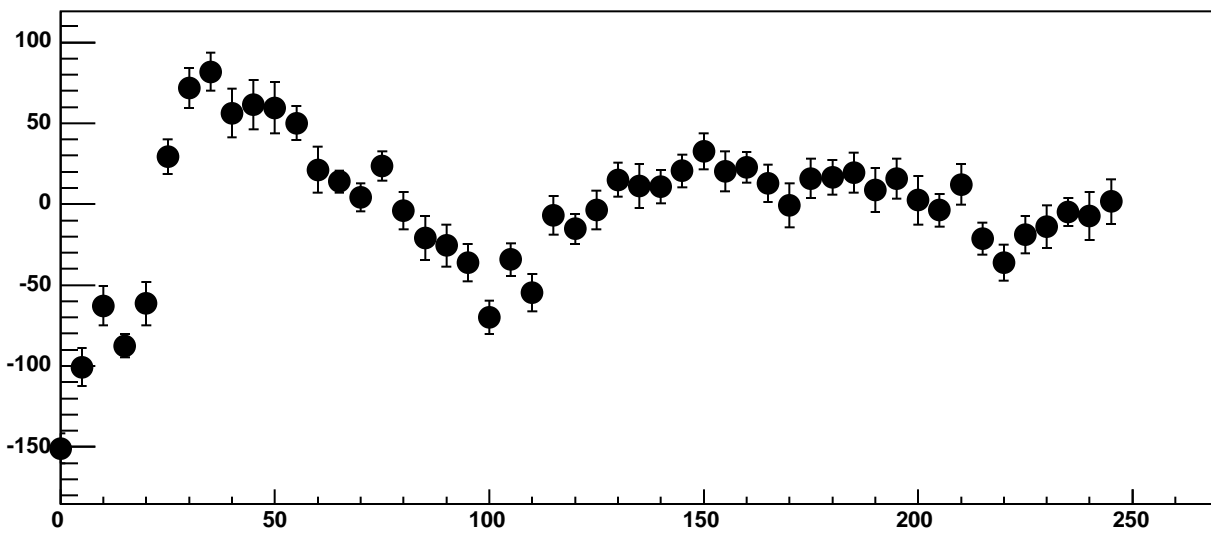


$\chi^2 / \text{ndf}$	493.5 / 41
p0	$-879.6 \pm 3.54$
p1	$100.5 \pm 1.127$
p2	$-3.974\text{e}+08 \pm 1.14\text{e}+07$
p3	$6.972\text{e}+07 \pm 1.479\text{e}+06$
p4	$4.624 \pm 0.09465$

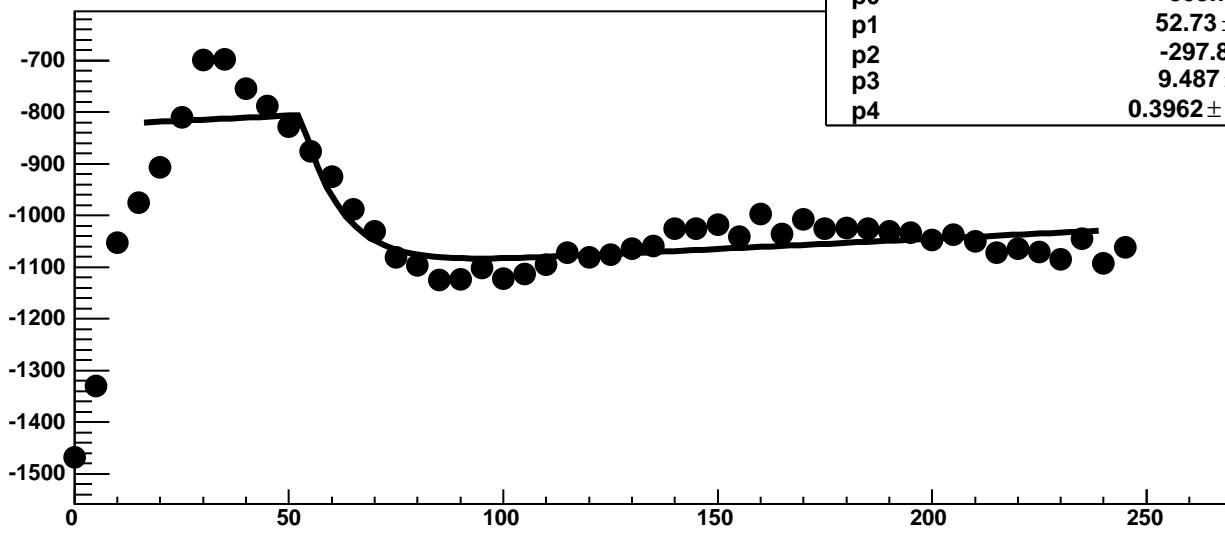
Chip 11, Channel 17, Enable 1, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 17, Enable 1, DAC=1600, ADC Residuals vs Hold

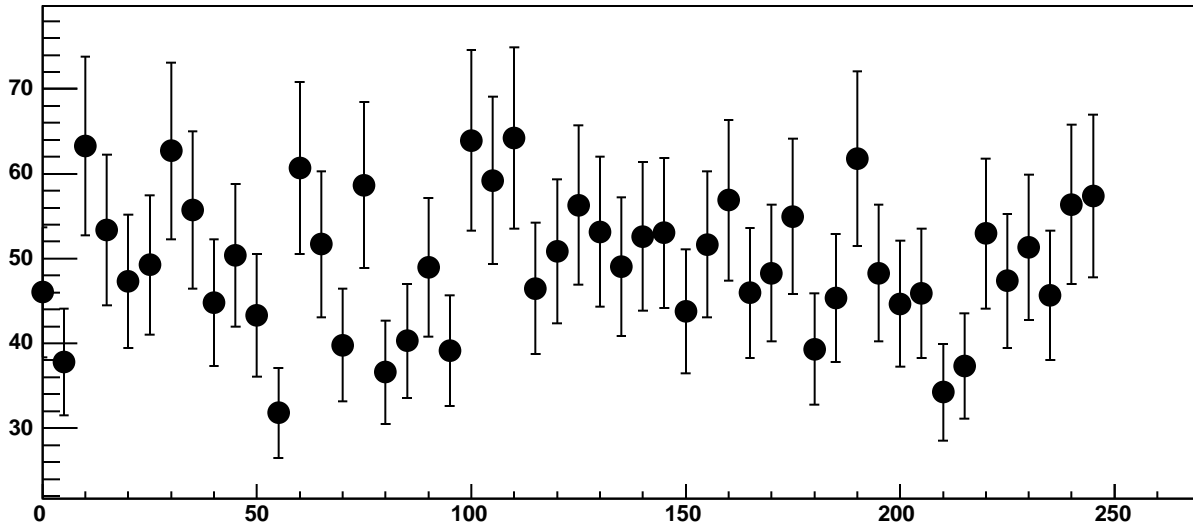


Chip 11, Channel 17, Enable 2, DAC=1600, ADC Mean vs Hold

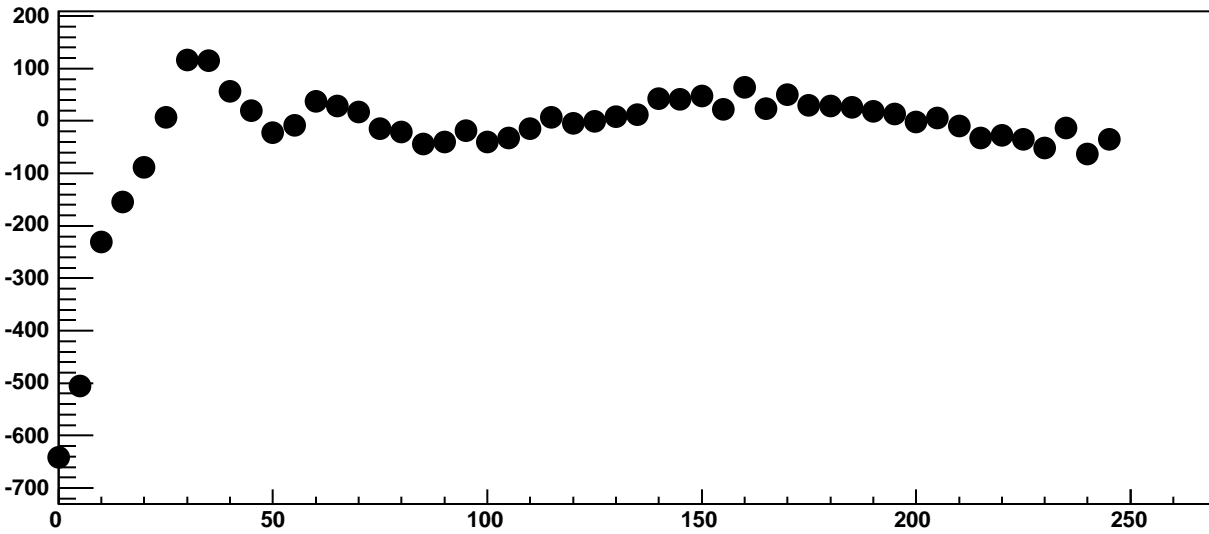


$\chi^2 / \text{ndf}$	690.6 / 41
p0	$-805.7 \pm 4.074$
p1	$52.73 \pm 0.3733$
p2	$-297.8 \pm 7.107$
p3	$9.487 \pm 0.6661$
p4	$0.3962 \pm 0.04159$

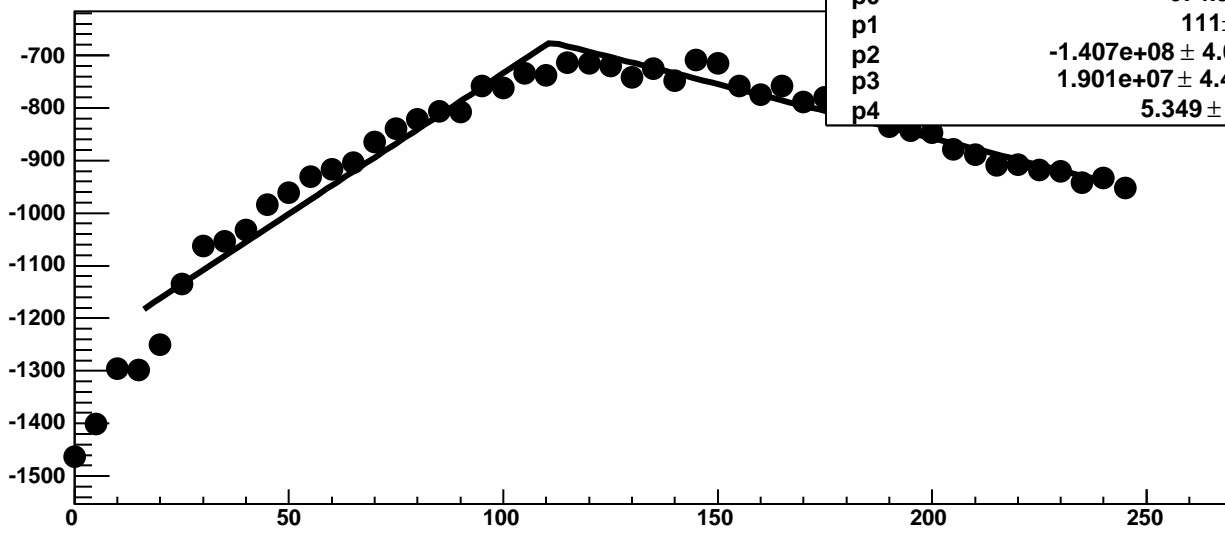
Chip 11, Channel 17, Enable 2, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 17, Enable 2, DAC=1600, ADC Residuals vs Hold

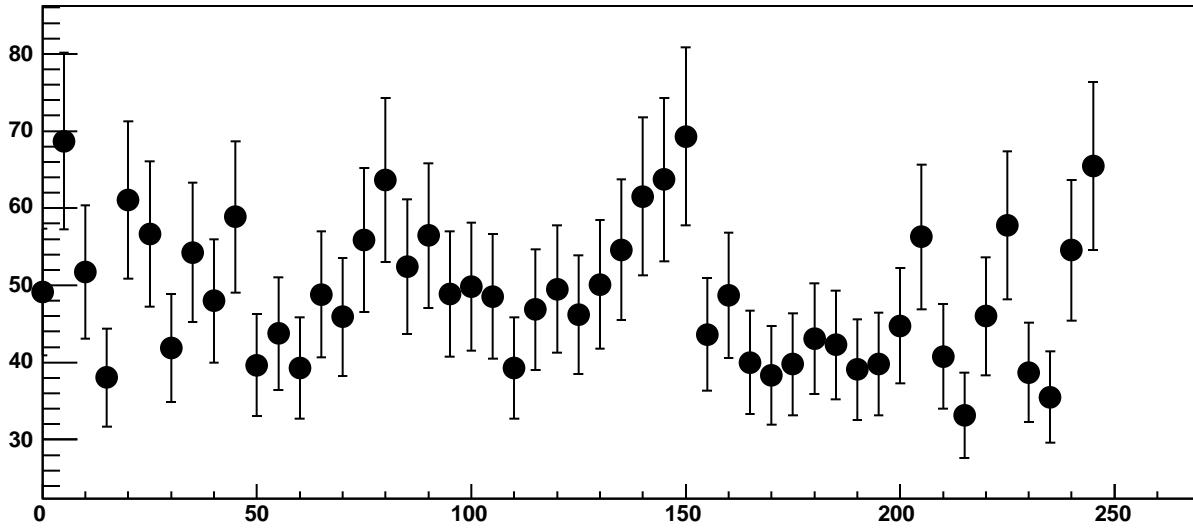


Chip 11, Channel 17, Enable 3, DAC=1600, ADC Mean vs Hold

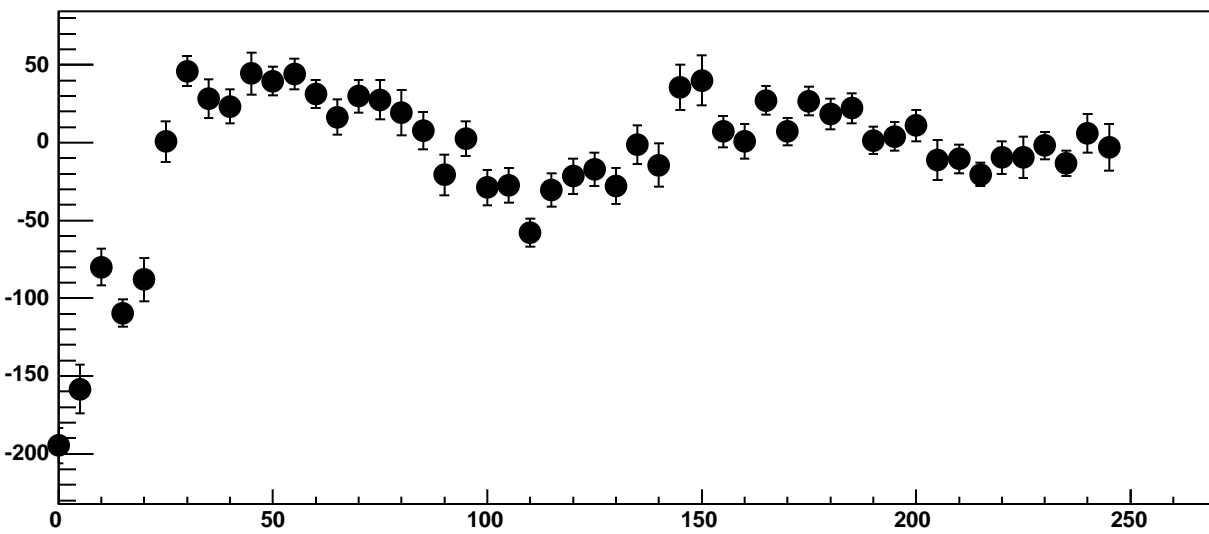


$\chi^2 / \text{ndf}$	439.6 / 41
p0	$-674.9 \pm 3.514$
p1	$111 \pm 0.8928$
p2	$-1.407\text{e}+08 \pm 4.027\text{e}+06$
p3	$1.901\text{e}+07 \pm 4.444\text{e}+05$
p4	$5.349 \pm 0.08384$

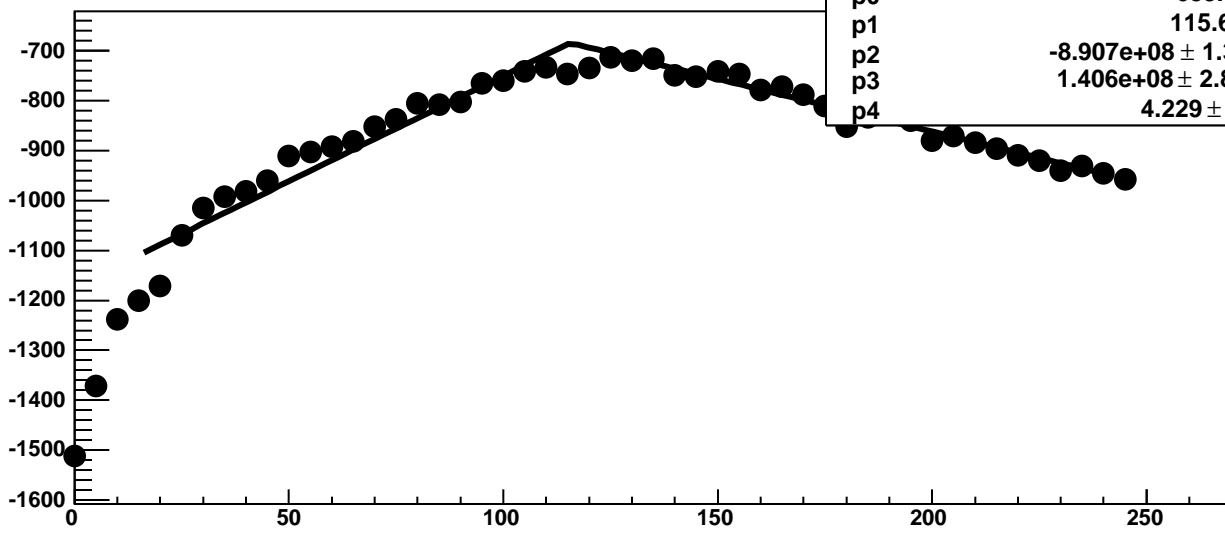
Chip 11, Channel 17, Enable 3, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 17, Enable 3, DAC=1600, ADC Residuals vs Hold

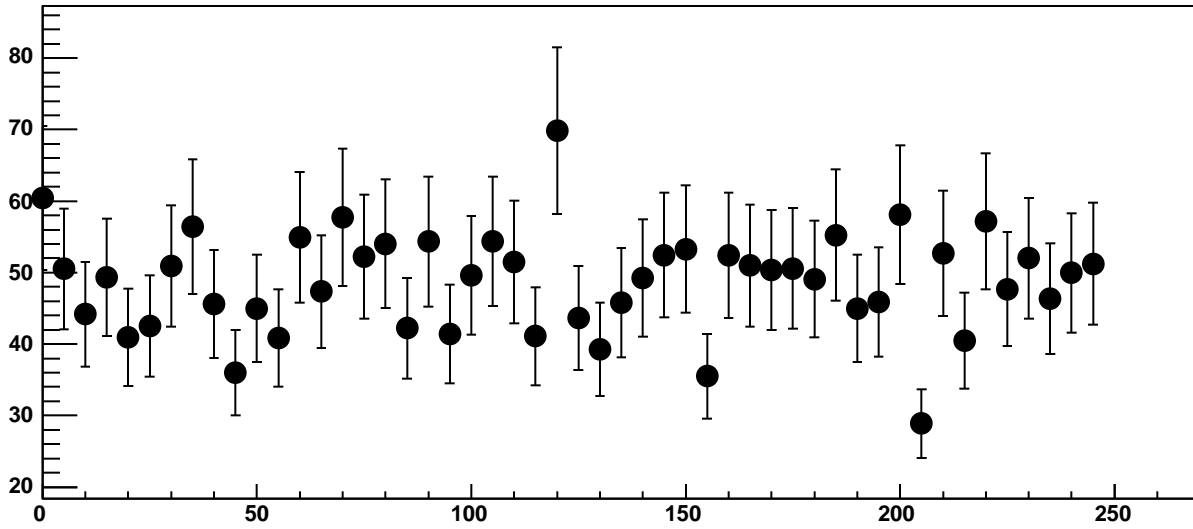


Chip 11, Channel 17, Enable 4, DAC=1600, ADC Mean vs Hold



$\chi^2 / \text{ndf}$	314.6 / 41
p0	-683.9 ± 3.36
p1	115.6 ± 1.013
p2	-8.907e+08 ± 1.381e+07
p3	1.406e+08 ± 2.823e+05
p4	4.229 ± 0.07633

Chip 11, Channel 17, Enable 4, DAC=1600, ADC Noise vs Hold



Chip 11, Channel 17, Enable 4, DAC=1600, ADC Residuals vs Hold

