CALICE ECAL Readout Electronics Conceptual Design Review

External interface : VME

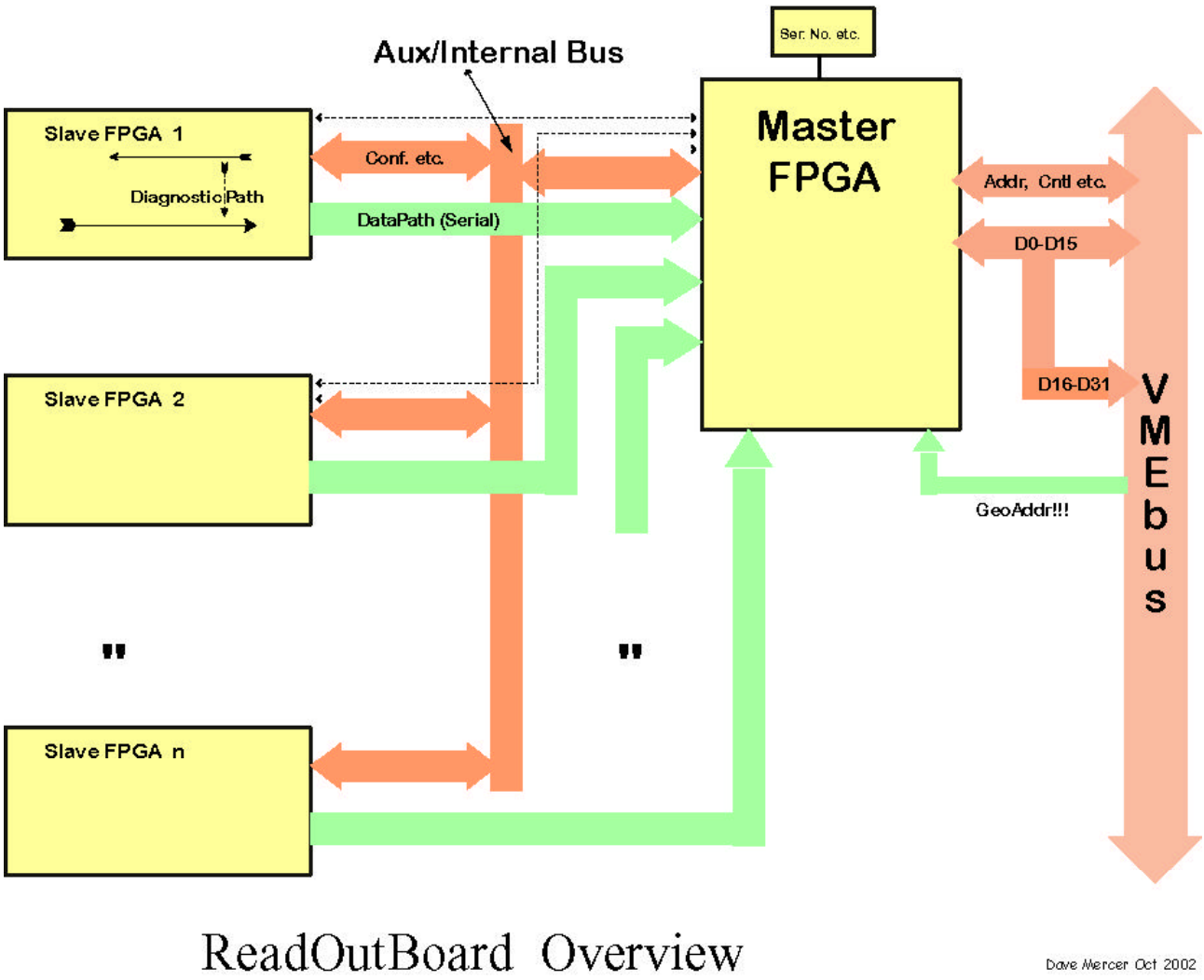

Fig 1

- Geographical Addressing.

We have a VME crate full of Readout Modules and they have to be individually addressed. We will use 6 spare pins on the VME J2 connector with a hard wired address which the module can read ; pull ups are on the module and backplane pins are grounded or floating. Access to the rear of the motherboard is needed but only once. The 2 outer rows of the J2 96 way connector
are usually left long and can be wire wrapped to an adjacent gnd pin.

- Aux/Internal bus (16 bit data; 12? bit address)

This is for configuration and diagnostics ; the fast datapath is separate .. see Fig 1. It is a very *simple* synchronous bus because all FPGAs share a (carefully routed common clock. The VME FPGA is always master and the Slave FPGAs always slaves ie. the slaves only speak when spoken to ; therefore there is never any contention . For any eventuality we will add a bussed LocalBusy signal so that slaves can signal to the master they are busy (collectively busy ,all slaves being equal). This should not be needed in normal running.

The VME synchronization and handshaking is done in the VME FPGA
I will generate the exact specification separately

- Sideband Signals

These are shown dotted above and are point to point , say about 4

1. Master to Slave ; <slave FPGA addressed >. The sub-address decoding to address the Slave FPGA's is done in the Master FPGA . This way all the slave FPGAs can have *IDENTICAL* VHDL inside. Indeed they could even be configured (loaded) in parallel saving money and time….but this needs further discussion perhaps.

2. Slave to Master ; < slave FPGA request attention. > for any reason error conditions etc.

3 , 4 spare

- Datapath (Slave to Master) (Serial internally / 32 bit to VME)

In fact the Slave is "Master"! Each slave FPGA pushes its data serially to its own area of Dual Port RAM in the master FPGA. All slaves do this in parallel. This same RAM appears to the VME as one large contiguous memory and can be accessed by one DMA

- All on board devices inc. FPGA's 3v3 I/O except possibly any VME bufferchips .

FPGA internal supply 1.8 or 2.5v depending on family chosen.
for Altera) It may be that the Xilinx has not got enough strengyh to drive the VME directly,in which case 74ABT(E) buffers will be used (not shown above). It might be more versatile to have D16->31 direct from FPGA ,not as shown .

- All internal registers must be Read / Write ; ie nothing read only.
- Master FPGA has unique , hard wired, serial number eg. Dallas "one wire" plus optional EEPROM I2C or "one wire"
- Master FPGA is VME interrupter ;
  slave FPGAs interrupts via Master (via sideband signal)
- Diagnostic 4bit Hex/Dil switch to FPGA
- Diagnostic LEDS on front panel (Red => error, otherwise green)

- Logic analyzer header (NOT SHOWN !) connected to FPGA(s)

- JTAG output from Master to (re)program Slaves
  Initially via software from VME (like JAM player or bit bashing)
  Later hardware assisted if necessary.

- Load all FPGA's in one chain from a single "big" Configuration SROM;
  perhaps all slave FPGA's loaded in parallel ?

- Use XILINX FPGA's ? Spartan II or IIe