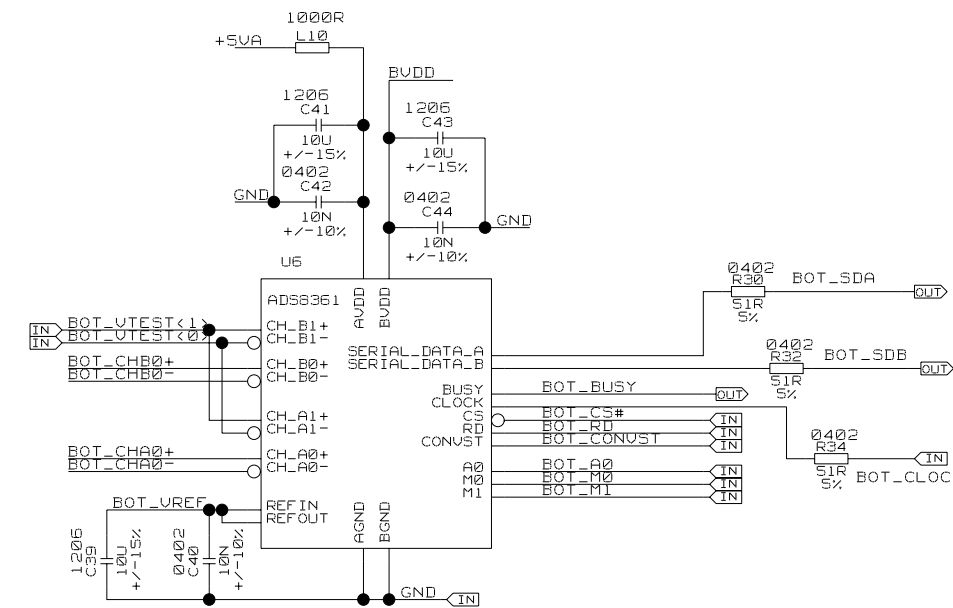
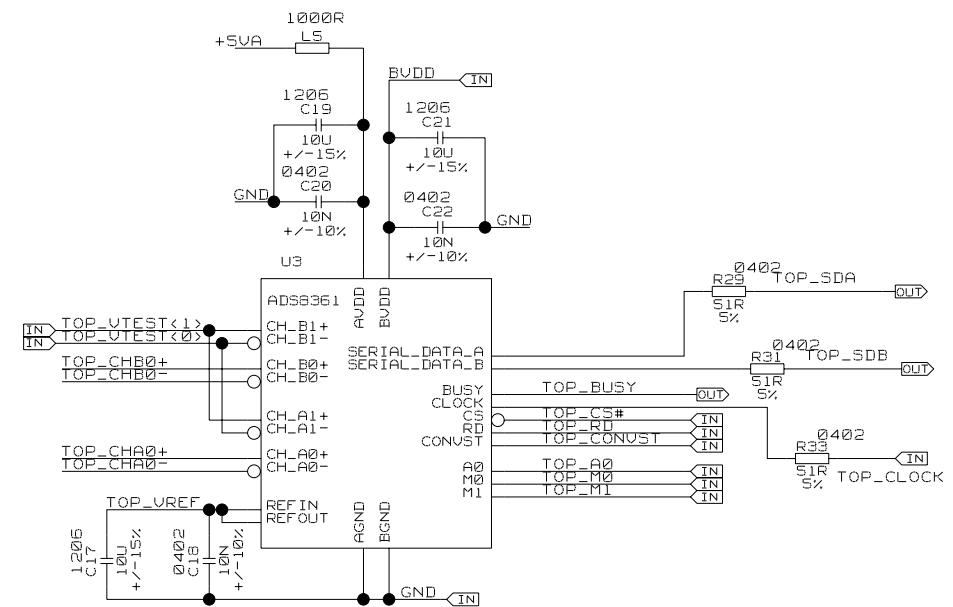
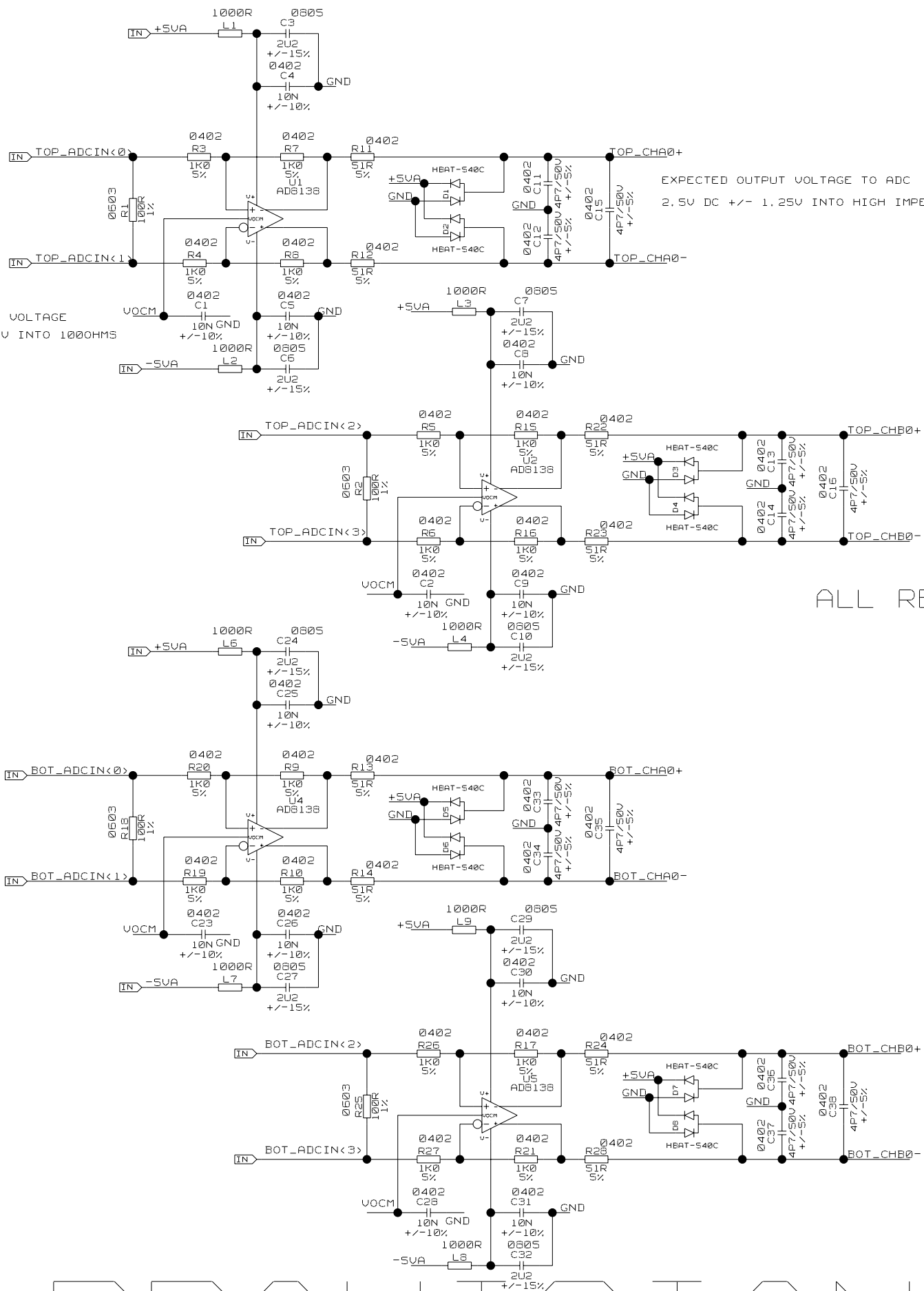


EXPECTED INPUT VOLTAGE  
0V DC +/- 1.25V INTO 100OHMS  
DIFFERENTIAL

EXPECTED OUTPUT VOLTAGE TO ADC  
2.5V DC +/- 1.25V INTO HIGH IMPEDANCE

ALL RESISTORS MUST BE CHANGED TO 1% TOLERANCE

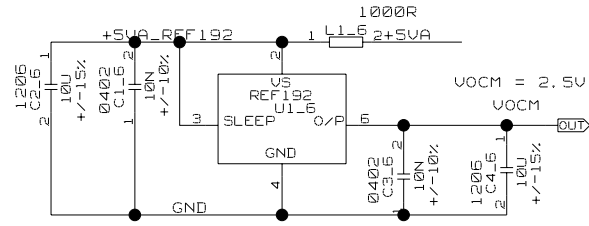


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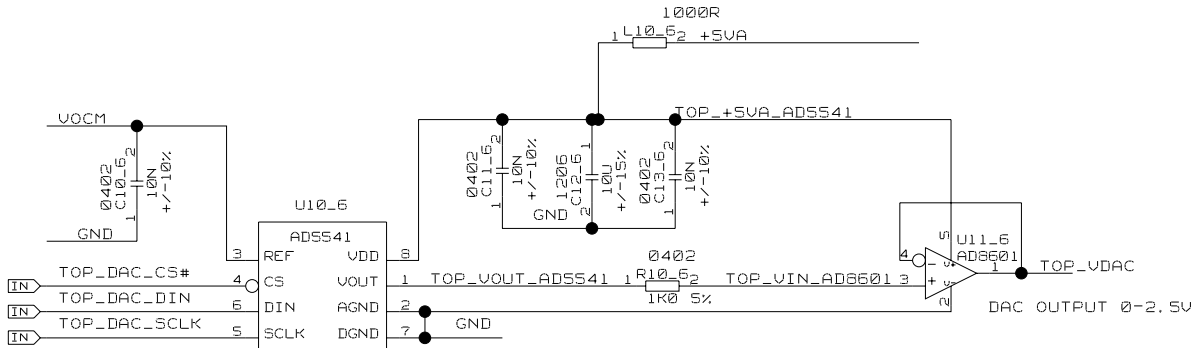
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TITLE  
 CALICE ADC DESIGN  
 A2

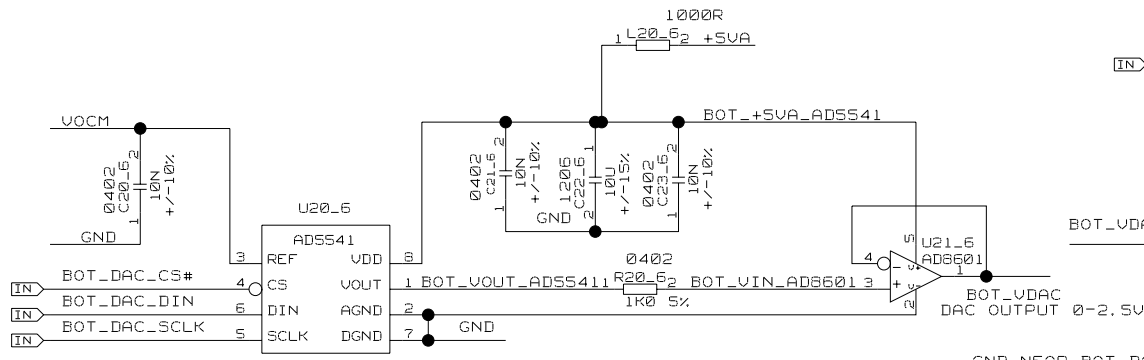
VOLTAGE REFERENCE



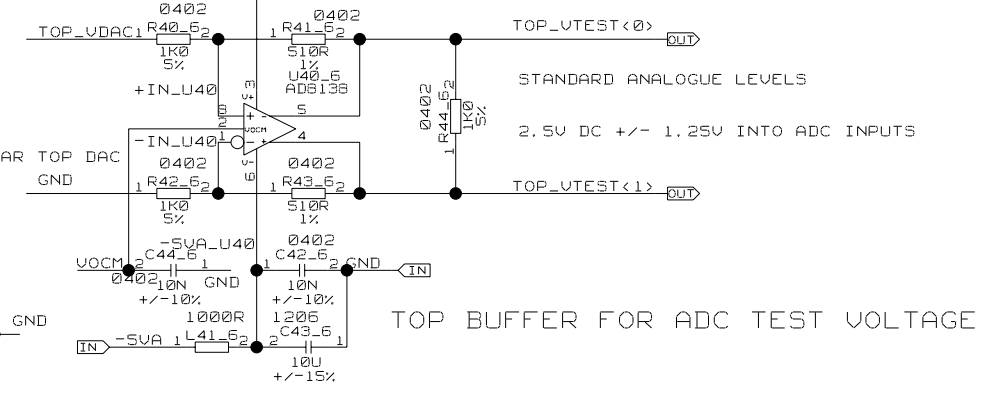
TOP DAC



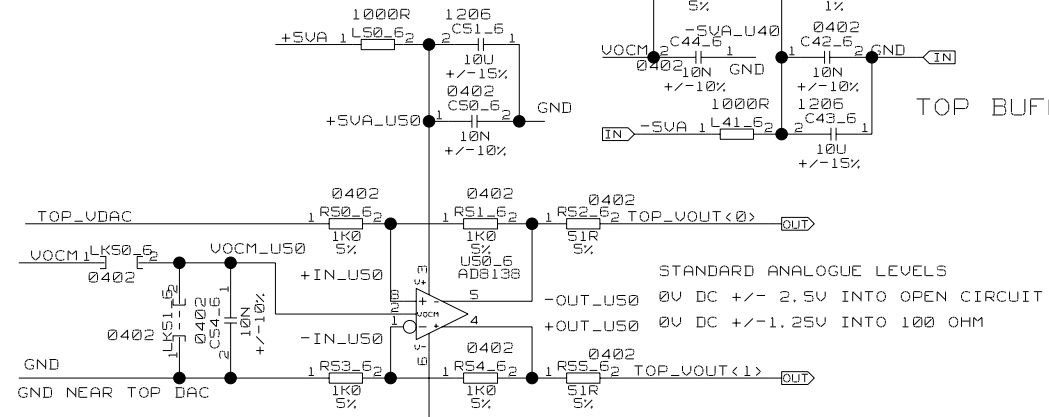
BOT DAC



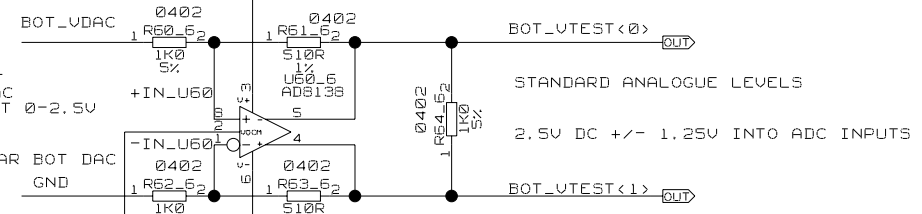
TOP BUFFER FOR ADC TEST VOLTAGE



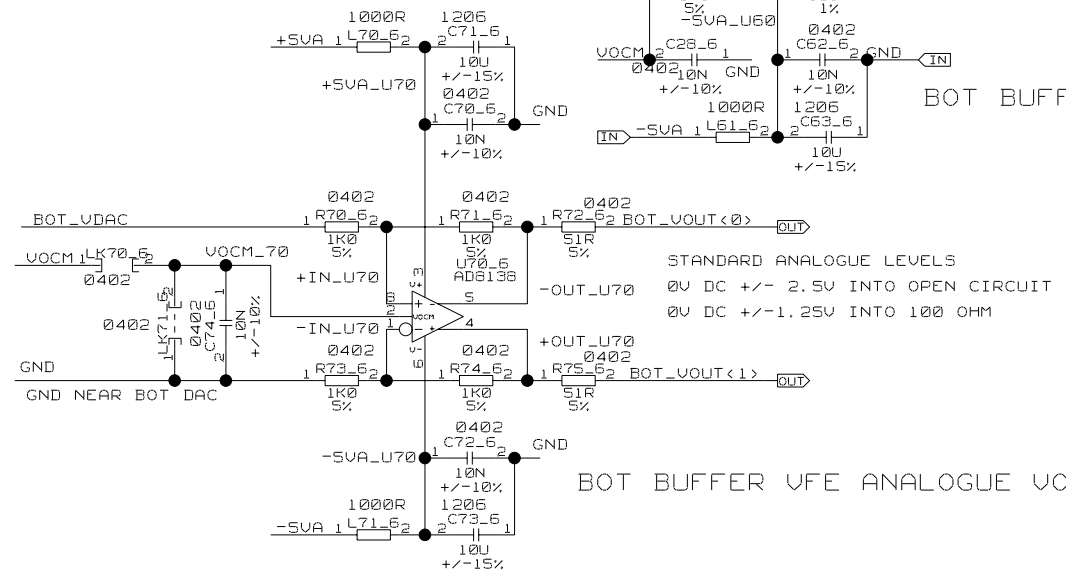
TOP BUFFER VFE ANALOGUE VOLTAGE



BOT BUFFER FOR ADC TEST VOLTAGE



BOT BUFFER VFE ANALOGUE VOLTAGE



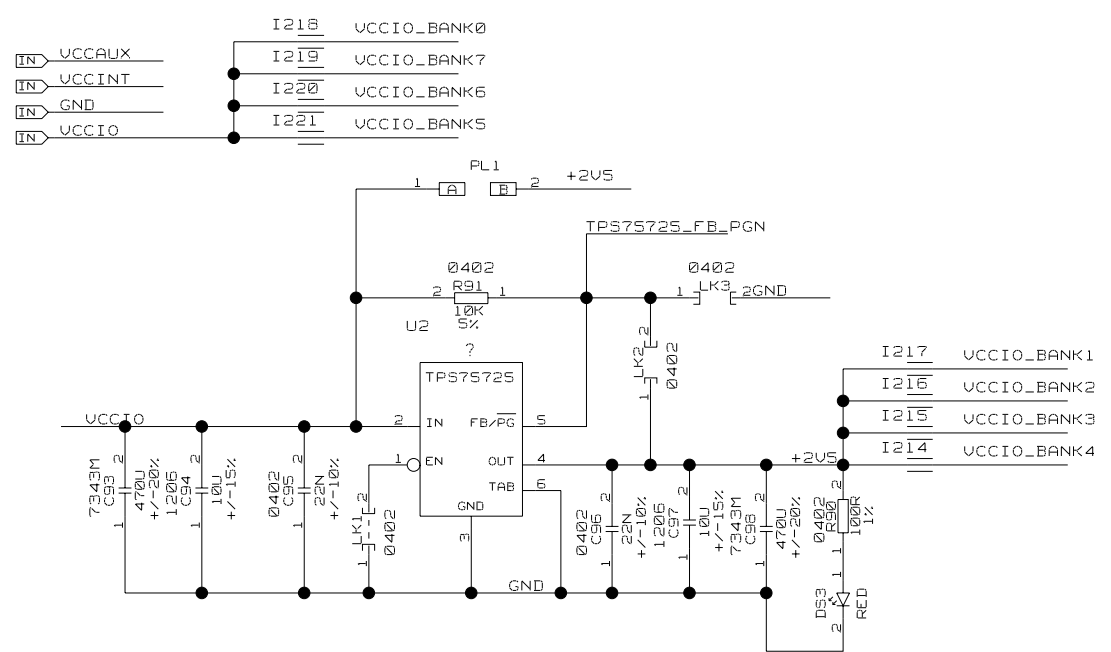
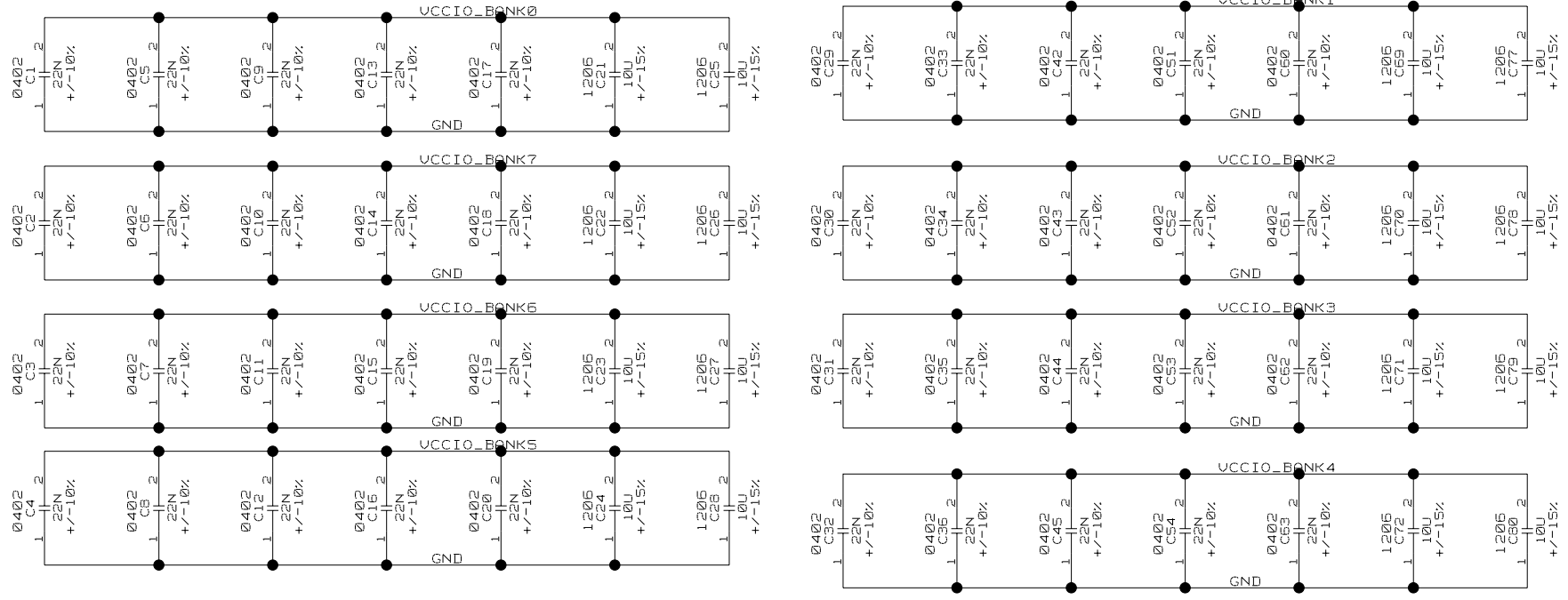
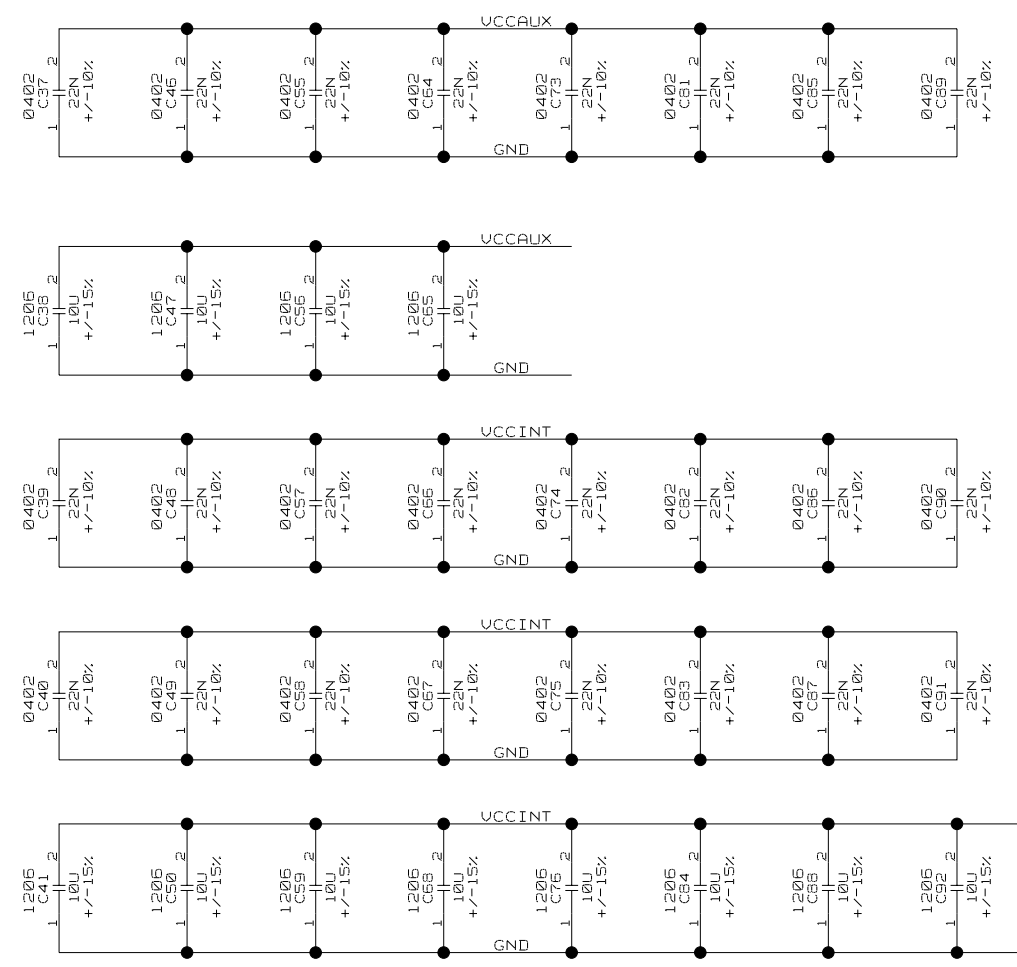
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ALL RESISTORS SHOULD BE CHANGED TO 1% TOLERANCE

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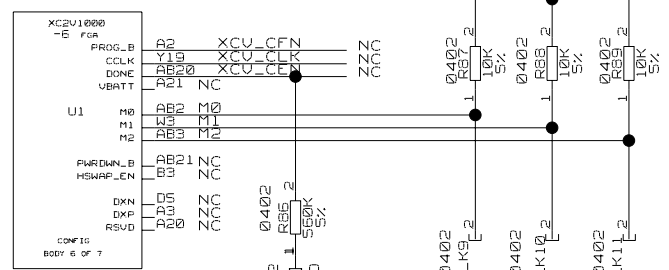
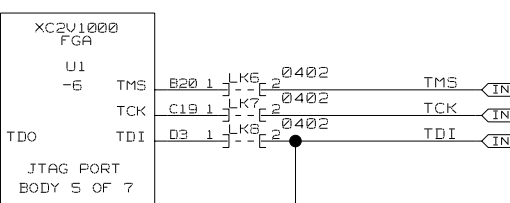
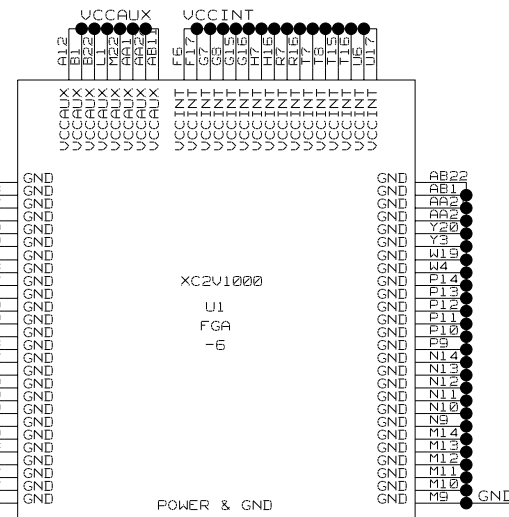
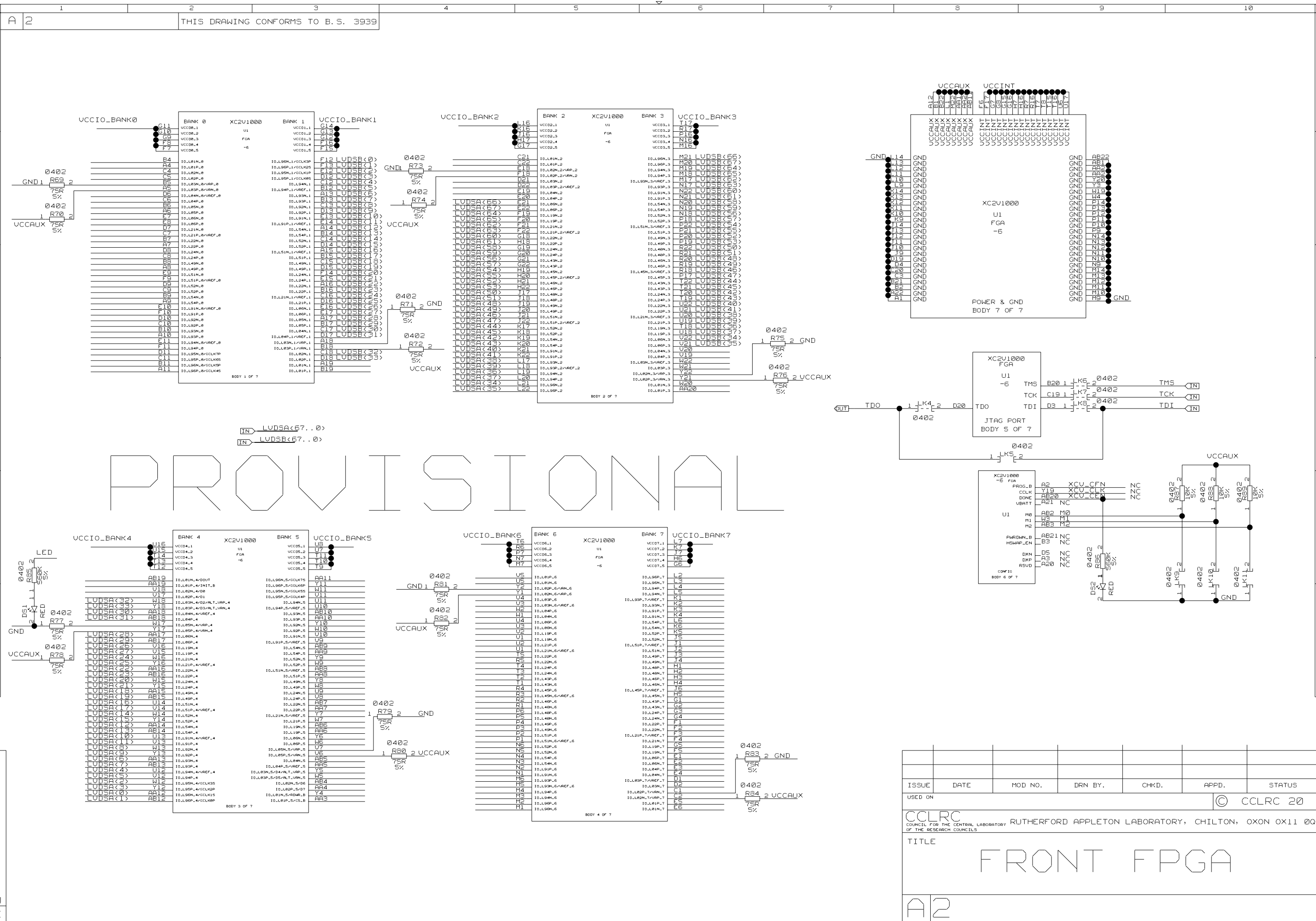
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CALICE DAC DESIGN



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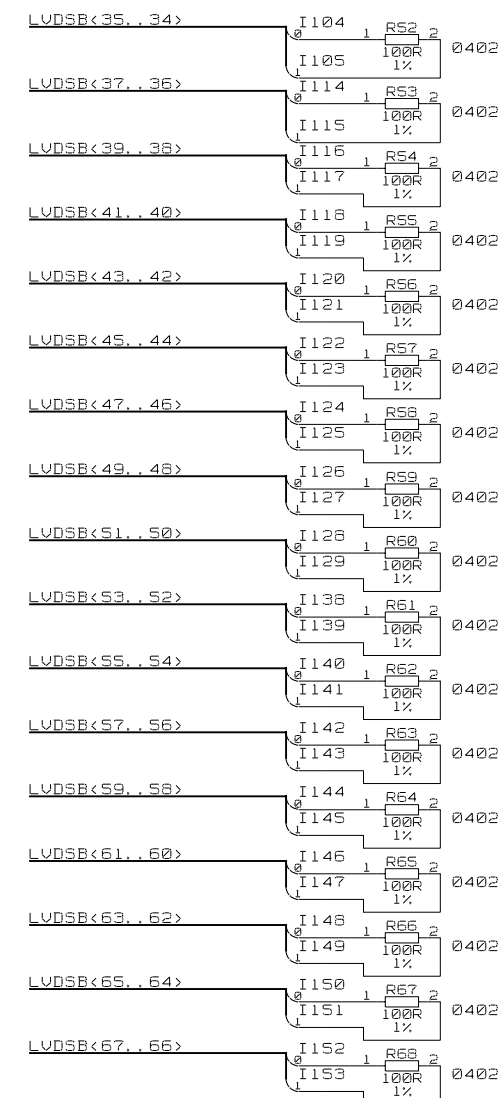
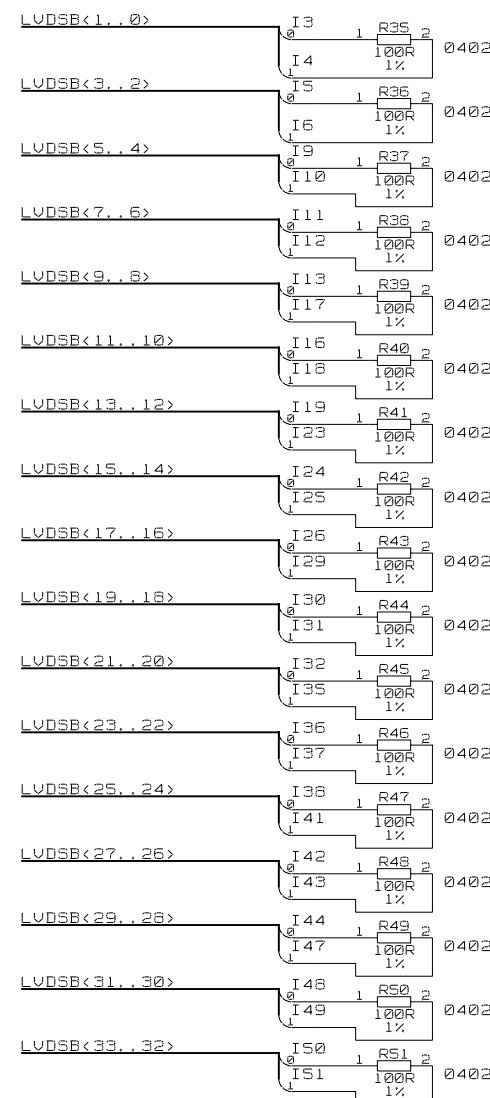
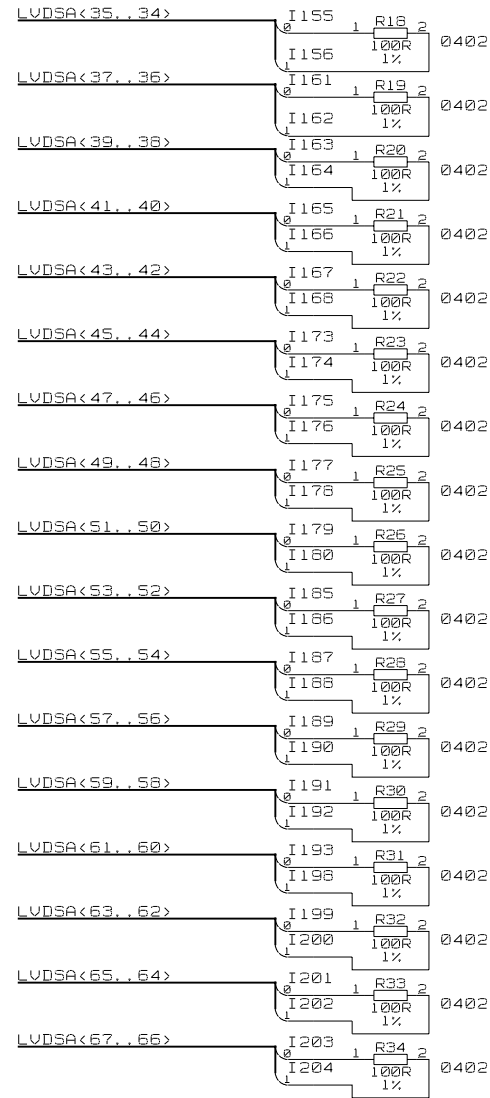
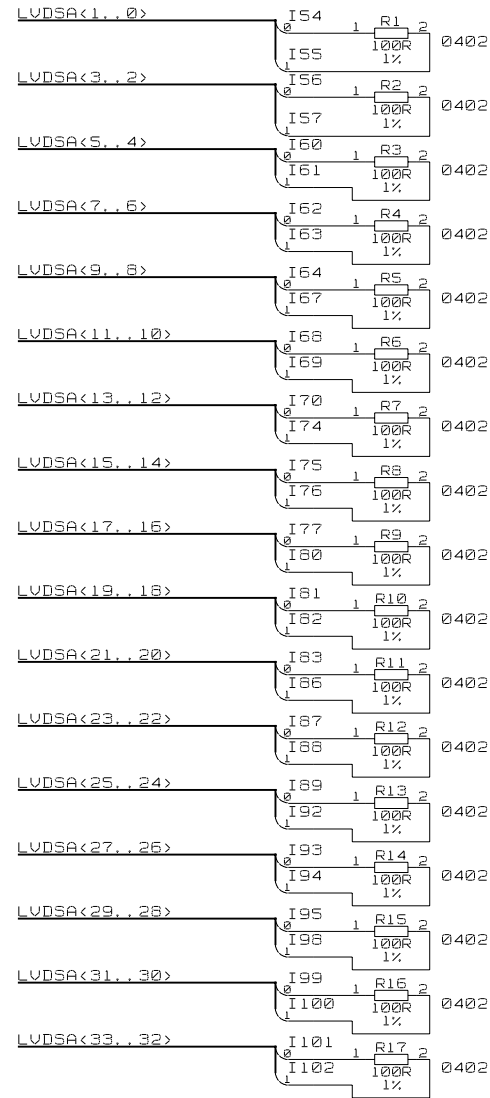
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TITLE						
FPGA DECOUPLING AND 2V5 LVDS UCCIO PSU						
A2						



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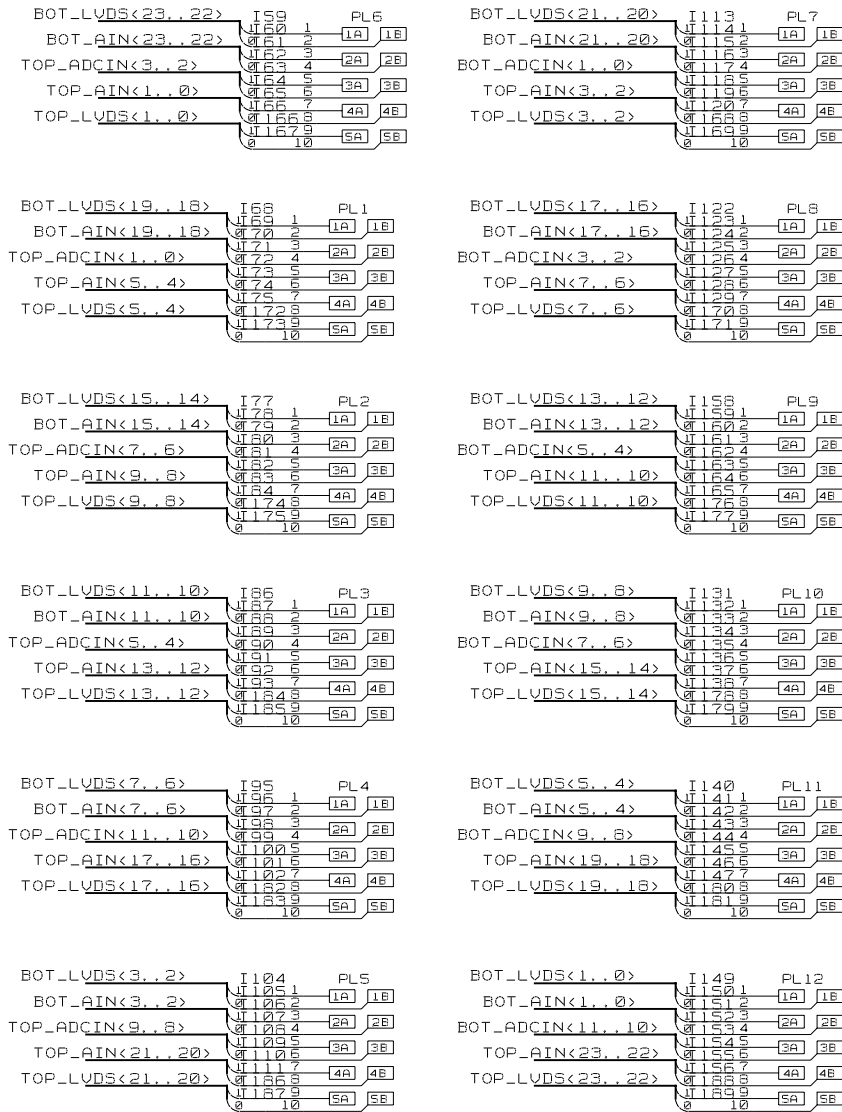
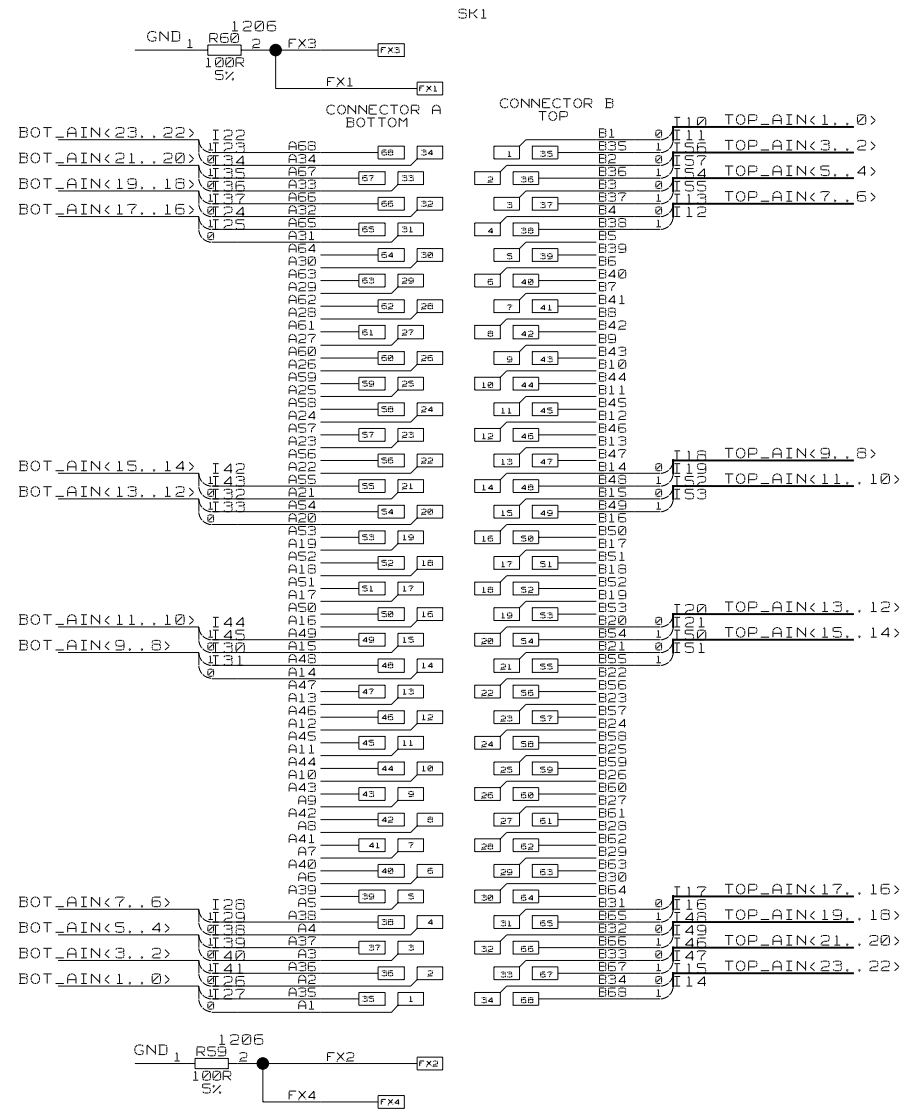
TITLE  
 FRONT FPGA



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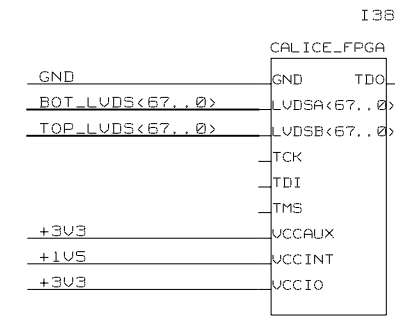
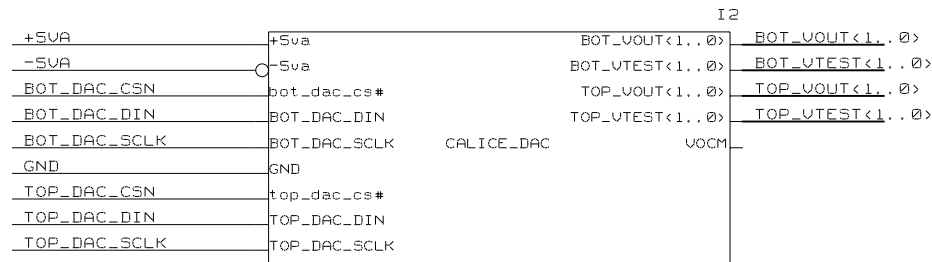
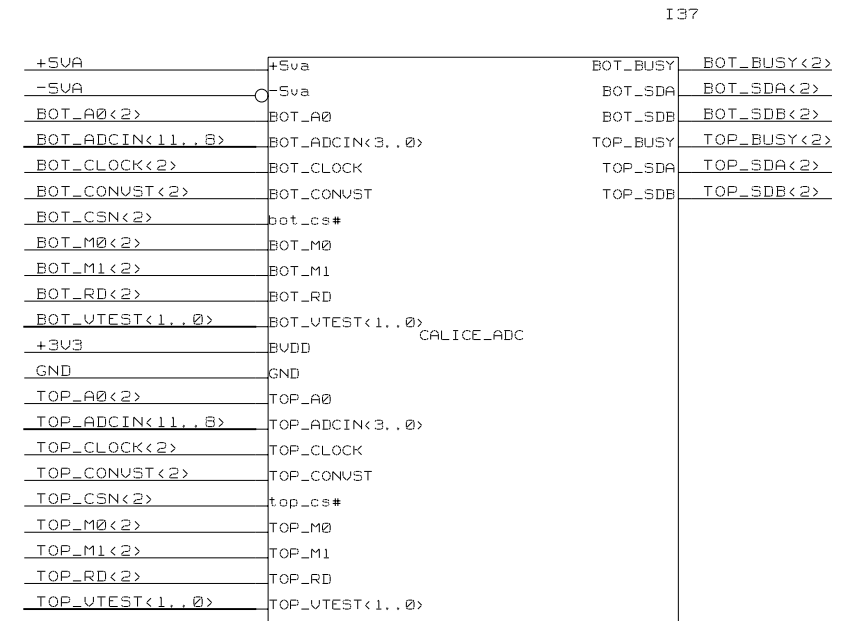
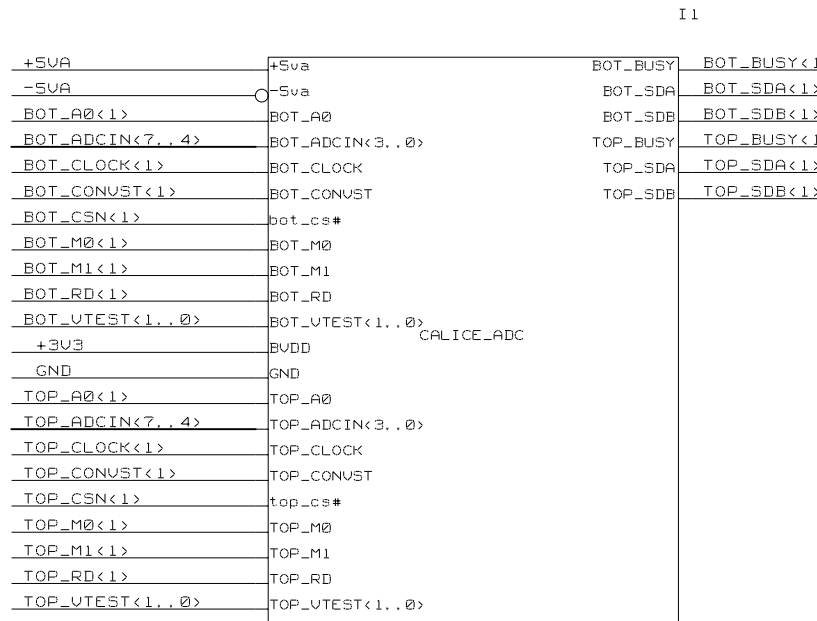
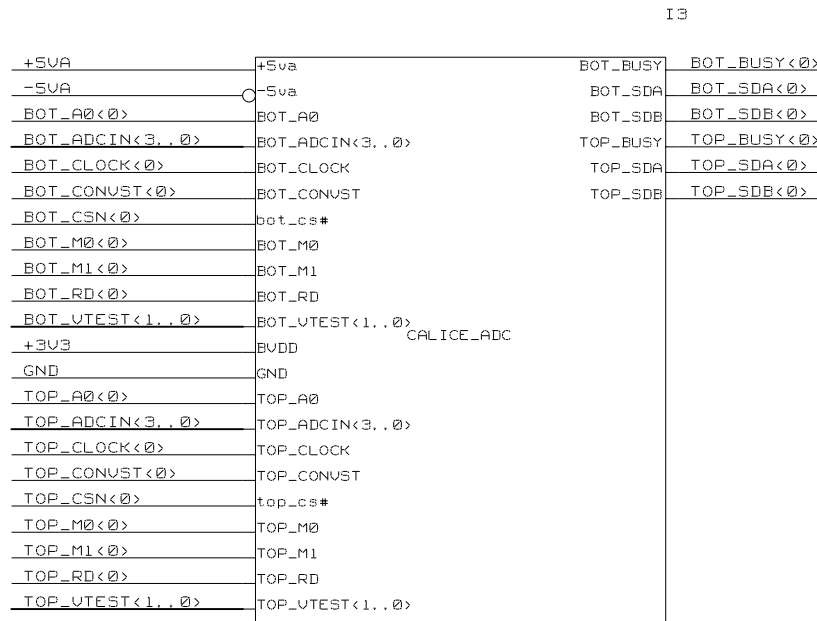
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A2						

THIS PINOUT WILL CHANGE



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TITLE						
SCSI CONNECTOR AND SELECTION JUMPERS						
A2						



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TITLE						
ALL MODULES						
A2						