Imperial College London

CALICE Calorimeter for LC

Electronics Status

For the Imperial, Manchester, RAL, and UCL groups

Dan Bowerman
Imperial College

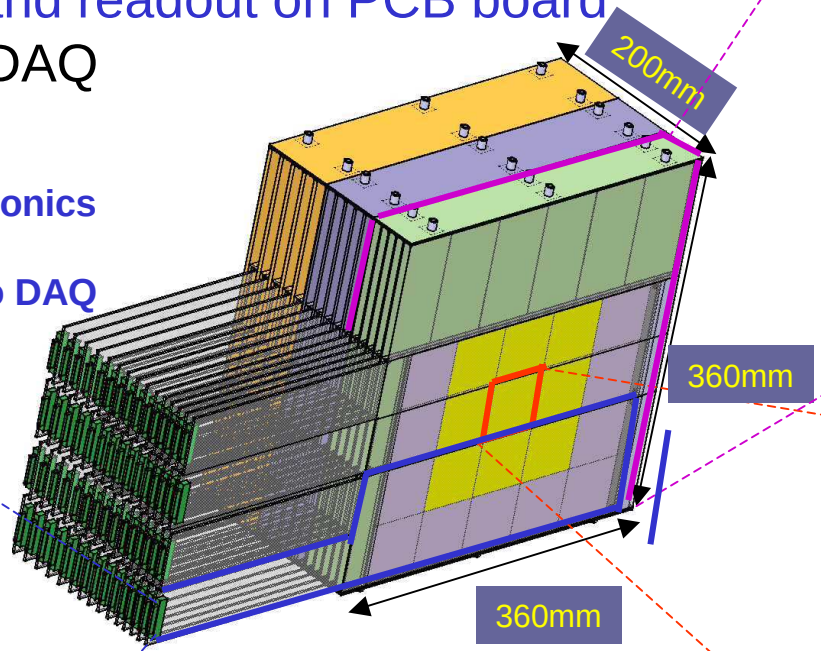
Calice Meeting - UCL
10th November 2004

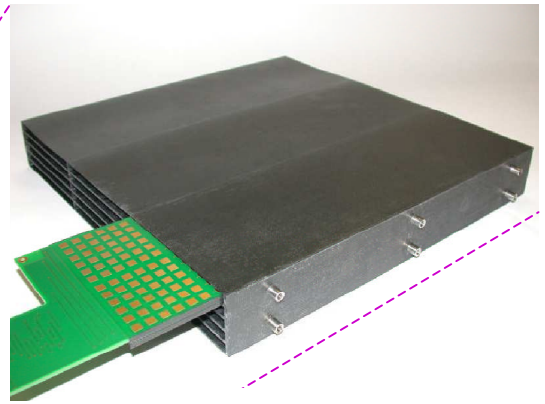
Overview

- **Ecal prototype overview**
- **Front end electronics and PCB status**
- **The UK readout boards**
- **Test boards system tests**
- **Cosmics data with full detector chain**
- **From Test to Production boards**
- **First tests of production boards**
- **Timelines, Finances and plans**
- **Conclusions**

Ecal Prototype Overview

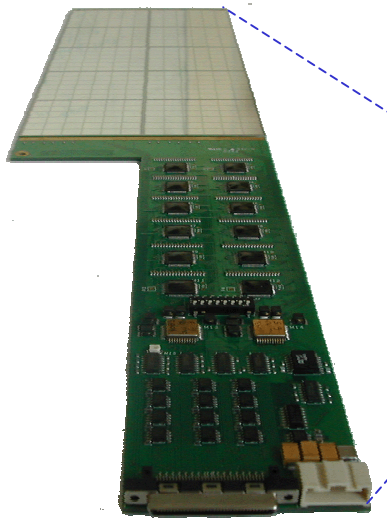
- 30 layers of variable thickness Tungsten
- Active silicon layers interleved
- Front end chip and readout on PCB board
- Signals sent to DAQ

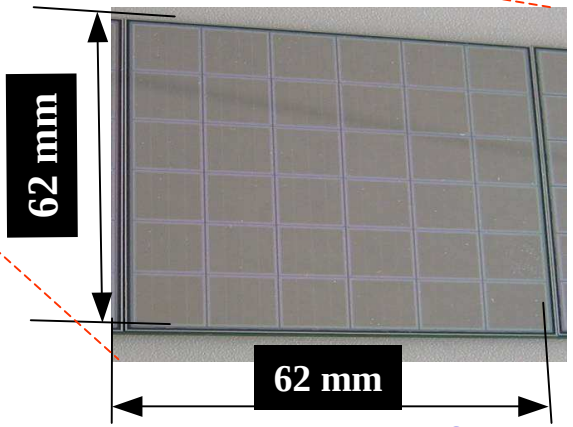




- Tungsten layers wrapped in Carbon Fibre
- 8.5 mm for PCB & Silicon layer

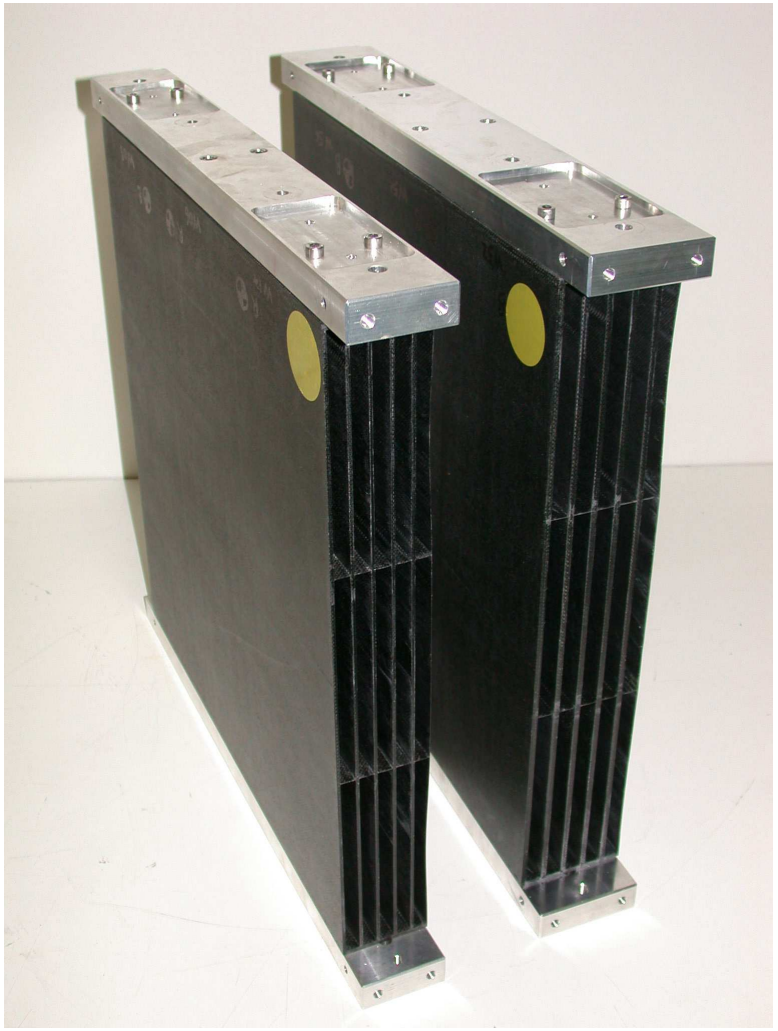
- PCB contains VFE electronics
- 14 layers, 2.1mm thick
- Analogue signals sent to DAQ

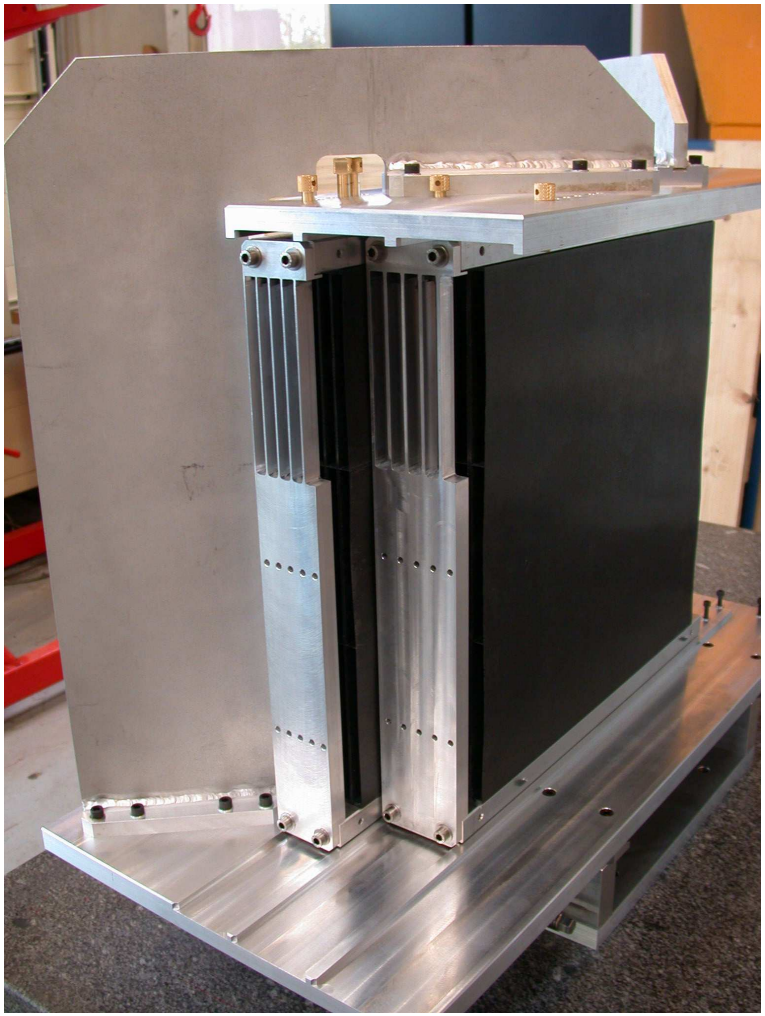




- 6x6 1x1cm^2 silicon pads
- Connected to PCB with conductive glue

Mechanical structure for TestBeam

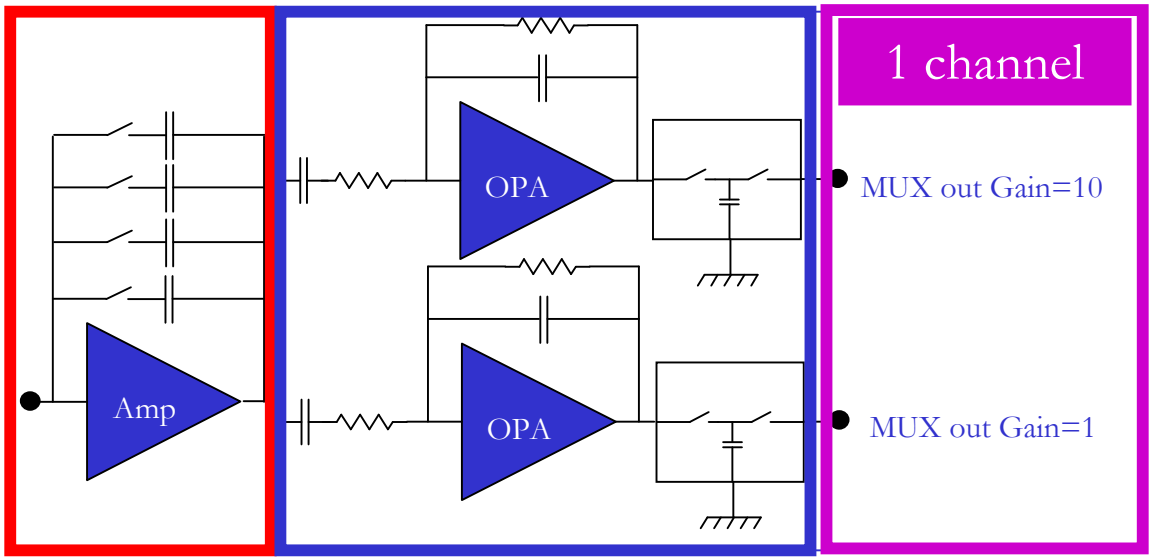




Very Front End Electronics

VFE consists of

- Preamp with 16 gains (gain selected offline)
- CR-RC shaper (~200ns), track and hold
- 18 channels in, one Multiplexed output



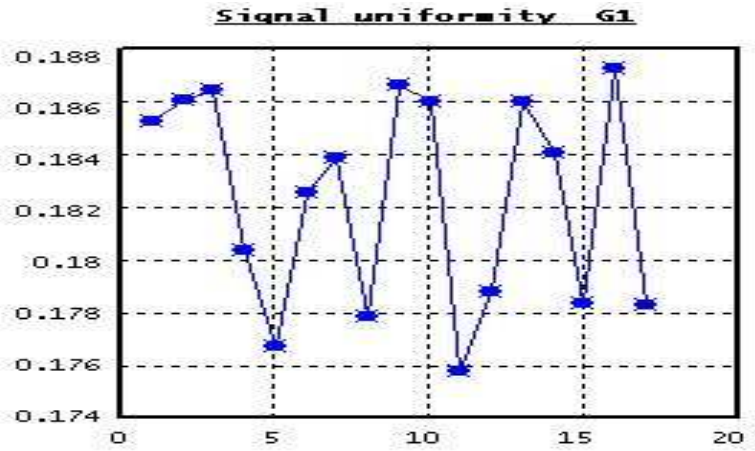
Each chip serves 18 channels

2 chips per wafer

Linearity: ± 0.2 %

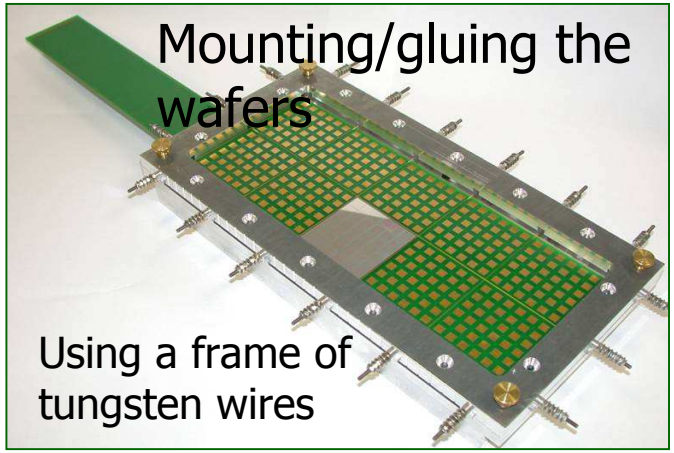
Range: ~1000 MIPS

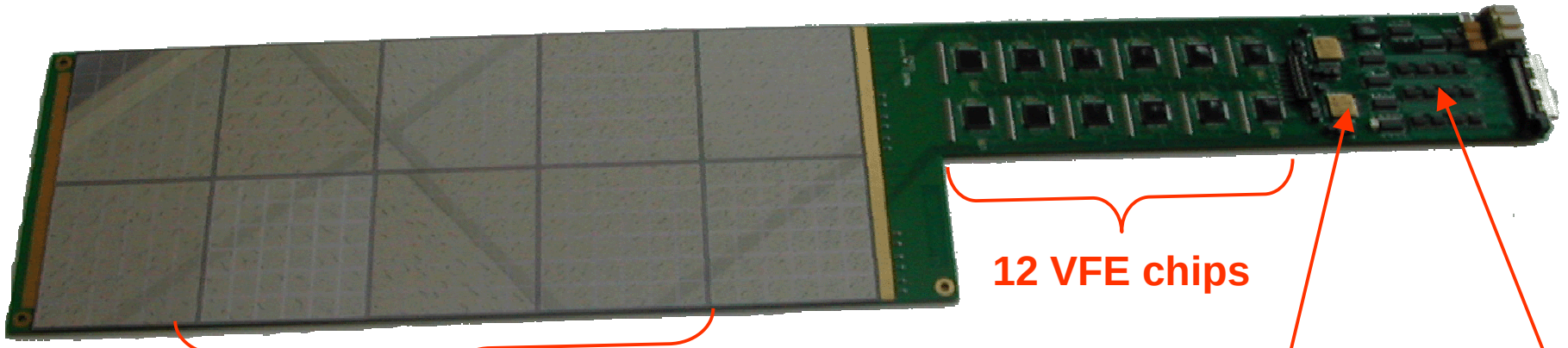
Crosstalk < 0.2%



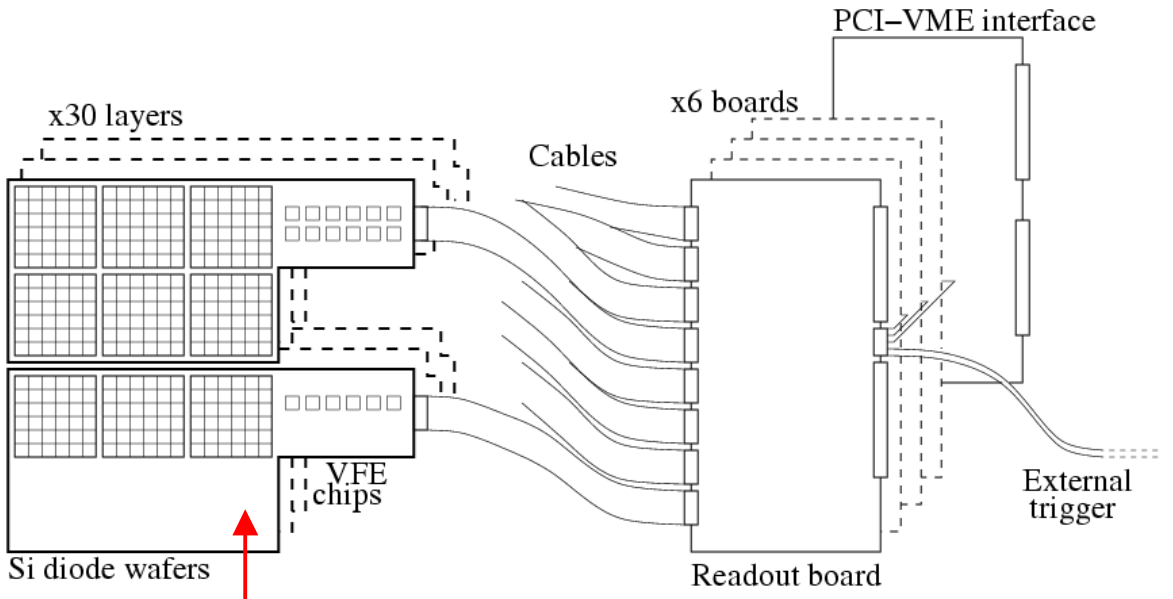
Production & Testing

- **PCB designed in LAL-Orsay, made in Korea (KNU)**
- **60 Required for Prototype**
- **An automatic device is use to deposit the conductive glue : EPO-TEK® EE129-4**
- **Gluing and placement (± 0.1 mm) of 270 wafers with 6×6 pads, 10 000 points of glue**
- **About 10 000 points of glue.**
- **Production line set up at LLR**





Prototype DAQ



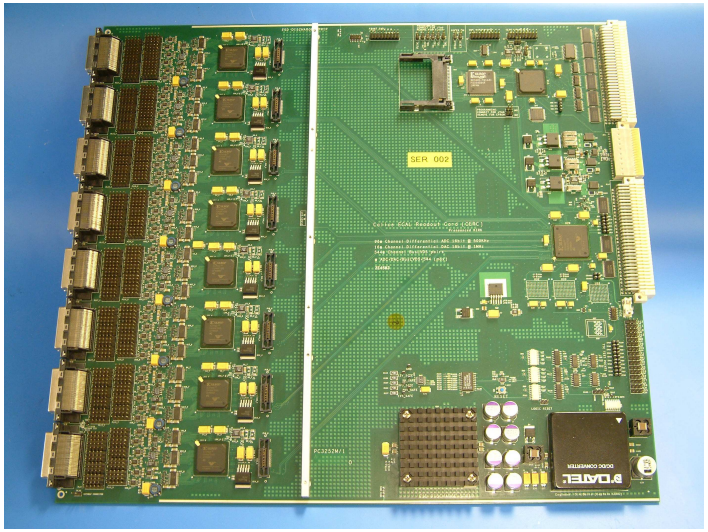
Layers face each other so have 2 types of half-filled VFE PCBs: right and left

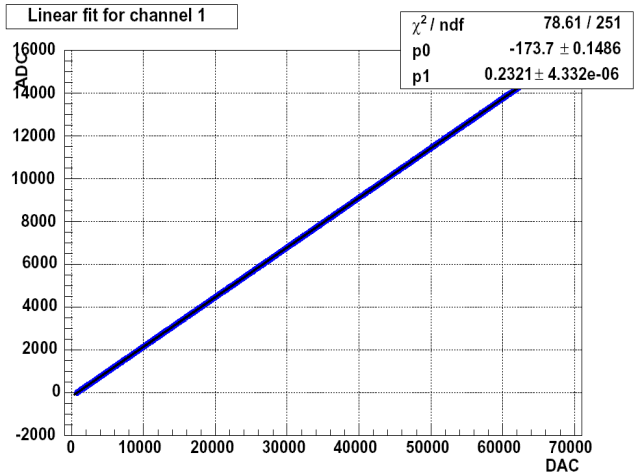
In 9U VME crate

- The 30 layers of VFE PCBs are read out through 6 readout boards when triggered
- The readout boards are housed in a 9U VME crate

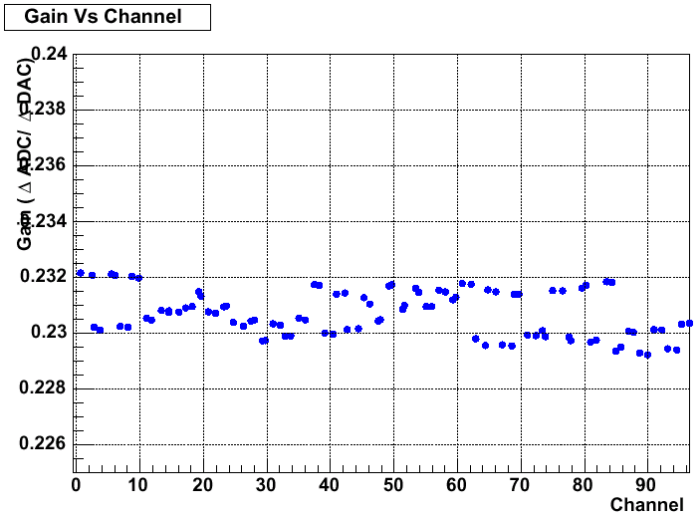
Prototype DAQ

- Use custom VME readout board
- Based on CMS tracker front-end board (FED)
- Uses several FPGA's for main controls
- Dual 16-bit ADCs (500 kHz) and 16-bit DAC
- On-board buffer memory 8 Mbytes. 1.6k event buffer, no data reduction





- Prototype design completed summer 2003
- Two prototype boards fabricated in November 2003
- Noise ~ 1ADC count
- Linear to 0.01%
- Gains uniform to 1%



System Tests

Extensive tests in Paris between April - June

- **Noise**
- **Calibration with DAC**
- **Cosmics**

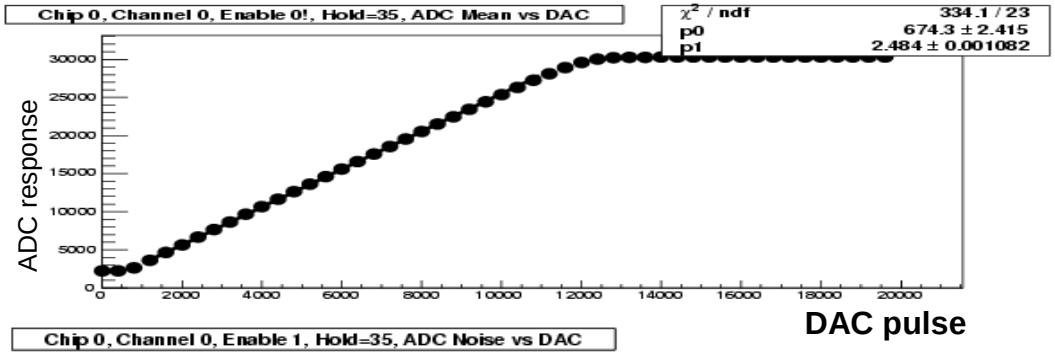
Aim To check

- **Problems: are there things which need to be changed?**
- **Uniformity: do all channels look similar?**
- **Dynamic range and signal/noise: are they sufficient?**
- **Optimisation: are there changes which will improve the system?**

System Tests

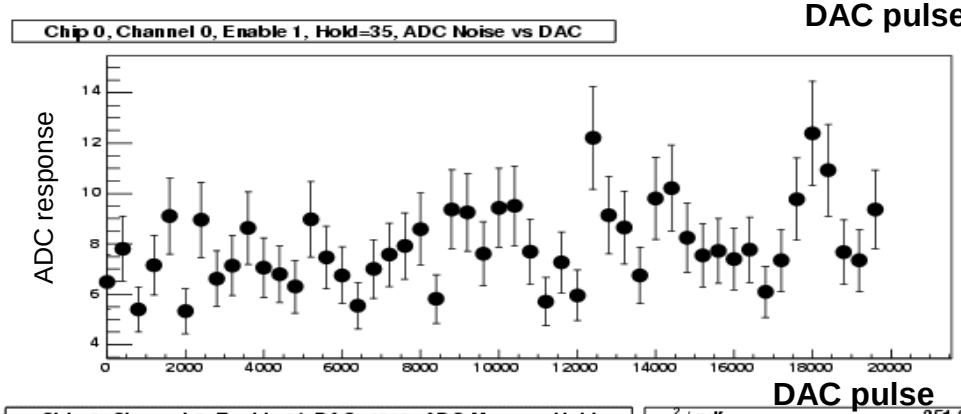
Linearity

- Progressively pulse DAC and readout channels ADC value
- Typical channel, gain x1, good linearity seen across system



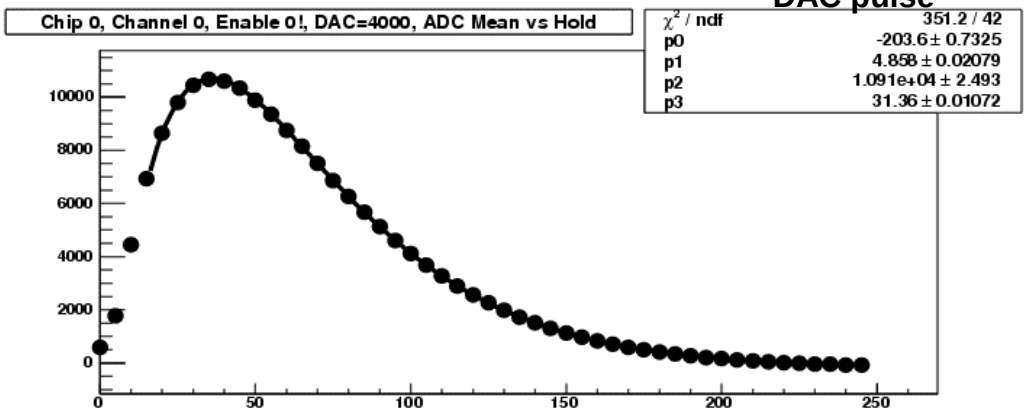
Noise

- Measure Noise as pulse DAC
- No large DAC dependence seen, uniform noise throughout system
- Noise ~ 7.5 ADC counts

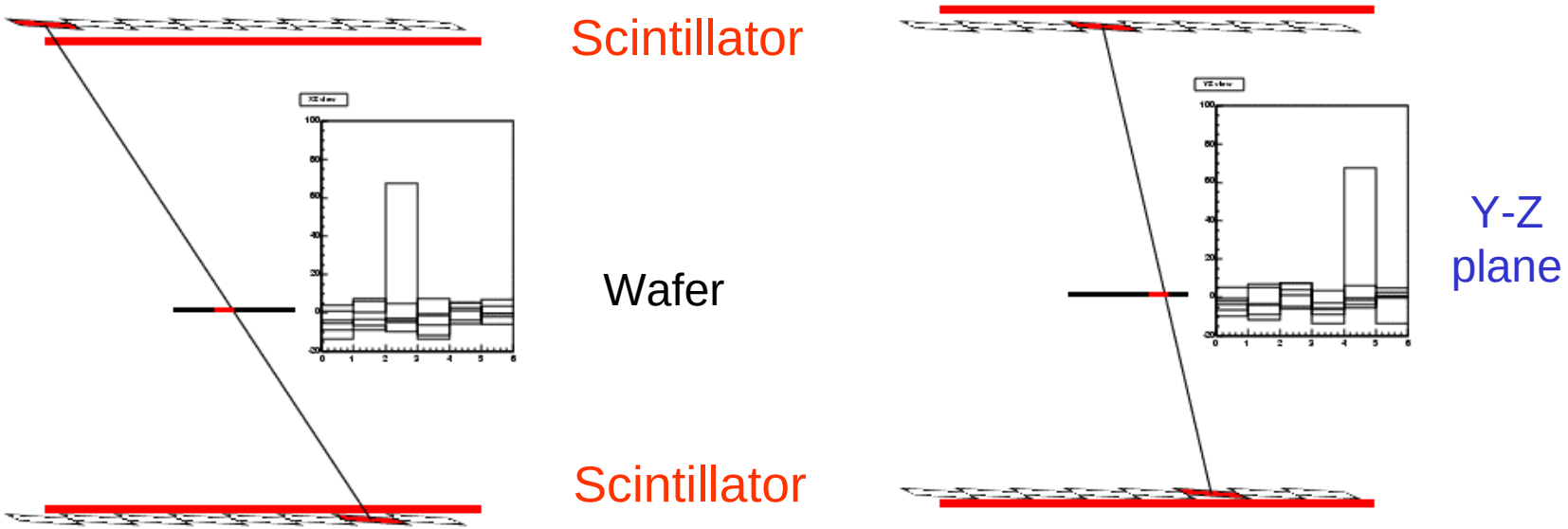


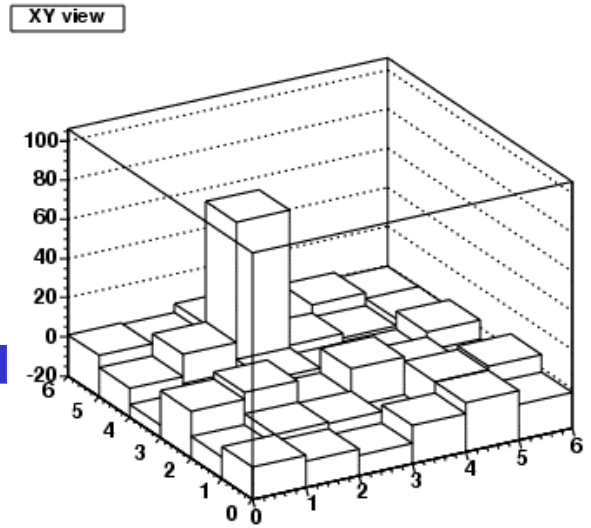
Timing

- Output signal is shaped by CR-RC circuit, shaping time ~200ns
- Fit xe^{-x} shape to response
- Shaping time = p3 = 31.36 units = 196 ns, good uniformity across system



Full Chain - Cosmics

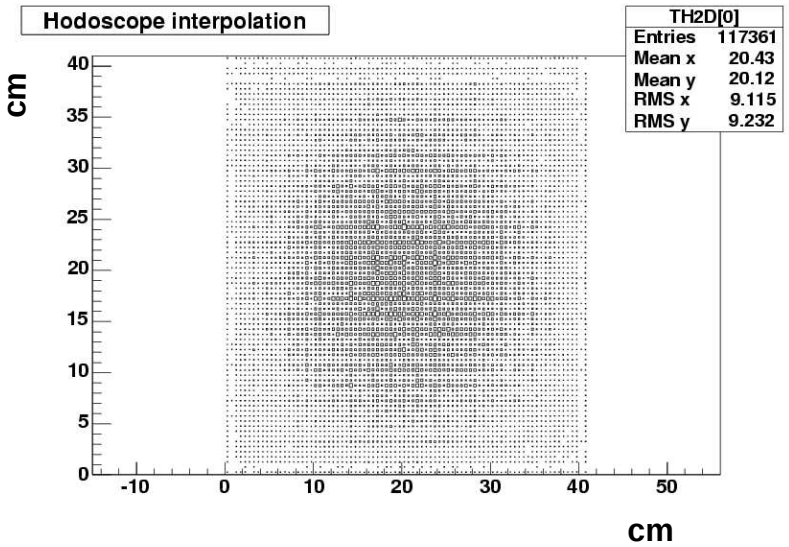


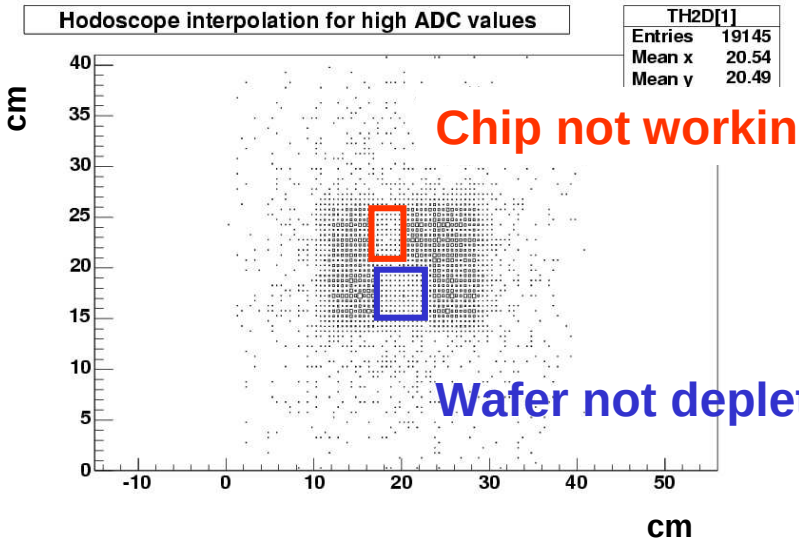


- **Example of Cosmic Event**
- **Passes through scintillators**
- **Extrapolated through silicon**
- **Appears as clear signal above background**
- **Use full readout chain for capture**

Cosmics Run

- Full PCB used in Ecole Polytechnique teststand, but…
  - Wafer 1 not depleted
  - Bad ADC on CERC for wafer 4; half the wafer has very high noise
- Ran over weekend 18-21 June
  - Total ~ 57 hours, 130083 events using RS232 readout
  - Around 90% have unique track from scintillators
  - Interpolate into plane of PCB; check for ADC value > 40



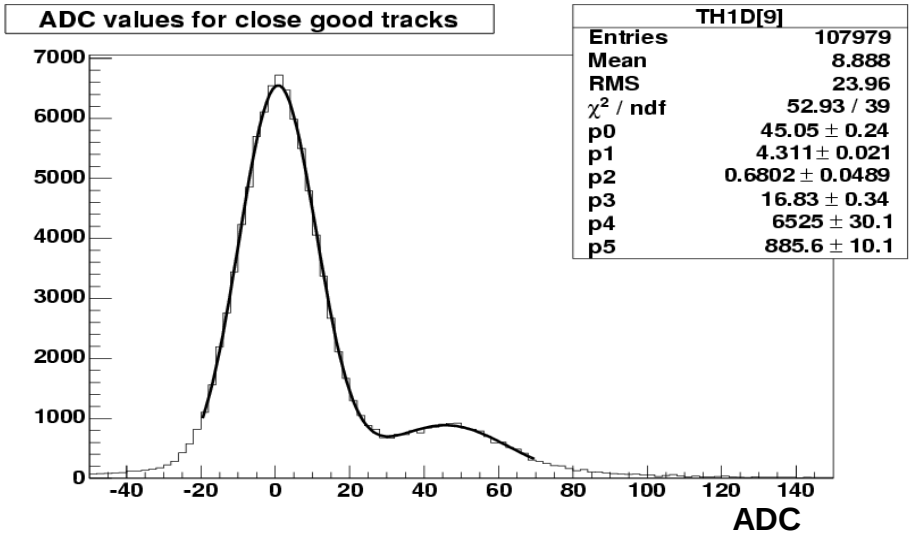


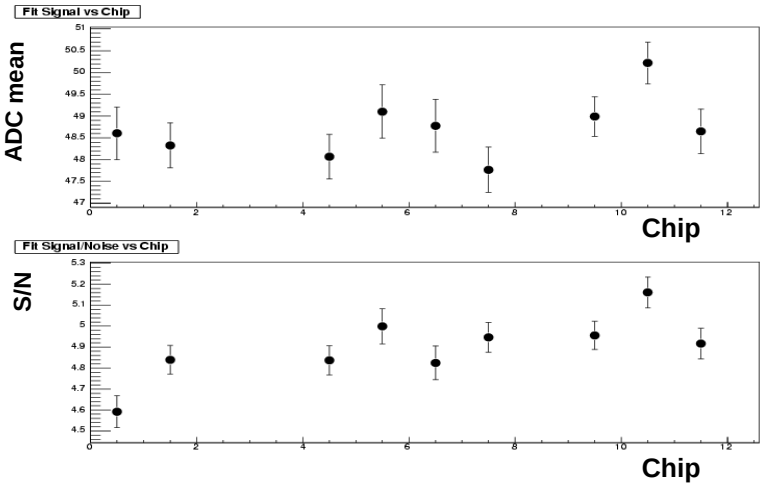
Chip not working

Wafer not depleting

Cosmics Signal

Select good channels and basic track quality cuts





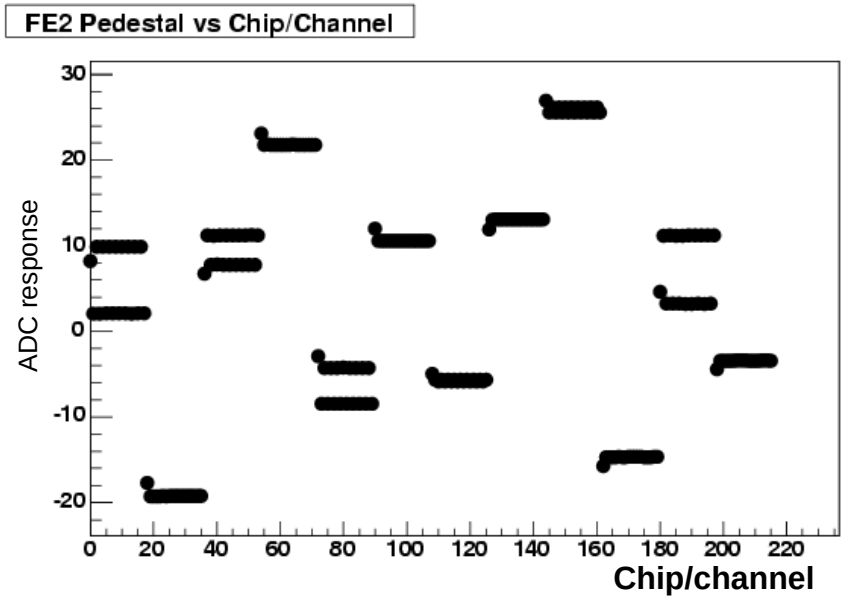
- Simple Gaussian fit given signal peak at 45 ADC counts
- But S/N = 4.3, i.e. noise is 10.5 counts, not 7 counts
- Perform fit, chip by chip – get better results
- Both uniform to ± 3% (tolerance on the wafer thickness)
- Fit gives higher signal ~ 49, and hence S/N ~ 4.9
- Once Common mode noise and full pedestal shift removed, expect S/N of 7 for peak value
- Gives range of 800 MIPS in current configuration

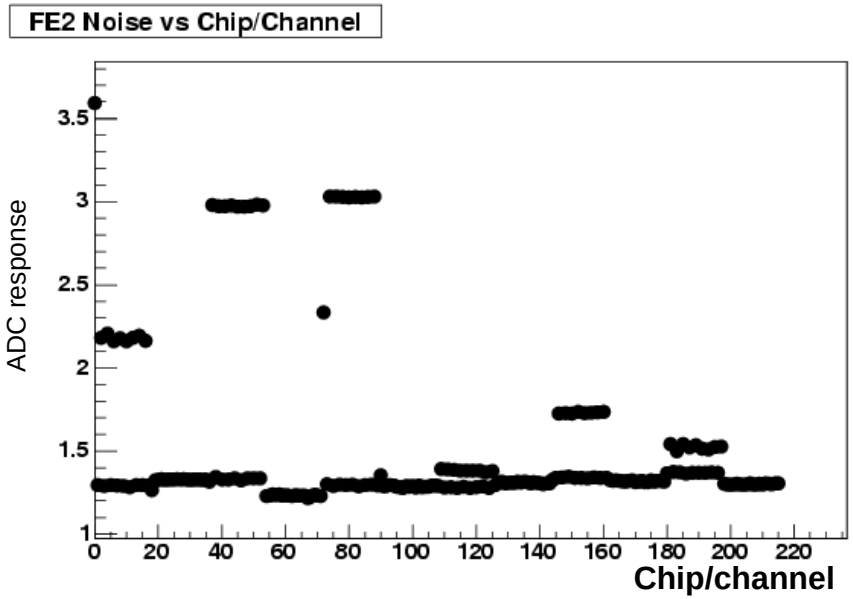
Very successful and useful testing in Paris

From tests to production

- Prototype tests completed successfully in June
  - Minor modifications for VFE-PCB and CERC identified
- VFE-PCB released for production in July
- CERC redesign was finalised in August
  - Several changes made to optimise board performance
  - Production boards sent out for fabrication in early September
  - 2 ½ Week turnaround ; but delayed by four weeks
  - Boards delivered in late October
  - Board line tests completed successfully
  - Two boards delivered to IC for testing 7 days ago
  - Remaining 7 boards ready for assembly when design verified
- Full data path of CERC completed in November
  - Back end data path completed
  - Able to read out boards in designed way
  - Some work to do on increasing readout rate

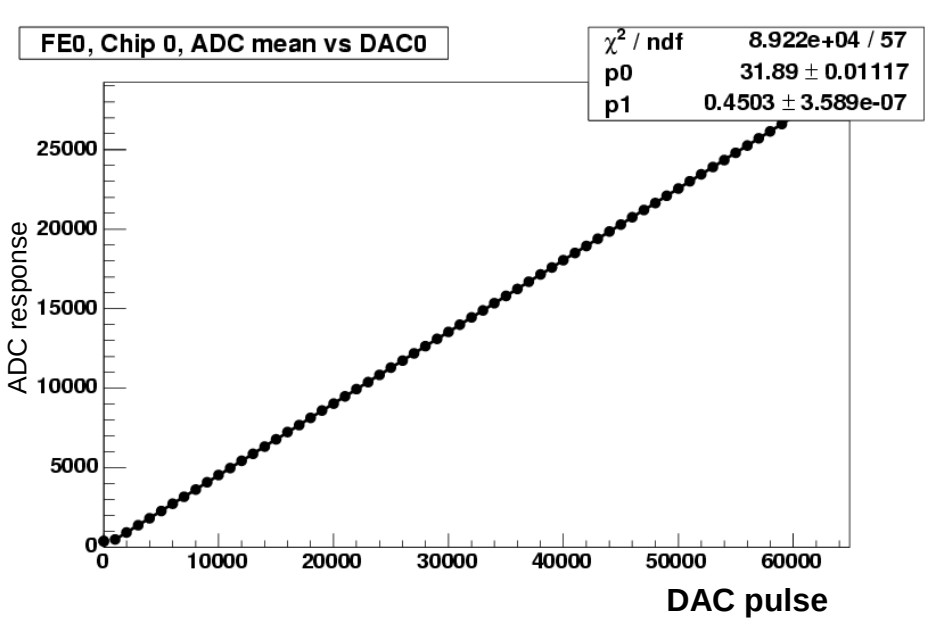
Initial tests with Production boards

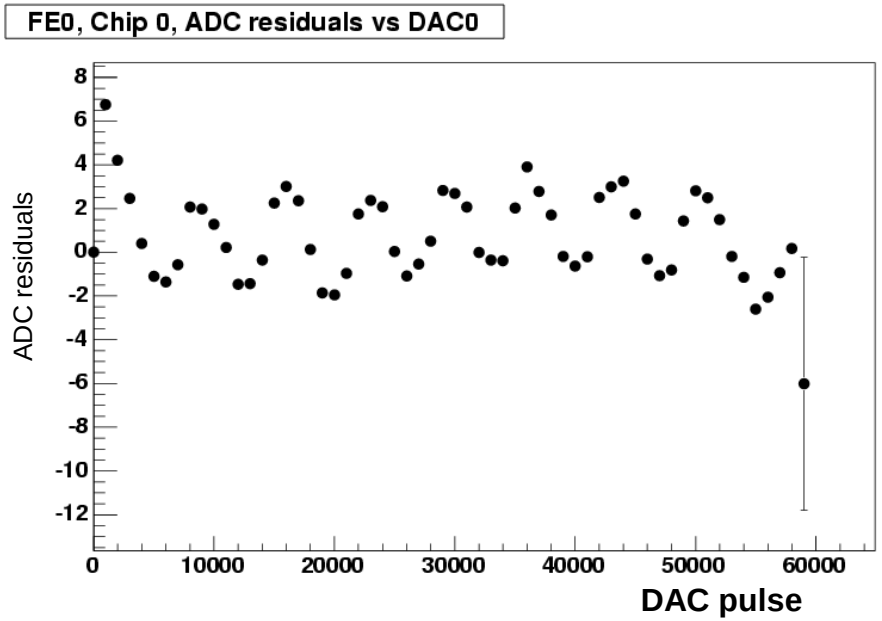




- **Two production quality boards delivered to Imperial last week**
- **Undertaking systematic tests of all channels**
- **Pedestals across all channels are close to zero (only using half range)**
- **Noise per channel ~ 1.2 ADC counts**
- **Structure due to known bit setting issue in data link (vlink)**

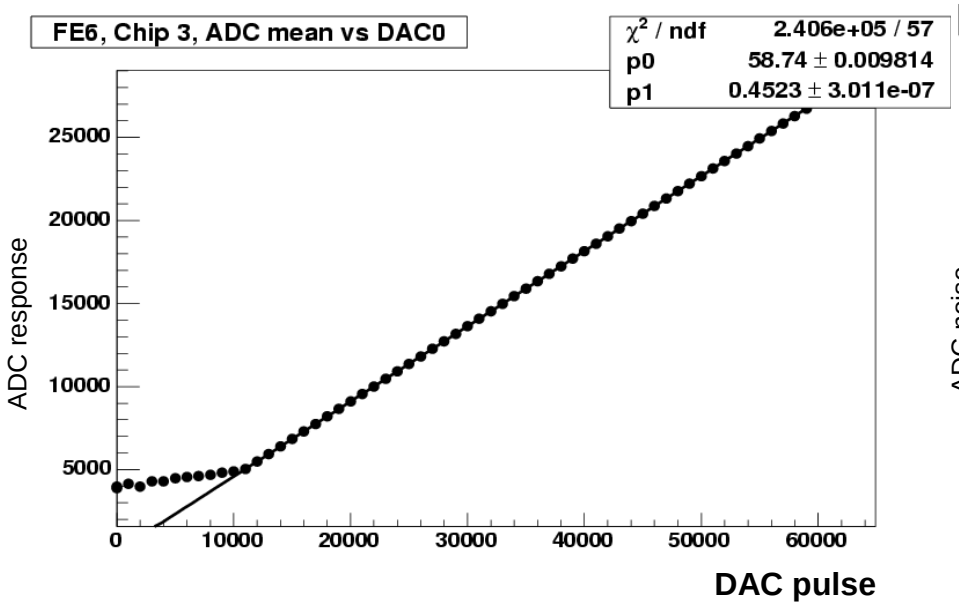
The Good

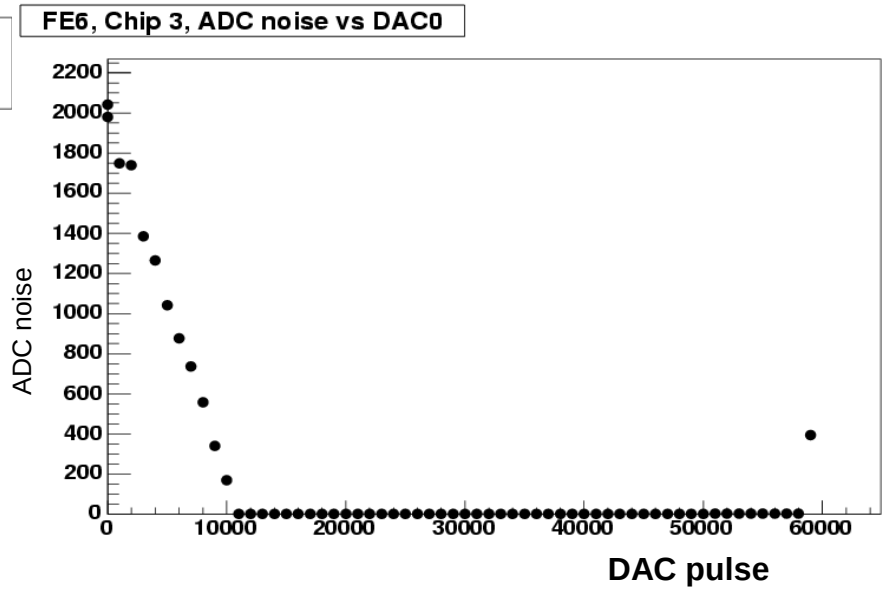




- **Check the internal consistency by pulsing DAC and reading out ADC**
- **Fit for the linearity of the system**
- **Gain ~ 0.45 (close to maximum possible of 0.5)**
- **Fit residuals show structure but at acceptable small level**
- **Many channels working like this**

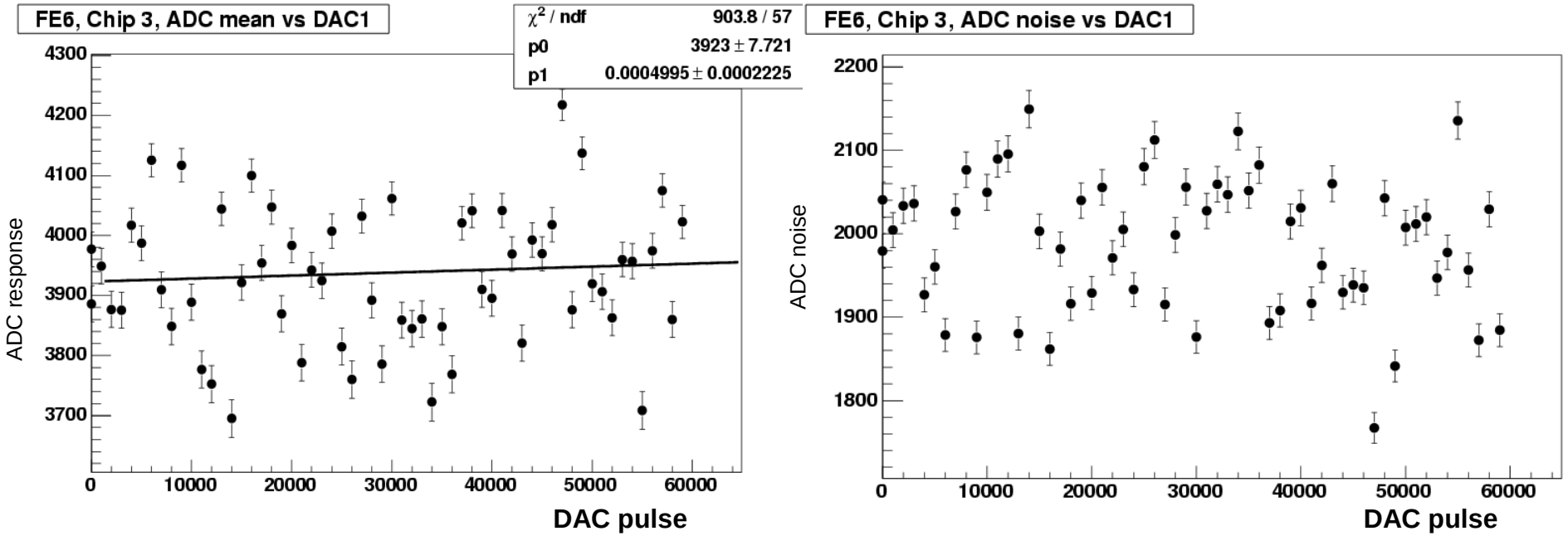
The Bad





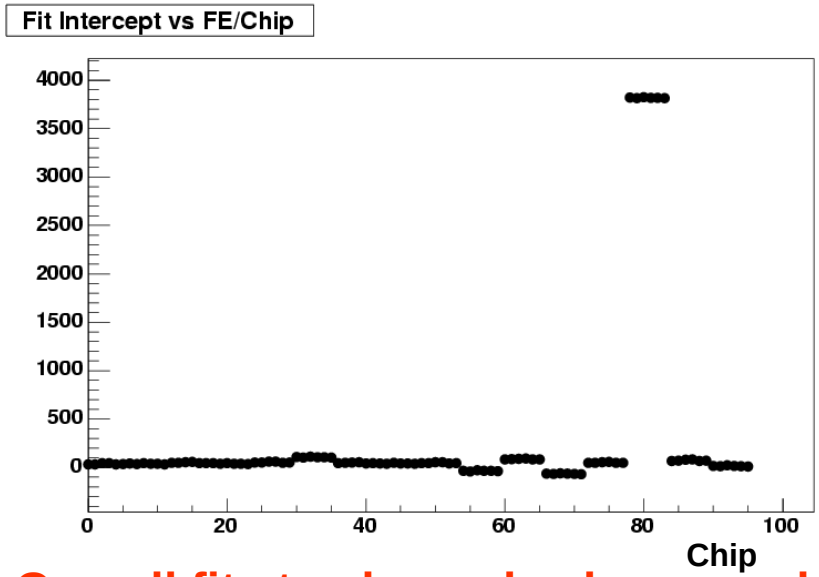
- See problems with some channels / Front ends
- At low DAC values (< 10000) have high ADC readout
- Also see high noise in this region – same effect
- Do not see this effect in prototype boards
- Points to possible modifications to Op-Amp from test to production

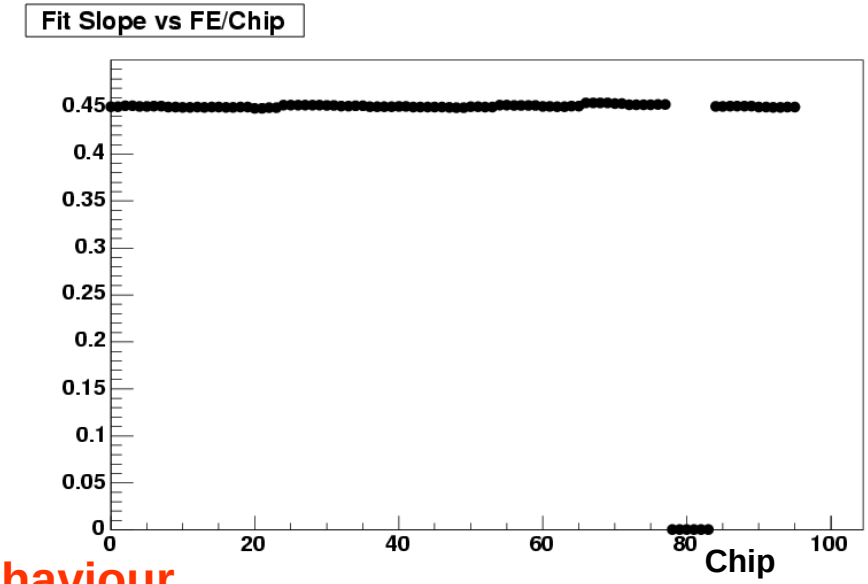
The Ugly



- Look at channels with DAC set to zero, while other channels pulsed
- See pedestal sitting at ~ 4000 ADC counts
- Noise once again at ~ 2000 ADC counts
- Again probably due to instability of DAC at low end
- Not seen on test boards
- May require some form of intervention on boards

Overall: in pretty good shape





- Overall fits to channels show good behaviour
- Intercepts are very close to zero as expected
- Good consistent gain (~ 0.45) and linearity
- A Few problems:
  - Instability at low DAC values, high noise
  - 3 complete Front ends not responding on second production board
  - Individual DACs and channels not working
- Need to debug, prepare changes, implement on other 7 boards for assembly

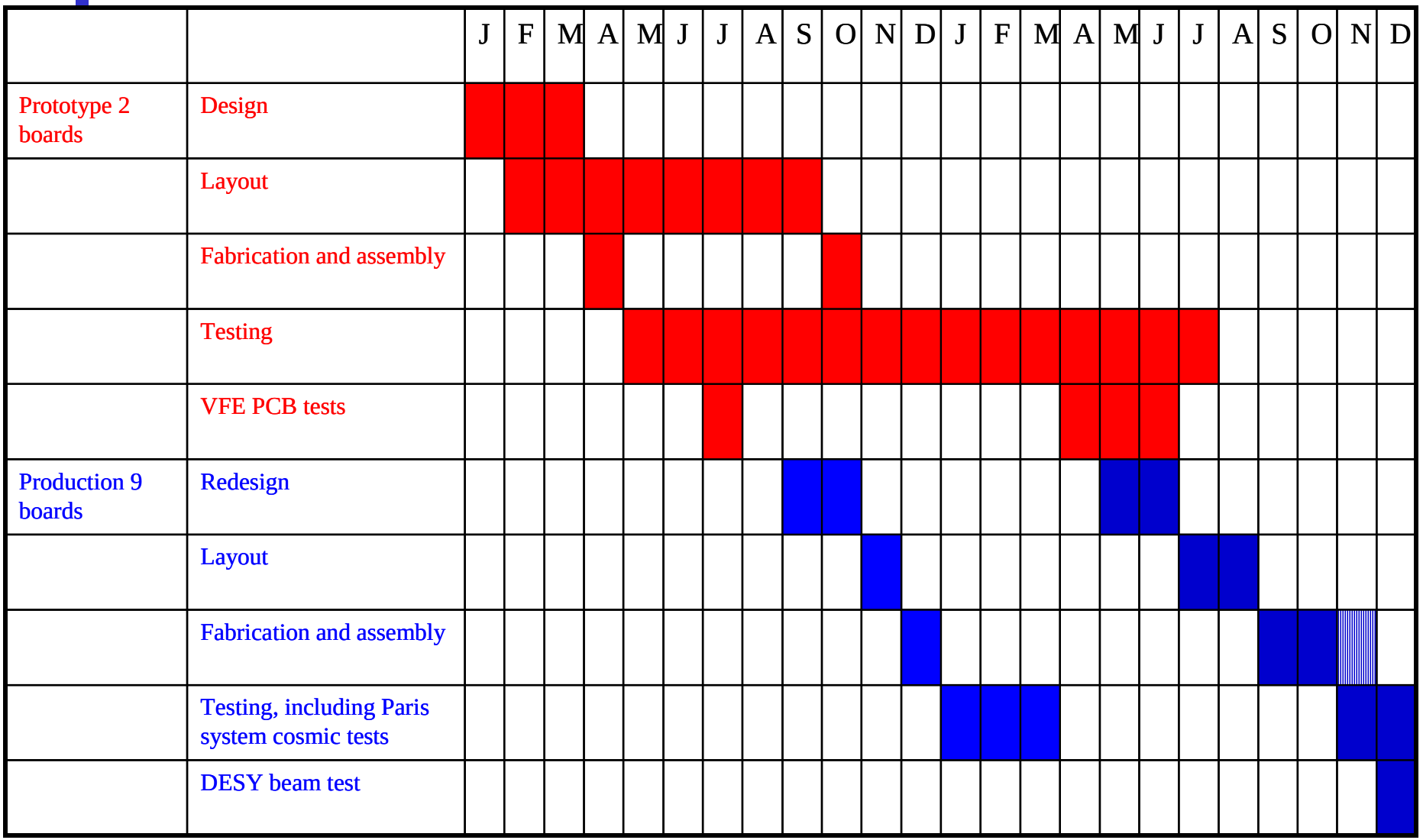
DAQ readout ideas

- **Will have Custom RAW data format; Linux only**
- **Will convert to LCIO format using calibration and alignment data; most users will only see LCIO**
- **People involved with calibration and alignment will have to use RAW data format**
- **Use ‘Records’; Contain objects of classes that have been registered with the DAQ**
- **Means typesafe insertion and access; Object are never removed!**
- **Actual exact class definitions are still in flux – firmware still evolving**
- **Will use CVS at RAL once data format/firmware stable**
- **George may mention more ideas about this later**

Key financials

		Original	Current
Prototype	NRE	2.5	2.8
(2 boards)	Components	8.0	8.1
	Fabrication	1.0	2.4
	Assembly	4.0	8.2
Production	NRE	2.5	6.1
(9 boards)	Components	36.0	36.6
	Fabrication	4.5	7.2
	Assembly	13.5	13.6
Cables		15.0	2.8
Total		**87.0**	**87.8**

Time Lines


J F M A M J J A S O N D J F M A M J J A S O N D
Prototype 2 boards
Design
Layout
Fabrication and assembly
Testing
VFE PCB tests
Production 9 boards
Redesign
Layout
Fabrication and assembly
Testing, including Paris system cosmic tests
DESY beam test

Future Plans

- Hope to complete final boards in the next month
  - Get boards fully debugged
  - Release 7 boards for assembly
- Move to Ecole – Polytechnique for Cosmic testing
  - 10 layers of silicon in Cosmic teststand
  - Full readout debugging
- Move to DESY during December
  - Undertake first low energy electron tests
  - Need one full crate working for initial runs
  - Build system and DAQ progressively as components become available
  - Prepare full DAQ / MC / Analysis chain
- Prepare integration with HCAL; Ordering 7/8 boards from RAL
  - Significant complication in DAQ due to multiple crates

Conclusions

- **Great deal of progress over the past year**
- Intrinsic performance of test boards appears good
- Captured Cosmics data with full detector chain
- Good initial results: S/N, Linearity, Crosstalk
- Production boards now under test
- Performance encouraging, some (small) problems
- Send remaining boards to assembly soon
- Data format and readout details to be finalised
- 10 layer silicon tests in Paris; then to DESY