Plans for Workpackage 2, Data acquisition

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- **Introduction**
- **Funding level from PPARC and expectation from EU**
- **Discussion of R&D**
- **Plans, start-up**

Introduction

Three parts to the DAQ system:

- **On detector: Very Front End (VFE) to Front End (FE)**
- **On detector to off detector**
- **Off detector receiver**

Have produced a concept for a DAQ system and will investigate its possibility and potential bottlenecks.

Generic system, apply to HCAL as well as ECAL (other detector systems?)

Based on commercial hardware, not bespoke.

Identify areas which could effect overall design - not just DAQ - e.g. need for FE. Connection directly from VFE to off-detector?

Tasks

Task 2.1: Readout multiple VFE ASICs

Task 2.2: Understand data transfer of $\sim$ GByte/s on 1.5 m PCB

Task 2.3: Options for network switching

Task 2.4: Transport of configuration, clock and control data

Task 2.5: Prototype off-detector receiver

Funding level from PPRP/PPARC

The research programme was generally well received by referees and interest was shown in the open session to the PPRP.

The closed session also did not question the programme too deeply.

However, the PPRP thought some of the work too “generic”, e.g. the task on building PCI cards and cut new-money request of £350 k by £125 k.

Value well above the total costs of their proposed task removal. Note that total equipment cost was about this amount.

Cuts could only come from staff, but we were ’saved’ by the delay in the start-up and extension to 3.5 year project.

Essential programme same.

and extended....

Funding level from EUDET

EUDET: Detector R&D towards the International Linear Collider is a bid within the Sixth Framework Programme for a contract for Integrating Activity implemented as an Integrated Infrastructure Initiative (I3).

The key idea is I3, e.g. a generic DAQ system, fits. Need "matching" funds, which we thought we would have and now do.

21 institutes requested about 8.7 MEUR (award 7 MEUR) for a four year grant to start 1 January 2006.

2.9 MEUR (award 2 MEUR) requested for Calorimetry (JRA3) coordinated by F. Sefkow (DESY) and C. de la Taille (LAL, Orsay)

Technically, R&D

Applied for funds to provide DAQ system for prototype systems built.

Build on R&D done within PPARC grants to "mass produce" for real systems.

Use of PCI cards in PC farm, linked to electronics via a switch.

A complete system to be ready by September 2008 (revise?)

Implications for CALICE-UK

Funding

Due to uncertainties in award from PPARC, UCL put in a bid as an administrative cover for other DAQ interested universities: ICL, RHUL, Cambridge, Manchester.

- **23.2 kEUR travel, award 14 KEUR**
- **225 kEUR personnel, award 150 kEUR**
- **150 kEUR consumables, award 100 kEUR**
- **(80 kEUR indirect costs, award 53 kEUR)**

Total $\sim$ 480 kEUR, award 320 kEUR. (Final amount almost set in stone)

With PPARC money, perform R&D for a concept; with EU money will actually put this into practice with a real prototype. Solidify our proof of concept and allow us to make a stronger report for the TDR.

EU money will more than make up for cut imposed by PPRP.

Task 2.1: Readout multiple VFE ASICs

Imperial College

Build a PCB to hold 32 ASICs provided by LAL/Orsay, thereby reading out 500 channels.

Get experience of issues involved and FE requirement

Feedback to new designs and redo study as new versions are produced

Similar PCB to readout the MAPS will be used

Independent of other tasks - to start in 2007

Task 2.2: Transfer of GB/s on 1.5 m PCB

Cambridge, UCL

Study transmission line performance on 1.5 m board.

Mixture of bench testing and CAD modelling.

Simulate final board by connecting two FPGAs - no need for real ASICs.

Results fed back to ASIC designers.

Use electrical or optical (chip-to-chip) connection.

Optical chip-to-chip is an active area of industrial research.

Task 2.3: Options for network switching

Manchester, RHUL, UCL

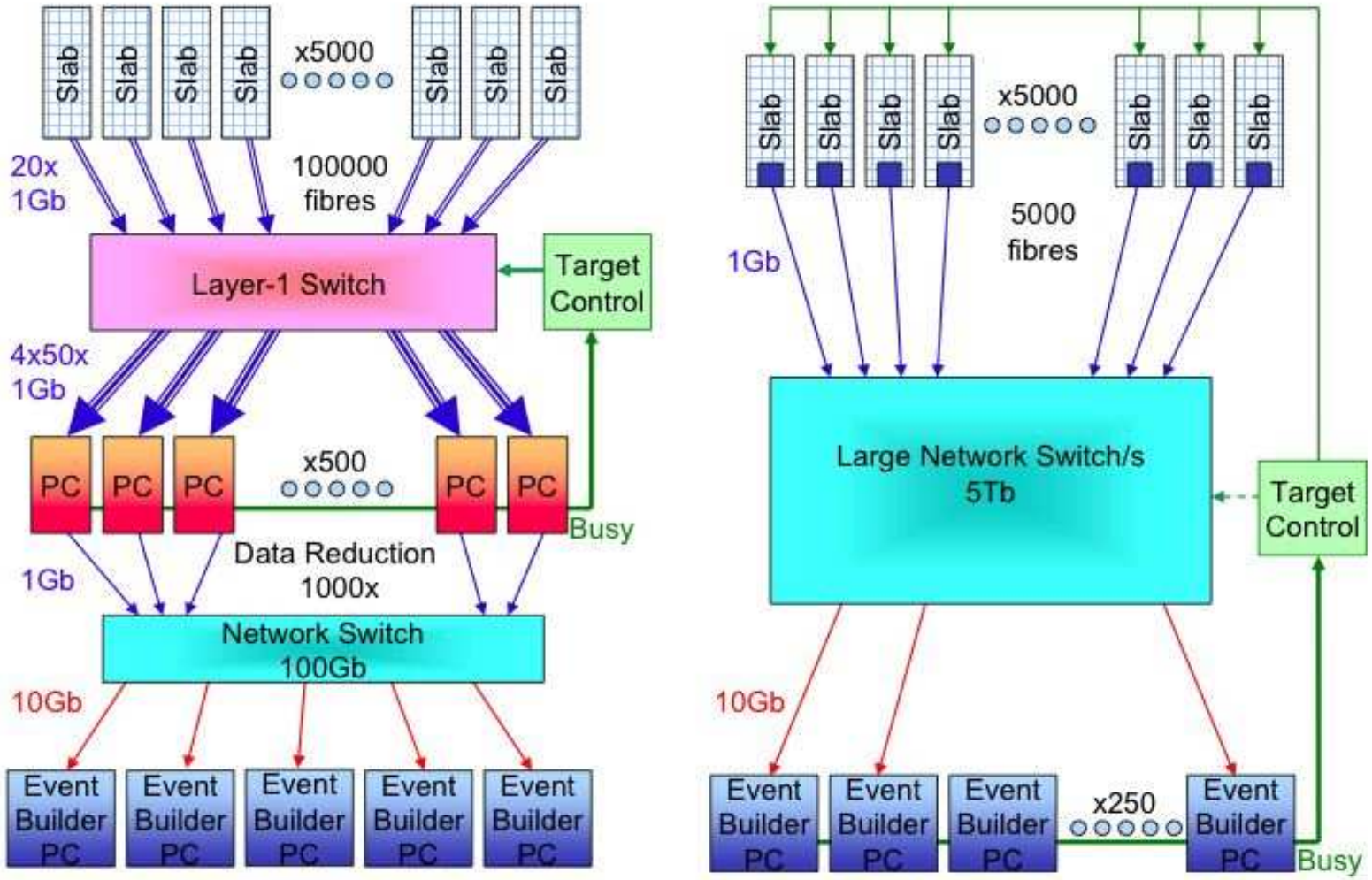
Consider amount of space on the detector and minimise

Model and test data rates with ILC timing structure with small networks and fast switching.

Optimal groupings of switches and PCs.

Standard network and/or optical network?

Evaluation of “layer 1” optical switch for re-routing data to multiple destinations.


Slab
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10Gb
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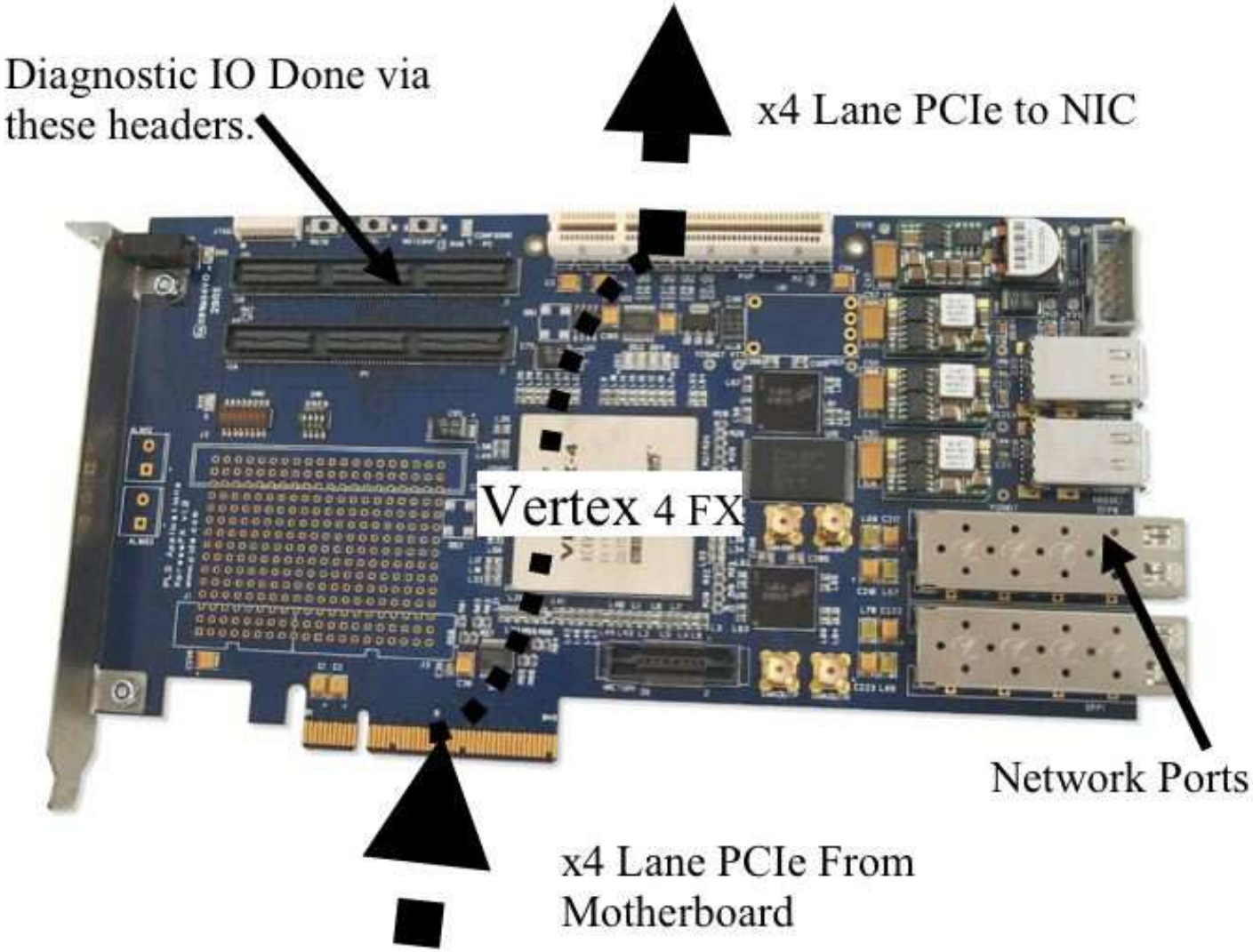
Networking studies at Manchester

Get PCI 'spy' card from PLDa. Data flows though FPGA.

Want to purchase Standard card now. Free upgrade to faster version after Christmas.

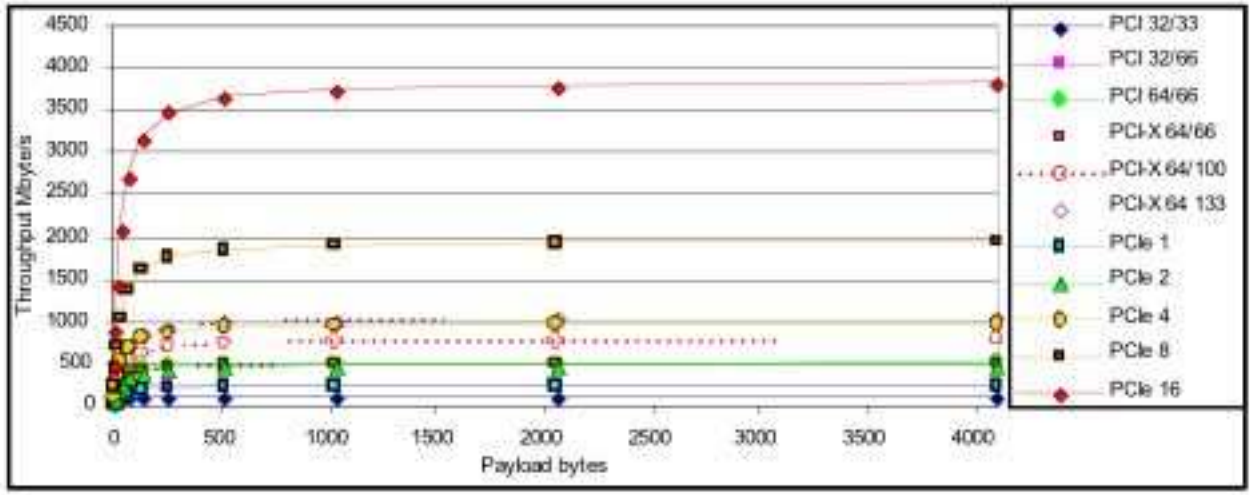
Off the shelf PLDa, PCI XpressFX. Has x8 lane PCIe input, x4 lane PCIe output, plus Vertex-4 FX-60 FPGA.

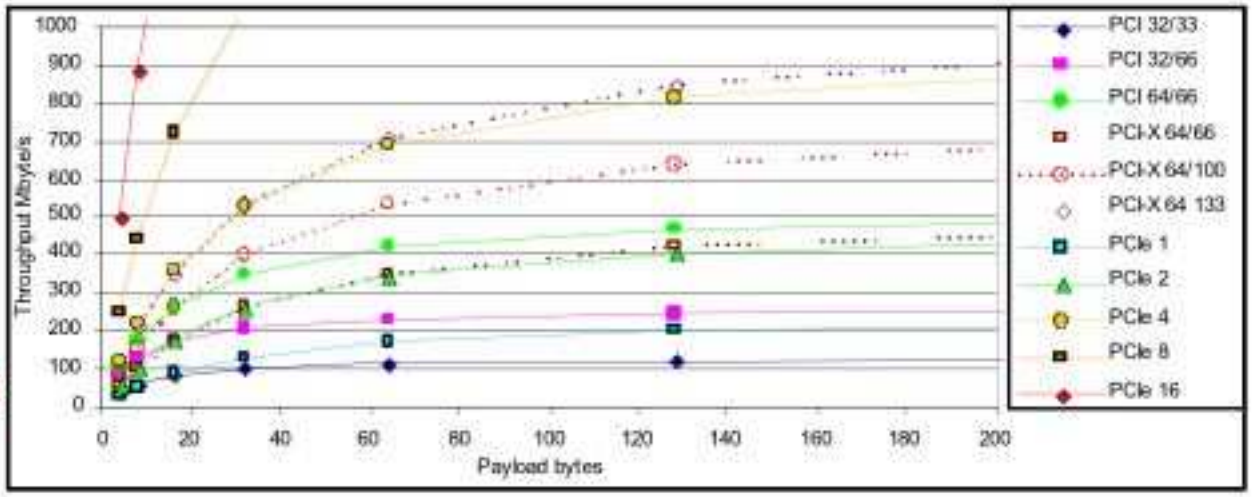
Connect 4 lanes from input to output via FPGA, and decode the PCIe packets as they pass through with custom firmware.


Diagnostic IO Done via these headers.
x4 Lane PCIe to NIC
Vertex 4 FX
Network Ports
x4 Lane PCIe From Motherboard

Calculated PCI PCI-X and PCI-Express Bus Transfer Rates

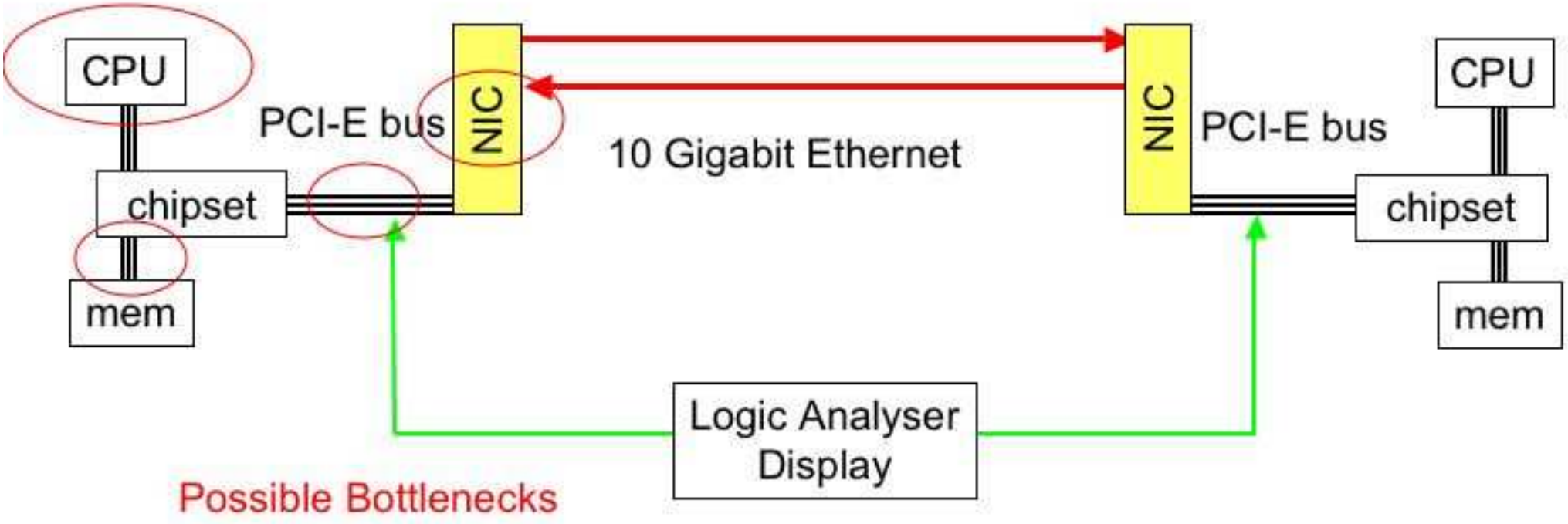
- PCI Activity
  - Read overhead 3 clocks
  - Write overhead 2 clocks
- PCI-X
  - Read overhead 4clocks
  - Write overhead 4 clocks
  - No mmbc limits
- PCI-Express
  - Lane clock 2.5Gbit
  - PHY+Datalink+Transaction overhead 28 bytes
- Best possible theoretical transfer rates
- NO Interface commands
- 4 lane ~= PCI-X 64bit/133MHz
- Wont do 10 Gbit





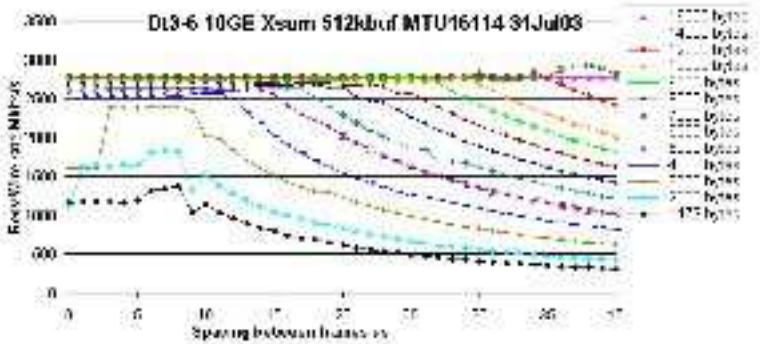
PCI-Express Bus & Gigabit Ethernet Activity

- **PCI Activity**
- Logic Analyzer with
  - PCI-E Probe cards in sending PC
  - Gigabit Ethernet Fiber Probe Card
  - PCI-E Probe cards in receiving PC
- Examine how the PCI-E bus actually transfers data and control

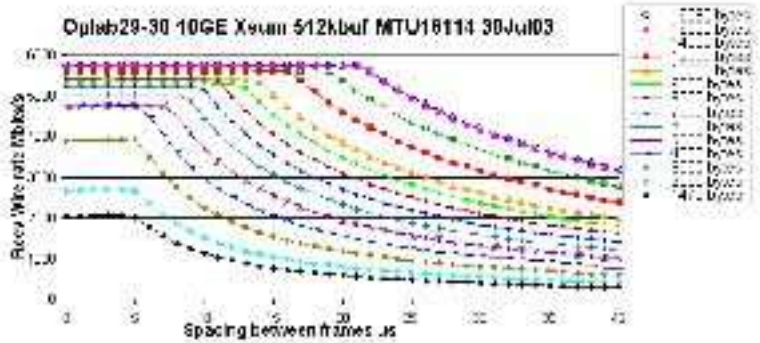


10 Gigabit Ethernet: UDP Throughput

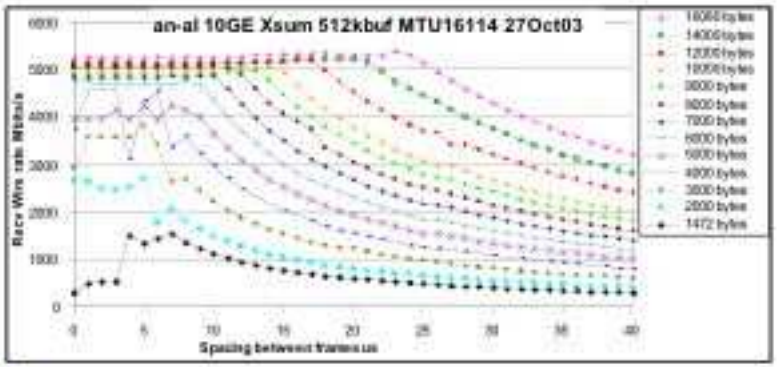
- 1500 byte MTU gives ~ 2 Gbit/s
- Used 16144 byte MTU max user length 16080
- DataTAG Supermicro PCs
- Dual 2.2 GHz Xenon CPU FSB 400 MHz
- PCI-X mmrbc 512 bytes
- wire rate throughput of 2.9 Gbit/s



- CERN OpenLab HP Itanium PCs
- Dual 1.0 GHz 64 bit Itanium CPU FSB 400 MHz
- PCI-X mmrbc 4096 bytes
- wire rate of 5.7 Gbit/s

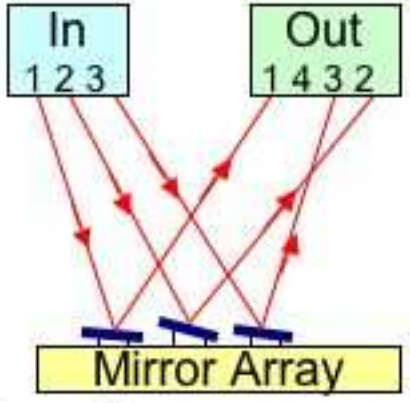


- SLAC Dell PCs giving a
- Dual 3.0 GHz Xenon CPU FSB 533 MHz
- PCI-X mmrbc 4096 bytes
- wire rate of 5.4 Gbit/s



Optical (Layer-1) Switching

New tech – array of programmable mirrors
We would like to investigate two applications:



1)Programmable optical patch panel
- Easily switch to redundant fibres remotely
- Useful for grouping fibres from physics region (e.g. logical grouping)

2) "Router" (able to switch at 10Hz for many years)
- Can change data destination per bunch-train.
- Regulate load by sending data directly to free resources
- As PC's become busy or fail, data is directed to a backup node.

Task 2.4: Transport of config., c & c data

UCL

All slabs need synchronising signals (Clock) and configuration (Control) signal. E.g. “bunch-train-start” signal.

Using commercial components which will all have a different clock to be synchronised.

With 6000 FPGAs in the detector, remote reprogramming - booting/loading - is essential.

This will reduce down-time. And reduce the complexity of the FE system.

Less material, cost and corruption. Regular re-programming reduces the risk of SEUs.

Task 2.5: Prototype off-detector receiver

Cambridge, RHUL, UCL

How much data can go into one PC, presumably not all of the ECAL.

Build a test system to measure realistic rates.

PCI receiver card with multiple fibres.

PC with multiple PCI cards.

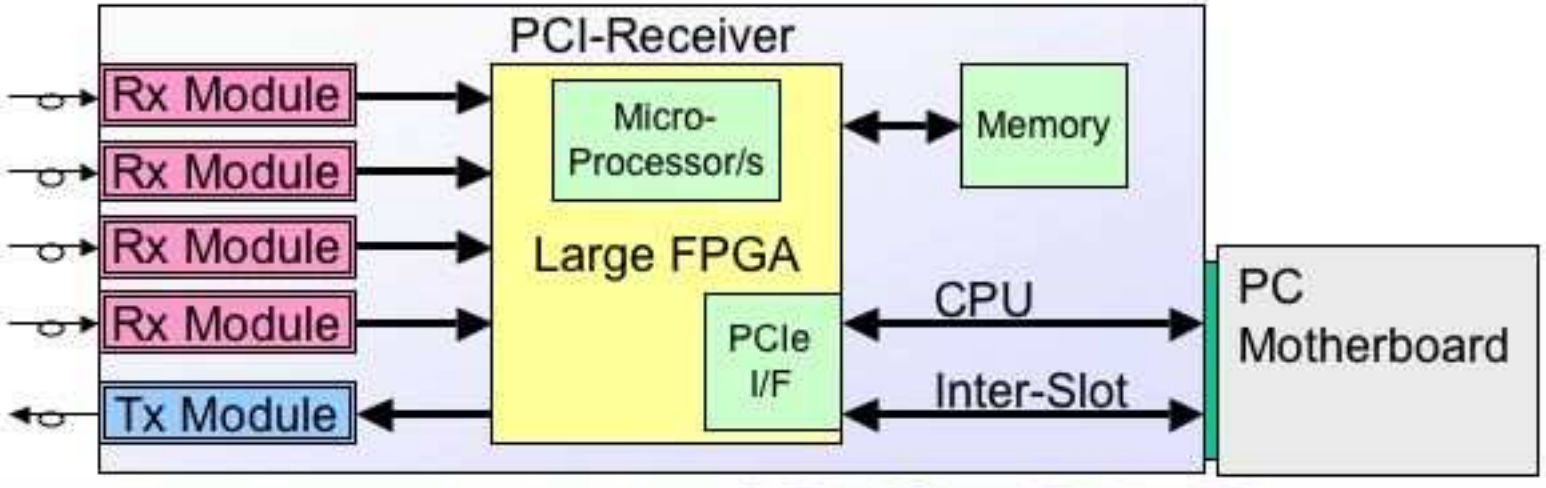
Data reduction, e.g. isolated hits, before full event reconstruction.

Receiver

Custom PCI-Express card designed to test:

- Data transfer standards/customisations
- Capabilities of PCIe - including local card-to-card links.
- Capabilities of FPGA to do data-processing
- Use as Clock+Control source (more later)

Rx/Tx module plug-in to allow card to be a data-source (slab-less testing)



EUDET Task: providing DAQ for prototypes

Will provide DAQ for prototype calorimeters in test beam.

Production of PCI cards, networks, etc., already planned.

Will happen towards the end of our EUDET/PPARC grant, i.e. we have already bench-tested the system.

Provide support for running our equipment at test beams.

Plans

Need to have a start-up meeting; some tasks need more coordination than others due to interdependency.

(Phone) Meeting in September.

- **Consider having meetings every month**

- **Do we need big meetings or some things be delegated on a task level? Task 2.1 is not interconnected, but Tasks 2.3 and 2.5 obviously are.**

M. Warren and I have been writing a note on our plans for DAQ. Concept and plans for R&D. Will help us get going. Release soon.