



Paths between VFE Chips and the FE Chip :

- . Clock and Control to VFE chips
- . Data from VFES to FE chip
- . Readout Token and Monitoring
- . Constraints: 1.2 to 1.8 m slab length - tight power budget

Technology and Architectural Choices:

- . Copper, or must we go to Optical ?
- . CMOS, LVDS (,CML,...) ?
- . Composite Clock and Data ? ... Clock recovery, Clock-Data encoding
- . Shared lines or point-to-point ?
- . Buffering, redundancy ?

SLAB Design options include :

- . Single 1.8 m PCB .. Can this be manufactured ?
- . Multiple Panels "stitched" together ?
- . Flexible circuit ?
- . VFE ASIC factors: these strongly effect the on-slab communications :
 - . # pads, available functions: LVDS, SERDEC, clock recovery ?
 - . Bunch-train buffering ?
 - . Zero suppression ?

Paper Studies :

- . Estimating data flows for different beam scenarios and VFE functionalities
- . Possible PHYs : e.g. Z_0 & C_0 of feasible PCB traces, pre-emphasis,,,
- . Proposing optimal architectures
- . Interaction with ASIC and slab design groups

Experimental Work :

- . Design and build of test PCB with "best-guess" solutions and variants
- . Evaluate
- . Interaction with ASIC and slab design groups (again)
- . Tune model
- . Iterate

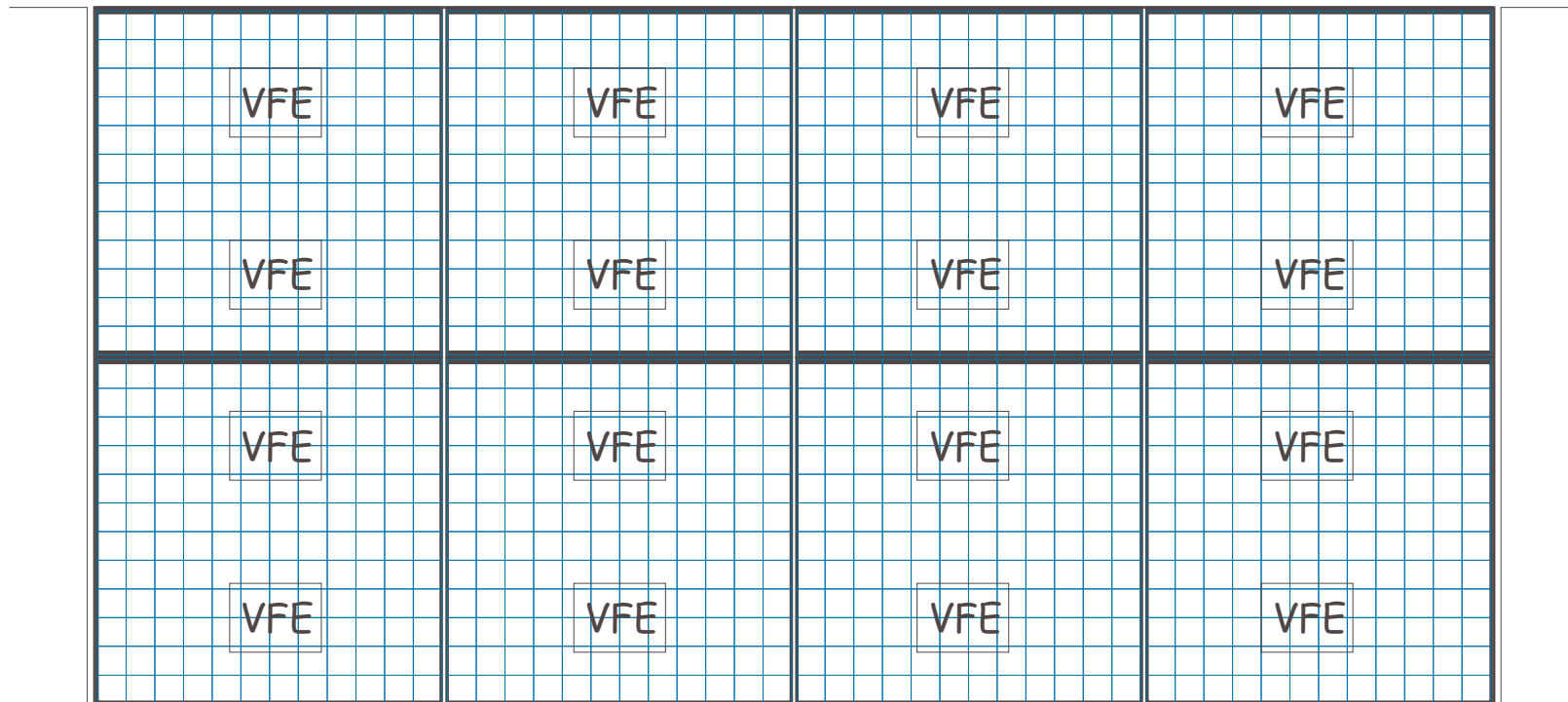
Conclusions :

- . Re-think ?
- . Arrive at viable design - both workable and affordable ?

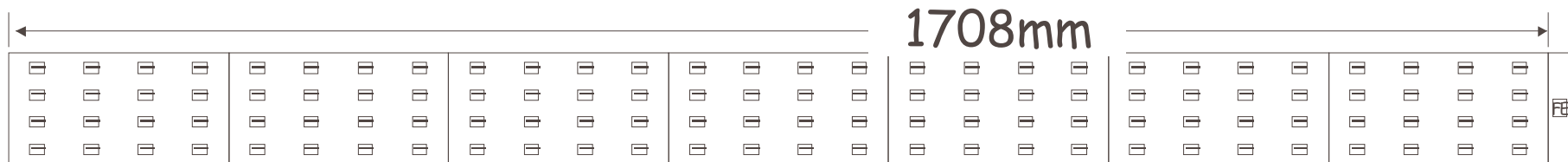
WP2.2 : Overview

There are lots of VFE ASICs on a slab:

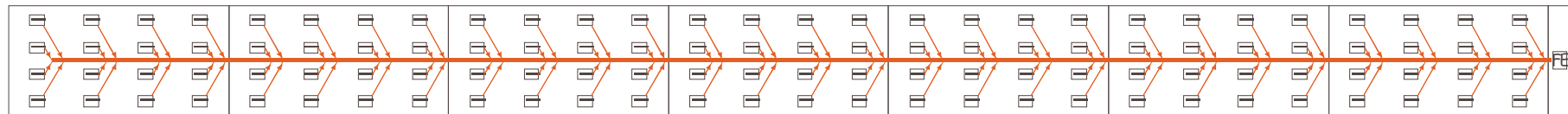
- A 240 x 120 mm panel has 16 on each side



Distributing the Clock and gathering the Data is non-trivial:
• There will be up to 7 panels per slab

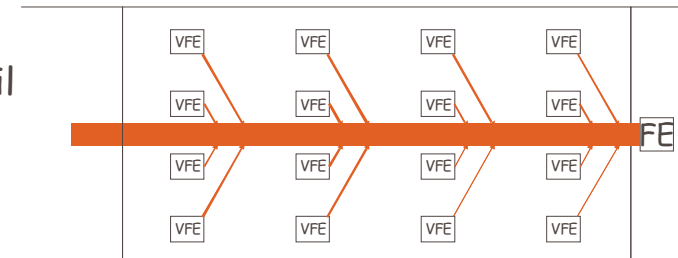


Just One Side of the SLAB!!

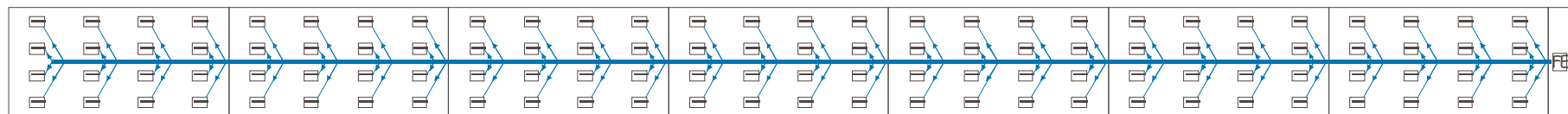


Read Out

Detail



Clock & Control

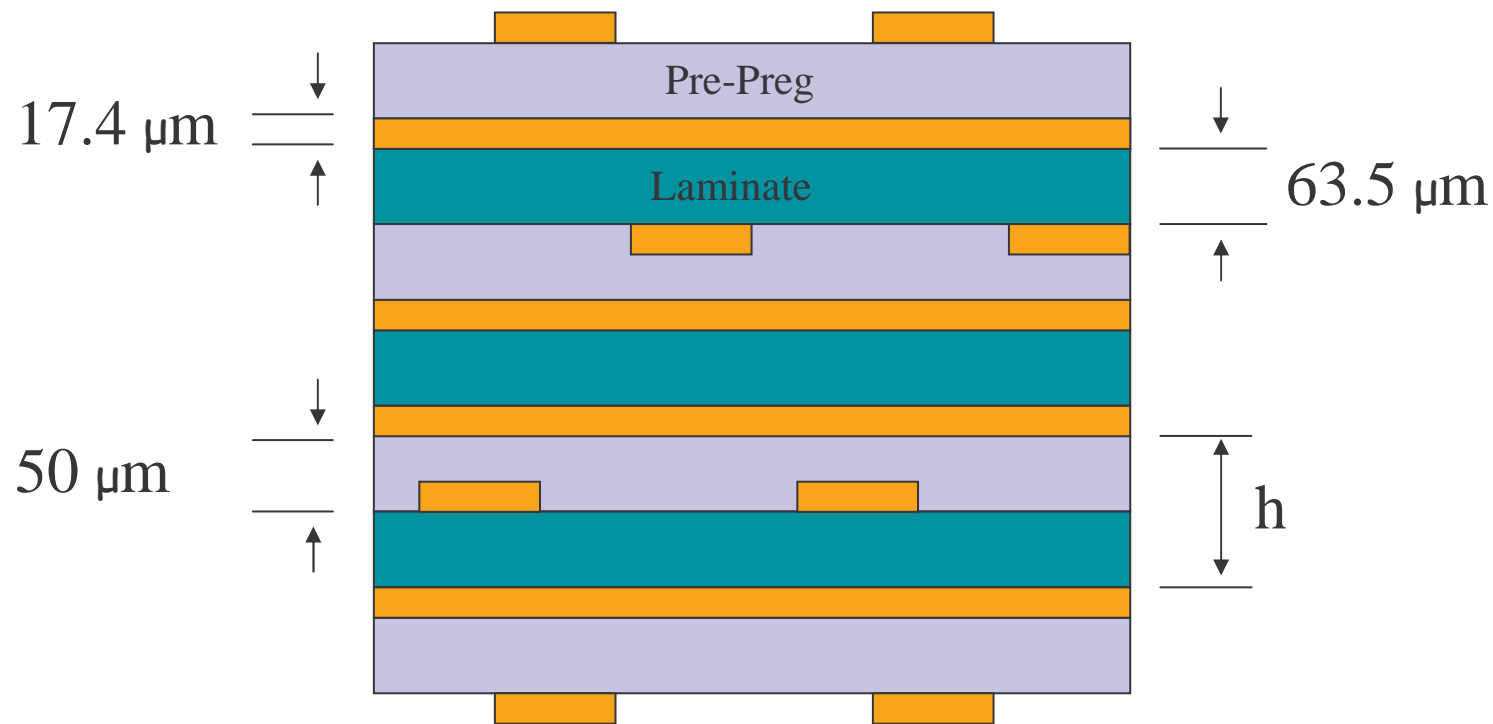


Rates:

- .Very difficult to pin down what the rates will be - depends on assumptions about occupancy and, particularly about zero suppression
- . The current design of ECAL VFE may only deliver a few Mbits/s per slab
- . Other scenarios deliver 120 Mbits/s even with zero-suppression

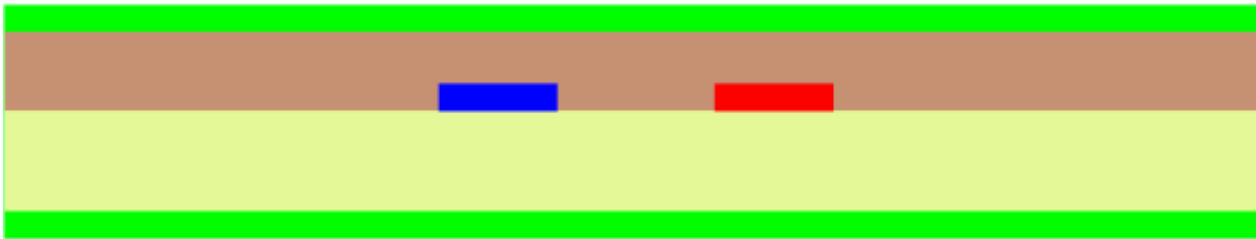
		Scenarios			
		ReadOut:	R1	R2	R3
Parameter		Beam:	B1	B1	B1
		CALICE:	C61	C62	C63
# BX per Bunch			4886	4886	4886
# BX per Sec			19544	19544	19544
# Pads per Average Slab			4000	3840	15360
# Bytes per BX	Per Slab non-Z Suppressed		8000	7680	30720
# MBytes per Bunch Train			39.1	37.5	150.1
# MBytes per sec			156.4	150.1	600.4
# Mbits per sec			1564	1501	6004
# Bytes per BX	Per Slab Zero Suppressed		160.0	153.6	614.4
# MBytes per Bunch Train			0.78	0.75	3.00
# MBytes per sec			3.13	3.00	12.01
# Mbits per sec			31.3	30.02	120.08

- The contemplated board build makes things difficult:
 - 8 layers in total thickness 600 μm !
 - means high capacitance tracks: ~ 300 pF/m for 150 μm track width
 - makes CMOS driving of long tracks noisy and power hungry
 - and means low Z_0 : $\sim 60 \Omega$
 - gives low voltage swings for LVDS (or similar) drivers



PCB Transmission Lines

- 64 μ m (2.5 thou) PCB thickness
- 50 μ m (2 thou) pre-preg thickness
- 17.4 μ m (0.7 thou) = 0.5 oz Cu layer

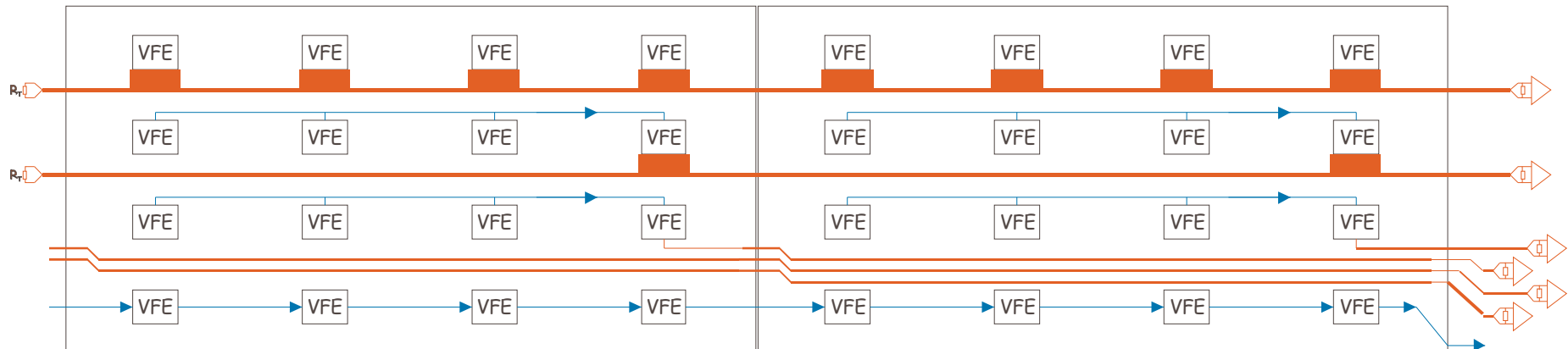


Trace width (μ m)	C0 (pF/m)	Z0 (Ohm)
200	373	16.5
150	305	20.3
100	229	27.1
75	± 160	32.8



Here are some schemes:

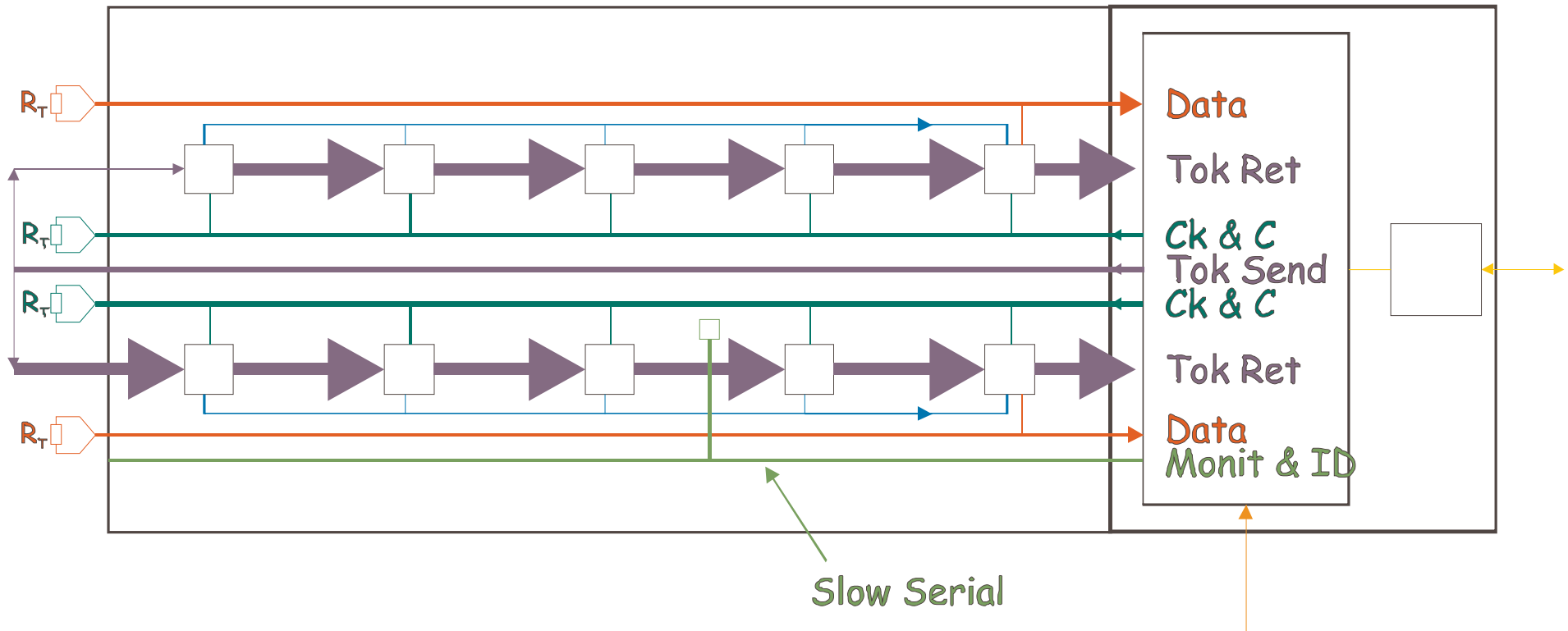
- Common differential readout line
- Collection among group of VFEs with transfer to common diff. line
- Collection among group of VFEs with transfer to private diff. line
- Daisy chained path: for lower rates this may work well with CMOS lines



WP2.2 - Other On-Slab Signals

There will be other signals to pass round the slabs:

- Token to initiate Readout
- Having a readable panel ID would be very useful
- Temperature and other monitoring



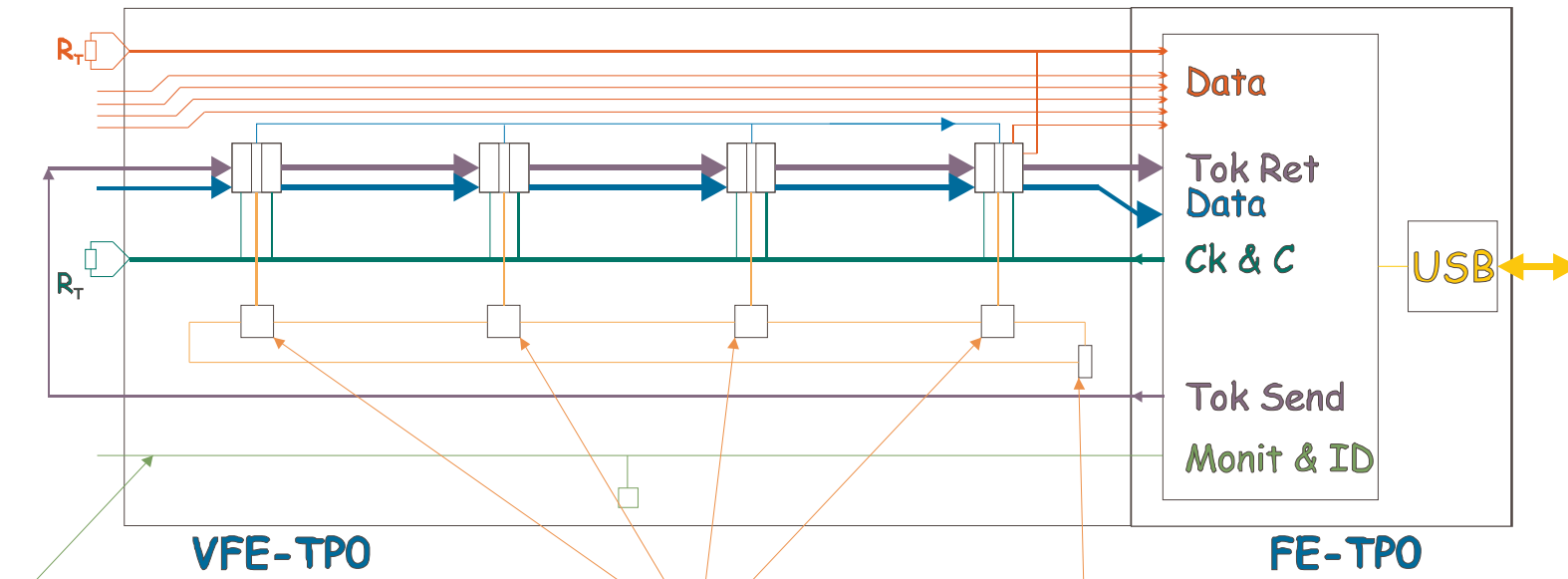
Signal Redundancy is also an important feature:
- it would be good to test ideas

WP2.2 - Test Panels

To test out these approaches and features, VFE and FE Test Panels are being built

Test Panels Version 0

Only need one row of Pseudo VFEs (PVFEs)
Each PVFE emulates 2 VFEs



Redundant paths have been included to try out redundancy schemes

FPGA Config PROMs

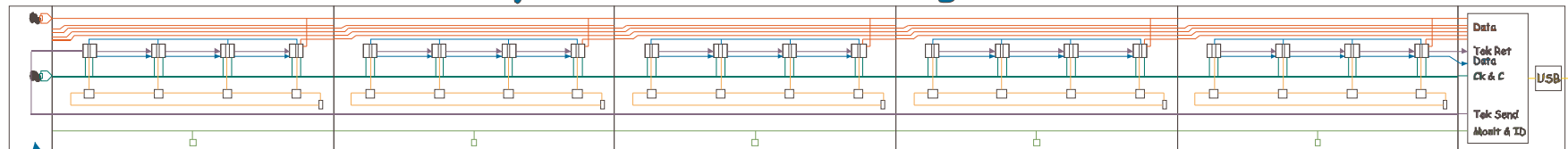
JTAG connector for FPGA Config

WP2.2 - Test Slab

A number of these test panels will be strung together to form a Test Slab

- not all need be populated to reduce the cost
- many options may be tried by changing the pVFE firmware
- many more testable by moving "zero-ohm links" on the PCB
- downloadable data
- data generation using PRN on the pVFE chips
- Bit Error Rate Testing (BERT) in FE FPGA
- USB to host PC for control and access to performance parameters

Multiple Test Panels forming a Test Slab



Terminator
Panel

Summary and Objectives

Plan:

- emulate multiple VFE chips on long, thin PCBs
- study the transmission behaviour
- optimise VFE PCB wrt the data-rate requirements

Needs:

- Segmented Test Slab PCBs
- FPGAs emulating VFE chips: pVFEs
- FE boards for distribution and reception of clock, controls, data etc.

Objectives:

- to contribute to the *CALICE* slab design
- to make our components (such as the FE design and test tools) available to the *CALICE* programme

WP2.2 - Beyond Here

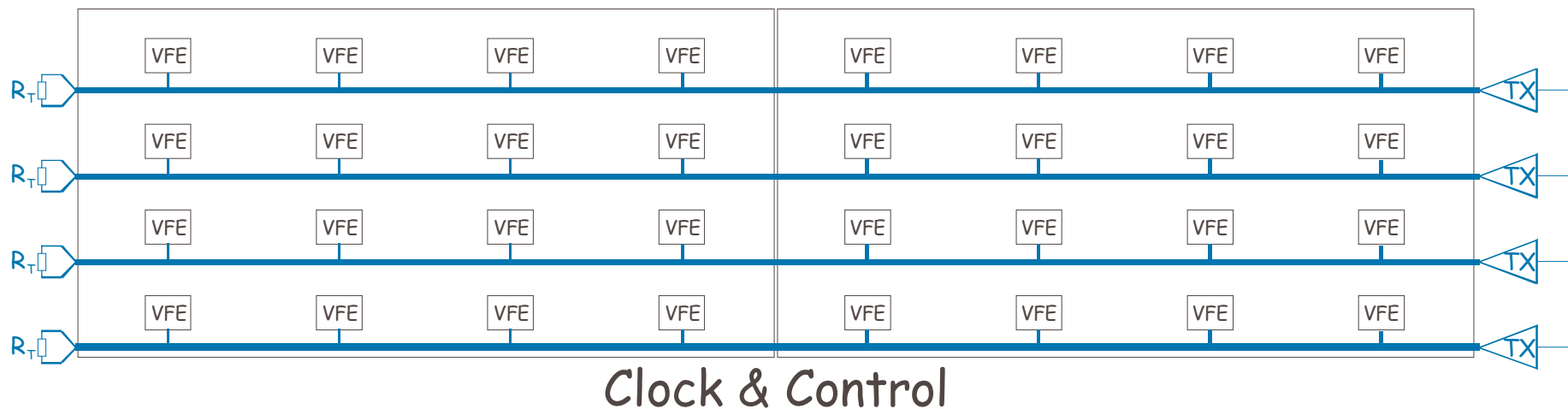


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Back-up Slides
From Munich Presentation

Distributing the Clock and Control Signals:

- . Separate or Encoded ?
 - . latter good for slew and reduces lines
 - . .. but needs CDR in ASIC, and may introduce jitter
- . Beam Clock is 5 MHz
- . Use 4 long lines (or pairs of lines) ?
- . Each has 1 Source TX, multiple RXs, single termination
- . Most dissipation in TX at slab end



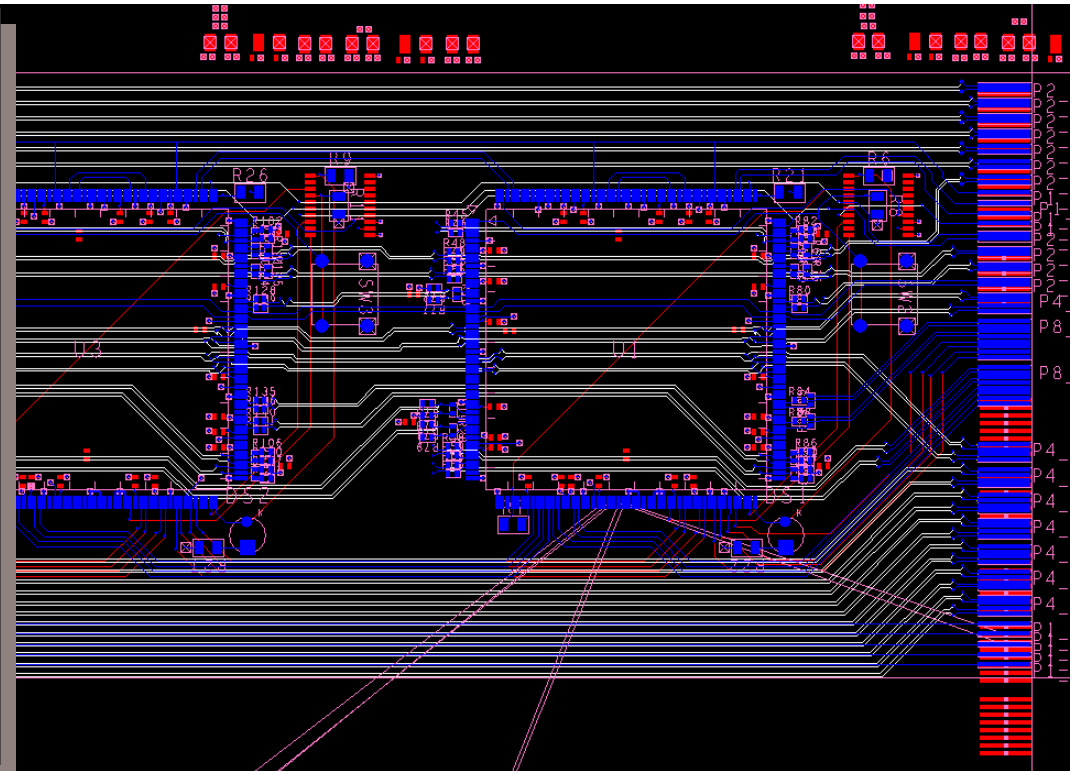
WP2.2 - PCB Status

Features thin (64µm) layers and narrow (75µm) traces

Traces for various clock distrib'n schemes and/or readout architectures incorporated in design

Rows of 4 FPGAs/board

Every FPGA mimics 2 VFE chips



- Ø Board schematics are 'finished'
- Ø PCB layout now completed

WP2.2 - pVFE FPGA progress:



- Simulation of actual VFE VHDL code using VFE technology specific SRAM
- Modification of VFE code and simulation using FPGA SRAM
- VFE chips incorporated in VHDL testbench
- Suggestions incorporated in VFE VHDL code V.2
- Single VFE chip+testbench running on Xilinx Spartan3E FPGA
- Two chips+testbenches fitted into single FPGA (X3S500E testboard)
- Design fits into envisaged pVFE FPGA and yet leaves room for extras:
 - 25% of logic used
 - 83% of block RAM used.
- Preliminary code available for alternative pVFE implementation