

# MAPS-based ECAL Option for ILC

*ECFA 2006, Valencia, Spain*

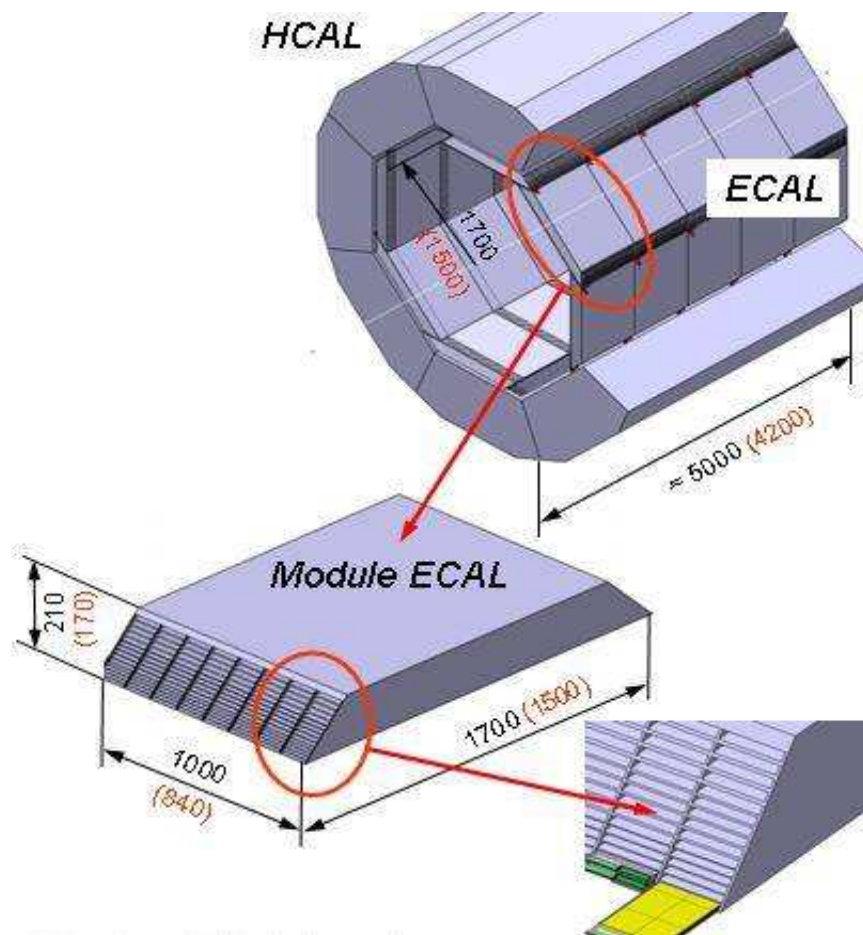
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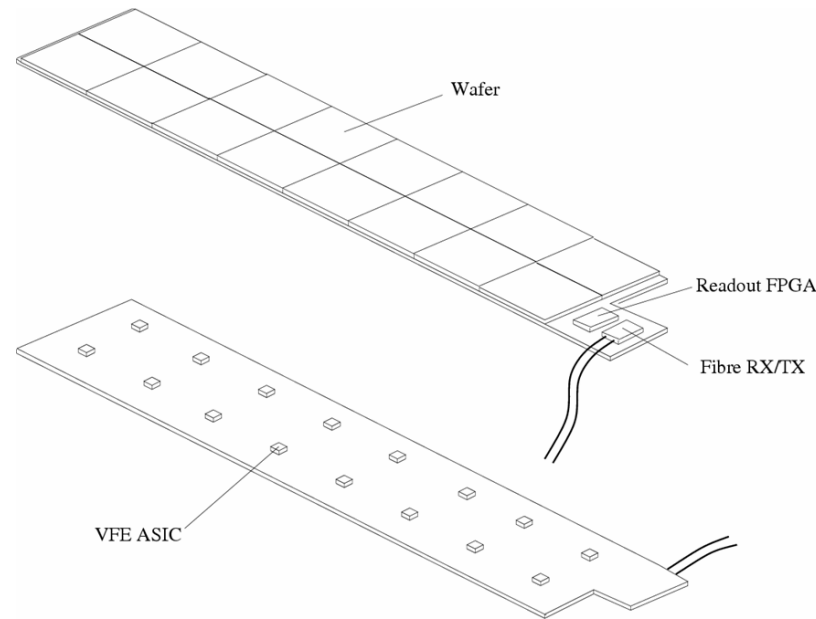
- ∇ **Introduction**
- ∇ **ECAL with Monolithic Active Pixel Sensors (MAPS)**
  - ⌊ **Requirements**
  - ⌊ **Simulations and design**
- ∇ **Conclusions**

# Introduction



- Work done within the CALICE collaboration
- Baseline ECAL design:
  - ∇ Sampling calorimeter, alternating thick conversion layers (tungsten) and thin detector layers (silicon)
  - ∇ Around 2 m radius, 4 m long, 30 layers, total Si area including endcaps  $\approx 2000 \text{ m}^2$  (for comparison CMS has  $205 \text{ m}^2 \text{ Si}$ )
- Mechanical structure
  - ∇ Half of tungsten sheets embedded in carbon fiber structure
  - ∇ Other half of tungsten sandwiched between two PCBs each holding one layer of silicon detector wafers
  - ∇ Whole sandwich inserted into slots in carbon fiber structure
  - ∇ Sensitive silicon layers are on PCBs  $\sim 1.5 \text{ m}$  long  $\times$  30cm wide

## Baseline ECAL with Silicon Diodes



- **Sensor is silicon diode pads with size between 1.0 cm×1.0 cm and 0.5 cm×0.5 cm**
- **Sensor wafers attached by conductive glue to a large PCB**
- **Pad readout is digitized to ~16 bits by the Very Front End (VFE) ASIC, mounted by on the other side of the PCB**
- **Total number of channels up to  $80 \times 10^6$**
- **Average dissipated power 1-4  $\mu\text{W}/\text{mm}^2$**

## Requirements for the ECAL



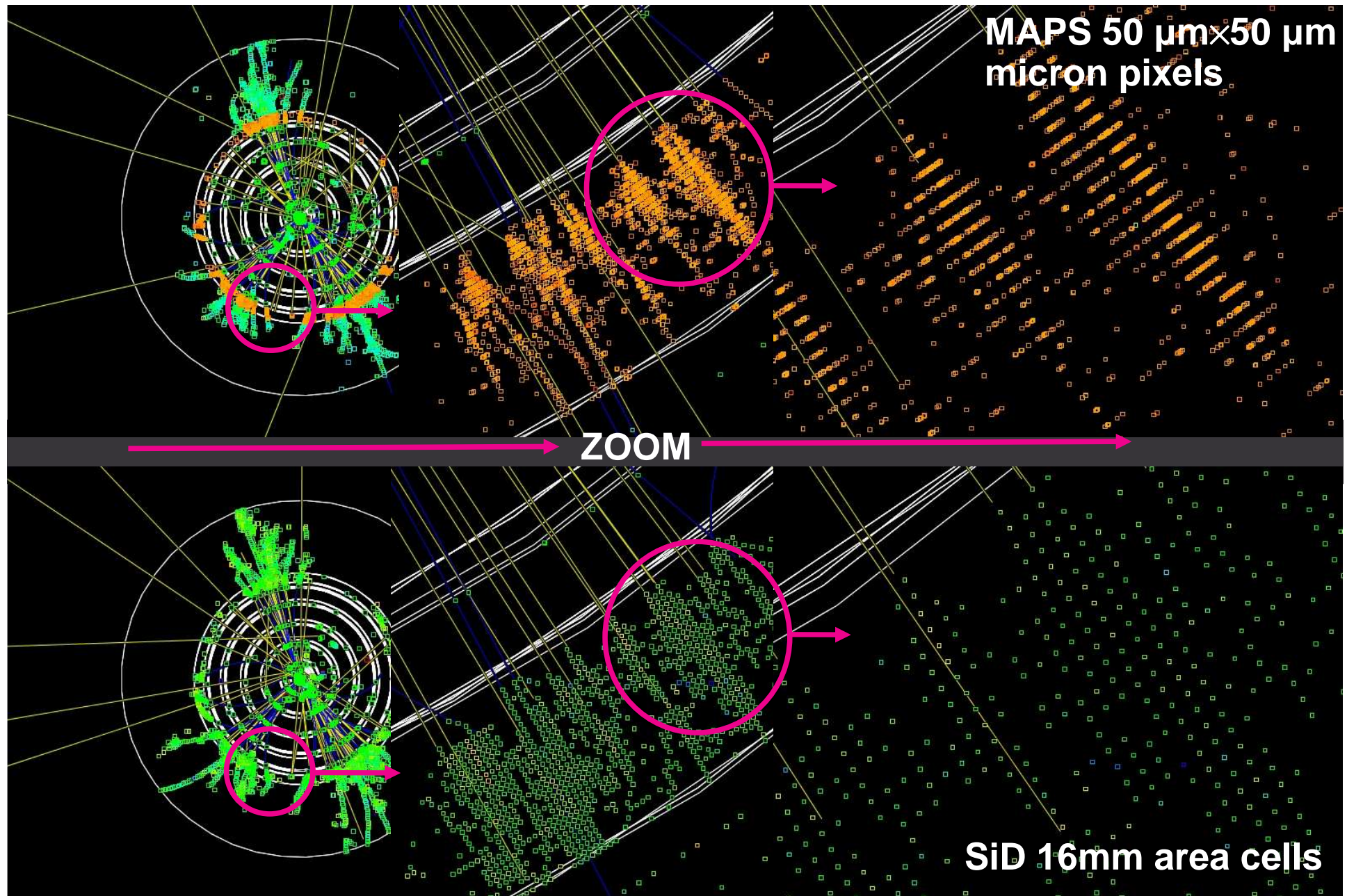
- Excellent energy and spatial resolution needed for Particle Flow – “tracking calorimeter”
- Nominal ILC beam timing parameters:
  - ∇ Beams collide during 1 ms-long bunch train, 337 ns inter-bunch spacing
  - ∇ Long “quiet” time (199 ms) between trains
- Physics event rate is small, pileup is low
- MAPS-based ECAL prototype being designed to cope with double the event rate and half the bunch spacing

## MAPS-based ECAL Design

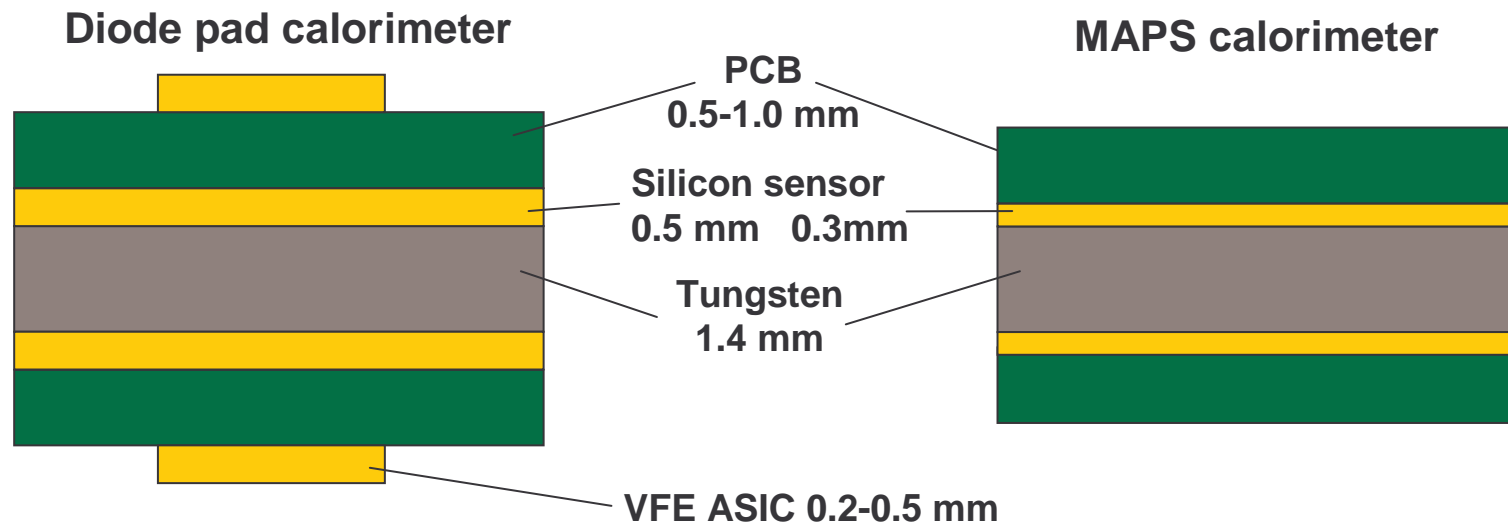
Features of the Monolithic Active Pixel Sensor (MAPS) -based calorimeter:

- **Binary readout:** hit or no hit per pixel (1-bit ADC)
- Pixels are small enough to ensure low probability of more than one particle passing through a pixel
- With  $\sim 100$  particles/mm<sup>2</sup> in the shower core and 1% probability of double hit the pixel size should be  $\sim 40 \mu\text{m} \times 40 \mu\text{m}$ 
  - **Current design with  $50 \mu\text{m} \times 50 \mu\text{m}$  pixels** – see Yoshi Mikami's talk
- Timestamps and hit pixel numbers stored in memory on sensor
- Information read out in between trains
- Total number of ECAL pixels around  $8 \times 10^{11}$ : Terapixel system
- Only monolithic designs can cope with that number of pixels – hence MAPS

# Diode pads and MAPS in ECAL (I)



## Diode pads and MAPS in ECAL (II)



- Baseline design largely unaffected by use of MAPS instead of diode pads
- Advantages in the MAPS design:
  - ∇ High granularity could improve the position resolution and reduce the number of layers (thus cost) for the same resolution
  - ∇ More uniform thermal dissipation from larger area
  - ∇ Less sensitivity to SEU, but higher SEU event rate – digital logic is spread out
  - ∇ **Cost saving** (CMOS vs. high resistivity Si wafers and/or overall more compact detector system)
  - ∇ Simplified assembly (single sided PCB, no need for grounding substrate)

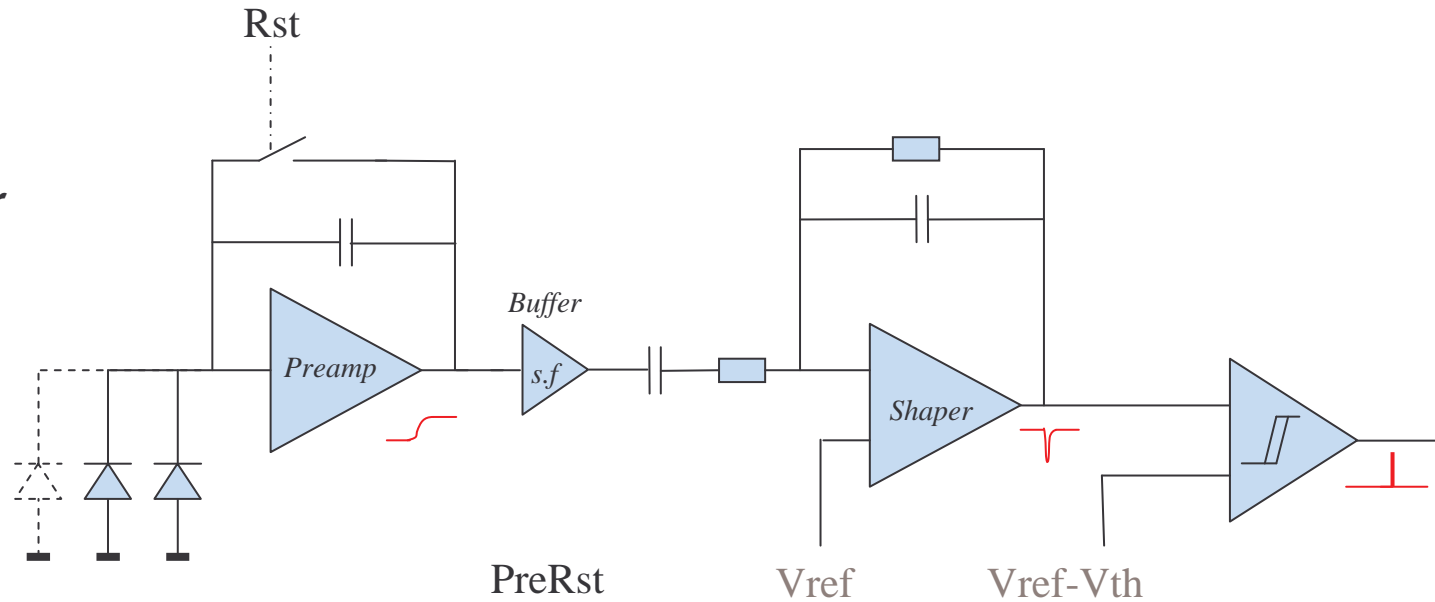
## MAPS-based Simulations and Design

- Design of the first prototype started at the CMOS Sensor Design Group at RAL
- Four different pixel architectures included in the first prototype
- Targeting 0.18  $\mu\text{m}$  CMOS imager process
- Goal of  $S/N > 15$  to achieve noise pixel rate below  $10^{-6}$ 
  - ∇ Data rate dominated by noise
  - ∇ Aim to reduce the electronics noise to the level of physics background (mini-jets and Bhabhas)
  - ∇ Faulty pixels masking and variable global threshold per chip included
  - ∇ Process non-uniformities contribute to threshold spread and are being studied
- Optimal pixel layout and topology essential to guarantee good S/N
- Power dissipation is a major issue

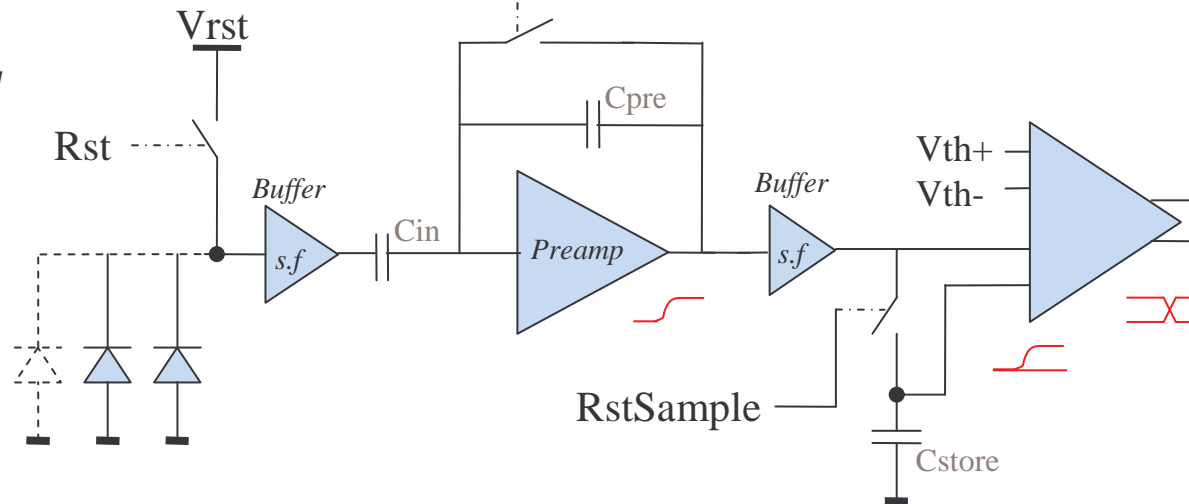


# Pixel Design : Overview

**Design A:**  
Charge amplifier  
with shaper

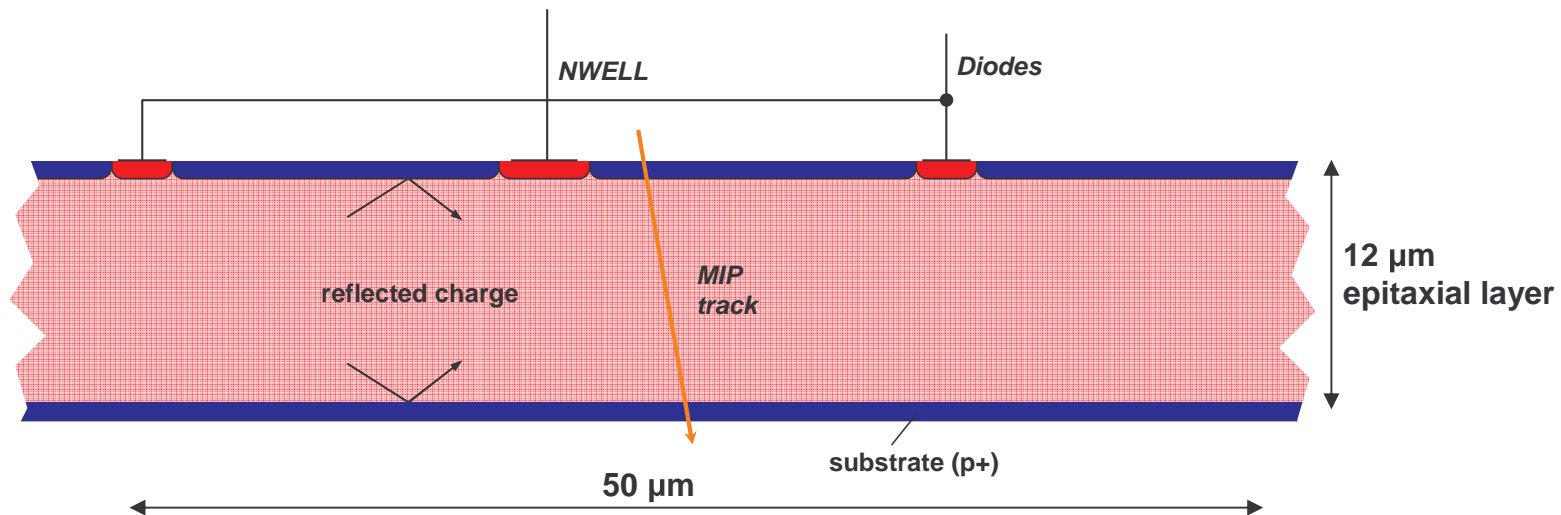
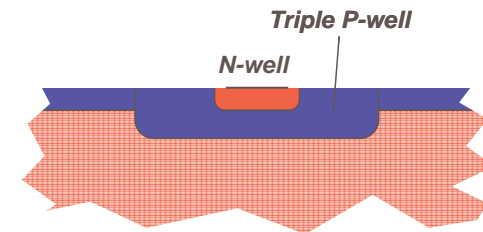


**Design B:**  
Voltage sensing  
with CDS

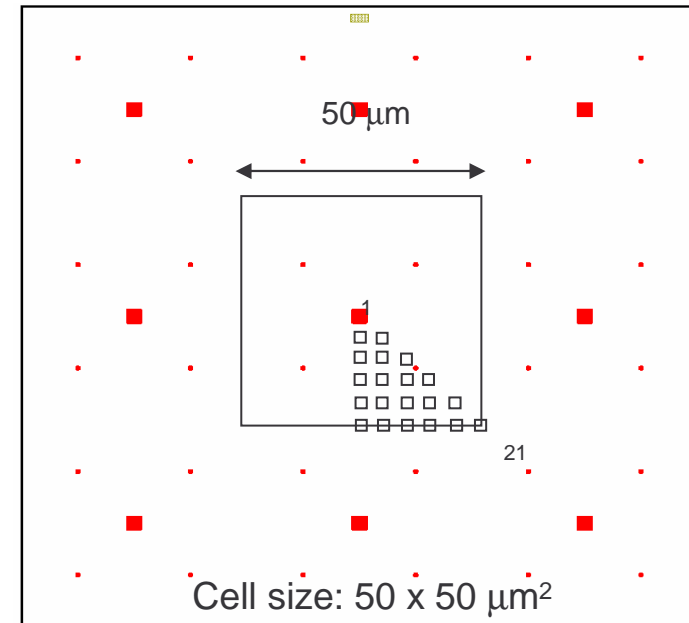
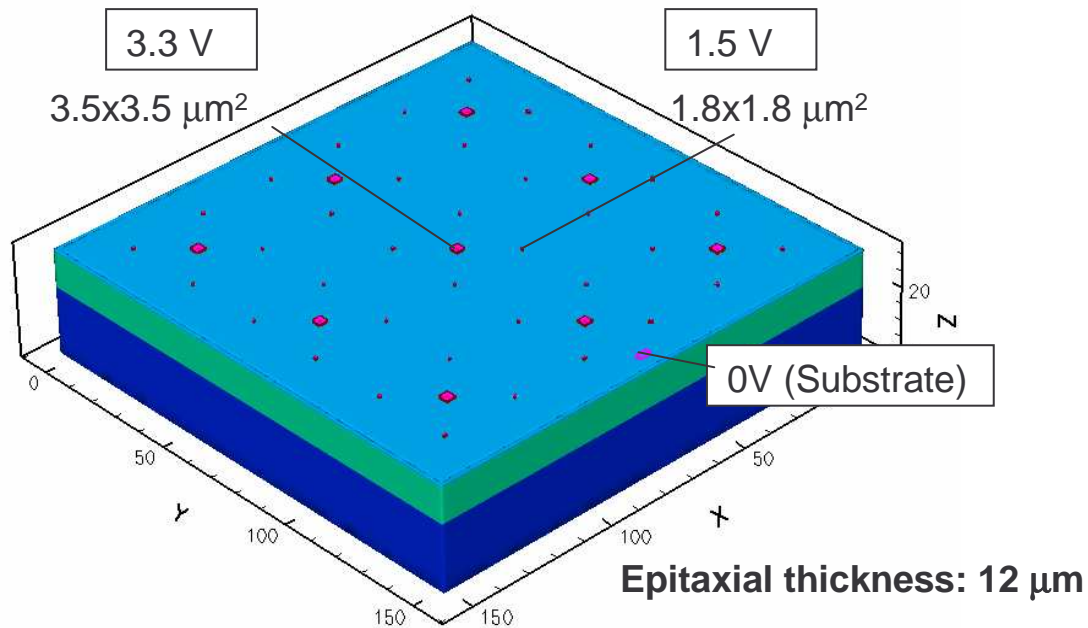


## Pixel Design : Charge Collection

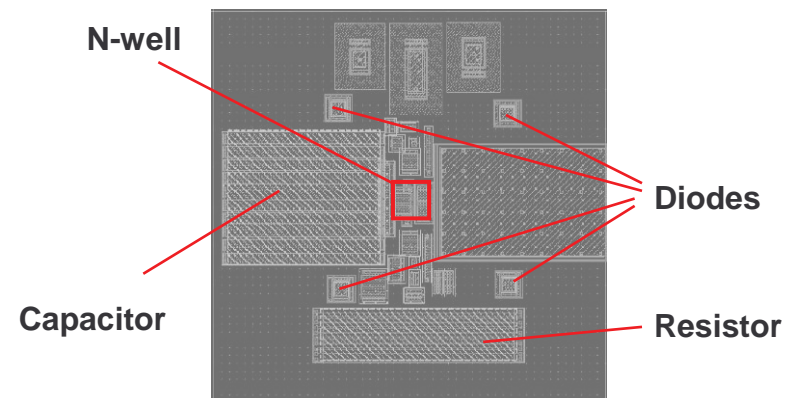
- Charge collected mainly by diffusion: ineffective process,  $\approx 250$  ns collection time
  - Depletion under the diodes is only  $2\ \mu\text{m}$
- Pixel is large and requires large collecting diodes
  - ∇ Large diodes add capacitance and noise
- N-well for PMOS transistors competes with the diodes and reduces the collected charge
  - Investigating triple P-well – **no charge loss**
- Charge sharing between pixels should be minimal
  - ∇ Optimization of the diode location and size is necessary



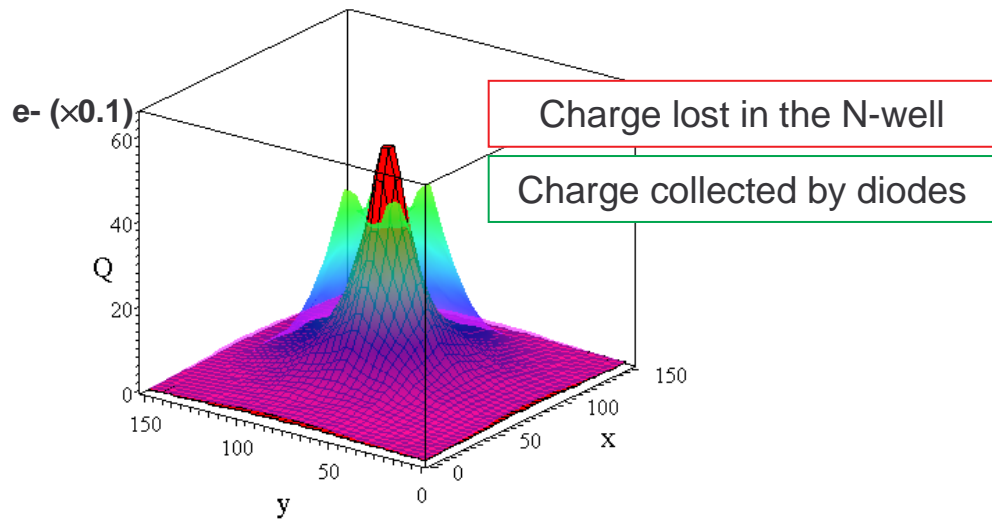
# Pixel Design: Simulations of Charge Collection (I)



- Full 3D device simulation using TCAD Sentaurus (Synopsys)
- 21 MIP hits/pixel simulated on  $5 \mu\text{m}$  pitch
- Using the symmetry the collected charge in the rest of the device is extrapolated

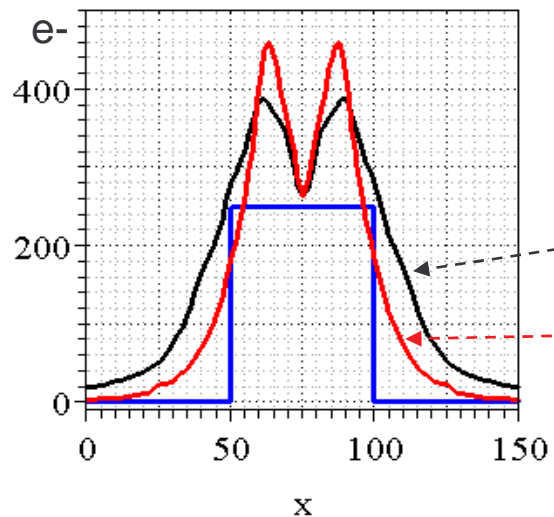


# Pixel Design: Simulations of Charge Collection (II)

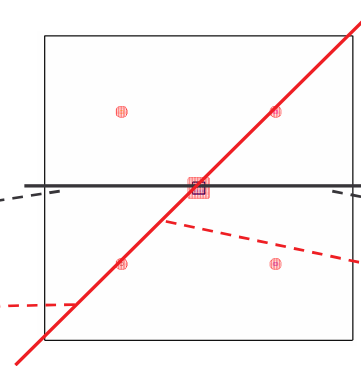
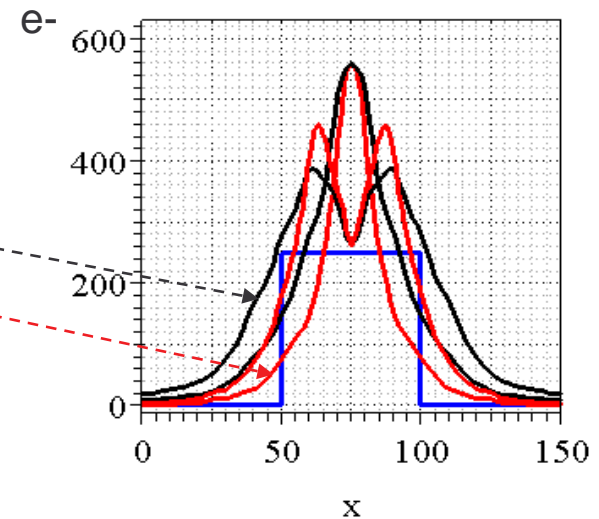


- 50% of the charge collected when a MIP hits the N-well
- Collected charge increases with the diode size

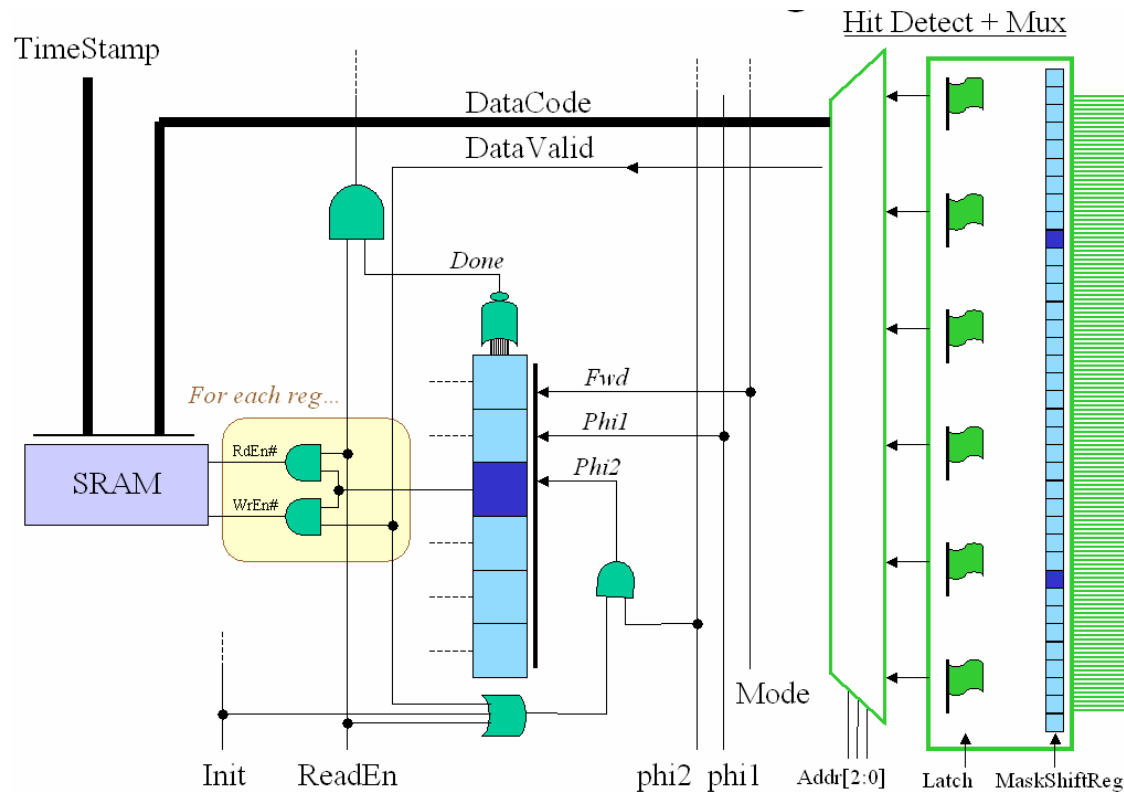
Collected charge on the diodes vs. MIP impact position



Collected charge on the diodes and on the N-well vs. MIP impact position

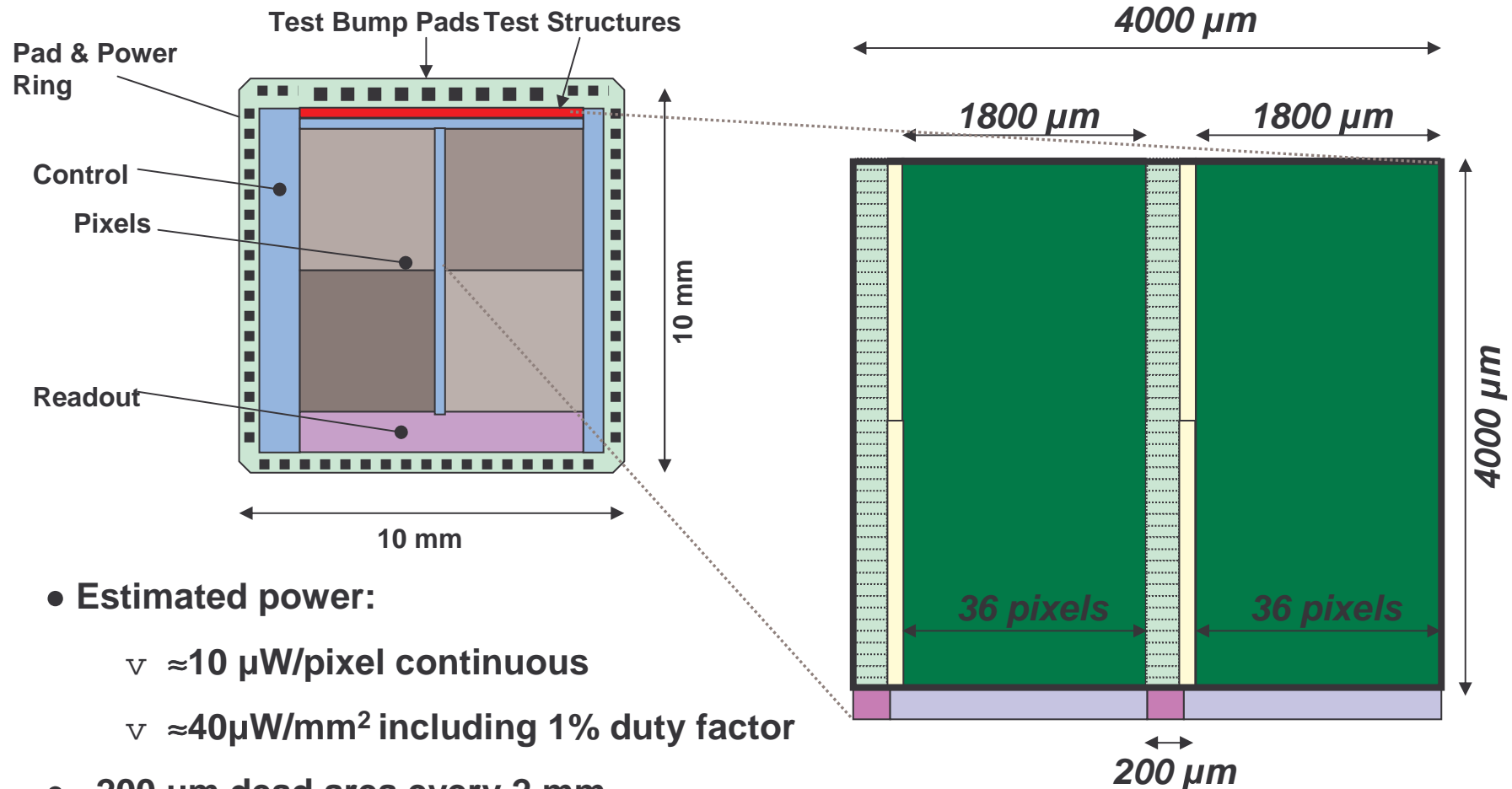


# Digital Design for the First Prototype



- In this design each digital block serves 36 pixels from one row
  - ▽ 48 or more pixels can be served, limited by the tracking
  - ▽ Adds about 10% dead area (less for more pixels served)
  - ▽ Narrow digital “strip” reduces power consumption
  - ▽ Register for masking out noisy pixels
- Address and timestamp written in SRAM

# Chip Layout



- Estimated power:
  - ∇  $\approx 10 \mu\text{W}/\text{pixel}$  continuous
  - ∇  $\approx 40 \mu\text{W}/\text{mm}^2$  including 1% duty factor
- $\approx 200 \mu\text{m}$  dead area every 2 mm
- MAPS chips could be  $\sim 2 \text{ cm} \times 2 \text{ cm}$ 
  - ∇ Stitching could be considered if larger devices are needed
- Each sensor could be flip-chip bonded to a PCB

## Conclusions

- **MAPS-based ECAL could offer numerous advantages**
- **Design of the first generation “proof of principle” MAPS for CALICE ECAL is advancing well**
- **Two types of analogue pixel circuits considered**
- **Charge collection studies are very important for good S/N**
  - ∅ **Optimization of diode position and size for maximum signal and minimum crosstalk**
  - ∅ **Goal is  $S/N > 15$  by design**
- **Power dissipation still high and needs to be addressed**
- **Chip submission most likely in April 2007**