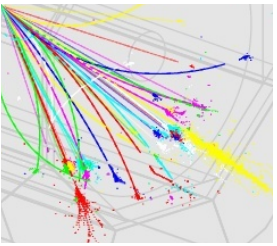

Status of the MAPS project

Imperial College 27.03.2007

Y. Mikami, O. Miller, V. Rajovic, N.K. Watson, J.A. Wilson
University of Birmingham
Mark Thomson
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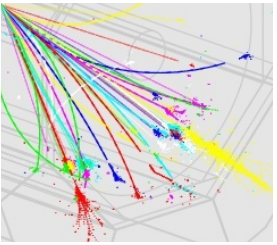
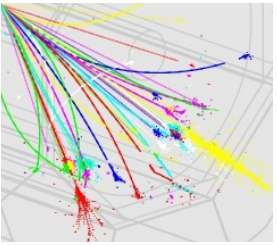
Imperial College London
J.P. Crooks, M. Stanitzki, K.D. Stefanov, R. Turchetta, M. Tyndel, E.G. Villani
Rutherford Appleton Laboratory



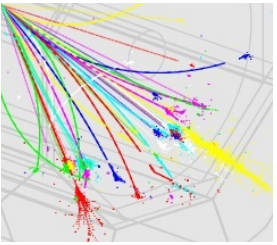
Overview

- Introduction
- Status
  - Sensor Design
  - Sensor Simulation
  - DAQ/Testing
  - Detector Simulations
- Next steps



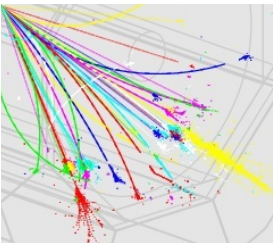
Introduction

- Development of an alternative readout sensor for the CALICE ECAL
- “Swap-In” Solution leaving mechanical structure untouched
- Use of MAPS with high granularity and digital readout

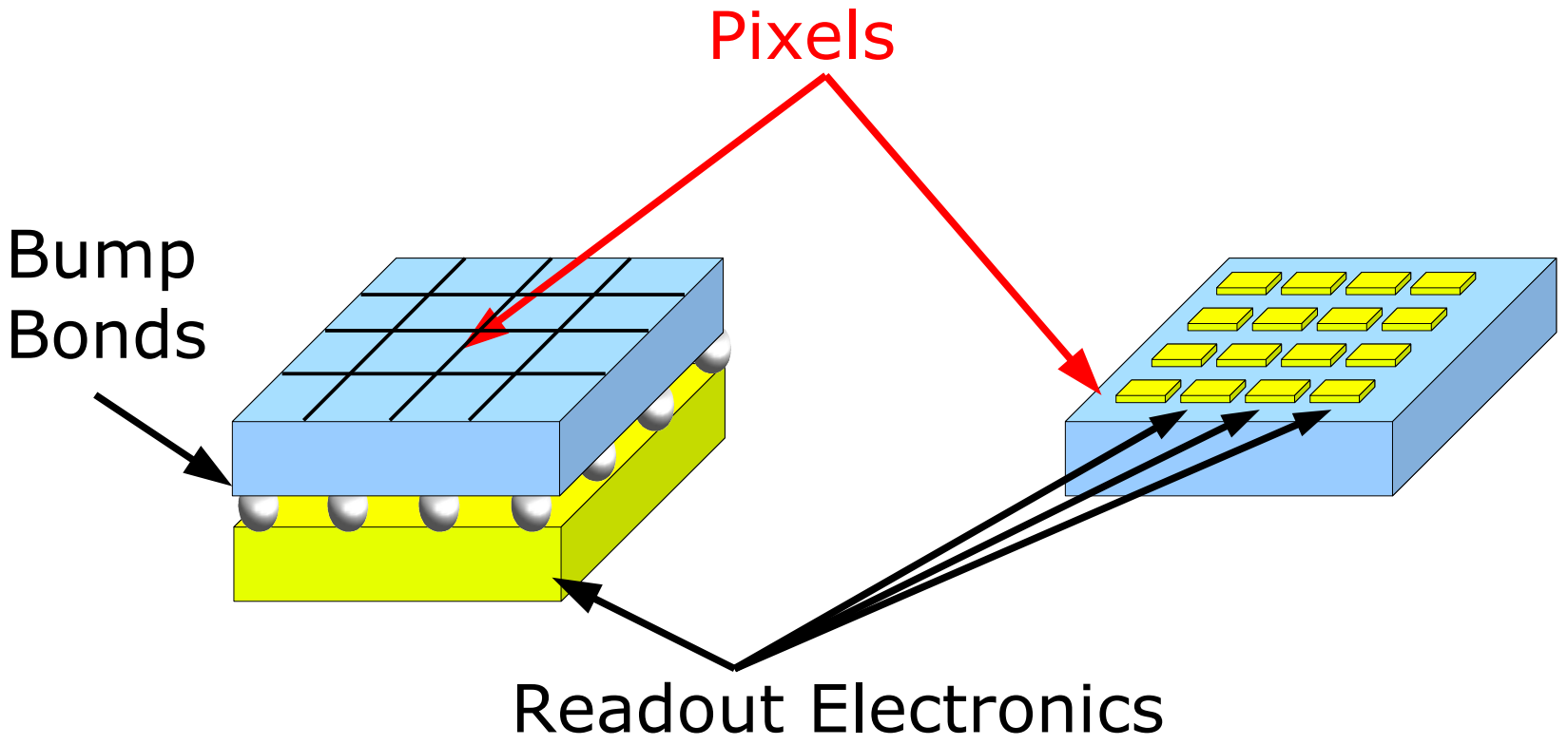


What are MAPS ?

- **M**onolithic **A**ctive **P**ixel **S**ensors
- Integration of Sensor and Readout Electronics
- Manufactured in Standard CMOS process
- Collects charge mainly by diffusion
- Development started in the mid-nineties, now a mature technology

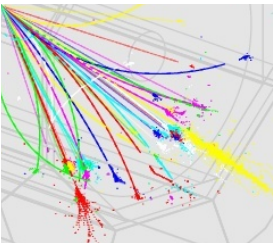


Hybrid Pixels and MAPS

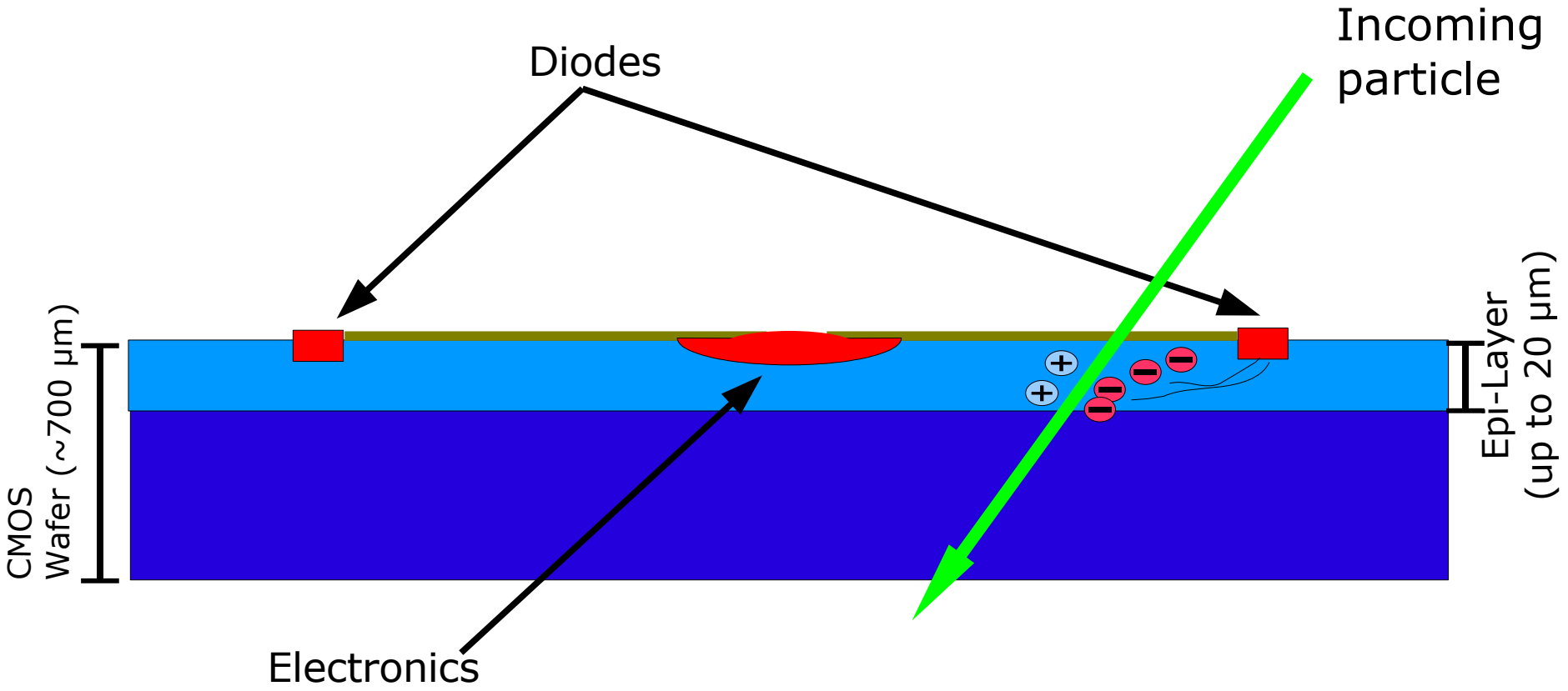


LHC-style Hybrid Pixel sensor

MAPS

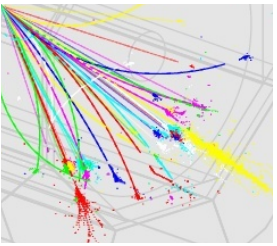


MAPS in Detail



MAPS architecture:

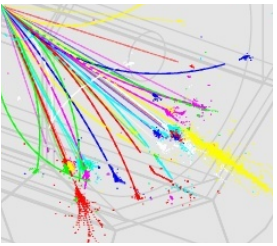
- Sensor and the electronics are integrated in one wafer
- Charge Collection mainly in epi-layer
- Charge collected mostly due to diffusion



The CALICE MAPS

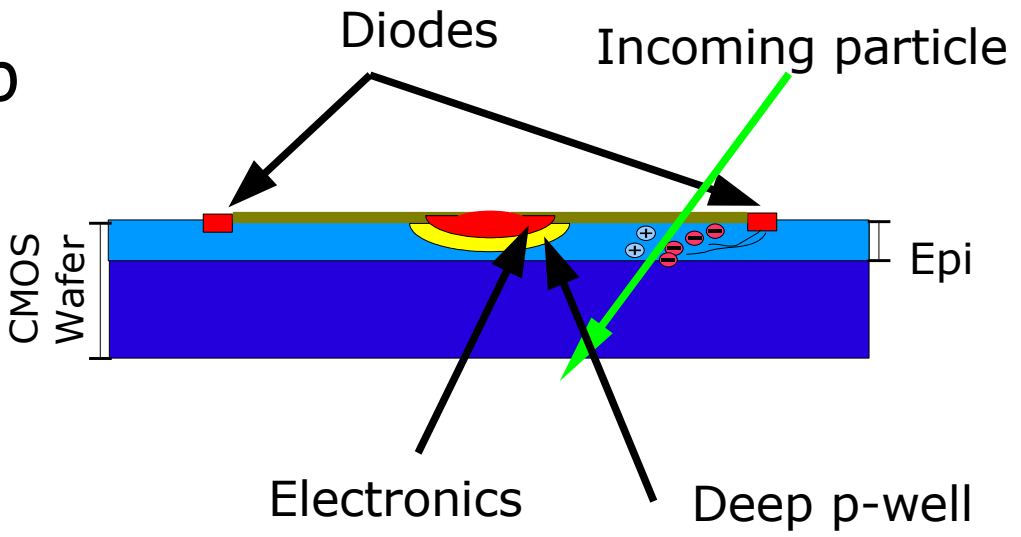
For the CALICE ECAL a specific MAPS was designed:

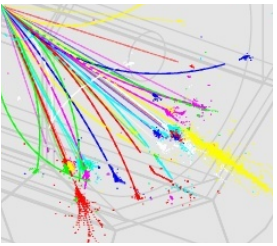
- Pixel Size (50 x 50 µ)
- Binary Readout (1 bit ADC realized as Comparator)
- 4 Diodes for Charge Collection
- 13 bit Time Stamping
- Hit buffering for entire bunch train
- Capability to mask individual pixels
- Threshold adjustment for each pixel



A new process technology

- Simulation showed, that the n-wells absorb a lot of charge (hence affecting the signal)
- We isolated the n-well with a "deep p-well" implant (3 µm thick)
- Novel *INMAPS* process used for the CALICE MAPS



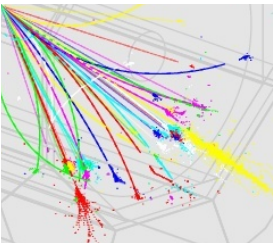


Sensor Electronics

- Two types of pixel readout
- Shaper & Sample

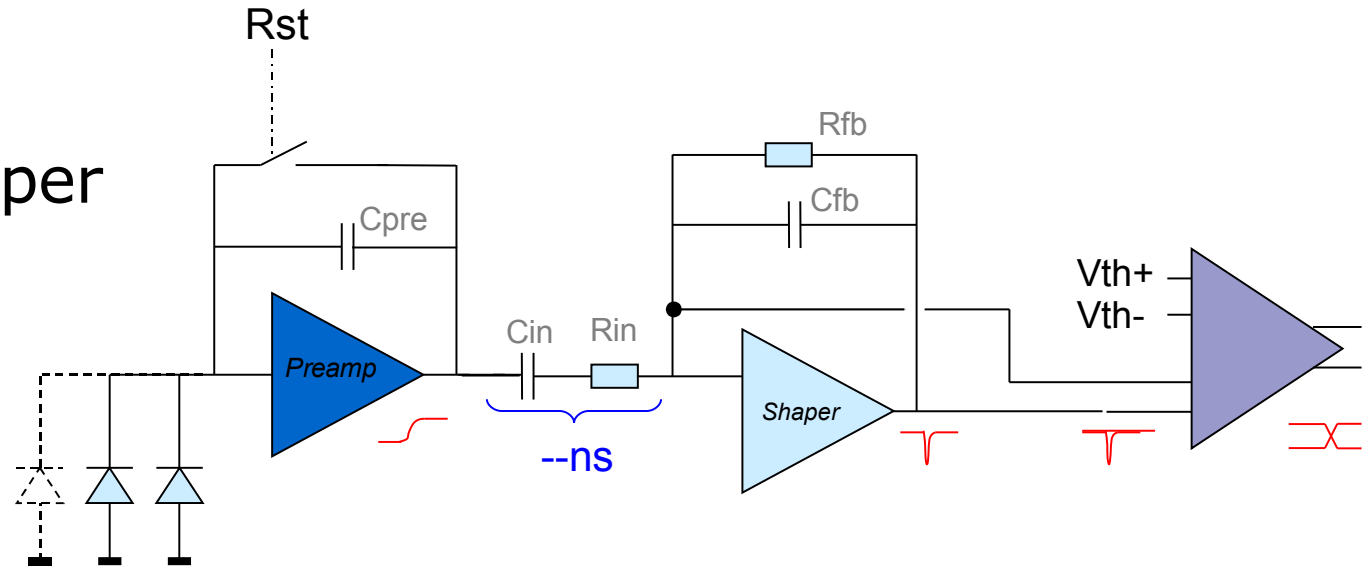
	Pre-Shaper	***Pre-Sampler***
Deadtime	Varies with Signal	Constant
Reset	Self-resetting	Active reset
Diode mode	Current	Voltage

- Average deadtime (~600 ns/ 450 ns)
- Simulation shows similar noise characteristics
- Both share the Comparator design
- Having two readout architectures allows us to explore several ideas at once

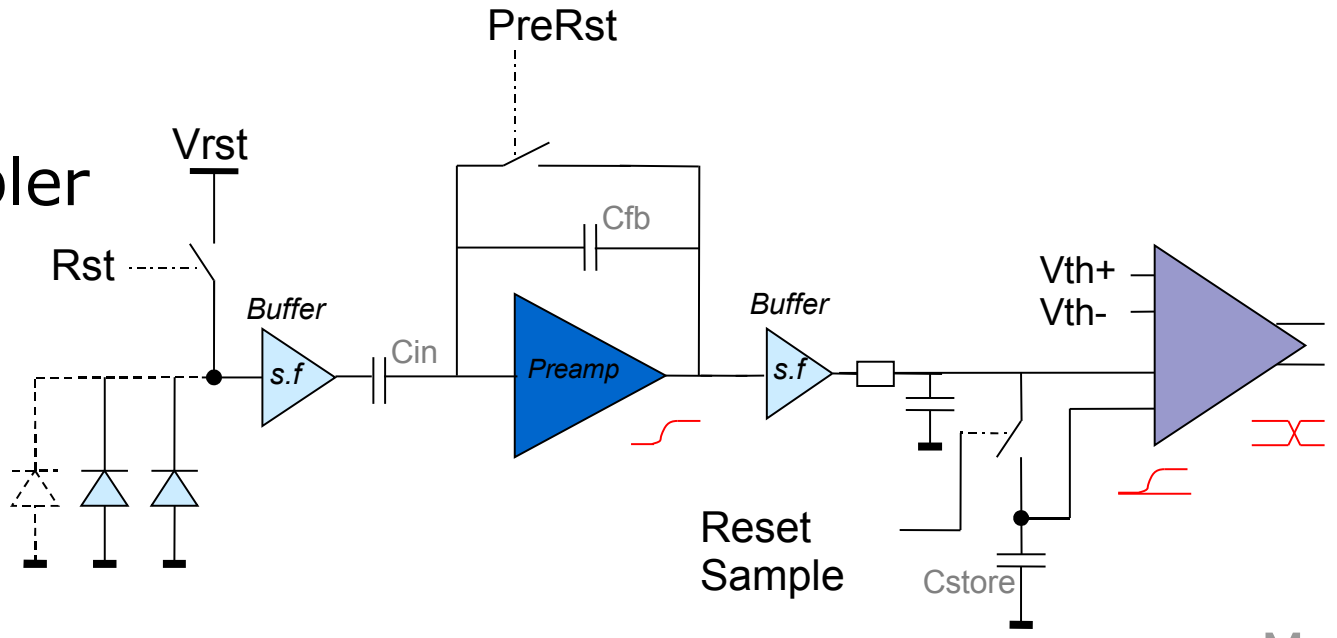


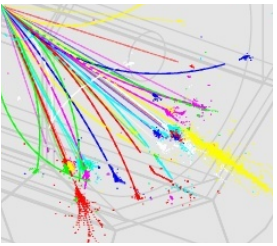
The two pixels

Pre-Shaper



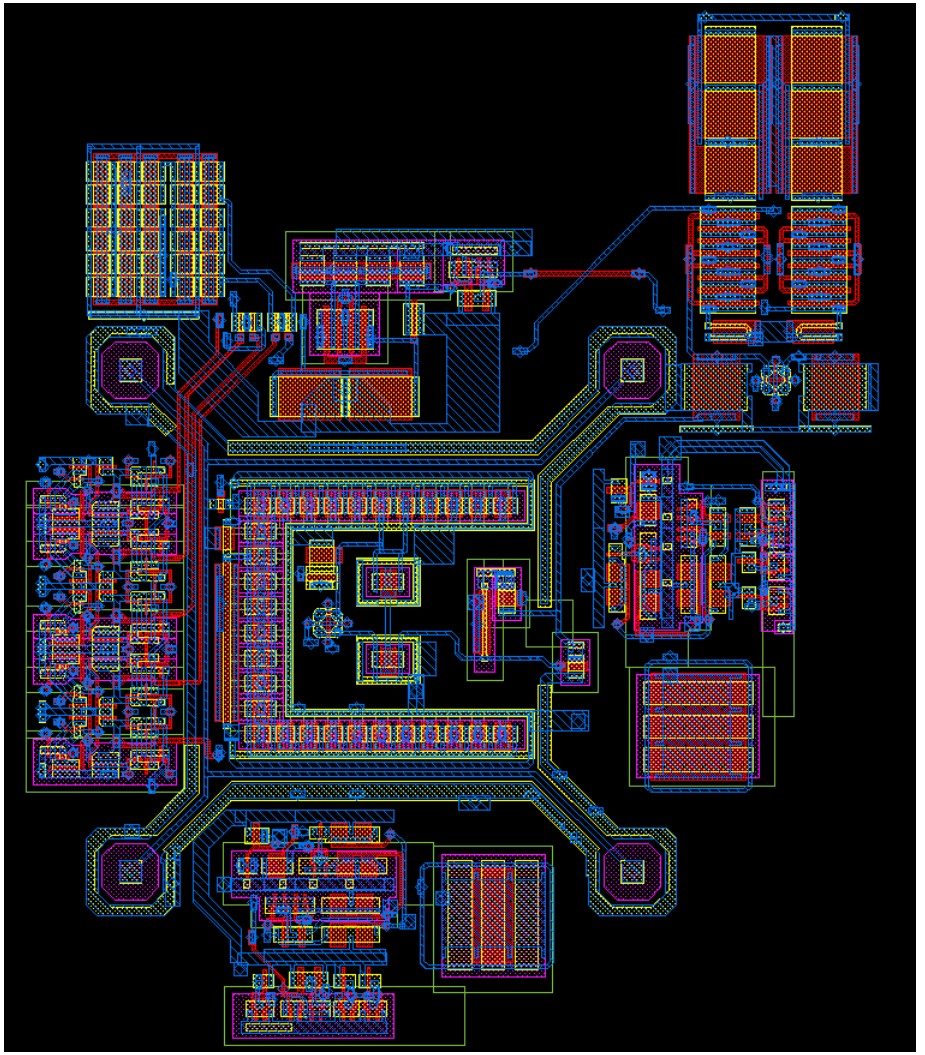
Pre-Sampler

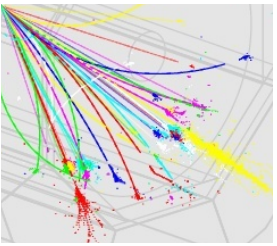




The Pixel

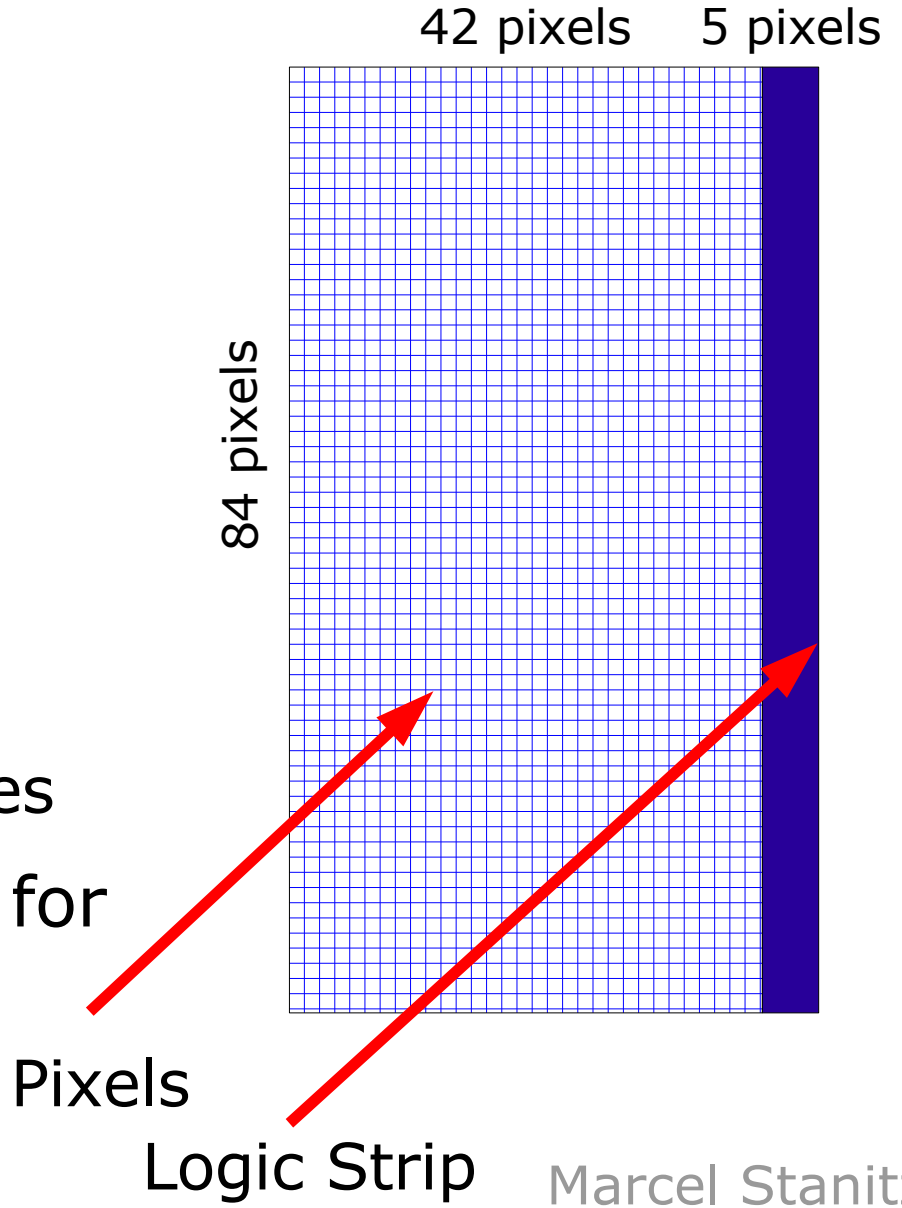
- 50x50 µm size
- 0.18 µm process
- 12 µm Epi-layer
- Deep p-wells
- 5 metal layers
- 224 1.8 V transistors
- 1 3.3 V transistor
- 36 capacitors

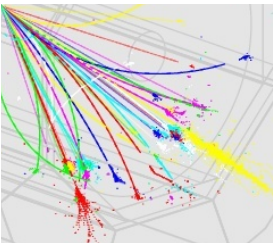




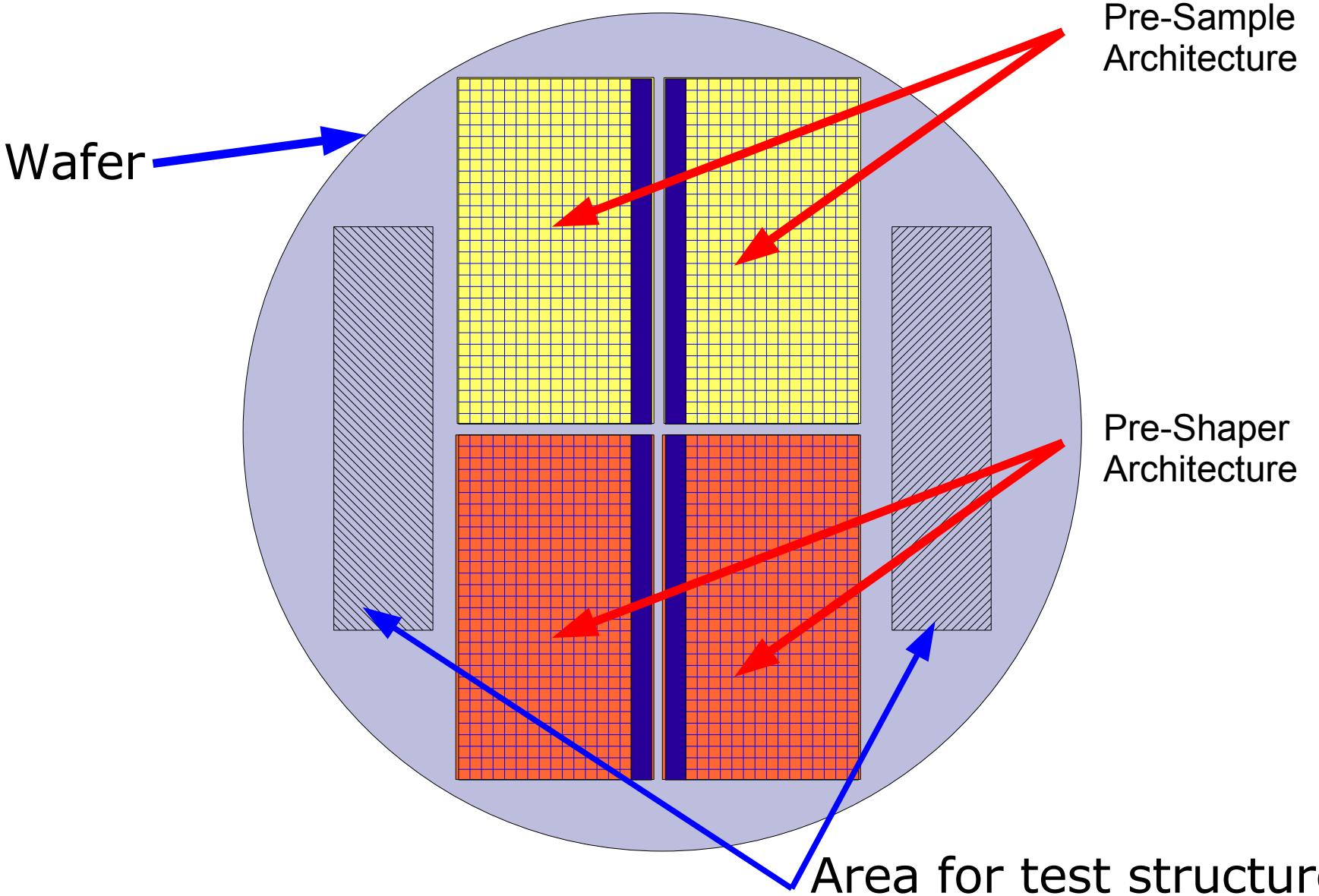
The test sensor (V1.0)

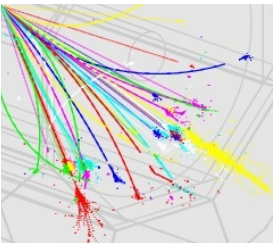
- Consists of 42x84 pixels
- Has a logic strip for
  - 5 pixels wide
  - Hit buffering using SRAM technology
  - Time stamping (13 bit)
  - Configuration registers
  - the only part with Clock lines
- Logic strip is a “dead area” for particle detection (~ 11 % inefficiency)





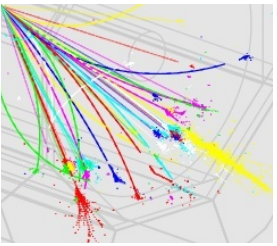
The test structure (V1.0)





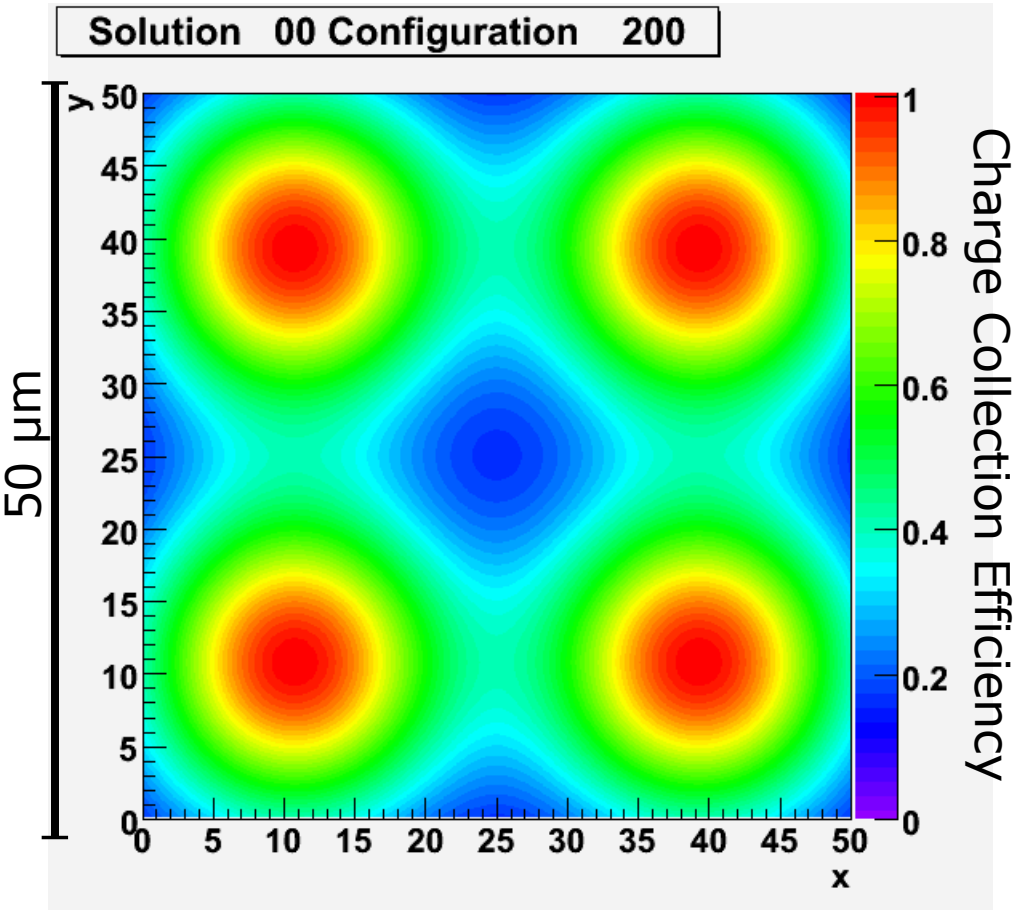
Sensor Simulation

- We are using Centaurus TCAD to simulate the sensor
- Using CADENCE GDS file for pixel description
- Simulate diodes from adjacent pixels for charge sharing effects
- Detailed Pixel performance studies
  - Collection Efficiency
  - Charge Collection Time
  - Signal/Noise

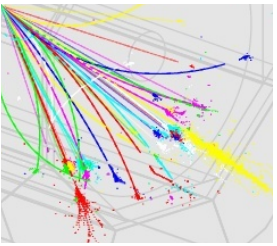


Diode placement

- Classical problem
  - Place n circles in a square
  - No analytical solution
- Only 4 Diodes as a starter
- Mathematics faces reality
  - Constraints due to Design Rules
  - Electronics
  - Space

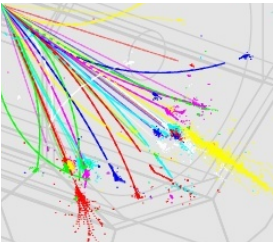


Numerical Solution

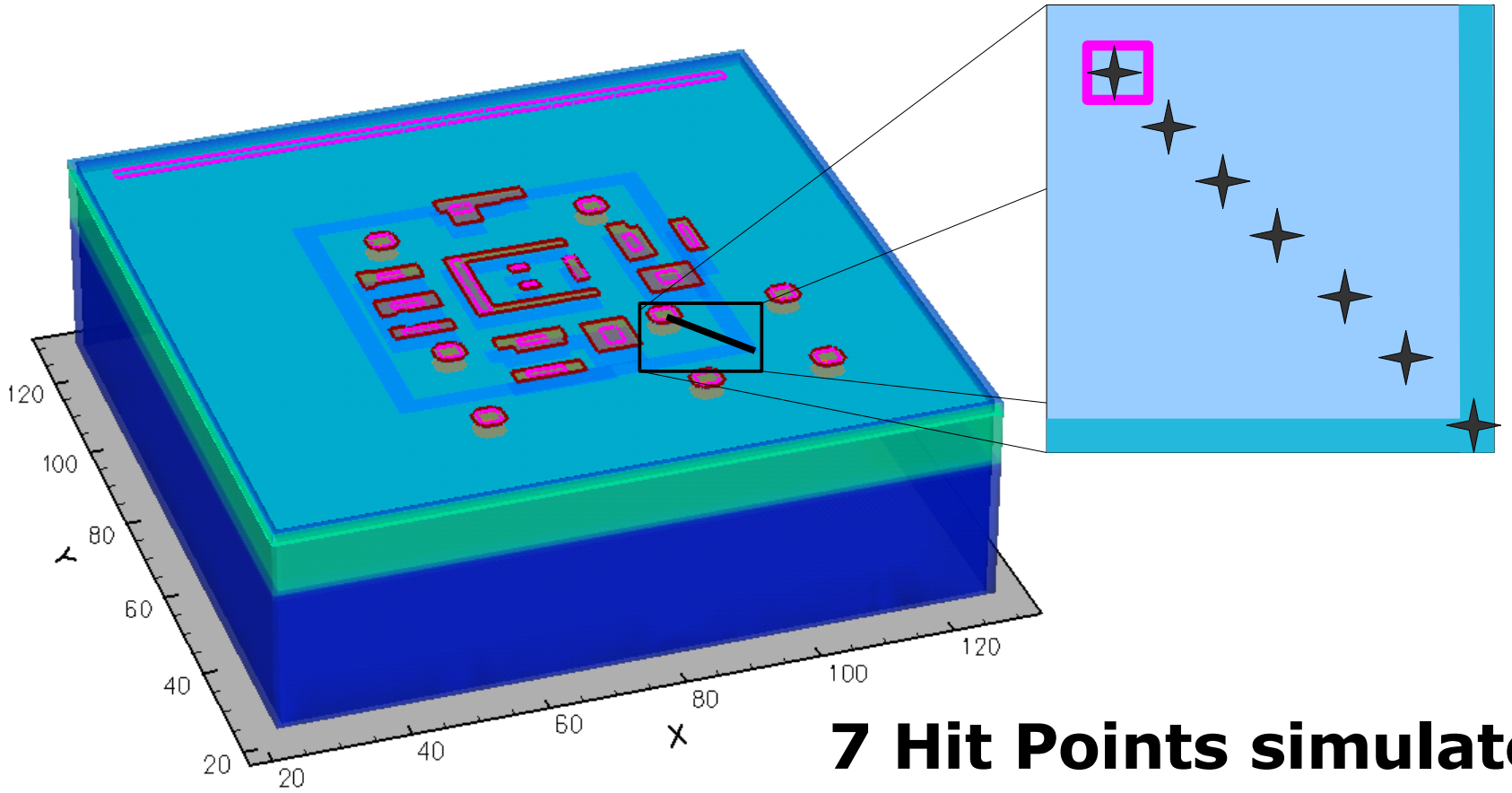


The setup

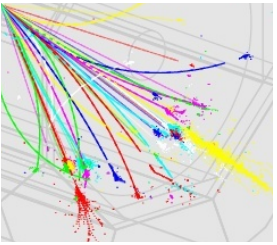
Electronics
Diodes
Adjacent Diodes
Bias:
•n-Well 1.8/1V
•Diodes: 1.5V
Substrate
Epi-Layer
120
100
80
60
40
20
Y
X



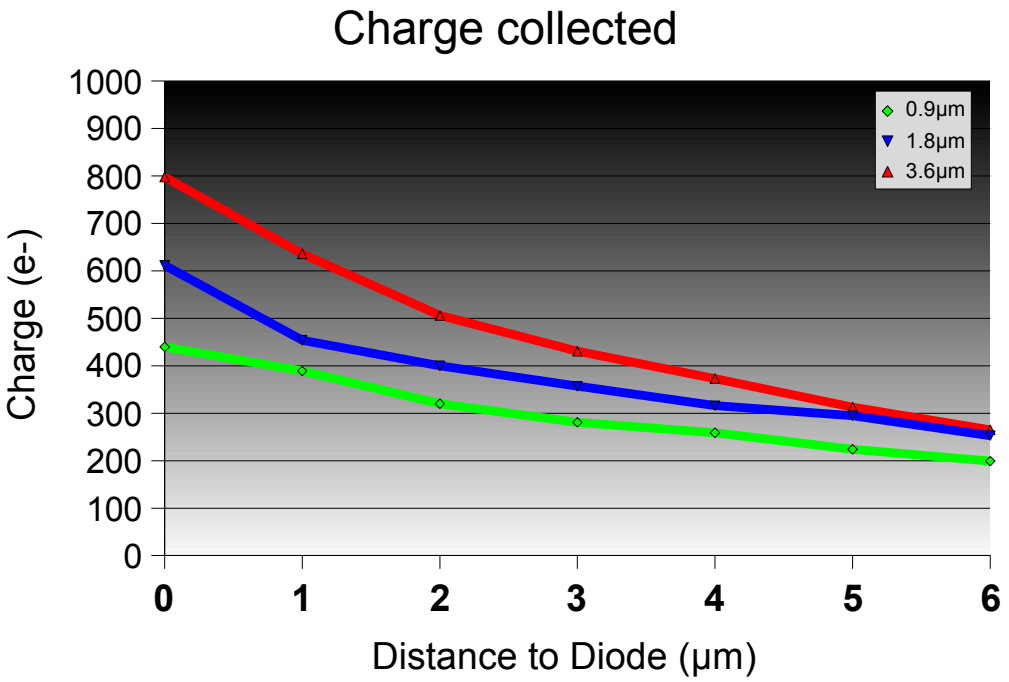
Simulation Setup

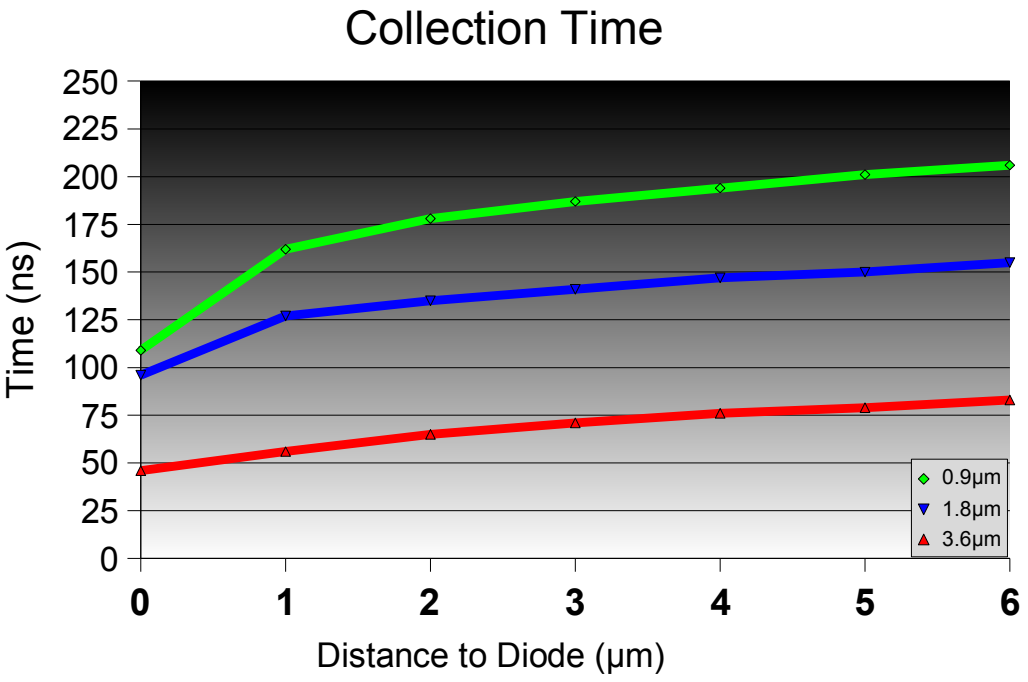


7 Hit Points simulated
1 µm distance



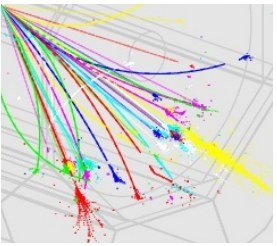
Charge Collection



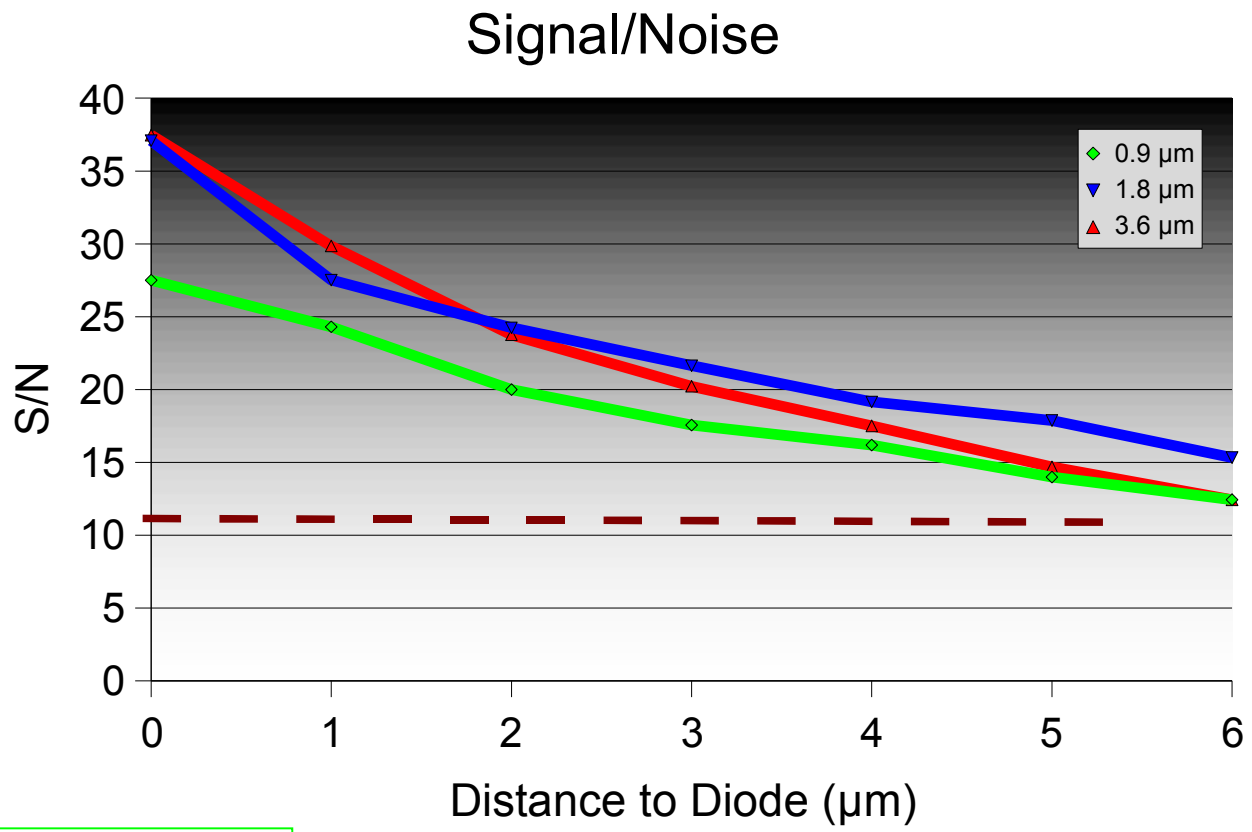


Main parameter to vary is Diode Size

ILC Bunch spacing ~ 300 ns



Signal/Noise

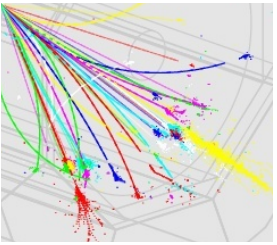


*N.B. S/N 0.9µm N = 16 e^-

*N.B. S/N 1.8µm N = 16.5 e^-

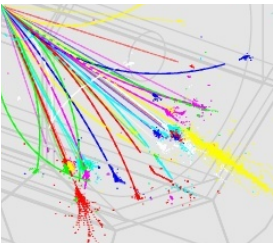
*N.B. S/N 3.6µm N = 21.3 e^-

Signal to Noise > 15 for 1.8 µm Diode Size



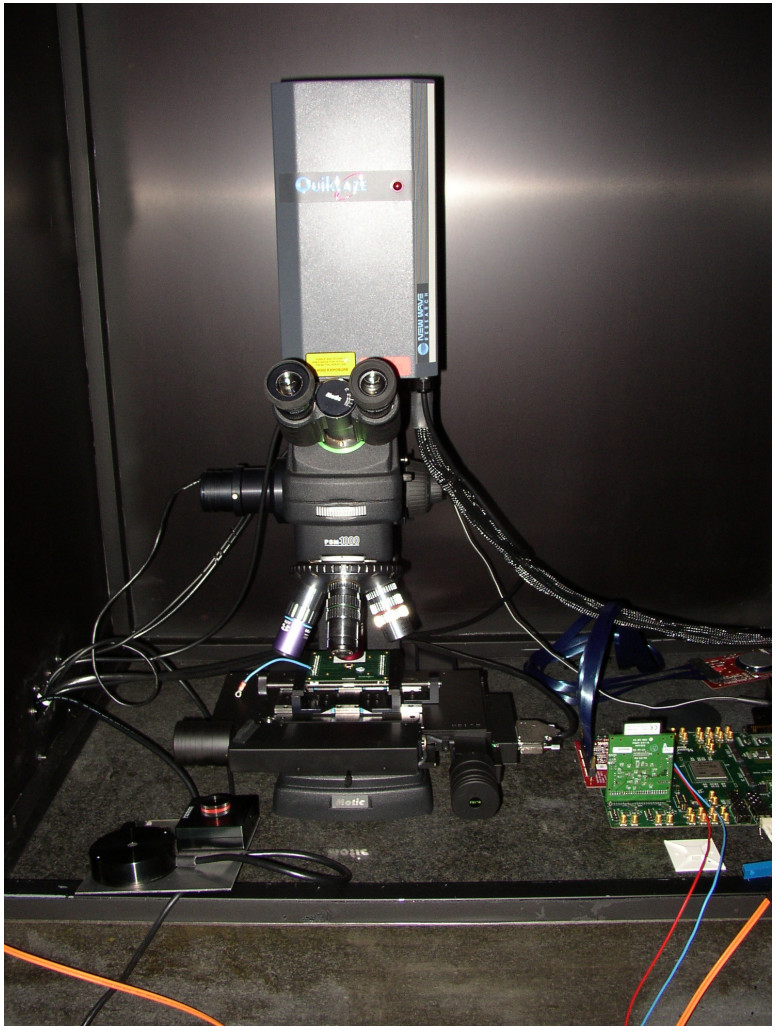
MAPS DAQ & Testing

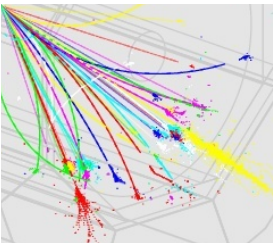
- Development of DAQ board and firmware has started
- Complete test setup foreseen
  - Cosmics
  - Sources
  - Laser
  - Test beam



RAL Laser Test setup

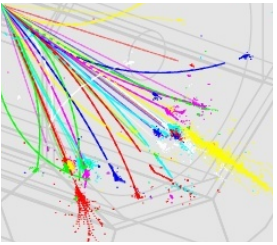
- Powerful Laser setup
- 1064, 532 and 355 nm Wavelength
- Accurate focusing (<2 µm)
- 50 Hz Repetition rate
- Fully automatized
- Will be used to test the CALICE MAPS



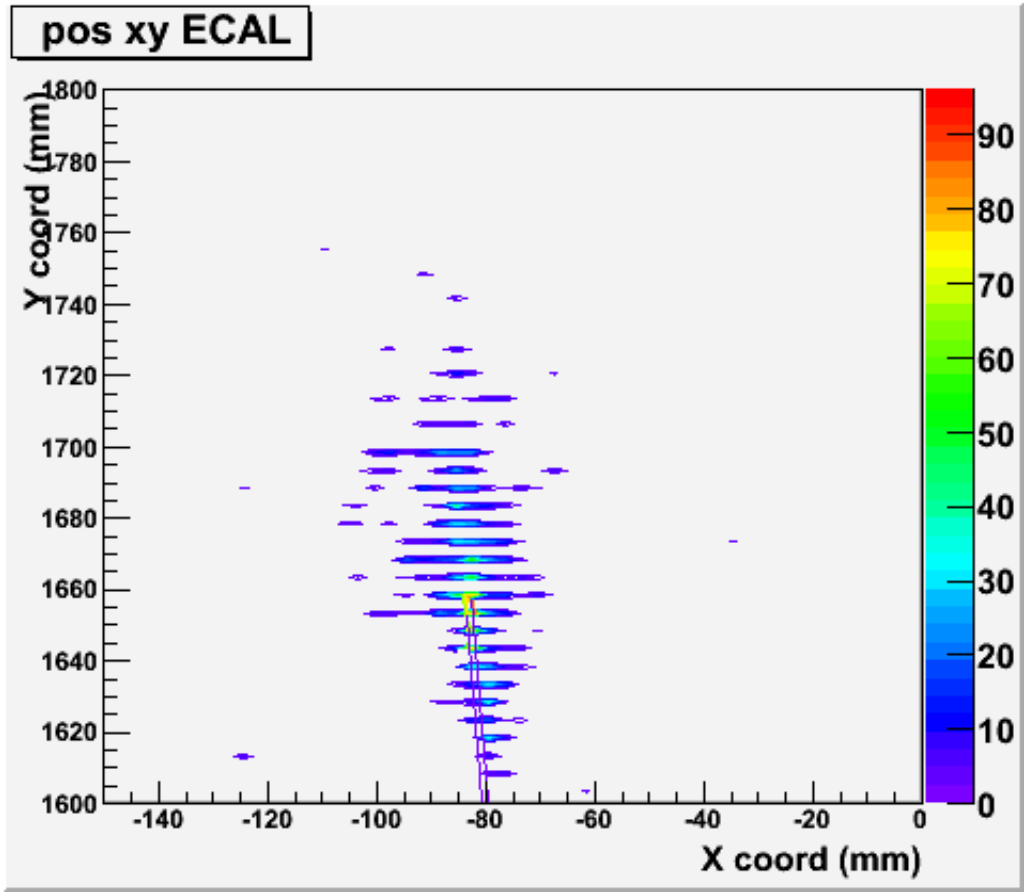


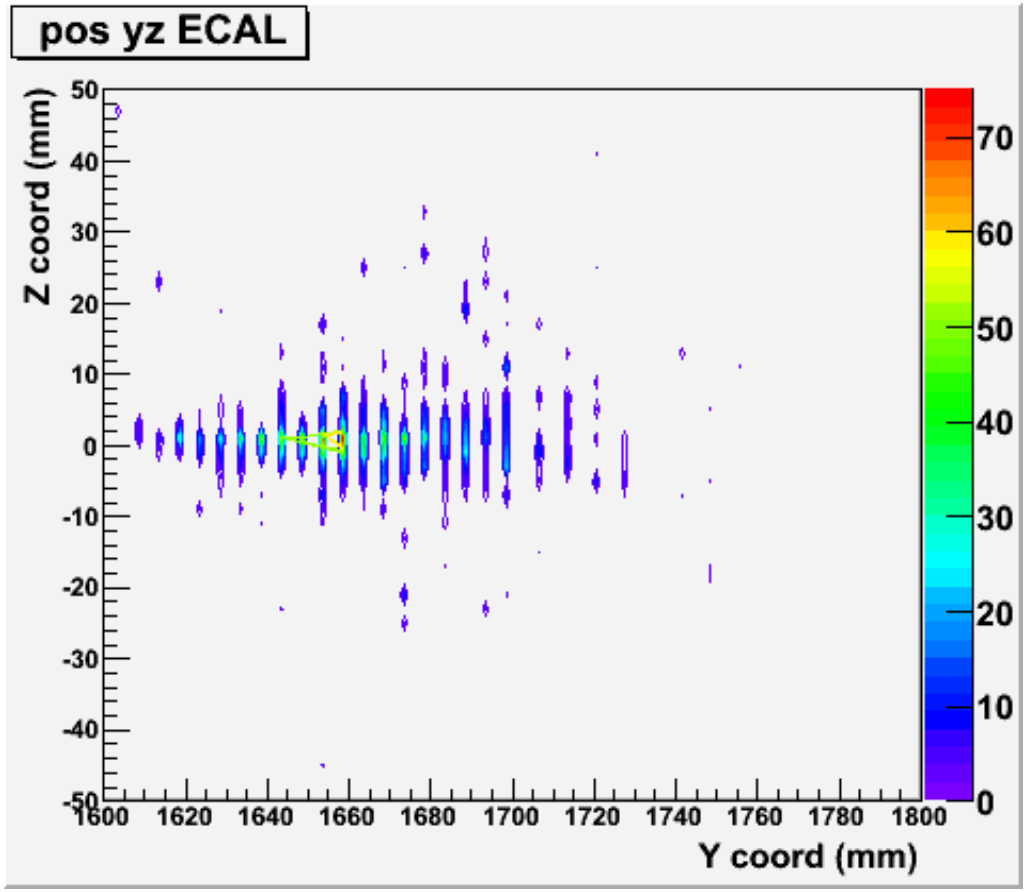
Detector Simulation

- Implementation of the MAPS into GEANT/MOKKA
  - Patched MOKKA 6.02
- 50x50 µm pixel size
- 15 µm "Active Area" (Epi-layer)
- Detector Model used LDC01(Sc)
- ECAL with 30 layers
  - 20 layers 2.1 mm Tungsten
  - 10 layers 4.2 mm Tungsten
- Charge diffusion and thresholds are implemented in a separate "Digitization" step

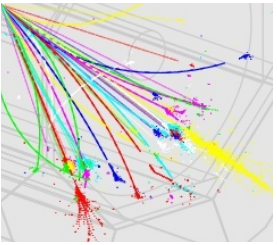


Shower Shapes



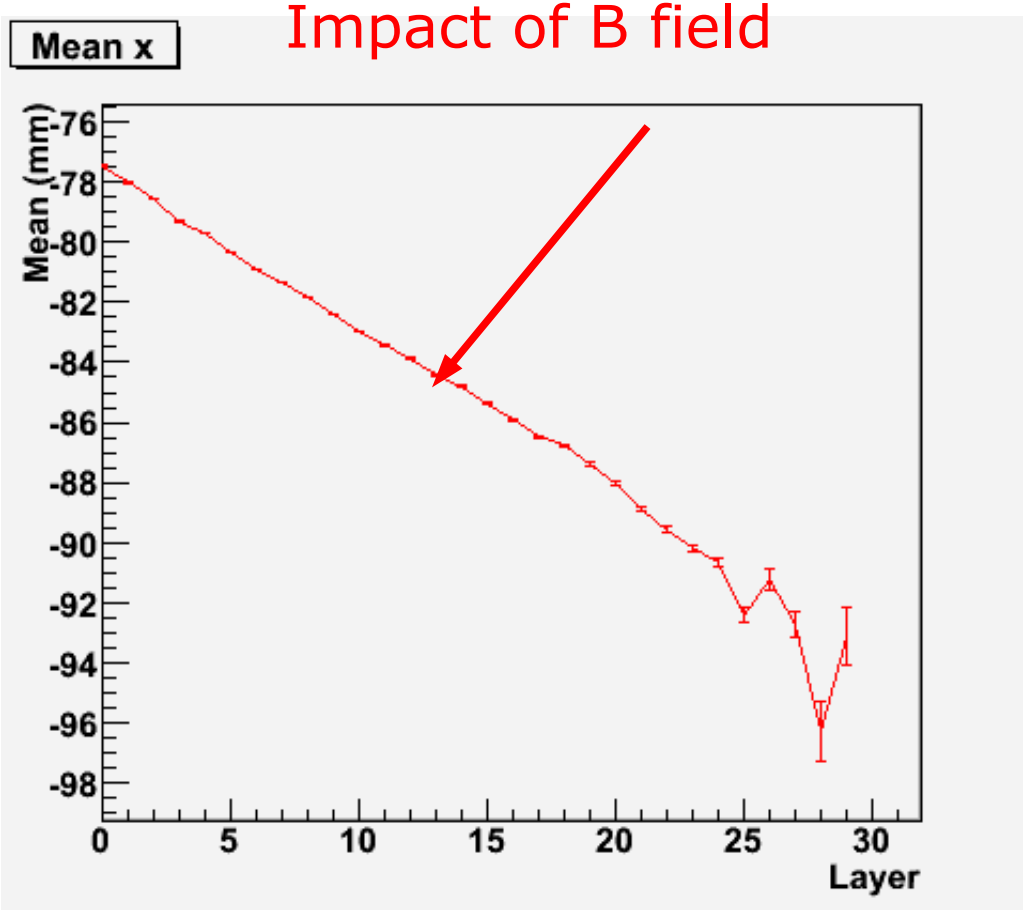


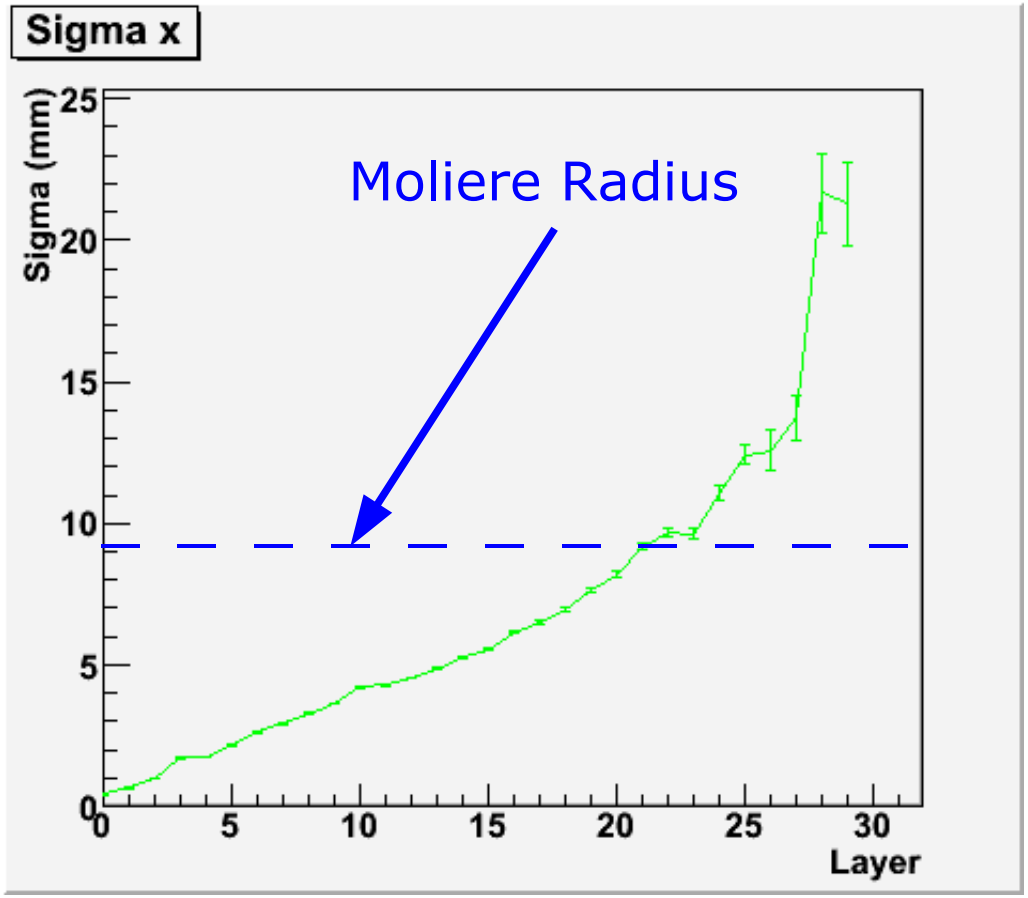
GEANT4 : One 20 GeV Electron shot along y-axis



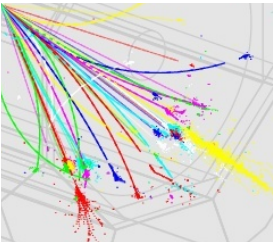
Spatial resolution in x

Impact of B field

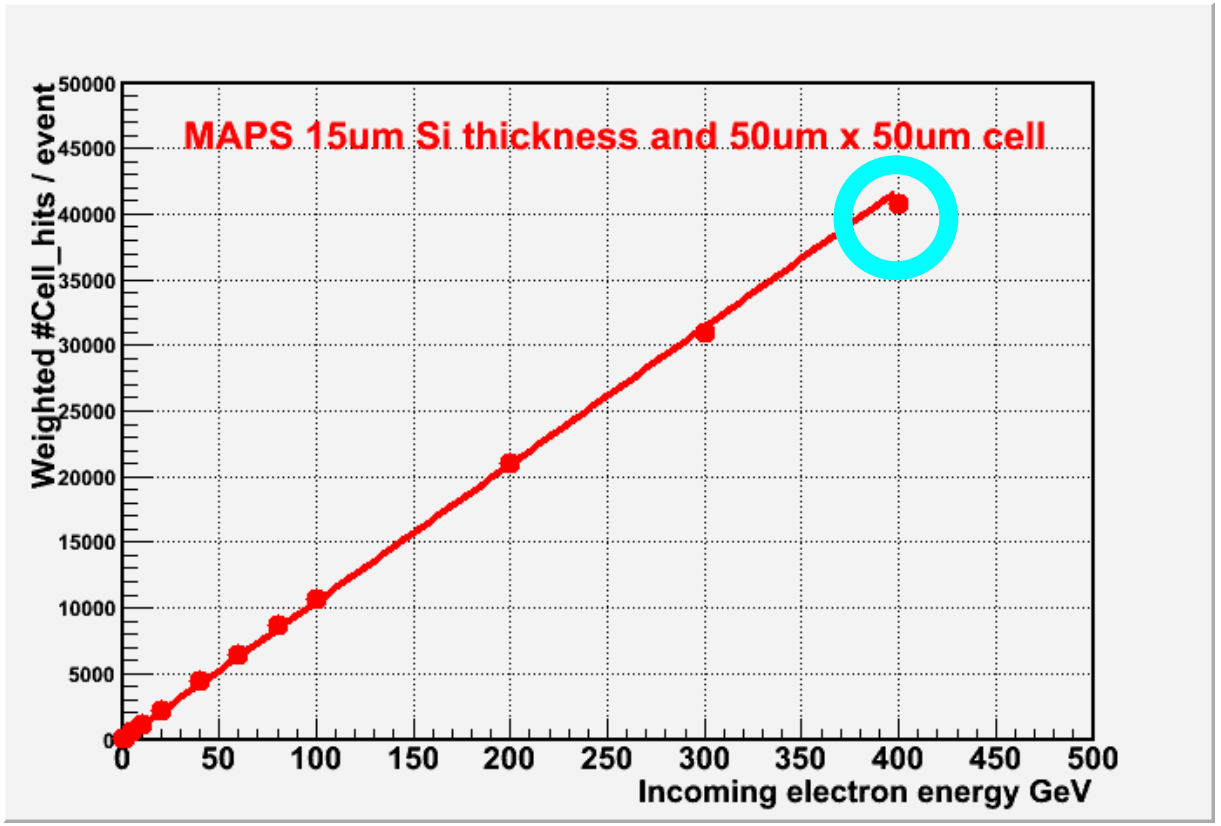




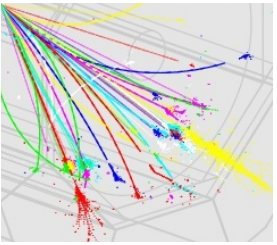
GEANT4 :20 GeV Electrons shot along y-axis



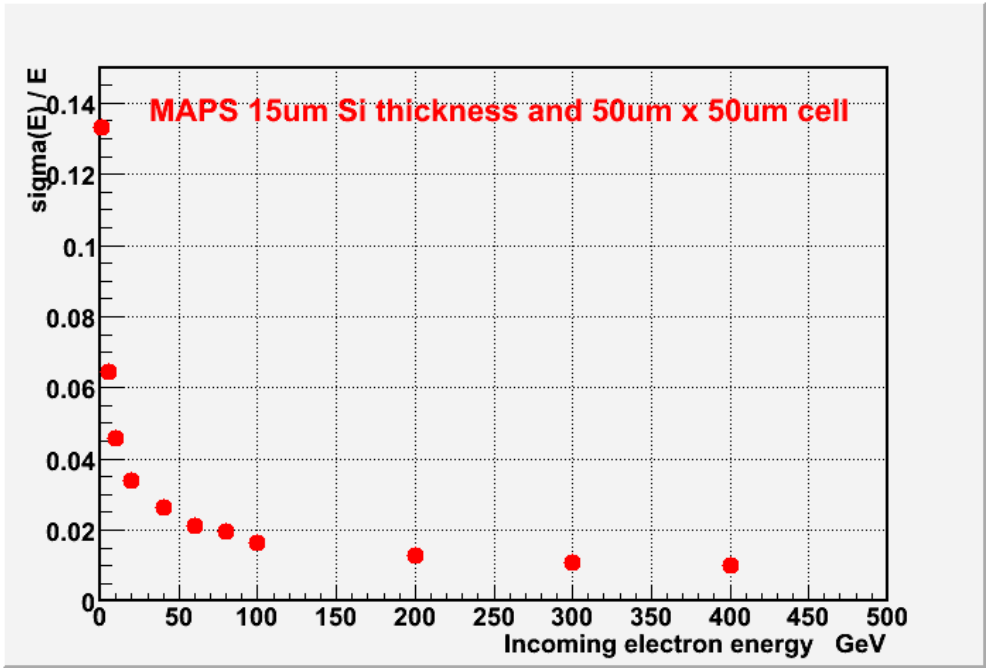
Linear Response

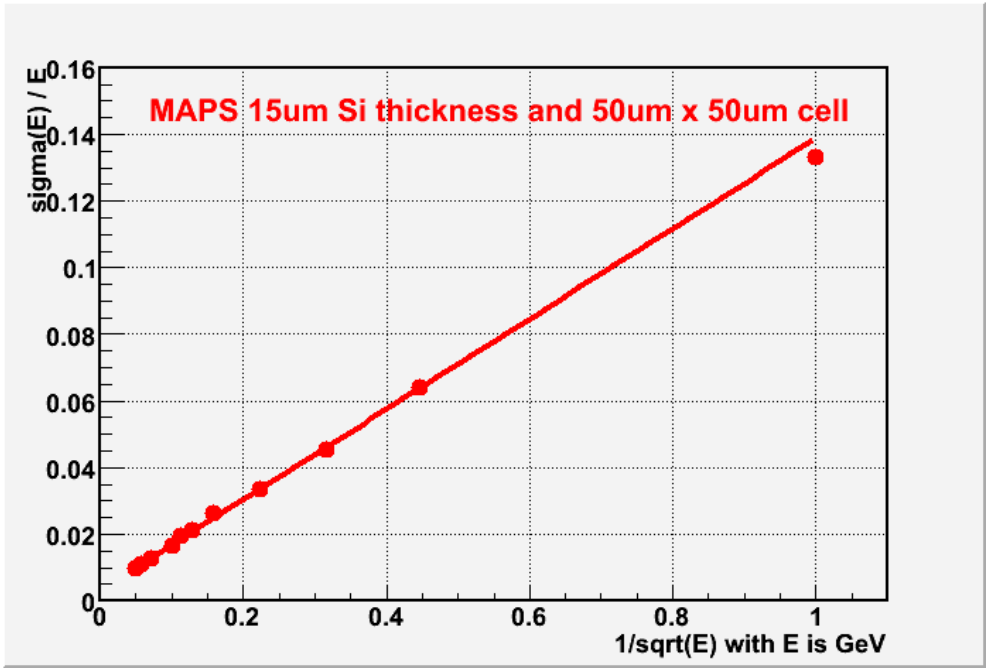


Linear response for electrons up to 400 GeV
GEANT4 level without charge diffusion

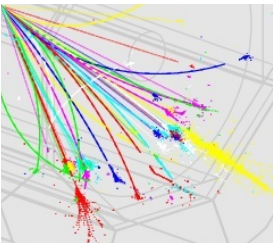


Resolution



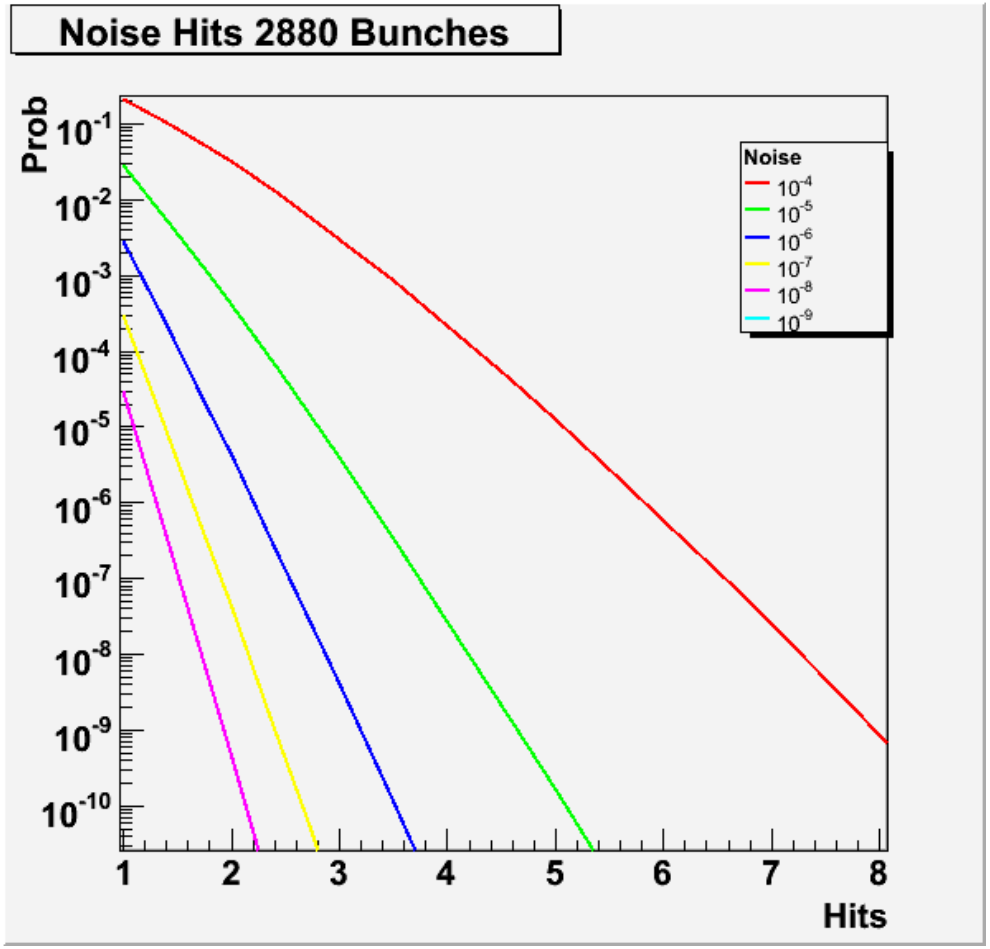


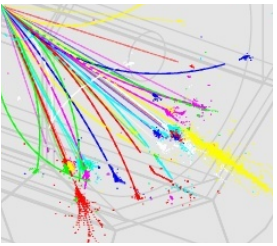
Good resolution over wide energy range
GEANT4 level without charge diffusion



Noise Occupancy

- Noise for 2880 bunches
- Vary noise probability
- With Noise=O(10^{-6})
  - P=0.3 % for 1 hit per pixel
  - P=0.0004 % for 2 hit per pixel
- But O(10^{12}) pixels !
  - ~3 10^{9} single hits
  - ~4 10^{6} double hits
  - ~0 triple hits



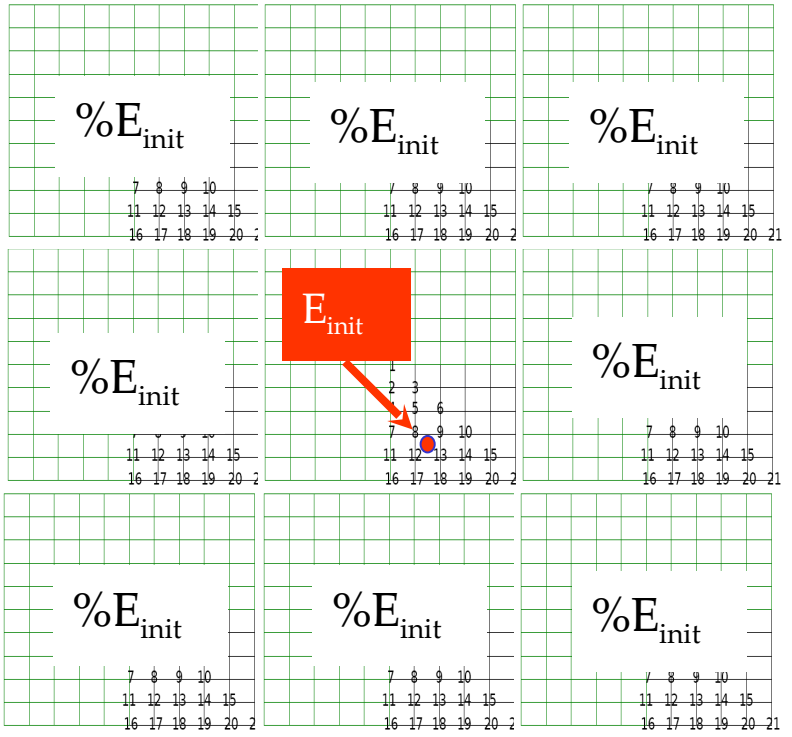


Charge sharing algorithm

Geant4 E_{init} in 5x5 μm² cells

→ Sum energy in 50x50 μm² cells E_{sum}

→ Apply charge spread $E_{after\ charge\ spread}$



← Add noise to signal hits with σ = 90 eV (1 e- ~ 3 eV 30e- noise)

↓ + noise only hits

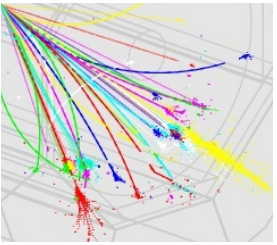
prob. 10^{-6} ➔ ~ 10^{6} hits in the whole detector

BUT in

a 1 cm² tower : ~30 hits in 30 layers.

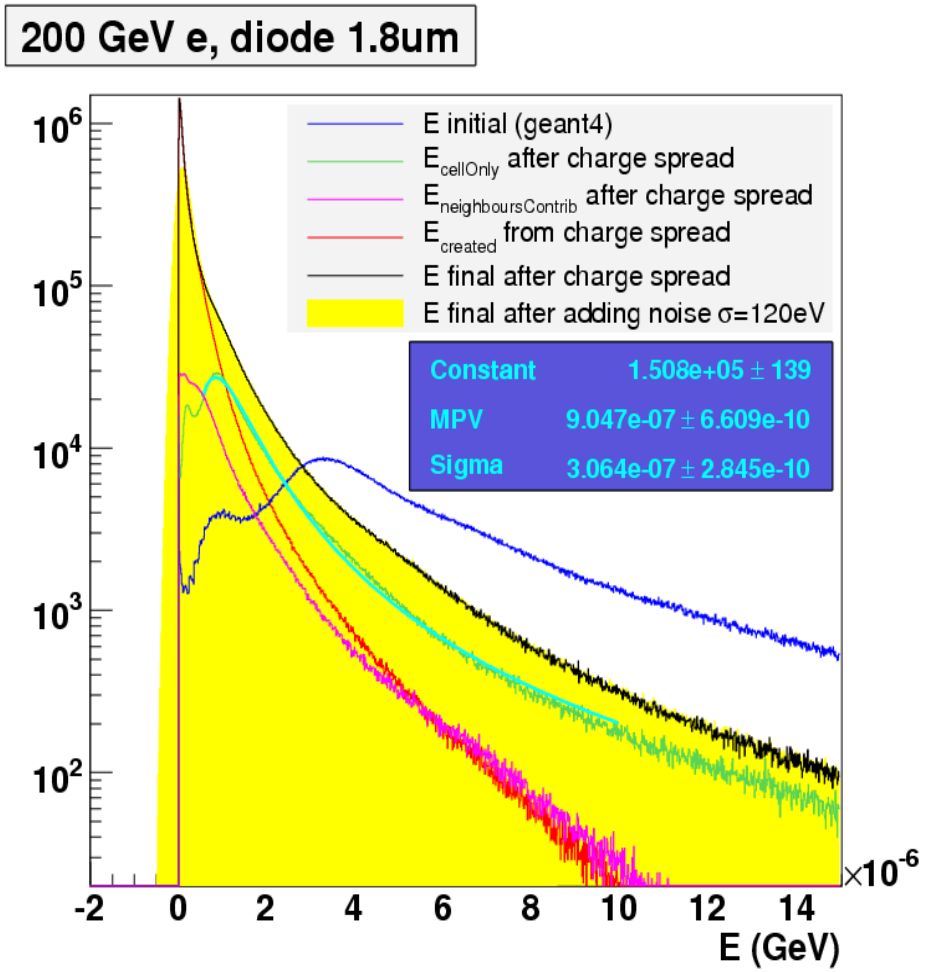
↓ Register the position and the number of hits above threshold

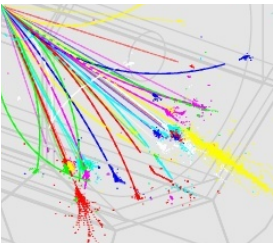
$$\sum E_{neighbours} \sim (50\% - 80\%) \times E_{init}$$



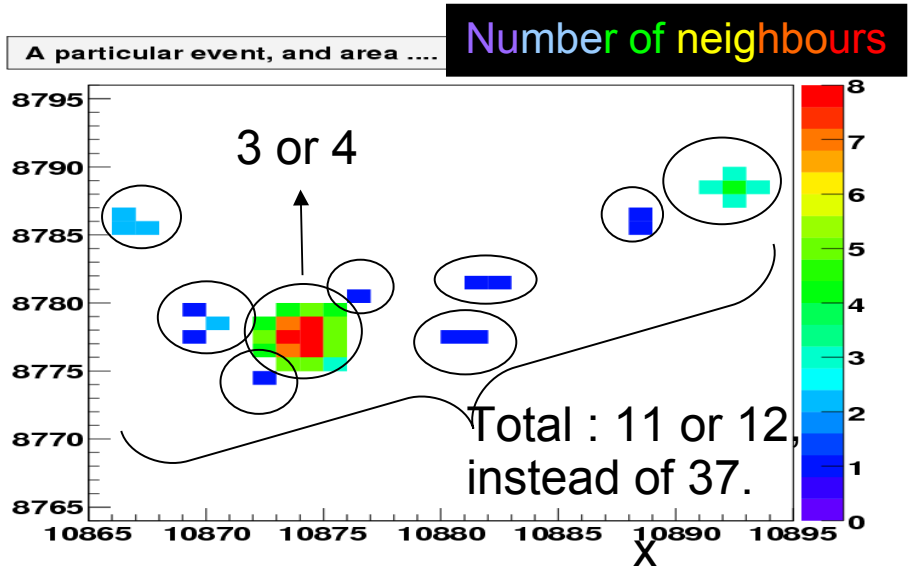
First results

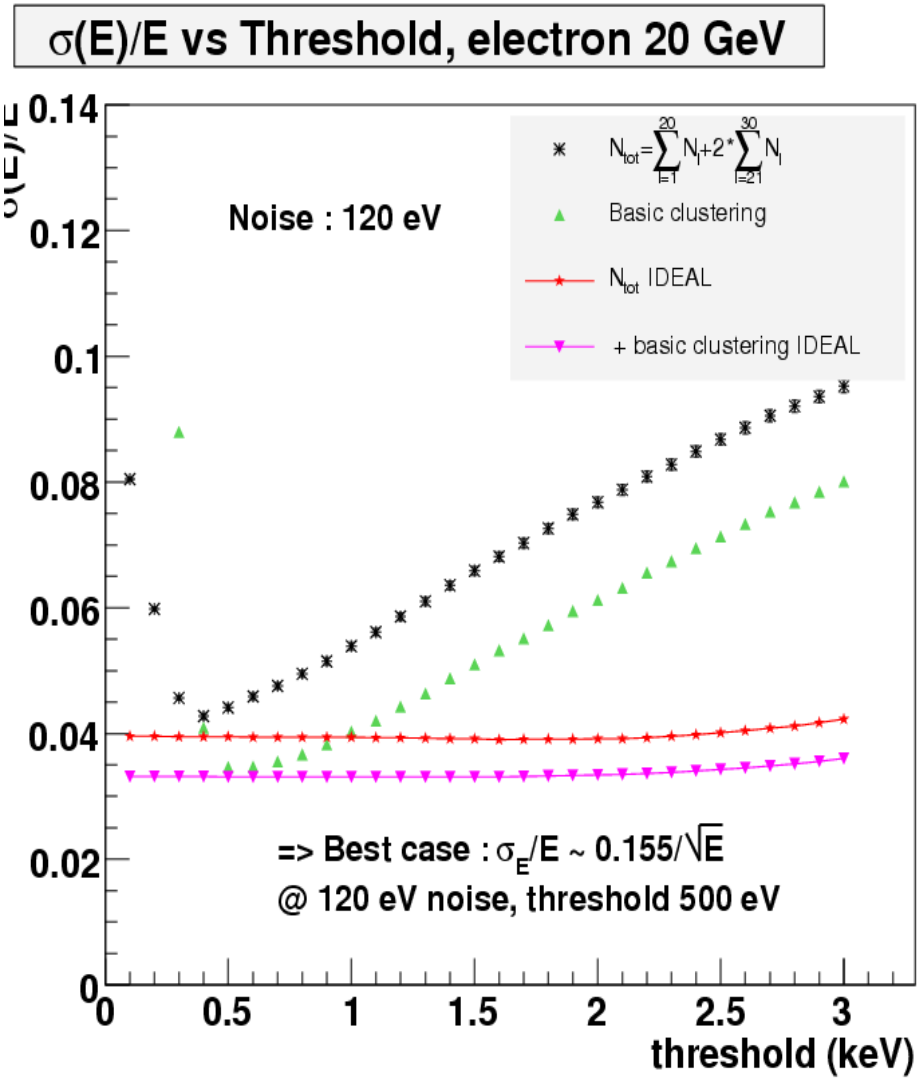
- Algorithm depends on accurate simulation input from Centaurus
- First results shows algorithm work nicely
- Does not take into account deep p-well yet
- Will be updated with the latest pixel simulations and noise estimates





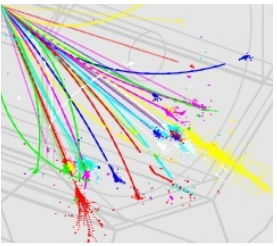
Basic Hit Clustering





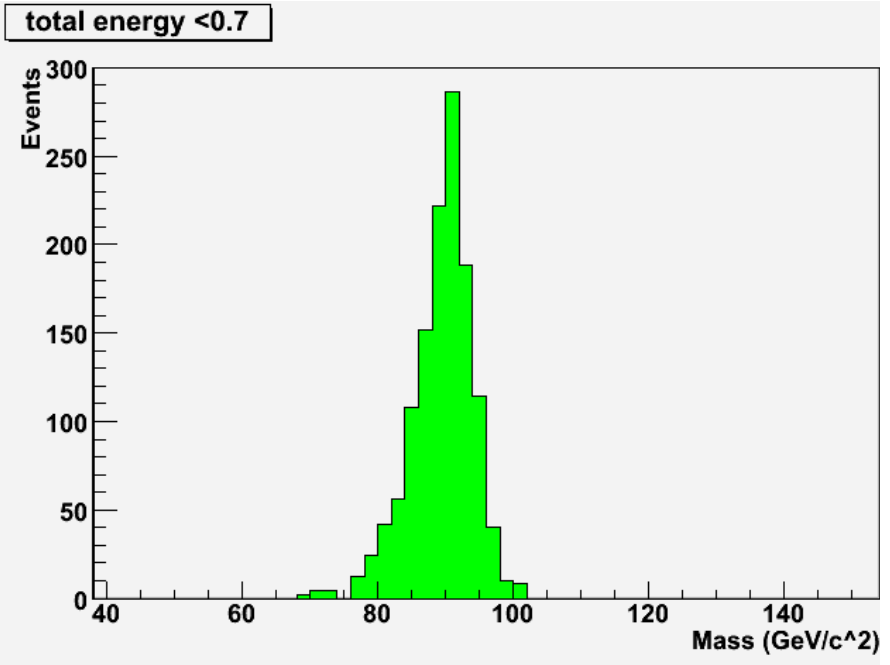
Hit Clustering

- Loop over hits classified by number of neighbors
- Number of neighbors < 8 :
  count only 1 (or 2 for last 10 layers) and discard the neighbors
- 8 neighbors AND one of the neighbor has 8 neighbors :
  count 2 (or 4) and discard the neighbors

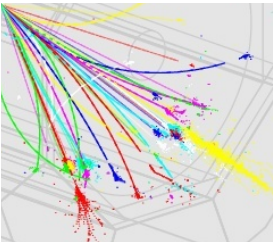


Particle Flow

- Extending **PandoraPFA** to handle Digital ECAL hits
- First development version is running
- Lots of things to improve
  - Calibration of MAPS response is critical
  - Optimize clustering for MAPS
  - Particle ID needs modifications
  - Take advantage of MAPS resolution

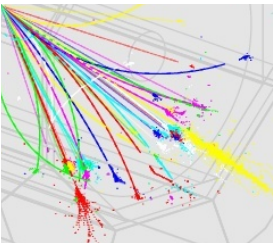


$\sigma_E/\sqrt{E}$ 0.36+0.01 for Z->uds at 91 GeV in the ECAL barrel



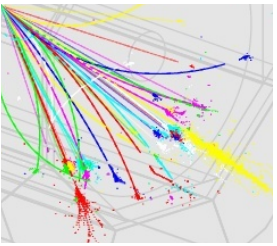
Design Issues

- Pixel parameters
  - Pixel size
  - Number of Diodes / Diode size
- PCB/Readout Chips
- Module structure
- Cooling
- Manufacturing
- Cost



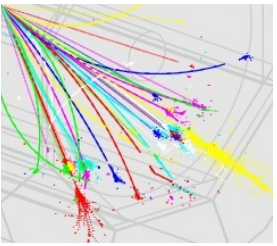
Pixel parameters

- MAPS Pixels improve spatial resolution/granularity by a factor of ~ 1000 compared to analog pad ECAL
- Lower pixel size is set by size of the integrated electronics (lower boundary of 50 µm)
- Upper bound set by charge collection time/efficiency and multiple hits
- No fixed upper bound, reasonable value is around 100 µm
- Best performance found with 4 diodes and 1.8 µm diode size

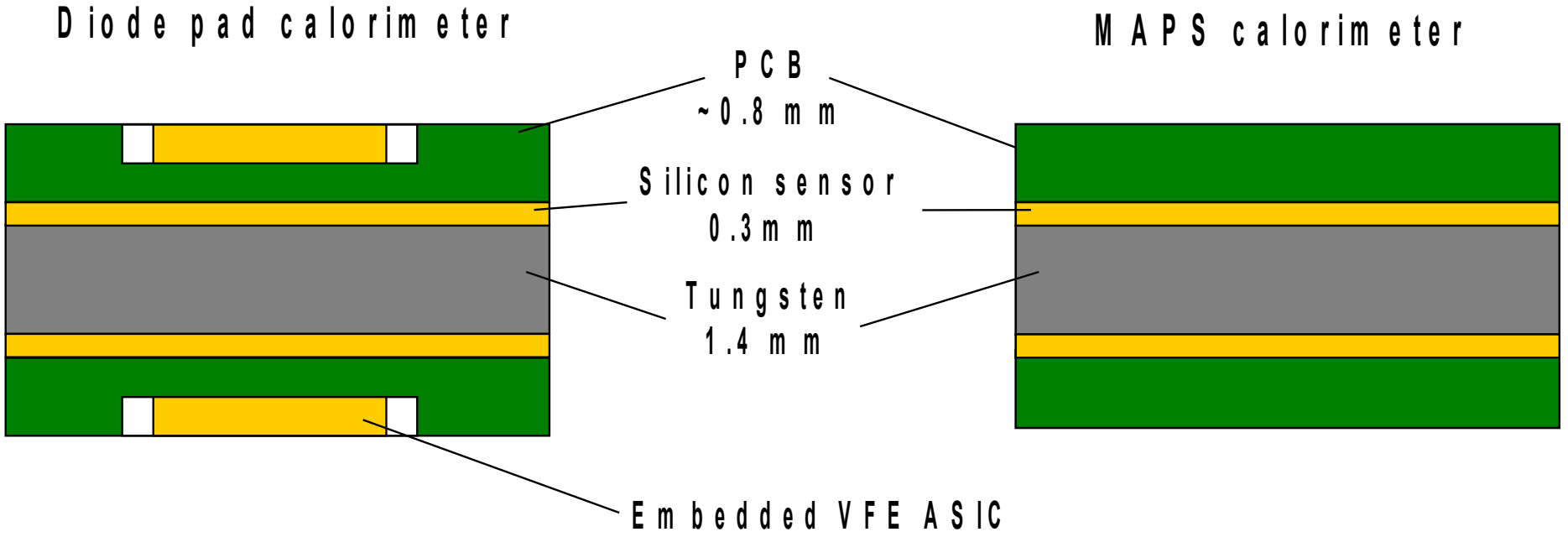


PCB/ Readout Chip

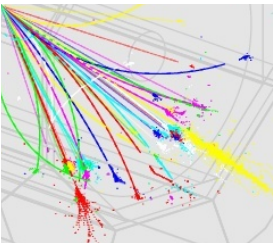
- All the electronics is integrated within the the sensor
- No need for
  - Complicated PCB design
  - Dedicated Readout Chip
- Still needs to provide Power/Clocks/Commands to the MAPS
- Can be done by “Stave Controller” at the end of the Stave



Stave Structure

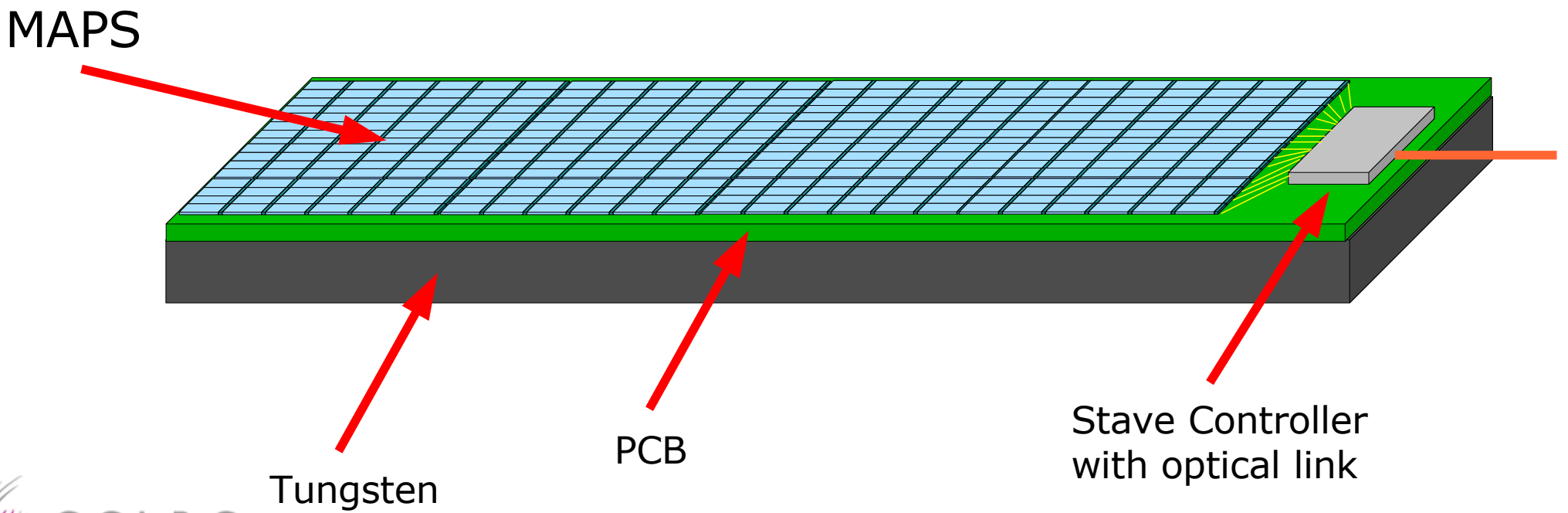


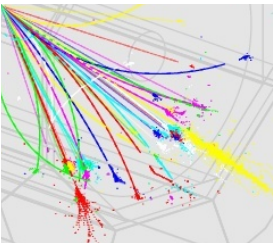
- MAPS can be used as swap-in solution without alterations to the mechanical design (Baseline)
- One can also take further use of MAPS benefits



How it could look like

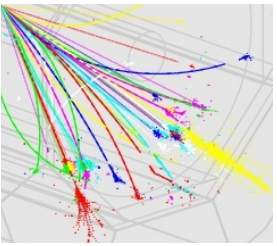
- Take advantage of MAPS benefits
- Lack of hybrids/ASIC allow less complex/thinner PCB
- Thinner sensors (down to 100 µm)
- Bump-bond MAPS





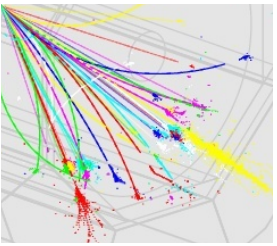
Cooling

- Cooling for the ECAL is a general issue
- Power Savings due to Duty Cycle (1%)
- Target Value for baseline ECAL 4 $\mu W/mm^2$
- Current Consumption of MAPS ECAL: 60 $\mu W/mm^2$ depending on pixel technology
- Compared to analog pad ECAL
  - Factor 1000 more Channels
  - Factor 10 more power
- Advantage: Heat load is spread evenly



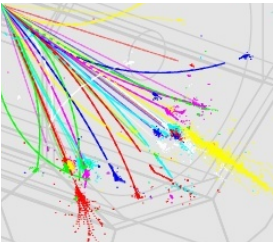
Manufacturing & Costs

- Less complex structure due to lack of VFE ASIC
- Need for large scale process (2000-3000 m^2)
- CMOS is an industry standard process
- Many foundries can do it
- CMOS wafers are readily available
- CMOS is ~2 cheaper than "HEP-style" silicon



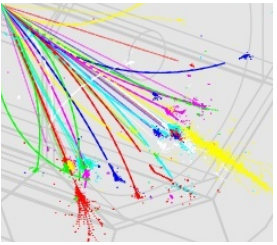
What happens next ?

- Submit Sensor V1.0 Mid April
- Sensor V1.0 due back Mid July
- Improve/enhance GEANT simulation
- Testing Sensor V1.0
- Do physics analyses with a MAPS based ECAL
- Improve sensor simulation with data from V1.0
- Design Sensor V2.0 using all the experience made with V1.0
- Submit Sensor V2.0

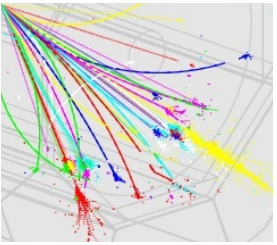


Summary

- MAPS effort is advancing well
- Sensor V1.0 is almost done
- Simulation of MAPS based ECAL made huge progress
- Still quite some challenges ahead
- Interested to work on MAPS ? Contact us !
- Thanks to everyone in the MAPS group for their help in preparing the talk

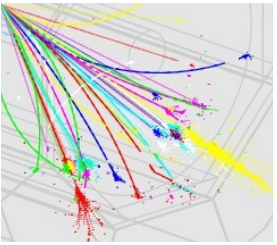


Backup

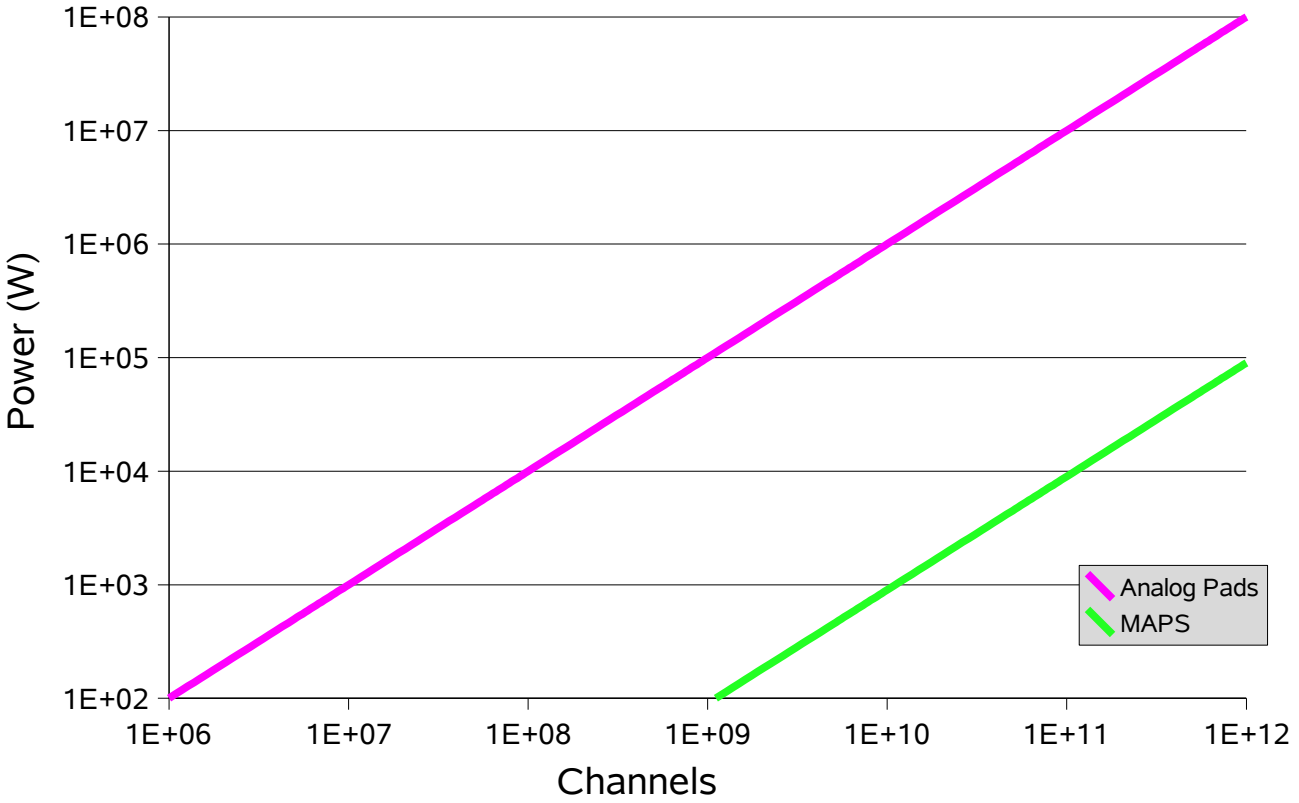


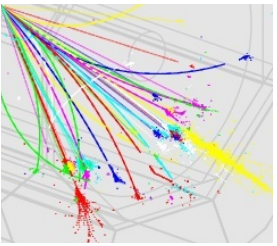
Beam background

- Owen ?



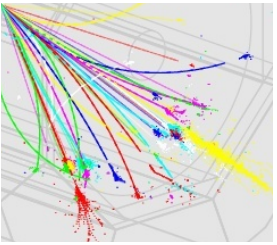
Cooling cont'd





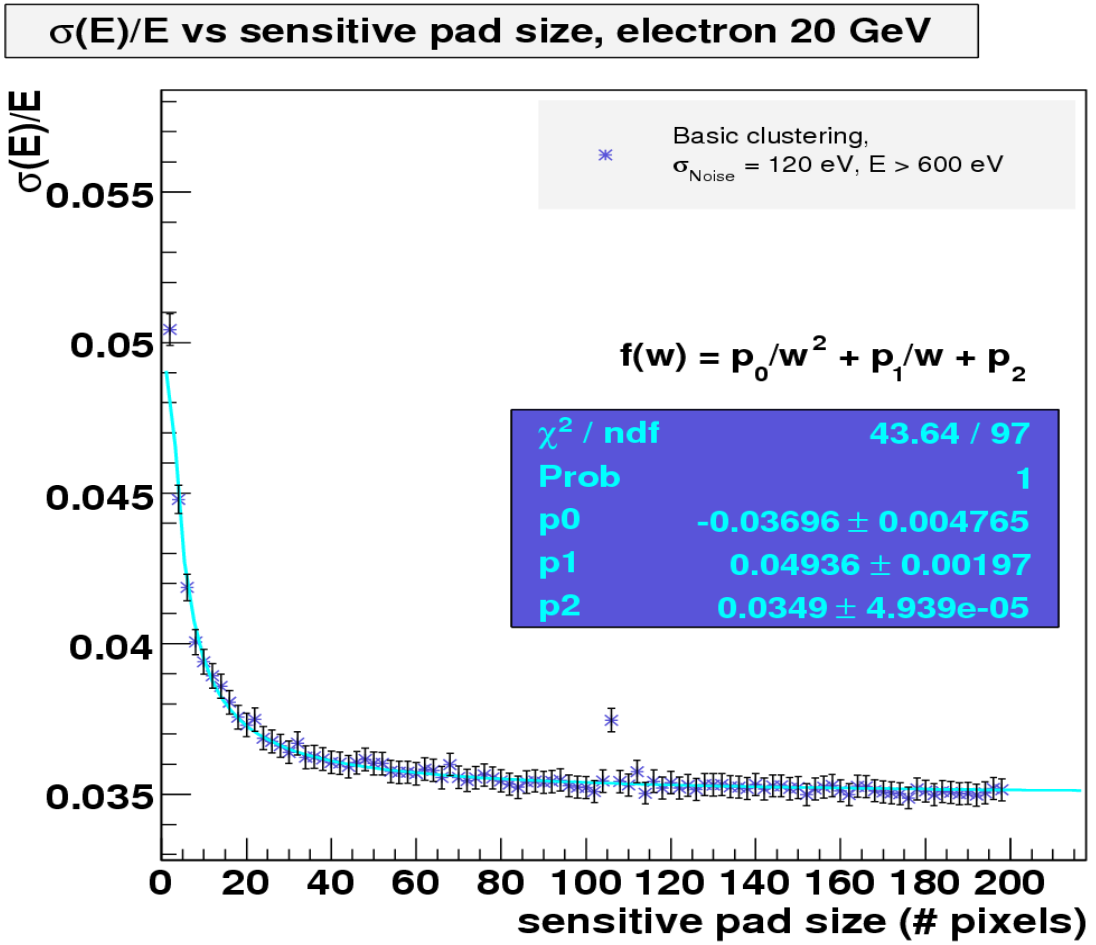
MAPS vs Baseline

	Baseline	MAPS
Sensor material	high resistivity	CMOS
Pixel size	5 x 5 mm	50 x 50 μm
Readout type	analog	digital
Readout Channels	$8x10^7$	10^{12}
Power consumption		



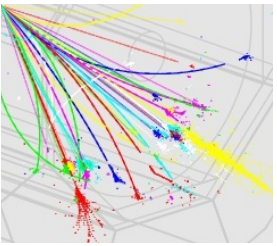
Dead area

- We need 5 dead pixels every ~42 sensitive pixels (under study) for the pixels logic.



σ(E)/E = α/√E
➔α = 0.1561 asymptotical value
➔α = 0.161 @ 42 sensitive pixels

➔ 3 % increase : we can live with that !!



DAQ data volume

- Physics rate is not the limiting factor
- Beam background and Noise will dominate
- Assuming 2880 bunches and 25 bits per Hit
  - 10^6 Noise hits per bunch
  - ~O(1000) Hits from Beam background per bunch (estimated)
- Per bunch train
  - ~9 Gigabyte Data
  - Readout Required 41 GB/s
  - CDF SVX-II can do 18 GB/s already