LCFI Status Report

Konstantin Stefanov on behalf of LCFI

CALICE UK Meeting, 27 March 2007

- **Introduction**
- **LCFI Vertex Package**
- **Vertex Detector R&D**
  - **Column-Parallel CCDs**
  - **In-situ Storage Image Sensors**
  - **Mechanical support studies**
- **Areas of Common Interest for LCFI and CALICE**
- **Conclusion**

Vertex Package – Overview (based on Sonja's presentations)

Goal:

- **Evaluation of the performance of the vertex detector and optimisation of its parameters**
  - **Development of tools**
  - **Studies of benchmark physics processes**
- **Vertex Package interfaces to the MarlinReco framework, adding important and so far missing contribution**
  - **Framework consists of software modules (processors)**
  - **Enabled and configured via XML file**
- **Path towards full MC simulation and reconstruction (MOKKA + MarlinReco)**
- **Developed by Ben Jeffery and Erik Devetak (Oxford), Mark Grimes (Bristol), under the leadership of Sonja Hillert (Oxford)**

Vertex Package – Status

Status:

- Fully functional
- ≈20,000 lines of C++ code
- Currently finalising issues with integration with the MARLIN framework and verifying performance
- Release is expected any time now
- Eagerly awaited worldwide
- After the release:
  - Will move to using full pattern recognition in MarlinReco, including all silicon detectors and the TPC (currently uses track cheaters)
  - Use more realistic Vertex detector geometry (ladders) instead of cylinders
- Tutorials for new users to be held starting in May

Vertex Package – Structure

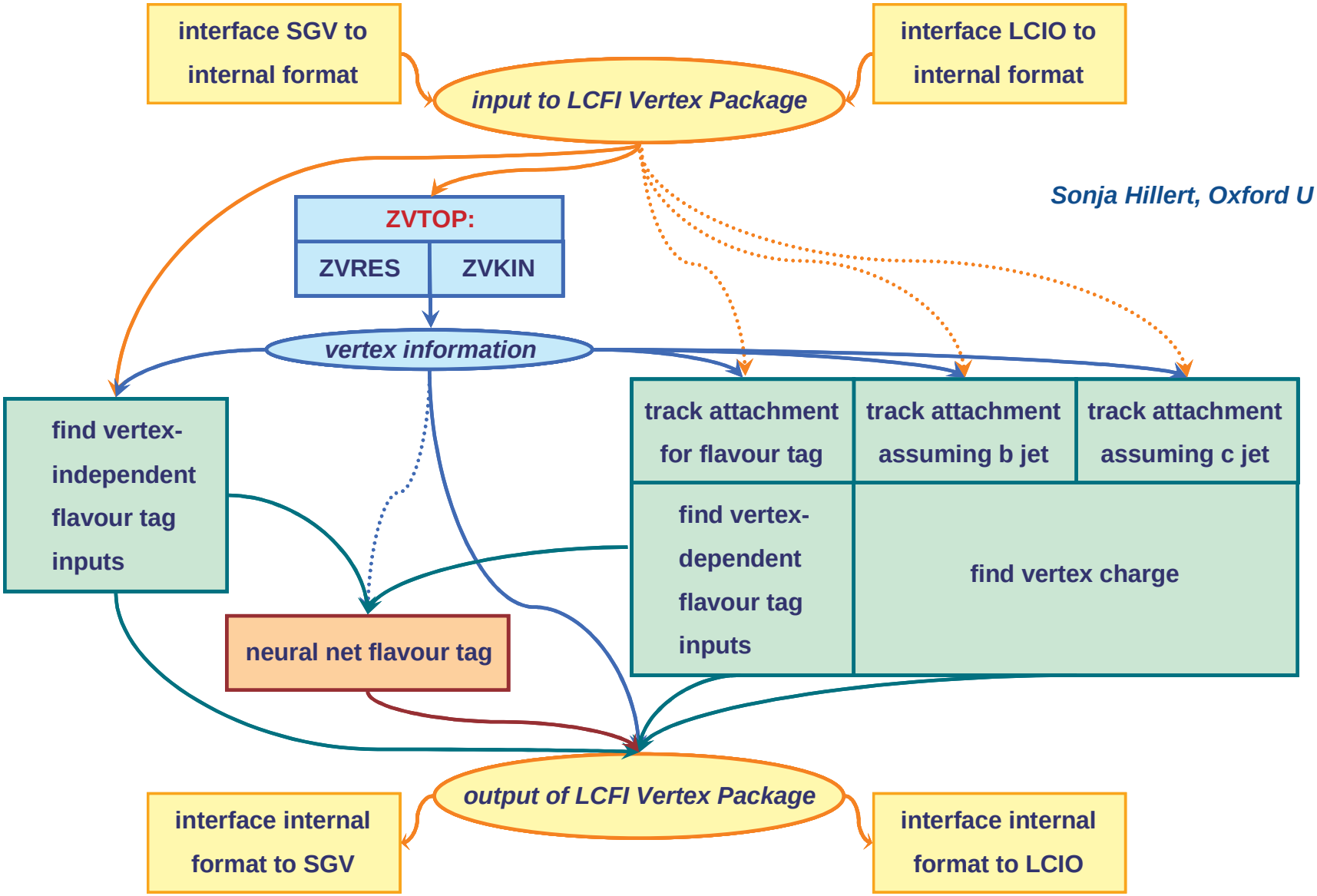
Input: LCIO events (SGV has been extended to write LCIO)

Output: Vertex information, flavour tag inputs, NN flavour tag output and vertex charge, output as LCIO file, using dedicated Vertex class

Code provides 9 Marlin processors:

1. Track selection cuts for ZVTOP, flavour tag and vertex charge
2. IP-fit processor
3. ZVRES – “classical” branch of the ZVTOP vertex finder, written for and extensively used at SLD
4. ZVKIN – “ghost track” algorithm based on kinematic dependencies on heavy flavour decays
5. Jet flavour MC truth information
6. Calculation of NN input variables and vertex charge from tracks and ZVTOP output
7. Training neural nets for flavour tag
8. Getting NN outputs for trained nets
9. PlotProcessor to plot flavour tag purity vs. efficiency

Vertex Package – Process Flow



Vertex Package – Verification

- Extensive verification over many months, a lot of hard work
  - 1st stage: comparisons between SGV and MARLIN using identical input events (SGV and the old FORTRAN ZVTOP very well known)
  - 2nd stage:
    - Same events from the 1st stage (PYTHIA) passed through full MC simulation MOKKA
    - Collaboration with DESY and MPI Munich for production of the input data sample
    - Comparisons of MARLIN (MOKKA input) with MARLIN (SGV input) and former BRAHMS results from TESLA TDR
  - First indications: MARLIN (C++) slightly outperforms SGV (FORTRAN)
- Debugging using the tool *Valgrind* http://valgrind.org – helps find memory leaks, improves performance by using profilers
- Documentation using *Doxygen* http://www.doxygen.org – provides automatic documentation from commented C++ code

Vertex Detector R&D

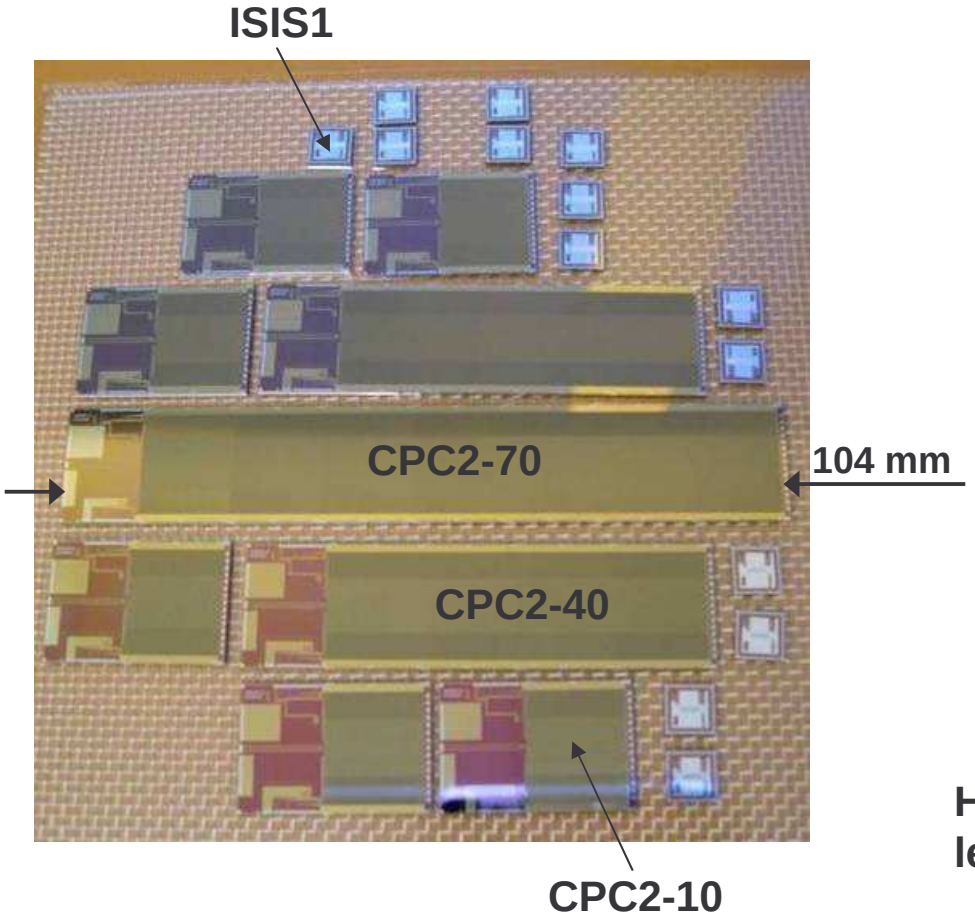
What is required for the vertex detector at ILC:

- **Excellent point resolution (3.5 μm), small pixel size = 20 μm, close to IP**
- **Low material budget (≤ 0.1% X_0 per layer), low power dissipation**
- **Fast (low occupancy) readout – challenging, two main approaches**
  - **Column parallel readout during the 1 ms beam at 50 MHz (L1) or 25MHz (L2-L5)**
  - **In-situ signal storage, readout in the 200 ms – long gap**
- **Tolerates Electro-Magnetic Interference (EMI)**

What LCFI has done so far:

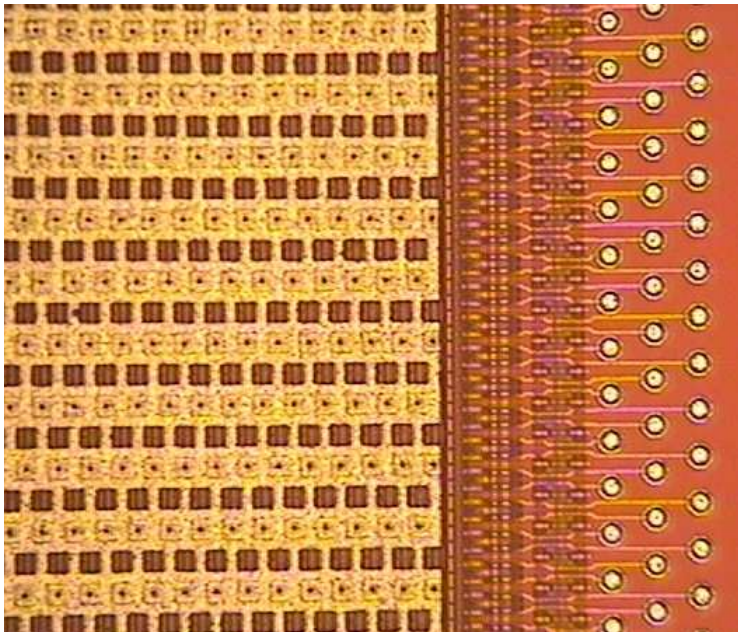
- **Made 2 generations of Column Parallel CCDs: CPC1 and CPC2**
- **In-situ Storage Image Sensor – proof of principle device ISIS1 designed and tested**
- **CMOS readout chips for CPC1/2: 2 generations, bump bonded to the CCDs**
- **Driver chip for CPC2 designed and manufactured**
- **Built lots of electronics to support the detectors**
- **Extensive tests of stand-alone devices and hybrid bump-bonded assemblies**

Second Generation CPCCD : CPC2



- CPC2 wafer (100 Ω.cm/25 µm epi and 1.5kΩ.cm/50 µm epi)
- Low speed (single level metallisation) and high speed versions

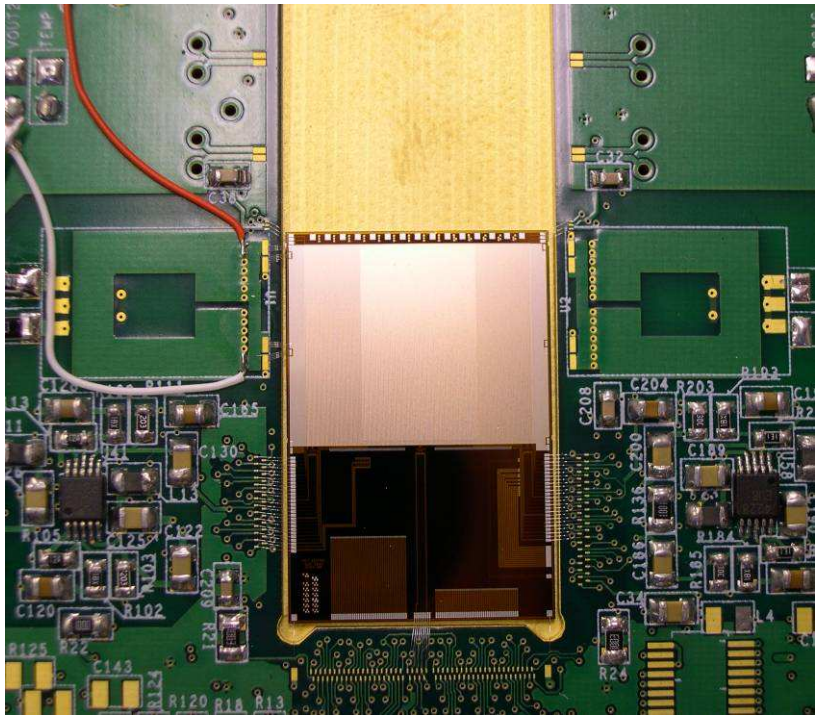
Busline-free CPC2



High speed (busline-free) devices with 2-level metal clock distribution:

- The whole image area serves as a distributed busline
- Designed to reach 50 MHz operation
- Important milestone for LCFI

Busline-free CPC2

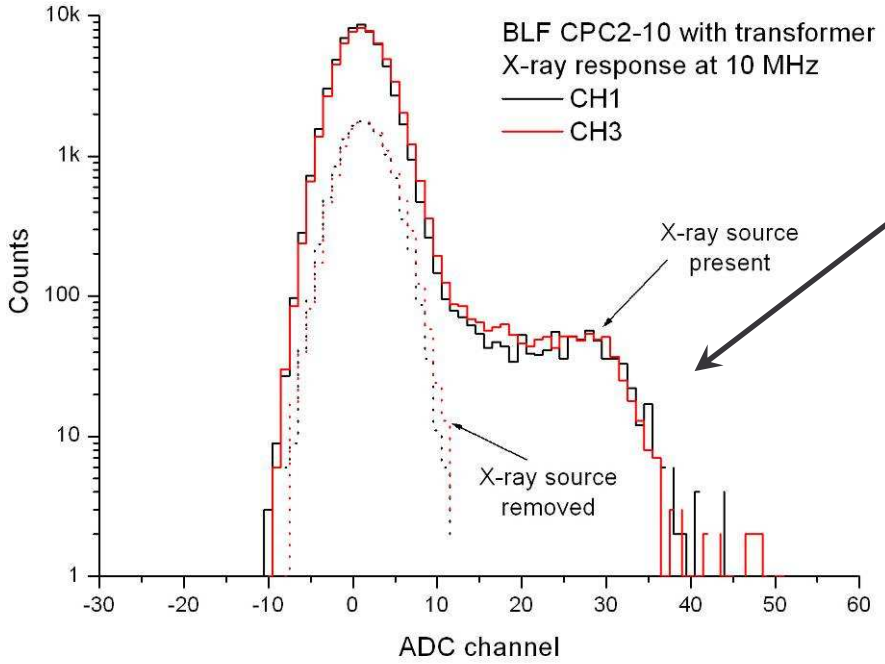


CPC2-10 clocked and working at 45 MHz!

CCD output (2-stage source follower), ≈ 2 V_{pk-pk} clocks

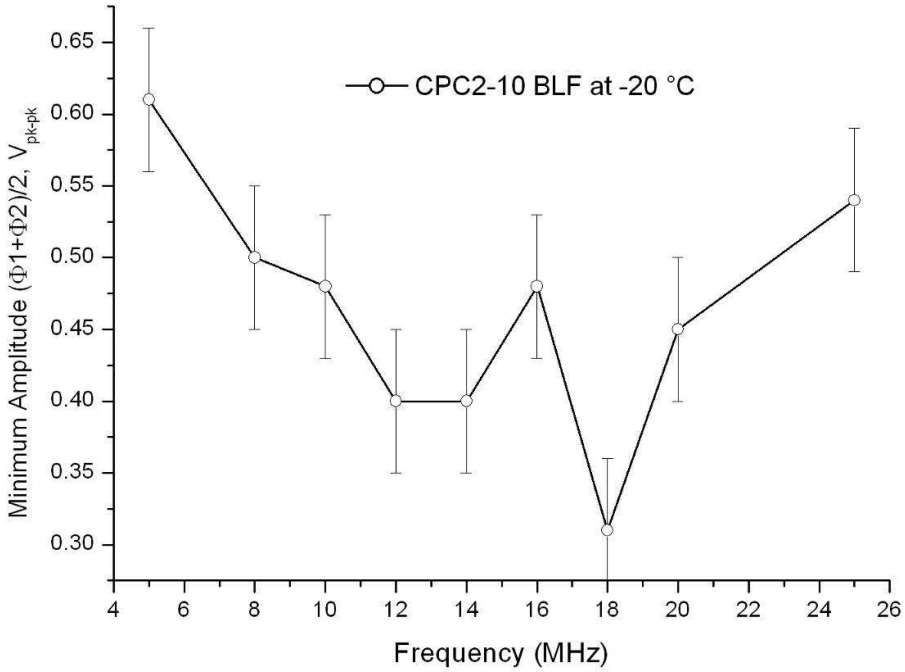
- **First tests showed clear X-ray hits at up to 45 MHz despite the huge clock feedthrough**
- **Transformer drive is challenging due to numerous parasitics**
- **Major result for LCFI**
- **But that is not all…**

Busline-Free CPC2

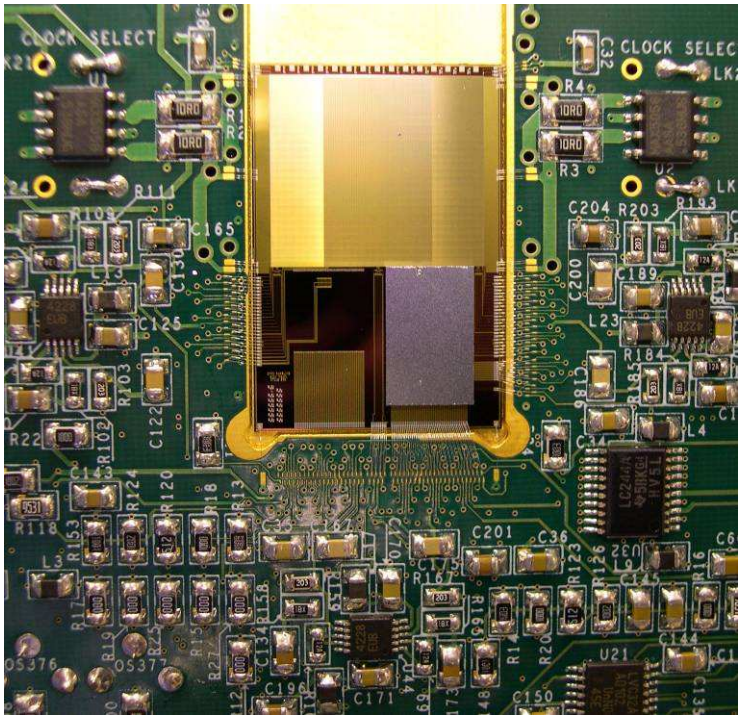


- **Hard to believe, but… clock amplitude is only 0.4 V_{pk-pk}**
- **At lower amplitudes charge transfer deteriorates**
- **Significant noise induced from the clock signals**

- **Low clock amplitude due to very low inter-gate implant barrier**
- **Resonance effect excluded**
- **Further tests will continue using CPD1 CMOS driver chip**

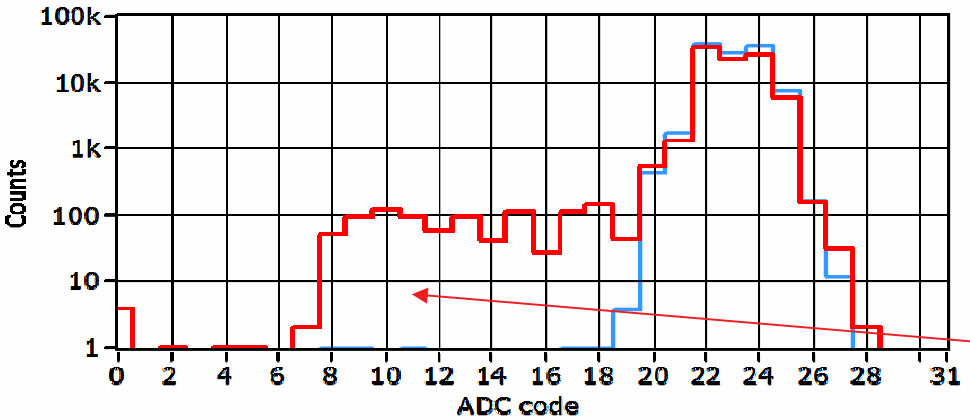


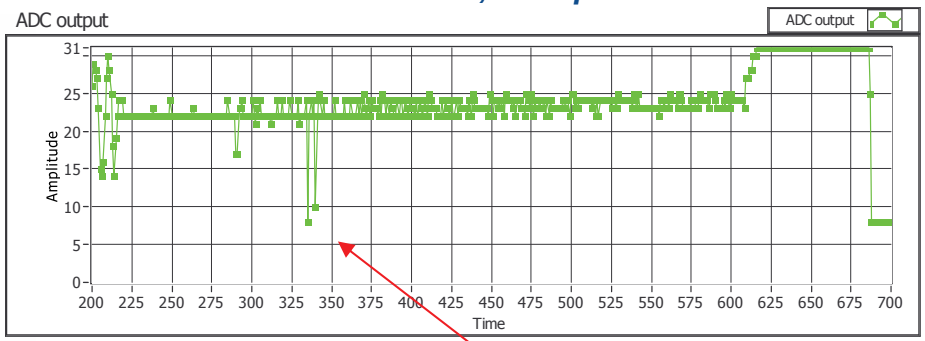
CPC2/CPR2 Hybrid Assembly Tests



- Two CPC2 wafers worth of bump-bonded assemblies received
- Tests have started
- First response to X-rays observed, but not all has gone smoothly

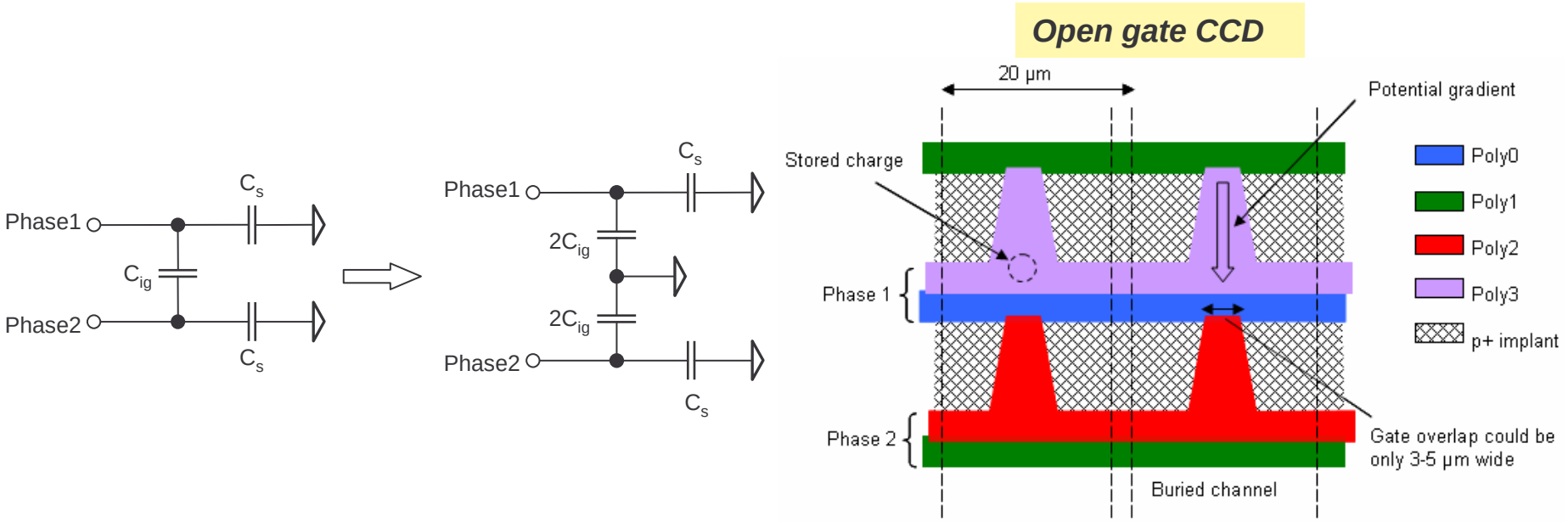
Tim Woolliscroft, Liverpool U





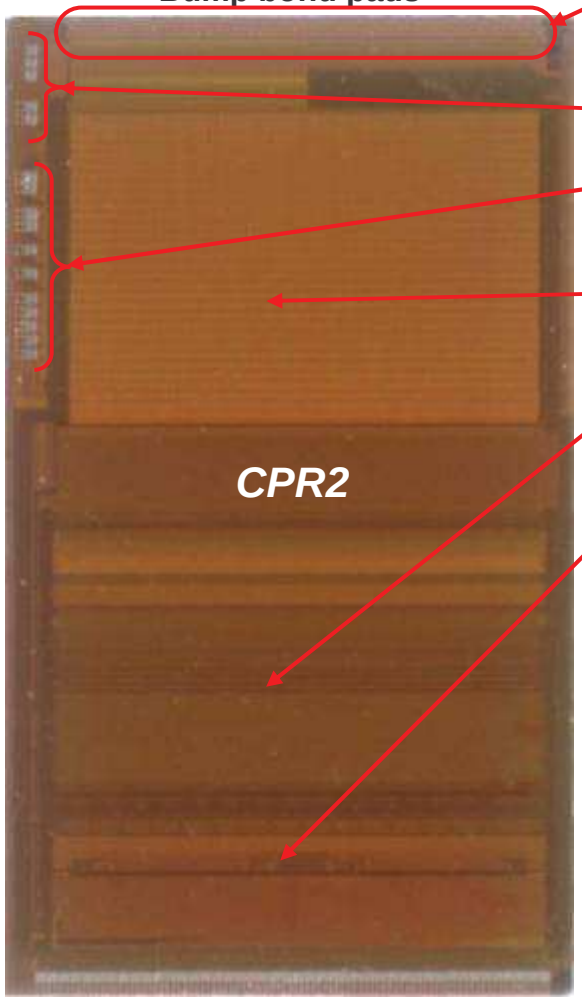
^{55}Fe signal

New Ideas: CCDs for Capacitance Reduction



- **High CCD capacitance is a challenge to drive because of the currents involved**
  - **Can we reduce the capacitance? Can we reduce the clock amplitude as well?**
  - **Inter-gate capacitance C_{ig} is dominant, depends mostly on the size of the gaps and the gate area**
  - **Open phase CCD, "Pedestal Gate CCD", "Shaped Channel CCD" – new ideas, could reduce C_{ig} by ~4!**
- **Have already designed numerous small CCDs to test several ideas on low clock and low capacitance, together with e2V Technologies**

Readout Chips – CPR1 and CPR2



Voltage and charge amplifiers 125 channels each

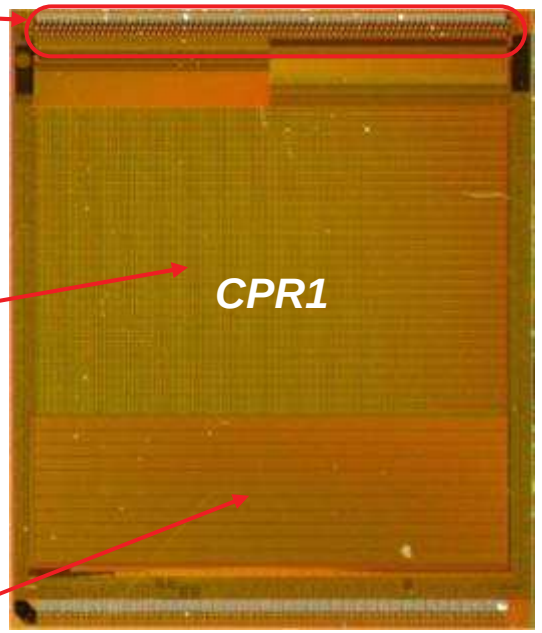
Analogue test I/O

Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

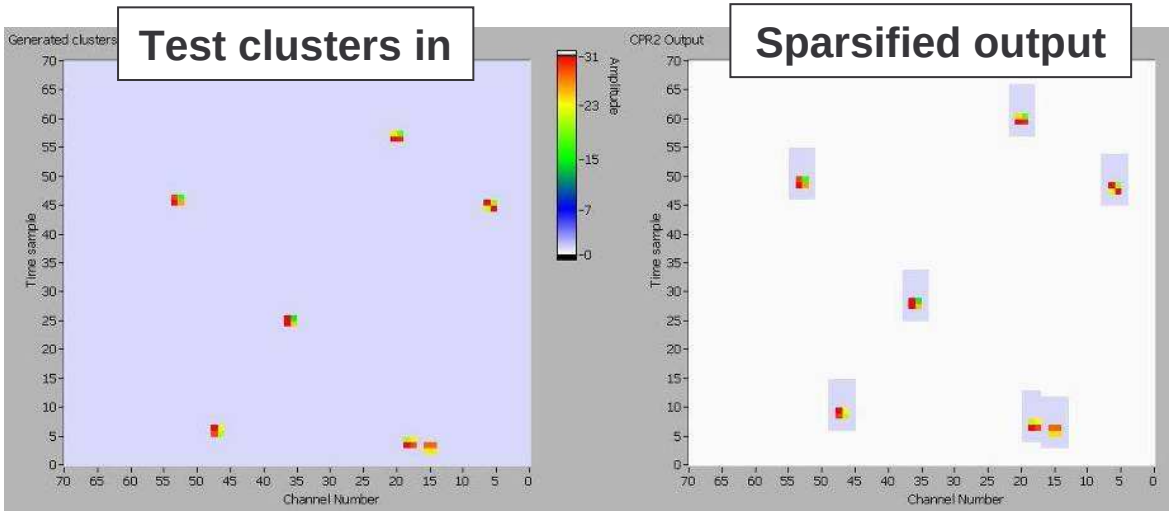
Sparse readout circuitry



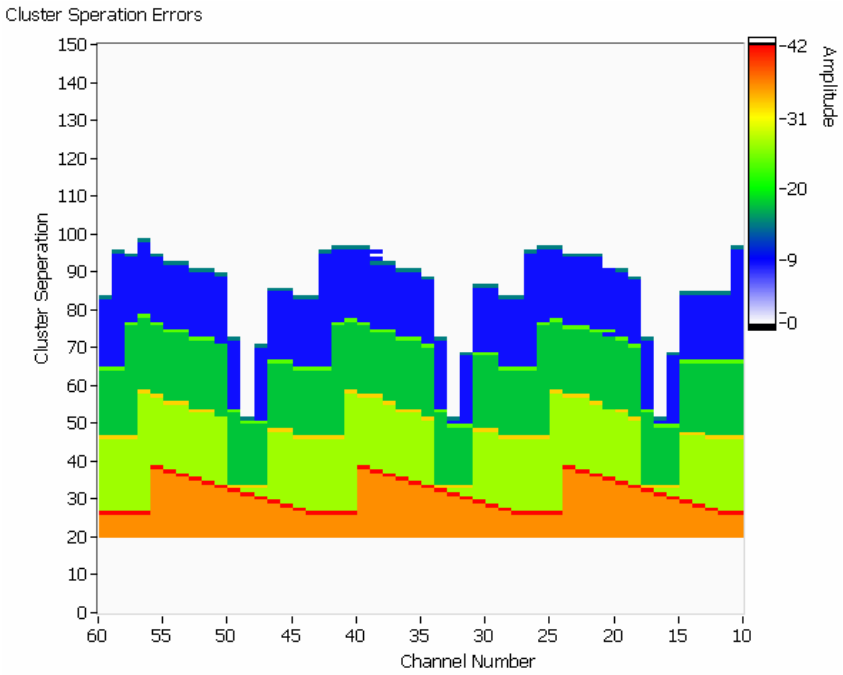
- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Manufactured and delivered February 2005

Steve Thomas/Peter Murray, RAL

CPR2 Test Results



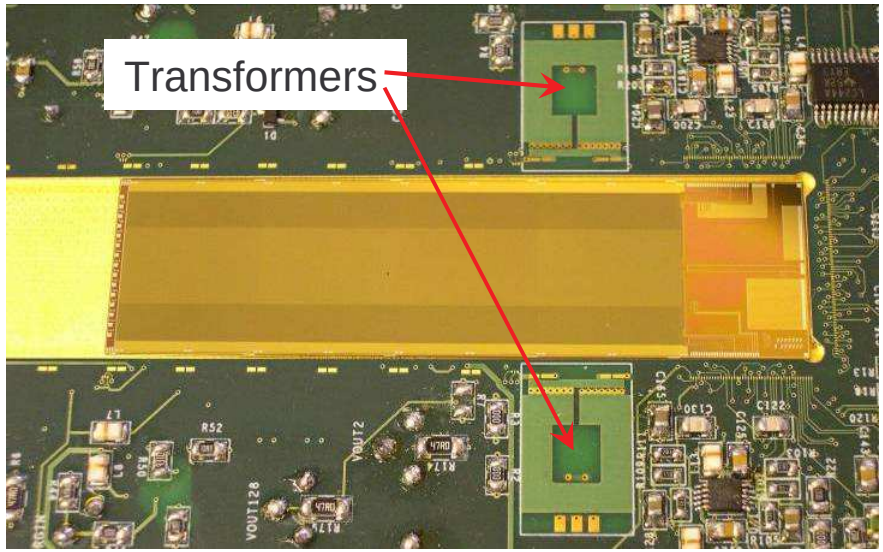
- Parallel cluster finder with 2×2 kernel
- Global threshold
- Upon exceeding the threshold, 4×9 pixels around the cluster are flagged for readout



- Tests on the cluster finder: works!
- Several minor problems, but chip is usable
- Design occupancy is 1%
- Cluster separation studies:
  - Errors as the distance between the clusters decreases – reveal dead time
- Extensive range of improvements to be implemented in the next version (CPR2A)
- CPR2A design well underway

Thanks to Tim Woolliscroft, Liverpool U

Clock Drive for CPC2



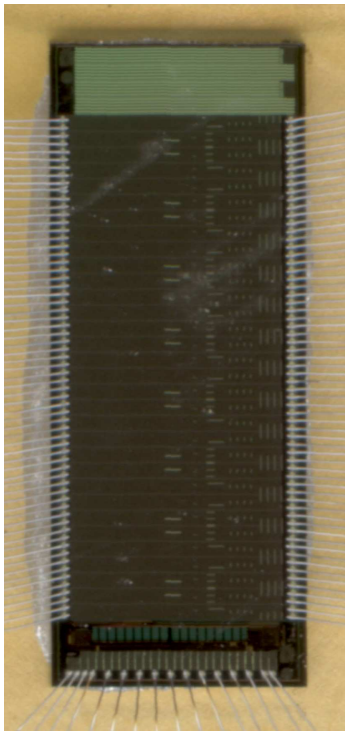
Johan Fopma/Brian Hawes, Oxford U

Transformer driver:

- **Requirements: 2 V_{pk-pk} at 50 MHz over 40 nF (half CPC2-40);**
- **Planar air core transformers on 10-layer PCB, 1 cm square**
- **Parasitic inductance of bond wires is a major effect – fully simulated**

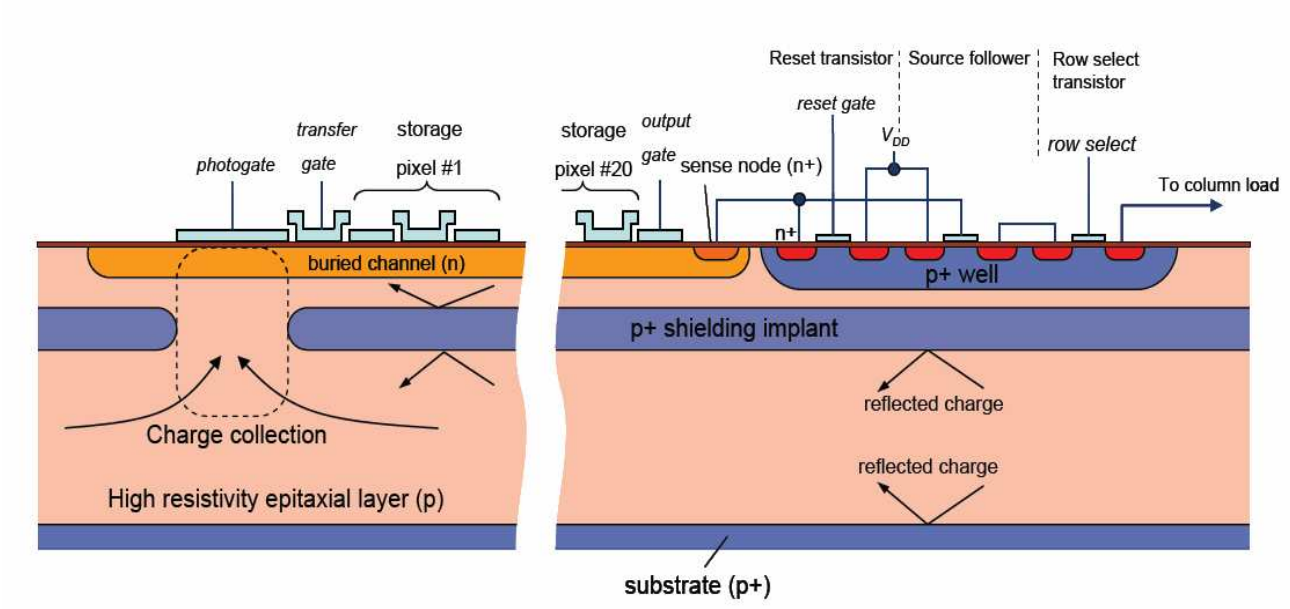
Chip Driver CPD1:

- **Designed to drive the outer layer CCDs (127 nF/phase) at 25 MHz and the L1 CCD (40 nF/phase) at 50 MHz**
- **One chip drives 2 phases, up to 3.3 V clock swing**
- **0.35 μm CMOS process, chip size 3×8 mm^2**
- **CPC2 requires 21 Amps/phase!**
- **First tests are very promising**



Steve Thomas/Peter Murray, RAL

In-situ Storage Image Sensor (ISIS)

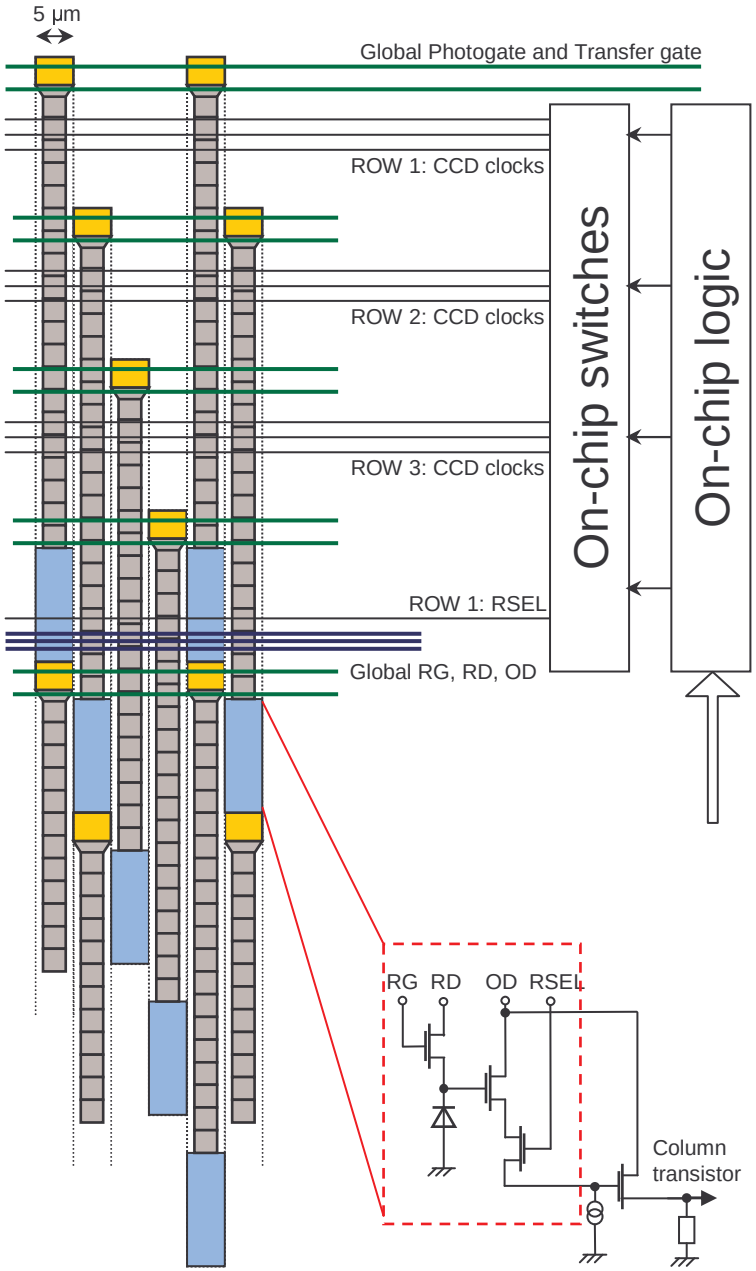


Chris Damerell, RAL

Operating principles of the ISIS:

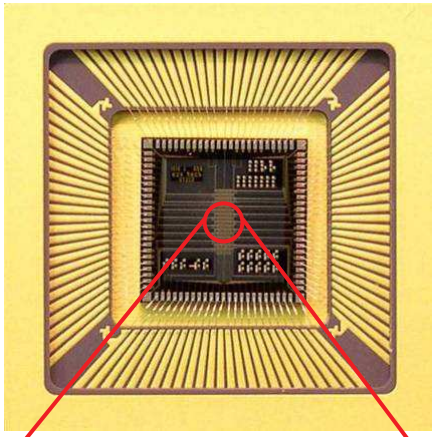
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup);**
4. **1 MHz column-parallel readout is sufficient;**

In-situ Storage Image Sensor (ISIS)

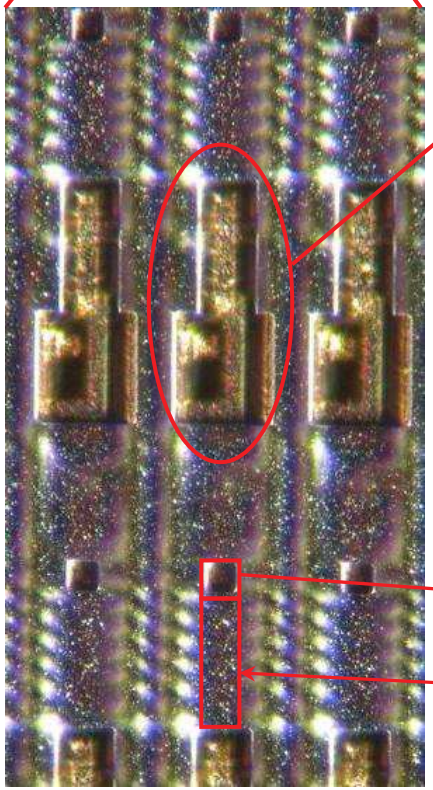


- The ISIS offers significant advantages:
  - **Easy to drive** because of the low clock frequency: 20 kHz during capture, 1 MHz during readout
  - ~100 times more **radiation hard** than CCDs (less charge transfers)
  - **Very robust to beam-induced RF pickup**
- ISIS combines CCDs, active pixel transistors and edge electronics in one device: **specialised process**
- Development and design of ISIS is more ambitious goal than CPCCD
- "Proof of principle" device (ISIS1) designed and manufactured by e2V Technologies

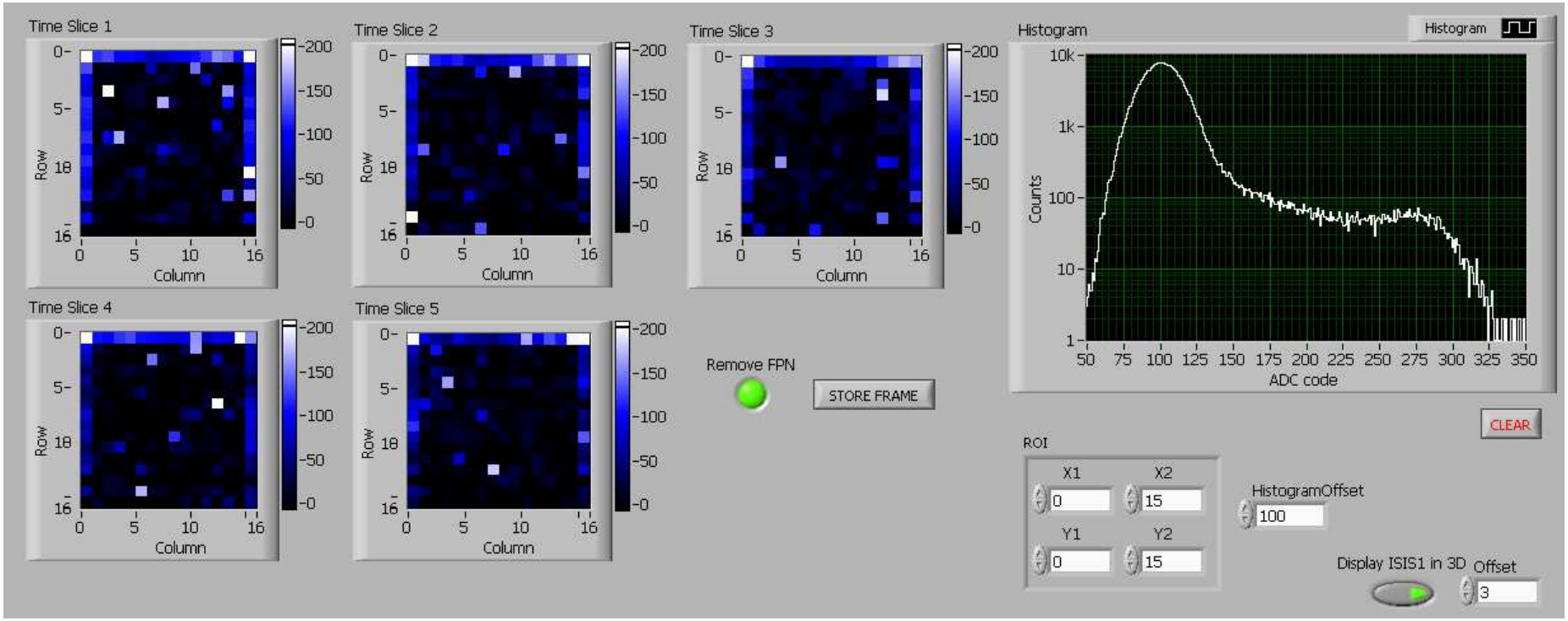
The ISIS1 Cell



- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm



Tests of ISIS1

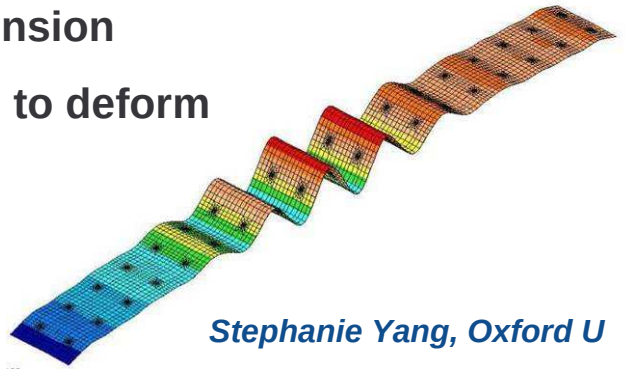


Tests with ^{55}Fe source

- The top row and 2 side columns are not protected and collect diffusing charge
- The bottom row is protected by the output circuitry
- ISIS1 without *p*-well tested first and works OK
- ISIS1 with *p*-well has very large transistor thresholds, permanently off – another set being manufactured now

Mechanical Support Studies

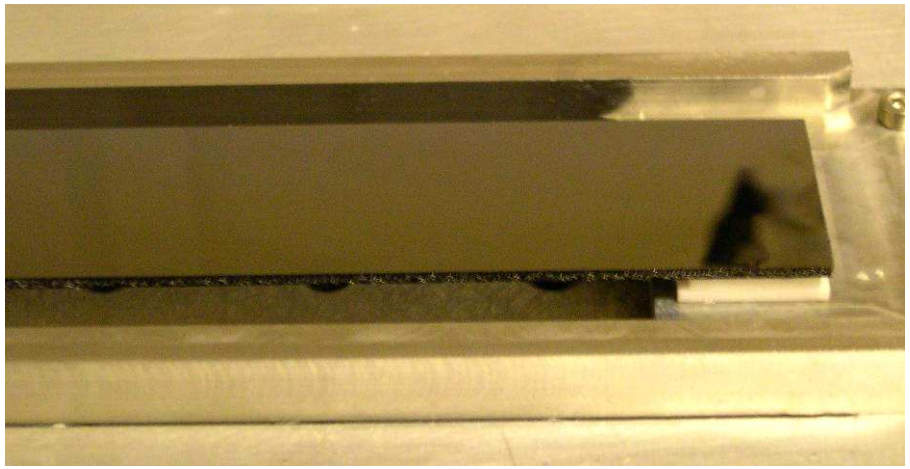
- Goal is 0.1% X_0 per ladder or better, while allowing low temperature operation (~170 K)
- Active detector thickness is only 20 μm
- Unsupported silicon
  - Stretched thin sensor (50 μm), prone to lateral deformation
  - Fragile, practically abandoned
- Silicon on thin substrates
  - Sensor glued to semi-rigid substrate held under tension
  - Thermal mismatch is an issue – causes the silicon to deform
  - Many studies done for Be substrate
- Silicon on rigid substrates
  - Shape maintained by the substrate
  - Materials with good thermal properties available
  - Foams offer low density and mass while maintaining strength



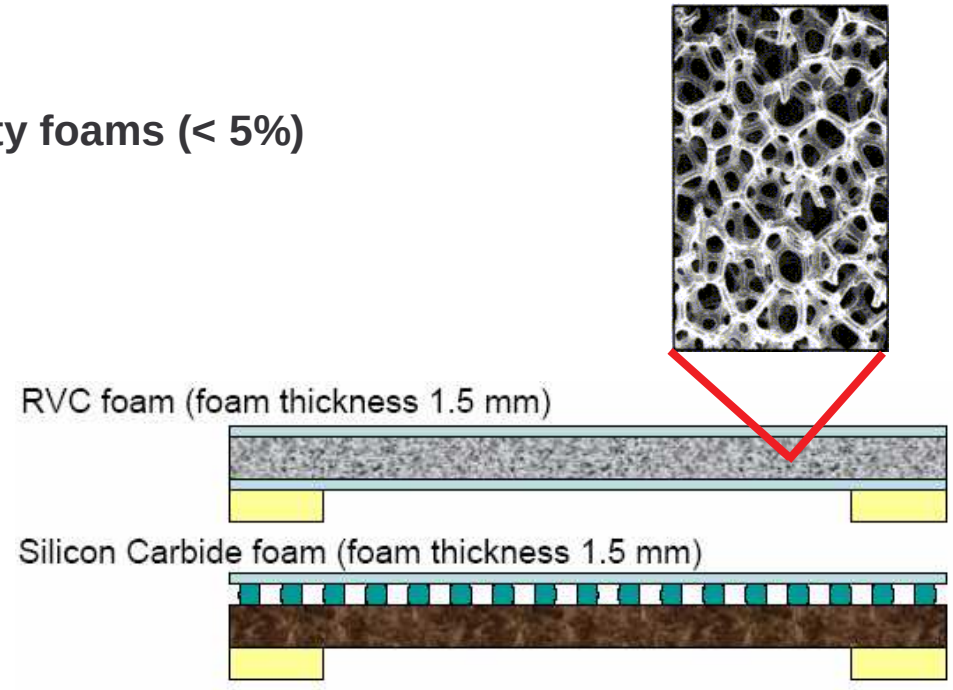
Stephanie Yang, Oxford U

Mechanical Support Studies

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~ 3% density)
  - Foam (1.5mm thick), sandwiched between two 25 μm silicon pieces – required for rigidity
  - Achieves 0.09% X_0
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 μm) on SiC foam (1.5mm);
  - Achieves 0.16% X_0
  - 0.09% X_0 possible with lower density foams (< 5%)



Thanks to Erik Johnson, RAL



Areas of Common Interest for LCFI and CALICE (personal opinion)

- **Detector simulations**
  - **Vertex package – provides important building block for full detector simulation and performance checks against benchmark physics processes**
- **Detector tests**
  - **Laser system at RAL could be used for both MAPS and CCD/ISIS test**
- **Detector design**
  - **Pulsed power – storage supercapacitors considered for LCFI**
- **Beam tests**
  - **Combined beam tests in the future welcome**
  - **Some overlap in the electronics may be possible**
  - **Presently resources for beam tests at LCFI are limited**
  - **Could conduct first beam tests on CPC2 this year if all goes well**

Conclusions

- **Vertex package near release**
  - **Major milestone for LCFI, huge amount of work by a small team**
  - **Will provide important contribution to the MARLIN event reconstruction framework**
  - **Eagerly anticipated worldwide**
- **Detector R&D program progressing well:**
  - **Second generation CPCCD and readout chip being evaluated**
  - **Driver system using CMOS chip and transformers under development**
  - **Third generation CMOS readout chips for CPC1/2 in design stage**
  - **Design of second generation, small pixel ISIS2 underway**
- **Mechanical support aims at ≤ 0.1% X_0 using modern materials**
- **Several areas of collaboration between CALICE and LCFI possible**