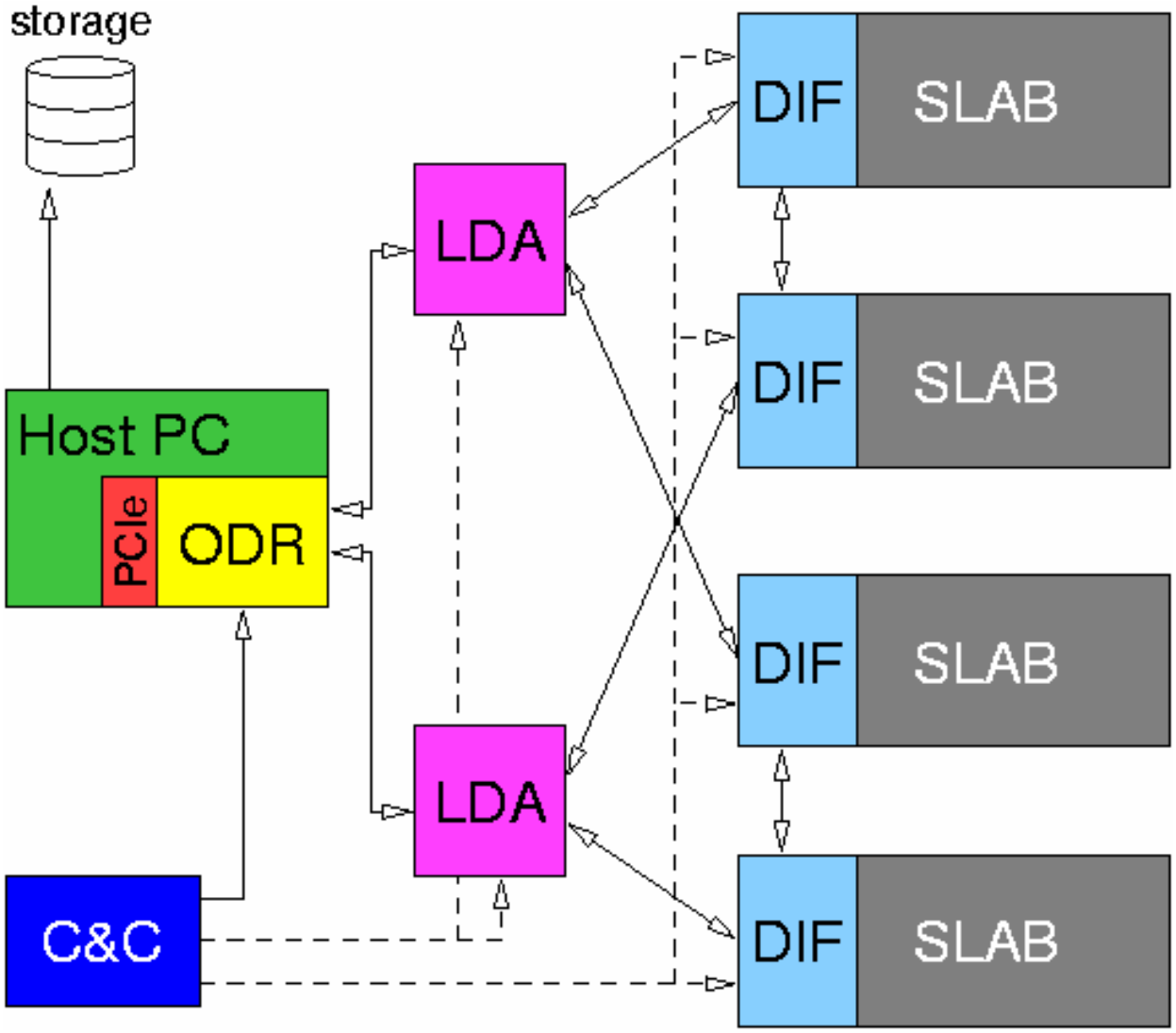
CALICE DAQ Developments

DAQ overview

DIF functionality and implementation

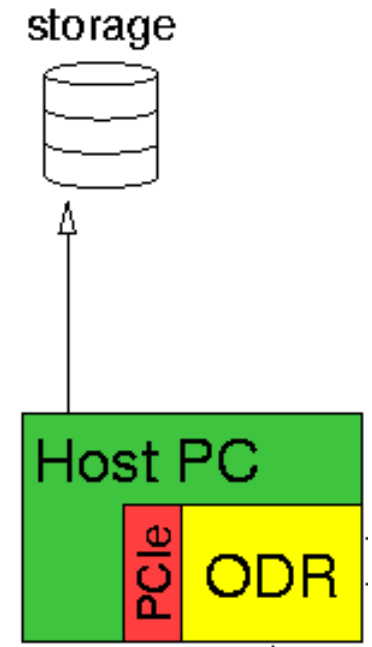
EUDET Prototype development path

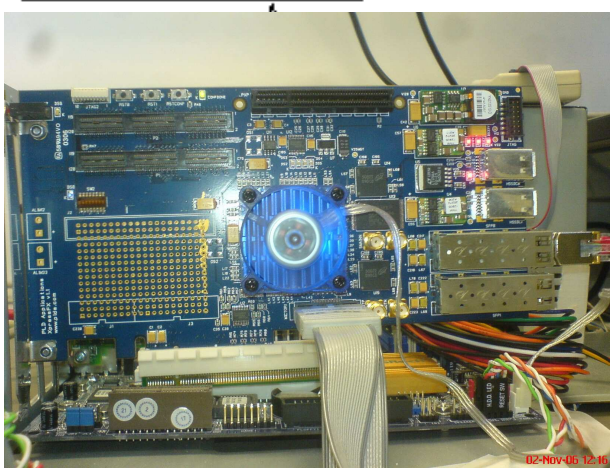
DAQ architecture



- Slab hosts VFE chips
- DIF connected to Slab
- LDA servicing DIFs
- LDAs read out by ODR
- PC hosts ODR, through PCIexpress
- C&C routes clock, controls

ODR and Data Rates





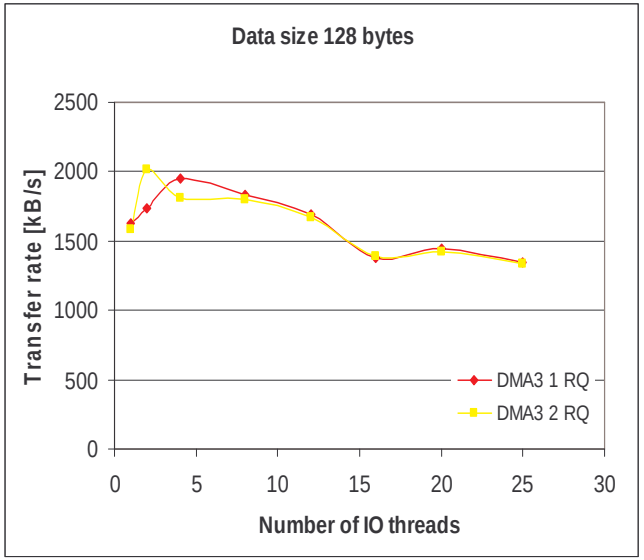
- ODR is a commercial FPGA board with PCIe interface

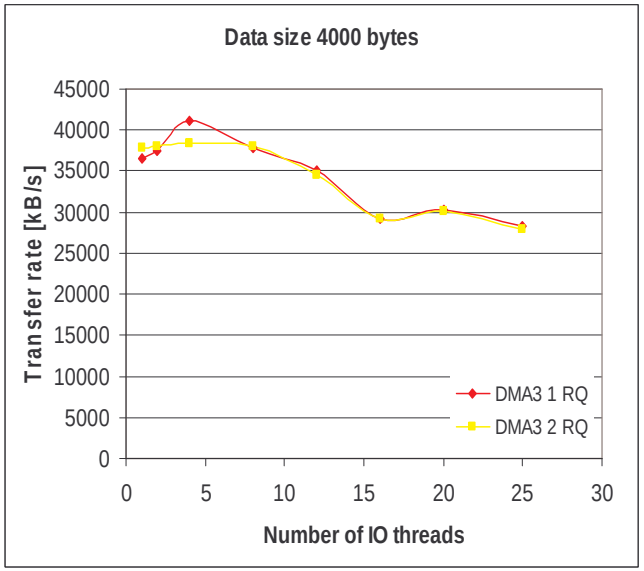
  (Virtex4-FX100, PCIe 8x, etc.)

- Customised firm- and software:

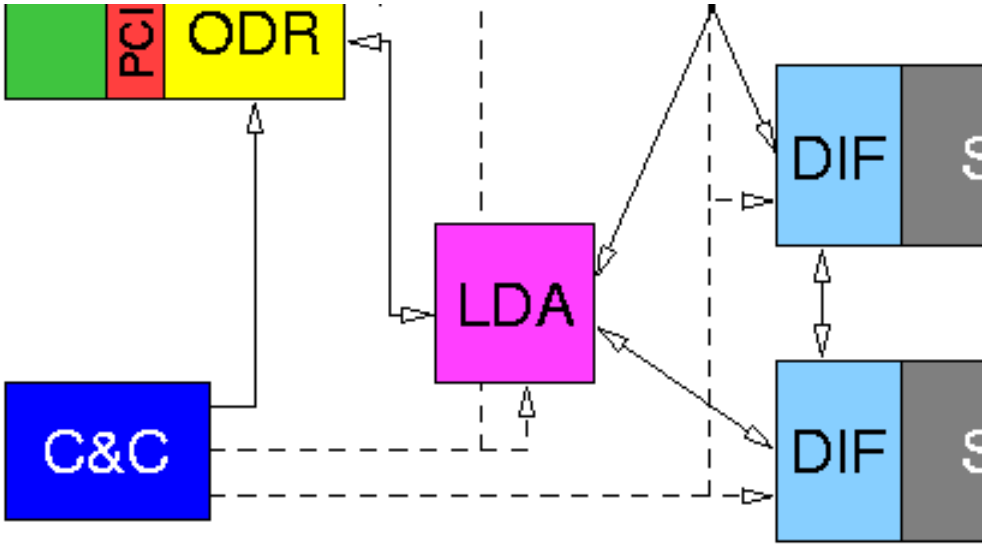
  DMA driver pulls data off the onboard RAM, writes to disk

- Performance studies & optimisation





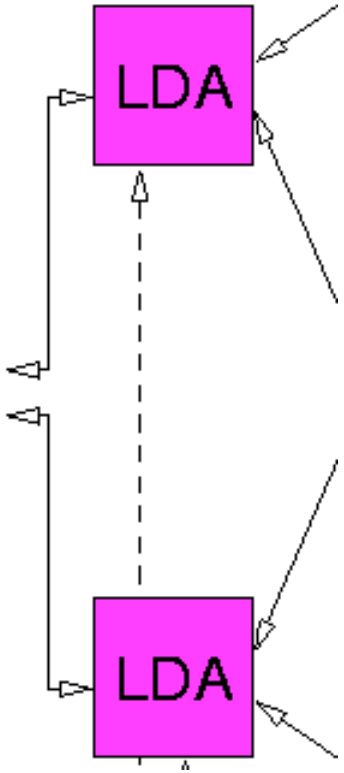
Clock & Controls Distribution

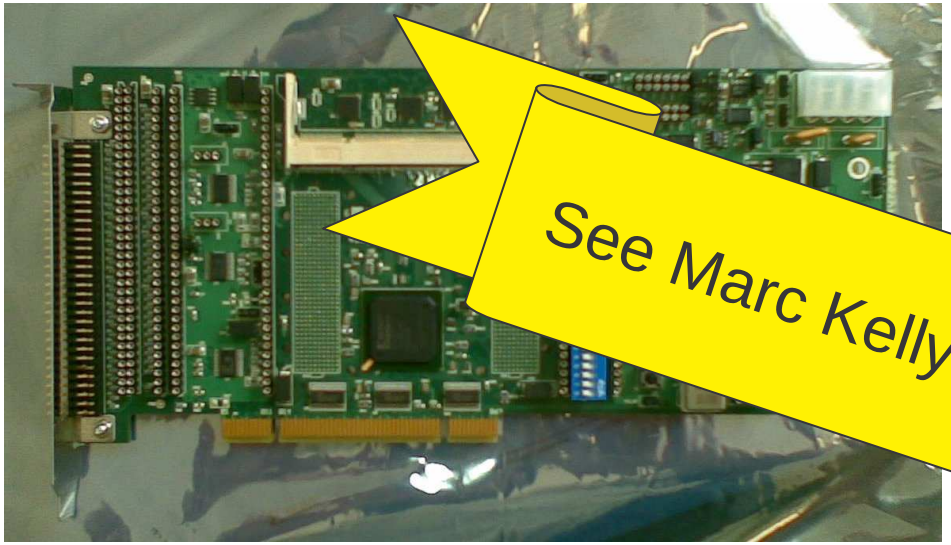


- C&C unit provides machine clock and fast signals to ODR, LDA (and DIF?)
- Clock jitter requirement seems not outrageous
  (at the moment)

- Fast Controls: encoded commands on the LDA-DIF link
- Slow Controls/Configuration: transfers on LDA-DIF link
- Low-latency fast signals: distributed ‘directly’ (if necessary)

LDA and link to ODR



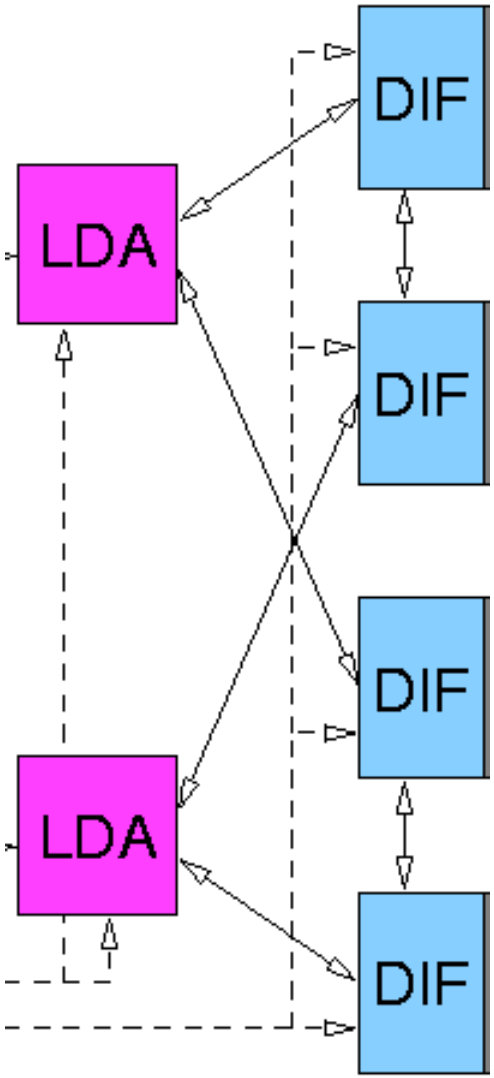


See Marc Kelly's talk

1st Prototype is again a commercial FPGA board with customised firmware and hardware add-ons:

- High-bandwidth link to ODR
- Many links towards DIFs

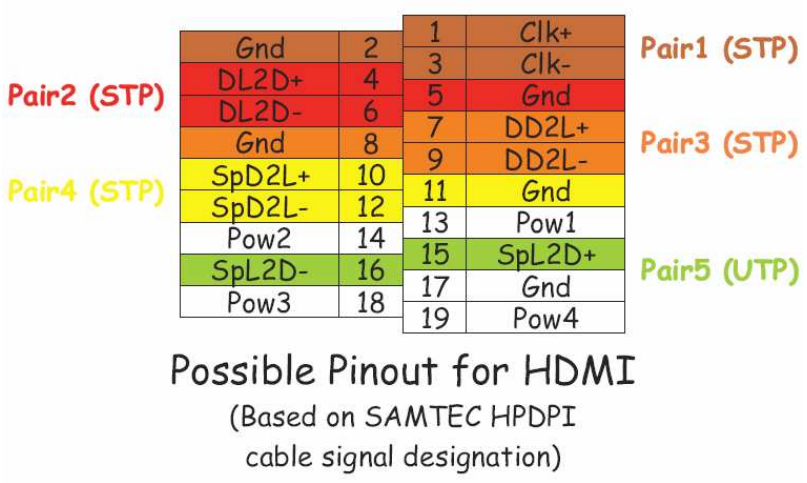
LDA-DIF link



LDA-DIF link:

- Serial link running at multiple of machine clock
- 50Mbps (raw) bandwidth minimum
- robust encoding (8B/10B or alike)
- anticipating 8…16 DIFs on an LDA, bandwidth permitting
- LDAs serve even/odd DIFs for redundancy

LDA-DIF physical interface



clock

data

control

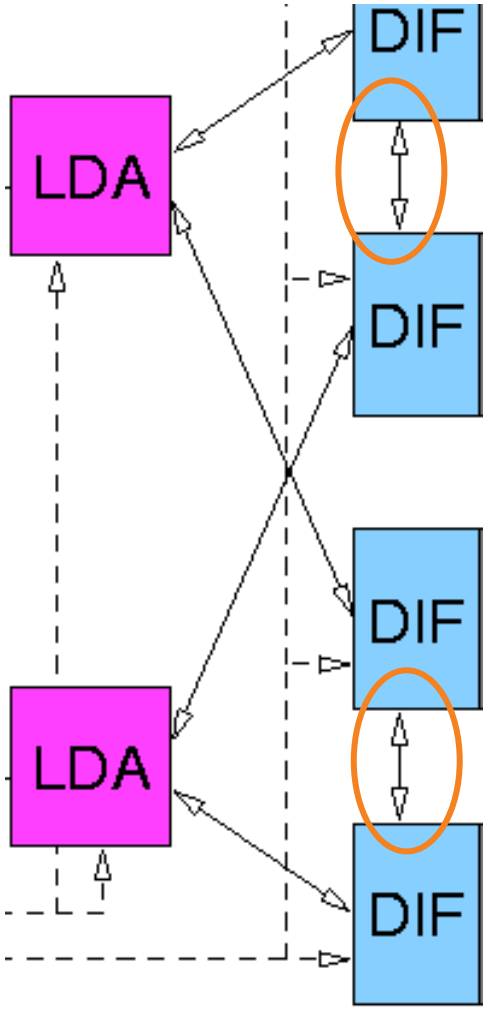
spare data

spare control

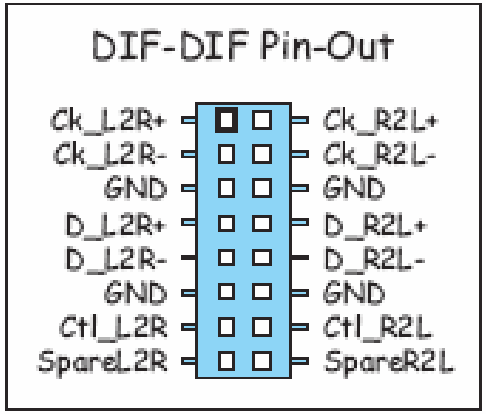
LDA-DIF link physical form factor:

- Differential signals on shielded twisted pairs
- Few single-ended control lines
- HDMI connectors and cabling: commercially available in high quality

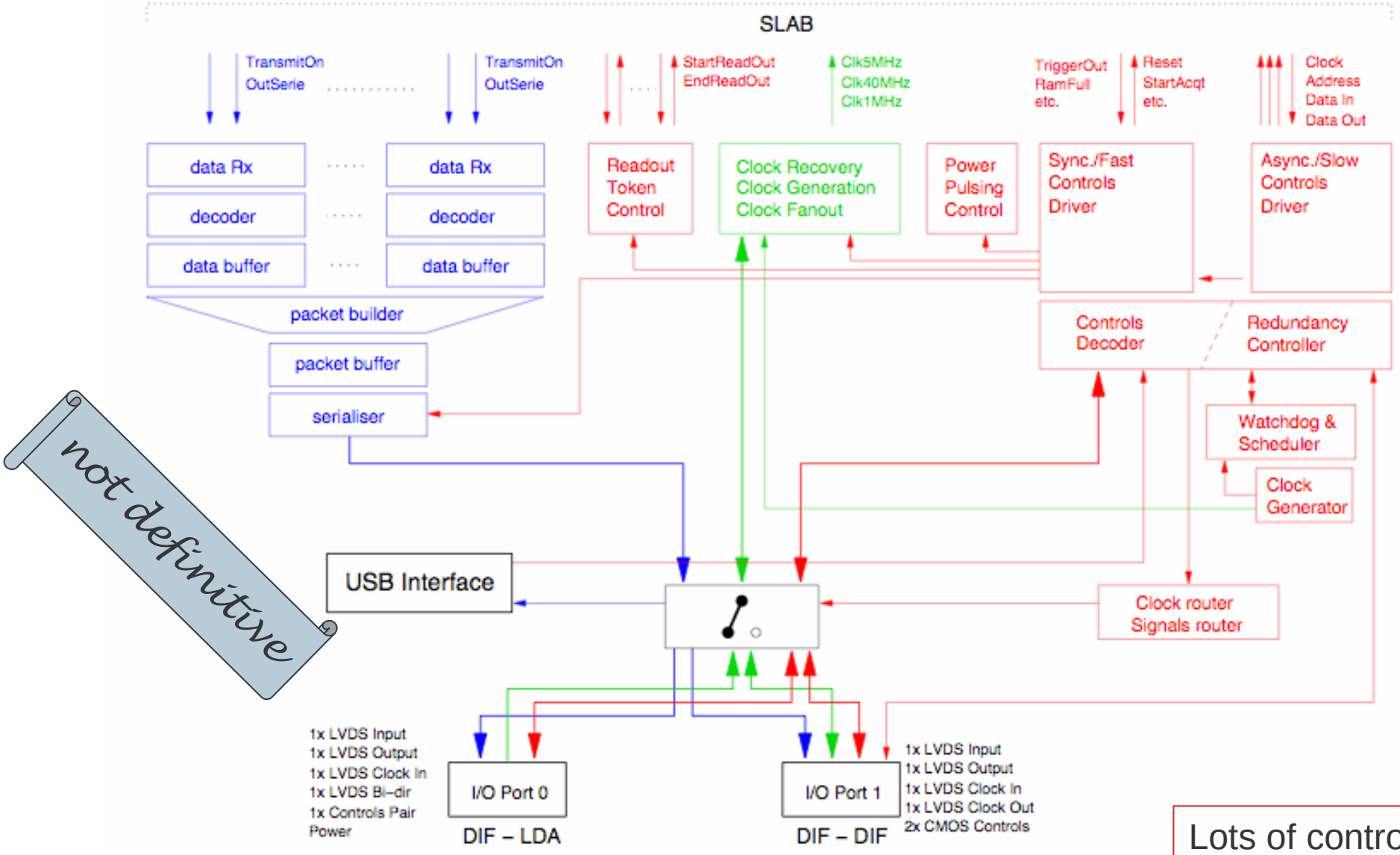
DIF-DIF link



- Redundancy against loss of LDA link
- Provides differential signals:
  - Clock in both directions
  - Data and Control connections
  - Two spares: one each direction
- Plus two single-ended control lines
- Single LDA-DIF link bandwidth sufficiently large for data of two DIFs



Draft DIF block diagram



Lots of controls….

DIF Functionality

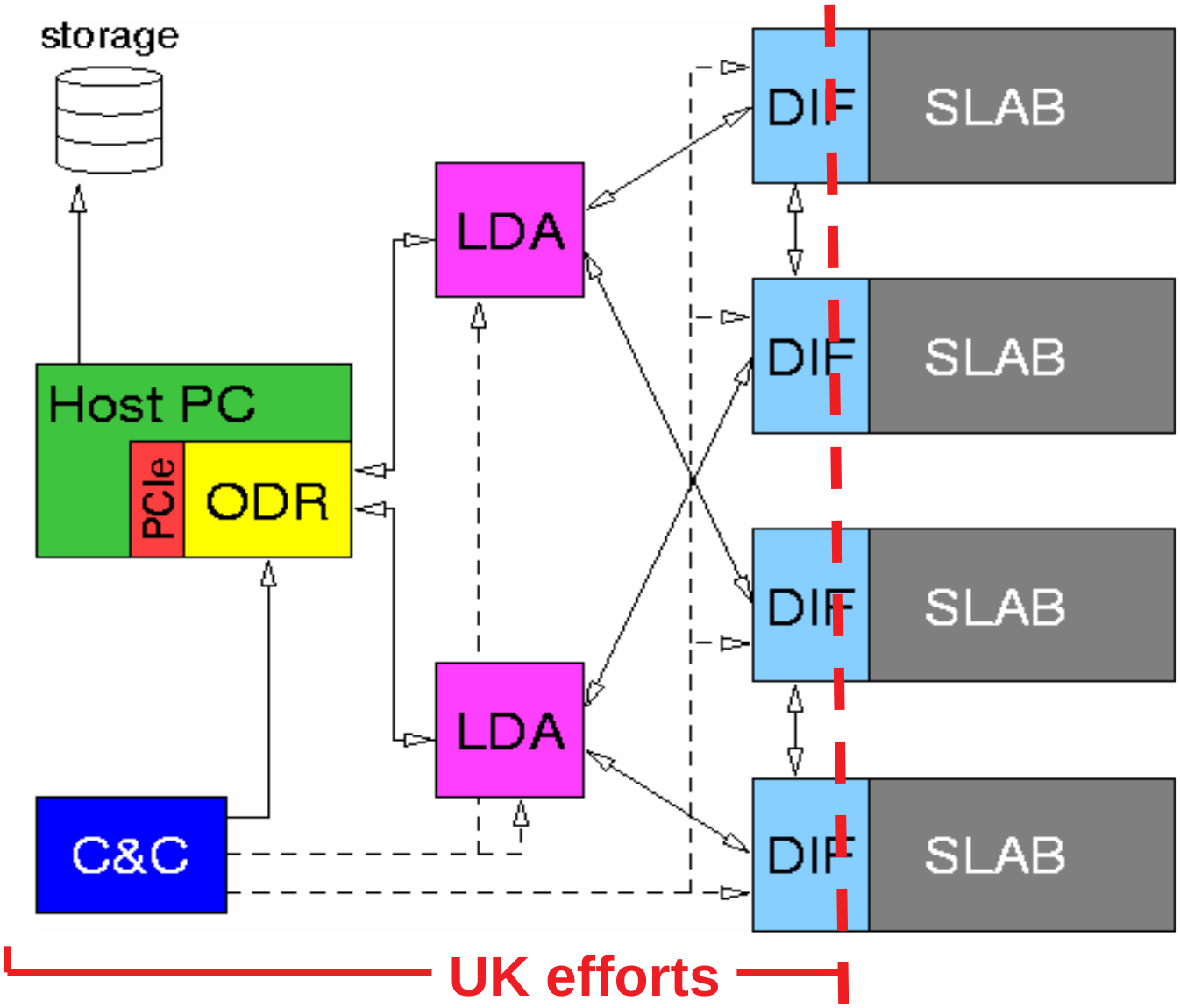
- Receive, regenerate and distribute clocks
- Receive, buffer, package and send data from VFE to LDA
- Receive and decode incoming commands and issue corresponding signals
- Control the DIF-DIF redundancy connection
- Receive, decode and distribute slow control commands
- Control power pulsing and provide watchdog functionality
- Provide an USB interface for stand-alone running and debugging
- …..on top of that: all the things we did not think of so far

DIF implementation

- The Slab is an integral part of the detector
- The LDA and ODR are transparent wrt detector type

- The DIF and its interface to the slab is detector-specific
- Large parts of the DIF firmware can/*should*/***must*** be generalised
- *DIF hardware should support firmware* to profit from common developments
- DIF working group to address common problems and share knowledge, experience, and VHDL code
- DIF wg: representatives of detectors + UK-DAQ person

Opportunity to memorise the acronyms:



DIF: Detector InterFace

LDA: Link/Data Aggregator

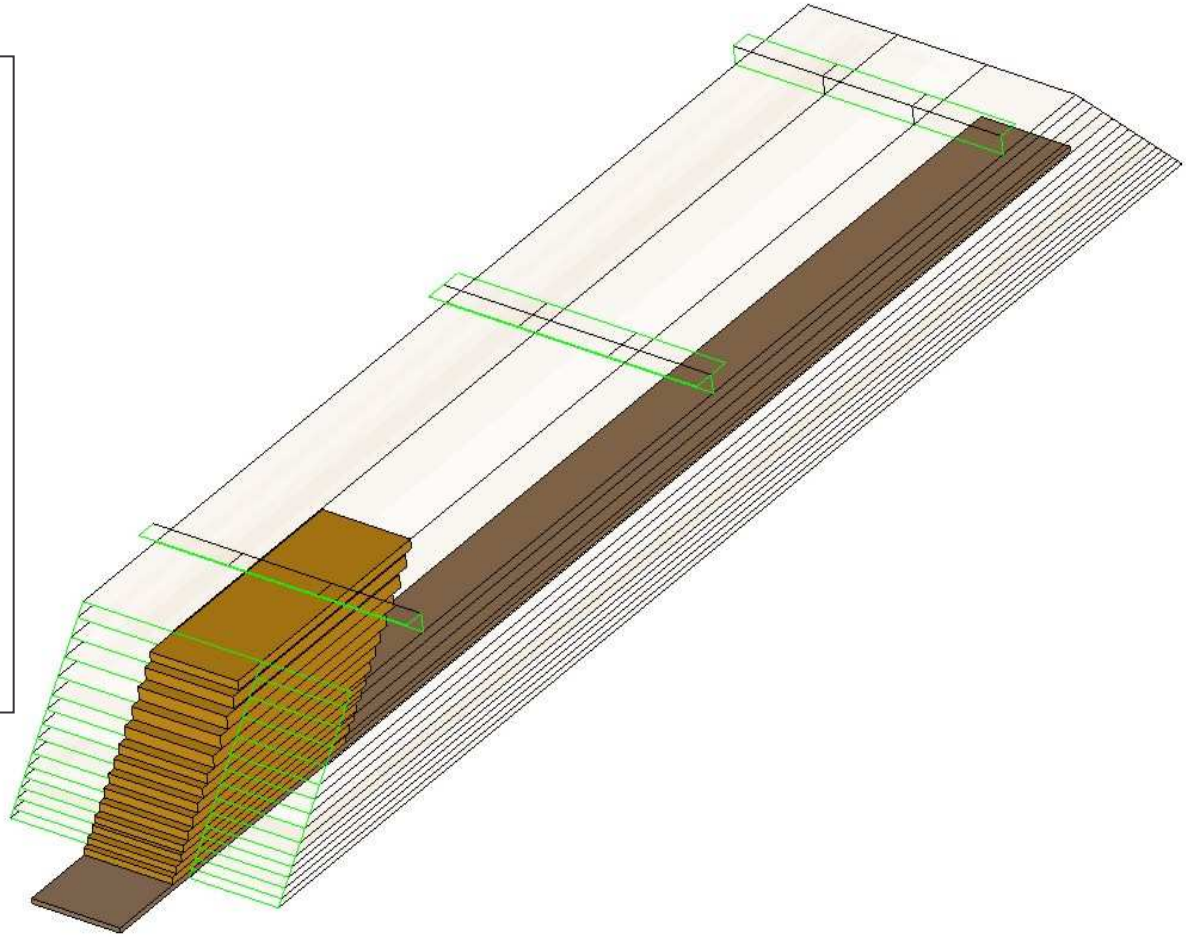
ODR: Off-Detector Receiver

C&C: Clock & Controls

PCIe: PCI-Express

The EUDET prototype

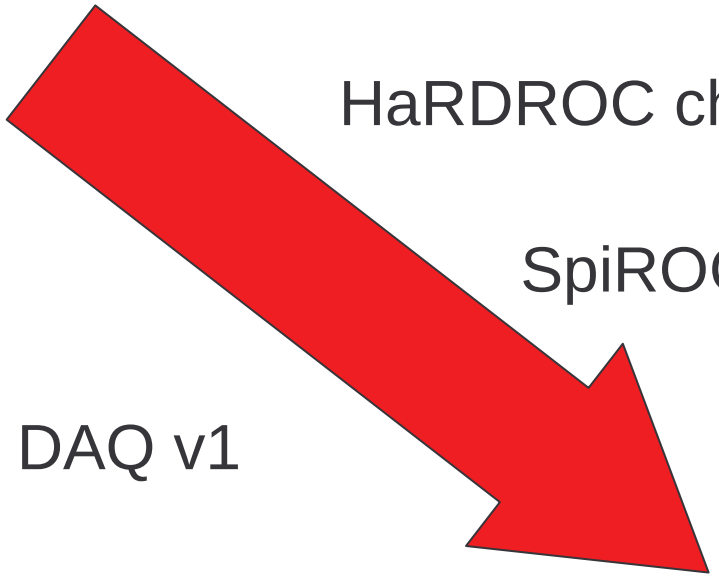
- Full stack: 15 slabs, instrumented on both sides
- As close to CALICE technology as reasonably possible



Prototype development

NOW 2008 2009

HaRDROC chip v1
Testbeam DAQ



HaRDROC chip v2

SpiROC/SkiROC chip v1

New DAQ v1

EUDET proto:
detector + DAQ

Technology prototype for physics results

EUDET module is quite a large and complex object.
Keep future mass production in mind:

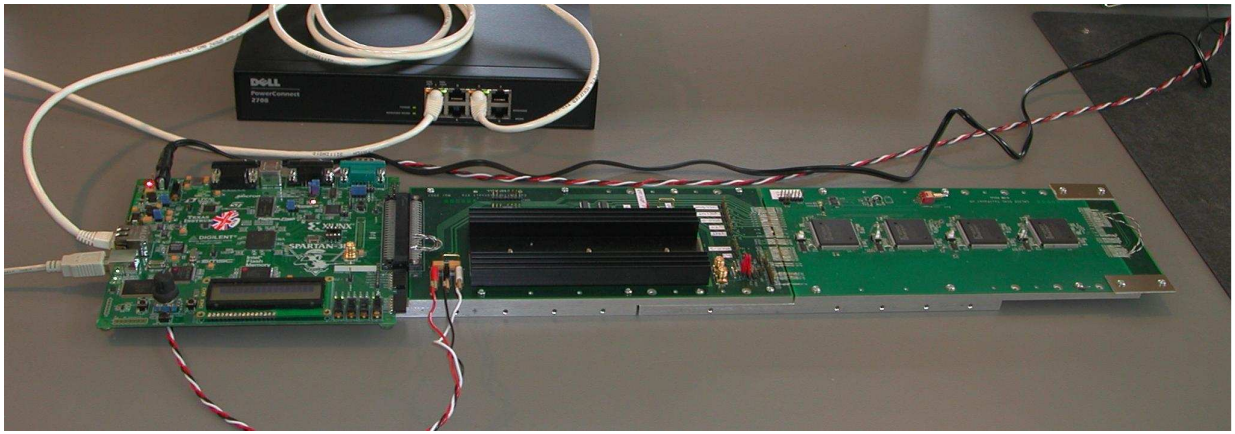
- large objects are assemblies of smaller objects
- develop testable objects

Many technology options require even more R&D:

- power consumption
- data rate: speed vs. power
- noise
- etc.

R&D for the EUDET prototype

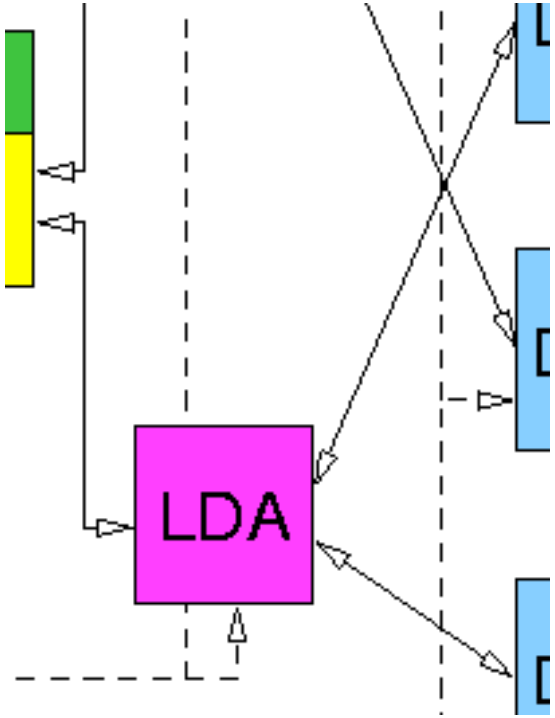
- Proto-slab:
  - FPGA for VFEs
  - provisional ‘DIF’ for ECAL



- Tests of signal distribution along long PCB lines: signal deterioration, termination options, speed, etc.
- Identification of possible issues with many (pseudo)VFE chips on long transmission paths
- Familiarise ourselves with VFE readout architecture

R&D for the EUDET prototype

More to come…..



…but let's look at the LDA design first