LDA and DIF Link

Marc Kelly
Just one of the many people involved in the LDA design.

University of Manchester

Basic LDA

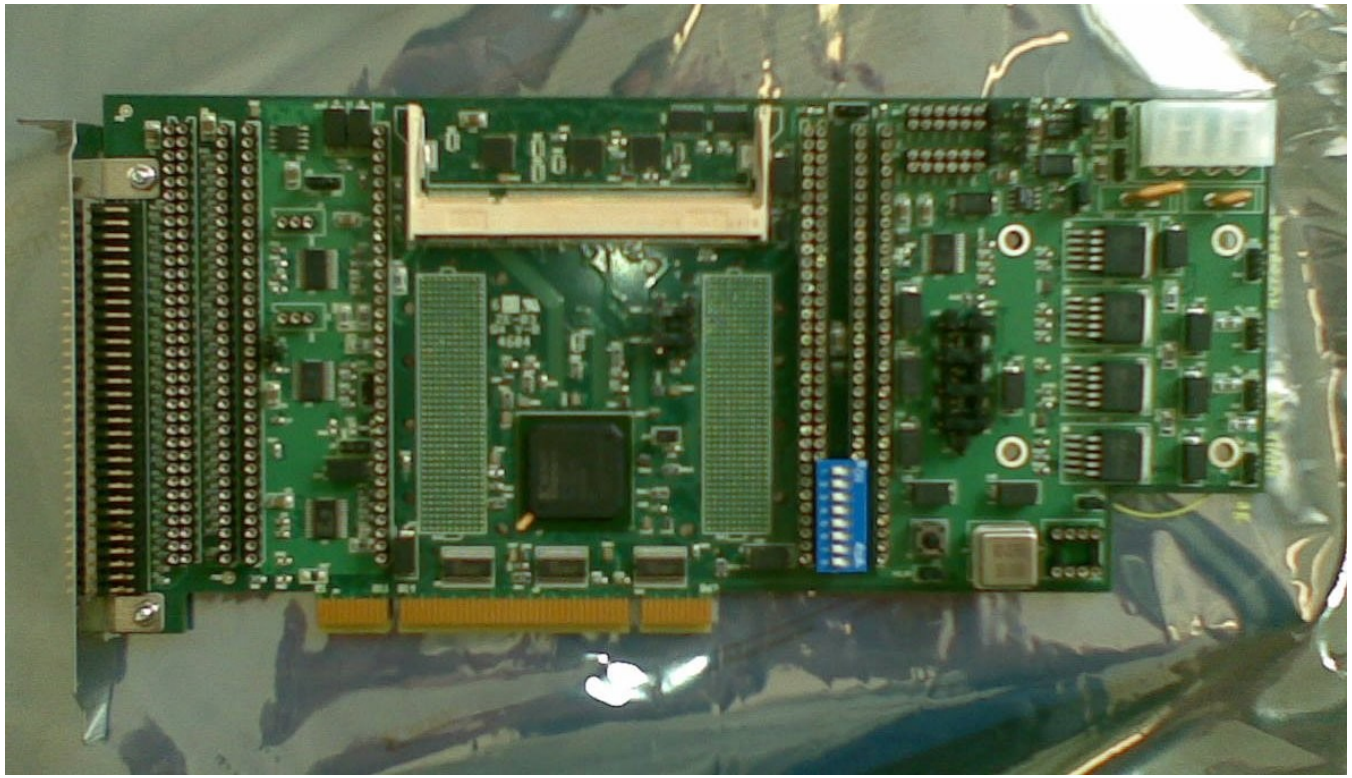
- Main Requirements
  - Needs to talk to N DIF's.
  - Needs to talk to 1 down stream ODR (and/or Ethernet switch)
  - Needs to be able to buffer event data ready for readout.
  - Be generic enough to handle any situation we can throw at it, within reason.

Basic LDA

- Secondary Requirements
  - DIF link must be small, ideally a single cable/fibre.
  - As many DIFs as possible per LDA, within reasonably power/design limits.
  - ODR link should be generic, commercially available and well understood.
  - Data rates possible should be scalable.
  - Prototype Link design should related closely to final system, to allow the DIFs to be used with later LDA designs.

Prototype LDA Design

Based on a commercial Spartan 3 FPGA development board. S3-2000 FPGA installed.



Board has SO-DIMM socket, allowing us to install ram for event buffering.

Lots of IO available, allowing us to design additional boards for the DIF-LDA and LDA-ODR links.

Prototype LDA Design

- LDA-DIF link.
  - Will use HDMI based system.
  - These (Type-A) are high data rate digital cables used in HDTV. Consists of 4 sets of twisted pairs, plus some control lines, in a nice easy to use format.
  - Available in long lengths, and are known to be available in Halogen free varieties.
  - Designed to handle data rates of ~350 Mbits/sec per pair in HDMI 1.3 Spec.

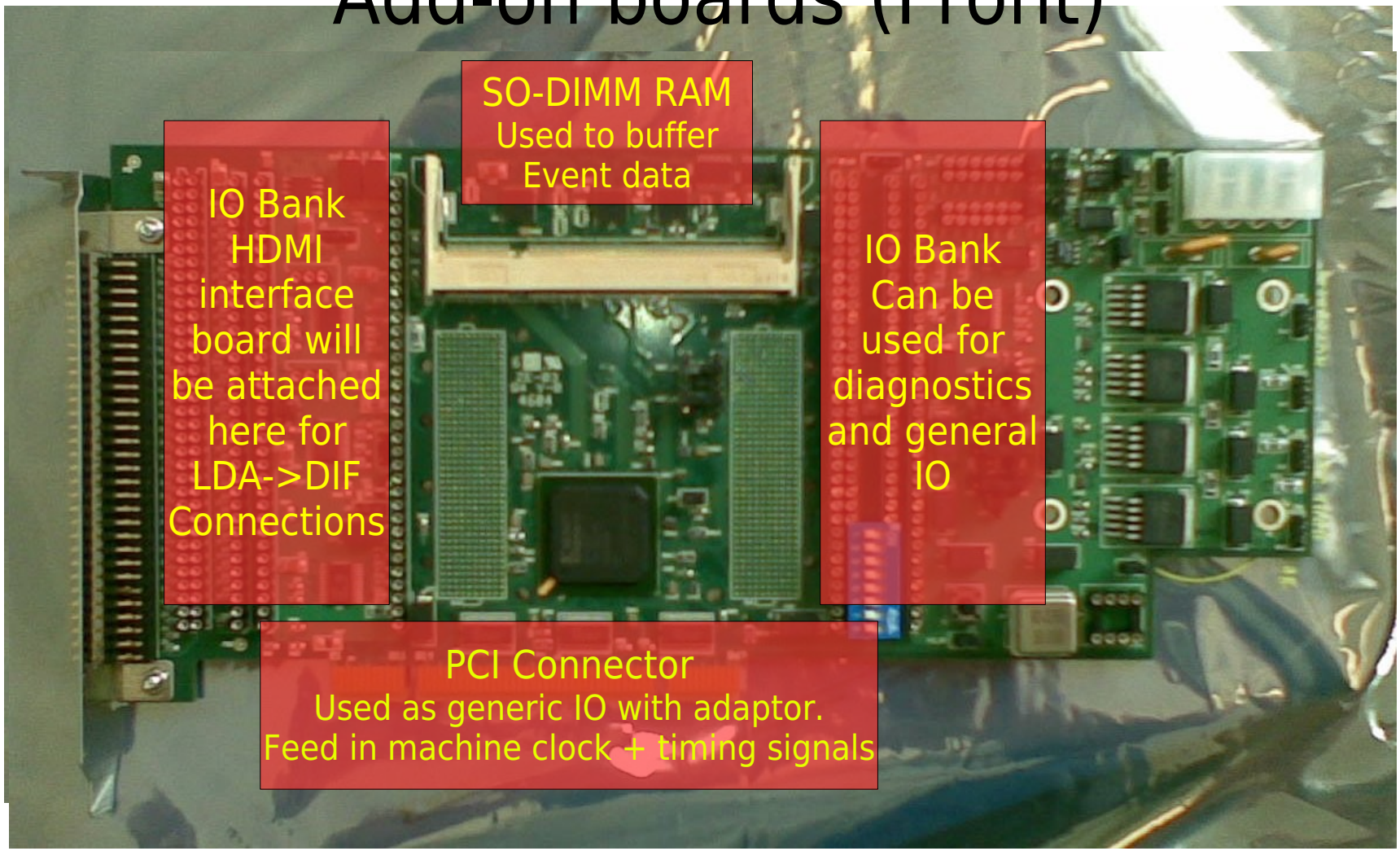
LDA-DIF Link details

- 1 TX pair for machine clock.
- 1 TX pair for LDA -> DIF data.
- 1 RX pair for DIF <- LDA data.
- 1 TX pair for Control channel.
- 1 RX pair for slow monitoring/misc side band data. (This pair is NOT designated a high bandwidth pair in the HDMI spec. SAMTEC cables have it as a UTP however.)
- TX and RX data is expected to be Encoded with 8B/10B or similar balancing scheme.
- The data will NOT, in current prototype undergo clock recovery, the data will be synchronous to a multiple of the TX machine clock.

LDA-DIF Link details

- LDA design will have 10 HDMI connections on it, giving fairly good connectivity. To run larger detectors, requiring more DIFs then more then 1 LDA will have to be used.
- These LDAs could be synchronised via the IO available on them. The PCI connector on the base is seen as a quick and simple way to do this in a rapid prototyping situation, although other mechanisms using the TLK2501 or GigEthernet link are being investigated.

Add-on boards (Front)



Prototype LDA Design

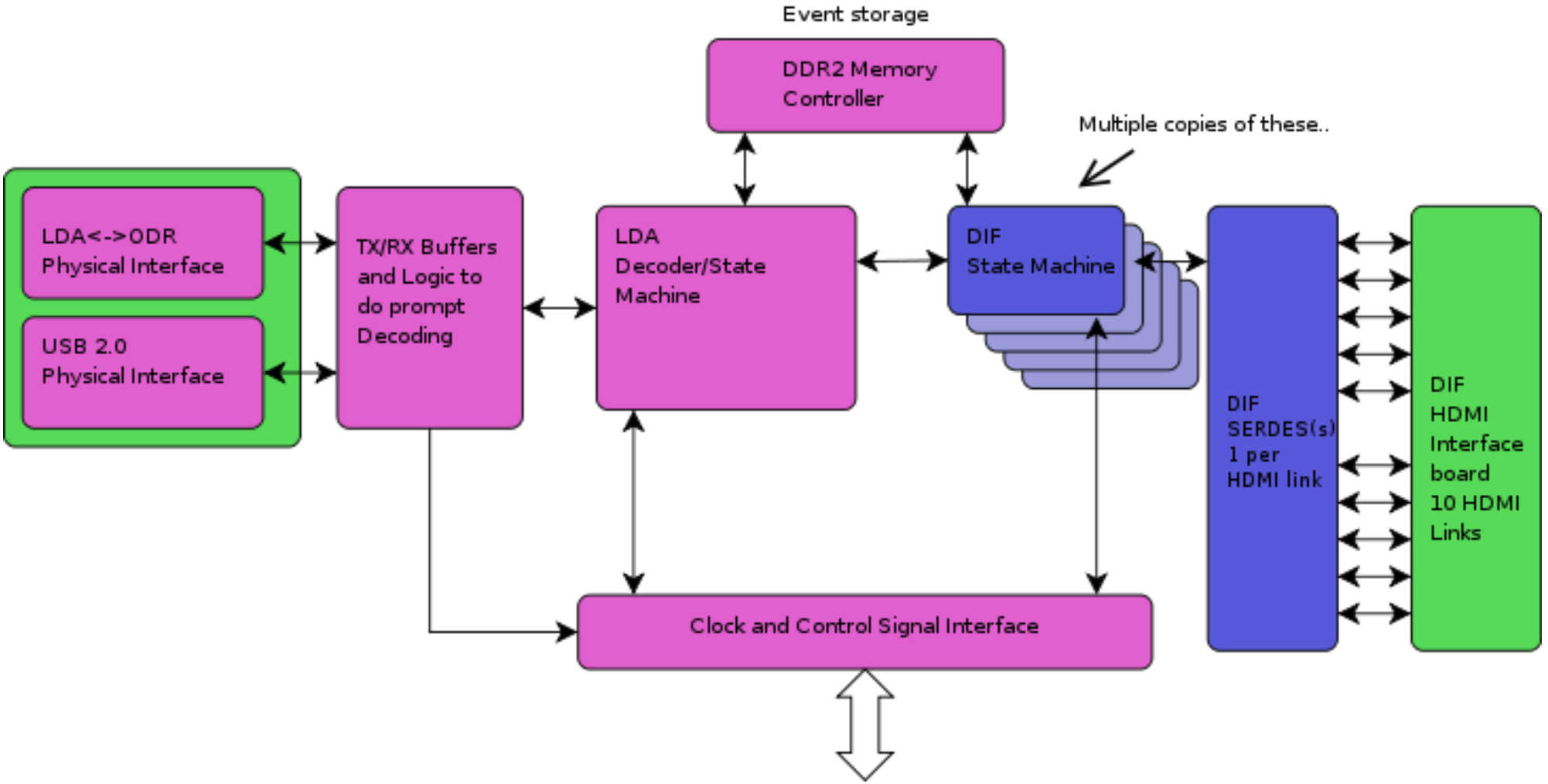
- LDA-ODR link has two current options.
  - Gigabit Ethernet. This has been tested and demonstrated to be easy to achieve with FPGAs. It is cheap, and can be fed into a switch to aggregate multiple LDAs output into a single ODR. However has issues for clock and control uplink from ODR, due to variable latency etc.
  - TLK 2501 chipset. Used in a lot of CERN equipment, is a generic 16:1 SERDES chipset that uses 8B10B encoded data streams to work at 1.25 -> 2.5 Gbit/sec.
  - Has better, more controllable latency, and could be used to distribute clock and control to LDA from ODR.

Add-on boards (Back)

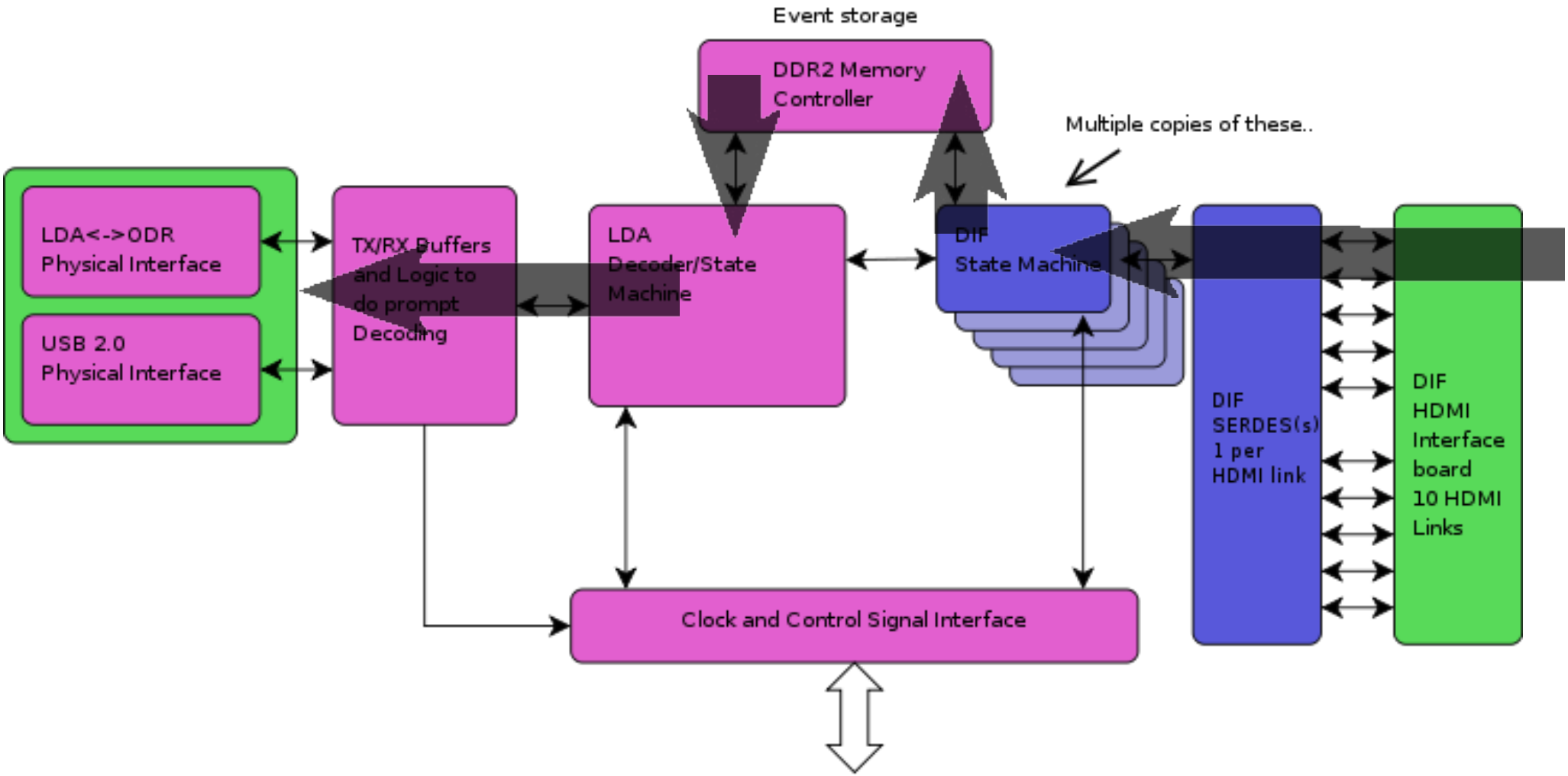
Prototype LDA Design

- USB interface
  - Intend to provide some kind of USB interface that allows testing and debugging of the LDA+DIF without the use of an ODR.
  - The plan is to duplicate the functionality of the ODR link as much as possible from the software's point of view.
  - The chipset will be one of the semi-generic all-in-one solutions on the market. Cypress FX2 etc.

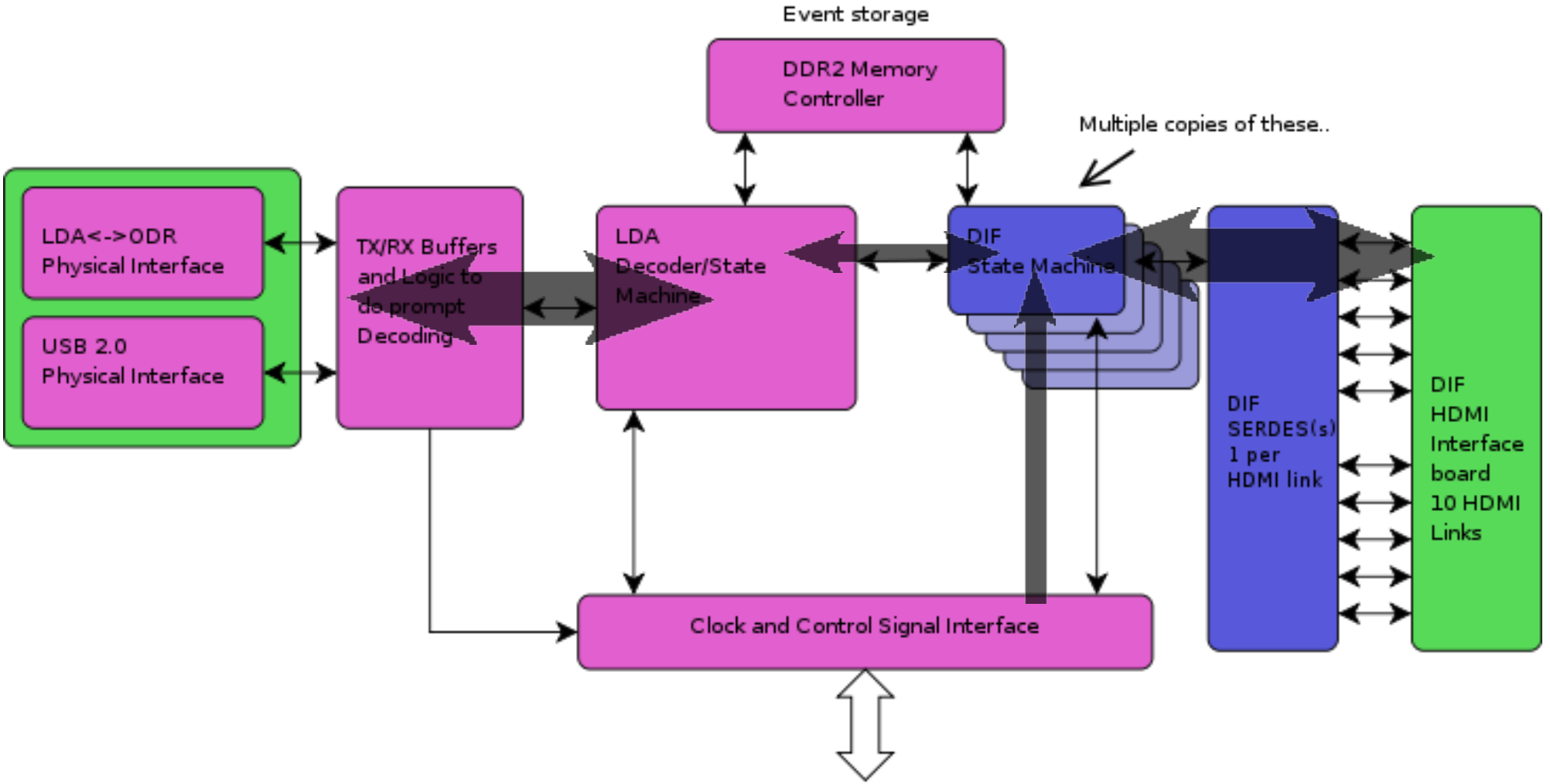
Rough first pass at some form of diagram



Data Path for Event Readout



Control and Configuration Path



Thoughts

- What goes in the boxes? A fair bet it will be a lot of state machines, FIFOs and all the usual DAQ things.
- Things like the SERDESs, FIFOs and Memory controllers are all “easy”.
- State machines are harder, and require some detailed though about the LDA usage.
- The LDA **does not** have to understand the data passing to the DIF, it just has to provide a generic method to address and pass data to/from the DIF(s).
- LDA **does** have to understand the concept of an “Event” and buffer blocks into memory ready for the ODR to request it. Event data format is reasonably generic, as far as LDA is concerned it is a header with a block of data.