LDA Development

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LDA Design

- Main Requirements
  - Needs to talk to ~8-10 DIF's.
  - A downstream link to an ODR. With ~ 1GBit bandwidth.
  - Needs to be able to buffer event data ready for readout.
  - Be generic enough to handle any situation we can throw at it, within reason.
  - Has to be flexible to test ideas and do further development work.

Current Design

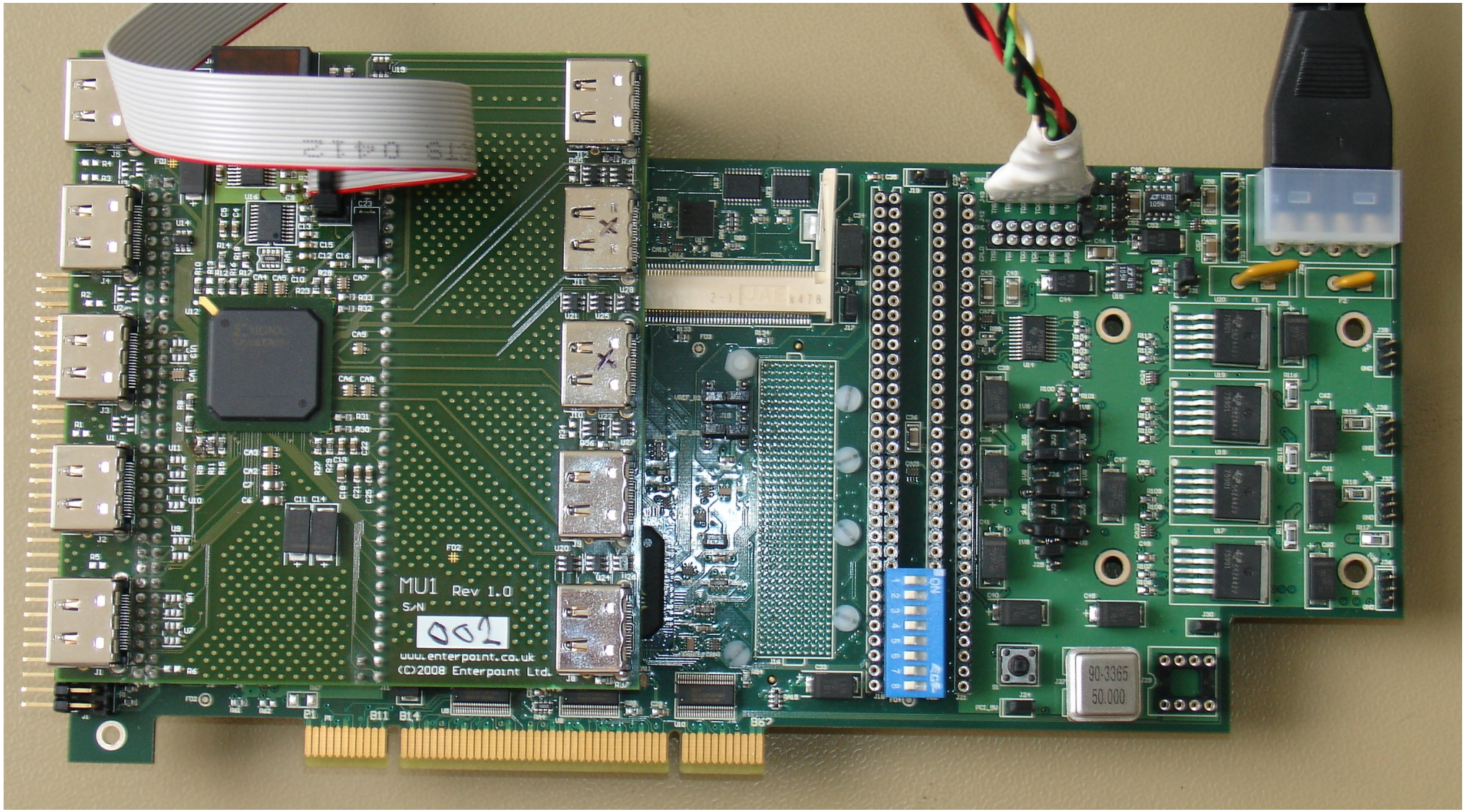
- Based on a commercial FPGA development board. Broaddown2 from Enterpoint UK
- Enterpoint were asked to make adaptor boards for the LDA-ODR and LDA-DIF links.
- Main FPGA is a Spartan3-2000.
- DIF links are HDMI cables, mainly due to availability,bandwidth and flexibility.
- ODR link is either Ethernet or a proprietary (TLK 2501) similar to the CERN SLink.
- Both links are there to test various design ideas.
- USB as a test bench interface for stand alone working.

Experience so far

Using an external design company has had some issues:

- They were not totally open about the amount of available IO on the board. In my opinion they said “yes we can do it.” without really knowing if it was possible.
- They obviously were looking to design something they could reuse.
- Was hard to keep an eye on what they were designing.
- Some hidden costs have surfaced. The Ethernet board's connection to the BD2 is a Samtec GZF connector, and the cost is **NOT** included in the design. 2 Connectors are needed per board. That comes to ~50 UKP for the pair. We have “acquired” a pair for the first prototype at no cost.

HDMI Interface Board



HDMI Board

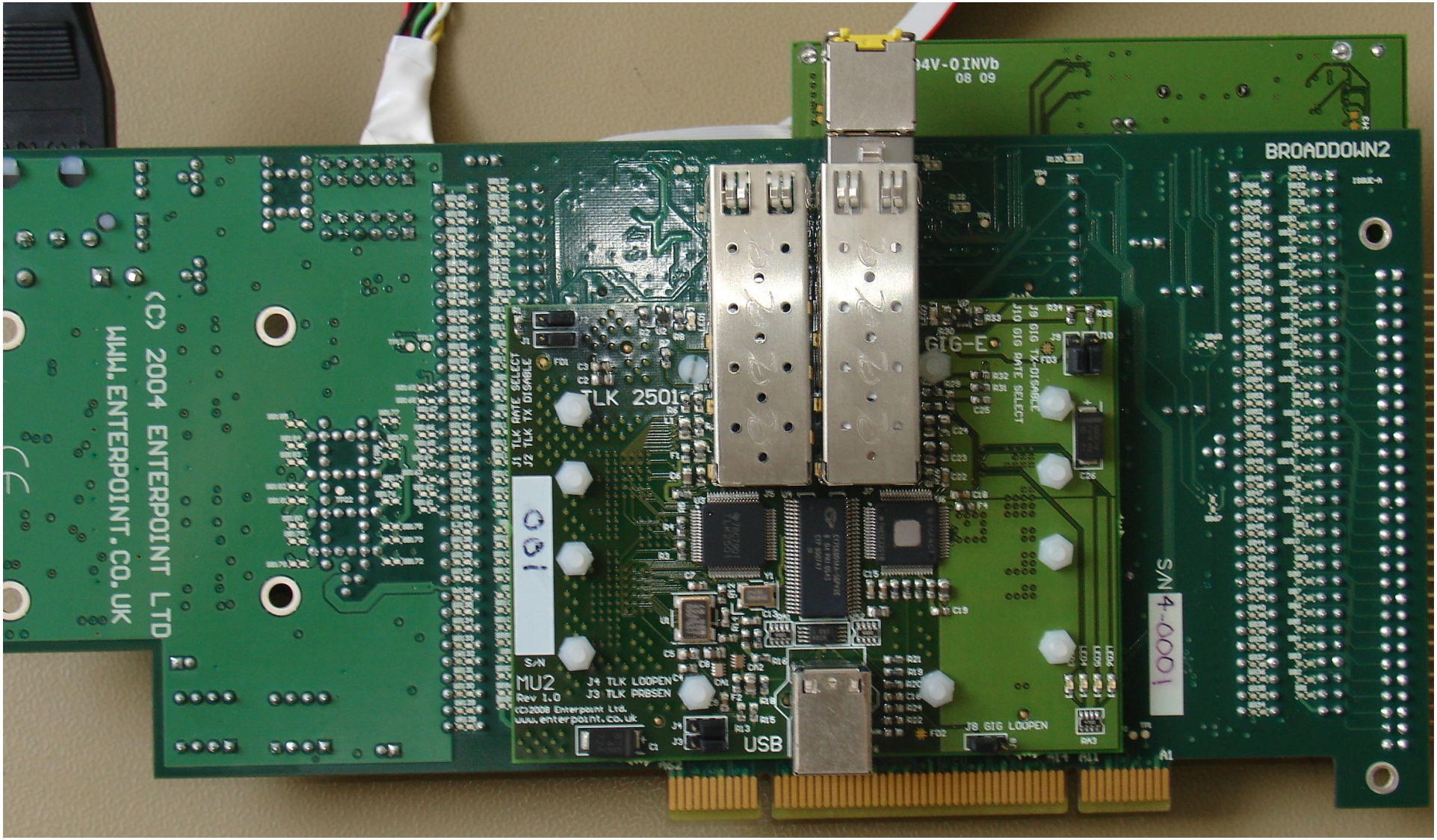
Some note worth points for these initial prototypes.

- We have 10 boards produced, as that the minimum they wanted to do for the costings.
- They have 10 HDMI connectors. HOWEVER in the design only 8 are fully functional. The other 2 require the add-on board be populated with an S3-1000 NOT the S3-400 it currently has.
- This WAS NOT EXPLAINED to us before hand. However the initial specification was "*at least 8 HDMI, ideally 10*" so they have in fact met the requirement we gave them even if only in letter but not the spirit.
- Links are NOT AC-Coupled. This is probably my fault for not insisting it constantly while we argued about things. It was mentioned and was shown in DIF link specification sent to them that came from Cambridge.

HDMI Board

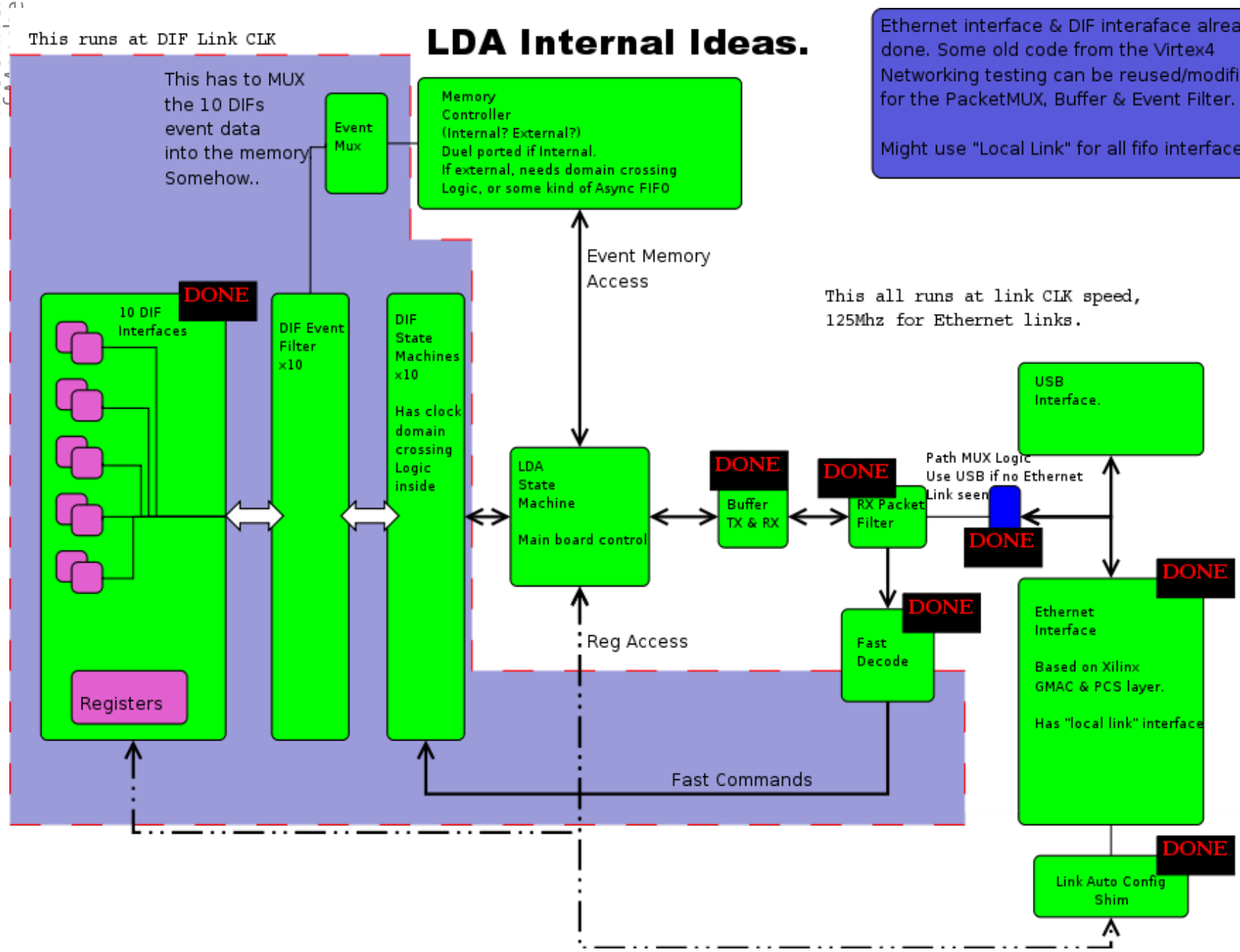
- They added a SATA link on top that is extra to the specification, but it is used in a silly way as 2 single ended links and not as two LVDS pairs.
- We told them we were thinking of using SAMTEC HDMI cables.. So they designed it so we will use SAMTEC cables.
- The clearance on the RHS HDMI sockets means only low profile cables will fit. Most cheap cables would need the strain relief trimming to slide in.

Ethernet Interface Board



ODR Interface Board

- Not enough I/O to route all the signals to the BD2, some are to jumpers for some settings, others are hard wired.
- This should not effect usage...
- It does have 4 nice LEDs on it...
- Having both Ethernet and TLK takes a lot of signals.
- Previous issue with the cost of the GZF connectors... we thought they would be included in the board costings.. Enterpoint thought we would be buying them.


This runs at DIF Link CLK
LDA Internal Ideas.
Ethernet interface & DIF interaface already done. Some old code from the Virtex4 Networking testing can be reused/modified for the PacketMUX, Buffer & Event Filter.
Might use "Local Link" for all fifo interfaces.
This has to MUX the 10 DIFs event data into the memory Somehow..
Event Mux
Memory Controller (Internal? External?) Duel ported if Internal. If external, needs domain crossing Logic, or some kind of Async FIFO
Event Memory Access
This all runs at link CLK speed, 125Mhz for Ethernet links.
DONE
10 DIF Interfaces
DIF Event Filter x10
DIF State Machines x10
Has clock domain crossing Logic inside
LDA State Machine
Main board control
DONE
Buffer TX & RX
DONE
RX Packet Filter
Path MUX Logic
Use USB if no Ethernet Link seen
DONE
USB Interface.
DONE
Ethernet Interface
Based on Xilinx GMAC & PCS layer.
Has "local link" interface
DONE
Fast Decode
DONE
Link Auto Config Shim
Reg Access
Fast Commands
Registers

Firmware Design

- Lots of work done on the framework. Large amounts of this is done.
- Needs work on protocol and main state machines, as well as the event buffer.
- Low level SERDES work is pretty well done, and Ethernet using Xilinx Core(s) is implemented, but requires a license from Xilinx for full usage. We are trying to get a free donation. A commercial quote was 14k USD for a license…
- USB will have to be implemented by someone who wants to use it, the “hooks” are already there to do it.
- The idea with the TLK interface and the USB is to basically fake an Ethernet style packet, so that the rest of the firmware does not need to be altered.

Firmware Design

- Basic idea is two clock domains, the DIF links all exist in one, and the ODR link is in another.
- ODR domain will be dependant on the Link, 125Mhz when Ethernet, but could be lot less when USB.
- Need to try to minimise the crossings.
- Have some niggles about the FPGA capacity to do everything, but only having 8 working links will help this.
- If we can't get the Xilinx Ethernet Core cheap, then some serious thinking is needed. OpenCores.org has GigEthernet core, but it will not meet timing in this S3 device (I tried).
- Designing a GigE MAC is ~3 months full time work at a guess.

Conclusion

- We're getting there.
- Testing of Ethernet will happen in next few weeks.
- Rest of boards will turn up in next few days.
- Need to document the ODR-LDA link spec and packet formats, this exists but not in a public form. Like all people documenting things is not my strong point. Enterpoint also have this problem sadly..
- DIF link packet format needs sorting out too. Will be some simple packet based idea. Error detection is up for debate.
- Will work on the current boards, and maybe consider a respin later for the HDMI boards. Depending on costs, maybe other will do that.
- We maybe need to see who owns the design files...

THE END

Some personal thoughts, which some of you already know :)

- Using “Off the shelf” and “commercial” boards has been a pain in the a**e.
- Too many compromises need to be made, and you end up with not quite what you want.
- As a testbench idea prototype, this is fine, and for the EUDET level it's probably also okay.
- For serious usage, its going to become a little too hard to deal with. Full custom design would allow us to get what we want, with no compromises. More links etc.
- Manpower and cost are the drawbacks.