CCLRC
Rutherford Appleton Laboratory

CMOS Monolithic Active Pixel Sensors (MAPS)

for future vertex detectors

… but not just

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CCLRC - Technology

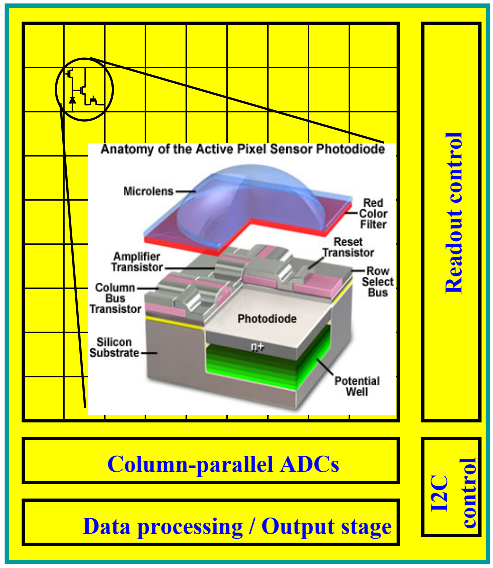
Outline

- Introduction. MAPS for charged particle detection
- Results so far
  - 3T-pixel
  - Pipeline pixels
  - Digital sensors/pixels
- MAPS in an experiment
  - STAR
  - Belle
  - ILC: vertex and calorimetry
- Conclusion

CMOS Monolithic Active Pixel Sensor (MAPS)

(Re)-invented at the beginning of ’90s: JPL, IMEC, …

- **Standard CMOS technology**
- **all-in-one detector-connection-readout = *Monolithic***
- **small size / greater integration**
- **low power consumption**
- **radiation resistance**
- **system-level cost**
- **Increased functionality**
- **increased speed (column- or pixel- parallel processing)**
- **random access (Region-of-Interest ROI readout)**



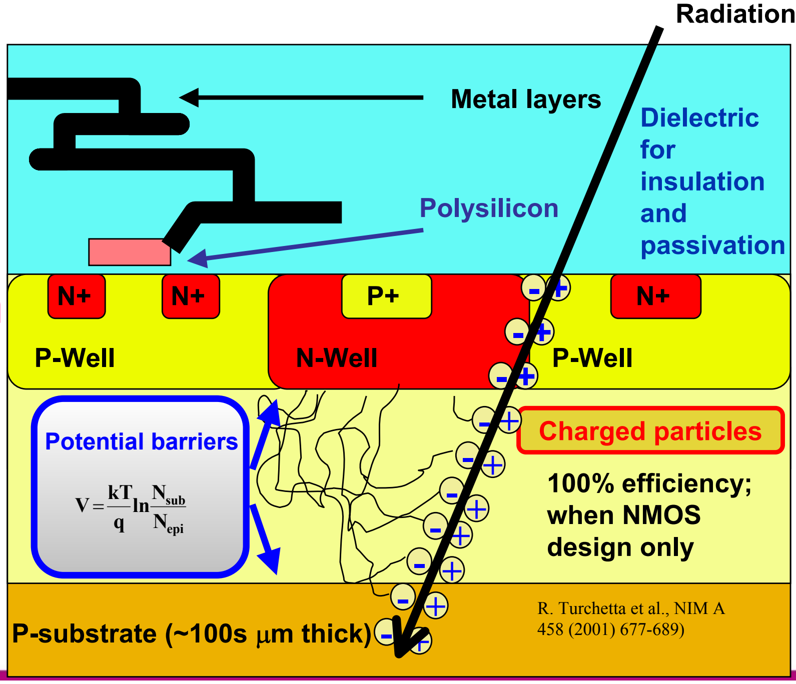
CMOS sensors in digital cameras

Digital intraoral imaging

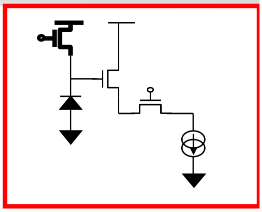
Consumer/prosumer
Digital cameras

Digital mammography

MAPS for charged particle detection



3T pixel



Baseline (minimum) design.

Low noise detection of MIPs first demonstrated in 2001.

Since then, with a number of technologies/epi thickness:

AMS 0.6/14, 0.35/∞, 0.35/14, 0.35/20, AMIS (former MIETEC) 0.35/4, IBM 0.25/2, TSMC 0.35/10, 0.25/8, 0.25/∞, UMC 0.18/∞

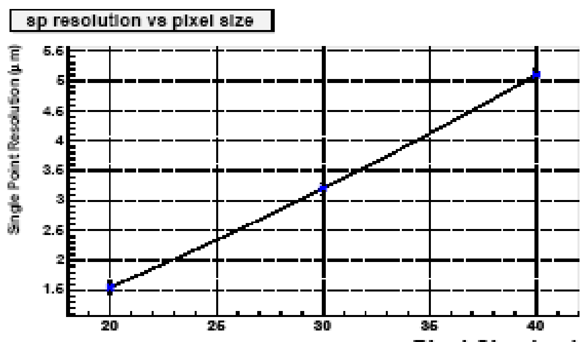
Noise <~ 10 e- rms

Spatial resolution 1.5 µm @ 20 µm pitch, with full analogue readout

Good radiation hardness

Low power

Speed: rolling shutter can be a limit



Radiation hardness

Transistors.

Threshold shift: reduces with shrinking feature size

Bird's beak effect: use enclosed geometry transistors

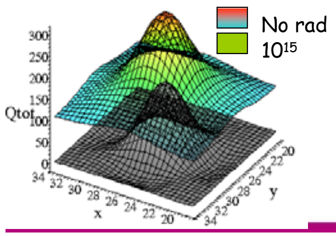
Transistor leakage current: use guard-rings to separate transistors

Diodes.

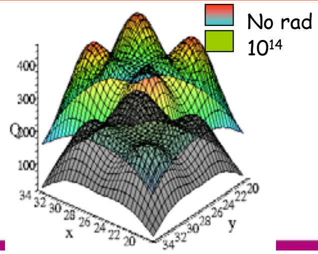
Radiation damage increases leakage current

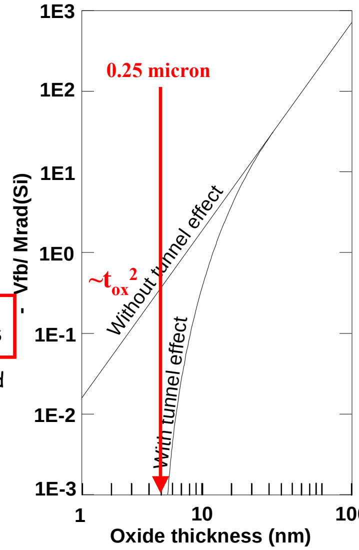
Radiation damage reduces minority carrier lifetime → diffusion distance is reduced

15-μm pixel with 1 diode

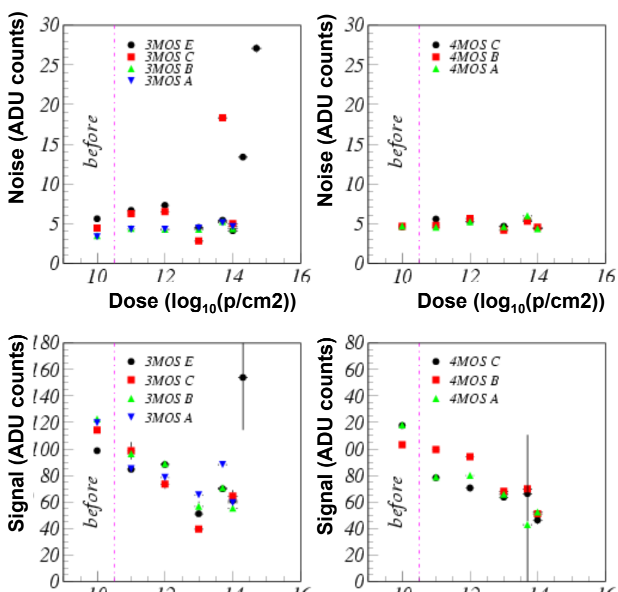


15-μm pixel with 4 diodes

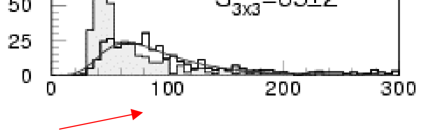




Radiation test. Source results

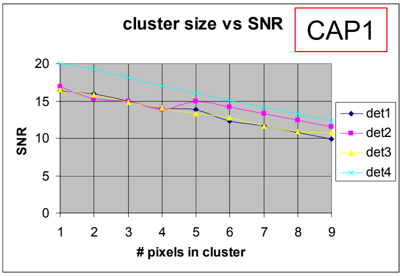


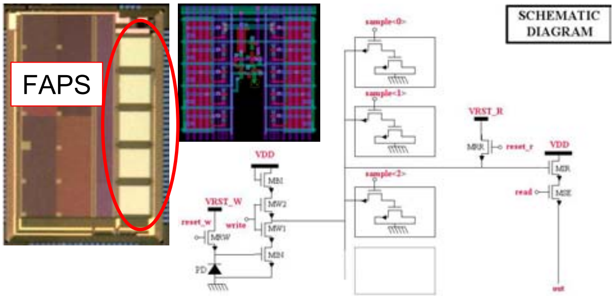
- Test with parametric test sensor RAL_HEPAPS2. Designed in TSMC 0.25/8, in-pixel transistors with 0.35-equivalent oxide thickness
- Several types of pixels
- Noise seems to increase slightly with dose.
- Signal decreases with dose.
- Leakage current increase only noticeable beyond 10^{14} p/cm^2



Pipeline pixels

Flexible Active Pixel Sensor (FAPS, RAL): TSMC 0.25/8, 10 memory cell per pixel; 28 transistors per pixel; 3 sub-arrays of 40x40 pixels @ 20 μm pitch, sampling rate up to 10 MHz. Noise ~ 40 e- rms, single-ended readout





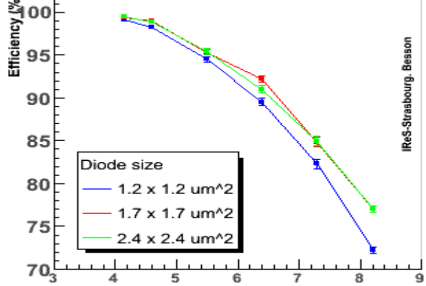
Continuous Acquisition Pixel (CAP, Hawaii): three versions (CAP1/2/3) in TSMC 0.35/8 and 0.25/8, 5 pairs cell/pixel in CAP3 40-50 e- rms single ended → 20-25 differential

MIMOSA12 (Strasbourg) in AMS 0.35/14: 4 pairs/pixel

Digital readout

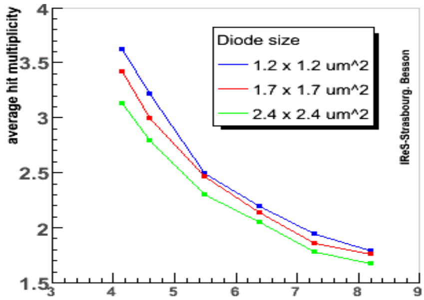
- Several imagers designed by RAL with column-parallel ADC: single-slope (10-bit) and successive approximation (up to 14-bit)
- Mimosa 8 (Saclay)
  - Test in lab: ^{55}Fe results
    - Pixel noise ~ 15 e-
    - CDS ending each column
    - ⇨ Pixel-to-pixel dispersion ~ 8 e-
  - Test beam results (DESY, 5GeV e-)
    - S/N (MPV) ~ 8.5 - 9.5
    - Efficiency > 98%

- TSMC 0.25 μm fab. process with ~ 8 μm epitaxial layer
- Pixel pitch: 25 μm
- 3 sub matrices with 3 diode size: 1.2 x 1.2 μm², 1.7 x 1.7 μm², 2.4 x 2.4 μm²
- 24 // columns of 128 pixels with 1 discriminator per column



Discri. S/N cut

Average hit multiplicity
(num of pixels in cluster)

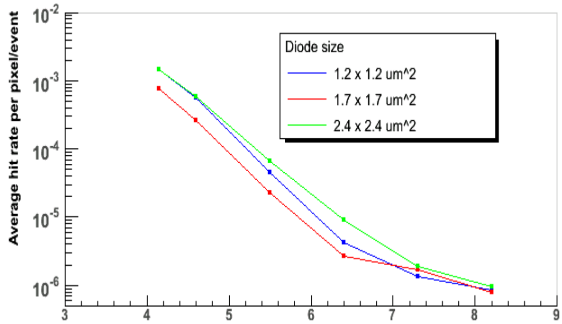


Discri S/N cut

Column comparator

Temp. = 20°C; r.o. = 40 MHz

Fake Hit rate / pixel / event

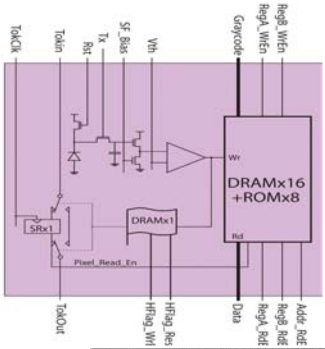


S/N(seed) cut > 5.5
(⇨ discri. threshold =5 mV)
Contamination ~< 5 x 10^{-5}

Discri. S/N cut

In-pixel digitisation

- OPIC (On-Pixel Intelligent CMOS Sensor). Designed by RAL within UK MI3 consortium
- In-pixel ADC (single-slope 8-bit)
- In-pixel TDC
- Data sparsification



Test structure. 3 arrays of 64x72 pixels
@ 30 μm pitch
Fabricated in TSMC 0.25/8
PMOS in pixel → sub-100% efficiency
Starting point for R&D on ILC-ECAL
Calice

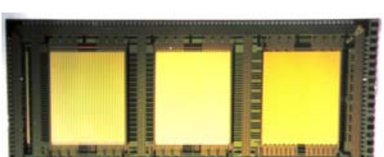
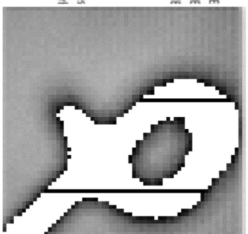
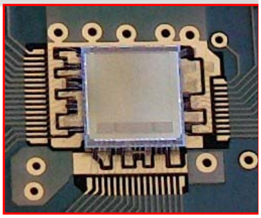


Image obtained with the sensor working in TDC mode with sparse data scan. White pixels are those which didn't cross



MAPS for STAR



MimoSTAR-2 (France)
- AMS 0.35 µm OPTO. 30 µm pitch
- 2 matrices 64 x 128, JTAG architecture
- Rad. hard structure (based on Mimosa 11)

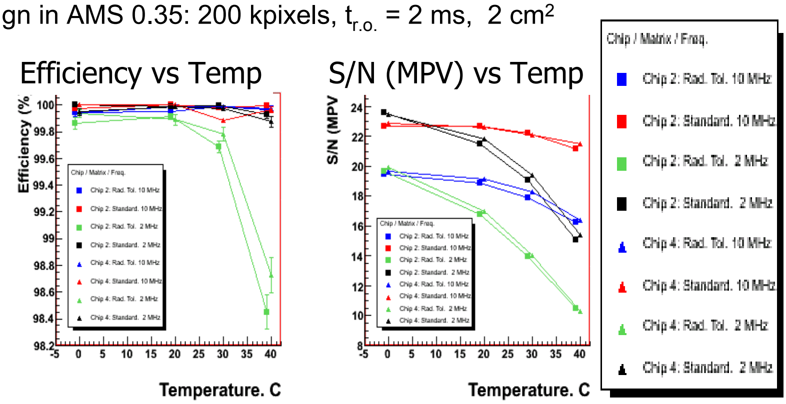
To be installed in STAR (2006)
- ⇨ Ionising radiation tolerant pixel validated at temperature up to + 40 °C
- ⇨ No active cooling needed at int. time ~< O(1 ms)

MimoSTAR-3L in design in AMS 0.35: 200 kpixels, $t_{r.o.}$ = 2 ms, 2 cm²

⇨Test-beam results (DESY, 5 GeV e-)

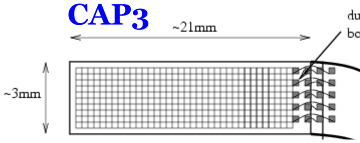
✓ 2 r.o. time (2 and 10 MHz)

⇨ 800 µs and 4 ms

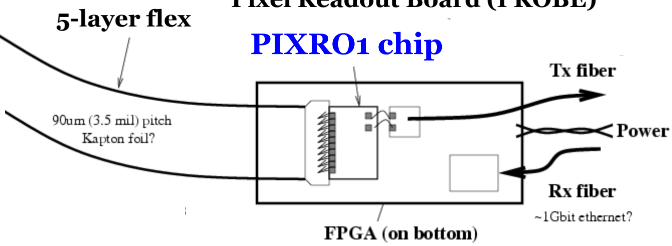


MAPS for Belle

CAP3



Half ladder scheme



128 x 928 pixels, 22.5µm²

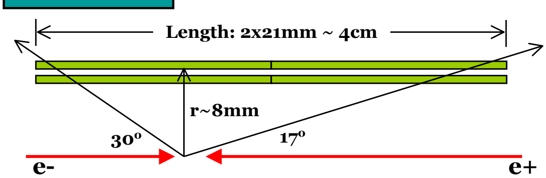
~120 Kpixels / CAP3

0.25 µm process

5 pipeline cell pairs per pixel

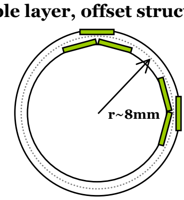
CAP4 also in design

Side view



End view

Double layer, offset structure



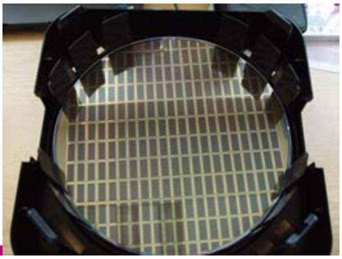
MAPS for ILC

Vertex: R&D in France (MIMOSA family) and UK (RAL_HEPAPS family)

MIMOSA family: latest is n. 15. Several prototypes with different technologies and pixel architectures: 3T, column-parallel comparator, pipeline pixel. Good S/N, radiation hardness, spatial resolution, detection efficiency, … demonstrated

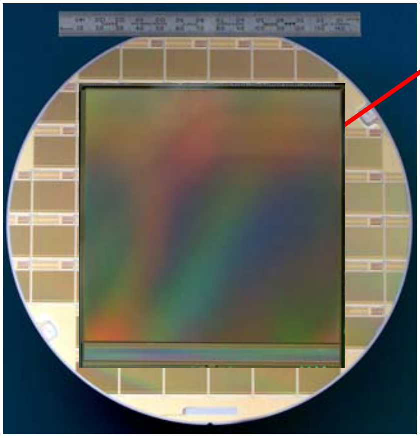
RAL_HEPAPS family: latest is n.4. First demonstrator (FAPS) of pipeline architecture. Fast, column-parallel ADC demonstrated within LCFI- CPCCD

RAL_HEPAPS 4: large format. 3 versions, each with 1026x384 pixels (0.4M pixel), 15 μm pitch, 3T pixel. D1: single diode, enclosed geometry transistors. D2: double-diode. D4: four-diode
ENC <~ 15 e- rms (reset-less)
5 MHz line rate
Rad-hard: > Mrad



ECAL (Calice): R&D just starting in the UK for large area, digital MAPS

Large area sensors



Reticle. Size limited to ~ 2 cm. Reticle is stepped-and repeated → gaps between reticles

CCD foundry. Sometimes large chips are required → different programming of stepping to have no gap ⇔ *'stitching'*

↓ CMOS sensor market

Driven by design of CMOS sensors as replacement of 35 mm film. At a few foundries, it is now possible to design stitched (seamless) sensors → 'wafer-scale'
Foundry choice rapidly widening

Stitched sensors likely to be needed for ILC: Vertex and ECAL (Calice)

Conclusions

CMOS MAPS first proposed as detectors for particle physics in 1999

100% efficiency detection demonstrated in 2000

Since then, good performance in terms of S/N, detection efficiency, radiation hardness, spatial resolution demonstrated with 3T

New sensors architecture developed: pipeline pixels, digital sensors, digital pixels

R&D for MAPS at Belle and STAR well underway. They could be the first experiments to have a MAPS-based vertex detector

Development at ILC in progress for both Vertex and ECAL. They are likely to need stitched sensors

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