

Master I/O Connectors

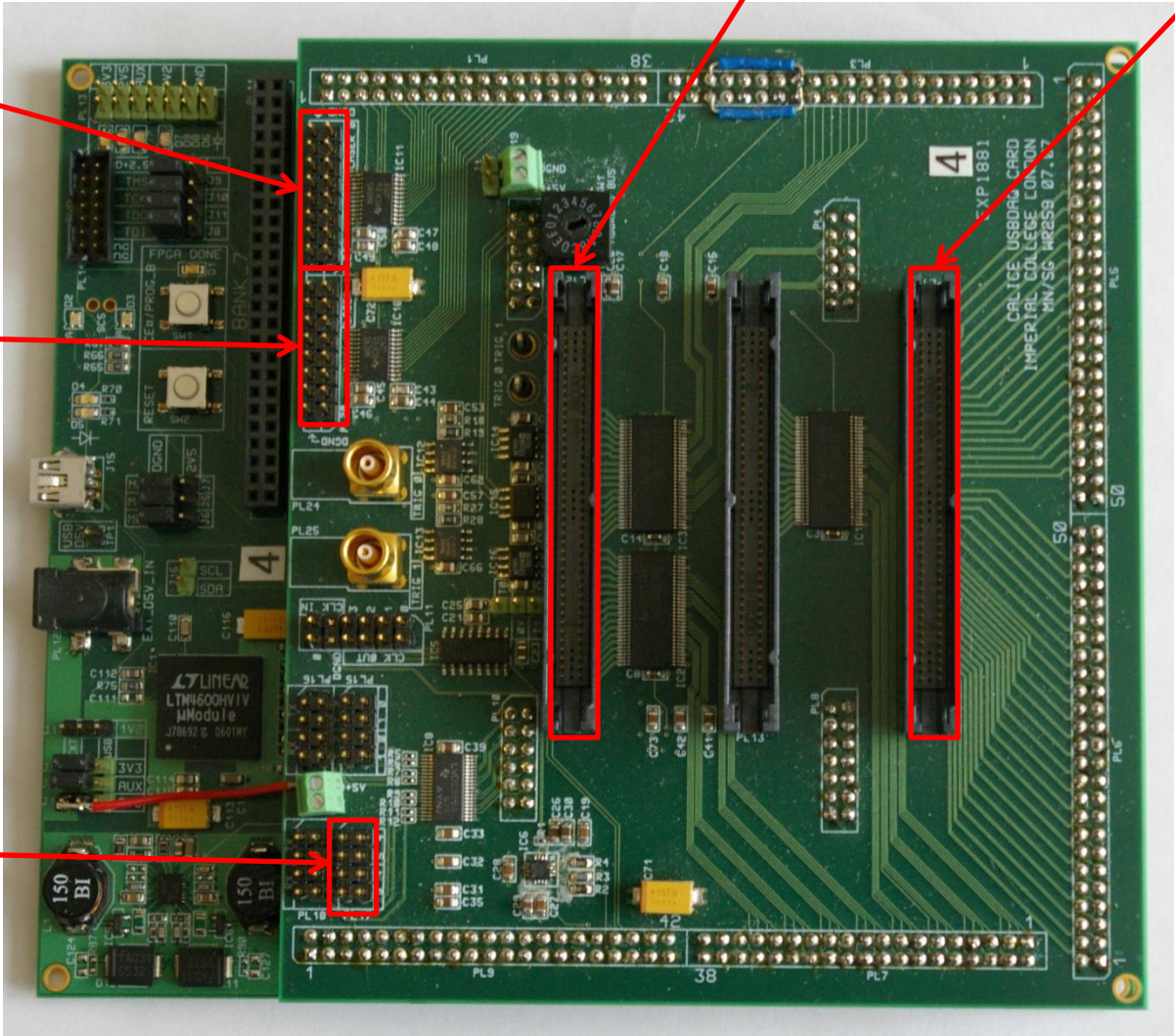
PL21

PL20

PL17

PL12

PL14



PL12: Clock, bunch train start

All LVDS; polarity not checked

Pair 39, unused

Etc.

Pair 33, unused

Pair 32, unused

Pair 31, bunch train start

Pair 30, 40MHz clock

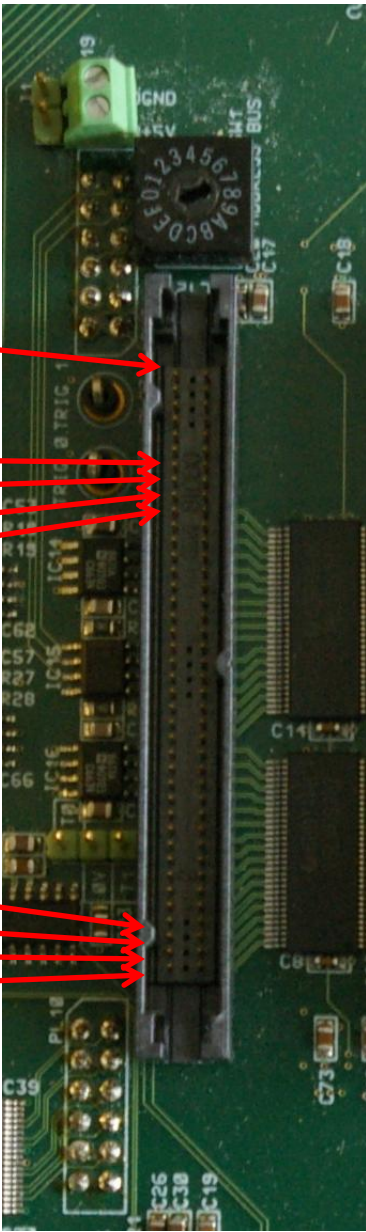
Etc.

Pair 3, bunch train start

Pair 2, 40MHz clock

Pair 1, bunch train start

Pair 0, 40MHz clock

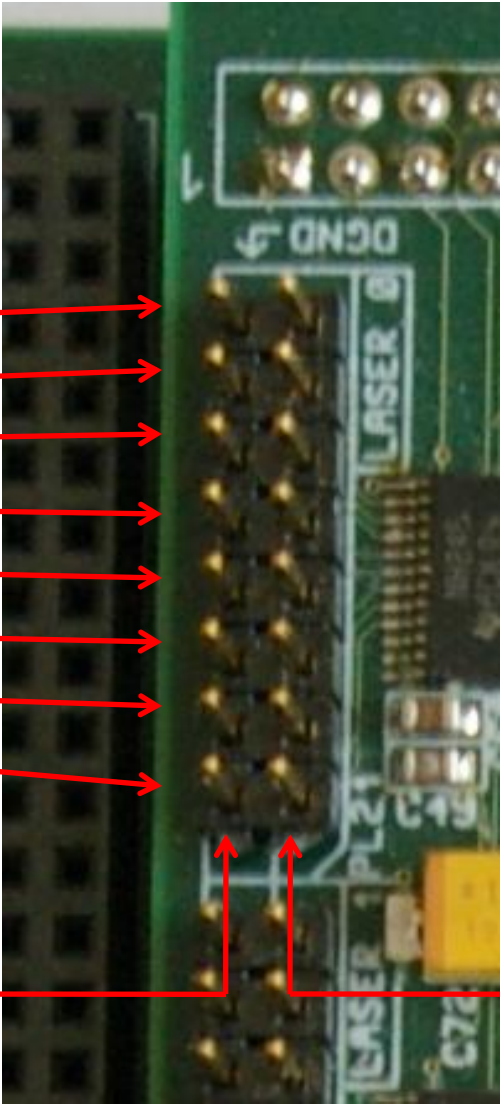


PL21: Output signals

All TTL

- Pair 7, End of bunch train
- Pair 6, Bunch train active
- Pair 5, H/w trigger
- Pair 4, Test bit 2
- Pair 3, Test bit 1
- Pair 2, Test bit 0
- Pair 1, S/w trigger bit 1
- Pair 0, S/w trigger bit 0

Gnd +5/Gnd



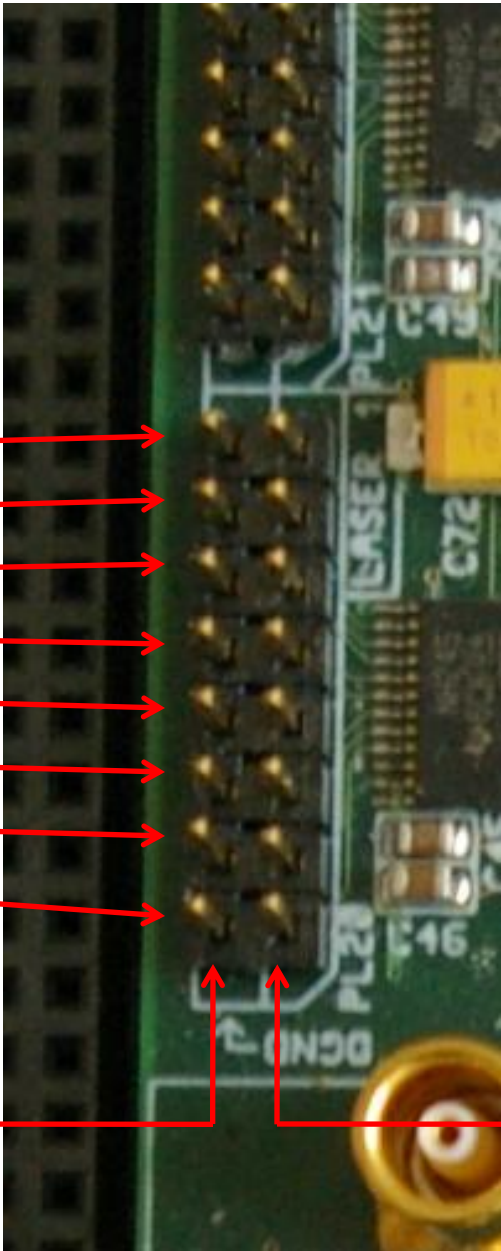
PL20: Input bits 0-7

All TTL

- Pair 7, Input bit 7
- Pair 6, Input bit 6
- Pair 5, Input bit 5
- Pair 4, Input bit 4
- Pair 3, Input bit 3
- Pair 2, Input bit 2
- Pair 1, Input bit 1
- Pair 0, Input bit 0

Gnd

+5/Gnd



PL14: Input bits 8-15

All LVDS; polarity not checked,
order not checked

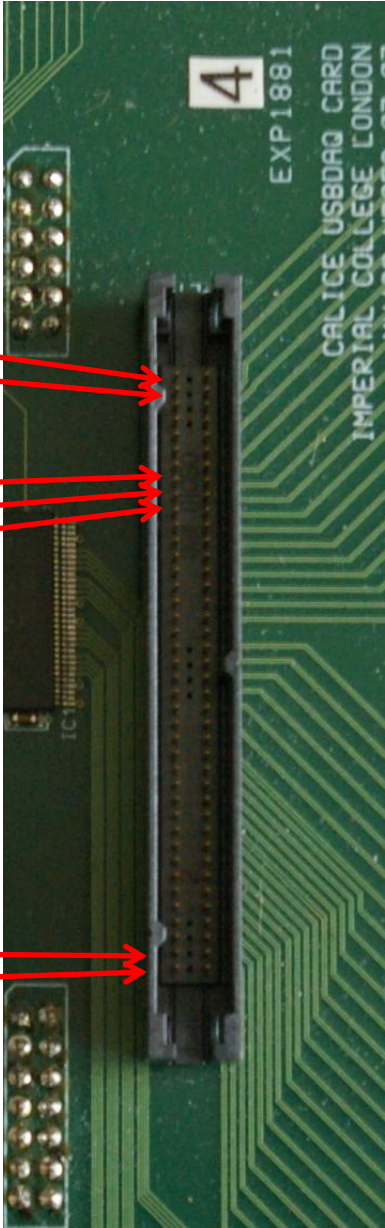
Pair 39, Input bit 8
Pair 38, Input bit 9

Etc.

Pair 32, Input bit 15
Pair 31, unused
Pair 30, unused

Etc.

Pair 1, unused
Pair 0, unused



PL17: TLU interface

All LVDS

- Pair 0, Busy
- Pair 1, Trigger
- Pair 2, Trigger clock
- Pair 3, TLU reset

Negative Positive

