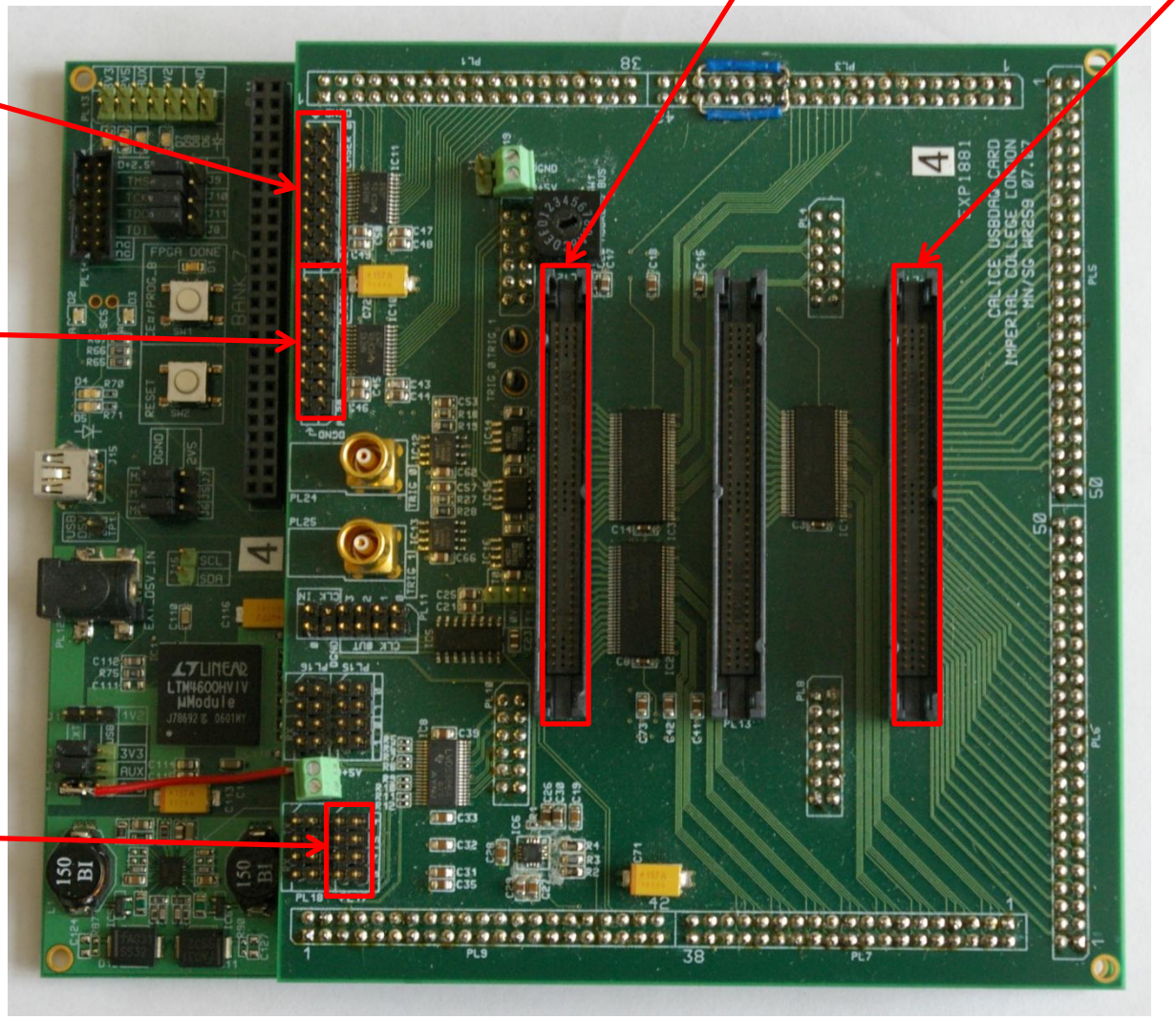
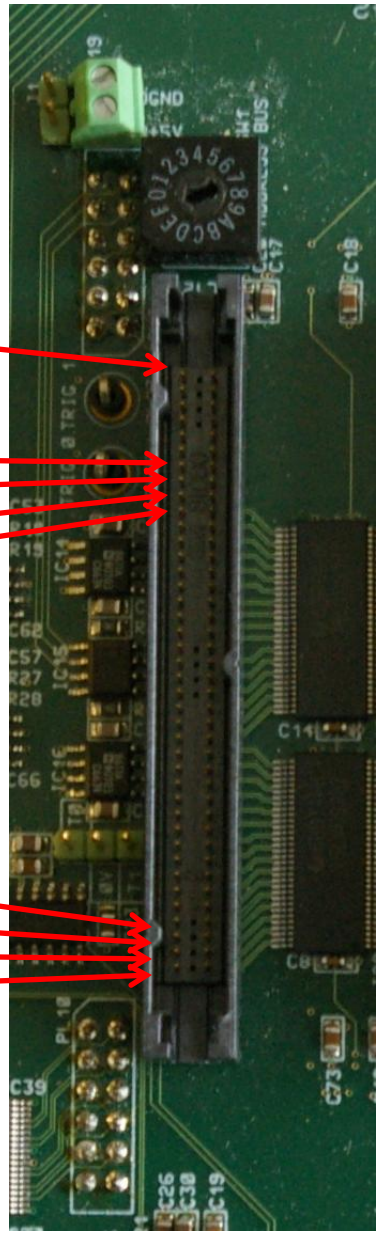
# Master I/O Connectors



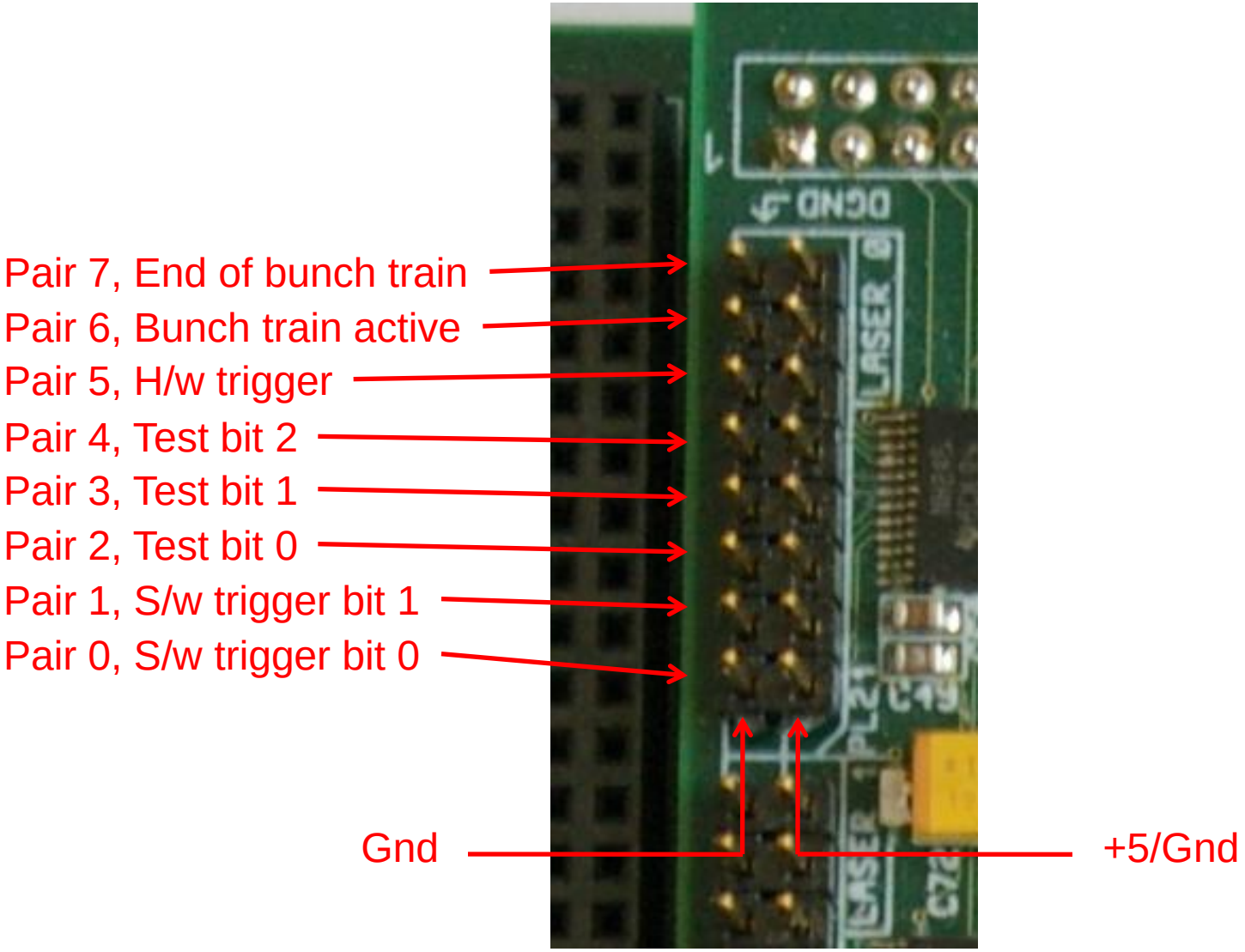
# PL12: Clock, bunch train start

All LVDS; polarity not checked



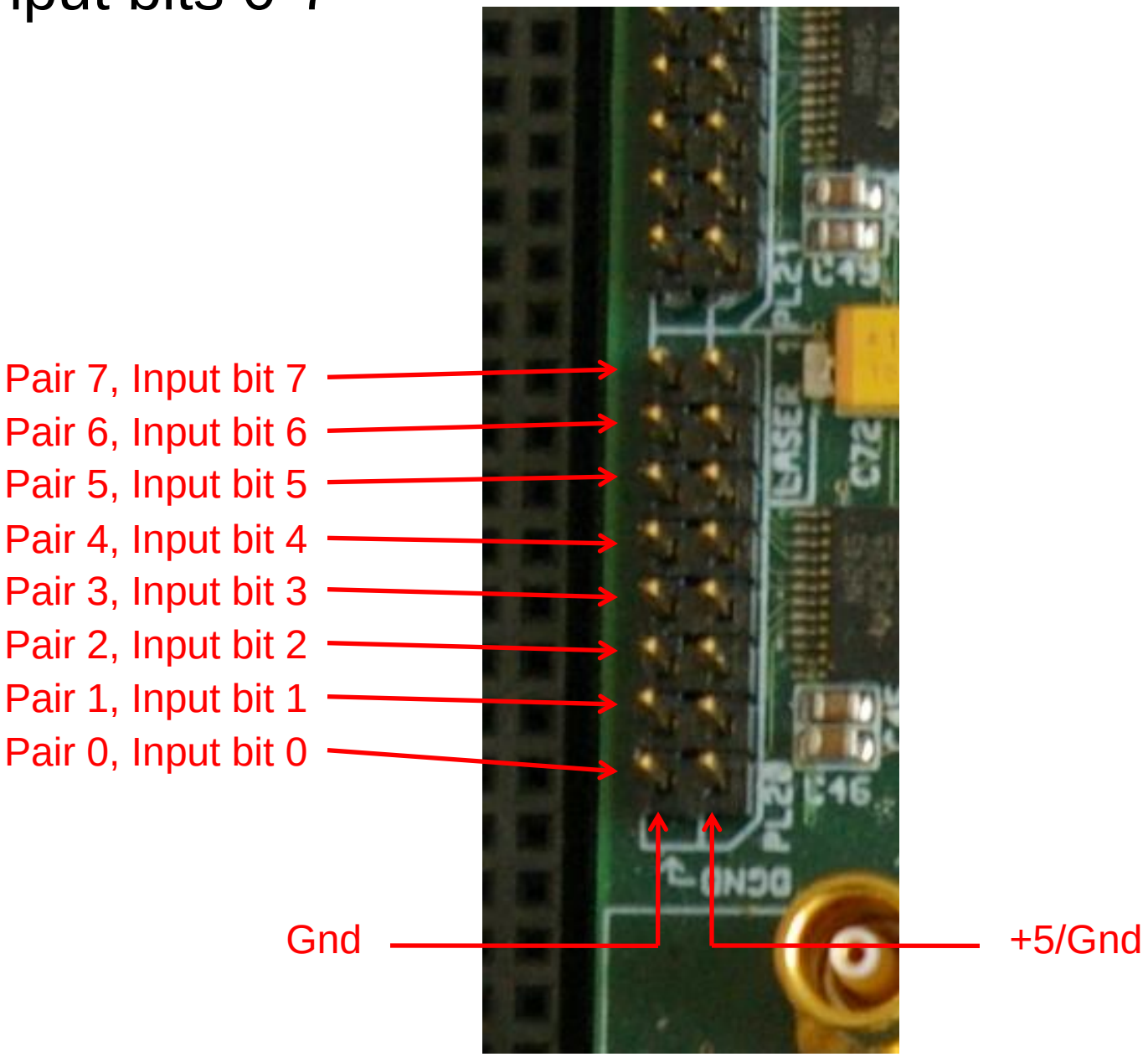
# PL21: Output signals

All TTL



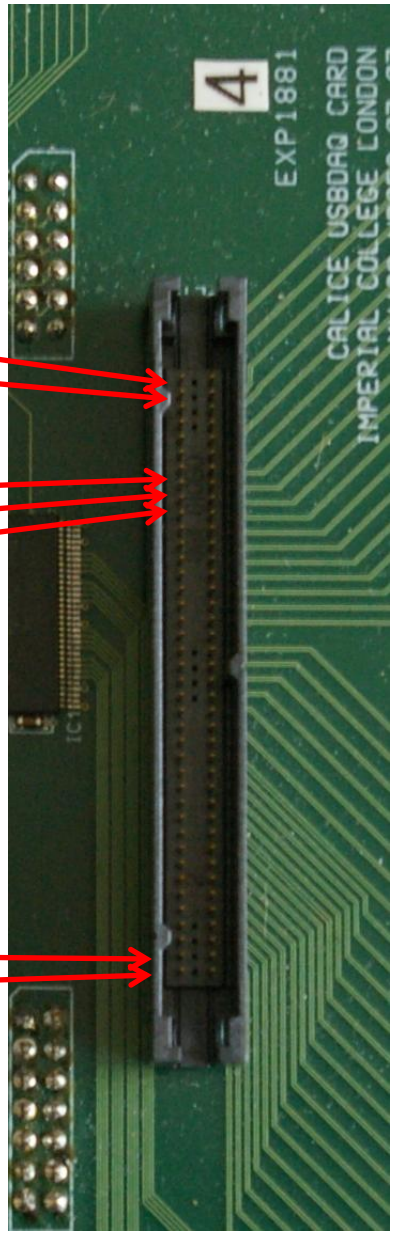
# PL20: Input bits 0-7

All TTL



# PL14: Input bits 8-15

All LVDS; polarity not checked, order not checked




Pair 39, Input bit 8
Pair 38, Input bit 9

Etc.

Pair 32, Input bit 15
Pair 31, unused
Pair 30, unused

Etc.

Pair 1, unused
Pair 0, unused

# PL17: TLU interface

All LVDS