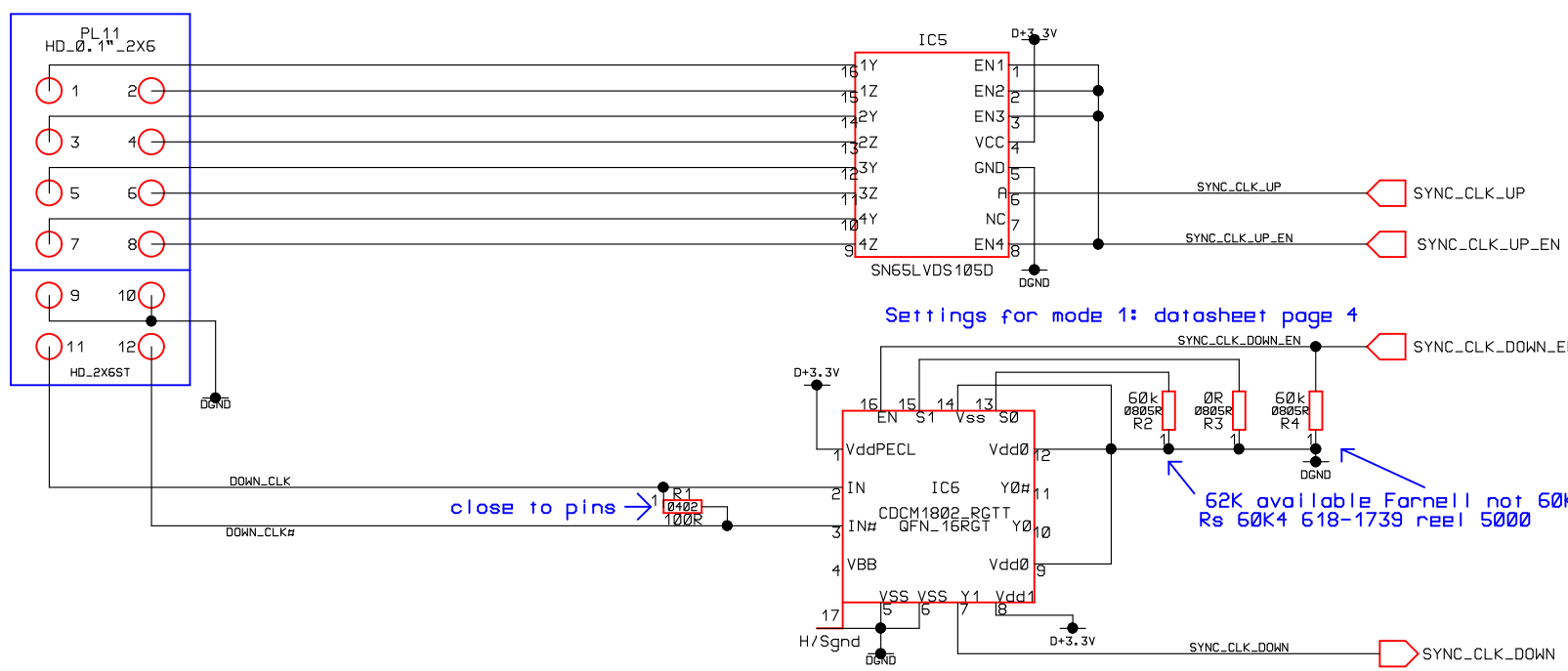


Pins rather than sockets on this sheet

SYNC_INTERFACE

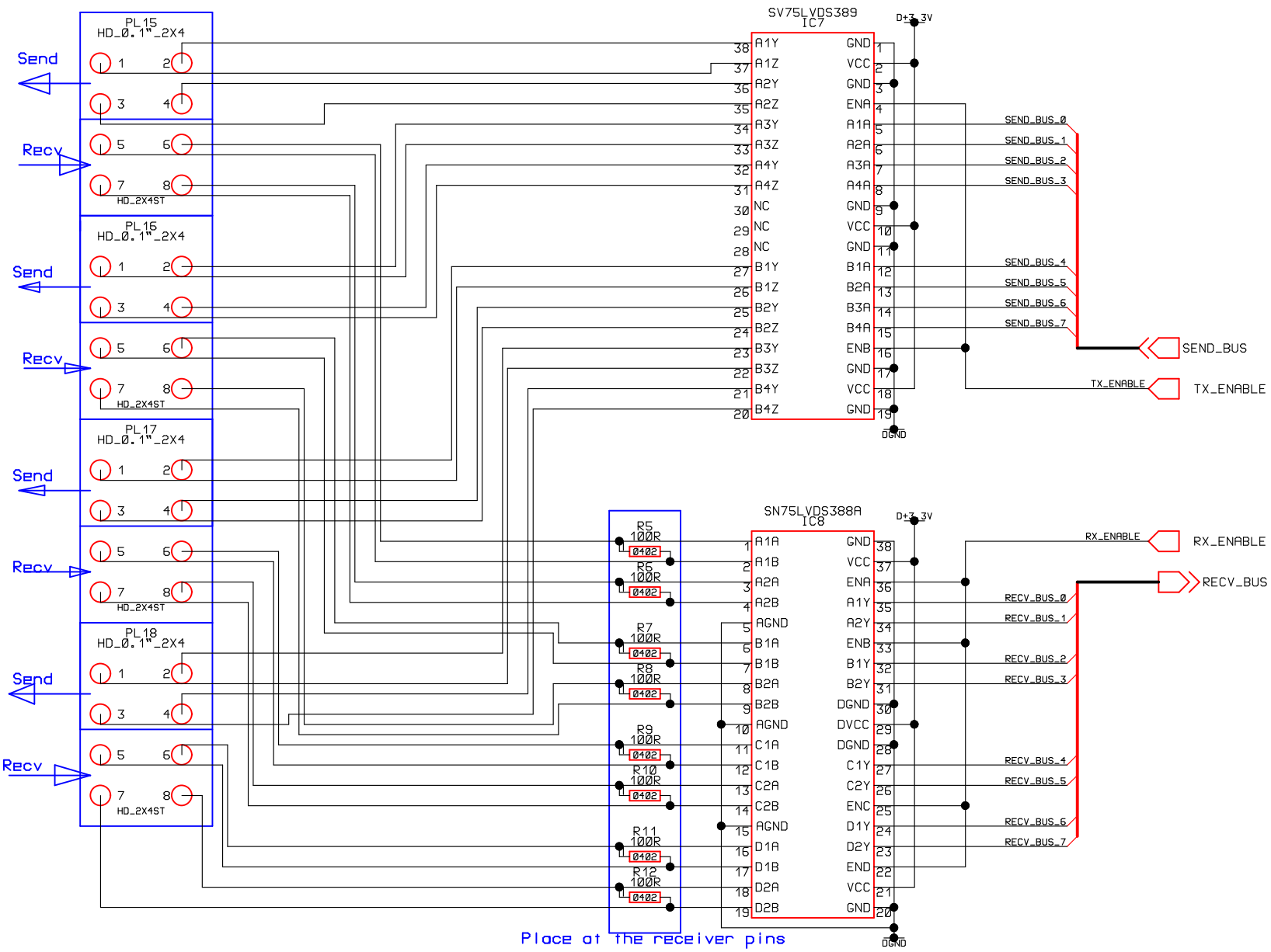
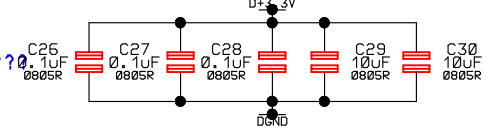
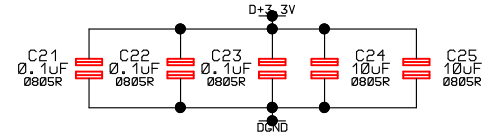
Upstream Clocks

Downstream Clock

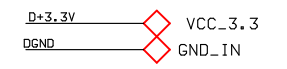
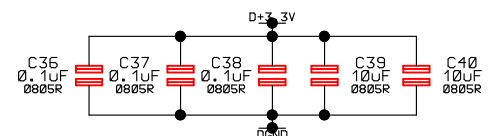
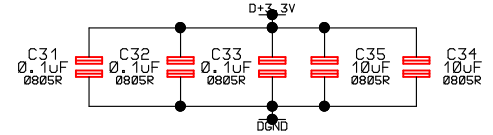


Settings for mode 1: datasheet page 4

62K available Farnell not 60K????
Rs 60K4 618-1739 reel 5000



Place at the receiver pins



HEP, Imperial College, London		
Title: USBDAQ/CALICE	Engineer:	
Subtitle:	Drawn by:	
SYNC INTERFACE		
Ver: v12b4.rxl	Date: 3.7.07	
Sheet:	of:	