Pins rather than sockets on this sheet

SYNC_INTERFACE

Upstream Clocks

Downstream Clock

PL11 HD_0.1"_2X6

SN65LVDS105D IC5

SYNC_CLK_UP

SYNC_CLK_UP_EN

Settings for mode 1: datasheet page 4

SYNC_CLK_DOWN_EN

DOWN_CLK

DOWN_CLK#

close to pins

R1 0402 100R

CDCM1802_RGTT IC6 QFN_16RGT

52K available Farnell not 60K???? 0.
Rs 60K4 618-1739 reel 5000

H/Sgnd

SYNC_CLK_DOWN

C21 0.1UF 0805R
C22 0.1UF 0805R
C23 0.1UF 0805R
C24 10UF 0805R
C25 10UF 0805R

C26 0.1UF 0805R
C27 0.1UF 0805R
C28 0.1UF 0805R
C29 10UF 0805R
C30 10UF 0805R

Send

Recv

PL15 HD_0.1"_2X4

PL16 HD_0.1"_2X4

PL17 HD_0.1"_2X4

PL18 HD_0.1"_2X4

HD_2X4ST

SV75LVDS389 IC7

SEND_BUS_0
SEND_BUS_1
SEND_BUS_2
SEND_BUS_3
SEND_BUS_4
SEND_BUS_5
SEND_BUS_6
SEND_BUS_7

SEND_BUS

TX_ENABLE

C31 0.1UF 0805R
C32 0.1UF 0805R
C33 0.1UF 0805R
C35 10UF 0805R
C34 10UF 0805R

SN75LVDS388A IC8

R5 100R 0402
R6 100R 0402
R7 100R 0402
R8 100R 0402
R9 100R 0402
R10 100R 0402
R11 100R 0402
R12 100R 0402

Place at the receiver pins

RX_ENABLE

RECV_BUS

RECV_BUS_0
RECV_BUS_1
RECV_BUS_2
RECV_BUS_3
RECV_BUS_4
RECV_BUS_5
RECV_BUS_6
RECV_BUS_7

C36 0.1UF 0805R
C37 0.1UF 0805R
C38 0.1UF 0805R
C39 10UF 0805R
C40 10UF 0805R

D+3.3V VCC_3.3

DGND GND_IN

HEP, Imperial College, London		
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Subtitle: SYNC INTERFACE		Drawn by:
		Ver: v12b4.rx1
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