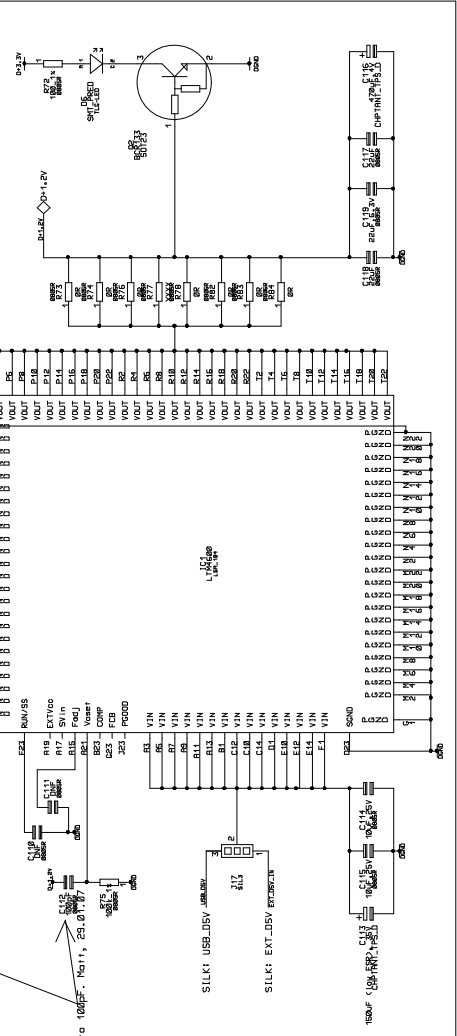
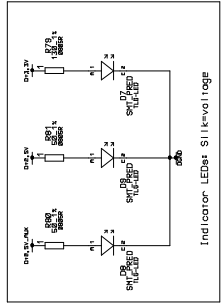
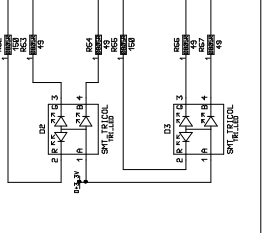


VOULE ??

Tab1:Pages of the databseet



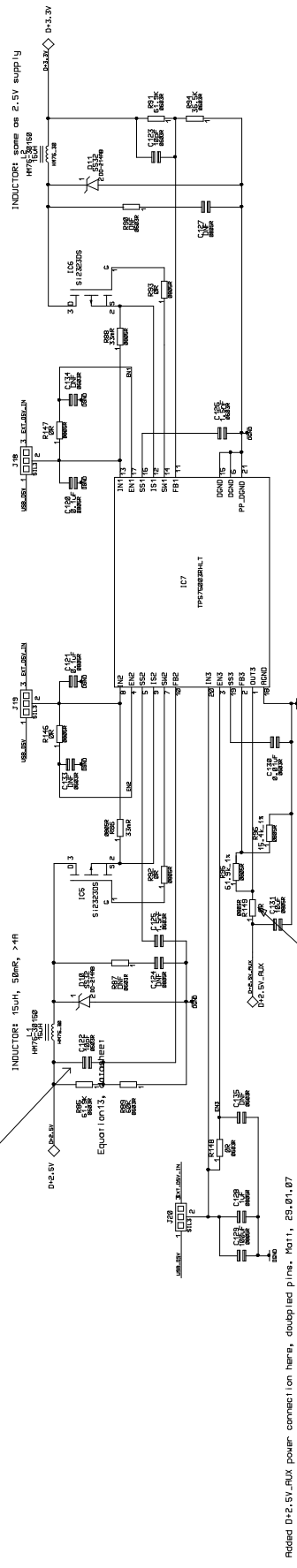
Front Panel LEDs
VME, POWER, ETHERNET, USB
Note that LEDs are numbered 1, 0, 3, 2, 5, 4, etc from top to bottom on front panel.
These are now driven directly by the FPGA



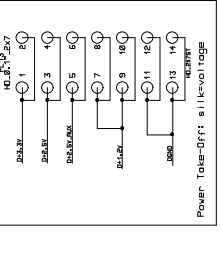
Please see layout guidelines in databseet for both these regulators.

looked again at the databseet and it is 100pF. Not1, 29.01.07

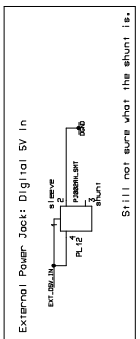
100PF???



Added D+2.5V_RUX power connection here, duplicated pins. Not1, 29.01.07



I'd like to add this zero ohm link if possible. Not1, 29.01.07



Still not sure what the shunt is.

REP: Imperial College, London	Engineer:
Title: USB_DQO_POWER338	Drawn By:
SubTitle: v0.2f	Ver:
Sheet: X	Date: 21.11.05