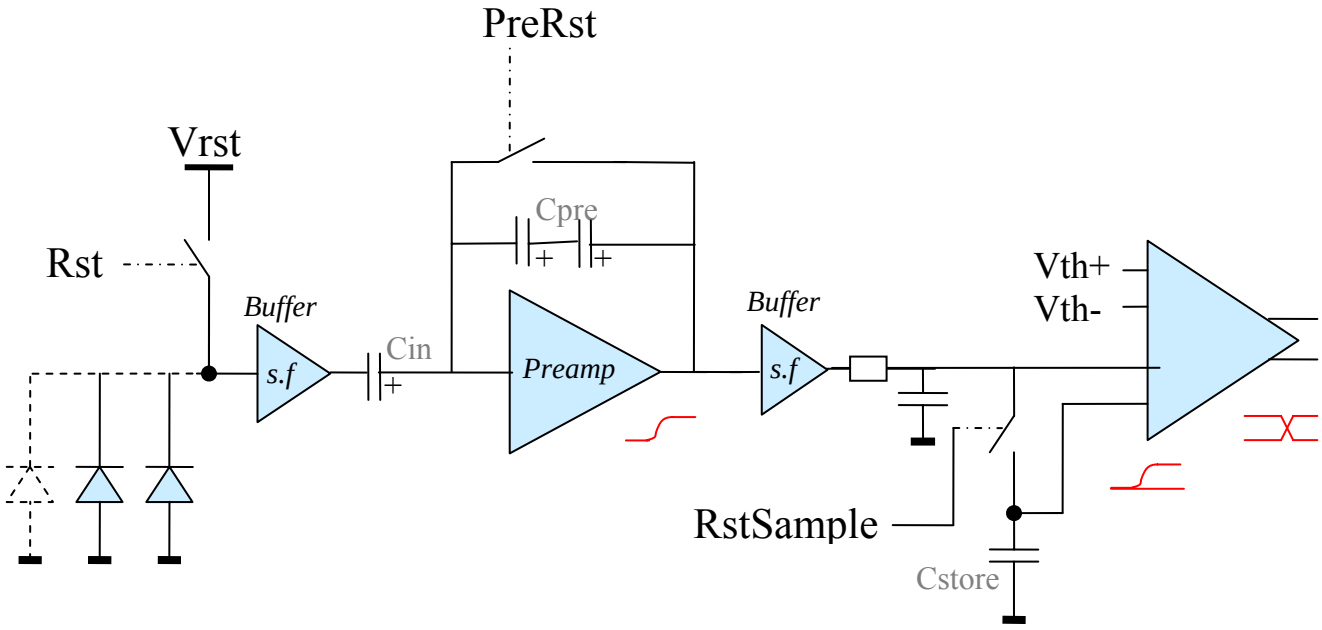
FDR: PreSample pixel changes & simulations

Summary/Dialogue

A number of minor modifications were made to the preSample pixel during layout. These are listed below:

a) Capacitor technology changed to NWCAP for the input and feedback capacitors in the shaper circuit *[see separate doc.]*
b) Capacitor technology changed to NMOSCAP for the storage and filtering capacitors
c) Native transistors removed (on advice from foundry) – PMOS source follower used in place of native source follower circuit originally used. Bias lines at column and array level are adjusted accordingly.
d) Filter transistor (resistor) removed (neg. effect)
e) External reset is separated such that analog and sample can be correctly reset in sequence from outside the pixel (ie at start of bunch train).
f) Comparator trim circuit common bias is moved from pixel to column level.
g) Diodes are implemented as 3.6um, with chamfered corners.
h) NMOS comparator load reduced to ¾ size (was made large to achieve better matching, but layout was too tight – is still large and immediately adjacent to the mirror device to matching is as good as it can be)
i) Monostable (nwcap) capacitor sizes adjusted slightly to aid efficient layout.
j) Substrate contacts added around diodes

Review: PreSample Pixel Overview



Extracted Node Parasitics

The final preSample pixel layout is evaluated for parasitic capacitances. The table below shows the summed parasitics on each circuit node, sorted to show the largest parasitic capacitances, truncated at 5fF (full list is much longer).

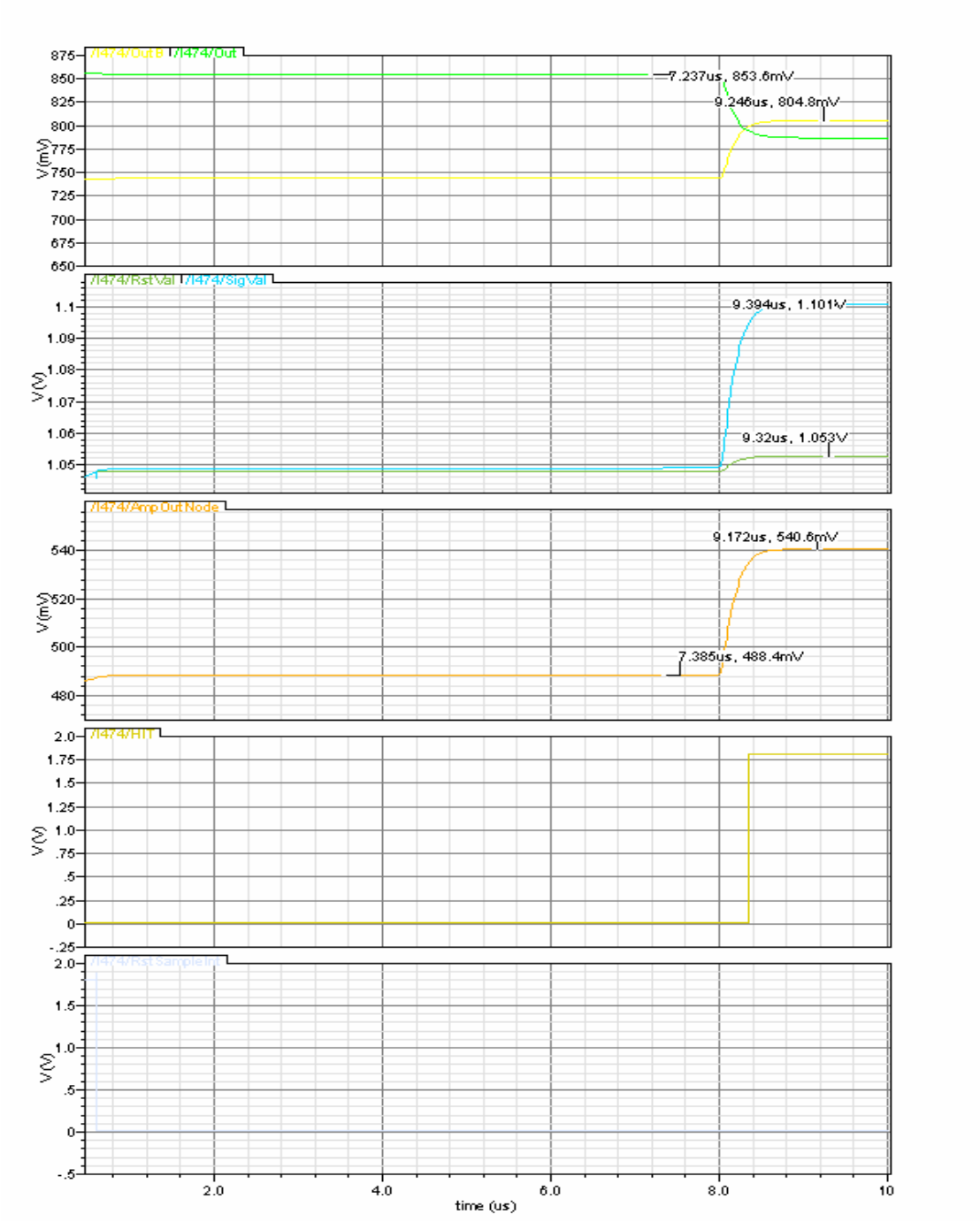
NetName	R	sum C	sum L
/VSS	NA	221.665f	0
/VDD1V8dco	NA	29.0081f	0
/VDD1V8mso_sram	NA	27.9685f	0
/sf1out	NA	23.9827f	0
/compbias1	NA	20.4627f	0
/VDD1V8pix	NA	20.012f	0
/AmpIn	NA	18.1769f	0
/biascomptrim	NA	17.9075f	0
/Diode_Node	NA	13.901f	0
/VDD1V8aco	NA	11.852f	0
/SigVal	NA	10.4975f	0
/invbiasn	NA	10.2849f	0
/HIT	NA	9.67877f	0
/OutB	NA	9.47132f	0
/invbiasp	NA	9.46558f	0
/Out	NA	9.29804f	0
/I5/I5/net030	NA	8.80373f	0
/vrst	NA	7.85108f	0
/I420/net0129	NA	7.77374f	0
/RstVal	NA	7.53939f	0
/MASK_BIT	NA	7.24326f	0
/I4/I5/net030	NA	6.66885f	0
/TRIM<0>	NA	6.65256f	0
/TRIM<1>	NA	6.18537f	0
/row_phi2	NA	5.87444f	0
/I420/net071	NA	5.6216f	0
/I8/net0132	NA	5.5772f	0
/I8/net098	NA	5.5263f	0
/pixsfbias	NA	5.48471f	0
/TRIM<2>	NA	5.43698f	0
/row_phi2b	NA	5.32531f	0
/I5/I5/net056	NA	5.28091f	0
/row_phi1b	NA	5.13044f	0

The diode node (highlighted) is reported at 13.9fF. This is larger than the 8fF assumed during schematic simulations, and will contribute to a higher total noise than originally predicted.

The higher capacitance can most likely be attributed to the shielding tracks that run alongside the diode node connections, and also the slightly longer track lengths for connecting to diodes placed towards the pixel corners.

Full Pixel simulation

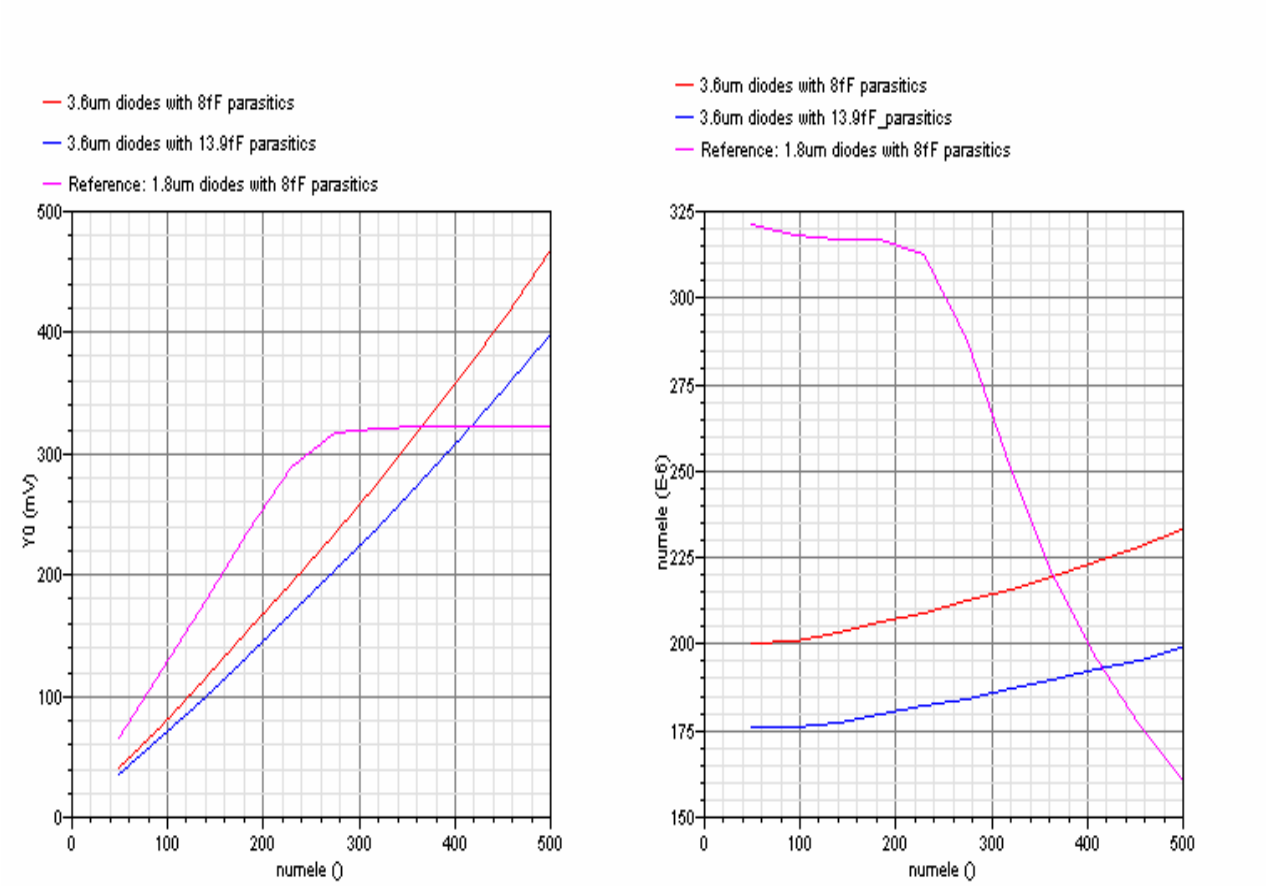
The pixel schematic that was used to match LVS is re-simulated to double-check correct functionality.



[RT]

Signal Gains

The larger (3.6um) diode size used in the pixel means the circuit gain is reduced. The additional capacitance also contributes to this effect. The original values stated in previous documents refer to the 1.8um diode case, so these are plotted for reference.



Charge-voltage gain is tabulated below for the ~linear gain region:

Diode size	**Parasitics**	**Gain** *(@numele=250)*
1.8 um	8 fF	310 uV/e-
3.6 um	8 fF	210 uV/e-
3.6 um	13.9 fF	183 uV/e-

(Lower gain does offer larger full-well capacity.)

Noise Analysis

```
/I474/M3          id        0.00515363              41.81
/I474/M3          fn        0.00333495              17.51
/I474/M1          fn        0.00321423              16.26
/I474/M1          id        0.00272007              11.65
/I474/M2          id        0.00151063              3.59
/I474/M5          id        0.00115704              2.11
/I474/M5          fn        0.00115485              2.10
/I474/R0          rn        0.00101067              1.61
/I471/M110        id        0.000882931             1.23
/I471/M33         id        0.000453306             0.32
/I474/M2          fn        0.00043443              0.30
/I471/M110        fn        0.000309375             0.15
/I474/I14/M7      id        0.00025816              0.10

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.0079701
Total Input Referred Noise = 0.0524133
The above noise summary info is for noise data
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Applying √2 factor to account for sampling this becomes 11.27mV. Referring this back to the input using the realistic new conversion gain (183uV/e-) yields a total noise of 61.6e-.

Discrepancy identified as Cfb series pair polarities → were mounted "back-to-back" in the initial simulations for the capacitor change document) but have since been changed to straight series connection (possibly due to a design rule?). May need to consult with tower (possible use of pixel variant?); also need to check with eldo.

Device	Param	Noise Contribution	% Of Total
/I474/M3	id	0.00515367	41.81
/I474/M3	fn	0.00333499	17.51
/I474/M1	fn	0.00321427	16.26
/I474/M1	id	0.0027201	11.65
/I474/M2	id	0.00151064	3.59
/I474/M5	id	0.00115705	2.11
/I474/M5	fn	0.00115487	2.10
/I474/R0	rn	0.00101068	1.61
/I471/M110	id	0.000882938	1.23
/I471/M33	id	0.00045331	0.32
/I474/M2	fn	0.000434435	0.30
/I471/M110	fn	0.000309379	0.15
/I474/I14/M7	id	0.00025816	0.10

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.00797017
Total Input Referred Noise = 0.0524132
The above noise summary info is for noise data

Current cap orientation

Device	Param	Noise Contribution	% Of Total
/I474/M3	id	0.000254508	32.95
/I474/I14/M7	id	0.000244988	30.53
/I474/I14/M0	id	0.000191309	18.62
/I474/I8/M34	id	6.89003e-05	2.41
/I474/M3	fn	6.7157e-05	2.29
/I474/I14/M7	fn	6.57004e-05	2.20
/I471/M43	id	5.79238e-05	1.71
/I474/M5	id	5.71395e-05	1.66
/I474/I8/M2	id	4.85234e-05	1.20
/I474/I8/M23	id	4.32819e-05	0.95
/I471/M110	id	4.29315e-05	0.94
/I474/I14/M0	fn	3.75391e-05	0.72
/I474/I8/M33	id	3.26424e-05	0.54

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.00044338
Total Input Referred Noise = 0.0235281
The above noise summary info is for noise data

"Back-to-back" cap orientation