Review Approval Form

Type of Review: FDR-part1 (preliminary design of all preSample pixels)

Project Name: TeraPixel APS for CALICE

Documents Reviewed
Latest top level schematics Latest layouts → full chip top level , excluding pads, only preSample pixels. Logic changes v0.9 PreSample pixel changes v1.3 PreSample capactitor technology change document v1.2 Attendees: JC, RT, Paul Dauncey, Nicola Guerrini, Mark Prydderch, Matt Noy, Marcel Stanitzki, Konstantin Stefanov, Mike Tyndel, Giulio Villani
Comments
Full minutes taken by Paul Dauncey, available on web at http://www.hep.ph.ic.ac.uk/calice/maps/fdr1/notesPart1.txt PreSample pixel Noise should be verified with Eldo Capacitors should be changed to the preferable "back-to-back" configuration, or ideally every permeatation checked for an informed decision. Outstanding from IDR2: Check likelihood of the comparator output sitting at mid-rail causing current flow in subsequent logic. Pixel should be simulated as RCX view. Pixel layout changes - re-route RstExt200 to avoid input amp - power monostables separately - separate monostable ground Diode node is seen to be approx 75microns in length, with 0.5um separation to ground – hand calculations (post-review) confirm the total RCX parasitics on this node to be 13.9fF. Investigate increasing this separation (does the easily achievable 0.2-0.3 microns make much difference?) PreShape pixel Layout still in progress, so nothing directly to review: Comments that the second monostable (not needed) could be left in place and tied inactive to make the two pixel designs as similar as possible. Optimal capacitors will still need to be re-selected to allow the PreShape circuit design to fit into the allowable space. Logic Changes are summarised in the corresponding document – these were each identified and explored in varying detail. Antenna design rules currently not checked, but likely to require additional diodes on long clock and control lines in the logic. Large config-programming simulation shows a two-cycle delay in correct data appearing at the other end of the chip – this is most likely a bug in the simulation stimulus, but should be investigated at some point (low priority).

Approval: emails indicating approval are an adequate substitute for hardcopy signatures

Review Report agreed
Group Leader (sign/date) as required by the Project Management Plan

Customer (sign/date) as required by the Project Management Plan

Others – as stated in the Project Management Plan

Review Report agreed and any changes incorporated
Project Manager (sign/date) always required