Review Approval Form

Type of Review: FDR-part2 (completed design, but with pixel test structures omitted)

Project Name: TeraPixel APS for CALICE

Documents Reviewed
Latest top level schematics Latest layouts → full chip top level , including pads, test structures not implemented. PreShape pixel capacitor options PreSample pixel capacitor options Calice_powers summary ppt Attendees: JC, RT, Paul Dauncey, Nicola Guerrini, Mark Prydderch, Marcel Stanitzki

Comments

Full minutes taken by Paul Dauncey, available on web at
http://www.hep.ph.ic.ac.uk/calice/maps/fdr1/notesPart2.txt

Note to try LVS and DRC in 64-bit mode – ask Mark for more details, may improve speed/memory usage for top-level checks.
1.8um diodes are selected as optimum based on results from Giulio.

PreSample pixel

Capcitor orientation results for all 8 combinations are presented – Eldo and Spectre disagree on the numbers (at least a factor of two worse in spectre) but do agree in trends. Spectre cannot simulate with the internal floating node, but one of these scores well in Eldo. Configuration BTTBTB is seen to be a high scorer in both simulation tools and is selected as one variant. Configureation BTBTTB is seen to score well in Eldo but is not possible to siumluate in spectre – however, the physical arrangement of the two Top-to-Top nodes in the series capacitance is attractive since the floating node is metal, and the two nwell nodes are driven low-impedance nodes, hence this is selected as the other variant.

PreShape pixel

Four capacitors make 16 configurations, but only spectre results are available at this time. These results should be repeated in Eldo if possible to verify the decisions made here. The fourth capacitor (final feedback) seems to make negligible difference, so will be set to TB in both cases so the bottom nwell node is driven by the output of the shaper. Combinations TBBTBT and TBBTTB will be selected (note different ordering of capacitors!) – essentially the same equivalent options to the preSample pixel, but again the latter cannot be proven with spectre.

Layout required the redundant monostable to be removed to allow room for the 4Mohm resistor (previously suggested this should be left in but tied inactive).
Shaper load may benefit from moving to the right to avoid coupling onto the floating mid-point of the series capacitors – RT will evaluate and change as appropriate.
DPW layer should be a cross, symmetrical in all directions, and with 2um overlap of nwell regions. Same for all pixel variants.

Other comments

No DPW should be added to biases or Logic
Antenna checks must be run and errors mitigated with diodes
Variant for test structures should be the best performing variant if not space for both.

If enough pads, Vth for neighour should be wired separately to properly model a neighbour hit, rather than the current method of wiring the monostable input.
Add two more Vrst pads on right hand side of chip
Check the RC time constant on the 8mm lines! Must be able to support the 50Mhz non-overlapping clocks; add intermediate buffers if necessary (will add slight skew but assure operating speed is possible).
RT to check with foundry that wafers are not metallised on the back (from previous FDR)

Some concern that M3 may need dummy fill to meet coverage requirements: Final DRC checks will report this – any corrective action should be carefully controlled in the pixel (not auto/random generated).

Recommend a dry-run submission ASAP to verify the processes involved are working and to get a preliminary look at likely DRC error load.

Approval: emails indicating approval are an adequate substitute for hardcopy signatures

Review Report agreed
Group Leader (sign/date) as required by the Project Management Plan

Customer (sign/date) as required by the Project Management Plan

Others – as stated in the Project Management Plan

Review Report agreed and any changes incorporated
Project Manager (sign/date) always required