Change Request

Project	Change Request No.
MAPS for CALICE	2

Part A (to be completed by the Originator)

Description of Change Requested
Could be very useful to add some primitive device test structures to TPAC1.1 design. The foundry's PCM structures do not monitor performance of transistors placed with the deep p-well, and whilst initially thought not to be affected, other sources have suggested there could be some threshold shift. Since there are free pad sites on TPAC1.1 (and space between pad cells) it could be beneficial to add some test transistors to this submission, so we can monitor the effects of DPW and (if made) Hi-Res Epi on typical transistors. Such test structures could also include a copy of the layout of the 4Mohm resistor in the preShape pixel, which might give some direct indication of the real value & spread thereof which would also be of interest.
Anticipated Benefits/Reason for Change
Opportunity for in-house transistor parameter extraction to further understand process modifications (primarily the Deep p-well implant and hi-res epi wafer)

Please click on the box with the most likely result of the change in each row

	Substantial Reduction	Reduction	No change	Increase	Substantial Increase
Cost	☐	☐	✓	☐	☐
Schedule	☐	☐	☐	✓	☐
Performance	☐	☐	✓	☐	☐
Resources	☐	☐	✓	☐	☐
Risk	☐	☐	✓	☐	☐

Minor effort required ~3 days to make new layout as drop-in replacement for empty pad sites in current design.

Originator	JC		
Signature		**Date**	

Approval Required in (click on box)	**1 week**	✓	**2 weeks**	☐	**1 month**	☐	**2 months**	☐

Part B (to be completed by the Project Manager)

Recommended for (click on box)		Project Manager Signature	Date
Implementation ✓	**Rejection** ☐		
Approval for Implementation		**Customer/Sponsor Signature**	**Date**
JC			

Action Required/Comments

If approved, Rebecca Coath would make a "drop-in" circuit block that could be placed in the top left of the design (currently a long space with no occupied pad sites). No change to CALICE pcb is required since these are independent of all operational circuits.

Some discussion with Steve Thomas required to understand the most suitable structures to place for interaction with the keithly and other device characterisation equiplment.

For testing, the devices would be packaged in DIP units to fit into standard keithley test equipment.