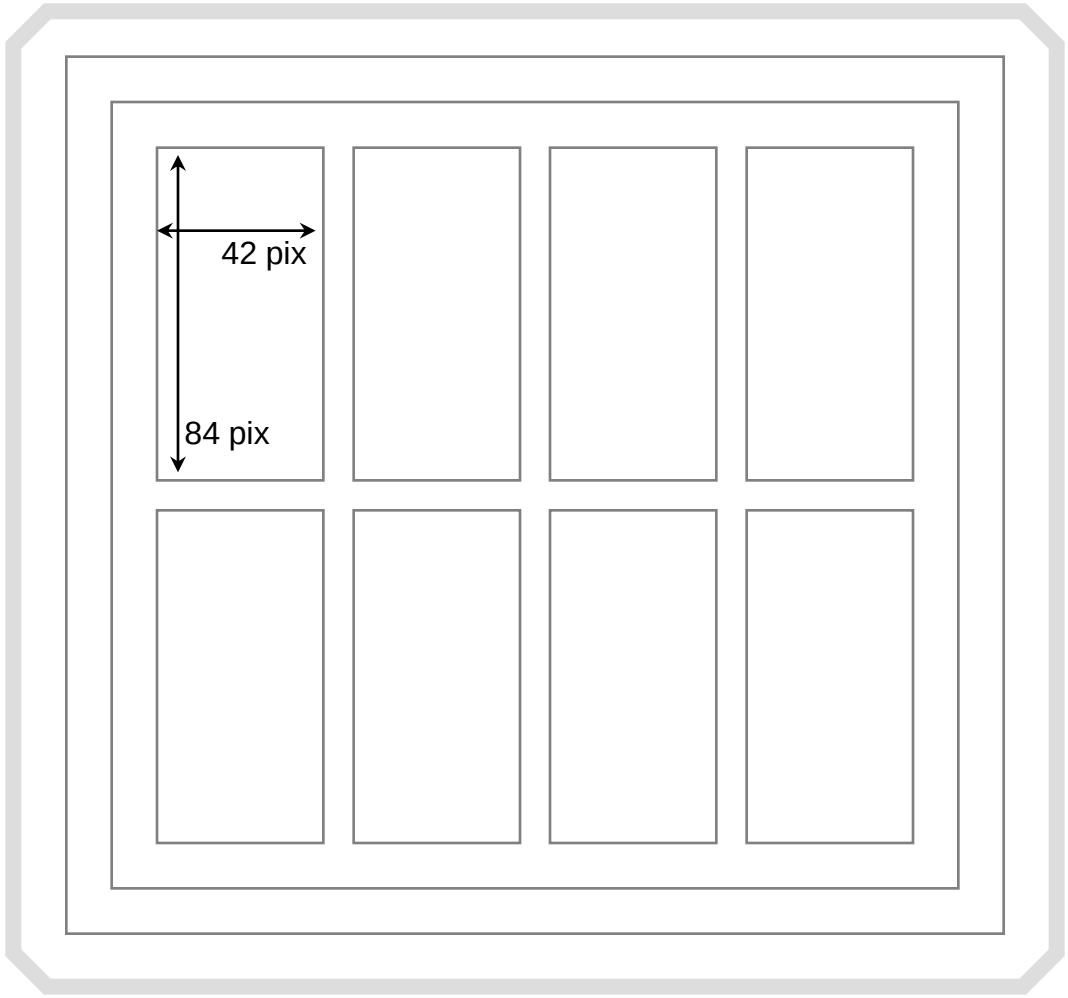
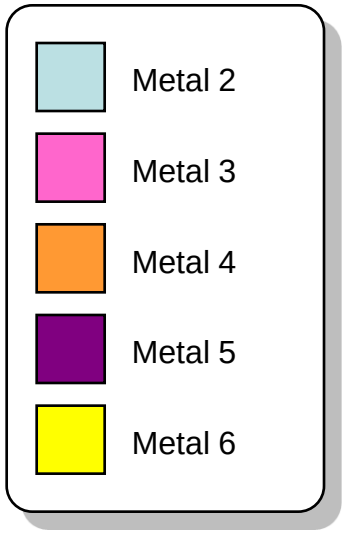
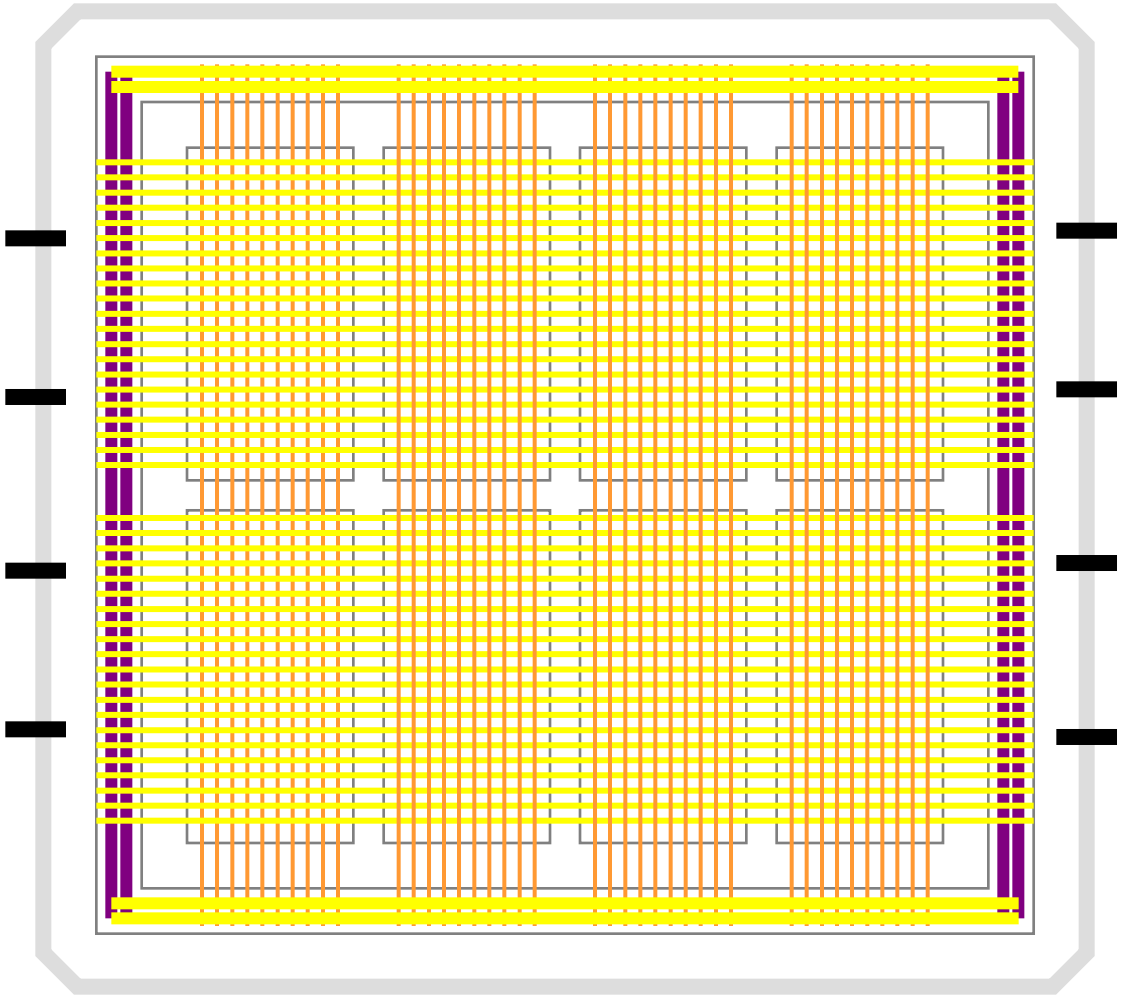
CALICE TPAC1.1: Power Plan





(Top Level)

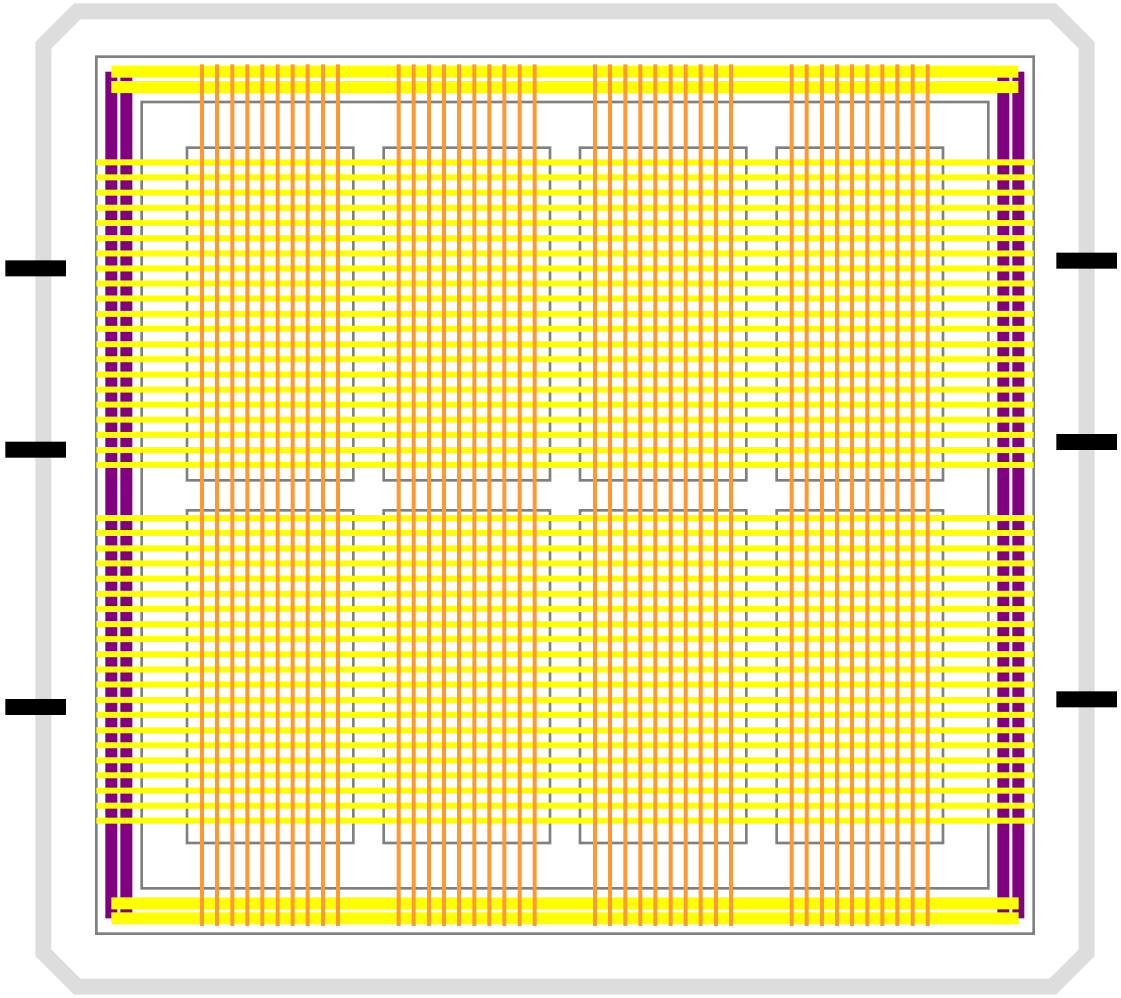
VDD1V8pix & VSS:Gpix



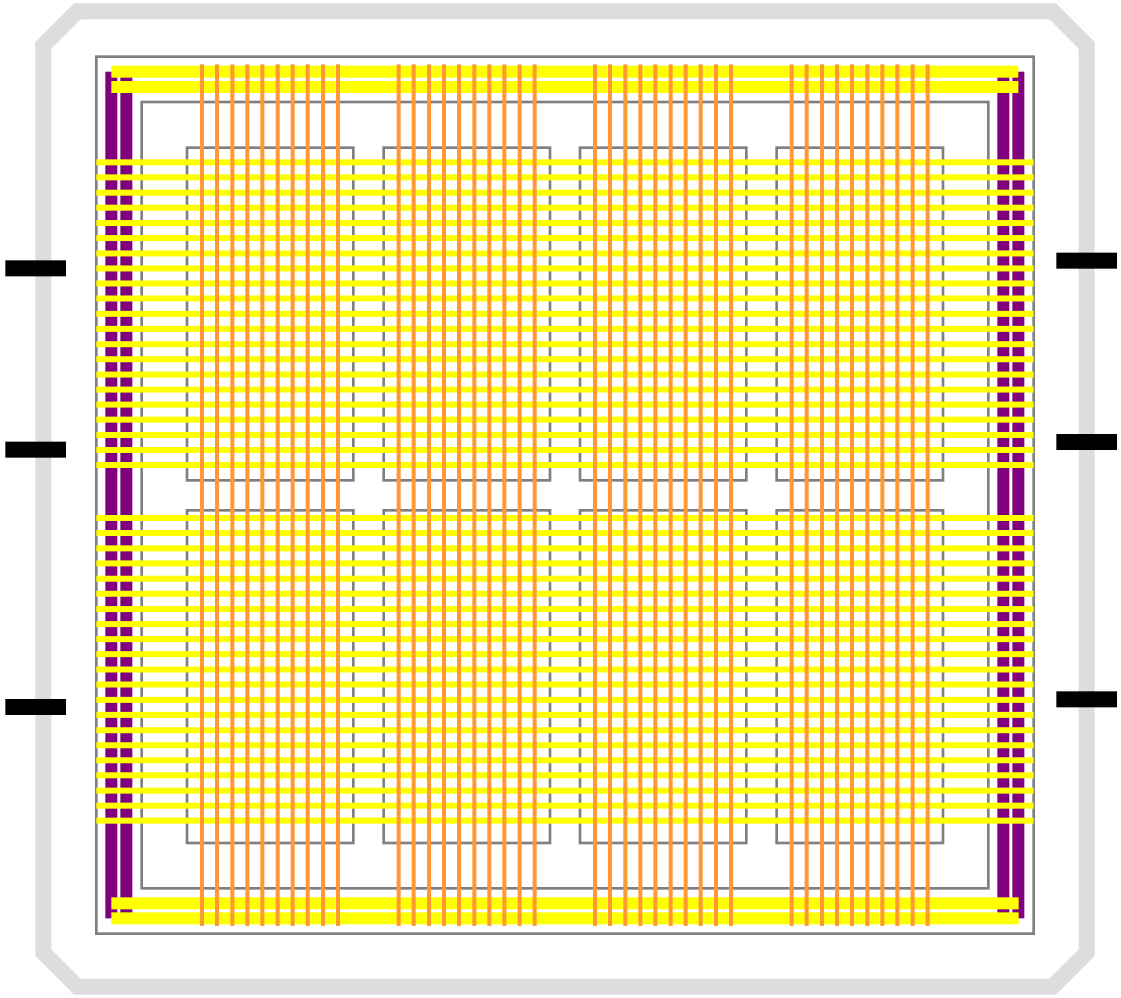
VDD1V8aco & VSS:Gaco

1.1

(new mesh)



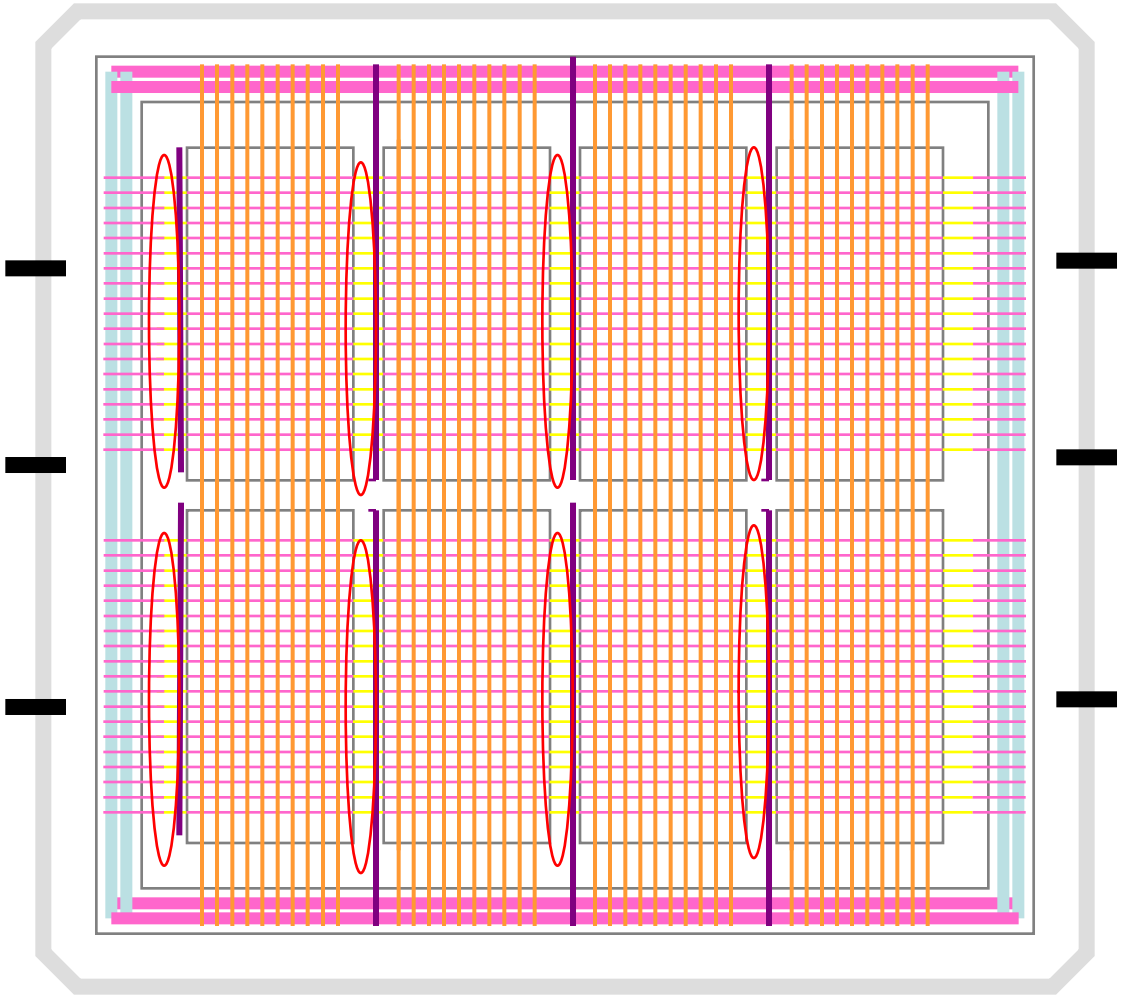
VDD1V8dco & VSS:Gdco



VDD1V8mso & VSS:Gmso

1.1

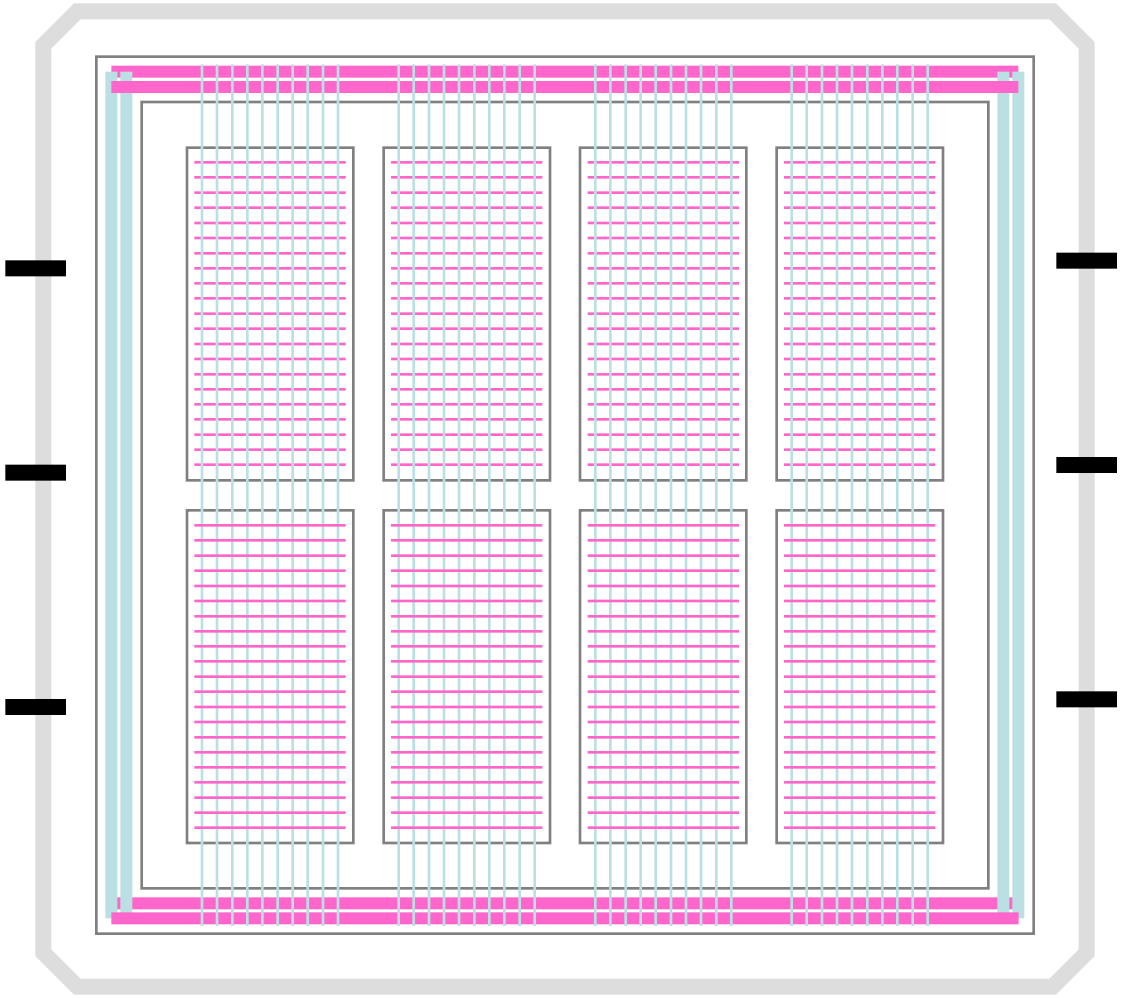
(attn!)



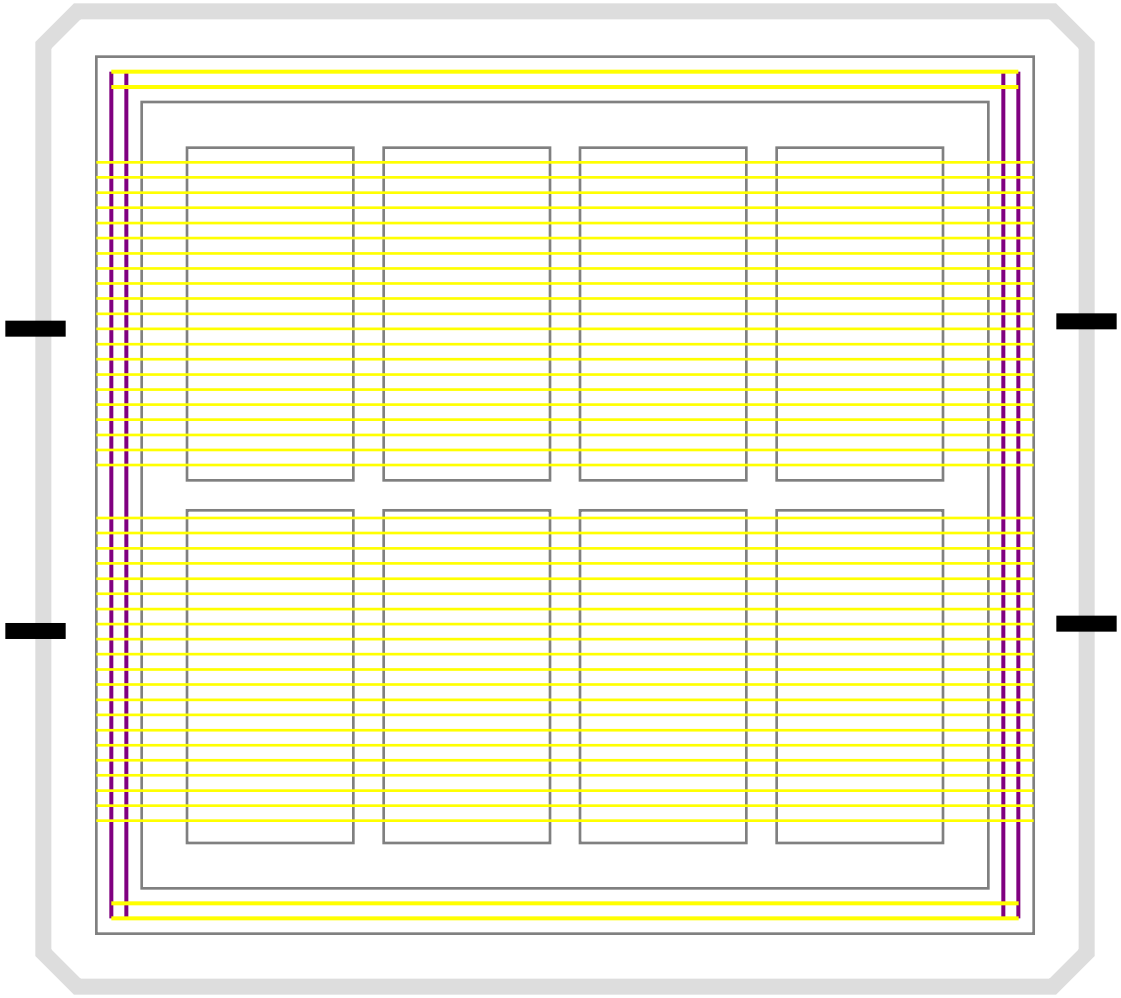
Horizontal links between sub-arrays missing!

TO DO

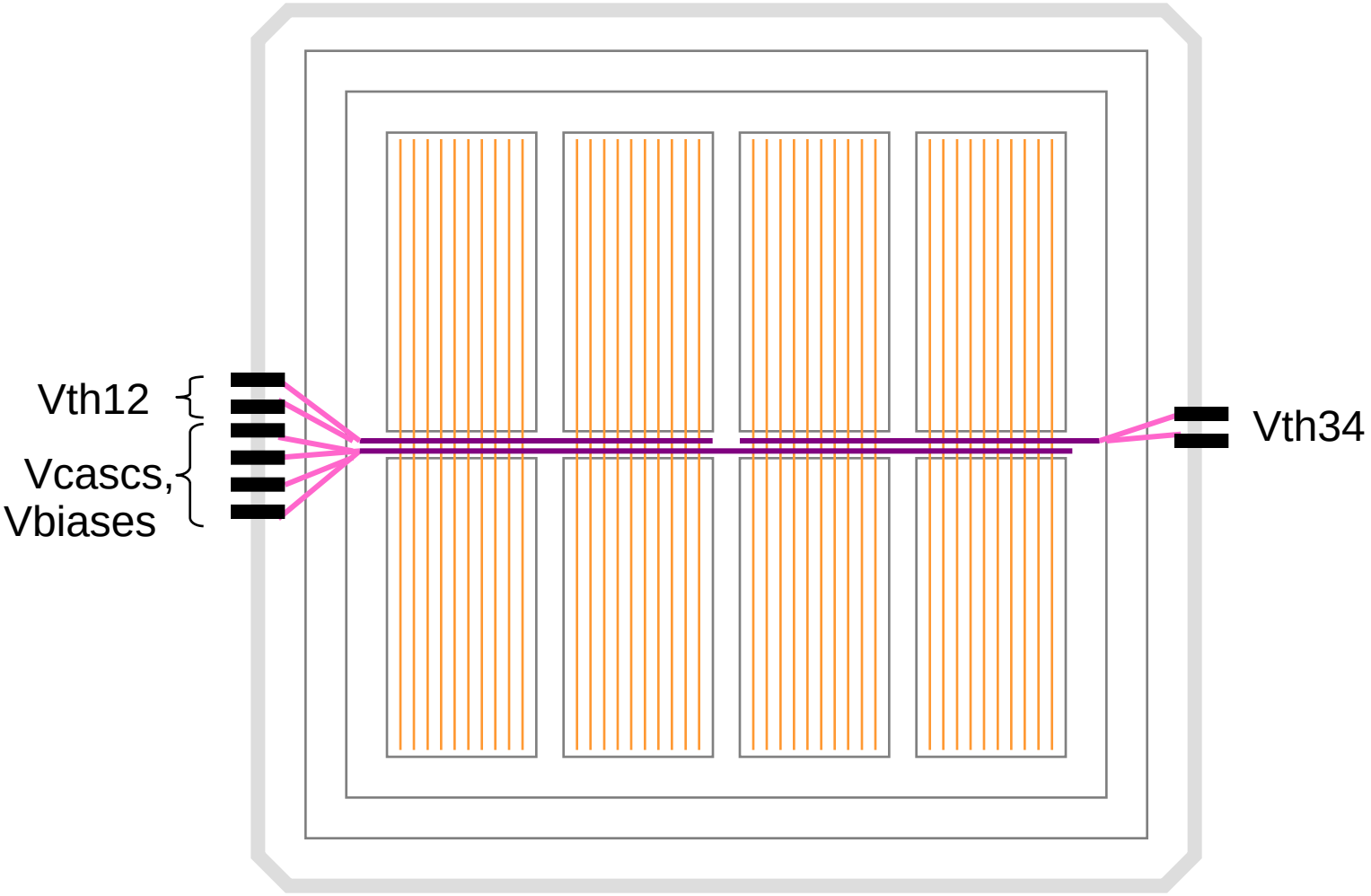
VDD1V8sram & VSS:Gsram



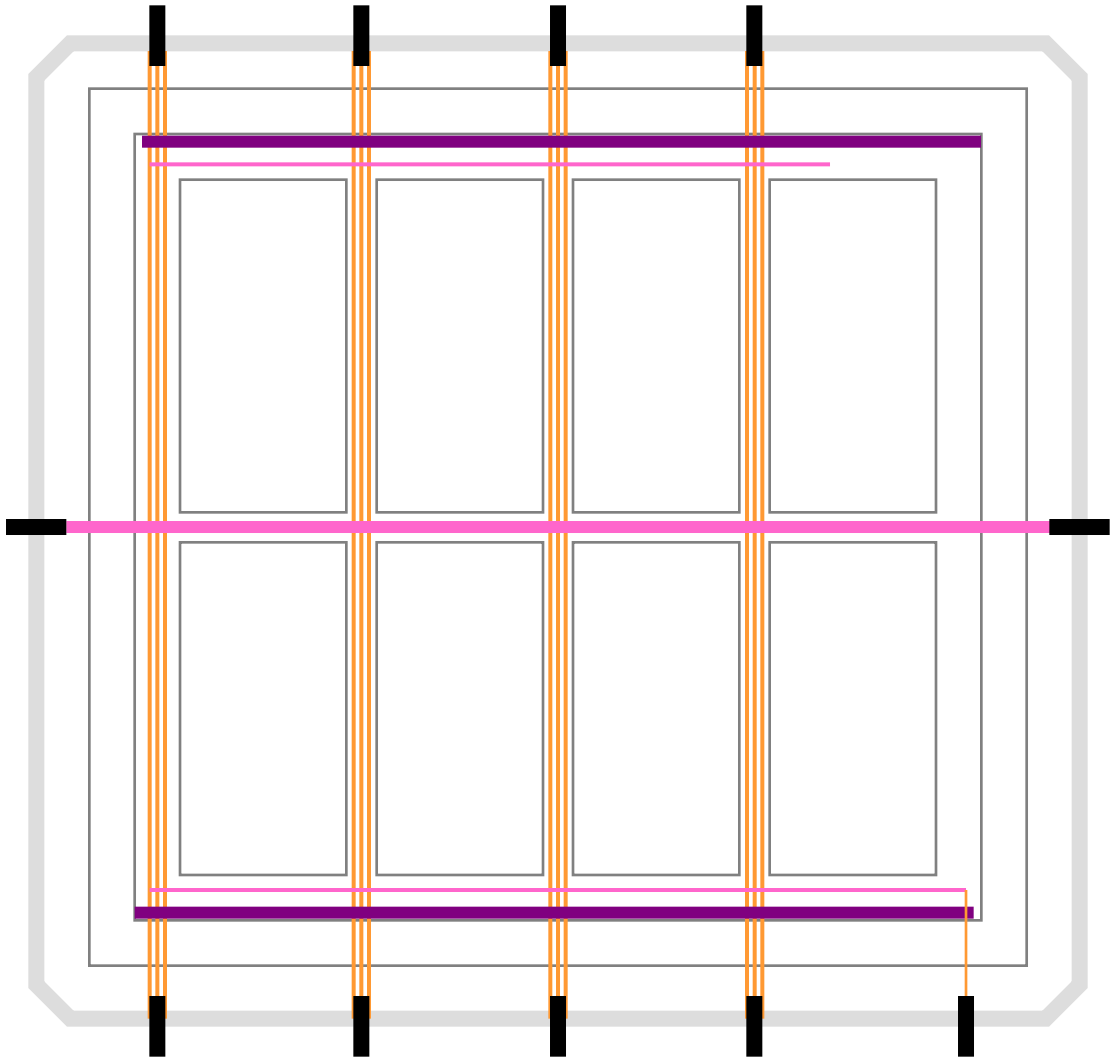
VGUARD (not yet used)



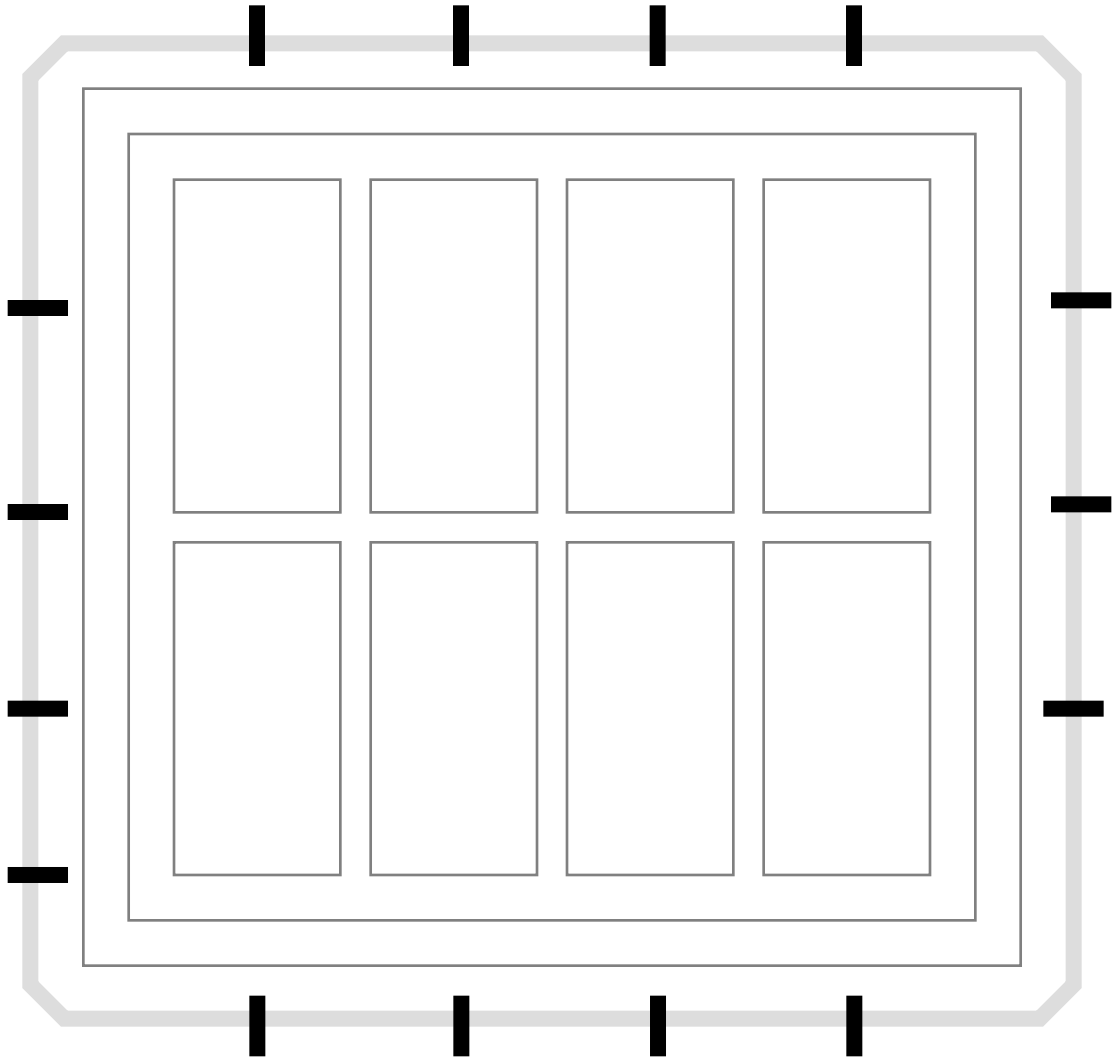
Vth(+/-) & Vcasc(s)



VDD1V8dig & VSS:Gdig



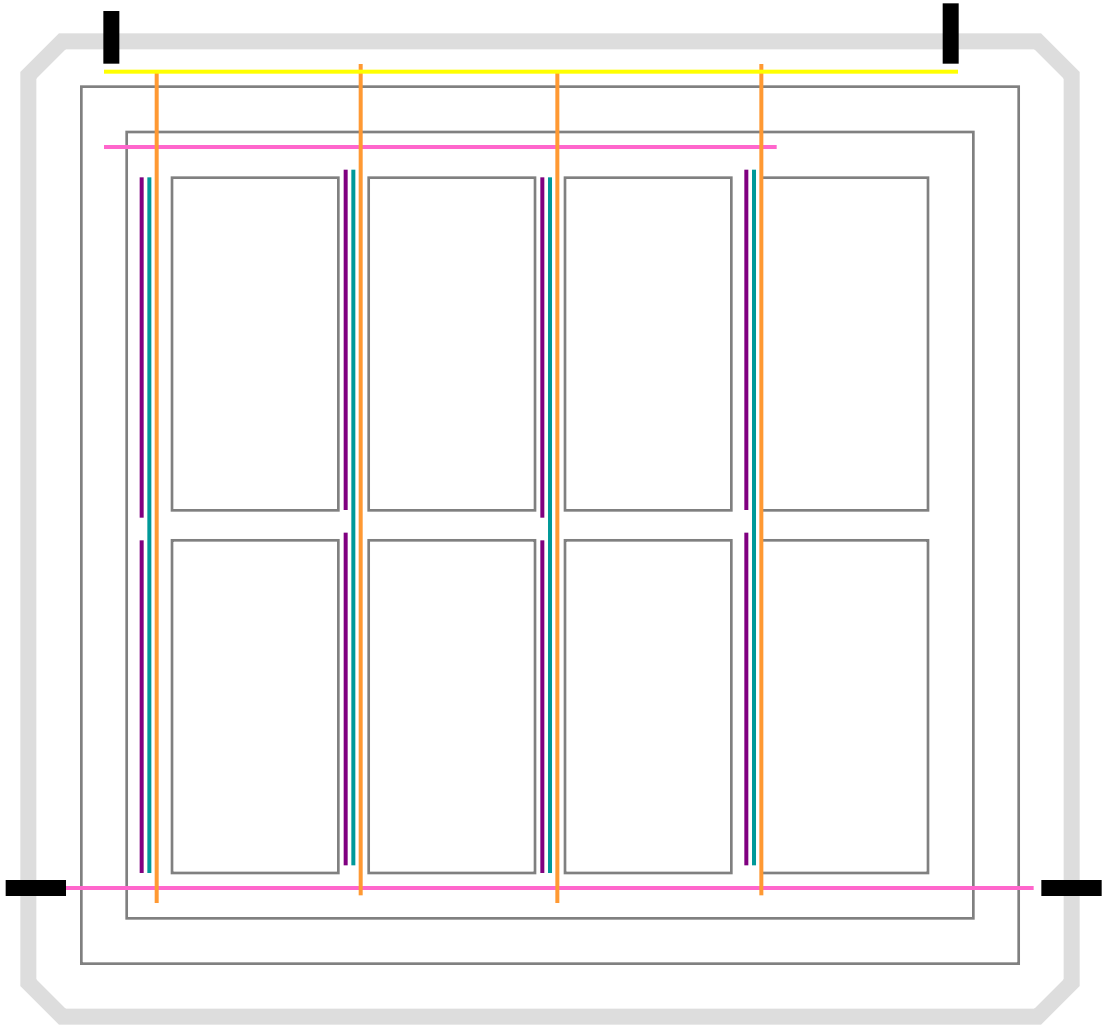
VDDO & VSSO (3.3v max)



VDD2V5dig *(=3.3v for SRAM WrEn)*

1.1

(review)



Pixel Identification