Change Request

Project	Change Request No.
MAPS for CALICE	3

Part A (to be completed by the Originator)

Description of Change Requested
Mask changes for TPAC1.2 as summarised below M2 Pixel coupling – see problem report 3 for TPAC1.1 – metal 2 should be extended to adequately shield the comparator output signal (M3) from the diode node (M1). CS Row addressing – see problem report 1 for TPAC1.1 – the "top" addressing cell should replace the duplicated "bot" address cell in the layout and schematics such that pixel rows are unique. The change to these cells implements a difference only in the CS mask

Anticipated Benefits/Reason for Change
Should restore pixel operation to ~TPAC1.0 quality so TPAC1.2 (with its other improvements, uniform array) can be used for beam tests etc. Fixing the addressing bug is convenient, and adds little to the overall cost.

Please click on the box with the most likely result of the change in each row

	Substantial Reduction	Reduction	No change	Increase	Substantial Increase
Cost				✔ 35k	
Schedule				✔	
Performance					✔
Resources			✔		
Risk			✔		

Minor effort required ~1 month to make new layouts and run GDS diff, LVS & DRC routines.

Originator		JC	
Signature		**Date**	

Approval Required in (click on box)	**1 week**	✔	**2 weeks**	☐	**1 month**	☐	**2 months**	☐

Part B (to be completed by the Project Manager)

Recommended for (click on box)		Project Manager Signature	Date
Implementation ✔	**Rejection** ☐		
Approval for Implementation		**Customer/Sponsor Signature**	**Date**
JC			

Action Required/Comments

The changes listed here will be implemented and submitted as updates to only M2 and CS masks, thus fixing problems found on TPAC1.1. The functionality and technical specification of TPAC1.2 is therefore unchanged from TPAC1.1 hence no new equivalent documentation has been generated.

These two functional changes (bug-fixes) shall be the only design changes made from TPAC1.1 to TPAC1.2.

A formal FDR will be held before submission, to review the problem report documents, their associated fixes in the design schematic and layout, and check a GDS diff analysis to ensure changes are only made to M2 and CS layers, and only in the intended circuit areas.