Problem Report

Report Number: 1

Project Name: TeraPixel APS for CALICE v1.1

Item: Row Addresses

Problem
Row address codes (evaluated by running the sensor in "override mode") are inconsistent with v1.0 V1.0 row address codes run 0→167 V1.1 row address codes run 0→83, 0→83 Therefore row address codes are not unique, leading to ambiguity in identifying locations of hit data. **Originator (Sign/Date)** Reported by: Paul Dauncey + Matt Noy, Imperial College **Project Manager (Sign/Date)**
Remedial Action
This is clearly a bug introduced into the design (confirmed in schematics and layout) caused by the copying of one pixel array (in v1.0) to the upper array (in v1.1). There is no simple fix post-manufacture (to update the design is trivial, as the addressing cell exists from v1.0) Suggested operating mode (MN) to use one memory element per row to store a false hit, thus reading every row to give non-ambiguous identification of locations of real hits → reduces the number of memory elements available to 18 per row, but is simple to implement (one fwd direction init clock before bunch train). **Project Manager (Sign/Date)**