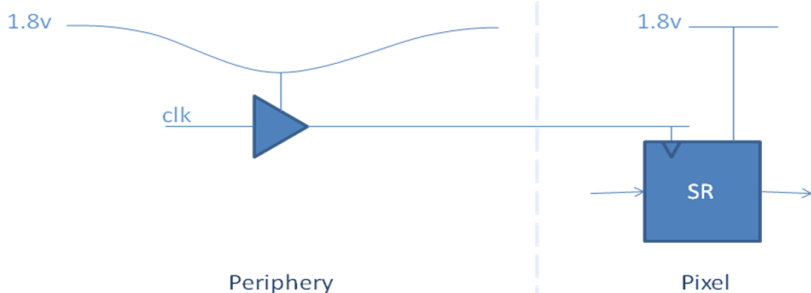


Problem Report

Report Number: 5

Project Name: TeraPixel APS for CALICE **v1.1**

Item: Configuration Registers: Power droop in buffer supplies

Problem
<ul style="list-style-type: none"> • Were reporting many errors and not holding the correct data • Problem due to different power domains and high loading of “slow” clock drivers  <p>The diagram illustrates a clock signal path between two power domains. On the left, labeled 'Periphery', a blue triangle represents a clock buffer. It is connected to a 1.8v power supply. A signal line labeled 'clk' originates from the buffer. On the right, labeled 'Pixel', a blue square represents a Shift Register (SR). It is also connected to a 1.8v power supply. A vertical dashed line separates the 'Periphery' and 'Pixel' domains. The 'clk' signal line crosses this boundary to connect to the SR register.</p>
<p>Originator (Sign/Date)</p> <p>JC</p> <p>Project Manager (Sign/Date)</p>
Remedial Action
<ul style="list-style-type: none"> • Fixed by driving one of the power domains at 1.6v (previously 1.8v) • Implemented using the power module developed for TPAC1.0 with updated resistor values and driving VDD1V8sram through J7 • Proved, reliable fix provided 2% tolerance on resistors on power module board.
<p>Project Manager (Sign/Date)</p> <p>JC</p>