Review Approval Form

Type of Review: IDR (pixel schematics)

Project Name: TeraPixel APS for CALICE

Documents Reviewed

Latest top level schematics :
PreShape simulation results document
PreSample simulation results document
Comparator simulation results document

Referred to but not explicitly reviewed:
Logic and top-level simulation results document

Attendees: JC, RT, Paul Dauncey, Nicola Guerrini, Mark Prydderch, Mike Tyndel.

Comments

Full minutes taken by Paul Dauncey, available on web at http://www.hep.ph.ic.ac.uk/calice/maps/idr1/idr1.html
PreShape pixel
Investigate offset in different traces on preshape example
Check current consumption of pixels for very large signals (amplifiers turning off might raise power rails)
Check leakage figures for the diodes
Update the documents (eg power in comparators) so they can form accurate documentation for the chip, and add page numbers
Run a simulation for power supply rejection – set the spec for the chip power supply?
Add expected parameter spread to the table of risks for pixel components
Evaluate/prove effectiveness of using two series feedback capacitors instead of one à change schematics as req
Review in-pixel resistors in same context of matching – may require two parallel resistors if small hi-poly is used.

PreSample pixel
Quantify component risks as for pre-shape
[Note: C_{in}/C_{fb} references swapped in doc pg17]
Make the feedback capacitor from two caps in series
Check AC analysis of analog circuits, phase margin etc? (also for pre-shape pixel)

It was queried whether the pixel circuits will be re-optomised when the input capacitance is known – if time is available then some quick checks can be made but no major changes would be anticipated.

Comparator
Repeat threshold-timing sim for 120mV case (only 30mV and 60mV considered)
Check transient noise with Eldo & compare with spectre results
Investigate discrepancy in the with-adjustment results (dialogue contradicts plot labelling)

Logic
There was not time to evaluate the logic parts in full details, although a top-level summary was given which yielded the following comments:
Add a parallel-load serial-output shift register to read back the mask & trim settings that were programmed – very useful for validating what was written.
Separate the "overflow" outputs for each pixel type;
Data mux and row encoder designs to be completed.

Approval: emails indicating approval are an adequate substitute for hardcopy signatures

<u>Review Report agreed</u>
Group Leader (sign/date) as required by the Project Management Plan

Customer (sign/date) as required by the Project Management Plan

Others – as stated in the Project Management Plan

<u>Review Report agreed and any changes incorporated</u>
Project Manager (sign/date) always required