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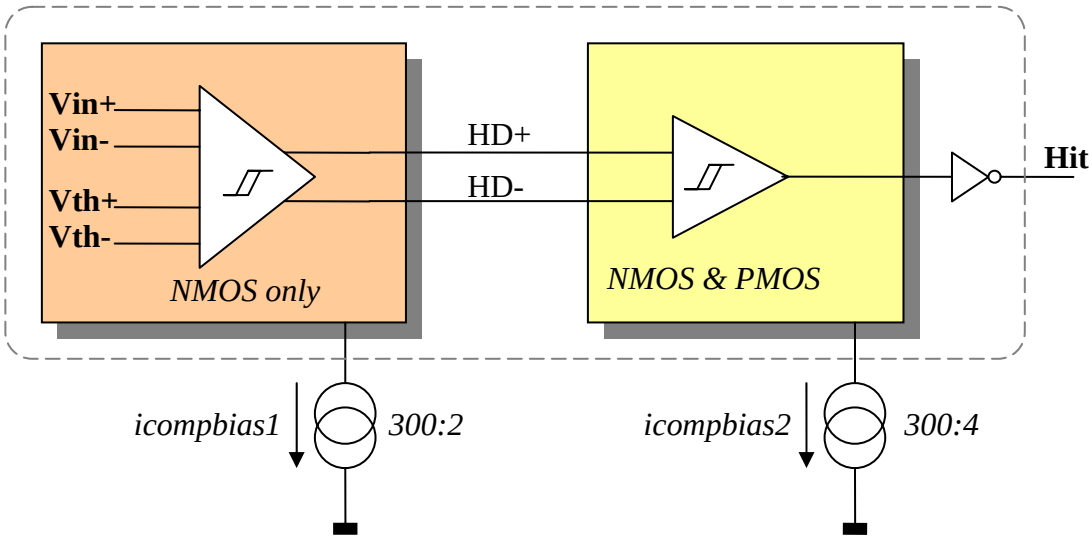
Revision History

1.0	30th November 2006	Document created

Comparator Overview

The comparator comprises two distinct parts. Originally the circuit was designed so the nmos part could be located in the pixel, and the pmos part in the control logic. The availability of a deep P-implant allows both parts to be located in the pixel thus reducing the size of the control logic, hence reducing dead area.



Two operating cases are considered, where the current in the input (nmos) stage is doubled to improve performance. These are detailed below:

icompbias1	Current in each arm	Total current in first stage	icompbias2	Current in input stage (x3)	Current in output stage (x1)	Total current (both parts)	
100uA	333nA	666nA	100uA	1uA	333nA	2.0uA	3.6uW
200uA	666nA	1.33uA	100uA	1uA	333nA	2.6uA	4.8uW

DC Operation

Note definitions of signals for these simulations are as follows:

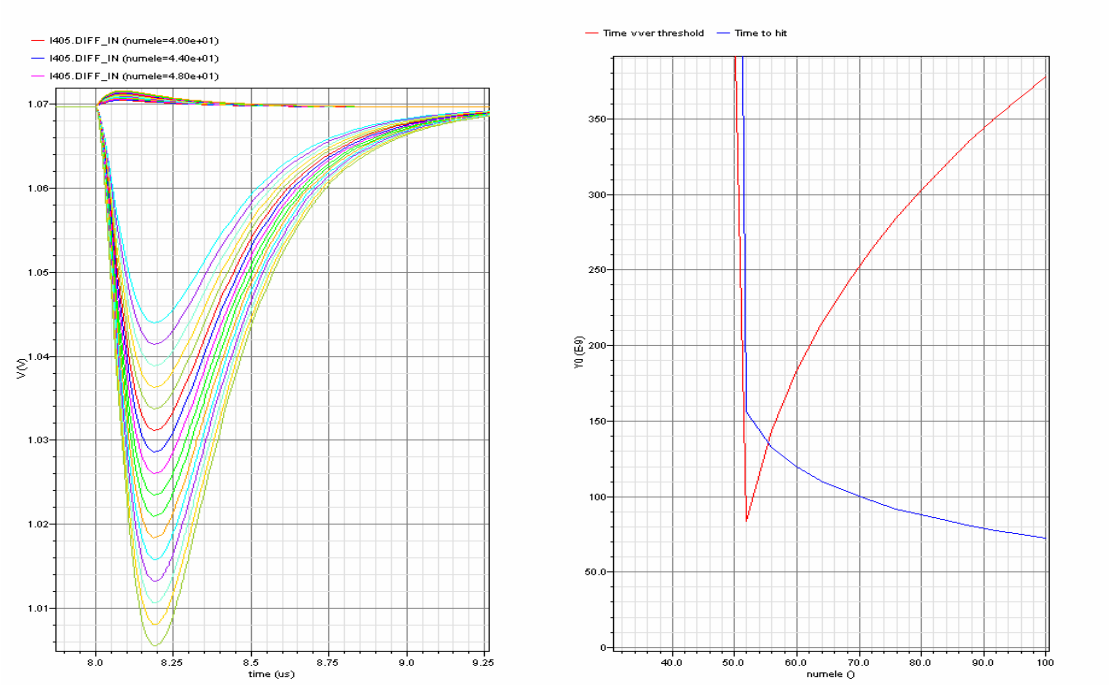
Sig = (IN-) – (IN+)
Vth = (VTH+) – (VTH-)

Input condition	Corresponding state of Differential Nodes	Comparator Output
Sig > Vth	(HD+) < (HD-)	1.8
Sig < Vth	(HD+) > (HD+)	0

Comparator input signal & desired operation

First it is useful to understand the key characteristics of the input signal the comparator will be expected to monitor, and understand the desired operation.

PreShape signal waveforms

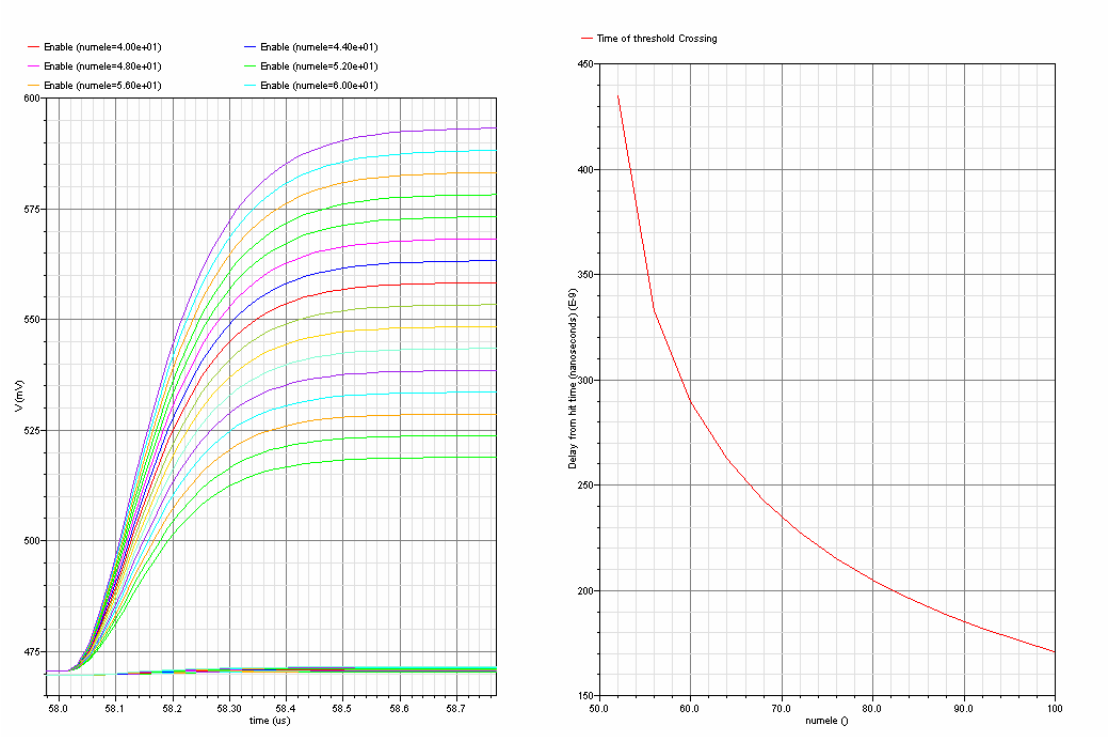


The preShape pixel analog output exhibits a signal-dependant delay between hit and the output crossing the threshold, and subsequent signal-dependant delay before the output crosses the threshold again on its return to the baseline. These two timings are shown in the right hand plot.

Ideal case

- Comparator fires when the differential signal input exceeds the differential threshold input.
- Zero (or fixed) threshold offset
- Zero threshold offset variation due to process corners & mismatch
- Zero (or fixed) delay from threshold crossing to output changing (in both positive and negative directions).
-

PreSample signal waveforms



The preSample pixel analog output exhibits a signal-dependant delay between hit and the output crossing the threshold. This timing is shown in the right hand plot.

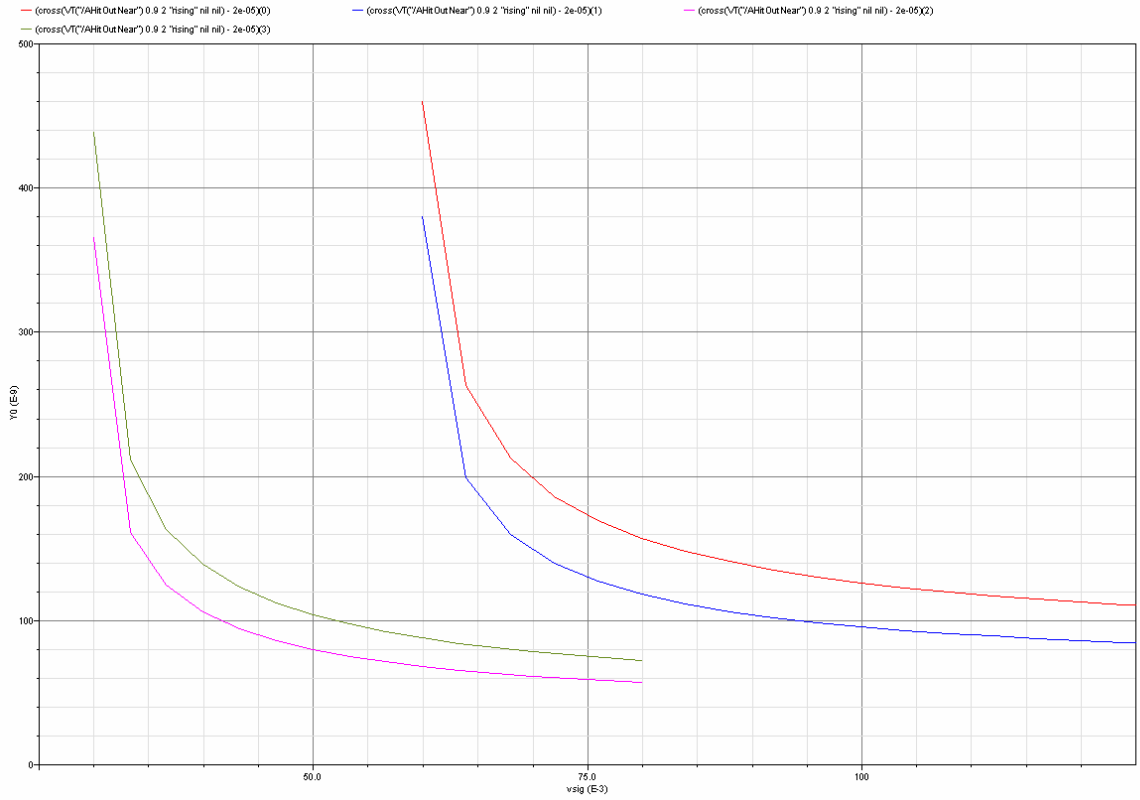
Ideal case

- Comparator fires when the differential signal input exceeds the differential threshold input.
- Zero (or fixed) threshold offset
- Zero threshold offset variation due to process corners & mismatch
- Zero (or fixed) delay from threshold crossing to output changing

Response Time

A finite time delay is expected between the inputs of the comparator changing and a corresponding change in the output. This is most critical for signals that are close to the threshold.

Results

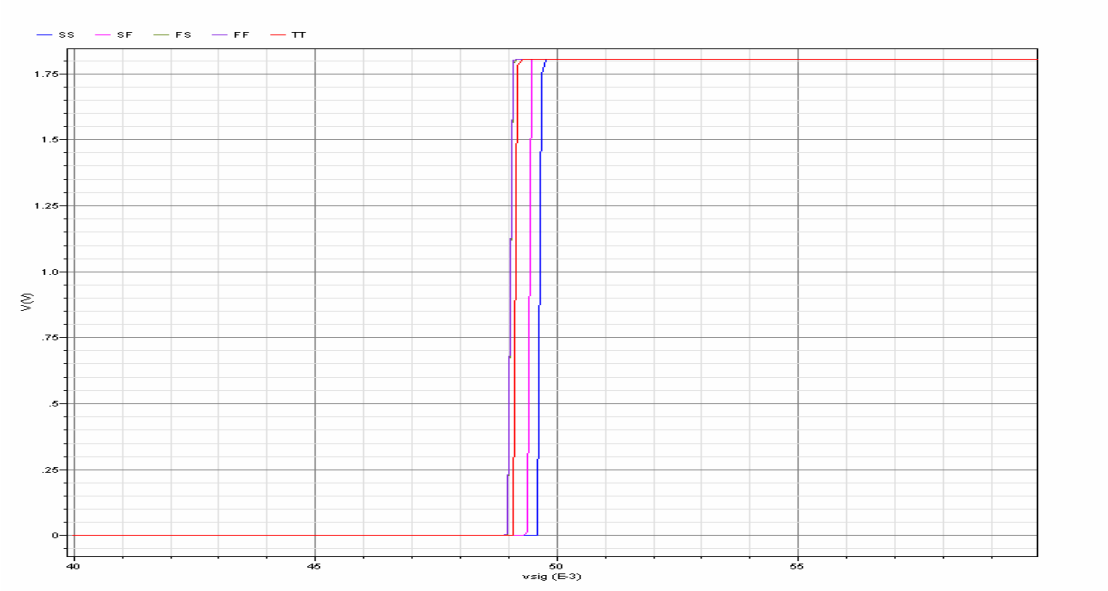


Above: Two examples are presented, one with the threshold set at 30mV, the other at 60mV. In each case a range of input signals are applied in each simulation. The time taken for the comparator output to ‘fire’ (if at all) is plotted for the higher and lower power settings.

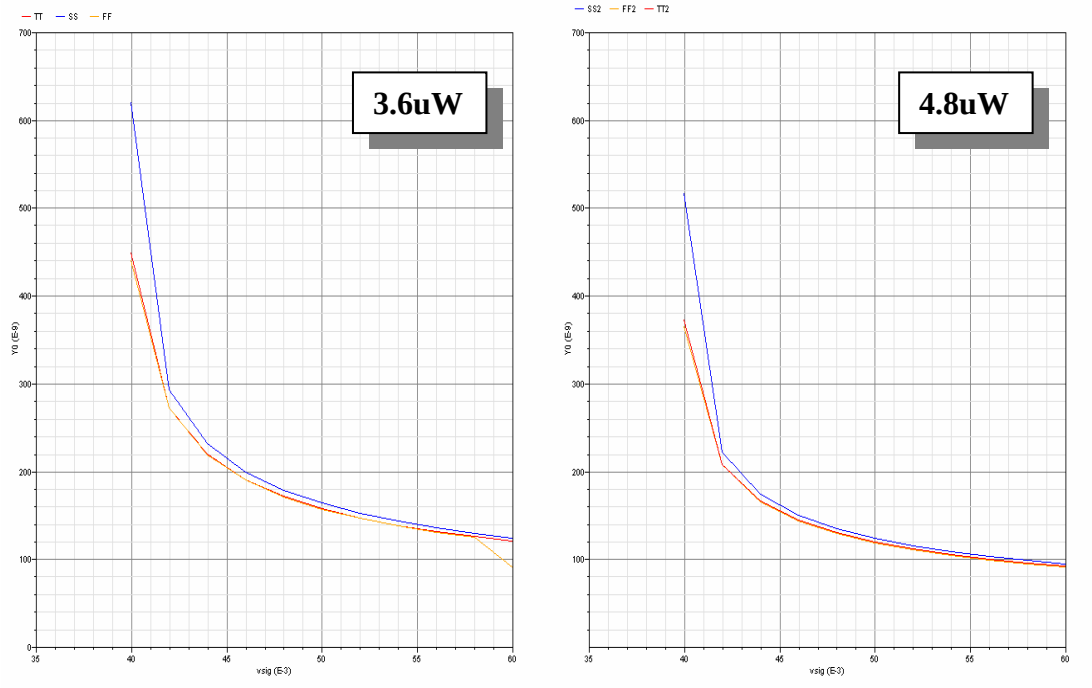
Process Variations

DC and transient performance are checked in the process corners.

Results

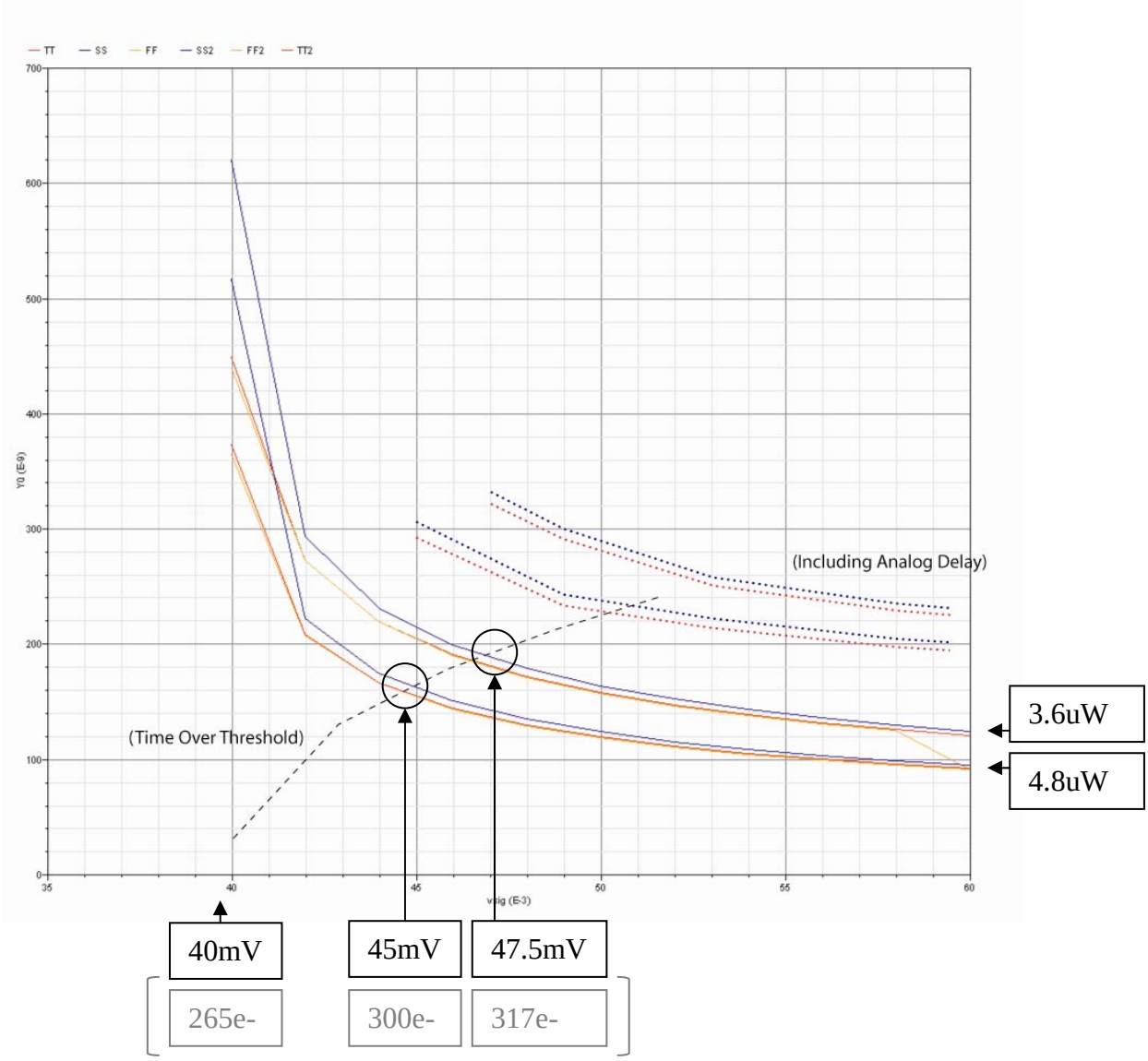


Above: DC analysis in process corners. 50mV threshold yields a mean switching point of 49.3mV with a standard deviation of 0.27mV.



Above: Transient performance in process corners differs around the threshold but is otherwise consistent. 40mV threshold is simulated in these cases. (see also below).

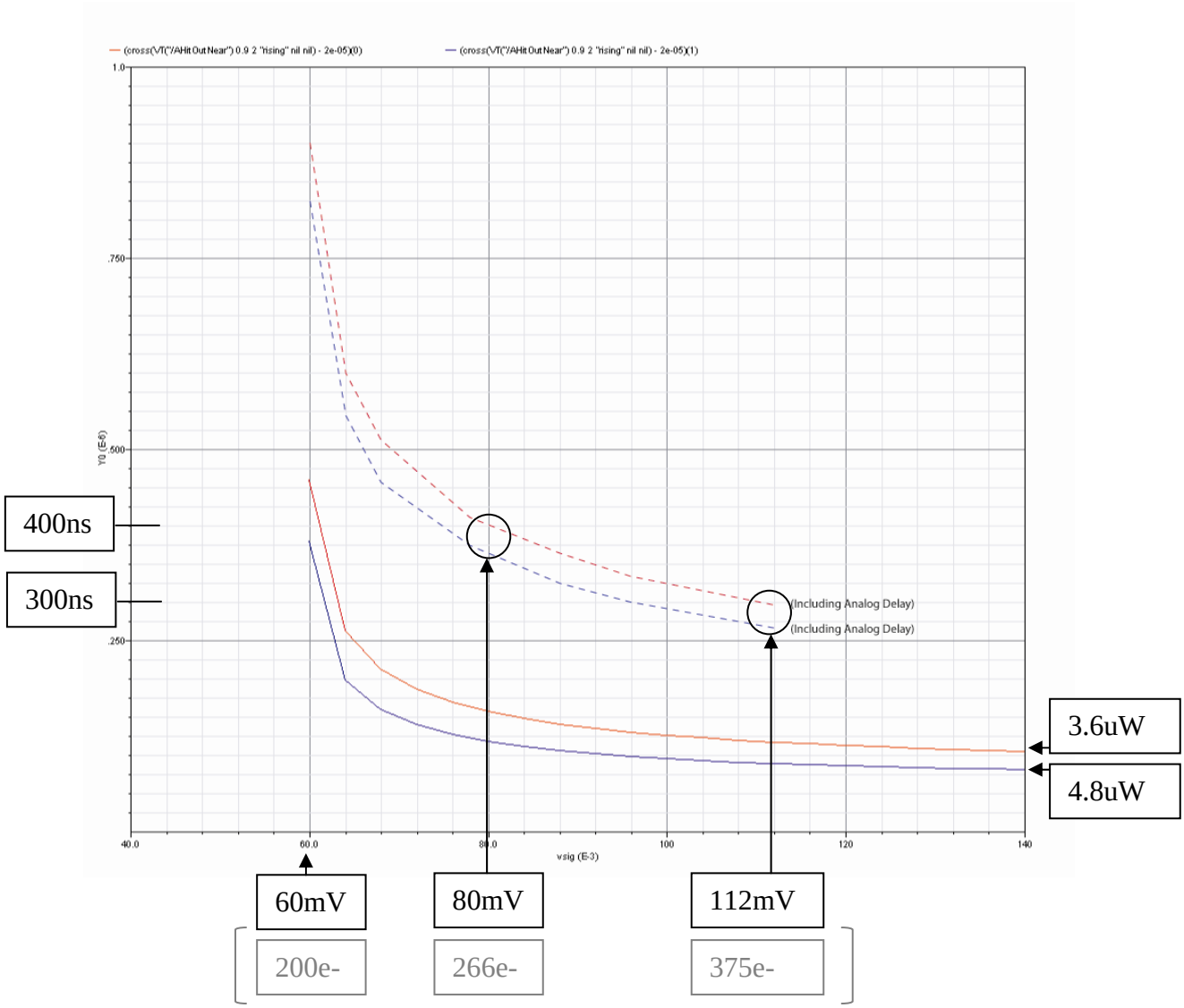
Realistic Operation (PreShape pixel)



Above: The (Vth=40mV) transient performance is compared with the analog performance of the PreShape analog circuits. For very small input signals around the threshold, the shaper output is only above threshold for a short time. Where this time is less than the response time of the comparator, it will not register the hit. Therefore the above graph indicates the "real" threshold is likely to be 5-8mV higher than that set from off-chip. Signals that do register will be subject to the additional analog delay with respect to the moment the hit occurred – this is also estimated with the dotted lines.

In one regard this is convenient, since it eliminates the widening variation between comparator response times to very small signals, and ensures we are operating in a region where process corner variations do not play a significant role.

Realistic Operation (PreSample pixel)

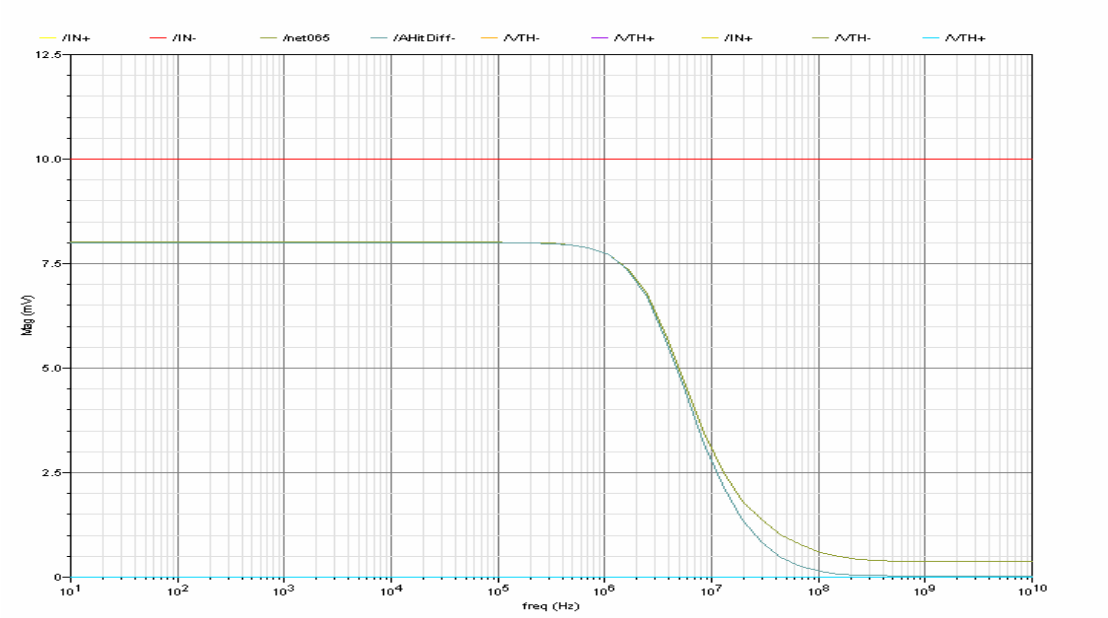


Above: Typical delay for the comparator (Vth=60mV) is plotted from simulation. Manually added to this is the corresponding delay between the Hit and the shaper output crossing the 60mV threshold. This gives a realistic indication of the delay from the hit incident to the hit flag rising.

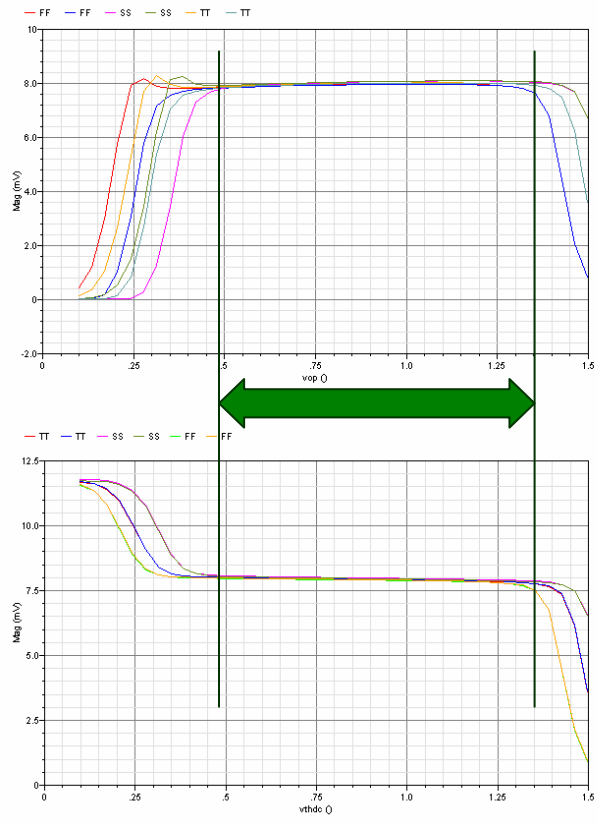
AC Analysis

The first comparator is considered as a low gain differential amplifier. The threshold inputs are tied to the same DC point (vthdc). The signal inputs are biased at the same DC point (vop) and a 10mV analog signal is applied to the negative signal node.

Results



Above: The two differential outputs each show an 8mV magnitude output in the flat region. Since the input is applied to only one of the differential input nodes, and the two outputs considered as differential, this is effectively a differential signal gain of 16/10 = 1.6. This gain is unaffected by process corners.



Left: The dc point for the signal and the threshold are swept across the full supply range to check the valid operating region for this comparator/amplifier in three process corners.

The safe DC operating region for the comparator lies between 0.5 and 1.35v.

Noise Analysis

The internal differential nodes between the first and second comparator stages must be checked for noise since they follow a low gain amplifier.

Results

- Positive differential node with respect to ground:

```
Device        Param    Noise Contribution    % Of Total
/I165/M23     id       0.000876738           34.62
/I165/M33     id       0.000796271           28.56
/I165/M34     id       0.00056442            14.35

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.00149004
Total Input Referred Noise = 0.00909199
The above noise summary info is for noise data
```

- Negative differential node with respect to ground:

```
Device        Param    Noise Contribution    % Of Total
/I165/M33     id       0.0010014             36.23
/I165/M23     id       0.000921937           30.70
/I165/M24     id       0.000617032           13.75

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.00166381
Total Input Referred Noise = 0.00963205
The above noise summary info is for noise data
```

- Negative differential node with respect to Positive differential node:

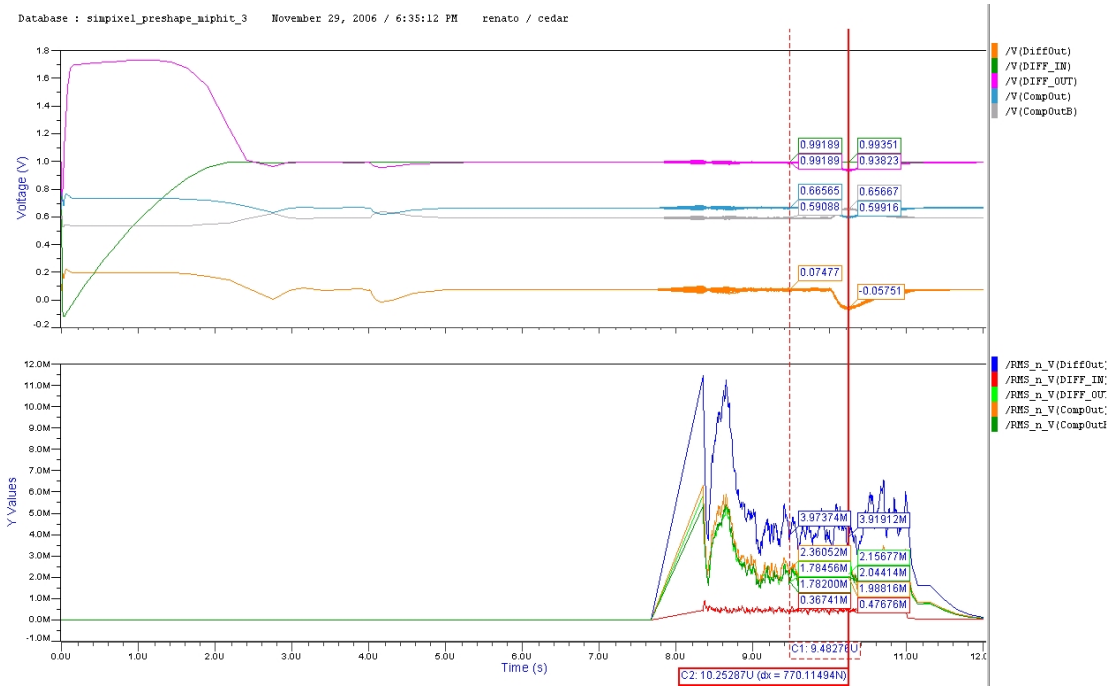
```
Device        Param    Noise Contribution    % Of Total
/I165/M33     id       0.00176424            38.82
/I165/M23     id       0.0017393             37.73
/I165/M24     id       0.00093149            10.82

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Output Noise = 0.00283161
Total Input Referred Noise = 1.27669
The above noise summary info is for noise data
```

Referring the differential noise back to the input this implies an additional 1.75mV is added to the signal at this point;

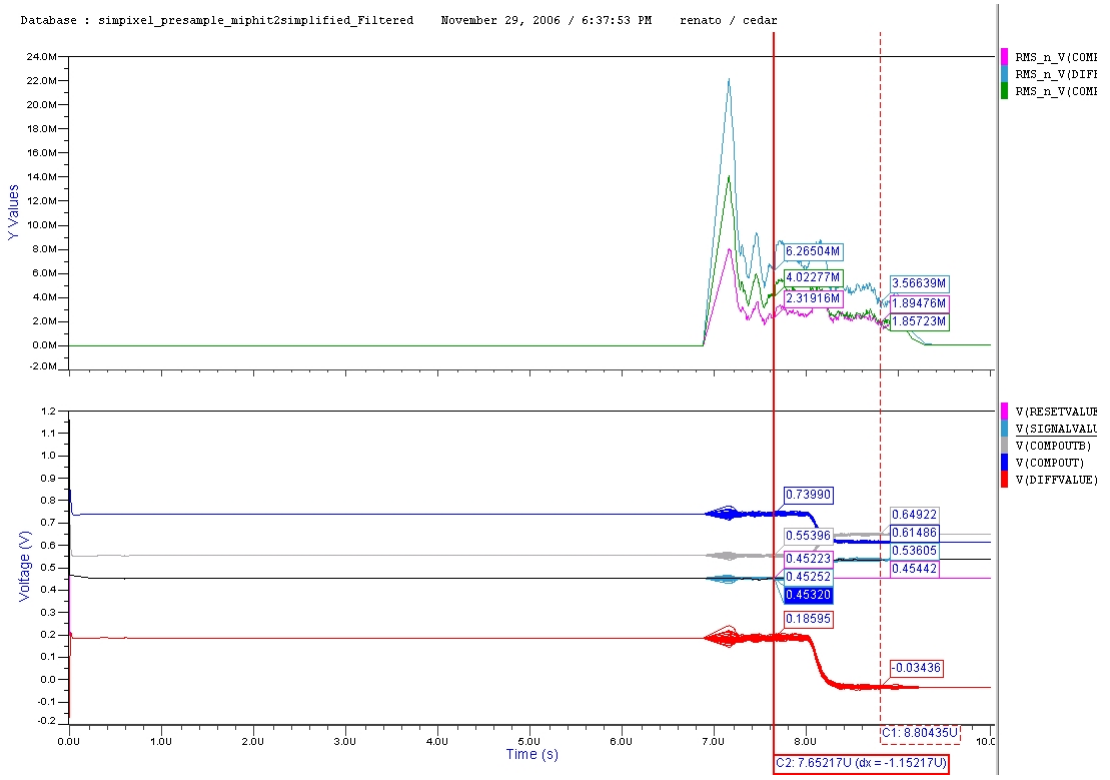
- For the preShape pixel this is ~11.6e- additional noise referred to the doide
- For the preSample pixel this is ~6e- additional noise referred to the doide

TO BE CHECKED WITH ELDO

Eldo Noise Simulations

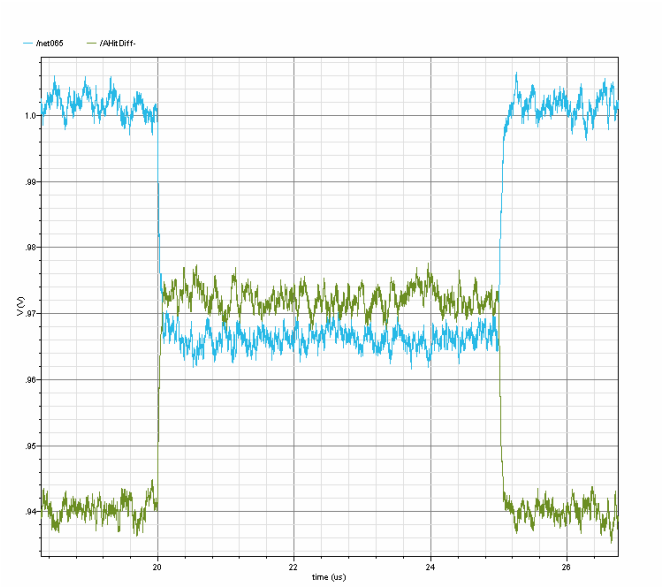


Above: The preShape pixel: ~4mV noise



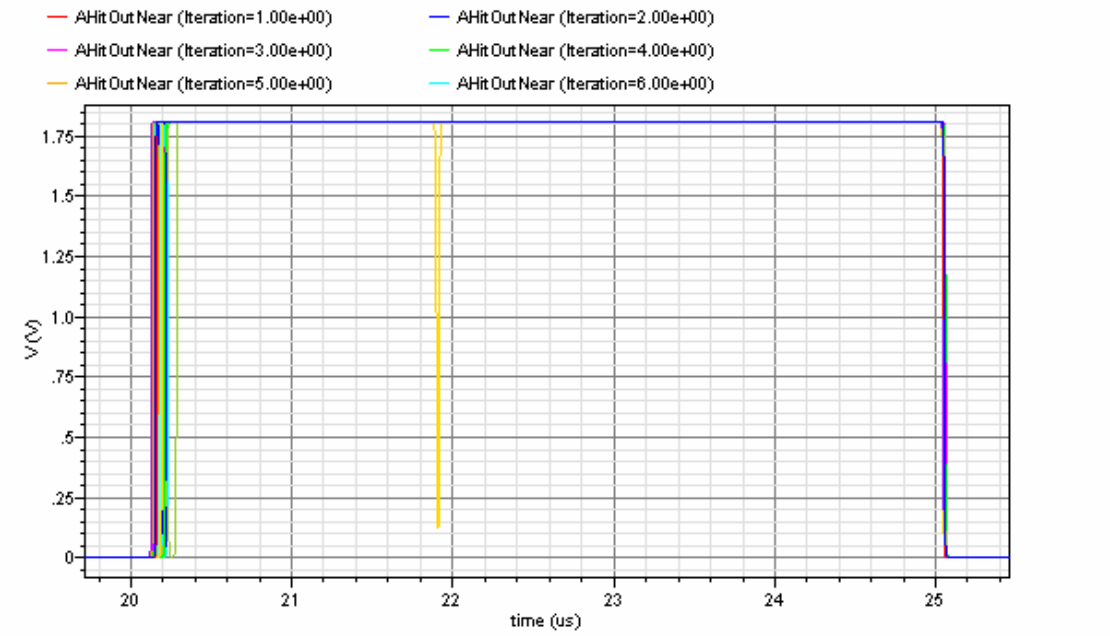
Above: The preSample pixel: ~6.2mV noise

Transient Noise Results



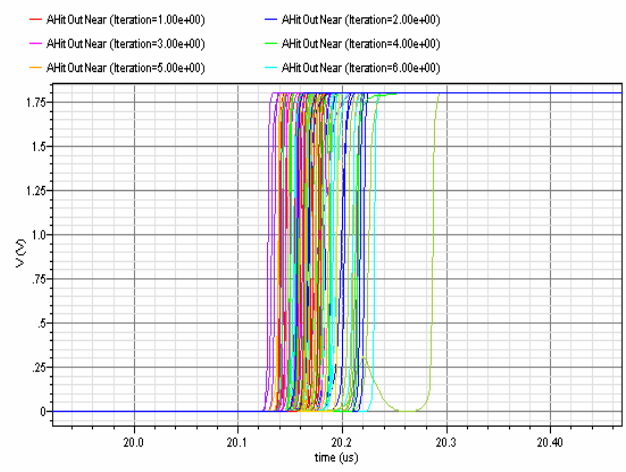
The comparator is simulated with transient noise. The threshold is set to 30mV, and a signal of 33mV is applied between 20us and 25us.

Left: The internal differential nodes between the two parts of the comparator.



Above: Comparator output in 100 transient noise simulations for the case Vth=30mV, Vsig = 33mV. In just one run the noise causes the comparator output to momentarily flip from the correct “hit” status.

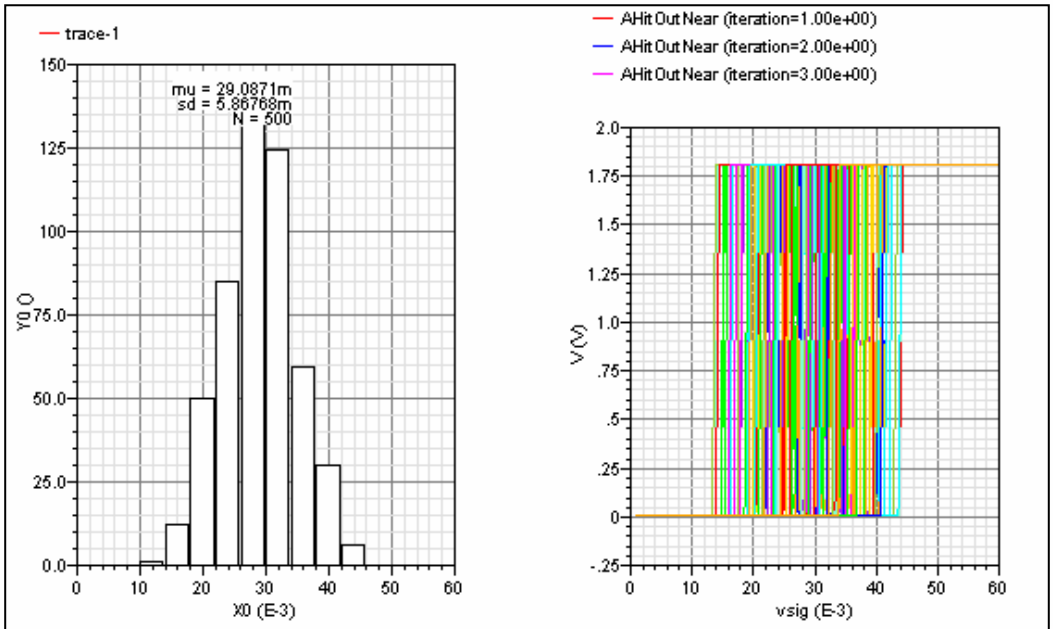
Right: Rising edge detail: Spread ~100ns.



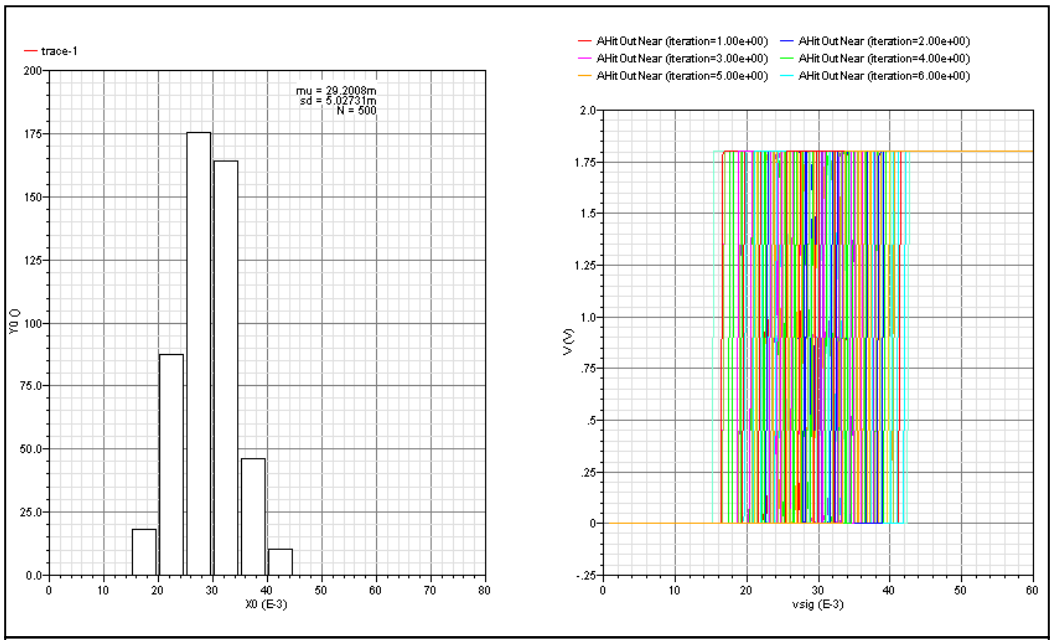
Mismatch

The threshold is set to 30mV. The DC analysis sweeps the differential input signal from 1 to 60mV during 500 Monte Carlo mismatch simulations.

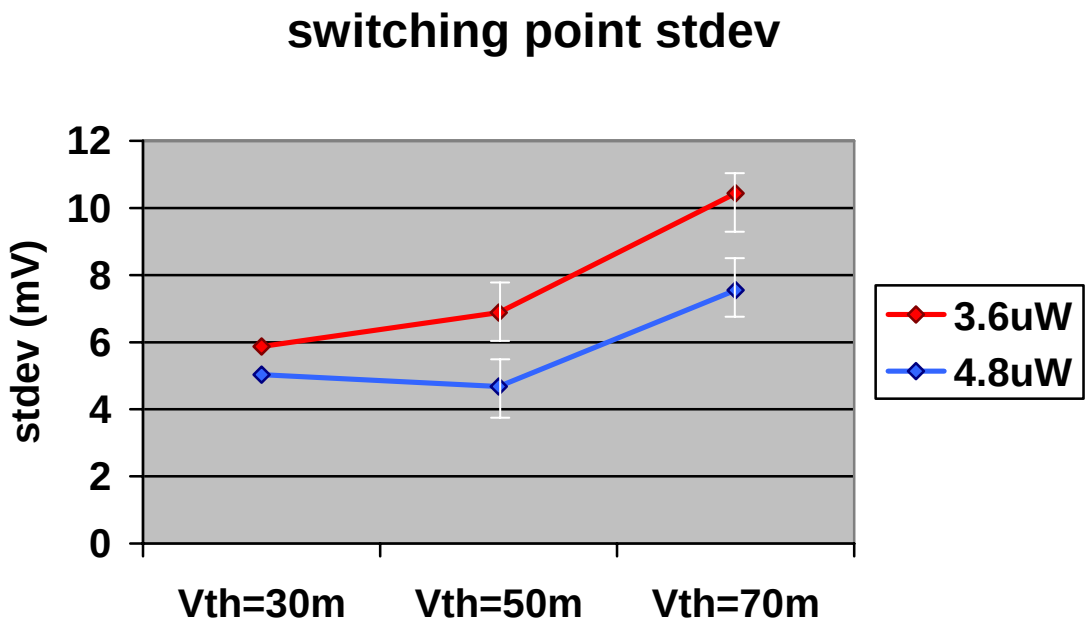
Results



(icompbias1 = 100uA) → 0.66uA in-pixel
(icompbias2 = 100uA) → 1.33uA in-pixel → 2.0uA total → **3.6uW**



(icompbias1 = 200uA) → 1.33uA in-pixel
(icompbias2 = 100uA) → 1.33uA in-pixel → 2.6uA total → **4.8uW**



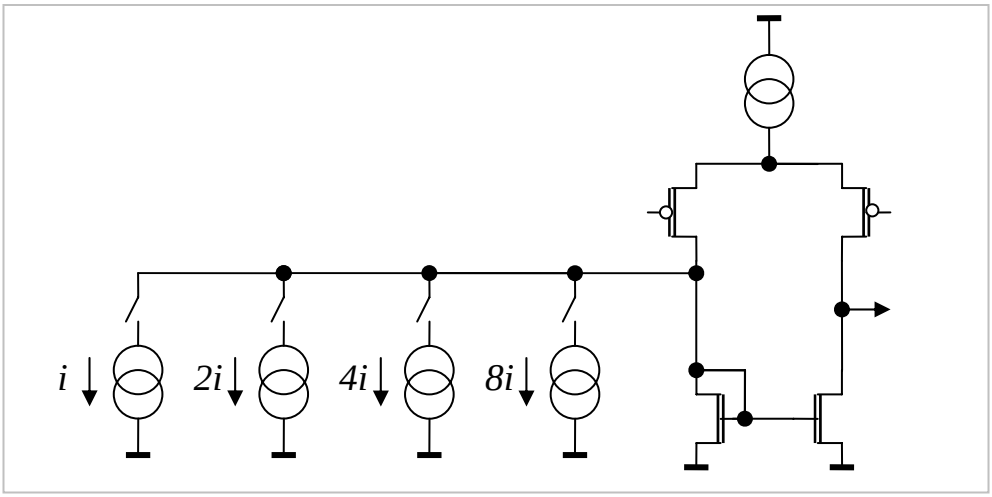
Above: Two further pairs of Monte Carlo simulations are run for higher thresholds of 50mV and 70mV. The standard deviations of the threshold in these new conditions are plotted with those from above.

The 50m and 70m cases were run for 100 iterations, whilst the 30m case was run for 500 iterations.

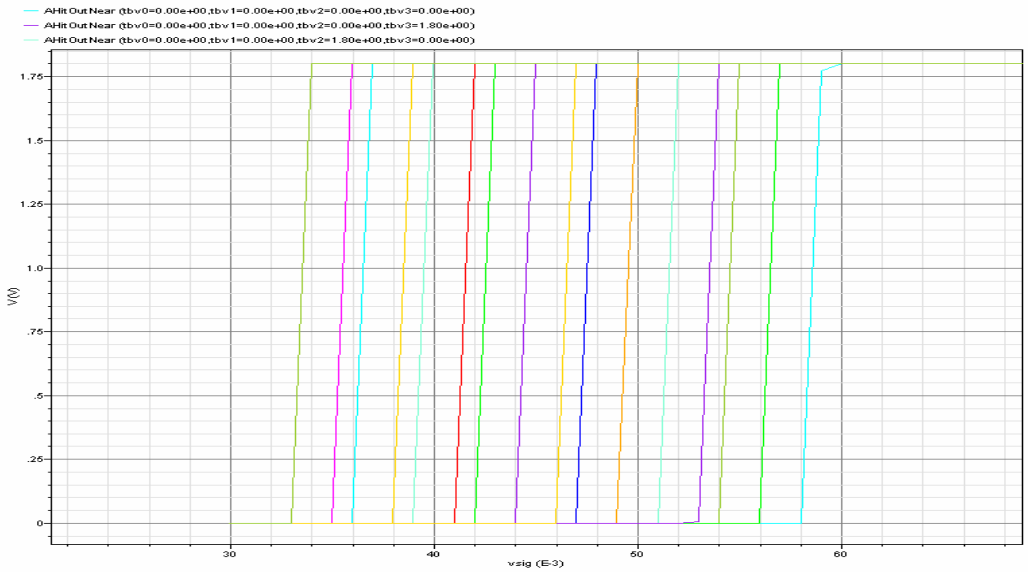
Threshold Adjustment

The mismatch simulations suggest the comparator threshold matching is unlikely to give the accuracy required. To address this issue, per-pixel threshold trimming can be added for programming during setup.

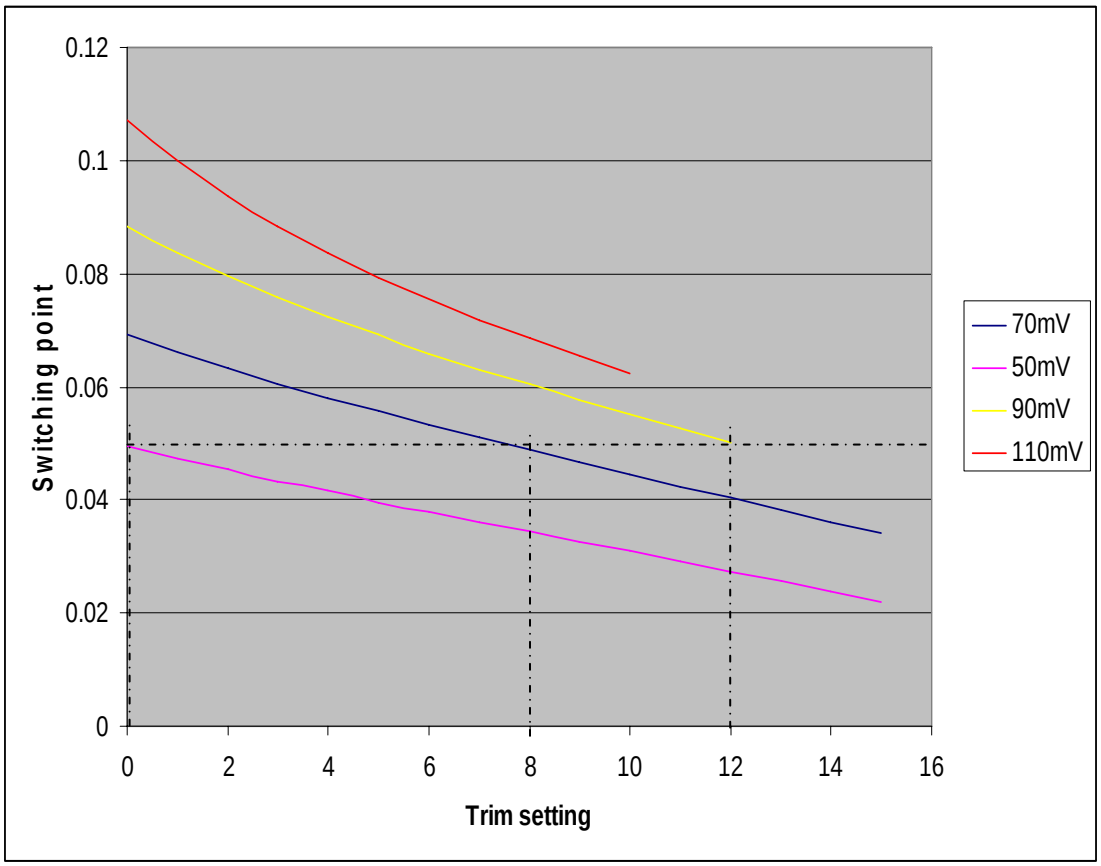
The pixel trim is achieved by applying a small imbalance in the currents flowing in the two arms of the comparator differential pair. N switches allow N mirror devices to be selected in any of 2^N combinations. The mirrors are weighted such that 1x, 2x, 4x and 8x currents can be combined to give 16 monotonic steps. The effective voltage range across which these 16 steps are available can be adjusted off-chip by means of a bias current setting.



The threshold adjustment is applied in one direction only (ie to reduce the switching point), so in general the global threshold will be set higher than desired, and each pixel adjusted downwards to the correct switching point.



Above: Example DC sweep for the comparator in each of the 16 trim settings. The threshold is set to 60mV; the trim settings allow ~20mV threshold adjustment in this case.



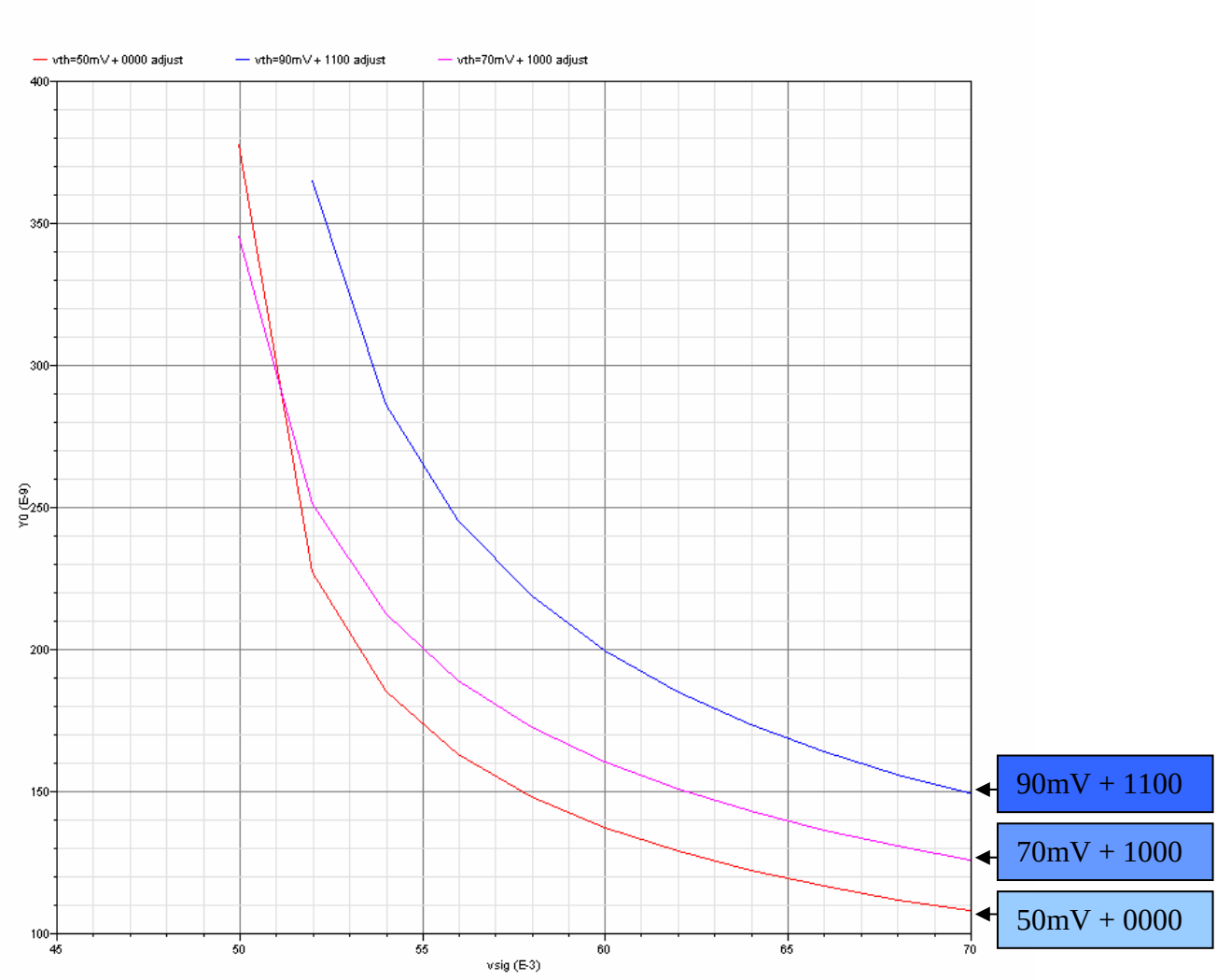
Above: Collated results from DC sweeps. Four sweeps are performed with the global threshold set to 50, 70, 90 and 110mV. In each case, all of the trim codes are tested to determine the actual DC switching point. The dashed lines indicate how the threshold 50mV can be achieved with different degrees of global threshold and local adjustment. These are the points checked for timing in the next section.

Response Time with Trim settings

As the trim circuit effectively ‘steals’ current from the comparator circuit it is worth checking how the switching response time is affected. Three cases are considered:

Global Vth	Trim setting	Trim bias	Effective Vth
50mV	0000	512nA	50mV
70mV	1000	512nA	50mV
90mV	1100	512nA	50mV

Results

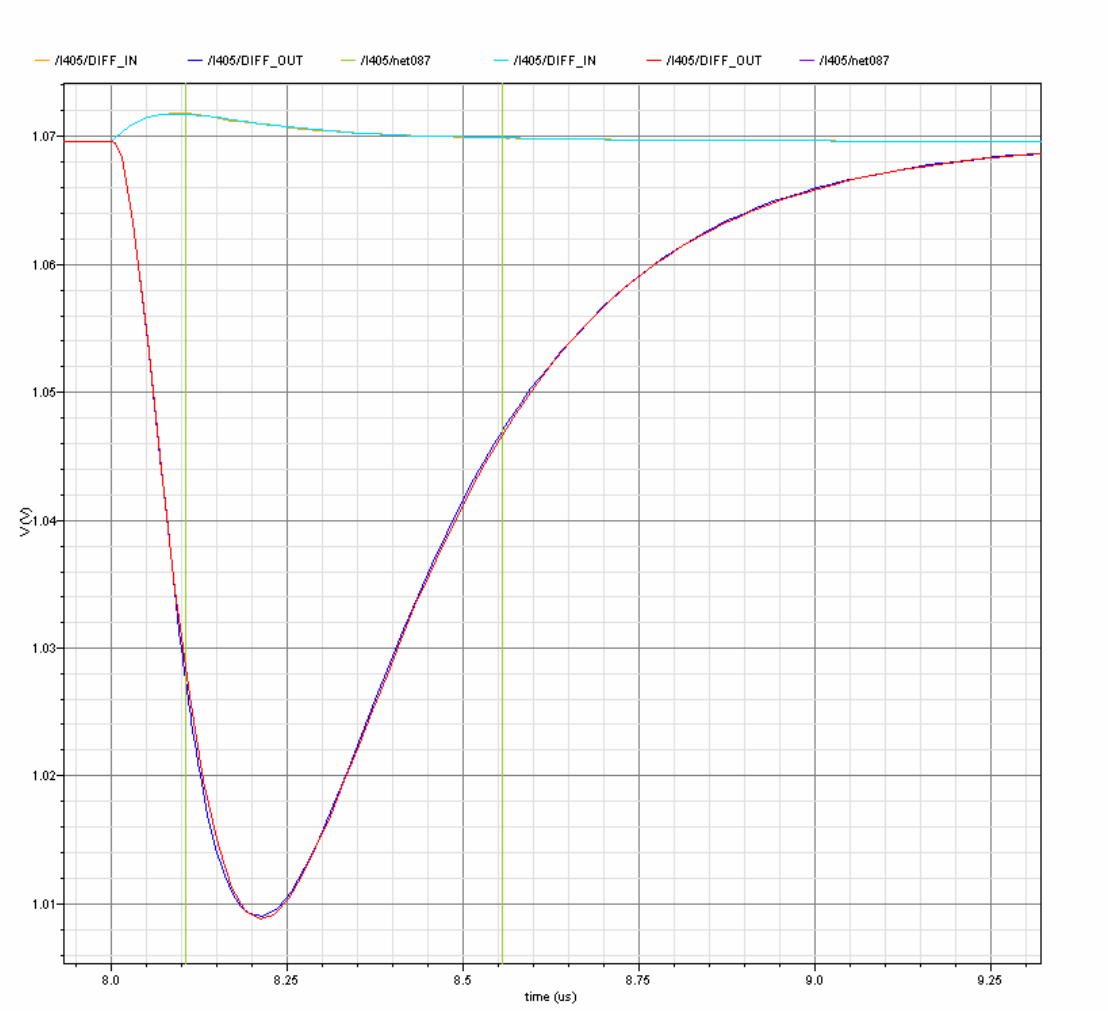


Above: Response curves for the three cases are plotted together. The profile of the curves are similar, although the [70mV+1000] case looks to yield a threshold of 52mV rather than 50mV.

Feedback onto input nodes

Some of the comparator designs investigated were noted to cause significant disturbance to the input signal when the comparator fires (capacitive coupling via input transistors). This is an undesirable behaviour since it distorts the input signal, and also the global threshold which might disturb other pixels. To check for these effects the comparator it attached to the analog signal chain from the two pixel designs. Small incident signals are simulated with the threshold set at 50% and the threshold at 200%. The difference between the analog signal in these two conditions should indicate the degree of disturbance the input and threshold node will expereicne when the comparator 'fires'.

Results



Above: Shaper output pulse for 400e- input with and without the comparator firing is almost identical.