Tera-Pixel APS for CALICE

ASIC1 Technical Specification

Document Revision 0.4

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	Name	Signature	Date
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1. TABLE OF CONTENTS

2. TABLE OF INITIAL REQUIREMENTS

This section contains a tabulated version of the initial requirements document provided at the very start of the feasibility study. These requirements form a good introduction to the overall project goals.

2.1 ILC accelerator worst case assumptions

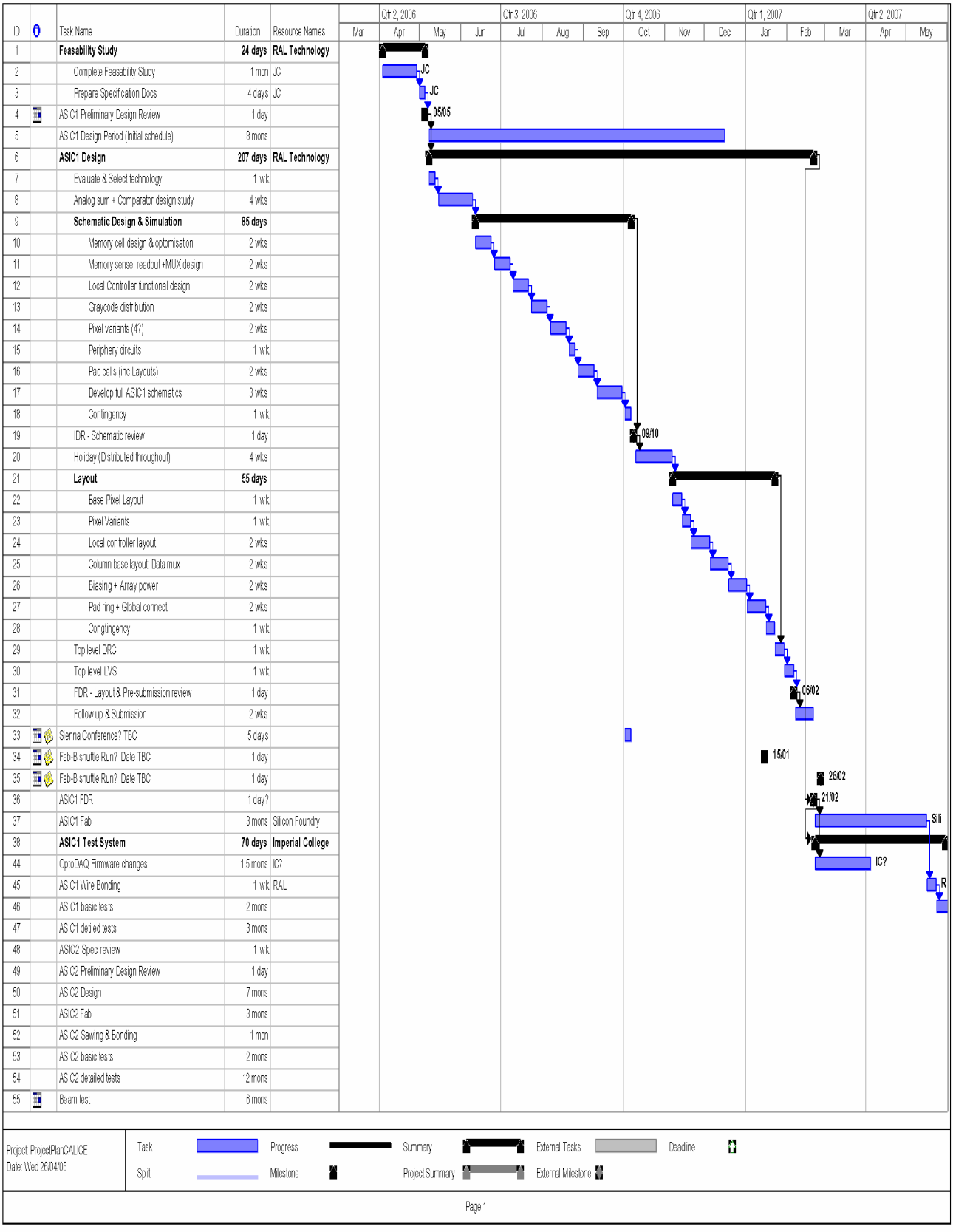
Beam crossing period	150ns, so rate = 6.7MHz
Number of crossings per train	14000, so length ~ 2ms
Train repetition rate	10Hz, so period = 100ms , duty factor = 2%
Luminosity	$5\times10^{34}/cm^2/s$, integrated luminosity per train = 5/nb

2.2 MAPS Requirements

Pixel response	The pixels must give one hit per charged particle crossing the sensor. This is of course impossible in practise but is the ideal we should aim to be close to
Maximum inefficiency (defined as one particle giving no hit)	5% within pixel (also see below).
Maximum crosstalk (defined as one particle giving two hits)	5% (?) within pixel.
Maximum noise hit rate	10^{-5}, target rate 10^{-6}. The noise rate must be insensitive to expected temperature changes (TBD).
Maximum dead space	10%. Working assumption is that basic sensor structure is $2\times2cm^2$ with a 250μm contact pad strip around the outside. This gives 5% dead space; the other 5% is random dead areas over the pixels (bad pixels, non-sensitive n-well areas, etc), as above.
Pixel size	Minimum size $20\times20\mu m^2$, maximum size $60\times60\mu m^2$.
Comparator	The comparator/storage cycle time must occur within 100ns of a trigger signal.
	The trigger should be able to come a minimum of 50ns after the particles cross the sensor

	The comparator threshold must be set/trimmed by on-sensor DAC. The DAC should be common to multiple pixels, which are therefore required to be uniform
	The threshold setting must be insensitive to expected temperature changes
Working assumptions	Triggers will have minimum spacing of 150ns but could be arbitrary times apart (many seconds for cosmics).
	Worsening the time resolution to more than 150ns could be done if necessary but is not very desirable.
Memory	The timestamps can require up to 16 bits
	The memory needs to be able to hold data for at least hundreds of ms for ILC operation. For beam tests, sources and cosmics, it would be useful to have the memory hold data for many seconds.
	All data in memories must be able to be read out within 98ms under normal conditions (reasonable occupancy, etc, TBD).
	Bad pixels should be able to be masked
	Pixels with no hits should be ignored during readout
The number of allowed timestamps	Minimum = 4, Maximum number = 16. ** Note this requirement assumes N independent registers inside every pixel, but can also be expressed as a probability of pixel overflow, (dependant on noise rate), see section 4.4)*
External contacts	The contacts should mechanically allow the sensor to be placed inverted on a PCB preferably using standard BGA-like solder technology (ASIC 2)
	All required I/O termination circuitry should be within the sensor
	No substrate ground should be needed
	Data output must be able to drive signals down 1.5m tracks on a PCB
Power	The maximum averaged power during timing equivalent to ILC operation must be 1 uW/mm^2

3. GANNT CHART



ID	Task Name	Duration	Resource Names
1	**Feasability Study**	**24 days**	**RAL Technology**
2	Complete Feasability Study	1 mon	JC
3	Prepare Specification Docs	4 days	JC
4	ASIC1 Preliminary Design Review	1 day	
5	ASIC1 Design Period (Initial schedule)	8 mons	
6	**ASIC1 Design**	**207 days**	**RAL Technology**
7	Evaluate & Select technology	1 wk	
8	Analog sum + Comparator design study	4 wks	
9	**Schematic Design & Simulation**	**85 days**	
10	Memory cell design & optomisation	2 wks	
11	Memory sense, readout +MUX design	2 wks	
12	Local Controller functional design	2 wks	
13	Graycode distribution	2 wks	
14	Pixel variants (4?)	2 wks	
15	Periphery circuits	1 wk	
16	Pad cells (inc Layouts)	2 wks	
17	Develop full ASIC1 schematics	3 wks	
18	Contingency	1 wk	
19	IDR - Schematic review	1 day	
20	Holiday (Distributed throughout)	4 wks	
21	**Layout**	**55 days**	
22	Base Pixel Layout	1 wk	
23	Pixel Variants	1 wk	
24	Local controller layout	2 wks	
25	Column base layout: Data mux	2 wks	
26	Biasing + Array power	2 wks	
27	Pad ring + Global connect	2 wks	
28	Congtingency	1 wk	
29	Top level DRC	1 wk	
30	Top level LVS	1 wk	
31	FDR - Layout & Pre-submission review	1 day	
32	Follow up & Submission	2 wks	
33	Sienna Conference? TBC	5 days	
34	Fab-B shuttle Run? Date TBC	1 day	
35	Fab-B shuttle Run? Date TBC	1 day	
36	ASIC1 FDR	1 day?	
37	ASIC1 Fab	3 mons	Silicon Foundry
38	**ASIC1 Test System**	**70 days**	**Imperial College**
44	OptoDAQ Firmware changes	1.5 mons	IC?
45	ASIC1 Wire Bonding	1 wk	RAL
46	ASIC1 basic tests	2 mons	
47	ASIC1 detiled tests	3 mons	
48	ASIC2 Spec review	1 wk	
49	ASIC2 Preliminary Design Review	1 day	
50	ASIC2 Design	7 mons	
51	ASIC2 Fab	3 mons	
52	ASIC2 Sawing & Bonding	1 mon	
53	ASIC2 basic tests	2 mons	
54	ASIC2 detailed tests	12 mons	
55	Beam test	6 mons	

4. SPECIFICATION OF ASIC1 & ASIC2

It is important to identify the key requirements that will be addressed in the first and second ASIC designs. In general, the first ASIC will be primarily concerned with the pixel design, and the second ASIC will develop this into a larger device considering system and global requirements.

Specifications listed for ASIC2 are guidelines to indicate distribution of requirements across the two fabrication runs, and do not form an agreed specification of the second design effort. An appropriate review period and secondary PDR will be held at a suitable time before design work starts for ASIC2.

4.1 Format

ASIC1	ASIC2
Test Structures: Opportunity to explore several different designs depending on design study.	Single large design: Selecting specific sub-designs from ASIC1 based on test results.
Sub-reticle size, possibly MPW run if available / cost efficient.	Full reticle or stitched design, engineering run to produce enough sensors for final beam test

Specific pixel variants will become clear during the design process. The likely approach would be 4 pixel variants forming one active array with common control signals (see example floor plan in section 5)

Specific pixel options are listed in priority order below.

a) Comparator circuit (2 options)

b) Analog sum of 4 pixel diodes

c) Diode reset (continuous / pulsed)

d) Standard / Deep NWELLs

4.2 General

ASIC1	ASIC2
External (pcb-mounted) components will be used where needed	Use of external components will be minimised
No constraint on number of control and power signals (pads)	Number of control and power signals will be minimised
No constraint on overall power consumption, but circuits will be selected for long-term low power goal.	Total averaged power consumption will be minimised
Standard cell pad library from foundry, arranged in a standard pad ring around edge of chip. Bump-bond test pads may be included as additional test structures (see section 4.5) depending on time availability in schedule.	Could implement bump-bondable pads for all signals, and also consider locating pads on one side or in one central region (depending on limitations of stitching process)
Technology: to be selected • Foundry A (0.35um) • Foundry B (0.18um)	Technology will not change for ASIC2, allowing circuits designed and proven in ASIC1 to be reused with confidence.

4.3 System

ASIC1	ASIC2
Will aim to maximise active area in pixel regions only	Will aim to maximise active area across full ASIC area
Parallel data output for debug	Will consider high-speed serial data output, eg LVDS.
No peripheral data storage, live parallel data must be captured or lost	Will consider peripheral data storage (FIFO) to support possible handshaking/request protocol from controller FPGA/system.
Sparse pixel readout should be demonstrated in this device (using mostly external control signals)	Sparse readout should be incorporated into on-chip control logic based on evaluation of first device.
Comparator threshold is driven from off-chip.	Comparator threshold is generated on-chip with digital programmable DAC.
Individual pixel masking will be implemented to facilitate testing (also an end requirement of system)	No change

4.4 Pixel

ASIC1	ASIC2
50 microns pixel size	50 microns pixel size
EPI thickness: Maximum offered on chosen technology: >12um.	No change
4 diodes per pixel Physics simulations will define precise location of each.	4 or more diodes per pixel Physics simulations may be required to redefine precise location of each if in-pixel circuits change between ASIC1 and ASIC2.
Diode type: to be selected from available technology options based on physics simulations. Eg: Standard/Deep NWELL	Diode type will be selected based on physics testing of ASIC1
Diode reset: possible options include continuous / Pulsed reset	Diode reset: to be selected based on ASIC1 testing
Minimum detectable input: "Fire" threshold ~50% equivalent MIP signal, subject to physics simulations.	
Noise rate (false hits): 10^{-5}	Target noise rate: 10^{-6}

ASIC1	ASIC2
Comparator design study to identify a suitable comparator design to meet the above requirements: Either local threshold trimming or autozero will be necessary to overcome mismatch, reset noise (if applicable) to meet target noise rate. Clocked/continuous circuits will be considered and evaluated for their low-power operation.	Comparator design to be selected based on ASIC1 testing. Possible redesign if measured noise rate will fail to meet the target above.
Acceptable probability of pixel overflow= 10e-10 (Equivalent to 6 local memories per pixel at 10e-5 noise rate, or 3 local memories per pixel at 10e-6 noise rate)	
If in-pixel memories would be DRAM. Will consider resulting output data rate to respect DRAM lifetime, possibly requiring refresh cycles/on-chip static storage. If memories are not located inside the pixel, SRAM cells may be preferred for their long-term storage capability. The selection of DRAM vs SRAM will be made early into the design process, but is left open for further study at this PDR.	The selected approach for ASIC1 will be carried forward to ASIC2.
Time available for readout between bunch trains = 98ms	
16 bits implemented for time-stamp storage	16 bits implemented for time-stamp storage
Outcome from feasibility study recommends implementing the memory management logic for a set of pixels in one dead pixel called a "local controller". This reduces the logic in the pixel (improving sensitivity) at the cost of one known dead pixel per 2N active pixels & high routing density (negligible impact for high energy particles). Depending on process technology chosen, N might range from 8 to 15, yielding an average dead space of 6% to 3% respectively.	

4.5 Additional Test Structures

ASIC1	ASIC2
Test transistors	Test transistors
Isolated comparator designs, with inputs and outputs wired to pads for test/characterisation in isolation.	
Trial bump bond pads on one edge for assembly tests. (subject to available design time before target submission deadline).	

4.6 Requirements that may/will not be met

The specifications listed above do not necessarily meet the full set of initial requirements set out in section 2, but have evolved over the course of the feasibility study and regular monthly meetings with the collaborators. This section highlights those initial requirements that will not be met, or have had to be compromised in this development plan.

4.6.1 Memories

The number of allowed timestamps	Minimum = 4, Maximum number = 16.

Due to space limitations in the pixel, the number of registers is very unlikely to increase over the minimum (4). More registers increases pixel complexity, routing & control logic which have a detrimental effect on dead space.

Memory	The memory needs to be able to hold data for at least hundreds of ms for ILC operation. For beam tests, sources and cosmics, it would be useful to have the memory hold data for many seconds.

If DRAM circuits are targeted for this design there exists a finite data-retention time of order 5ms with no refresh cycle. Refresh cycles would increase dead space (extra circuity) and involve extra signal timing/control. Feasibility of this aspect is not concluded at the time of PDR, and will be completed within 1 month of PDR.

Use of DRAM impacts the applications cited as requiring "hundreds of ms" data hold time, unless refresh/SRAM options are selected.

4.6.2 System / Global

External contacts	All required I/O termination circuitry should be within the sensor

Where possible, termination and decoupling will be included on-chip for ASIC2. Achieving zero external components may prove difficult, but will be considered during ASIC2 development: A likely outcome is an ASIC2 that could be evaluated with/without external components for performance comparisons.

Power	The maximum averaged power during timing equivalent to ILC operation must be 1 uW/mm^2

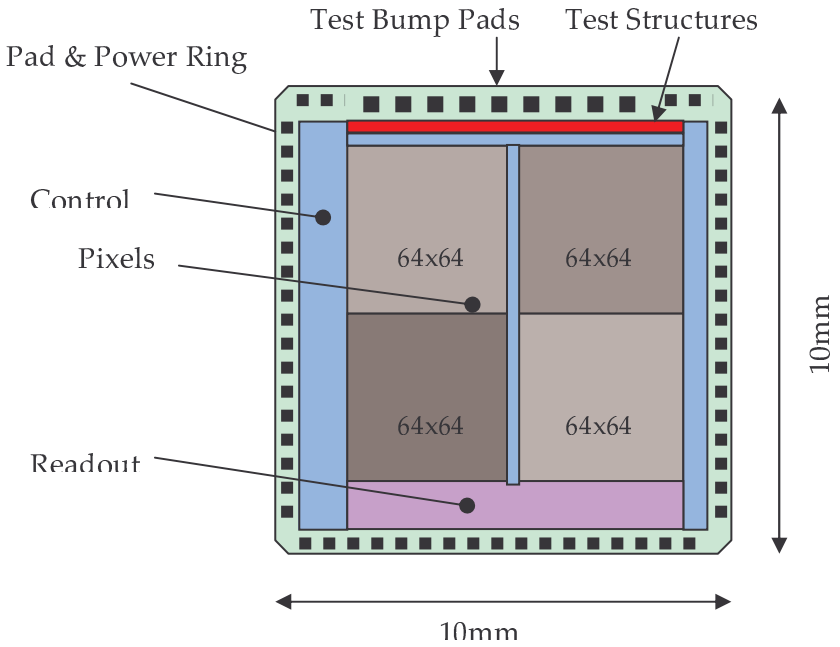
This specification has already been identified as extremely tight, and is unlikely to be met in either ASIC1 or ASIC2. The focus of ASIC2 will be low power operation, so whilst the target is unobtainable, the sensor produced should demonstrate the realistic extent of the low-power capabilities of current technology.

4.6.3 Functional/Pixel

Comparator	The comparator threshold must be set/trimmed by on-sensor DAC. The DAC should be common to multiple pixels, which are therefore required to be uniform

The exact implementation of the comparator is not yet known. The issue of non-uniformity between pixels will be addressed throughout (primarily ASIC1) but the specific approach first identified may not be the winning solution. Local DAC trimming may prove to be costly solution, where auto-zero comparator designs may be more appropriate. An initial design study will investigate and draw conclusions, with the overall final choice brought back to the collaboration meeting.

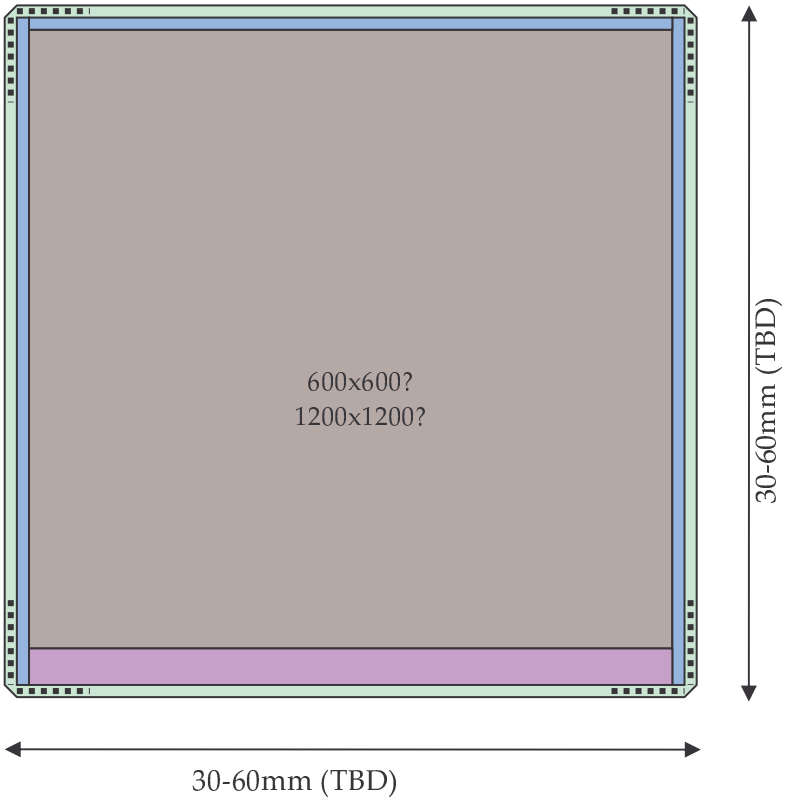
5. ASIC1 GUIDE FLOORPLAN



Four pixel variants with shared control and readout circuits so the device behaves as a single sensor.

Overall active area
= 128x128 pixels @ 50um
= 6.4mm x 6.4mm

6. ASIC2 GUIDE FLOORPLAN



Single pixel variant is selected.

Large sensitive area (possibly stitched) with optimised periphery circuits