Tera-Pixel APS for CALICE

Sensor Testing Specification

Document Revision 0.4

Jamie Crooks, Paul Dauncey, Giulio Villani,

28 April 2006

	Name	Signature	Date
Project Manager	Jamie Crooks		
Customer/Sponsor	Paul Dauncey		

1. TABLE OF CONTENTS

2. INTRODUCTION

This document details the tests which will be needed for the first round of MAPS sensor production (ASIC1). The tests will be split into groups and these will be performed at physically different locations. The first "basic" tests will be done in RAL Technology and will check the functionality of the sensor. The more "detailed" tests will then be done (assuming the sensor is functioning). Tests for comparison with the sensor simulations will be performed at RAL PPD, while tests of the sensors in terms of physical detectors with radioactive sources and cosmics will be done at Imperial and Birmingham, respectively.

3. ITEMS WHICH NEED TO BE TESTED

It is important to identify the key items that will need to be verified when testing the sensor. These are listed below and a reference is given to the section where the relevant test is detailed.

Test	Section
Test Structures	Basic
Pixel digital circuit functionality	Basic
Comparator functionality	Basic
DRAM decay times	Basic
Global digital circuit functionality and data I/O	Basic
Power consumption	Basic
Effect of substrate connection	Basic
Non-wire bonded mounting	Basic
Charge diffusion	Simulation
Crosstalk	Simulation
Charge collection time	Simulation, possibly source
ILC timing operation	Basic, source
Noise rate vs. threshold	Basic (qualitative test, observation), source, cosmics (quantitive tests, statistics)
Relative efficiency vs. threshold	Simulation, source
Relative efficiency vs. time	Source

Time-correlation of noise hits, noise vs. clock rate	Source, cosmics
Uniformity of threshold, temperature and time dependence	Basic (qualitative tests, observation), source (quantitive tests, statistics)
Uniformity of gain, temperature and time dependence	Source
Uniformity of noise rate, temperature and time dependence	Source, cosmics
Magnetic field effects; operation in fields up to 5T as available	Source (setup moved to location of magnet)
Absolute MIP calibration	Cosmics

4. BASIC TESTS

These tests will be done at RAL Technology. The main aim is to measure the basic functionality of the sensor.

4.1 Schedule

The specific schedule of functional tests will ultimately depend on the circuits that are manufactured, but a typical indicative schedule is presented below:

Power-on PCB with no chip.	FPGA holds board in idle (safe) state. Measure current consumption, check reference voltages, currents (where possible without chip). Probe each individual power pad to check	1 day
Power-on PCB with bonded chip	FPGA holds board in idle (safe) state. Set adjustable current biases. Measure current consumption & voltages at pads, compare with expected/simulation values. Probe individual chip outputs for expected states (ie logic zero/one). Proves power supplies, pads, bond connections.	2 days
Shift register tests	FPGA holds board in idle state, then clocks (each/any of those available, eg mask setting, readout, data) shift registers: Insert single-cycle token or known pattern into one end; should emerge N clock cycles later at shift-register output. Proves digital logic power supplies, correct digital functionality of minimum size nmos & pmos transistors, integrity of routing, output drive capability of digital output pads	3 days
Comparator test structure	Test structure comparator inputs driven with typical pixel-level input signals and output checked for correct operation. Pulse/waveform generator bench equipment and oscilloscope	1 day

|	should be sufficient for this, no need for FPGA control.	
Test transistor verification	Other test structures placed may only be visited if the preceding tests suggest possible process / low-level problems exist. A few devices would be required to be stored long-term (beyond end of project) at RAL in nitrogen cabinets so these transistors could be characterised in the future, for process monitoring.	
Blind test	FPGA configures all pixels into masked mode, and threshold is set to maximum. No pixels should trigger. Data output architecture is operated. Check outputs all read zeros (no stuck bits), proves data registers are correctly reset. Check that read token emerges intact if no registers are hit – is worst case for distance travelled in single clock cycle.	3 days
Single column tests	FPGA configures only one column of pixels as un-masked. Allows tests that cause every pixel to be "hit" ie setting threshold to minimum: Data readout architecture is operated. Check correct number of hits are output, and addresses are unique and correct. Repeat for every column across sensor. Build data/address map of full sensor array. Confirms each pixel variant is working correctly.	5 days
Full frame tests: Single shot	FPGA drives sensor in single-shot mode: Timestamp code is set to known pattern, and trigger samples once. Full readout cycle collects "hit" pixel data. Threshold scan to check chip response in overflow conditions (compare with calculated expected)	4 days
Full frame tests: N shot	FPGA drives sensor for N shots (ie 2) recording different time stamp codes (eg AAA and 555). Full readout cycle checks that each time-stamp code features in ouput data. Known threshold values from previous test can be used to predict result: Example case – trigger N times to reach estimated memory-full condition, then trigger a few more times with new time-stamp codes to check data is not overwritten in memories.	4 days
Full frame tests: continuous mode	FPGA drives sensor in "normal" operation mode for full bunch-train length. Dark operation should record noise hits only. Threshold scan/adjust as required. Qualitative checks that noise hits go up/down with threshold scan.	2 days

Testing capabilities at RAL do not currently include equipment that would allow any quantitive tests regarding temperature.

5. SENSOR SIMULATION TESTS

These tests will be done at RAL PPD. The main aim is to measure the sensor parameters which can be compared with the sensor simulation at pixel level. The parameters of interest are collected charge by individual pixels against spatial coordinates of hits, crosstalk among neighbouring pixels, sensitivity to fraction of MIP and collection time.

5.1 Test setup

The test setup will consist of a programmable pulsed Laser coupled with a microscope and XYZ stages housed in a dark enclosure kept in a thermally stable environment.

Laser Source

Focusing optics and attenuators

Sensor

Readout PCB

XYZ stage
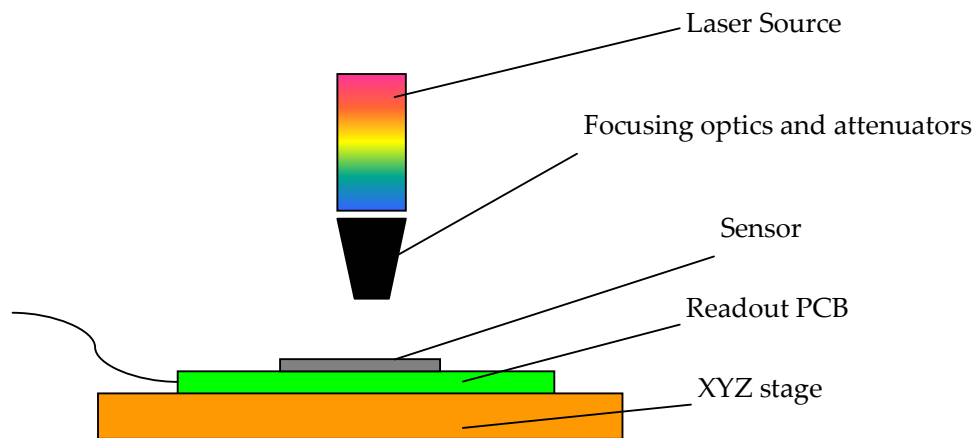
A laser beam of selectable parameters (wavelength, intensity and beam size) will be used initially in the mid IR mode (1064 nm). The intensity of the beam will be set to a level corresponding to MIP generation in Si. The size of the laser beam can be selected from a minimum of around 1x1 μm to 25x25 μm at the maximum magnification but different optics arrangements will allow even 50x50 μm, so as to illuminate a single or a small group of pixel.

5.2 Charge collection efficiency

The beam will be scanned over the surface of the detector with the same, or finer, XY resolution used in simulation (4.1 μm for a 25 μm cell). A digital camera coupled to the microscope will allow visual indication as to where the laser will be focused. If the material on top of the sensor does not allow the beam to get through an alternative would be to hit from the back (i.e. from the substrate) and determine the spot location by measuring the collected charge.

 On each location the laser will fire at a maximum rate of 50 Hz for a number of times to allow enough statistics to be built then will move onto the next adjacent location. In this way a 3D representation of charge collected can be compared with simulation results. The process will be fully automated using a PC running some dedicated VIs written in Labview to control the whole system. The laser system will allow input and output triggering to synchronize with readout phases.

5.3 Crosstalk

By firing the laser onto a known location within a pixel and measuring the charge collected by the neighbouring pixels (3x3 groups or even bigger) an indication of crosstalk (i.e. charge sharing) can be obtained.

5.4 Sensitivity to fractional MIP

The intensity of the beam, calibrated against detectors of known characteristics, can be varied regardless of the beam spot size to correspond to fractional equivalent MIP.

5.5 Charge collection time

Charge collection time of individual pixels can be determined once the temporal shape of the laser pulse and impulse response of the readout electronics is known.

The pulse width of the laser is known to be about 4 – 5 ns max but its actual shape will be determined using a combination of fast detectors and amplifiers, operating in the GHZ range. The pole locations of the readout electronics should be known from simulations or can be determined by directly exciting appropriate input stages of the readout.

The temporal evolution of charge collection would require access to the analogue output from the readout electronics. Alternatively, and more simply, only the temporal digital delay of the comparator's output against its threshold should be known (again from simulation or from other direct measurement). Once the laser is fired with a set level of energy corresponding to a known comparator's threshold, any further delay seen at the output is related to the delay in charge collection. The method then would be to provide triggering to the sensor by the Q-switch signal of the laser (see below) and make sure that the comparator starts sampling immediately after the laser pulse (which should correspond to a known and repeatable time delay from the Q-switch signal), at the peak of collection charge process. The delay seen at the output will be a combined delay due to charge collection process and known readout delay. Alternatively, with a clocked sample comparator, then varying the sample time after the laser signal will provide the same measurement.

5.6 Rates

To compare simulations with test results a minimum number of 13 x 13 = 169 samples / pixel are needed, for a 50 x 50 μm cell. For a group of 3x3 cells this corresponds to 1521 hits. If 100 hits are needed for each location, at the maximum laser pulse rate of 50 Hz this corresponds to 3042 sec. Assuming a maximum number of threshold scans of 10 on each location, this would correspond to 30420 sec. Taking into account the time required for each step motion, assumed in the order of 0.5 sec, it follows that around 8.7 hrs are needed for a charge collection and pixel crosstalk test. In reality, the time could be much less, as there is no need to continue on each location with an increased higher threshold when that the rate of positive hits (i.e. hits that flip the comparator) has decreased to a low level.

This test analysis will be simplified by having the option of masking all pixels except for the group of 3x3 cells centred around the pixel of interest. The data rates will be dependent on the threshold level set. Assuming a maximum rate of 50 hits/sec and 5 bytes/pixel, at the lower threshold level without using the mask, around 10^4 pixels would result, corresponding to 2.5MBytes/sec, which sets the maximum DAQ rate for these tests.

The trigger to the readout can be provided by the internal Q-switch of the laser. This is a 5V 6 μs wide pulse that occurs when the Q-switch is energized. The laser pulse will exit the cavity

around 80 ns after the rising edge of this pulse. The reset phase of the sensor could be started by the rising edge of this signal if it does not last longer than say 50 ns, before the laser fires. The exact delay of the laser beam exiting the cavity after the Q-switch signal will be determined during the calibration and assessment of the laser system.

6. RADIOACTIVE SOURCE TESTS

These tests will be done at Imperial College London. The main aim is to characterise the response to a physics energy deposit similar to a MIP as well as measure the efficiency as a function of the threshold setting. Some tests of noise rate and ILC timing can also be done.

6.1 Test setup

The test setup will be a single sensor with associated DAQ system, a source and some triggering.
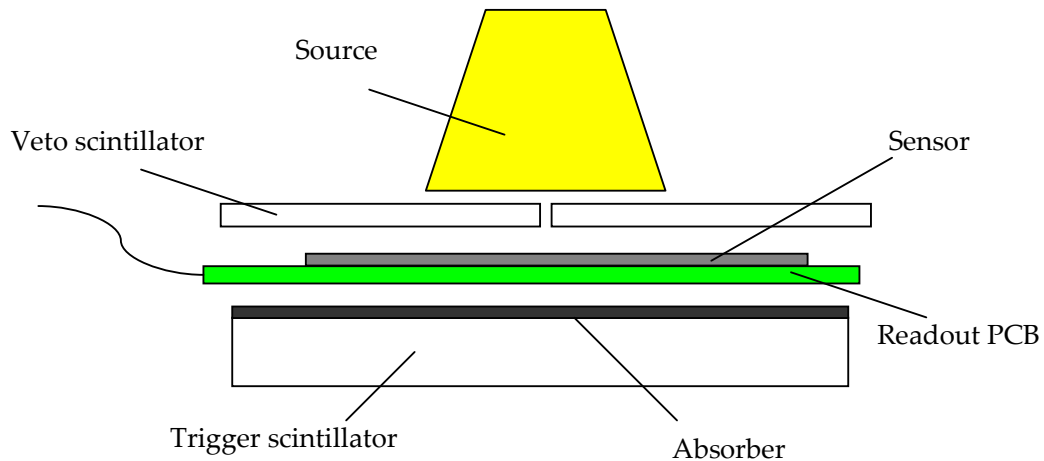
A β source with a reasonable maximum energy, such as ^{90}Sr, will be used. A scintillator on the far side of the sensor, possibly behind a thin absorber, will provide a trigger or timing reference. A further scintillator on the source side of the sensor with a small hole could act as a veto collimator. There would be two basic modes of operation: triggered and free-running. Both would be operated with the sensor between the source and the trigger and also with the sensor placed well away, to give a measurement of background rate.

6.2 Triggered mode

This mode would operate with the lower trigger scintillator providing a bunch crossing signal to the sensor. The time between the trigger and the bunch crossing signal would need to be adjusted so the comparator samples at the peak of the collected charge. (In principle, this delay could be scanned to give a measurement of the charge collection although it can be more accurately done with the laser system described above.) Following each trigger, the sensor readout is performed, giving at most one timestamp per pixel. The sensor is then reset and the trigger cycle repeated. It would also be possible to send two or three more bunch crossing signals following the trigger, spaced by around 150ns, to allow the decay of the physical signal with time to be observed. This mode would be used for most of the source

measurements, as it gives a more efficiency collection of source hits than the free-running mode.

6.3 Free-running mode

This mode would run the sensor with timing similar to that expected for ILC operations. This will allow a check that the signal size is not sensitive to the sensor timing. In this mode, following a sensor reset, around 10^4 bunch crossing signals will be generated at around 6MHz. The "trigger" scintillator will not be used as a trigger but the time of the hits in it (and the veto scintillator if used) will be recorded by a multi-hit TDC. This time measurement allows the source hit to be associated with a particular timestamp; in fact, the TDC measurement should be accurate enough to give information on the phase of the trigger relative to the 6MHz clock and so on the efficiency as a function of the time offset. Only a few threshold values, rather than a full scan, will be required to cross-check the triggered mode results.

6.4 Rates

A threshold scan of around ten values would be sufficient. If each value requires of order 100 source hits per pixel, then for 128×128 pixels, i.e. around 10^4 pixels, this is around 10^7 source hits. To gather this in one day (around 10^5 secs) needs a rate of around 100Hz.

The DAQ system needs to be able to sustain this rate. Each source hit should give one or two pixels per trigger. Each pixel hit will need to be read out as five bytes, to contain the timestamp and the row and column locations.

In triggered mode, then with a noise rate of 10^{-5} , each trigger will only give around 0.1 noise hit at the nominal threshold. However, for the lower threshold values in the scan, a much higher rate will be seen, potentially up to a significant fraction of all 10^4 pixels. These runs set the required DAQ capability and so, at these thresholds, this would give a data volume per readout of 50kByte and hence a rate of around 5MByte/s at 100Hz.

In free-running mode, a full ILC-type bunch train of around 10^4 samples within 2ms would give around 10^3 noise hits for thresholds close to nominal and this would be repeated at a rate of 10Hz. This then requires around 10 source hits per bunch train to achieve the desired source hit rate of 100Hz. This corresponds to a source hit rate of 5kHz within the 2ms bunch train. The readout data rate is dominated by the noise and corresponds to around 5kByte per bunch train. Overall, this is 50kBytes/s but requires the data to be transferred off the sensor within around 2ms after the bunch train before the DRAM lose the data. The rate off sensor is then 2.5MByte/s.

To give a usable source hit rate of 5kHz in free-running mode, the source will need to be at least 10^5 Becquerel (3 µCurie). This will clearly satisfy the triggered mode requirement also.

7. COSMICS TESTS

These will be done at Birmingham. The main aim is to give an absolute measurement of the response to a MIP and hence the MIP efficiency vs threshold. Because of the low rate of cosmics, only part of the threshold range near the likely operating point will be scanned, with the source results being used to extrapolate to other thresholds. To ensure that individual

sensor variation is accounted for, at least one sensor would be tested in both the source and the cosmic test systems.

7.1 Test setup

The test setup will consist of a cosmic ray telescope of four (or more) layers with a pair of trigger scintillators above and below.

Trigger scintillator

Sensor

Readout PCB

Trigger scintillator
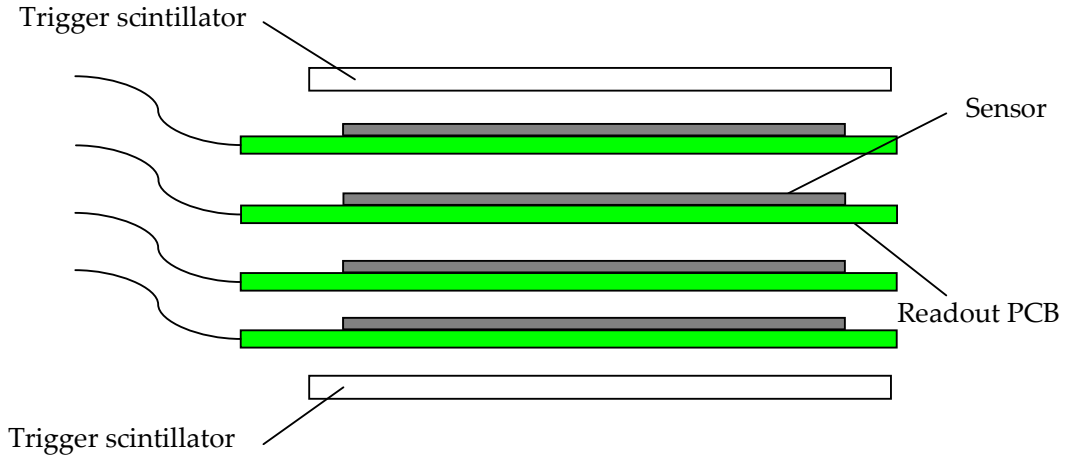
The trigger scintillators would provide the bunch crossing signal and the sensor readout would follow immediately after this, in a similar way to the source trigger mode. During a threshold scan, the threshold would be adjusted in a single layer (or possibly even or odd layers) at a time, allowing an fixed-efficiency track reconstruction in the layers not being scanned. This would allow the absolute efficiency of the scanned layer(s) to be determined by interpolation or extrapolation.

7.2 Rates

The rates will be low so the setup for this test would need to be dedicated to this one measurement and left to run stably for a significant period. The physical rate of cosmics in such a telescope, with dimensions around 1×1 cm^2, would be of order 0.01Hz. To do a scan over four threshold values with at least 10^3 cosmics per value would take around 10^6 secs, i.e. two weeks. This would have to be done four times, once per layer (or possible twice, once for even and once for odd layers).

The DAQ rate at 0.01Hz would be much smaller than for other tests and so will not be an issue, even with four sensors being read. However, frequent noise runs at each threshold value using a non-cosmic (higher rate) trigger to check background noise rates will be needed, to ensure any time and temperature variations over the long periods of the test are correctly compensated.

8. DAQ READOUT SYSTEM

All test setups require a readout system for the sensor and a single design will be used which is common for all. This will consist of a PCB to hold the sensor, a control board to operate it and a PC to run the control board.

8.1 Sensor PCB

A simple PCB will be built to take the sensor. This will have a simple ribbon cable connecting it to the control board which will provide all differential clock, control and readout. Ideally, the PCB would be entirely passive except for the sensor. However, a DAC to control the threshold might be required if there is not one on the control board.
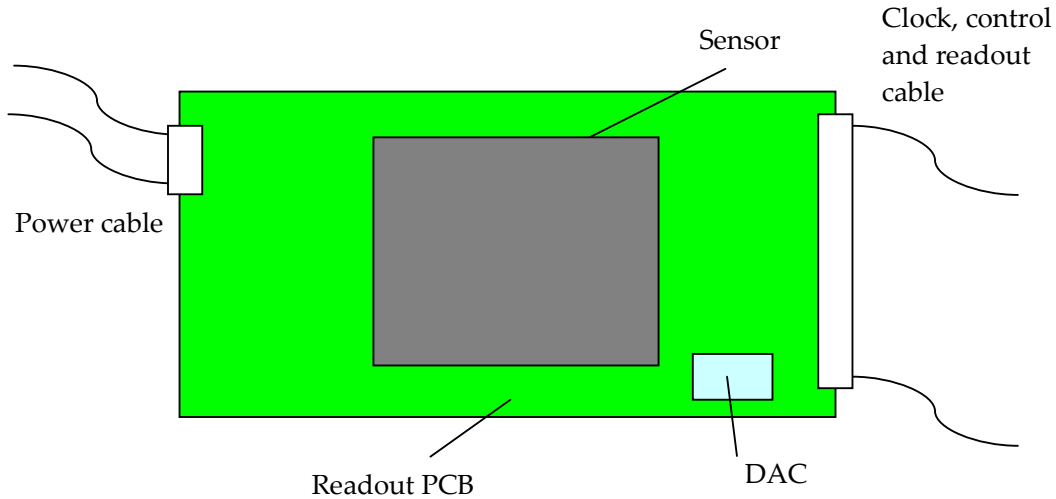
For mechanical compatibility among different test setups, the PCB will have a size dictated by the allowed sizes of the laser setup sample holder:
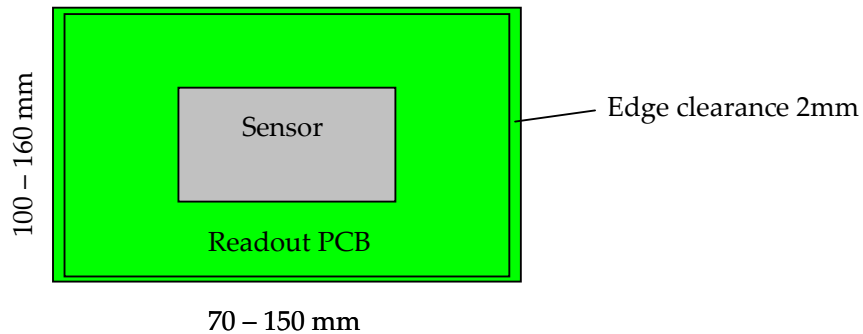
The maximum thickness of the PCB should be 2mm.
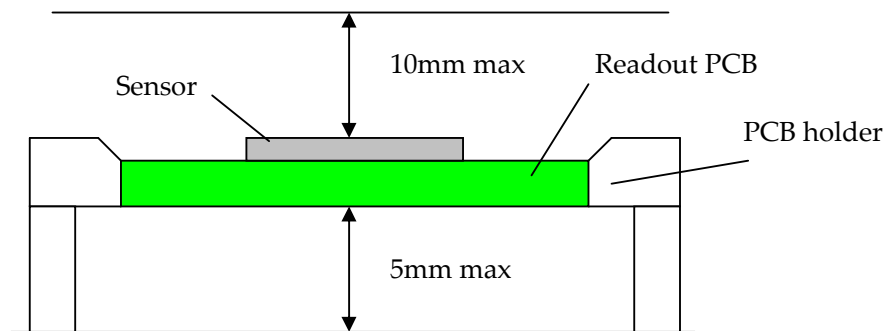
There are no further physical (dimension) constraints on the PCB from the basic, source or cosmics testing aspects.

The PCB design and manufacture will take place through Imperial. However, it will be important for RAL to be involved in the specification and review of the PCB designs to ensure the necessary test features are included, such as

- Test probe points on key signals, VDD and GND.

- Adequate buffering/termination of critical digital control signals, high speed clocks etc

- Adjustable (potentiometer) control of chip bias currents

8.2 Control board

The control board will probably be a commercial FPGA development board to minimise design work. The FPGA board will need a connection to a PC, such as a USB port. USB 2.0 is around 30MBytes/s at realistic rates (i.e. half nominal rate of 60MBytes/s), which should be sufficient for the required readout speeds needed.

The board will need a wide connector to provide the clock, control and readout signals to the sensor, preferably all under direct FPGA control. It will require an external trigger input as well as the ability to self- and software-trigger.

FPGA firmware development will take place at Imperial. However, it will be important for RAL to be involved in the specification and review of the FPGA firmware designs where they concern the sensor, to ensure the necessary features are included or can be modified, such as

- Debug/test routines

    o Shift register clocking & read-back checking, (eg Mask Set Registers, + any others in design)

    o Readout testing, eg:

        ▪ Set all comparators by driving low threshold

        ▪ Set timing code to test pattern.

        ▪ Trigger the device

        ▪ Run full chip readout, checking for stuck bits in data architecture

    o DRAM decay (if dynamic cells have are used) --> force known value into DRAMs and repeat read until data is corrupted.

    o DAC Characterisation (albeit on-pcb or on-chip)

- Chipscope (or equivalent tool) to check signal timings

Many of these routines could be developed at RAL during the basic tests, and need not be written in advance.

In order to recompile/configure the FPGA firmware during basic testing at RAL, compatibility with the existing tools flow at RAL is important. The following FPGA development tools are currently available for use at RAL

- Xilinx ISE 7.1i

- FPGA Advantage 6.3 PS

- ModelSim 5.8c

- Chipcscope Pro 7.1i

Modifying & regenerating the FPGA design will be necessary during the process of the basic tests.