# Problem Report

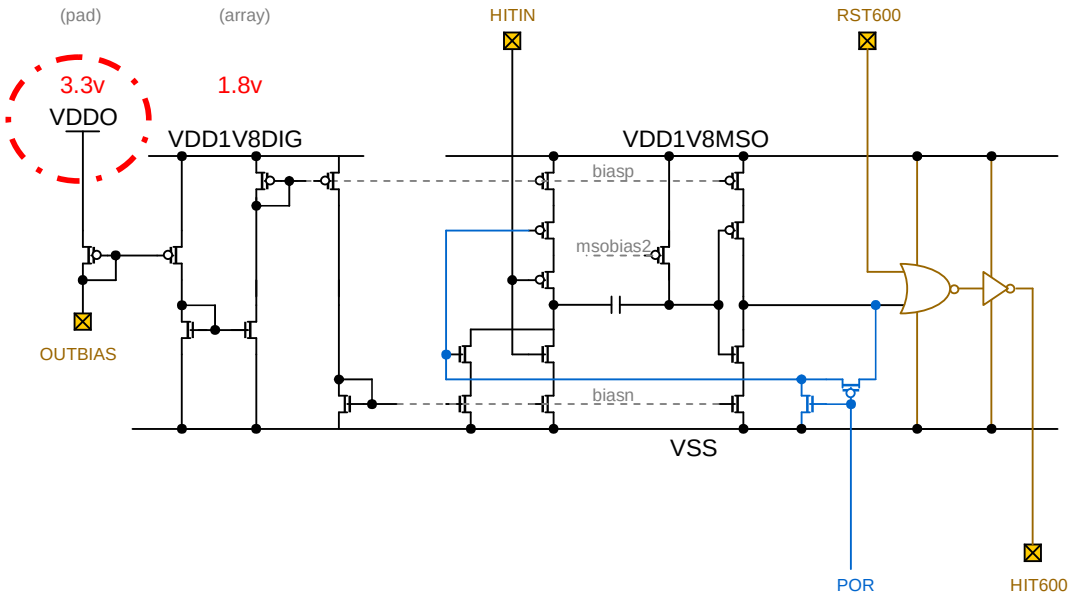
**Report Number: 1**

**Project Name: TeraPixel APS for CALICE**

**Item: ASIC1 Sensor design: Monostable biases**

**Problem**

The monostable circuits were found to be non-operational on all three chips in first round of testing. The problem was finally diagnosed in the bias chain for the current-limited inverter. The general purpose bias pad cell was incorrectly connected such that "Vref" was tied to VDDO. This was proved by connecting VDDO to 2v and VDD1V8DIG to 2v. With the power rails the same the monostable circuit were seen to operate correctly, although this is not a practical long-term solution since the LVDS transceivers on the PCB run on a 3.3v supply.




**Originator (Sign/Date)**

**Project Manager (Sign/Date)**

**Remedial Action**

The options discussed at meeting of 31st September 2007 were:

| | | Sensor card | DAQ card | Cable | Timesacle | Cost |
|---|---|---|---|---|---|---|
| 1 | Level shifters | Re-design | No change | 2m ok | ~4 weeks? | |
| 2 | Direct connect | Modify existing | Modify existing | Minimum lengths only | ~1 week? | |
| 3 | Adjust power supplies | Modify existing | No change | 2m ok | ~instant | |
| 4 | New FPGA+Sensor card | Abandon | Re-design | None | ~4 weeks? | |
| 5 | Die modifications | No change | No change | | ~2 weeks? | (a) Quote requested (b) Giulio? |
| 6 | Design modify + re-fab | No change | No change | | ~8 weeks? | ~$25K |
| 7 | daughter card for sensor PCB to contain LVDS receivers and level shifters that then drive the sensor directly. | | | | | |

The FIB option was preferred as relatively low cost, fairly fast turnaround and no change to PCBs. The first 10 chips were quoted at ~£2k by SMC in Edinburgh. This was not pursued.

A simple alternative was suggested, simulated and shown to work: Placing a low value resistor (100 ohms) from the bias pad to ground pulls enough current through the incorrectly connected PMOS transistor to develop around 3 volts drop from the power rail. This sets the gate of the linked bias transistor to approx 350mV which turns it on enough to activate the monostable circuits. There is very limited control of the current, but this is deemed sufficient to save the expense of FIB modification to a small selection of chips.

Current limiting in the monostables may cause power droop if they all fire at once, therefore correct operation of the power-on-reset and global threshold voltages are essential to ensure correct sensor operation.

*UPDATE (29/11/07): Noise effects in the bulk pixels were diagnosed to be due to excessive current flow in adjacent monostables drooping the power local supply and triggering other local pixels. On further investigation it was discovered that there is reasonable control of monostable current with this solution – therefore the recommended fix is now a 2k2 resistor to ground, which still ensures monostables operate correctly but with limited power.*

DESIGN FIX: Change OUTBIAS reference transistor to connect to 1.8v instead of 3.3v

**Project Manager (Sign/Date)**