Problem Report

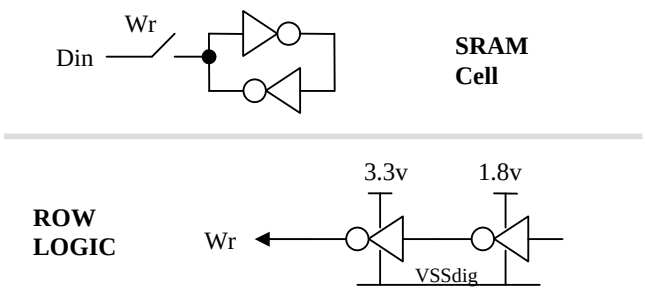
Report Number: 3

Project Name: TeraPixel APS for CALICE

Item: ASIC1 Sensor design: SRAM write enable signal, & VDD2V5dig power supply

Problem

In order to overpower the SRAM cells the write signal must be driven >1.8v to successfully write a '1'. The write signal is generated in the row logic and then buffered with an inverter powered with VDD2V5dig, but shares the VSSdig ground net with the rest of the digital row logic. The VDD2V5dig net was up-rated late in the design process from 2.5v to 3.3v to avoid bit errors seen in monte-carlo simulations (the net name remained)



The 1.8v logic high from the row logic sits right in the switching point for the 3.3v inverter, turning both transistors on, thus drawing large currents such that it cannot be used. Setting the VDD2V5dig power rail to 2.5v reduces the static current flow to <2mA (full chip) but just begins to introduce bit errors in the SRAM data that is stored & read back (as the simulation predicted).

Setting the VDD2V5dig power rail above 2.5v starts to draw a larger current (tens of mA) which (it is believed) has the effect of raising the internal VSSdig ground net. This causes bit errors in the address ROM readout bits from the middle of the column, spreading outwards as the voltage (and therefore current) is increased.

Originator (Sign/Date)

Project Manager (Sign/Date)

Remedial Action

If the SRAM cells can be "reset" such that they hold a logic 1 before use, then the write action only needs to ever change the state from 1à 0, which can be achieved with a lower VDD2V5dig.

Experimental results show that 2.6v is required for the SRAM reset, but this can then be lowered to 2.3v for normal operation. (Normal operation is possible at 2.6v supply but high current (40mA) static current flows through the VSSdig ground net which may compromise performance of the logic. The spare DAC channel with a transistor/buffer amplifier to provide the requisite current should provide a working solution allowing software control of this power supply.

UPDATE (29/11/07): No adverse effects have been seen running this supply at 2.65v so a simple plug-in breadboard adapter with a 100mA regulator has been designed and manufactured by technicians at IC – this will be fitted to each board to avoid the need for separate 2.65v power supply (particularly for beam & cosmic tests where 4 boards are to be operated at once).

DESIGN FIX: Implement level-shifting logic to drive the SRAM write-enable signals

Project Manager (Sign/Date)