Tera-Pixel APS for CALICE

ASIC1.1 Technical Specification

Document Revision 1.1

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2. INTRODUCTION

Due to changes in the funding situation in STFC, the scope of this project has changed considerably. The originally planned ASIC2 will now fall under a new project & scope, and will therefore be defined in a separate specification document as/when that new project is approved and begins.

This project will make one further submission, denoted version 1.1, intended to be a subtle variant on the original ASIC1. This variant will fix some design bugs, reduce the number of pixel variants based on testing results, and implement new compatible test structures to further our understanding and produce test results for publication / support of future grant applications.

3. BUG FIXES

Design errors identified in ASIC1 will be corrected in this new revision. These are tabulated below:

Prob report	Summary	Corrective action
1	Monostable inactivity, due to incorrect VDD reference on final bias transistor in IOUTBIAS reference.	Change VDDO reference to VDD1V8dig on the IOUTBIAS12 and IOUTBIAS34 references.
2	Incorrect biasing of data sense amplifiers due to current mirror made from different transistor types.	Change the referencing transistor from LV to HV transistor for correct matching of oxide thicknesses and therefore currents.
3	Internal SRAM write enable signals cannot be overdriven to the required 3.3v without large static current flow in the row logic.	Replace the write-generating logic with new level-shifting cells to correctly up-scale the SRAM write signal without causing large static currents.

Further information on the design errors and their fixes may be found in their respective problem report documents.

4. SPECIFICATION OF ASIC1.1

This section is intended to specify the changes that will be made to ASIC1 for the revision, 1.1. The initial specifications for ASIC1 are shown in grey boxes, while changes (if applicable) are outlined on the right hand side.

4.1 Format

ASIC1	ASIC1.1
Test Structures: Opportunity to explore several different designs depending on design study.	Pixel architectures The preSample pixel variants will be replaced with preShape pixels. The two variants of the preShape pixel will remain, since there is insufficient data to choose between them at this time. Bias lines will be shared between the original and newly-added preShape pixels, so the full array will be biased at the same operating point (bias pads/DACs used previously for the preSample pixel will be redundant) Test pixels The preSample test pixels in ASIC1 will be replaced with corresponding preShape test pixels, and neighbouring NWELLs for realistic modelling of charge-sharing effects.
Sub-reticle size, possibly MPW run if available / cost efficient.	Footprint and pin-out must remain compatible with ASIC1 PCB. Therefore: 4-seats MPW

4.2 General

<table>
<tr><th>ASIC1</th><th>ASIC1.1</th></tr>
<tr><td>External (pcb-mounted) components will be used where needed</td><td rowspan="3">(no changes)</td></tr>
<tr><td>No constraint on number of control and power signals (pads)</td></tr>
<tr><td>No constraint on overall power consumption, but circuits will be selected for long-term low power goal.</td></tr>
<tr><td>Standard cell pad library from foundry, arranged in a standard pad ring around edge of chip.

Bump-bond test pads may be included as additional test structures (see section 4.5) depending on time availability in schedule.</td><td>Pads may not be added, but some pads may be ‘retired’ if not necessary for updated design (these can be omitted from bonding) or end use changed if compatible with existing PCB design (ie change of use of a control signal driven directly by FPGA)

No bump bond test pads were included on ASIC1 – no opportunity to include on ASIC1.1 is foreseen.</td></tr>
<tr><td>Technology: <u>to be selected</u>

• Foundry A (0.35um)

• Foundry B (0.18um)</td><td>Foundry B (as used previously)

Wafer count & splits

• 12um + DPW 4 wafers = 80 parts

• 12um – DPW 2 wafers = 40 parts</td></tr>
<tr><td></td><td></td></tr>
</table>

4.3 System

<table>
<tr><th>ASIC1</th><th>ASIC1.1</th></tr>
<tr><td>Will aim to maximise active area in pixel regions only</td><td rowspan="6">(no changes to system design)</td></tr>
<tr><td>Parallel data output for debug</td></tr>
<tr><td>No peripheral data storage, live parallel data must be captured or lost</td></tr>
<tr><td>Sparse pixel readout should be demonstrated in this device (using mostly external control signals)</td></tr>
<tr><td>Comparator threshold is driven from off-chip.</td></tr>
<tr><td>Individual pixel masking will be implemented to facilitate testing (also an end requirement of system)</td></tr>
<tr><td></td><td><u>Per Pixel Trimming</u>

A feasibility study will determine whether 2 additional bits of trim resolution can be added to the existing preShape pixel design to improve resolution/range of spread adjustment capability.</td></tr>
</table>

4.4 Pixel

ASIC1	ASIC1.1
50 microns pixel size	Pixel design (preShape) will remain unchanged except for the addition of extra trim bits (if feasible).
EPI thickness: Maximum offered on chosen technology: >12um.	
4 diodes per pixel Physics simulations will define precise location of each.	
Diode type: to be selected from available technology options based on physics simulations. Eg: Standard/Deep NWELL	
Diode reset: possible options include continuous / Pulsed reset	
Minimum detectable input: "Fire" threshold ~50% equivalent MIP signal, subject to physics simulations.	
Noise rate (false hits): 10^{-5}	

<table>
<tr><th>ASIC1</th><th>ASIC1.1</th></tr>
<tr><td>Comparator design study to identify a suitable comparator design to meet the above requirements: Either local threshold trimming or autozero will be necessary to overcome mismatch, reset noise (if applicable) to meet target noise rate. Clocked/continuous circuits will be considered and evaluated for their low-power operation.</td><td>Comparator architecture will not change, but extra trim range is desirable (ideally 2 additional bits)</td></tr>
<tr><td>Acceptable probability of pixel overflow=

10e-10

(Equivalent to 6 local memories per pixel at 10e-5 noise rate, or 3 local memories per pixel at 10e-6 noise rate)</td><td>(no changes affecting this)</td></tr>
<tr><td>If in-pixel memories would be DRAM. Will consider resulting output data rate to respect DRAM lifetime, possibly requiring refresh cycles/on-chip static storage.

If memories are not located inside the pixel, SRAM cells may be preferred for their long-term storage capability.

The selection of DRAM vs SRAM will be made early into the design process, but is left open for further study at this PDR.</td><td>The selected approach (SRAM) for ASIC1 will be carried forward to ASIC1.1</td></tr>
<tr><td>Time available for readout between bunch trains = 98ms</td><td></td></tr>
<tr><td>16 bits implemented for time-stamp storage</td><td>13 bits implemented for time-stamp storage (as in ASIC1)</td></tr>
<tr><td colspan="2">Outcome from feasibility study recommends implementing the memory management logic for a set of pixels in one dead pixel called a “local controller”. This reduces the logic in the pixel (improving sensitivity) at the cost of one known dead pixel per 2N active pixels & high routing density (negligible impact for high energy particles). Depending on process technology chosen, N might range from 8 to 15, yielding an average dead space of 6% to 3% respectively.</td></tr>
<tr><td></td><td></td></tr>
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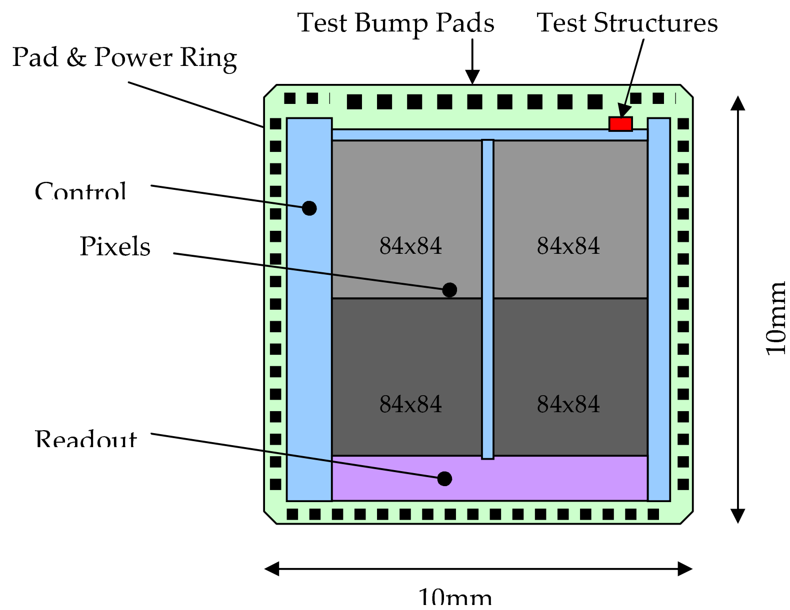
4.5 Additional Test Structures

ASIC1	ASIC1.1
Test transistors	None (as ASIC1)
Isolated comparator designs, with inputs and outputs wired to pads for test/characterisation in isolation.	Comparator input/outputs may be accessed in one of the test pixels.
Trial bump bond pads on one edge for assembly tests. (subject to available design time before target submission deadline).	No bump-bond test pads.

5. ASIC1.1 GUIDE FLOORPLAN



Pin compatibility with ASIC1 must be maintained so the existing PCB and DAQ system can be used for ASIC1.1 testing.