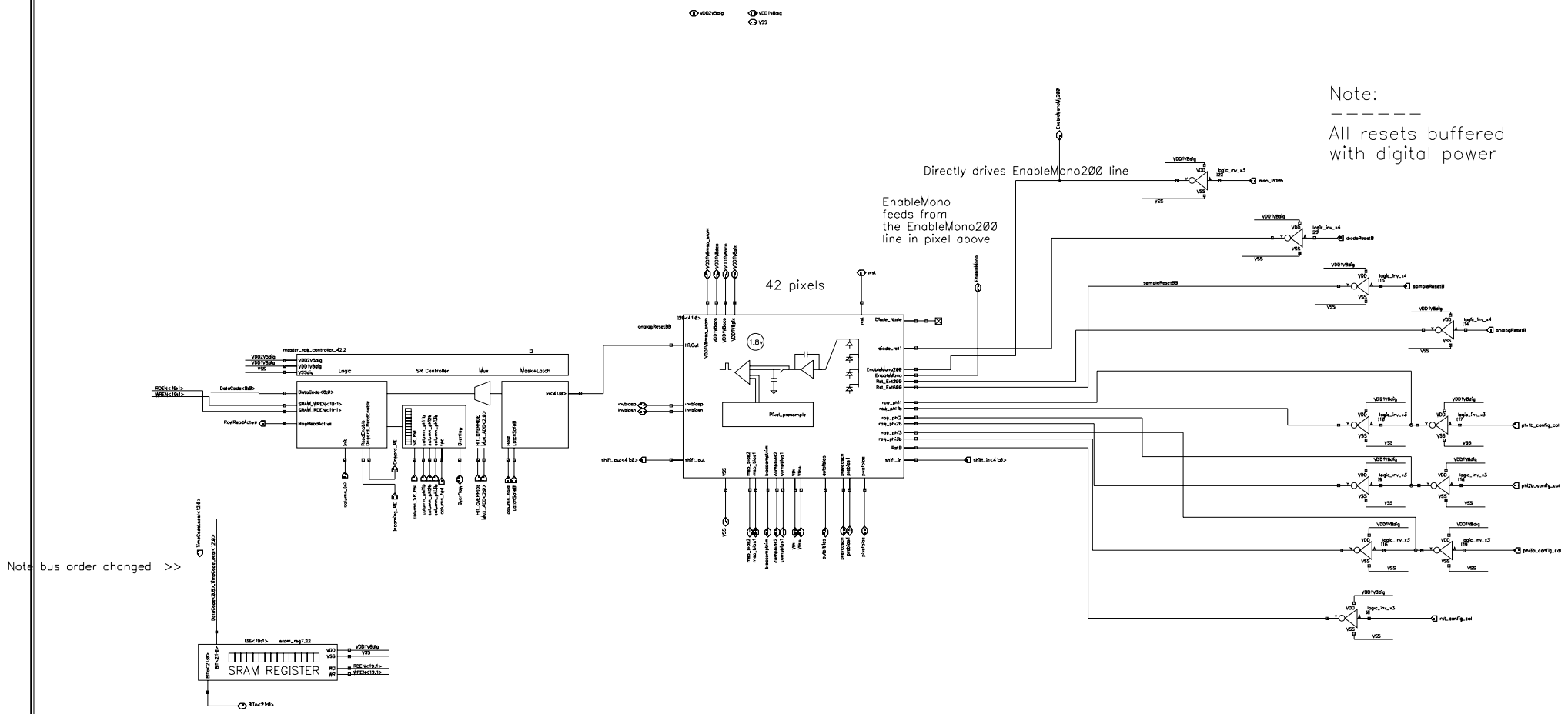
# Pre-Sample Pixel Half-Array 84rows x 42cols

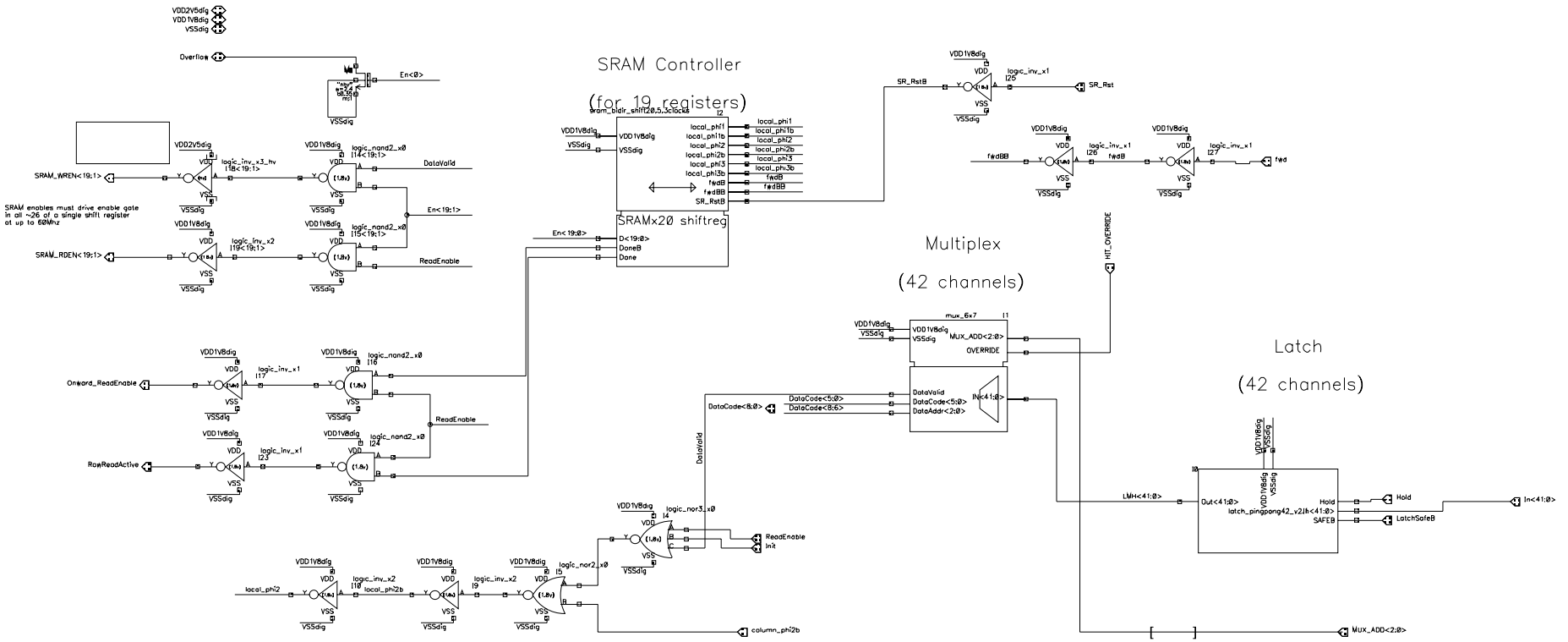
Spare inverter
in layout, tied
off to gnd

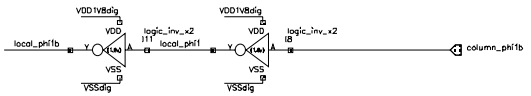
Un-Buffered Global
Voltage signals: Static
during operation

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | pixel_array1_presample_v1.4 |
| Last OA Review | |
| Last Changed | Feb 27 18:43:10 2007 |


Note:
All resets buffered with digital power
Directly drives EnableMono200 line
EnableMono feeds from the EnableMono200 line in pixel above
42 pixels
Note bus order changed >>
SRAM REGISTER
Pixel_presample
1.8v
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
calice_circuits
Block Name
pixel_slice_presample_v1.3LVS
Last QA Review
Last Changed
Feb 26 10:08:30 2007

# 42-CHANNEL 3-CLOCKS VERSION



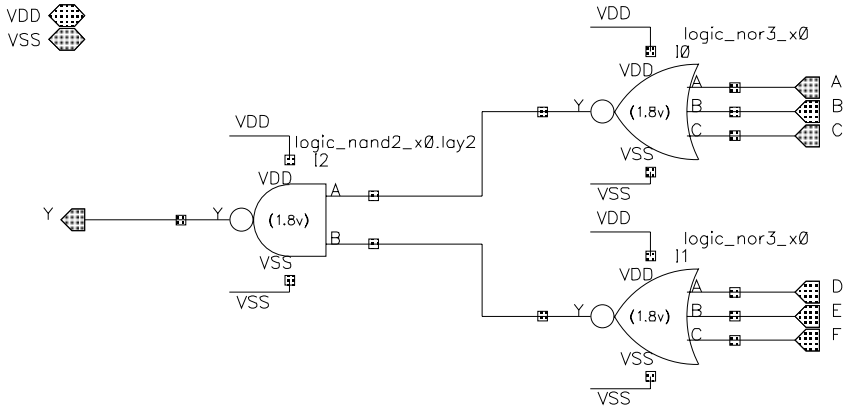




SRAM clocks are distributed as inverse polarity

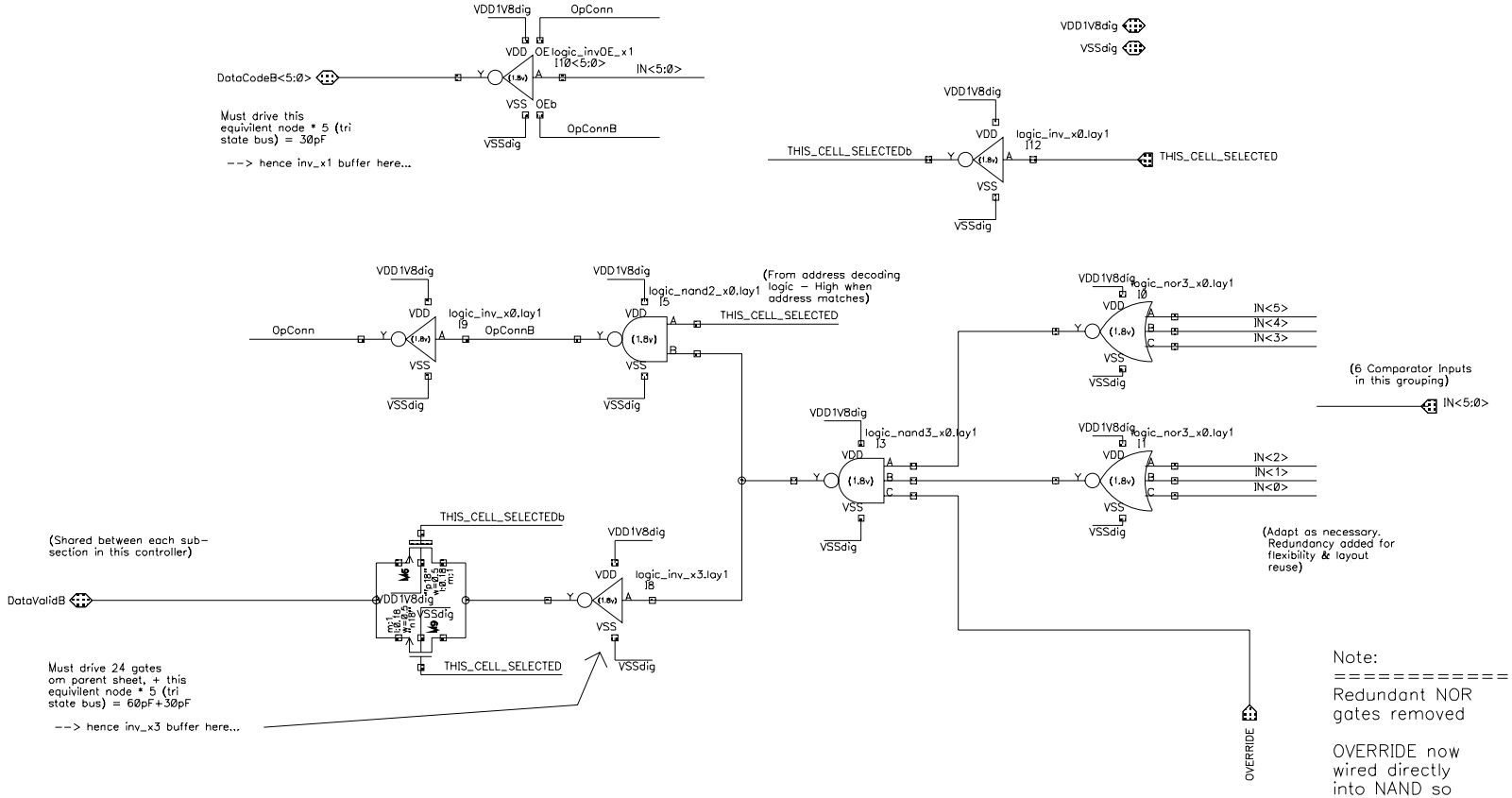
is convenient for phi2 gating, since the inverted phi2 input to the NOR gate completes inversion of its inputs and outputs to turn it into an AND gate

phi1 is distributed in inverted form for consistency

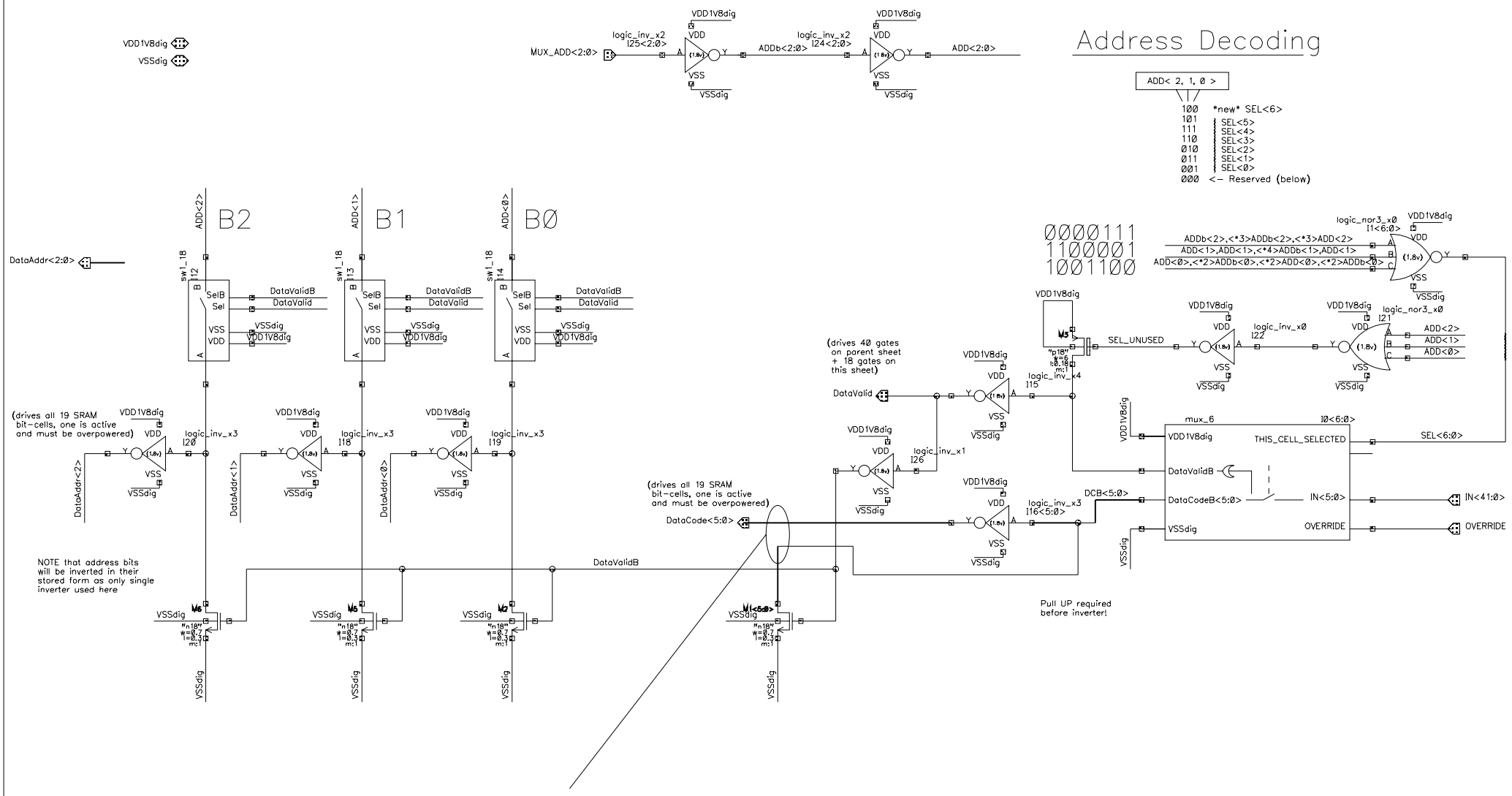
| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | master_row_controller_42.2 |
| Last QA Review | |
| Last Changed | Feb 26 10:07:39 2007 |



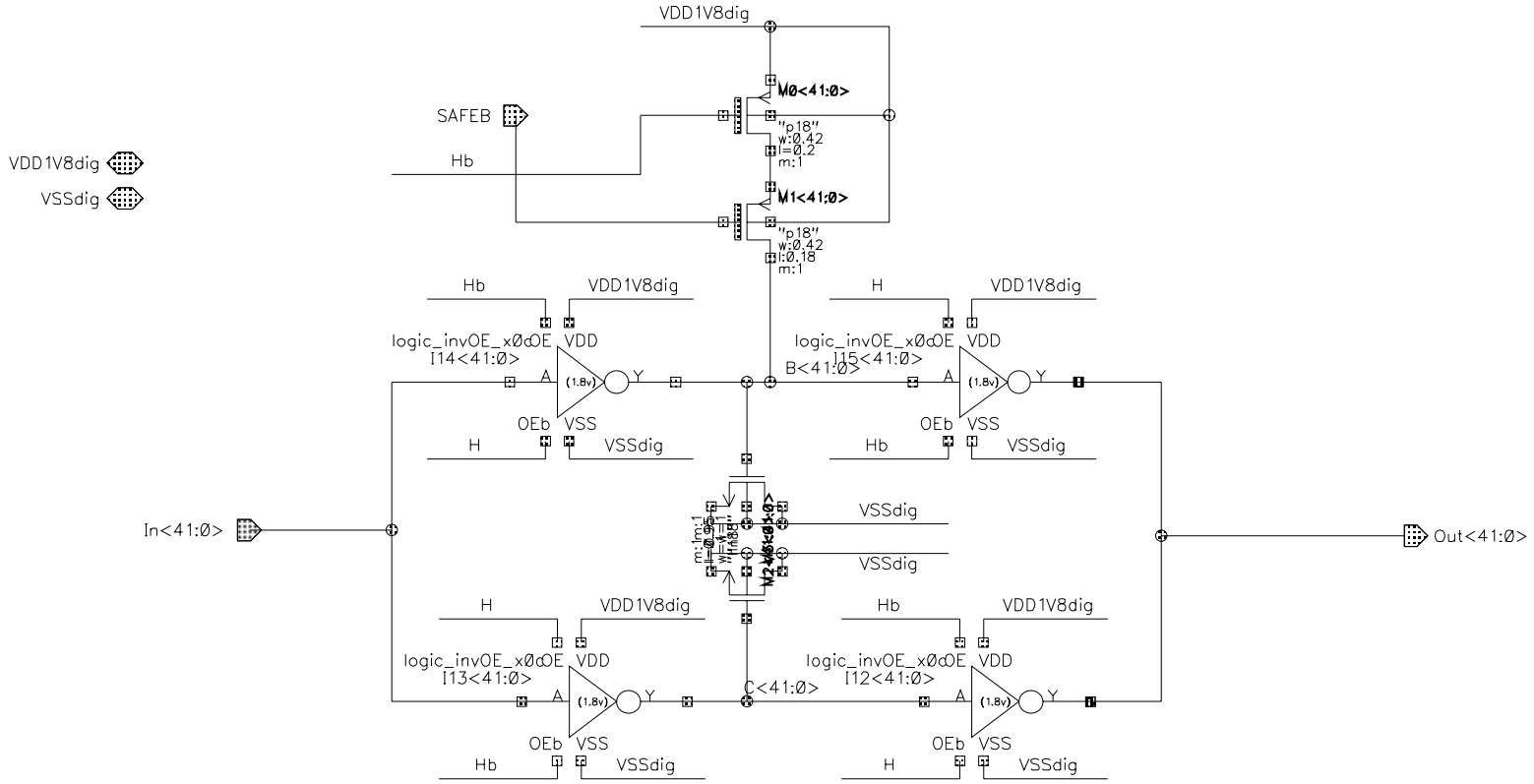

| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | logic_or6 | |
| Last QA Review | | |
| Last Changed | Feb 15 11:02:18 2007 | |

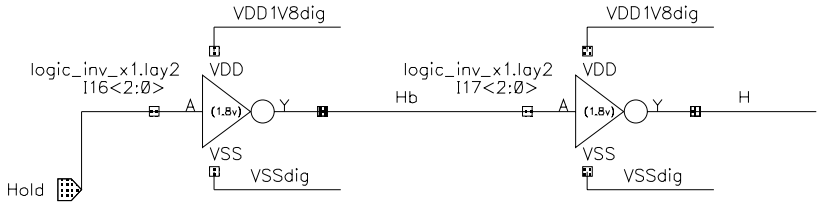



| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | mux_6 |
| Last QA Review | |
| Last Changed | Jan 11 15:41:42 2007 |

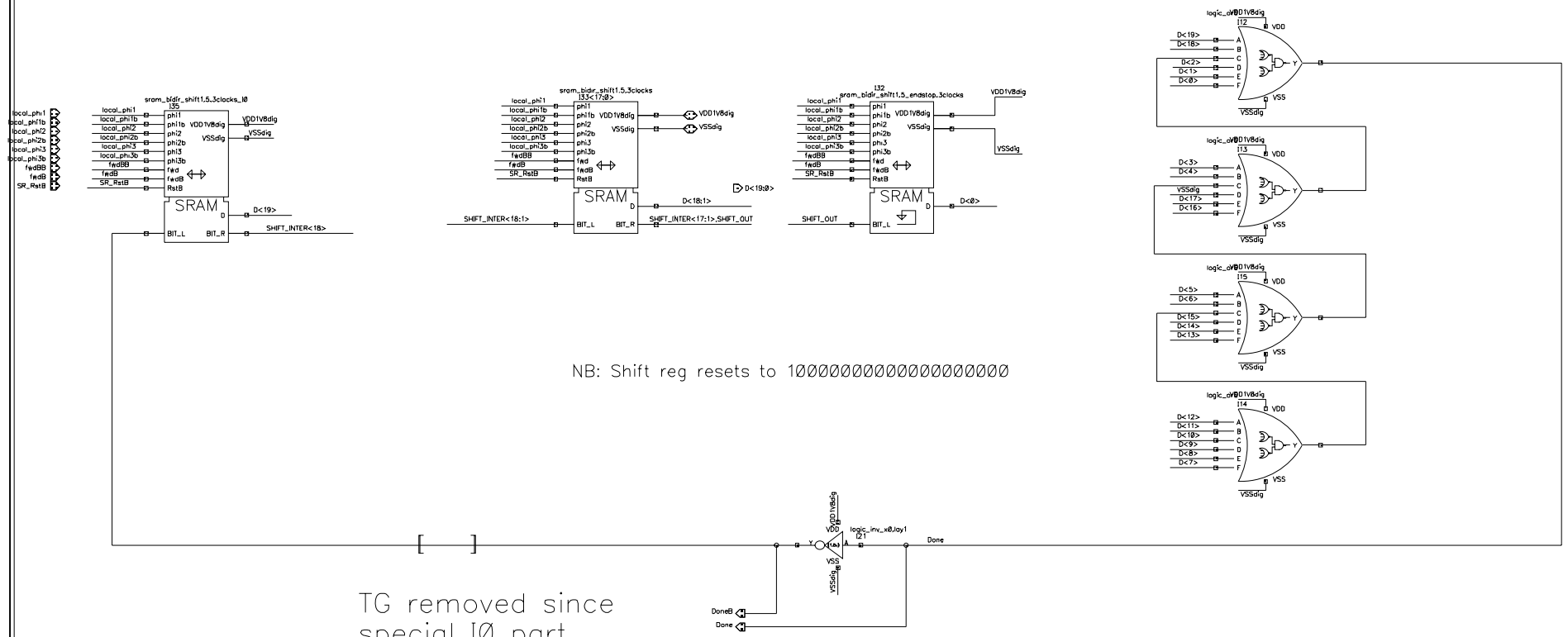



| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | mux_6x7 |
| Last QA Review | |
| Last Changed | Feb 16 10:35:10 2007 |

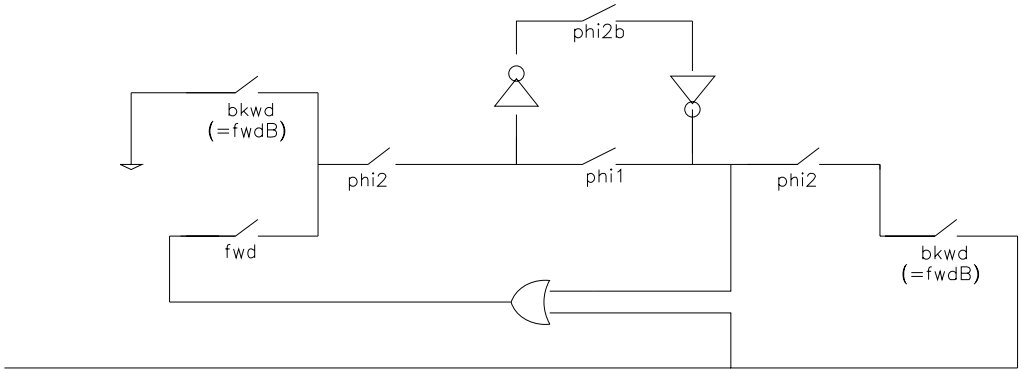



| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | latch_pingpong42_v2.1 |
| Last QA Review | |
| Last Changed | Feb 12 18:50:02 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sram_bidir_shift20.5.3clocks |
| Last QA Review | |
| Last Changed | Feb 15 10:27:03 2007 |




POWER UP

phi1 off
phi2 on
RstB on (low)

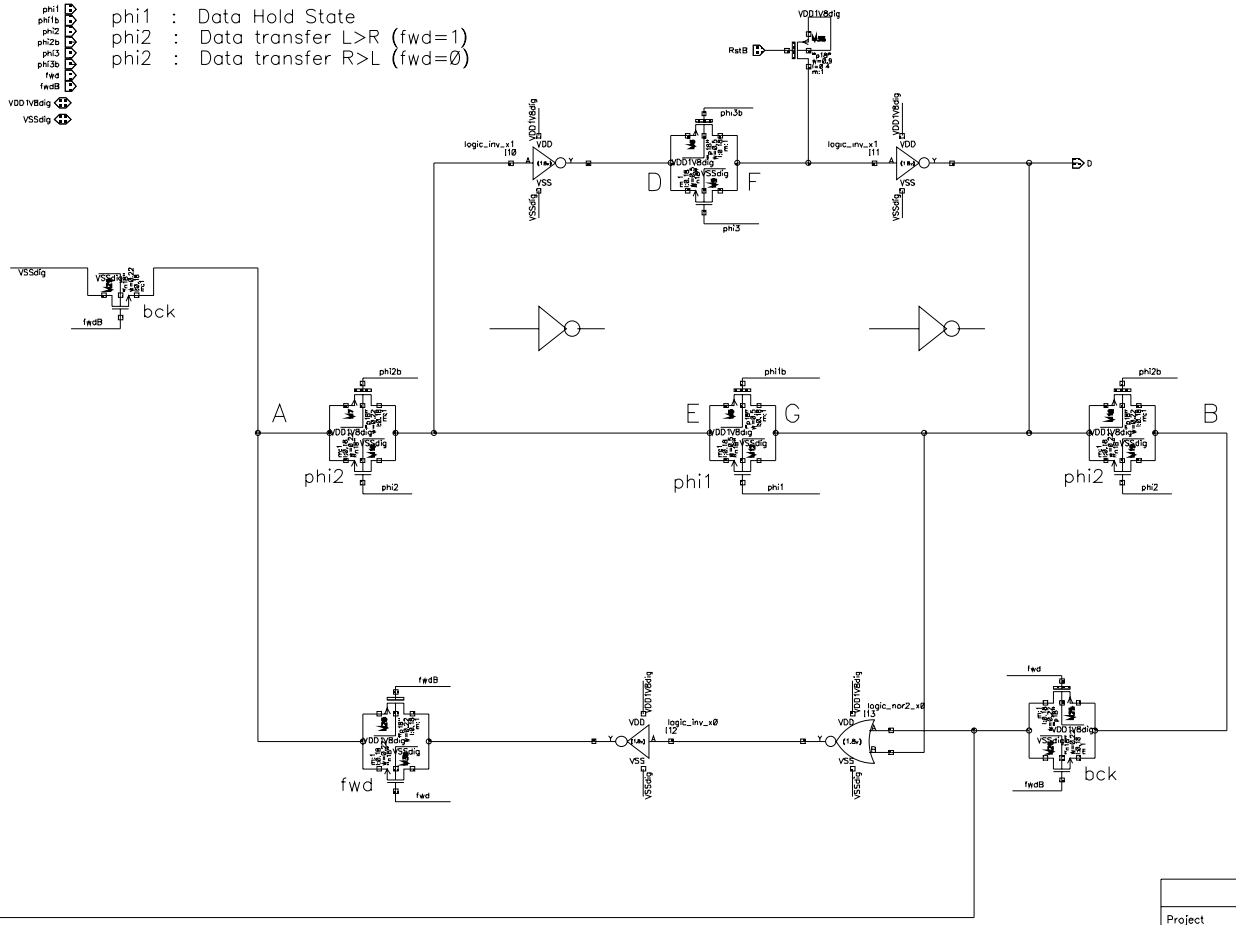
IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low)
during phi2

INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)

phi1 : Data Hold State
phi2 : Data transfer L>R (fwd=1)
phi2 : Data transfer R>L (fwd=Ø)




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sram_bidir_shift1.5_endstop.3clocks |
| Last QA Review | |
| Last Changed | Feb 5 18:18:07 2007 |

New Shiftreg Revision 1.3 3CLOCKS!

> Added third clock for slow edge immunity

Layout inspired changes:

Reset transistor modified wider shorter
All TGs made width Ø.42

Resim & Check [ ]

POWER UP

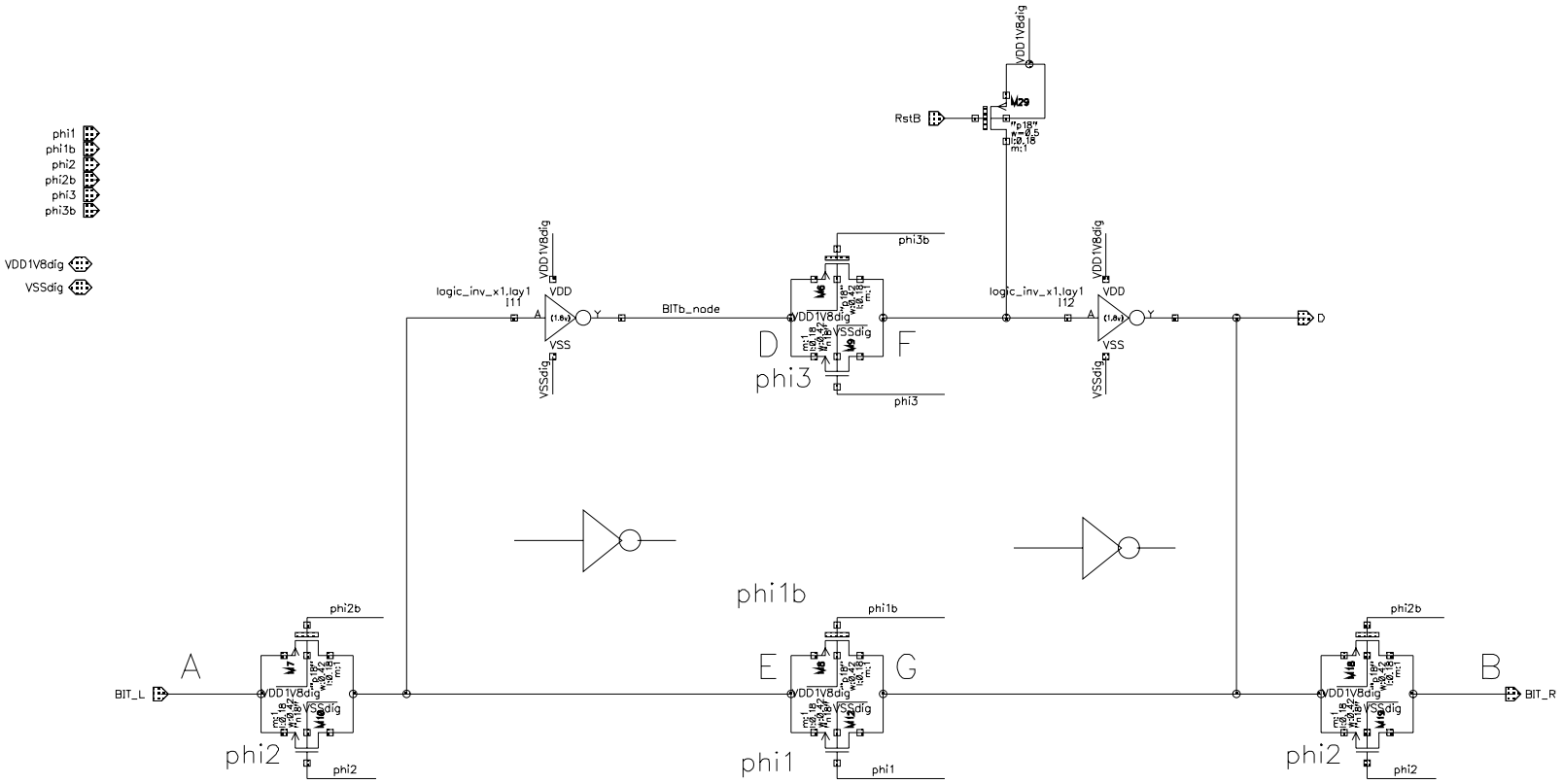
phi1 off
phi2 on
RstB on (low)

IN-SERVICE RESET

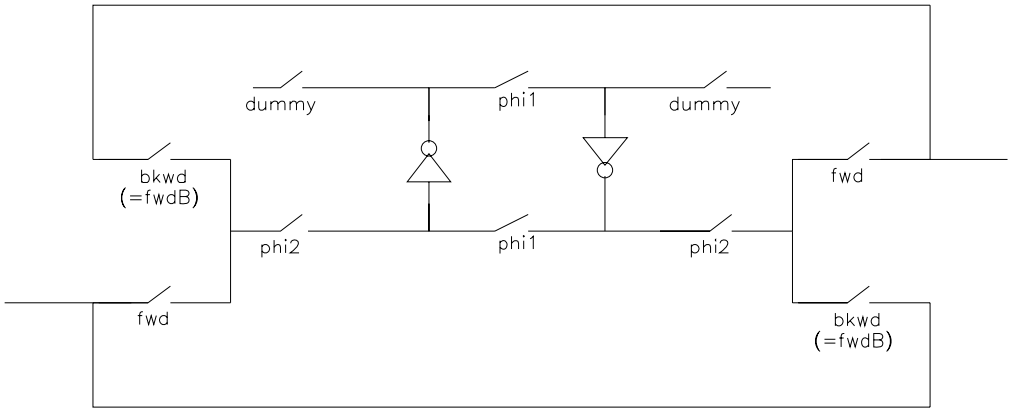
phi1 off
phi2 on
RstB pulsed on (low)
during phi2

INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sram_maskreg_shift1.3_3clocks.lay20x10 |
| Last QA Review | |
| Last Changed | Feb 9 10:48:37 2007 |




POWER UP

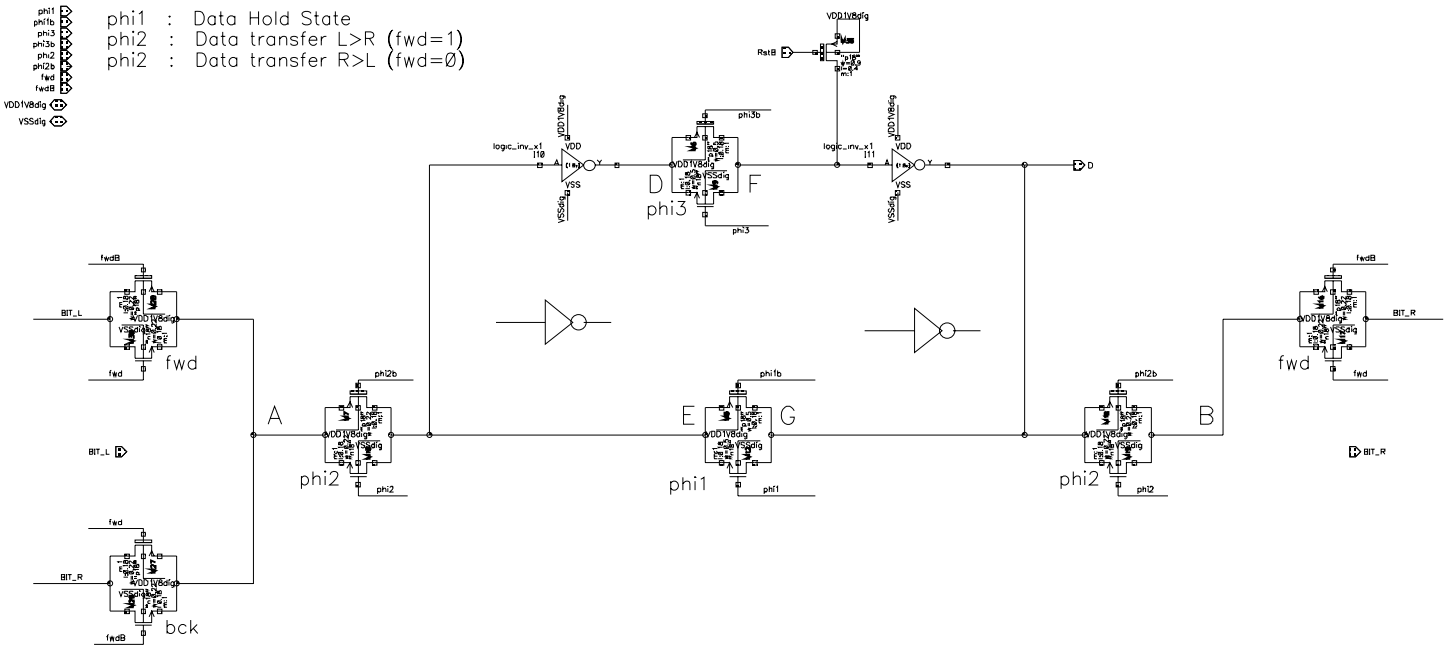
phi1 off
phi2 on
RstB on (low)

IN-SERVICE RESET

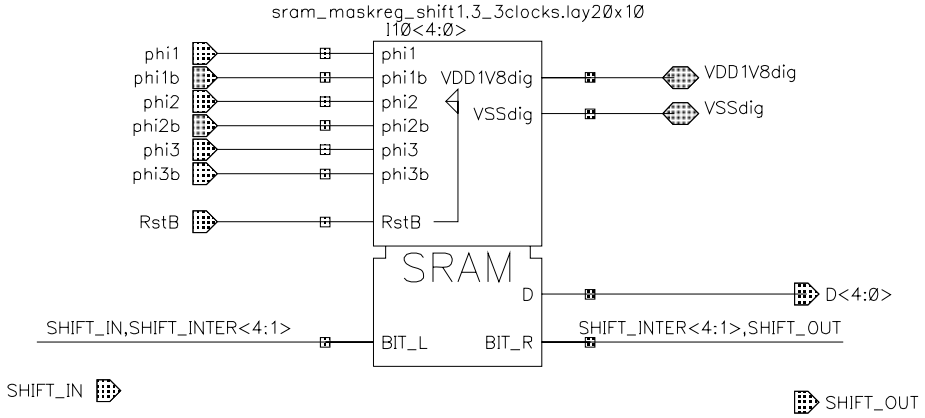
phi1 off
phi2 on
RstB pulsed on (low)
during phi2

INVALID STATE

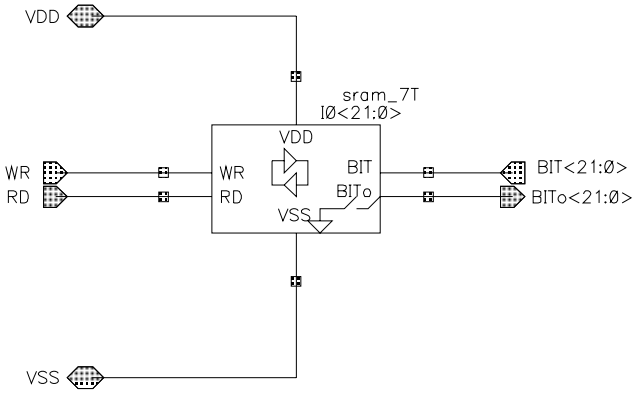
phi1 X
phi2 off (low)
RstB on (low)



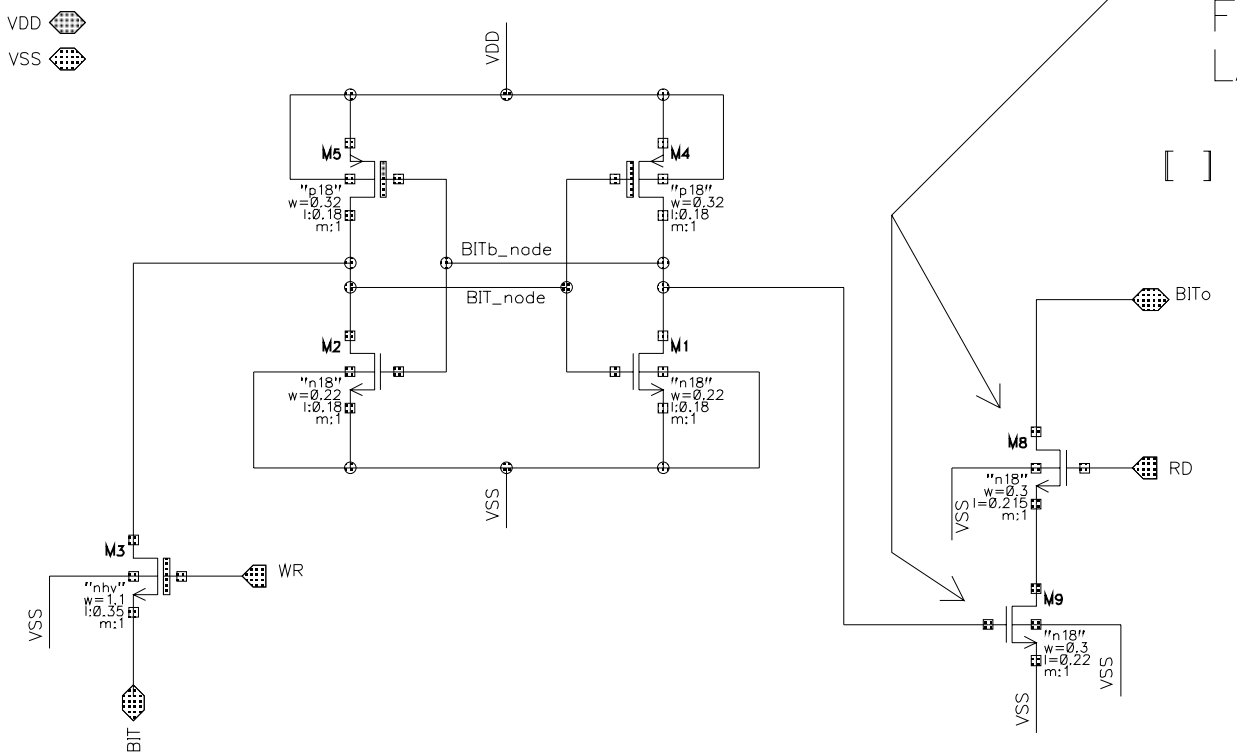

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sram_bidir_shift1.5.3clocks_l0 |
| Last QA Review | |
| Last Changed | Feb 2 14:07:46 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | sram_maskreg_shift5.lay20x10 |
| Last QA Review | |
| Last Changed | Feb 9 11:11:15 2007 |



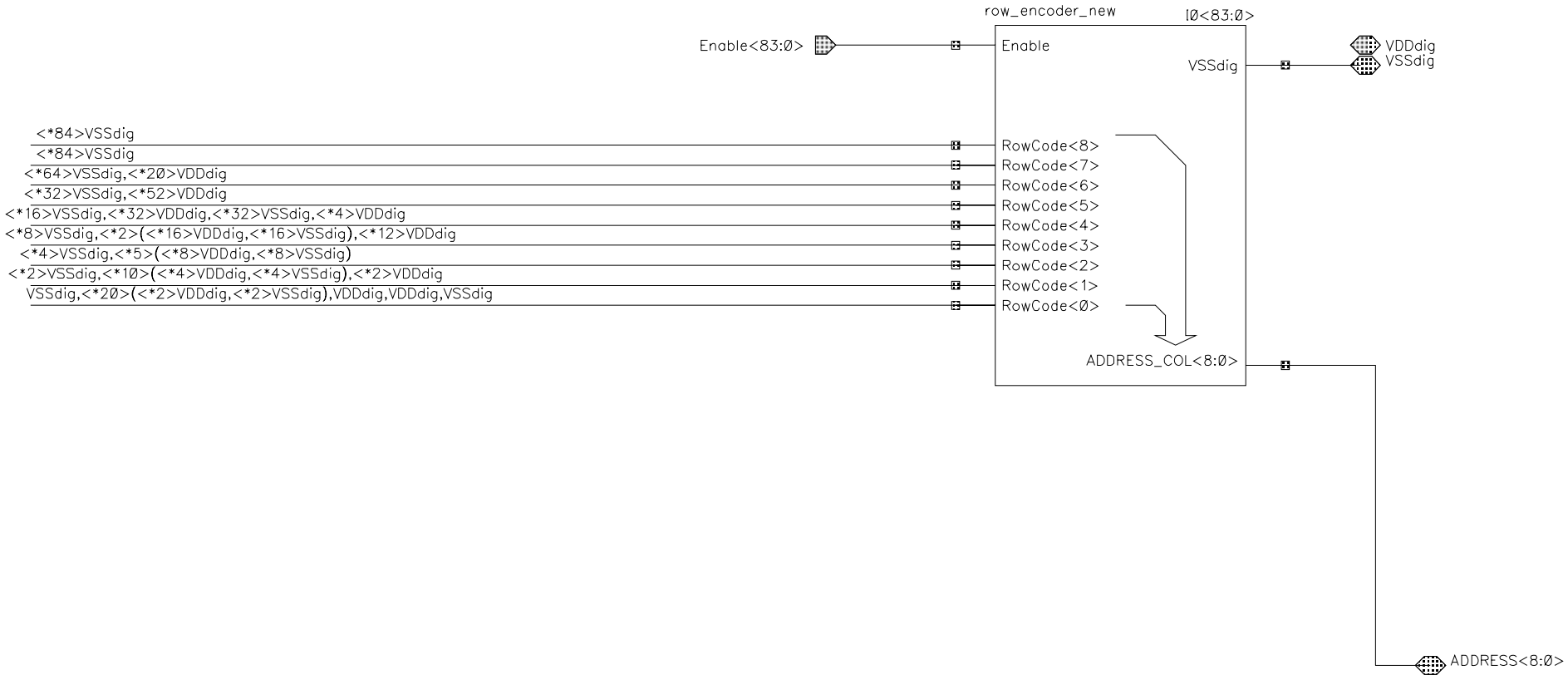

| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | sram_reg7.22 | |
| Last QA Review | | |
| Last Changed | Jan 2 16:08:03 2007 | |



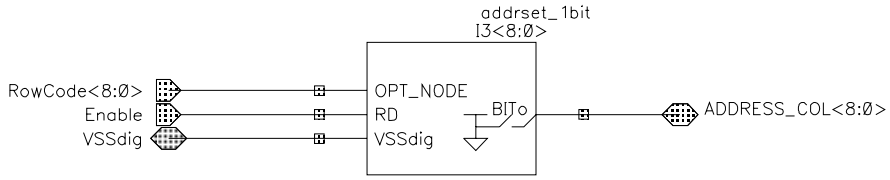

NB: TRANSISTOR LENGTH REDUCED Ø.3um TO Ø.22um FOR BETTER LAYOUT

[ ] RE-SIM CORNERS

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sram_7T |
| Last QA Review | |
| Last Changed | Feb 19 18:38:06 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | row_encoder_84 |
| Last QA Review | |
| Last Changed | Jan 15 09:52:29 2007 |

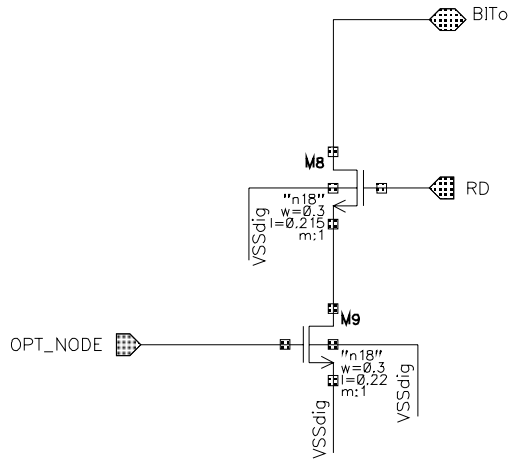



Set Row Code input to the unique row address: with net names in schematics; with repeated tie up/down cells in layout.

GRAY CODE should be used

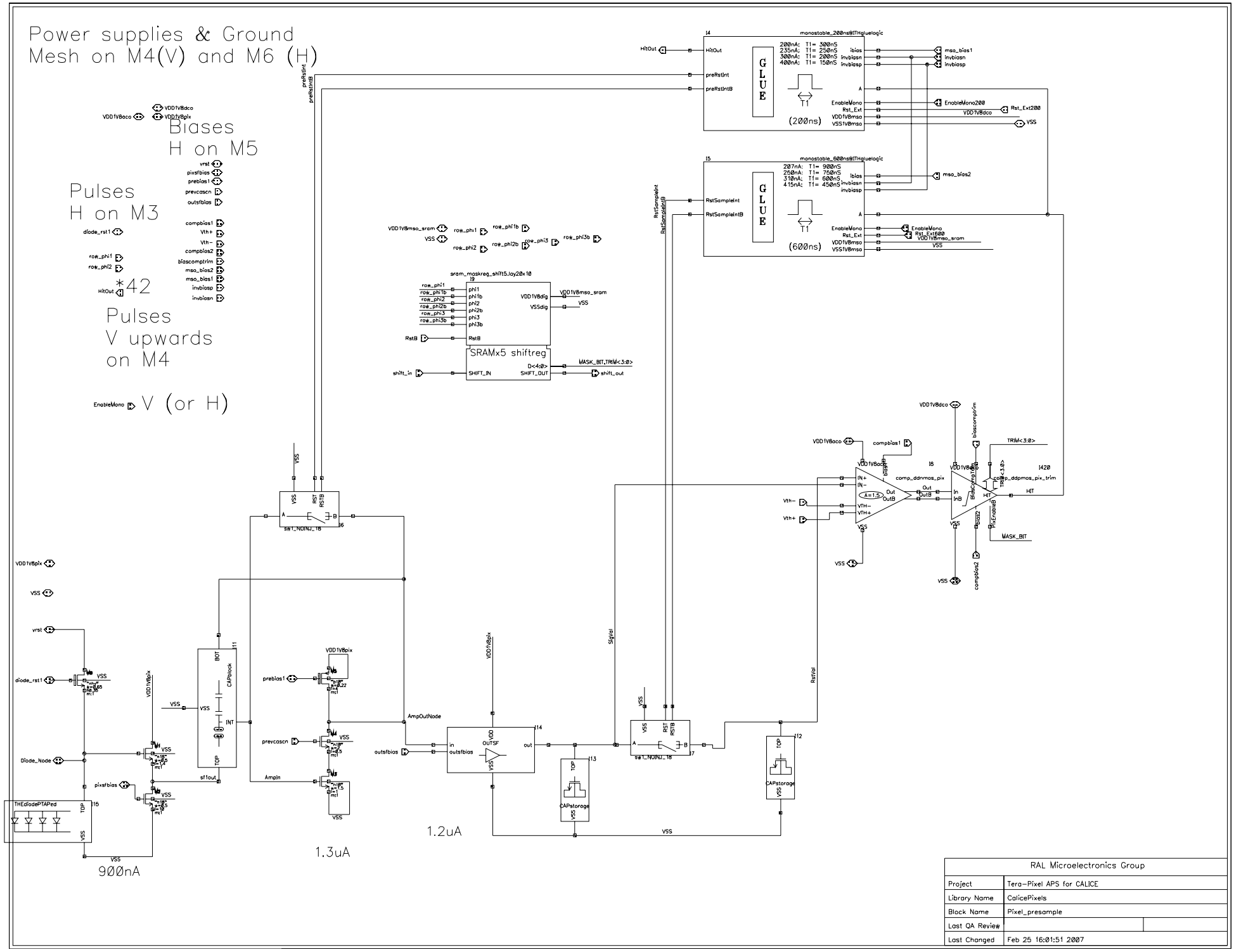
| RAL Microelectronics Group | |
|---|---|
| Project | Tera–Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | row_encoder_new |
| Last QA Review | |
| Last Changed | Jan 15 09:39:09 2007 |

VSSdig

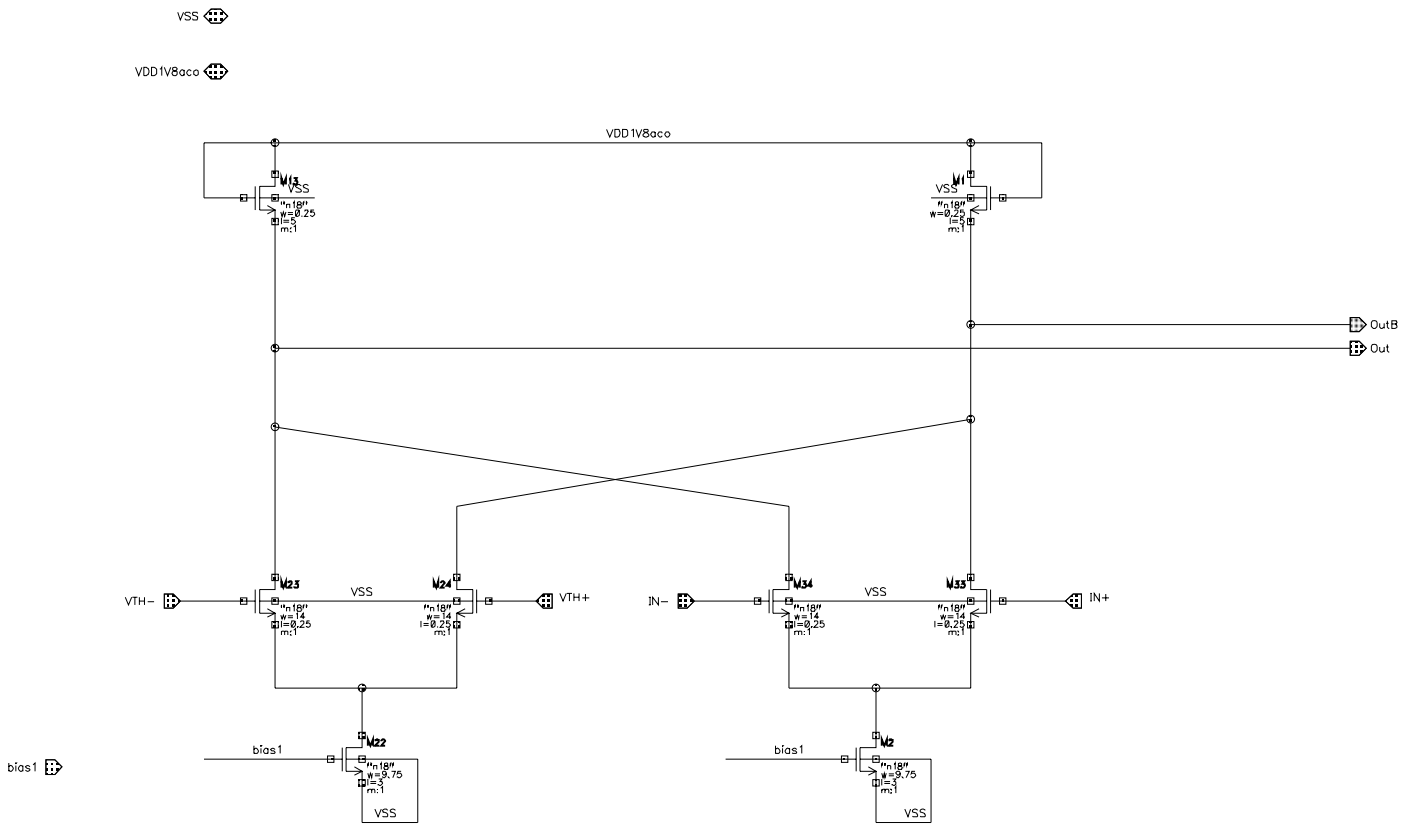



Tie OPT_NODE to either vdd
or gnd to effectively set
the address code that will
be read when RD is asserted

| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | addrset_1bit | |
| Last QA Review | | |
| Last Changed | Jan 15 09:35:52 2007 | |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | Pixel_presample |
| Last QA Review | |
| Last Changed | Feb 25 16:01:51 2007 |

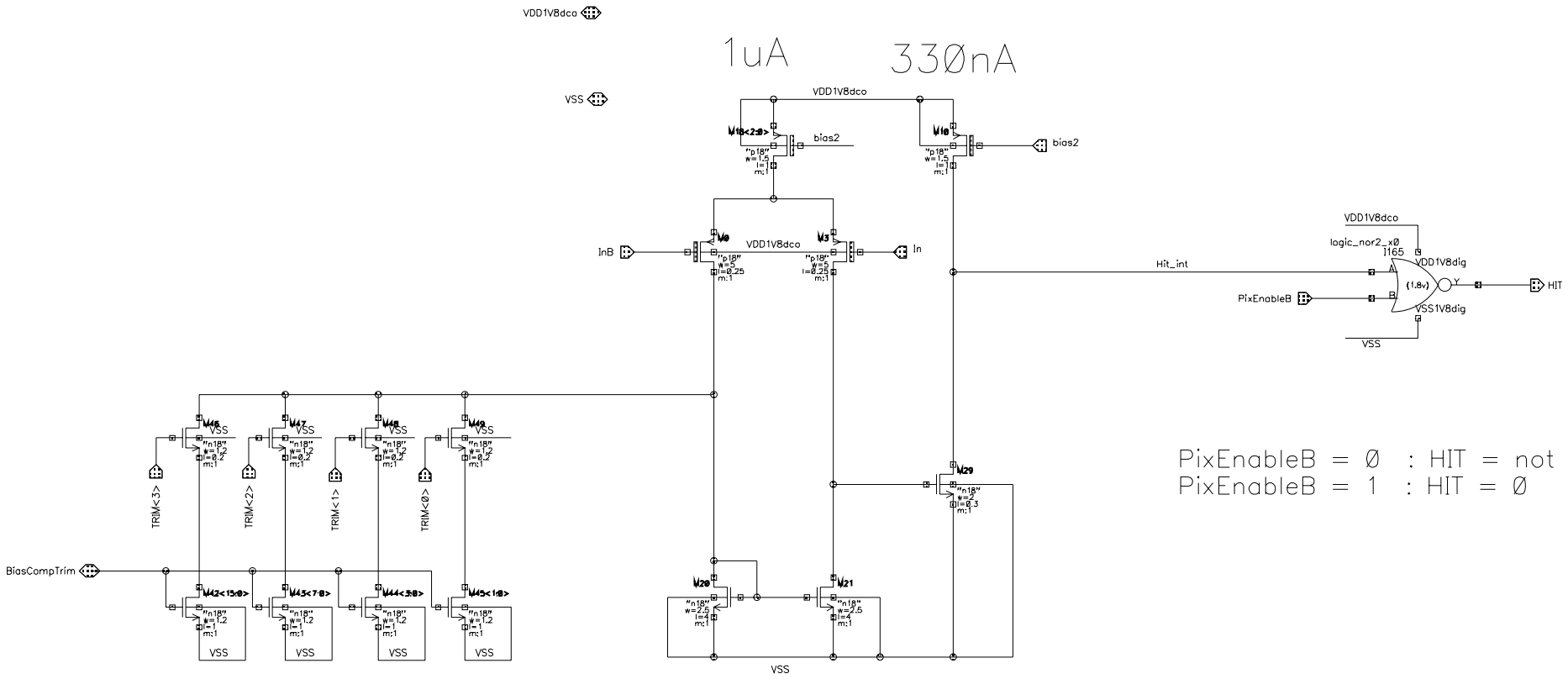



330nA

330nA

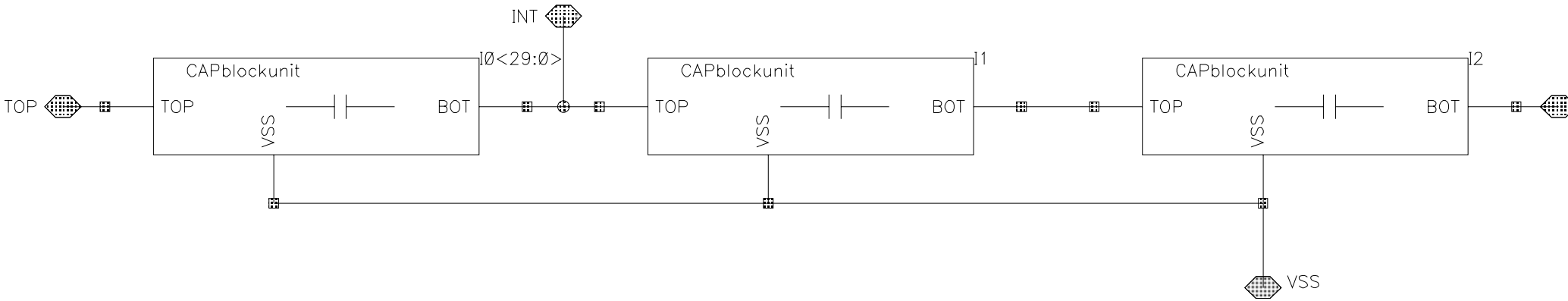
differential (10s of mV)
hit signal wired across
to pmos comparator at row
logic

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | comp_ddnmos_pix |
| Last QA Review | |
| Last Changed | Feb 25 17:02:52 2007 |

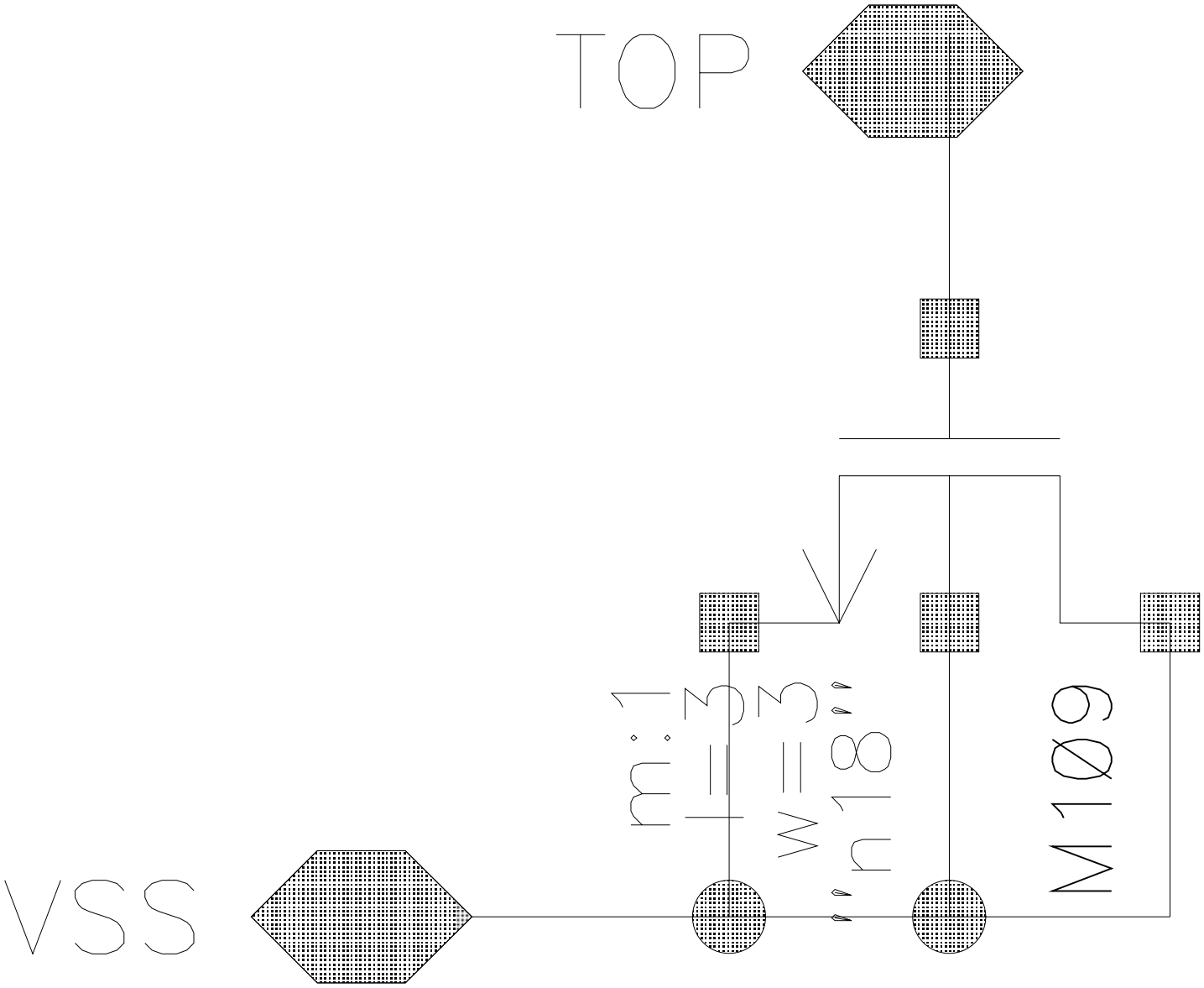


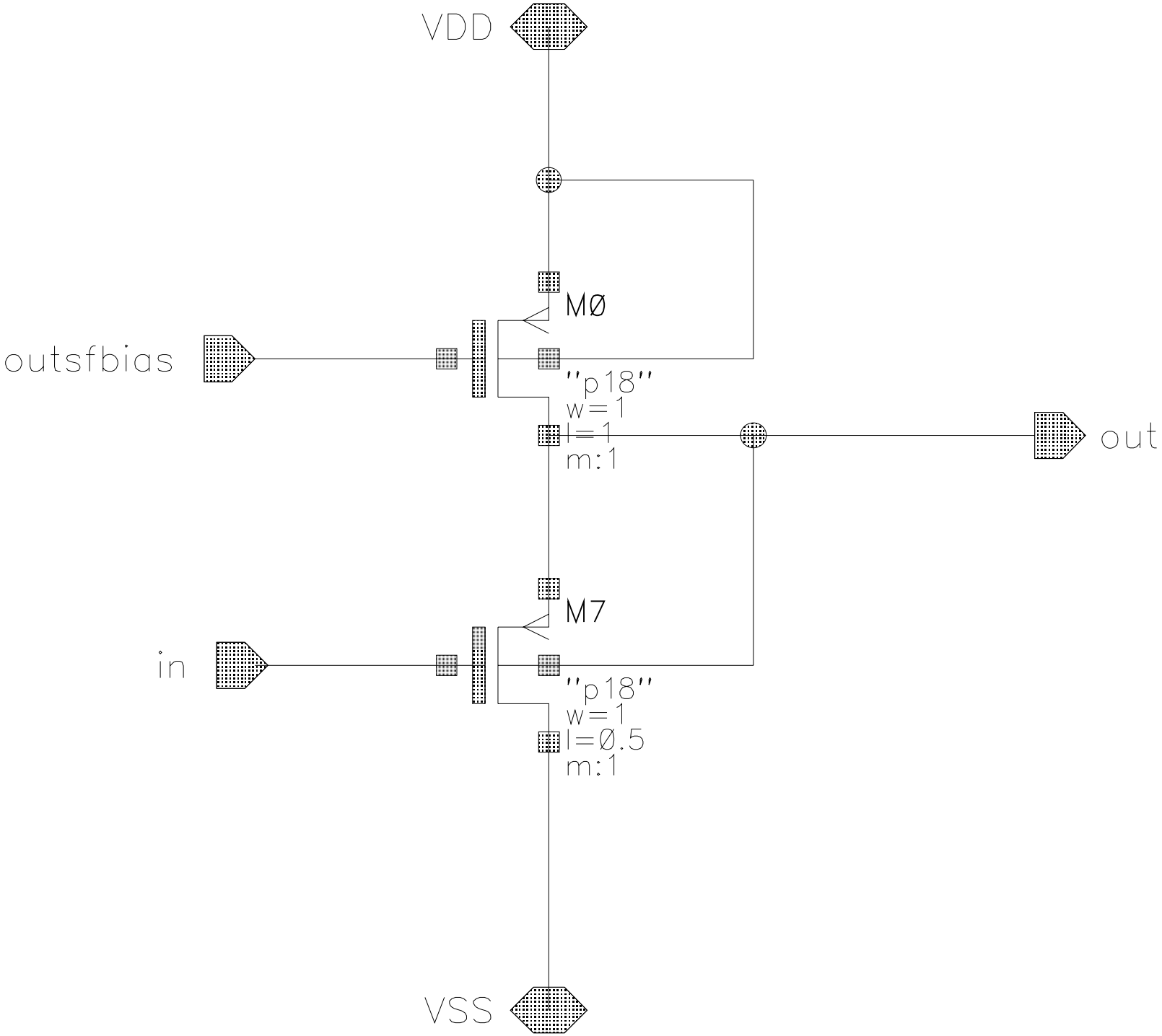

PixEnableB = Ø : HIT = not Hit_Int
PixEnableB = 1 : HIT = Ø

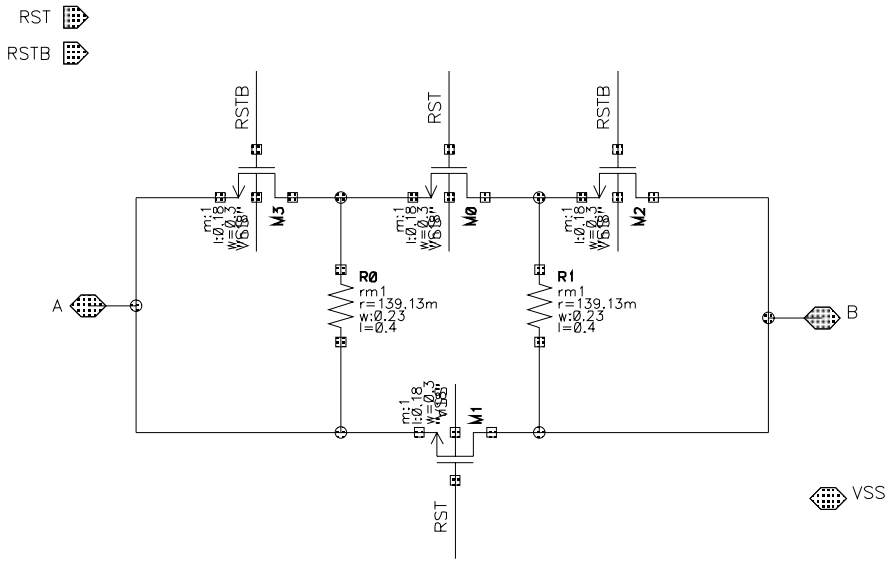
| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | comp_ddpmos_pix_trim |
| Last QA Review | |
| Last Changed | Feb 17 16:53:26 2007 |


INT
I0<29:0>
CAPblockunit
I1
CAPblockunit
I2
CAPblockunit
TOP
TOP
BOT
VSS
TOP
TOP
BOT
VSS
TOP
TOP
BOT
VSS
VSS

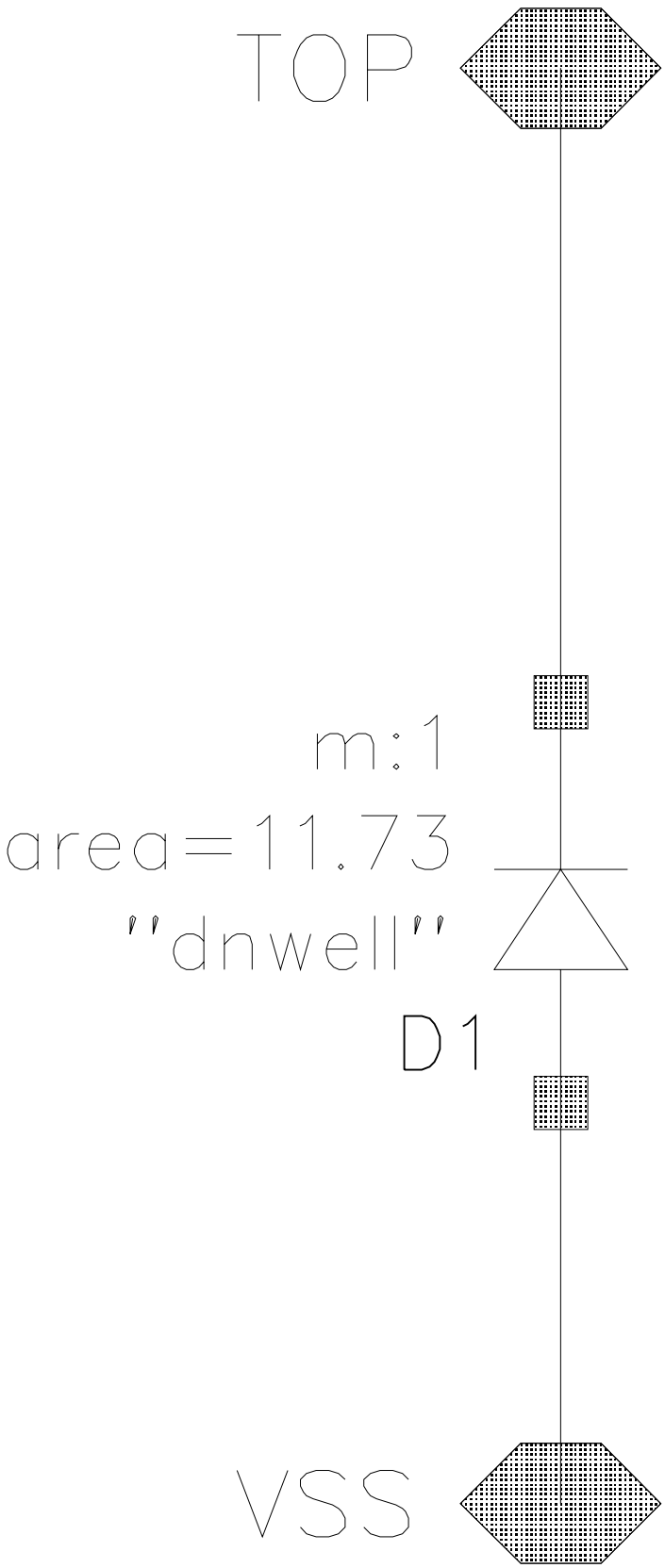
TOP
BOT
cnwnmos_thn3t
C0
"nwcap3t"
S
W=1
wTotal=1
l=1
m:1

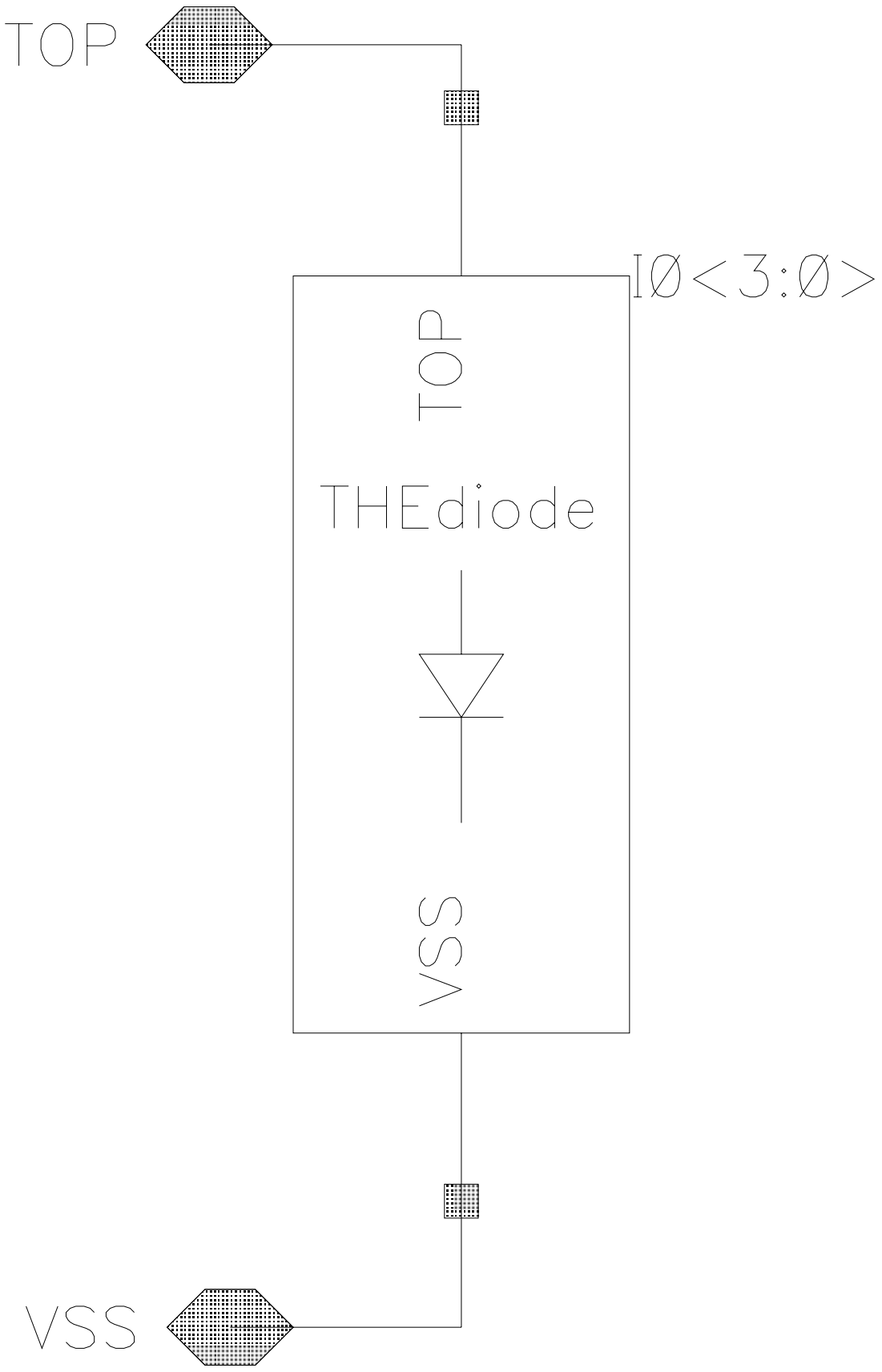

TOP
VSS
m:1
l=33"
w=18"
M109

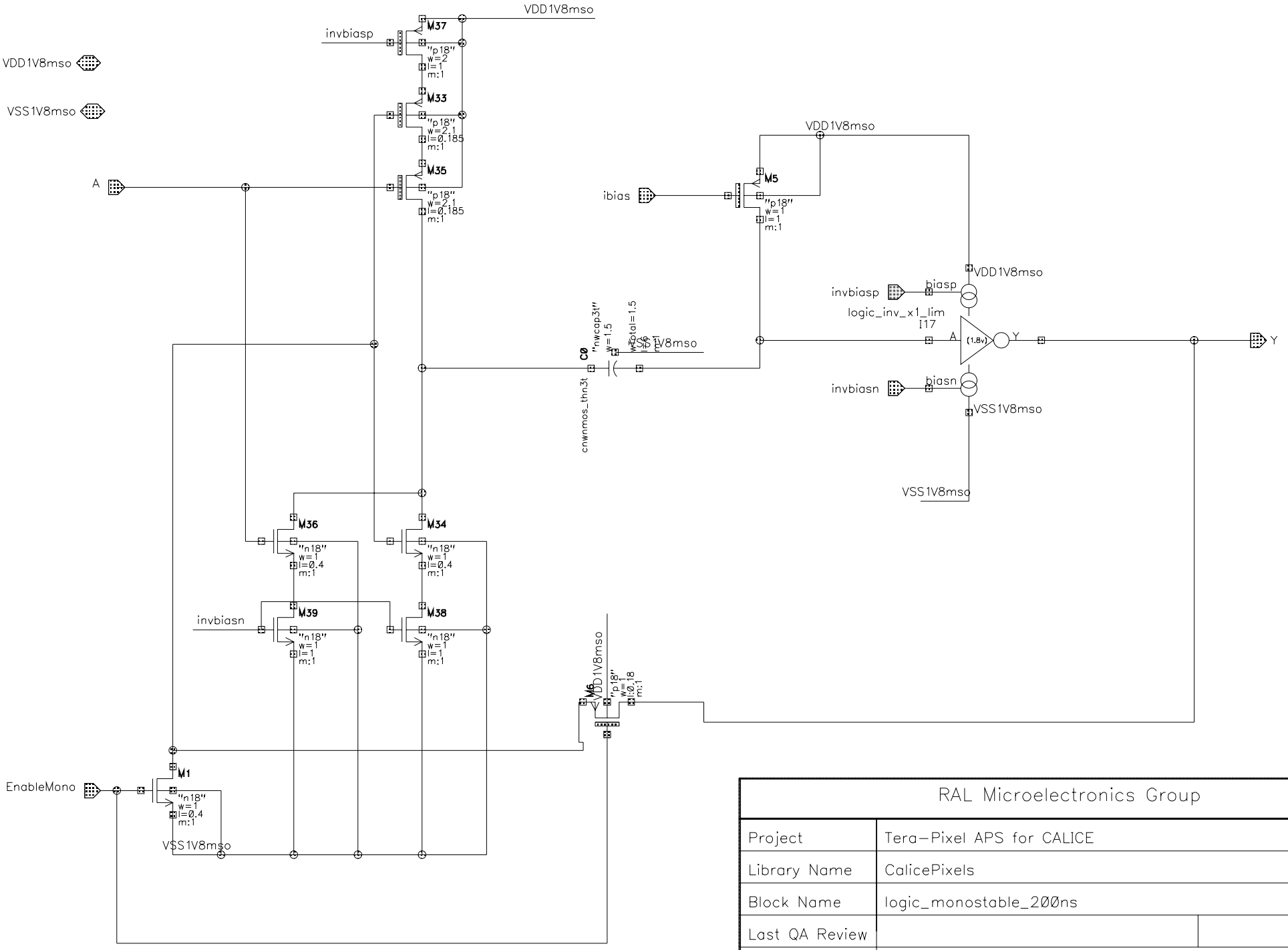

VDD
M0
outsfbias
''p18''
w=1
l=1
m:1
out
M7
in
''p18''
w=1
l=0.5
m:1
VSS



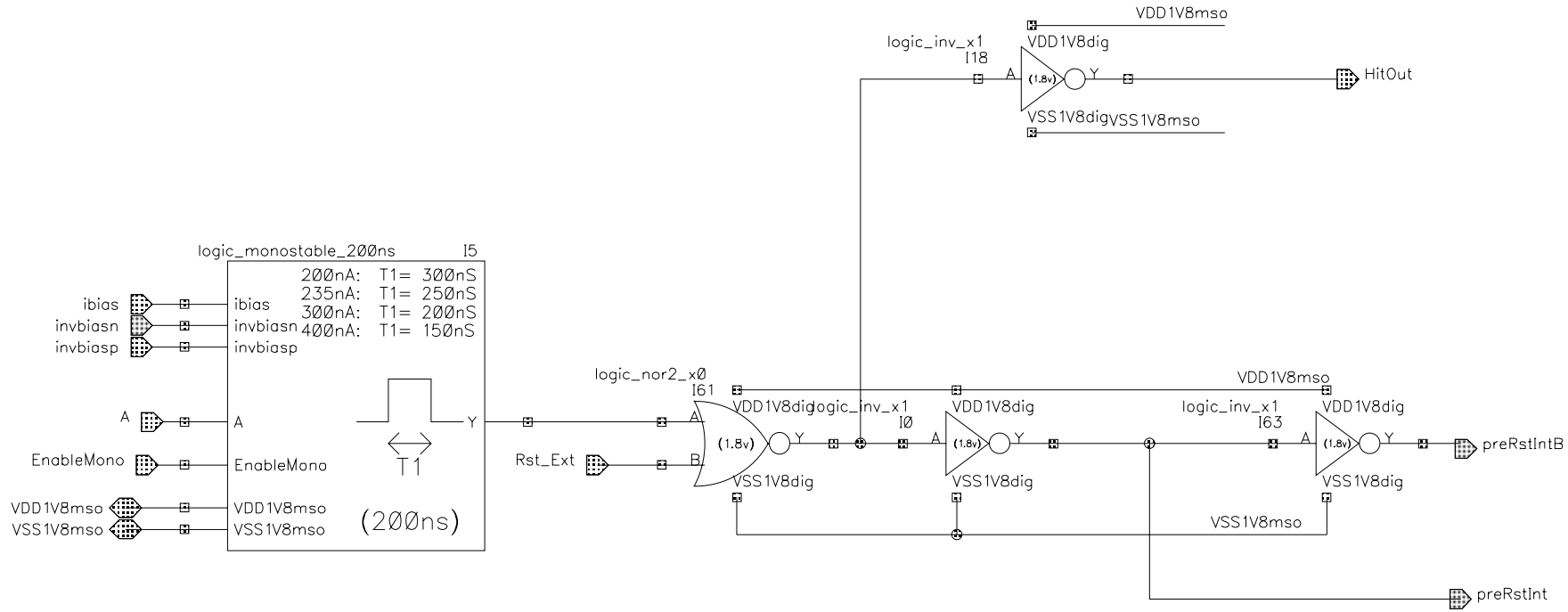

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | sw1_NOINJ_18 |
| Last QA Review | |
| Last Changed | Feb 17 18:13:08 2007 |


TOP
m:1
area=11.73
''dnwell''
D1
VSS

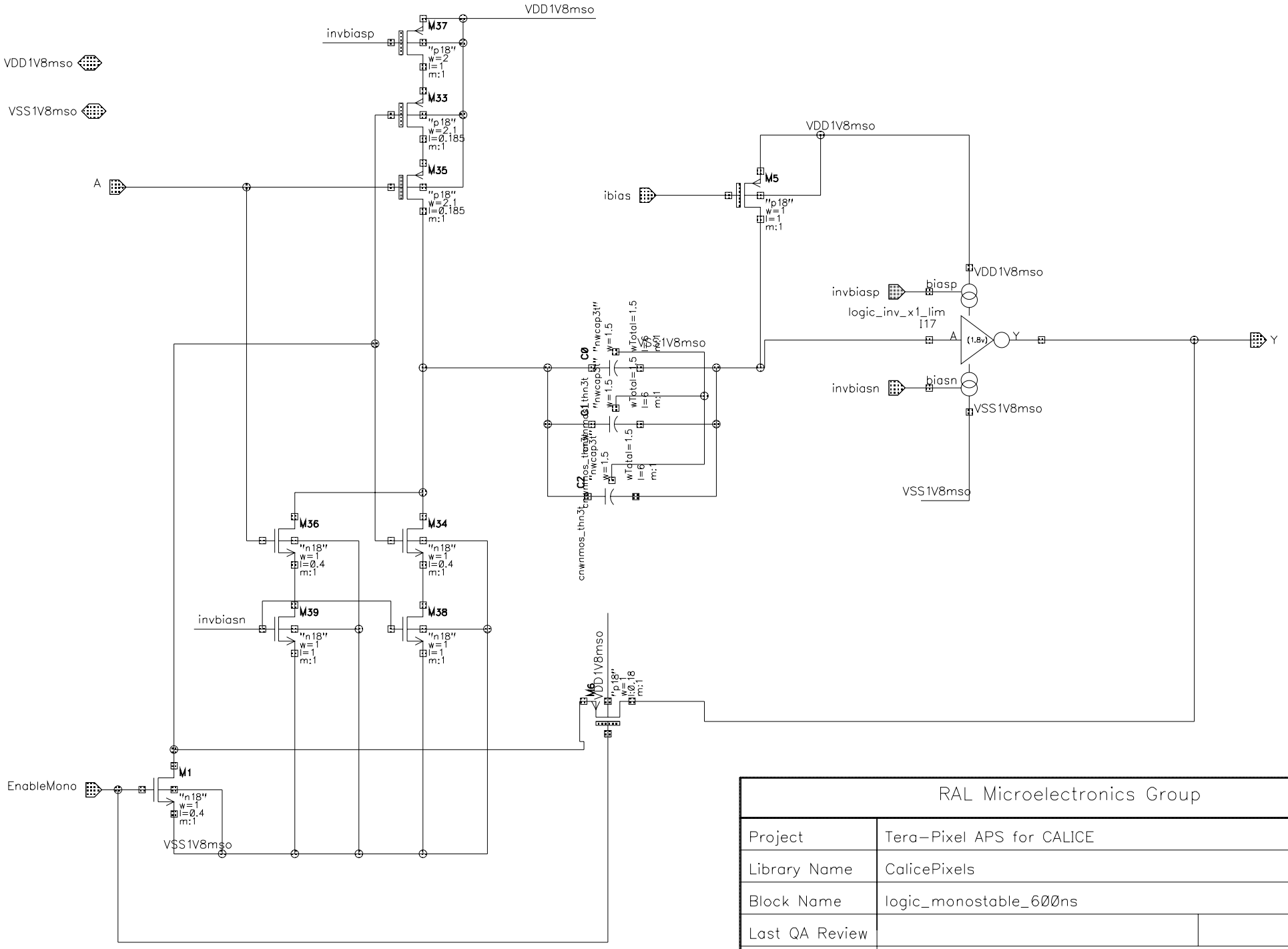

TOP
I0<3:0>
TOP
THEdiode
VSS
VSS



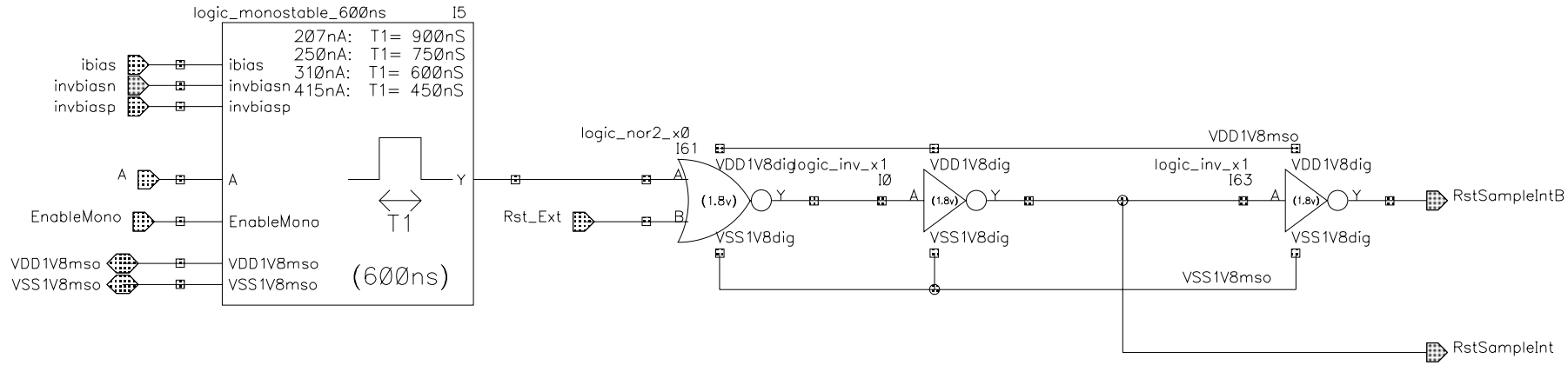

| RAL Microelectronics Group | |
|---|---|
| Project | Tera–Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | logic_monostable_200ns |
| Last QA Review | |
| Last Changed | Feb 14 10:50:33 2007 |



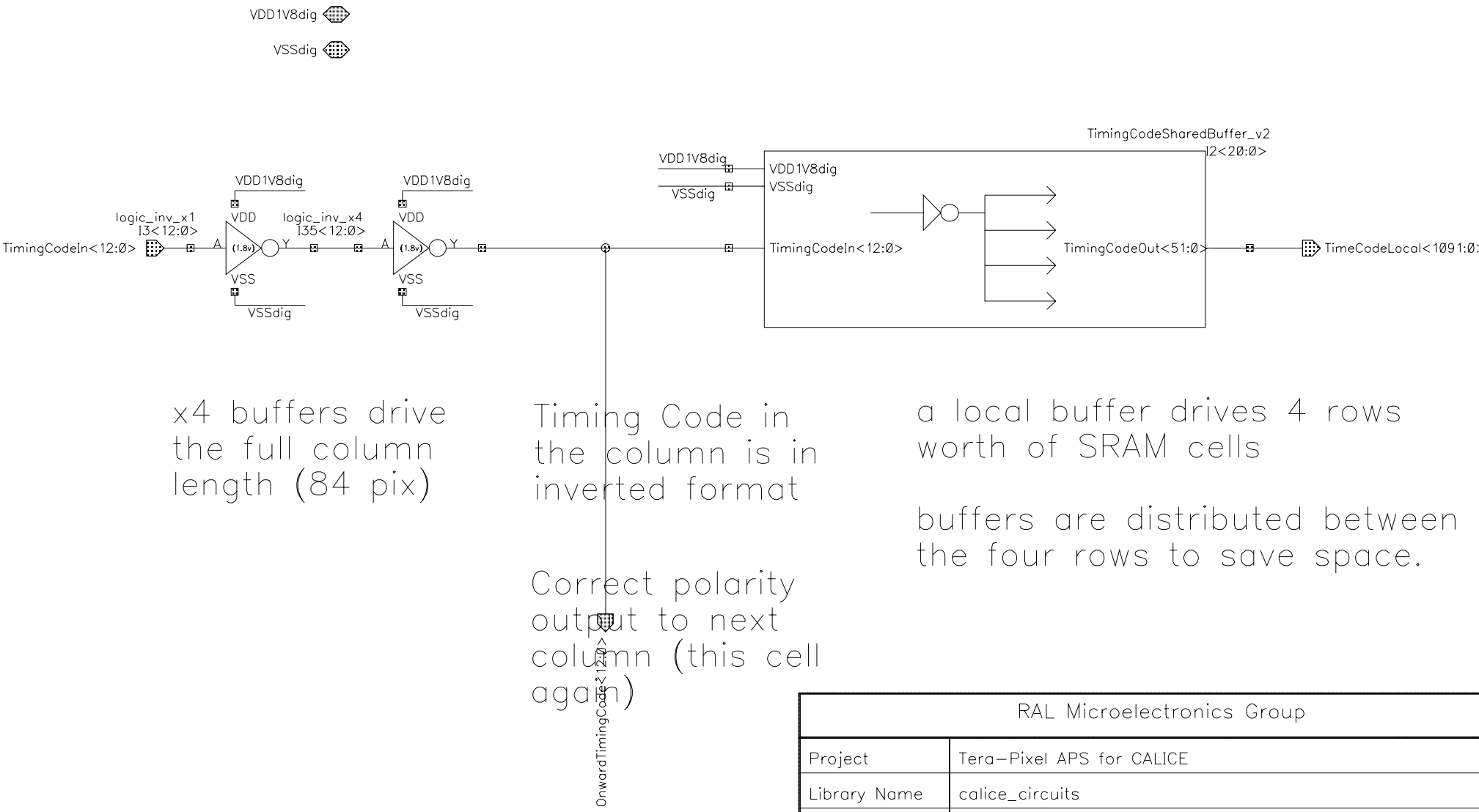

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | monostable_200nsWITHgluelogic |
| Last QA Review | |
| Last Changed | Feb 13 11:47:56 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera–Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | logic_monostable_600ns |
| Last QA Review | |
| Last Changed | Feb 14 10:48:02 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | monostable_600nsWITHgluelogic |
| Last QA Review | |
| Last Changed | Feb 14 10:52:08 2007 |




x4 buffers drive the full column length (84 pix)

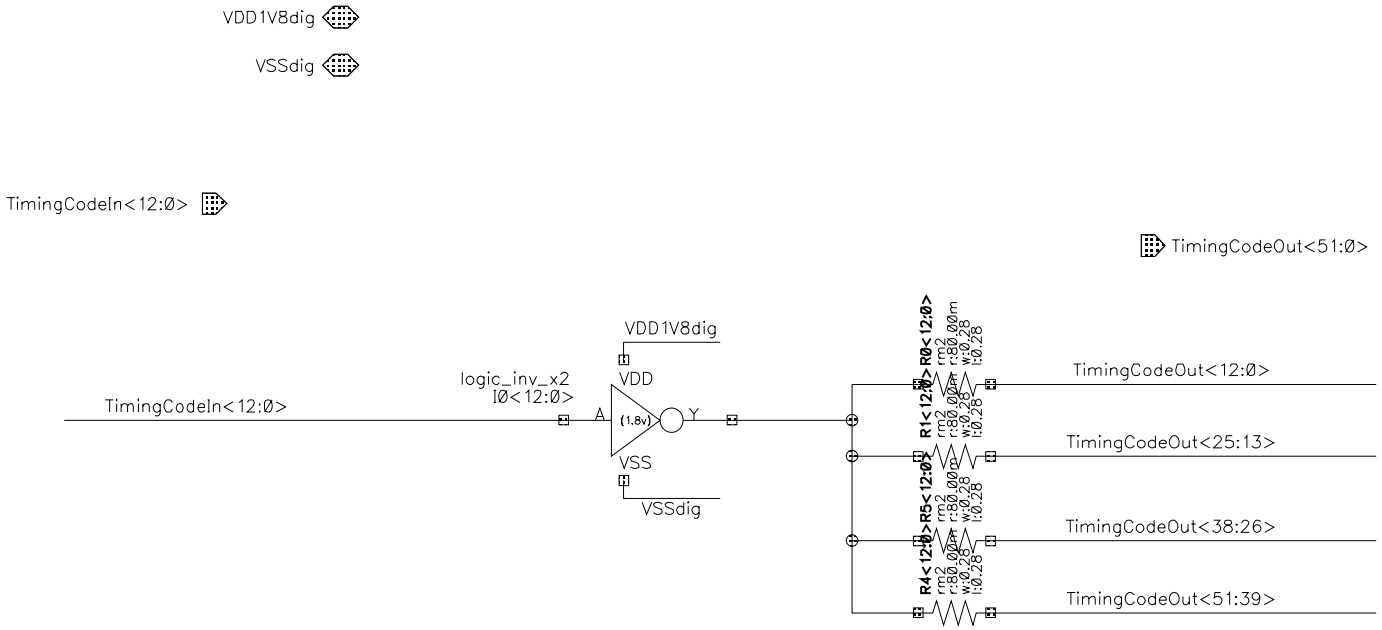
Timing Code in the column is in inverted format

Correct polarity output to next column (this cell again)

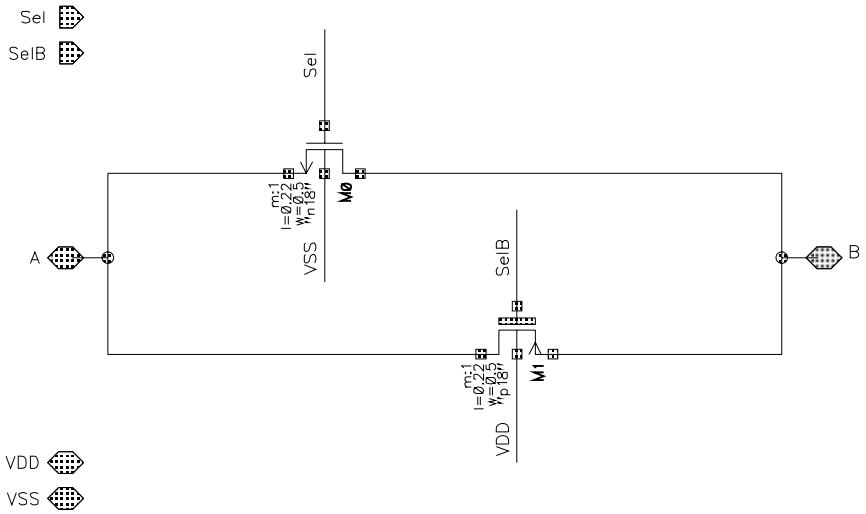
a local buffer drives 4 rows worth of SRAM cells

buffers are distributed between the four rows to save space.

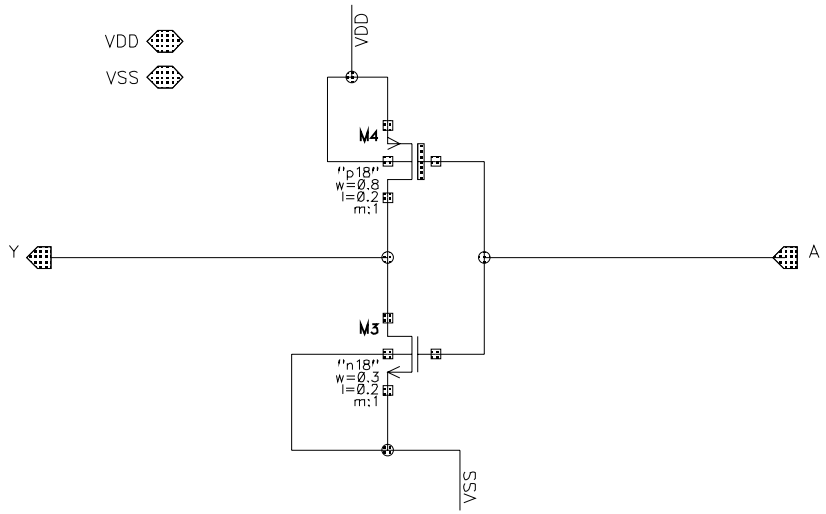
| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | TimingCodeDistribution_v2 | |
| Last QA Review | | |
| Last Changed | Feb 27 17:50:55 2007 | |



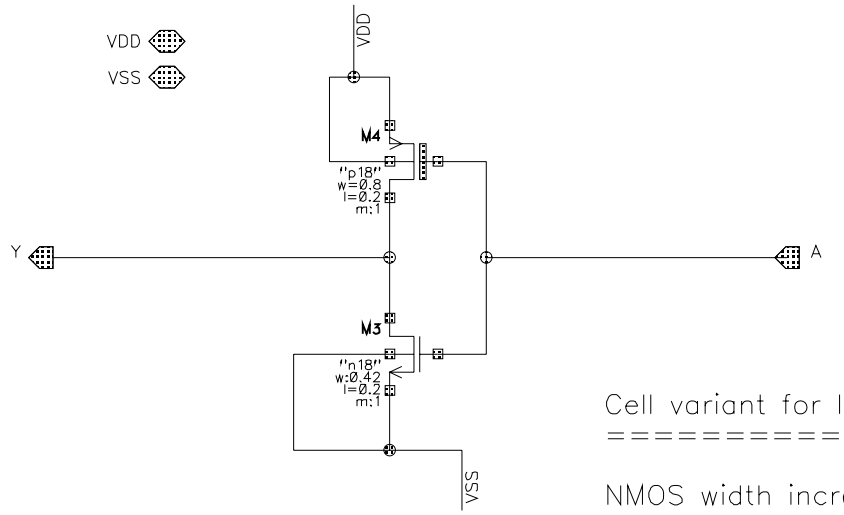

| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera–Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | TimingCodeSharedBuffer_v2 | |
| Last QA Review | | |
| Last Changed | Feb 20 09:23:44 2007 | |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | sw1_18 |
| Last QA Review | |
| Last Changed | Sep 28 11:41:21 2006 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x0 |
| Last QA Review | |
| Last Changed | Sep 28 11:41:11 2006 |

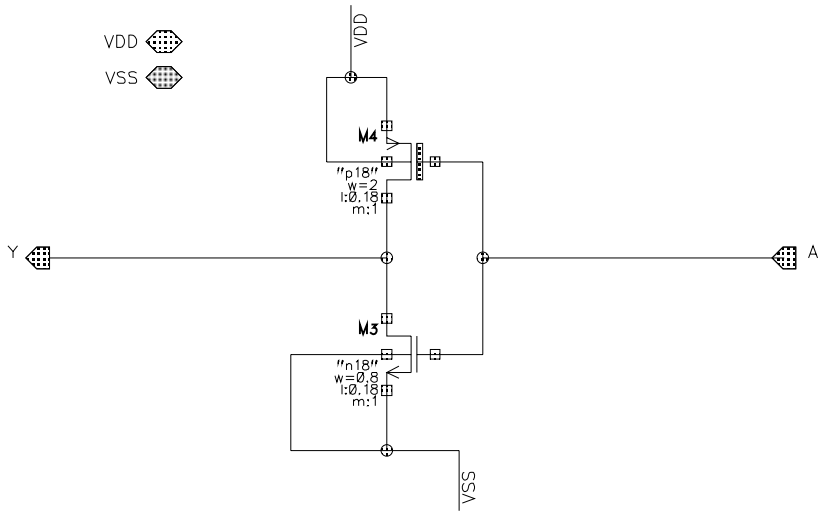



Cell variant for layout ".lay1"

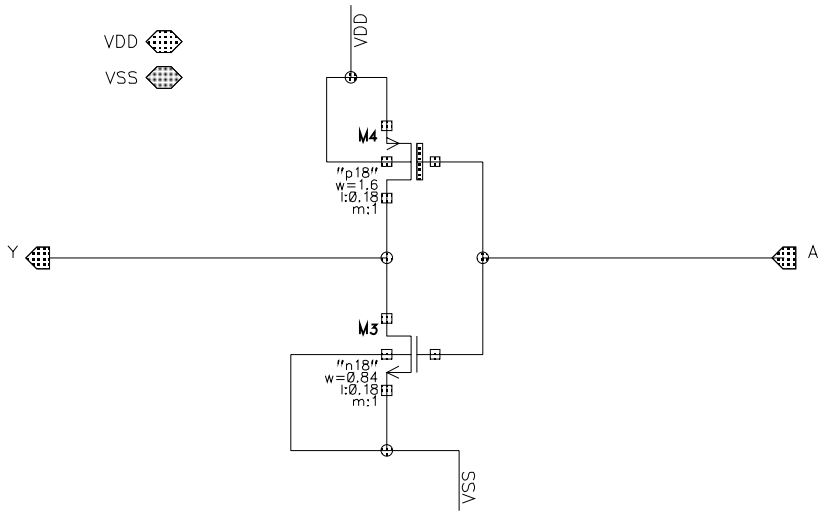
==========

NMOS width increased from 0.3 to 0.42um

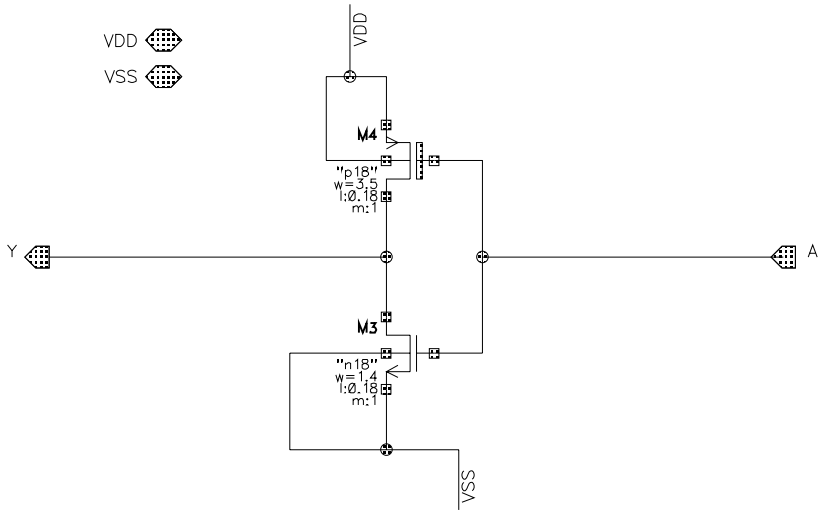
| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | logic_inv_x0.lay1 | |
| Last QA Review | | |
| Last Changed | Jan 11 15:41:07 2007 | |



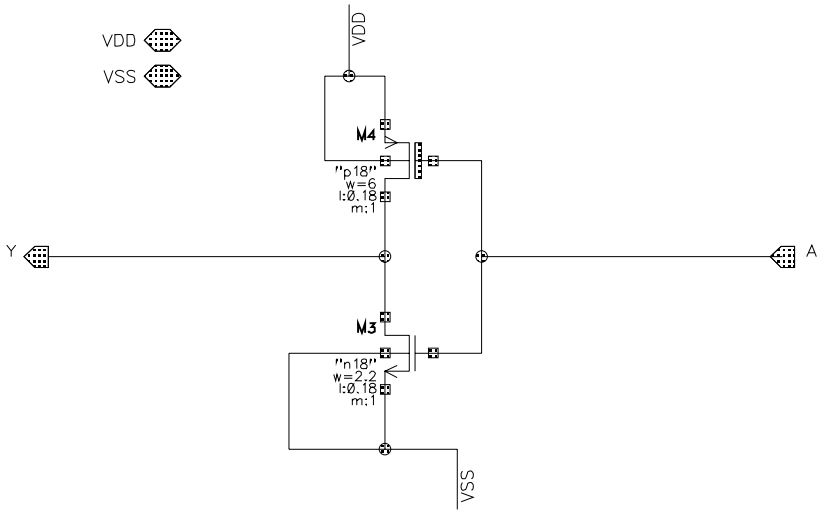

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x1 |
| Last QA Review | |
| Last Changed | Sep 28 11:46:11 2006 |



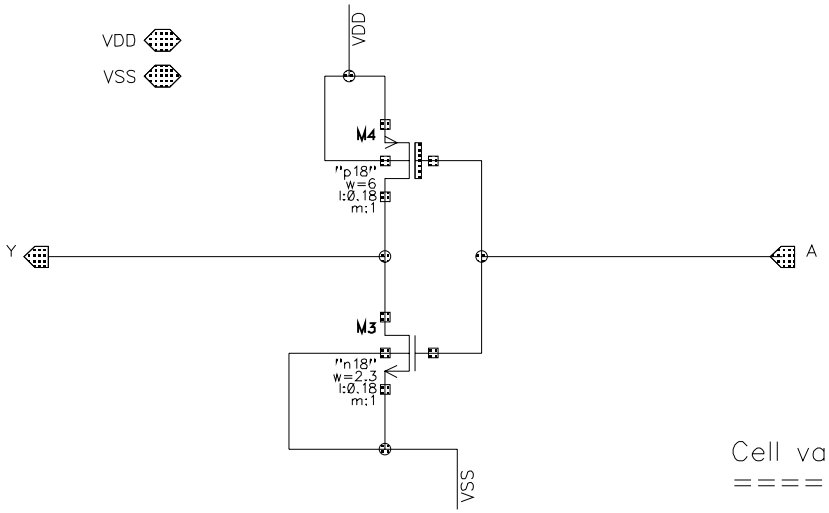

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x1.lay2 |
| Last QA Review | |
| Last Changed | Feb 12 18:45:22 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x2 |
| Last QA Review | |
| Last Changed | Sep 28 11:45:54 2006 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x3 |
| Last QA Review | |
| Last Changed | Sep 28 11:42:15 2006 |

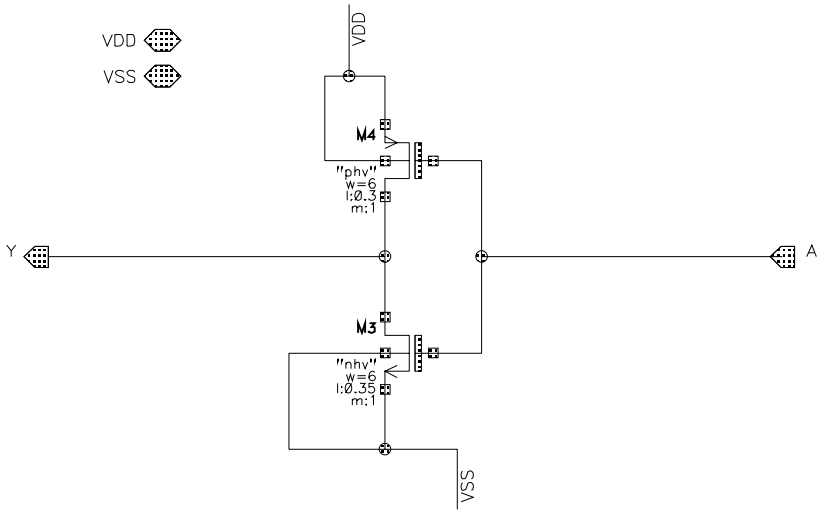



Cell variant for layout ".lay1"

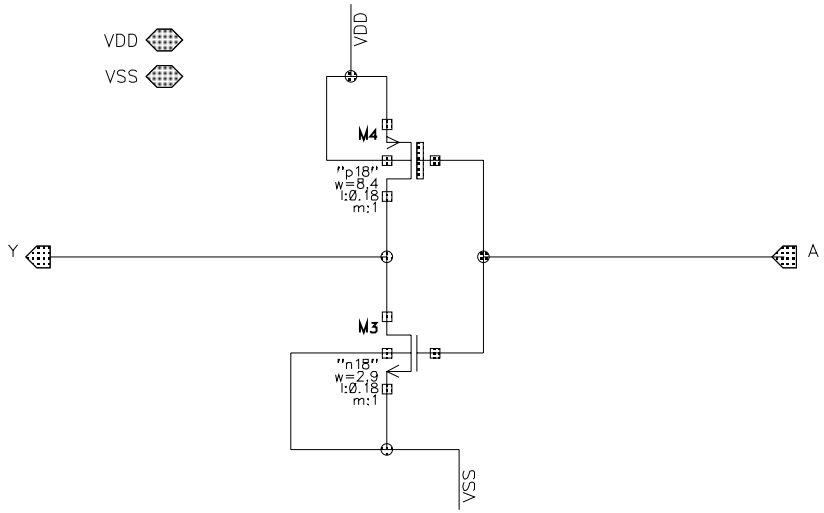
==========

NMOS width increased from 2.2 to 2.3

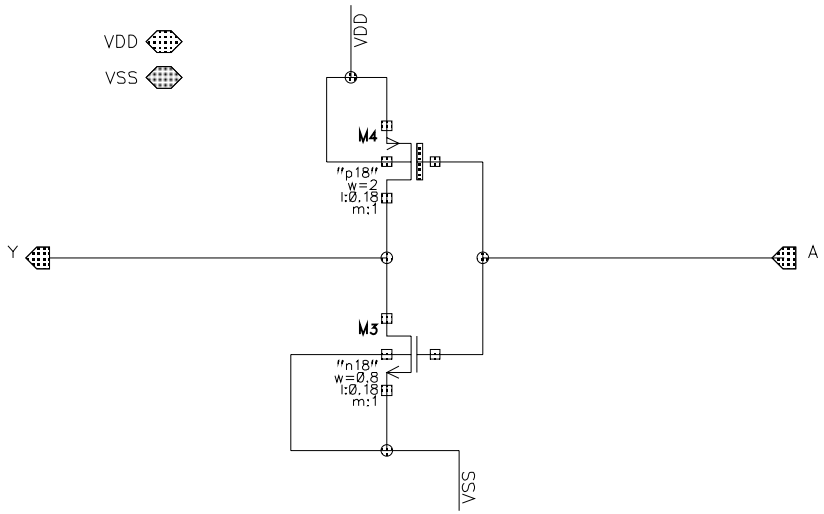
| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | logic_inv_x3.lay1 | |
| Last QA Review | | |
| Last Changed | Jan 10 14:27:47 2007 | |



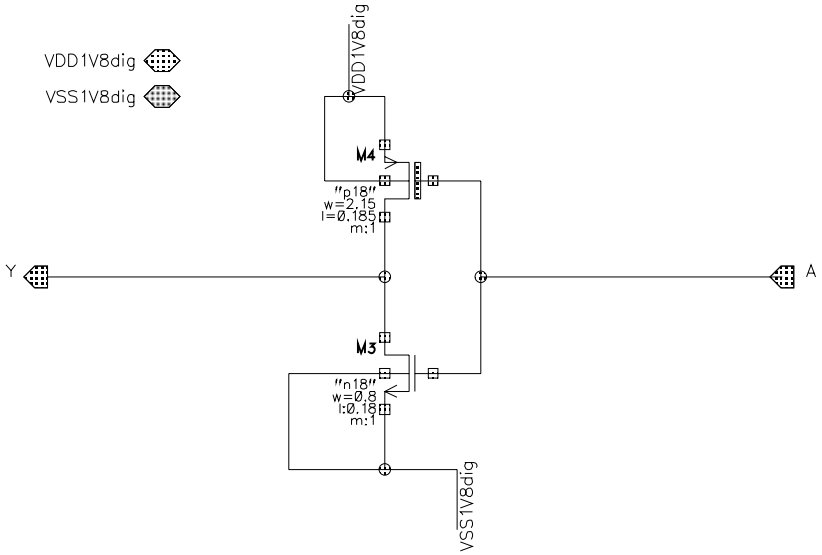

| RAL Microelectronics Group | |
|---|---|
| Project | Tera–Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x3_hv |
| Last QA Review | |
| Last Changed | Sep 29 15:18:48 2ØØ6 |



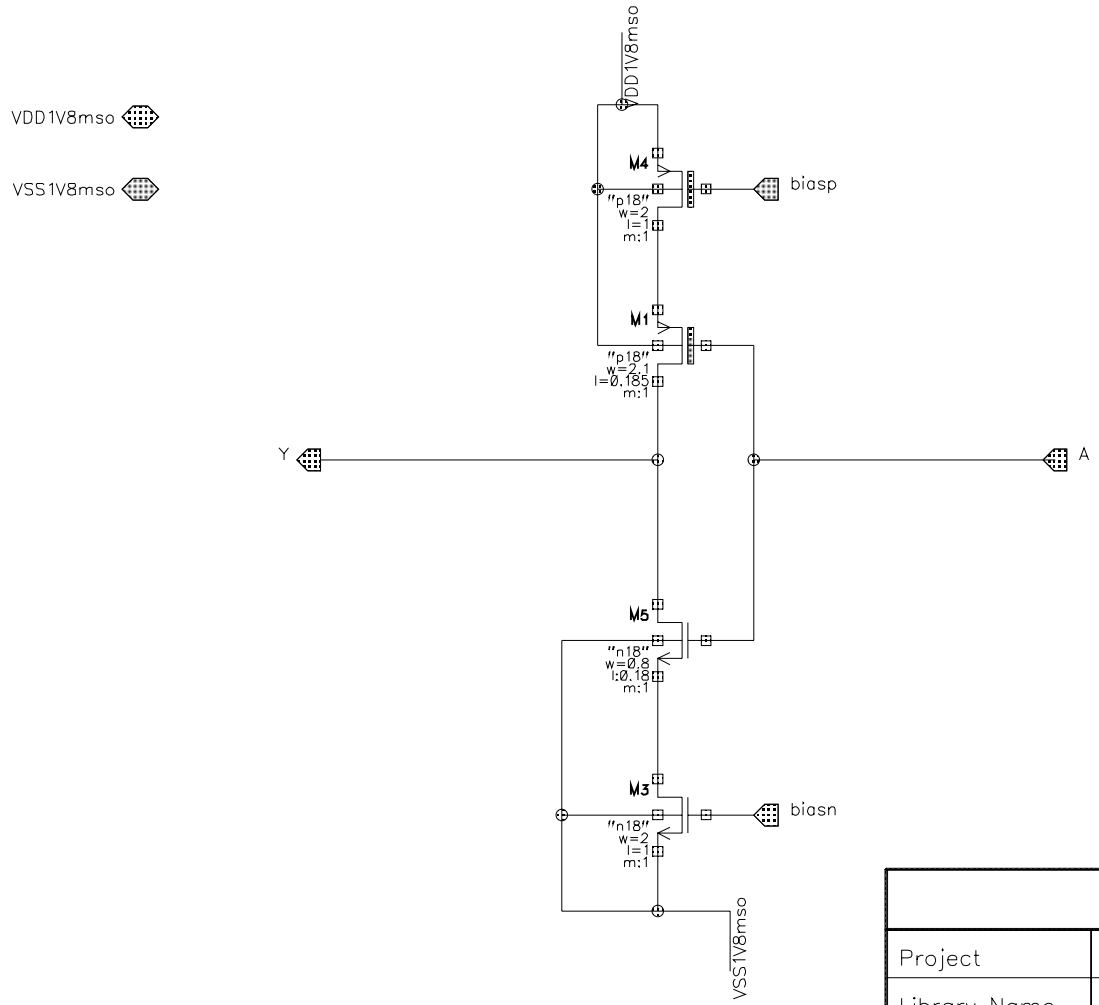

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_inv_x4 |
| Last QA Review | |
| Last Changed | Sep 28 11:42:24 2006 |



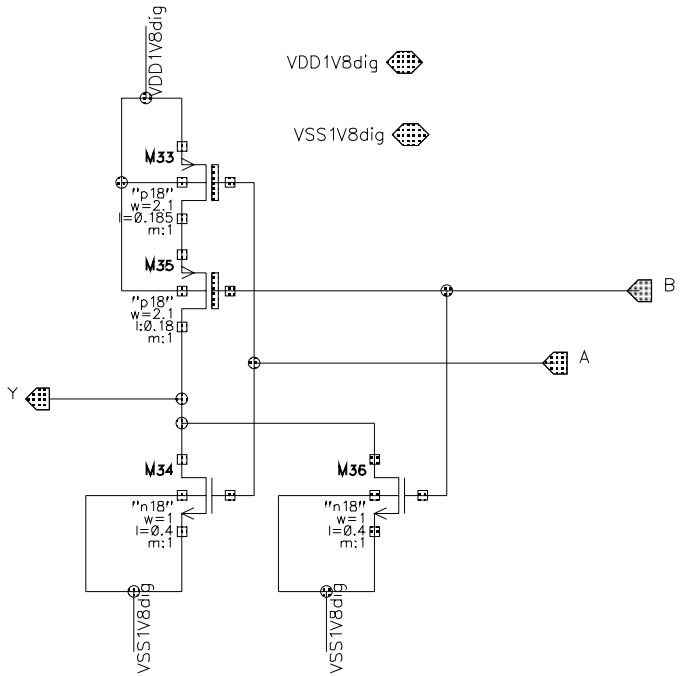

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_feasability |
| Block Name | logic_inv_x1 |
| Last QA Review | |
| Last Changed | Sep 28 11:46:11 2006 |



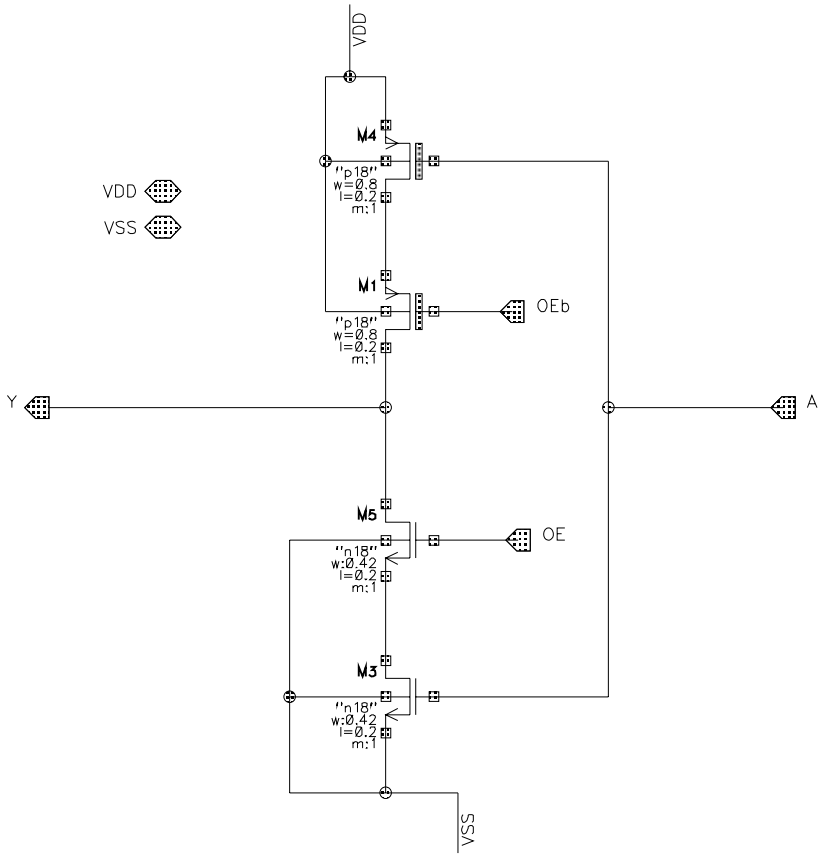

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | logic_inv_x1 |
| Last QA Review | |
| Last Changed | Feb 5 17:55:09 2007 |



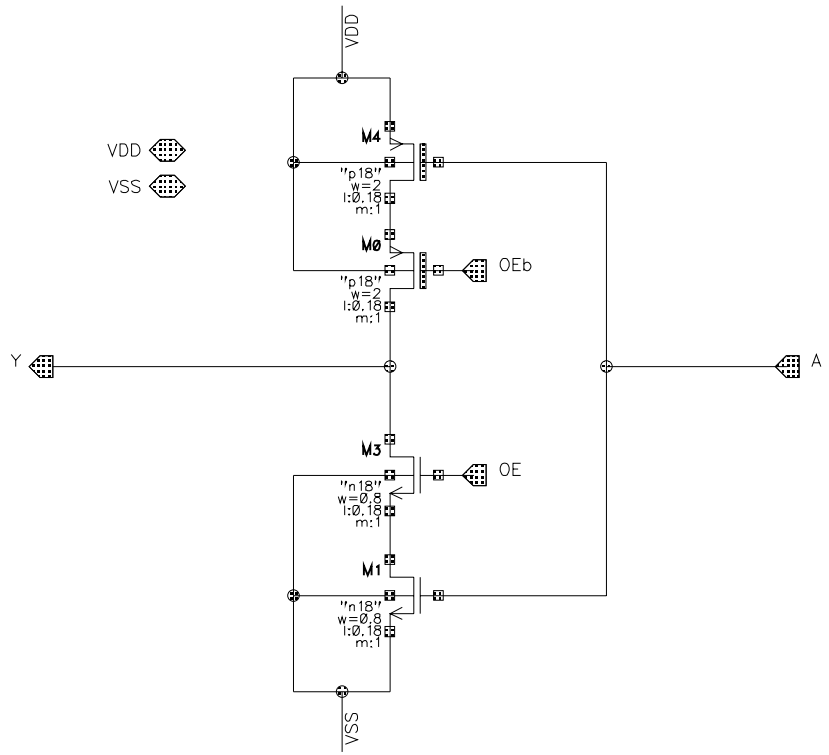

| RAL Microelectronics Group | |
|---|---|
| Project | Tera–Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | logic_inv_x1_lim |
| Last QA Review | |
| Last Changed | Jan 24 17:38:39 2007 |



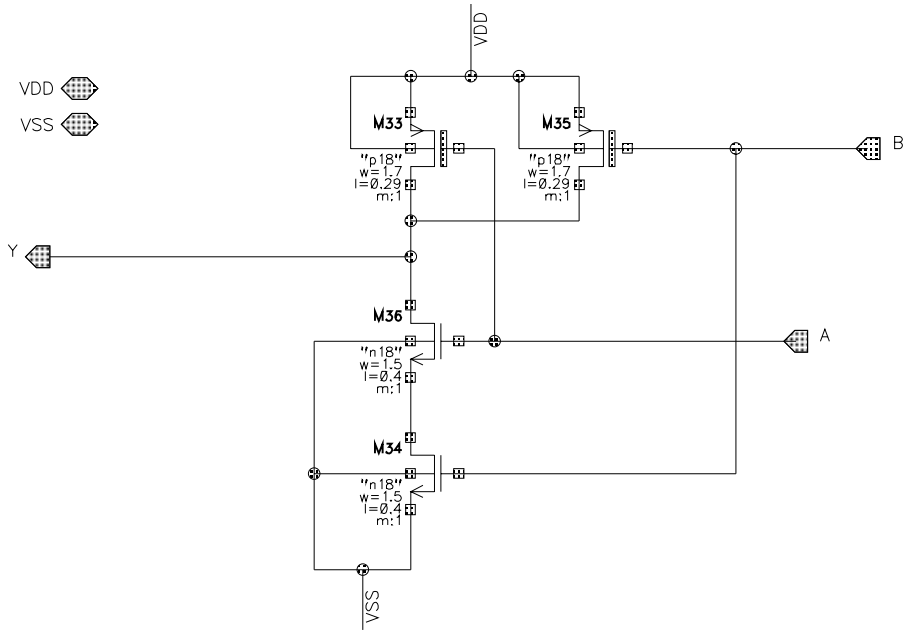

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | CalicePixels |
| Block Name | logic_nor2_x0 |
| Last QA Review | |
| Last Changed | Feb 5 18:38:32 2007 |



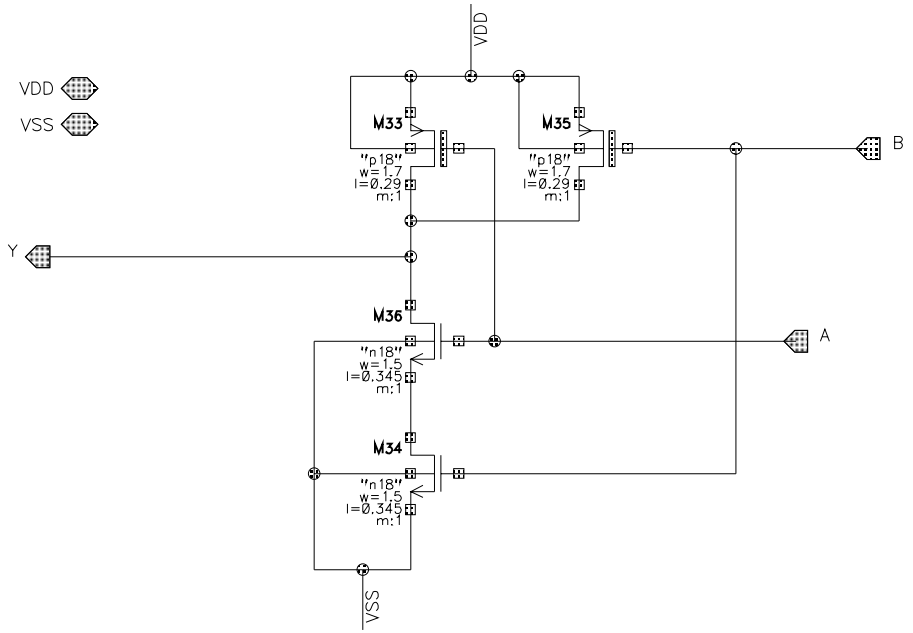

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_invOE_xØc |
| Last QA Review | |
| Last Changed | Feb 12 18:49:59 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_invOE_x1 |
| Last QA Review | |
| Last Changed | Sep 28 11:42:37 2006 |



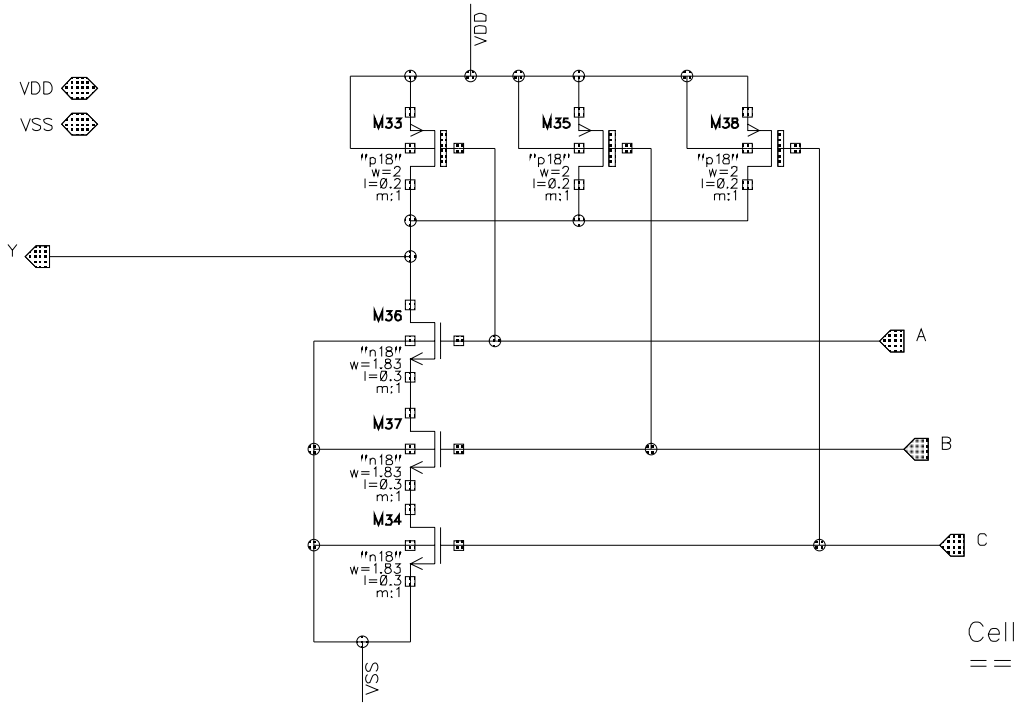

| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_nand2_x0 |
| Last QA Review | |
| Last Changed | Jan 4 09:07:25 2007 |




Cell variant for layout ".lay1"
==========

NMOS lengths reduced from Ø.4 to Ø.345

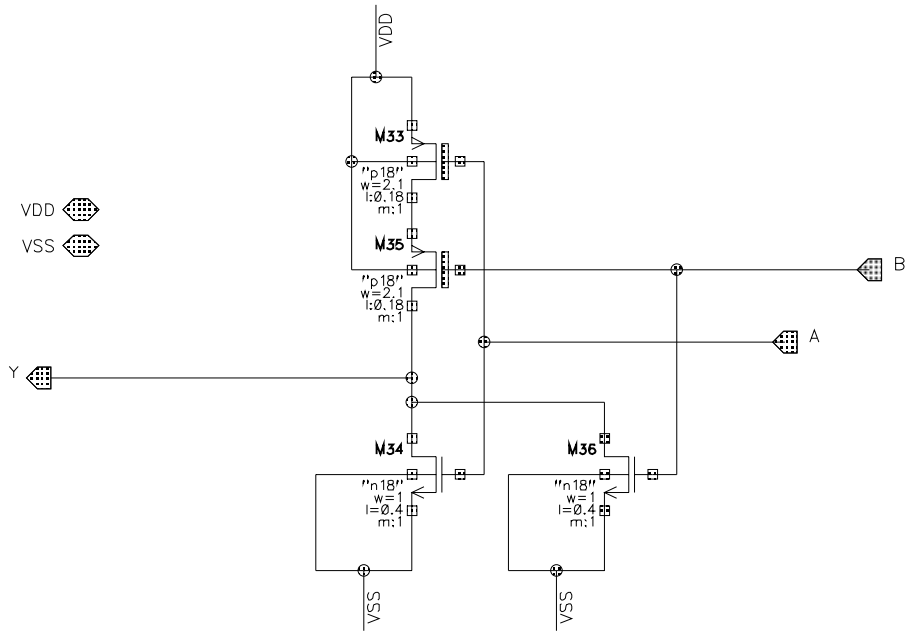
| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_nand2_xØ.lay2 |
| Last QA Review | |
| Last Changed | Feb 5 16:11:45 2007 |



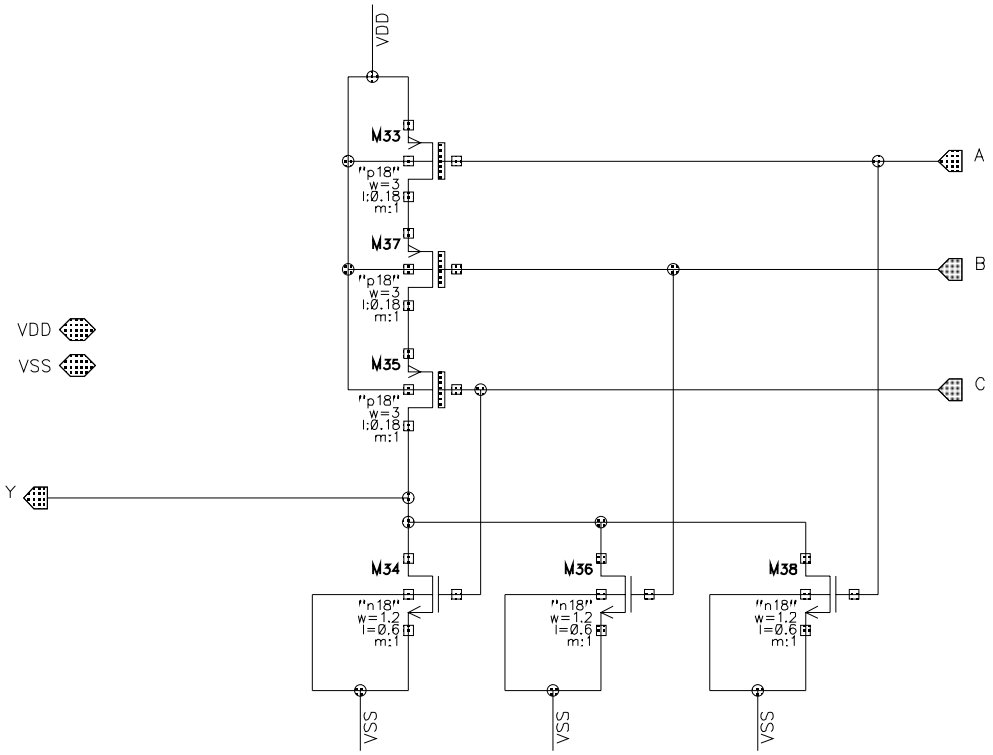

Cell variant for layout ".lay1"

NMOS width reduced from 1.9 to 1.83

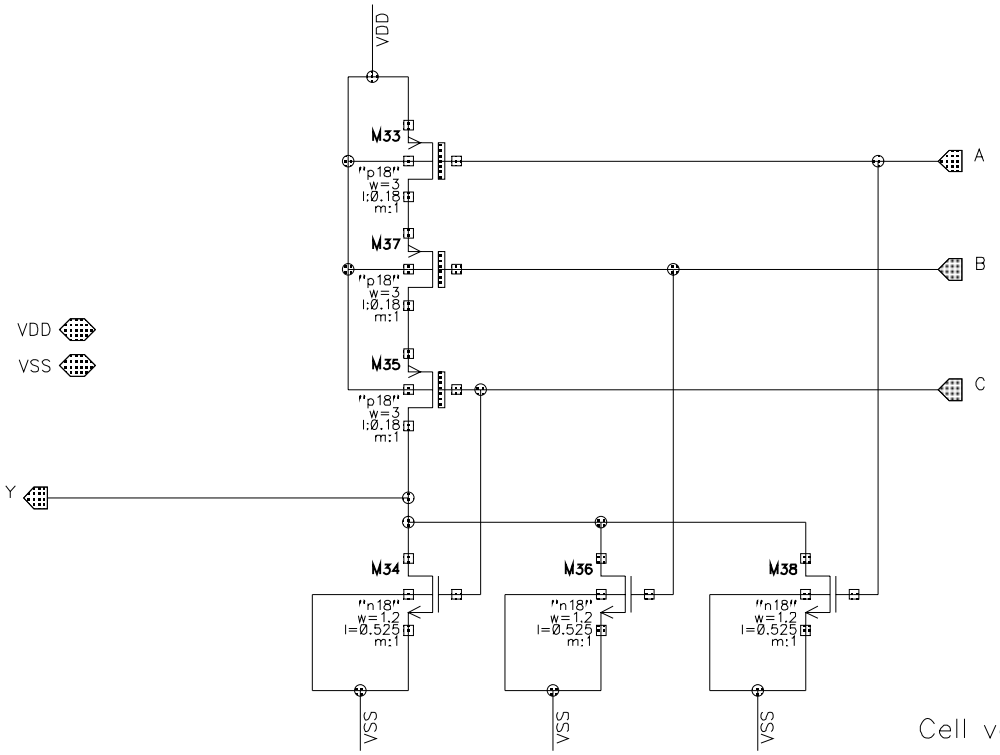
| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_nand3_x0.lay1 |
| Last QA Review | |
| Last Changed | Jan 10 14:24:41 2007 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_nor2_x0 |
| Last QA Review | |
| Last Changed | Sep 28 11:45:21 2006 |




| RAL Microelectronics Group | |
|---|---|
| Project | Tera-Pixel APS for CALICE |
| Library Name | calice_circuits |
| Block Name | logic_nor3_x0 |
| Last QA Review | |
| Last Changed | Jan 10 14:06:59 2007 |




Cell variant for layout: ".lay1"

==========

NMOS length reduced from 0.6 to 0.525

| RAL Microelectronics Group | | |
|---|---|---|
| Project | Tera-Pixel APS for CALICE | |
| Library Name | calice_circuits | |
| Block Name | logic_nor3_x0.lay1 | |
| Last QA Review | | |
| Last Changed | Jan 10 14:20:51 2007 | |