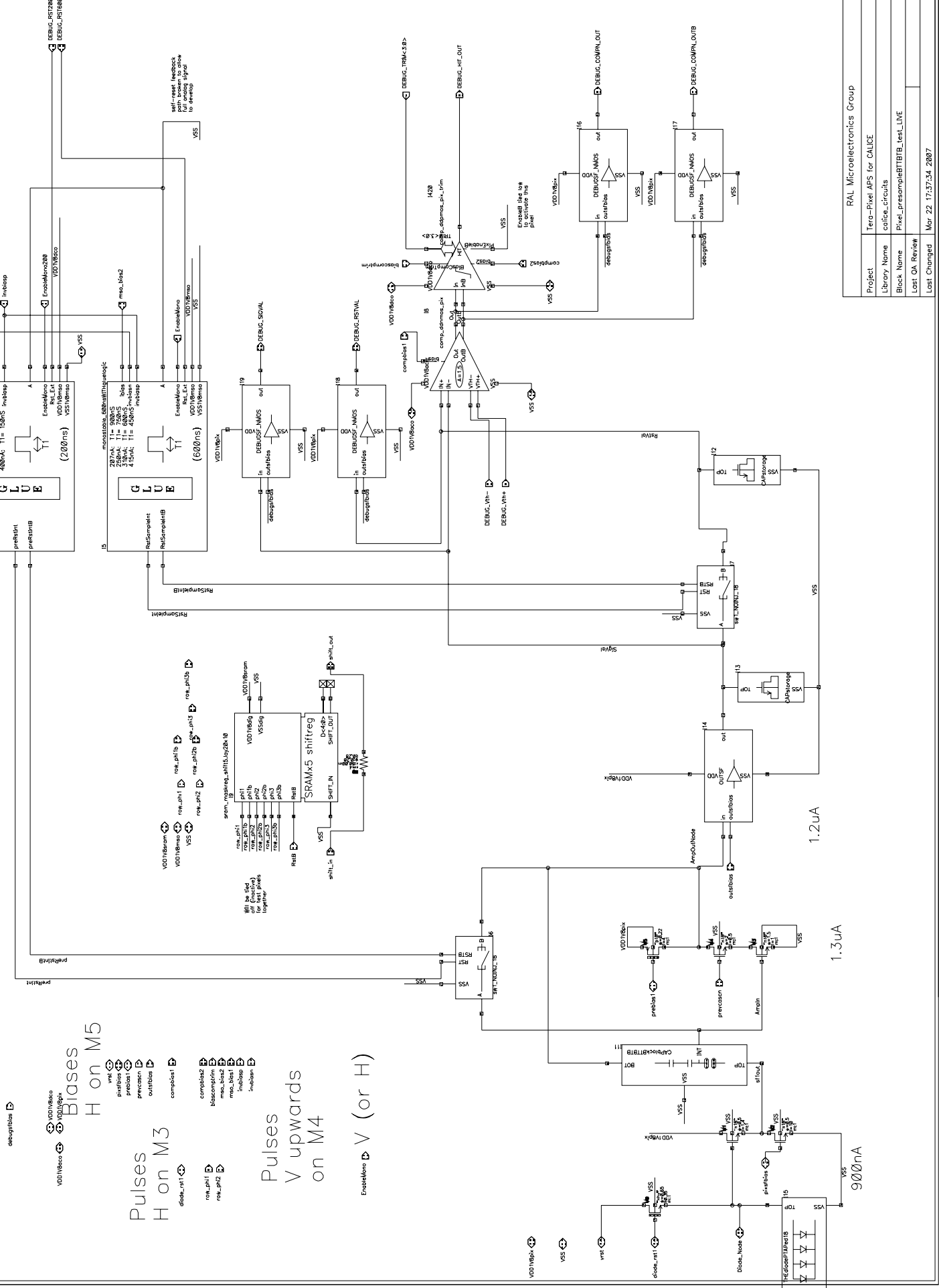


TEST STRUCTURE PIXEL



debugbus

VDD1V8p0

Biases
H on M5

Pulses
H on M3

Pulses
V upwards
on M4

EnableM5 V (or H)

900nA

1.3uA

1.2uA

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampBT1BTB_Test_LIVE
Last CA Review	Mar. 22 17:37:34 2007

TEST STRUCTURE NEIGHBOURS

VDD1V8sc0 VDD1V8sc1 VDD1V8sc2 VDD1V8sc3

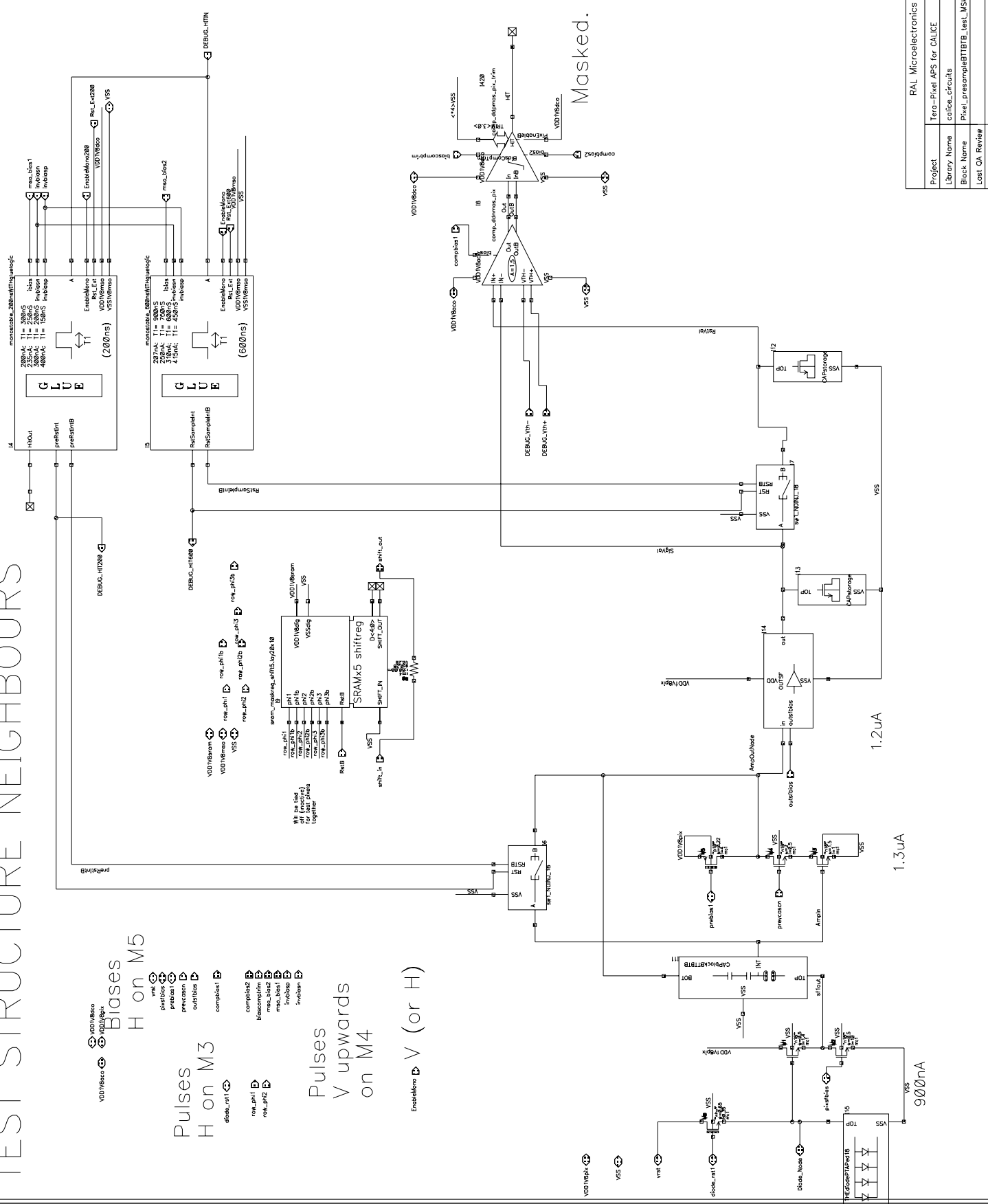
Biases
H on M5

Pulses
H on M3

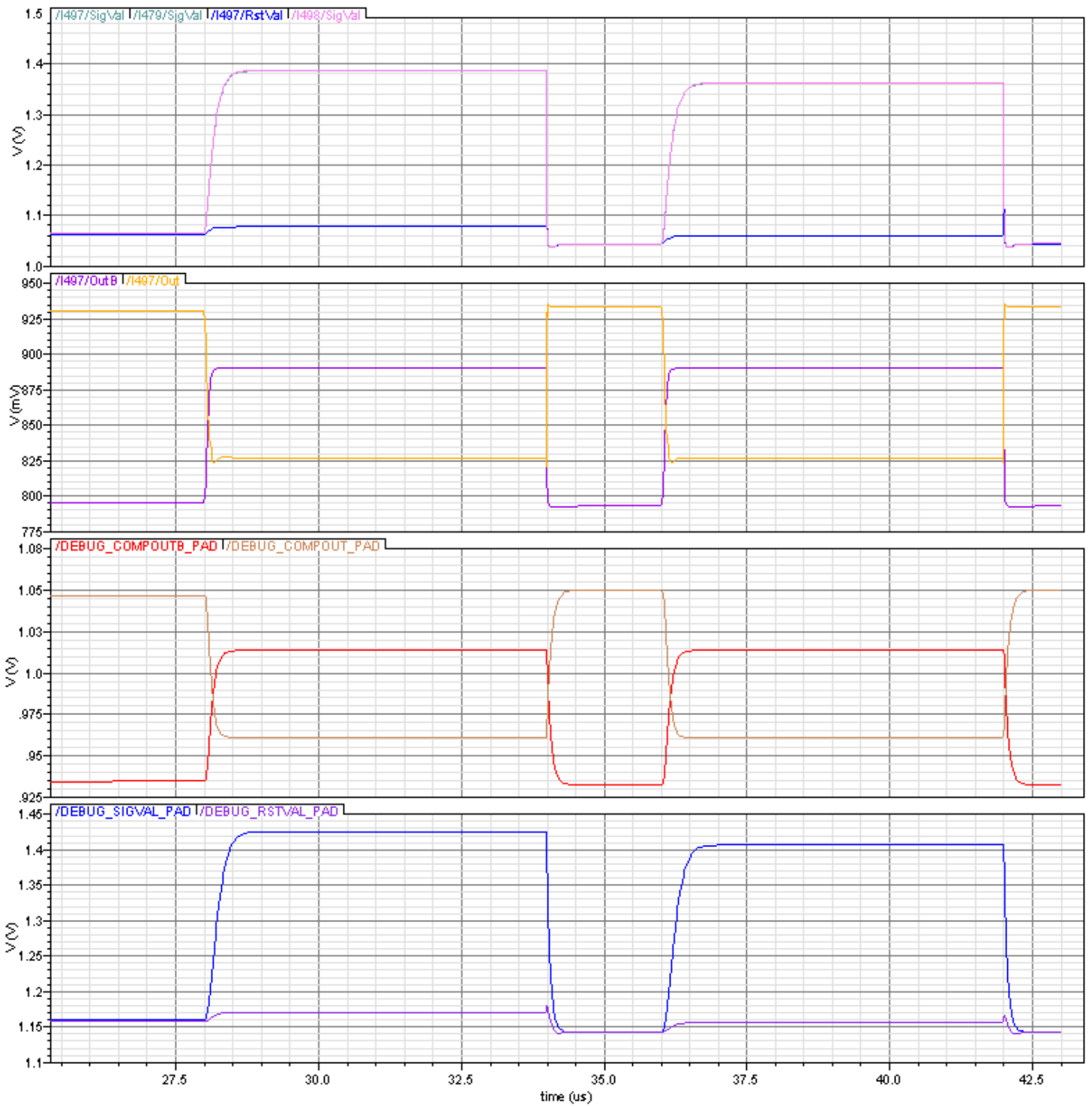
- vrh
- prebias
- prebias1
- prebias2
- prebias3
- prebias4
- prebias5
- prebias6
- prebias7
- prebias8
- prebias9
- prebias10
- prebias11
- prebias12
- prebias13
- prebias14
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- prebias94
- prebias95
- prebias96
- prebias97
- prebias98
- prebias99
- prebias100

Pulses
V upwards
on M4

EnableM5 V (or H)



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampBTBTB_test_M5K0
Last QA Review	
Last Changed	Mar. 22 17:37:42 2007



Output PMOS source follower current = 40uA.
Loads of 10pF and 20pF simulated.

