Master Controller

Preshape Biases

Configuration SR

Analog References

Global Power

Analog Core 1.8v

Digital Core 1.8v

Analog I/O 1.8v

Digital I/O 1.8v

Core 0v

Core 1.8v

Core 2.5v

Core 3.3v

Data Columns

Data Sense

!! MUX !!

Configuration SR

PreSample Biases

Analog References

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	ASIC1_top
Last QA Review	
Last Changed	Dec 18 19:06:47 2006