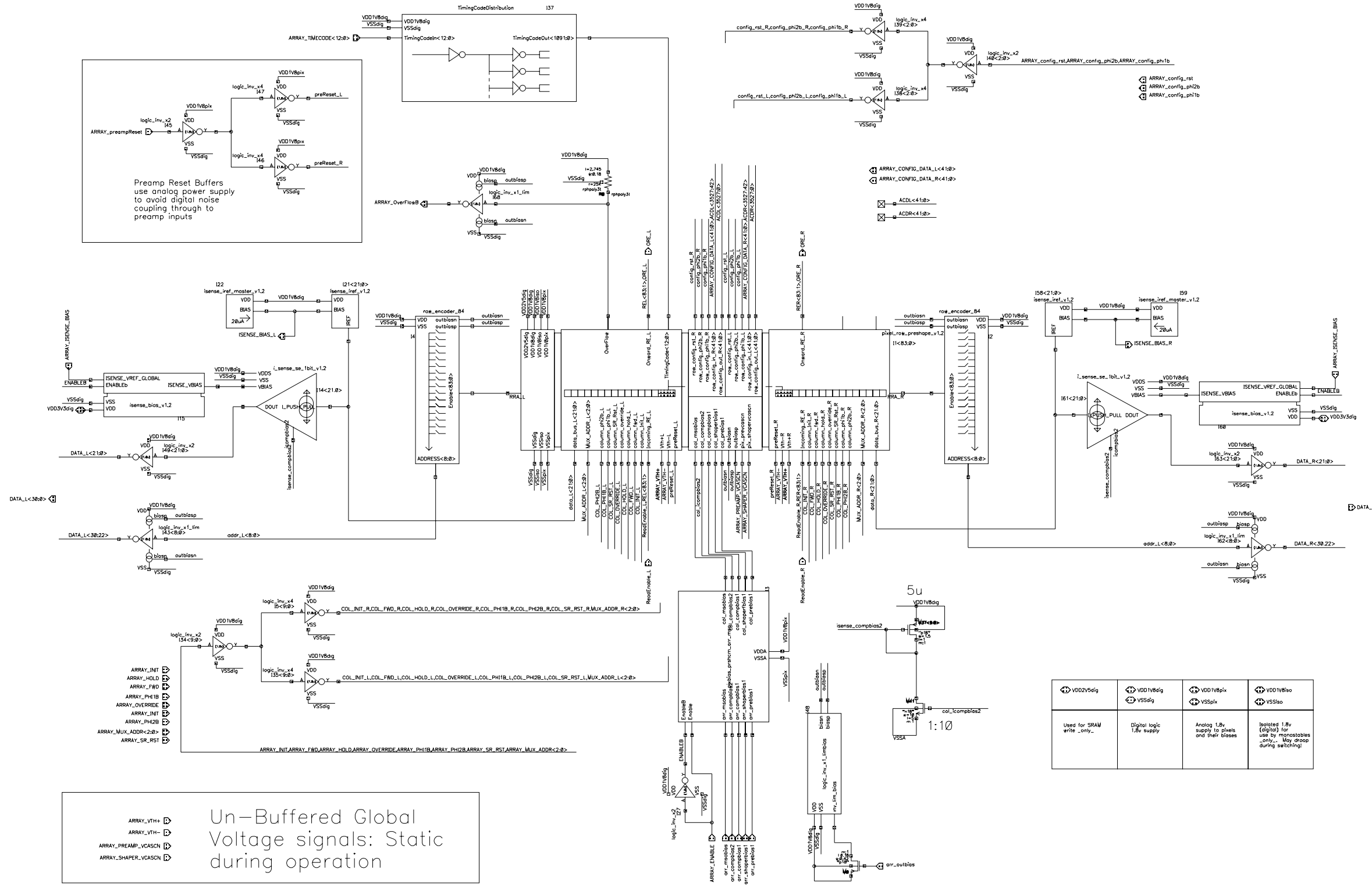
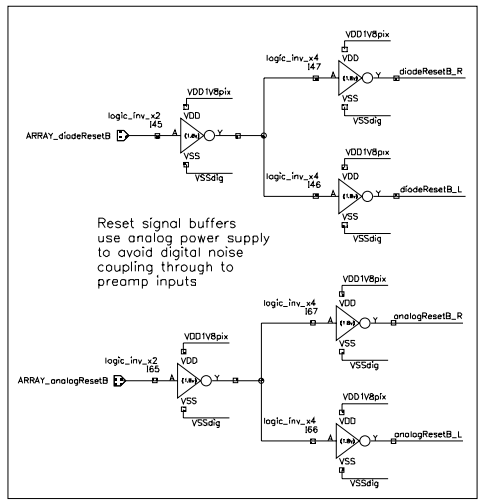
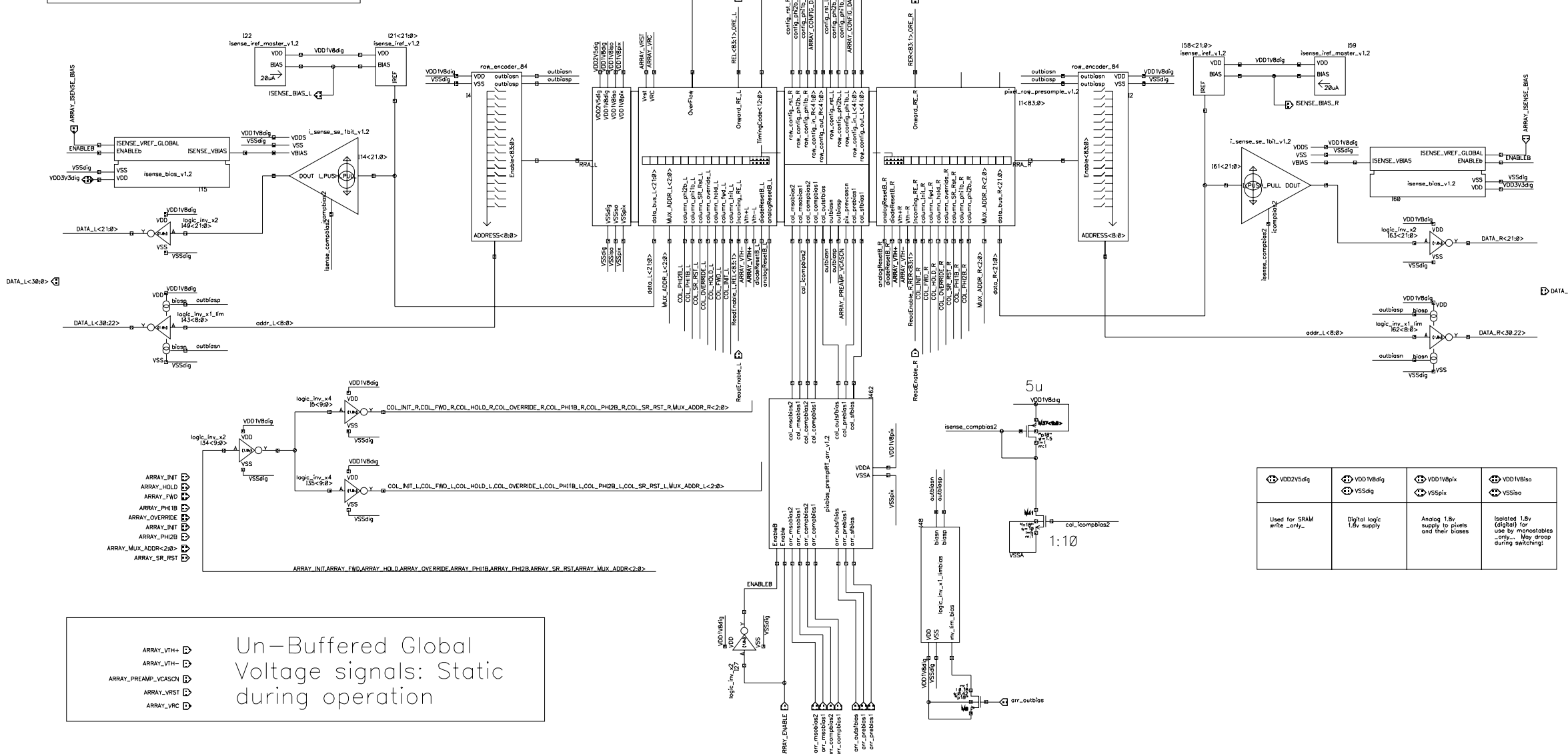
Pre-Shape Pixel Array 84x84



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array1_preshape_v1.2
Last QA Review	
Last Changed	Dec 15 10:57:42 2006

Pre-Sample Pixel Array 84x84



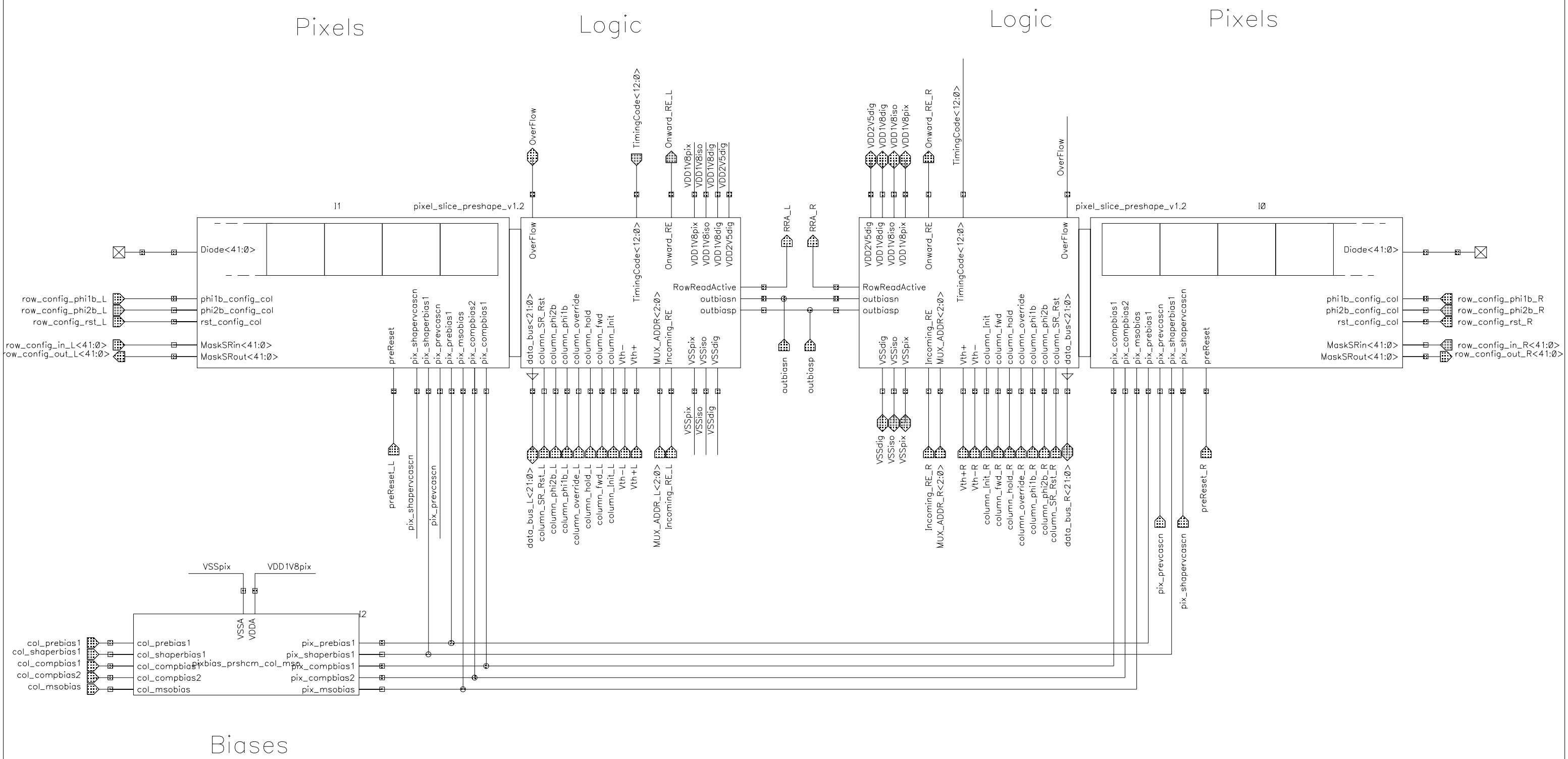


VDD2V5dig VSSdig	VDD1V8dig VSSdig	VDD1V8pix VSSpix	VDD1V8iso VSSiso
Used for SRAM write _only_	Digital logic 1.8v supply	Analog 1.8v supply to pixels and their biases	Isolated 1.8v (digital) for use by monostables _only_. May droop during switching!

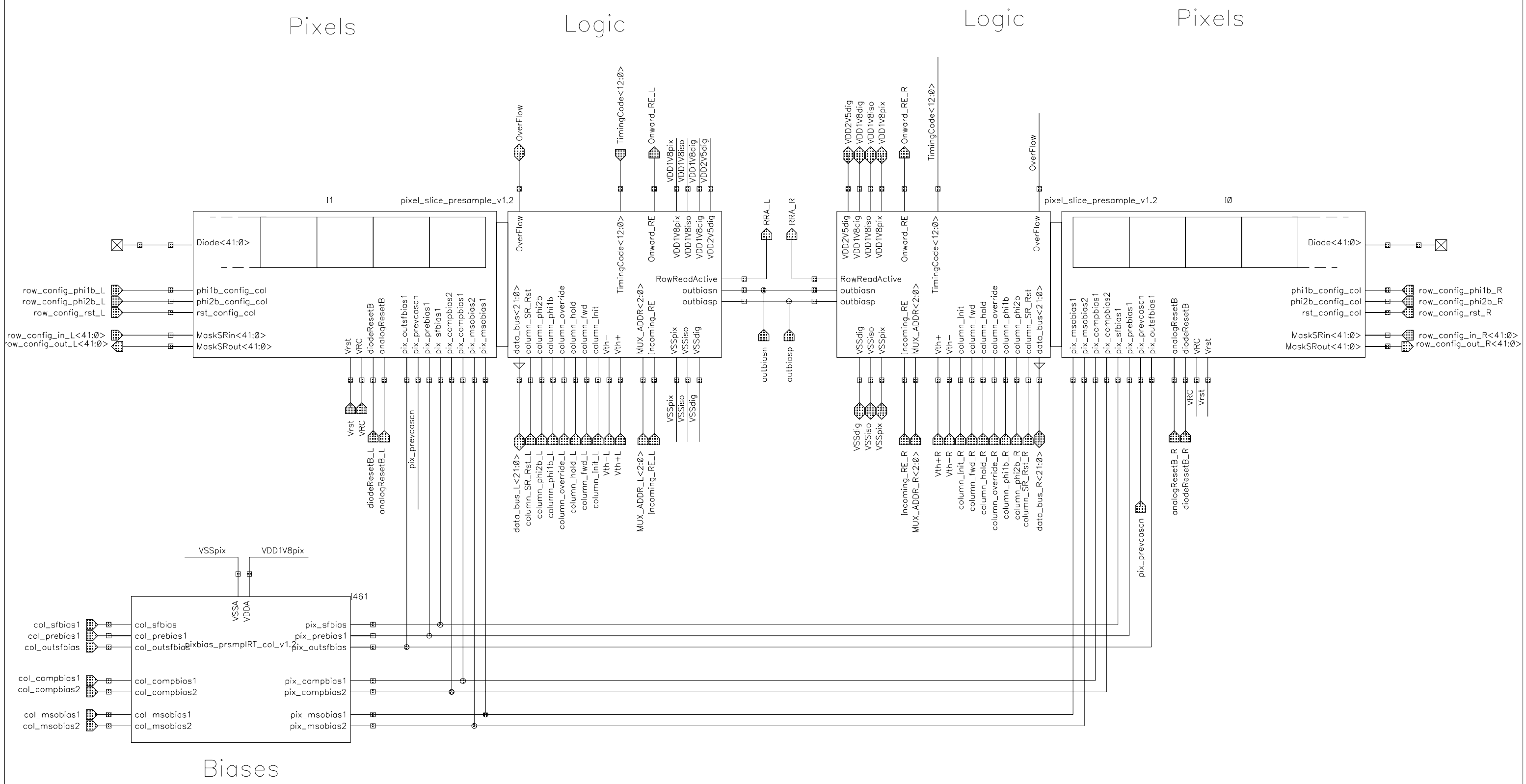
ARRAY_VTH+
ARRAY_VTH-
ARRAY_PREAMP_VCASCN
ARRAY_VRST
ARRAY_VRC

Un-Buffered Global Voltage signals: Static during operation

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array1_presample_v1.2
Last QA Review	
Last Changed	Dec 15 10:57:39 2006

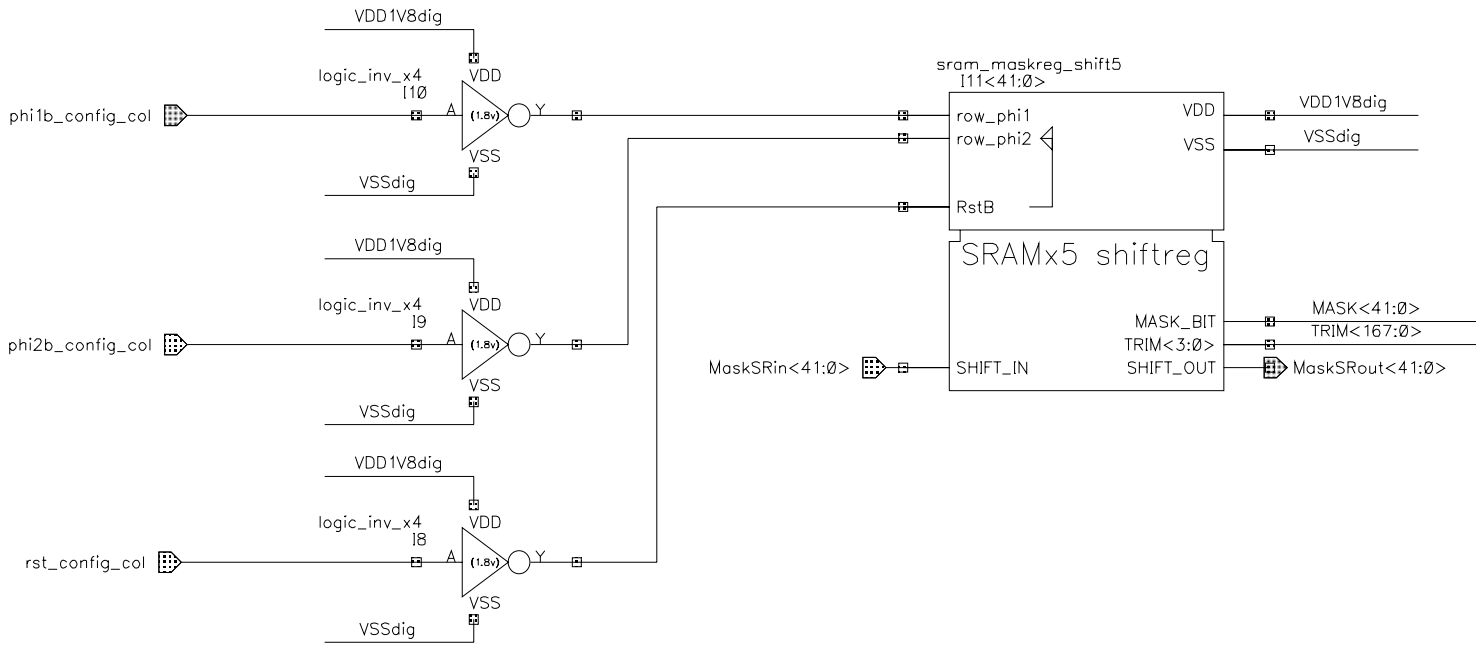


RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_row_preshape_v1.2
Last QA Review	
Last Changed	Dec 14 15:55:52 2006

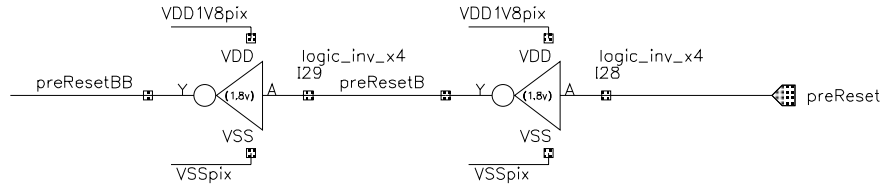


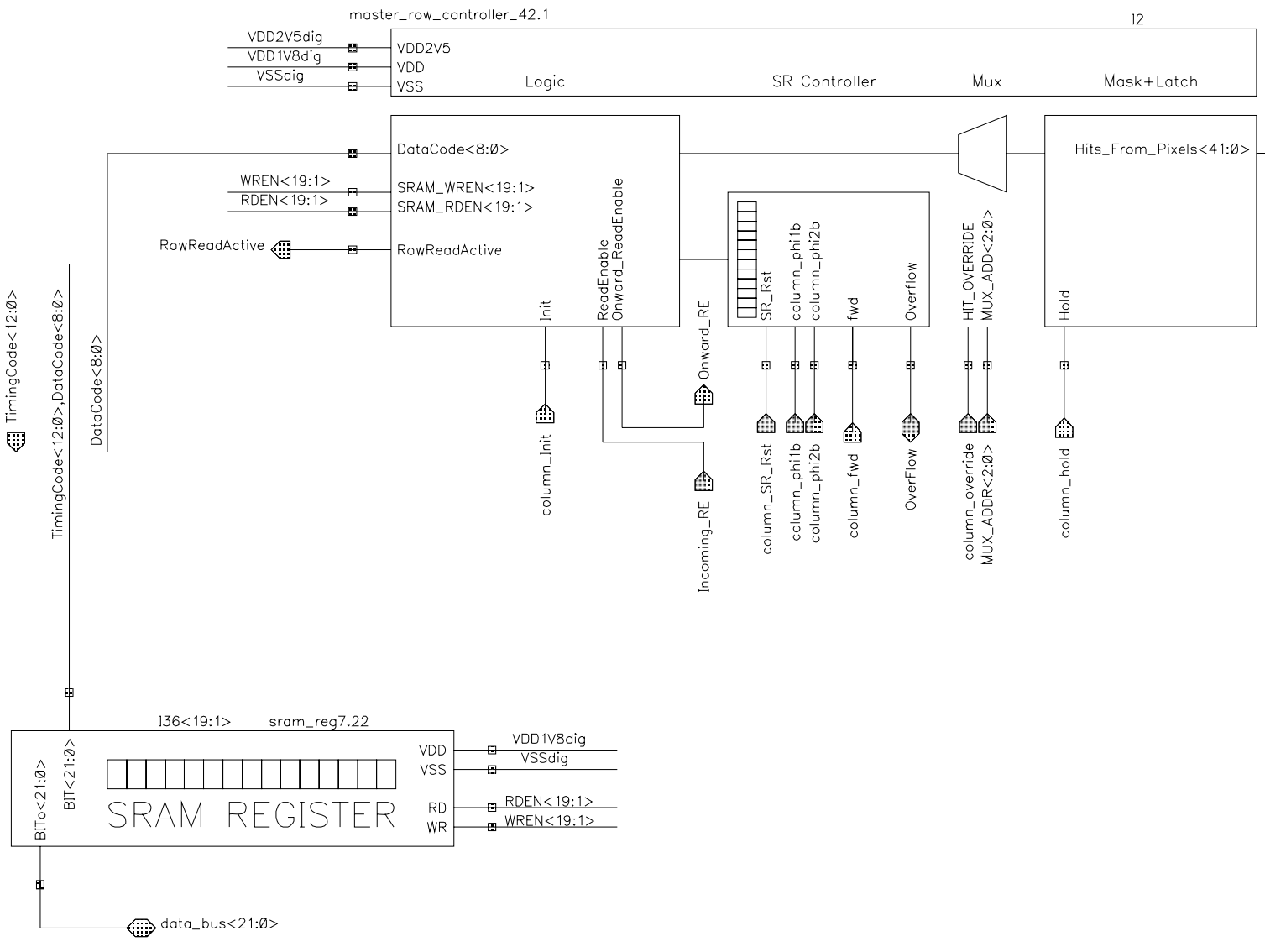
RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_row_presample_v1.2
Last QA Review	
Last Changed	Dec 14 16:04:06 2006

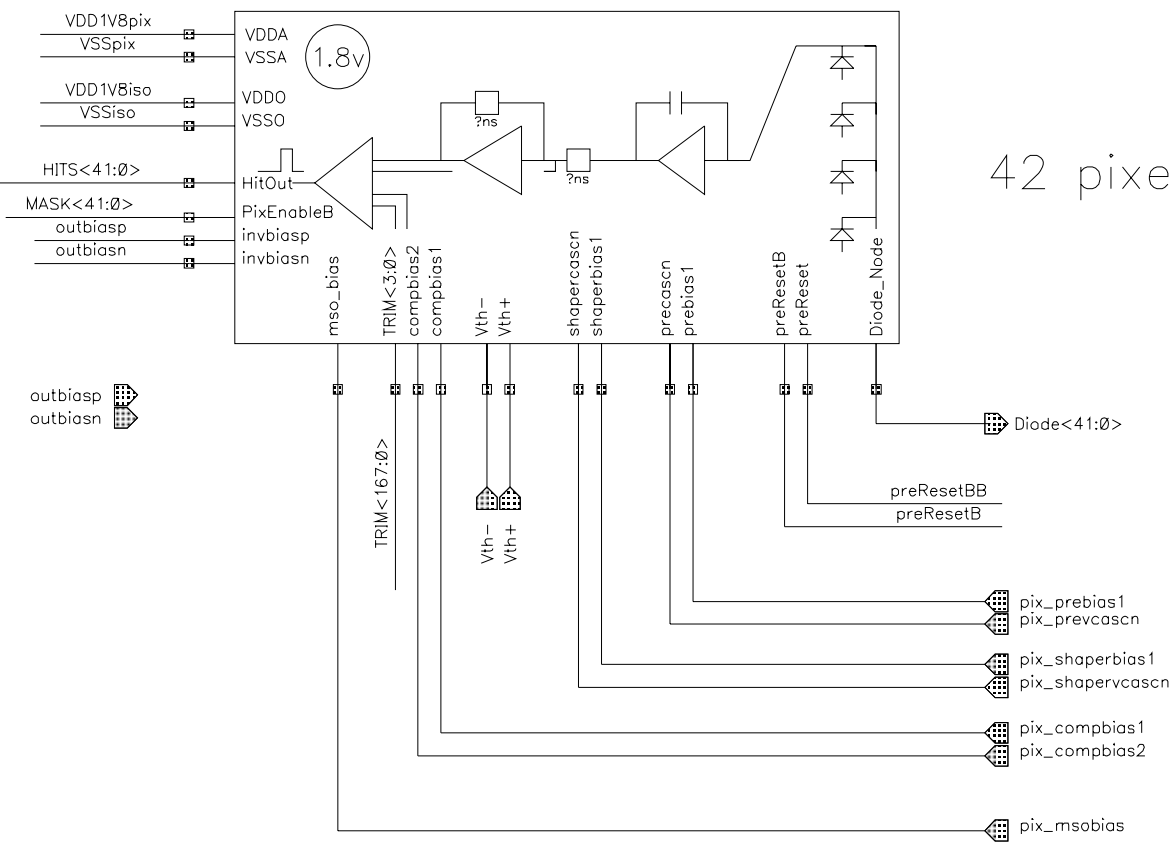
Config SR clocks



VDD2V5dig	VDD1V8dig VSSdig	VDD1V8pix VSSpix	VDD1V8iso VSSiso
Used for SRAM write _only_	Digital logic 1.8v supply	Analog 1.8v supply to pixels and their biases	Isolated 1.8v (digital) for use by manostables _only_. May droop during switching!



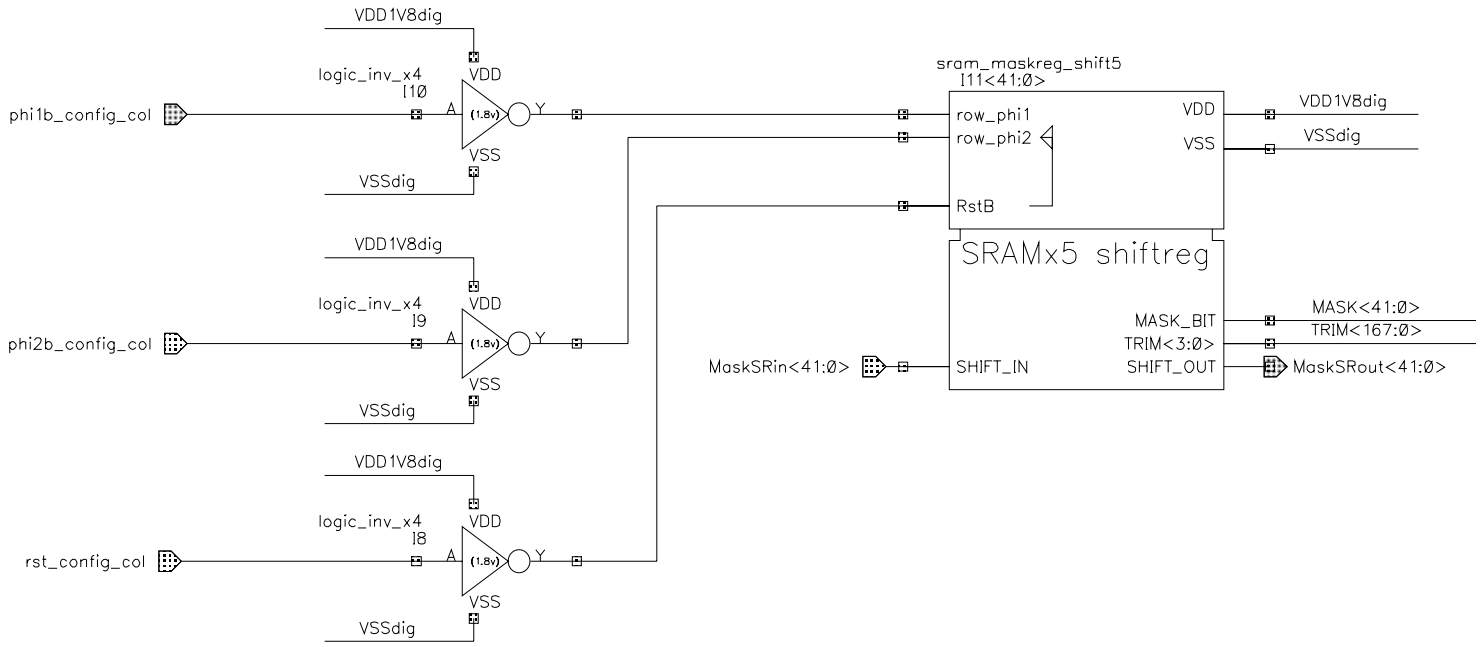




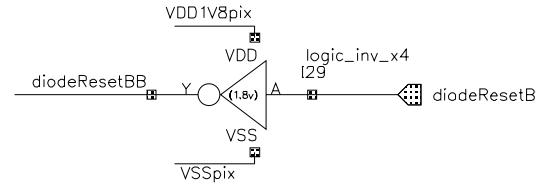
42 pixels

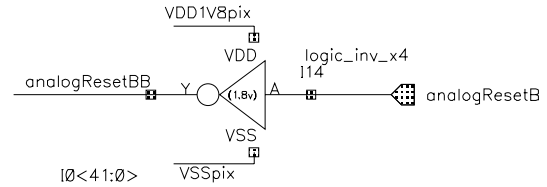
RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_slice_preshape_v1.2
Last QA Review	
Last Changed	Dec 14 15:31:15 2006

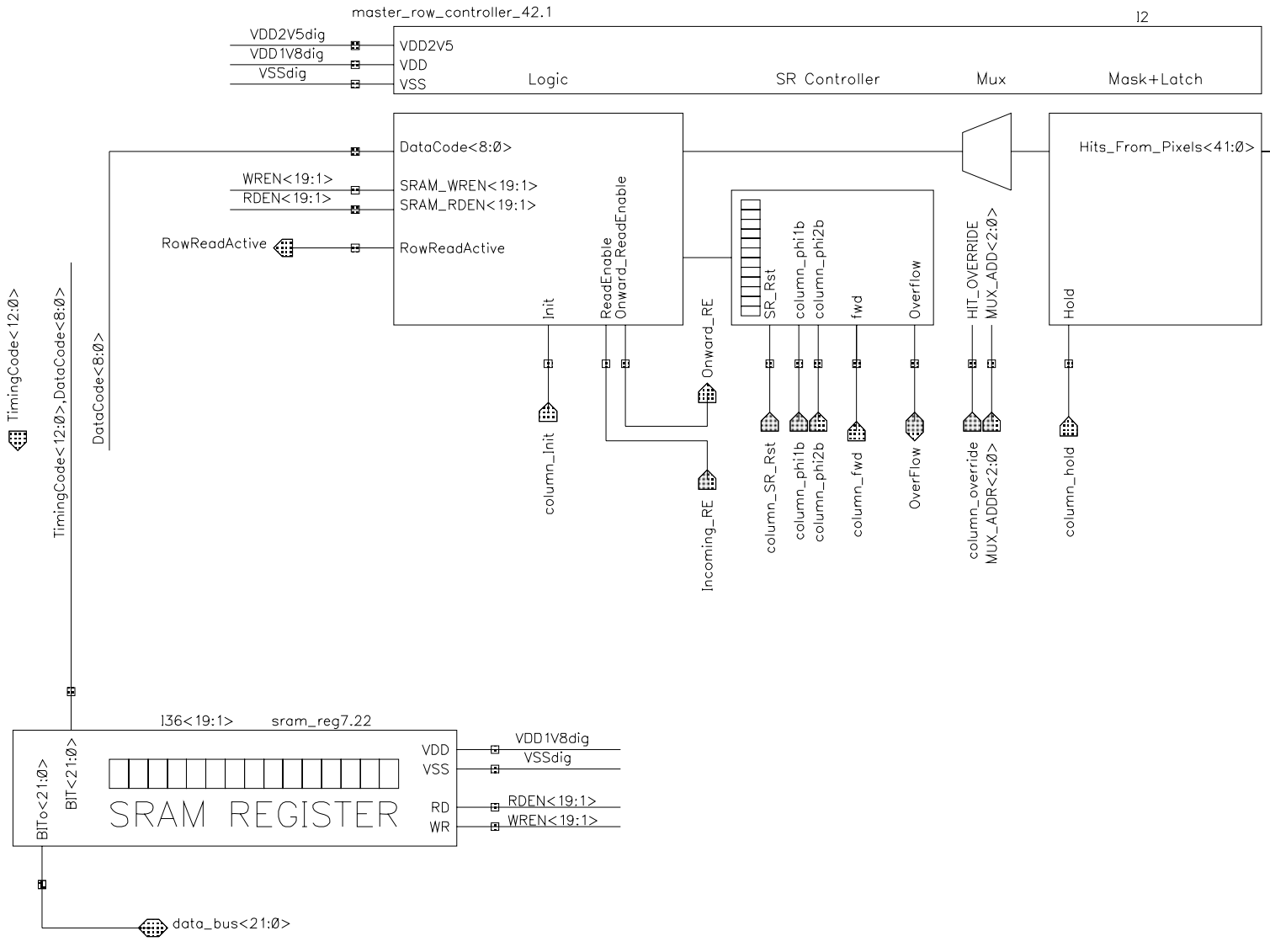
Config SR clocks

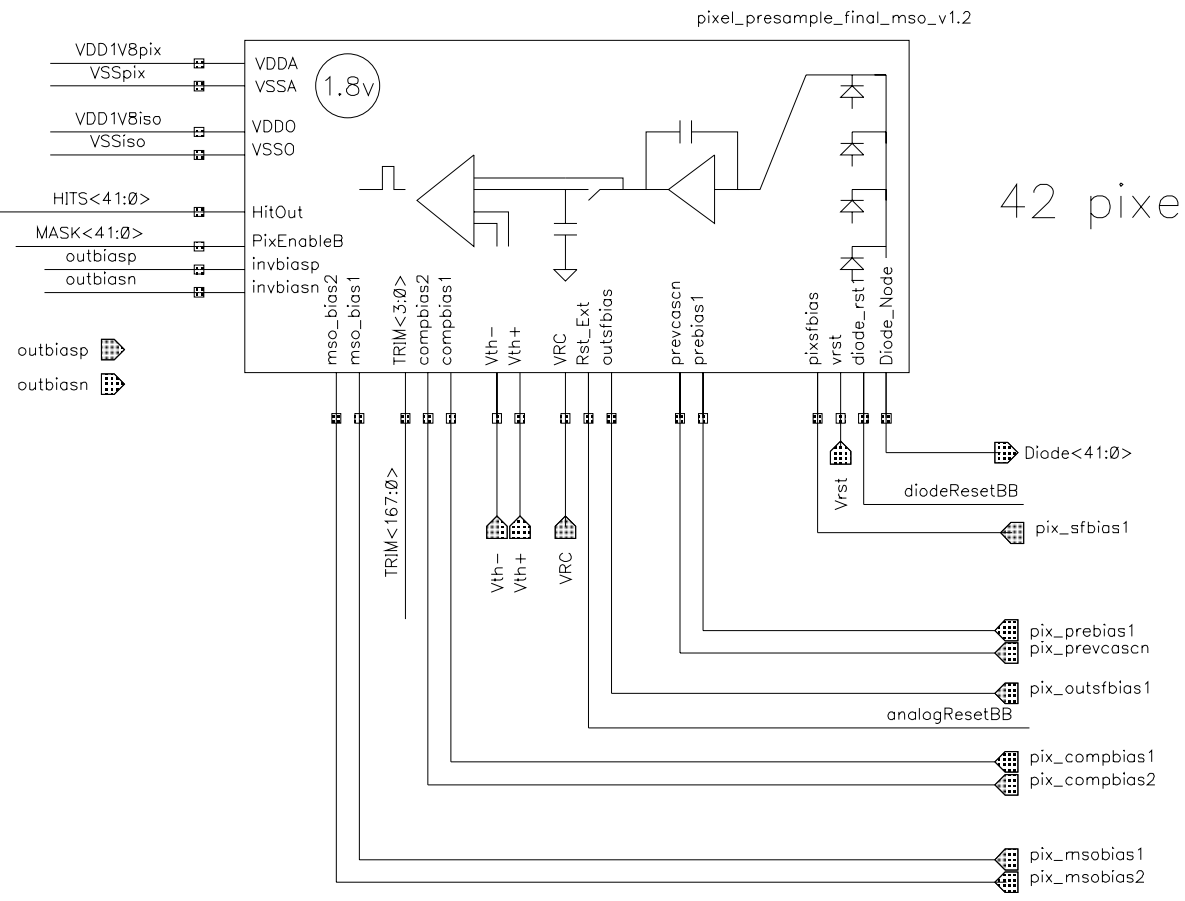


VDD2V5dig	VDD1V8dig VSSdig	VDD1V8pix VSSpix	VDD1V8iso VSSiso
Used for SRAM write _only_	Digital logic 1.8v supply	Analog 1.8v supply to pixels and their biases	Isolated 1.8v (digital) for use by manostables _only_. May droop during switching!



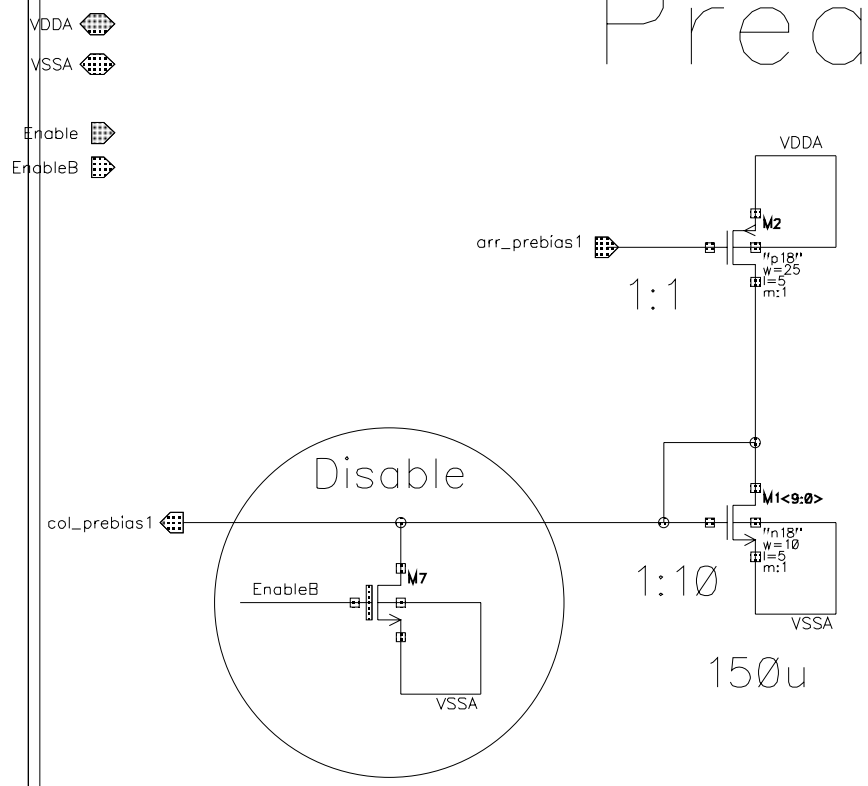




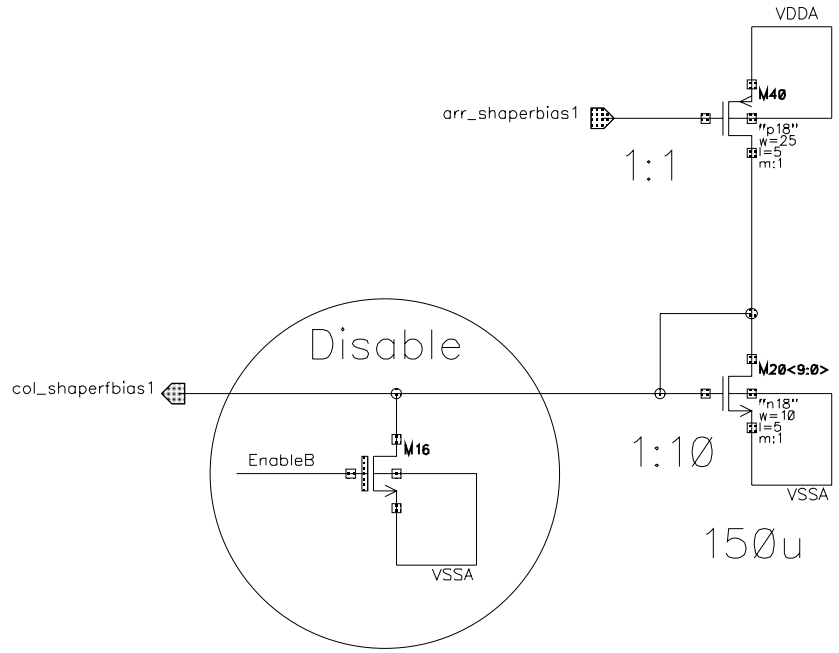


RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_slice_presample_v1.2
Last QA Review	
Last Changed	Dec 14 15:39:30 2006

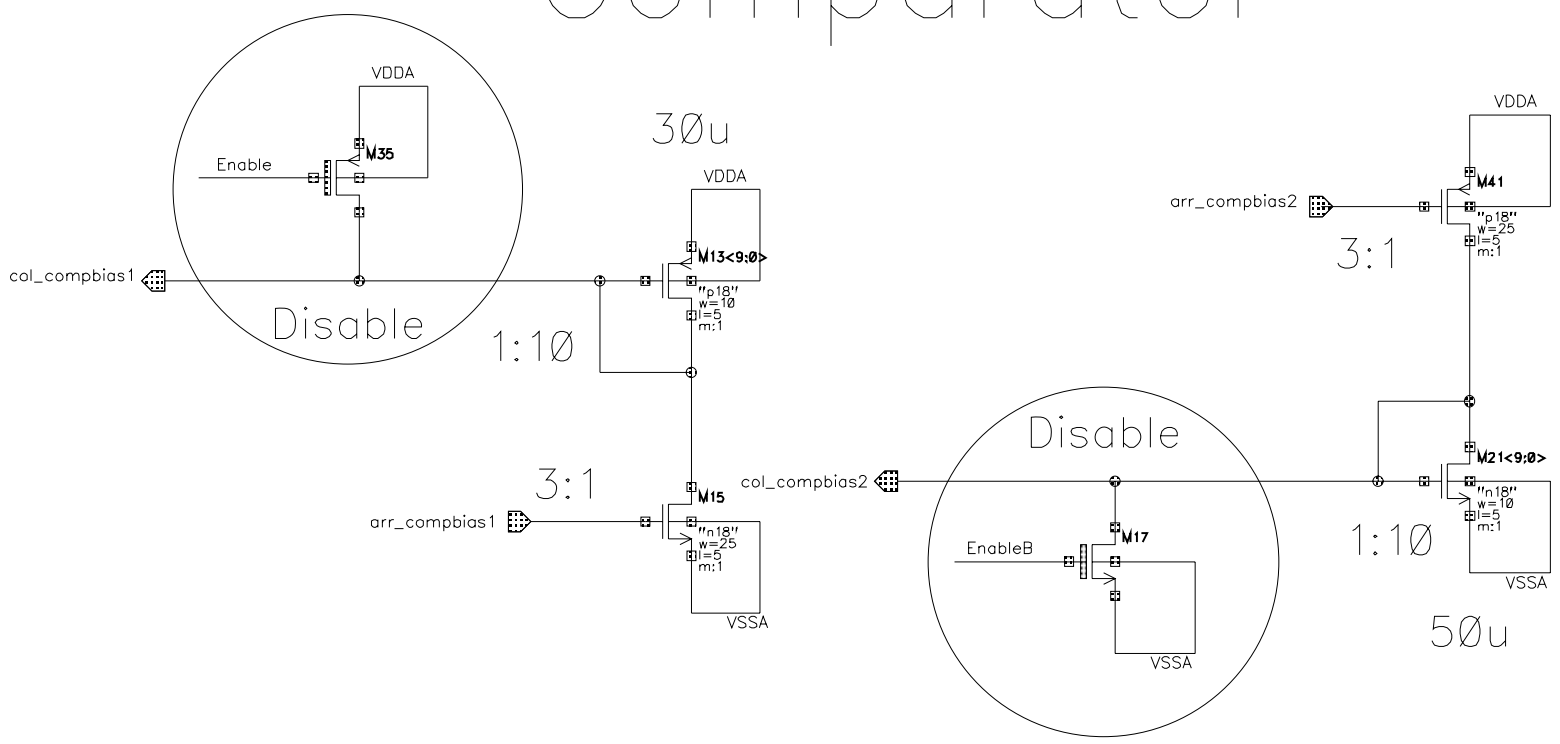
Preamp Bias



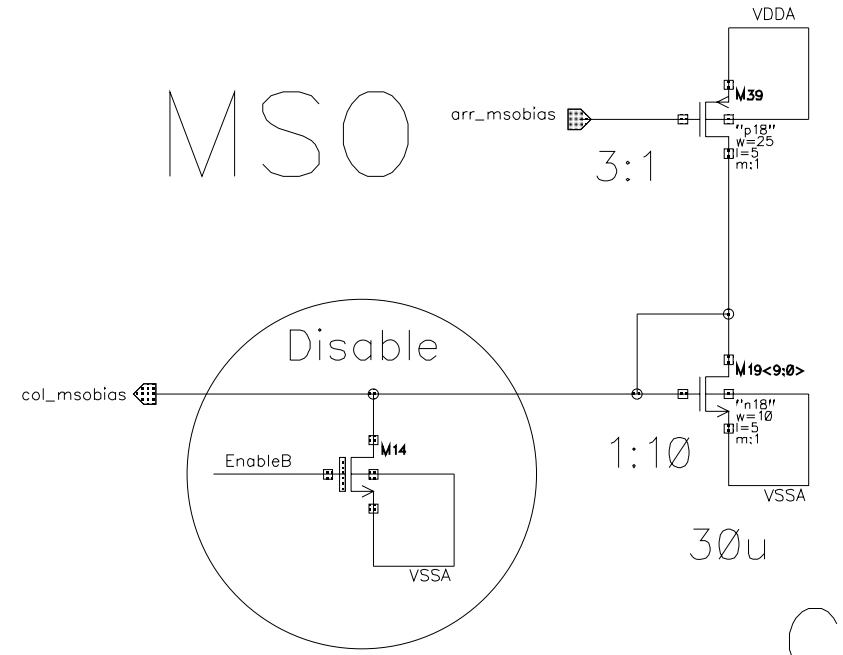
Shaper Bias



Comparator



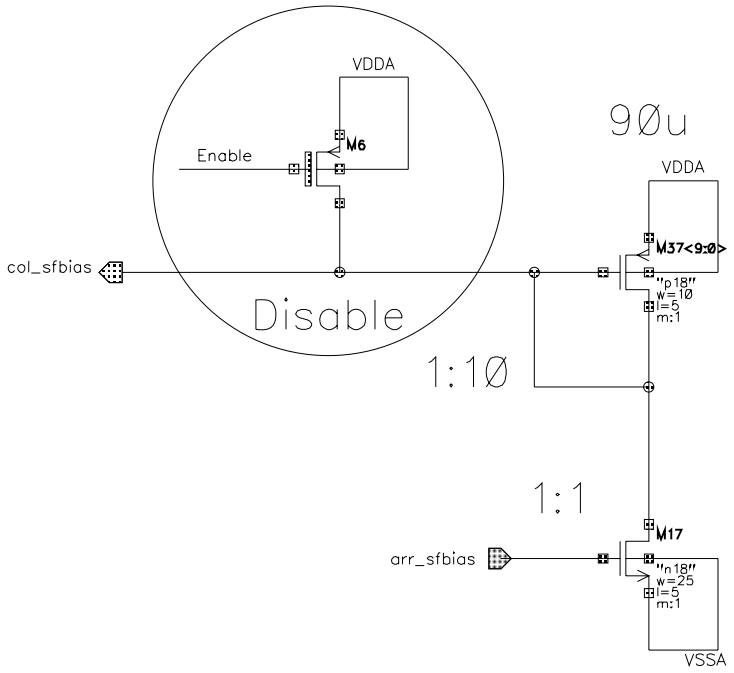
MSO



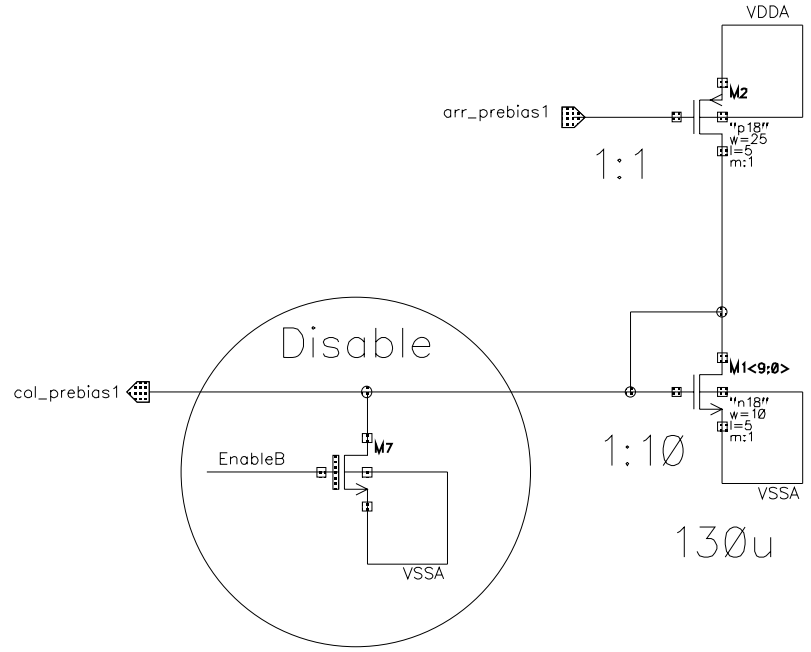
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_arr_mso
Last QA Review	
Last Changed	Dec 13 18:13:23 2006

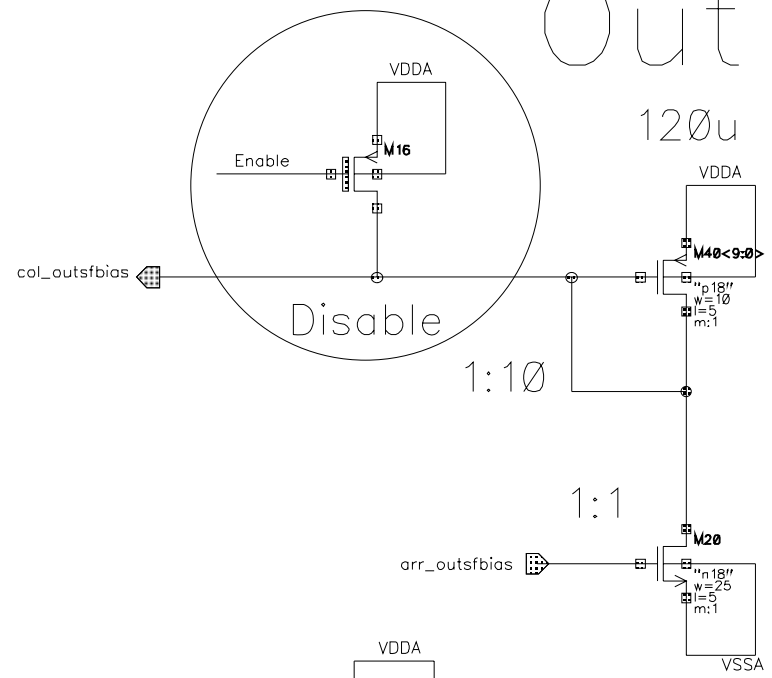
Pixel SF

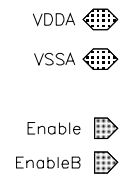


Preamp Bias

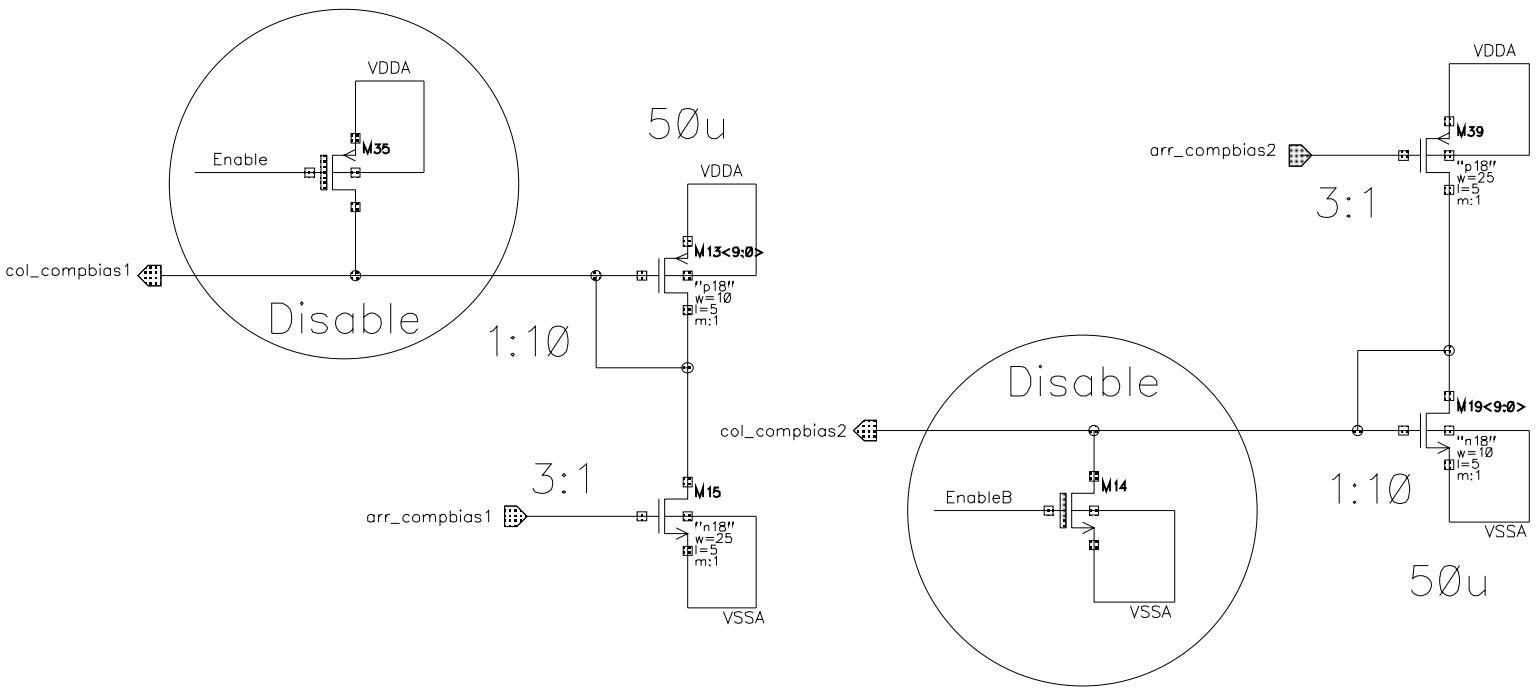


Out SF

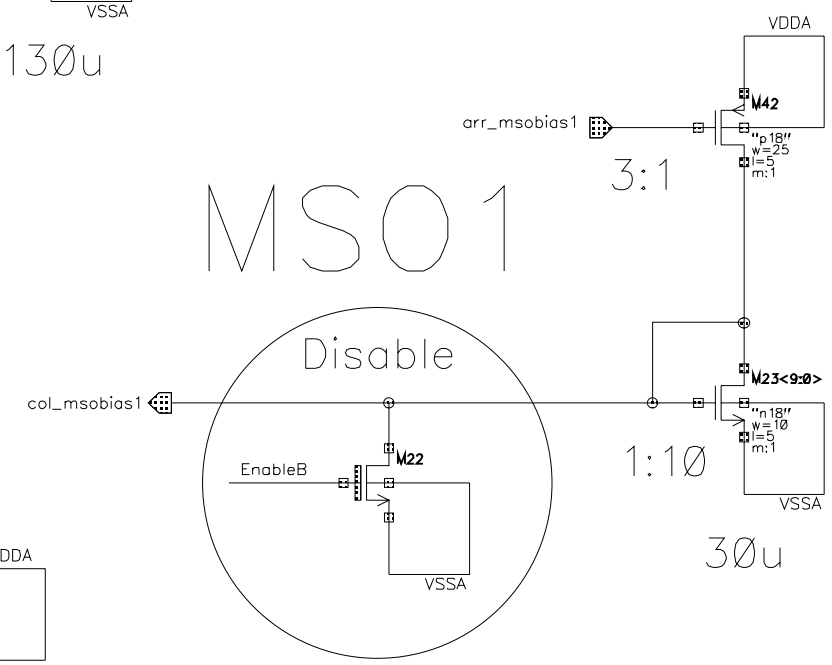




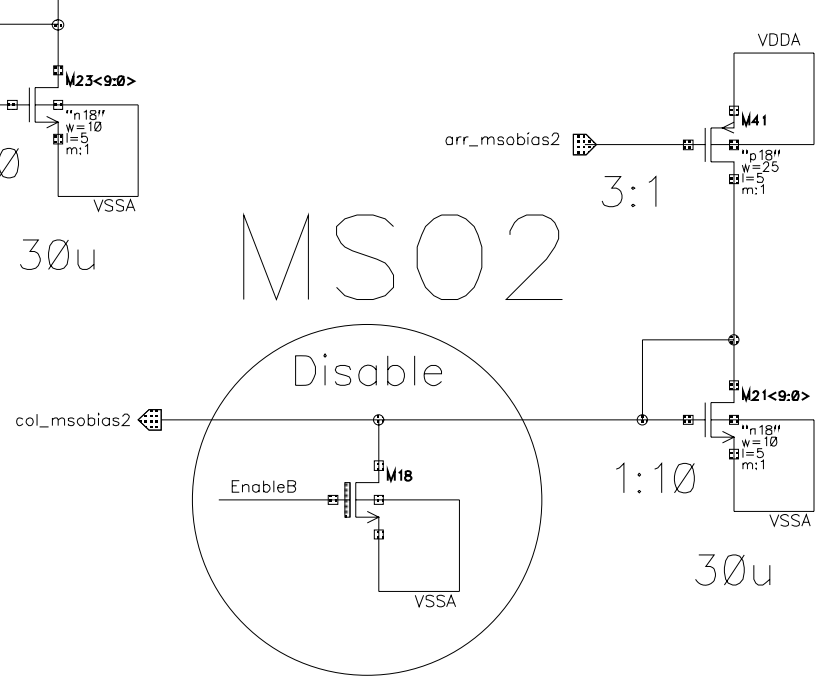
Comparator



MS01



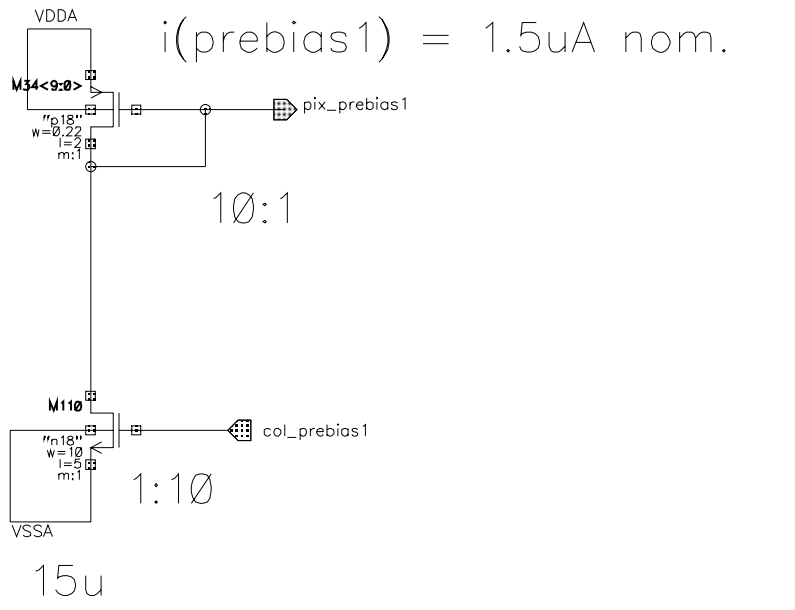
MS02



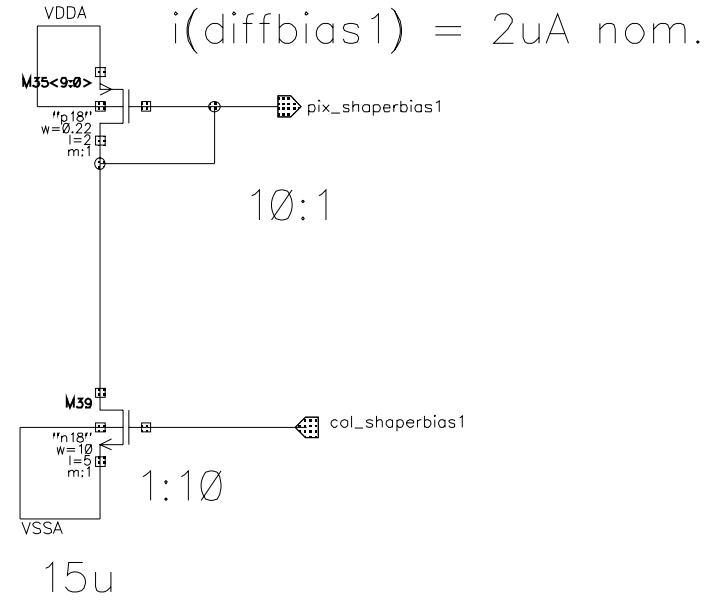
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prsmplRT_arr_v1.2
Last QA Review	
Last Changed	Dec 14 14:01:40 2006

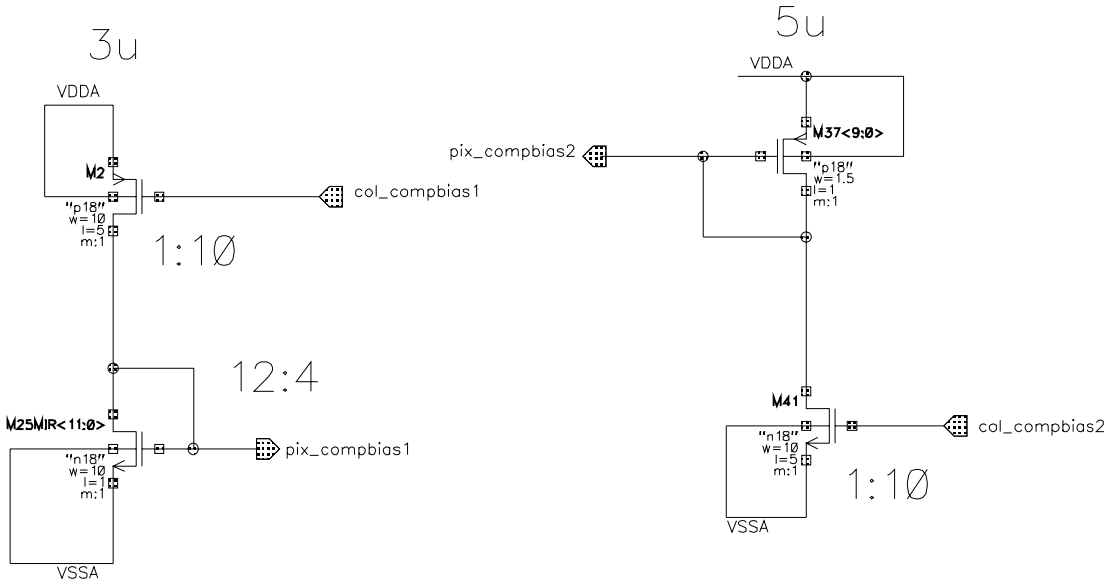
Preamp Bias



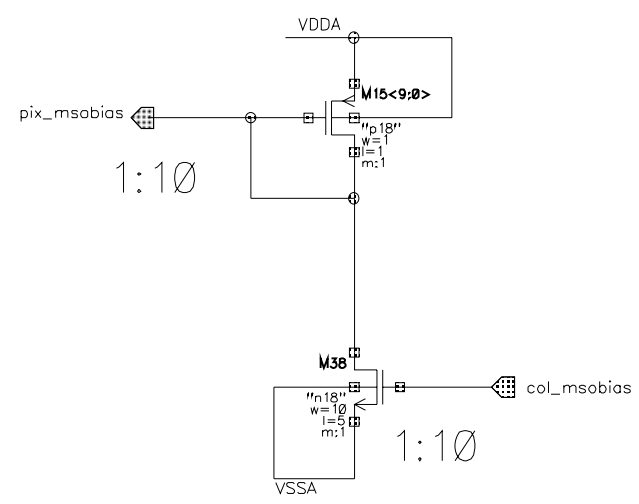
Shaper Bias



Comparator Bias



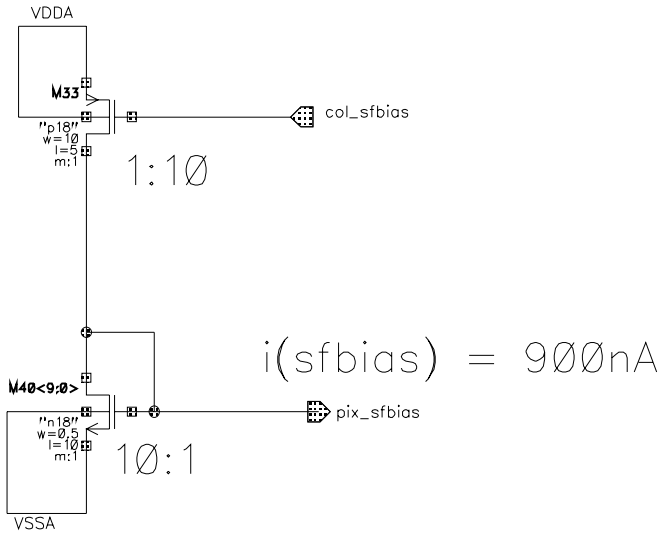
MSO



COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_col_mso
Last QA Review	
Last Changed	Dec 14 14:30:20 2006

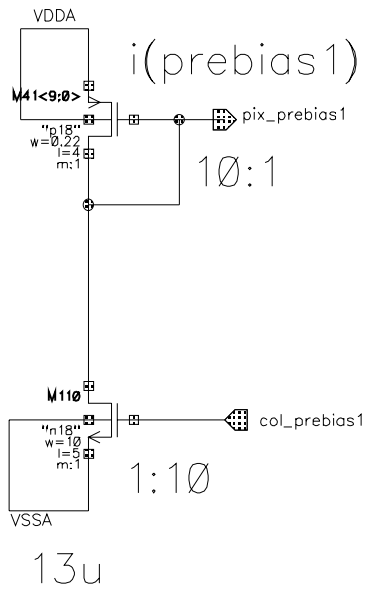
Pixel SF



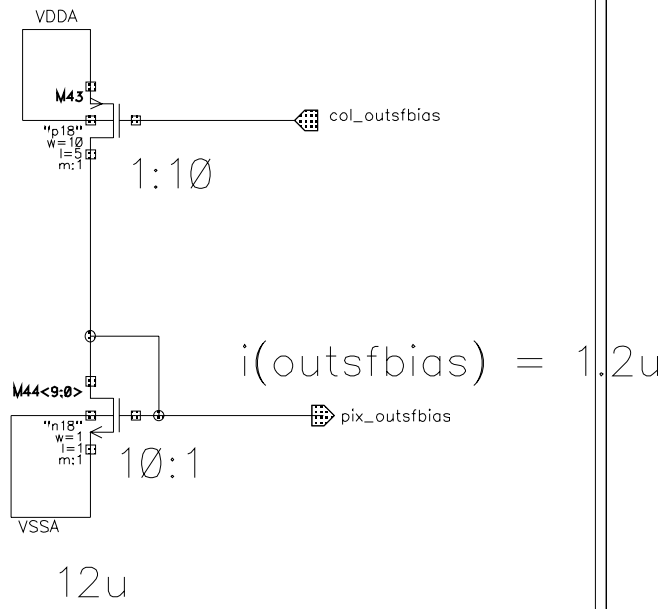
VDDA

VSSA

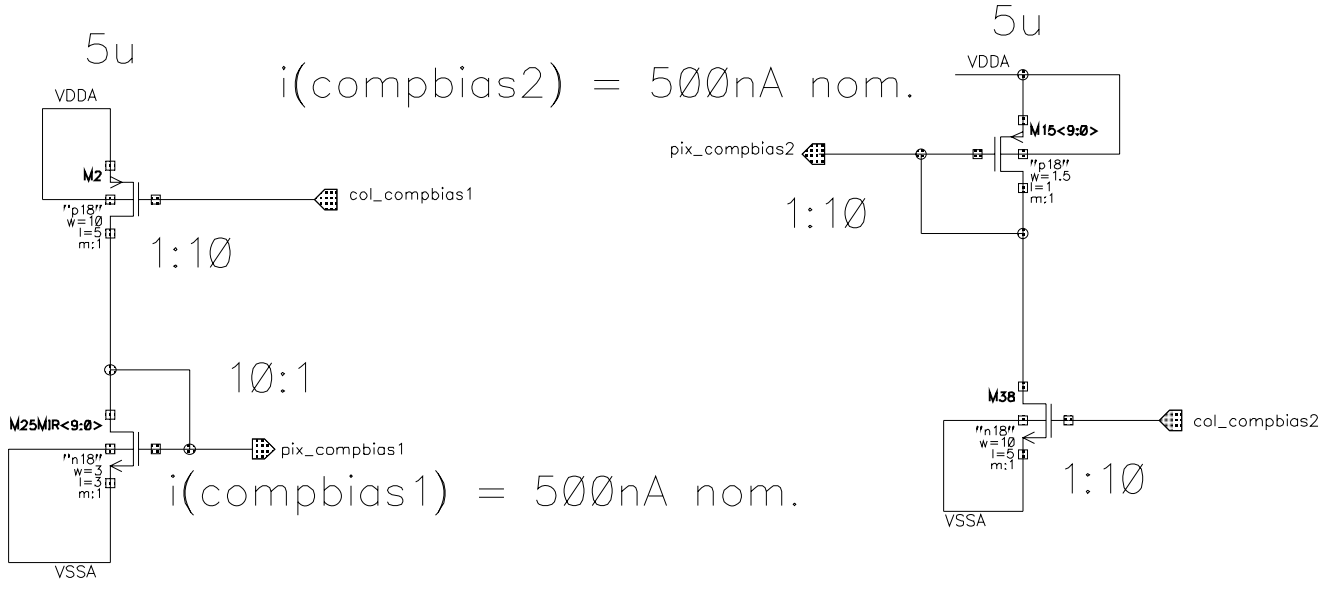
Preamp Bias



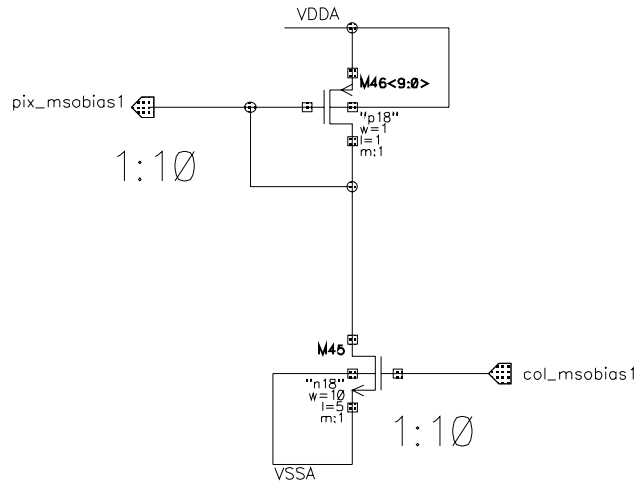
Out SF



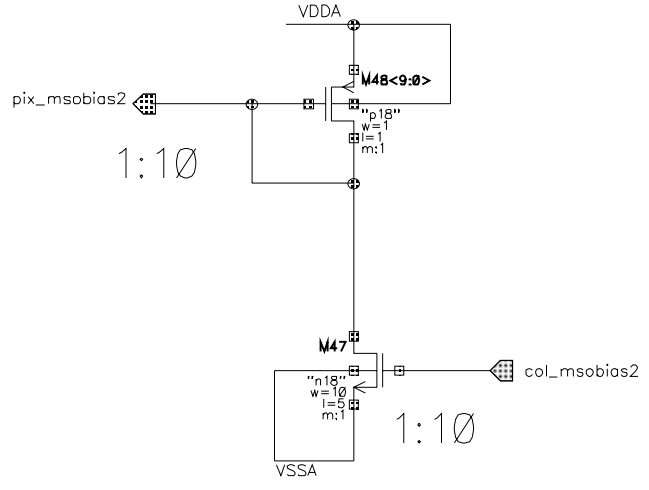
Comparator Bias



MS01



MS02



COLUMN CIRCUITS

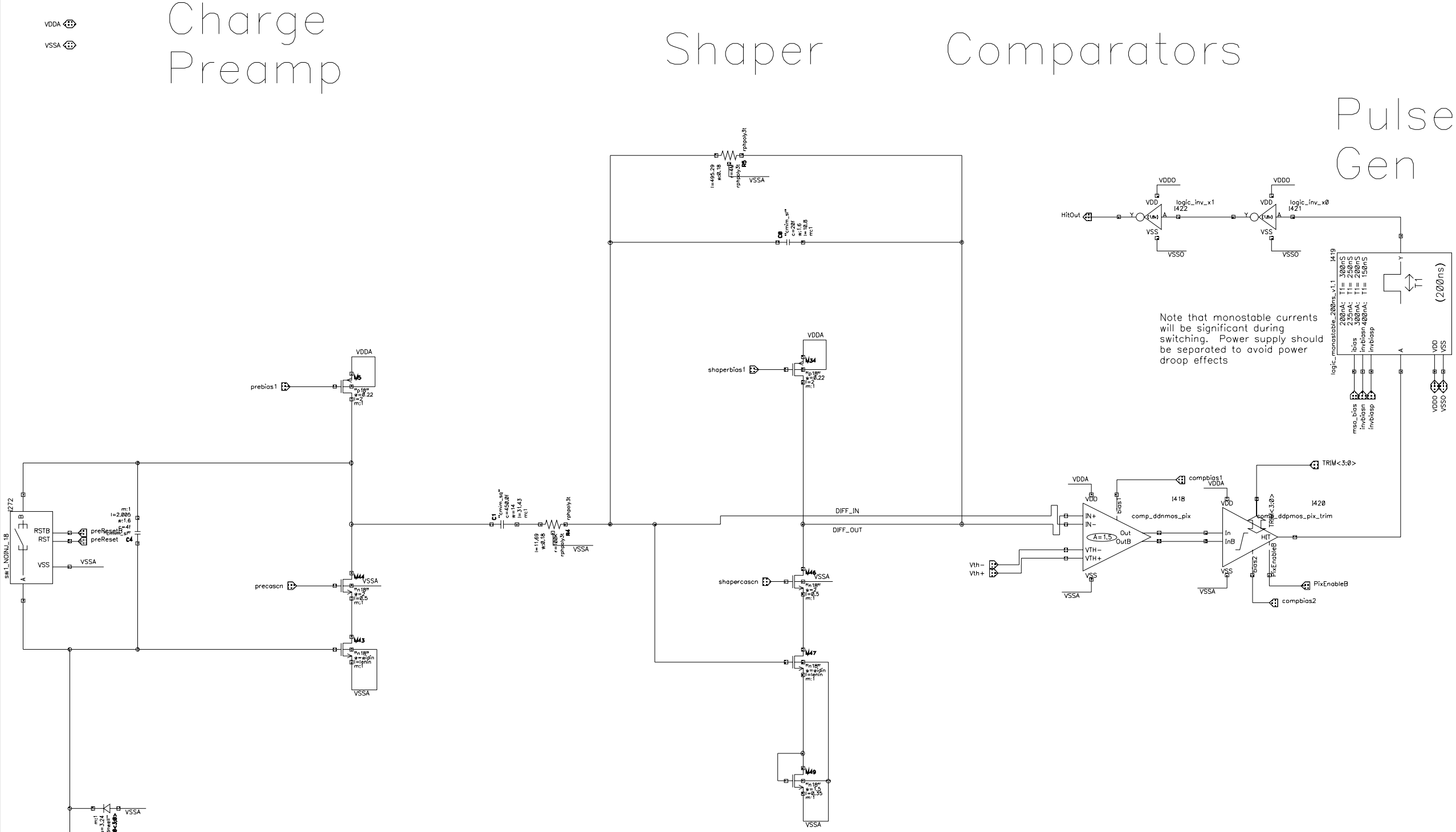
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prsmpIRT_col_v1.2
Last QA Review	
Last Changed	Dec 14 13:57:04 2006

Charge Preamp

Shaper

Comparators

Pulse Gen



i(prebias1) = 1.5uA nom.

precascn = 1.5v

i(shaperbias1) = 1.5uA nom.

shapercascn = 1.5v

i(compbias1) = 250nA nom.

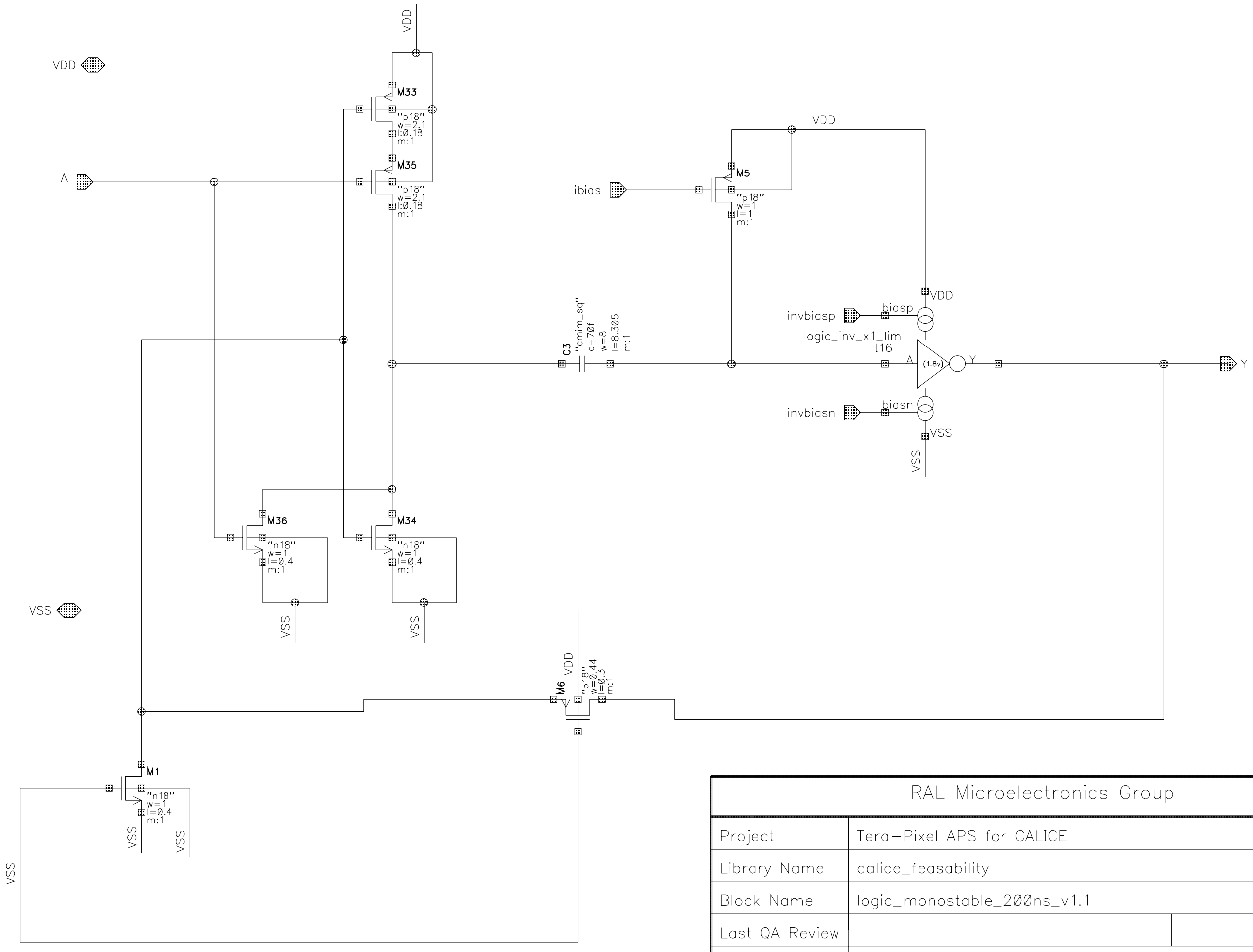
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_preshape_final_mso_v1.2
Last QA Review	
Last Changed	Dec 14 15:18:05 2006

Pulse Gen

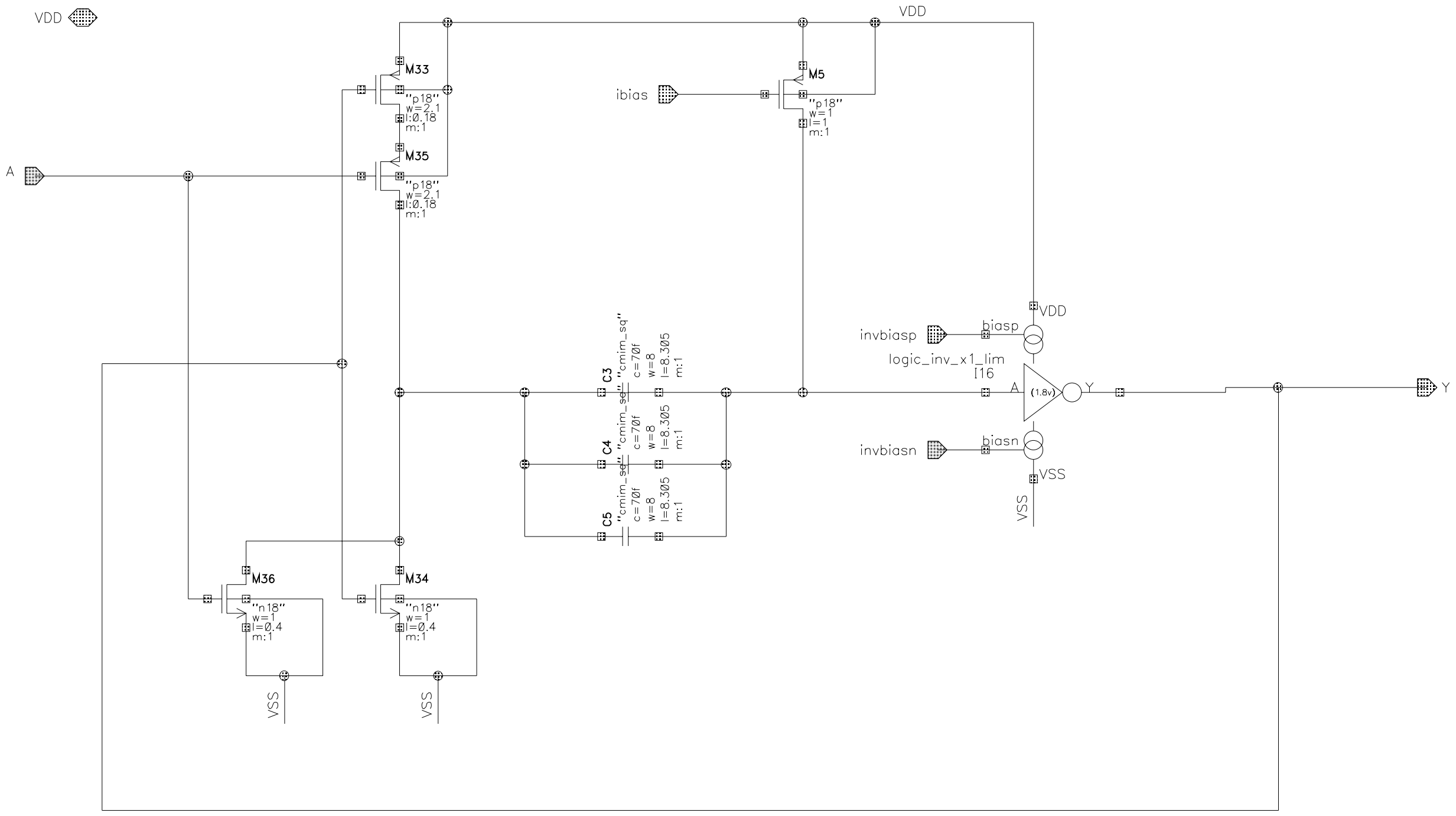
Comparators

SF Charge Amp SF Sample

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_presample_final_mso_v1.2
Last QA Review	
Last Changed	Dec 14 14:21:33 2006

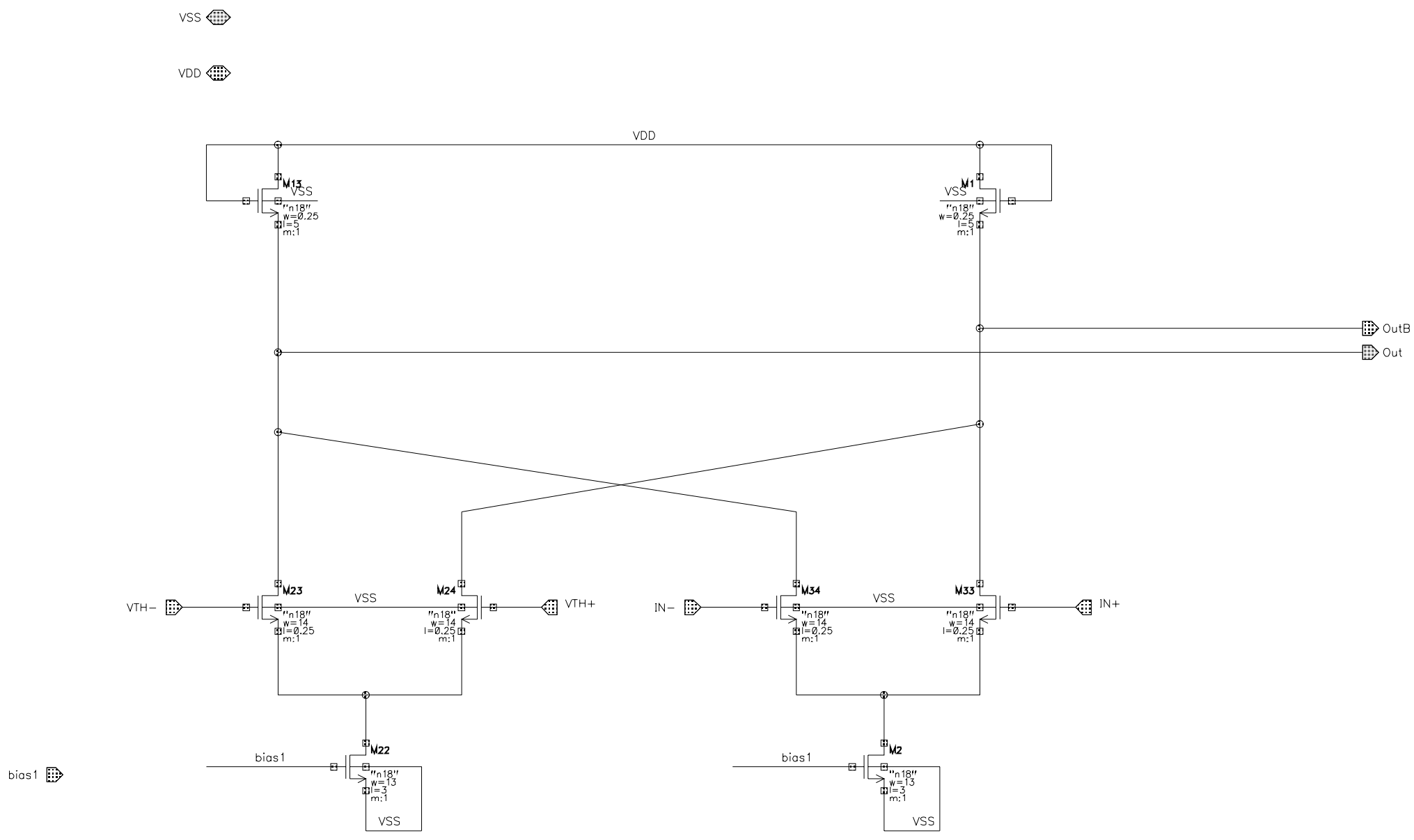


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_monostable_200ns_v1.1
Last QA Review	
Last Changed	Dec 13 14:07:22 2006



VSS

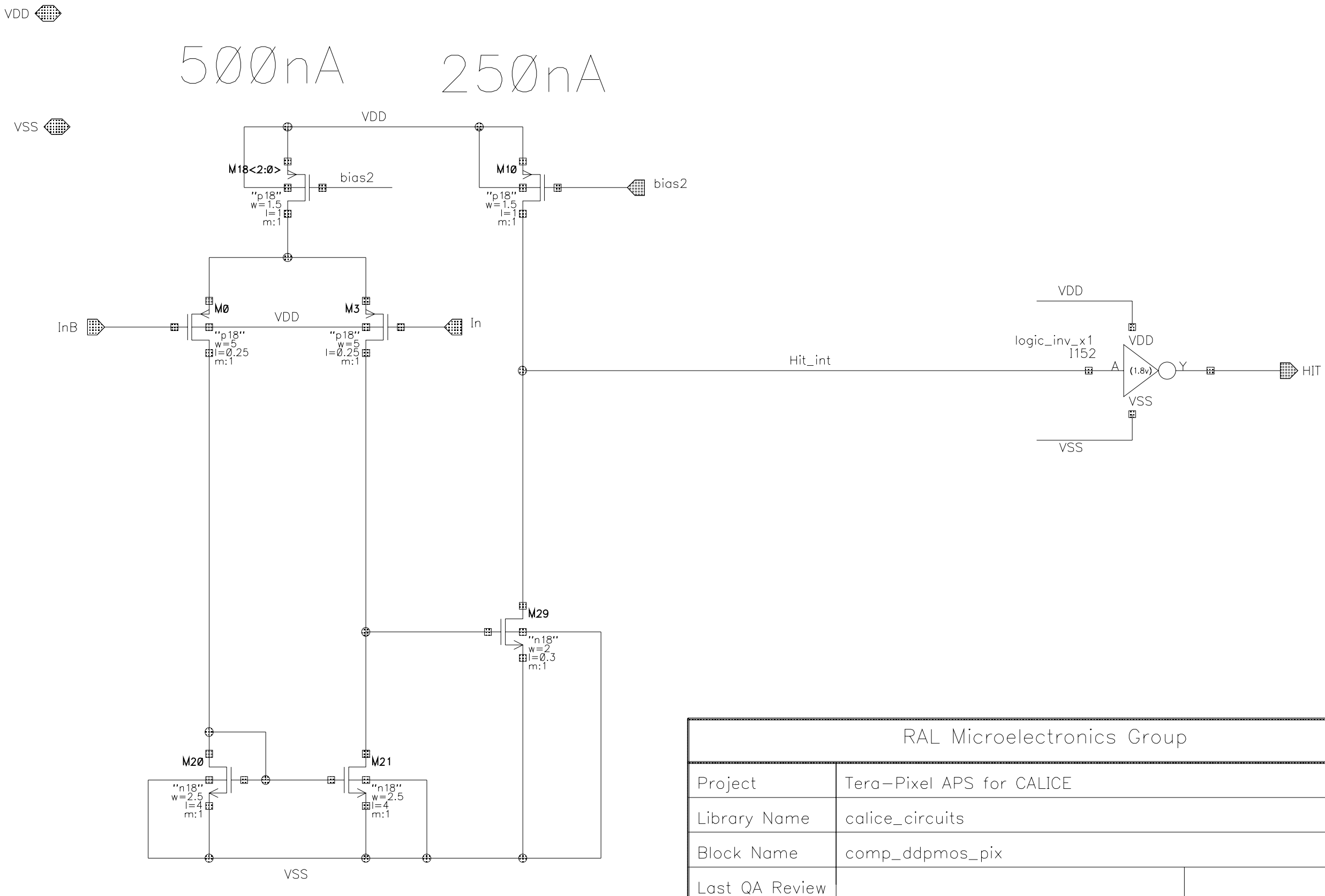
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_monostable_600ns_v1.1
Last QA Review	
Last Changed	Dec 14 13:48:09 2006



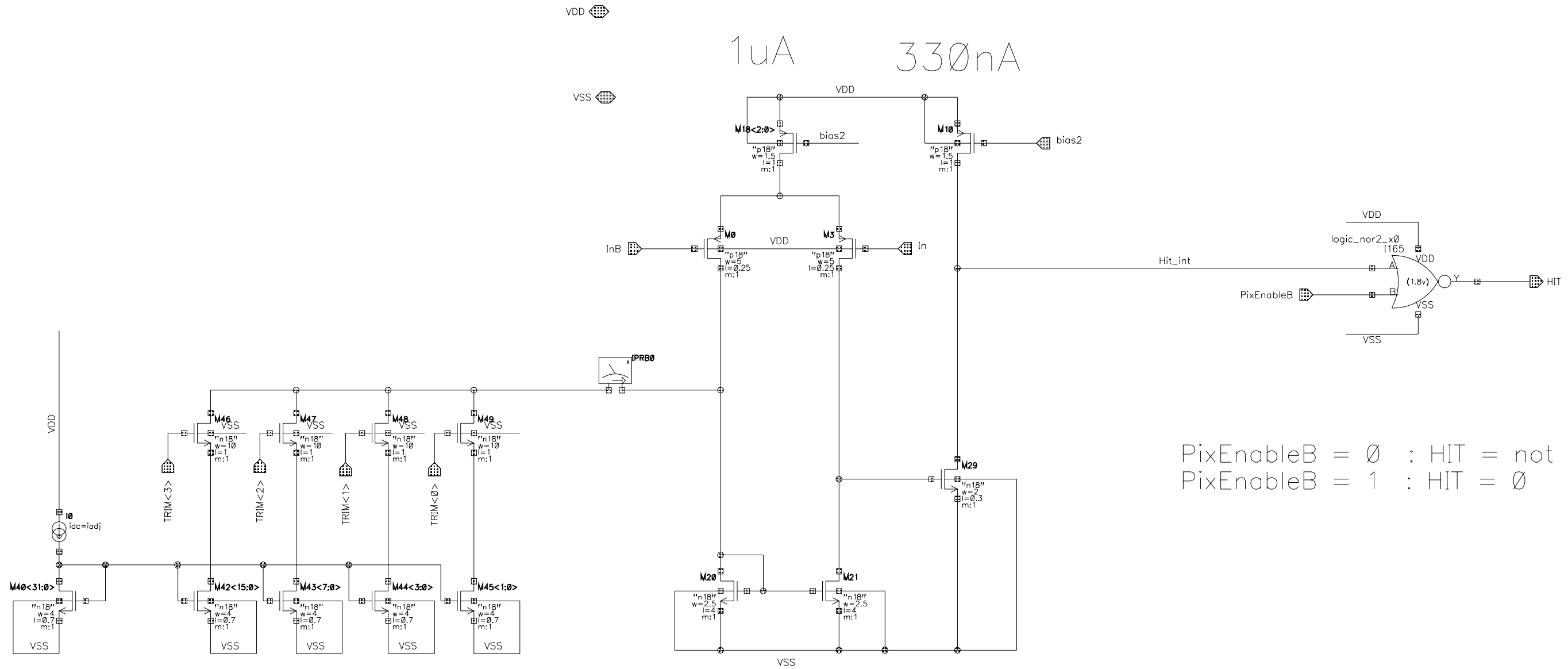
differential (10s of mV) hit signal wired across to pmos comparator at row logic

RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Dec 11 16:16:13 2006

<<<<< AT ROW LOGIC >>>>>



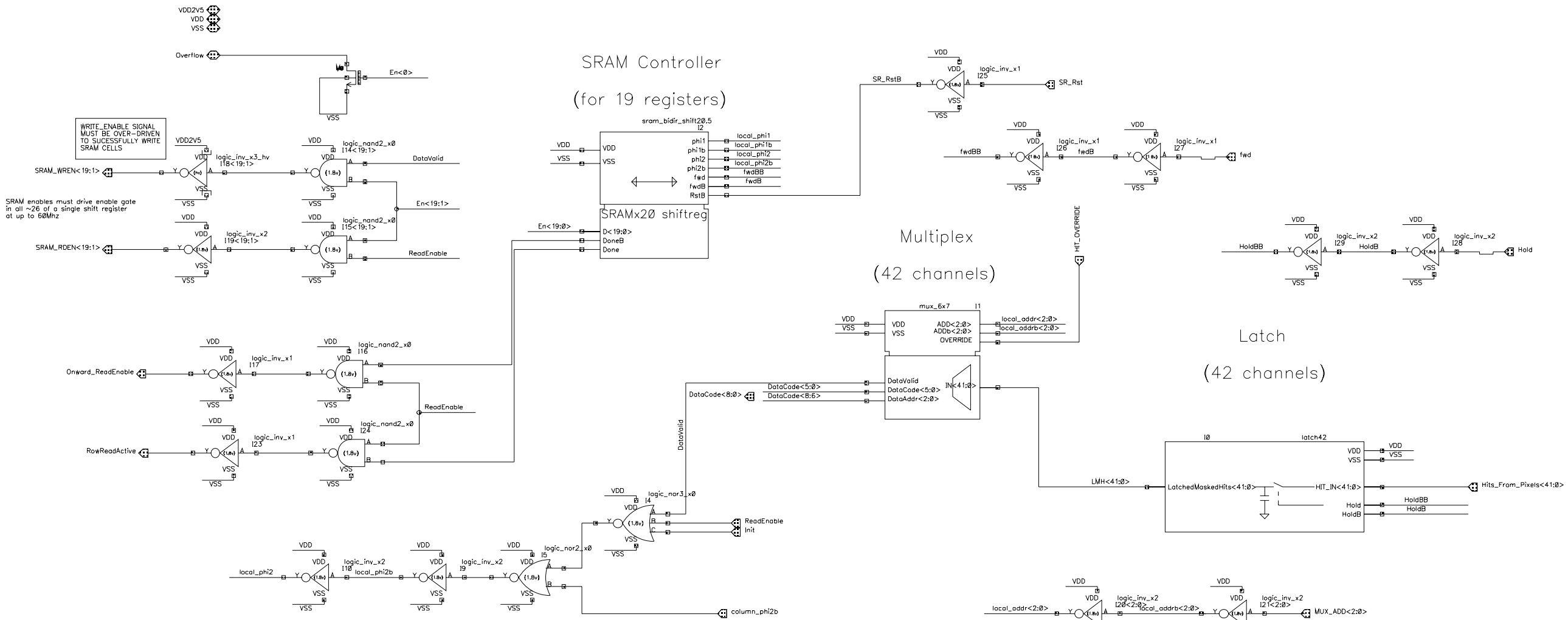
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	comp_ddpmos_pix	
Last QA Review		
Last Changed	Nov 24 16:22:21 2006	



PixEnableB = Ø : HIT = not Hit_Int
PixEnableB = 1 : HIT = Ø

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddpmos_pix_trim
Last QA Review	
Last Changed	Dec 7 11:11:15 2006

42-CHANNEL VERSION



TO DO / NOTES

Check drive strengths of all logic parts – only drawn for functionality so far – not tested for loading and edge speeds

Note that no onward clock buffering is included in this cell – next level up should implement periodic clock buffers to propagate mask & SR control clocks up the columns

May need level shifting / 3.3v tolerant input gates at the Hits_From_Pixels input or in the Mask+Latch logic (these signals are likely to be 3.3v signals from analog circuits in the pixel).

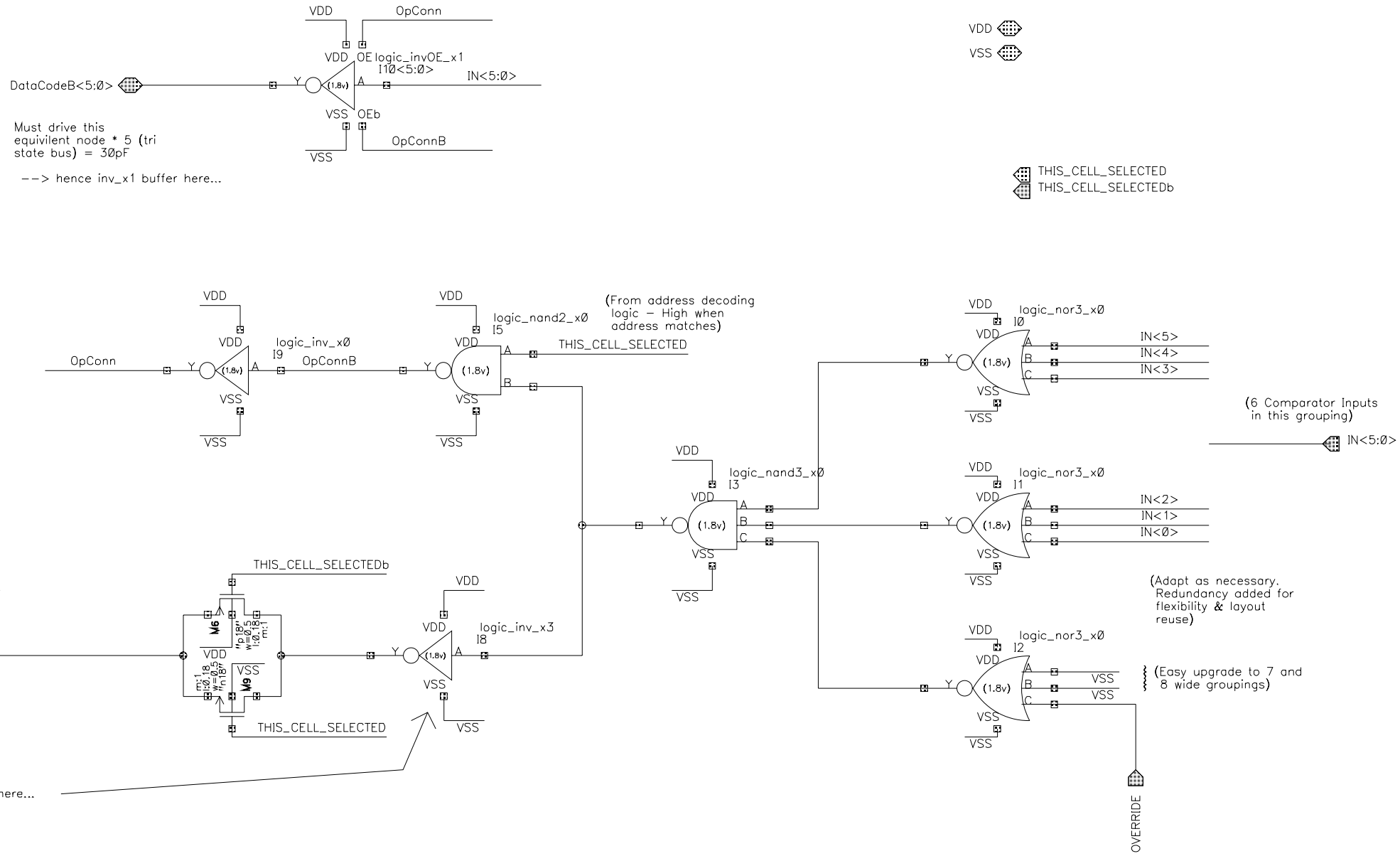
N/A for 1.8v pixel

SRAM clocks are distributed as inverse polarity

is convenient for phi2 gating, since the inverted phi2 input to the NOR gate completes inversion of its inputs and outputs to turn it into an AND gate.

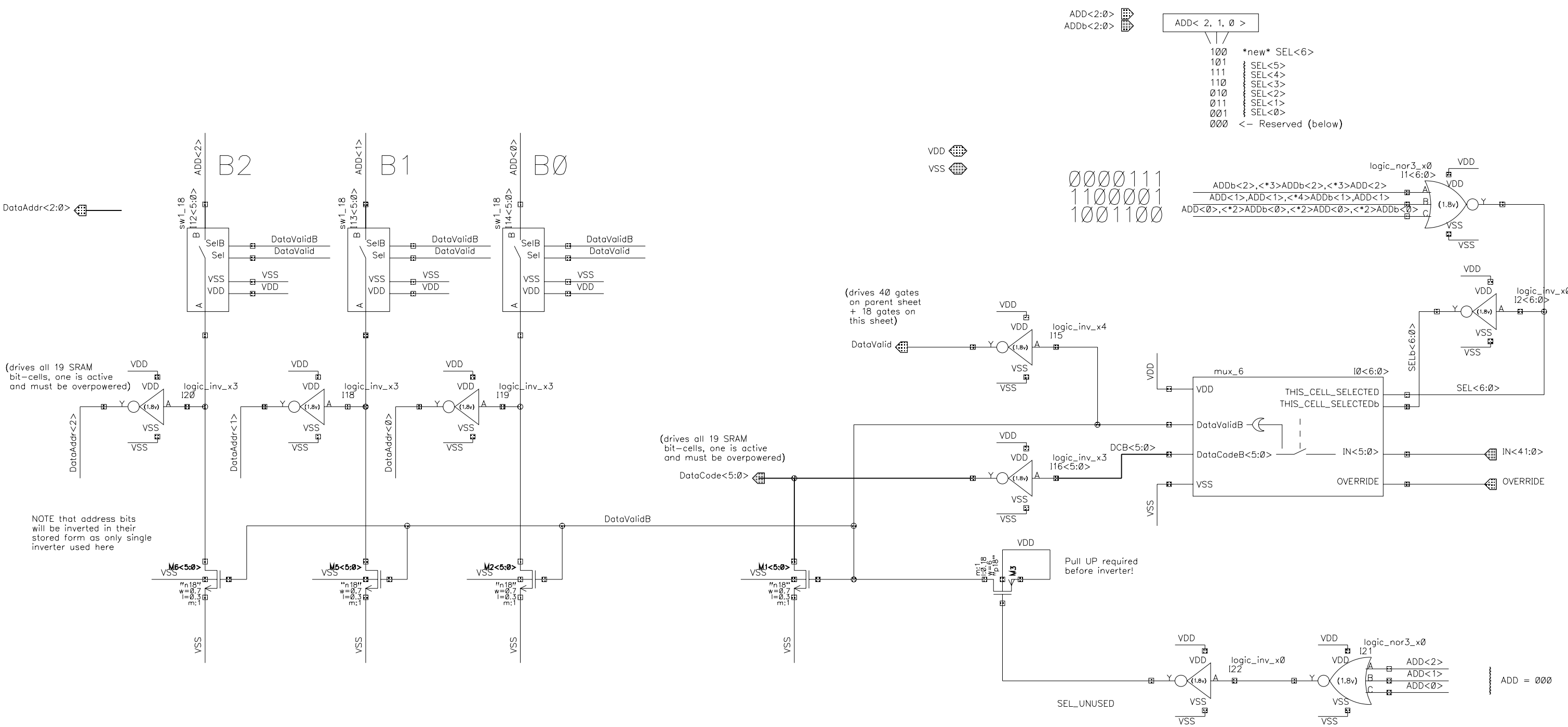
phi1 is distributed in inverted form for consistency

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	master_row_controller_42.1
Last QA Review	
Last Changed	Dec 11 16:41:38 2006



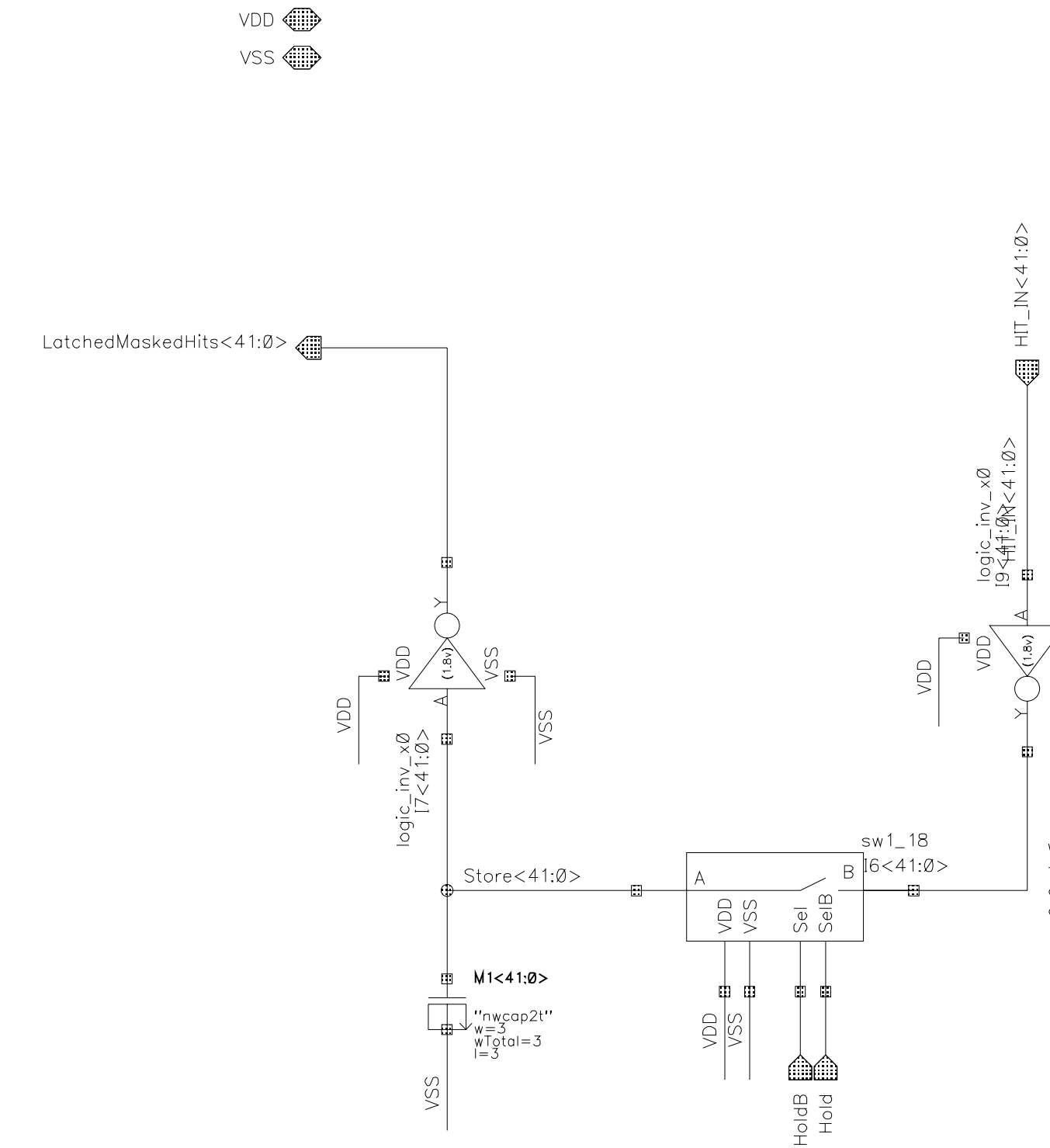
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6
Last QA Review	
Last Changed	Sep 28 11:41:55 2006

Address Decoding



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6x7
Last QA Review	
Last Changed	Dec 5 15:14:03 2006

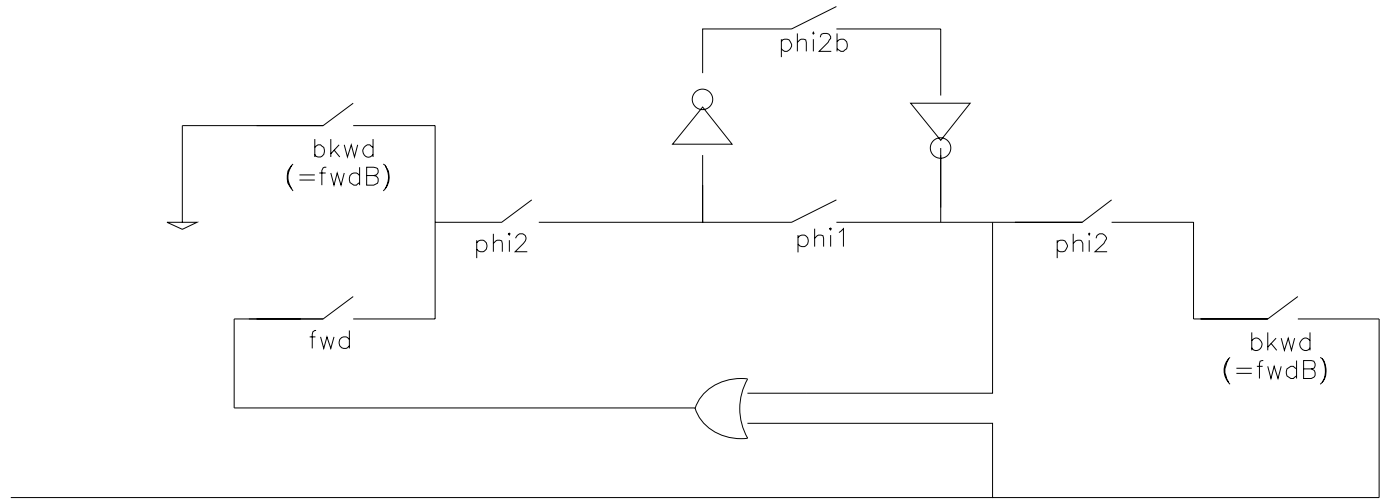
Assume each clock input
is connected to 126 gates
Local buffer required for
every row.



When Hold goes high, the switch
turns off, preserving the state
of the AND output at that time
on the storage node

NB: Check lifetime and leakage on this storage cap
Default (non-hit) case is to charge this cap to 1.8v

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	latch42
Last QA Review	
Last Changed	Dec 5 13:28:12 2006



POWER UP

phi1 off
phi2 on
RstB on (low)

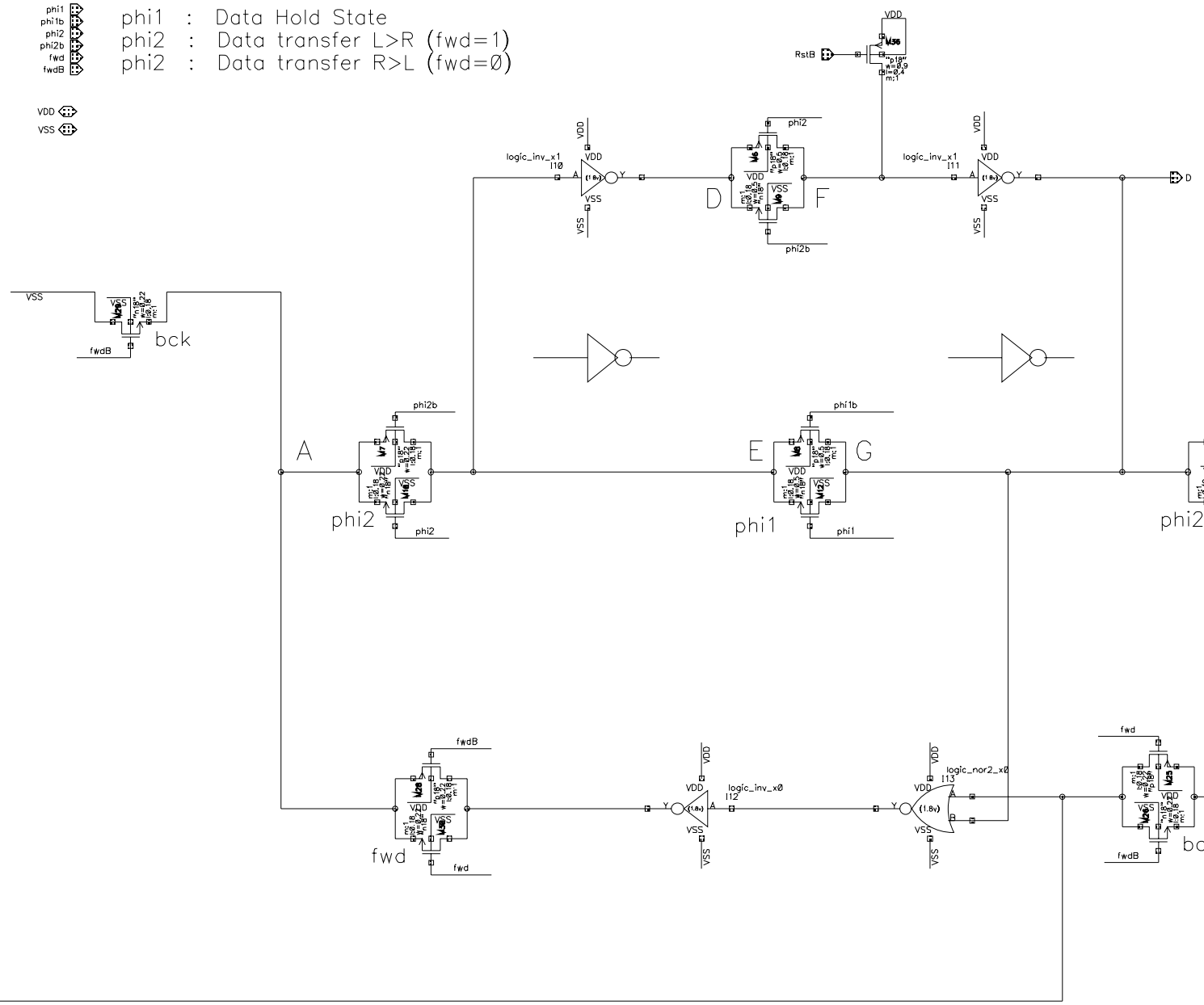
IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low)
during phi2

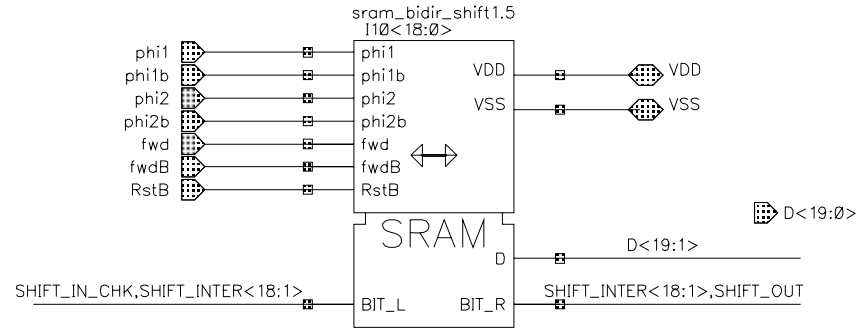
INVALID STATE

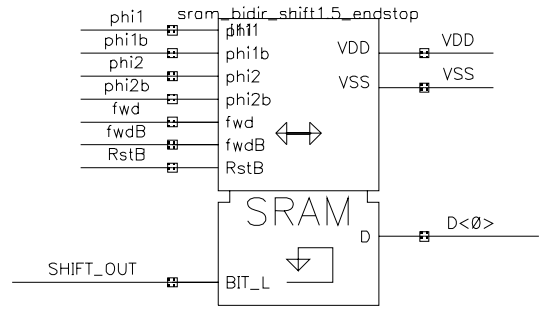
phi1 X
phi2 off (low)
RstB on (low)

phi1 : Data Hold State
phi2 : Data transfer L>R (fwd=1)
phi2 : Data transfer R>L (fwd=Ø)

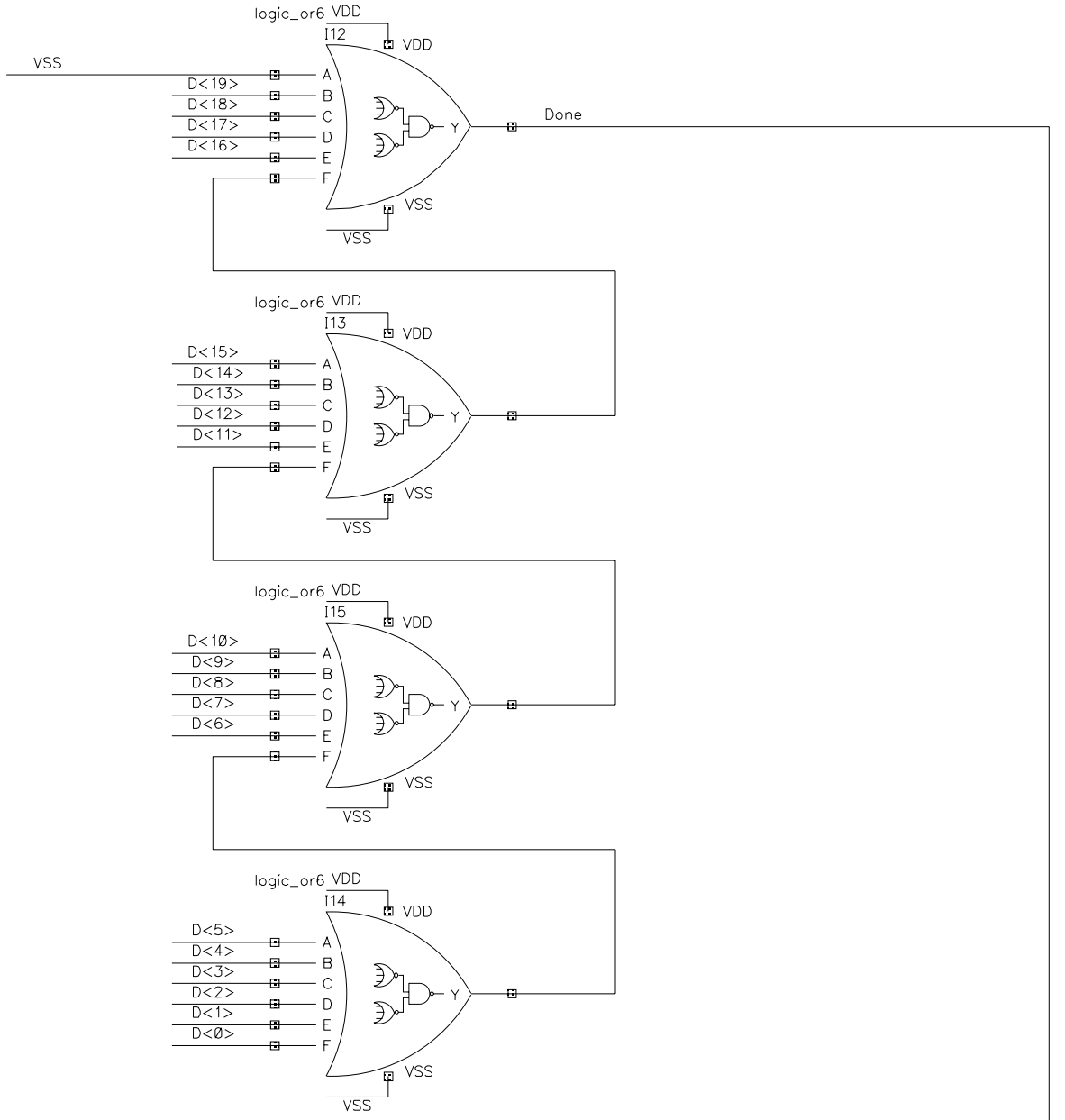


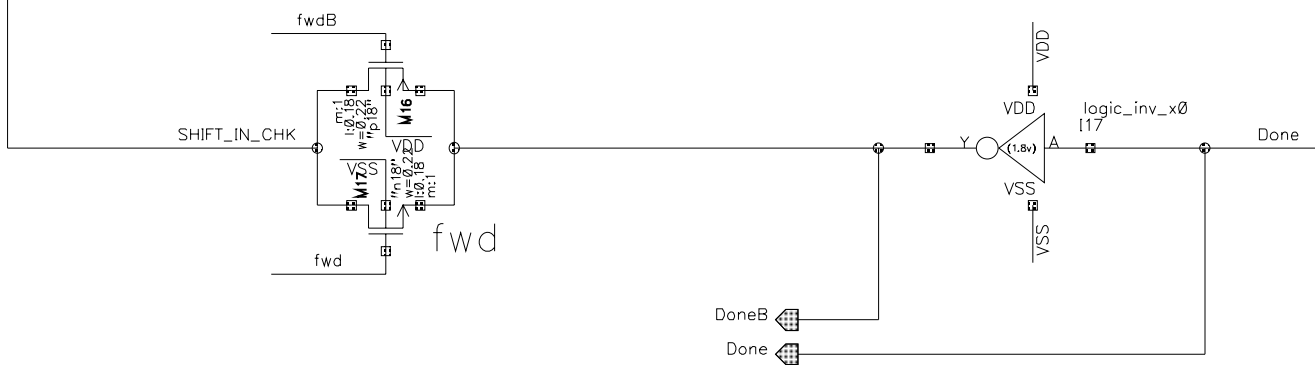
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bidir_shift1.5_endstop
Last OA Review	
Last Changed	Dec 9 09:20:13 2006





NB: Shift reg resets to 10000000000000000000

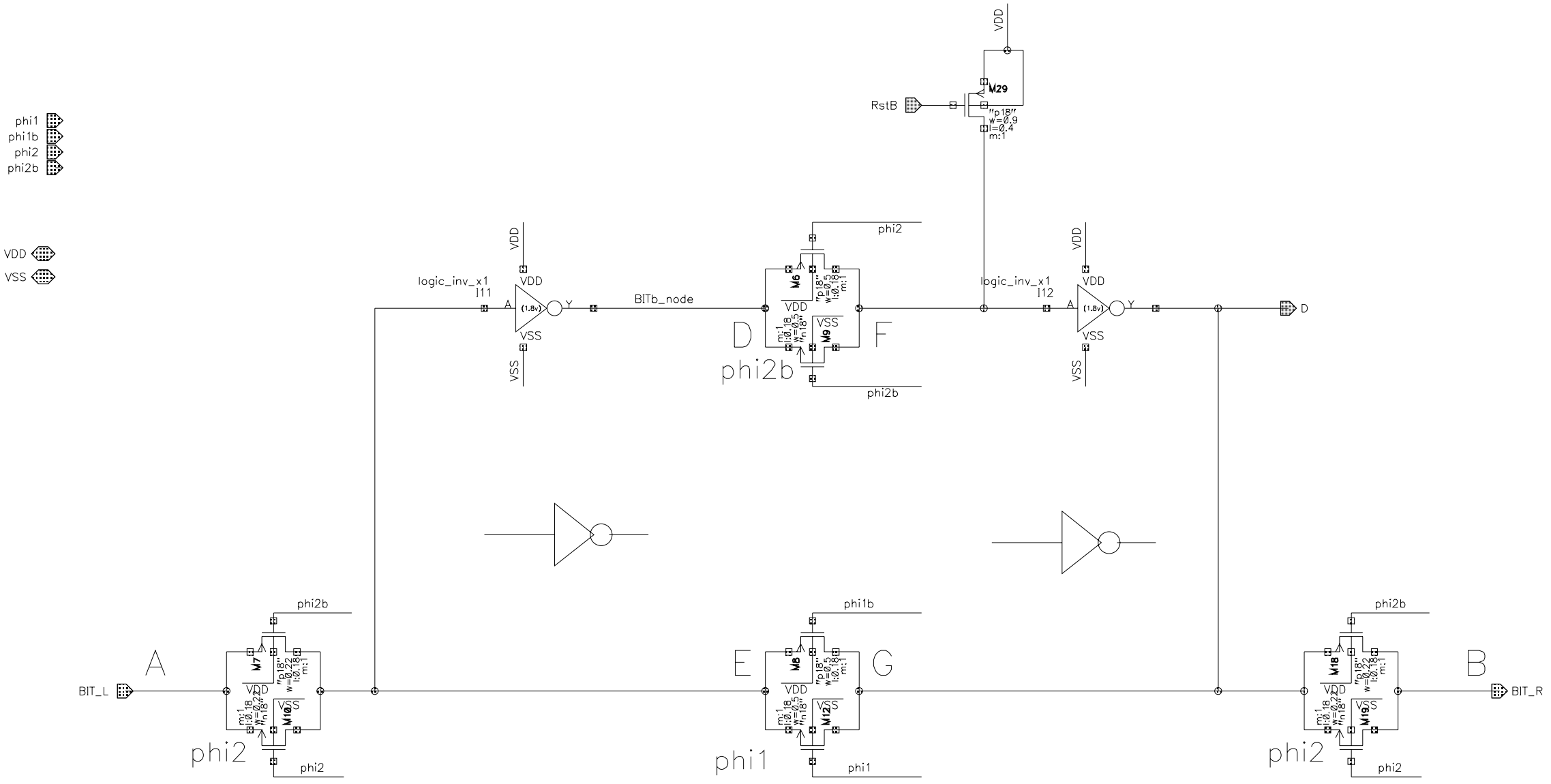




RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bidir_shift20.5
Last QA Review	
Last Changed	Dec 9 10:48:05 2006

New Shiftreg Revision 1.3

> Inverters made equal size (x1)
> Added reset transistor



POWER UP

phi1 off
phi2 on
RstB on (low)

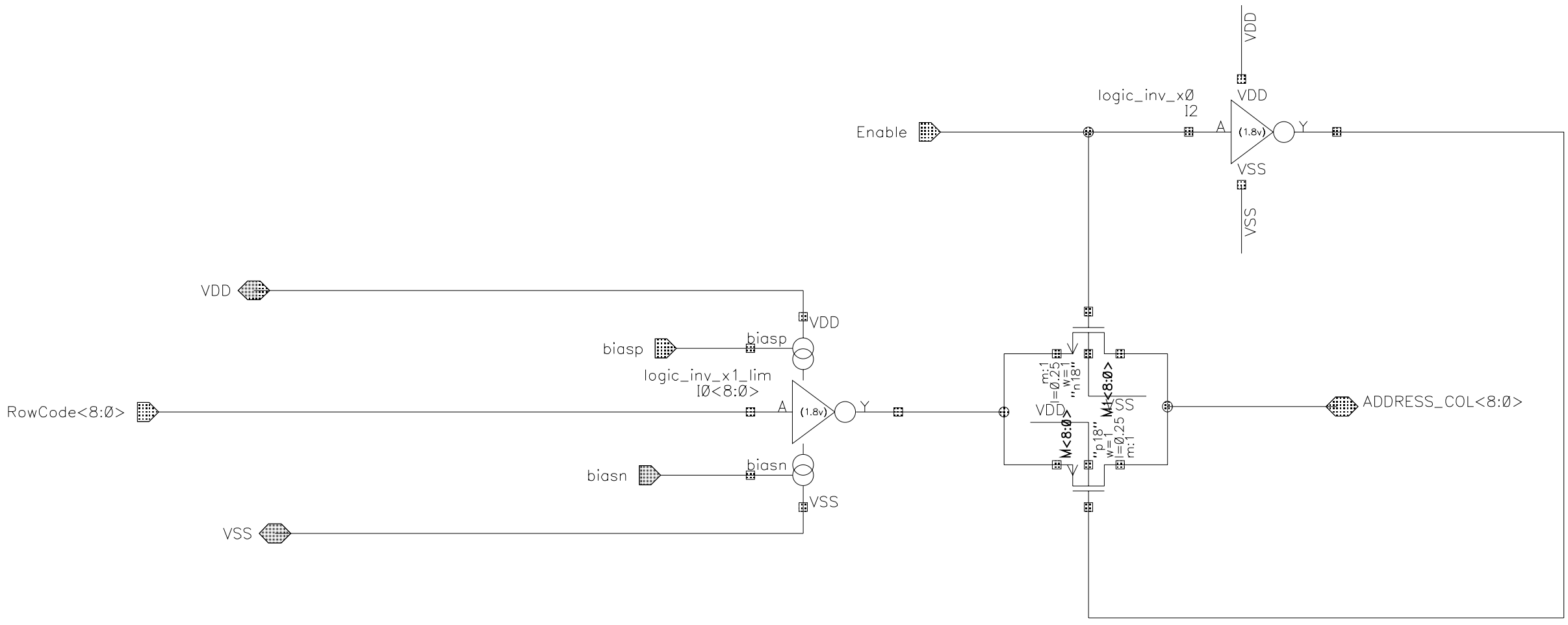
IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low)
during phi2

INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)

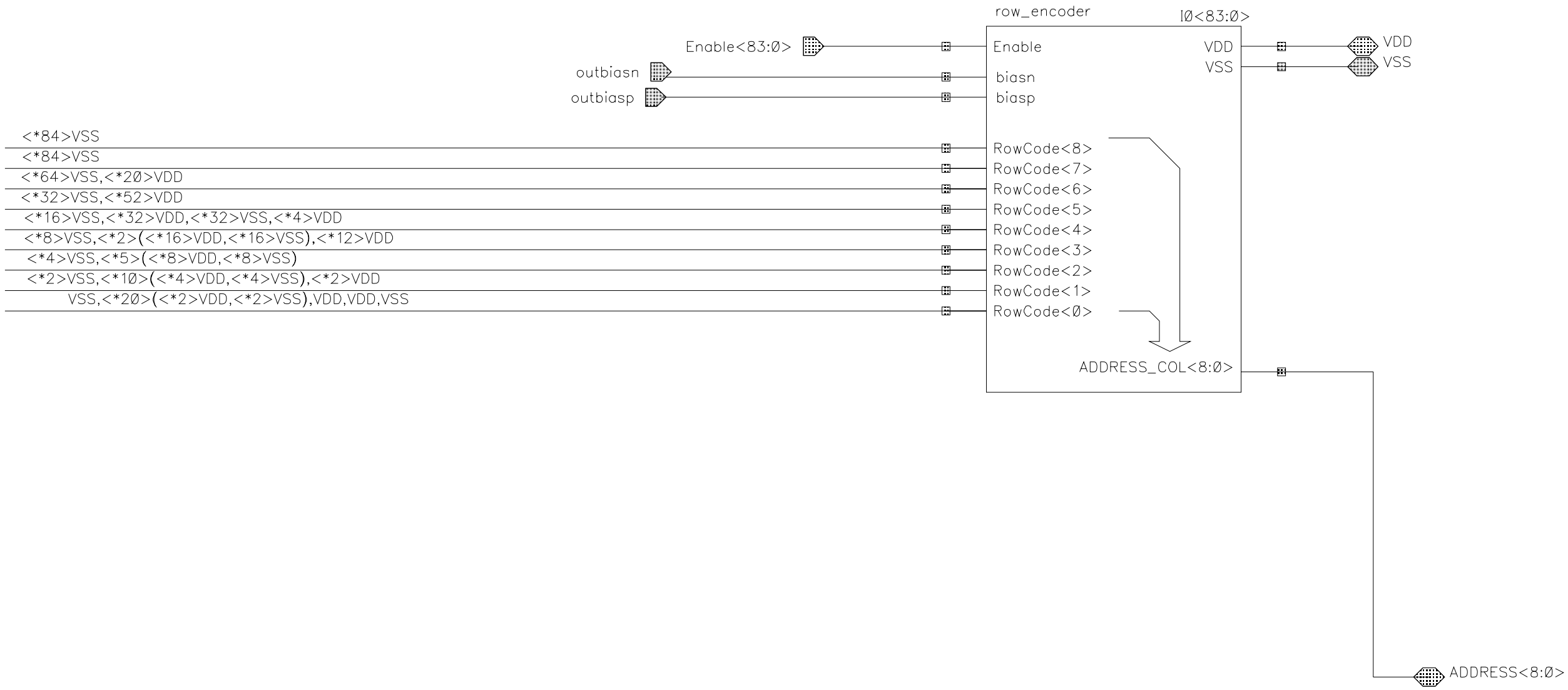
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift1.3
Last QA Review	
Last Changed	Dec 5 14:23:33 2006



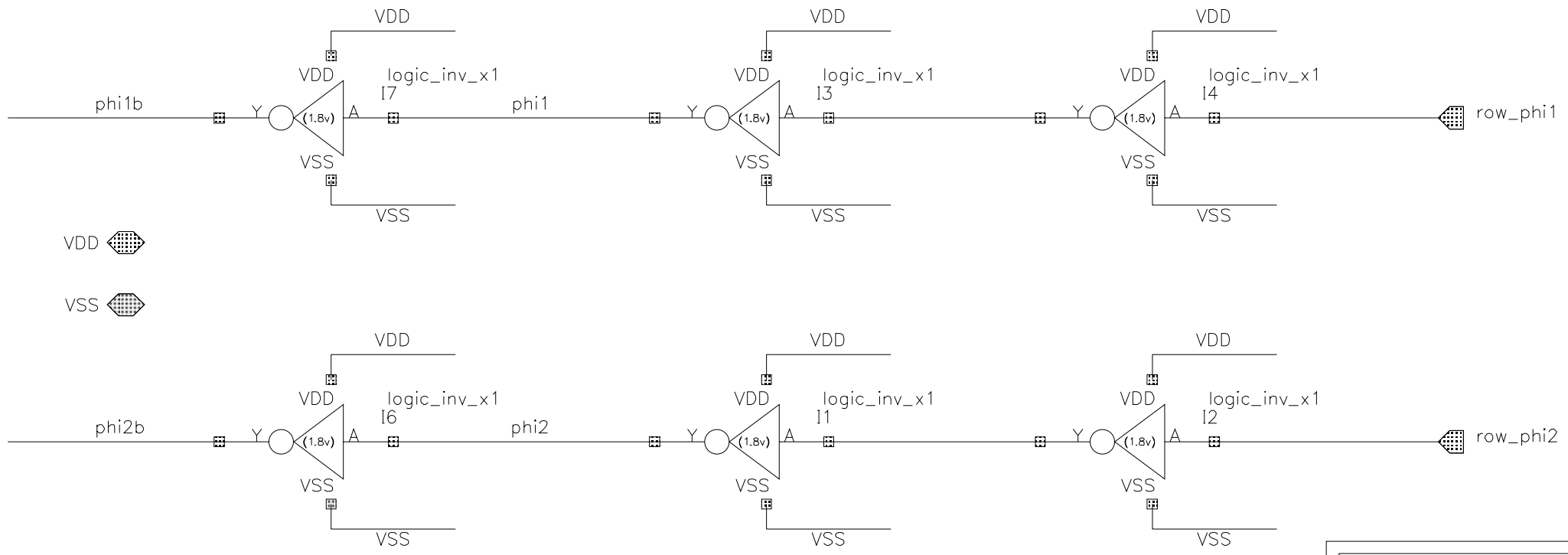
Set Row Code input to the unique row address: with net names in schematics; with repeated tie up/down cells in layout.

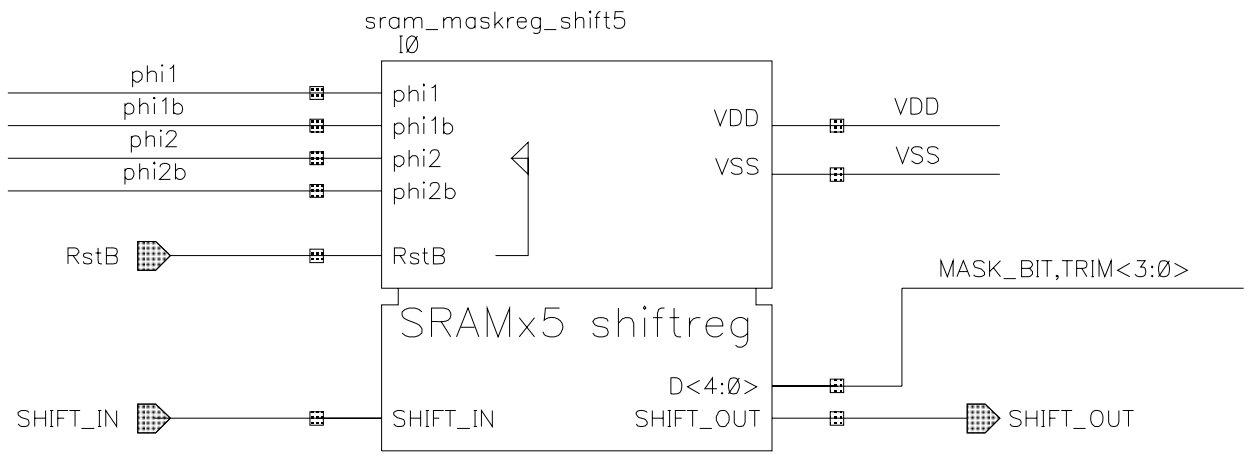
GRAY CODE should be used

RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	row_encoder	
Last QA Review		
Last Changed	Dec 8 11:53:09 2006	



RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	row_encoder_84	
Last QA Review		
Last Changed	Dec 13 11:11:22 2006	





MASK_BIT

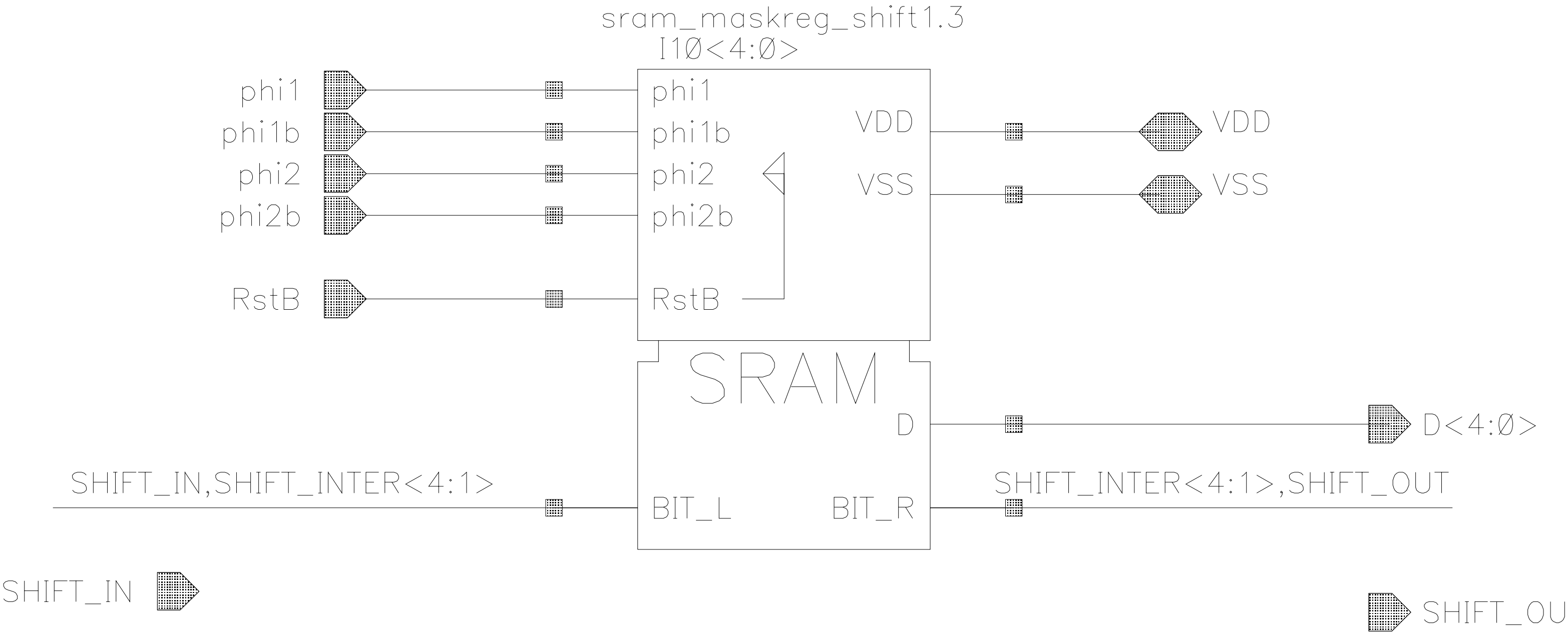
TRIM<3:0>

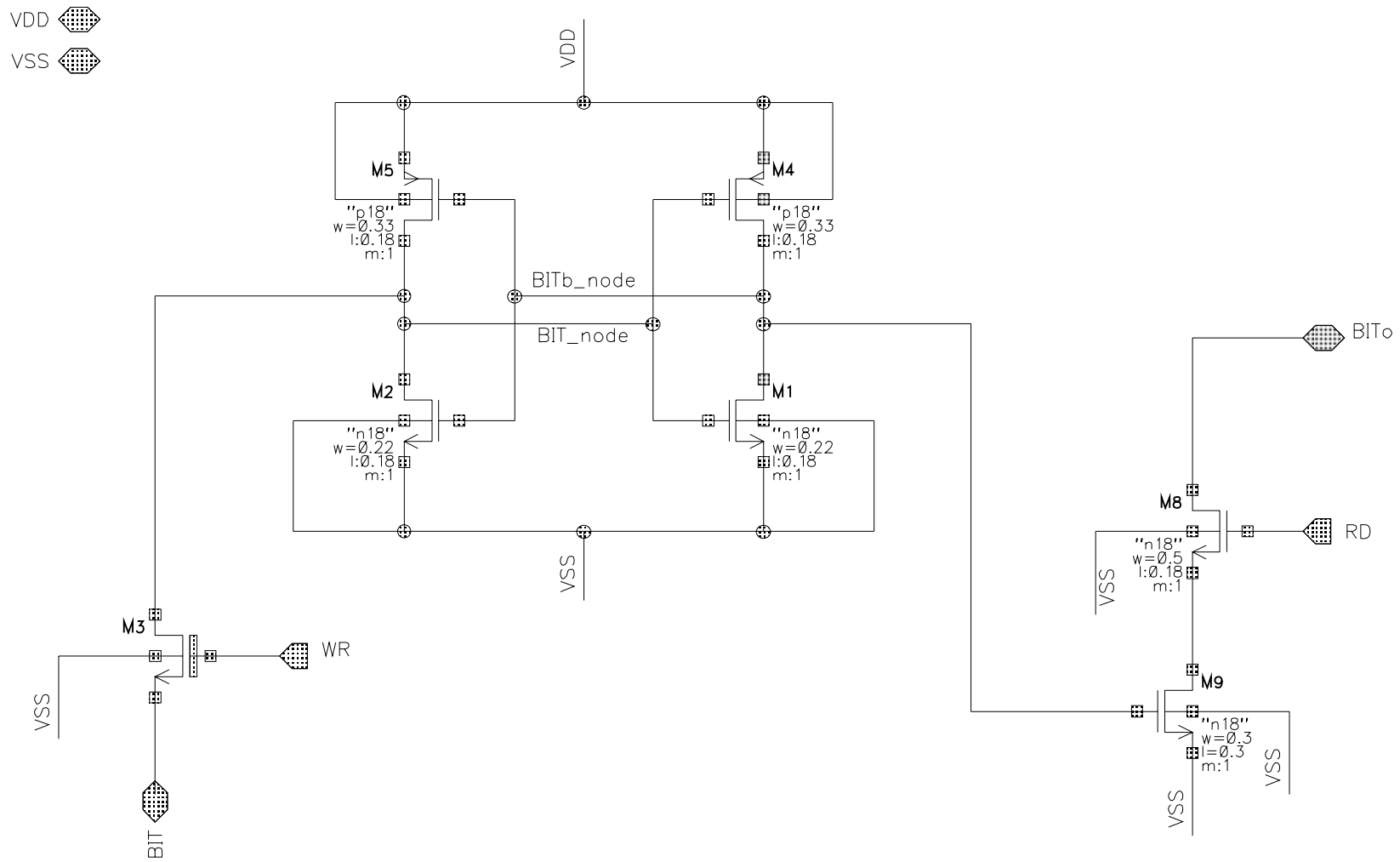
5 bit pixel config code:

MSB = Mask
3:0 = Trim

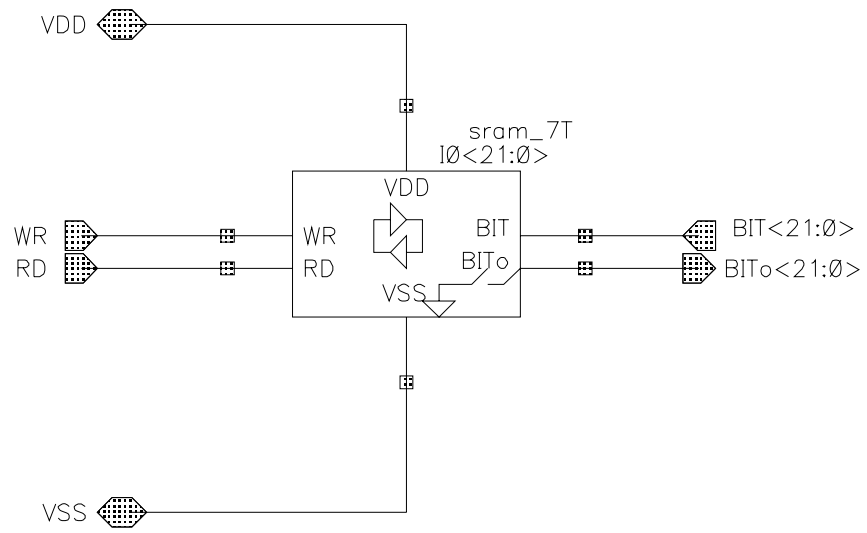
Data shifts in LSB first

RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	maskreg5	
Last QA Review		
Last Changed	Dec 6 15:24:19 2006	

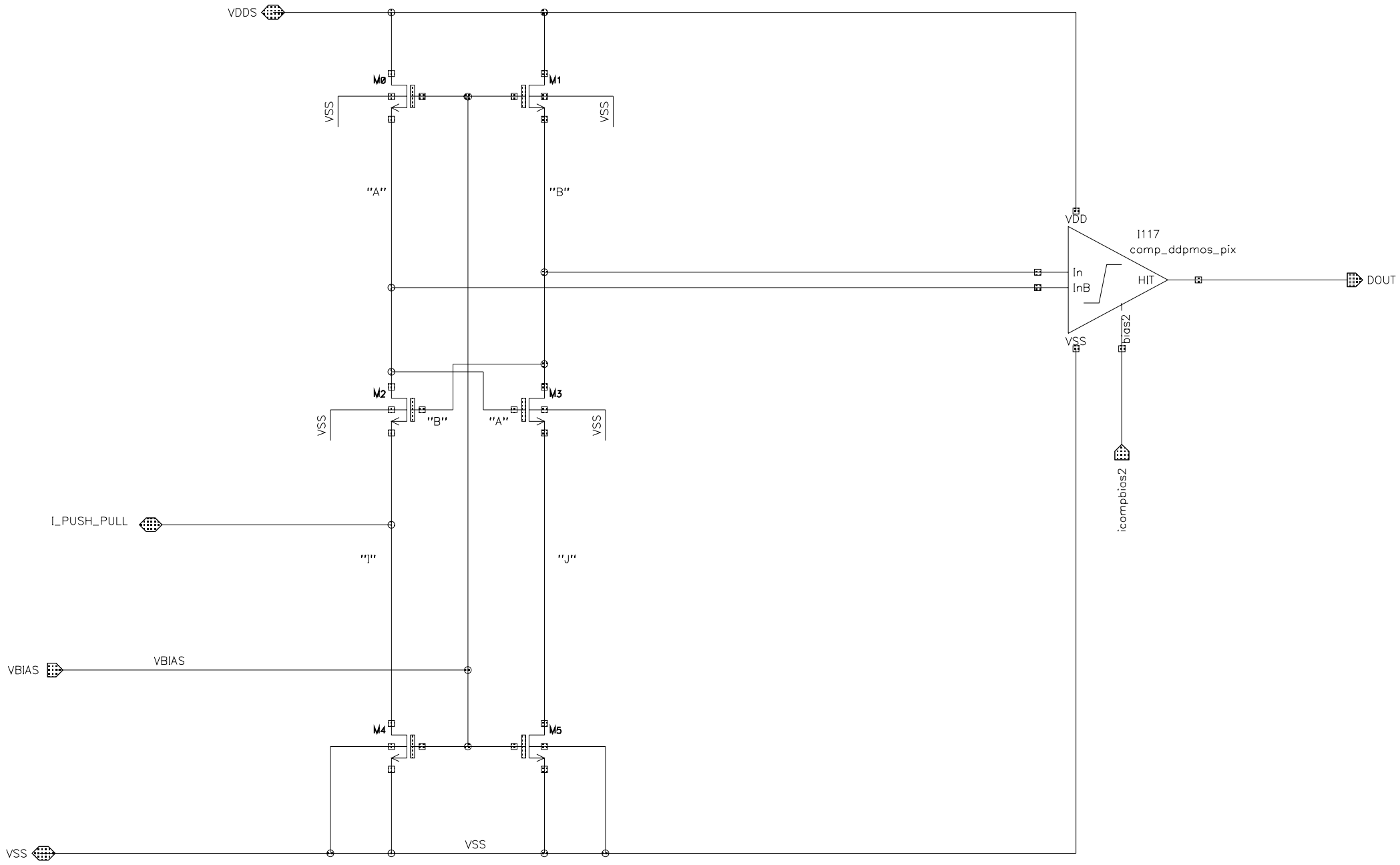

sram_maskreg_shift1.3
I10<4:0>
phi1
phi1b
phi2
phi2b
RstB
phi1
phi1b
phi2
phi2b
RstB
VDD
VSS
SRAM
D
BIT_L
BIT_R
VDD
VSS
D<4:0>
SHIFT_IN,SHIFT_INTER<4:1>
SHIFT_INTER<4:1>,SHIFT_OUT
SHIFT_IN
SHIFT_OU



RAL Microelectronics Group		
Project	Tera–Pixel APS for CALICE	
Library Name	calice_feasability	
Block Name	sram_7T	
Last QA Review		
Last Changed	Sep 29 13:22:30 2006	

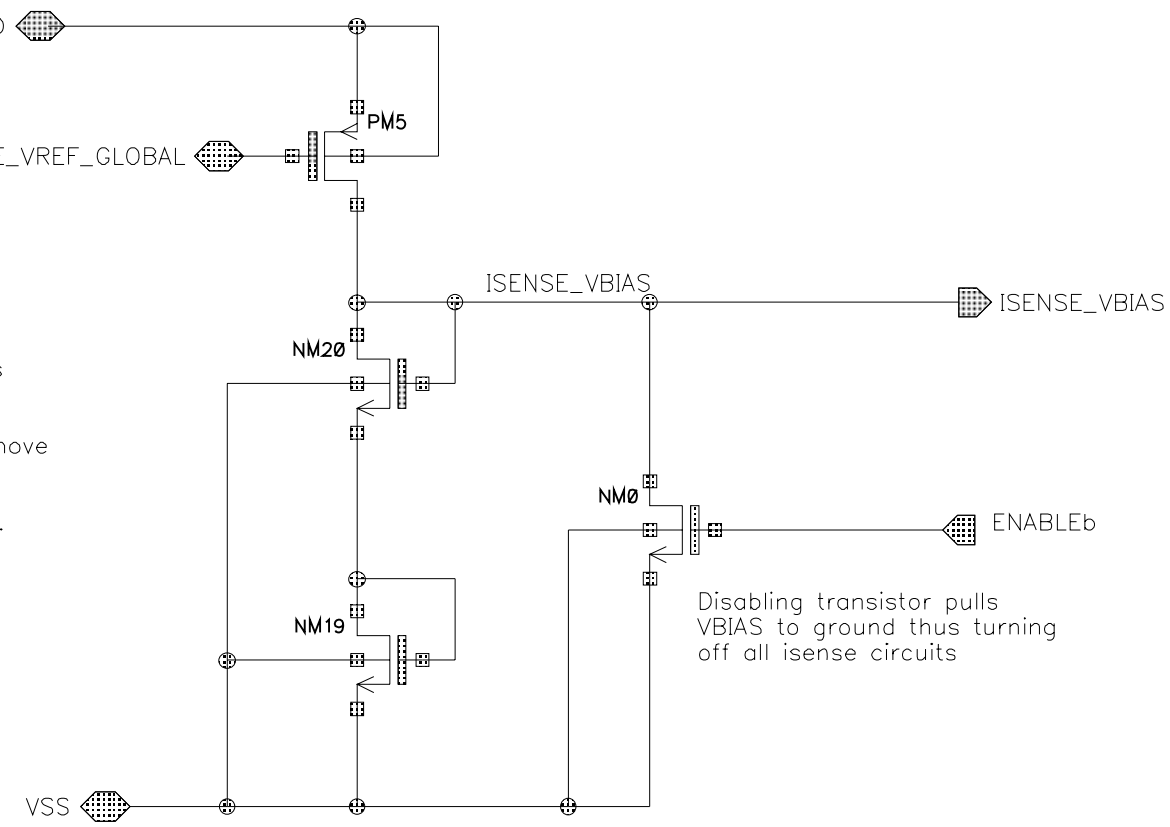


RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	sram_reg7.22	
Last QA Review		
Last Changed	Dec 12 17:09:22 2006	



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	i_sense_se_1bit_v1.2
Last QA Review	
Last Changed	Dec 15 10:46:29 2006

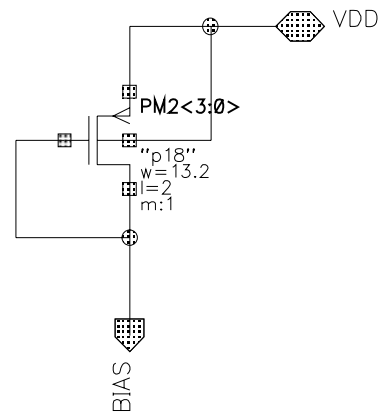
NOTE VDD MUST BE 3v3, hence hv transistors used



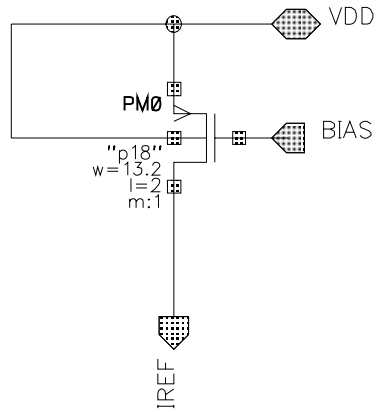
VBIAS generator circuit:
Current reference effectively sets current in sense amplifier, which effectively sets sensing speed.
Bias generator allows VBIAS to move with process corners maintaining approx constant current figure independant of process variation.

Disabling transistor pulls VBIAS to ground thus turning off all isense circuits

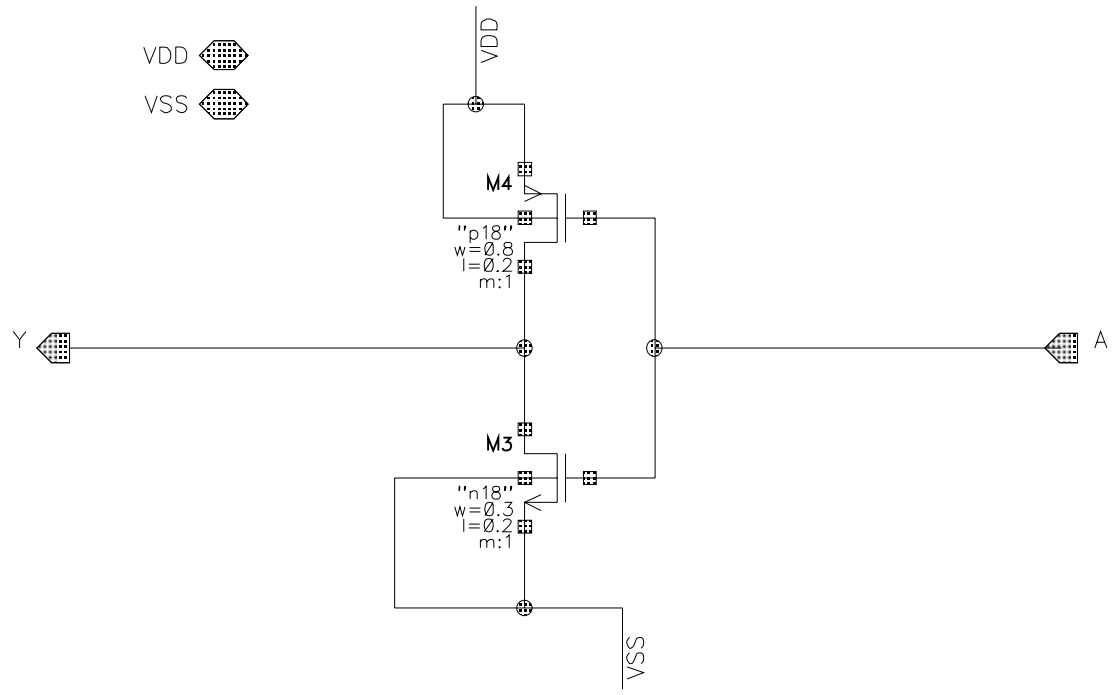
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	isense_bias_v1.2	
Last QA Review		
Last Changed	Dec 15 09:28:26 2006	



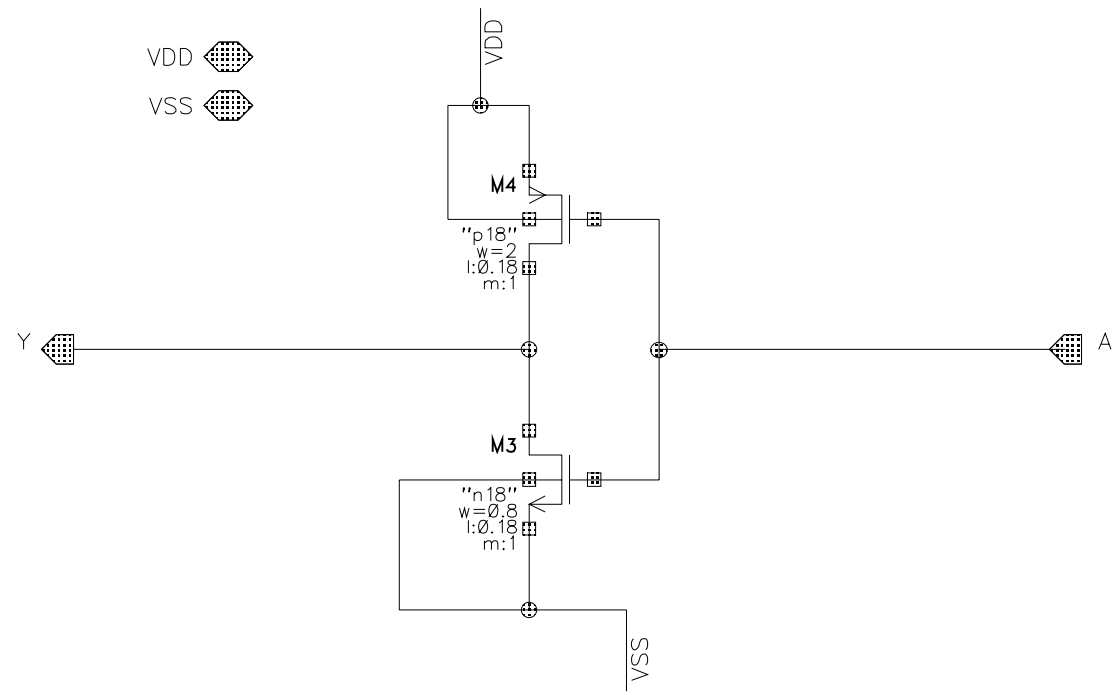
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_master_v1.2
Last QA Review	
Last Changed	Dec 14 11:49:02 2006



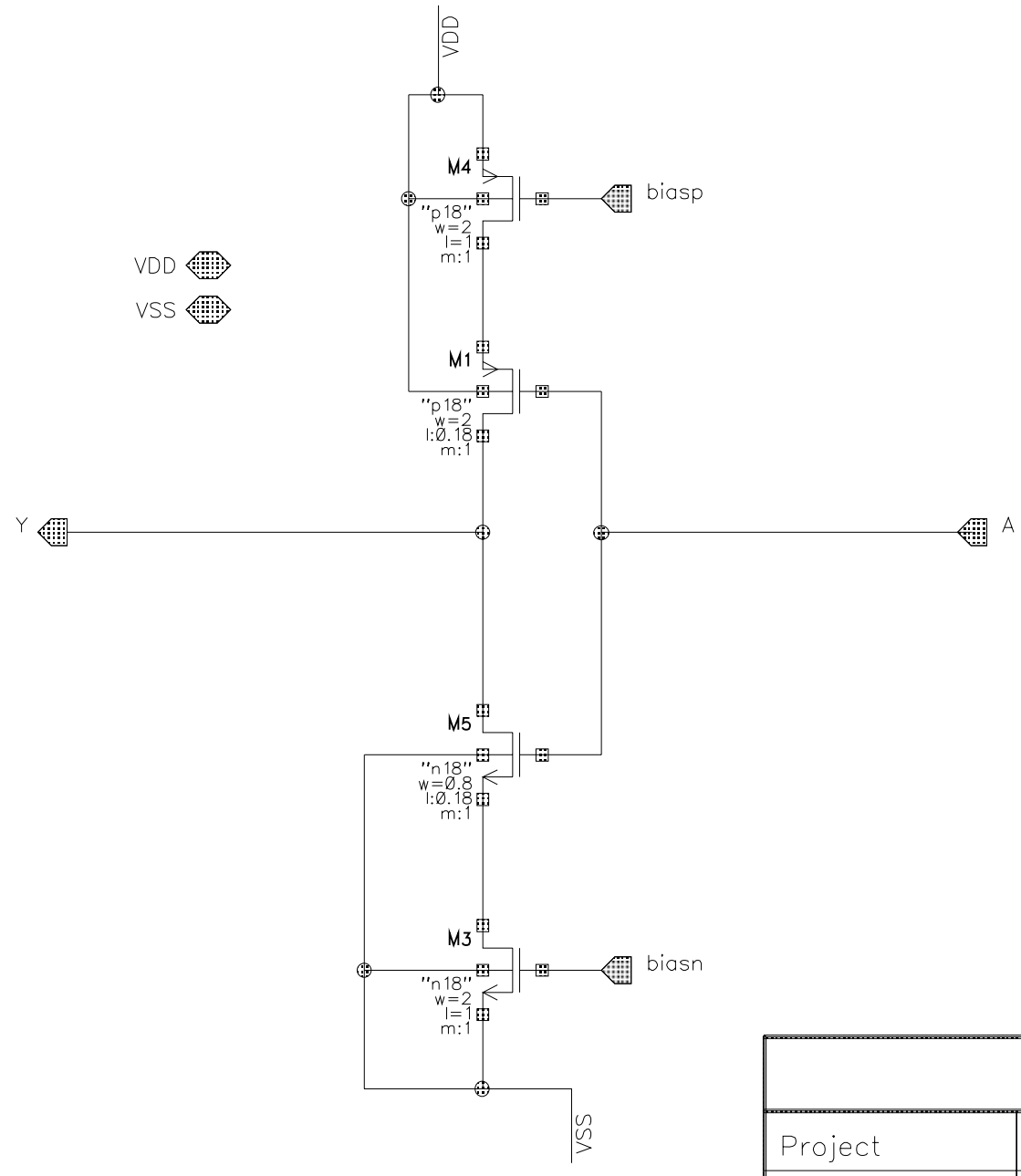
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	isense_iref_v1.2	
Last QA Review		
Last Changed	Sep 29 10:33:57 2006	



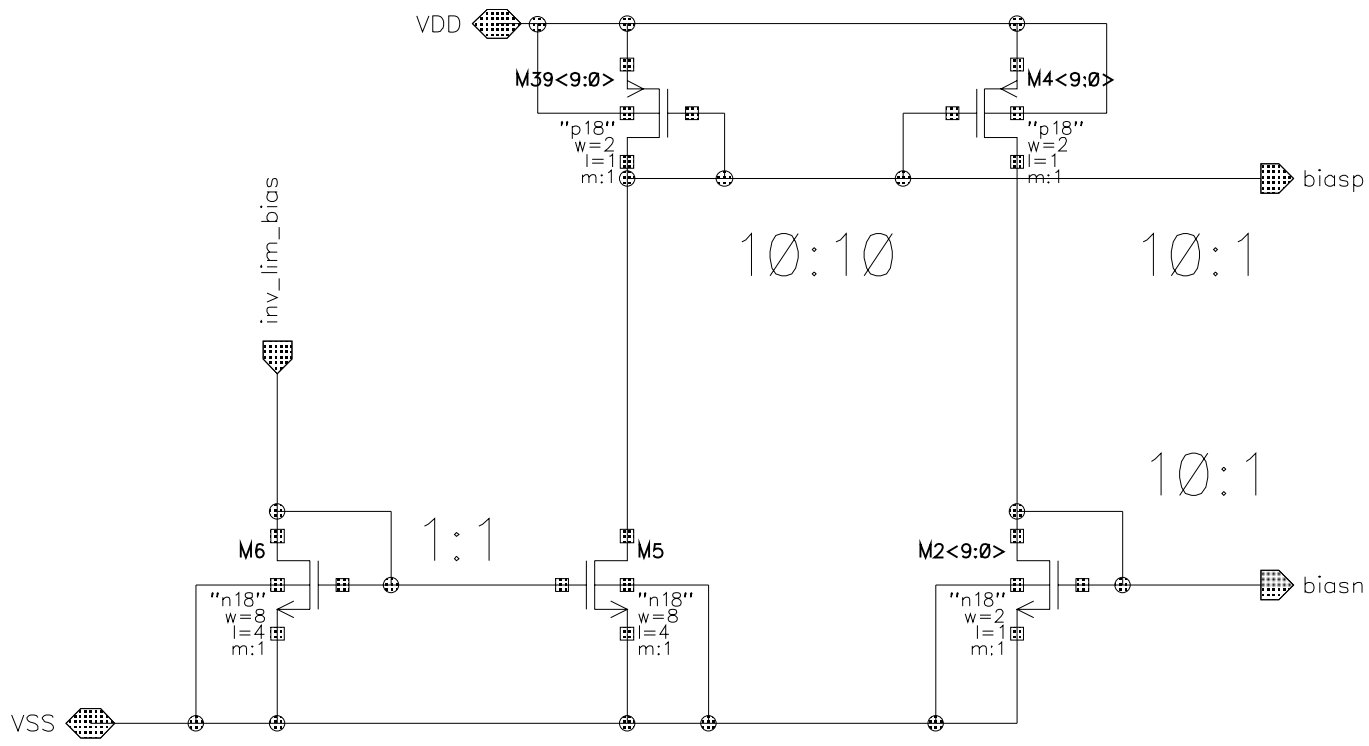
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	logic_inv_x0	
Last QA Review		
Last Changed	Sep 28 11:41:11 2006	



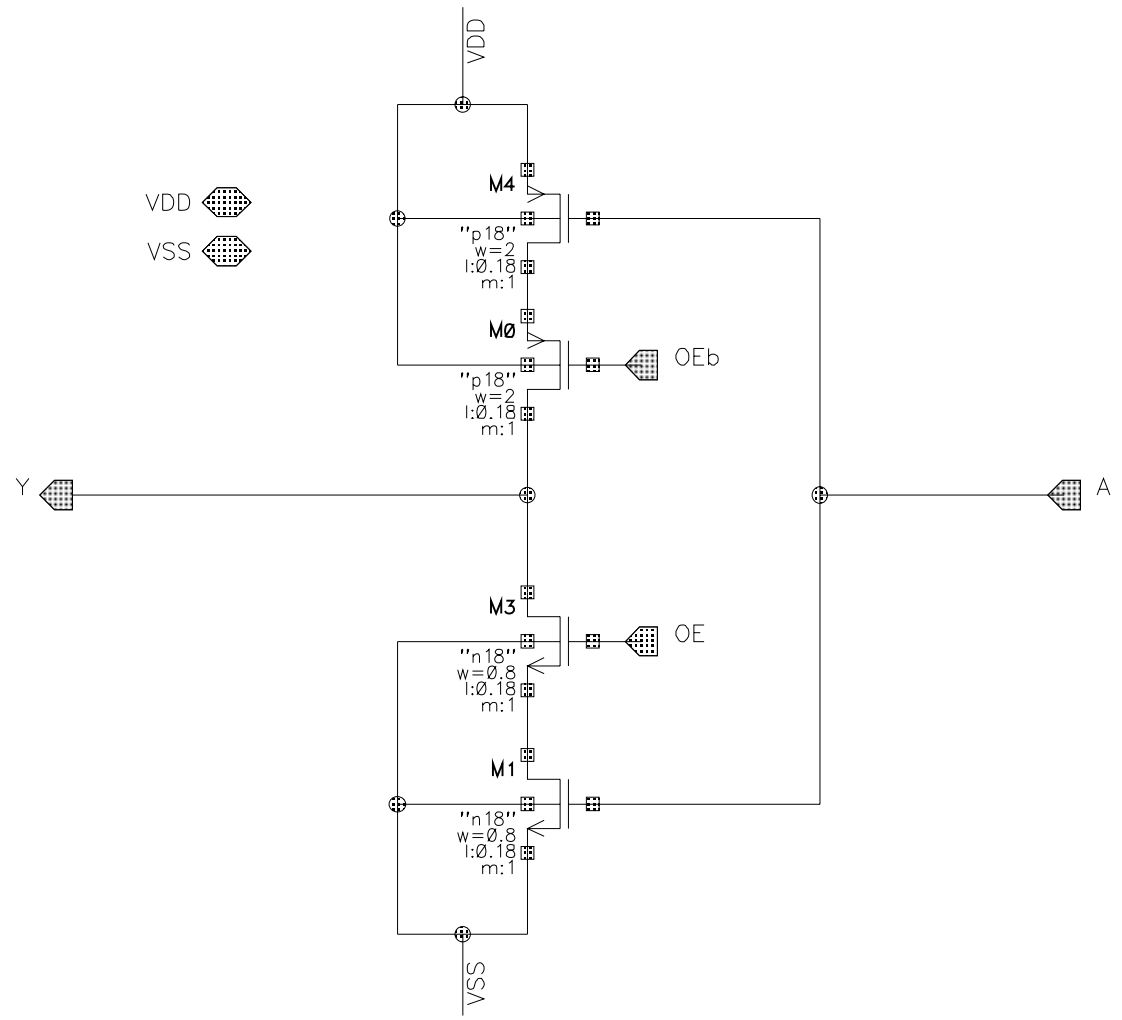
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	logic_inv_x1	
Last QA Review		
Last Changed	Sep 28 11:46:11 2006	



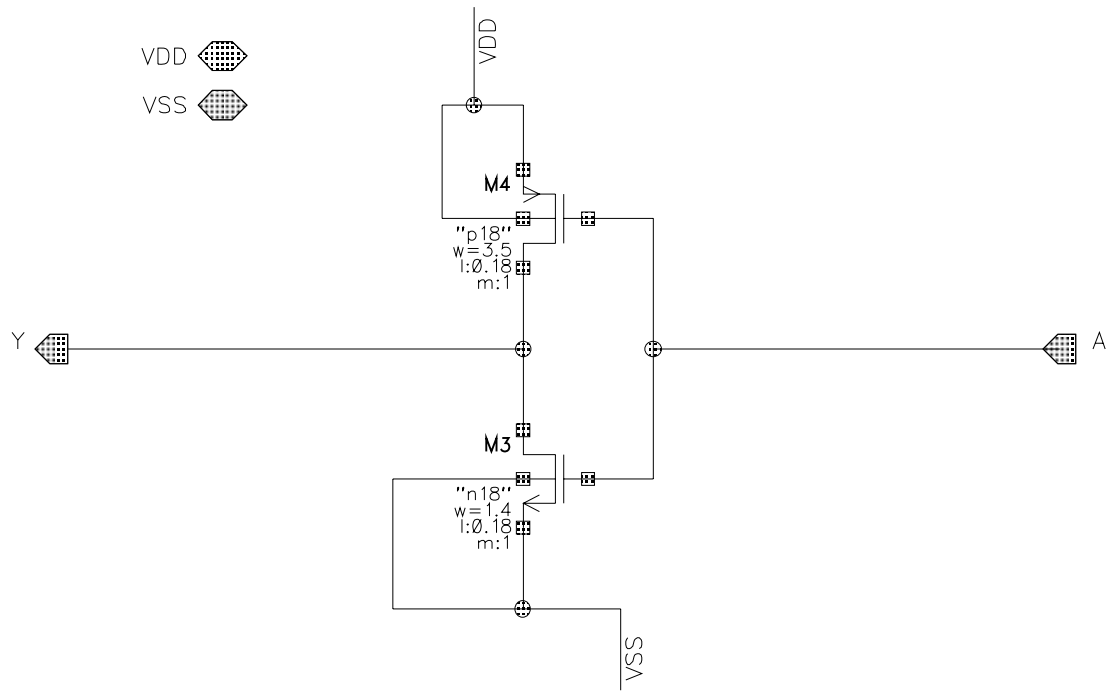
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_lim
Last QA Review	
Last Changed	Dec 8 11:32:40 2006



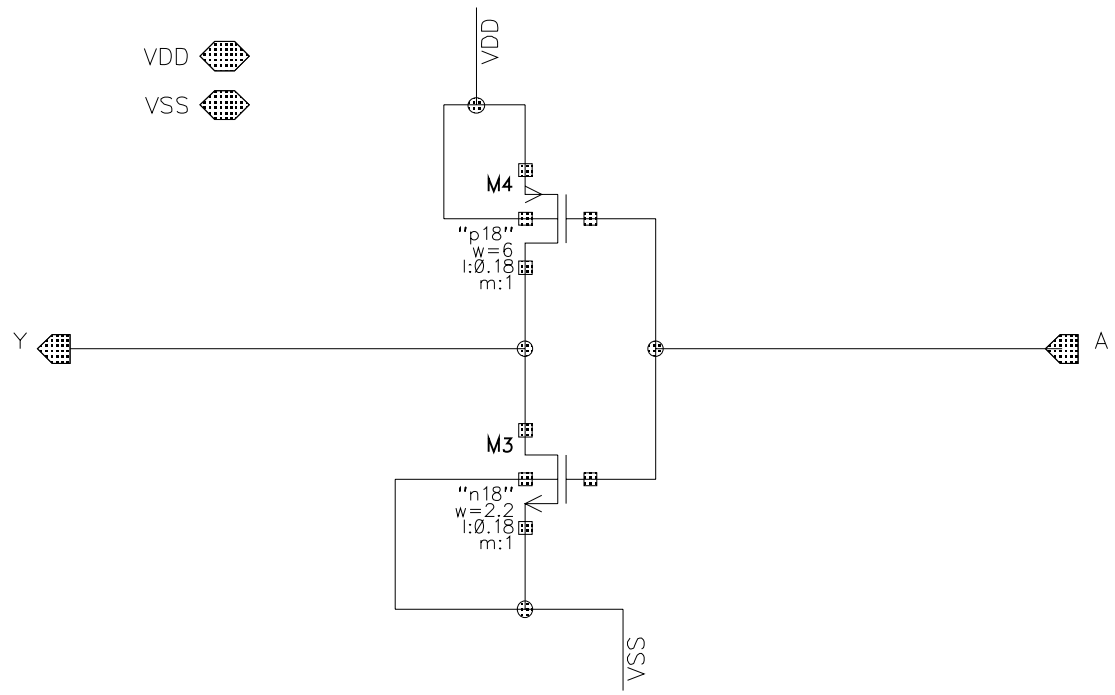
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_limbias
Last QA Review	
Last Changed	Dec 8 12:02:56 2006



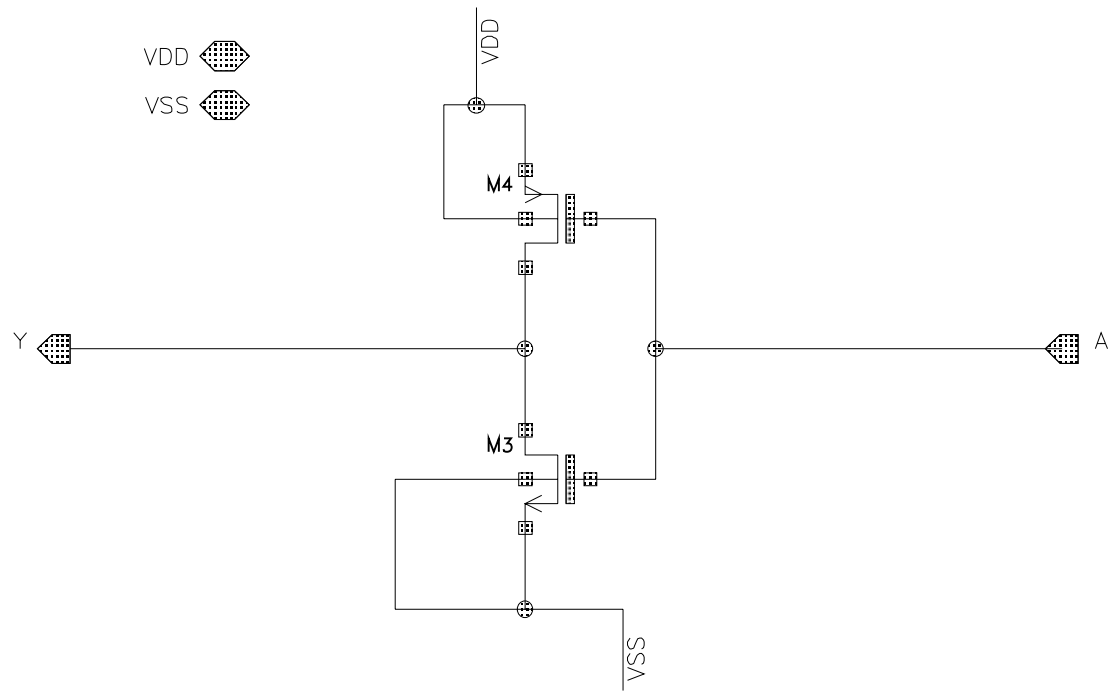
RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x1
Last QA Review	
Last Changed	Sep 28 11:42:37 2006



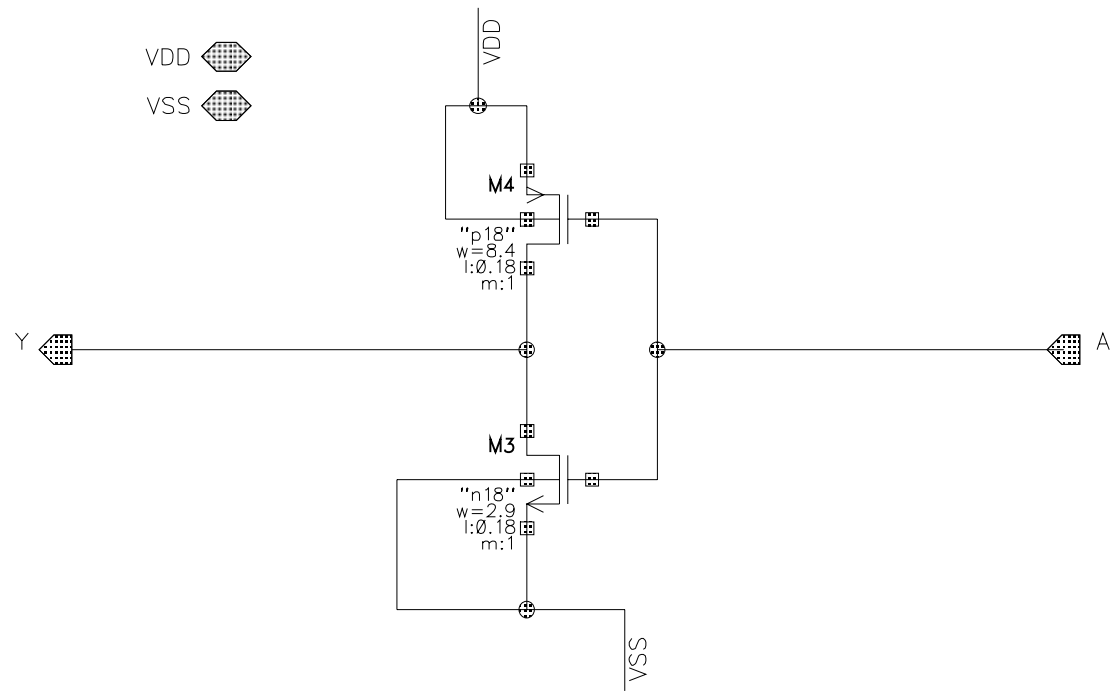
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2
Last QA Review	
Last Changed	Sep 28 11:45:54 2006



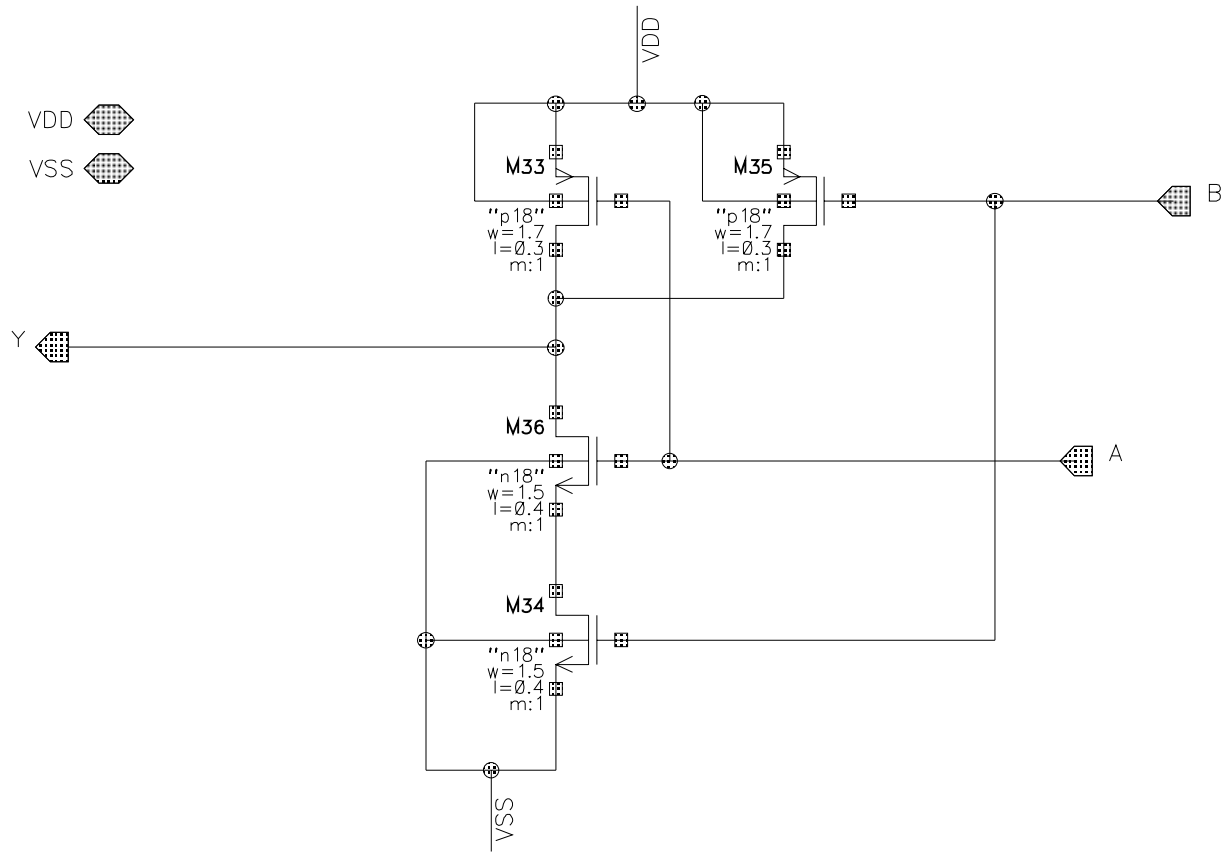
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	logic_inv_x3	
Last QA Review		
Last Changed	Sep 28 11:42:15 2006	



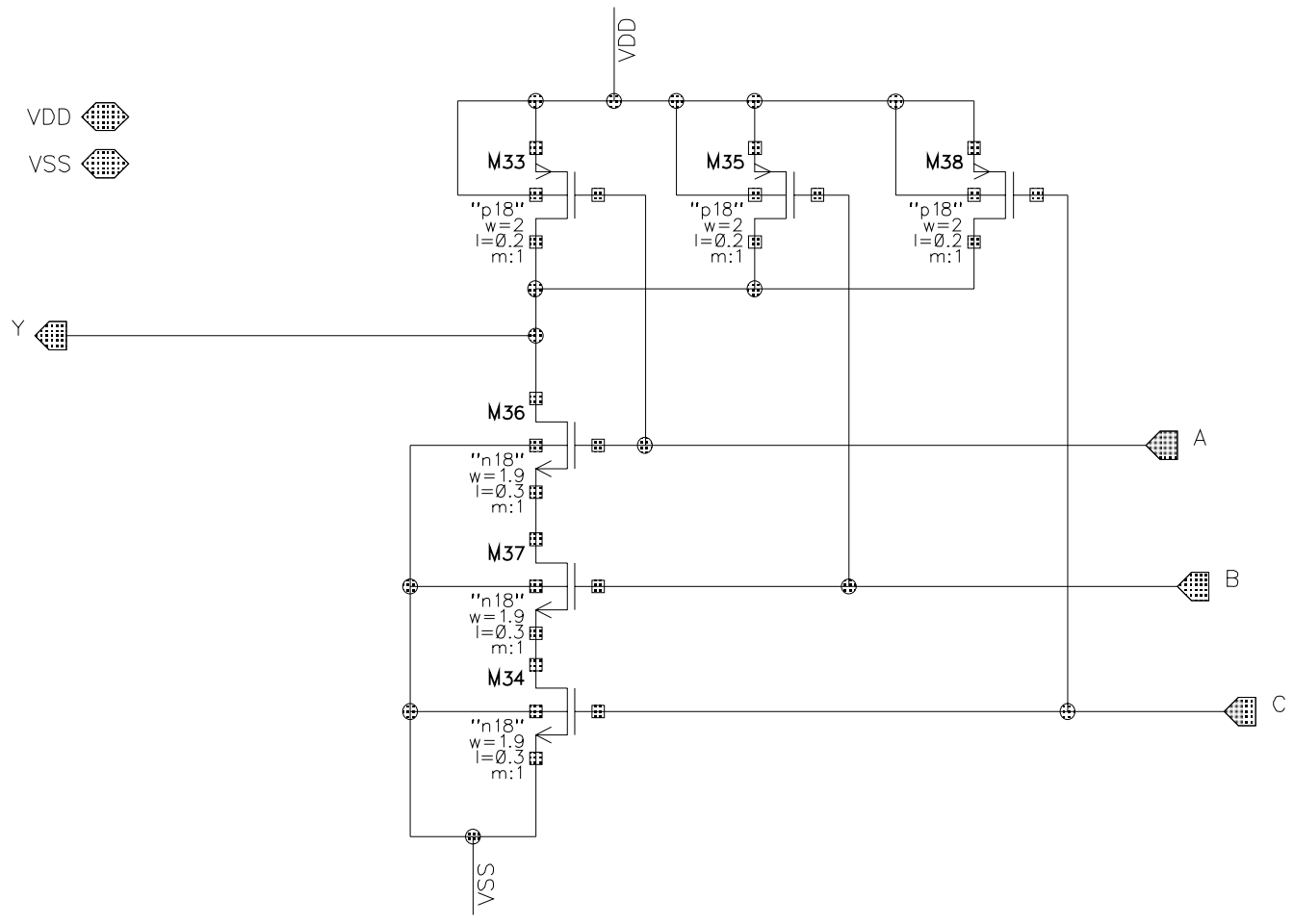
RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3_hv
Last QA Review	
Last Changed	Sep 29 15:18:48 2006



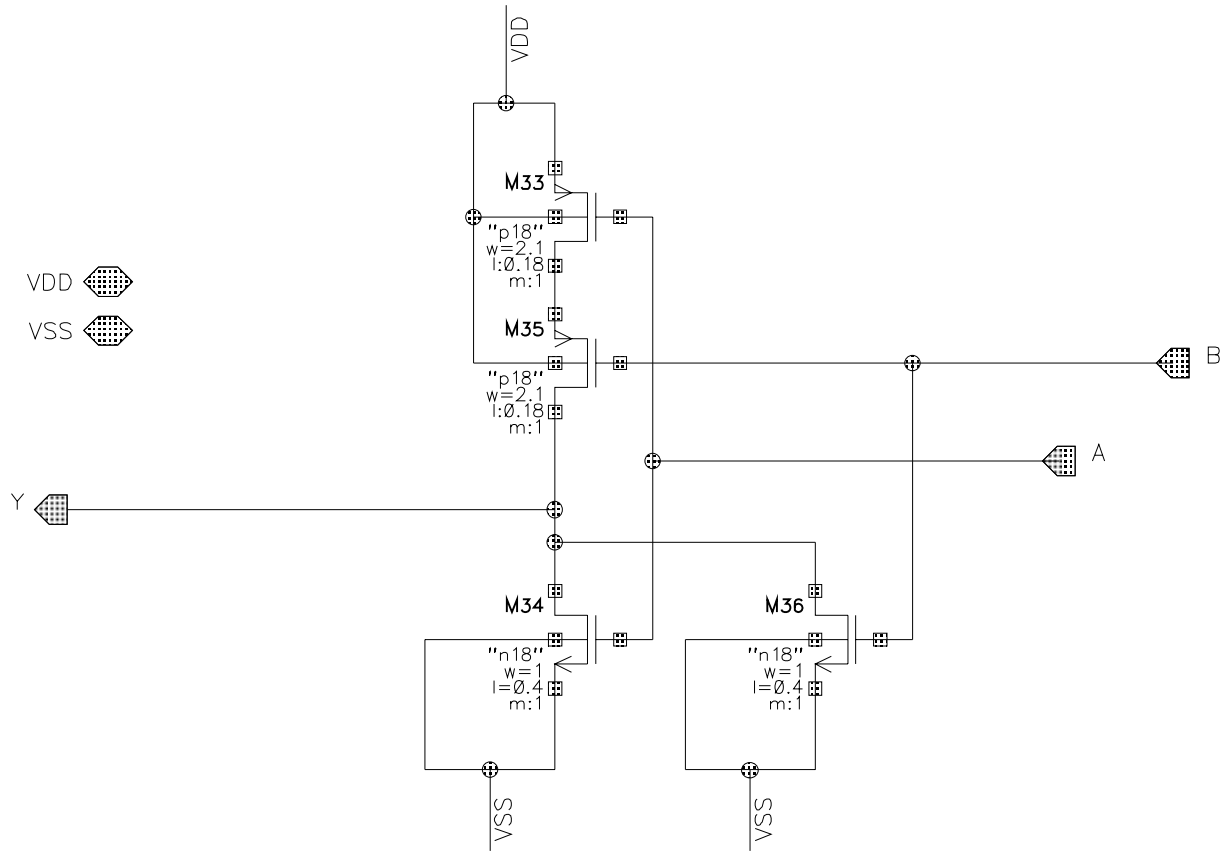
RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4
Last QA Review	
Last Changed	Sep 28 11:42:24 2006



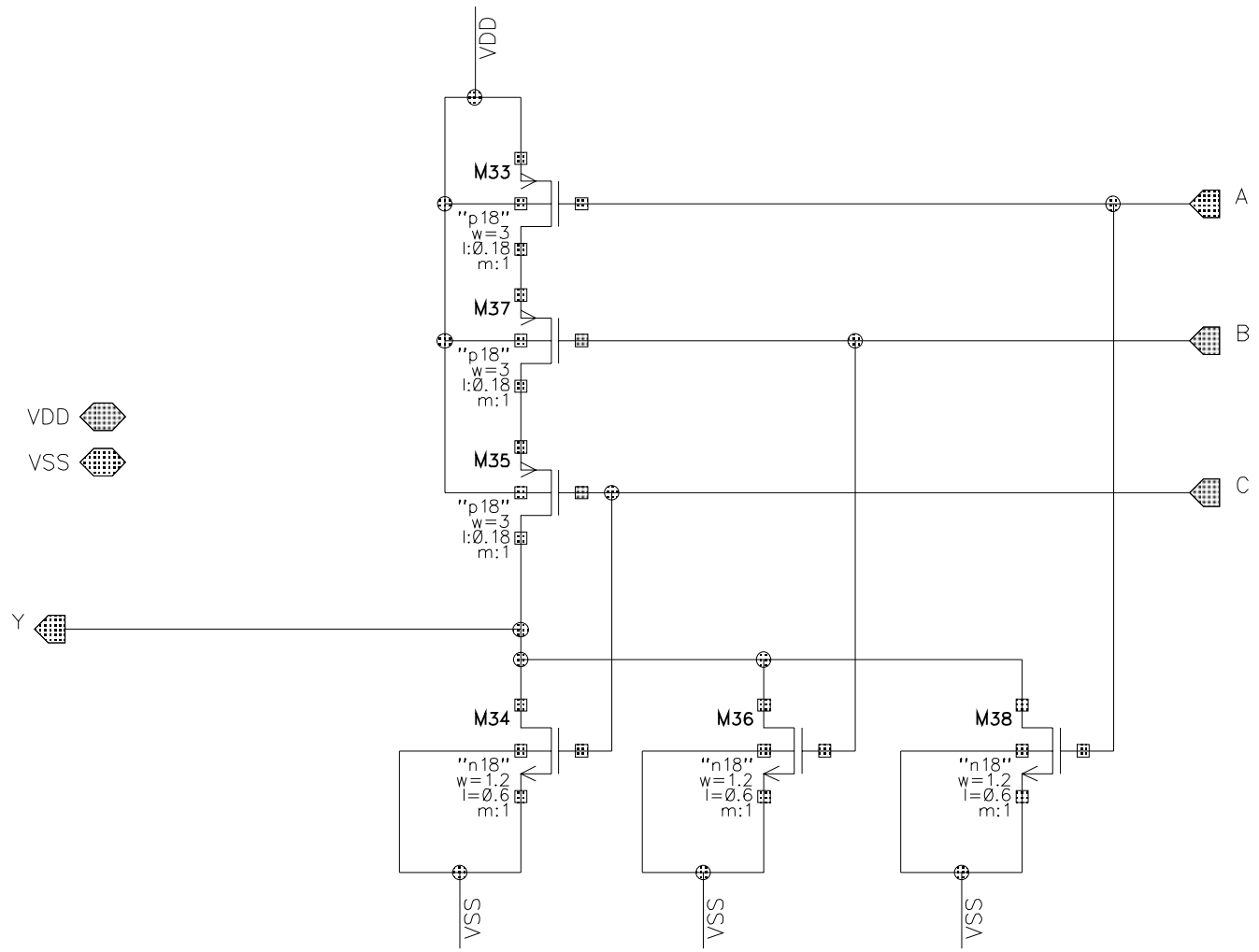
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	logic_nand2_x0	
Last QA Review		
Last Changed	Sep 28 11:41:02 2006	



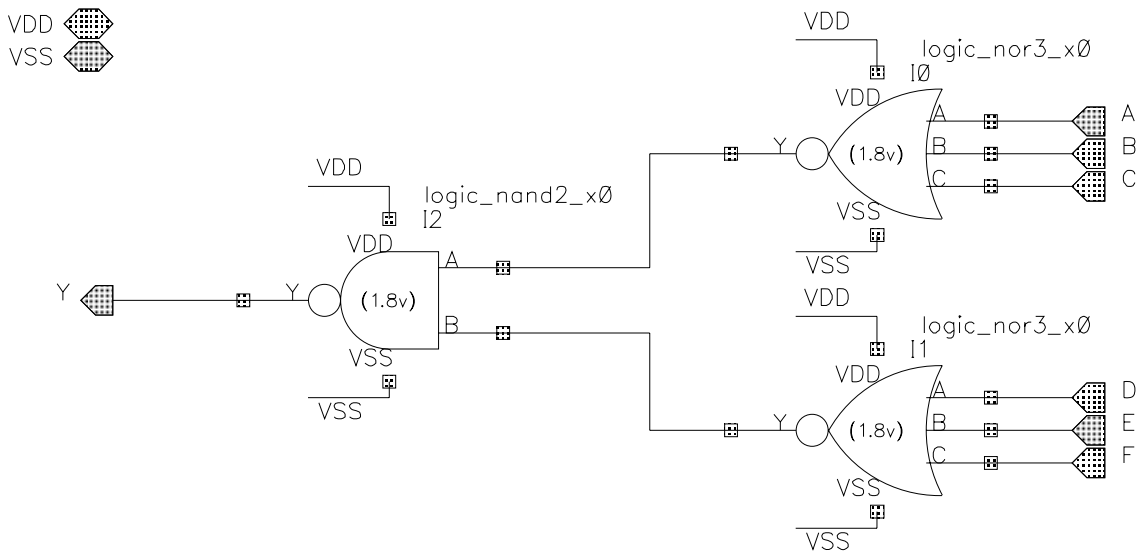
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	logic_nand3_x0	
Last QA Review		
Last Changed	Sep 28 11:42:56 2006	



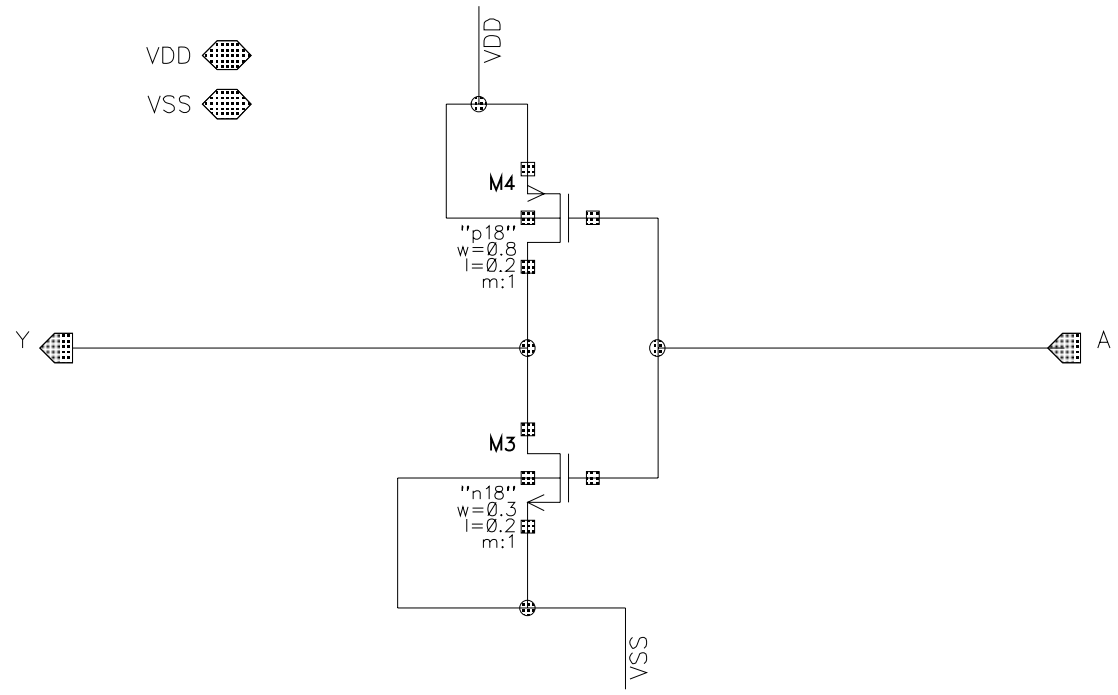
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor2_x0
Last QA Review	
Last Changed	Sep 28 11:45:21 2006



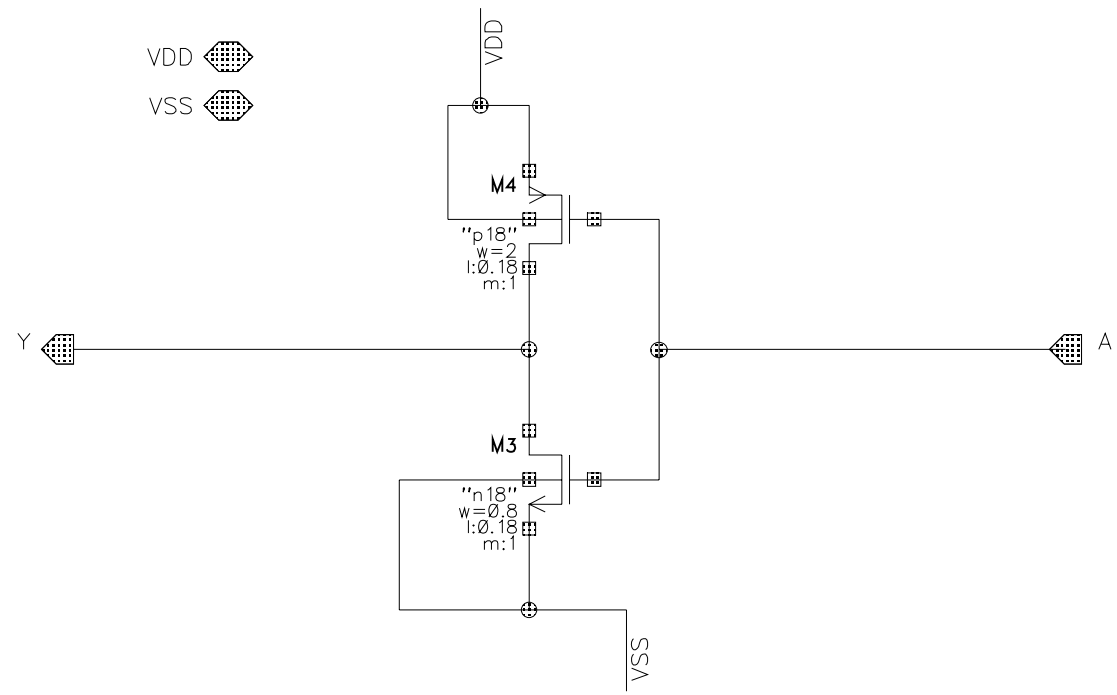
RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_xØ
Last QA Review	
Last Changed	Sep 28 11:41:39 2ØØ6



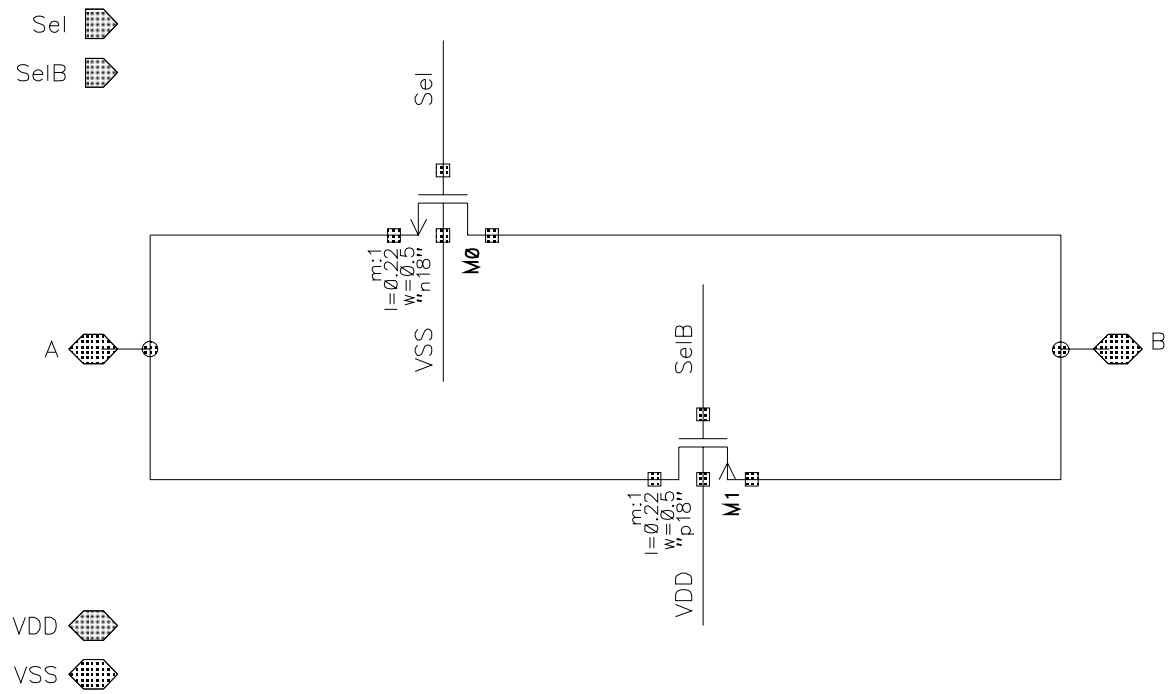
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_or6
Last QA Review	
Last Changed	Sep 28 11:43:44 2006



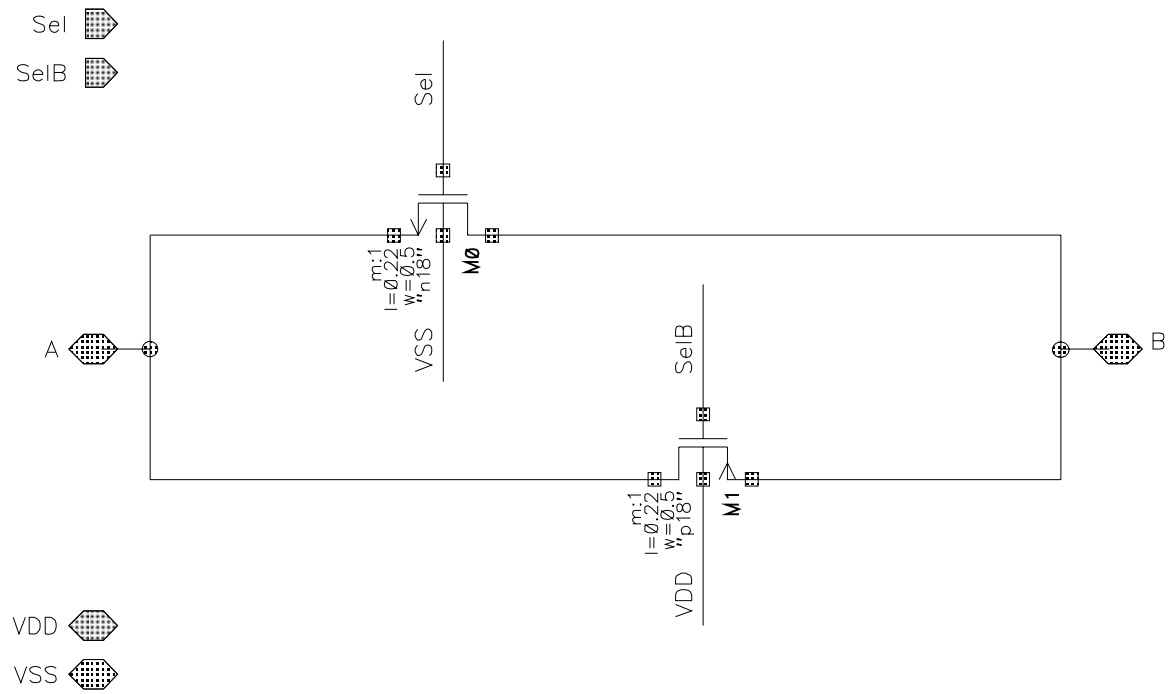
RAL Microelectronics Group		
Project	Tera–Pixel APS for CALICE	
Library Name	calice_feasability	
Block Name	logic_inv_x0	
Last QA Review		
Last Changed	Sep 28 11:41:11 2006	



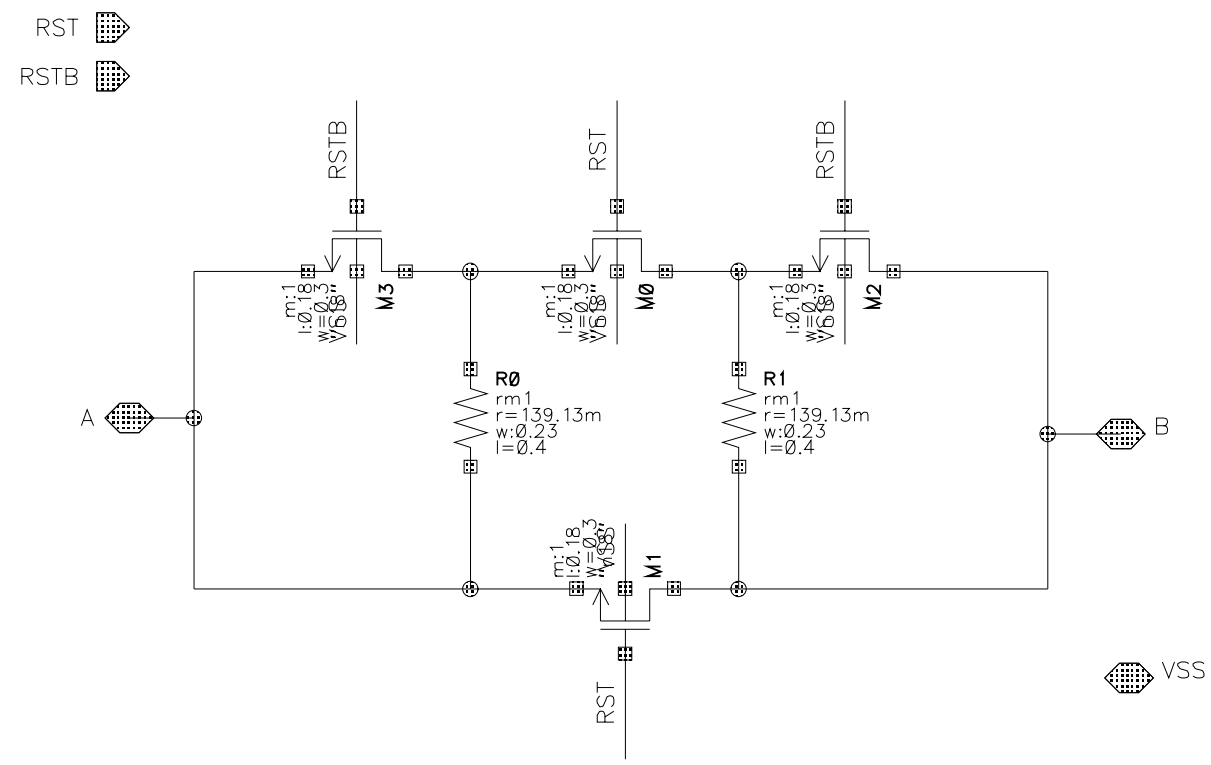
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_feasability	
Block Name	logic_inv_x1	
Last QA Review		
Last Changed	Sep 28 11:46:11 2006	



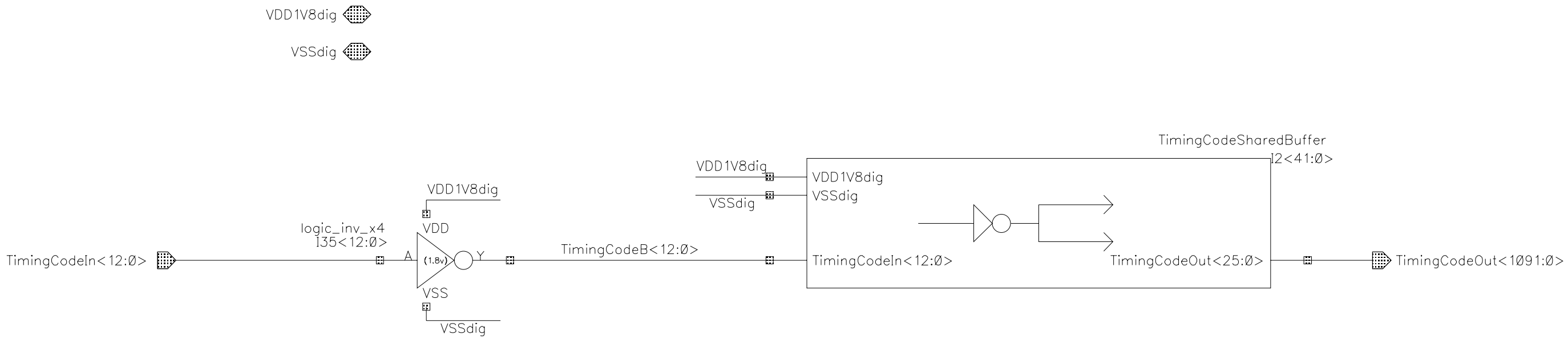
RAL Microelectronics Group		
Project	Tera–Pixel APS for CALICE	
Library Name	calice_feasability	
Block Name	sw1_18	
Last QA Review		
Last Changed	Sep 28 11:41:21 2006	



RAL Microelectronics Group		
Project	Tera–Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	sw1_18	
Last QA Review		
Last Changed	Sep 28 11:41:21 2006	



RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	caliceRT	
Block Name	sw1_NOINJ_18	
Last QA Review		
Last Changed	Oct 13 10:05:15 2006	



x4 buffers drive the full column length (84 pix)

Timing Code in the column is in inverted format

Every second pixel row (every 100um) a local buffer drives 2 rows both left and right (ie 4 SRAM banks)

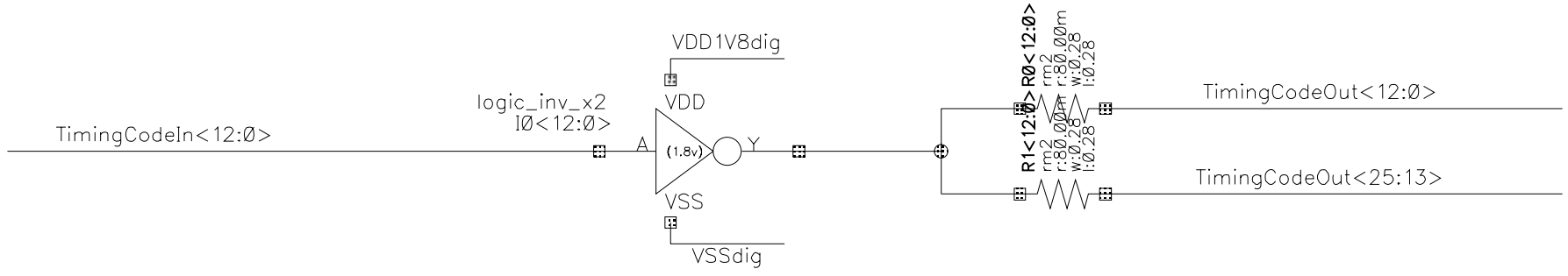
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	TimingCodeDistribution	
Last QA Review		
Last Changed	Dec 12 11:16:13 2006	

VDD1V8dig

VSSdig

TimingCodeIn<12:0>

TimingCodeOut<25:0>



RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	TimingCodeSharedBuffer	
Last QA Review		
Last Changed	Dec 12 11:07:32 2006	