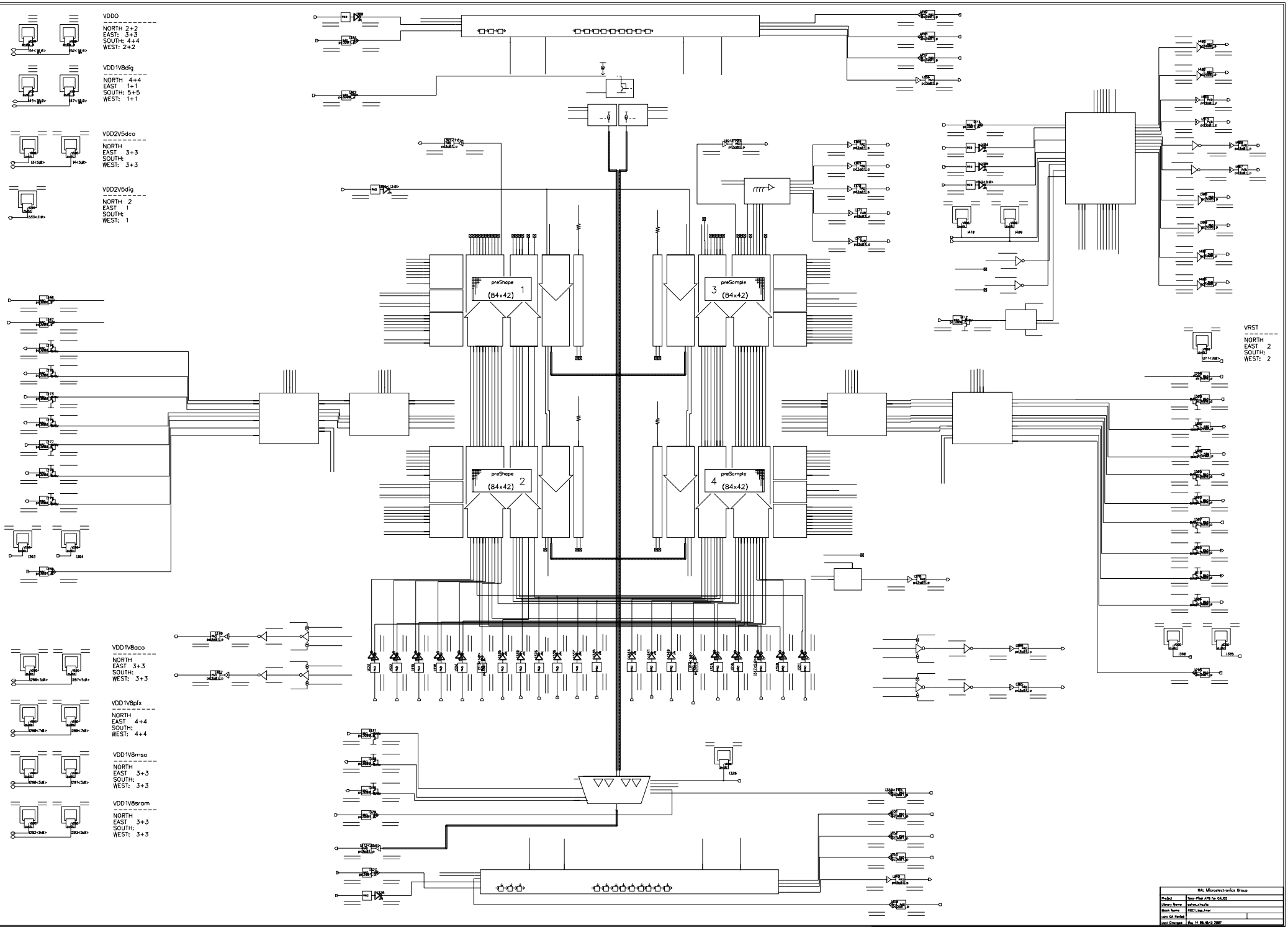
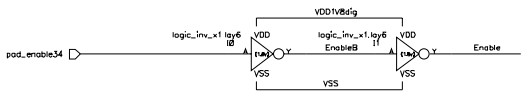
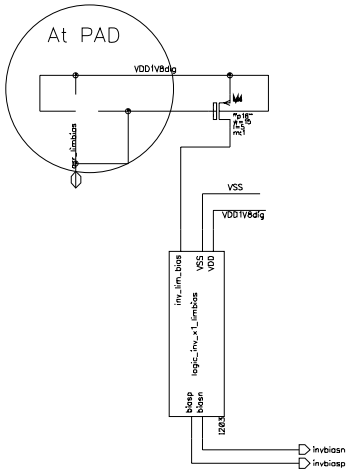
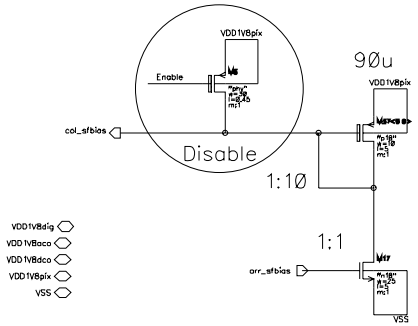

VDDO
NORTH 2+2
EAST: 3+3
SOUTH: 4+4
WEST: 2+2
VDD1V8dig
NORTH 4+4
EAST 1+1
SOUTH: 5+5
WEST: 1+1
VDD2V5dco
NORTH
EAST 3+3
SOUTH:
WEST: 3+3
VDD2V5dig
NORTH 2
EAST 1
SOUTH:
WEST: 1
preShape 1 (84x42)
preSample 3 (84x42)
preShape 2 (84x42)
preSample 4 (84x42)
VRST
NORTH
EAST 2
SOUTH:
WEST: 2
VDD1V8dco
NORTH
EAST 3+3
SOUTH:
WEST: 3+3
VDD1V8pix
NORTH
EAST 4+4
SOUTH:
WEST: 4+4
VDD1V8mso
NORTH
EAST 3+3
SOUTH:
WEST: 3+3
VDD1V8sram
NORTH
EAST 3+3
SOUTH:
WEST: 3+3
RAL Microelectronics Group
Project
Library Name
Block Name
Last Changed

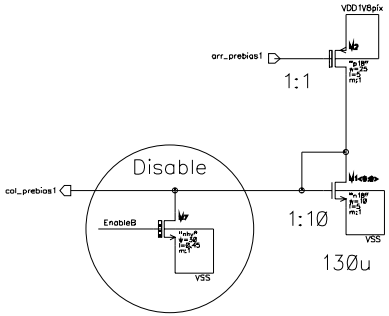




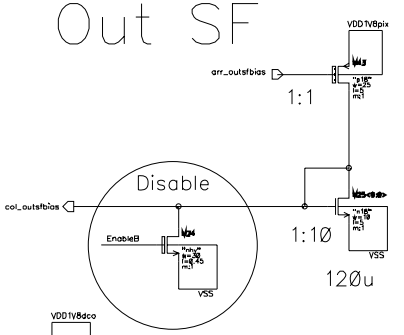
Pixel SF



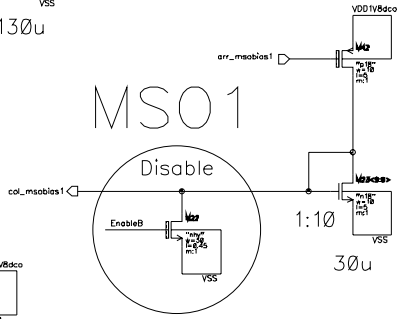
Preamp Bias



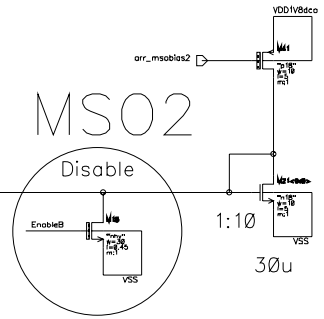
Out SF



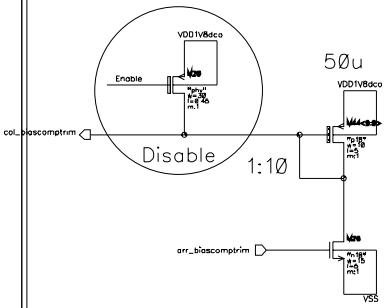
MSO1

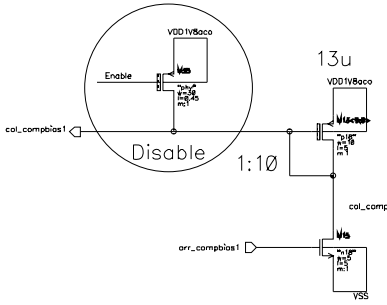


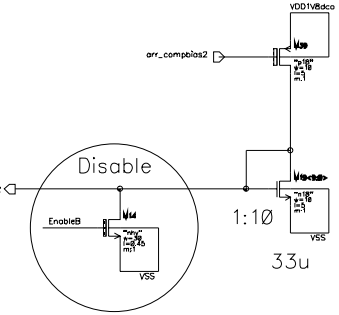
MSO2



Comparator



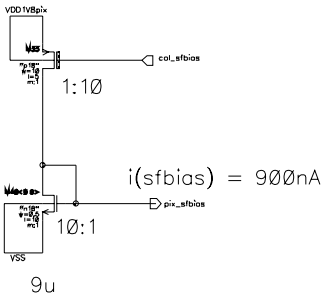




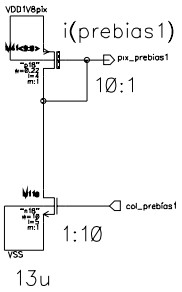
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presample_bias_arr_v1.3
Last QA Review	
Last Changed	Apr 30 09:07:20 2007

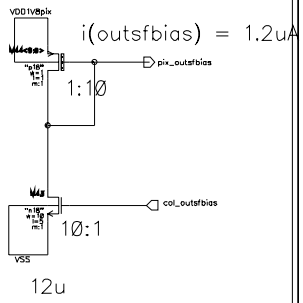
Pixel SF



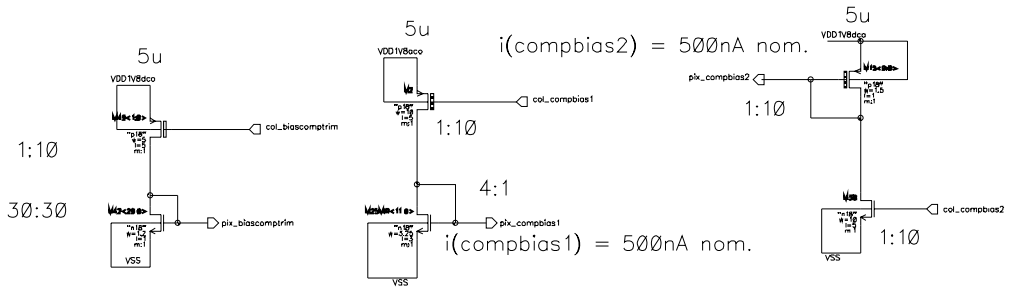
Preamp Bias



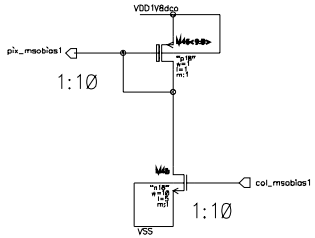
Out SF



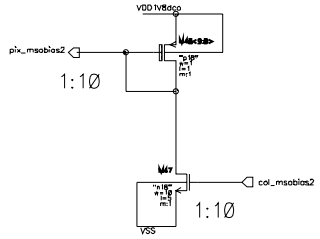
Comparator Bias



MS01 3u

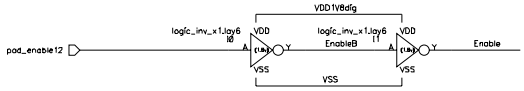


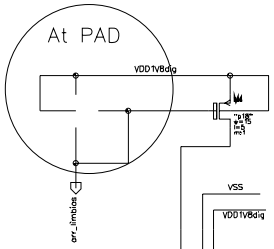
MS02 3u

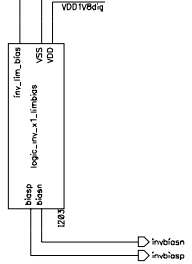


COLUMN CIRCUITS

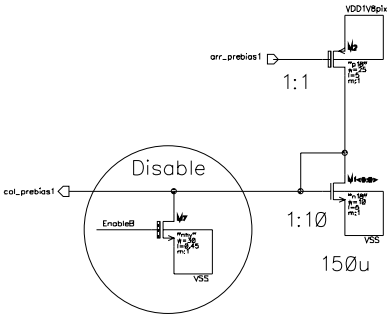
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	pixbias_prsmpIRT_col_v1.2
Last QA Review	
Last Changed	Mar 8 14:21:08 2007



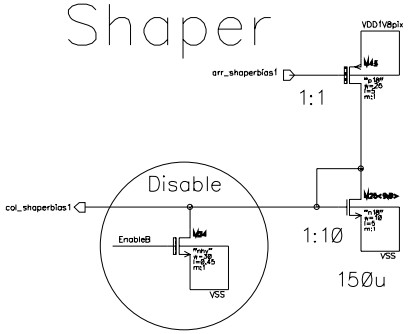




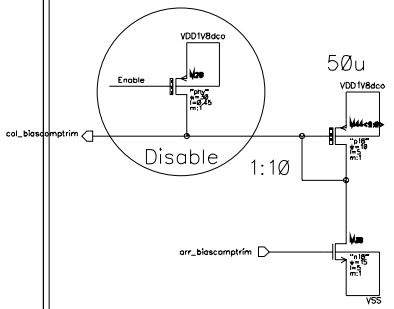
Preamp Bias

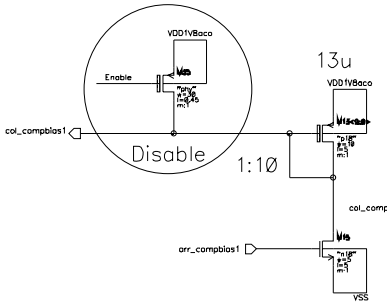


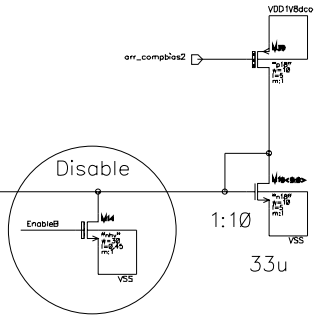
Shaper



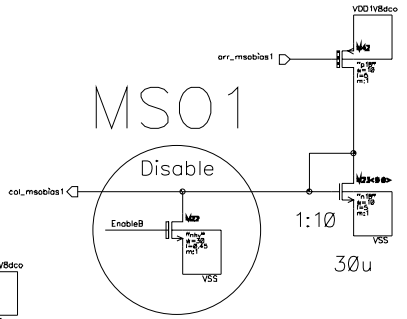
Comparator







MSO1

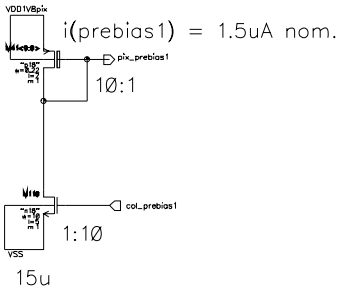


ARRAY CIRCUITS

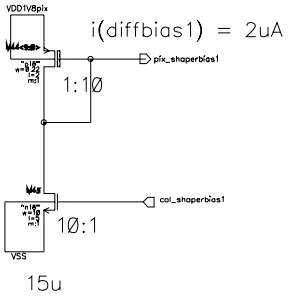
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_preshape_bias_arr_v1.3
Last QA Review	
Last Changed	Mar 26 16:12:09 2007

VDD1V8aco
VDD1V8dco
VDD1V8mso
VDD1V8pix
VSS

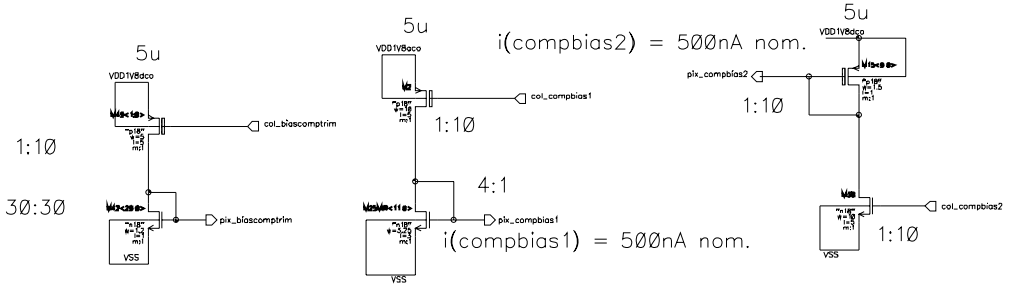
Preamp Bias



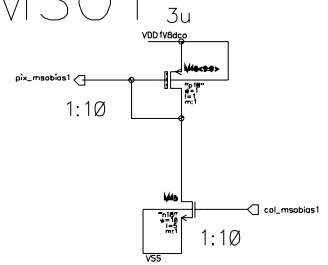
Shaper



Comparator Bias



MSO1



COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	pixbias_prshp_col
Last QA Review	
Last Changed	Mar 22 18:15:00 2007

Pre-Shape Pixel Half-Array 84rows x 42cols

Pre-Sample Pixel Half-Array 84rows x 42cols

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array2_preshape_TBTBBTTB
Last OA Review	
Last Changed	Apr 17 13:20:44 2007

Pre-Sample Pixel Half-Array 84rows x 42cols

Spare inverter in layout, tied off to gnd

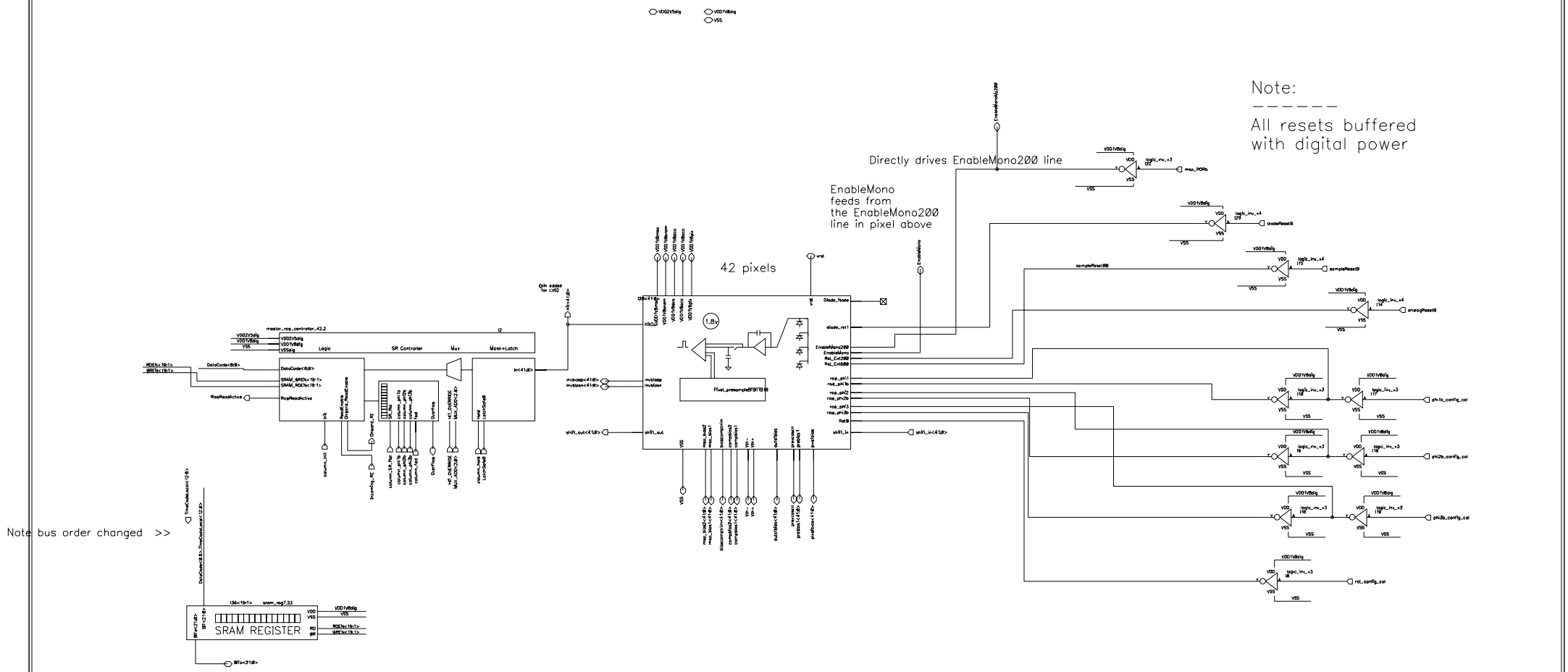
Un-Buffered Global Voltage signals: Static during operation

ARRAY_VTH+
ARRAY_VTH-
ARRAY_PREAMP_VCASCN
ARRAY_VRST

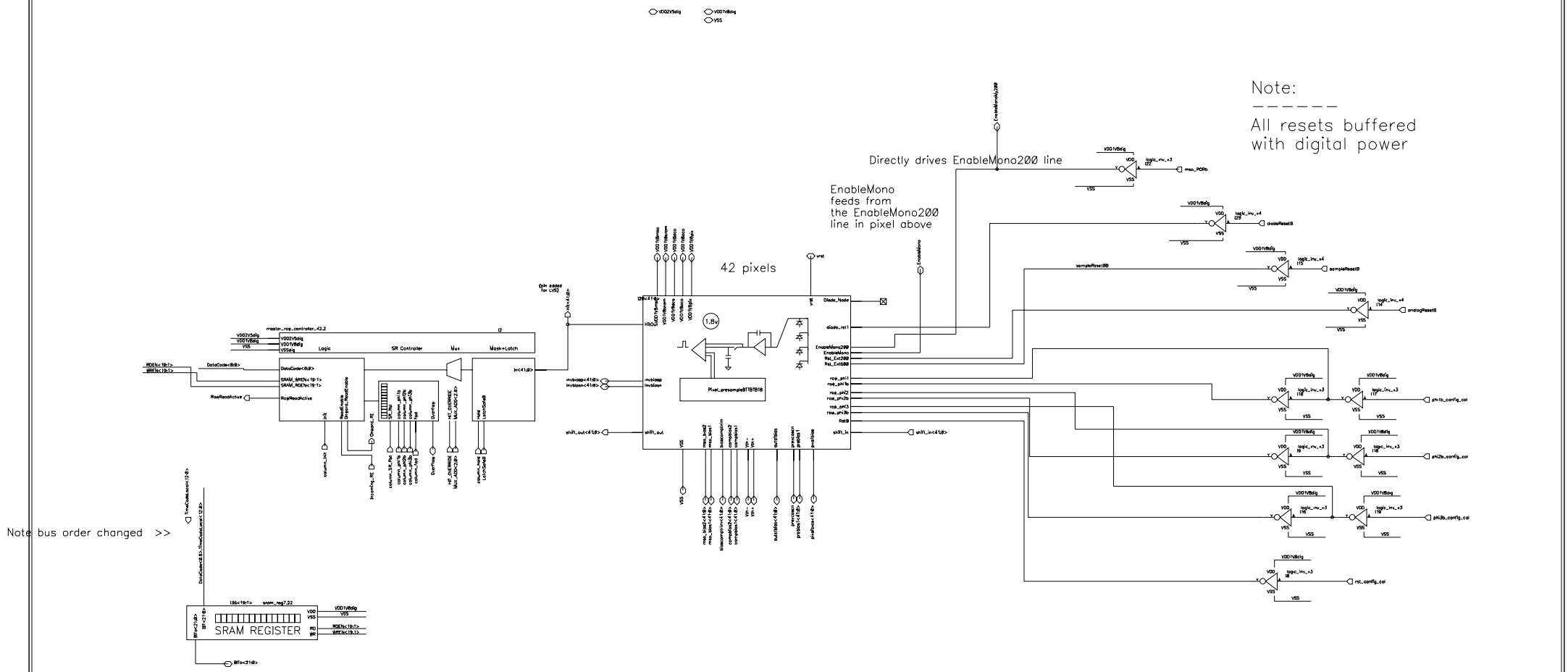
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array3_presample_BTBTTB
Last OA Review	
Last Changed	Apr 17 10:14:43 2007

Pre-Sample Pixel Half-Array 84rows x 42cols

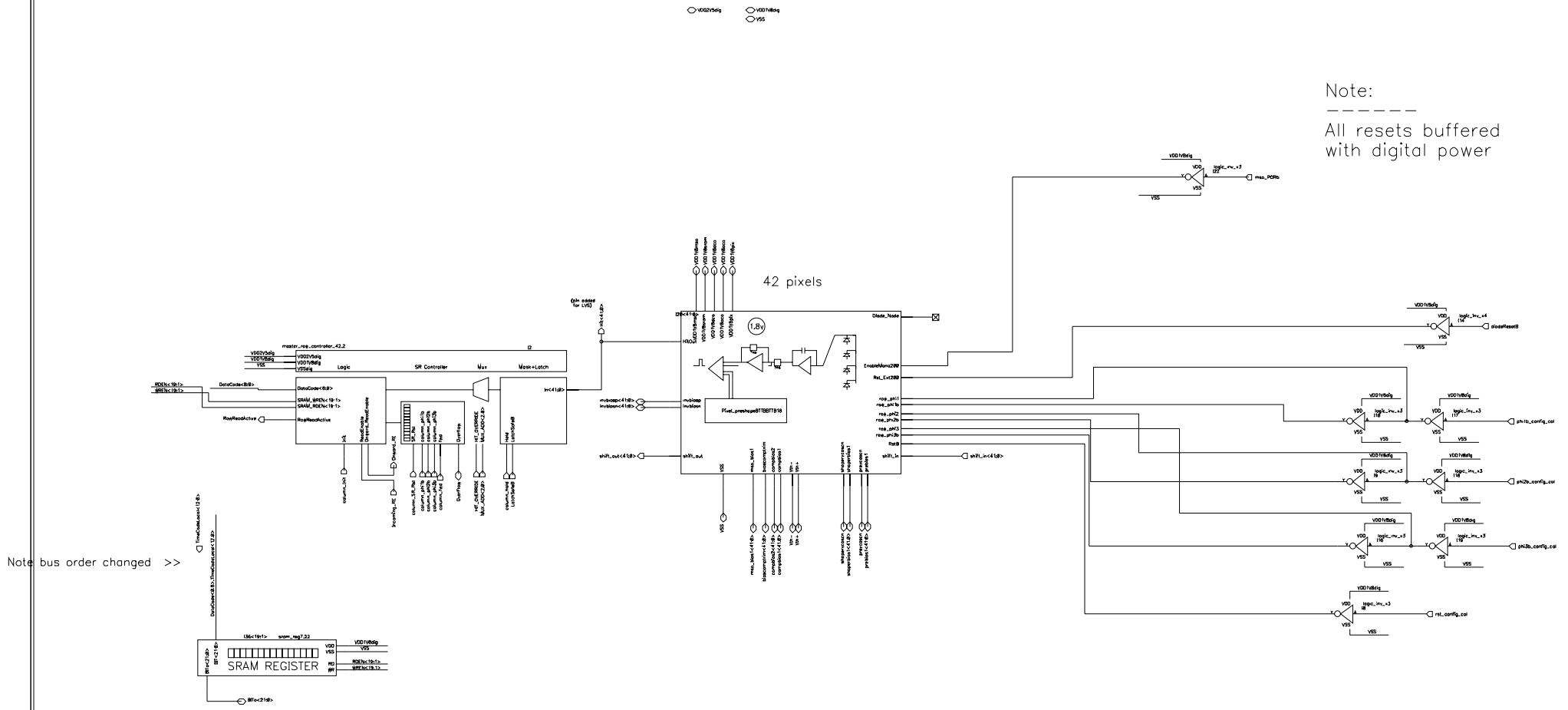
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_array4_presample_BTTBTB
Last OA Review	
Last Changed	Apr 17 13:19:19 2007

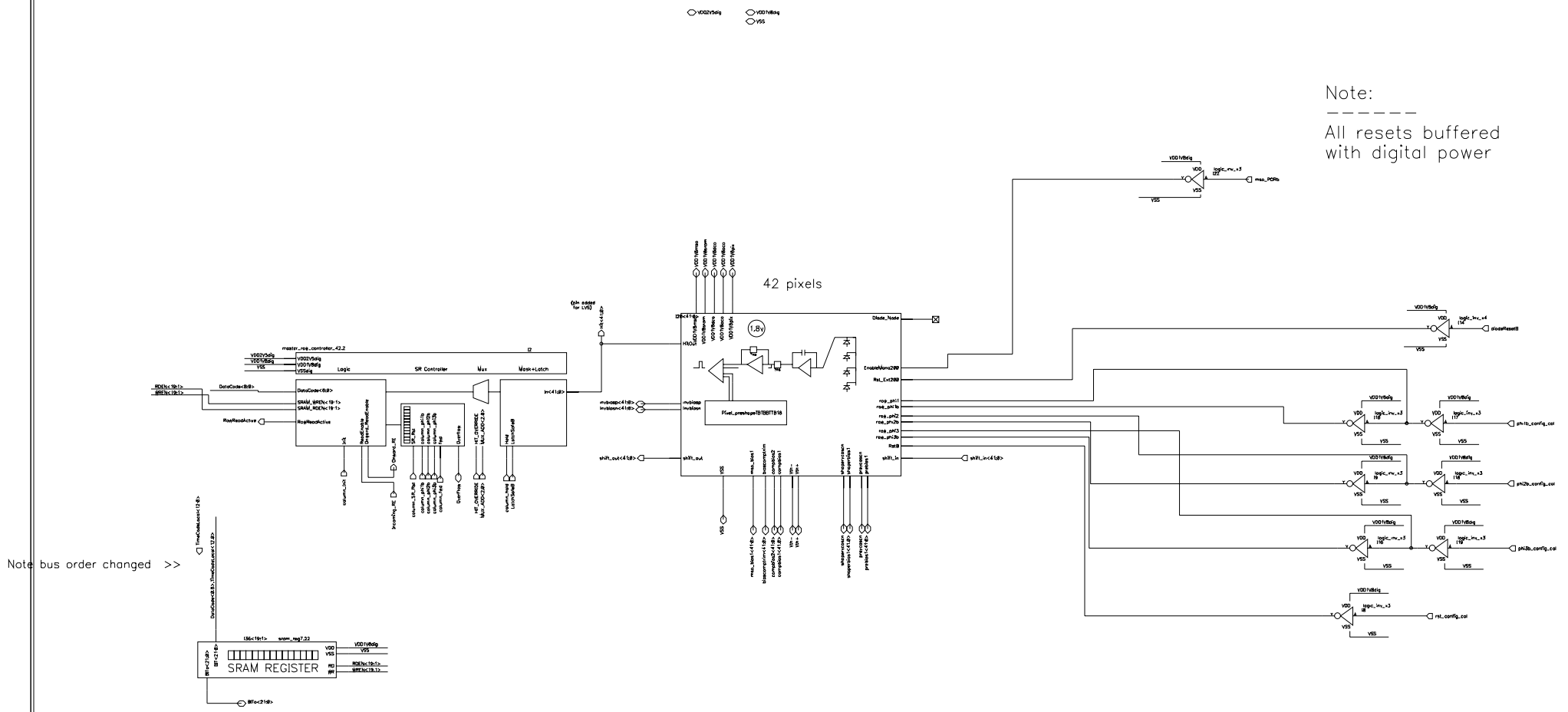


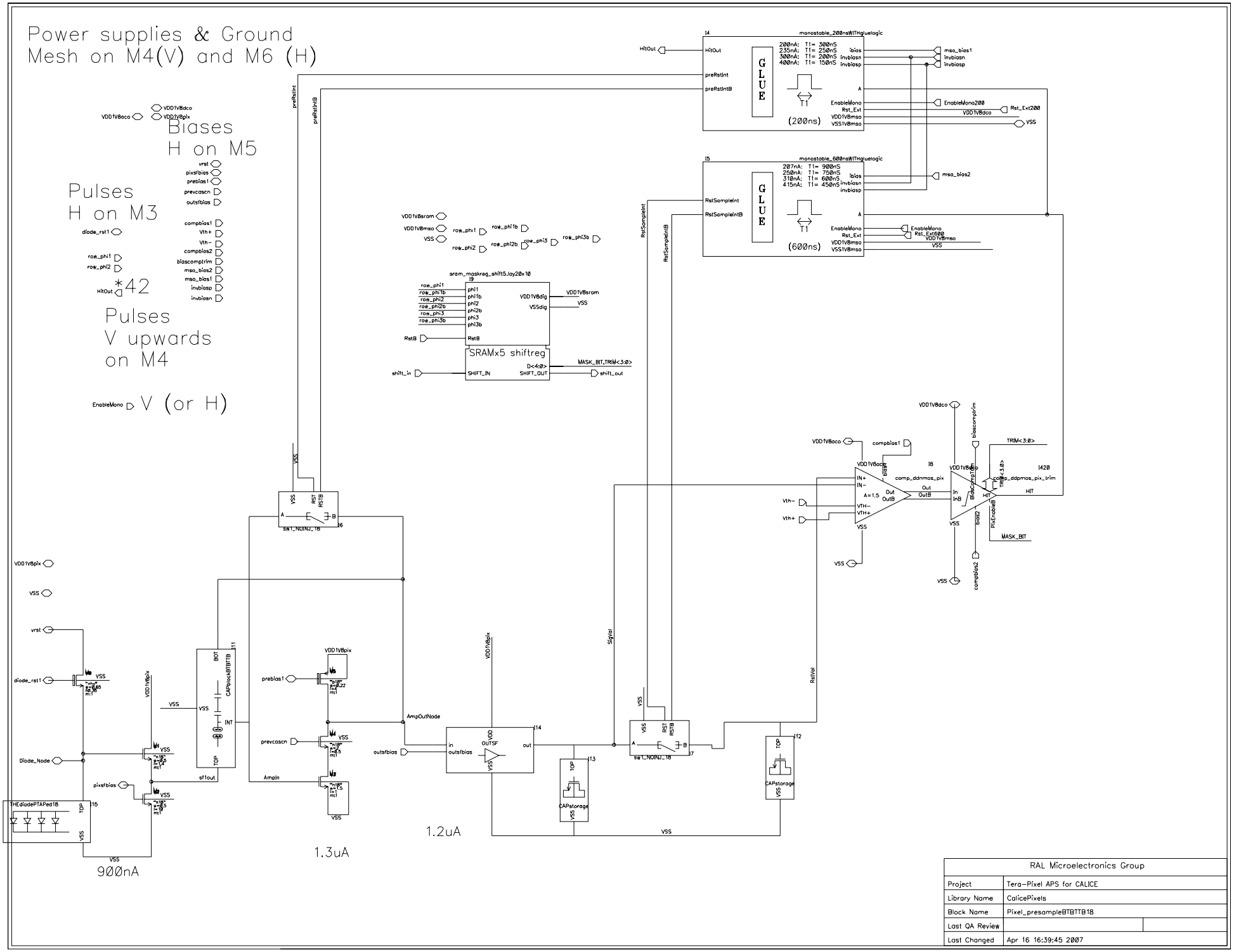
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_slice_presample_BTBTTB
Last QA Review	
Last Changed	Apr 17 09:29:37 2007



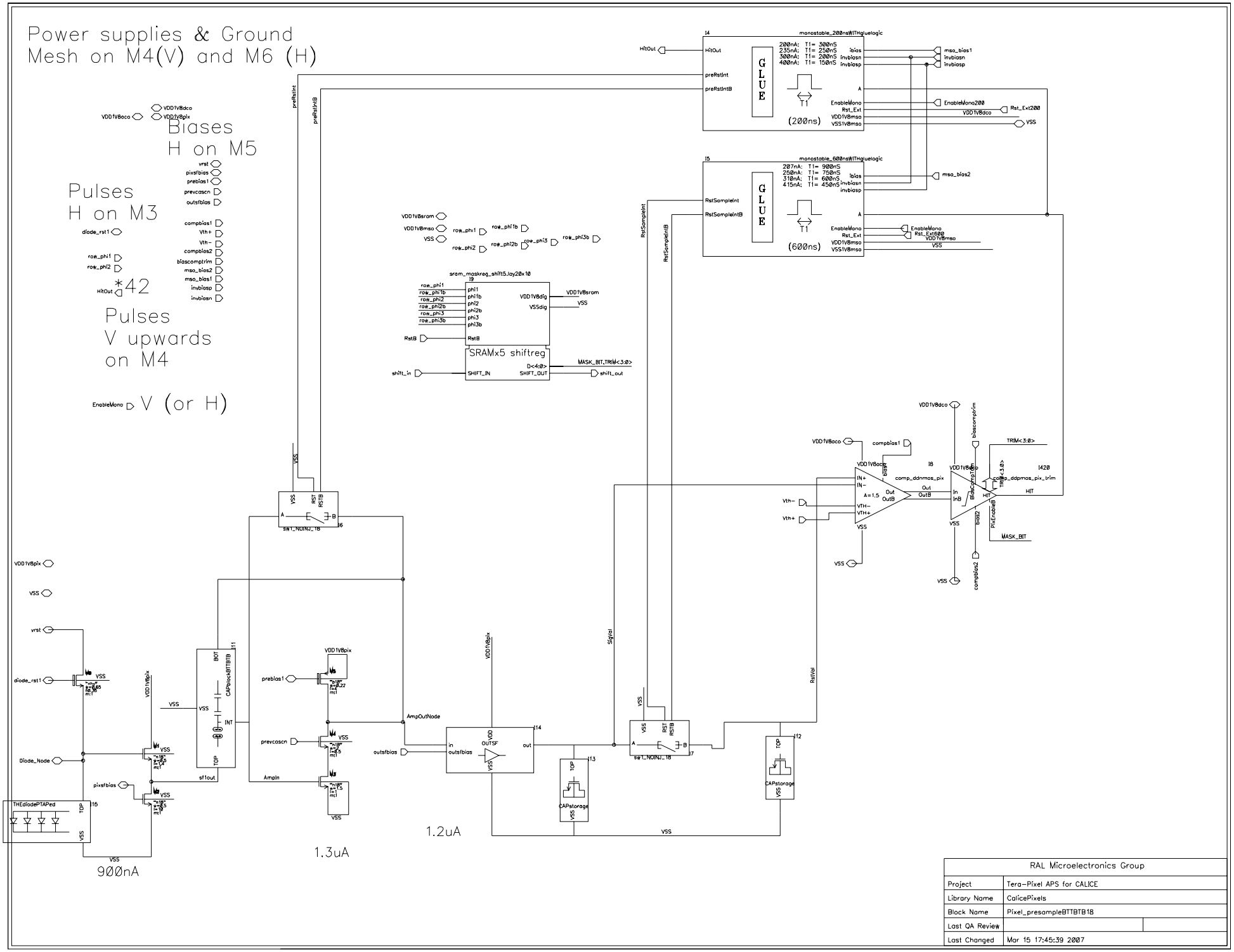
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_slice_presample_BTTBTB
Last QA Review	
Last Changed	Apr 17 09:35:24 2007

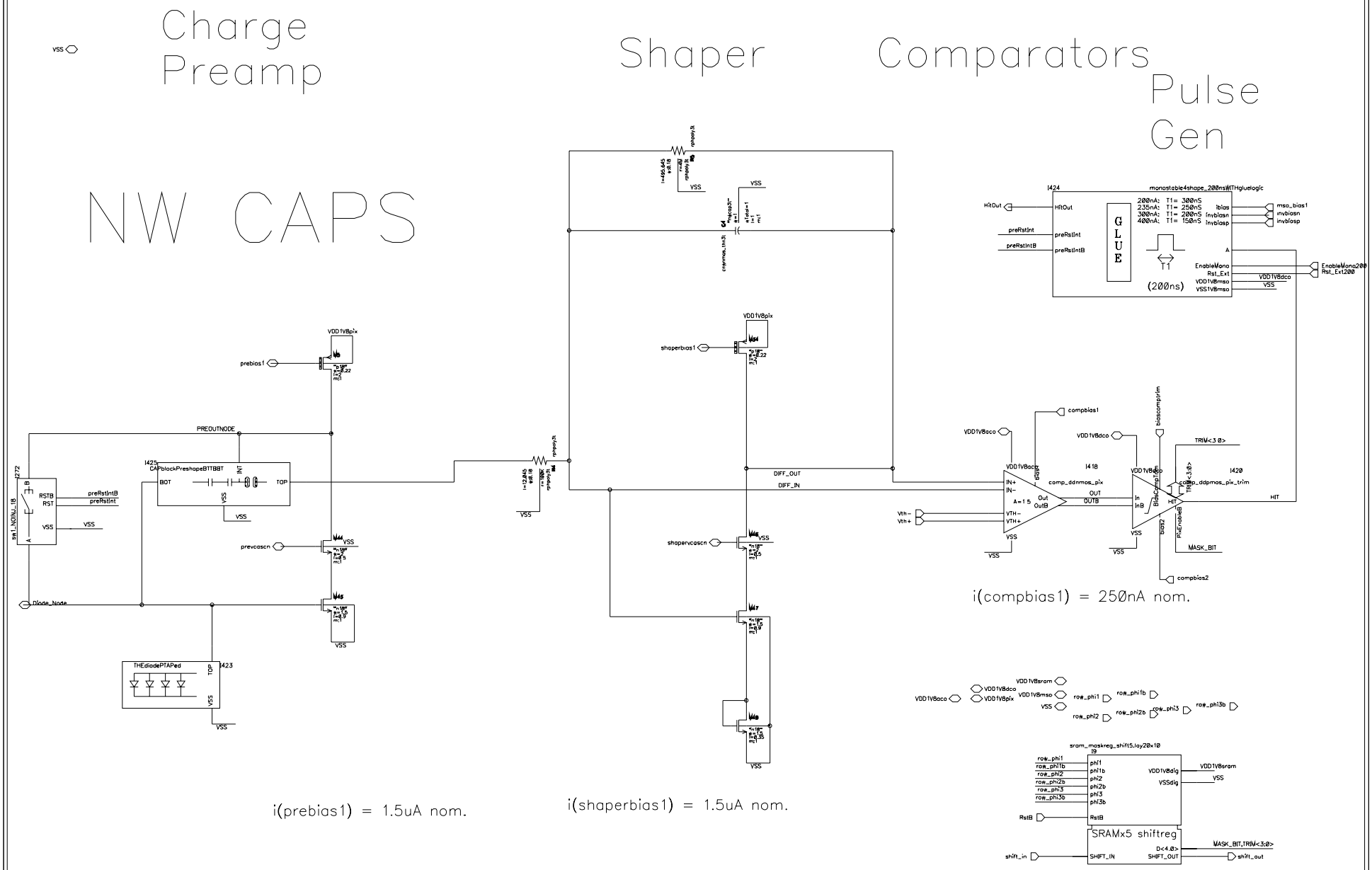

Note:
All resets buffered
with digital power
42 pixels
Note bus order changed >>
SRAM REGISTER
Logic
SR Controller
Mux
Mask+Latch
Pixel_preshapeBTTBBTTB
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
calice_circuits
Block Name
pixel_slice_preshape_BTTBBTTB
Last QA Review
Last Changed
Apr 17 09:39:17 2007


Note:
All resets buffered
with digital power
42 pixels
Note bus order changed >>
SRAM REGISTER
Logic
SR Controller
Mux
Mask+Latch
Pixel_preshapeTBTBBTTB
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
calice_circuits
Block Name
pixel_slice_preshape_TBTBBTTB
Last QA Review
Last Changed
Apr 17 09:44:30 2007

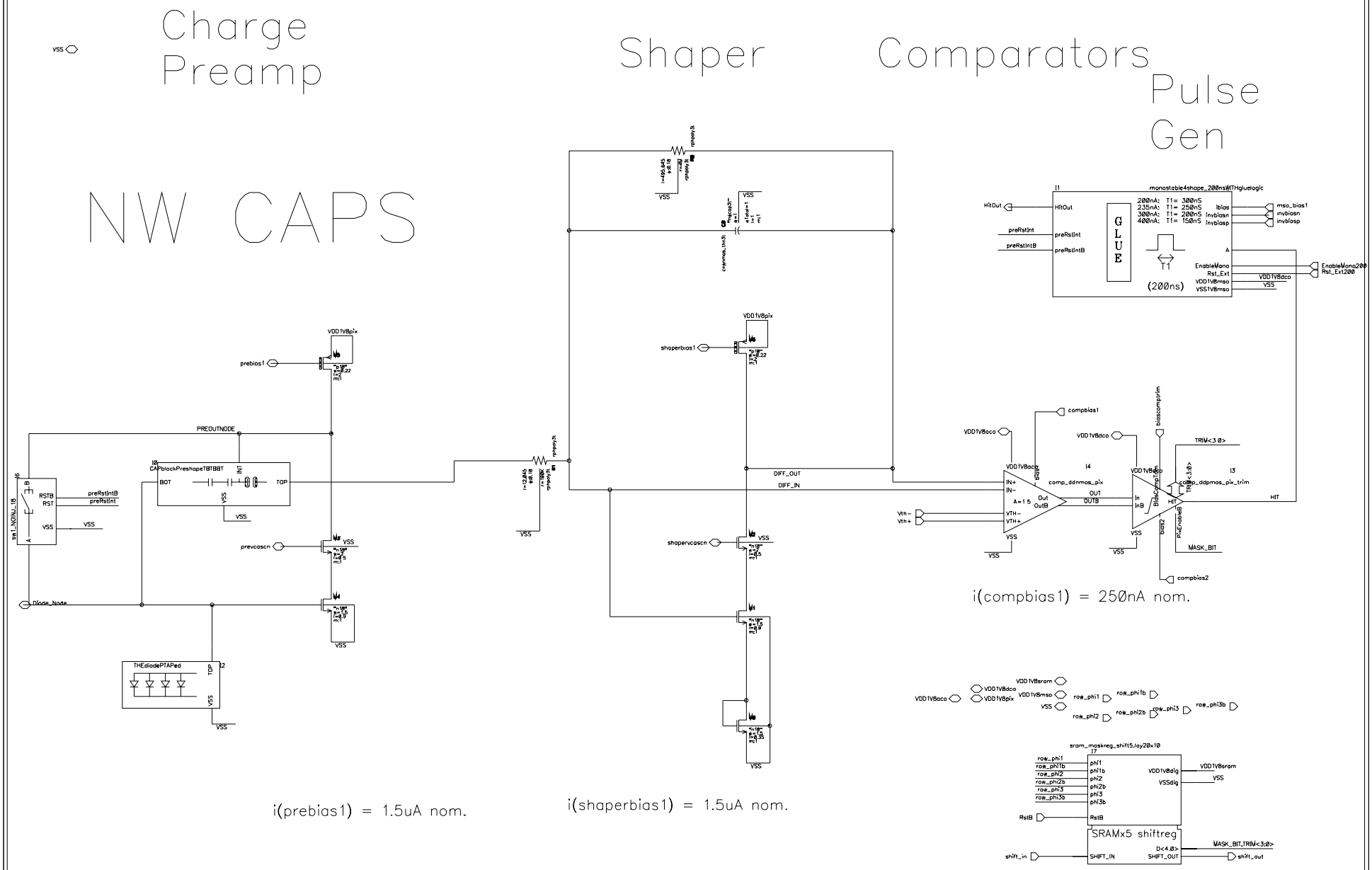


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_presampleBTBTTB18
Last QA Review	
Last Changed	Apr 16 16:39:45 2007

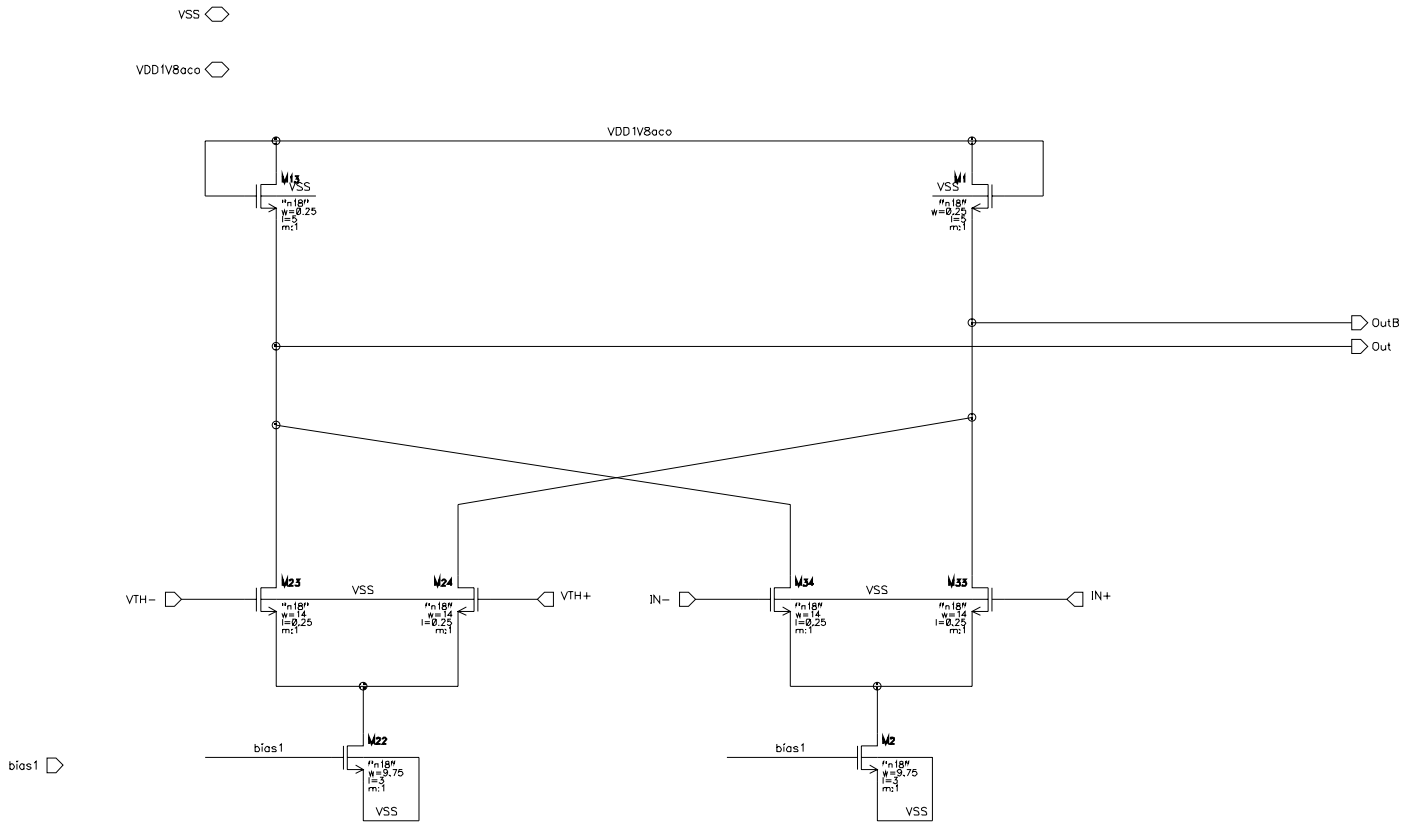

Power supplies & Ground
Mesh on M4(V) and M6 (H)
Biases
H on M5
Pulses
H on M3
*42
Pulses
V upwards
on M4
EnableMono V (or H)
monostable_200nsWITHgluelogic
monostable_600nsWITHgluelogic
GLUE
(200ns)
(600ns)
SRAMx5 shiftreg
sram_maskreg_shift5.lay20x10
sw1_NOINJ_18
CAPblockBTTBTB
CAPstorage
THEdiodePTAPed
1.3uA
1.2uA
900nA
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
CalicePixels
Block Name
Pixel_presampleBTTBTB18
Last OA Review
Last Changed
Mar 15 17:45:39 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_preshapeBTTBBTTB18
Last QA Review	
Last Changed	May 1 16:45:08 2007

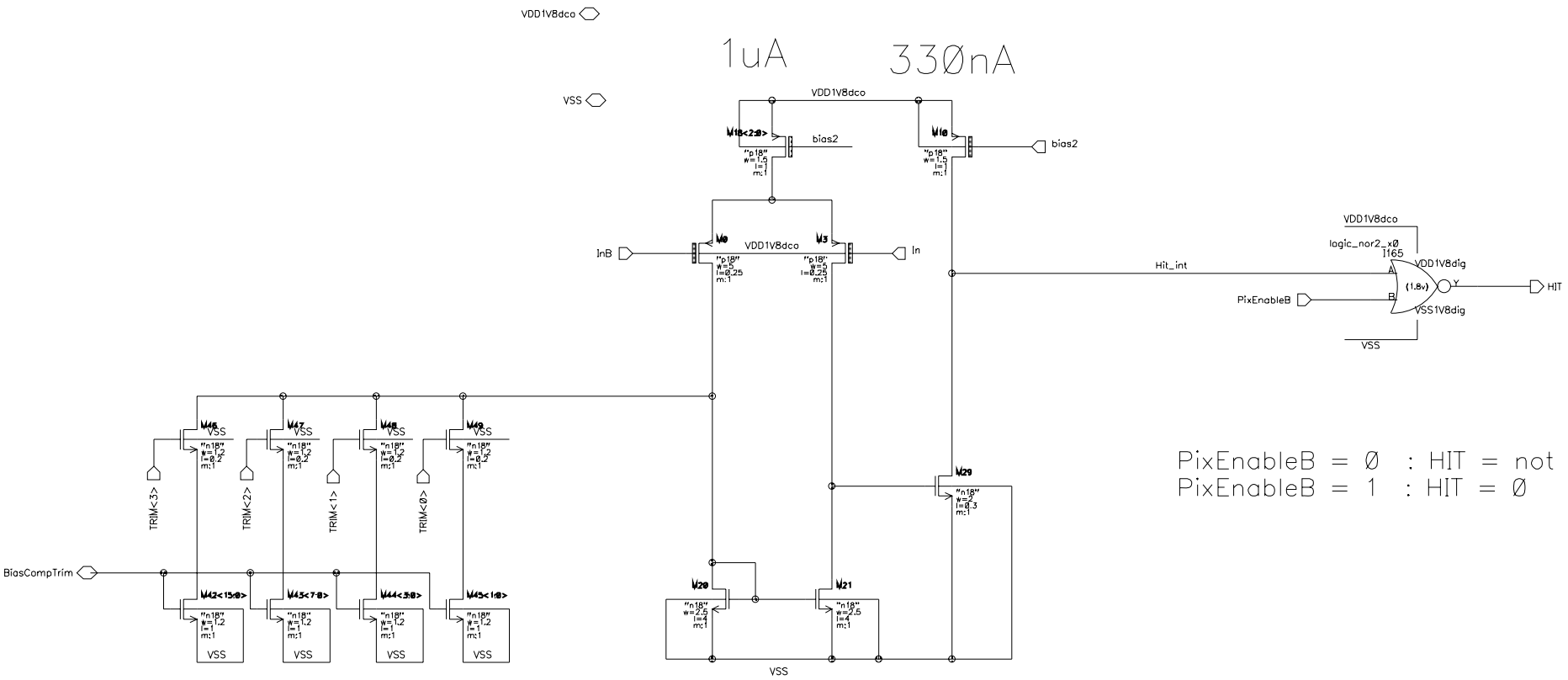


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	Pixel_preshapeTBTBBTTB18
Last QA Review	
Last Changed	May 3 09:42:12 2007



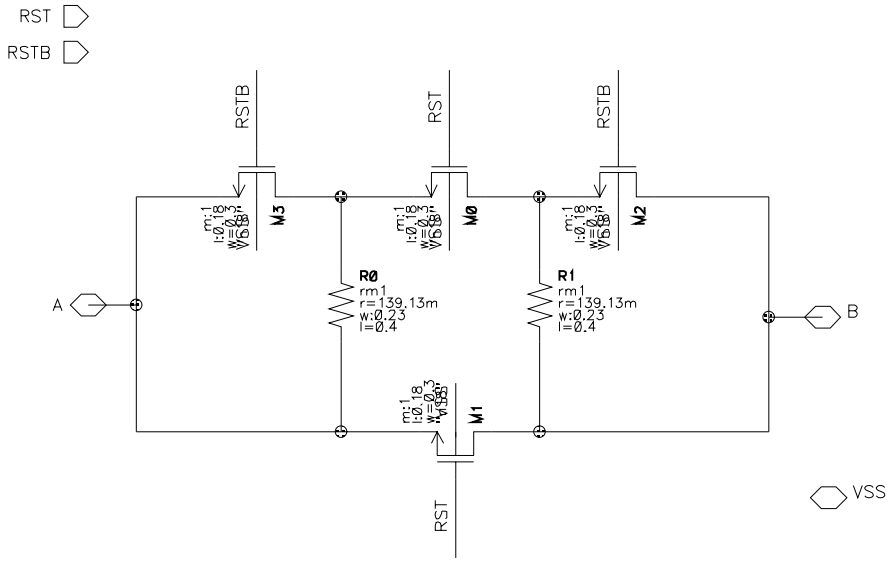
differential (10s of mV) hit signal wired across to pmos comparator at row logic

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Feb 25 17:02:52 2007

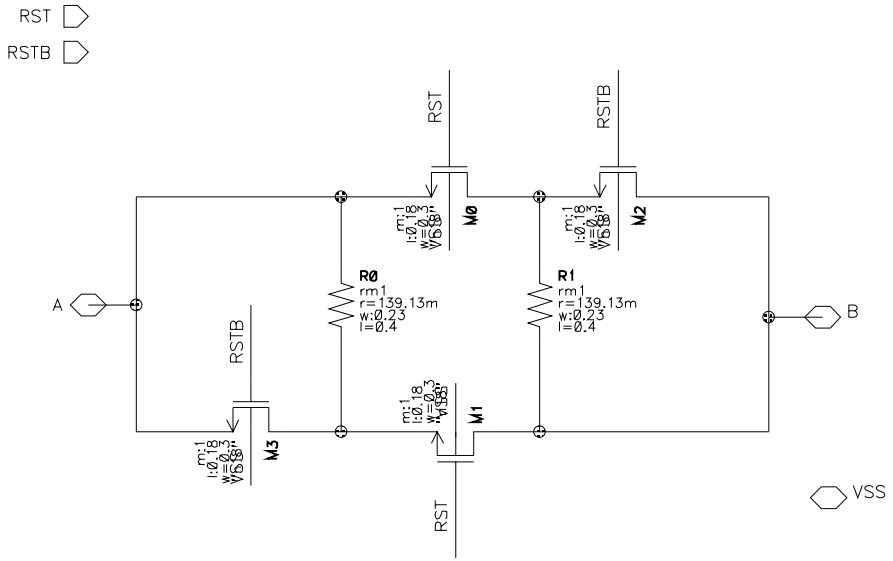


PixEnableB = Ø : HIT = not Hit_Int
PixEnableB = 1 : HIT = Ø

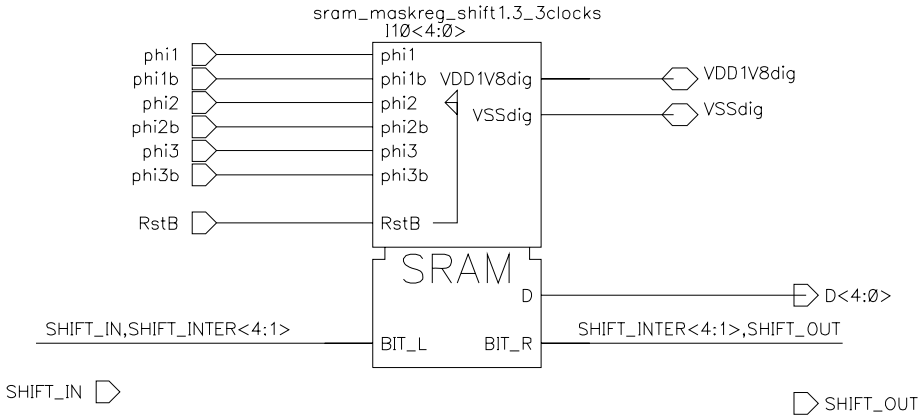
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	comp_ddpmos_pix_trim
Last QA Review	
Last Changed	Feb 17 16:53:26 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sw1_NOINJ_18
Last QA Review	
Last Changed	Feb 17 18:13:08 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sw1_NOINJ_18sh
Last QA Review	
Last Changed	Mar 20 19:34:26 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sram_maskreg_shift5.lay20x10
Last QA Review	
Last Changed	Mar 8 17:41:45 2007

New Shiftreg Revision 1.3 3CLOCKS!

> Added third clock for slow edge immunity

Layout inspired changes:

Reset transistor modified wider shorter
All TGs made width Ø.42

Resim & Check [ ]

POWER UP

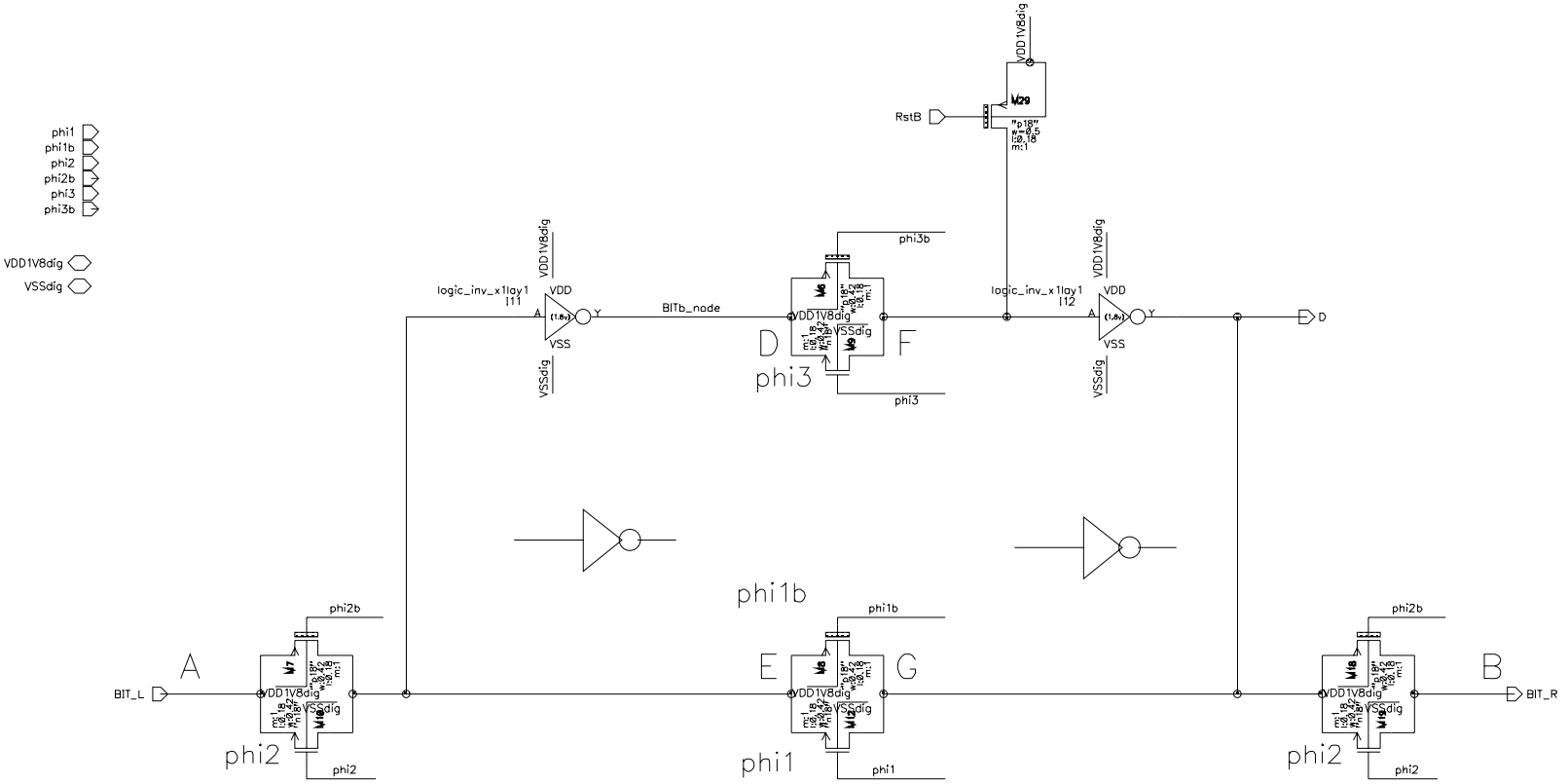
phi1 off
phi2 on
RstB on (low)

IN-SERVICE RESET

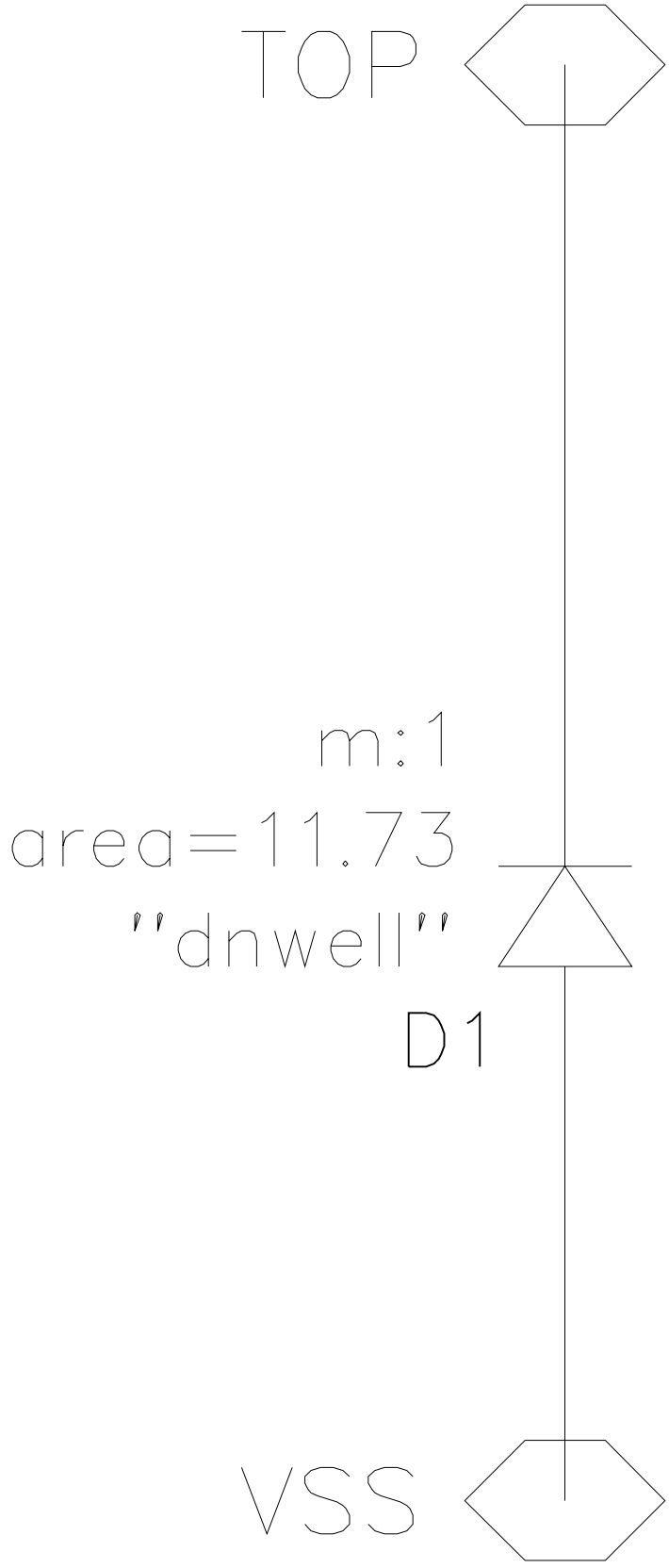
phi1 off
phi2 on
RstB pulsed on (low)
during phi2

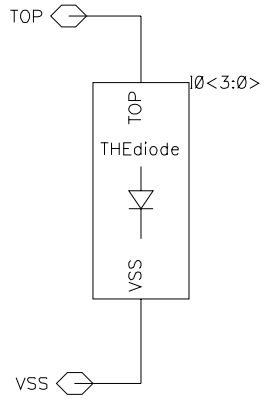
INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)

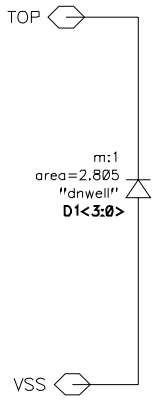


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	sram_maskreg_shift1.3_3clocks
Last QA Review	
Last Changed	Jun 27 11:55:45 2007

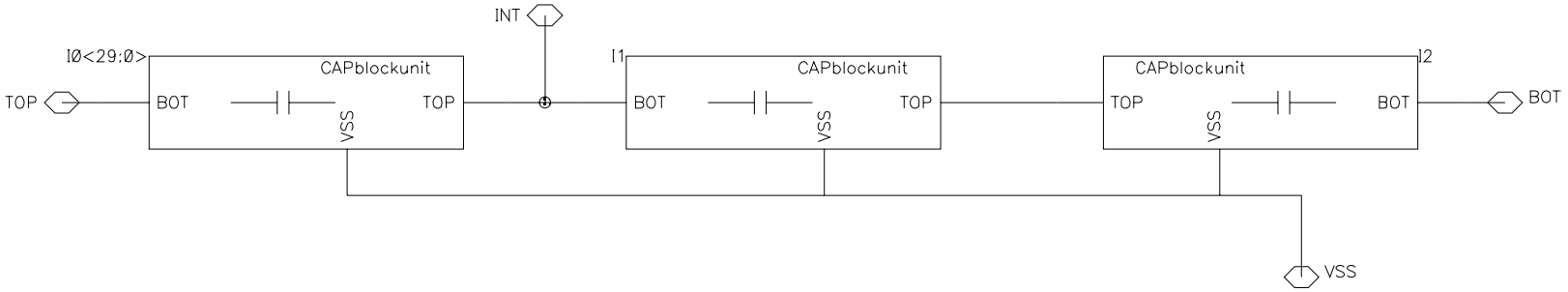

TOP
m:1
area=11.73
"dnwell"
D1
VSS



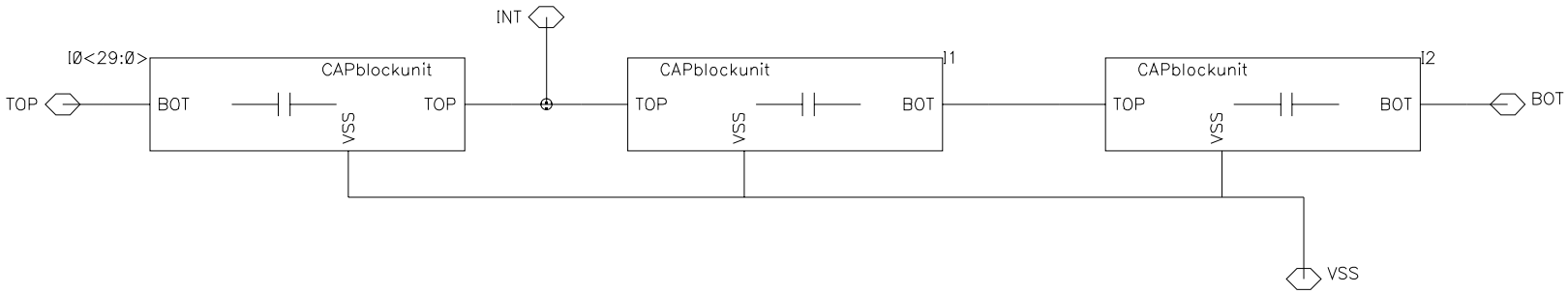
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	THEdiodePTAPed
Last QA Review	
Last Changed	Jun 27 11:57:01 2007



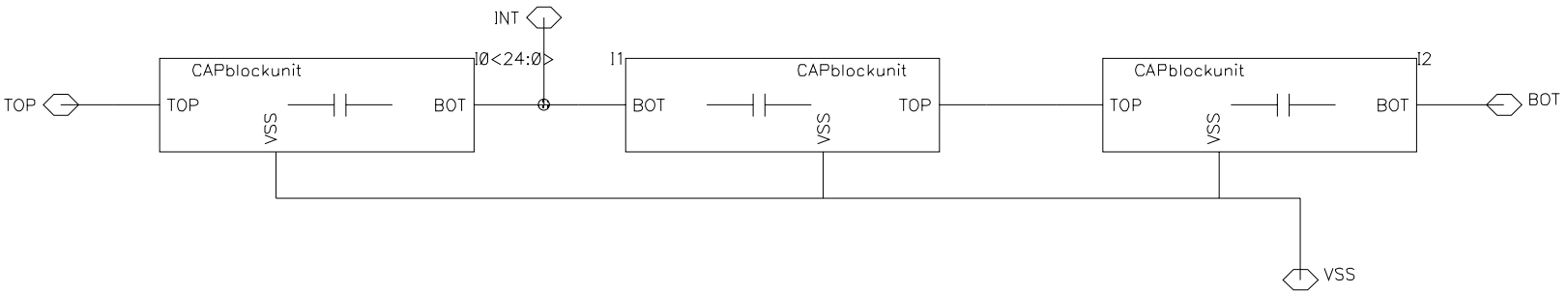
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	THEdiodePTAPed18
Last QA Review	
Last Changed	Jun 27 11:54:18 2007



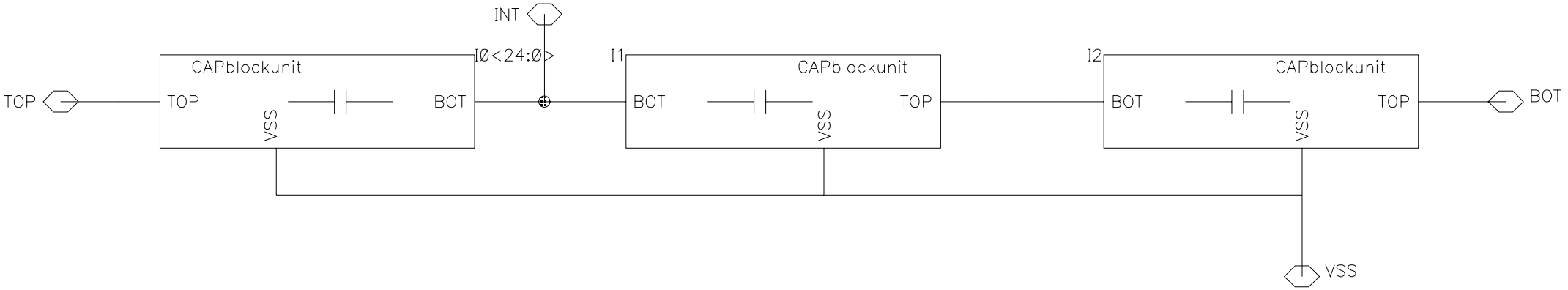
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockBTBTTB
Last QA Review	
Last Changed	Jun 27 11:53:27 2007

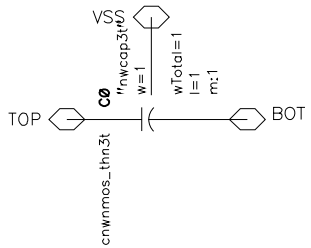


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockBTTBTB
Last QA Review	
Last Changed	Jun 27 11:57:11 2007

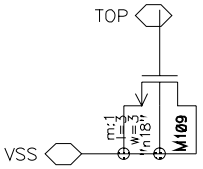


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockPreshapeBTTBBT
Last QA Review	
Last Changed	Jun 27 11:58:37 2007

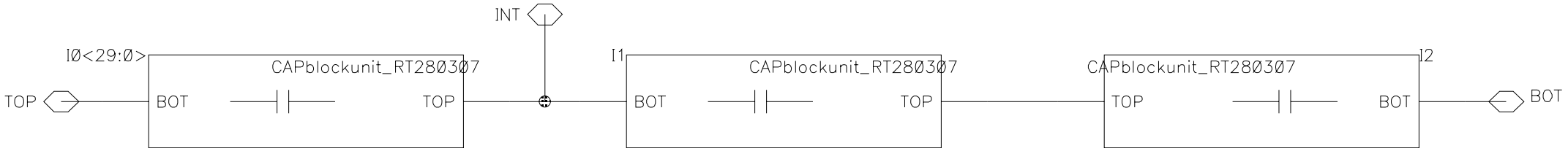

INT
I0<24:0>
I1
I2
CAPblockunit
CAPblockunit
CAPblockunit
TOP
TOP
BOT
BOT
TOP
BOT
TOP
BOT
VSS
VSS
VSS
VSS



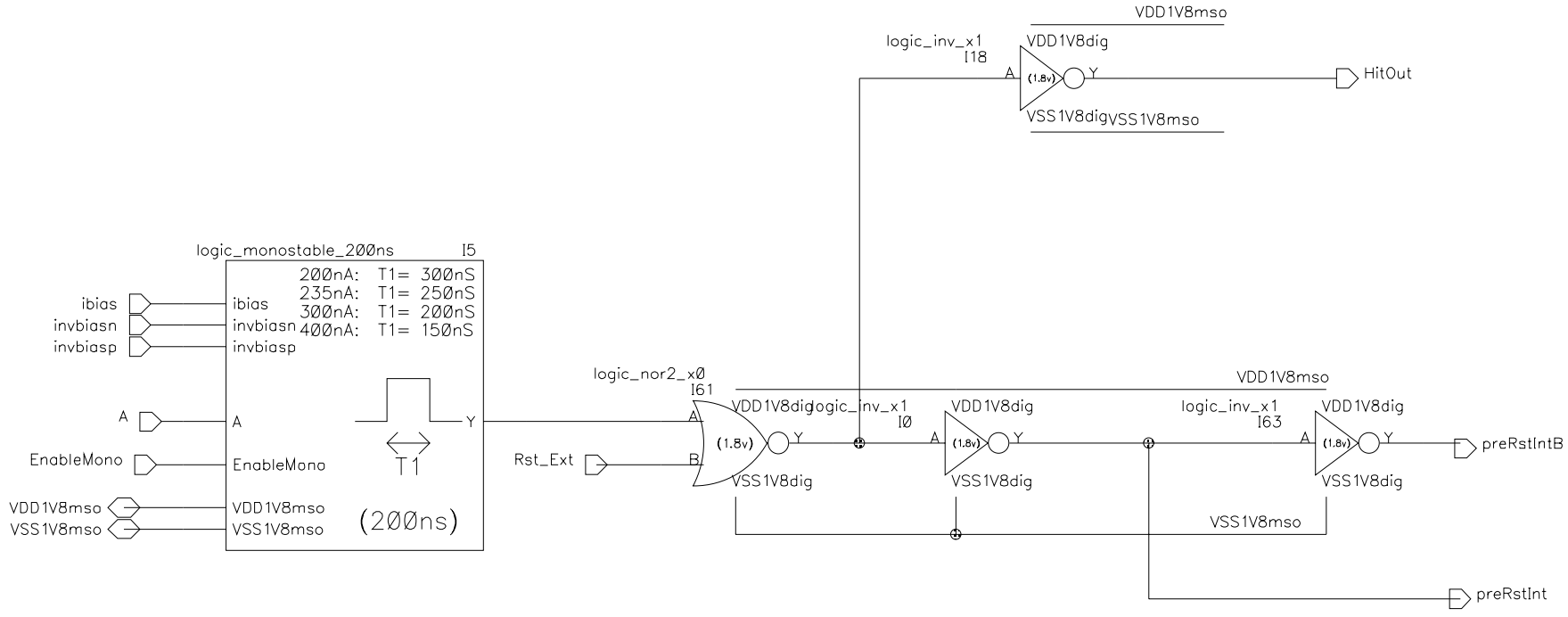
RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	CalicePixels
Block Name	CAPblockunit
Last QA Review	
Last Changed	Jun 27 11:53:47 2007



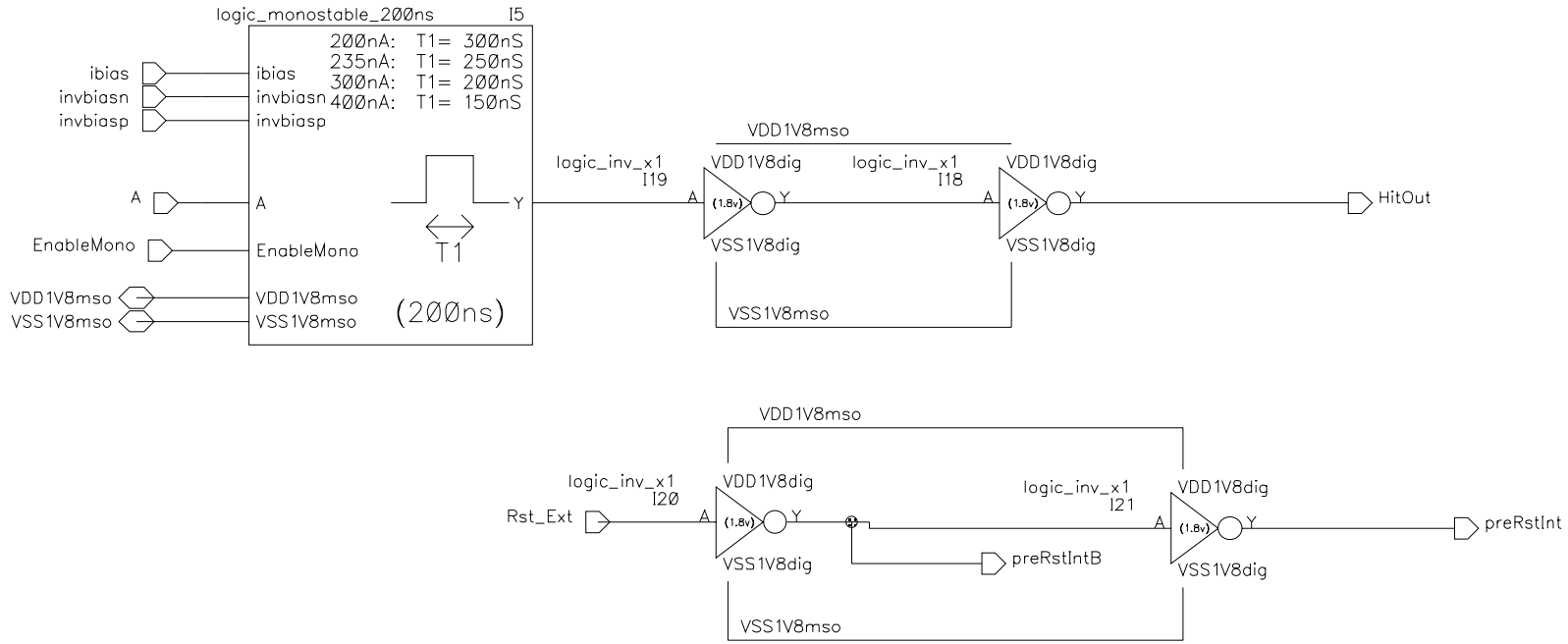
RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	CalicePixels	
Block Name	CAPstorage	
Last QA Review		
Last Changed	Jun 27 11:54:52 2007	


INT
I0<29:0>
CAPblockunit_RT28Ø3Ø7
I1
CAPblockunit_RT28Ø3Ø7
CAPblockunit_RT28Ø3Ø7
I2
TOP
BOT
TOP
BOT
TOP
BOT
TOP
BOT

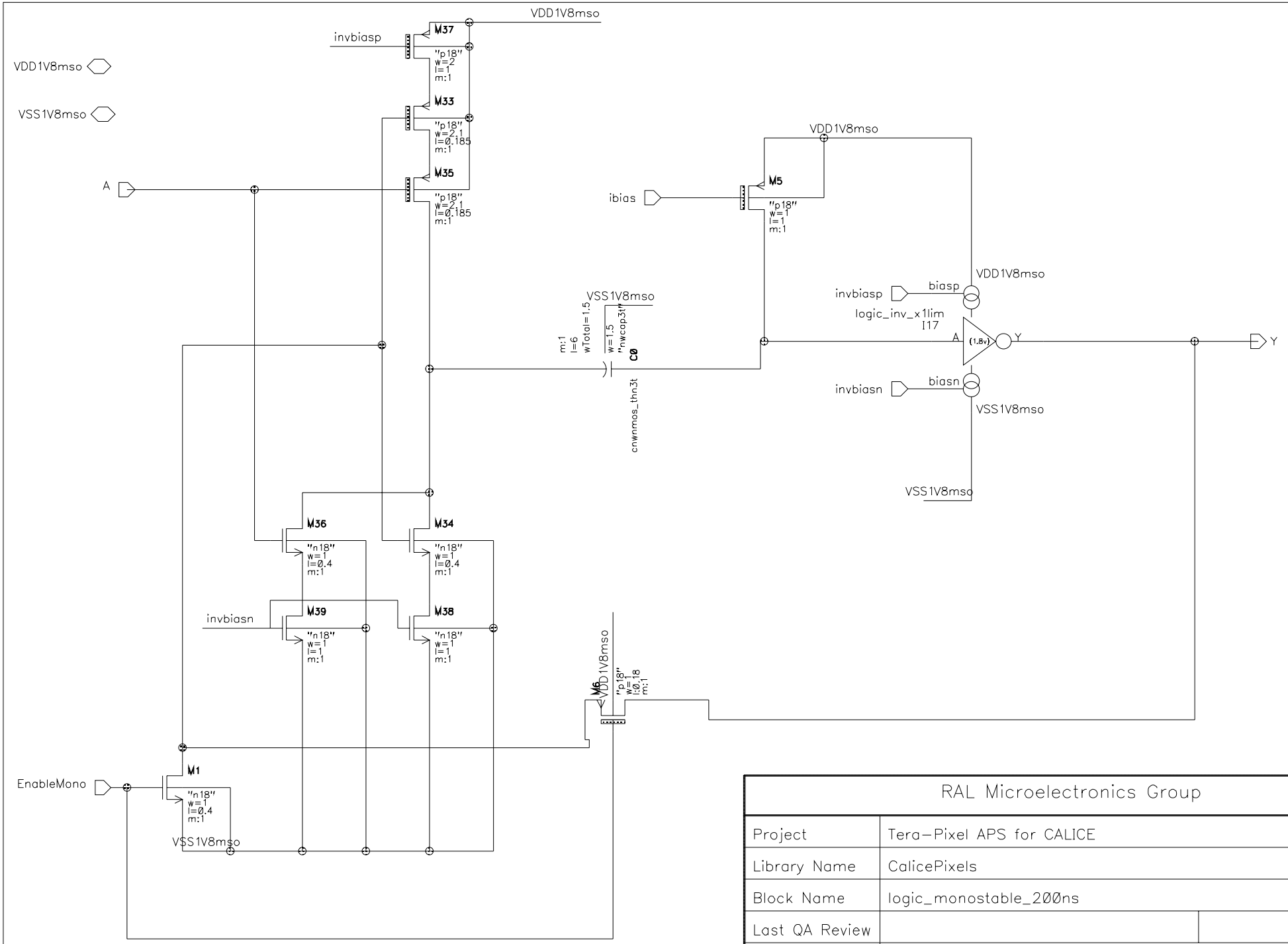
Top
C0
"nwcap2t"
W = 1
WTotal = 1
l = 1
Bot



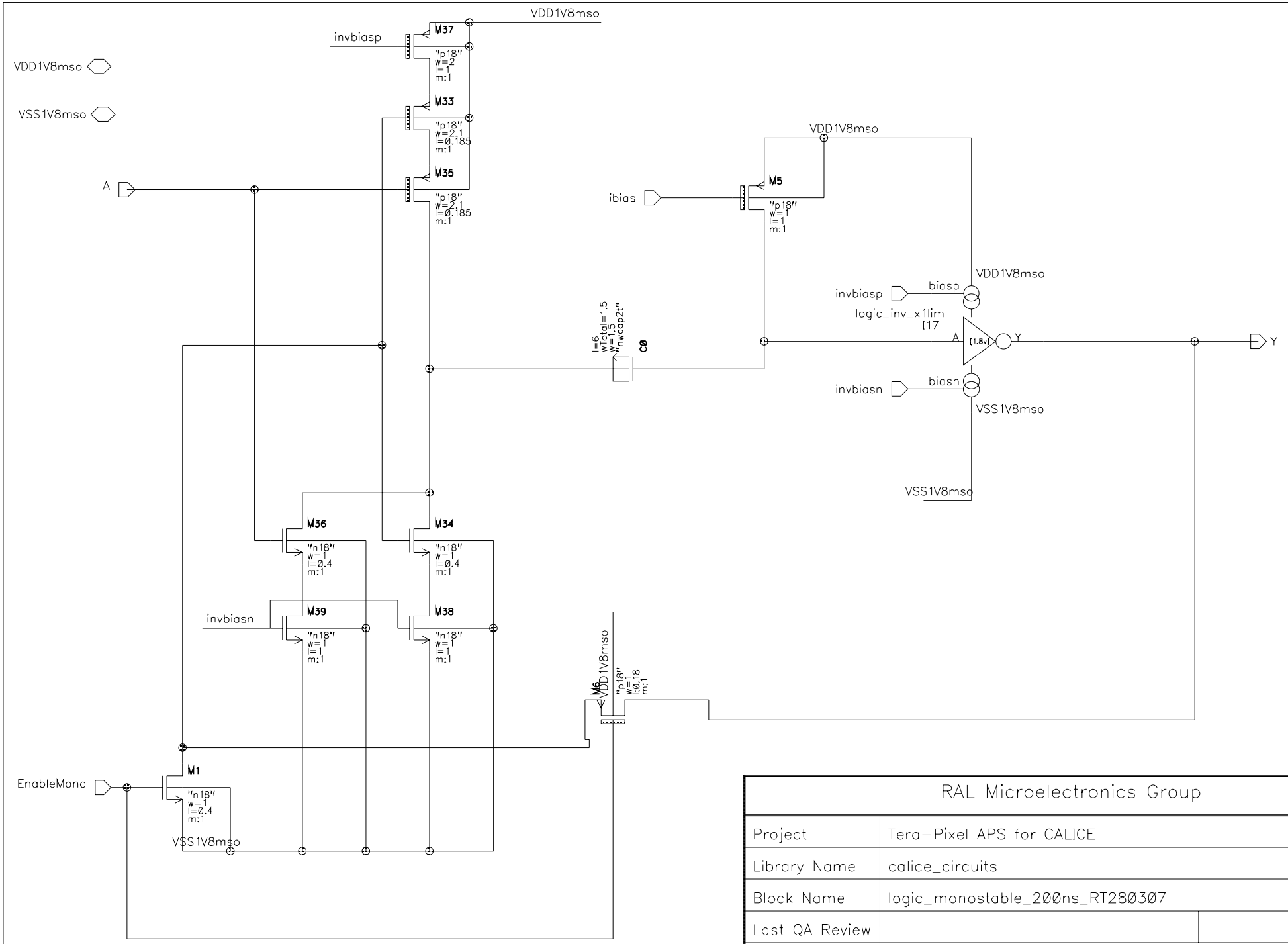
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_200nsWITHgluelogic
Last QA Review	
Last Changed	Feb 13 11:47:56 2007



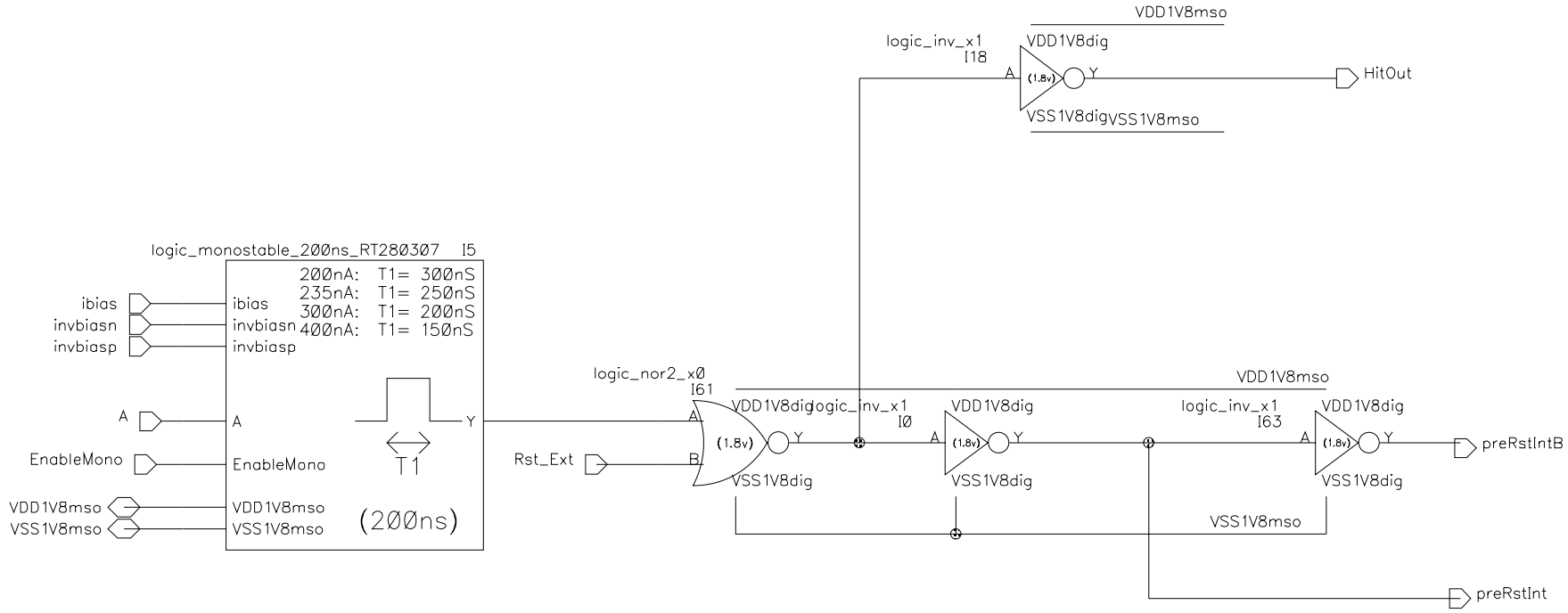
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable4shape_200nsWITHgluelogic
Last QA Review	
Last Changed	May 1 16:43:18 2007



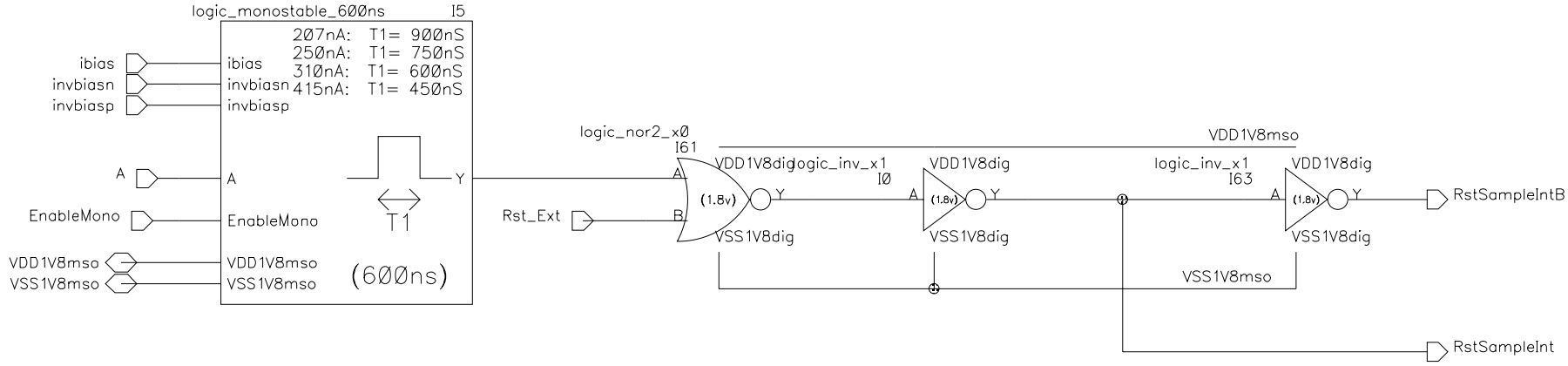
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_monostable_200ns
Last QA Review	
Last Changed	May 1 16:43:13 2007



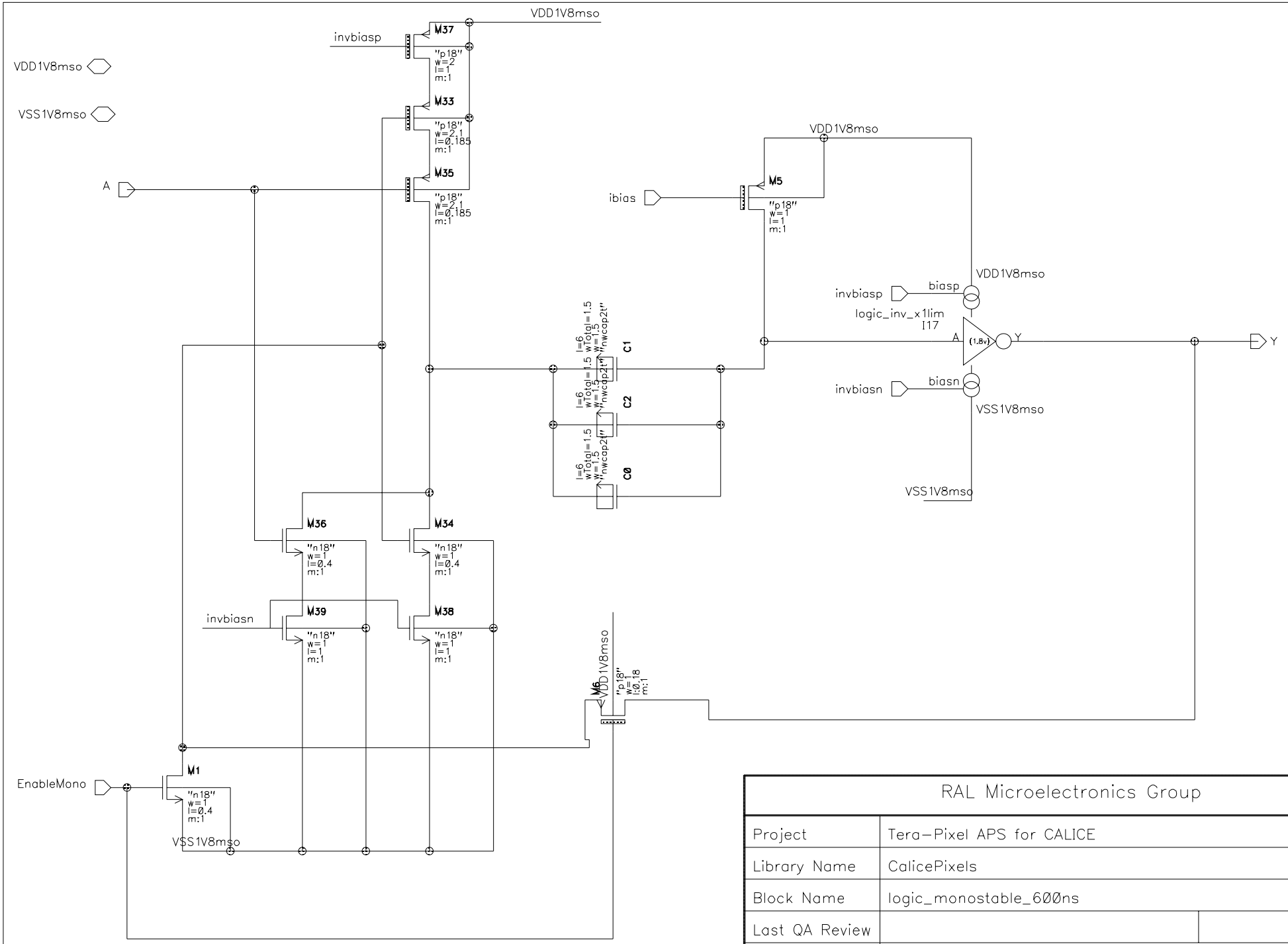
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_monostable_200ns_RT280307
Last QA Review	
Last Changed	Mar 28 13:40:15 2007



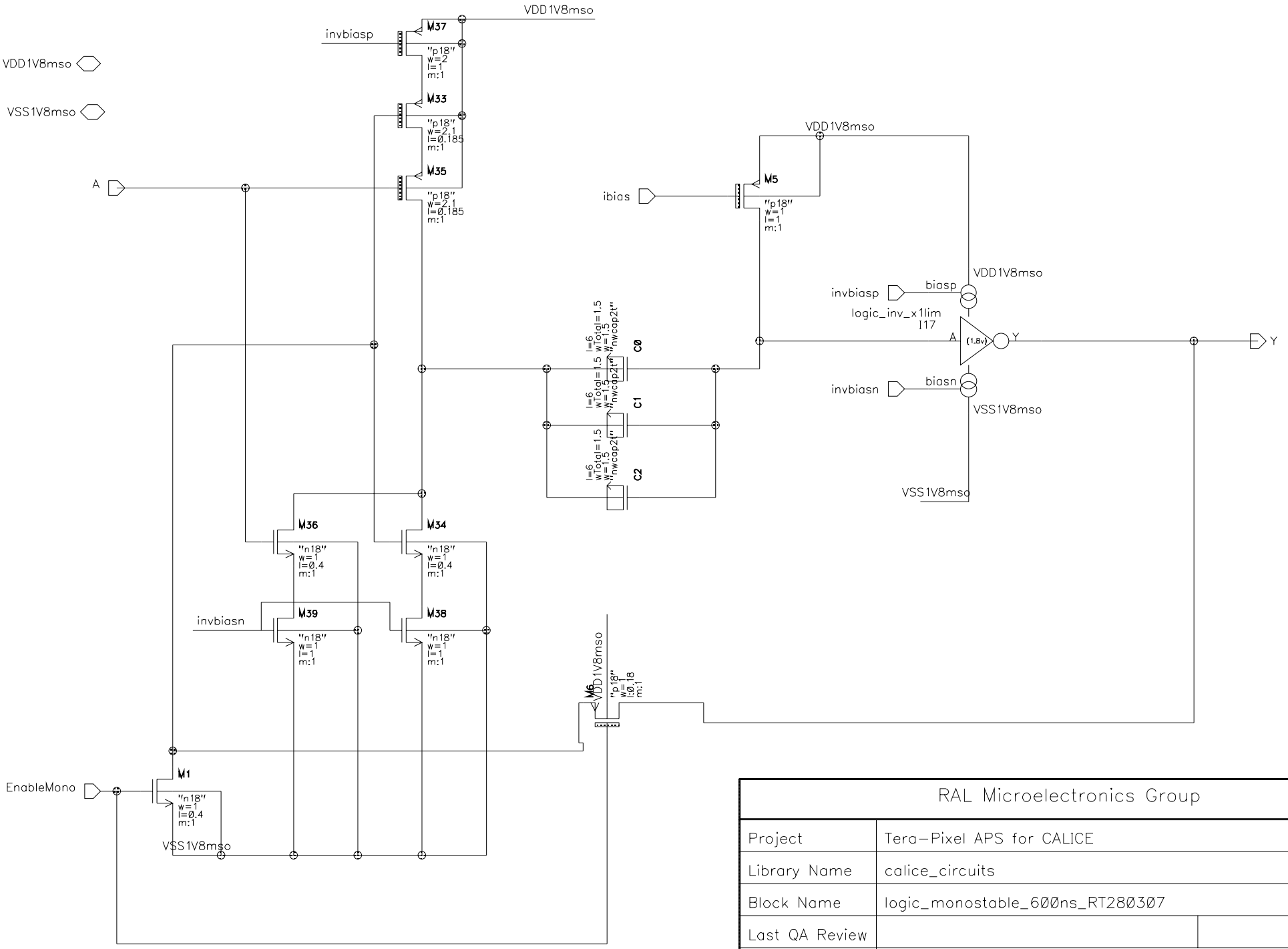
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	monostable_200nsWITHgluelogic_RT280307
Last QA Review	
Last Changed	Mar 28 13:40:20 2007



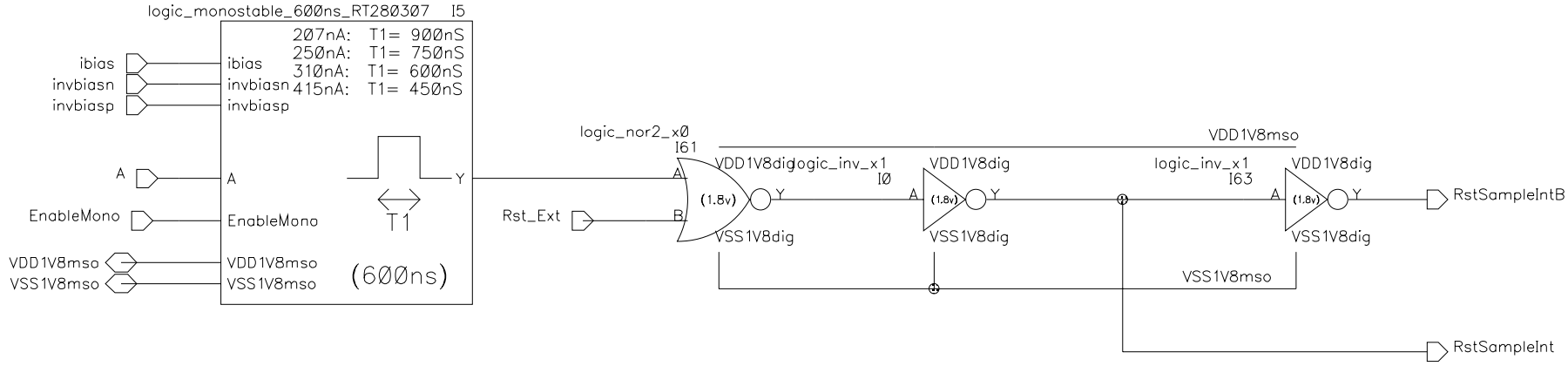
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	monostable_600nsWITHgluelogic
Last QA Review	
Last Changed	Mar 15 16:42:09 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_monostable_600ns
Last QA Review	
Last Changed	Apr 16 16:39:18 2007

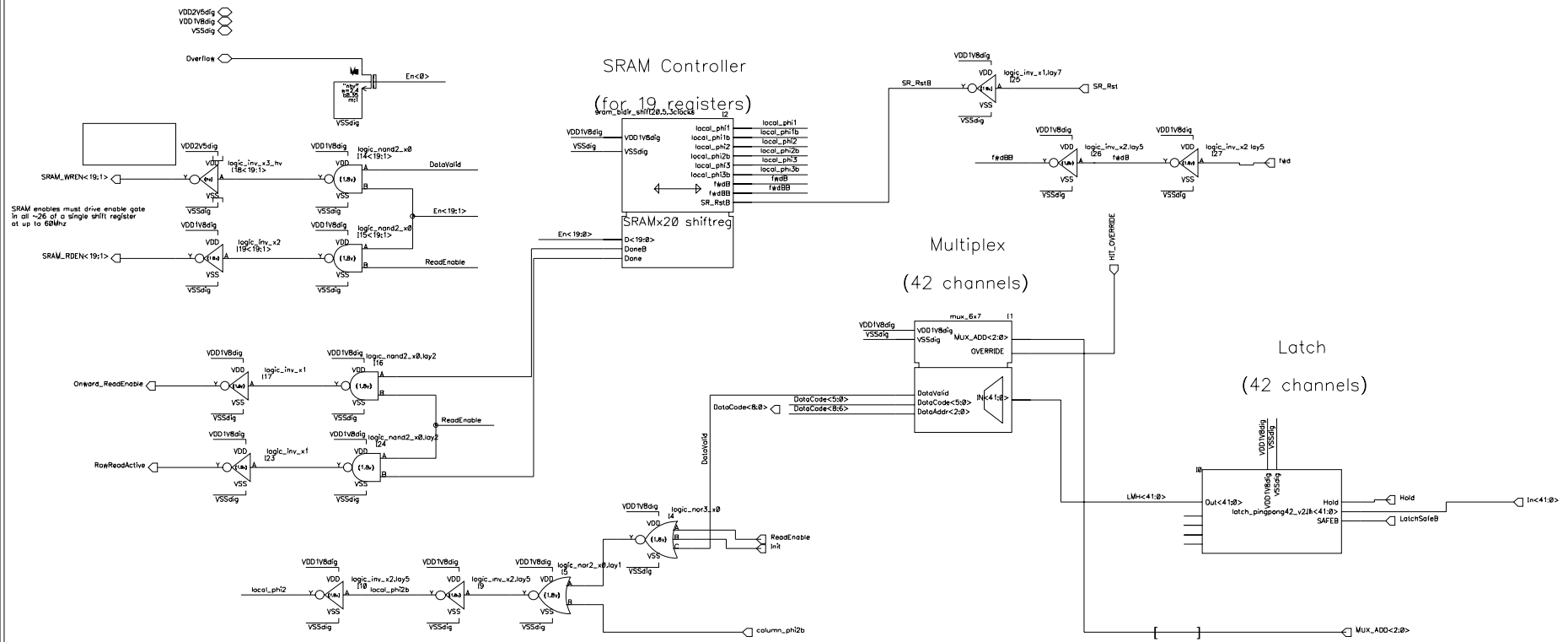


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_monostable_600ns_RT280307
Last QA Review	
Last Changed	Mar 28 13:41:16 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	monostable_600nsWITHgluelogic_RT280307
Last QA Review	
Last Changed	Mar 28 13:41:19 2007

42-CHANNEL 3-CLOCKS VERSION

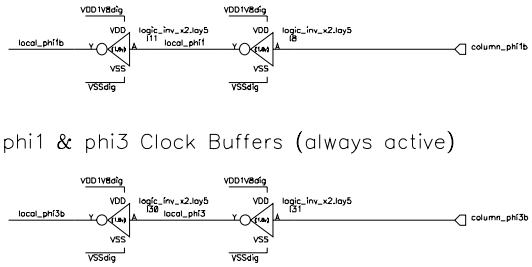


SRAM clocks are distributed as inverse polarity

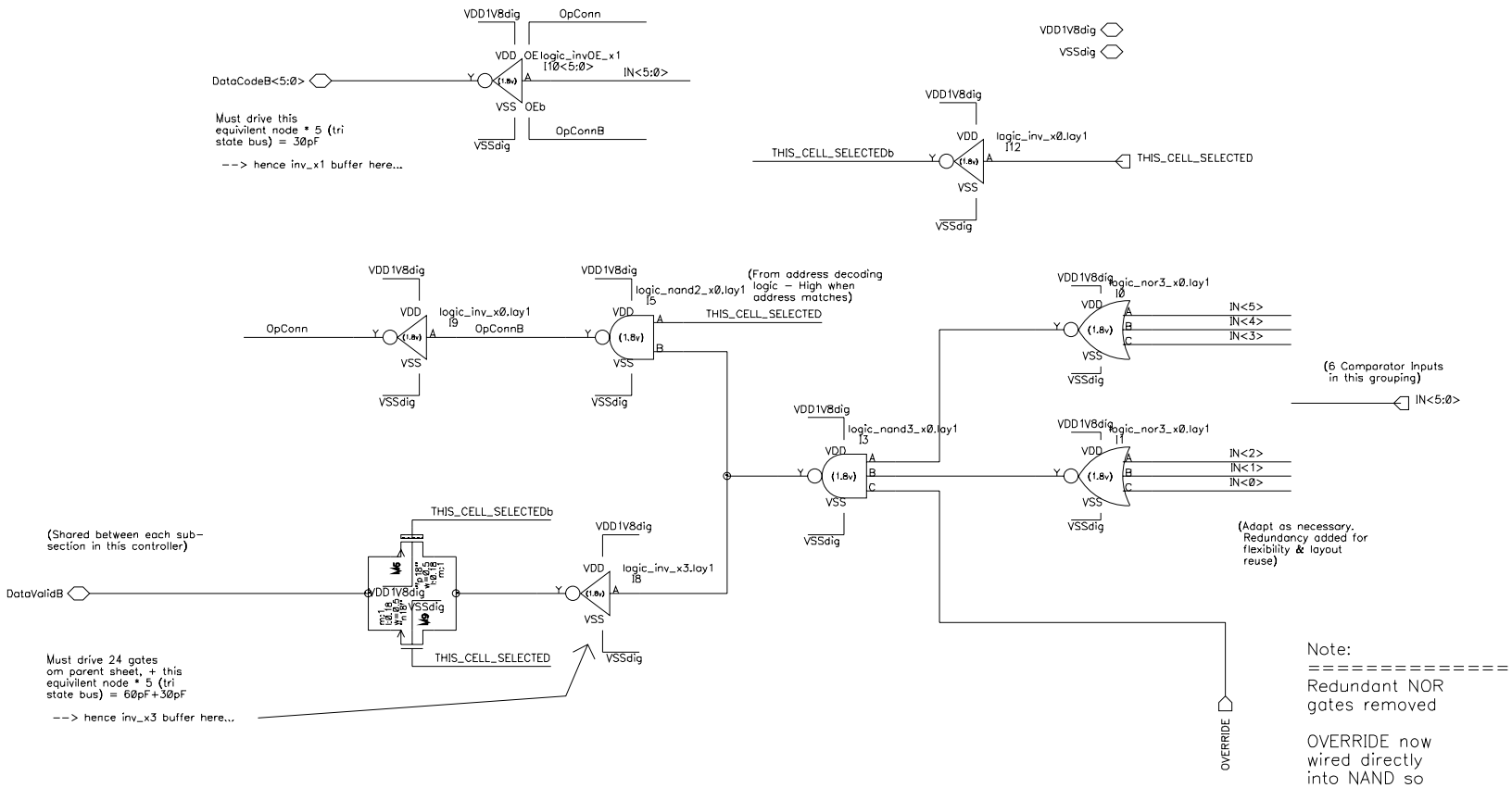
ra convenient for phi2 gating, since the inverted phi2 input to the NOR gate completes inversion of its inputs and outputs to turn it into an AND gate

phi1 is distributed in inverted form for consistency

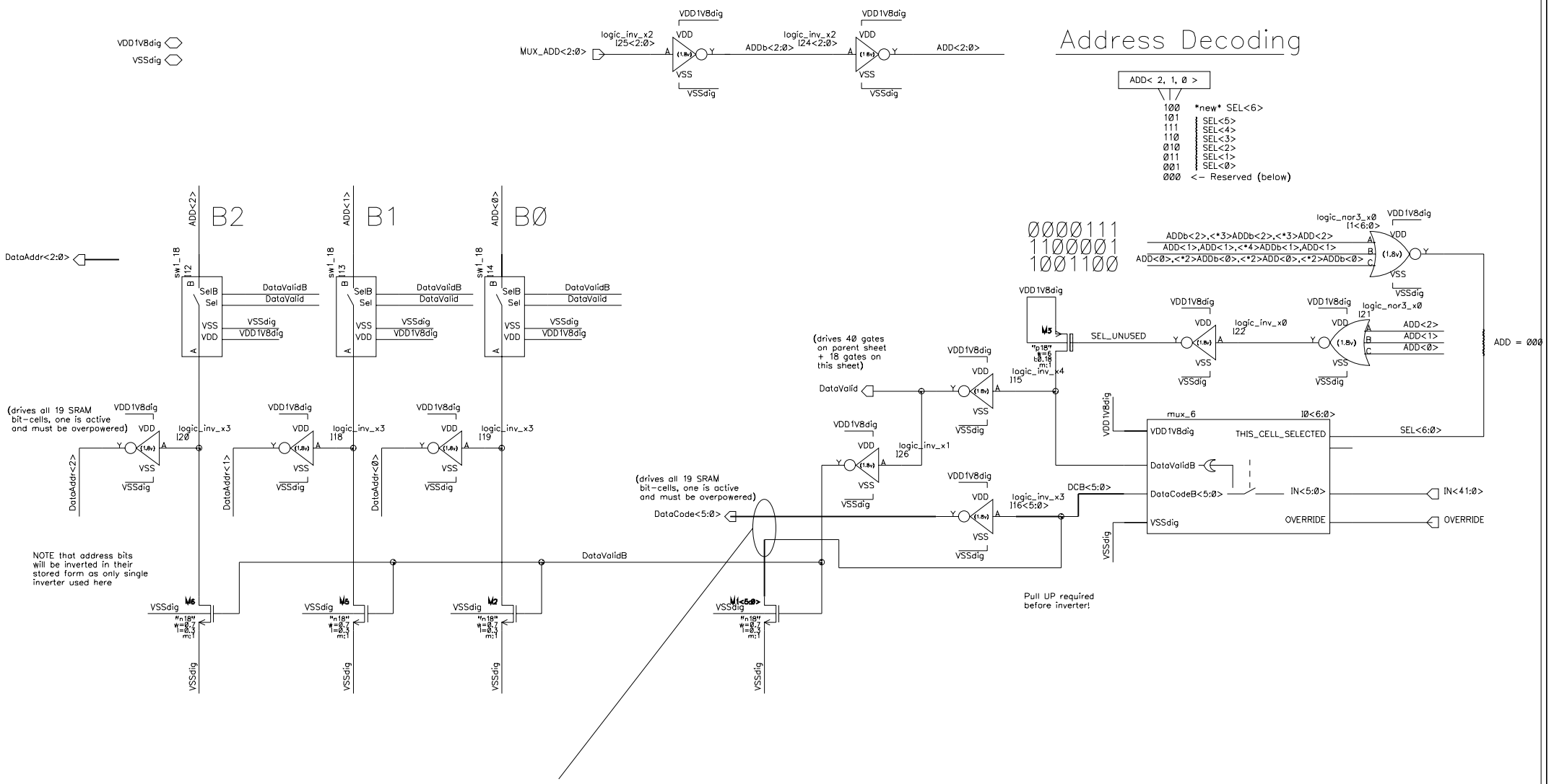
Local phi1 & phi3 Clock Buffers (always active)



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	master_row_controller_42.2
Last QA Review	
Last Changed	Apr 19 11:33:28 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6
Last QA Review	
Last Changed	Jan 11 15:41:42 2007



Note new buffer for local DataValid

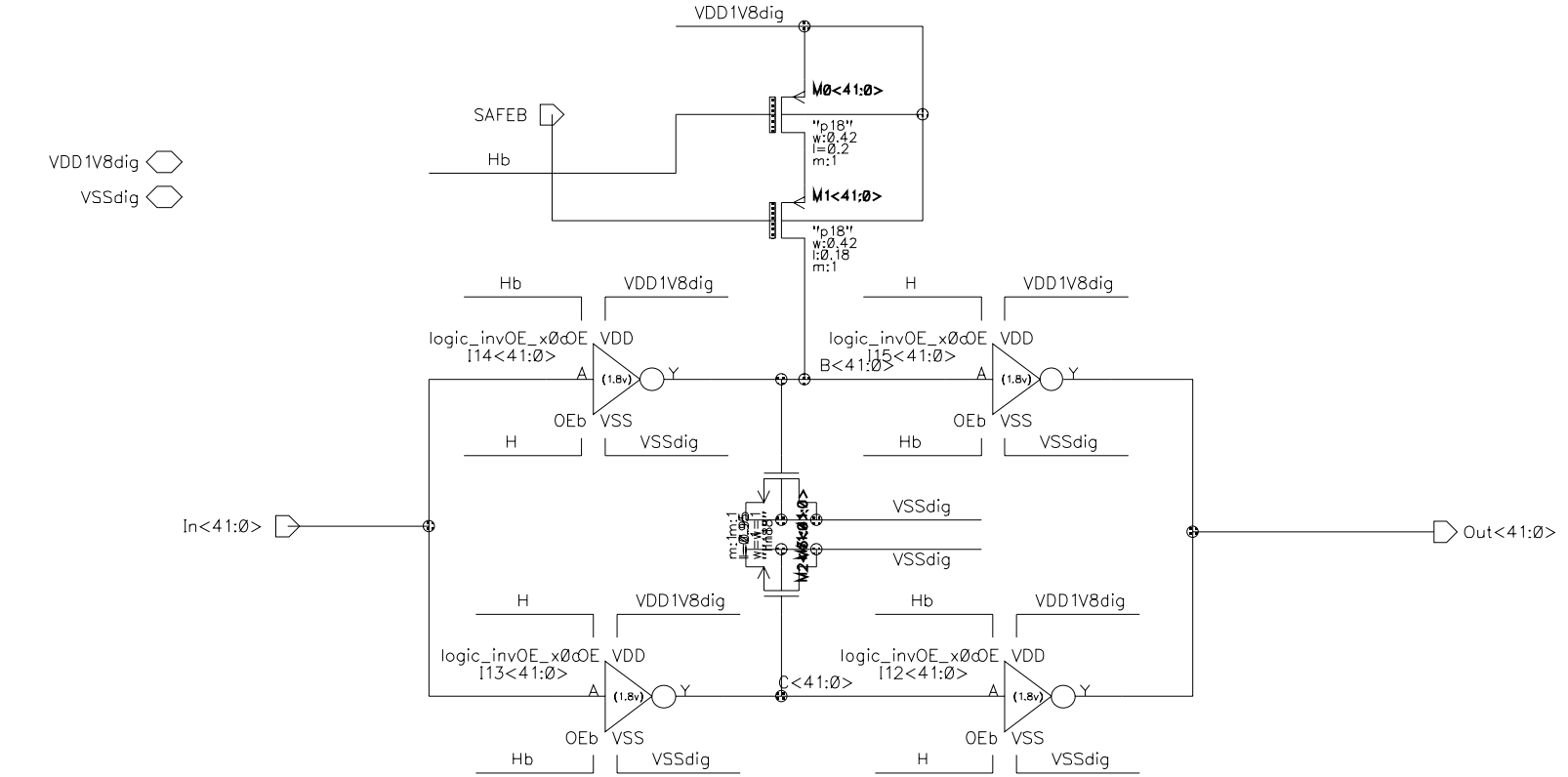
Modifications in progress – CONFIRM!

ERROR CORRECTED:

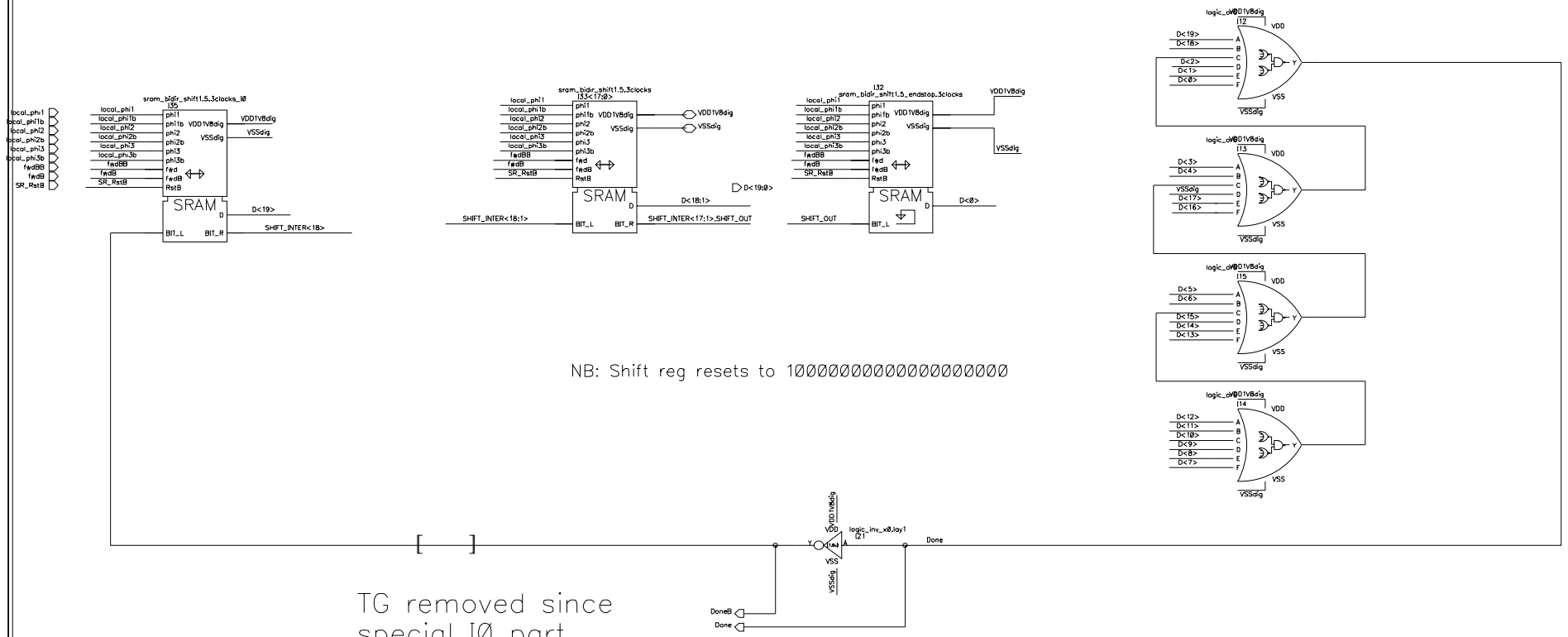
DataCode should be pulled down BEFORE the inverter not after

ReSim to confirm.

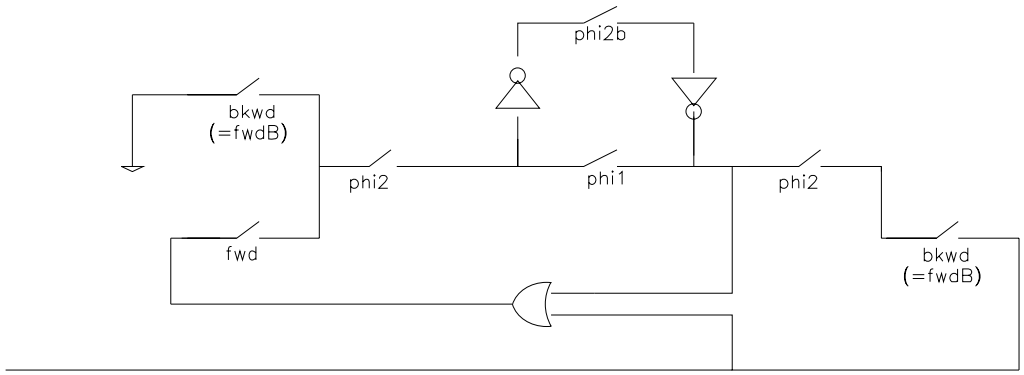
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	mux_6x7
Last QA Review	
Last Changed	Feb 16 10:35:10 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	latch_pingpong42_v2.1
Last QA Review	
Last Changed	Mar 27 19:20:29 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bidir_shift20.5.3clocks
Last QA Review	
Last Changed	Apr 19 11:33:26 2007



POWER UP

phi1 off
phi2 on
RstB on (low)

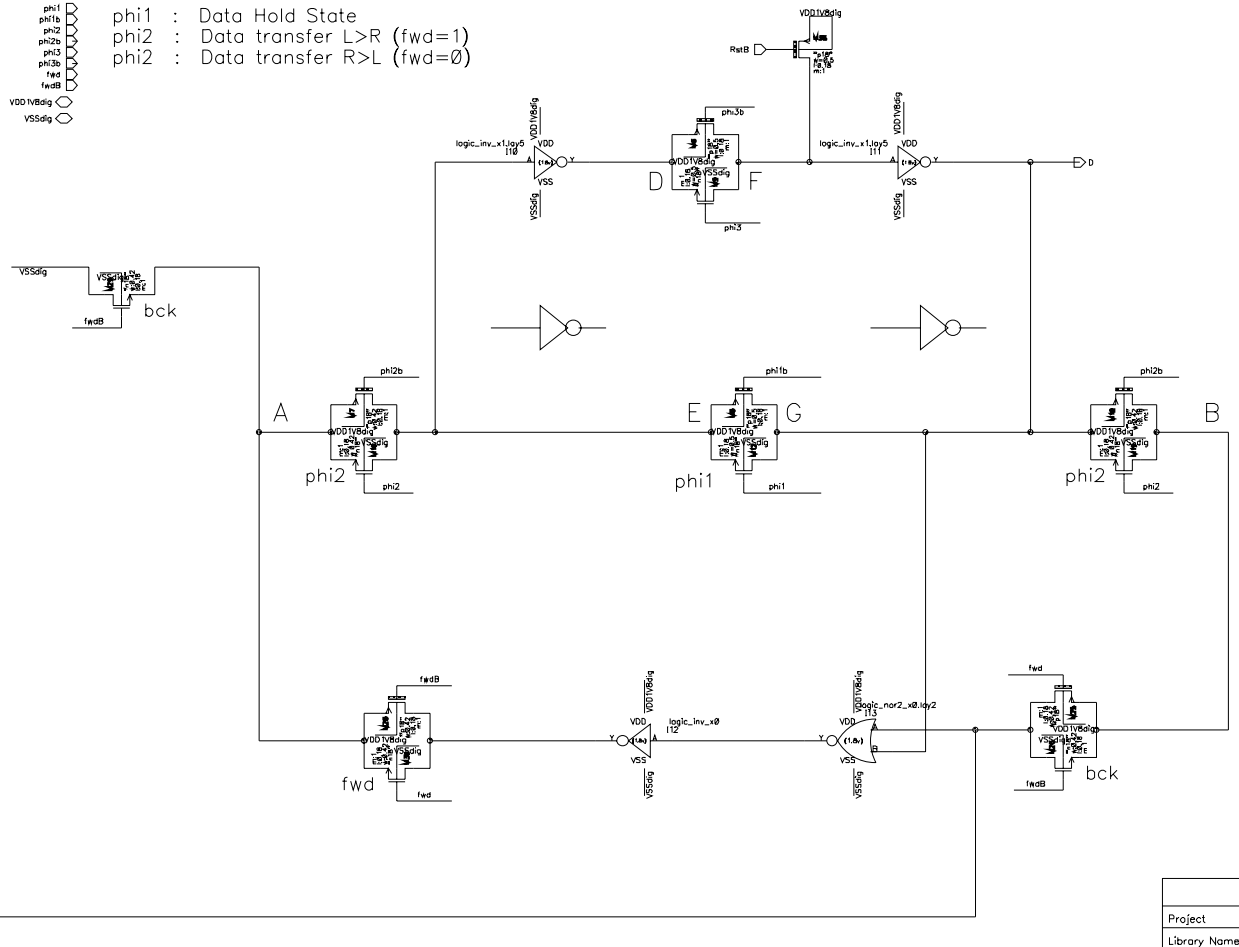
IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low)
during phi2

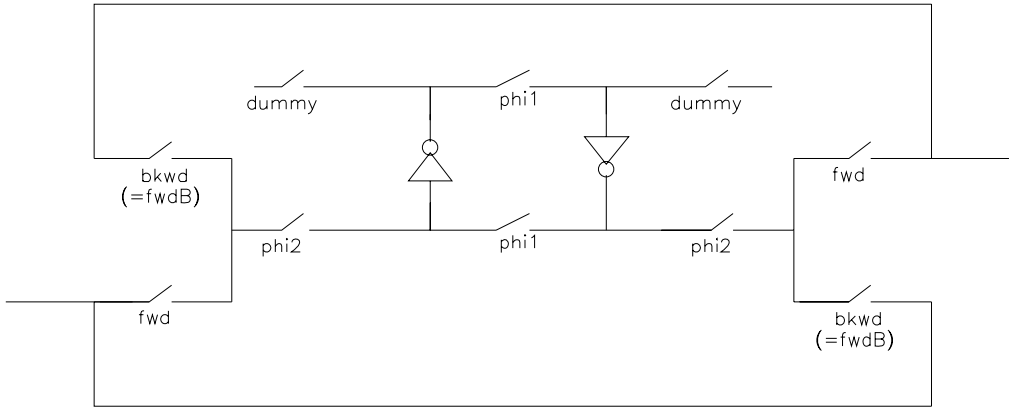
INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)

phi1 : Data Hold State
phi2 : Data transfer L>R (fwd=1)
phi2 : Data transfer R>L (fwd=Ø)



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bidir_shift1.5_endstop.3clocks
Last QA Review	
Last Changed	Apr 19 10:55:08 2007



POWER UP

phi1 off
phi2 on
RstB on (low)

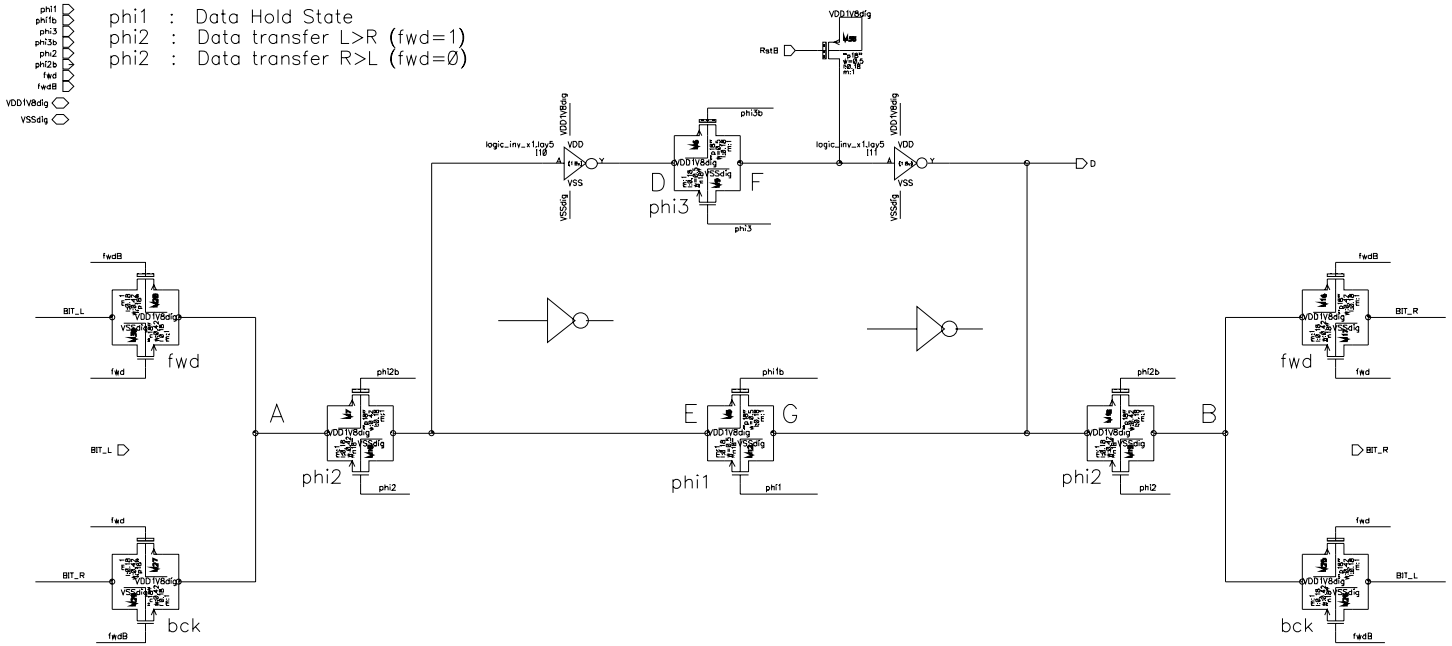
IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low)
during phi2

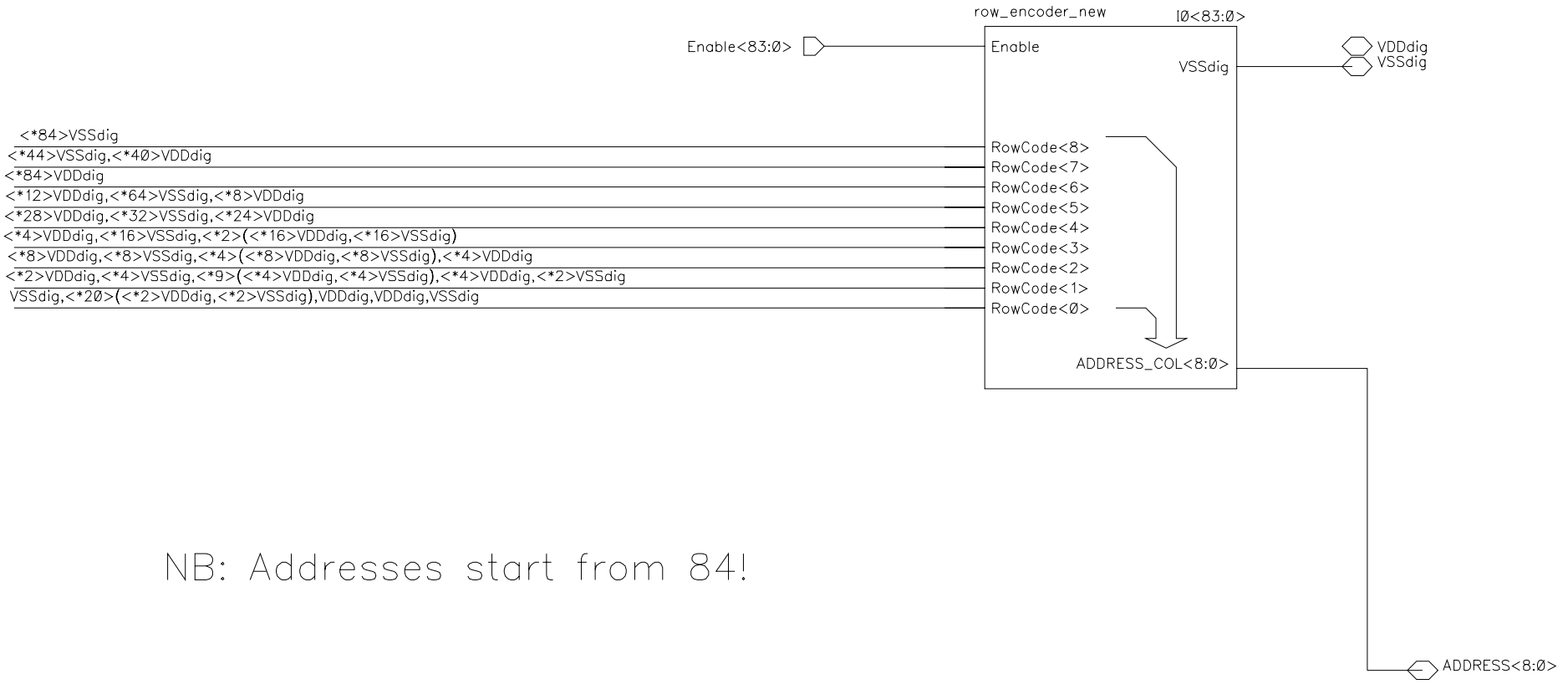
INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)

phi1 : Data Hold State
phi2 : Data transfer L>R (fwd=1)
phi2 : Data transfer R>L (fwd=Ø)

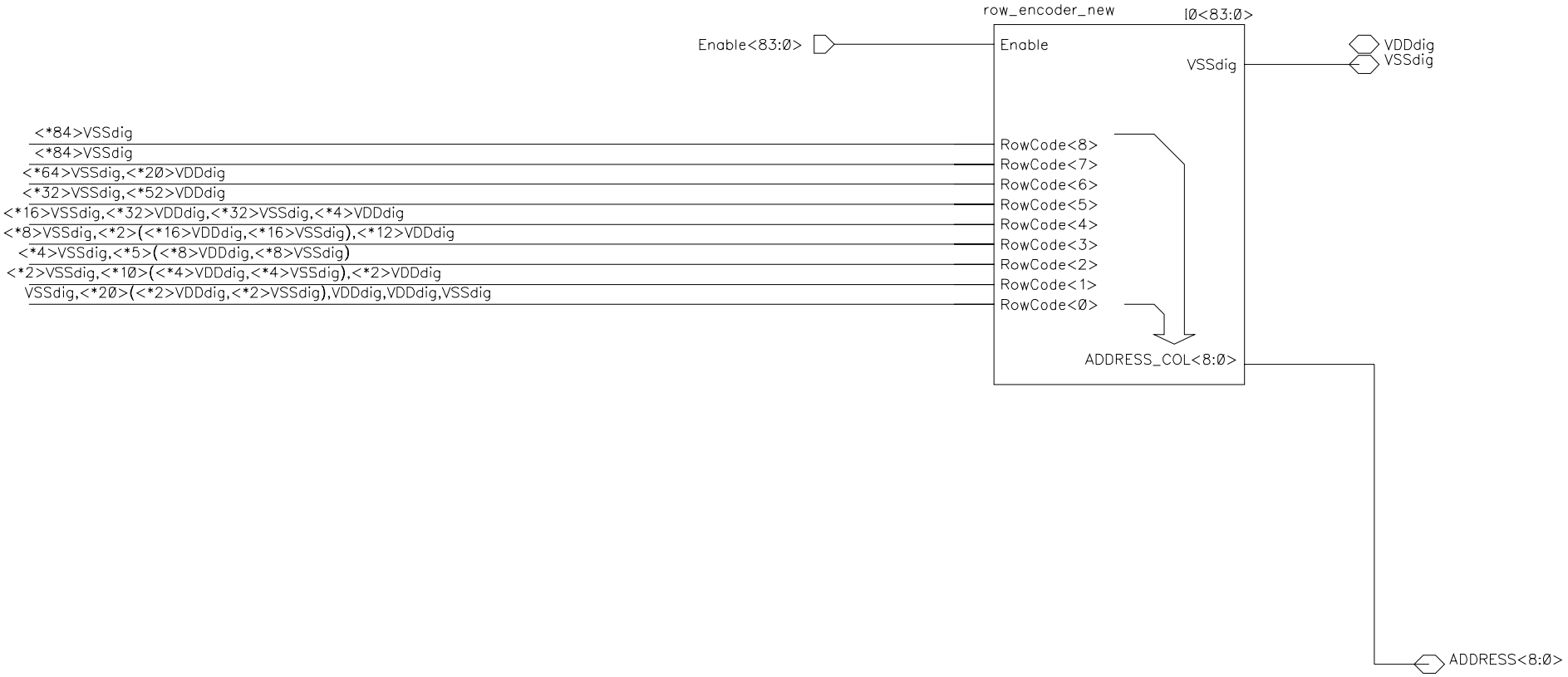


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_bidir_shift1.5.3clocks
Last QA Review	
Last Changed	Apr 19 11:06:51 2007

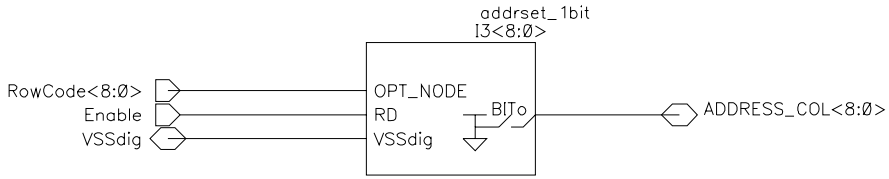


NB: Addresses start from 84!

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	addrset_84top
Last QA Review	
Last Changed	Mar 15 17:05:41 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_84
Last QA Review	
Last Changed	Jan 15 09:52:29 2007

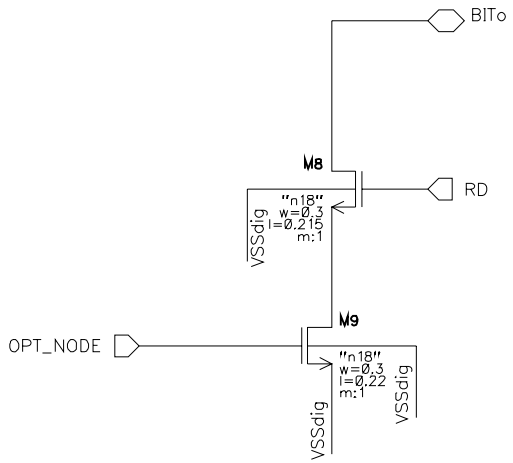


Set Row Code input to the unique row address: with net names in schematics; with repeated tie up/down cells in layout.

GRAY CODE should be used

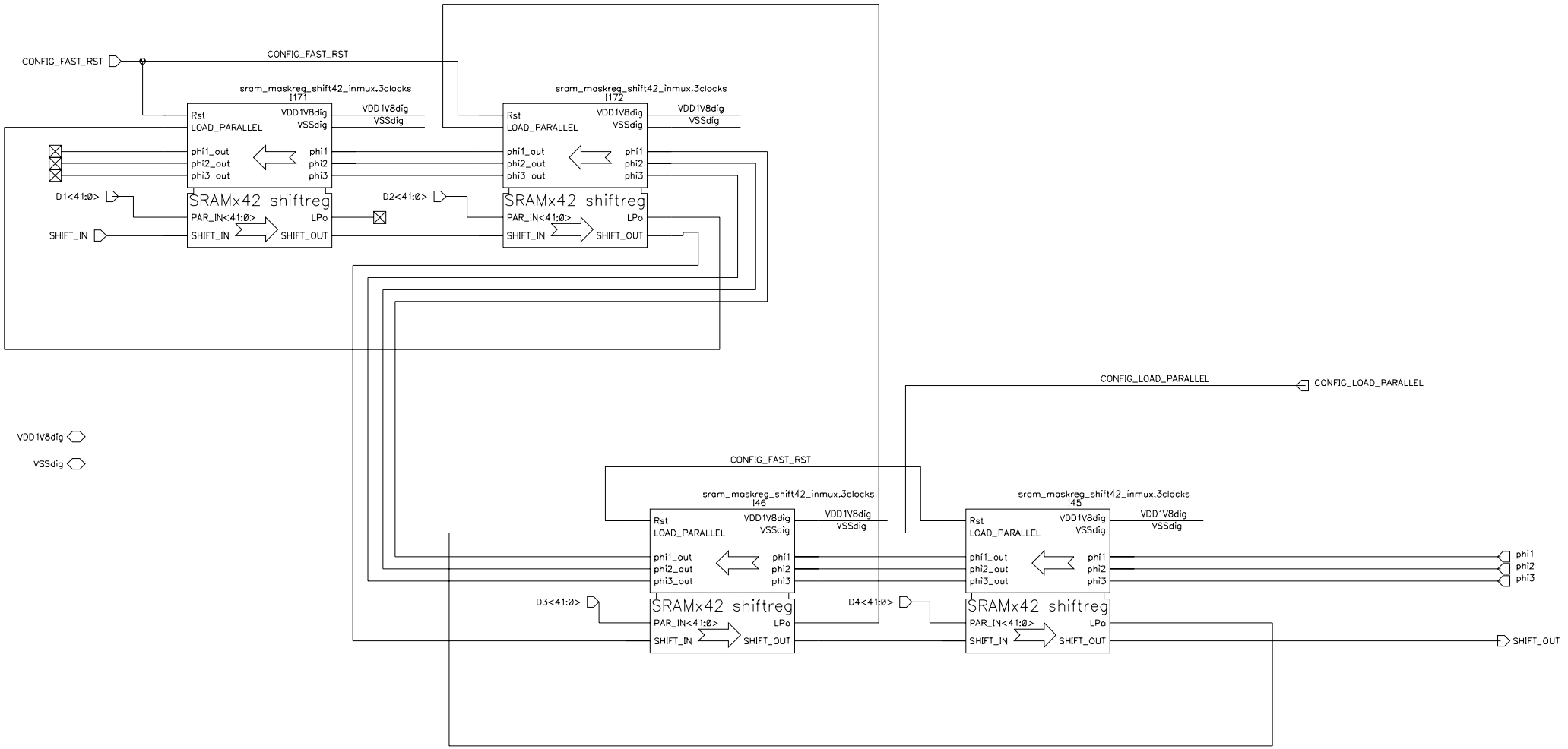
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	row_encoder_new
Last QA Review	
Last Changed	Jan 15 09:39:09 2007

VSSdig

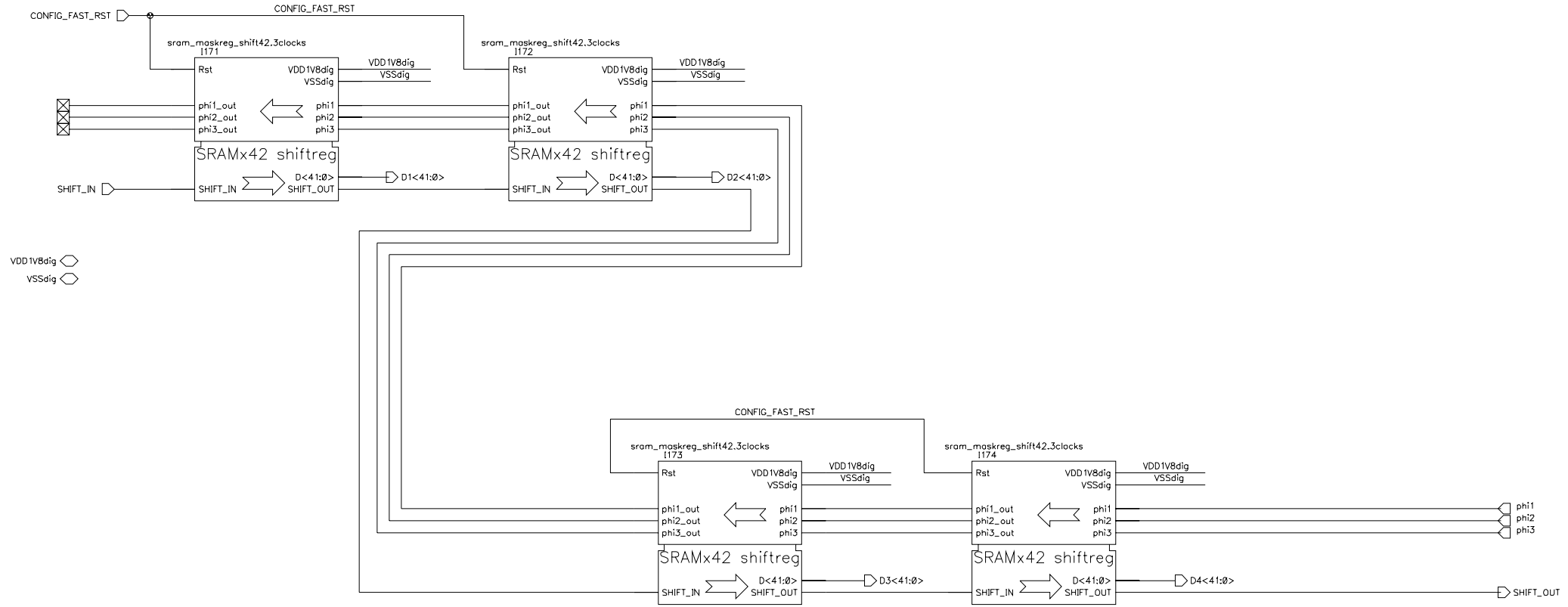


Tie OPT_NODE to either vdd
or gnd to effectively set
the address code that will
be read when RD is asserted

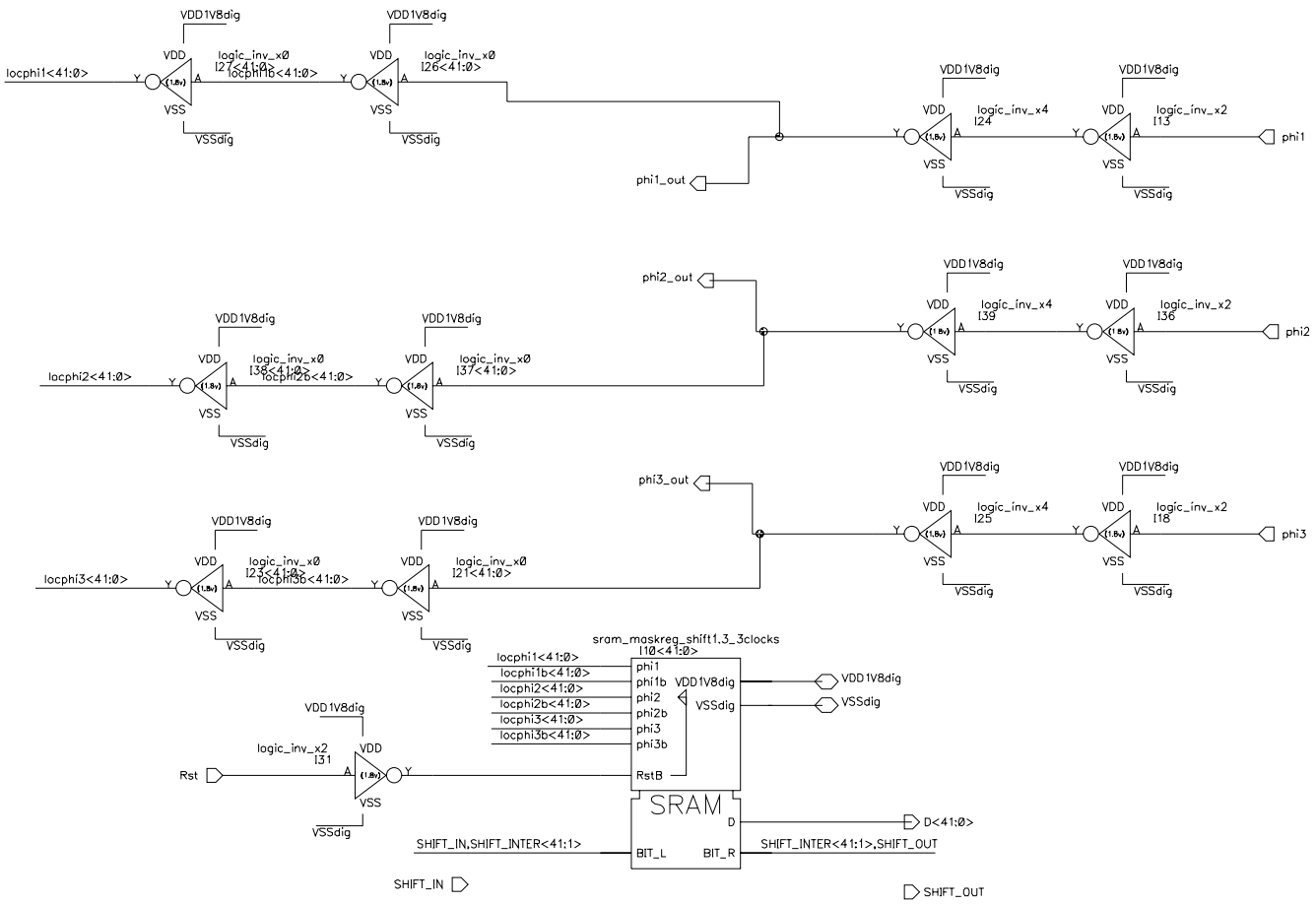
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	addrset_1bit
Last QA Review	
Last Changed	Jan 15 09:35:52 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	config_sr_bot_v1.1
Last QA Review	
Last Changed	Mar 19 13:07:17 2007

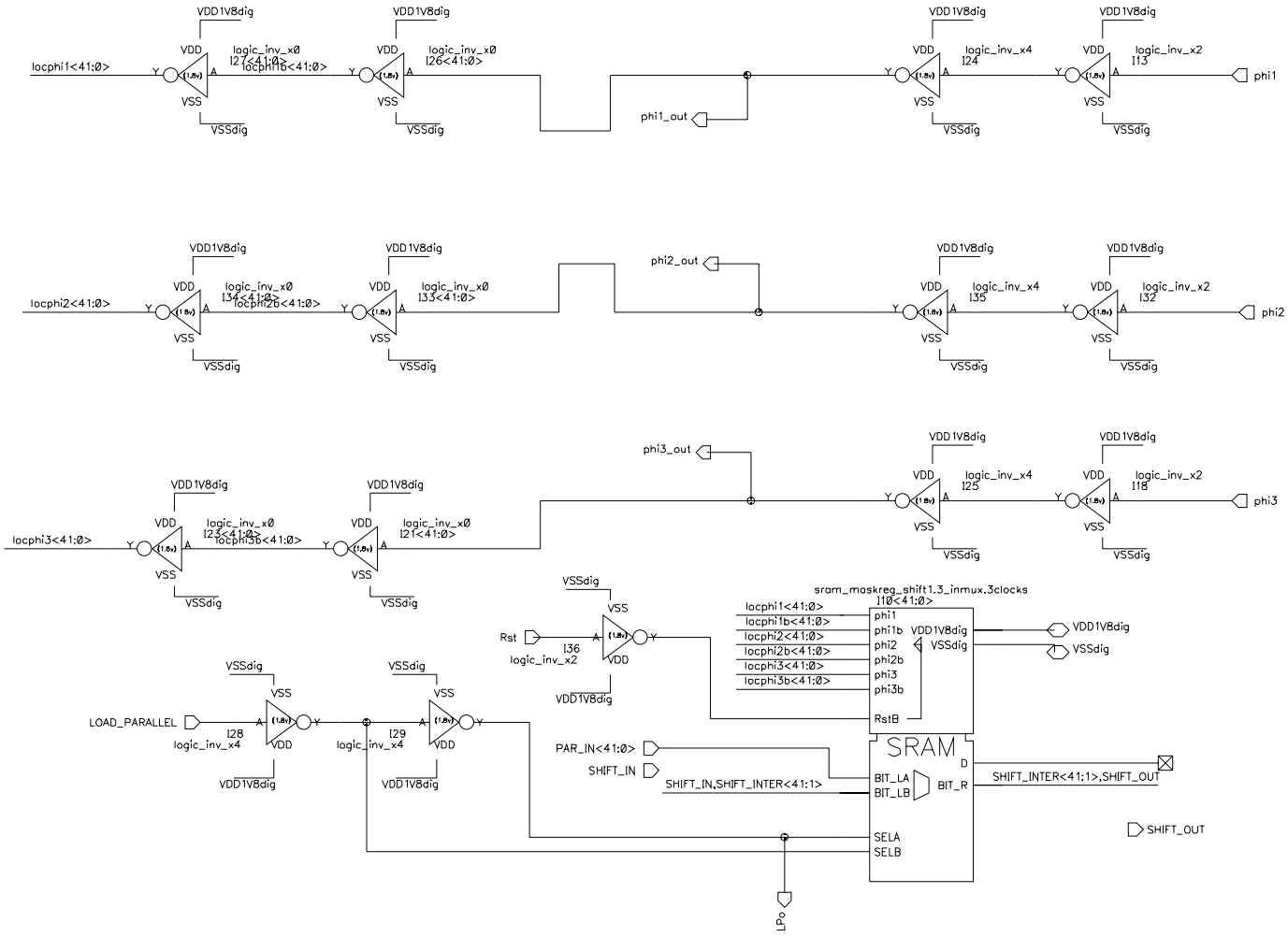


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	config_sr_top_v1.1
Last QA Review	
Last Changed	Mar 19 13:05:52 2007



Each cell has minimum size clock buffers to ensure clock integrity. 4x buffers drive the global clock signal for the length of the full 42 cells

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift42.3clocks
Last QA Review	
Last Changed	Jan 30 13:41:34 2007



LOAD_PARALLEL = 1 sets shift register inputs to point to the PAR_IN<41:0> inputs

LOAD_PARALLEL = 0 sets the shift register to internal serial mode (will shift its own data out)

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift42_inmux.3clocks
Last QA Review	
Last Changed	Mar 13 10:47:23 2007

Shiftreg Revision 1.3 with input multiplexing

> Two inputs can be selected for use as either serial/parallel input

POWER UP

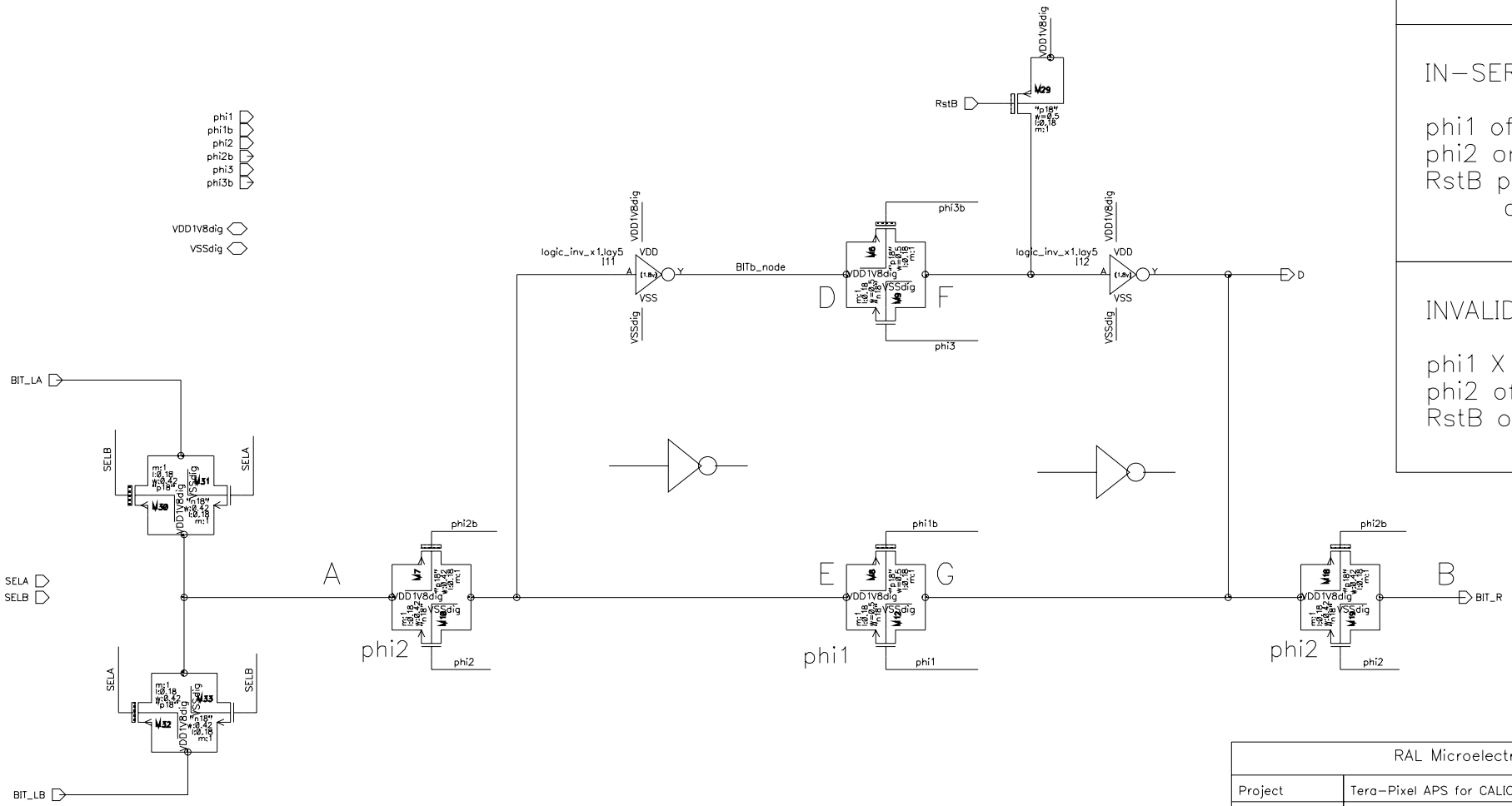
phi1 off
phi2 on
RstB on (low)

IN-SERVICE RESET

phi1 off
phi2 on
RstB pulsed on (low) during phi2

INVALID STATE

phi1 X
phi2 off (low)
RstB on (low)



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift1.3_inmux.3clocks
Last QA Review	
Last Changed	Mar 12 17:32:36 2007

New Shiftreg Revision 1.3 3CLOCKS!

> Added third clock for slow edge immunity

Layout inspired changes:

Reset transistor modified wider shorter
All TGs made width Ø.42

Resim & Check [ ]

POWER UP

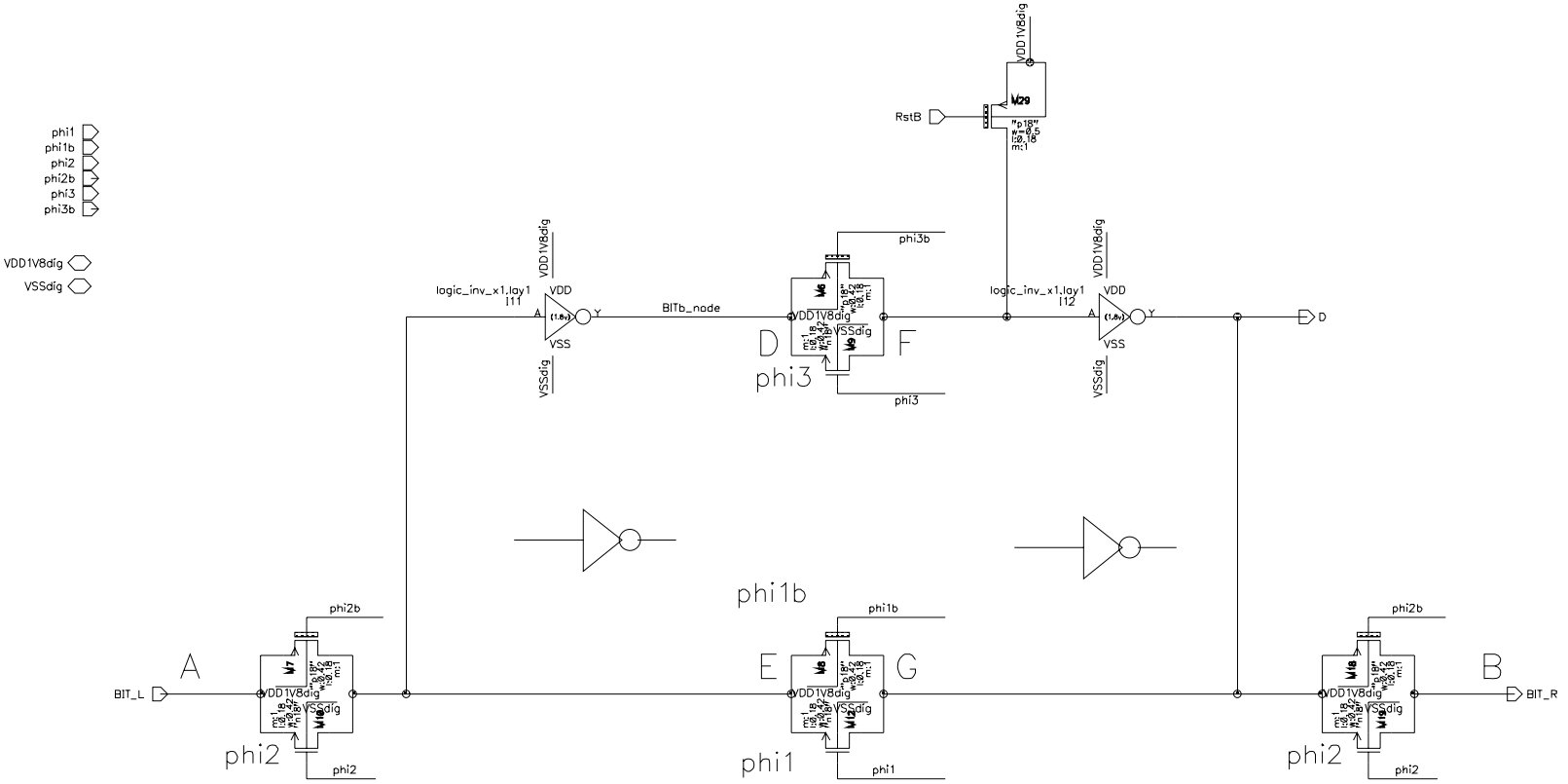
phi1 off
phi2 on
RstB on (low)

IN-SERVICE RESET

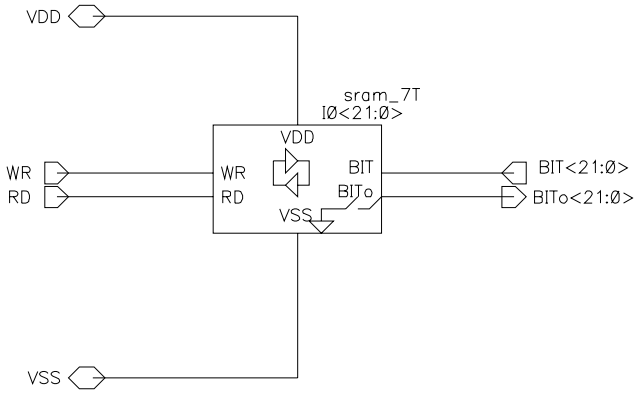
phi1 off
phi2 on
RstB pulsed on (low)
during phi2

INVALID STATE

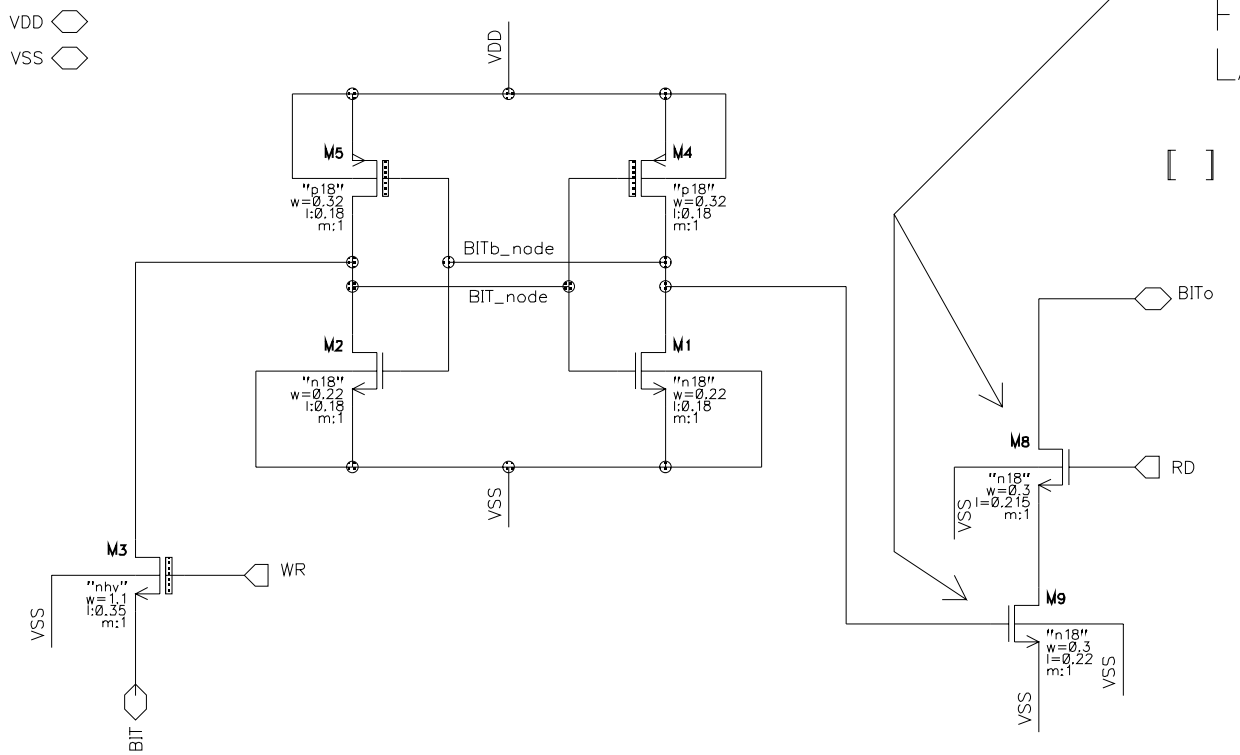
phi1 X
phi2 off (low)
RstB on (low)



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_maskreg_shift1.3_3clocks
Last QA Review	
Last Changed	Mar 12 11:20:58 2007



RAL Microelectronics Group		
Project	Tera-Pixel APS for CALICE	
Library Name	calice_circuits	
Block Name	sram_reg7.22	
Last QA Review		
Last Changed	Jan 2 16:08:03 2007	

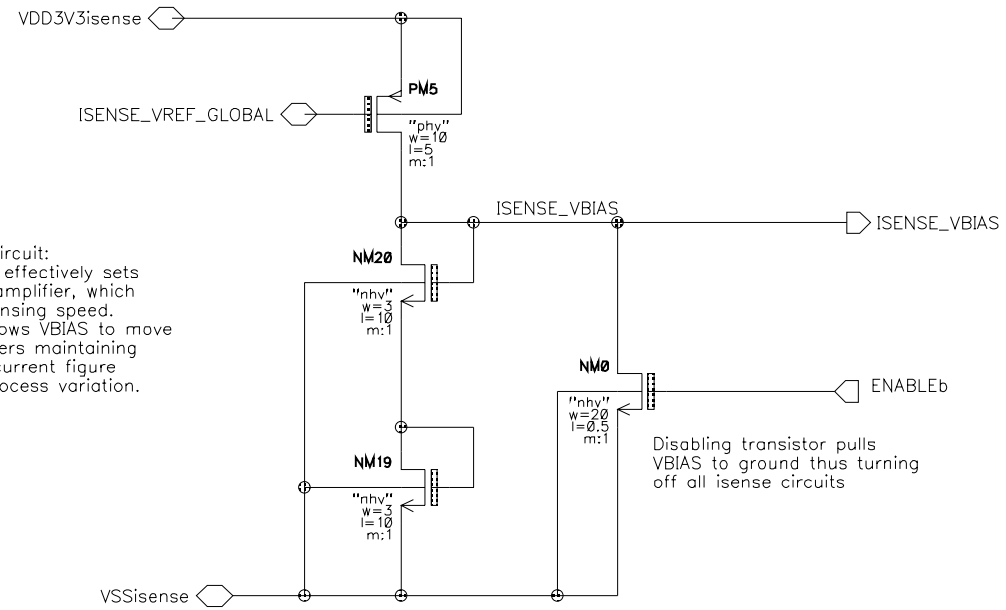


NB: TRANSISTOR LENGTH REDUCED Ø.3um TO Ø.22um FOR BETTER LAYOUT

[ ] RE-SIM CORNERS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_7T
Last QA Review	
Last Changed	Feb 19 18:38:06 2007

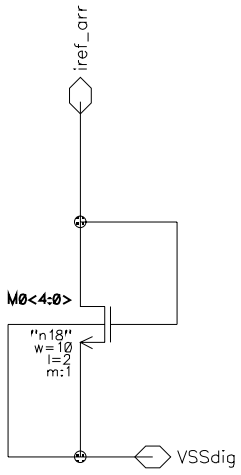
NOTE VDD MUST BE 3v3, hence hv transistors used



VBIAS generator circuit:
Current reference effectively sets current in sense amplifier, which effectively sets sensing speed.
Bias generator allows VBIAS to move with process corners maintaining approx constant current figure independant of process variation.

Disabling transistor pulls VBIAS to ground thus turning off all isense circuits

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_bias_v1.2
Last QA Review	
Last Changed	Mar 2 17:52:37 2007



5:1

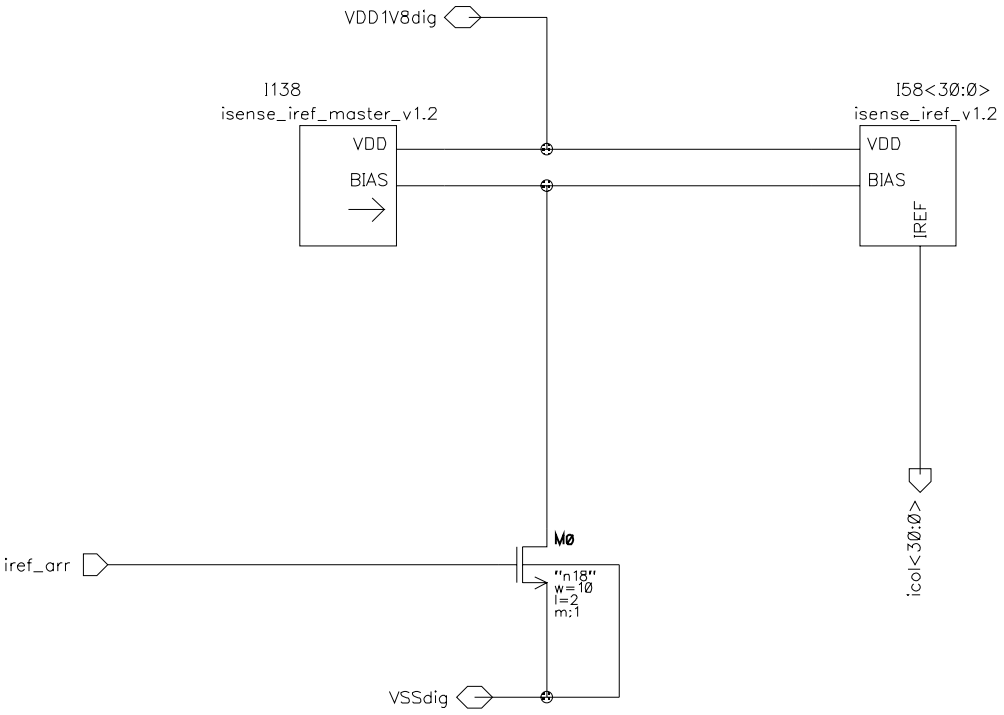
50uA typ

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_arr
Last QA Review	
Last Changed	Apr 10 09:08:45 2007

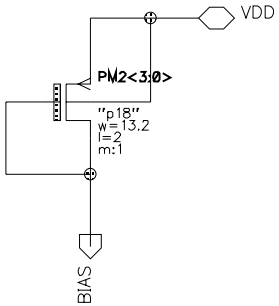
10uA typ

2.5uA typ

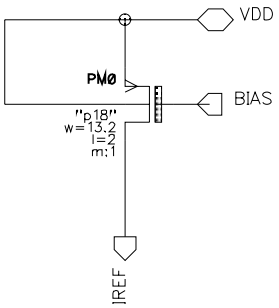
4:1



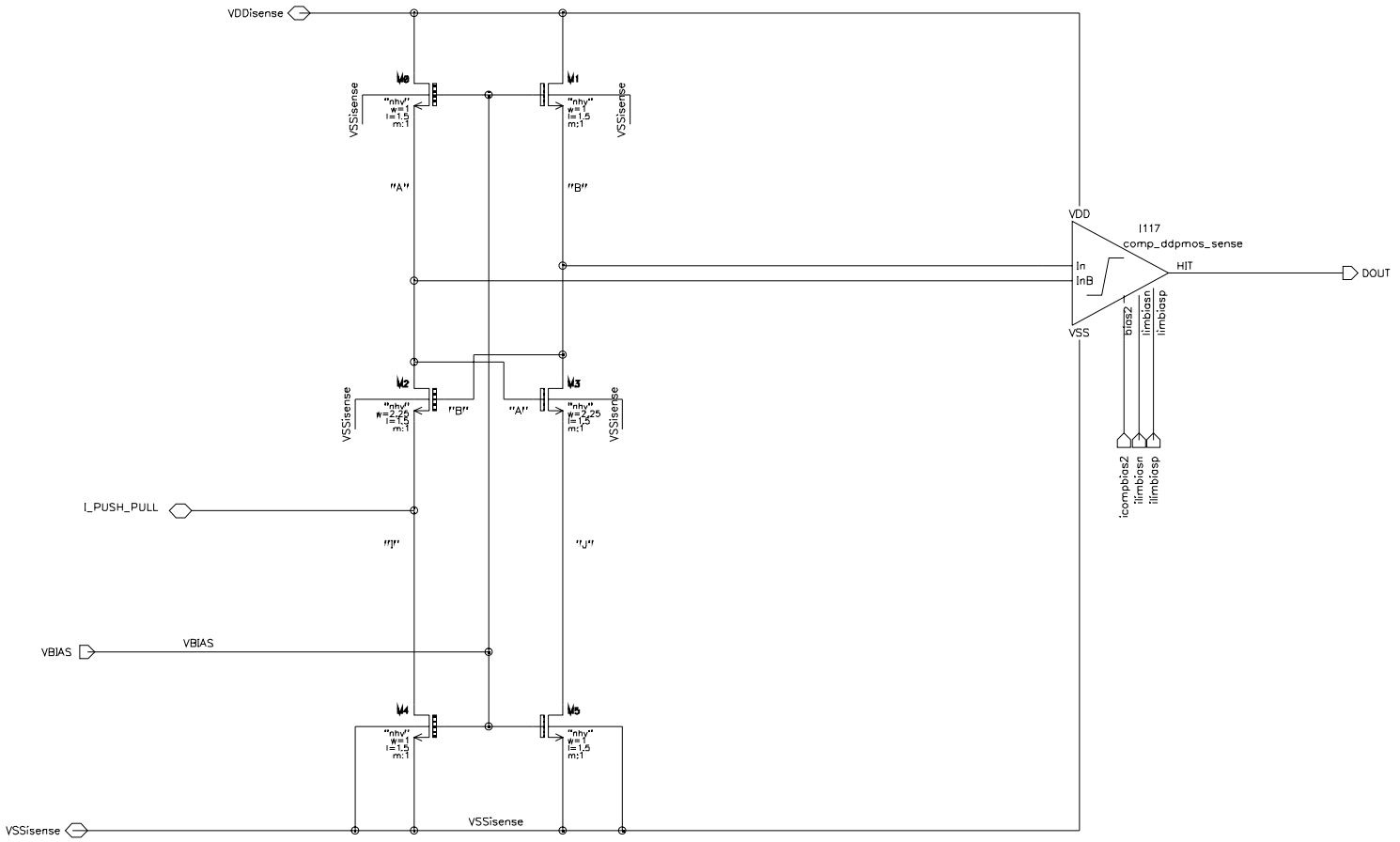
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_col
Last QA Review	
Last Changed	Mar 14 13:29:16 2007



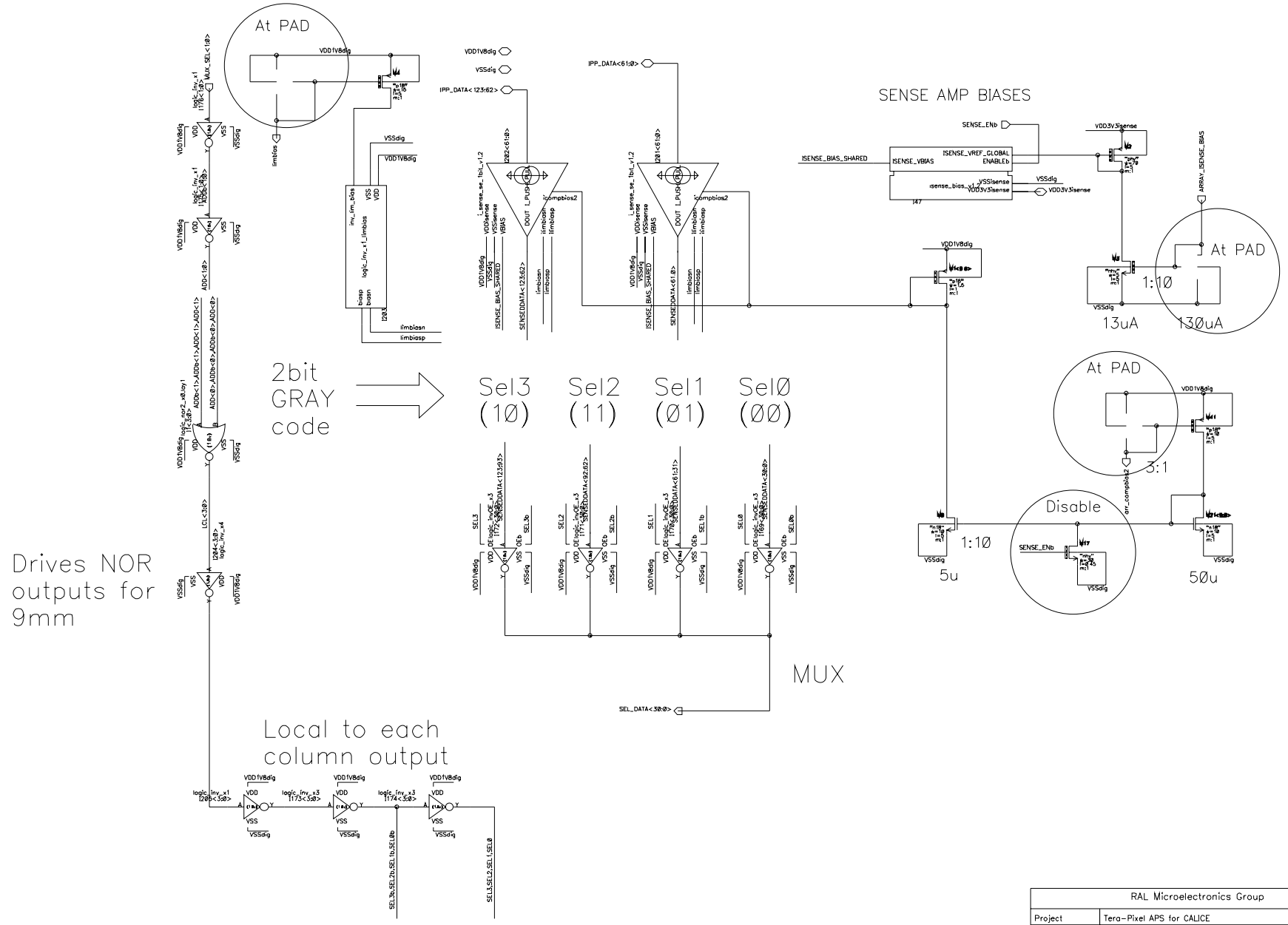
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_master_v1.2
Last QA Review	
Last Changed	Dec 14 11:49:02 2006



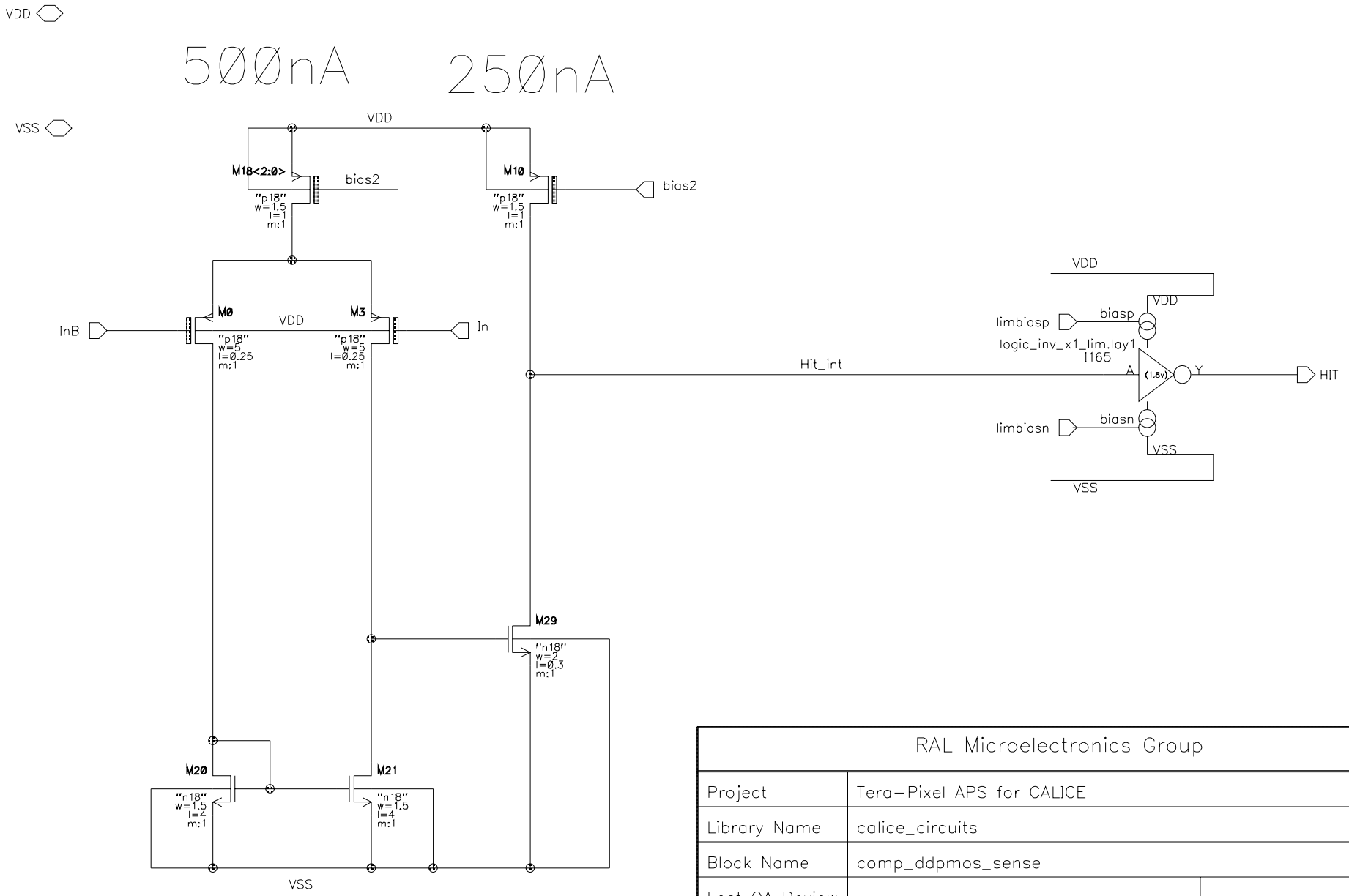
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	isense_iref_v1.2
Last QA Review	
Last Changed	Sep 29 10:33:57 2006



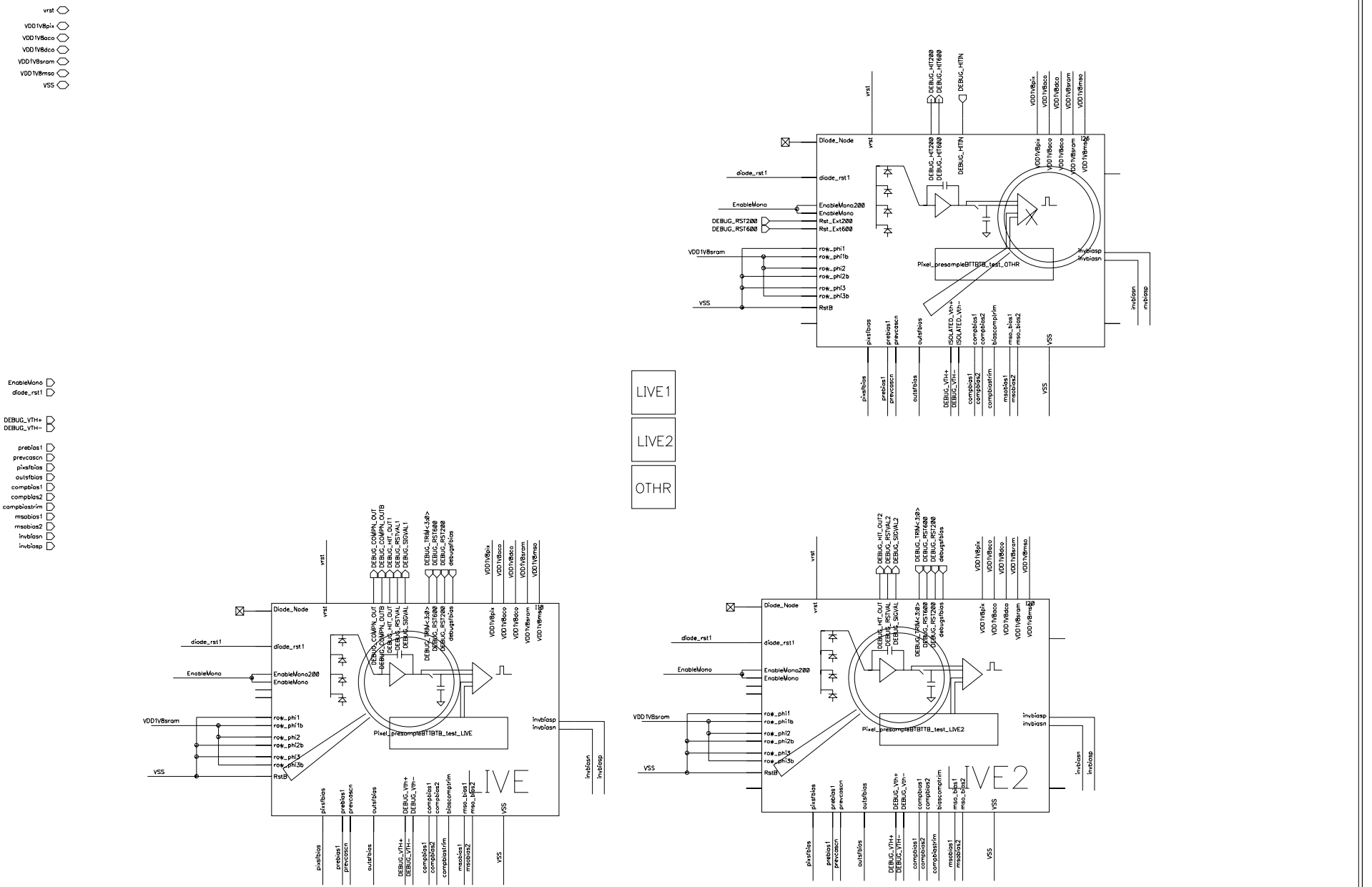
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	i_sense_se_1bit_v1.2
Last QA Review	
Last Changed	Mar 1 17:58:05 2007



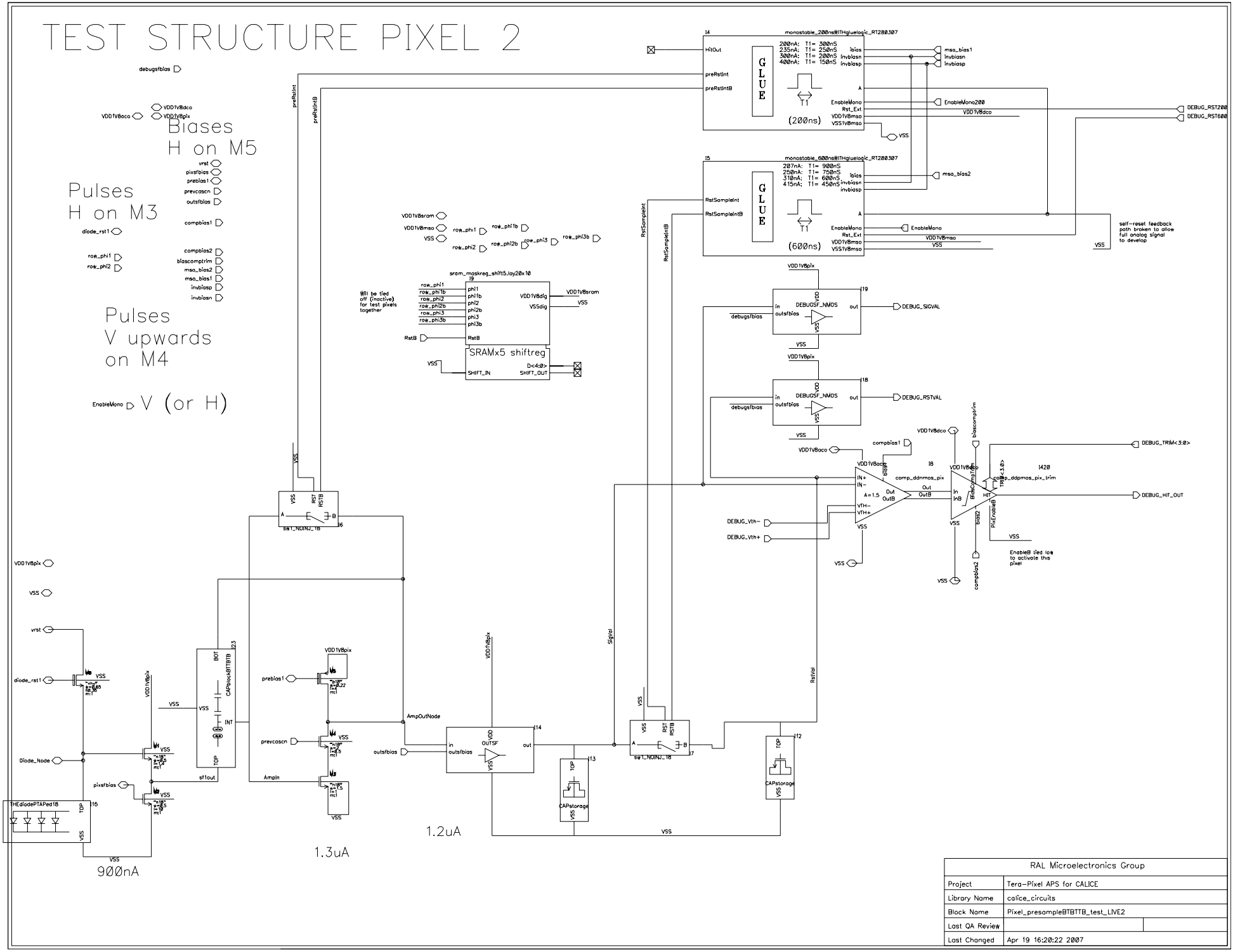
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sense_mux_v1.2
Last QA Review	
Last Changed	Mar 29 10:50:11 2007



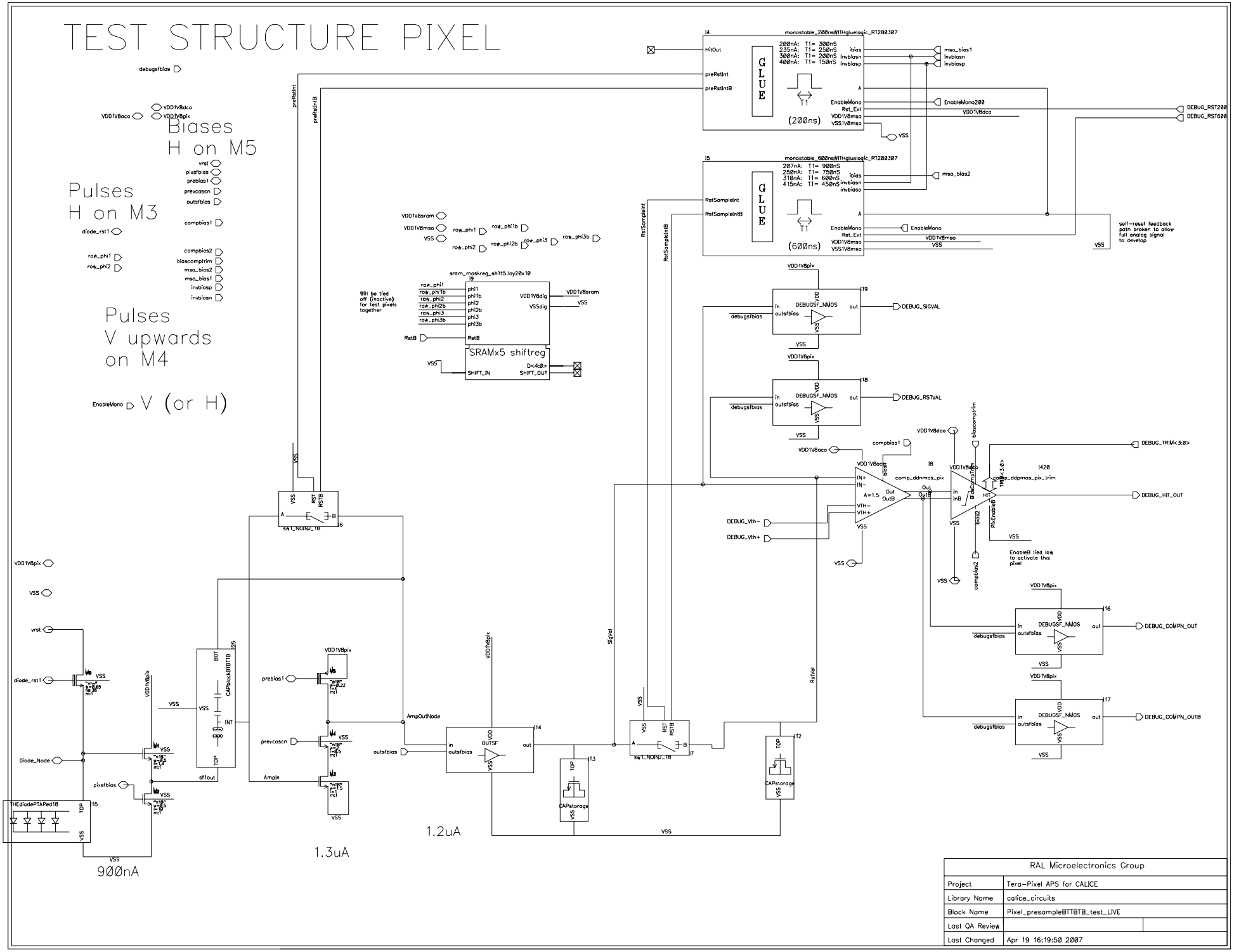
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddpmos_sense
Last QA Review	
Last Changed	Mar 1 17:57:36 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampleBTTBTB_test_setof3
Last QA Review	
Last Changed	Apr 21 14:45:44 2007

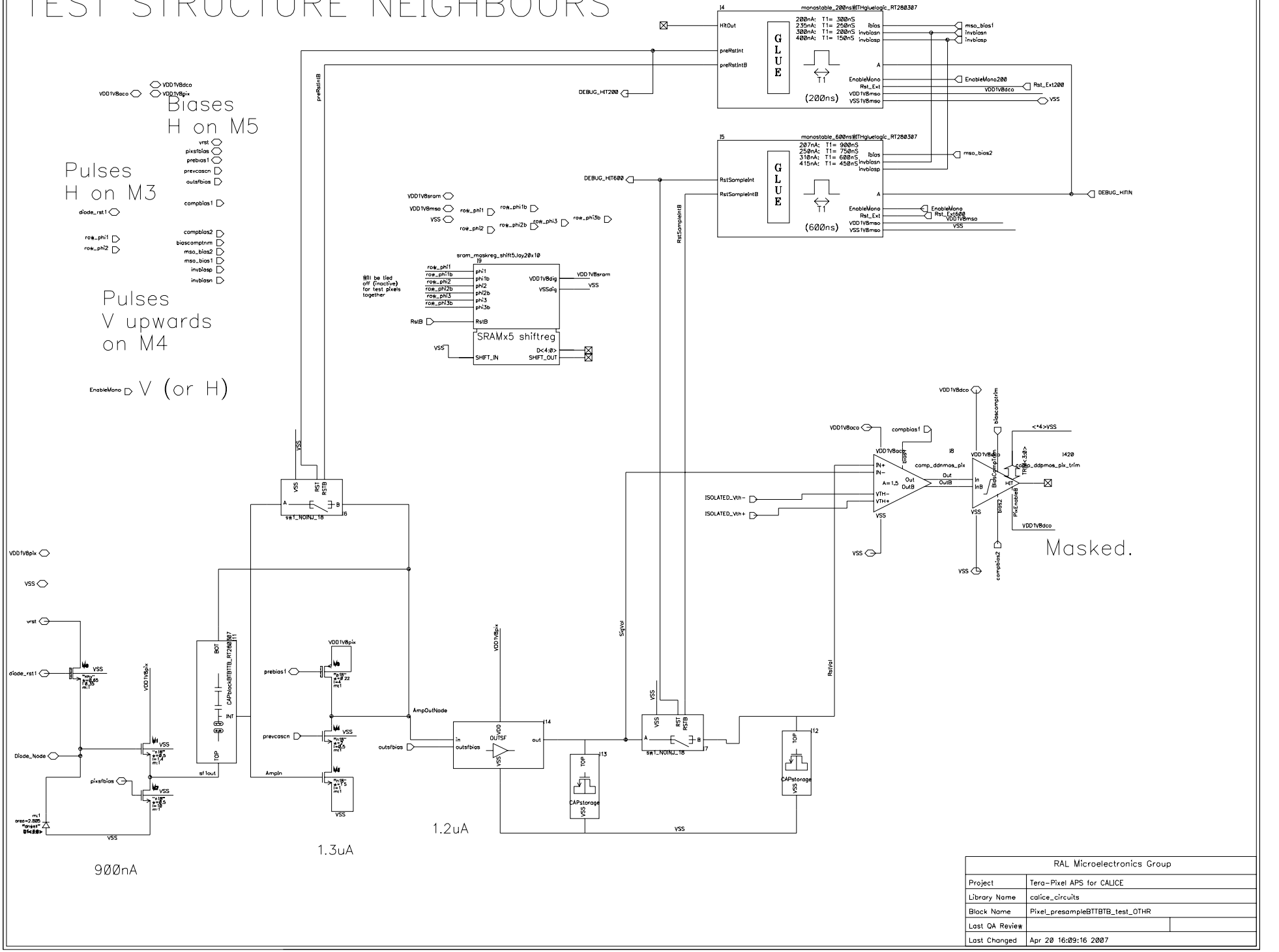


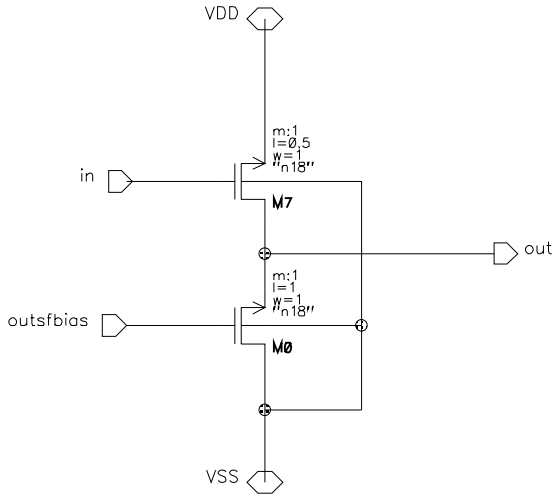
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampleBTBTTB_test_LIVE2
Last QA Review	
Last Changed	Apr 19 16:20:22 2007



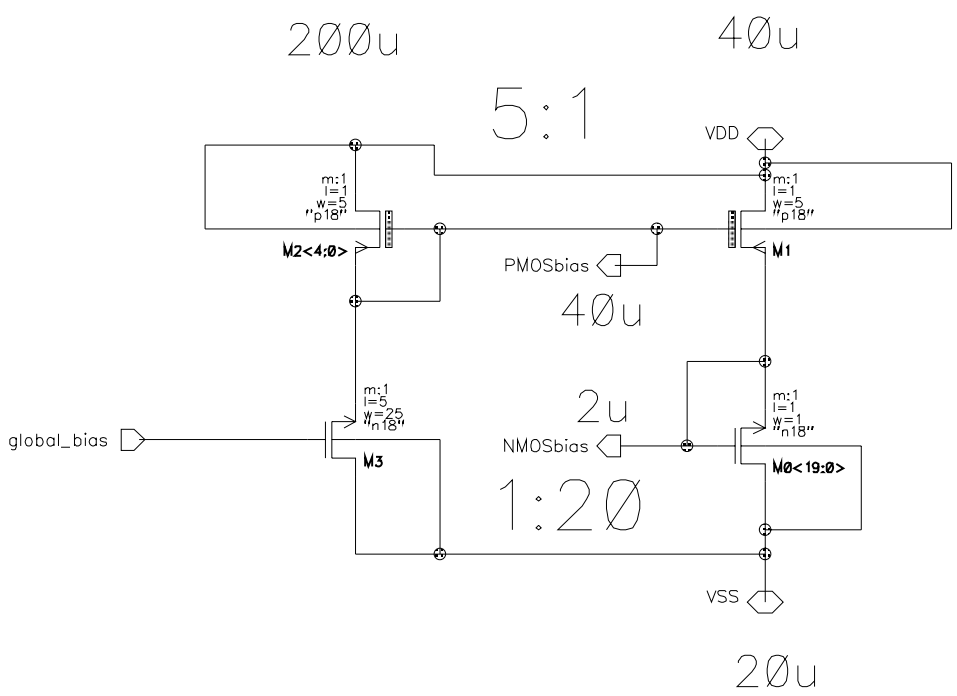
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	Pixel_presampleBTTBTB_test_LIVE
Last QA Review	
Last Changed	Apr 19 16:19:50 2007

TEST STRUCTURE NEIGHBOURS





RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_NMOS
Last QA Review	
Last Changed	Jul 3 13:42:33 2007



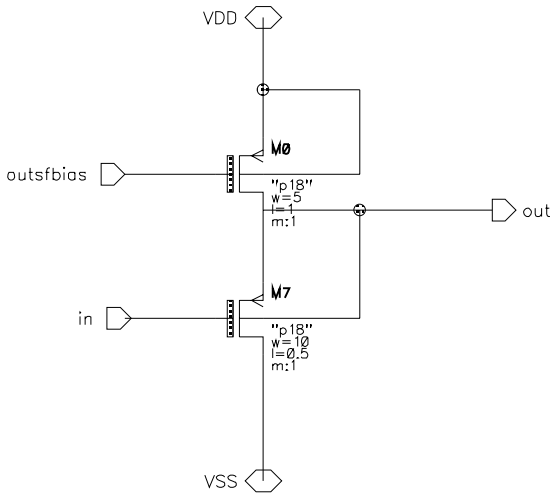
PMOS bias is 20x NMOS bias

Note: 28-6-07

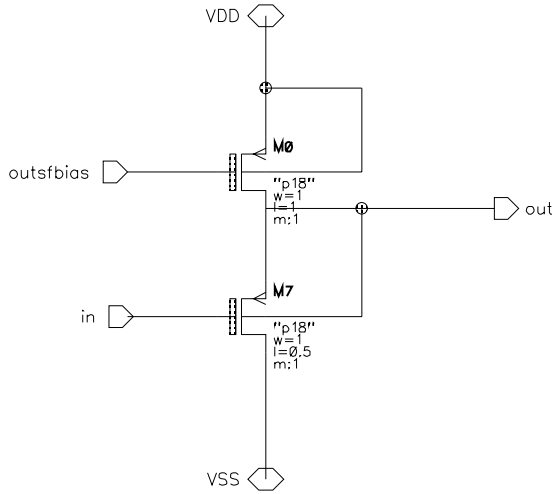
Transistor symbols upside-down (noticed post-submission, hence not changed in this version of schematic)

No effect to operation. but should be corrected if this cell is used in ASIC2.

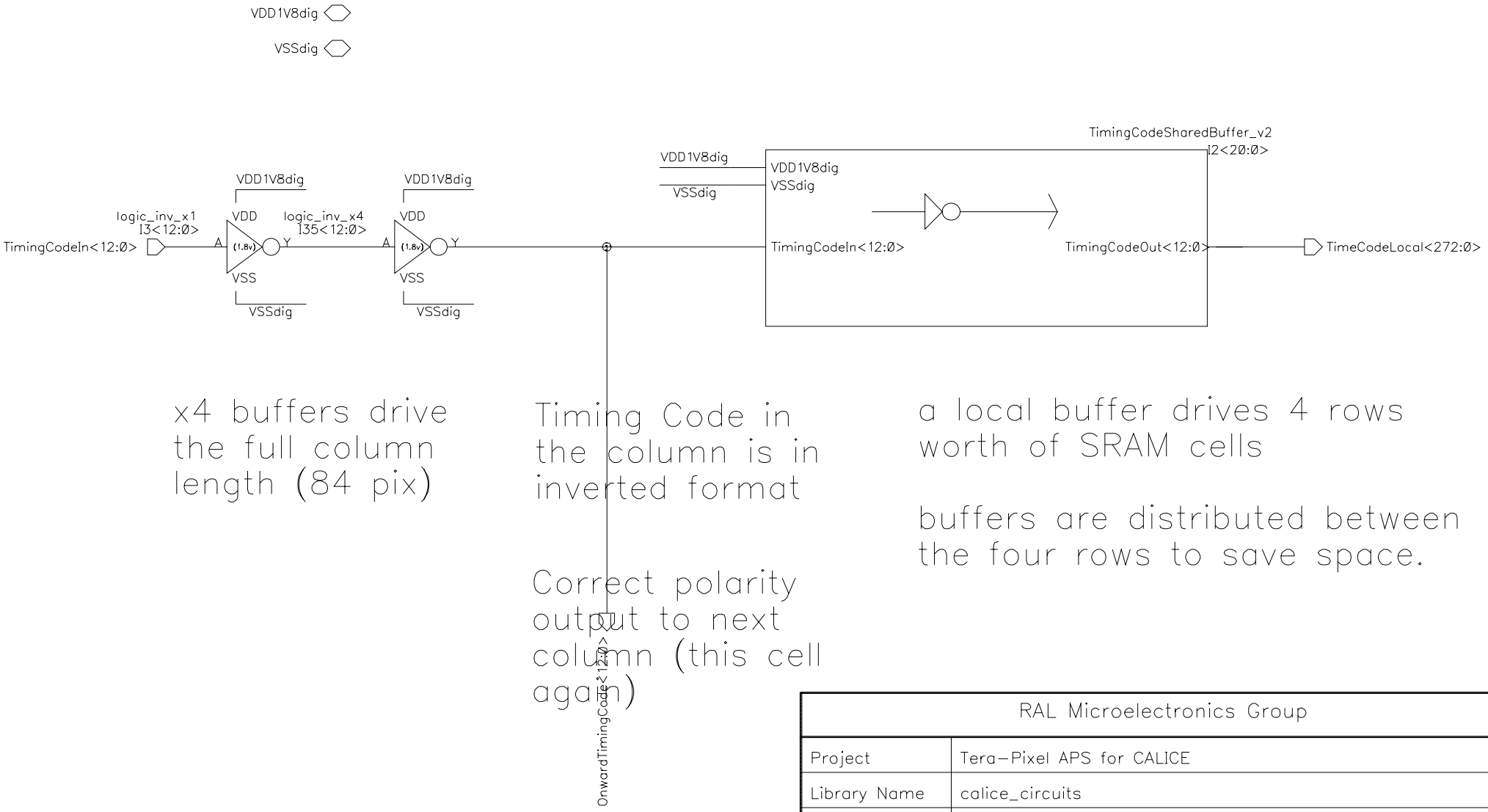
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_NMOS_BIAS
Last QA Review	
Last Changed	Jun 28 09:06:56 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	DEBUGSF_PMOS
Last QA Review	
Last Changed	Jul 3 13:42:59 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	OUTSF
Last QA Review	
Last Changed	Jun 27 11:54:06 2007



x4 buffers drive the full column length (84 pix)

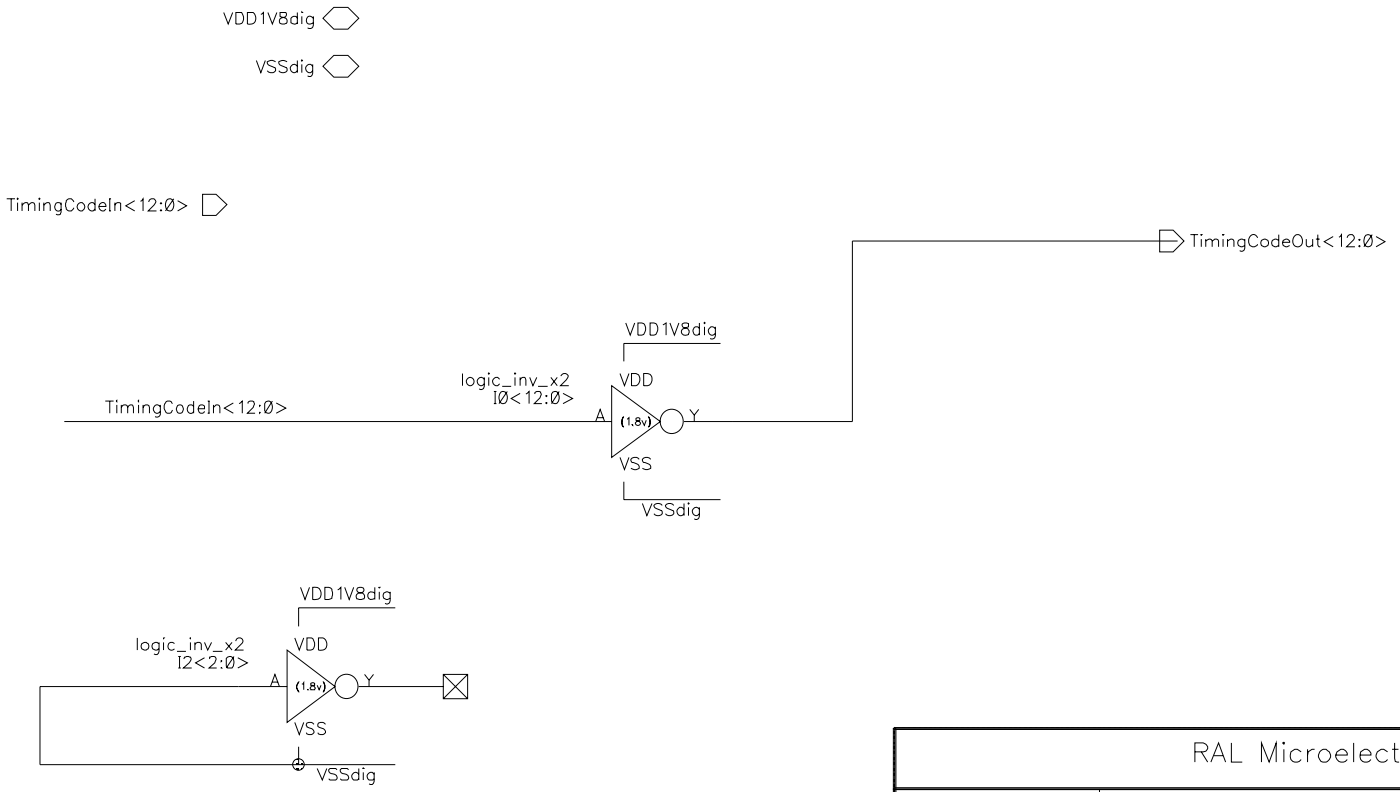
Timing Code in the column is in inverted format

Correct polarity output to next column (this cell again)

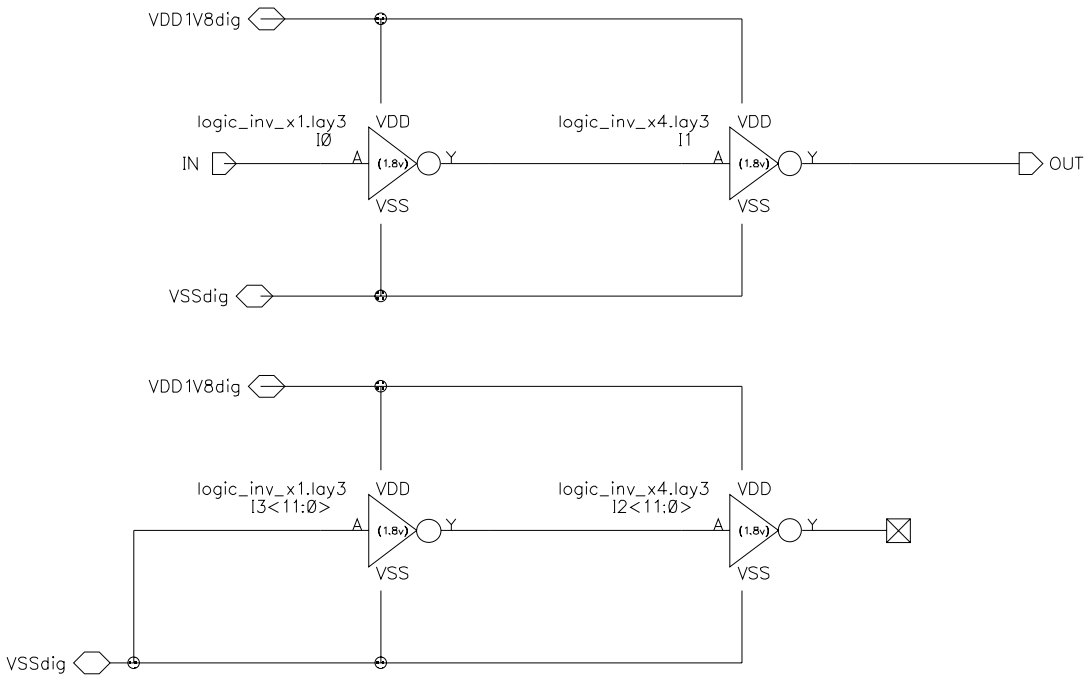
a local buffer drives 4 rows worth of SRAM cells

buffers are distributed between the four rows to save space.

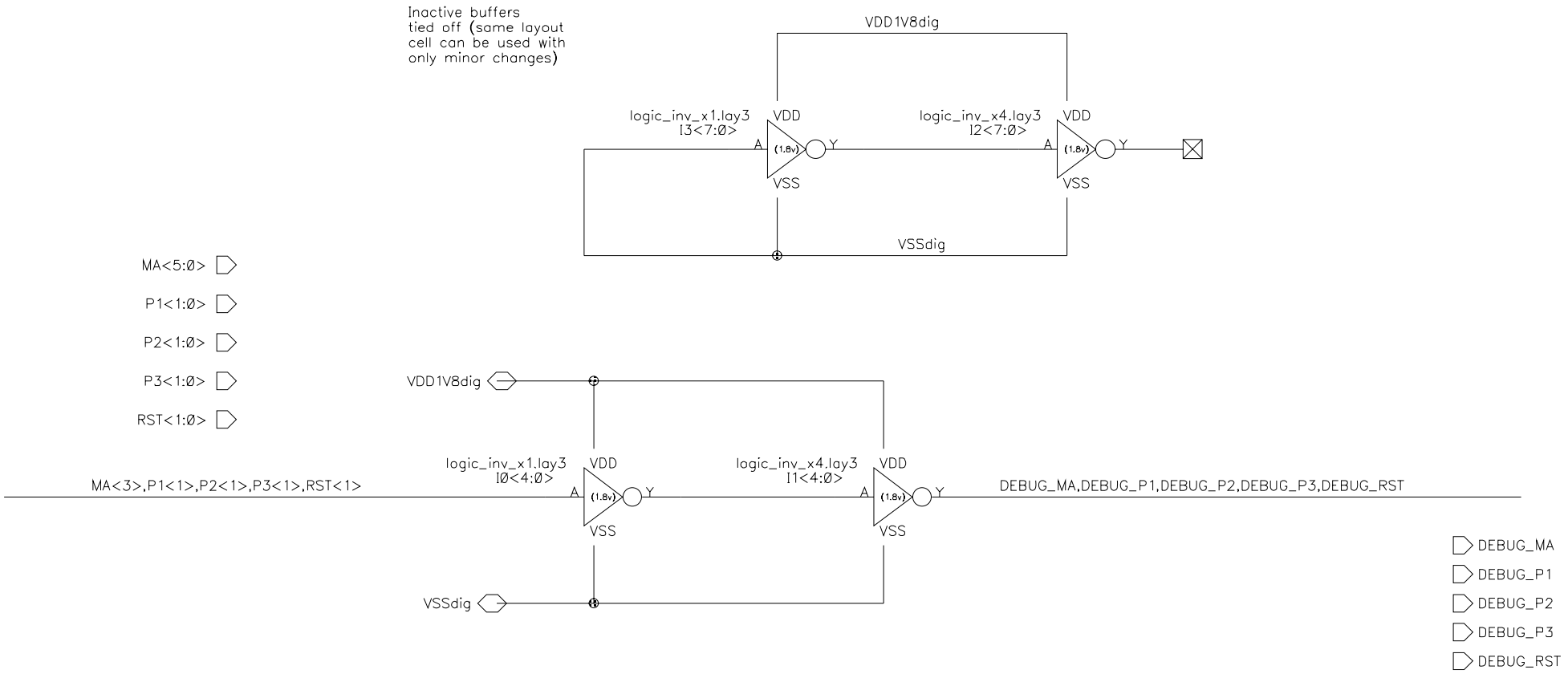
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeDistribution_v2
Last QA Review	
Last Changed	Mar 5 16:22:47 2007



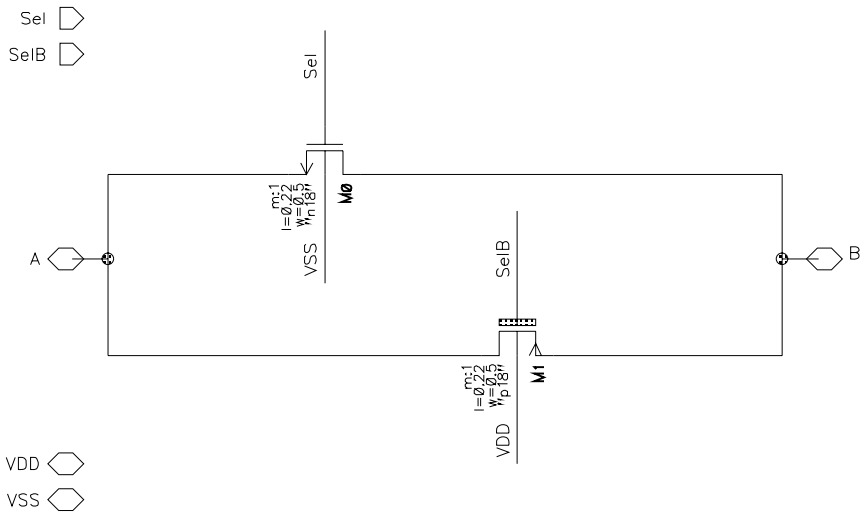
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	TimingCodeSharedBuffer_v2
Last QA Review	
Last Changed	Mar 5 11:36:51 2007



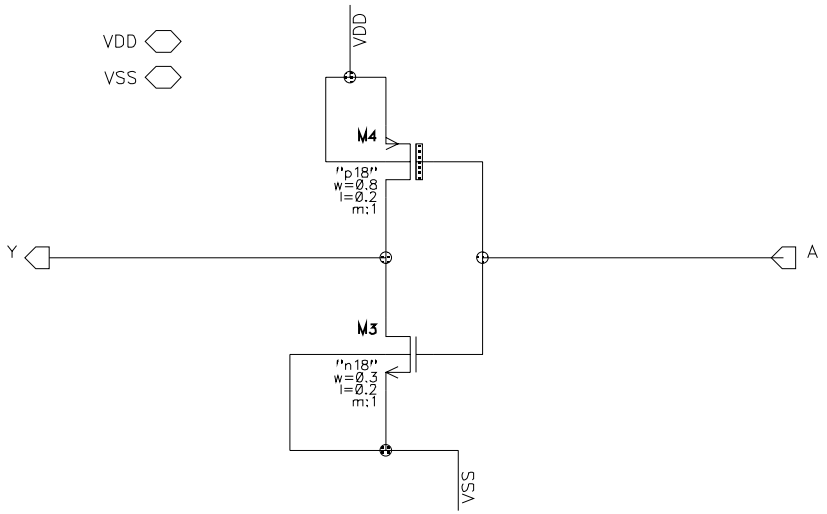
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sram_rpt_buffers_DN_debug
Last QA Review	
Last Changed	Jul 3 13:43:19 2007



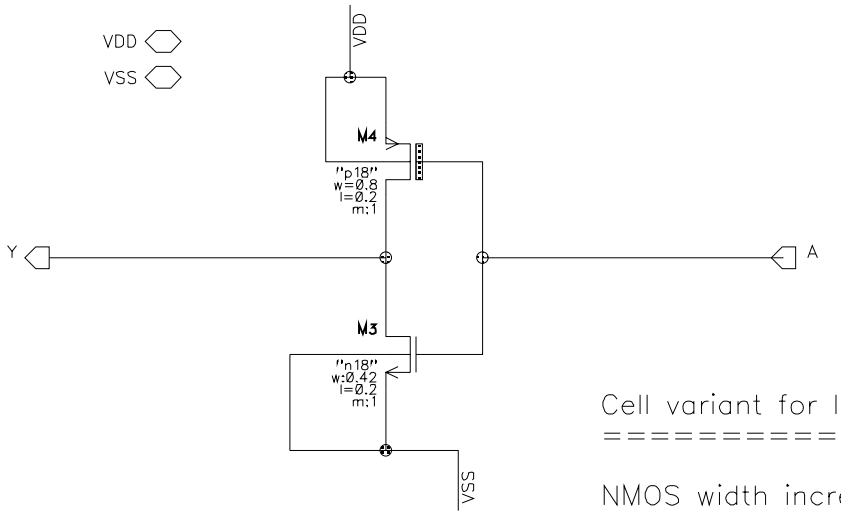
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_rpt_buffers_debug
Last QA Review	
Last Changed	Jul 3 13:37:44 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sw1_18
Last QA Review	
Last Changed	Sep 28 11:41:21 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x0
Last QA Review	
Last Changed	Sep 28 11:41:11 2006

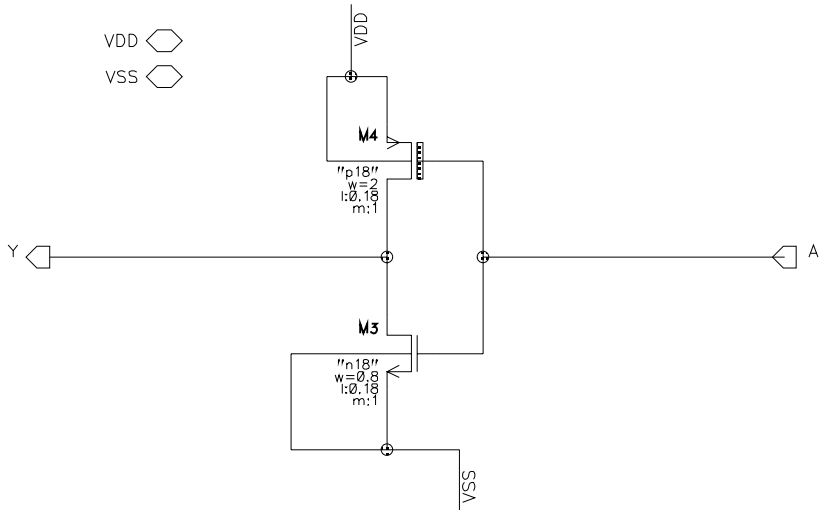


Cell variant for layout ".lay1"

==========

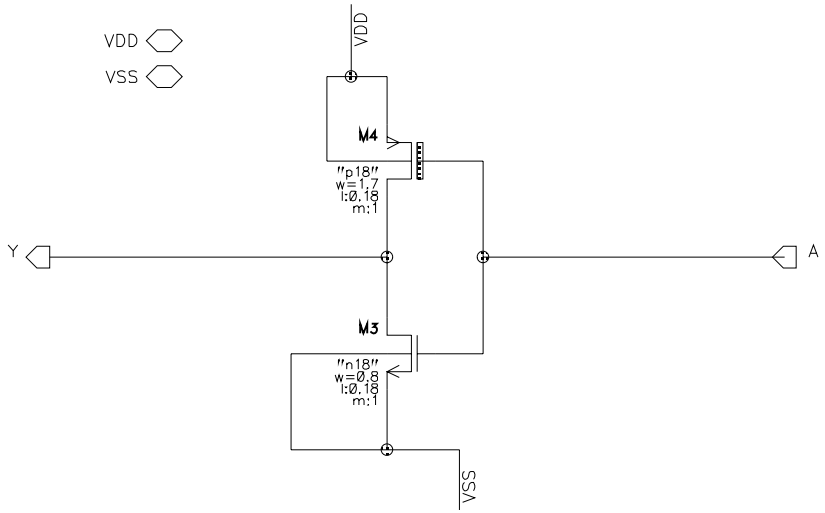
NMOS width increased from Ø.3 to Ø.42um

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_xØ.lay1
Last QA Review	
Last Changed	Jan 11 15:41:Ø7 2Ø07

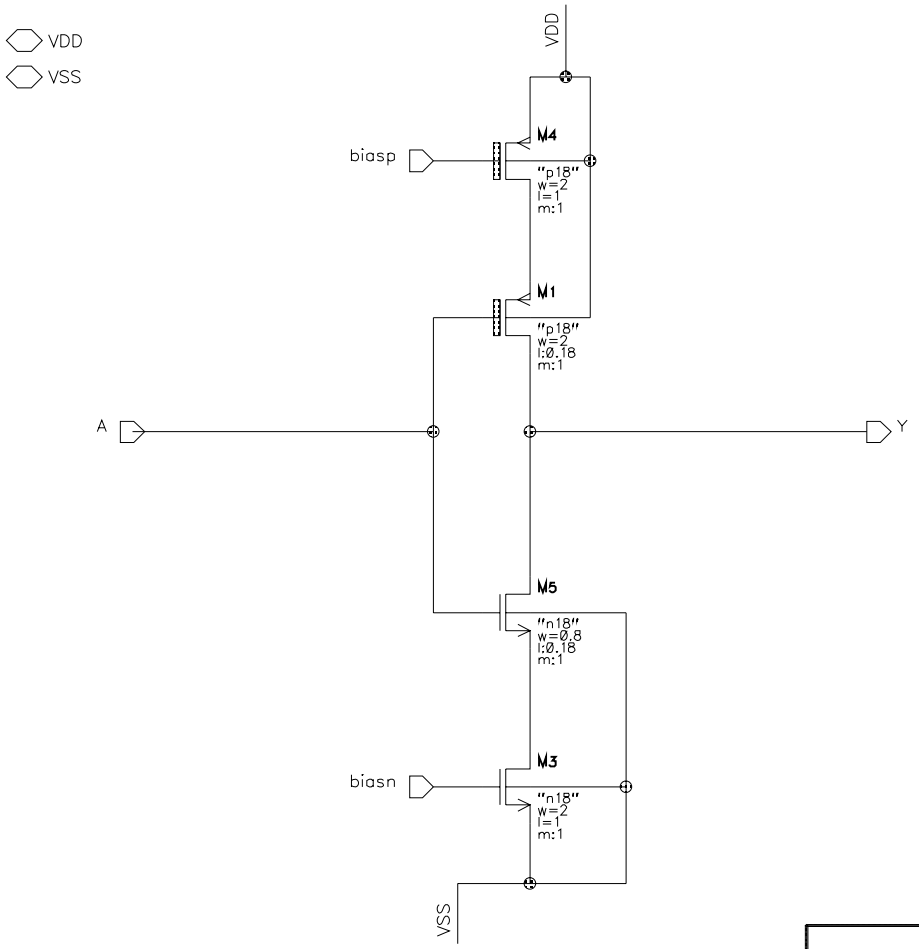


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

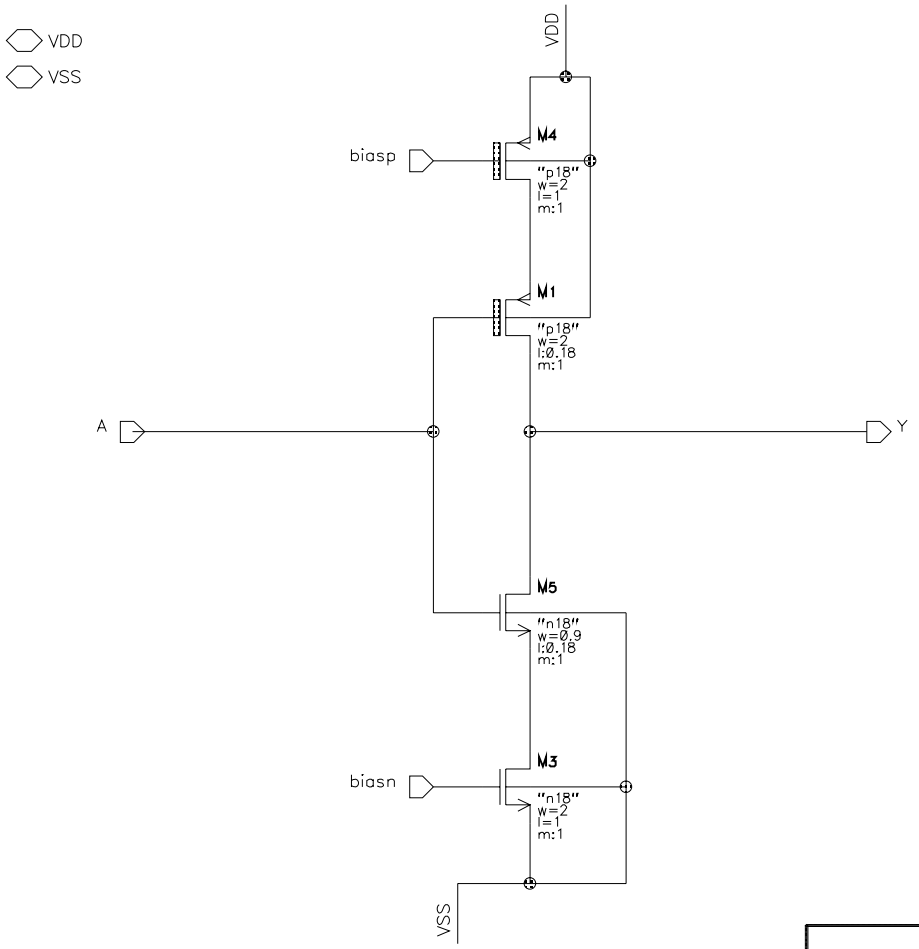
PMOS width reduced from 2um to 1.7um to aid efficient SRAM layout



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1.lay1
Last QA Review	
Last Changed	Feb 9 10:48:31 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_lim
Last QA Review	
Last Changed	Jan 22 16:24:31 2007

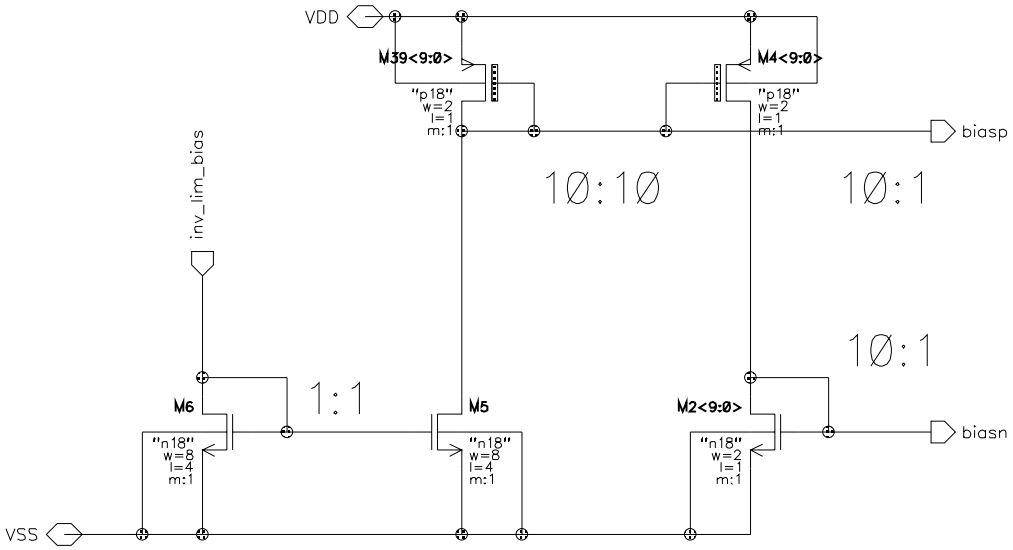


Layout variant 1

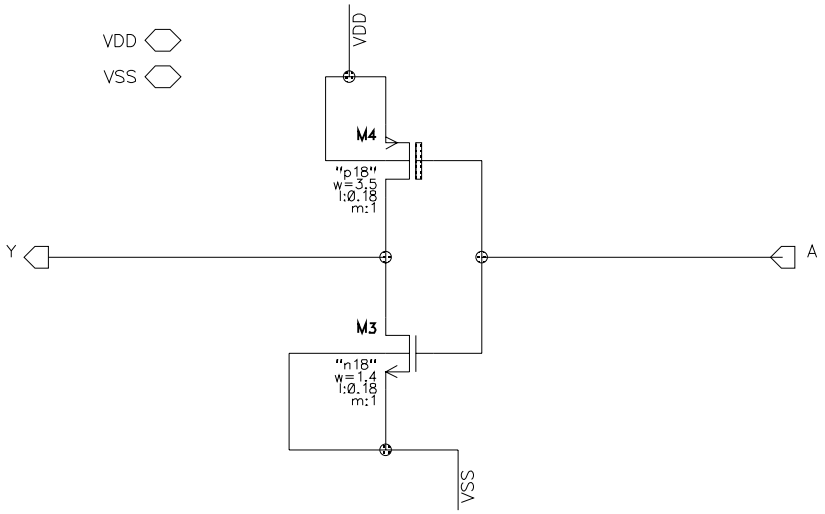
==========

NMOS width increased from 0.8 to 0.9 so there are two contacts in the pcell (preferred for yield)

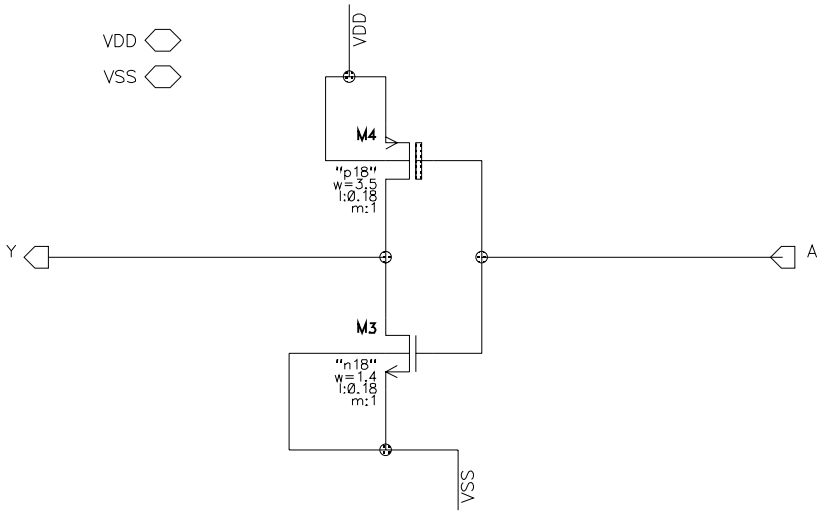
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_lim.lay1
Last QA Review	
Last Changed	Feb 20 17:08:47 2007



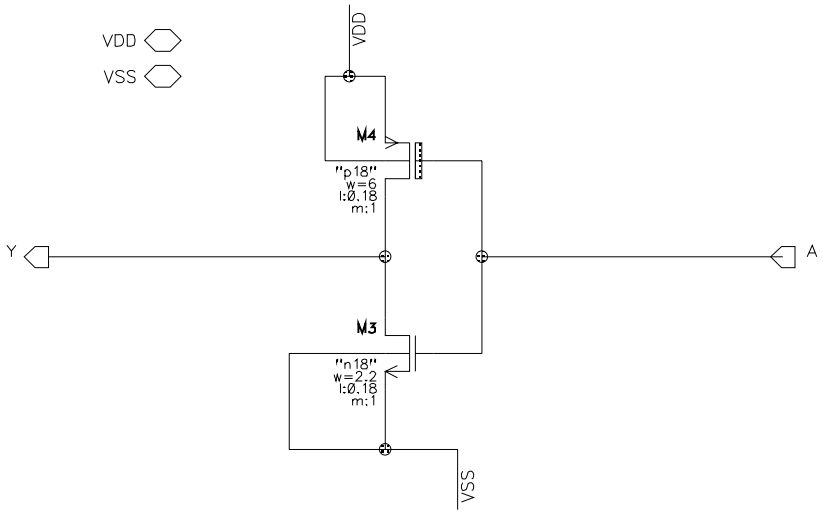
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1_limbias
Last QA Review	
Last Changed	Mar 3 13:08:07 2007



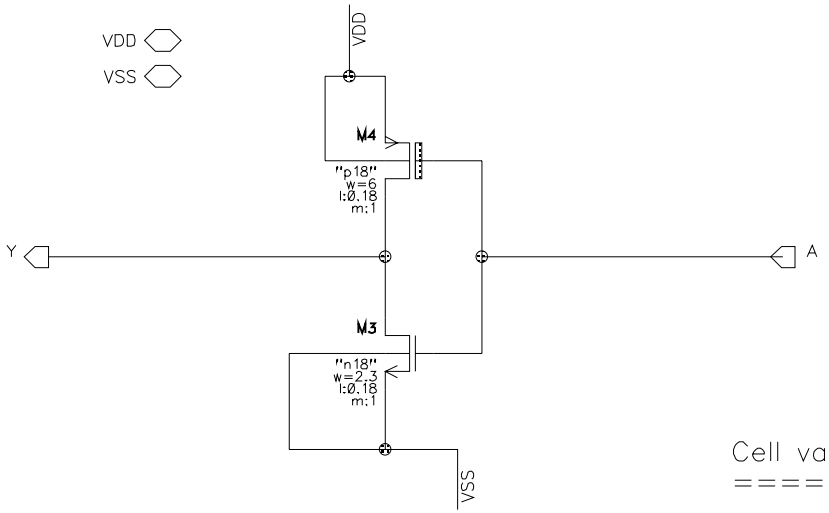
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2
Last QA Review	
Last Changed	Sep 28 11:45:54 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x2.lay3
Last QA Review	
Last Changed	Sep 28 11:45:54 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3
Last QA Review	
Last Changed	Sep 28 11:42:15 2006

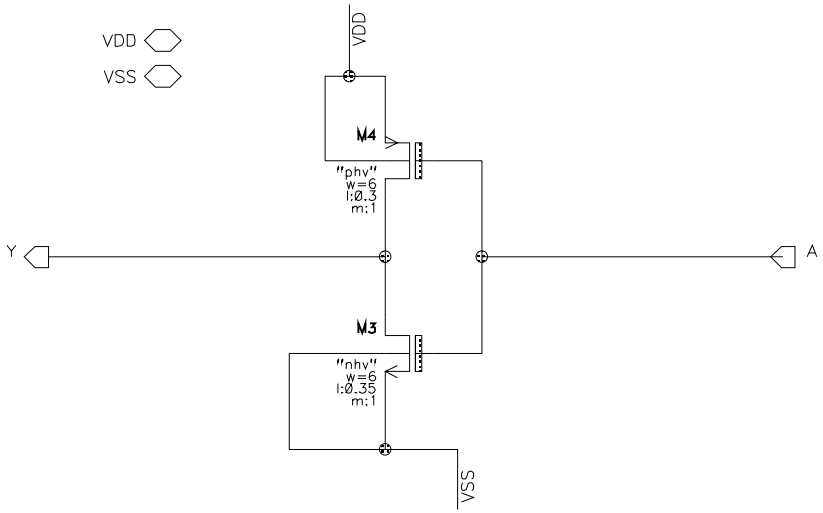


Cell variant for layout ".lay1"

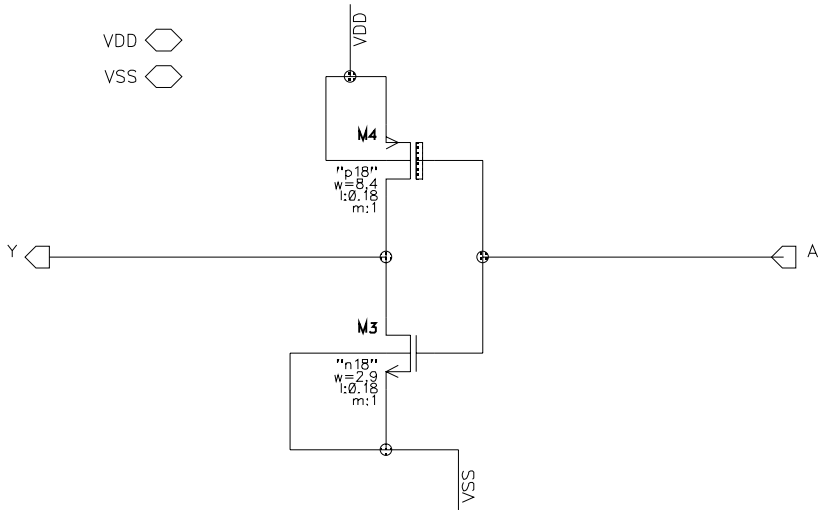
==========

NMOS width increased from 2.2 to 2.3

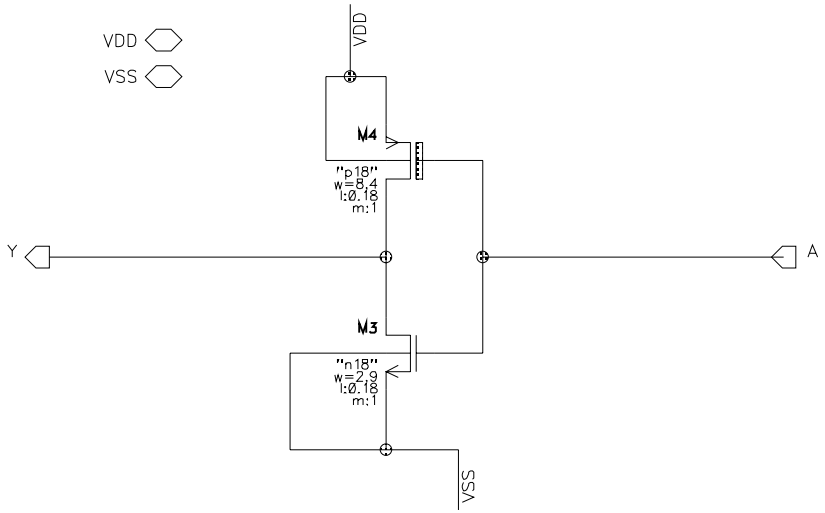
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3.lay1
Last QA Review	
Last Changed	Jan 10 14:27:47 2007



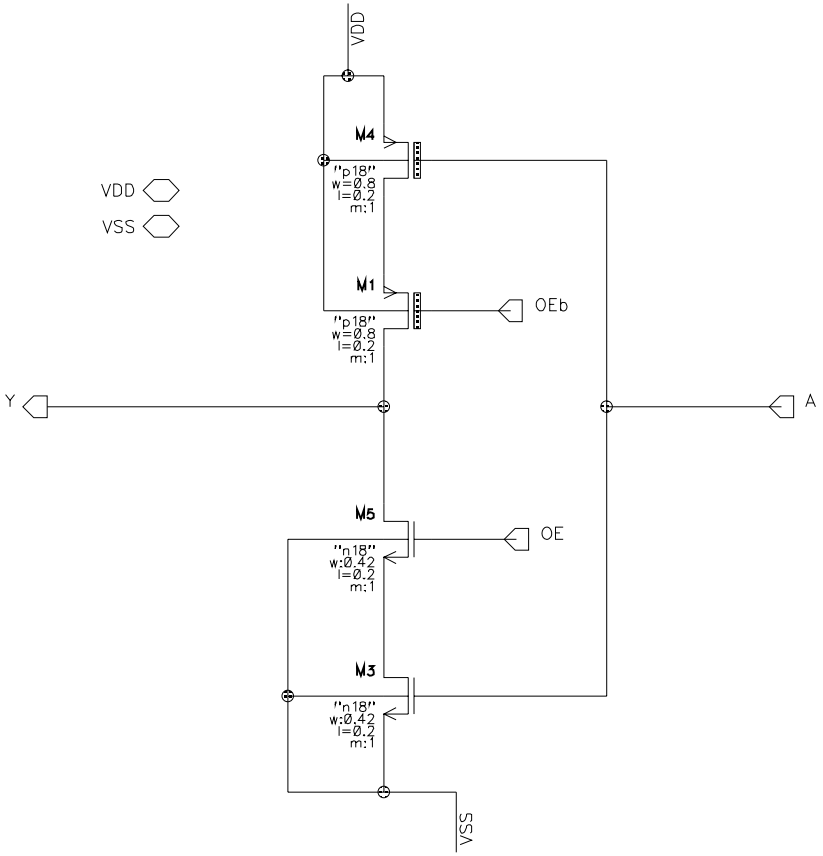
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x3_hv
Last QA Review	
Last Changed	Sep 29 15:18:48 2006



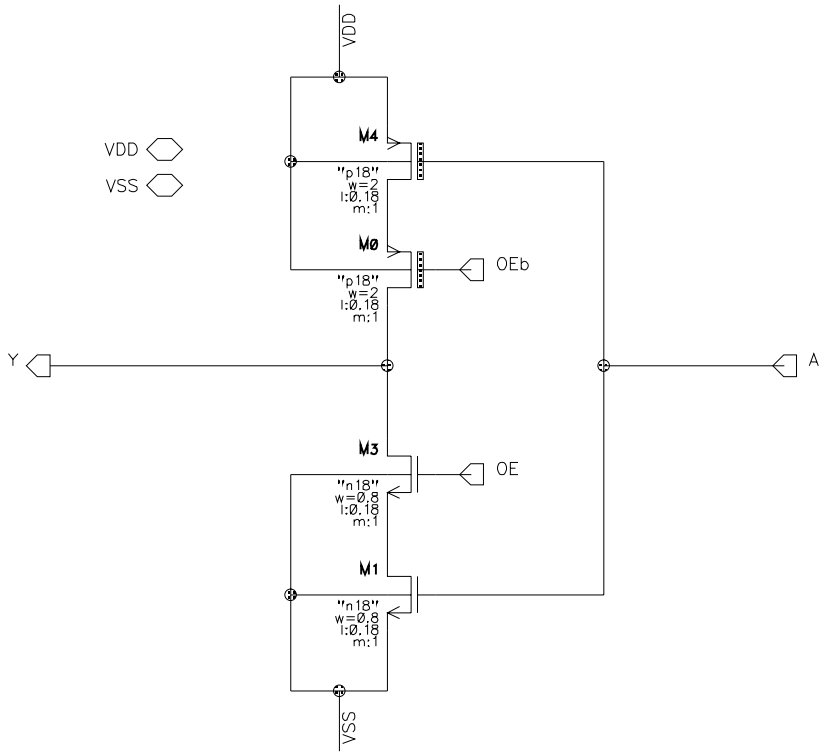
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4
Last QA Review	
Last Changed	Sep 28 11:42:24 2006



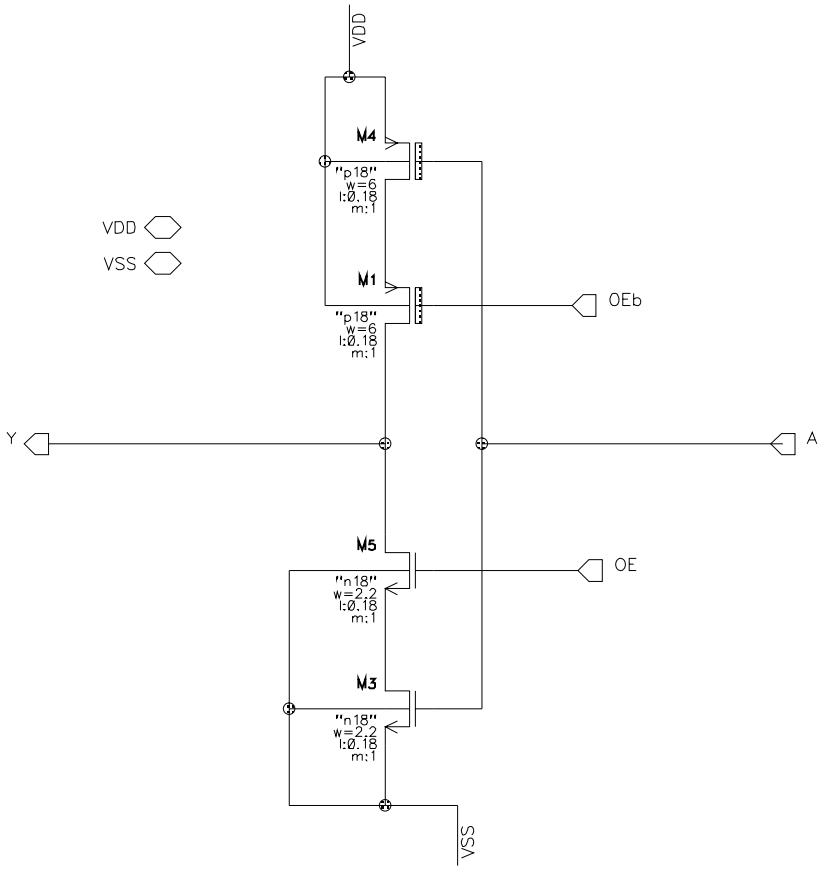
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x4.lay3
Last QA Review	
Last Changed	Sep 28 11:42:24 2006



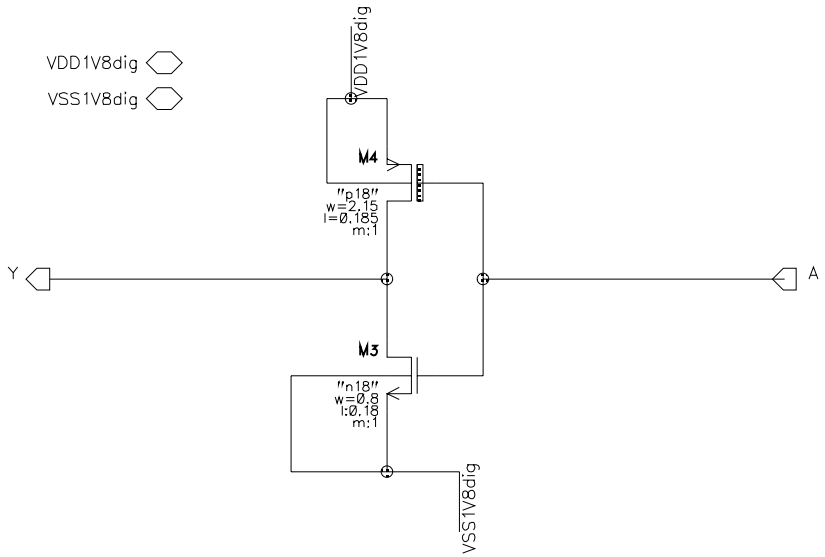
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x0c
Last QA Review	
Last Changed	Feb 12 18:49:59 2007



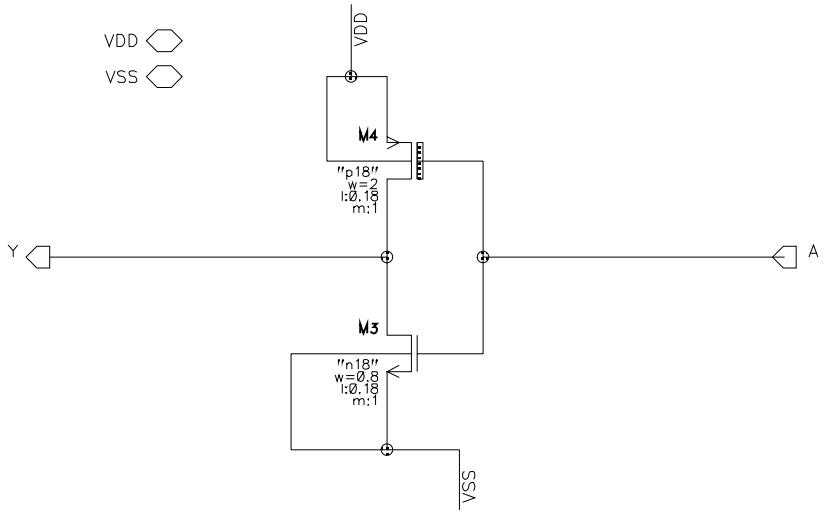
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x1
Last QA Review	
Last Changed	Sep 28 11:42:37 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_invOE_x3
Last QA Review	
Last Changed	Jan 22 10:54:26 2007

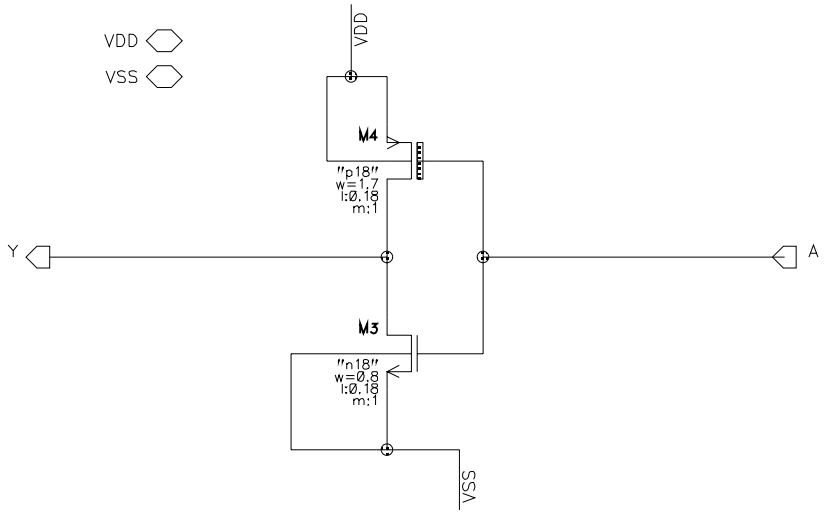


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Feb 5 17:55:09 2007

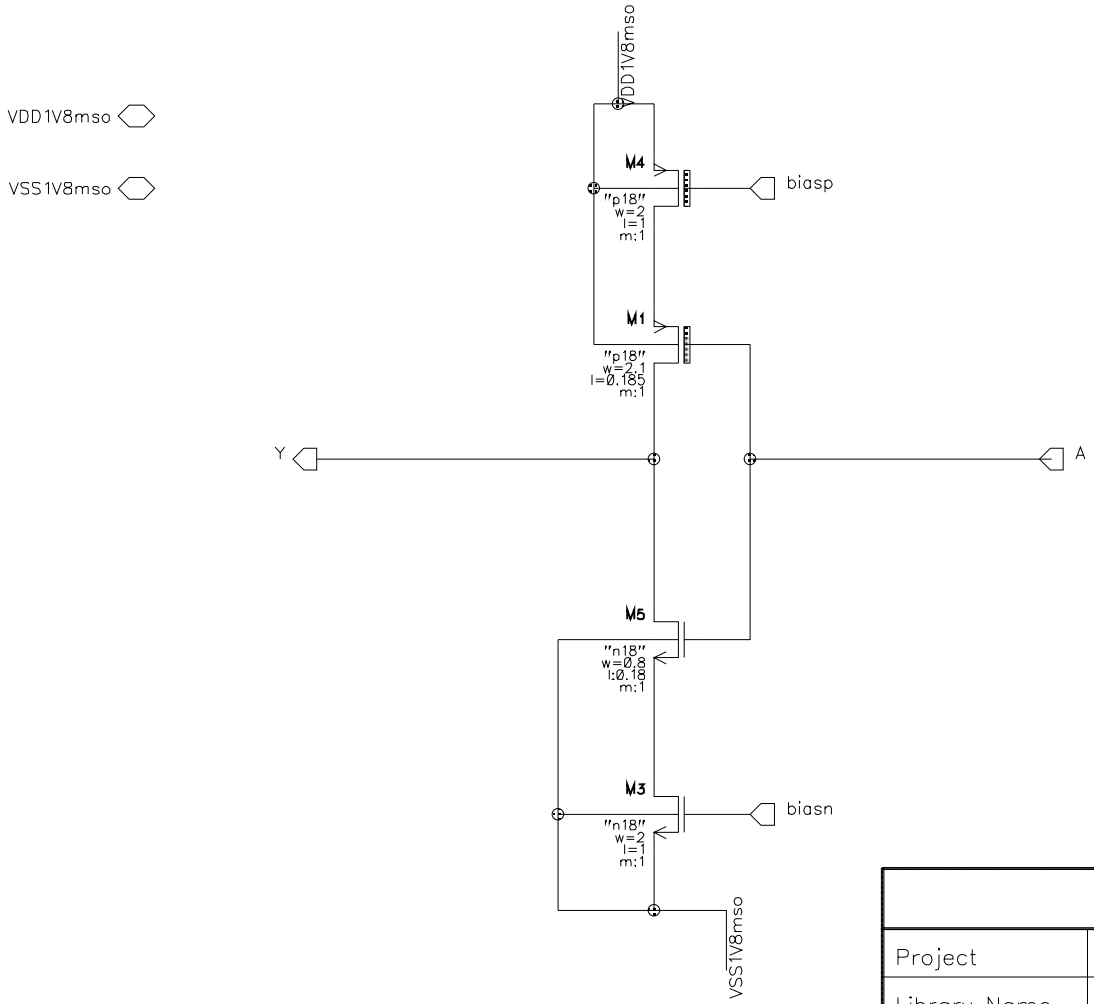


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Mar 12 17:30:10 2007

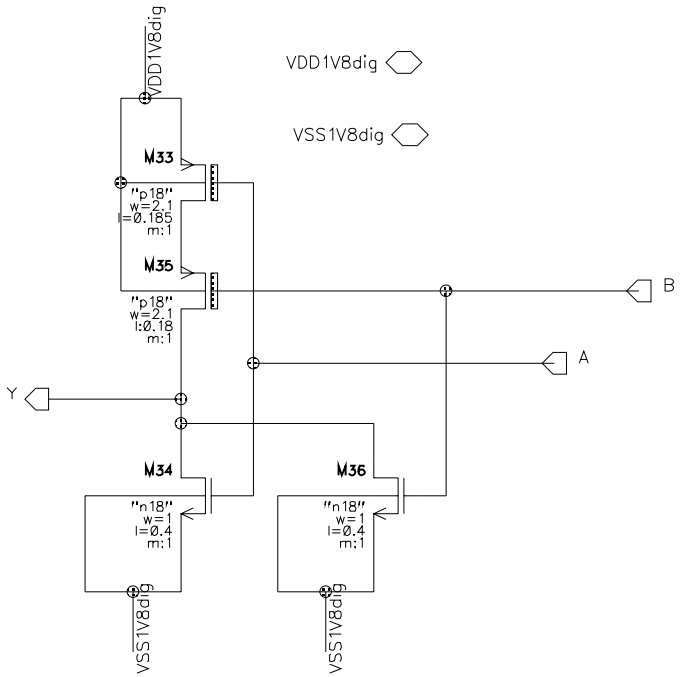
PMOS width reduced from 2um to 1.7um to aid efficient SRAM layout



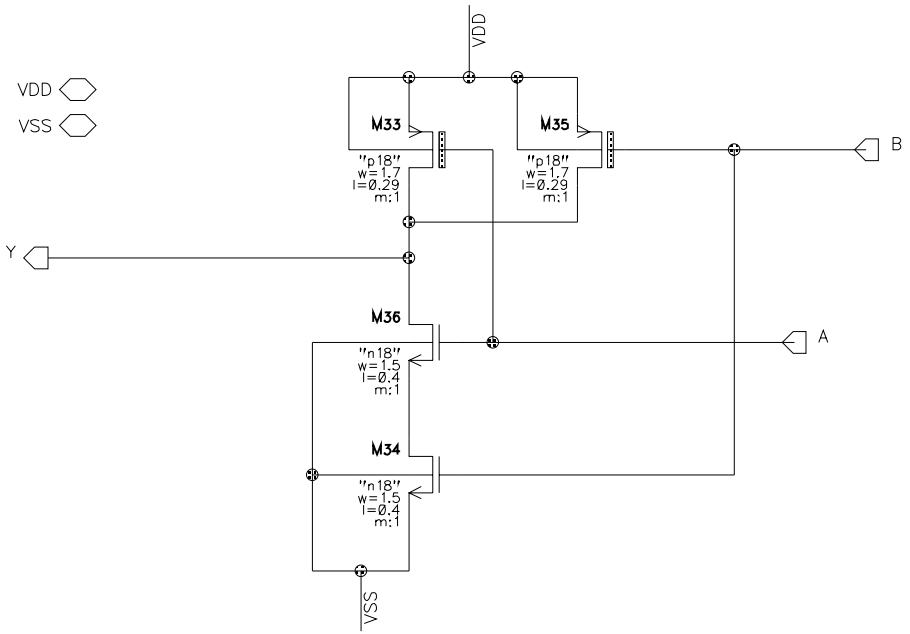
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1lay1
Last QA Review	
Last Changed	Mar 8 17:41:16 2007



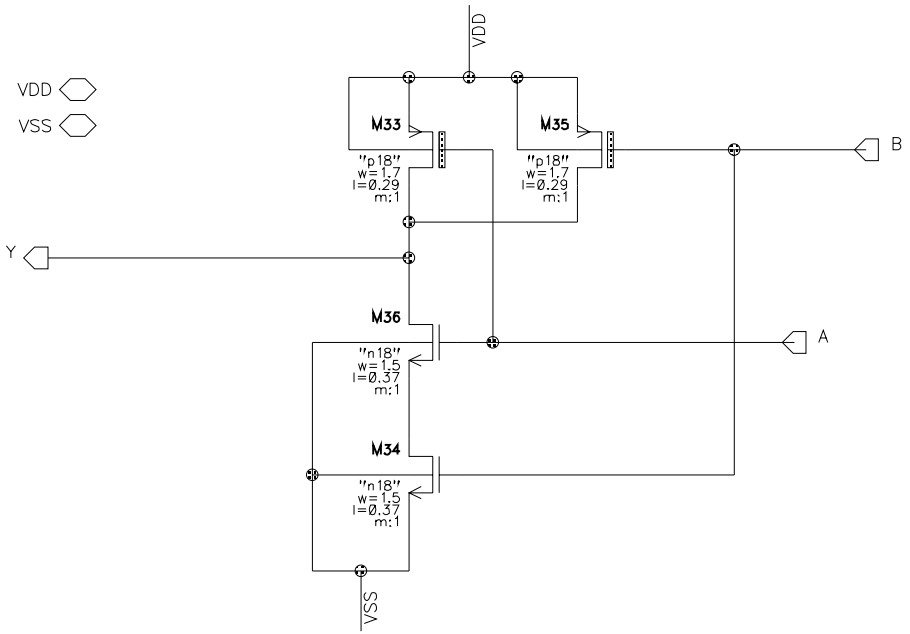
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_inv_x1lim
Last QA Review	
Last Changed	Mar 8 17:45:02 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	CalicePixels
Block Name	logic_nor2_x0
Last QA Review	
Last Changed	Mar 15 16:09:42 2007



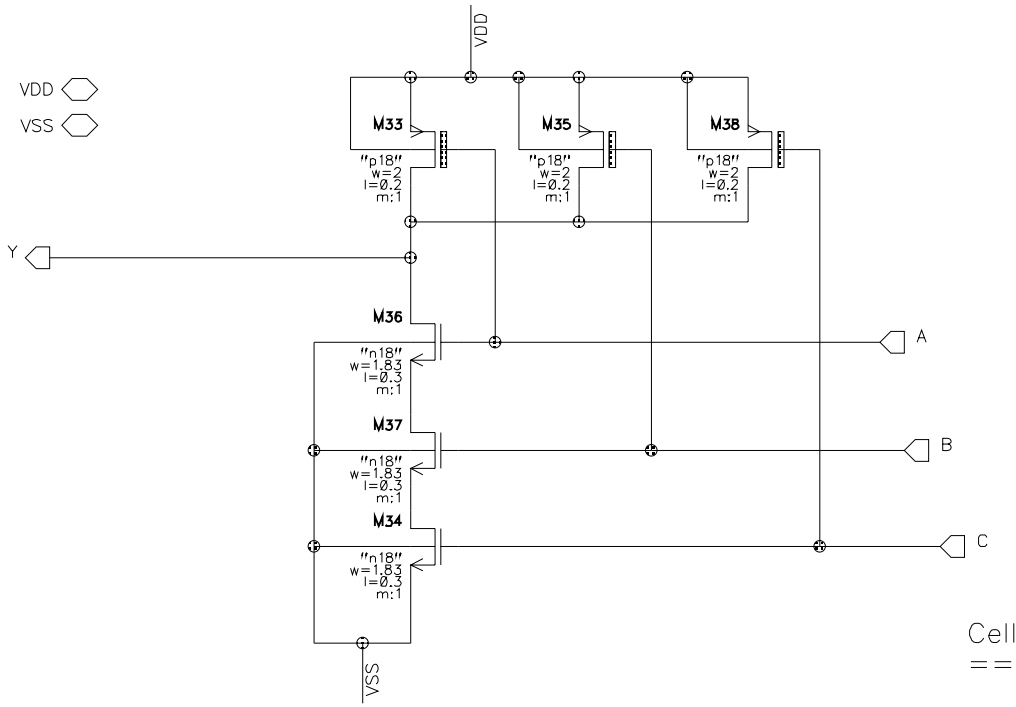
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_x0
Last QA Review	
Last Changed	Jan 4 09:07:25 2007



Cell variant for layout ".lay1"
==========

NMOS lengths reduced from Ø.4 to Ø.37

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand2_xØ.lay1
Last QA Review	
Last Changed	Jan 10 14:22:40 2007



Cell variant for layout ".lay1"

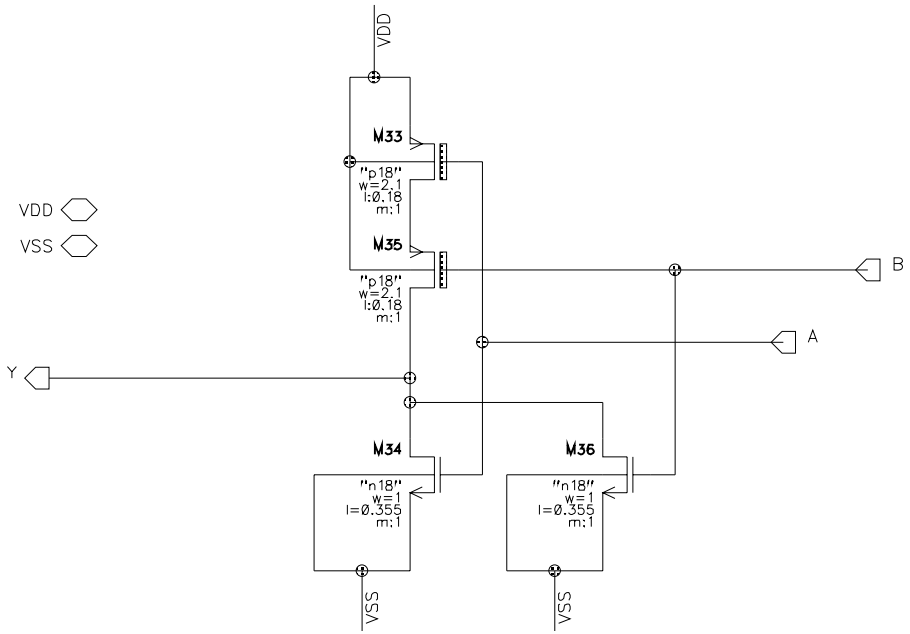
==========

NMOS width reduced from 1.9 to 1.83

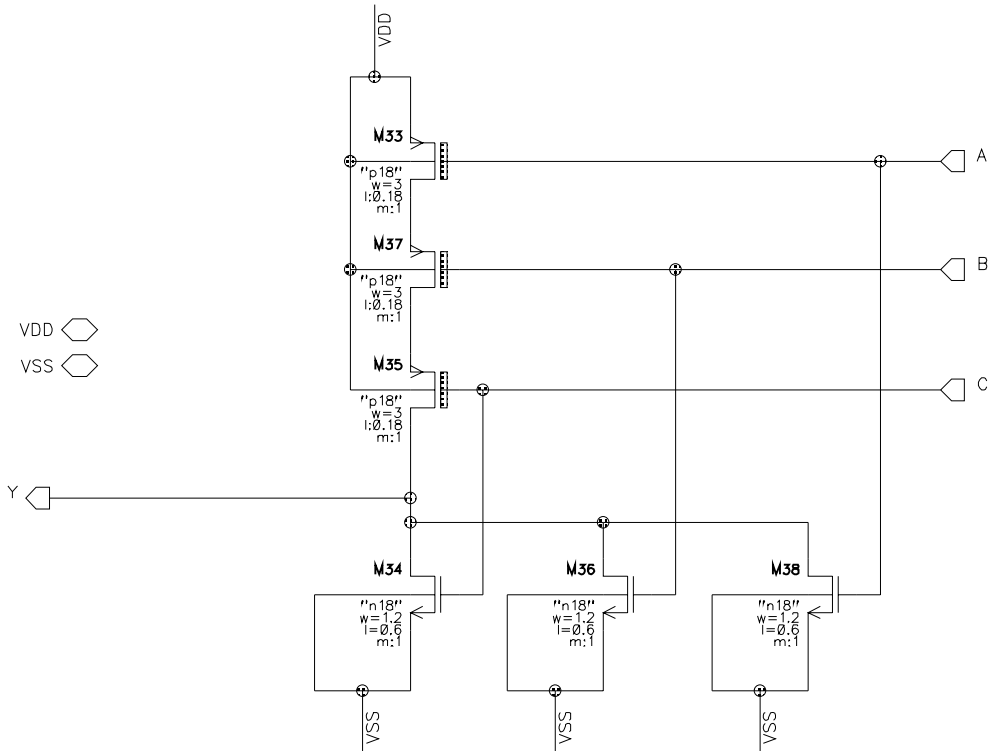
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nand3_x0.lay1
Last QA Review	
Last Changed	Jan 10 14:24:41 2007

Layout variant

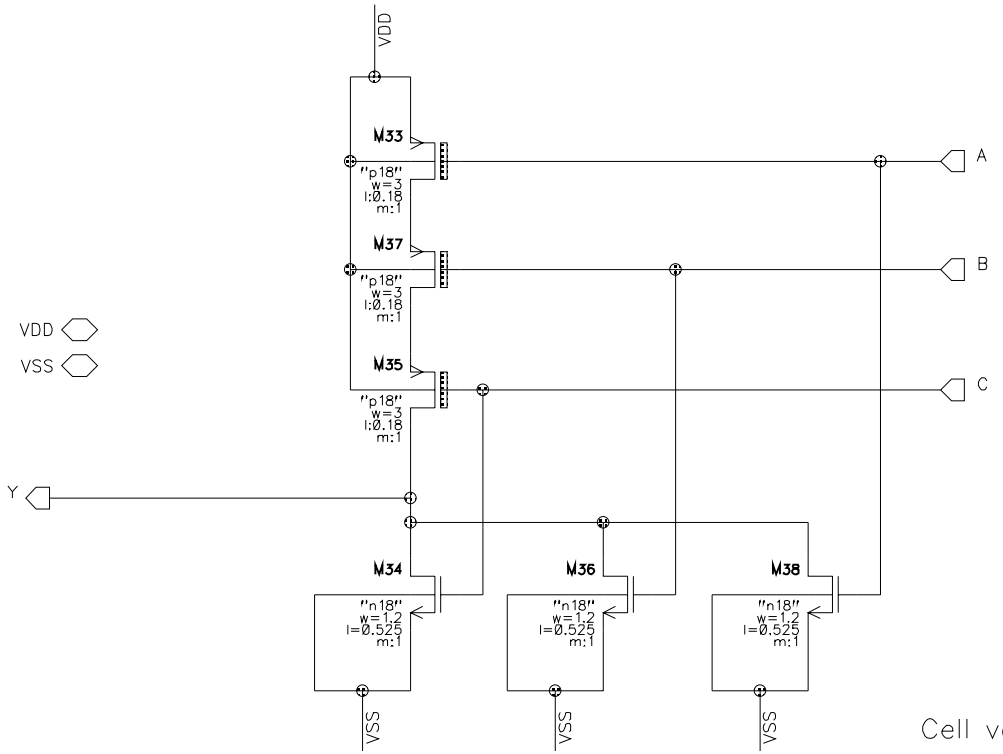
nmos length reduced from Ø.4 to Ø.355



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor2_xØ.lay1
Last QA Review	
Last Changed	Mar 26 11:50:49 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_x0
Last QA Review	
Last Changed	Jan 10 14:06:59 2007

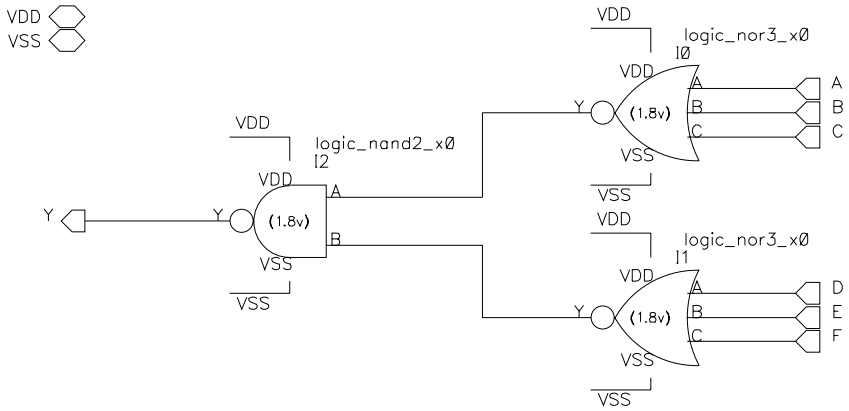


Cell variant for layout: ".lay1"

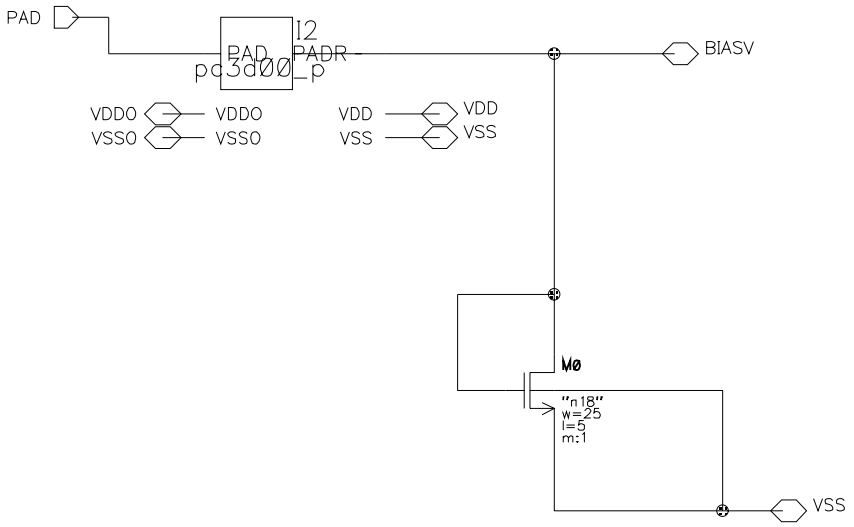
==========

NMOS length reduced from Ø.6 to Ø.525

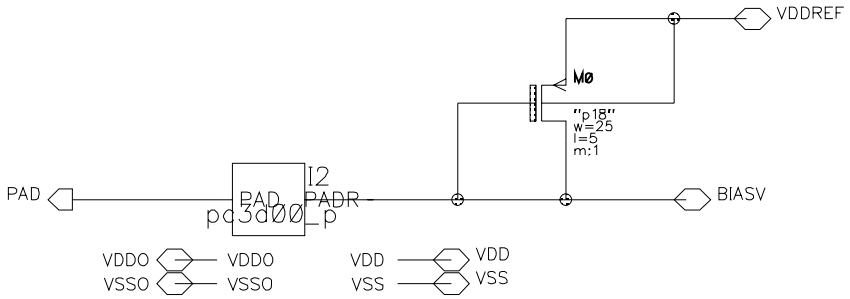
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_nor3_xØ.lay1
Last QA Review	
Last Changed	Jan 10 14:20:51 2007



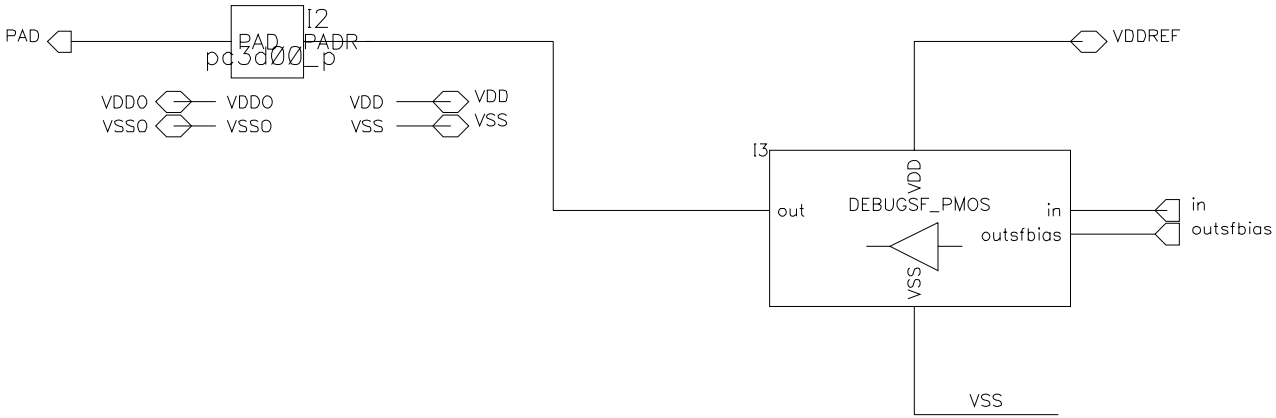
RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_or6
Last QA Review	
Last Changed	Apr 19 11:34:27 2007



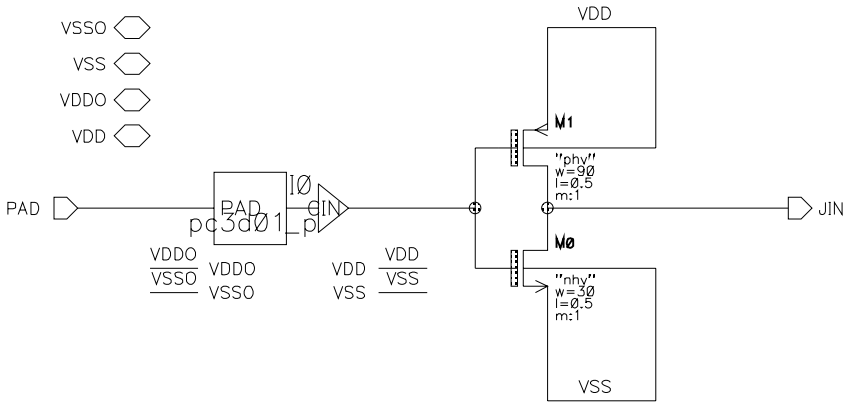
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_INPUT_x1_irefNMOS
Last QA Review	
Last Changed	Jun 28 09:07:13 2007



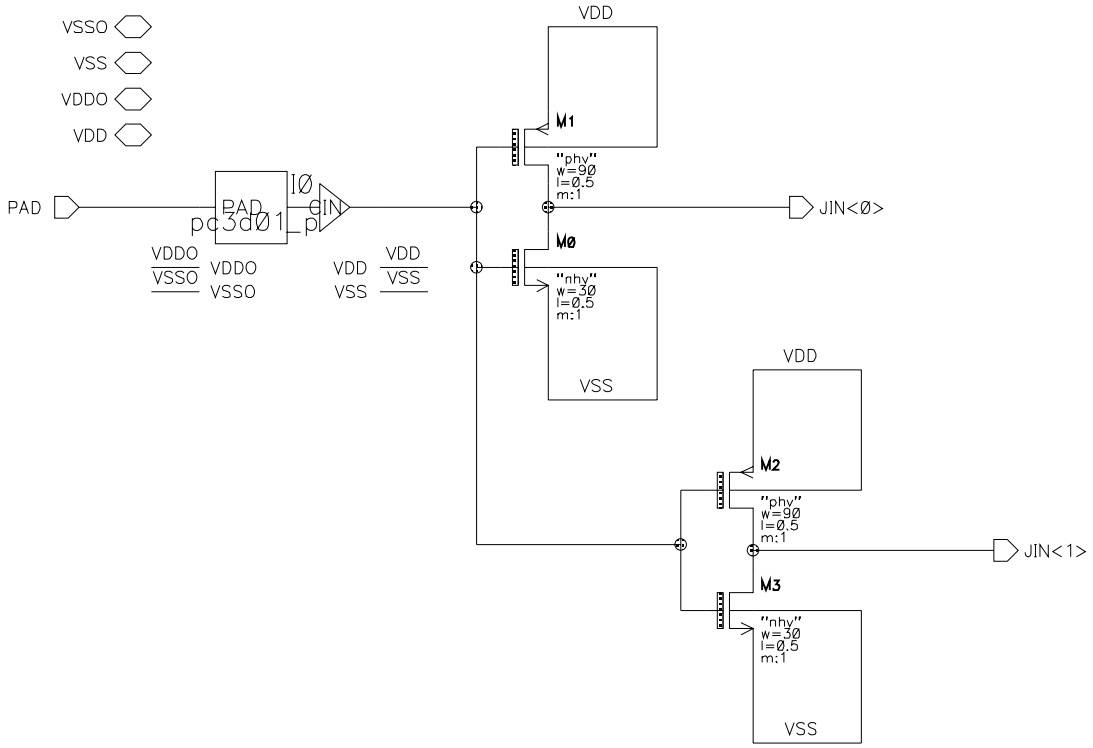
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_OUTPUT_x1_irefPMOS
Last QA Review	
Last Changed	Jul 3 13:44:02 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	ANALG_OUTPUT_x1_PMOSsf
Last QA Review	
Last Changed	Jul 3 13:43:00 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	DIGITAL_INPUT_JCbigbuf
Last QA Review	
Last Changed	Jul 3 13:44:55 2007



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_padlib
Block Name	DIGITAL_INPUT_JCdblbuf
Last QA Review	
Last Changed	Jul 3 13:45:Ø4 2Ø07