PCB Changes: TPAC1.0 → TPAC1.1

Standard PCB Modifications

1. Assign & label a unique board number (21 is the first available number for the 2008 batch)
2. Set DIP code to match assigned board number
3. If missing, fit jumpers to J1,J2,J3,J4,J5,J6,J7,J8,J9,J23*,J24*
   * 3-pin headers: fit in position closest to sensor/central cut-out
4. If missing, an 0603 zero-ohm resistor should be fitted to R86 in the "VDD" position

PCB modifications for compatibility with bonded Test Devices

5. Remove IC14, R69, R70, R71, R73
6. Remove IC17, R65, R66, R67, R68

Resistor value changes

7. Some resistor values still need changing, so the full biasing set are summarised below for reference (partial duplication of information from previous section)

Ref	Value	Signal	Notes
R65	-		Do not fit
R66	-		Do not fit
R67	-		Do not fit
R68	-		Do not fit
R69	-		Do not fit
R70	-		Do not fit
R71	-		Do not fit
R72	-		Do not fit
R73	-		Do not fit
R74	6K2	debug_sfbias	As TPAC1
R75	100K	I12compbiastrim	May change to adjust full trim range
R76	48K7	IsenseColRef	Original fitted value Subject to review
R77	5K1	I12msobias1	As TPAC1
R78	560R	I12prebias1	As TPAC1
R79	560R	I12shaperbias1	As TPAC1
R80	560R	I12compbias2	As TPAC1
R81	560R	Isense_ioutbias	As TPAC1
R82	560R	Isense_icompbias	As TPAC1
R83	20K	I12_compbias1	As TPAC1
R84	20K	Isensebias	Subject to review (bug fixed TPAC1.1)
R85	560R	I12_outbias	Subject to review (bug fixed TPAC1.1)

Control Signal Inverters

8. The two on-board inverters for control signals, IC5 and IC6 should be fitted with the higher-speed part: TBC [Matt Noy]

cont…/

Since the FPGA design will need to change for the new sensor design, it makes sense to implement this change to clock timing for the new batch of boards from the outset, and then all board are identical and capable of driving for faster operation when this has been proven.

Redundant PCB modifications from TPAC1.0

If a PCB from the TPAC1.0 batch is being modified for TPAC1.1, then the following PCB modifications must be un-done. Note this only applies to boards numbered 1→20.

9. The original [note1] modification involving lifting pins 1&2 on IC17 and adding 2k2 to ground is not necessary for TPAC1.1
10. The original [note2] modification involving removing TR1 and adding 2k2 between pin2 and ground no longer applies: TR1 must be present as original board design.
11. The power module [note 5] is no longer needed for TPAC1.1; jumper J1 should be fitted.

PCB Changes to functionality: TPAC1.0 → TPAC1.1

Power supplies

VRST now controls VGUARD, the n-well ring around the bulk pixels. Same option (through J24) of DAC channel 24 or VDD1V8 applies.

Control signals

Signal DEBUG_RST600 (pin166) functionality changed to DEBUG_TRIM[4]
Signal ENABLE34* (pin166) functionality changed to DEBUG_TRIM[5]
* note that ENABLE34 is wired through an on-board inverter so will have opposite polarity

On-board DACs

For normal operation of the sensor, the following DAC channels are no longer relevant:

DAC	SIGNAL	PIN	NEW FUNCTIONALITY	BONDED
0	I34_IOUTBIAS	101	Diode test structure	
1	I34_MSOBIAS2	104	Capacitor test structure	
2	I34_MSOBIAS1	105	Capacitor test structure	
3	I34_COMPBIAS2	106	Capacitor test structure	
4	I34_PREBIAS	122	Resistor test structure	✓
5	I34_OUTSFBIAS	123	Resistor test structure	✓
6	I34_COMPBIAS1	107	Not used	
7	I34_SFBIAS	121	Resistor test structure	✓
8	I34_COMPBIASTRIM	124	Resistor test structure	✓
26	VPREAMPCASC34	125	Resistor test structure	✓

Note that some of these signals will be bonded to the PCB which has introduced additional PCB modifications to avoid conflicts.