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CMOS Sensor Design Group

Tera-Pixel APS for CALICE

TPAC1.1 User Manual

Document Revision 2.0.143

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11 September 2008

1. INTRODUCTION

This document has been updated to reflect changes applied to make TPAC1.1. Most chip functionality remains from TPAC1.0 but with single pixel variant and different test structures.

The development of the *Monolithic Active Pixel Sensor* (MAPS) prototype solution for the CALICE project is spread across three years and will produce two sensors. The first sensor ("TPAC1.1"; this document) specifically targets the pixel design, of which four are implemented for evaluation. The most favourable pixel design will then be implemented into a larger-scale "ASIC2" device suitable for beam tests.

This document provides a complete technical reference manual for the TPAC1.1 test sensor.

Some useful facts and figures:

TPAC1.1 chip	Number of pads	265 *(numbered as 300 pad sites)*	
	Number of pixels	28,224	
	Pixel size	50x50 microns	
	Sensitive area	79.4mm^2	
	…of which "dead"	11.1%	
	Dimensions (design)	10.31 x 9.54 mm	
	Dimensions (cut die)	10.50 x 9.70 mm	
Manufacturing process	Feature size	0.18 micron	
	Metal routing layers	6	
	Poly layers	1	
	Epitaxial Layer	12 & 5.5 micron wafer splits	
	Special implant	None & std Deep P-Well wafer splits	
	Die thickness	16 mils *(~400 microns)*	
Number of transistors	preShape pixel	160 *(+27 capacitors)*	
	preSample pixel	189 *(+34 capacitors)*	
	Control logic *(total)*	~1.3 million	
	Embedded SRAM *(total)*	~2 million	
	TPAC1.1 sensor *(total)*	~8.2 million	
Analog pixel performance	preShape pixel	Gain	94 $\mu V/e^-$
		Noise	23 e^-
		Power *	8.9uW
Data Architecture	Configuration memory	141,120 bits	
	SRAM storage memory	280,896 bits *(effective[†] 383,040)*	
	Readout architecture	30 bit parallel data	
	Max readout speed	5Mhz	

* Quoted pixel power is for a single pixel operating continuously at typical operating current: any powering duty cycle is not included in this figure.

† Effective memory includes row-address ROM which is read at the same time as hit-data

1.1 RELATED DOCUMENTS

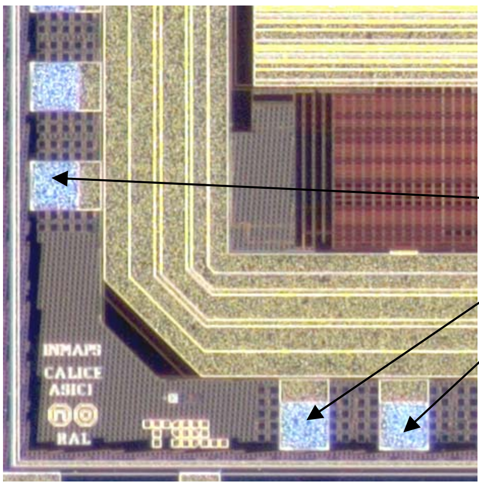
Document Title	Author
TPAC1.1 Pin list	J Crooks
TPAC1.1 Schematics	J Crooks
TPAC1.1 Testing Specification	

1.2 REVISION HISTORY

Comment	Revision code	Date
Draft document distribution	1.0.24	
Draft document distribution	1.0.77	
Draft document distribution	1.0.123	6/7/07
Full document release (v1.0)	1.0.135	17/7/07
Added parallel load signal timings to config shift register information. Updated missing cross-reference section numbers Minor changes to explicitly state that all diagrams are drawn viewing the sensor from above. Elaborated SRAM operation to show input data sampling window and when output data changes	1.1.xxx	
Updated document for TPAC1.1 - Removed references to preSample pixels - Updated sensor diagram(s) - Updated config load section for extra bits - Updated test pixels section - Added details of test devices	2.0.xxx	11/9/08

1.3 Top Level Layout

The plot above excludes top level metal, as this has 83% coverage with few recognisable features. The image shows clearly the areas of pixels (dark), the logic columns and the single row of bias transistors across the centre. [Note: plot not updated to show extra pads present on TPAC1.1]



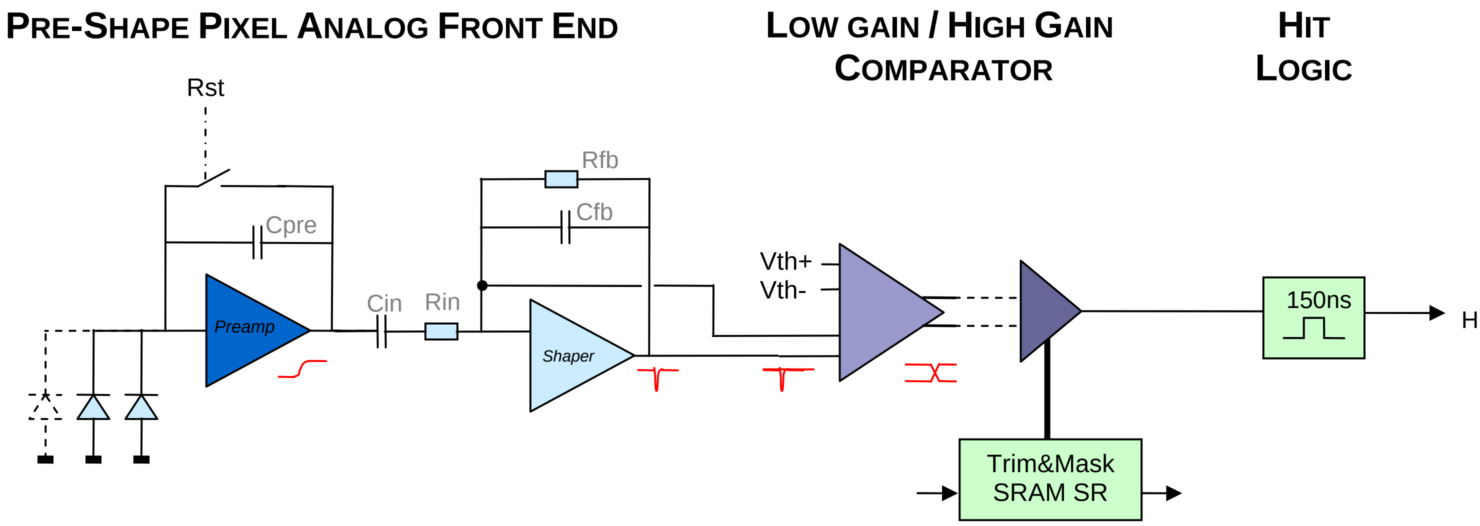
Chip orientation marks are located in the bottom left corner, and include © symbol, manufacturer TSL logo and name characters: INMAPS, RAL, CALICE ASIC1.1.

Overall chip dimensions (edge of pads) = 10.31 x 9.54 mm
Overall chip dimensions (cut die approx) = 10.5 x 9.7 mm

1.4 Pixel Overview

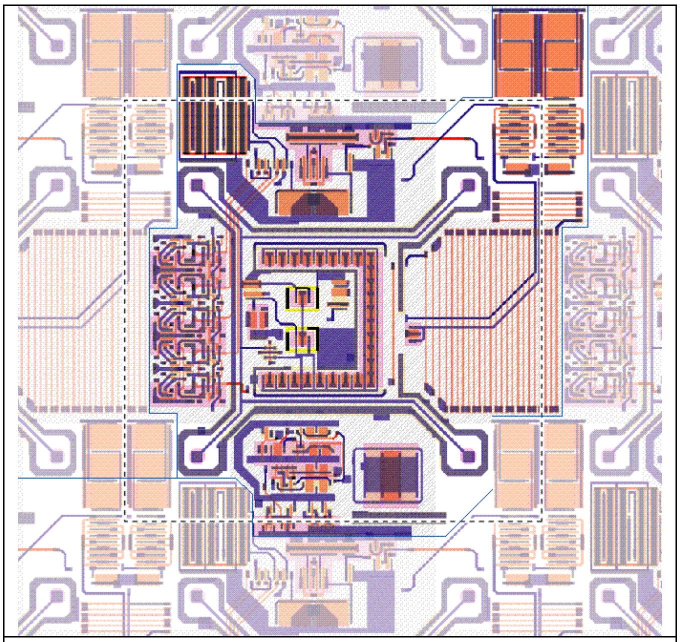
One pixel architecture for charged particle detection is implemented: The 50 micron pixels contain four N-well diodes for charge-collection; analog front-end circuits for signal pulse shaping; comparator for threshold discrimination; digital logic for threshold trim adjustment and pixel masking. Block diagrams are shown below.

The "preShape" pixel contains single-ended charge preamplifier, shaper, differential comparator and hit-logic. The comparator takes the input and output of the charge preamplifier as the pseudo-differential signal level. During a hit event the hit-logic will generate a one-time "hit-flag" output to the logic. The CR-RC shaper output will decay according to input signal magnitude, after which the pixel can accept another event.



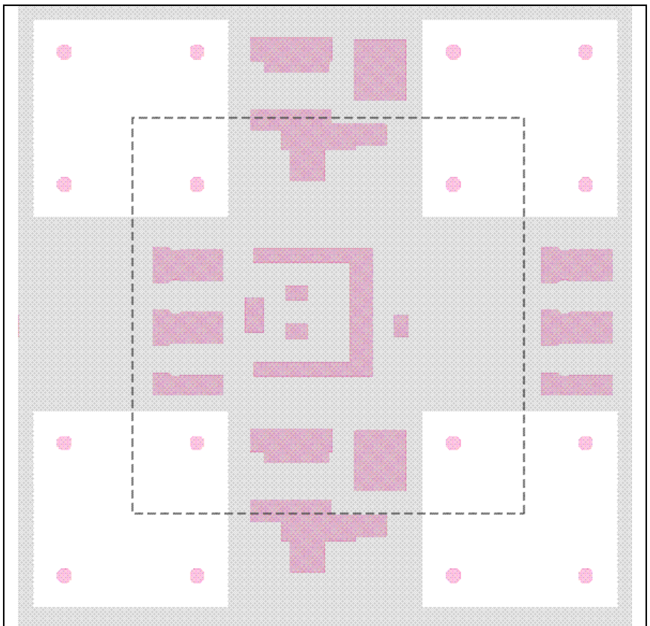
1.5 Pixel Layouts

Pixel layouts up to metal 1 are shown below. Since the pixel layouts overlap into neighbouring pixels, the dotted square is added to show the boundary of a single 50 micron pixel.



preShape pixel

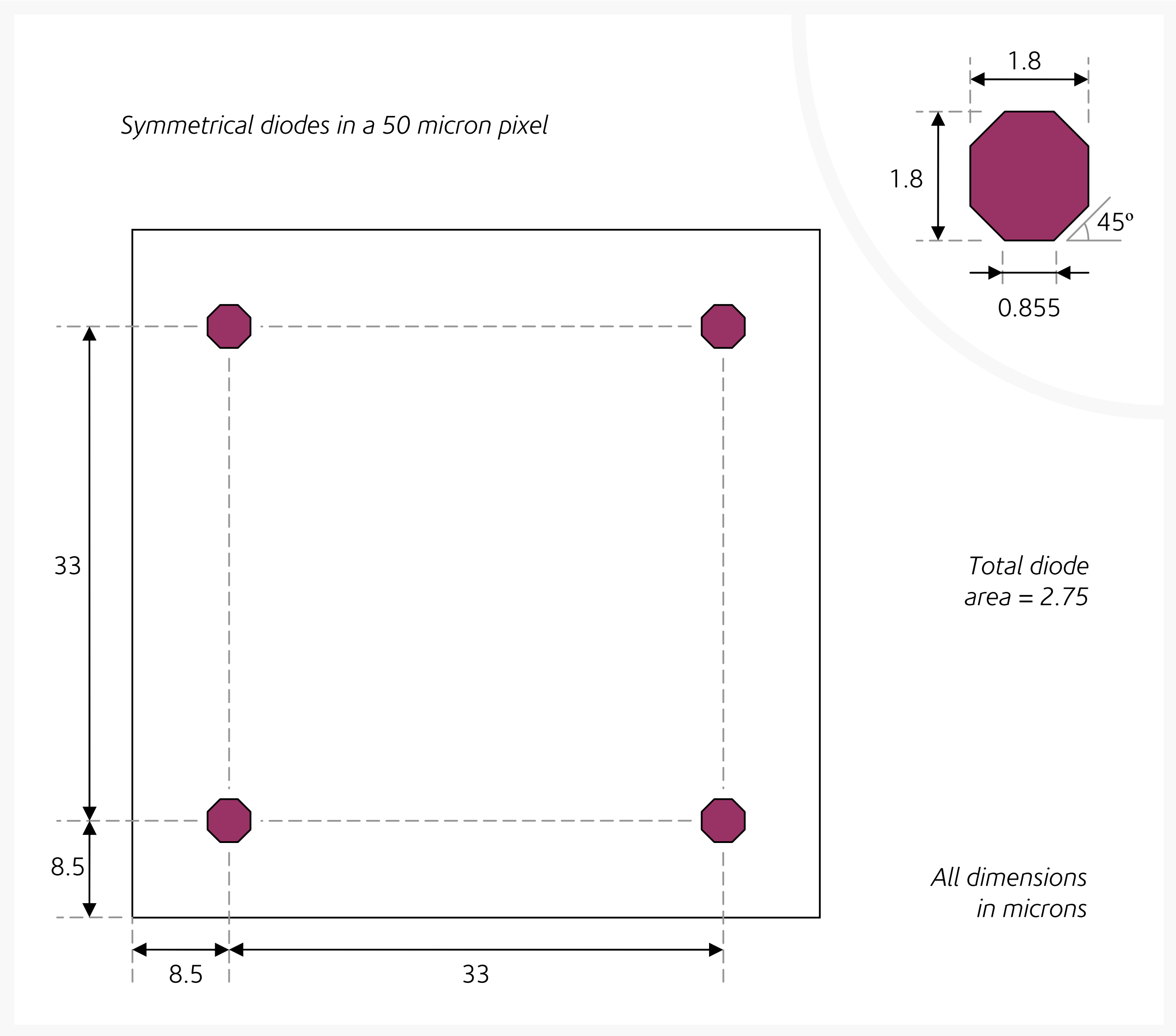
The same region is shown again with only N-Well and deep P-Well layers shown, again with the dotted line to indicate the boundary of a single 50 micron pixel. Only the four pixel diodes (pushed towards the corners) are left unshielded by deep P-Well.



preShape pixel

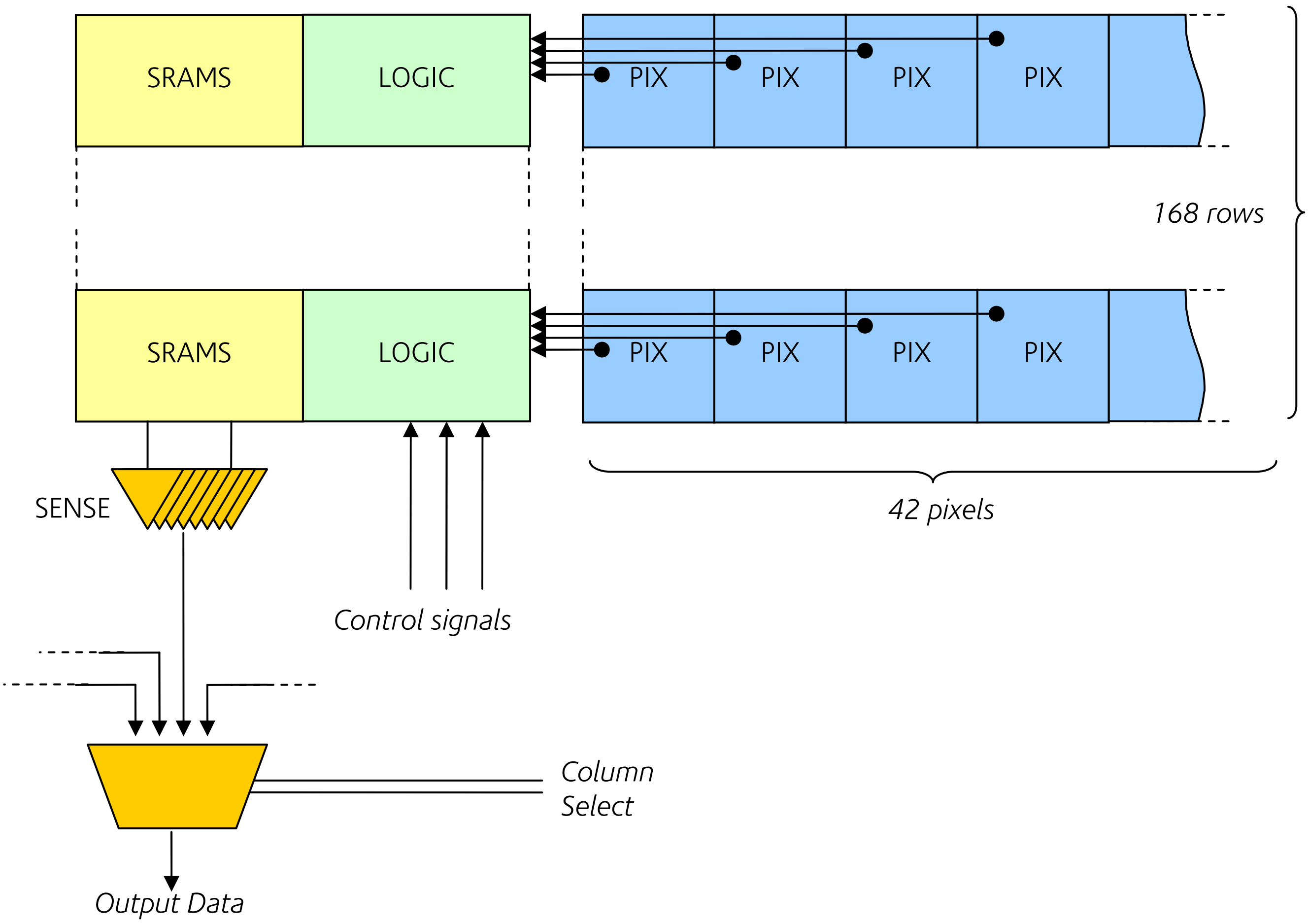
1.6 Diode Size & Location

The exact locations of diode centres within a pixel are specified below:



1.7 Digital System Overview

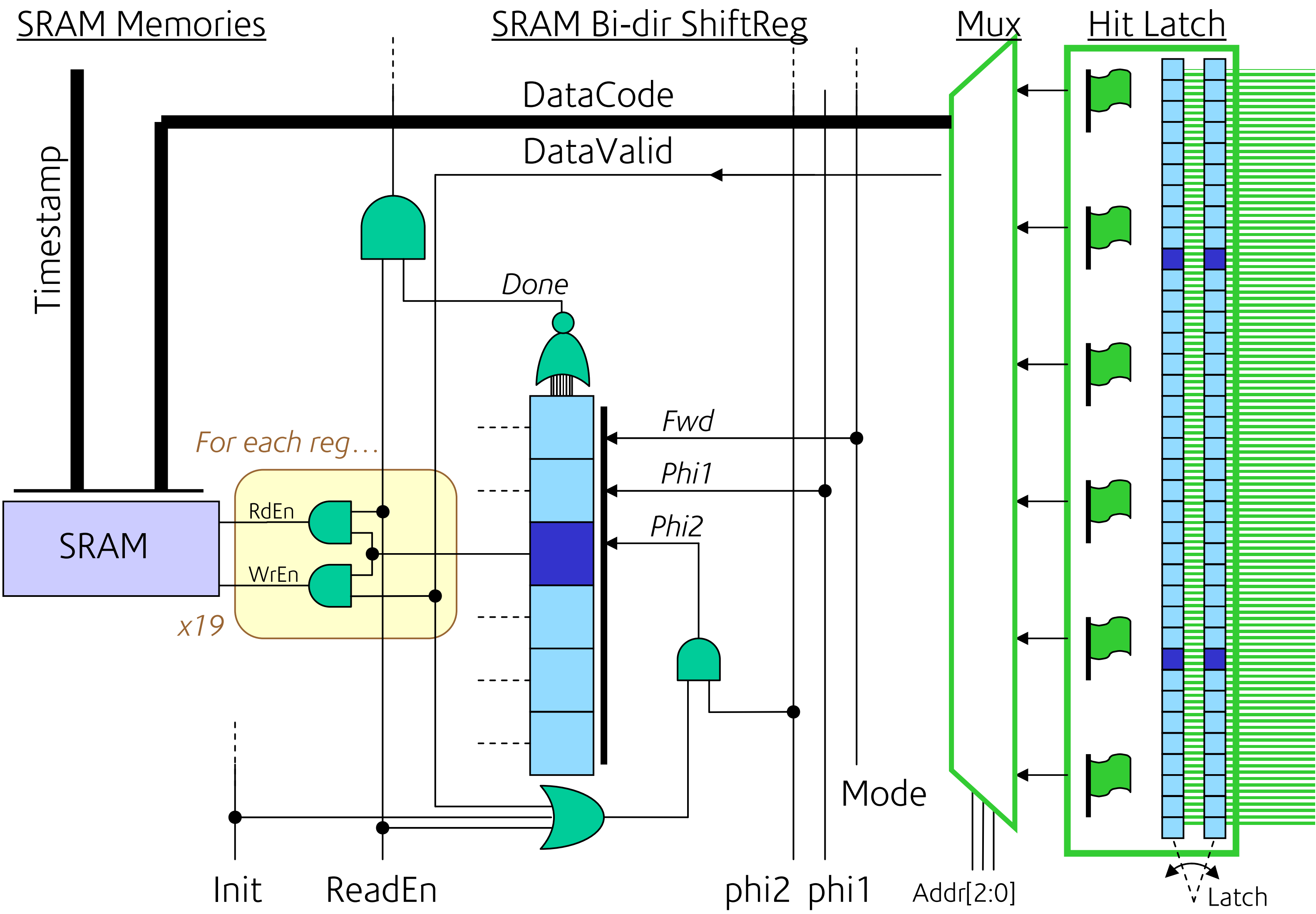
A row of 42 pixels is served by a block of control logic, which takes the 42 hit inputs and stores locations of hits in its available SRAM registers. During the readout phase, the SRAM registers that contain hit data are read out through sense amplifiers at the base of the column.



The full "column" contains 168 active rows, each comprising 42 pixels, logic and SRAM (equivalent to another 5 "dead" pixels). The column is 2350 microns wide. Four of these are placed adjacent to make the full sensing area in TPAC1.1.

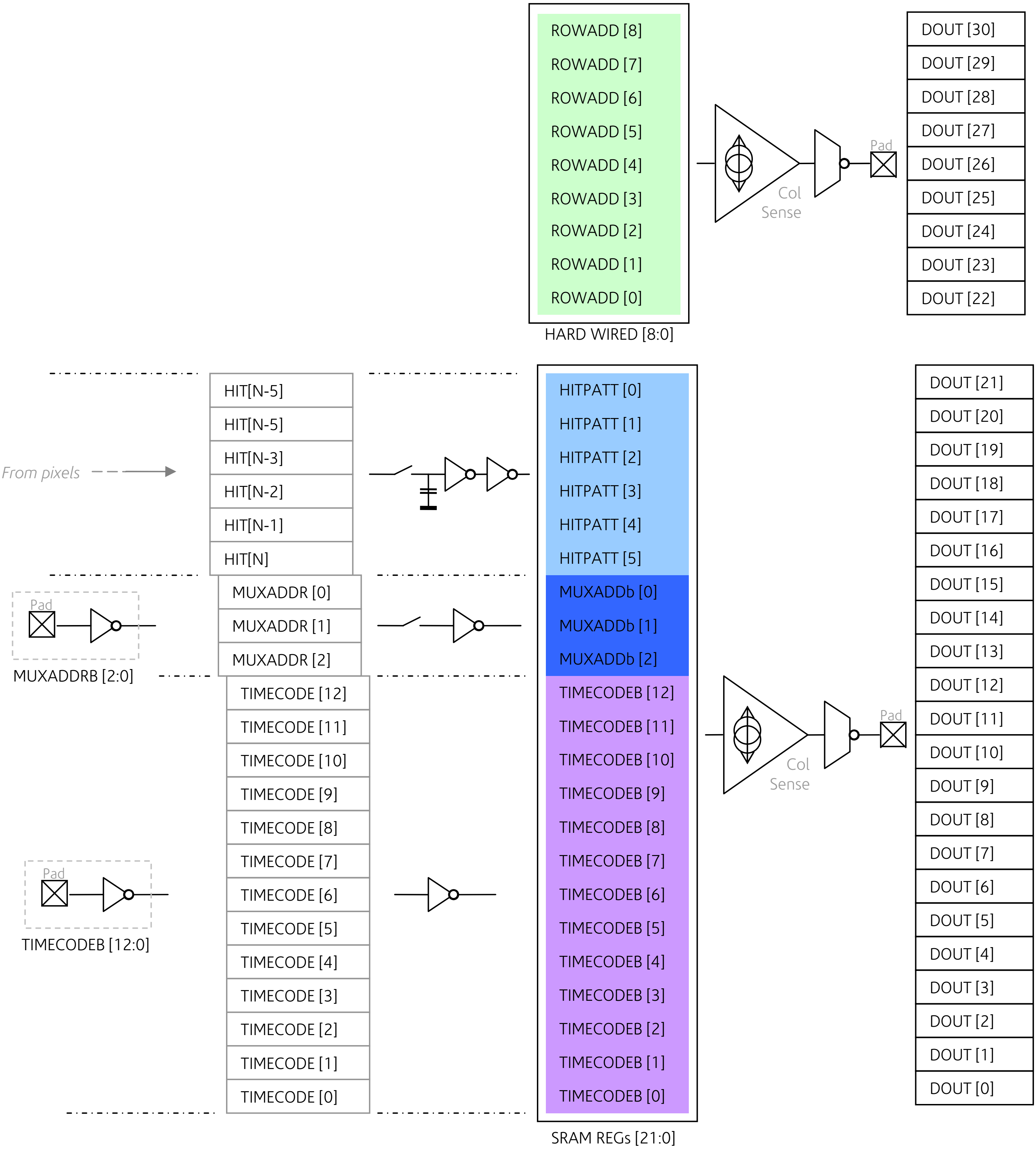
1.8 Row Logic Overview

The internal row logic comprises latch-hold circuits which sample the current state of the 42 "hit" input signals. These are arranged into banks of 6, each of which generates a hit flag. A multiplexer sequences through 7 address codes, interrogating each of the 7 hit flags. If a hit flag is set, the 6-bit hit pattern is written to the next available SRAM memory, along with a bank code and the global timestamp. SRAM locations available are controlled by a bi-directional shift register, which is clocked once for each hit pattern that is stored. This register is then clocked in reverse during readout, so activate the memory cells which have valid data. There are 19 SRAM registers in each row controller. Block diagram representation of the row logic is shown below.



1.9 Data Format

The parallel data output is summarised in the diagram below to illustrate bit assignments and inversions so hit data can be reconstructed off-chip.



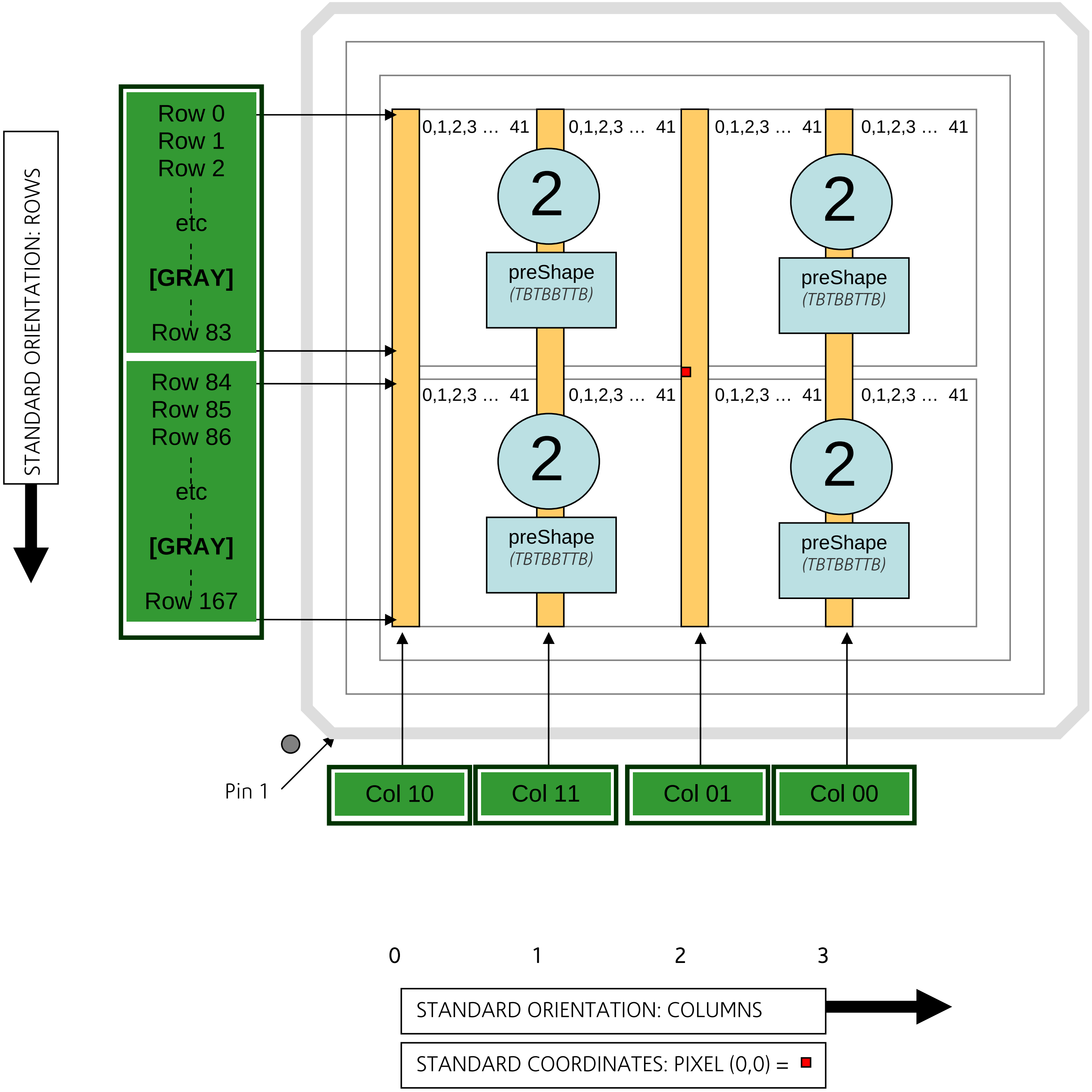
1.10 HIT LOCATION LOOK-UP TABLE

Pixel #	MUXADDb	HITPATT
41 40 39 38 37 36	011	5 4 3 2 1 LSB
35 34 33 32 31 30	010	5 4 3 2 1 LSB
29 28 27 26 25 24	000	5 4 3 2 1 LSB
23 22 21 20 19 18	001	5 4 3 2 1 LSB
17 16 15 14 13 12	101	5 4 3 2 1 LSB
11 10 9 8 7 6	100	5 4 3 2 1 LSB
5 4 3 2 1 0	110	5 4 3 2 1 LSB

1.11 Pixel Identification

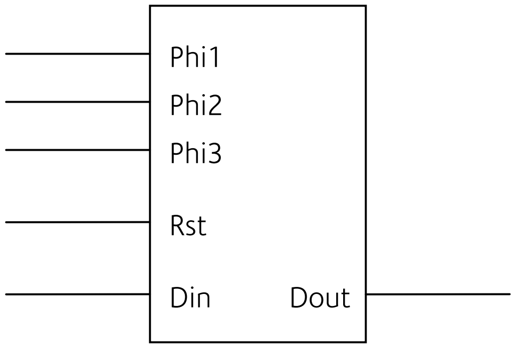
The diagram below may be useful when reconstructing physical location of hit data. Quadrant, pixel, row and column numbers are indicated to create a unique address space. The large black orientation arrows are replicated on the silkscreen of the PCB to avoid confusion: (The sensor will be mounted on the reverse of the test PCB).

<u>Sensor viewed from above:</u>



1.12 Shift Registers

The TPAC1.1 sensor implements the same standard three-clock-phase shift register cell in a number of locations. The basic cell is illustrated here:



The table below summarises the different application of this basic cell in the sensor, and the polarity (*at the pins*) for each of the clocks and reset signals.

Application of SR Cell	Control Signals			
Fast Config (top)	Phi1	Phi2	Phi3	RstB
Slow Config	Phi1	Phi2	Phi3	Rst
Fast Config (bottom)	Phi1	Phi2	Phi3	RstB
Logic SRAM controller	Phi1	Phi2	Phi3	RstB

The table below summarises the functional stable states for the shift register cell:

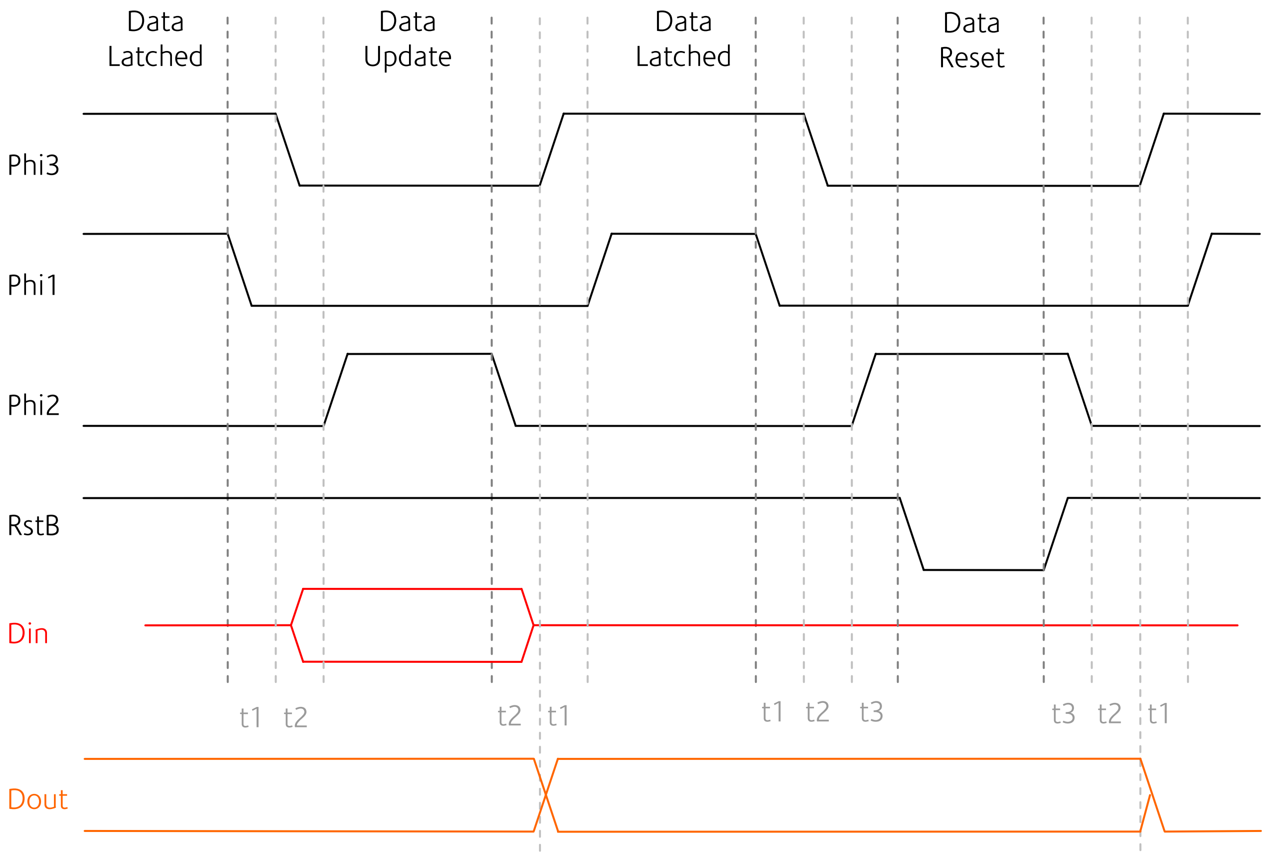
	Phi1	Phi2	Phi3	Rst
Reset	0	1	0	1
Stable (data held)	1	0	1	0
Transfer (dynamic storage)	0	1	0	0

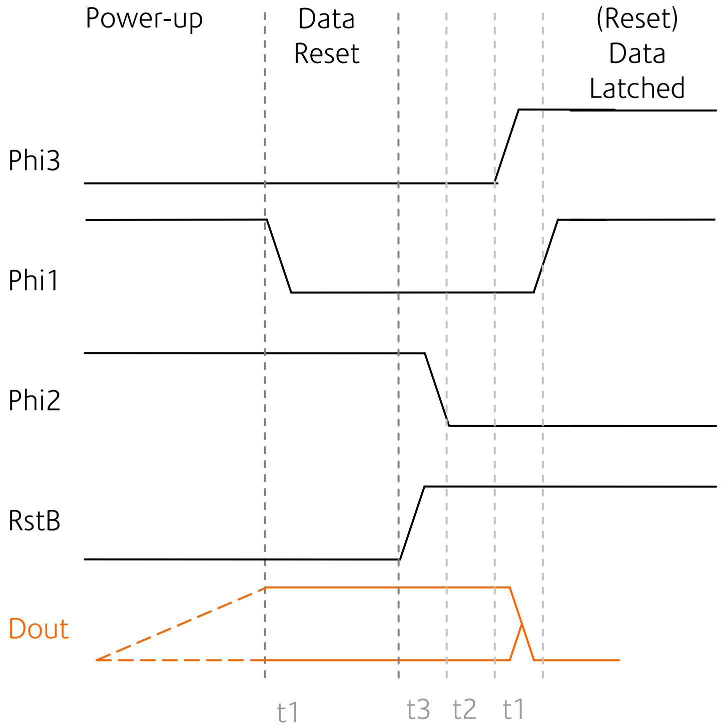
The conditions defined below should be observed during power-up & operation to prevent possible internal conflict:

	Phi1	Phi2	Phi3	Rst
Invalid state	X	X	1	1
Power-up (recommended)	1	1	0	1

After power-up, the recommended state should be advanced to the Reset state by changing phi1 from 1 → 0.

Clock diagrams for correct operation are illustrated below:





Din is sampled on falling edge of phi2

Dout is updated on rising edge of phi3

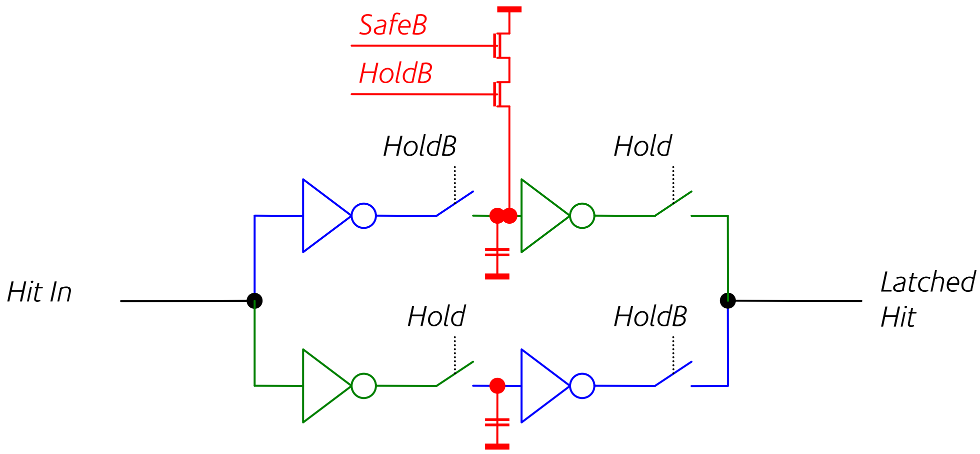
(t1) For zero-to-one transitions, phi3 must lead phi1
(t1) For one-to-zero transitions, phi1 must lead phi3
(t2) Phi2 and phi3 must be non overlapping (also with phi1 ensured by statements above).
(t3) Reset must be applied (active low) during phi2 phase

Typical values used in 50Mhz simulations are shown in the table below:

t1	Phi1 ←→ Phi3	2ns
t2	Phi3 ←→ Phi2	2ns
t3	Phi2 ← → RstB	2ns
Data Update		6ns
Data Latched		6ns

1.13 Latch Hold Circuit

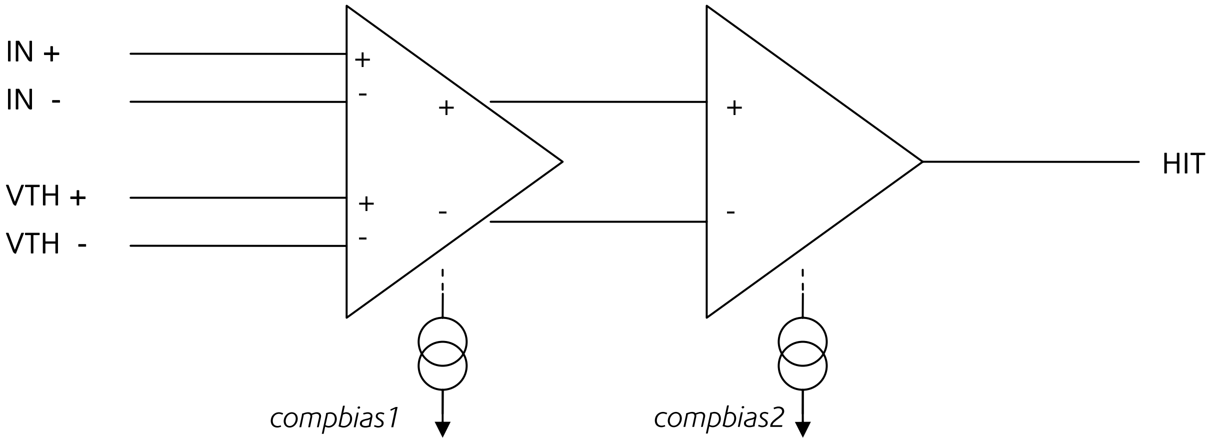
A circuit diagram of a single channel latch hold circuit is shown below.

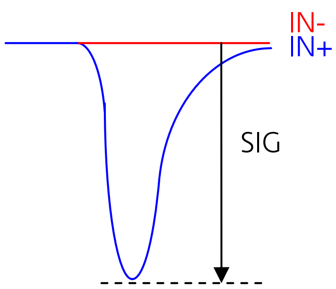


The table below summarises the functional stable states for the latch-hold cell (control signals are referred to by their name and correct polarity for the TPAC1.1 pin):

Circuit behaviour	HOLDB	LATCHSAFE
Hit Latched	1	0
Hit Latched	0	0
Inactive: Safe State	0	1

1.14 Comparator Operation



	preShape pixel
Typical “Hit” signal	 SIG = (IN-) – (IN+)
Threshold Voltage	 THR = (VTH+) - (VTH-)
HIT goes high when	SIG > THR
Preferred power-up state	VTH+ >> VTH-

1.15 BIAS CURRENTS

The table below summarises all the bias currents that are required for TPAC1.1 operation.

Pin	Name	Direction	Circuit	Typical Value	Ratio
157	debugsfbias	Input	Debug Test Structures (all)	200uA into pad	5:1 100:1
277	I12_IOUTBIAS	Output	PreShape pixels: Front end	125uA out of pad	25:1
274	I12_MSOBIAS1	Output	PreShape pixels: Monostable	90uA out of pad	250:1
258	I12_PREBIAS	Output	PreShape pixels: Front end	150uA out of pad	100:1
272	I12_COMP1BIAS	Input	PreShape pixels: Low gain comp	65uA into pad	200:1
273	I12_COMP2BIAS	Output	PreShape pixels: High gain comp	83uA out of pad	250:1
256	I12_COMPBIASTRIM	Input	PreShape pixels: Comp trim	85uA into pad	500:1
257	I12_SHAPERBIAS	Output	PreShape pixels: Front end	150uA out of pad	100:1
232	ISENSE_COLREF	Input	Sense amplifier column bias	50uA into pad	20:1
295	ISENSE_ICOMPBIAS	Output	Sense amplifier bias: Comparator	83uA out of pad	250:1
296	ISENSE_IOUTBIAS	Output	Sense amplifier bias: Output	125uA out of pad	25:1
294	ISENSEBIAS	Input	Sense amplifier bias	65uA into pad	32:1

1.16 REFERENCE VOLTAGES

The table below summarises all the reference voltages that are required for TPAC1.1 operation.

Pin	Name	Circuit	Typical Value
255	VPRECASC12	PreShape pixels	0.8v
100 128 246 297	VGUARD	Full sensor	Guard ring potential
254	VSHAPECASC12	PreShape pixels	1.5v

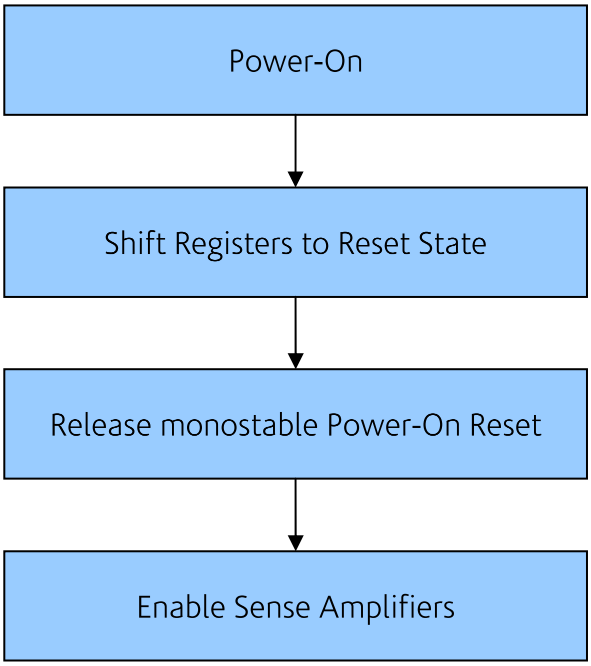
1.17 Power Supplies

Name	#Pins	Scope	Volts	Current	PCB ISO	Group
VDD1V8pix VSSpix	8 8	Analog pixel circuits: Front end preamplifiers and shapers	1.8v	180mA (typical static *)	J5	A4
VDD1V8aco VSSaco	6 6	Analog (first-stage) comparator in the pixel	1.8v	37mA (typical static *)	J8	A4
VDD1V8dco VSSdco	6 6	Digital (second stage) comparator in the pixel and 200ns monostable	1.8v	75mA (typical static *) +280mA max† TBC	J6	D4
VDD1V8mso VSSmso	6 6	Isolated 600ns monostable power supply	1.8v	280mA max† TBC	J4	D4
VDD1V8sram VSSsram	6 6	Isolated power supply for in-pixel config SRAMs	1.8v	10mA (switching current during config)	J7	D3
VDD1V8dig VSSdig	11 11	Digital logic: Row controllers, SRAM memories,	1.8v	250mA TBC (switching current)	J3	D2
VDDO VSSO	11 11	Digital IO buffers	3.3v	32mA (switching current)	J9	D1
VDD3V3dig	1	Bias reference for sense amplifiers	3.3v	Neg. <0.1mA (static bias ref)	J2	D2
VDD2V5dig	4	SRAM write buffers: overdrive supply	3.3v	30mA max (switching current)	J1	D1

* Static power in pixels reduces to ~zero when the enable pins are deactivated.

† Max current occurs when every pixel detects a hit simultaneously (extremely rare!) – this figure should be divided by the number of pixels (28k) for hit-rate calculations

2. SENSOR INITIALISATION



2.1 Summary of Required Signals during Power-Up

For the various shift register cells

Application of SR Cell	Control Pins: Power-up requirement			
	Phi1	Phi2	Phi3	Rst (/RstB)
Fast Config (top)	1	1	0	0
Slow Config	1	1	0	1
Fast Config (bottom)	1	1	0	0
Logic SRAM controller	1	1	0	0

For the latch-hold circuit

Pin Name	Power-up requirement
LATCHSAFE	1
HOLDB	0

For the monostable power-on reset:

Pin Name	Power-up requirement
MONOPOR	1

For the sense amplifiers

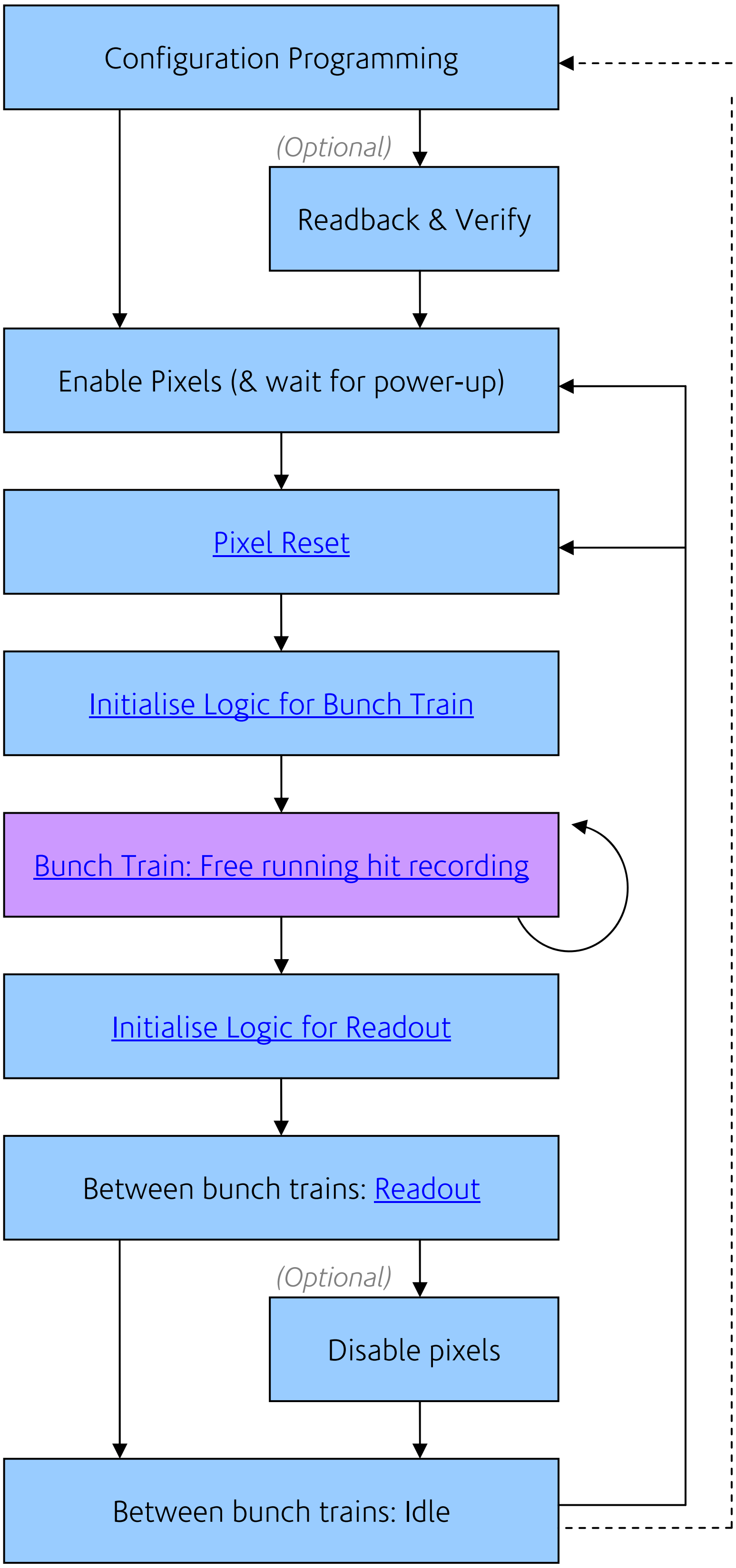
Pin Name	Power-up requirement
SENSE_Enb	1

To disable the analog pixel circuits

Pin Name	Corresponding circuits	Power-up requirement
ENABLE12	PreShape pixels	0
ENABLE34	PreSample pixels	0

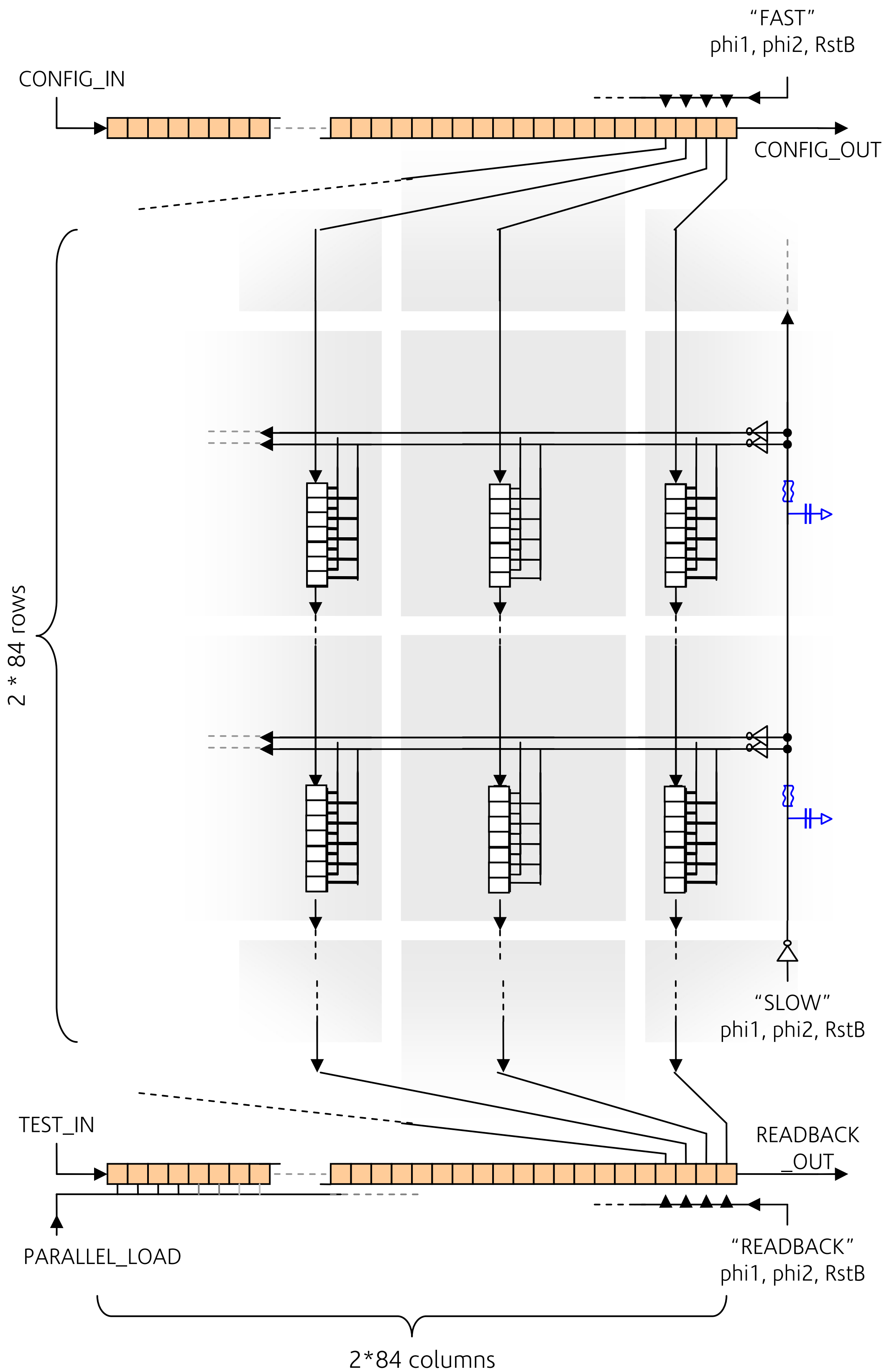
3. SENSOR OPERATION

The general cycle of operation is summarised in the diagram below. Each of these sections is considered in more detail in the pages that follow.

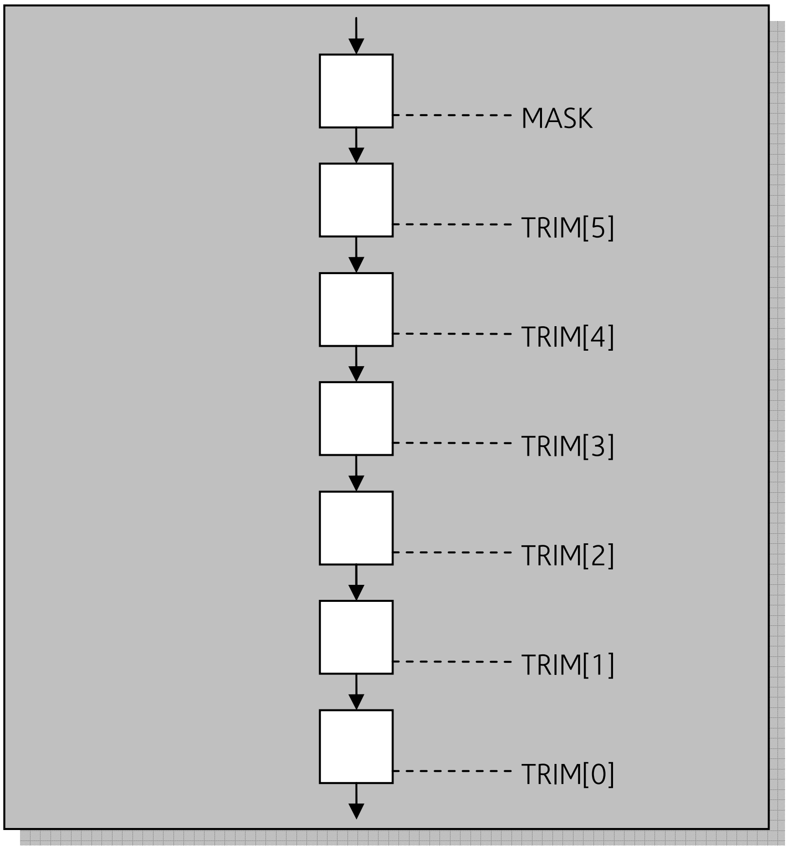


3.1 Configuration Programming

The diagram below illustrates the configuration structure, as viewed from above. Referring to the pixel identification diagram in section 1.11, the configuration for pixel at row 167, column 3 is input first; configuration for pixel at row 0, column 0 is input last.



The configuration shift register inside each pixel is arranged as follows:



	Reset Value	Action when 0	Action when 1
MASK	0	Pixel active	Pixel hits are suppressed
TRIM[#]	0	Weighted current source is inactive	Weighted current source is active. LSB switches the smallest current; MSB switches the largest (binary weighted) current.

3.1.1 TOTAL CONFIGURATION MEMORY

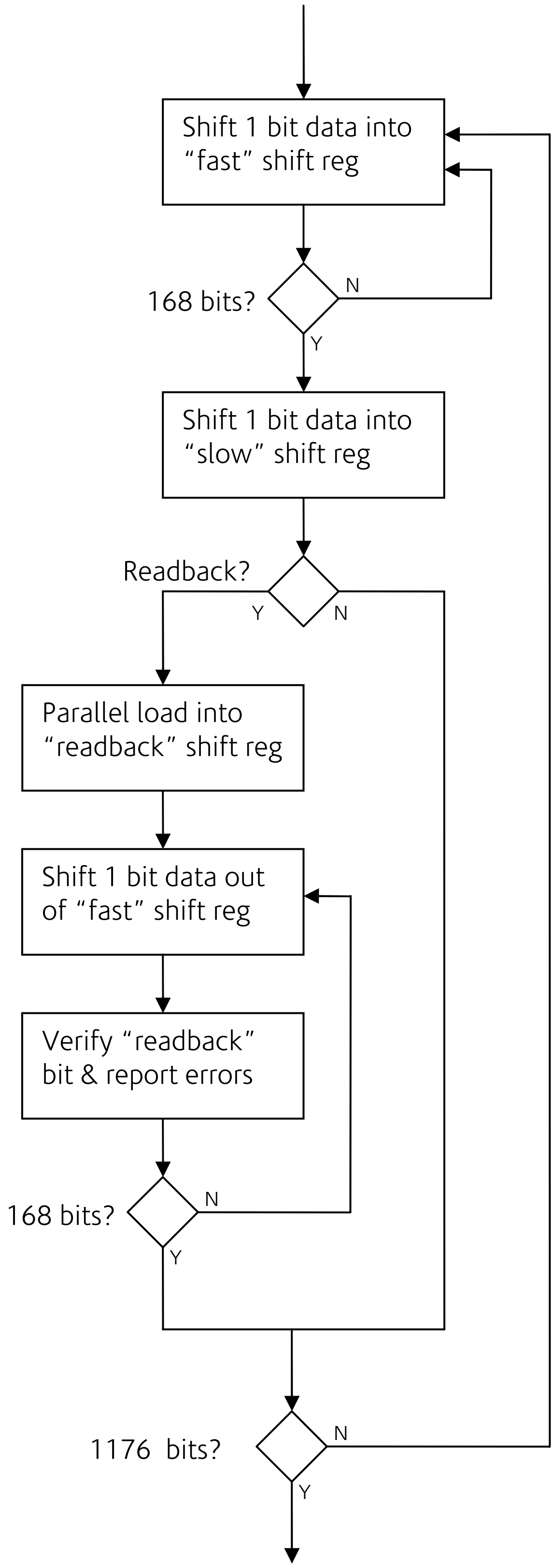
The total configuration memory space comprises 7 bits per pixel; for the full TPAC1.1 sensor this requires 197,568 bits.

3.1.2 COLD START

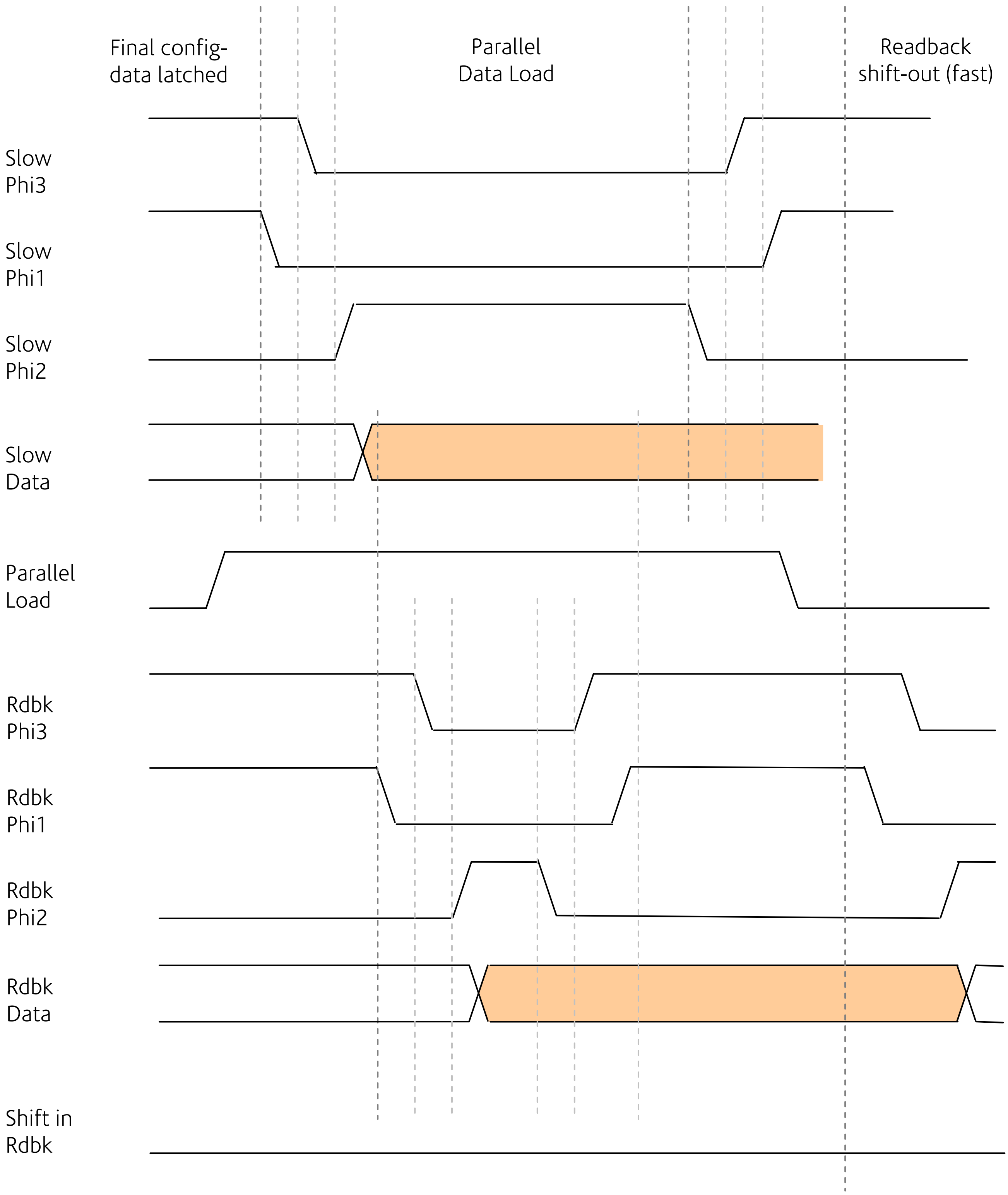
The configuration routine may be omitted, provided the "slow" configuration shift register is reset according to the diagram in section 1.12. The pixel trim and mask bits' reset value are included in the table above: the default operation is for the pixel to be active (unmasked) with no comparator trim adjustment.

3.1.3 DETAILED FLOW DIAGRAM

The configuration routine comprises alternating between" fast" programming the top serial shift register; and slow clocking the in-pixel shift registers in parallel. "Readback" from the top and/or bottom shift register is possible to verify the data that was programmed.

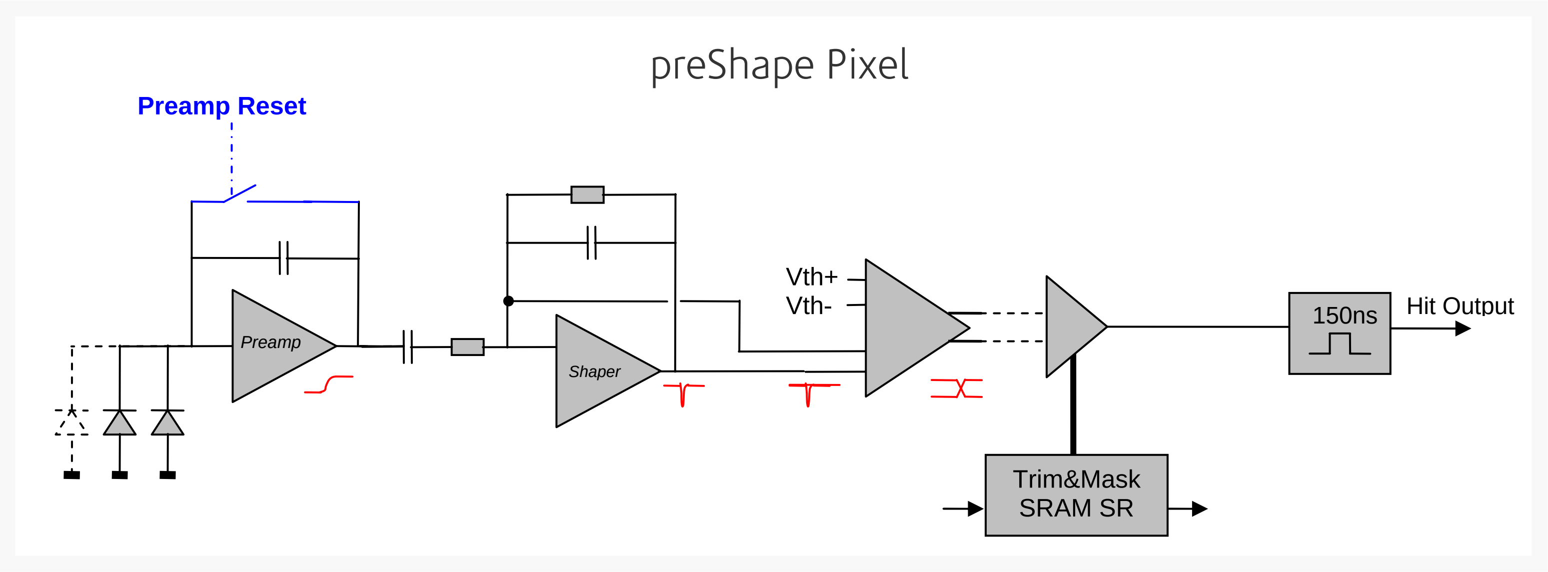


3.1.4 Detailed Parallel Load Timing

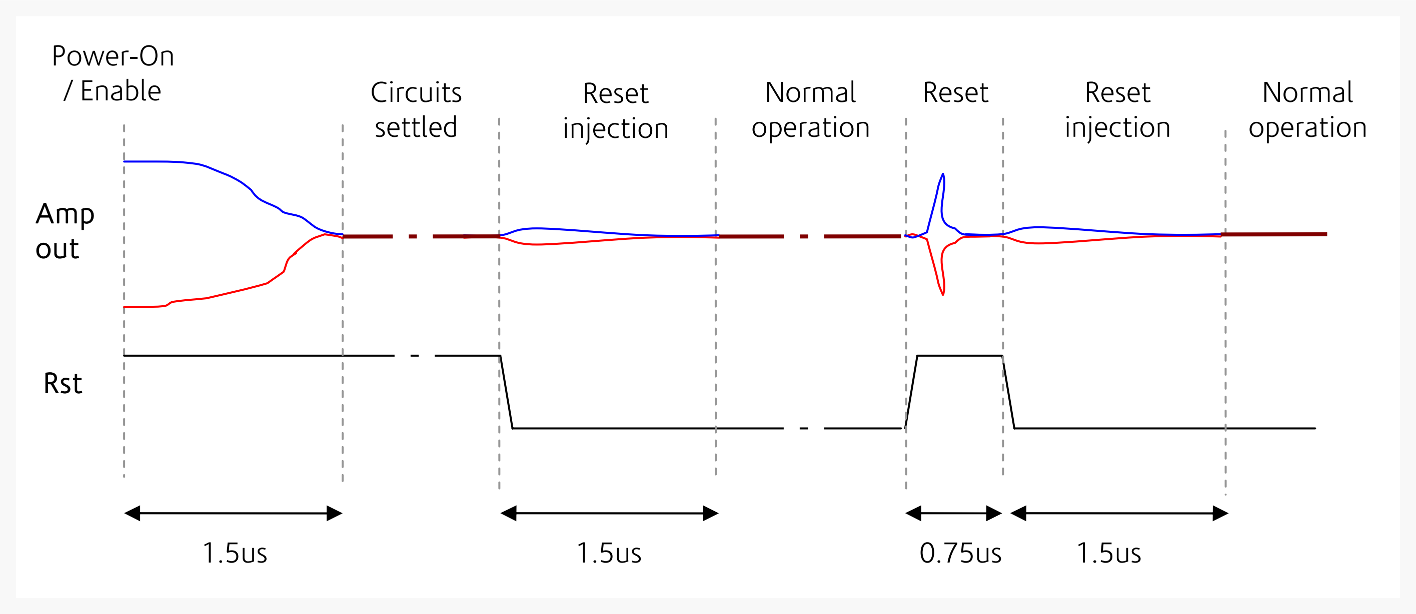


3.2 PRESHAPE PIXEL RESET

The analog front end in the preShape pixel has a single reset switch around the diode preamplifier. During bunch-train operation, the reset switch remains open: The diode node voltage drops as signal charge is collected (eventually saturating). In the typical case, the pixel is expected to be reset immediately before each bunch train commences, and then powered down during readout.

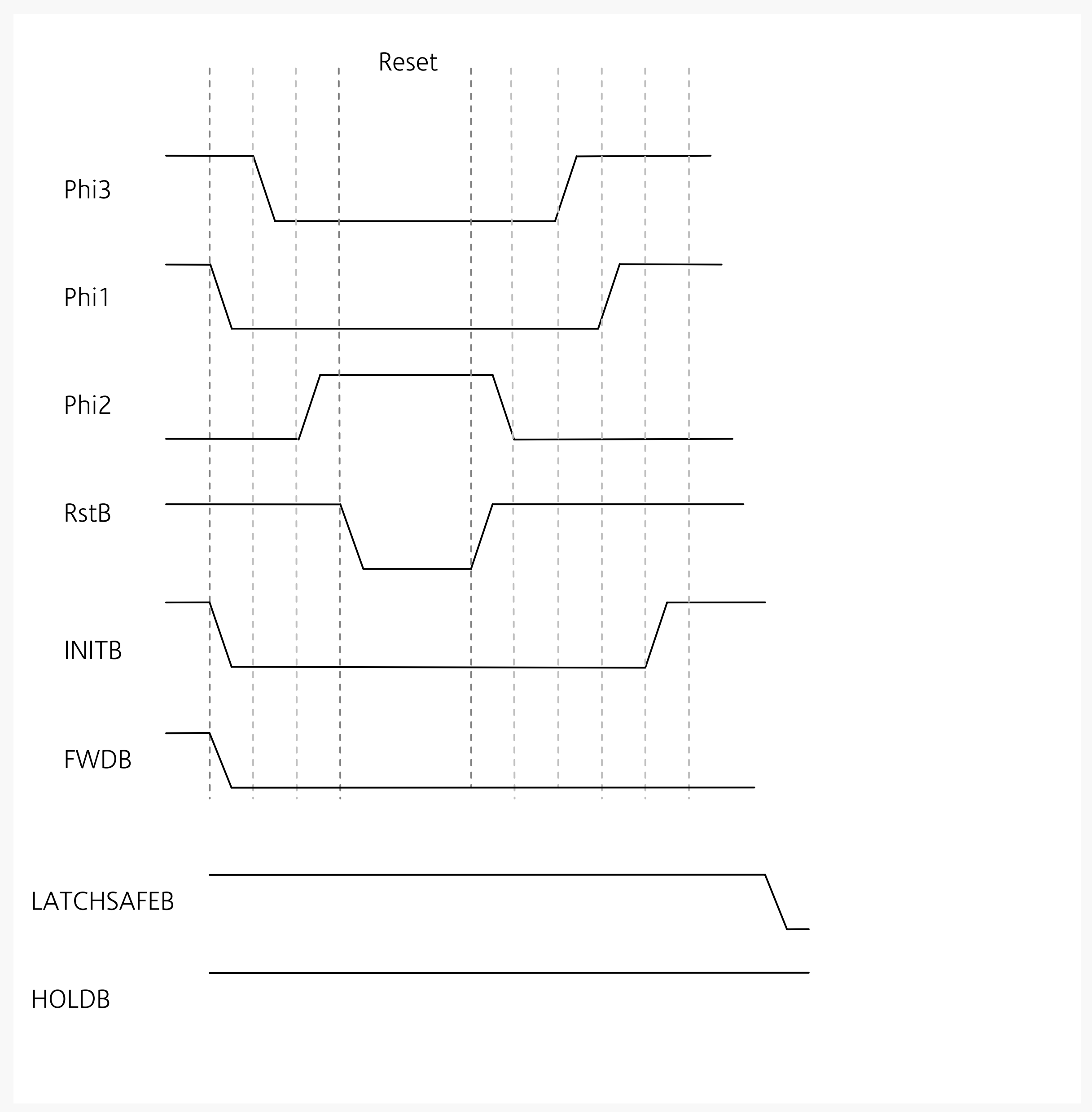


A total of 3 microseconds should be allowed from powering/enabling the preShape pixel before it is ready for normal operation. The initial power-up and reset sequence allows time for the amplifier outputs to settle in reset, and then again once the reset has been released due to charge injection. A shorter "in-service" reset pulse may be used if the pixel has not been disabled. Both reset timings are illustrated in the diagram below:



3.3 Initialise Logic for Bunch Train

The row control logic must be initialised (reset) for bunch train operation. The reset automatically sets the internal row controller to state {10000000000000000000} ready for bunch train operation.



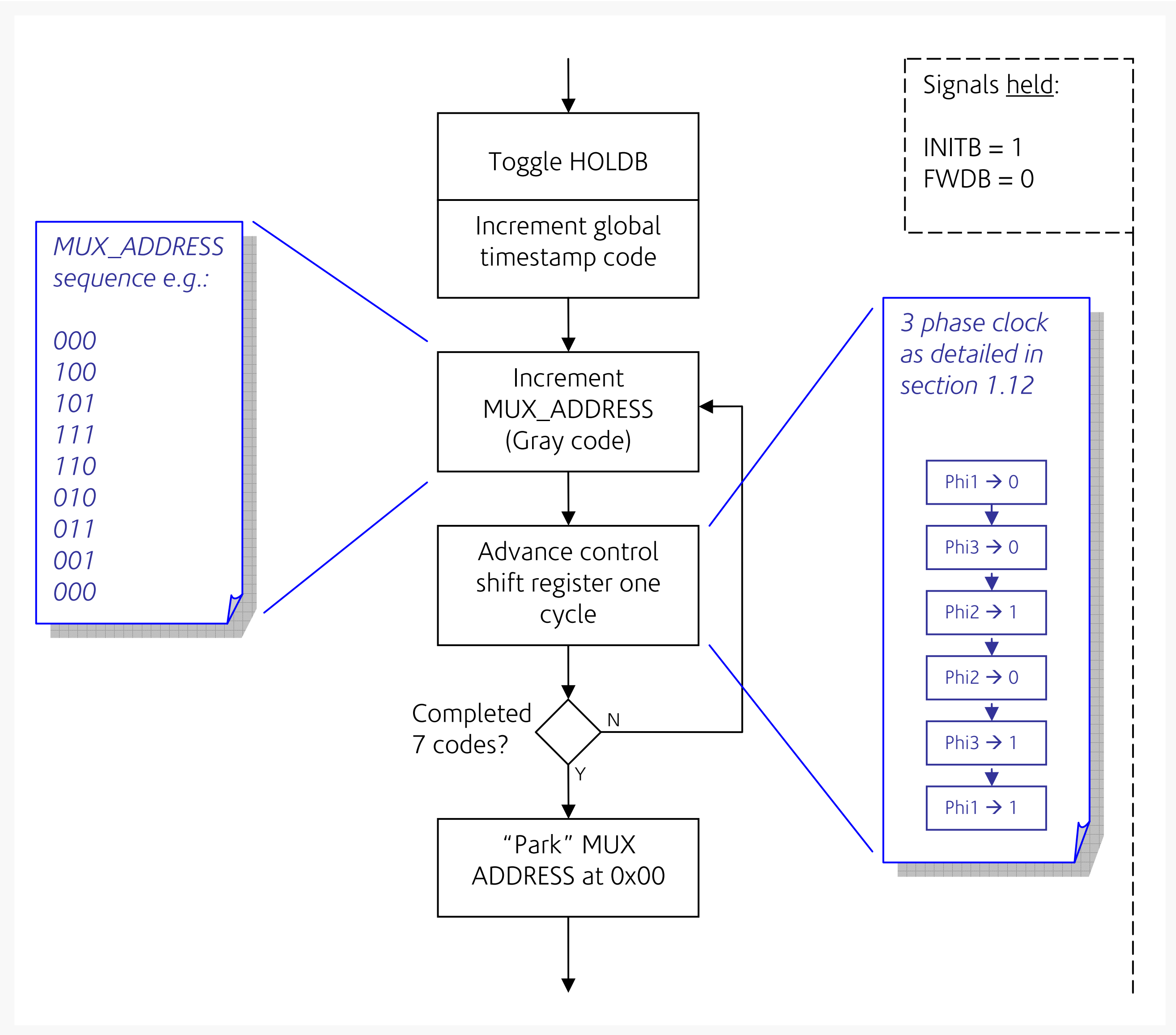
In order to properly apply the reset to the row-controller internal shift register, the INIT signal should asserted (internally this is enables the local phi2 signal to the shift register cells).

The FWD signal must be set to "forward" during reset, and should be left in the "forward" direction for the duration of the free-running bunch train operation.

The LATCHSAFEB signal should be released ready for hit capture using HOLDB

3.4 Bunch train operation (Hit Capture)

During bunch trains, the column logic operates in a "free-running" mode synchronised to the bunch crossing rate. For each bunch crossing, the sequence illustrated below is executed in the time available. Logic whose pixels have registered a hit will use these "free-running" signals to record the hit data and administer their SRAM memory banks accordingly.



The order of MUX_ADDRESS is not important, provided a GRAY code scheme is used.

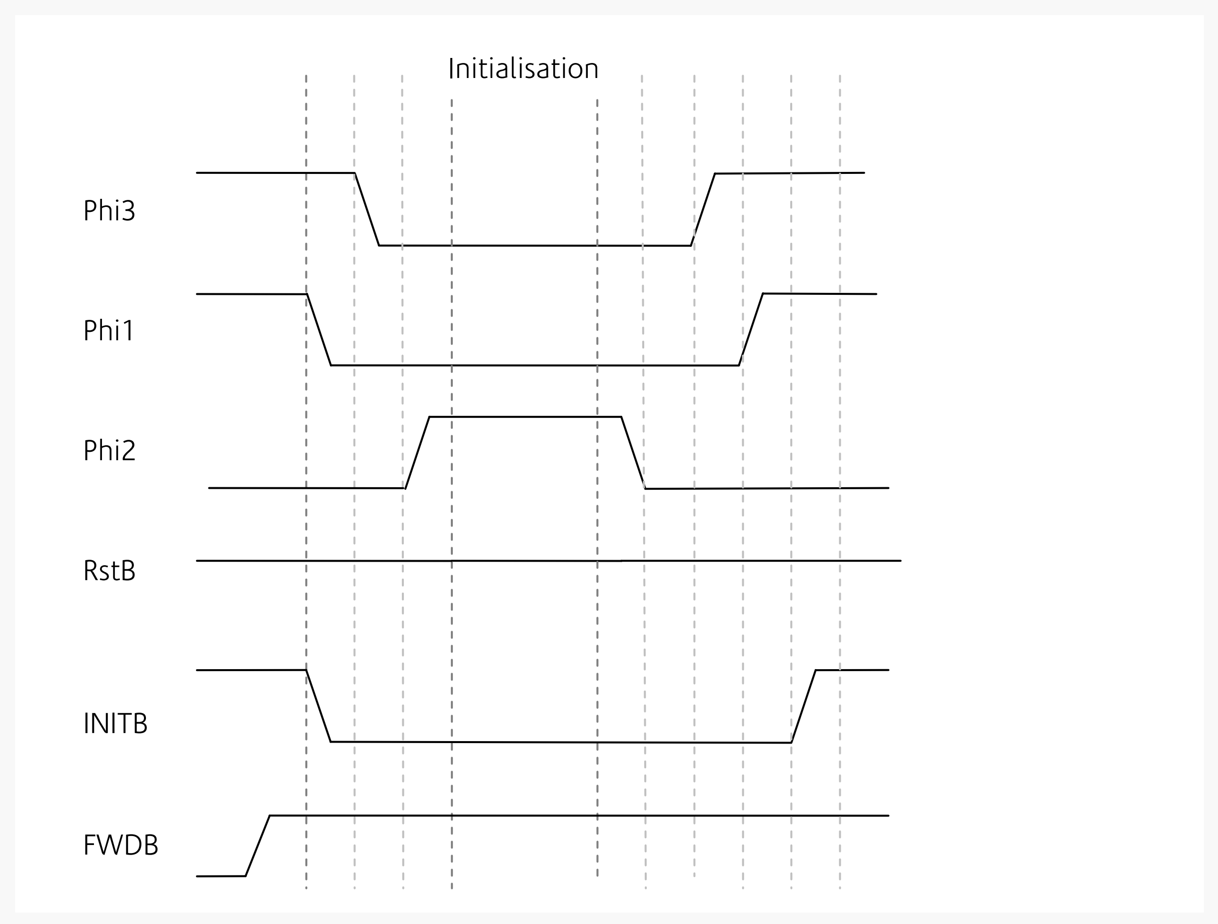
To achieve the full sequence in 150ns will require precise timing of signals at ~50Mhz. This may require some tuning in the early stages of sensor testing. (Initially, some of the gray codes may be omitted while correct logic behaviour is verified).

3.5 Initialise Logic for Readout

The row control logic must be initialised for readout following a bunch train. This is also the natural time to "park" the latch circuits in a safe state.

3.5.1 Row controller Initialisation

The row controller should be set to the "backward" direction and advanced one clock cycle with "INIT" asserted.



The FWDB signal should be left in the "backward" direction for the duration of the readout.

3.5.2 Latch safe mode

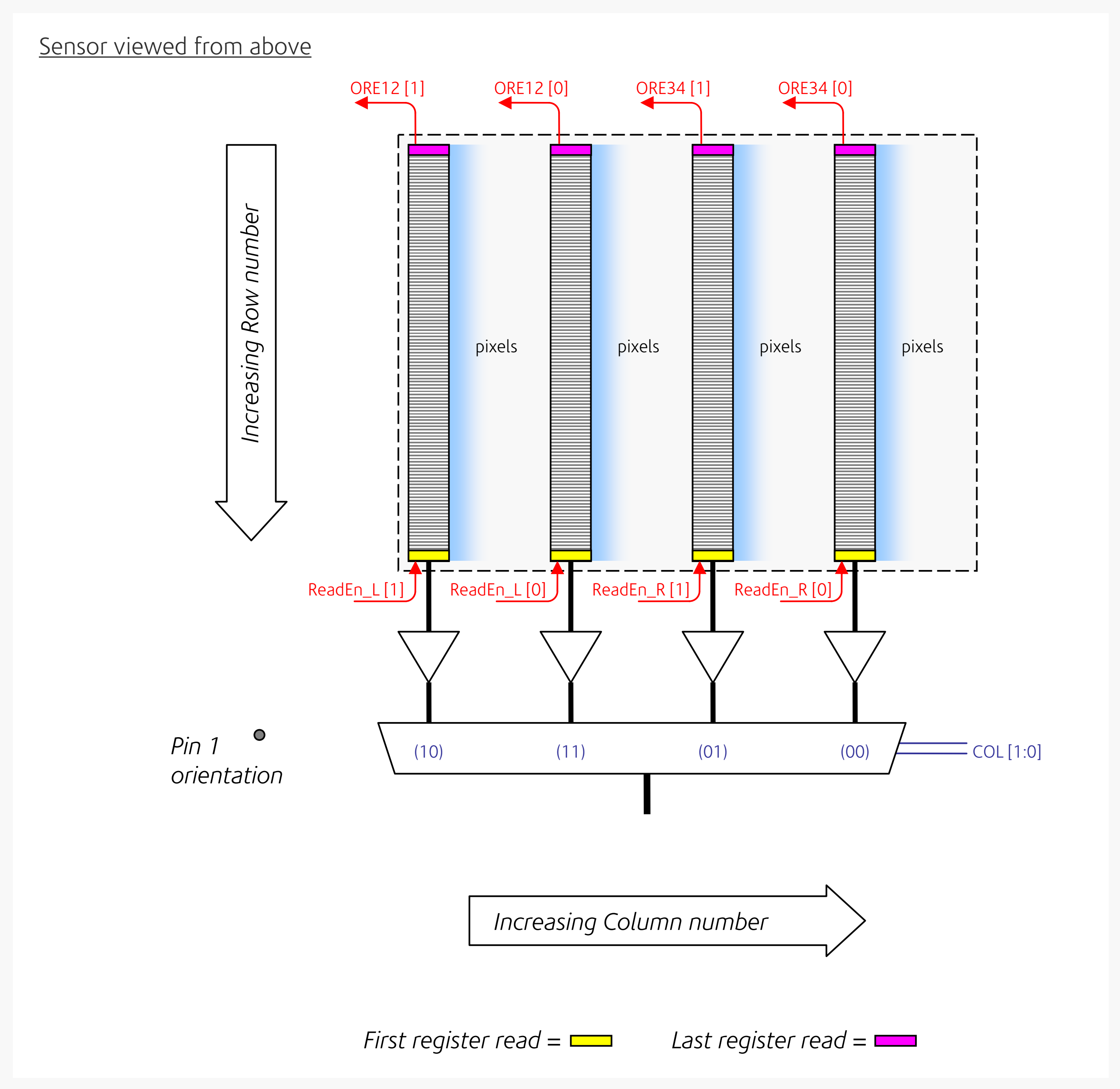
The latch circuit uses dynamic storage nodes, which when not clocked will leak over long periods (milliseconds). To avoid high currents while these nodes deteriorate, a latch safe-mode circuit was implemented.

The HOLDB and LATCHSAFE signals should be set according to the table below.

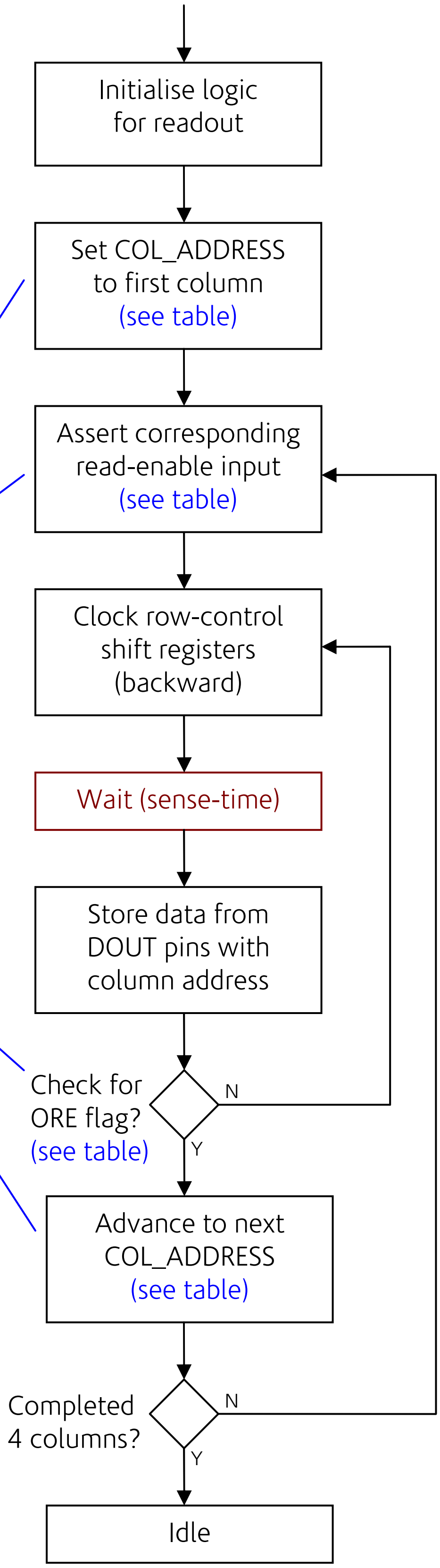
	HOLDB	LATCHSAFE
Inactive: Safe State	0	1

3.6 Data Readout

The sensor readout operates independently in the four columns, but the data output is multiplexed such that one column may output data at a time.



The recommended readout scheme addresses a single column at a time. The read enable signal is asserted (and held) for the active column and the row controllers are clocked in "backward" direction. The read enable signal propagates (by combinational logic) to the first valid register: that register is immediately enabled for read access, and after a short sensing delay is available at the sensor pins via the multiplexer. On each subsequent clock cycle, the read-enable signal propagates up the column to the next valid register until it emerges at the corresponding ORE (onward-read-enable) output. When the ORE output is flag is seen, column readout is complete, and the next column may be read in the same way.



Column order	Address code	Read Enable	Onward Read-Enable
First	10	ReadEn_L [1]	ORE12 [1]
Second	11	ReadEn_L [0]	ORE12 [0]
Third	01	ReadEn_R [1]	ORE34 [1]
Last	00	ReadEn_R [0]	ORE34 [0]

Typical Data Sense Delays

Delay	Min	Max
Data Sense	110ns	150ns
Multiplex	25ns	25ns
Total	135ns	175ns

Safe readout rate 5Mhz.

4. SENSOR TESTING

A variety of test features and procedures are summarised in this section: This is not an exhaustive list of the tests that may be required during initial verification process.

4.1 HIT OVERRIDE

An external control signal "OVERRRIDEB" allows false hits to be generated at the input to the row control logic. This allows for verification of the logic independent of pixel activity.

Pin: OVERRIDEB	Circuit behaviour
0	Standard row-logic operation, only hit signals from pixels will be stored in local SRAMs.
1	Override mode: Pixel hits are ignored, and stored regardless of state.

In override mode, every bank of pixels (for each of the 7 MUX addresses) will be seen to have a hit and will therefore be stored as a pattern of hits. The hit pattern that is stored is the actual state of the pixel hit signals (which may be useful for diagnostic/initial testing).

Note that the memory banks will fill up very quickly in override mode: For one bunch-train crossing cycle, 7 banks of pixels are interrogated, and will therefore fill 7 of the available 19 SRAM memory banks. Therefore in the third cycle the memory will overflow.

This feature is particularly useful to verify many parts of the logic, including the full readout chain, the propagation of read-enable signal along the full length of the column, proving the row address space is unique and complete, checking the overflow and ORE outputs function correctly.

If in normal operation the sensor memory fills up unexpectedly quickly or is populated with hit patterns of zeros then the polarity/setting of this override pin should be checked!

4.2 DEBUG OUTPUTS

Some key control signals are available to probe as outputs from the TPAC1.1 sensor. These signals have been distributed and re-buffered on-chip along one particular column. They may be of interest to compare the relative timing of critical signals as seen inside the logic. These signals are not necessary for normal operation of the sensor, and therefore are likely to be available at PCB test-points only.

Pin Name	Description
DEBUG12_MA0	Row control Mux Address Bit 0
DEBUG34_RST	Row control reset signal
DEBUG34_P3B	Row control phi3 clock
DEBUG34_P2B	Row control phi2 clock
DEBUG34_P1B	Row control phi1 clock

4.3 Overflow Flag

The sensor is designed with a simple flag to indicate when the column SRAM memory banks are full. The overflow flag is a wired-or of the local overflow signal in each row, and is separated for each pixel variant.

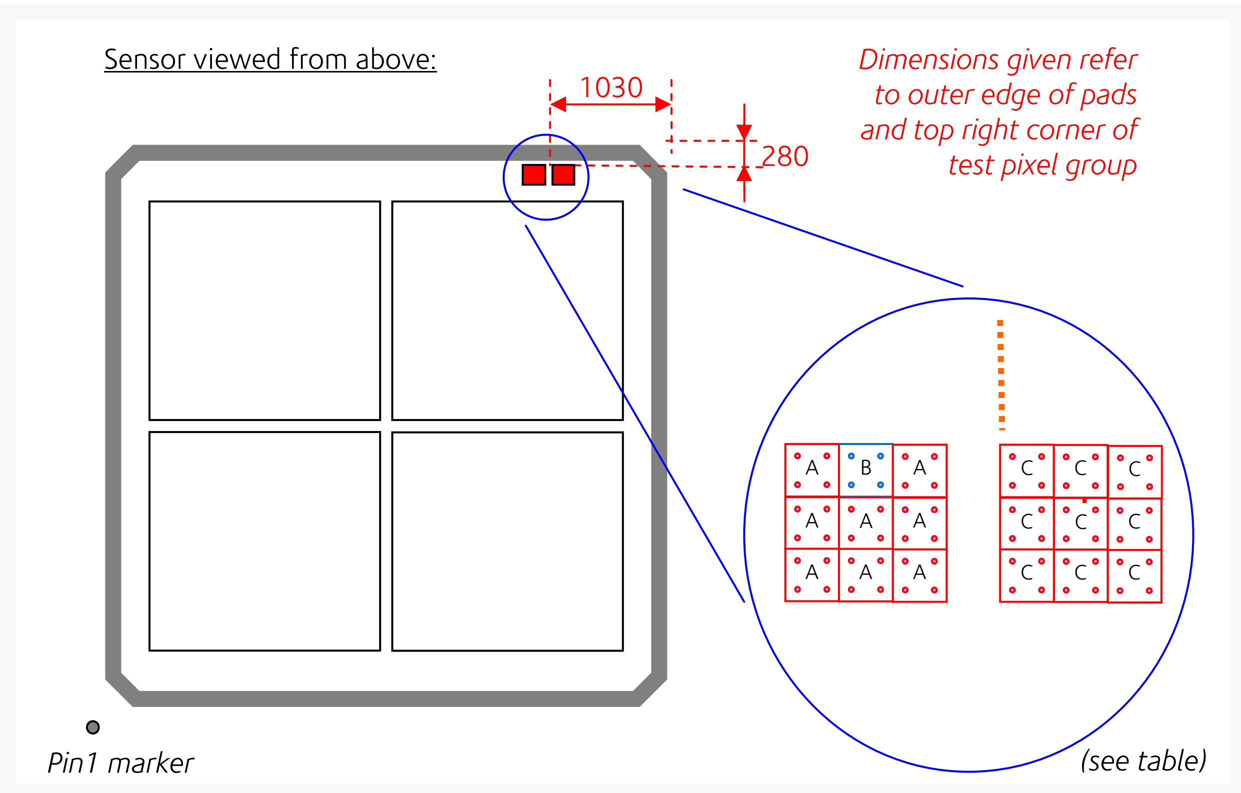
Overflow Signal	Pixel Architecture	Pixel Variant
OF1	preShape	② (TBTBBTTB)
OF2		② (TBTBBTTB)
OF3	preShape	② (TBTBBTTB)
OF4		② (TBTBBTTB)

The overflow flag will rise on the first occurrence of a row-controller filling its memory: Other rows will continue to operate normally, but no further indication of the total memory used is available. The rows that reach this full memory status will correctly store and read back the first 19 hits that occurred; any subsequent hit data is discarded.

Specific overflow location information is not available, but may be deduced by switching to readout immediately after the flag goes high, and searching for the row address that appears the maximum (19) times.

4.4 Pixel Test Structures

Pixels of the preSample architecture, and both variant were added in the periphery of the chip with (buffered) access to internal analog nodes. The PCB includes a notch to allow rear illumination by laser during initial testing: location and orientation information is given below:



4.4.1 Quick reference table

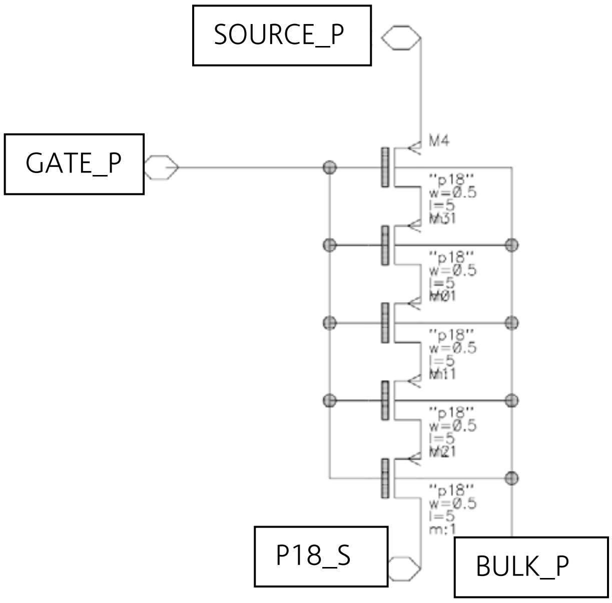
Test pixel	Schematic Cell Name *	Pixel Variant	Related Inputs	Related Outputs
A		preShape ② (revised TPAC1.1)	DEBUG_VTH+ DEBUG_VTH- DEBUG_RST200B DEBUG_TRIM[5:0] debugsfbias	DEBUG_SIGVAL1 DEBUG_RSTVAL1 DEBUG_COMPN_OUT DEBUG_COMPN_OUTB DEBUG_HITOUT1
B		preShape ② (revised TPAC1.1)	DEBUG_HITIN	DEBUG_HIT200
C		preShape ② (original TPAC1)	DEBUG_RST200B DEBUG_TRIM[5:0] debugsfbias	DEBUG_SIGVAL2 DEBUG_RSTVAL2 DEBUG_HITOUT2

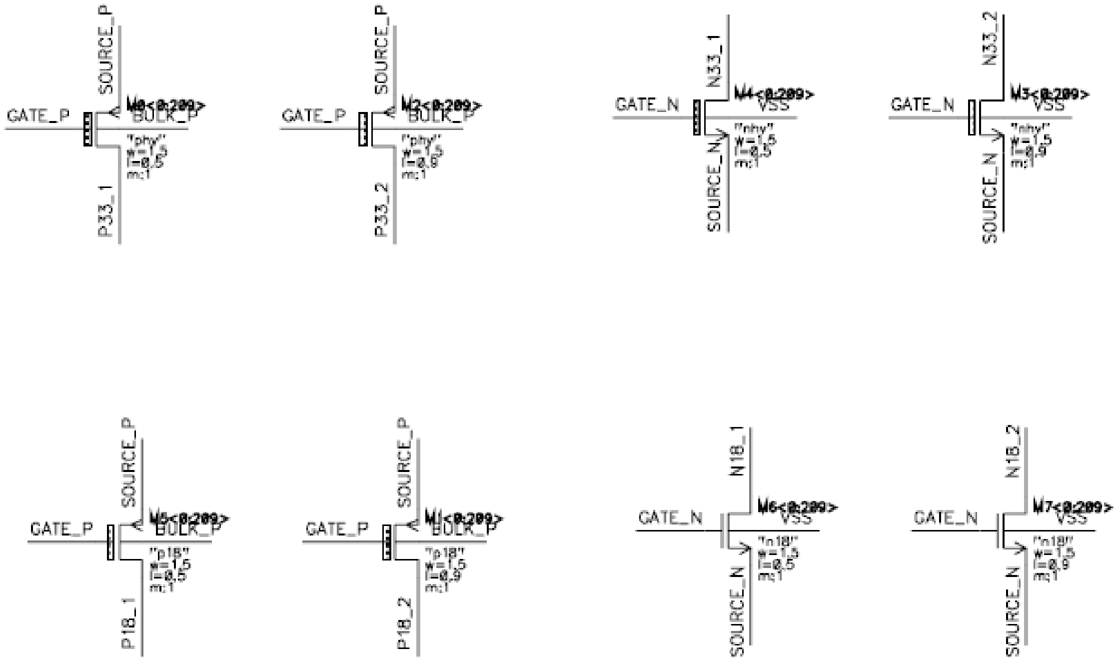
4.5 Test Devices

Spare pad sites around the periphery were used for test devices; these are detailed in this section.

4.5.1 Transistors

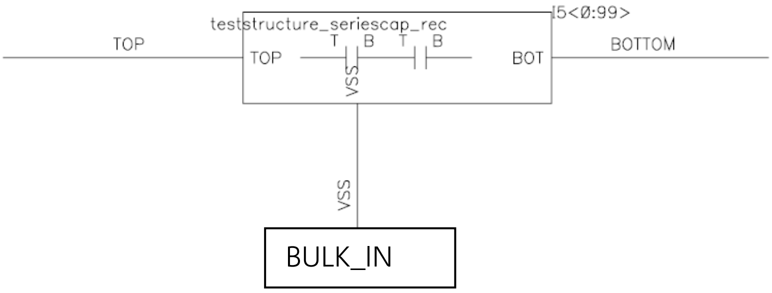
210 P18_S_IN
211 P33_2_IN
212 P33_1_IN
213 SOURCE_P_IN
214 GATE_P_IN
215 BULK_P_IN
216 P18_2_IN
217 P18_1_IN
218 N33_2_IN
219 N33_1_IN
220 SOURCE_N_IN
221 GATE_N_IN
222 BULK_N_IN
223 N18_2_IN
224 N18_1_IN





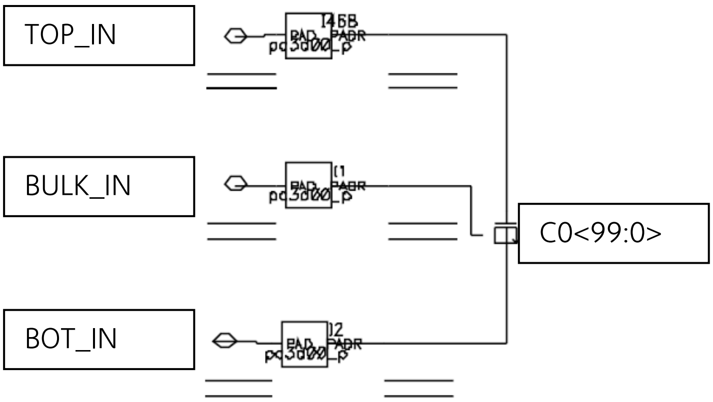
4.5.2 Series Capacitor

248 TOP_IN_SERIESCAP
249 BULK_IN_SERIESCAP
250 BOTTOM_IN_SERIESCAP



4.5.3 Parallel Capacitor

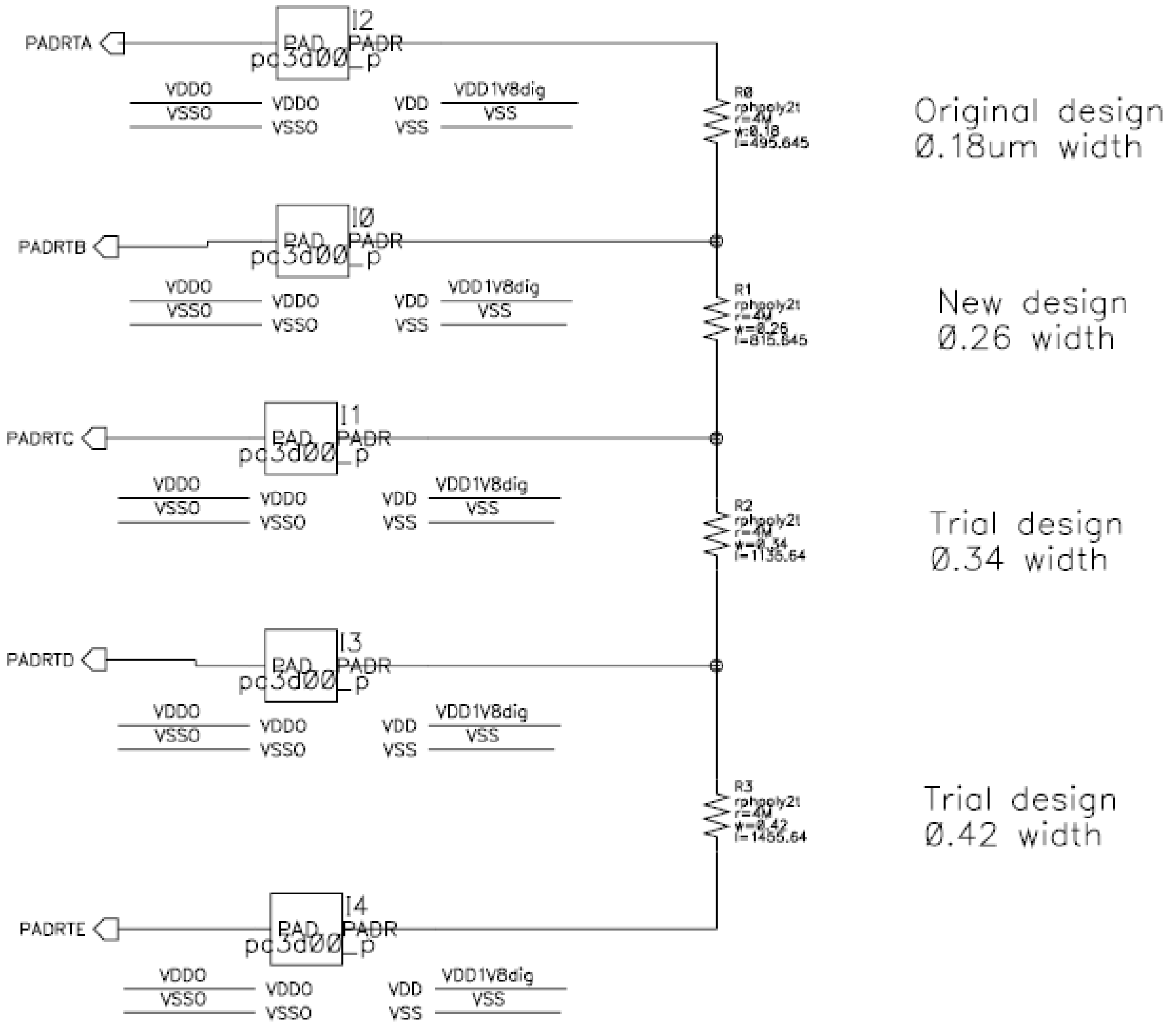
104 TOP_IN_CAP
105 BULK_IN_CAP
106 BOTTOM_IN_CAP



4.5.4 Resistors

121 PADRTA
122 PADRTB
123 PADRTC
124 PADRTD
125 PADRTE

Four resistors, all nominal 4Mohm, for direct measure of resistance.



4.5.5 Diodes

98 DIODE_TOP_IN
101 DIODE_BOTTOM_IN

100 parallel diodes with individual guard rings (substrate contacts)

4.5.6 Nwell Separation

128 VGUARD
129 V1_IN
130 V2_IN
131 V3_IN
132 V4_IN
133 V5_IN

Five Nwells at different spacings as detailed below: