MAPS award and issues

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MAPS award

- Modified proposal spread over four years: FY05/06 to FY08/09
  - Delayed by ~9 months compared to original proposal
- Effort
  - RAL/ID; RT 1SM/year (for all 4 years), JC 3SM, 12SM, 12SM, 9SM
  - RAL/PPD; MT 1SM/year (for all 4 years), GV 5SM/year (for all 4 years), new RA 12SM for last 2 years
- Money
  - Equipment and consumables; £2k, £4k, £105k, £156k
  - Travel; £1k, £5k, £7k, £17k
- Obvious constraints
  - Cannot start design full-time until Jan 2006 (although…)
  - Cannot be sure we can pay for first fabrication until Apr 2007 and second fabrication until Apr 2008 (although…)
- Implies a real delay of ~12 months

Original schedule

		FY	5/6			FY	6/7			FY	7/8			FY	8/9	
	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Feasibility study	=															
Design 1		=	=	=	=											
Fabrication 1					=	=										
Basic tests 1						=	=									
Detailed tests 1							=	=	=	=						
Design 2							=	=	=							
Fabrication 2									=	=						
Basic tests 2										=	=					
Detailed tests 2										=	=	=				
Beam test PCB								=	=	=	=					
Beam test												=				

Possible schedule given constraints?

		FY	5/6			FY	6/7			FY	7/8			FY	8/9	
	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Feasibility study	=	=	=													
Design 1 (+6M)				=	=	=	=	=								
Fabrication 1 (+12M)									=	=						
Basic tests 1										=	=					
Detailed tests 1											=	=	=	=		
Design 2											=	=	=			
Fabrication 2													=	=		
Basic tests 2														=	=	
Detailed tests 2														=	=	=
Beam test PCB												=	=	=	=	
Beam test																=

ILC parameters

- Exact beam timing parameters not yet defined
  - Assume close to previous (“TESLA”) design
  - Beams collide rapidly within a quick burst (“train”)
  - Long dead time between trains
- Assume timing as follows
  - Beam collision rate within train = 5MHz, i.e. 200ns between collisions
  - Number of collisions within train = 5000, i.e. train is 1ms long
  - Train rate = 5Hz, i.e. 199ms between trains; 0.5% duty cycle
- Rate of signals
  - ILC is not like LHC; rate of physics processes is small
  - Most collisions give nothing, but when reaction does happen, many adjacent channels will be hit
  - Expected rate not very well known; needs detailed simulation modeling
  - Assume average ~10^{-6} hits/pixel/crossing, which is ~0.005 hits/pixel/train

MAPS concept for ILC

- Divide wafer into small pixels
  - Each has comparator and memory
- Discriminate pixel signal for every collision within a train
  - Gives binary value for each collision
- Record collision numbers (timestamps) each time above threshold
  - Timestamps can have values up to 5000, i.e. 13 bits
  - Store result in memory during train up to some maximum number of timestamps
- Read out all timestamps in dead time before next train
  - Ensure total readout completed before next train
- Alternative: sum number of hits over $\sim 1 \times 1 \mathrm{cm}^2$ "pad"
  - Report out number of hits per pad per collision
  - Degraded information but lower data volume

MAPS technology

- How big should the pixels be? How thick should the epi be?
  - Physical particle density sets maximum around $50\times50\mu m^2$ area but smaller would be better with respect to saturation from multiple hits/pixel
  - Want to minimise charge sharing between neighbours (crosstalk) but maintain high efficiency within pixel
  - Want to maximise signal in epitaxial layer; 15μm feasible?
- How low can the noise hit rate be made?
  - Would like to be comparable with physics rate $\sim10^{-6}$ hits/pixel/crossing
  - Implies S/N of at least 10
- Single Event Upset (SEU)
  - What are the failures due to SEU? What is the rate of SEU?
- How much memory can fit into a pixel?
  - Area required for each bit? $2\times2\mu m^2$ area?
  - Up to 16 timestamps/pixel should be easily sufficient; ~30 bytes

Power issues

- Power and cooling are critical issues
  - Detector would be very compact and inaccessible
- Should be comparable to alternative technologies
  - I.e. standard silicon diode wafer and preamplifier chip
  - Chip dominates ~1W/wafer (i.e. for MAPS ~ 10^7 pixels ~ $16 \times 16 cm^2$)
  - Averages to 5mW/wafer if only powered on during train
- MAPS power dominated by comparator (?)
  - Single comparator ~ 2μW, gives 20W/wafer
  - Averages to 0.1W/wafer if only powered on during train
  - To reduce further, need to only power on comparator when needed
- Issues are
  - Comparator stability and reproducibility
  - Comparator settling time

Thin profile and dead area issues

- MAPS detector also needs to be
  - Thin profile (to be compact)
  - Few dead areas (to be efficient)
- Need wafers to be closely packed with no protrusions
  - Implies no wire bonds from edges; they give dead space between wafers as well as thickening detector
  - Can all contacts be placed on top, i.e. like BGA components?
- No back contacts on wafer
  - Can wafer operate with substrate not grounded?
- What will be the fractional dead area?

Other questions

- Require bad pixel masking to reduce data volume
  - Load mask as configuration data before data taking
  - What rate of bad pixels is likely?
- How is wafer comparator threshold set?
  - DAC(s) on wafer?
  - Adjustable at what granularity in terms of pixels?
  - How uniform will the pixels be?
- What I/O rate can wafer output?
  - Needs to drive signals over ~1.5m PCB to controller FPGA
- Need high-tech PCB developments also
  - Large PCB (~1.5m) or "flat" join of smaller PCBs
  - PCB "other side" components embedded flush (or do without)

Physics simulation work is also needed

- Need quantitative answers to many questions
  - First thing is to write a realistic physics simulation of a MAPS including the thin sensitive layer
- What is the rate from beam interactions in the pixels?
  - If too high, then the data volume would be prohibitive
- What pixel size is really needed?
  - Is $50\times50\ \mu m^2$ sufficient?
  - Would we see saturation effects from multiple tracks per pixel?
- What is the requirement on noise in the pixels?
  - How often can we tolerate a fake hit in a pixel?
  - Signal/noise of >10 could give 10^{-6} probability of fake hit, if Gaussian
  - Is one fake in every 10^6 samples good enough for physics?
  - This impacts both resolution on the shower energy and pattern recognition; which is the more critical?

Simulation work (cont)

- What is a tolerable inefficiency per pixel?
  - The surface readout electronics may absorb some charge
  - May be a localised inefficiency; is this acceptable?
  - Does it affect resolution or pattern recognition more?
- What rate of crosstalk is acceptable?
  - Diffusion means tracks near pixel edges will share charge with neighbour
  - Better to have low threshold and hence two hits, or high threshold and hence zero hits?
  - What rate of sharing is tolerable?
- What improvement is achieved with a 1mm gap reduction?
  - Drive to thin detector
  - Is this significant for shower separation?

Previously discussed pogramme

- 3.5 year programme to validate (or dismiss!) concept
  - Produce some prototype MAPS and test whether they work, in terms of signal size, noise rate, stability of threshold/pedestal, etc.
  - Put in a beam test for further checks, including single event upsets
  - Plan for two iterations of wafer manufacturing
- First iteration will have several different designs
  - Two? Nine?? All share a ~1×1 cm^2 (or smaller) area
  - Test various choices for comparator, readout, reset, etc.
- Second iteration will be a single design
  - Use modification of the best design from first iteration
  - Make 2×2 cm^2 area devices; standard commercial size
  - Would get standard run of six wafers, each holding ~50 sensors
  - Even allowing for bad yield, would be able to make several layers of e.g. 10×10 cm^2 area for a beam test

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Beam test															=	=