



CCLRC
Rutherford Appleton Laboratory

Intelligent Digital Sensors

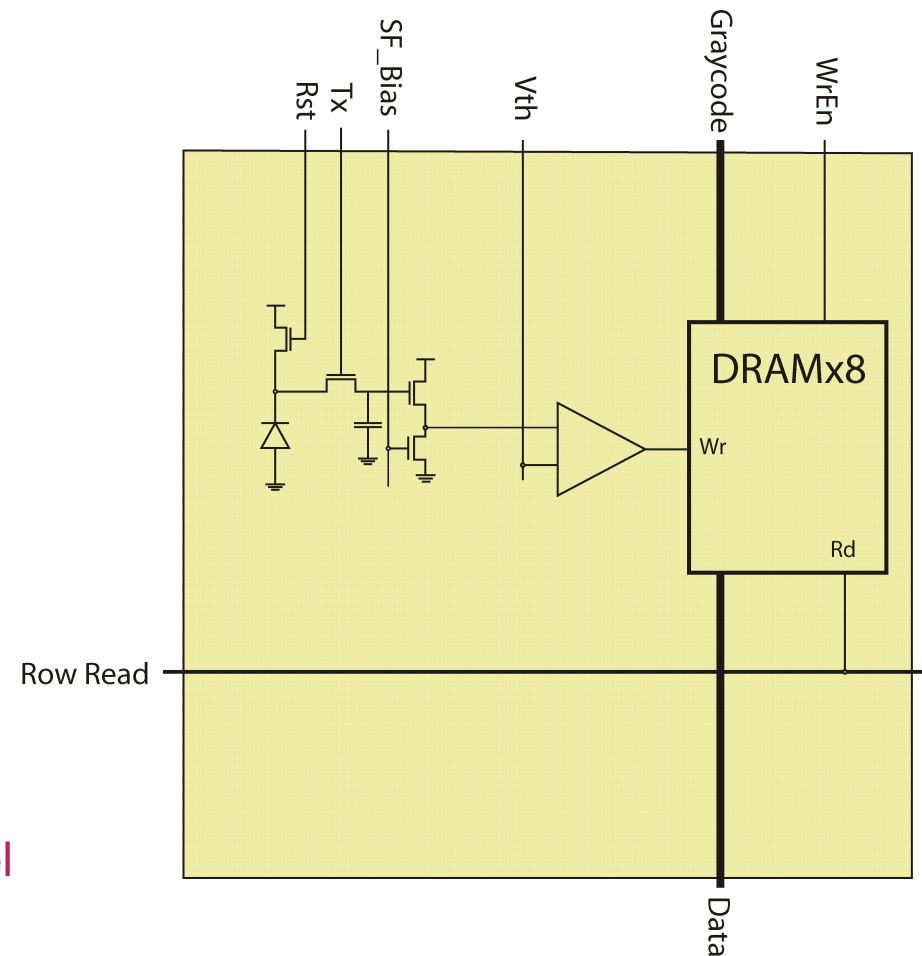
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Active Pixel Sensors: Challenges

- High speed region of interest
 - [1st talk this session]
- High dynamic range, adaptive imaging
 - [2nd talk this session]
- In-pixel “intelligence”
 - Sparse readout
 - ADC and storage in each pixel
 - Threshold + functionality
- High frame rates

The digital pixel

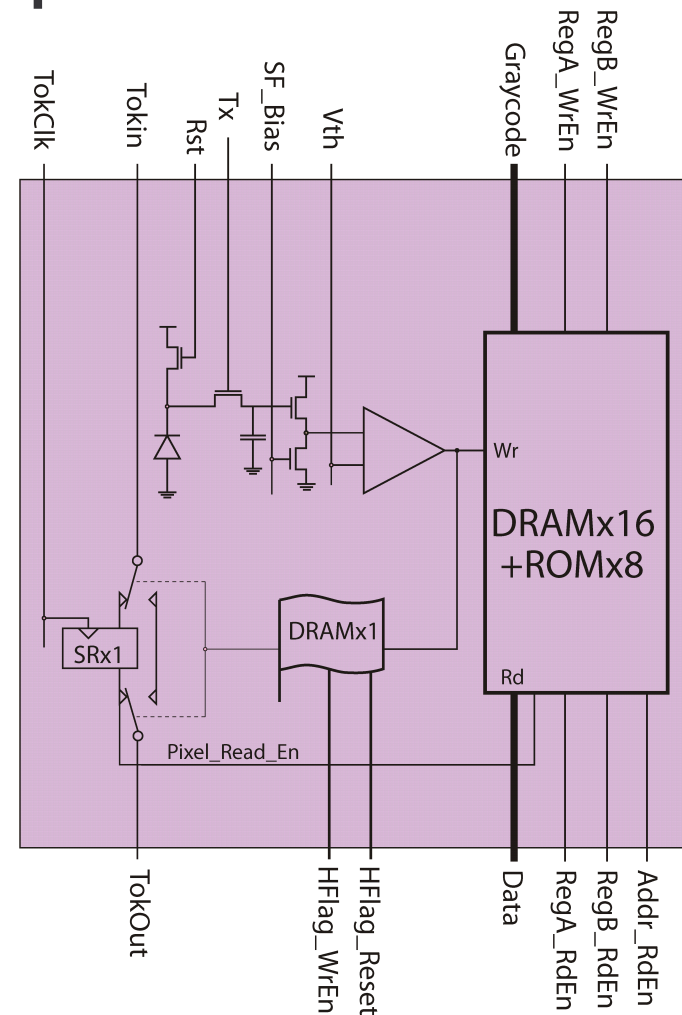
- Conventional APS pixel
- Sampling node
- Comparator (ADC)
- Digital memory
- Digital readout architecture
- A 10000 Frames/s CMOS Digital Pixel Sensor. Kleinfelder et al, Stanford University. IEEE JSSC Dec 2001.



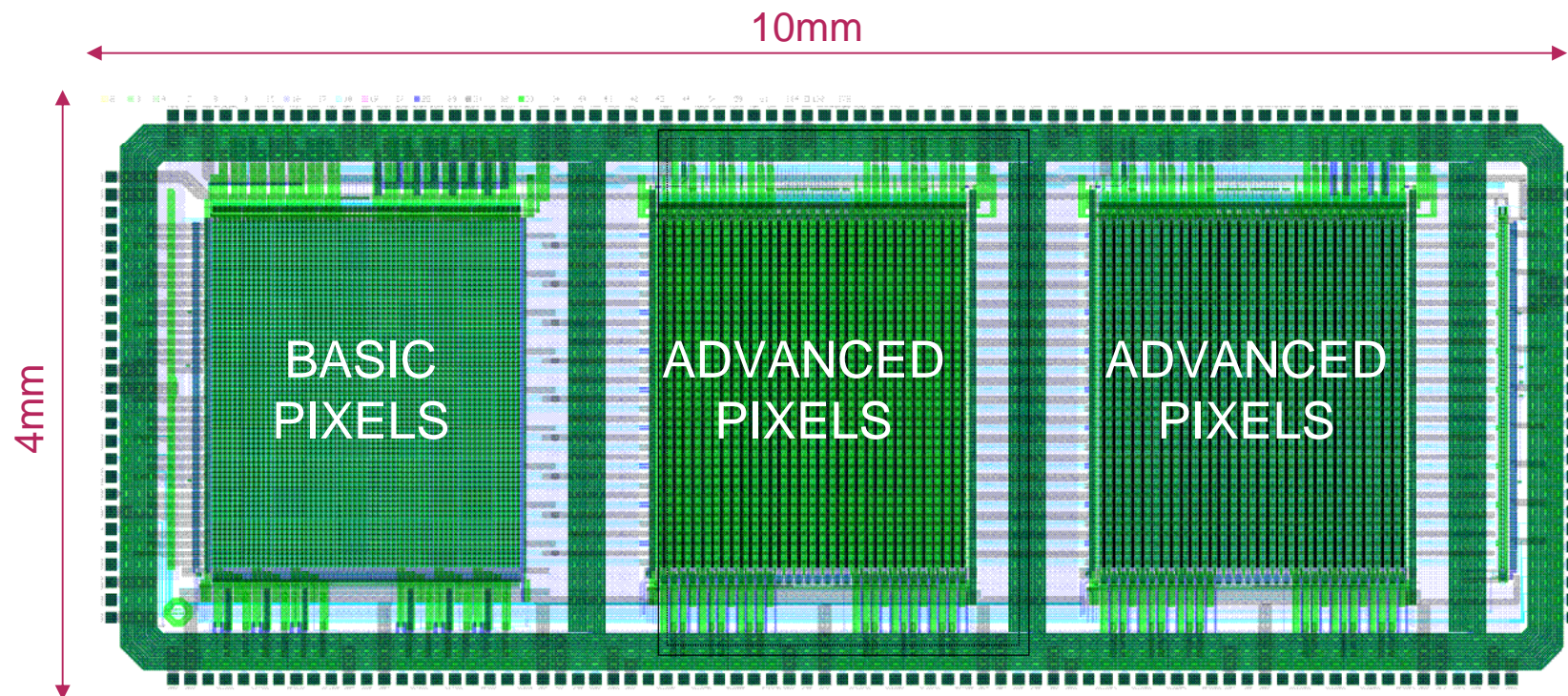
Advanced digital pixel capabilities

- Threshold sensing
 - "Hit" status / timing
- Self-select readout
(sparsification at pixel level)
- Multiple registers
- Address ROM
- Image pre-processing

...intelligence...

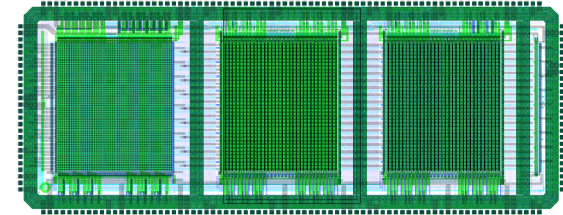


On-Pixel-Intelligent-CMOS (OPIC)



- Feasibility study: CFI grant (Centre-For-Instrumentation)
- RAL test structure for M13 collaboration

On-Pixel-Intelligent-CMOS (OPIC)



- 30um pixels (64x64 arrays)
- Full frame imaging (up to 10k frame/s)
- Sparse (threshold defined) frame imaging
- In-pixel 8-bit ADC + Threshold timing
- Extended dynamic range coding
- Optical imaging (~10% fill factor)
- Charged particle imaging applications
- Due back: July 2005!

Conclusion

- **Example applications**
 - Pulsed laser imaging
 - Collider detector physics
- **Constraints**
 - 800Mb/sec max. output data rate
 - Data acquisition, processing, and storage challenges!
- **Acknowledgements**
 - MI3(Basic Technology), CFI, Stanford(CA)