CALICE Meeting at RAL

10/10/05

Jamie Crooks
RAL

CCLRC
Rutherford Appleton Laboratory

Activities since last meeting

- OPIC testing
  - Promising results
- Ideas session with Renato
  - Produced a few questions!

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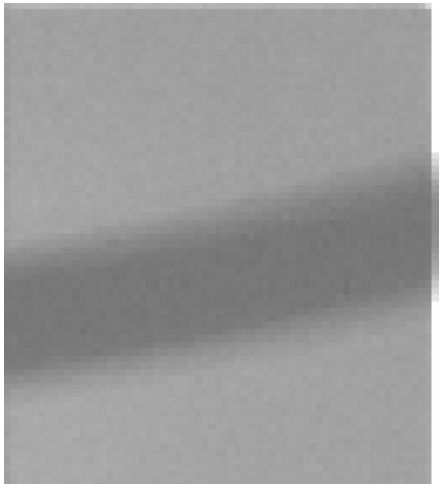
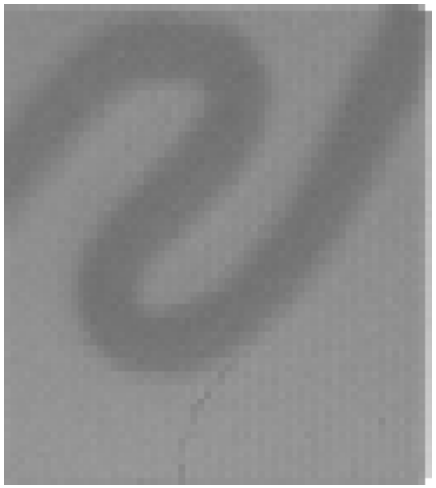
OPIC testing progress



Basic Pixel



Advanced Pixel (DFF)

- First images (in-pixel ADC)
- Working circuits (@16Mhz) :
  - DRAM
    - Sense amplifiers
    - 40ns readout seen on DRAM test blocks
  - Pixels
    - Comparator
    - Sparse readout token scheme

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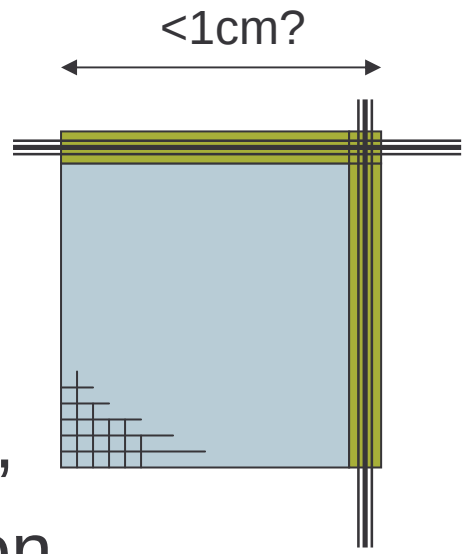
Outcomes from ideas session

- Probably favour a continuous reset scheme
- Possible pixel structure?
  - 4 diodes per pixel?
  - Single comparator/logic
- Possible ‘tile’ structure
  - Two sides used for control/readout,
  - buffering, signal & power distribution
-



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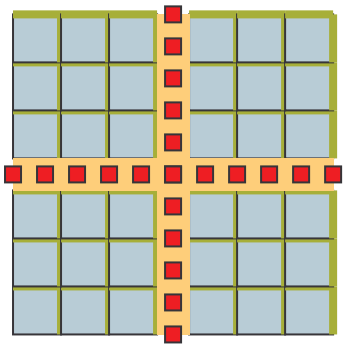
..cont

- Possible stitched chip structure
  - Flip/solder pads over power and control signal distribution across chip centre (dead area)



- Xfab offers 4 metals on 0.35 process – LOTS of hierarchical routing, 13 bit busses, power. Will be interesting! (Lots of metal everywhere!)

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MapsRequirements doc: Comments

- Dead space/inefficiency 10% requirement feels tight!
- Comparator timing? – please clarify
- Memory requirements
  - Why 16 bits?
  - Why need to hold data for seconds? (will add complexity into pixel)
- Power target of 1uW/mm2 sounds very tight!

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Questions

- How big (physically) is a jet/splash?
  - Will indicate volume of localised data the chip must cope with.
- What is the desired active area on the PCB?
- Who decides # and spec of FPGAs?
  - Anticipated data rates per FPGA?
- Is 150ns timing resolution really needed?