Power issues

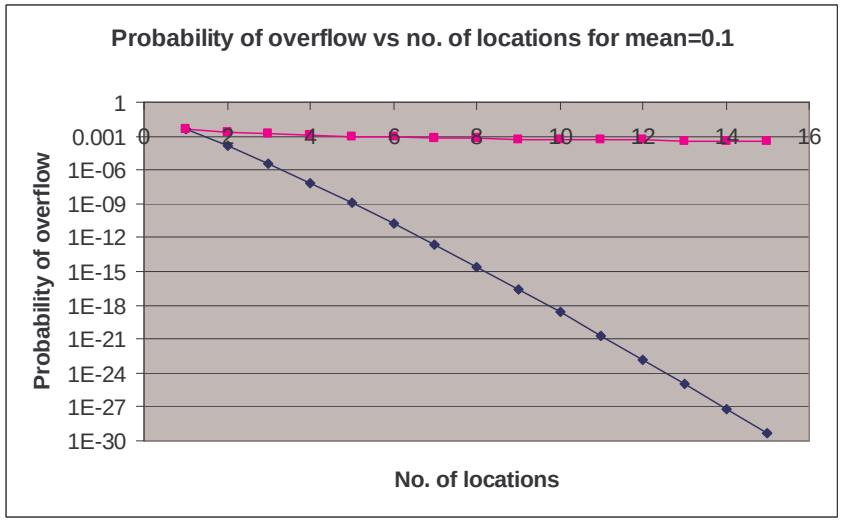
- Target power level stated in requirement was $1\mu W/mm^2$
  - This is averaged over whole period of operation with ILC bunch timing
- It needs to be competitive with analogue preamplifier ASIC
  - I asked Christophe de la Taille (the ASIC designer) about this during the CALICE meeting at DESY last month
  - Quoted target for ASIC is 10mW/channel at continuous power
  - Each channel corresponds to a $1\times1cm^2$ silicon diode pad
  - Power cycling during train gives factor of 100 reduction on average
  - Total is then $100\mu W/channel = 100\mu W/cm^2 = 1\mu W/mm^2$ ⌞
- MAPS comparator is roughly 1μA from 2.5V = 2.5μW (?)
  - For $50\times50\mu m^2$ pixels, this is 400 pixels/mm^2
  - Equivalent to $1mW/mm^2$ at continuous power; factor 1000 needed
  - 10^4 crossings per train and a train every 100ms is 10^{-5} sec/crossing average
  - For factor 1000 reduction, need comparator on for only 10^{-8} sec = 10ns
  - Smaller pixels (or more comparators per pixel) reduces this time accordingly

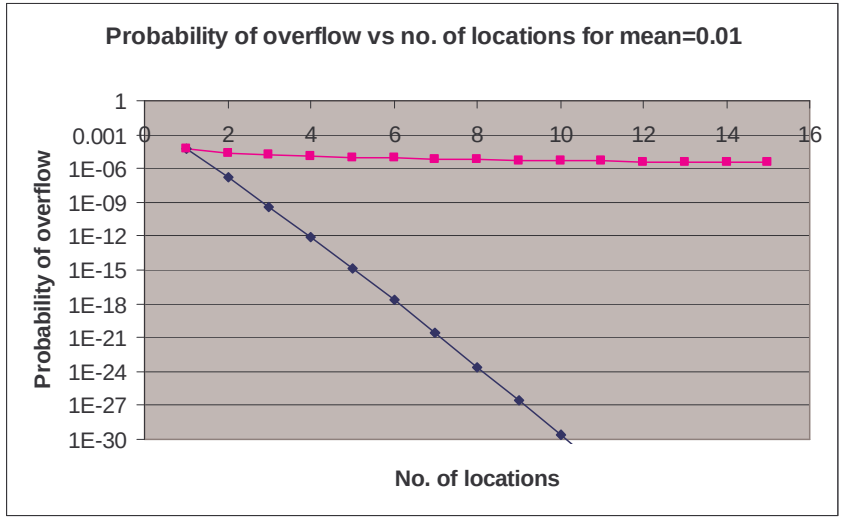
Buffer overflows

- Original concept
  - A number of memory locations per pixel, e.g.16 locations
  - Each pixel has separate counter for number of locations filled
  - Each time a hit above threshold is seen during train, timestamp recorded and pixel counter incremented; needs counter logic for every pixel
  - Buffer overflows if more than e.g. 16 hits in one train
  - Probability of N hits has Poisson distribution
- Jamie's suggestion
  - Have memory locations per pixel but no counter
  - Subdivide train into, e.g. 16 subtrains with one location per subtrain
  - Timestamp of any hit during train written into location for that subtrain
  - Single counter increments subtrain number globally; need counter logic only once
  - Overflow occurs if more than one hit in any subtrain
  - Number of subtrain overflows has binomial distribution

Buffer overflows (cont)

- Depends on mean number of hits per train
  - Within ~10^4 bunch crossings per train and a noise rate of 10^{-5}, then mean number per train is 0.1
  - For target noise rate of 10^{-6}, then mean number per train is 0.01
- Blue below is original, pink is new scheme

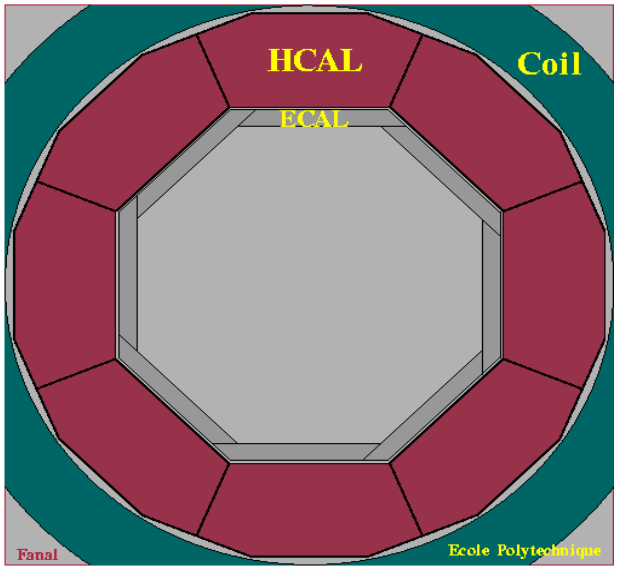


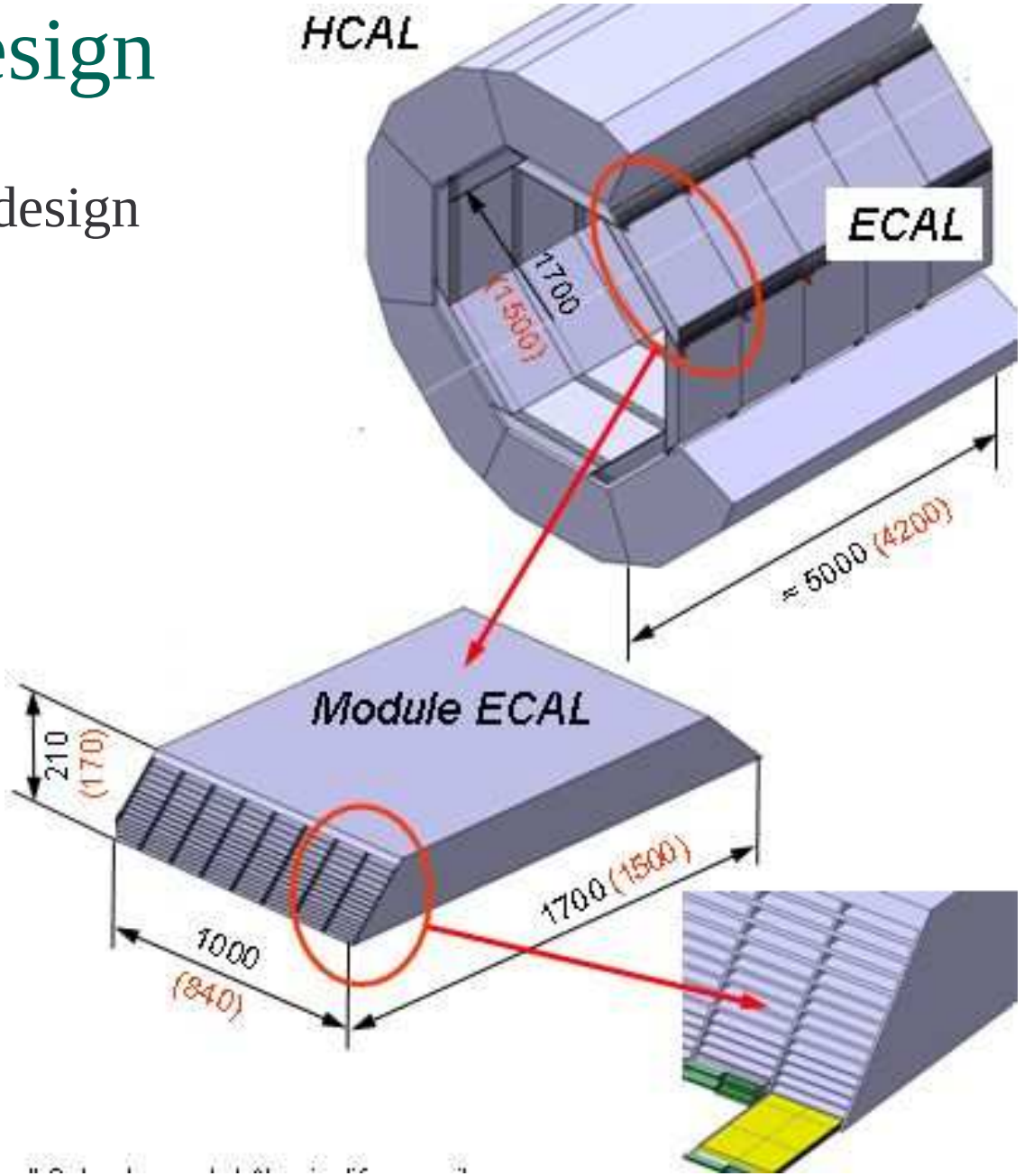


- New scheme only falls slowly with number of locations
  - Probability of overflow ~ mean*mean/2*$N_{locations}$

“Long” PCB design

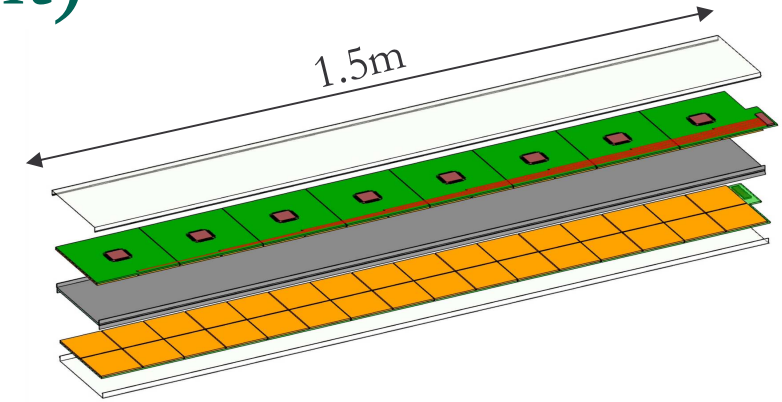
- Baseline (and MAPS) design needs ~1.5m PCBs
- Roughly 30cm wide
- As thin as possible

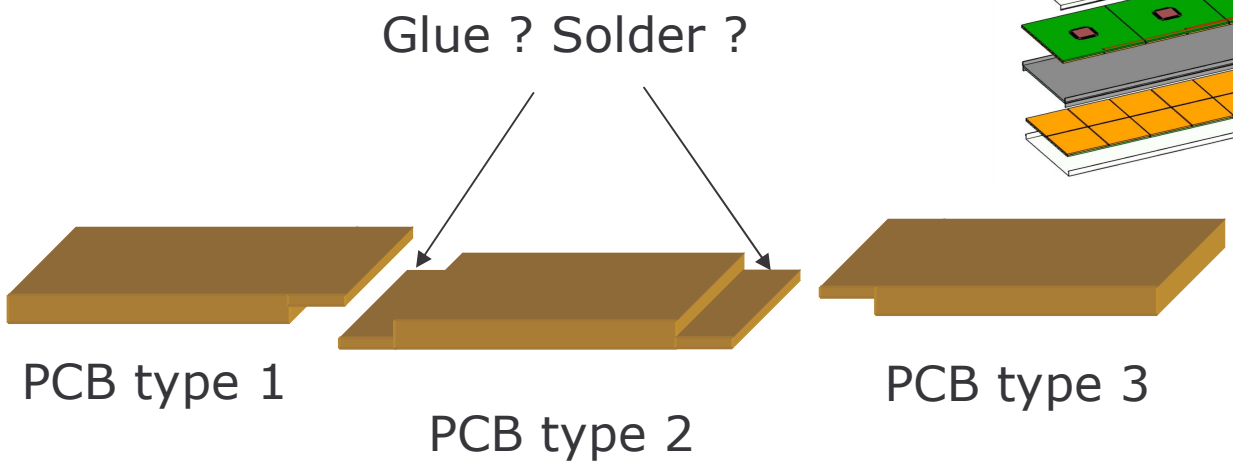




“Long” PCB design (cont)

- Length of ~1.5m problematic
  - PCB stitching possible?





- Thin PCB by embedding components?
  - Puts even more incentive on wirebond-less MAPS connections